

RMWP38001

37-40 GHz Power Amplifier MMIC

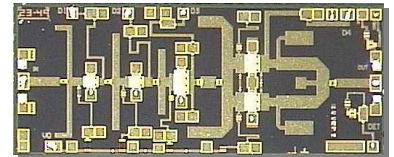
PRODUCT INFORMATION

Description

The RMWP38001 is a 4-stage GaAs MMIC amplifier designed as a 37 to 40 GHz Power Amplifier for use in point to point radios, point to multi-point communications, LMDS, and other millimeter wave applications. In conjunction with other Raytheon amplifiers, multipliers and mixers it forms part of a complete 38 GHz transmit/receive chipset. The RMWP38001 utilizes Raytheon's 0.25 μ m power PHEMT process and is sufficiently versatile to serve in a variety of power amplifier applications.

Features

- ◆ 4 mil substrate
- ◆ Small-signal gain 22 dB (typ.)
- ◆ 1dB compressed Pout 22 dBm (typ.)
- ◆ Chip size 3.4 mm x 1.4 mm

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Positive DC voltage (+4V Typical)	Vd	+6	Volts
Simultaneous (Vd - Vg)	Vdg	8	Volts
Positive DC Current	I _D	483	mA
RF Input Power (from 50 Ω source)	P _{IN}	+8	dBm
Operating Baseplate Temperature	T _C	-30 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C
Thermal Resistance (Channel to Backside)	R _{jc}	46	°C/W

Electrical Characteristics

(At 25°C),
50 Ω system,
Vd=+4 V,
Quiescent Current
Idq=250 mA

Parameter	Min	Typ	Max	Unit
Frequency Range	37		40	GHz
Gate Supply Voltage ¹ (Vg)		-0.5		V
Gain Small Signal at Pin=-10 dBm	18	22		dB
Gain Variation vs Frequency		4		dB
Gain at 1 dB Compression		21		dB
Power Output at 1 dB Compression		22		dBm
Power Output Saturated: Pin=+5 dBm	21	23.5		dBm
Drain Current at Pin=-10 dBm		250		mA
Drain Current at 1dB Compression		280		mA

Parameter	Min	Typ	Max	Unit
Drain Current at Saturated: Pin=+5 dBm		270		mA
Power Added Efficiency (PAE): at P1dB		15		%
Input Return Loss (Pin=-10 dBm)		12		dB
Output Return Loss (Pin=-10 dBm)		7		dB
OIP3		30		dBm
Noise Figure		6		dB
Detector Voltage (Pout= +15 dBm) (Bias Current = 0.02-0.05 mA)		0.15		V

Note:

1. Typical range of gate voltage is -2.0 to 0 V to set Idq of 250 mA.

Characteristic performance data and specifications are subject to change without notice.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

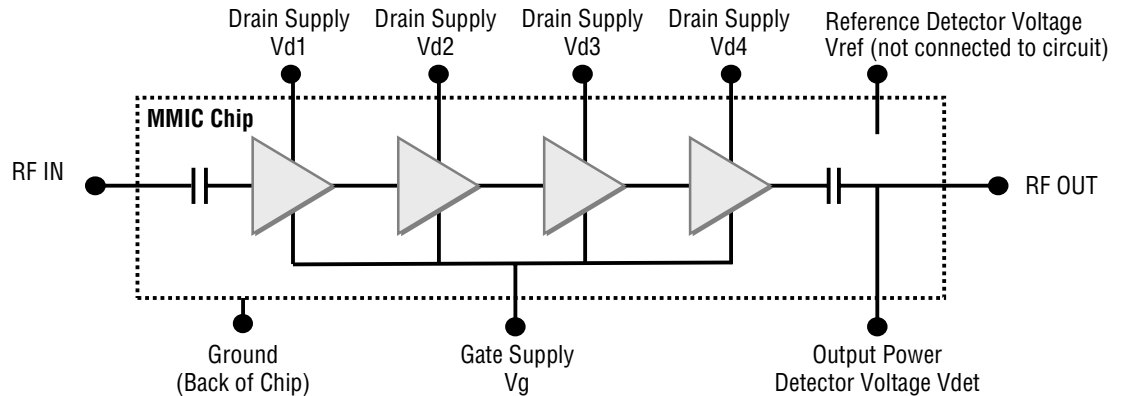
Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typically 2 mil between the chip and the substrate material.

Figure 1
Functional Block Diagram



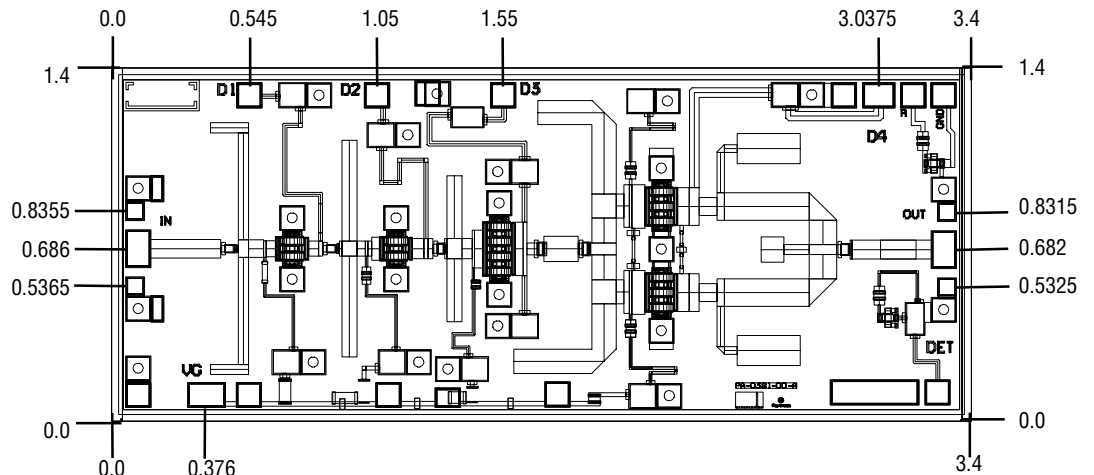
Note:

For output power level detection, bias both detector and reference diodes. DC voltage difference between detector and reference can be used to measure output power after calibration. If output power level detection is not desired, do not make connection to detector bond pad.

Figure 2
Chip Layout and Bond Pad Locations

Chip Size is 3.4 mm x 1.4 mm. Back of chip is RF and DC ground

Dimensions in mm



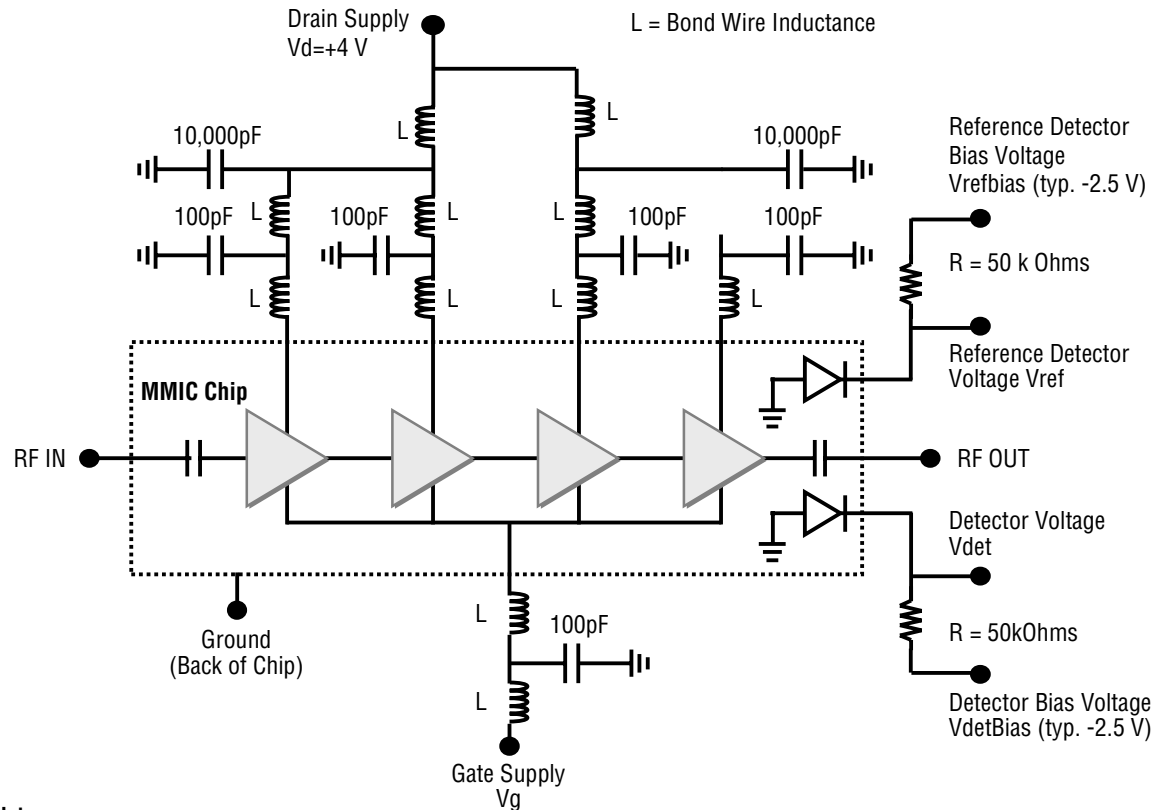
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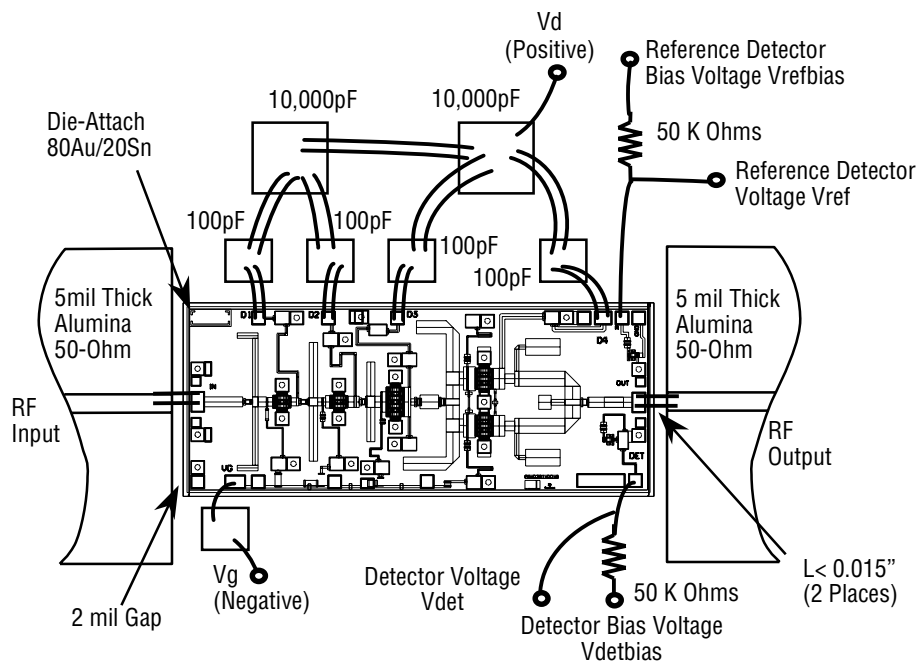
Figure 3
Recommended
Application Schematic
Circuit Diagram



Note:

For output power level detection, bias both detector and reference diodes. DC voltage difference between detector and reference can be used to measure output power after calibration. If output power level detection is not desired, do not make connection to detector bond pad.

Figure 4
Recommended
Assembly Diagram



Notes:

1. Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.
2. If output power level detection is not desired, do not make connection to detector bond pad.

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Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the grounds of the chip carrier.

Slowly apply negative gate bias supply voltage of -1.5 V to V_g .

Step 3: Slowly apply positive drain bias supply voltage of +4 V to V_d .

Step 4: Adjust gate bias voltage to set the quiescent current of $I_{dq}=250$ mA.

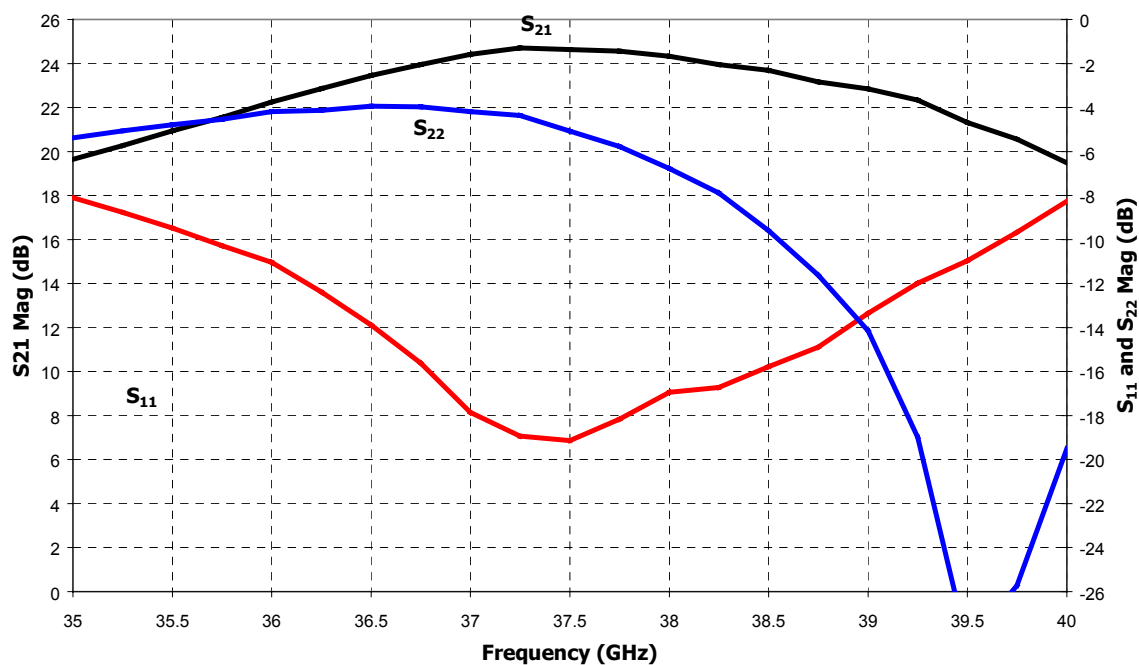
Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

- (i) Turn off RF input power,
- (ii) Turn down and off drain voltage (V_d),
- (iii) Turn down and off gate bias voltage (V_g).

Performance Data

RMWP38001, 38 GHz Power Amplifier Typical On-Wafer Measurements
 $I_{DQ} = 250$ mA $V_{DD} = 4$ V



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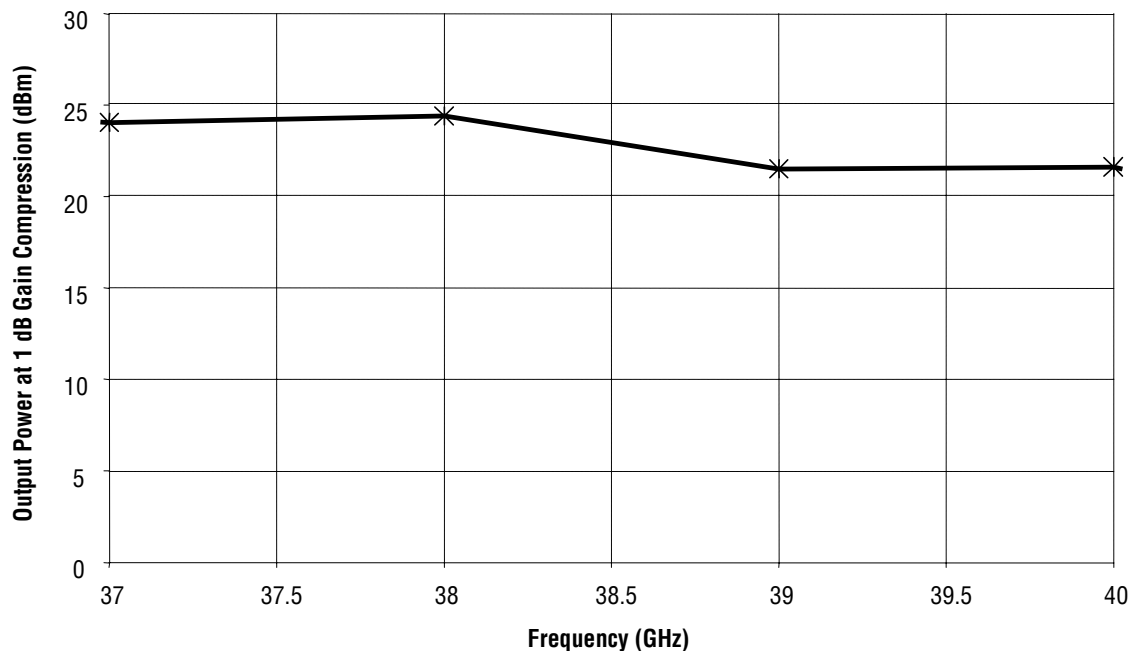
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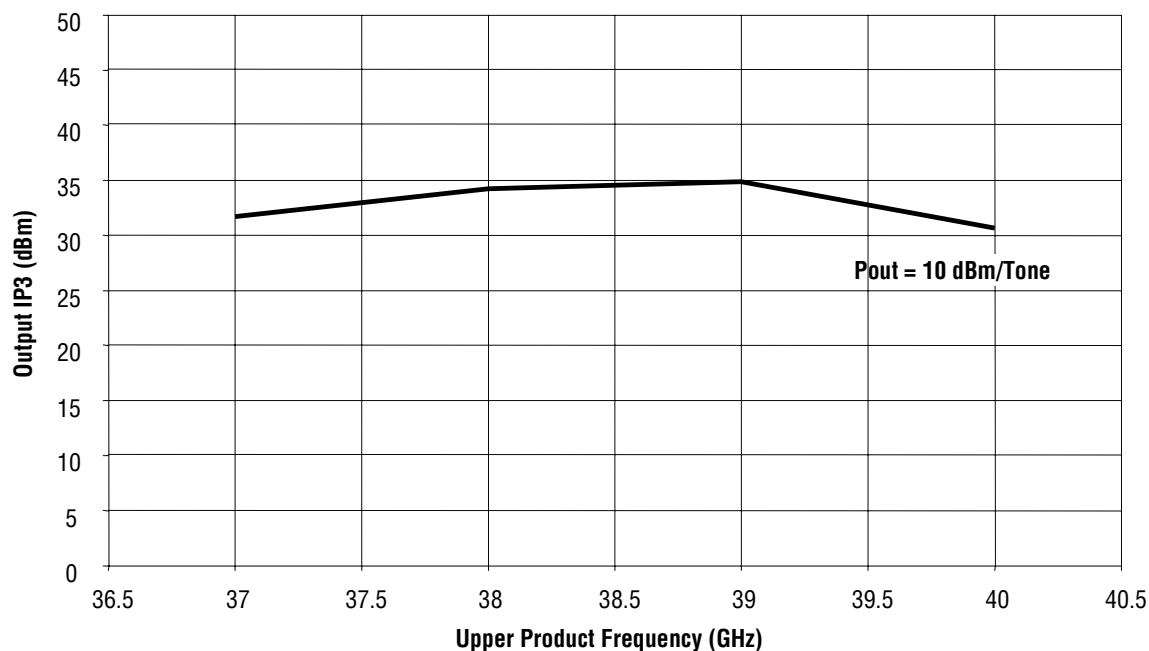
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Performance Data

RMWP38001 Typical On-Wafer Output Power at 1 dB Gain
Compression Measurements at $I_{DQ} = 290$ mA $V_{DD} = 4.0$



RMWP38001 38 GHz Power Amplifier. Typical Output IP_3 Performance in 50 Ohm Test Fixture.
 $I_{DQ} = 290$ mA, $V_{DD} = 4$ V. Tone Spacing = 1 MHz



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