

## CMOS PROGRAMMABLE DOWN COUNTERS

### FEATURES

- ◆ Internally Synchronous for High Speed
- ◆ BCD Decade (4522B) or 4-Bit Binary (4526B) Down Counters
- ◆ Asynchronous Preset Enable
- ◆ Asynchronous Reset
- ◆ Cascadable
- ◆ Logic Edge-Clocked Design
- ◆ Static Operation – DC to 5MHz @ 10Vdc
- ◆ Trigger from Either Edge of Clock Input

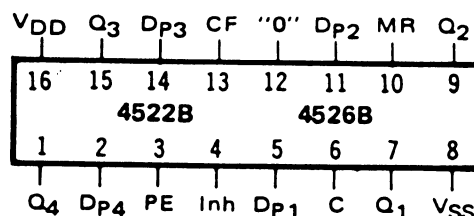
### DESCRIPTION

The 4522B BCD Counter and the 4526B Binary Counter are constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

### CONNECTION DIAGRAM (all packages)



### RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	$T_A$	-55 to +125	°C
		-40 to +85	°C

### TRUTH TABLES

#### Both Types

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
1	0	0	0	Count 1
x	1	0	0	No Count
1	x	0	0	Count 1
x	x	1	0	Preset
x	x	x	1	Reset

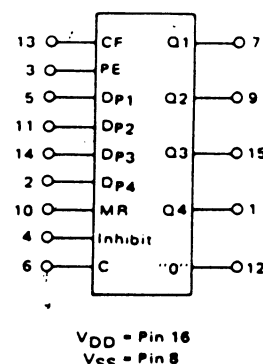
#### 4522B

Count	Output			
	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

#### 4526B

Count	Output			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

### BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS<sup>1</sup>

PARAMETER	V <sub>DD</sub> (Vdc)	CONDITIONS	T <sub>LOW</sub> <sup>2</sup>		+25°C			T <sub>HIGH</sub> <sup>2</sup>		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I <sub>DD</sub>	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub> All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	20	—	0.2	20	—	600	

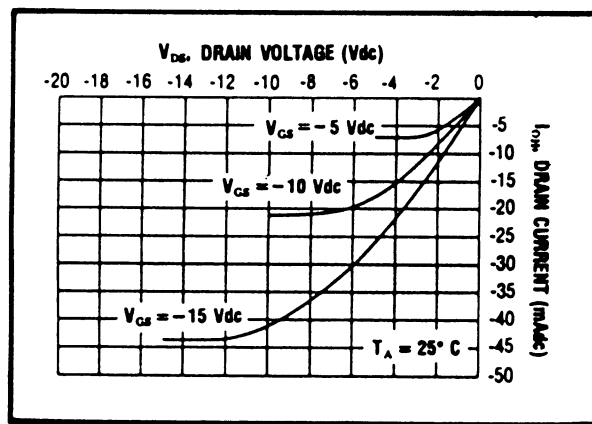
NOTES: <sup>1</sup> Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

<sup>2</sup> T<sub>LOW</sub> = -55°C for C  
       = -40°C for E  
       T<sub>HIGH</sub> = +125°C for C  
       = + 85°C for E

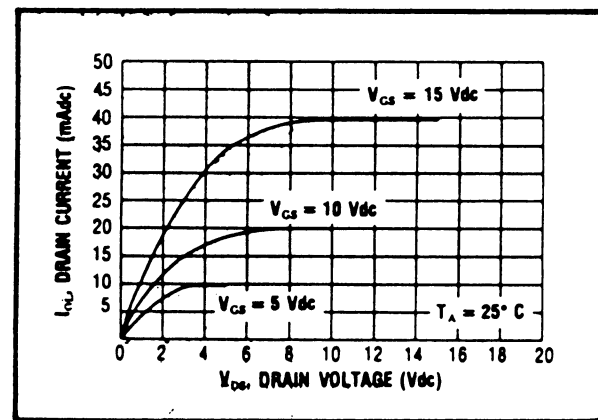
DYNAMIC CHARACTERISTICS (C<sub>L</sub> = 50pF, T<sub>A</sub> = 25°C)

PARAMETER		V <sub>DD</sub> (V dc)	Min.	Typ.	Max.	Units	
CLOCKED OPERATION							
PROPAGATION DELAY TIME Clock or Inhibit to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	5	—	415	830	ns	
		10	—	160	320		
		15	—	120	240		
	Clock or Inhibit to "O"	5	—	175	350	ns	
		10	—	125	250		
		15	—	100	200		
OUTPUT TRANSITION TIME	t <sub>TLH</sub> , t <sub>THL</sub>	5	—	100	200	ns	
10	—	50	100				
15	—	40	80				
MINIMUM CLOCK PULSE WIDTH	PW <sub>CL</sub>	5	—	125	250	ns	
10	—	50	100				
15	—	40	80				
MAXIMUM CLOCK FREQUENCY	f <sub>CL</sub>	5	1.5	2.0	—	MHz	
10	3.0	5.0	—				
15	4.0	6.6	—				
MAXIMUM CLOCK OR INHIBIT RISE AND FALL TIME <sup>1</sup>	t <sub>rCL</sub> , t <sub>fCL</sub>	5	15	—	—	μs	
10	15	—	—				
15	15	—	—				
PRESET OPERATION							
PROPAGATION DELAY TIME PE to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	5	—	415	830	ns	
		10	—	160	320		
		15	—	120	240		
	PE to "O"	5	—	175	350	ns	
		10	—	125	250		
		15	—	100	200		
MINIMUM PRESET ENABLE PULSE WIDTH	PW <sub>PE</sub>	5	—	125	250	ns	
10	—	50	100				
15	—	40	80				
MINIMUM DATA INPUT HOLD TIME	t <sub>hold</sub>	5	—	75	125	ns	
10	—	25	50				
15	—	20	40				
RESET OPERATION							
PROPAGATION DELAY TIME MR to Q	t <sub>PHL</sub>	5	—	415	830	ns	
		10	—	160	320		
		15	—	120	240		
	MR to "O"	t <sub>PLH</sub>	5	—	175	350	ns
			10	—	125	250	
			15	—	100	200	
MINIMUM MASTER RESET PULSE WIDTH	PW <sub>MR</sub>	5	—	150	300	ns	
10	—	125	250				
15	—	100	200				

<sup>1</sup> When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

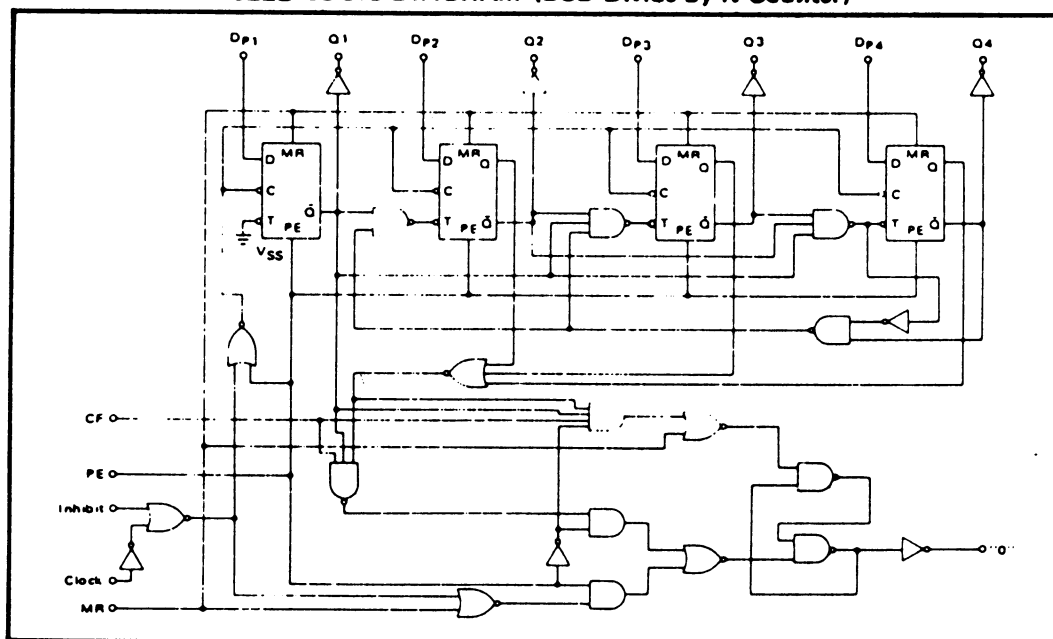


Typical P-Channel  
Source Current Characteristics

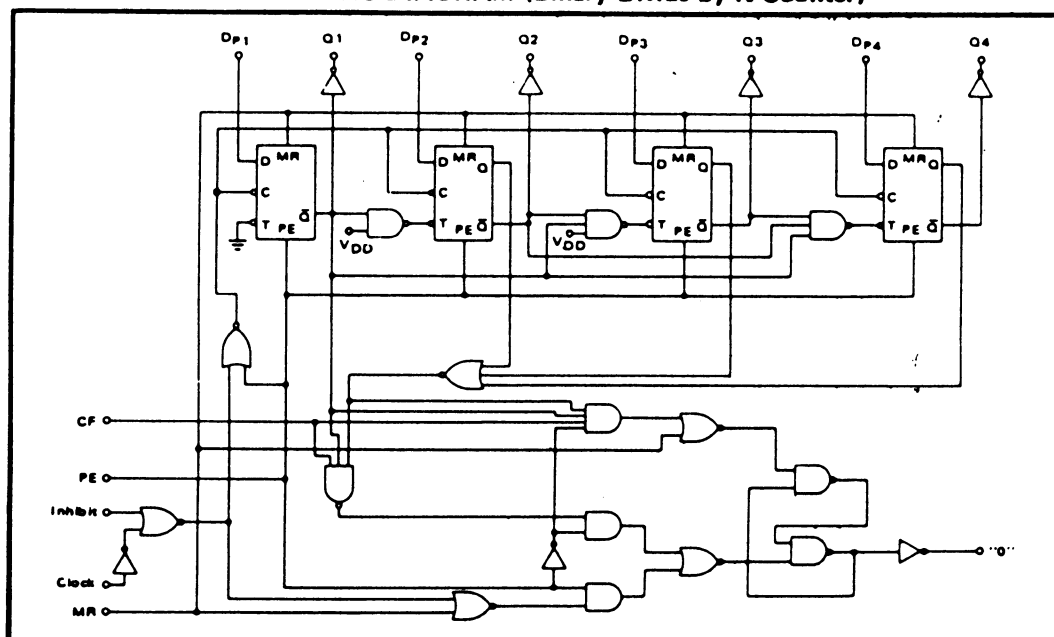


Typical N-Channel  
Sink Current Characteristics

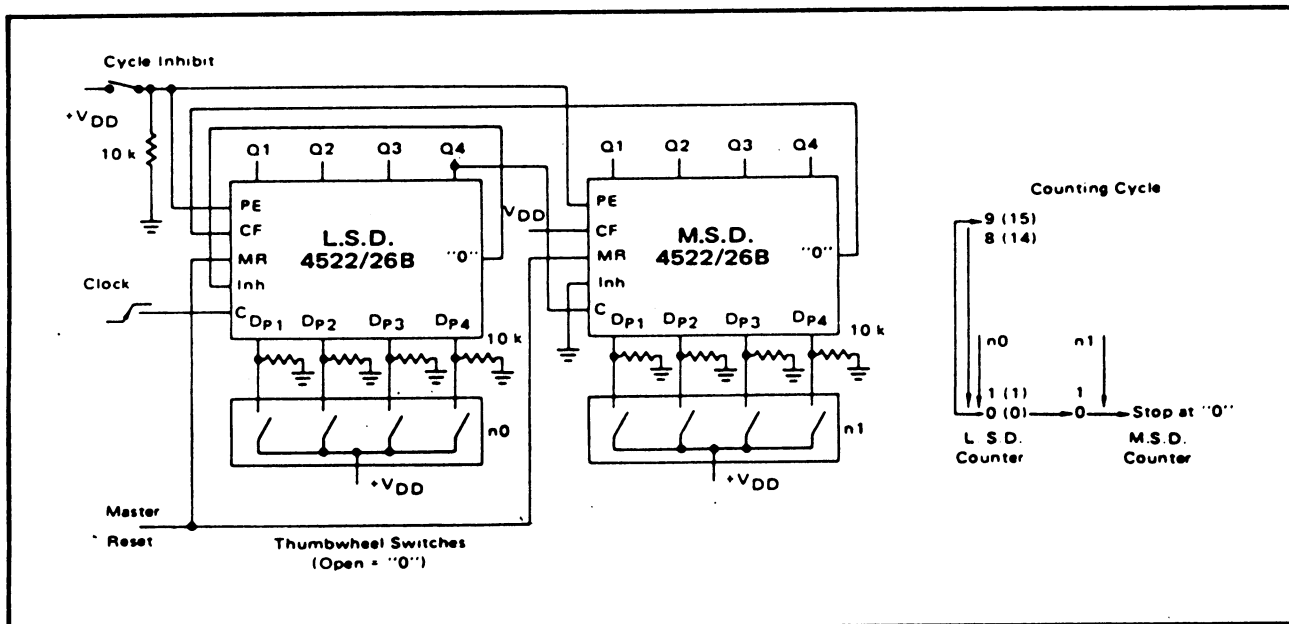
### 4522B LOGIC DIAGRAM (BCD Divide-by-N Counter)



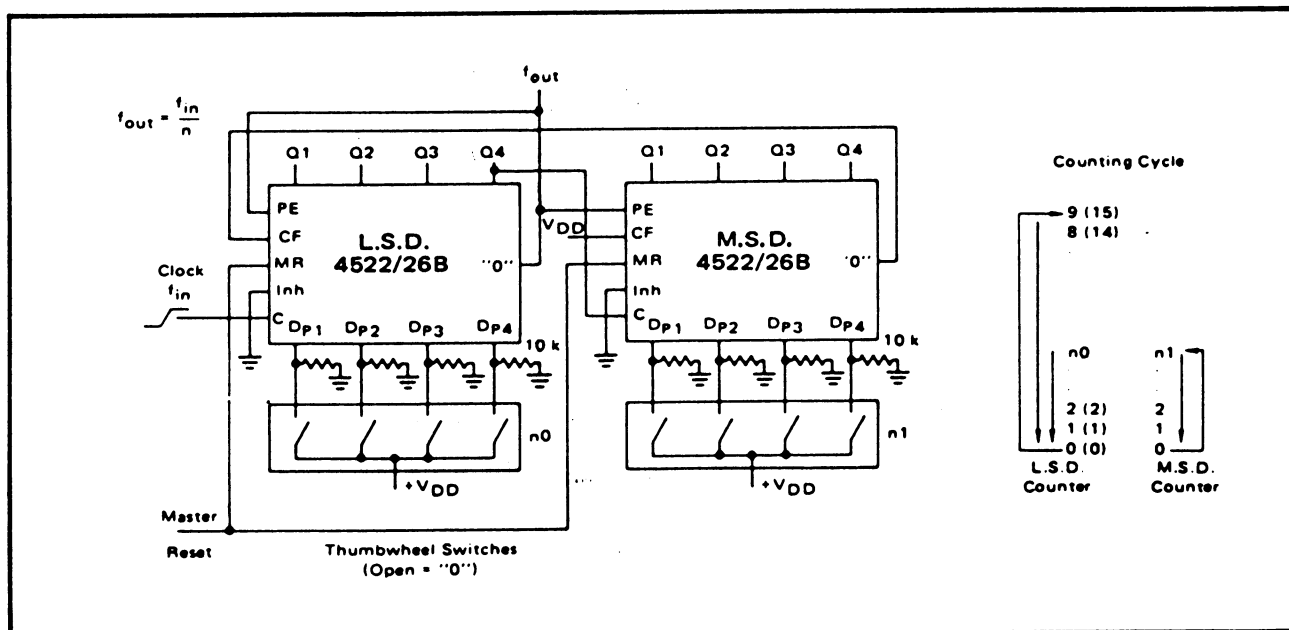
### 4526B LOGIC DIAGRAM (Binary Divide-by-N Counter)



## APPLICATIONS INFORMATION



### 2-Stage Programmable Down Counter (One Cycle)



## 2-Stage Programmable Frequency Divider