

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# H7N0307LD, H7N0307LS, H7N0307LM

Silicon N Channel MOS FET  
High Speed Power Switching

**RENESAS**

ADE-208-1516E(Z)

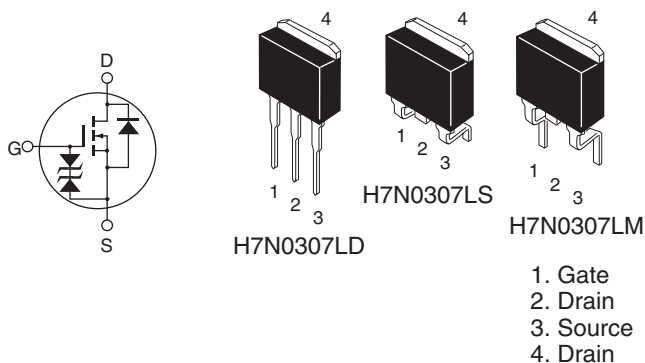
6th. Edition  
Aug. 2002

## Features

- Low on-resistance
- $R_{DS(on)} = 4.6 \text{ m}\Omega$  typ.
- Low drive current
- 4.5 V gate drive device can be driven from 5 V source

## Outline

LDPAK



**Absolute Maximum Ratings**

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	30	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	60	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	240	A
Body-drain diode reverse drain current	$I_{DR}$	60	A
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	90	W
Channel to Case Thermal Impedance	$\theta_{ch-c}$	1.39	°C/W
Channel to Ambient Thermal Impedance	$\theta_{ch-a}$	89	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1 \%$ 

2. Value at Tc = 25°C

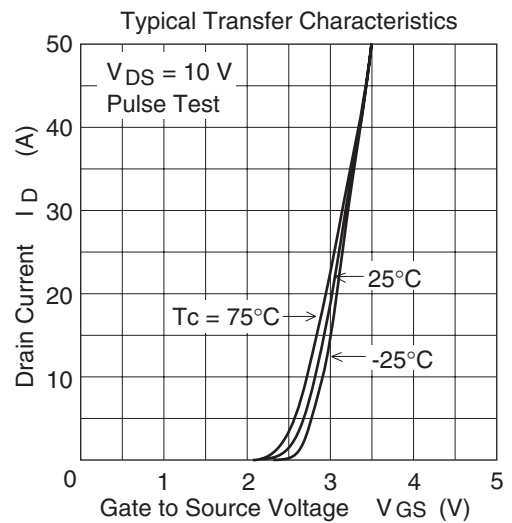
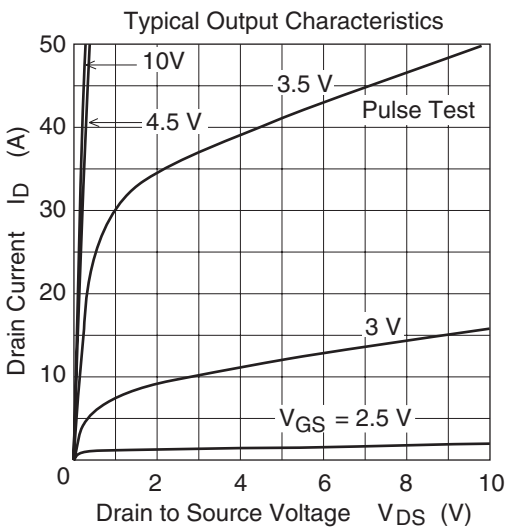
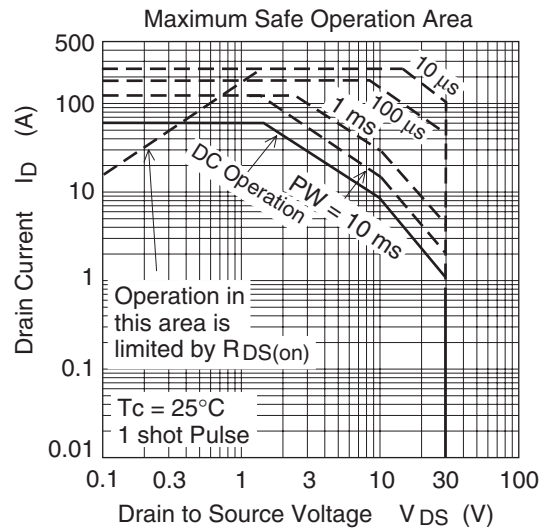
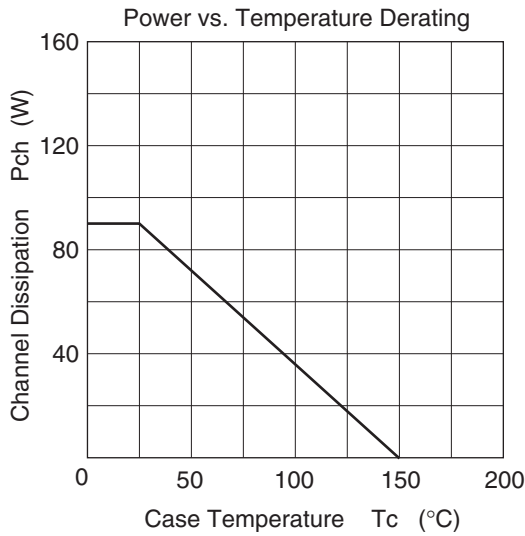
## Electrical Characteristics

(Ta = 25°C)

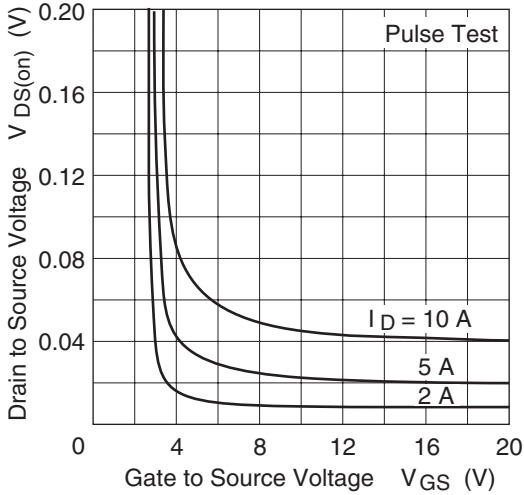
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—		$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}^{*1}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.6	5.8	$\text{m}\Omega$	$I_D = 30 \text{ A}$ , $V_{GS} = 10 \text{ V}^{*1}$
		—	8.0	11.5	$\text{m}\Omega$	$I_D = 30 \text{ A}$ , $V_{GS} = 4.5 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	40	65	—	S	$I_D = 30 \text{ A}$ , $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	$C_{iss}$	—	2500	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	650	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	350	—	pF	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	40	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	7	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	8	—	nc	$I_D = 60 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 30 \text{ A}$
Rise time	$t_r$	—	300	—	ns	$R_L = 0.33 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	$R_g = 4.7 \text{ }\Omega$
Fall time	$t_f$	—	20	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.92	—	V	$I_F = 60 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = 60 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Notes: 1. Pulse test

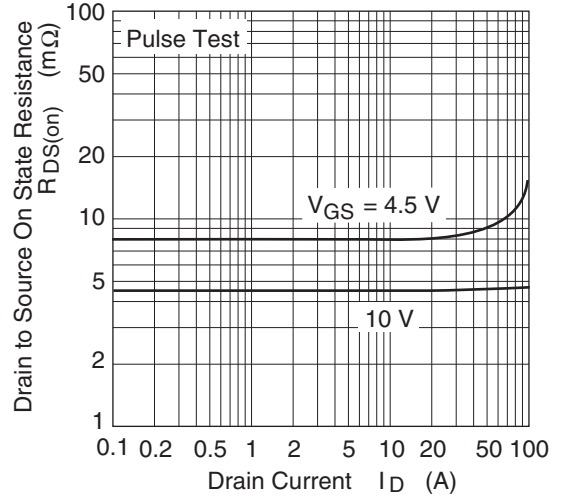
**Main Characteristics**



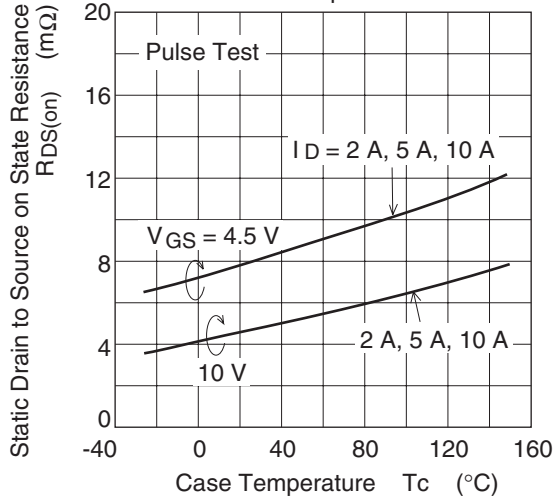
Drain to Source Saturation Voltage vs.  
Gate to Source Voltage



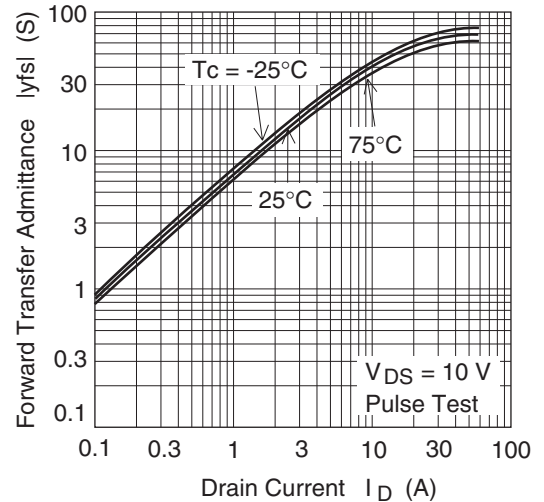
Static Drain to Source on State Resistance  
vs. Drain Current



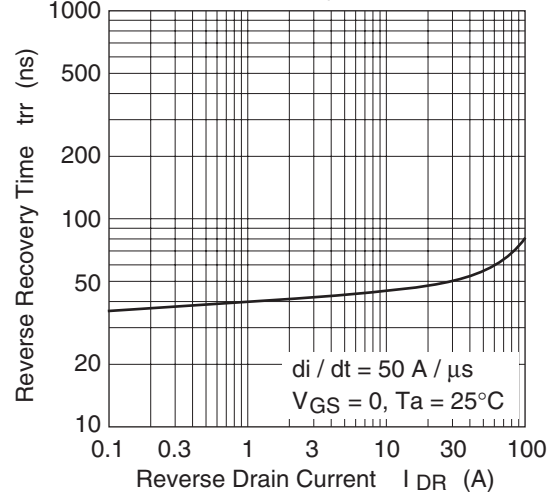
Static Drain to Source on State Resistance  
vs. Temperature



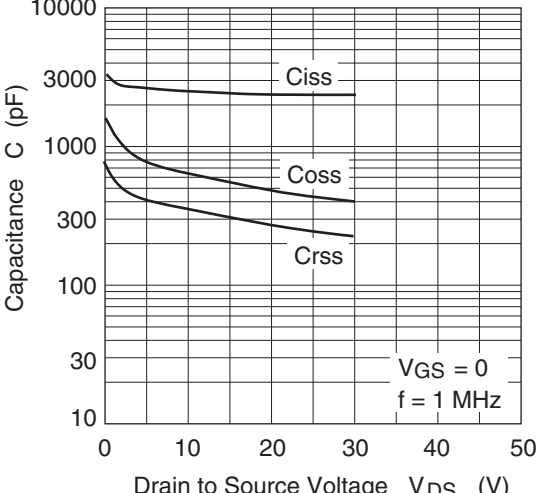
Forward Transfer Admittance vs.  
Drain Current



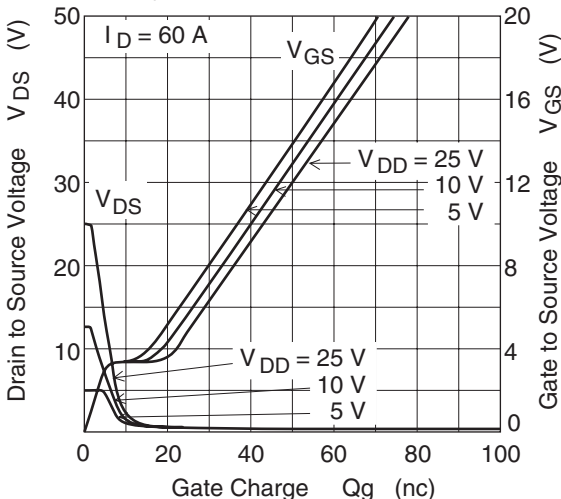
Body-Drain Diode Reverse Recovery Time



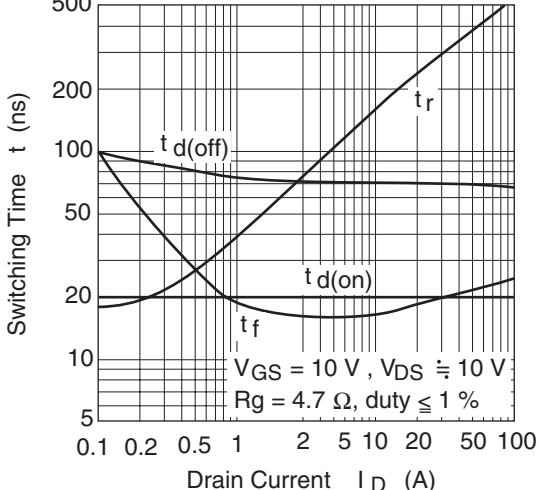
Typical Capacitance vs. Drain to Source Voltage



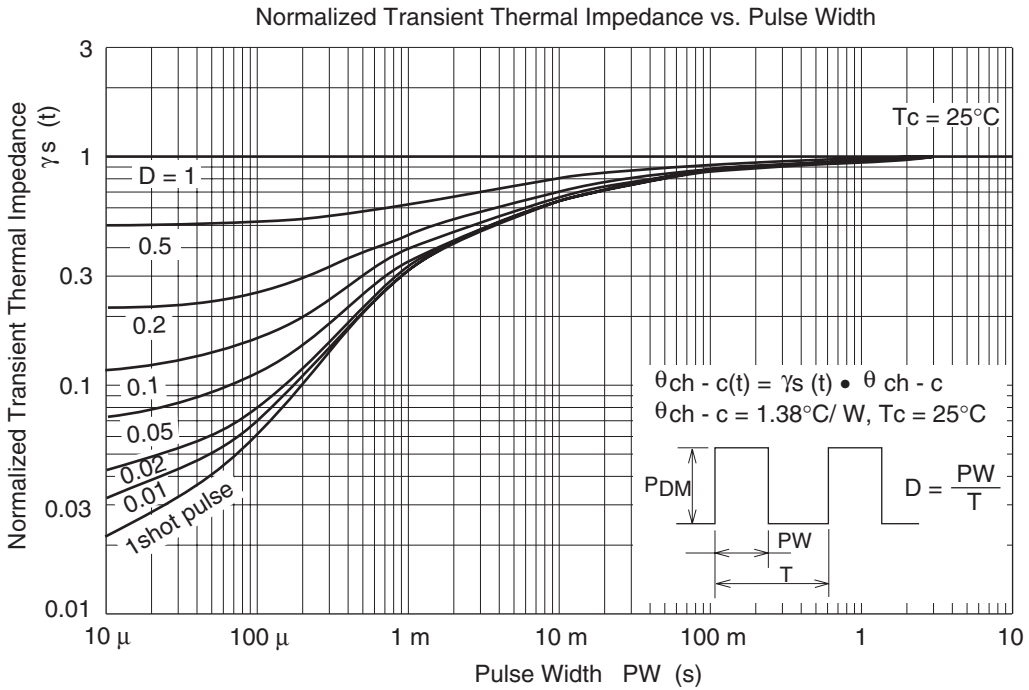
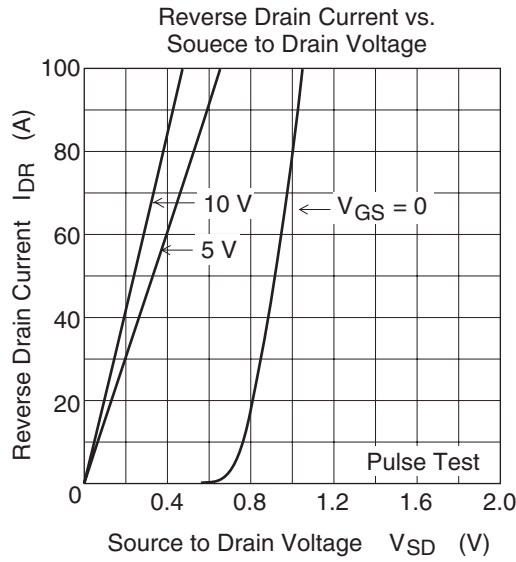
Dynamic Input Characteristics



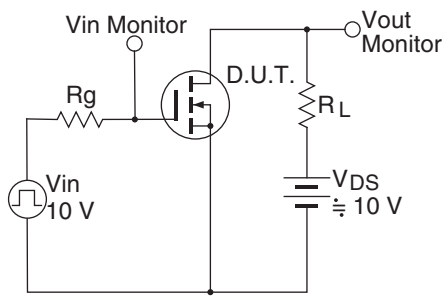
Switching Characteristics



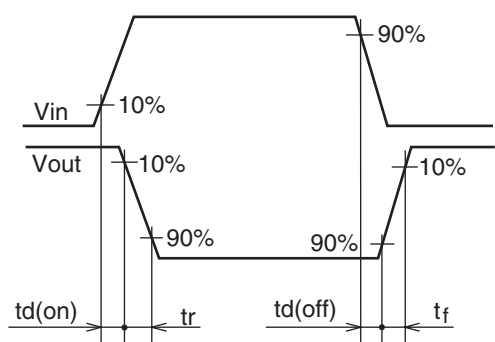




Switching Time Test Circuit



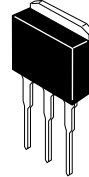
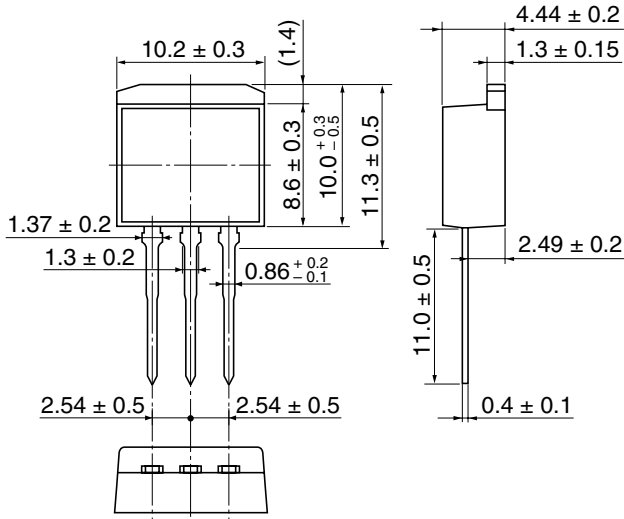
Switching Time Waveform



# Package Dimensions

## • H7N0307LD

Unit: mm

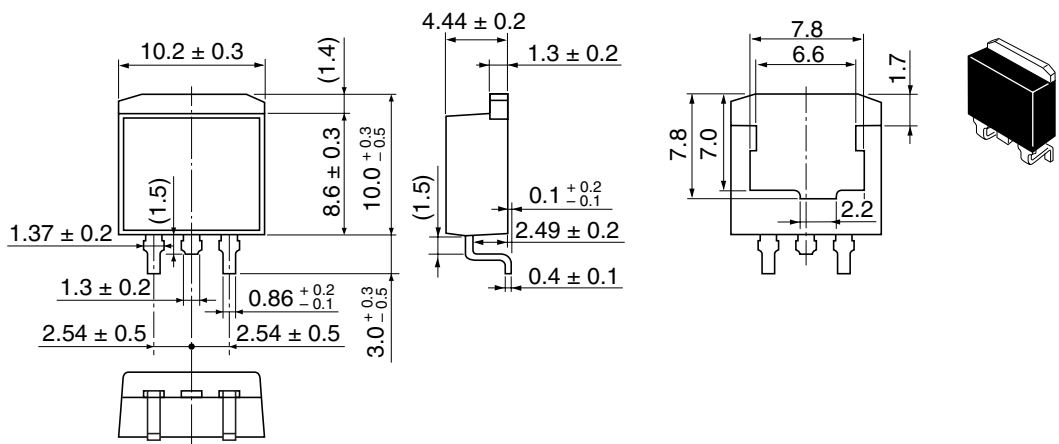


Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

H7N0307LD, H7N0307LS, H7N0307LM

• H7N0307LS

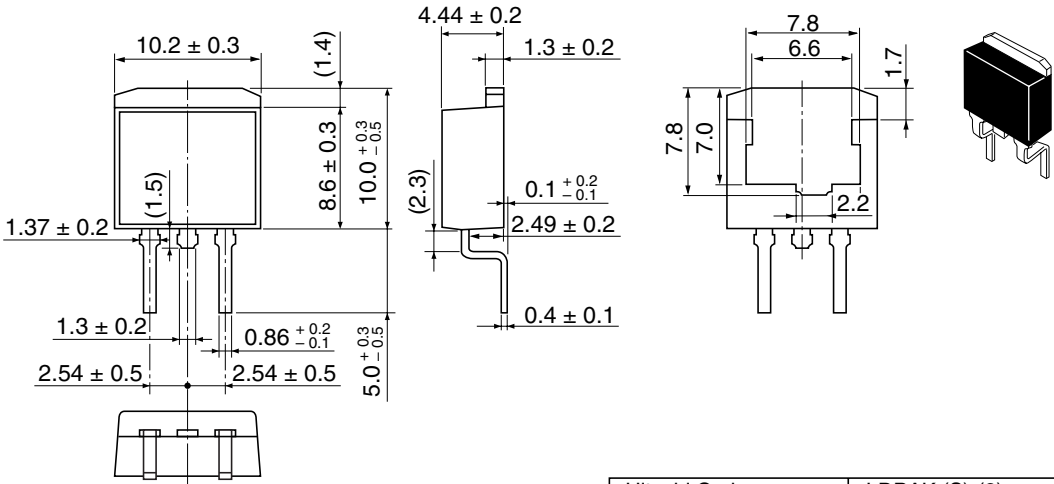
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

• H7N0307LM

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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# HITACHI

**Hitachi, Ltd.**

Semiconductor & Integrated Circuits  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL <http://www.hitachisemiconductor.com/>

**For further information write to:**

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe Ltd.  
Electronic Components Group  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585200

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher Straße 3  
D-85622 Feldkirchen  
Postfach 201, D-85619 Feldkirchen  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00  
Singapore 049318  
Tel: <65>-6538-6533/6538-8577  
Fax: <65>-6538-6933/6538-3877  
URL: <http://semiconductor.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road  
Hung-Kuo Building  
Taipei (105), Taiwan  
Tel: <886>-(2)-2718-3666  
Fax: <886>-(2)-2718-8180  
Telex: 23222 HAS-TP  
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon Hong Kong  
Tel: <852>-2735-9218  
Fax: <852>-2730-0281  
URL: <http://semiconductor.hitachi.com.hk>

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