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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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HAT2042T

Silicon N Channel Power MOS FET High Speed Power Switching

RENESAS

ADE-208-669F (Z)

7th. Edition

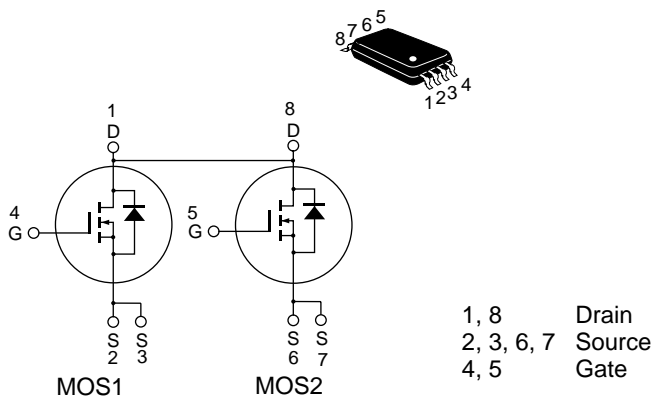
Feb. 1999

Features

- Low on-resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

Outline

TSSOP-8



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	28	V
Gate to source voltage	V_{GSS}	± 12	V
Drain current	I_D	5.0	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	40	A
Body-drain diode reverse drain current	I_{DR}	5.0	A
Channel dissipation	P_{ch} ^{Note2}	1.0	W
Channel dissipation	P_{ch} ^{Note3}	1.5	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	- 55 to + 150	°C

Note: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. 1 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10 s$

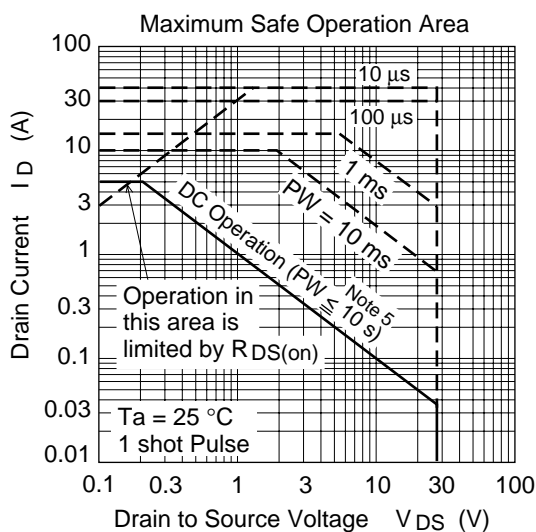
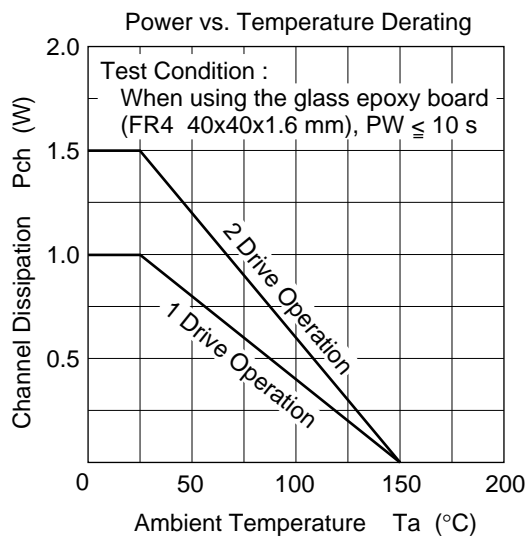
3. 2 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10 s$

Electrical Characteristics (Ta = 25°C)

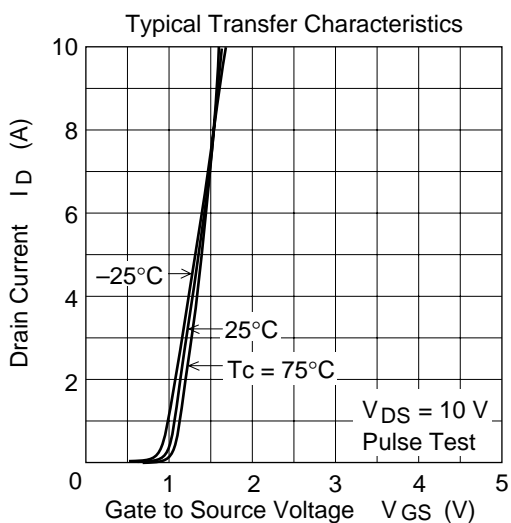
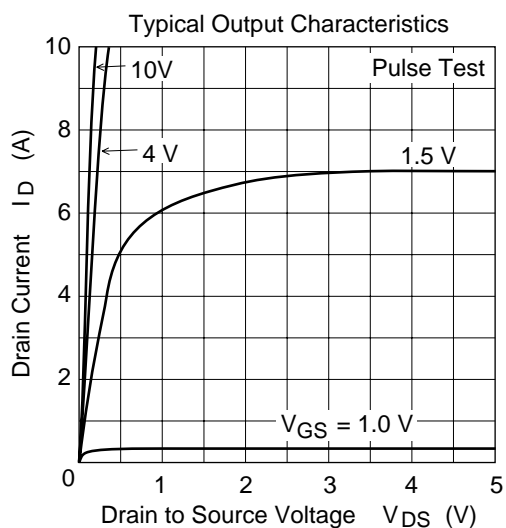
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	28	—	—	V	$I_D = 10mA$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 12 V$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 28 V$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 10 V$, $I_D = 1 mA$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.027	0.034	Ω	$I_D = 3 A$, $V_{GS} = 4 V$ ^{Note4}
	$R_{DS(on)}$	—	0.037	0.044	Ω	$I_D = 3 A$, $V_{GS} = 2.5 V$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	7	11	—	S	$I_D = 3 A$, $V_{DS} = 10 V$ ^{Note4}
Input capacitance	C_{iss}	—	510	—	pF	$V_{DS} = 10 V$
Output capacitance	C_{oss}	—	190	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	140	—	pF	$f = 1 MHz$
Total gate charge	Q_g	—	8.5	—	nc	$V_{DD} = 10 V$
Gate to source charge	Q_{gs}	—	4.5	—	nc	$V_{GS} = 4 V$
Gate to drain charge	Q_{gd}	—	4	—	nc	$I_D = 5 A$
Turn-on delay time	$t_{d(on)}$	—	14	—	ns	$V_{GS} = 4 V$, $I_D = 3 A$
Rise time	t_r	—	120	—	ns	$V_{DD} \equiv 10 V$
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	t_f	—	120	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.85	1.1	V	$IF = 5.0 A$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$IF = 5.0 A$, $V_{GS} = 0$ $diF/dt = 20 A/\mu s$

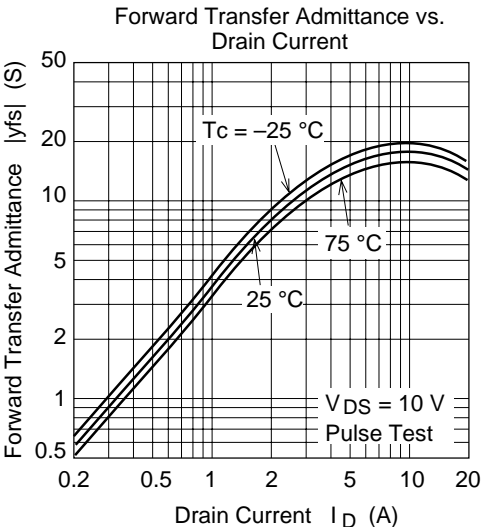
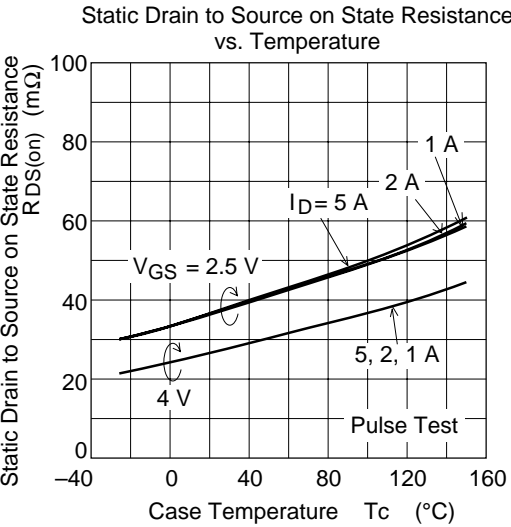
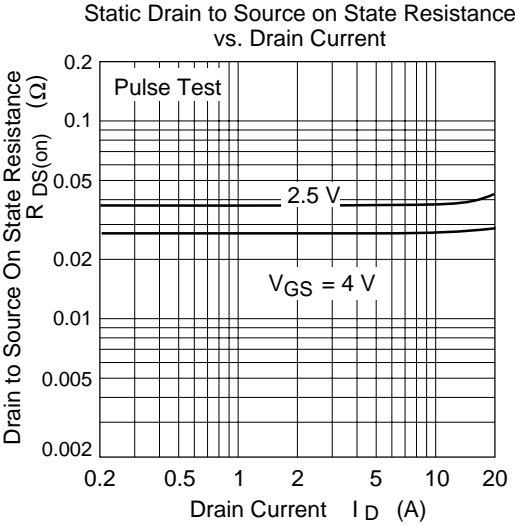
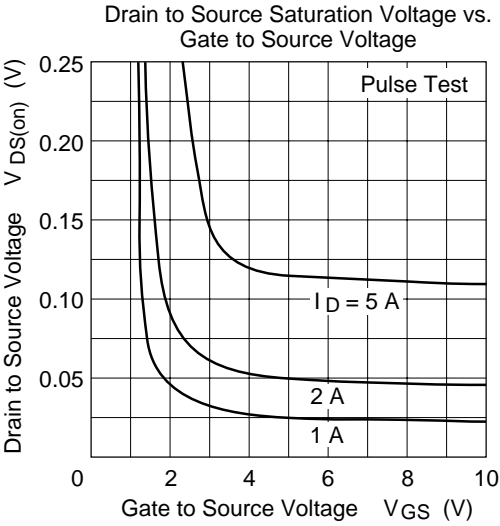
Note: 4. Pulse test

Main Characteristics

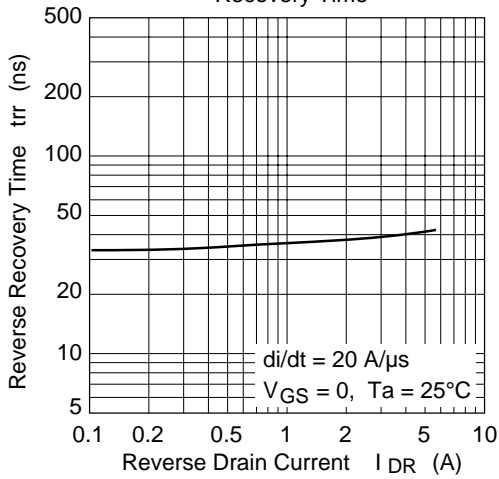


Note 5 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

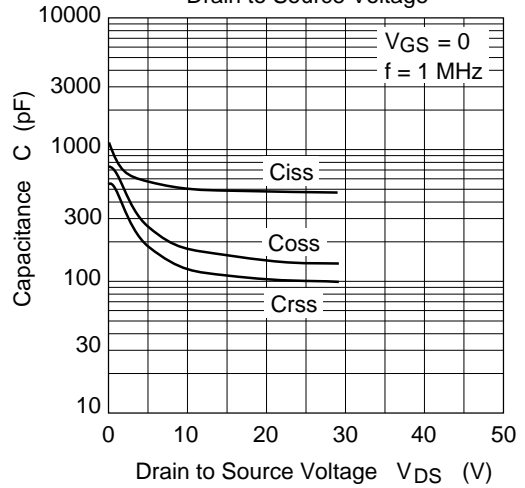




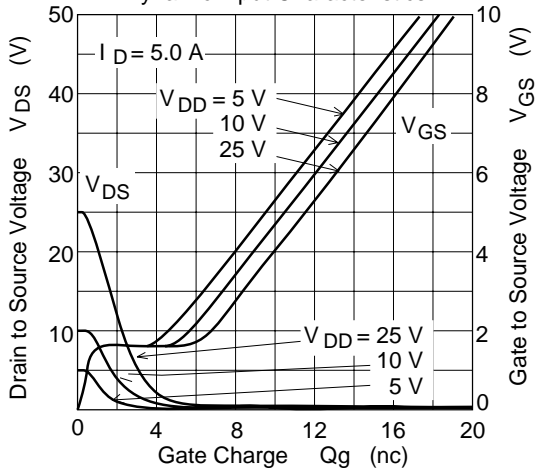
Body-Drain Diode Reverse Recovery Time



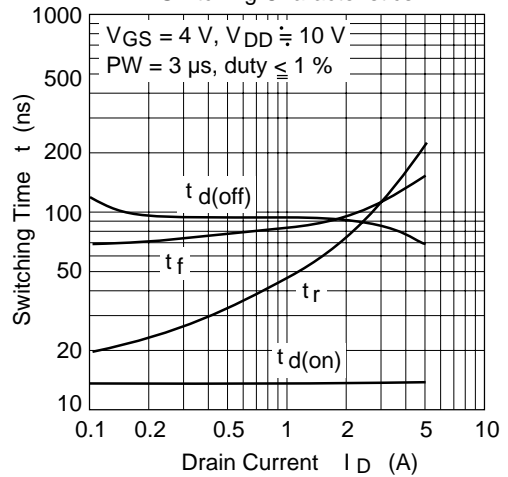
Typical Capacitance vs. Drain to Source Voltage

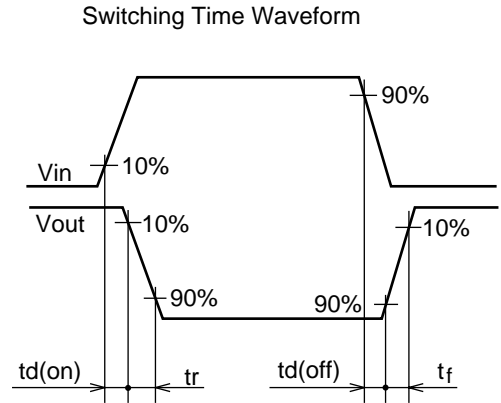
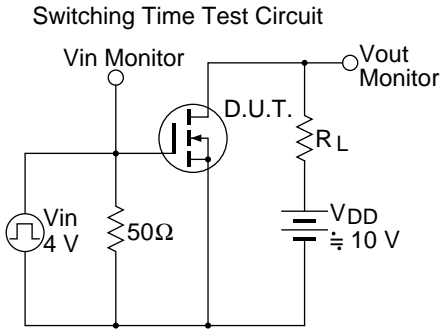
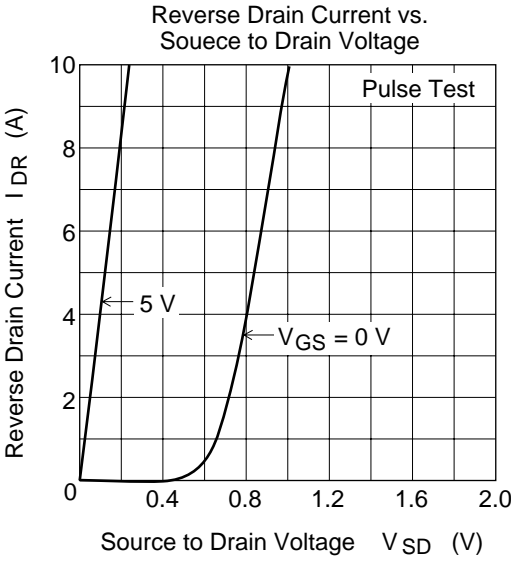


Dynamic Input Characteristics

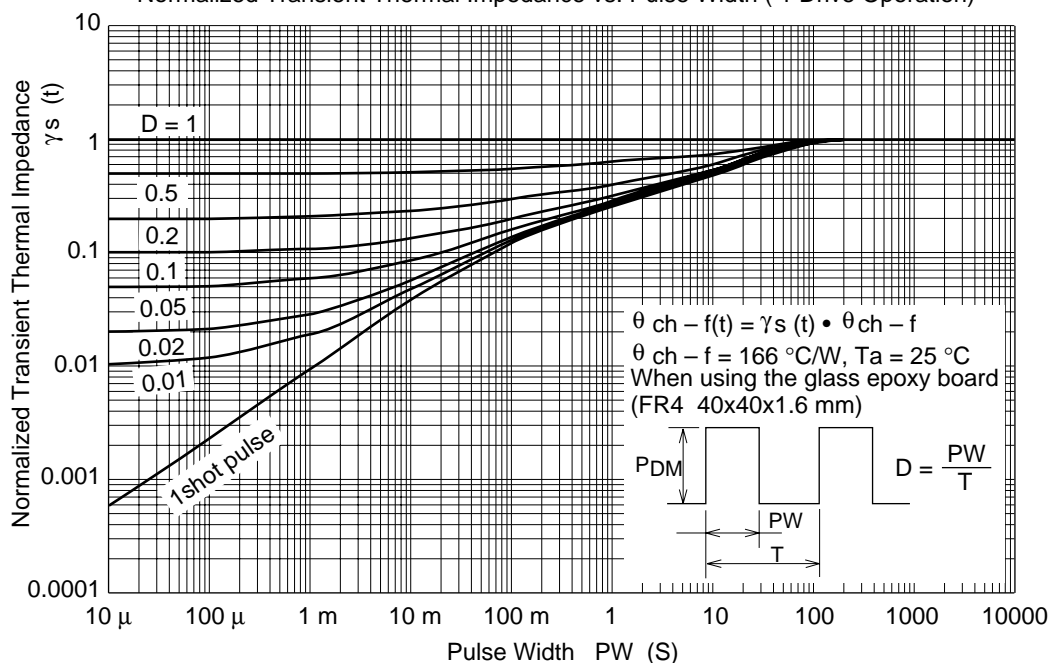


Switching Characteristics

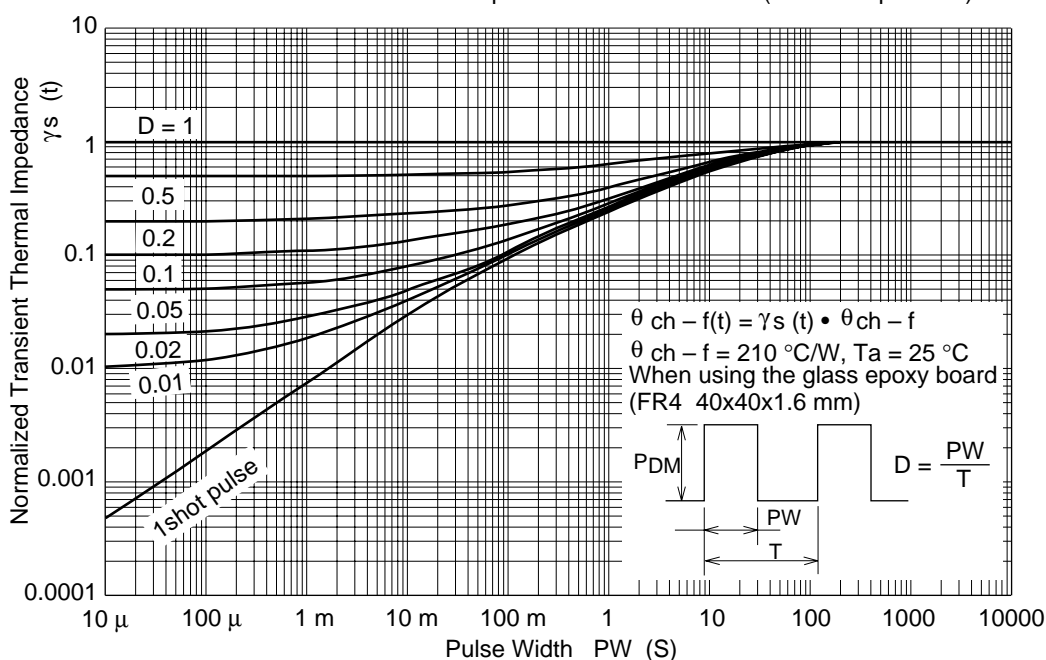




Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

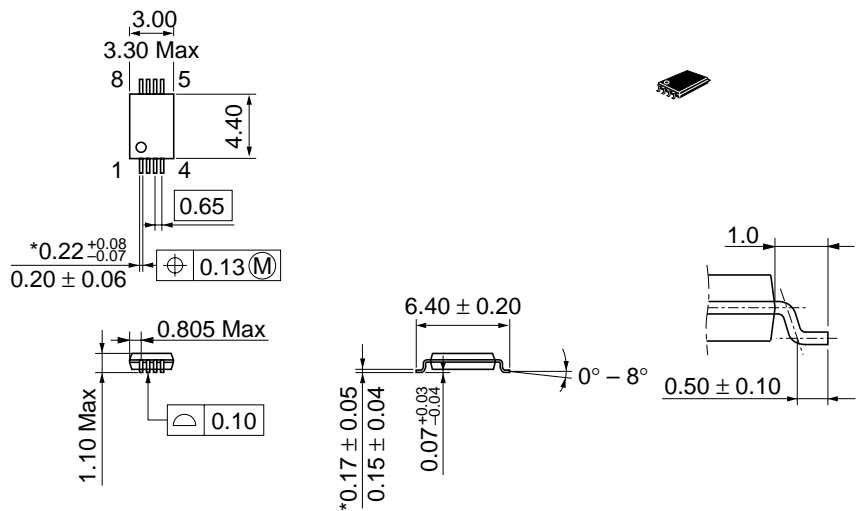


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)



Package Dimensions

As of January, 2001
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-8D
JEDEC	—
EIAJ	—
Mass (reference value)	—

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