

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT2085T

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

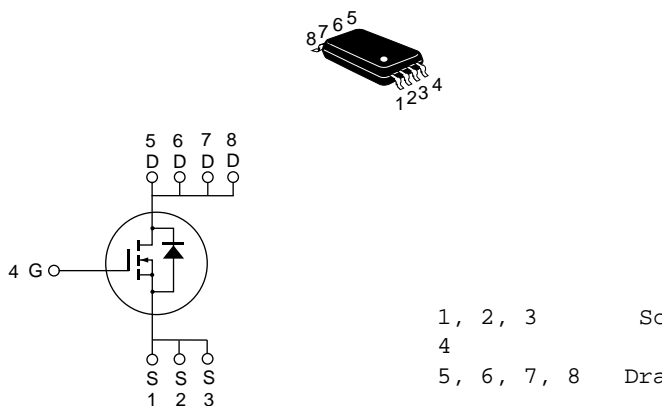
ADE-208-1028A(Z)
Target Specification 2nd. Edition
Dec. 2000

Features

- Low on-resistance
- Low drive current
- High density mounting

Outline

TSSOP-8



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	(1.4)	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	(11.2)	A
Body-drain diode reverse drain current	I_{DR}	(1.4)	A
Channel dissipation	P_{ch} ^{Note2}	1.3	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

Electrical Characteristics (Ta = 25°C)

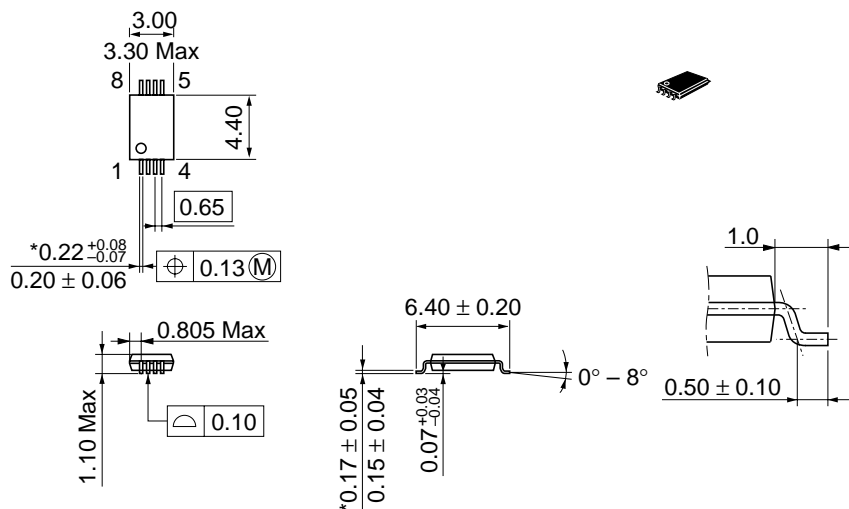
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10mA$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	$V_{GS} = \pm 30V$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 200V$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	(3.0)	—	(4.5)	V	$I_D = 1mA$, $V_{DS} = 10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.49)	(0.64)	Ω	$I_D = 0.7A$, $V_{GS} = 10V$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	(1.0)	(1.7)	—	S	$I_D = 0.7A$, $V_{DS} = 10V$ ^{Note3}
Input capacitance	C_{iss}	—	(300)	—	pF	$V_{DS} = 25V$
Output capacitance	C_{oss}	—	(43)	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	(12)	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	(19)	—	ns	$V_{DD} \cong 100V$, $I_D = 0.7A$
Rise time	t_r	—	(11)	—	ns	$V_{GS} = 10V$
Turn-off delay time	$t_{d(off)}$	—	(51)	—	ns	$R_L = 143\Omega$
Fall time	t_f	—	(17)	—	ns	$R_g = 10\Omega$
Total gate charge	Q_g	—	(10)	—	nC	$V_{DD} = 160V$
Gate to source charge	Q_{gs}	—	(2)	—	nC	$V_{GS} = 10V$
Gate to drain charge	Q_{gd}	—	(5)	—	nC	$I_D = 1.4A$
Body-drain diode forward voltage	V_{DF}	—	(0.8)	(1.2)	V	$I_F = 1.4A$, $V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	(60)	—	ns	$I_F = 1.4A$, $V_{GS} = 0$ $diF/dt = 100A/\mu s$

Note: 3. Pulse test

Package Dimensions

As of January, 2001

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-8D
JEDEC	—
EIAJ	—
Mass (reference value)	—

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
	Europe	:	http://www.hitachi-eu.com/hel/ecg
	Asia	:	http://sicapac.hitachi-asia.com
	Japan	:	http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor
(America) Inc.

179 East Tasman Drive,
San Jose, CA 95134

Tel: <1> (408) 433-1990

Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group

Dornacher Straße 3
D-85622 Feldkirchen, Munich

Germany

Tel: <49> (89) 9 9180-0

Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.

Electronic Components Group.

Whitebrook Park

Lower Cookham Road

Maidenhead

Berkshire SL6 8YA, United Kingdom

Tel: <44> (1628) 585000

Fax: <44> (1628) 585160

Hitachi Asia Ltd.

Hitachi Tower

16 Collyer Quay #20-00,

Singapore 049318

Tel: <65>-538-6533/538-8577

Fax: <65>-538-6933/538-3877

URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.

(Taipei Branch Office)

4/F, No. 167, Tun Hwa North Road,

Hung-Kuo Building,

Taipei (105), Taiwan

Tel: <886>-(2)-2718-3666

Fax: <886>-(2)-2718-8180

Telex: 23222 HAS-TP

URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.

Group III (Electronic Components)

7/F., North Tower,

World Finance Centre,

Harbour City, Canton Road

Tsim Sha Tsui, Kowloon,

Hong Kong

Tel: <852>-(2)-735-9218

Fax: <852>-(2)-730-0281

URL: <http://www.hitachi.com.hk>