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April 1, 2003

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HD151TS403SS

Mother Board Clock Generator for SiS 645/650 P4 Chipset



ADE-205-670 (Z)

Preliminary
Rev.0
Jan. 2002

Description

The HD151TS403 is a high-performance, low-skew, low-jitter, PC motherboard Clock generator. It is specifically designed for SiS645 / 650 Pentium®4 chipset.

Features

- 1 memory clock up to 200 MHz
- 2 differential pairs of HCSL CPU clock , up to 133 MHz
- 6 PCI clocks and 2 PCI_F clocks @3.3 V, 33.3 MHz typ.
- 2 copies of AGP clock @3.3 V, 66.6 MHz typ.
- 2 Zclock @ 3.3 V, 66.6 MHz typ.
- 1 copy of 48 MHz for USB @ 3.3 V
- 24 MHz / 48 MHz selectable clock @ 3.3 V
- 3 copies of 14.318 MHz reference clock @ 3.3 V
- Power save and clock stop function.
- Programmable clock output skew control function.
- I²C™ serial port programming
- Spread Spectrum modulation (−0.5% or ±0.25%)
- 48 pin SSOP (300 mils)
- Supports DDR application with clock buffer HD74CDCV851

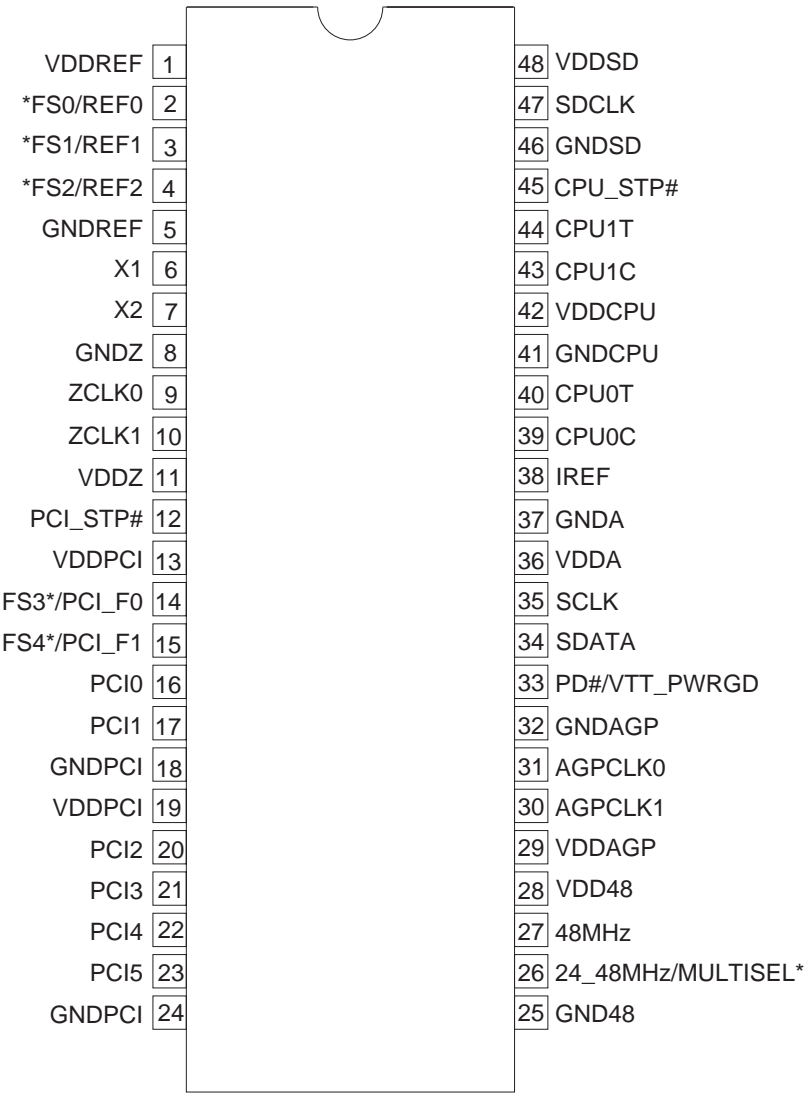
Notes: I²C is a trademark of Philips Corporation.

Pentium is registered trademark of Intel Corporation.

Key Specifications

- Supply Voltages: $VDD = 3.3\text{ V} \pm 5\%$
- Clock cycle to cycle jitter = $|250\text{ ps}|$
- CPU clock group Skew = $150\text{ ps}_{\text{max}}$
- AGP clock group Skew = $175\text{ ps}_{\text{max}}$
- ZCLK group skew = $175\text{ ps}_{\text{max}}$
- PCI clock group Skew = $500\text{ ps}_{\text{max}}$
- CPU (early) to PCI, AGP & ZCLK offset = 1 to 4 ns (typ. 2ns)

Pin Arrangement



(Top view)

* Latch input / multi function pin.

Note: FS0, 1, 2, 3, 4 = 120 kΩ Internal Pull-down.
PCI_STP#, MULTISEL, PD#, CPU_STP# = 120 kΩ Internal Pull-up.

Block Diagram

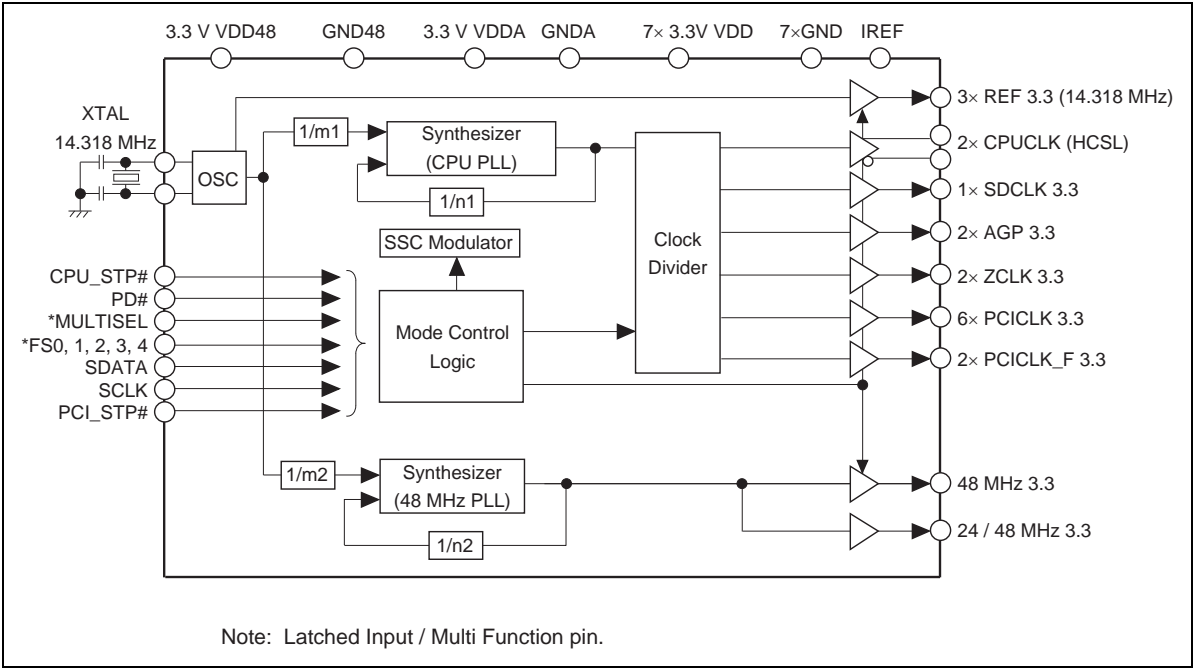


Table1 Clock Frequency Function Table & I²C

Byte0 (bit2, 4, 5, 6 & 7)

Bit2	Bit7	Bit6	Bit5	Bit4					
FS4	FS3	FS2	FS1	FS0	CPU	SDCLK	ZCLK	AGP	PCICLK
0	0	0	0	0	66	66	66	66.8	33.4
0	0	0	0	1	100	100	66	66.8	33.4
0	0	0	1	0	100	125	63	62.6	31.3
0	0	0	1	1	100	133	66	66.8	33.4
0	0	1	0	0	100	150	60	60.1	30.1
0	0	1	0	1	100	150	60	60.1	30.1
0	0	1	1	0	100	167	63	62.6	31.3
0	0	1	1	1	92	184	61	61.3	30.6
0	1	0	0	0	100	200	66	66.8	33.4
0	1	0	0	1	72	125	63	62.6	31.3
0	1	0	1	0	80	100	66	66.8	33.4
0	1	0	1	1	80	133	66	66.8	33.4
0	1	1	0	0	83	167	66	66.8	33.4
0	1	1	0	1	87	109	62	62	31
0	1	1	1	0	89	133	66	66.8	33.4
0	1	1	1	1	66	66	50	50.1	33.4
1	0	0	0	0	103	137	68	68.4	34.2
1	0	0	0	1	105	140	60	60	30
1	0	0	1	0	109	109	62	62	31
1	0	0	1	1	109	145	62	62	31
1	0	1	0	0	113	151	65	64.8	32.4
1	0	1	0	1	111	167	66	66.8	33.4
1	0	1	1	0	133	133	66	66.8	33.4
1	0	1	1	1	125	167	63	62.6	31.3
1	1	0	0	0	100	133	80	66.8	33.4
1	1	0	0	1	100	167	72	62.6	31.3
1	1	0	1	0	100	133	80	66.8	33.4
1	1	0	1	1	100	167	83	62.6	31.3
1	1	1	0	0	100	133	100	66.8	33.4
1	1	1	0	1	100	167	100	62.6	31.3
1	1	1	1	0	133	133	100	66.8	33.4
1	1	1	1	1	125	167	100	62.6	31.3

Table2 Outputs State at Power Down

INPUT		OUTPUTS						
PD#	CPUT	CPUC	SDCLK	PCICLK	ZCLK	AGP	24 / 48 MHz	48 MHz
0	2 x IREF	Hi-Z	L	L	L	L	L	L
1	Run	Run	Run	Run	Run	Run	Run	Run

Table3 CPUCLK Outputs Specification

MULTISEL (pin26)	Board Target Trace / Term Z	Reference R, Iref = VDD / (3 Rr)	Output Current loh	Voh @ Z
1	60 Ω	Rr = 475 1% I_REF = 2.32 mA	6 x Iref	0.85V @ 60 Ω
1	50 Ω	Rr = 475 1% I_REF = 2.32 mA	6 x Iref	0.71V @ 50 Ω
0	60 Ω	Rr = 475 1% I_REF = 2.32 mA	4 x Iref	0.56V @ 60 Ω
0	50 Ω	Rr = 475 1% I_REF = 2.32 mA	4 x Iref	0.47V @ 50 Ω

I²C Controlled Register Bit Map

Byte0 CLK Frequency & SSC Control Register

Bit	Description	Contents	Default
7	CLK Freq. Control bit	(See Table1)	0
6	CLK Freq. Control bit	(See Table1)	0
5	CLK Freq. Control bit	(See Table1)	0
4	CLK Freq. Control bit	(See Table1)	0
3	Freq. Select Mode bit	0 = Freq. is selected by latched input FS0 : 4 1 = Freq. is selected by I ² C Byte0 bit2, 4-7	0
2	CLK Freq. Control bit	(See Table1)	0
1	SSC Enable bit	"1" = SSC OFF, "0" = SSC ON	1
0	Outputs (All outputs) enable bit	0 = Running 1 = Tristate all outputs	0

Byte1 Multi Input-pin Read Back Register

Bit	Description	Contents	Default
7	(Reserved bit)		0
6	(Reserved bit)		0
5	MULTISEL (pin26) Read back		X
4	FS4 (pin15) Read back		X
3	FS3 (pin14) Read back		X
2	FS2 (pin4) Read back		X
1	FS1 (pin3) Read back		X
0	FS0 (pin2) Read back		X

I²C Controlled Register Bit Map (cont.)

Byte2 PCI_STP# & CPU_STP# Control Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	PCI_STP# (pin12) Function (PCI_F0 Control)	When this bit is "1", PCI_F0 will be stopped by PCI_STP# pin. When this bit is "0", PCI_F0 will not be controlled by PCI_STP# pin. (PCI_F0 = free running)	0
4	PCI_STP# (pin12) Function (PCI_F1 Control)	When this bit is "1", PCI_F1 will be stopped by PCI_STP# pin. When this bit is "0", PCI_F1 will not be controlled by PCI_STP# pin. (PCI_F1 = free running)	0
3	CPU_STP# (pin45) Function (CPU0T / 0C Control)	When this bit is "1", CPU0T / 0C will be stopped by CPU_STP# pin. CPU0T / 0C will be "fixed Low" at CPU_STP# = Low. Default is "1" Clock Stop Mode. When this bit is "0", CPU0T / 0C will not be controlled by CPU_STP# pin. (CPU0T / 0C = free running)	1
2	CPU_STP# (pin45) Function (CPU1T / 1C Control)	When this bit is "1", CPU1T / 1C will be stopped by CPU_STP# pin. CPU1T / 1C will be "fixed Low" at CPU_STP# = Low. When this bit is "0", CPU1T / 1C will not be controlled by CPU_STP# pin. (CPU1T / 1C = free running) Default is "0" Clock Free Running Mode.	0
1	CPU0T / 0C output Enable	1 = Enable, 0 = Disable (Tristate)	1
0	CPU1T / 1C output Enable	1 = Enable, 0 = Disable (Tristate)	1

I²C Controlled Register Bit Map (cont.)

Byte3 PCI Clock Outputs Control Register

Bit	Description	Contents	Default
7	PCI_F1 (pin15) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
6	PCI_F0 (pin14) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
5	PCI5 (pin23) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
4	PCI4 (pin22) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
3	PCI3 (pin21) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
2	PCI2 (pin20) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
1	PCI1 (pin17) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
0	PCI0 (pin16) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1

Byte4 Peripheral clocks Control Register

Bit	Description	Contents	Default
7	PD# (pin33) pin function enable	1 = Enable, 0 = PD# Disable	1
6	(Reserved)		0
5	48 MHz (pin27) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
4	24_48 MHz (pin26) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
3	24 MHz or 48 MHz Select	When this bit = "0", pin26 outputs 24 MHz When this bit = "1", pin26 outputs 48 MHz	0
2	(Reserved)		0
1	(Reserved)		0
0	Spread spectrum control register	0 : $\pm 0.25\%$ central spread. The modulation rate is 33 KHz. 1 : 0 to -0.5% down spread. The modulation rate is 33 KHz.	0

I²C Controlled Register Bit Map (cont.)

Byte5 Clock Output Enable Register

Bit	Description	Contents	Default
7	SDCLK (pin47) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
6	REF2 (pin4) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
5	REF1 (pin3) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
4	REF0 (pin2) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
3	ZCLK1 (pin10) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
2	ZCLK0 (pin9) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
1	AGPCLK1 (pin30) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
0	AGPCLK0 (pin31) output enable	1 = Enable, 0 = Disable (DC Low fixed)	1

Byte6 Reserved Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	(Reserved)		1
4	(Reserved)		1
3	(Reserved)		1
2	(Reserved)		1
1	(Reserved)		1
0	(Reserved)		1

Byte7 Reserved Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	(Reserved)		0
4	(Reserved)		0
3	(Reserved)		0
2	(Reserved)		0
1	(Reserved)		0
0	(Reserved)		0

I²C Controlled Register Bit Map (cont.)

Byte8 Byte Vendor / Device ID Read Back Register

Bit	Description	Contents	Default
7	Vendor ID bit3	Hitachi = "1111"	1
6	Vendor ID bit2		1
5	Vendor ID bit1		1
4	Vendor ID bit0		1
3	Device ID bit3		0
2	Device ID bit2		0
1	Device ID bit1		0
0	Device ID bit0		1

Note: Don't write to this byte.

Byte9 PLL N Divide Ratio Control Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	(Reserved)		0
4	(Reserved)		0
3	(Reserved)		0
2	PLL divide control register	0 : Byte0 (bit2, 4, 5, 6, 7) 1 : Byte9, 10, 11 (PLL N & M divider)	0
1	PLL N Divider Control bit9	PLL N Divider Control bit9	0
0	PLL N Divider Control bit8	PLL N Divider Control bit8	0

Byte10 PLL N Divide Ratio Control Register

Bit	Description	Contents	Default
7	PLL N Divider Control bit7	PLL N Divider Control bit7	0
6	PLL N Divider Control bit6	PLL N Divider Control bit6	0
5	PLL N Divider Control bit5	PLL N Divider Control bit5	0
4	PLL N Divider Control bit4	PLL N Divider Control bit4	0
3	PLL N Divider Control bit3	PLL N Divider Control bit3	0
2	PLL N Divider Control bit2	PLL N Divider Control bit2	0
1	PLL N Divider Control bit1	PLL N Divider Control bit1	0
0	PLL N Divider Control bit0	PLL N Divider Control bit0	0

I²C Controlled Register Bit Map (cont.)

Byte11 PLL M Divide Ratio Control Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	PLL M Divider Control bit6	PLL M Divider Control bit6	0
5	PLL M Divider Control bit5	PLL M Divider Control bit5	0
4	PLL M Divider Control bit4	PLL M Divider Control bit4	0
3	PLL M Divider Control bit3	PLL M Divider Control bit3	0
2	PLL M Divider Control bit2	PLL M Divider Control bit2	0
1	PLL M Divider Control bit1	PLL M Divider Control bit1	0
0	PLL M Divider Control bit0	PLL M Divider Control bit0	0

Byte12 Reserved Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	(Reserved)		0
4	(Reserved)		0
3	(Reserved)		0
2	(Reserved)		0
1	(Reserved)		0
0	(Reserved)		0

Byte13 Reserved Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	(Reserved)		0
4	(Reserved)		0
3	(Reserved)		0
2	(Reserved)		0
1	(Reserved)		0
0	(Reserved)		0

I²C Controlled Register Bit Map (cont.)

Byte14 CPU Clock Skew Control Register

Bit	Description	Contents	Default
7	CPUT / C0 Skew Control bit3	0000 : Ahead 2000 ps 0001 : Ahead 1500 ps 0010 : Ahead 1000 ps 0011 : Ahead 500 ps	0
6	CPUT / C0 Skew Control bit2	0100 : Ahead 0 ps (Default) 0101 : Delay 500 ps 0110 : Delay 1000 ps	1
5	CPUT / C0 Skew Control bit1	0111 : Delay 1500 ps 1000 : Delay 2000 ps	0
4	CPUT / C0 Skew Control bit0		0
3	CPUT / C1 Skew Control bit3	0000 : Ahead 2000 ps 0001 : Ahead 1500 ps 0010 : Ahead 1000 ps 0011 : Ahead 500 ps	0
2	CPUT / C1 Skew Control bit2	0100 : Ahead 0 ps (Default) 0101 : Delay 500 ps 0110 : Delay 1000 ps	1
1	CPUT / C1 Skew Control bit1	0111 : Delay 1500 ps 1000 : Delay 2000 ps	0
0	CPUT / C1 Skew Control bit0		0

Byte15 SDCLK (Mem. Clock) skew Control Register

Bit	Description	Contents	Default
7	SDCLK (Memory Clock) Skew Control bit3	0000 : Ahead 2000 ps 0001 : Ahead 1500 ps 0010 : Ahead 1000 ps 0011 : Ahead 500 ps	0
6	SDCLK (Memory Clock) Skew Control bit2	0100 : Ahead 0 ps (Default) 0101 : Delay 500 ps 0110 : Delay 1000 ps	1
5	SDCLK (Memory Clock) Skew Control bit1	0111 : Delay 1500 ps 1000 : Delay 2000 ps	0
4	SDCLK (Memory Clock) Skew Control bit0		0
3	(Reserved)		0
2	(Reserved)		0
1	(Reserved)		0
0	(Reserved)		0

I2C Controlled Register Bit Map (cont.)

Byte16 Reserved Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	(Reserved)		0
4	(Reserved)		0
3	(Reserved)		0
2	(Reserved)		0
1	(Reserved)		0
0	(Reserved)		0

Byte17 Reserved Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	(Reserved)		0
4	(Reserved)		0
3	(Reserved)		0
2	(Reserved)		0
1			0
0	(Reserved)		0

I²C Controlled Register Bit Map (cont.)

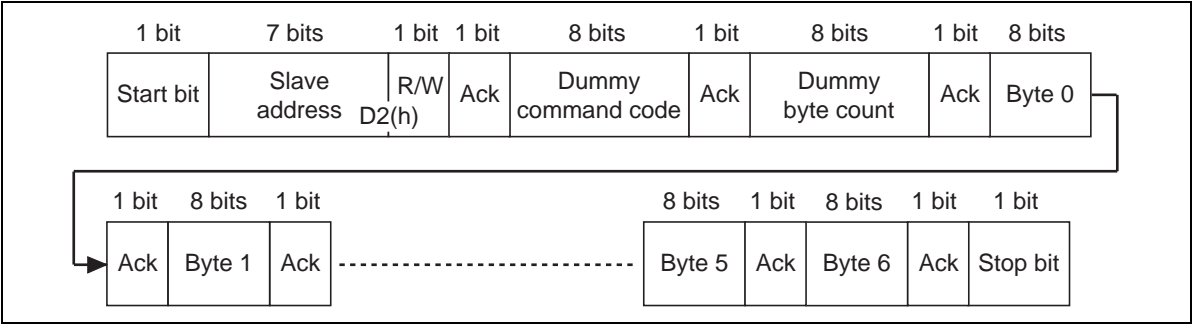
Byte18 CPU Clock PD# State Control Register

Bit	Description	Contents	Default
7	CPUCLKT / C0 state control at power down mode.	0 : CPUCLKT0 outputs 2x Iref current and CPUCLKC0 is tristate when PD# asserted. 1 : Both CPUCLKT0 and CPUCLKC0 are tristate when PD# asserted.	0
6	CPUCLKT / C1 state control at power down mode.	0 : CPUCLKT1 outputs 2x Iref current and CPUCLKC1 is tristate when PD# asserted. 1 : Both CPUCLKT1 and CPUCLKC1 are tristate when PD# asserted.	0
5	(Reserved bit)		0
4	(Reserved bit)		0
3	(Reserved bit)		0
2	(Reserved bit)		0
1	(Reserved bit)		0
0	(Reserved bit)		0

I²C Serial Interface Operation

1. Write mode

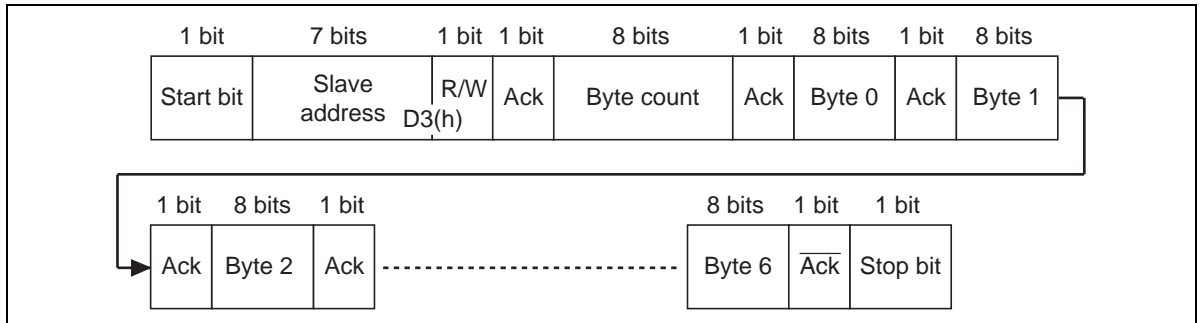
- 1.1 Controller (host) sends a start bit.
- 1.2 Controller (host) sends the write address D2 (h).
- 1.3 TS403 clock will acknowledge (TS403 sends “L”).
- 1.4 Controller (host) sends a dummy command code.
- 1.5 TS403 clock will acknowledge (TS403 sends “L”).
- 1.6 Controller (host) sends a dummy byte count.
- 1.7 TS403 clock will acknowledge (TS403 sends “L”).
- 1.8 Controller (host) starts sending first byte (Byte0) through byte6.
- 1.9 TS403 clock will acknowledge each byte one at a time.
- 1.10 Controller (host) sends a stop bit.



I²C Serial Interface Operation (cont.)

2. Read mode

- 2.1 Controller (host) sends a start bit.
- 2.2 Controller (host) sends the read address D3 (h).
- 2.3 TS403 clock will acknowledge (TS403 sends “L”).
- 2.4 TS403 clock will send the byte count. (TS403 send “12 (h)”).
- 2.5 Controller (host) acknowledges.
- 2.6 TS403 clock sends first byte (Byte0) through byte 6.
- 2.7 Controller (host) will need to acknowledge each byte.
- 2.8 Controller (host) send a stop bit.



- Notes:
1. The TS403 clock generator is a slave / receiver, I²C component. It can read back the data stored in the latches for the verification.
 2. The data transfer rate supported by this clock generator is 100 kbits / sec or less (standard mode).
 3. The input is operating at 3.3 V logic levels.
 4. The data byte format is 8 bit bytes.
 5. To simplify the clock generator I²C interface, the protocol is set to use only block-write from the controller.
The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The command code and byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a stop sequence is issued.
 6. At power-on, all registers are set to a default condition, as shown.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	VDD	−0.5 to 4.6	V	
Input voltage	V _I	−0.5 to 4.6	V	
Output voltage ^{*1}	V _O	−0.5 to VDD +0.5	V	
Input clamp current	I _{IK}	−50	mA	V _I < 0
Output clamp current	I _{OK}	−50	mA	V _O < 0
Continuous output current	I _O	±50	mA	V _O = 0 to VDD
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	Tstg	−65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

- 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	VDD	3.135	3.3	3.465	V	
DC input signal voltage		−0.3	—	VDD+0.3	V	
High level input voltage	V _{IH}	2.0	—	VDD+0.3	V	
Low level input voltage	V _{IL}	−0.3	—	0.8	V	
Operating temperature	Ta	0	—	70	°C	

Pin Descriptions

Pin name	No.	Type	Description
GND	5,8,18,24,25 32,41,46	Ground	GND pins
VDD	1,11,13,19, 28,29,42,48	Power	Power supplies pins. Nominal 3.3 V.
VDDA	36	Power	Power supply for PLL core.
GNDA	37	Power	Power supply for PLL core.
CPUT [1:0]	44,40	OUTPUT	“True” clocks of differential pair CPUCLK. These pins are HCSL outputs.
CPUC [1:0]	43,39	OUTPUT	“Complementary” clocks of differential pair CPUCLK. These pins are HCSL outputs.
SDCLK	47	OUTPUT	3.3 V Memory clock outputs.
CPU_STP#	45	INPUT	CPUCLK STOP pin. This asynchronous input halts CPU, SDRAM and AGP clocks at logic “0” level when driven low, the stop selection can be programmed through I2 C. 120 kΩ internal pulled-up.
PCI_F0	14	OUTPUT	Free running PCI clock 3.3 V output.
(*FS3)		INPUT	Latch input multi function pin for frequency select. This pin is internal pull-down to GND.
PCI_F1	15	OUTPUT	Free running PCI clock 3.3 V output.
(*FS4)		INPUT	Latch input multi function pin for frequency select. This pin is internal pull-down to GND.
PCICLK [5:0]	16,17,20,21 22,23	OUTPUT	3.3 V PCI clock outputs.
PCI_STP#	12	INPUT	PCICLK stop pin. Stops PCICLKs at logic “0” level when input low, the stop selection can be programmed through I2 C. 120 kΩ internal pulled-up.
ZCLK [1:0]	9,10	OUTPUT	Hyper Zip clock outputs.

Pin Descriptions (cont.)

Pin name	No.	Type	Description
REF0	2	OUTPUT	14.318 MHz reference clock.
(*FS0)		INPUT	Latch input multi function pin for frequency select. This pin is internal pull-down to GND.
REF1	3	OUTPUT	14.318 MHz reference clock
(*FS1)		INPUT	Latch input multi function pin for frequency select. This pin is internal pull-down to GND.
REF2	4	OUTPUT	14.318 MHz reference clock.
(*FS2)		INPUT	Latch input multi function pin for frequency select. This pin is internal pull-down to GND.
24_48 MHz	26	OUTPUT	SIO clock output. Default is 24 MHz. This pin's output frequency is able to change for 48 MHz by I2 C register.
(*MULTISEL)		INPUT	Latch input multi function pin for CPUCLK 's output current setting. This pin is internal pull-up.
AGPCLK0	31	OUTPUT	AGP clock output.
AGPCLK1	30	OUTPUT	AGP clock output.
VTT_PWRGD / PD#	33	INPUT	Power down pin. All circuits will be powered down. (Output state of each outputs are shown in page5 Table2.) Asynchronous active low input pin used to power down the device into low power state. The internal clocks are disabled and VCO and the crystal are stopped. The latency of power down will not be greater than 3 ms.
48 MHz	27	OUTPUT	3.3 V 48 MHz USB clock output.
X1	6	INPUT	XTAL input.
X2	7	OUTPUT	XTAL output.
SDATA	34	INPUT	Data input for I ² C logic. This pin is internal pull-up to VDD by 120 kΩ resistor.
SCLK	35	INPUT	Clock input for I ² C logic. This pin is internal pull-up to VDD by 120 kΩ resistor.
IREF	38	IN	A fixed resistor provides a reference current for the differential HCSL clock outputs.

Note: *FS [2:0] & MODE Input logic levels are latched an internal power-on reset. Use 10 kΩ resistor to program logic High to VDD or GND for logic low.

DC Electrical Characteristics / Serial Input Port

Ta = 0 to 70°C, VDD = 3.3 V

Item	Symbol	Min	Typ ^{*1}	Max	Unit	Test Conditions
Input Low Voltage	V _{IL}	—	—	0.8	V	
Input High Voltage	V _{IH}	2.0	—	—	V	
Input Current	I _I	-50	—	+50	μA	V _I = 0 V or 3.465 V, VDD = 3.465 V
Input capacitance	C _I	—	—	10	pF	SDATA & SCLK ^{*2}

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

2. Target of design, not 100% tested in production.

AC Electrical Characteristics / Serial Input port

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
SCLK Frequency	F _{SCLK}	—	—	100	kHz	Normal Mode	
Start Hold Time	t _{STHD}	4.0	—	—	μs		
SCLK Low Time	t _{LOW}	4.7	—	—	μs		
SCLK High Time	t _{HIGH}	4.0	—	—	μs		
Data Setup Time	t _{DSU}	250	—	—	μs		
Data Hold Time	t _{DHD}	0	—	—	ns		
Rise Time	t _r	—	—	1000	ns	SDATA & SCLK	0.8 to 2.0 V
Fall Time	t _f	—	—	300	ns	SDATA & SCLK	2.0 to 0.8 V
Stop Setup Time	t _{STSU}	4.0	—	—	μs		
BUS Free Time between Stop & Start Condition	t _{SPF}	4.7	—	—	μs		

Note: Target of design, not 100% tested in production.

DC Electrical Characteristics / SDCLK

Ta = 0 to 70°C, VDD = 3.3 V, CL = 20 pF

Item	Symbol	Min	Typ ^{*1}	Max	Unit	Test Conditions
Output voltage	V _{OH}	3.1	—	—	V	I _{OH} = −1 mA, VDD = 3.3 V
	V _{OL}	—	—	50	mV	I _{OL} = 1 mA, VDD = 3.3 V
Output Current	I _{OH}	—	—	−22	mA	V _{OH} = 2.0 V
	I _{OL}	25	—	—	mA	V _{OL} = 0.8 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / SDCLK

Ta = 0 to 70°C, VDD = 3.3 V, CL = 20 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t _{CCS}	−250	—	250	ps	133 MHz, Fig1	*1
Slew rate	t _{SL}	1.0	—	—	V / ns		0.4 to 2.4 V
Clock Duty Cycle		45	50	55	%		
SDCLK(early) to CPU Clock Skew		0	—	350	ps		*2
Output Impedance		—	30	—	Ω		

Notes: Difference of cycle time between two adjoining cycles.

- 1. Target of design, not 100% tested in production.
- 2. SDCLK Skew control register is default “0100”.

DC Electrical Characteristics / CPUCT / C HCSL Clock

Ta = 0 to 70°C, VDD = 3.3 V

Item	Symbol	Min	Typ ^{*1}	Max	Unit	Test Conditions
Output voltage	V _O	—	—	1.2	V	
Output Current	I _O	—	I (nom)	—	mA	VDD = 3.3 V ^{*2}
Output resistance		3000	—	—	Ω	V _O = 1.2 V ^{*3}

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions

2. I (nom) is output current (I_{oh}) shown in Page5 Table3.

3. Target of design, not 100% tested in production.

AC Electrical Characteristics / CPUCT / C HCSL Clock

Ta = 0 to 70°C, VDD = 3.3 V, CL = 2 pF, Rref = 475 Ω, 6xIref

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t _{CCS}	-250	—	250	ps	133MHz	^{*1}
CPU Group Skew (CPU clock out to CPU clock out)	t _{skS}	—	—	150	ps		
Rise time	t _r	175	—	700	ps	Vo =0.14 to 0.56V	
Fall time	t _f	175	—	700	ps	Vo=0.14 to 0.56V	
Clock Duty Cycle		47	50	53	%		
CPU(early) to AGP Skew		1.0	2.0	4.0	ns		
CPU(early) to PCI Skew		1.0	2.0	4.0	ns		
CPU(early) to ZCLK Skew		1.0	2.0	4.0	ns		
Cross point voltage	V _{cross}	0.45xVoh	—	0.55xVoh	V	100 / 133 MHz	

Notes: Target of design, not 100% tested in production.

1. Difference of cycle time between two adjoining cycles.

DC Electrical Characteristics / PCI Clock

Ta = 0 to 70 °C, VDD = 3.3 V, CL = 30 pF

Item	Symbol	Min	Typ ^{*1}	Max	Unit	Test Conditions
Output voltage	V _{OH}	3.1	—	—	V	I _{OH} = −1 mA, VDD = 3.3 V
	V _{OL}	—	—	50	mV	I _{OL} = 1 mA, VDD = 3.3 V
Output Current	I _{OH}	—	—	−22	mA	V _{OH} = 2.0 V
	I _{OL}	25	—	—	mA	V _{OL} = 0.8 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / PCI Clock

Ta = 0 to 70 °C, VDD = 3.3 V, CL = 30 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t _{CCS}	−250	—	250	ps	33.3 MHz, Fig1	^{*1} ,
PCI Group Skew (PCI clock out to PCI clock out)	t _{skS}	—	—	500	ps	Rising edge @ 1.5 to 1.5V Fig.2	
Slew rate	t _{SL}	1.0	—	—	V / ns		0.4 to 2.4 V
Clock Duty Cycle		45	50	55	%		
Output Impedance		—	30	—	Ω		

Notes: Target of design, not 100% tested in production.
1. Difference of cycle time between two adjoining cycles.

DC Electrical Characteristics / AGP Clock & ZCLK

Ta = 0 to 70 °C, VDD = 3.3 V, CL = 20 pF

Item	Symbol	Min	Typ ^{*1}	Max	Unit	Test Conditions
Output voltage	V _{OH}	3.1	—	—	V	I _{OH} = −1 mA, VDD = 3.3 V
	V _{OL}	—	—	50	mV	I _{OL} = 1 mA, VDD = 3.3 V
Output Current	I _{OH}	—	—	−22	mA	V _{OH} = 2.0 V
	I _{OL}	25	—	—	mA	V _{OL} = 0.8 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / AGP Clock & ZCLK

Ta=0 to 70 °C, VDD = 3.3 V, CL = 20 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t _{CCS}	−500	—	500	ps	66.6 MHz, Fig1	^{*1}
AGP Group Skew & ZCLK Group Skew	t _{skS}	—	—	175	ps	Rising edge @ 1.5 to 1.5V Fig.2	
Slew rate	t _{SL}	1.0	—	—	V / ns		0.4 to 2.4 V
Clock Duty Cycle		45	50	55	%		
Output Impedance		—	30	—	Ω		

Notes: Target of design, not 100% tested in production.
1. Difference of cycle time between two adjoining cycles.

DC Electrical Characteristics / 48 MHz, 24_48 MHz & REF Clock

Ta = 0 to 70 °C, VDD = 3.3 V, CL = 20 pF

Item	Symbol	Min	Typ ^{*1}	Max	Unit	Test Conditions
Output voltage	V _{OH}	3.1	—	—	V	I _{OH} = −1 mA, VDD = 3.3 V
	V _{OL}	—	—	50	mV	I _{OL} = 1 mA, VDD = 3.3 V
Output Current	I _{OH}	—	—	−22	mA	V _{OH} = 2.0 V
	I _{OL}	16	—	—	mA	V _{OL} = 0.8 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / 48 MHz, 24_48 MHz & REF Clock

Ta = 0 to 70 °C, VDD = 3.3 V, CL = 20 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Slew rate	t _{SL}	0.5	—	—	V / ns		0.4 to 2.4 V
Clock Duty Cycle		45	50	55	%		
Output Impedance		—	40	—	Ω		

Note: Target of design, not 100% tested in production.

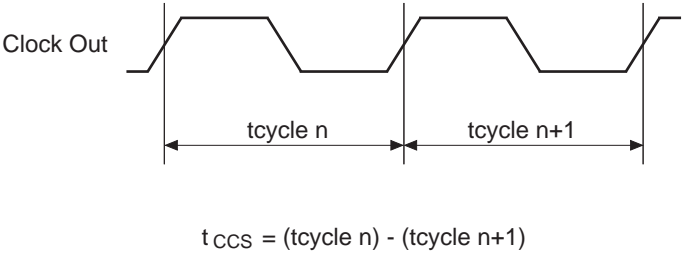


Figure1 Cycle to Cycle Jitter (3.3 V Single Ended Clock Output)

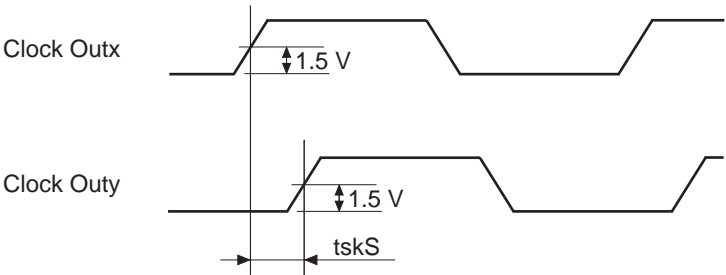


Figure2 Output Clock Skew (3.3 V Single Ended Clock Output)

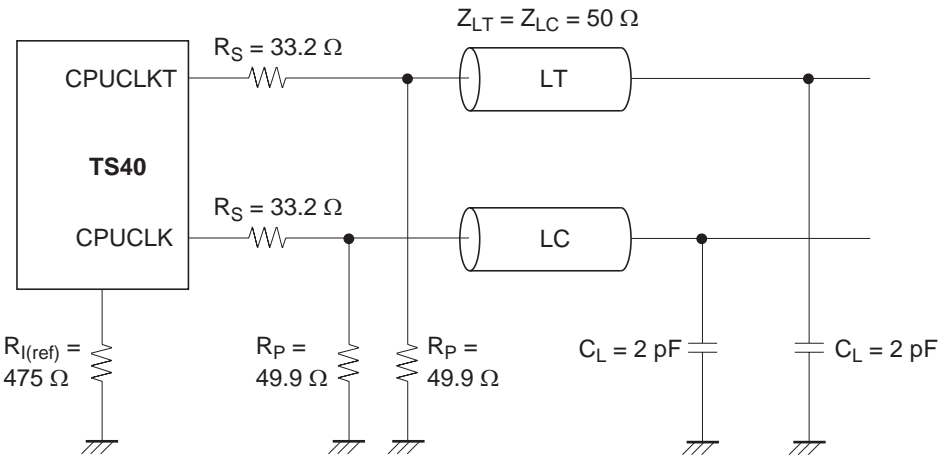
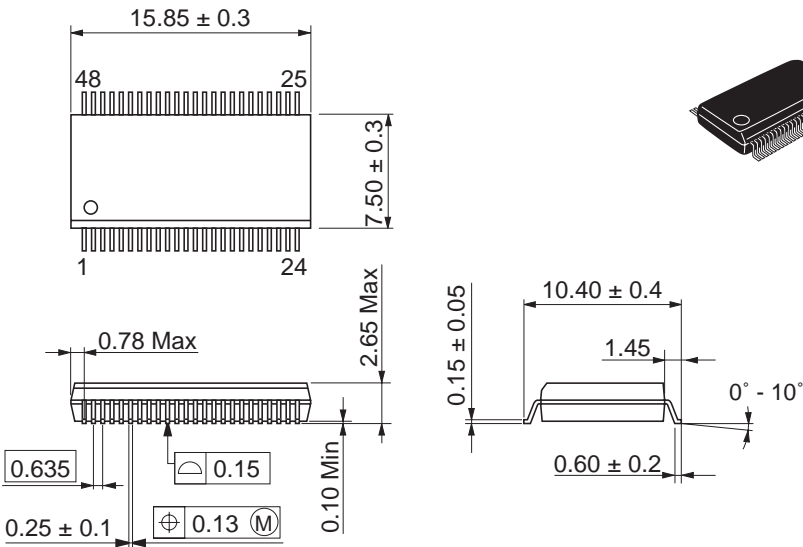


Figure3 Load Circuit for CPUCLKT / C

Package Dimensions

Unit: mm



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