

To all our customers

---

## **Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.**

---

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

## Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

---

# HD404318 Series



Rev. 6.0  
Sept. 1998

---

## Description

The HD404318 Series is 4-bit HMCS400-series microcomputer with large-capacity memory designed to increase program productivity. Each microcomputer has an A/D converter and input capture timer built in. They also come with high-voltage I/O pins that can directly drive a fluorescent display.

The HD404318 Series includes four chips: the HD404318 with 8-kword ROM; the HD404316 with 6-kword ROM; the HD404314 with 4-kword ROM; the HD4074318 with 8-kword PROM.

The HD4074318 is a PROM version ZTAT™ microcomputer. Programs can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a trademark of Hitachi Ltd.

## Features

- 34 I/O pins
  - One input-only pin
  - 33 input/output pins: 21 pins are high-voltage pins (40 V, max.)
- On-chip A/D converter (8-bit × 8-channel)
- Three timers
  - One event counter input
  - One timer output
  - One input capture timer
- 8-bit clock-synchronous serial interface (1 channel)
- Alarm output
- Built-in oscillators
  - Ceramic or crystal oscillator
  - External clock drive is also possible

---

## HD404318 Series

---

- Seven interrupt sources
  - Two by external sources
  - Three by timers
  - One each by the A/D converter and serial interface
- Two low-power dissipation modes
  - Standby mode
  - Stop mode
- Instruction cycle time 1  $\mu$ s ( $f_{osc} = 4$  MHz)

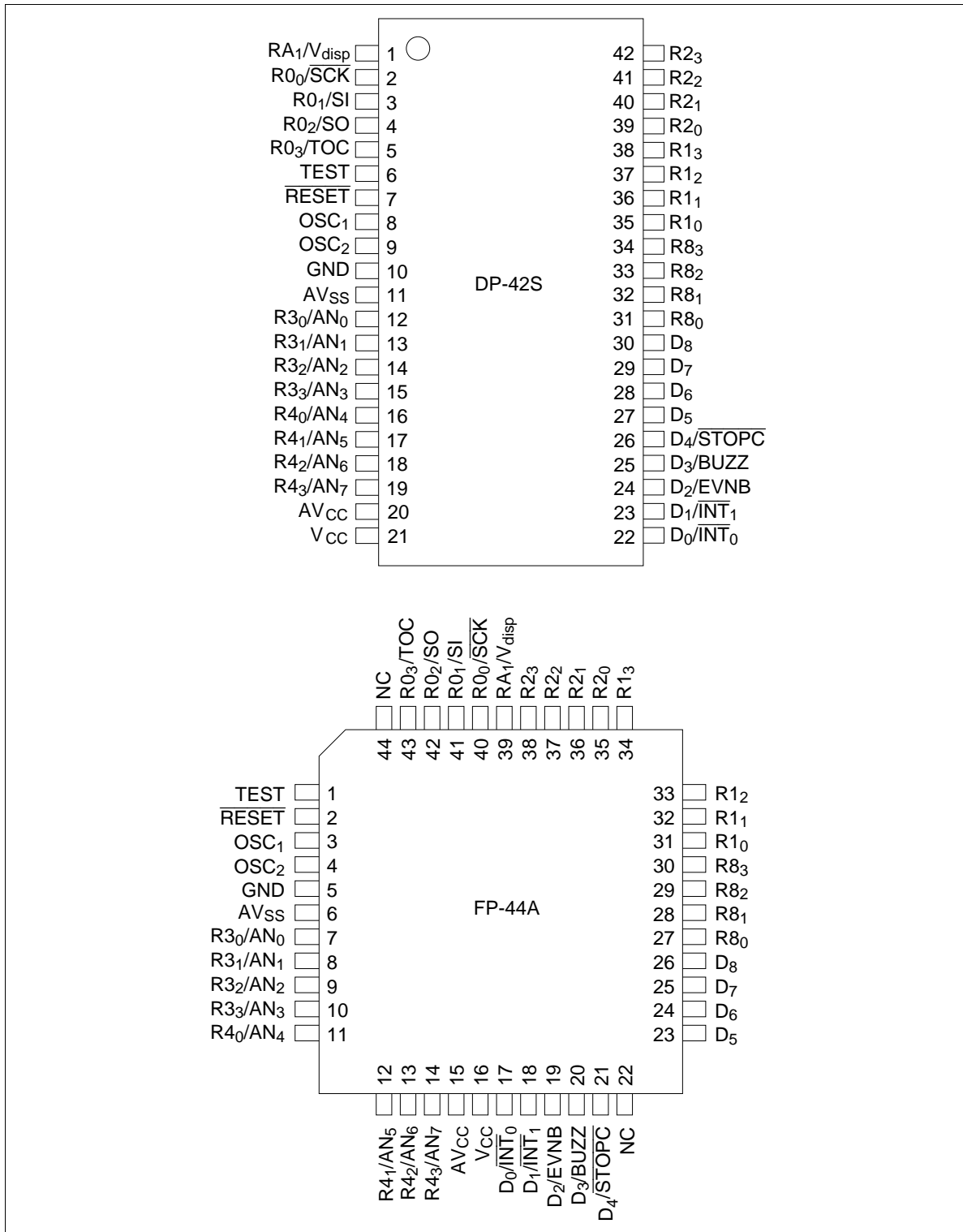
### Ordering Information

Type	Model Name	ROM (words)	RAM (digit)	Package
Mask ROM	HD404314S	4,096	384	DP-42S
	HD404314H			FP-44A
	HD404316S	6,144		DP-42S
	HD404316H			FP-44A
	HD404318S	8,192		DP-42S
	HD404318H			FP-44A
ZTAT™	HD4074318S	8,192	DP-42S	
	HD4074318H		FP-44A	

### Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacture	Model Name	Package	Manufacturer	Model Name
DATA I/O Corp.	121B	DP-42S	Hitachi	HS4318ESS01H
		FP-44A		HS4318ESH01H
AVAL Corp.	PKW-1000	DP-42S	Hitachi	HS4318ESS01H
		FP-44A		HS4318ESH01H

# Pin Arrangement



## HD404318 Series

### PinDescription

Item	Symbol	Pin Number			Function
		DP-42S	FP-44A	I/O	
Power supply	V <sub>CC</sub>	21	16		Applies power voltage
	GND	10	5		Connected to ground
	V <sub>disp</sub> (shared with RA <sub>1</sub> )	1	39		Used as a high-voltage output power supply pin when selected by the mask option
Test	TEST	6	1	I	Cannot be used in user applications. Connect this pin to GND.
Reset	RESET	7	2	I	Resets the MCU
Oscillator	OSC <sub>1</sub>	8	3	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic or crystal oscillator, or OSC <sub>1</sub> to an external oscillator circuit.
	OSC <sub>2</sub>	9	4	O	
Port	D <sub>0</sub> –D <sub>8</sub>	22–30	17–21, 23–26	I/O	Input/output pins addressed individually by bits; D <sub>0</sub> –D <sub>8</sub> are all high-voltage I/O pins. Each pin can be individually configured as selected by the mask option.
	RA <sub>1</sub>	1	39	I	One-bit high-voltage input port pin
	R0 <sub>0</sub> –R0 <sub>3</sub> , R3 <sub>0</sub> –R4 <sub>3</sub>	2–5, 12–19	40–43, 7–14	I/O	Four-bit input/output pins consisting of standard voltage pins
	R1 <sub>0</sub> –R2 <sub>3</sub> , R8 <sub>0</sub> –R8 <sub>3</sub>	31–42	27–38	I/O	Four-bit input/output pins consisting of high voltage pins
Interrupt	INT <sub>0</sub> , INT <sub>1</sub>	22, 23	17, 18	I	Input pins for external interrupts
Stop clear	STOPC	26	21	I	Input pin for transition from stop mode to active mode
Serial interface	SCK	2	40	I/O	Serial interface clock input/output pin
	SI	3	41	I	Serial interface receive data input pin
	SO	4	42	O	Serial interface transmit data output pin
Timer	TOC	5	43	O	Timer output pin
	EVNB	24	19	I	Event count input pin
Alarm	BUZZ	25	20	O	Square waveform output pin
A/D converter	AV <sub>CC</sub>	20	15		Power supply for the A/D converter. Connect this pin as close as possible to the V <sub>CC</sub> pin and at the same voltage as V <sub>CC</sub> . If the power supply voltage to be used for the A/D converter is not equal to V <sub>CC</sub> , connect a 0.1-μF bypass capacitor between the AV <sub>CC</sub> and AV <sub>SS</sub> pins. (However, this is not necessary when the AV <sub>CC</sub> pin is directly connected to the V <sub>CC</sub> pin.)
	AV <sub>SS</sub>	11	6		Ground for the A/D converter. Connect this pin as close as possible to GND at the same voltage as GND.
	AN <sub>0</sub> –AN <sub>7</sub>	12–19	7–14	I	Analog input pins for the A/D converter

**Pin Description in PROM Mode**

The HD4074318 is a PROM version of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

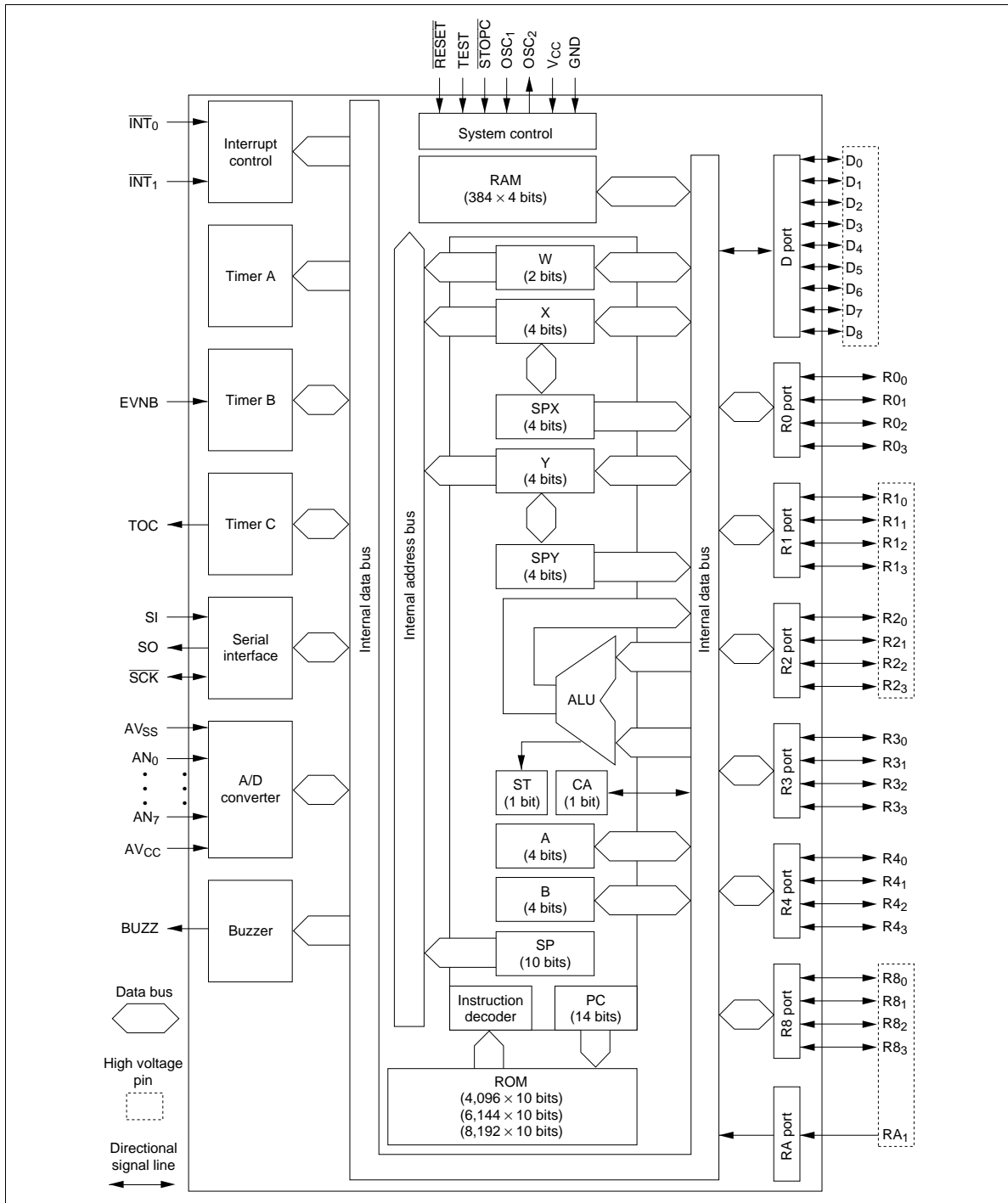
Pin Number		MCU Mode		PROM Mode	
DP-42S	FP-44A	Pin	I/O	Pin	I/O
1	39	RA <sub>1</sub> /V <sub>disp</sub>	I		
2	40	R0 <sub>0</sub> /SCK	I/O	V <sub>CC</sub>	
3	41	R0 <sub>1</sub> /SI	I/O	V <sub>CC</sub>	
4	42	R0 <sub>2</sub> /SO	I/O		
5	43	R0 <sub>3</sub> /TOC	I/O		
6	1	TEST	I	V <sub>PP</sub>	
7	2	RESET	I	RESET	I
8	3	OSC <sub>1</sub>	I	V <sub>CC</sub>	
9	4	OSC <sub>2</sub>	O		
10	5	GND		GND	
11	6	AV <sub>SS</sub>		GND	
12	7	R3 <sub>0</sub> /AN <sub>0</sub>	I/O	O <sub>0</sub>	I/O
13	8	R3 <sub>1</sub> /AN <sub>1</sub>	I/O	O <sub>1</sub>	I/O
14	9	R3 <sub>2</sub> /AN <sub>2</sub>	I/O	O <sub>2</sub>	I/O
15	10	R3 <sub>3</sub> /AN <sub>3</sub>	I/O	O <sub>3</sub>	I/O
16	11	R4 <sub>0</sub> /AN <sub>4</sub>	I/O	O <sub>4</sub>	I/O
17	12	R4 <sub>1</sub> /AN <sub>5</sub>	I/O	O <sub>5</sub>	I/O
18	13	R4 <sub>2</sub> /AN <sub>6</sub>	I/O	O <sub>6</sub>	I/O
19	14	R4 <sub>3</sub> /AN <sub>7</sub>	I/O	O <sub>7</sub>	I/O
20	15	AV <sub>CC</sub>		V <sub>CC</sub>	
21	16	V <sub>CC</sub>		V <sub>CC</sub>	
22	17	D <sub>0</sub> /INT <sub>0</sub>	I/O	M <sub>0</sub>	I
23	18	D <sub>1</sub> /INT <sub>1</sub>	I/O	M <sub>1</sub>	I
24	19	D <sub>2</sub> /EVNB	I/O	A <sub>1</sub>	I
25	20	D <sub>3</sub> /BUZZ	I/O	A <sub>2</sub>	I
26	21	D <sub>4</sub> /STOPC	I/O		
27	23	D <sub>5</sub>	I/O	A <sub>3</sub>	I
28	24	D <sub>6</sub>	I/O	A <sub>4</sub>	I
29	25	D <sub>7</sub>	I/O	A <sub>9</sub>	I
30	26	D <sub>8</sub>	I/O	V <sub>CC</sub>	

## HD404318 Series

Pin Number		MCU Mode		PROM Mode	
DP-42S	FP-44A	Pin	I/O	Pin	I/O
31	27	R8 <sub>0</sub>	I/O	$\overline{\text{CE}}$	I
32	28	R8 <sub>1</sub>	I/O	$\overline{\text{OE}}$	I
33	29	R8 <sub>2</sub>	I/O	A <sub>13</sub>	I
34	30	R8 <sub>3</sub>	I/O	A <sub>14</sub>	I
35	31	R1 <sub>0</sub>	I/O	A <sub>5</sub>	I
36	32	R1 <sub>1</sub>	I/O	A <sub>6</sub>	I
37	33	R1 <sub>2</sub>	I/O	A <sub>7</sub>	I
38	34	R1 <sub>3</sub>	I/O	A <sub>8</sub>	I
39	35	R2 <sub>0</sub>	I/O	A <sub>0</sub>	I
40	36	R2 <sub>1</sub>	I/O	A <sub>10</sub>	I
41	37	R2 <sub>2</sub>	I/O	A <sub>11</sub>	I
42	38	R2 <sub>3</sub>	I/O	A <sub>12</sub>	I

I/O: Input/output pin; I: Input pin; O: Output pin

# Block Diagram



## HD404318 Series

### Memory Map

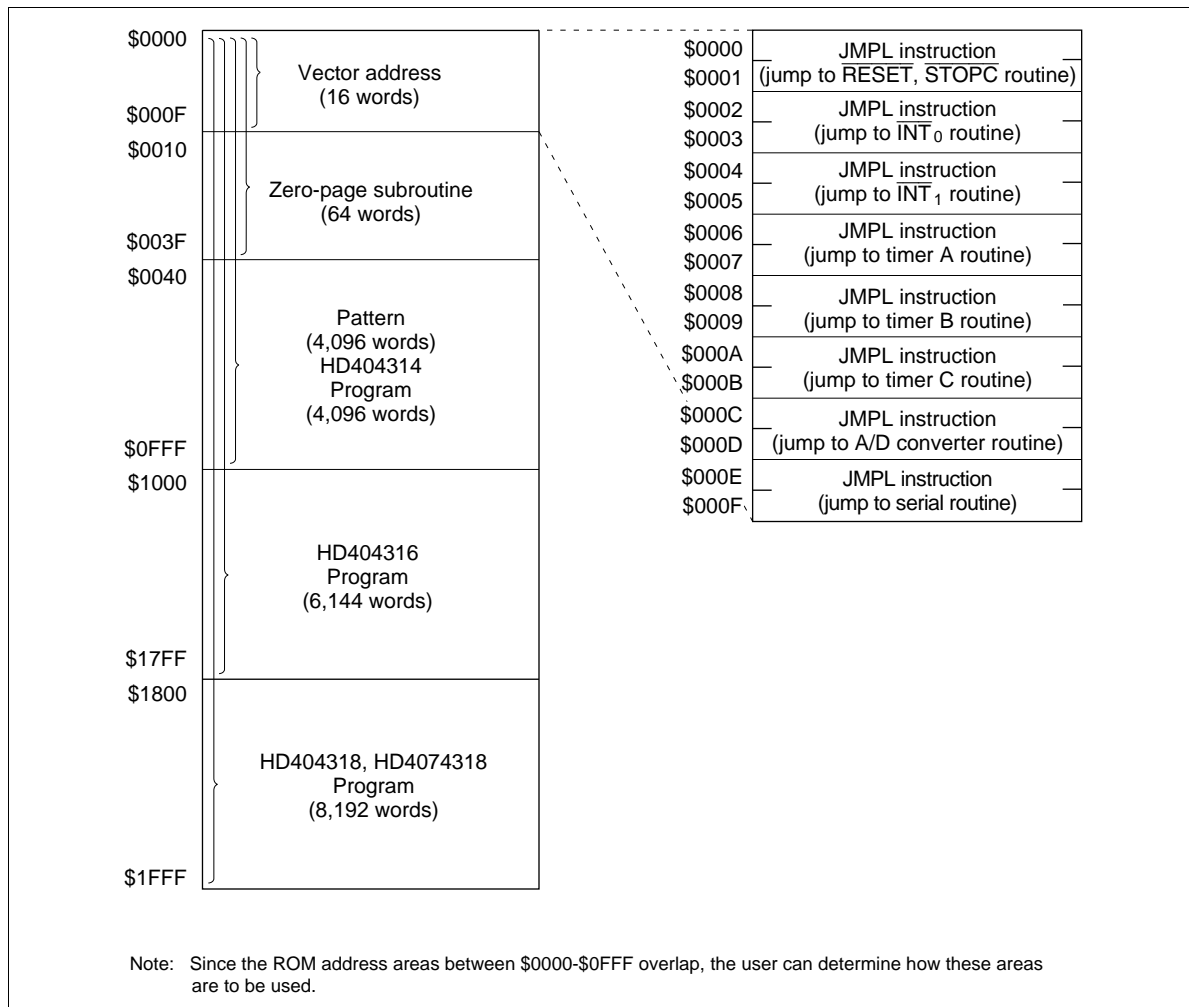
#### ROM Memory Map

**Vector Address Area (\$0000–\$000F):** Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines.

**Zero-Page Subroutine Area (\$0000–\$003F):** Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

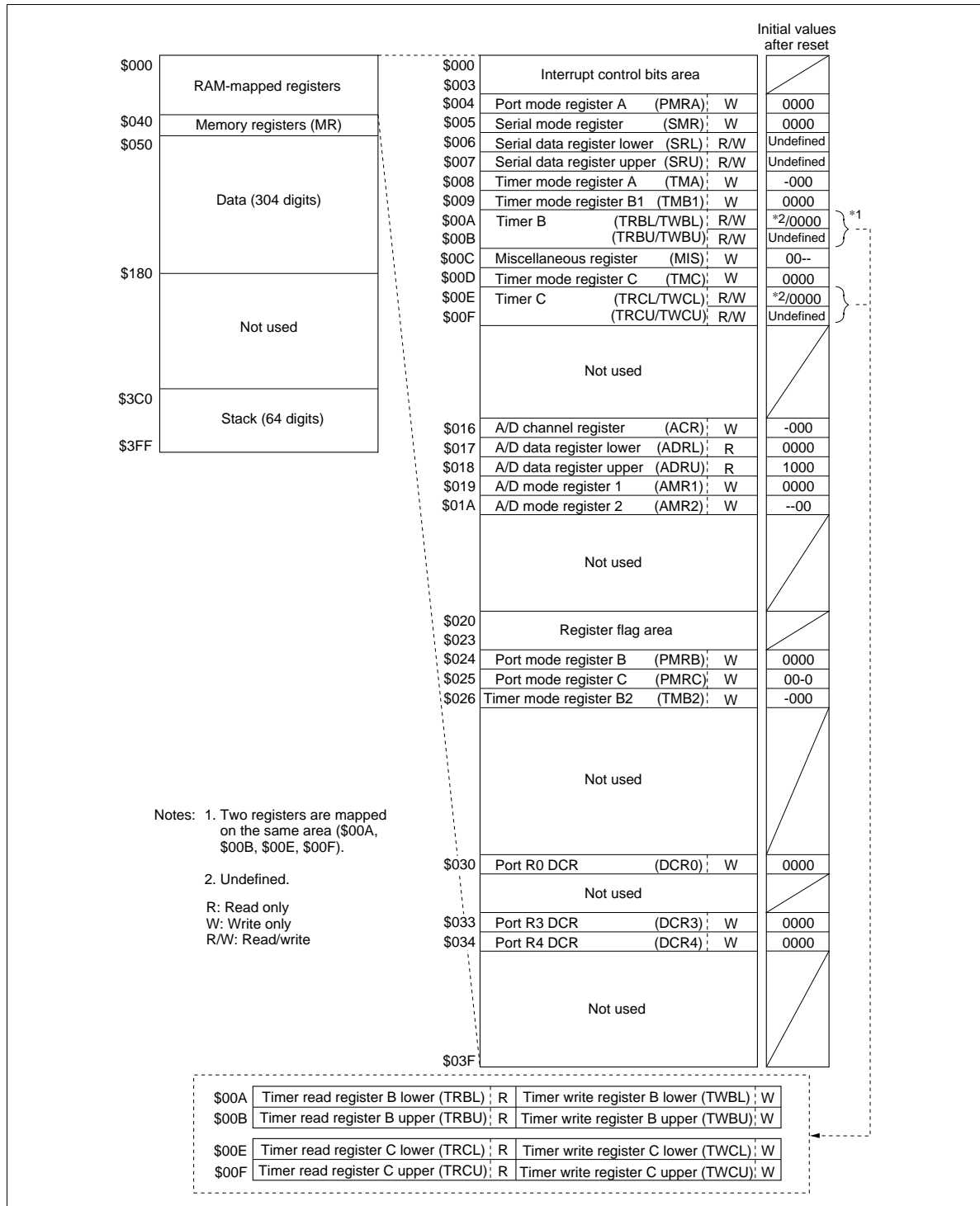
**Pattern Area (\$0000–\$0FFF):** Contains ROM data that can be referenced with the P instruction.

**Program Area (\$0000–\$0FFF (HD404314), \$0000–\$17FF (HD404316), \$0000–\$1FFF (HD404318, HD4074318)):** The entire ROM area can be used for program coding.



**Figure 1 ROM Memory Map**

## RAM Memory Map



**Figure 2 RAM Memory Map and Initial Values**

## HD404318 Series

**Table 1 Initial Values of Flags after MCU Reset**

Item		Initial Value
Interrupt flags/mask	Interrupt enable flag (IE)	0
	Interrupt request flag (IF)	0
	Interrupt mask (IM)	1
Bit registers	Watchdog timer on flag (WDON)	0
	A/D start flag (ADSF)	0
	Input capture status flag (ICSF)	0
	Input capture error flag (ICEF)	0
	I <sub>AD</sub> off flag (IAOF)	0
	RAM enable flag (RAME)	0

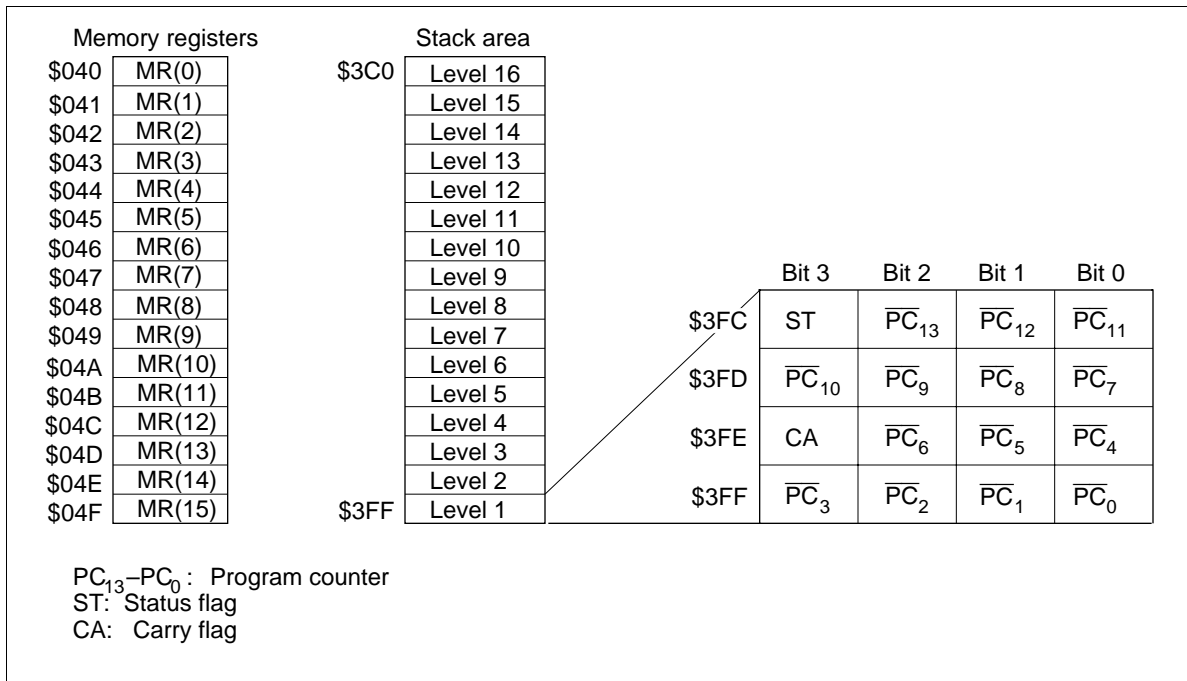
RAM Address		Bit 3	Bit 2	Bit 1	Bit 0
	\$0000	IM0 (IM of $\overline{\text{INT}}_0$ )	IF0 (IF of $\overline{\text{INT}}_0$ )	RSP (Reset SP bit)	IE (Interrupt enable flag)
	\$0001	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{\text{INT}}_1$ )	IF1 (IF of $\overline{\text{INT}}_1$ )
	\$0002	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)
	\$0003	IMS (IM of serial)	IFS (IF of serial)	IMAD (IM of A/D)	IFAD (IF of A/D)
Interrupt control bits area					
		Bit 3	Bit 2	Bit 1	Bit 0
	\$020	Not used	ADSF (A/D start flag)	WDON (Watchdog on flag)	Not used
	\$021	RAME (RAM enable flag)	IAOF (I <sub>AD</sub> off flag)	ICEF (Input capture error flag)	ICSF (Input capture status flag)
IF: Interrupt request flag IM: Interrupt mask IE: Interrupt enable flag SP: Stack pointer	\$022	Not used			
	\$023				
Register flag area					

**Figure 3 Interrupt Control Bits and Register Flag Areas Configuration**

	SEM/SEMD	REM/REMD	TM/TMD
IE	Allowed	Allowed	Allowed
IM			
IAOF			
IF	Not executed	Allowed	Allowed
ICSF			
ICEF			
RAME			
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
ADSF	Allowed	Inhibited	Allowed
Not used	Not executed	Not executed	Inhibited

Note: WDON is reset by MCU reset or by  $\overline{\text{STOPC}}$  enable for stop mode cancellation. The REM or REMD instruction must not be executed for ADSF during A/D conversion. If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

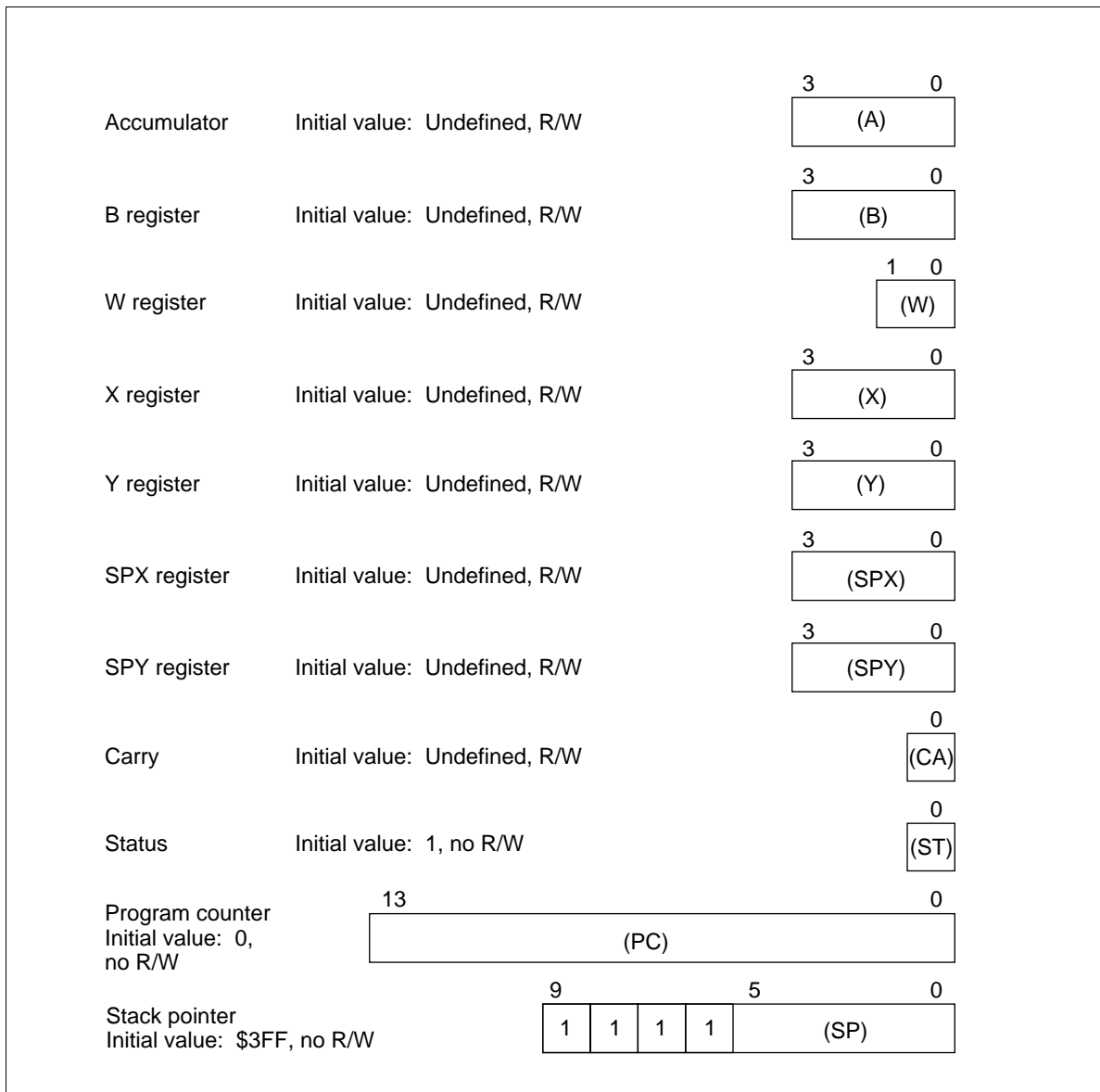
**Figure 4 Usage Limitations of RAM Bit Manipulation Instructions**



**Figure 5 Configuration of Memory Registers and Stack Area, and Stack Position**

## HD404318 Series

### Registers and Flags



**Figure 6 Registers and Flags**

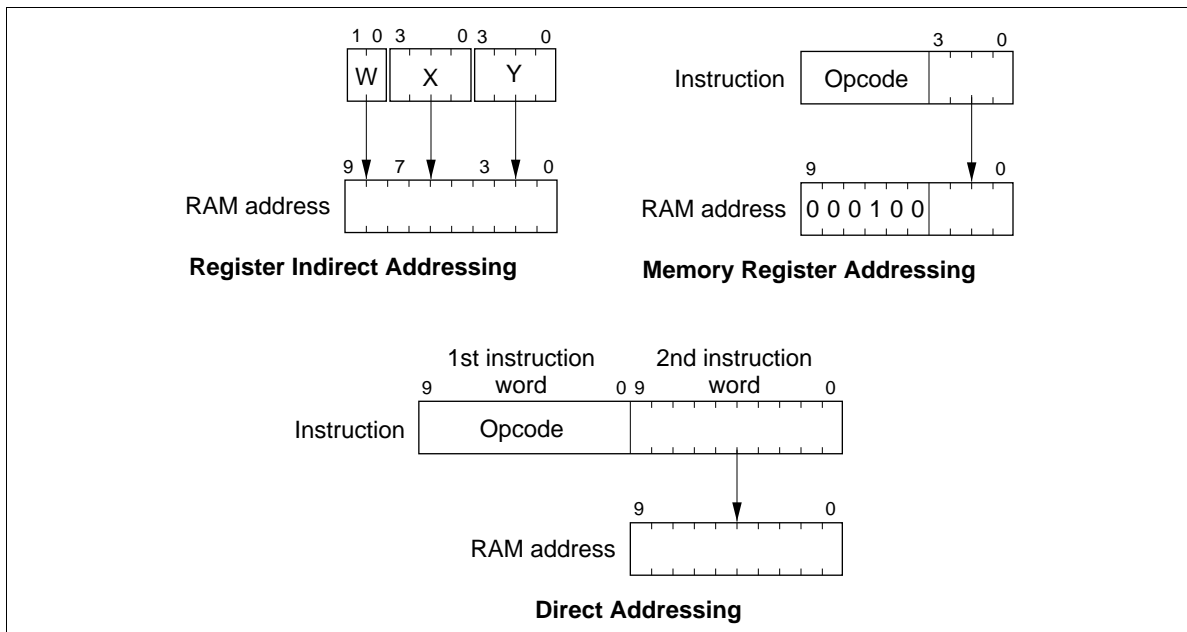
## Addressing Modes

### RAM Addressing Modes

**Register Indirect Addressing Mode:** The contents of the W, X, and Y registers (10 bits total) are used as a RAM address.

**Direct Addressing Mode:** A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

**Memory Register Addressing Mode (LAMR, XMRA):** The memory registers (MR), which are located in 16 addresses from \$040 to \$04F, are accessed with the LAMR and XMRA instructions.



**Figure 7 RAM Addressing Modes**

---

## HD404318 Series

---

### ROM Addressing Modes

**Direct Addressing Mode:** A program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction.

**Current Page Addressing Mode:** A program can branch to any address in the current page (256 words per page) by executing the BR instruction.

**Zero-Page Addressing Mode:** A program can branch to any subroutine located in the zero-page subroutine area (\$0000–\$003F) by executing the CAL instruction.

**Table Data Addressing Mode:** A program can branch to an address determined by the contents of 4-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

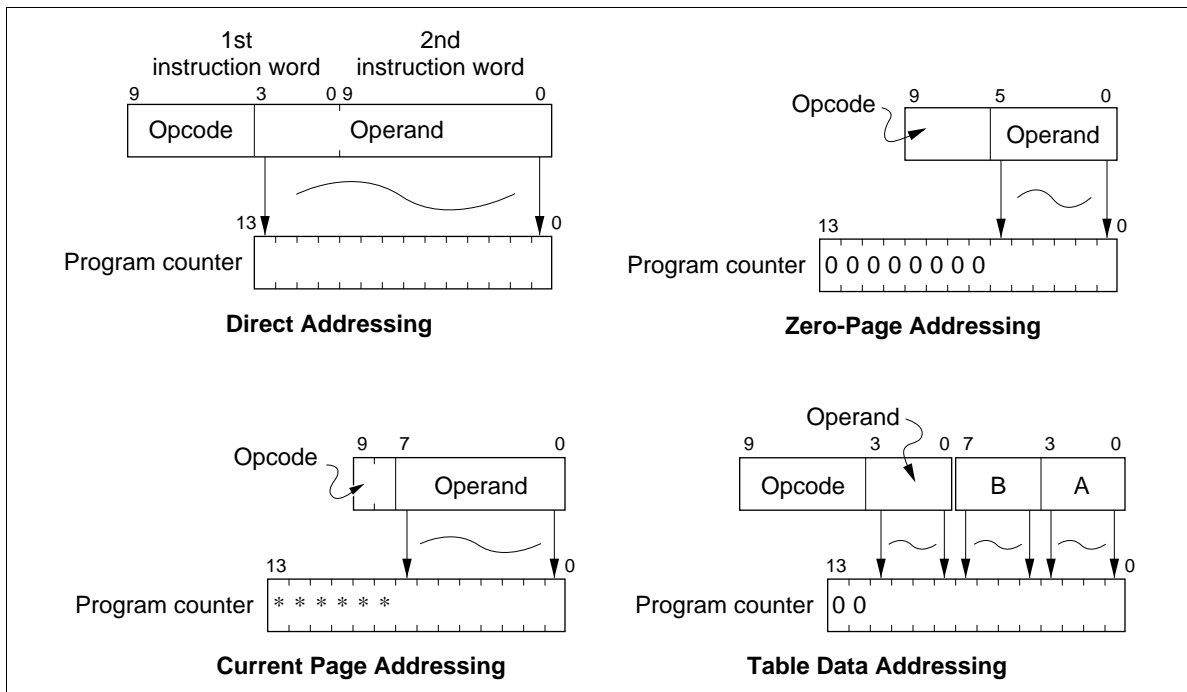
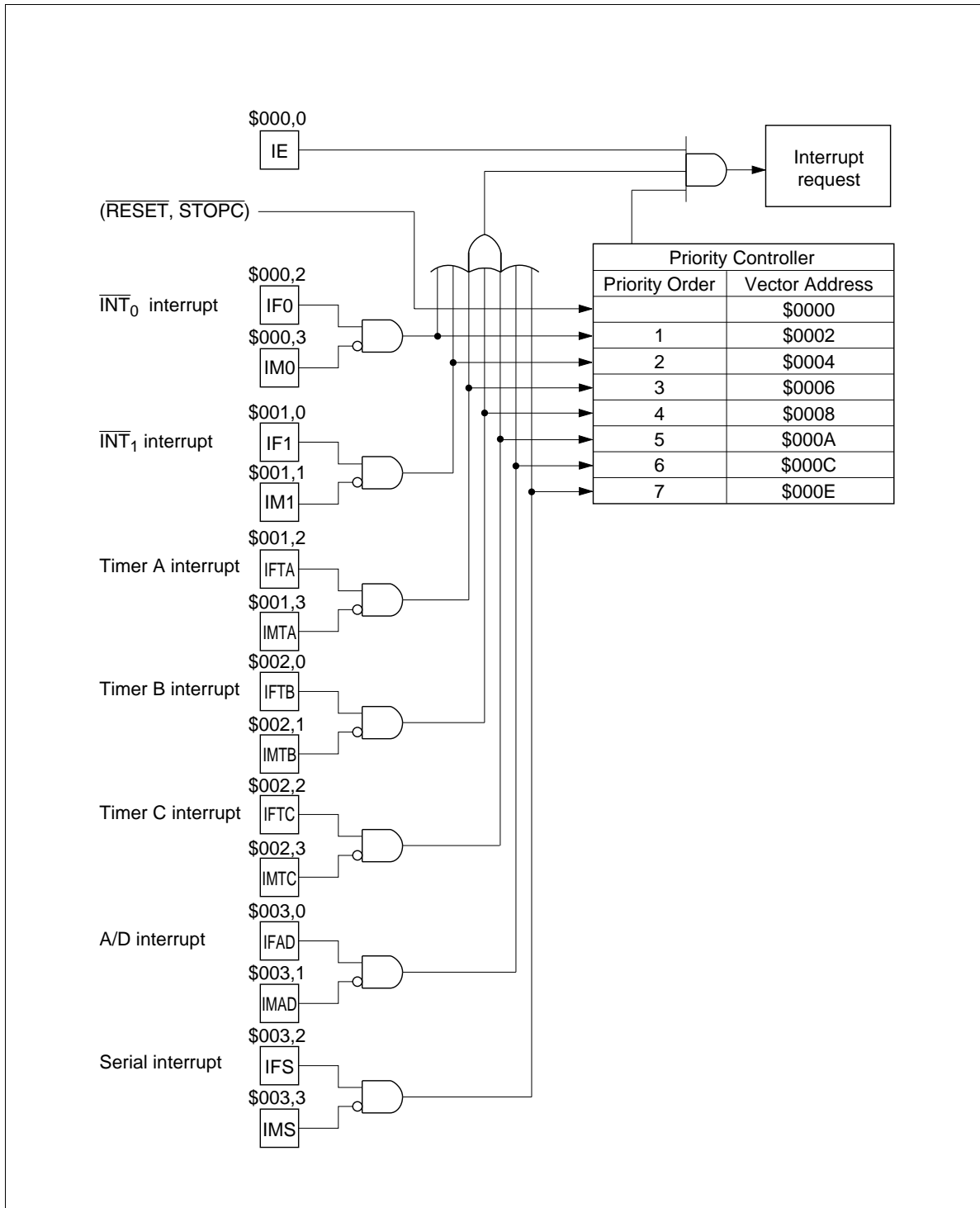


Figure 8 ROM Addressing Modes

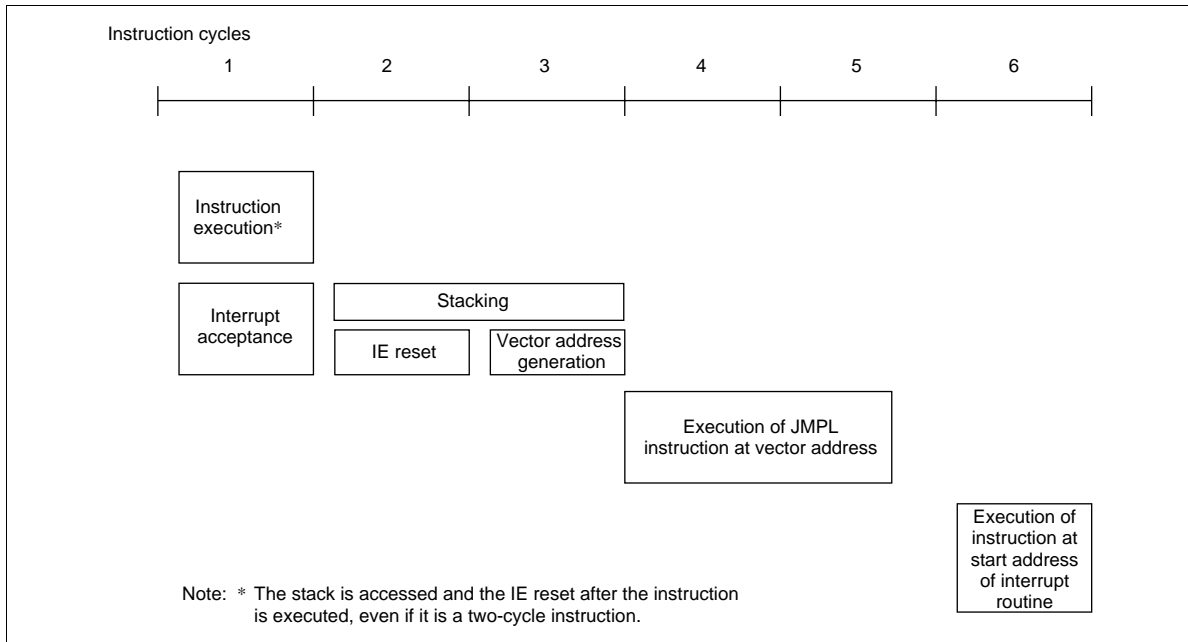
**Table 2      Instruction Set Classification**

<b>Instruction Type</b>	<b>Function</b>	<b>Number of Instructions</b>
Immediate	Transferring constants to the accumulator, B register, and RAM.	4
Register-to-register	Transferring contents of the B, Y, SPX, SPY, or memory registers to the accumulator	8
RAM addressing	Available when accessing RAM in register indirect addressing mode	13
RAM register	Transferring data between the accumulator and memory.	10
Arithmetic	Performing arithmetic operations with the contents of the accumulator, B register, or memory.	25
Compare	Comparing contents of the accumulator or memory with a constant	12
RAM bit manipulation	Bit set, bit reset, and bit test.	6
ROM addressing	Branching and jump instructions based on the status condition.	8
Input/output	Controlling the input/output of the R and D ports; ROM data reference with the P instruction	11
Control	Controlling the serial communication interface and low-power dissipation modes.	4
		Total: 101 instructions

## Interrupts



**Figure 9 Interrupt Control Circuit**



**Figure 10 Interrupt Processing Sequence**

---

## HD404318 Series

---

### Operating Modes

The MCU has three operating modes as shown in table 3. Transitions between operating modes are shown in figure 11.

**Table 3      Operations in Each Operating Mode**

Function	Active Mode	Standby Mode	Stop Mode
System oscillator	OP	OP	Stopped
CPU	OP	Retained	Reset
RAM	OP	Retained	Retained
Timer A	OP	OP	Reset
Timers B, C	OP	OP	Reset
Serial interface	OP	OP	Reset
A/D	OP	OP	Reset
I/O	OP	Retained	Reset

Note: OP implies in operation

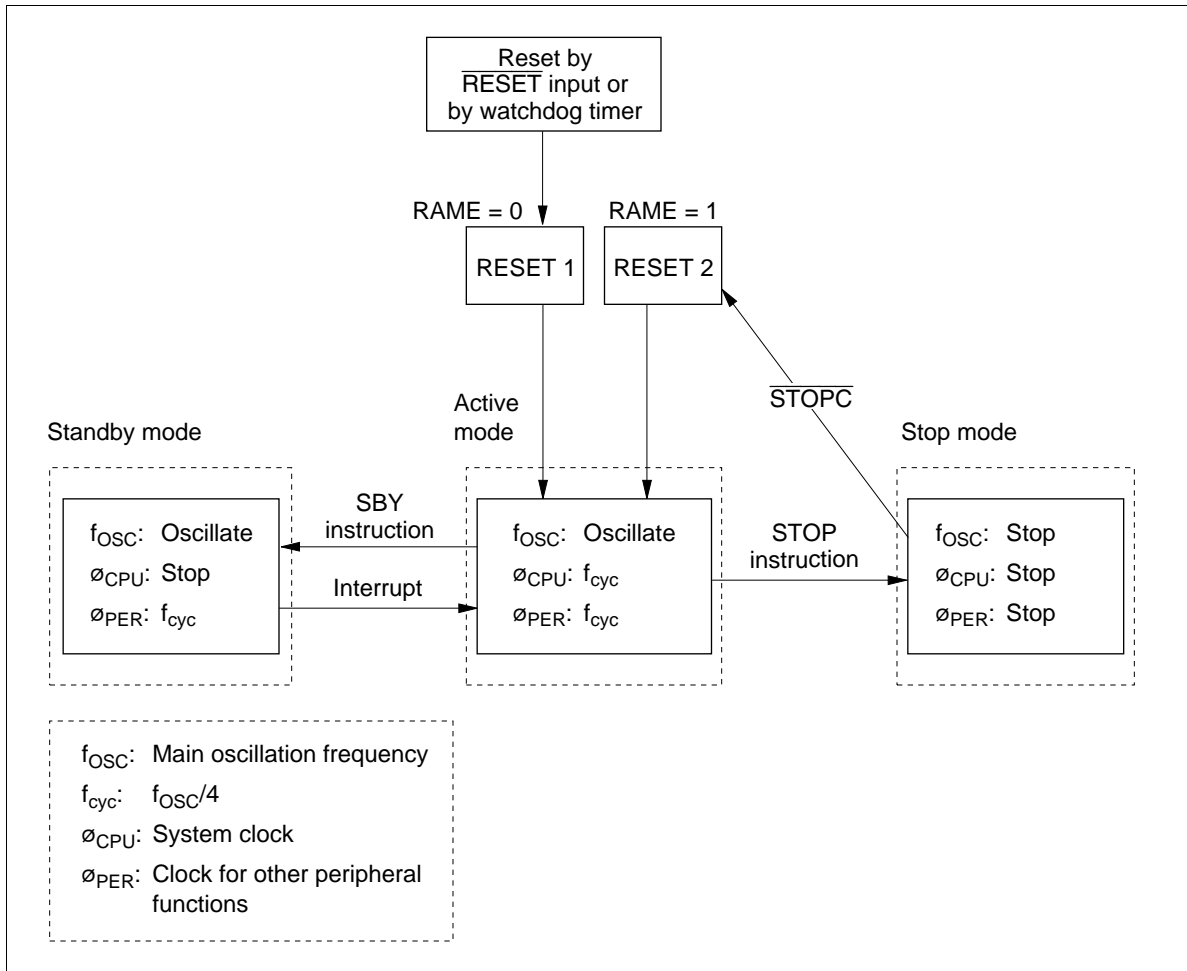


Figure 11 MCU Status Transitions

In stop mode, the system oscillator is stopped. To ensure a proper oscillation stabilization period of at least  $t_{\text{RC}}$  when clearing stop mode, execute the cancellation according to the timing chart in figure 12.

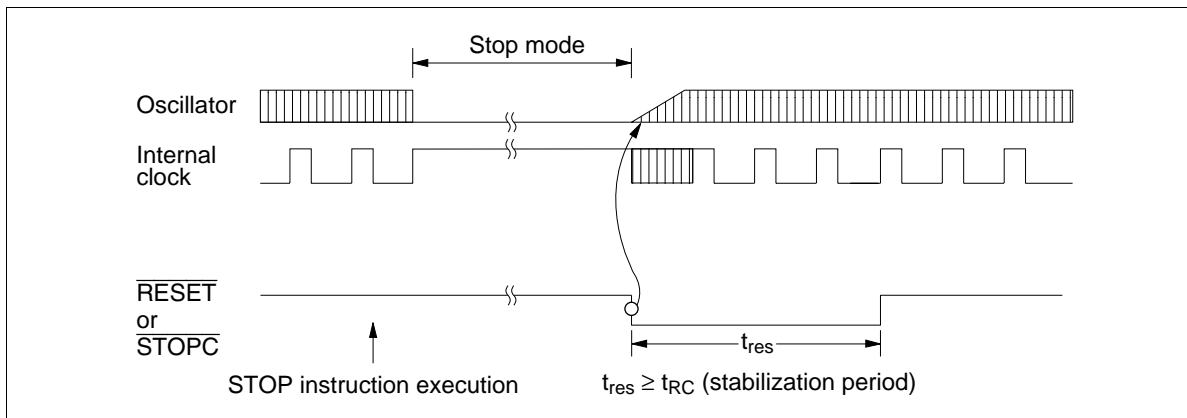
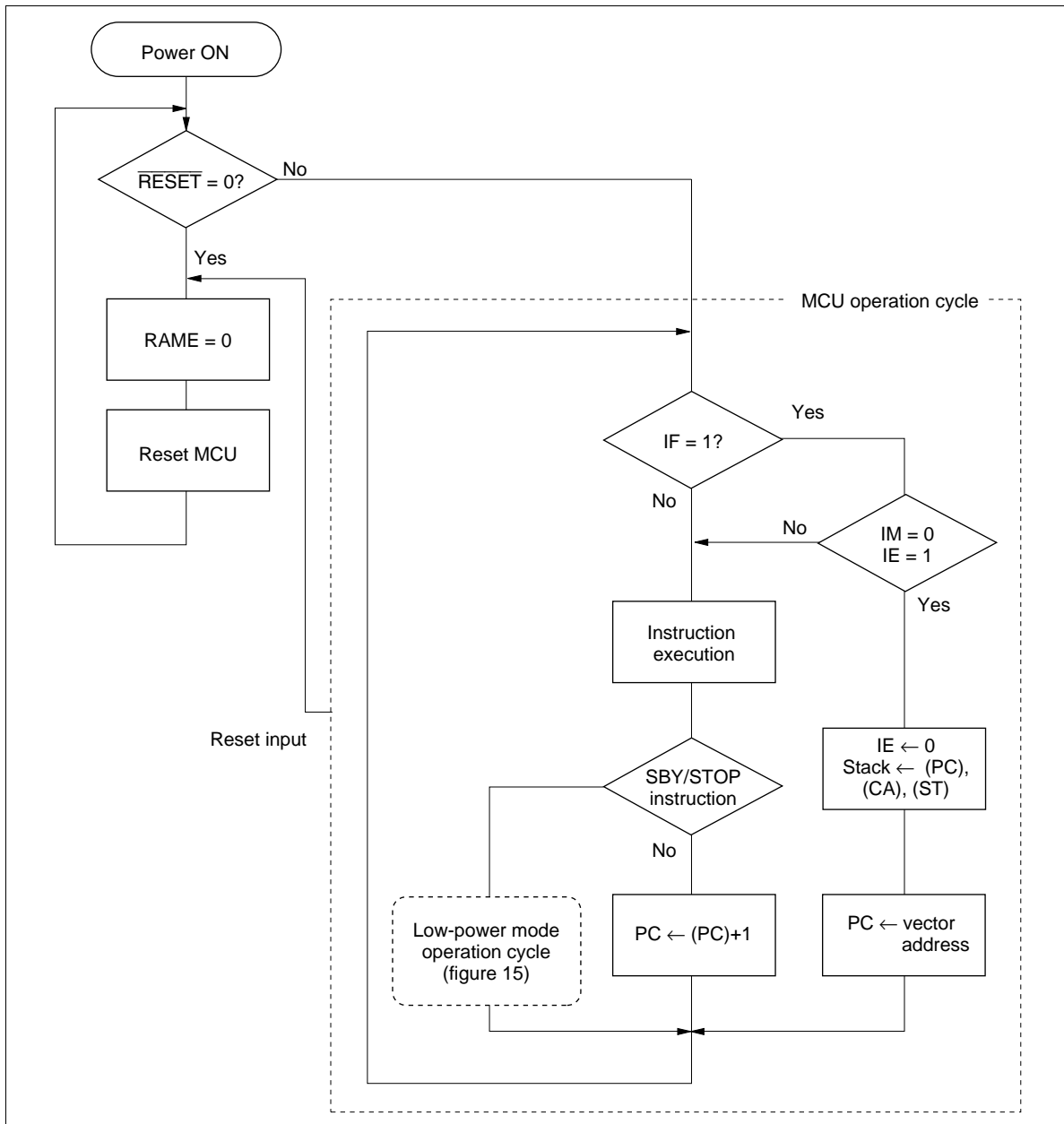


Figure 12 Timing of Stop Mode Cancellation

## HD404318 Series

**MCU Operation Sequence:** The MCU operates in the sequence shown in figure 13 and figure 14. The low-power mode operation sequence is shown in figure 14. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.



**Figure 13 MCU Operating Sequence (Power ON)**

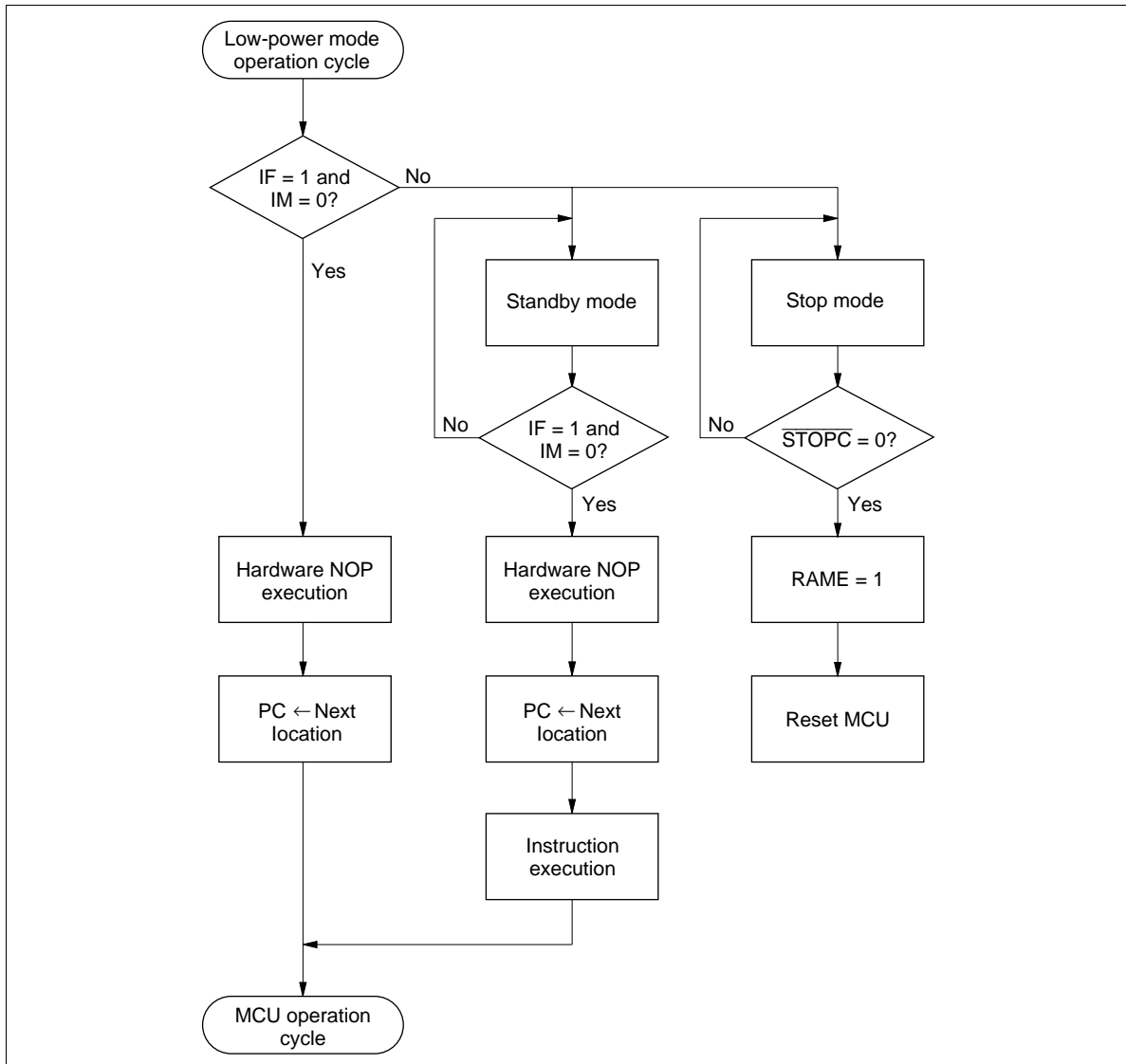
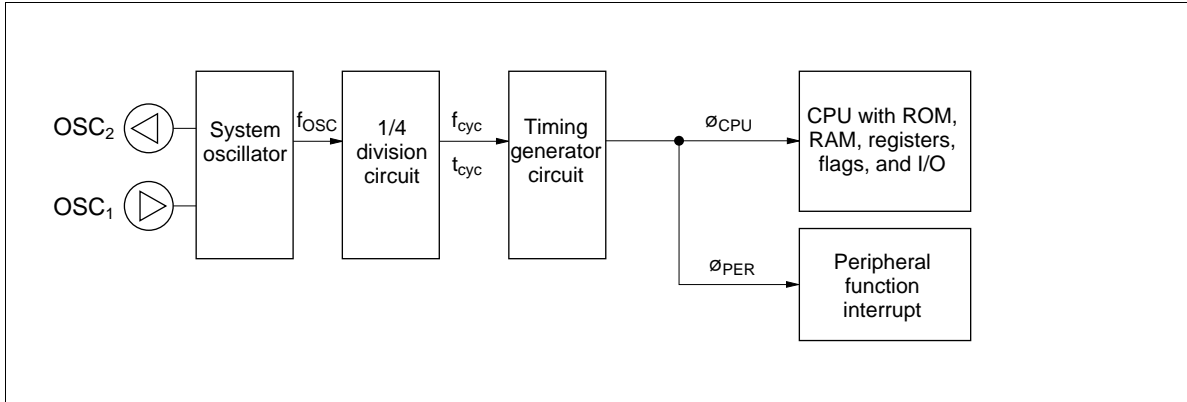


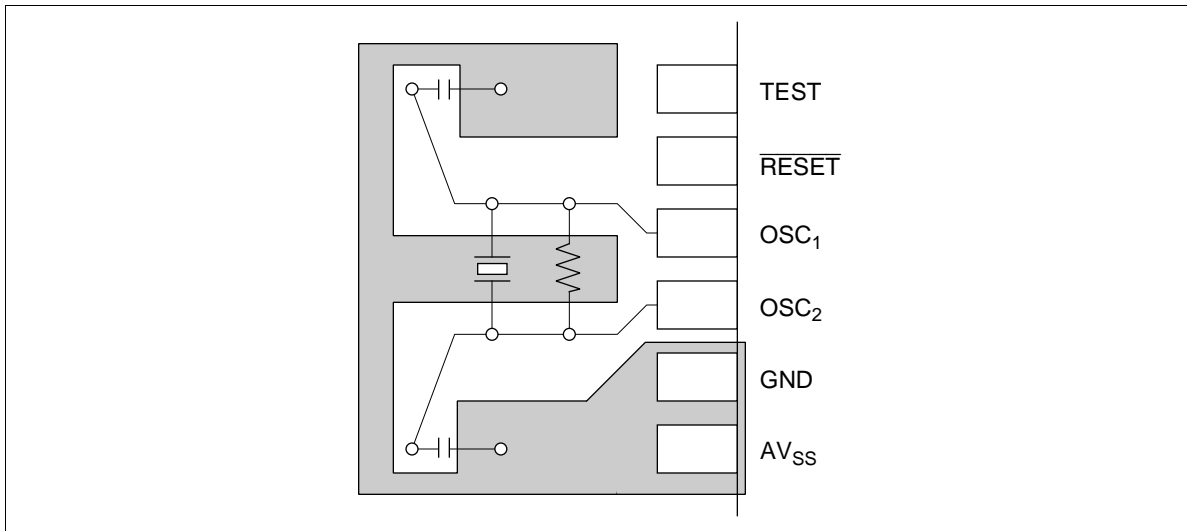
Figure 14 MCU Operating Sequence (Low-Power Mode Operation)

### Oscillator Circuit

Figure 15 shows a block diagram of the clock generation circuit.

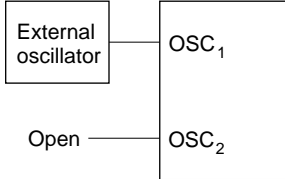
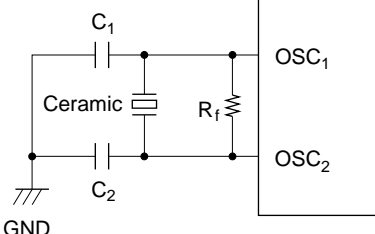
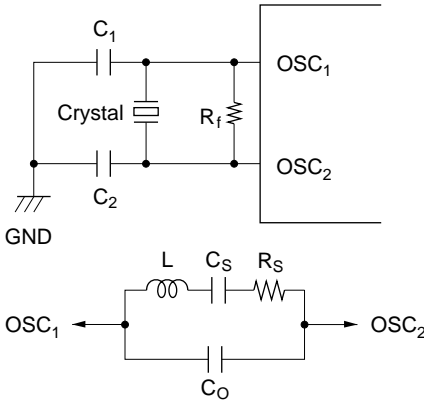


**Figure 15 Clock Generation Circuit**



**Figure 16 Typical Layout of Crystal and Ceramic Oscillator**

**Table 4 Oscillator Circuit Examples**

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC <sub>1</sub> , OSC <sub>2</sub> )		Ceramic oscillator: CSA4.00MG (Murata) $R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 30\text{ pF} \pm 20\%$
Crystal oscillator (OSC <sub>1</sub> , OSC <sub>2</sub> )		$R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 10\text{ to }22\text{ pF} \pm 20\%$ Crystal: Equivalent to circuit shown below $C_0 = 7\text{ pF max.}$ $R_s = 100\text{ }\Omega\text{ max.}$

- Notes:
1. Since the circuit constants change depending on the crystal or ceramic oscillator and stray capacitance of the board, the user should consult with the crystal or ceramic oscillator manufacturer to determine the circuit parameters.
  2. Wiring among OSC<sub>1</sub>, OSC<sub>2</sub>, and elements should be as short as possible, and must not cross other wiring (see figure 16).

## HD404318 Series

### I/O Ports

The MCU has 33 input/output pins ( $D_0$ – $D_8$ ,  $R_0$ – $R_4$ ,  $R_8$ ) and one input-only pin ( $RA_1$ ). The following describes the features of the I/O ports.

- The 21 pins consisting of  $D_0$ – $D_8$ ,  $R_1$ ,  $R_2$ , and  $R_8$  are all high-voltage I/O pins.  $RA_1$  is a high-voltage input-only pin. These high-voltage pins can be equipped with or without pull-down resistance, as selected by the mask option.
- All standard output pins are CMOS output pins. However, the  $R_0$ / $SO$  pin can be programmed for NMOS open-drain output.
- In stop mode, input/output pins go to the high-impedance state
- All standard input/output pins have pull-up MOS built in, which can be individually turned on or off by software

**Table 5 Control of Standard I/O Pins by Program**

MIS3 (bit 3 of MIS)		0		1		1	
DCR		0		1		0	
PDR		0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—
	NMOS	—	—	On	—	—	On
Pull-up MOS		—	—	—	—	On	On

Note: — indicates off.

**Data control register (DCR0: \$030, DCR3: \$033, DCR4: \$034)**

**DCR0, DCR3,  
DCR4**

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCR03, DCR33, DCR43,	DCR02, DCR32, DCR42,	DCR01, DCR31, DCR41,	DCR00, DCR30, DCR40

Bits 0 to 3	CMOS Buffer Control
0	CMOS buffer off (high impedance)
1	CMOS buffer on

Correspondence between ports and DCR bits

Register	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R_{03}$	$R_{02}$	$R_{01}$	$R_{00}$
DCR3	$R_{33}$	$R_{32}$	$R_{31}$	$R_{30}$
DCR4	$R_{43}$	$R_{42}$	$R_{41}$	$R_{40}$

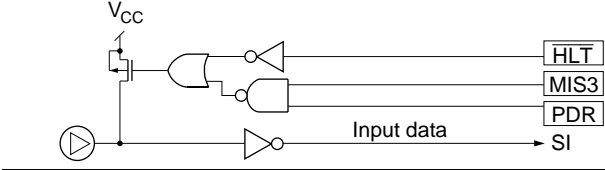
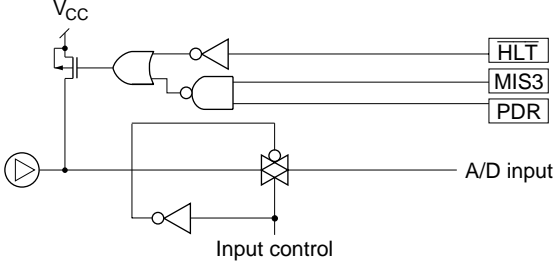
**Figure 17 Data Control Register (DCR)**

**Table 6** Circuit Configurations of Standard I/O Pins

I/O Pin Type	Circuit	Pins
Input/output pins		$R0_0, R0_1, R0_3$ $R3_0-R3_3,$ $R4_0-R4_3$
		$R0_2$
Peripheral function pins		SCK
Output pins		SO
		TOC

Notes on next page.

## HD404318 Series

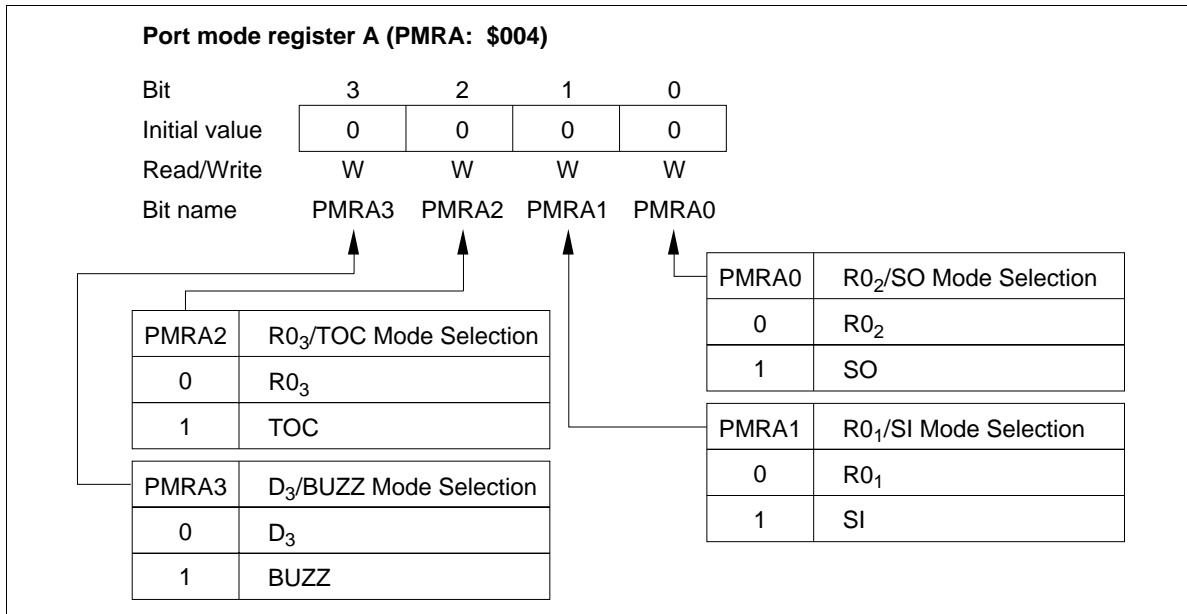
I/O Pin Type		Circuit	Pins
Peripheral function pins	Input/ pins		SI
			AN <sub>0</sub> –AN <sub>7</sub>

- Notes:
1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The  $\overline{\text{HLT}}$  signal goes low, and input/output pins the enter high-impedance state.
  2. The  $\overline{\text{HLT}}$  signal is 1 in active and standby modes.

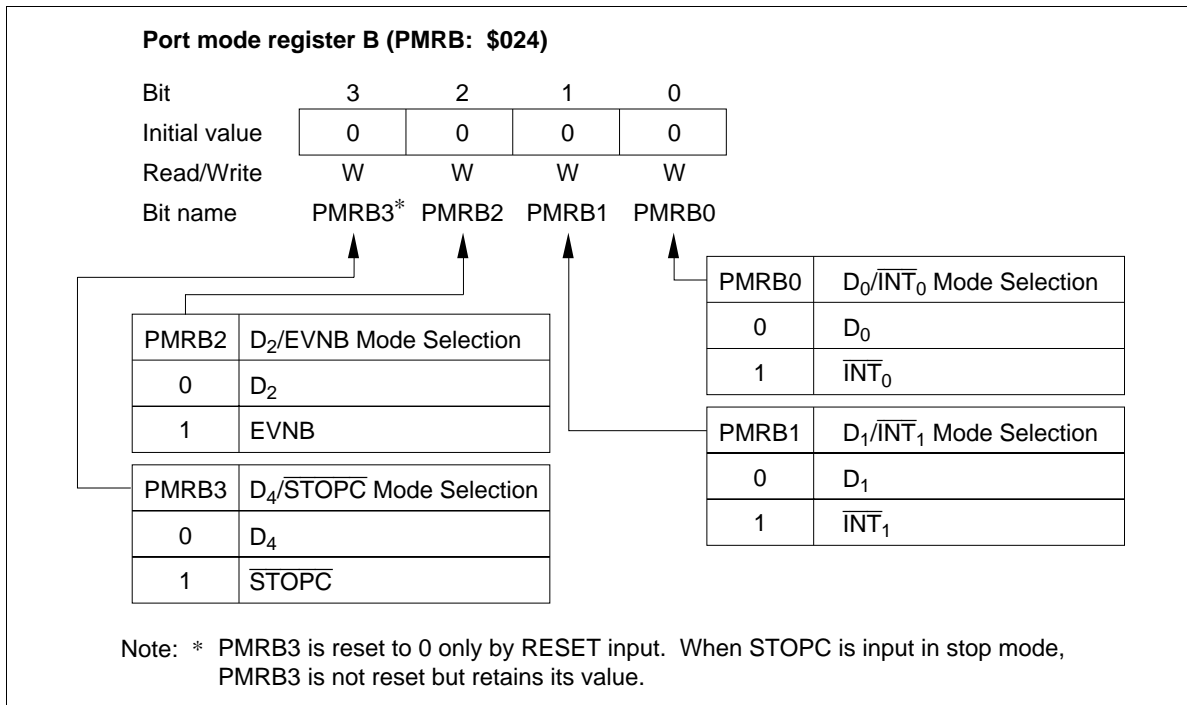
**Table 7** Circuit Configurations for High-Voltage Input/Output Pins

I/O Pin Type	With Pull-Down Resistance	Without Pull-Down Resistance	Pins
Input/output pins			$D_0-D_8$ , $R1_0-R1_3$ , $R2_0-R2_3$ , $R8_0-R8_3$
Input pins			$RA_1$
Peripheral function pins			BUZZ
Input pins			$\overline{INT}_0$ , $\overline{INT}_1$ , $\overline{EVNB}$ , $\overline{STOPC}$

- Notes:
1. In stop mode, the MCU is reset and the peripheral function selection is cancelled. The  $\overline{HLT}$  signal goes low, and input/output pins the enter high-impedance state.
  2. The  $\overline{HLT}$  signal is 1 in active and standby modes.
  3. The circuits of HD4074318 are without pull-down resistance.



**Figure 18 Port Mode Register A (PMRA)**



**Figure 19 Port Mode Register B (PMRB)**

**Miscellaneous register (MIS: \$00C)**

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	W	W	—	—
Bit name	MIS3	MIS2	Not used	Not used

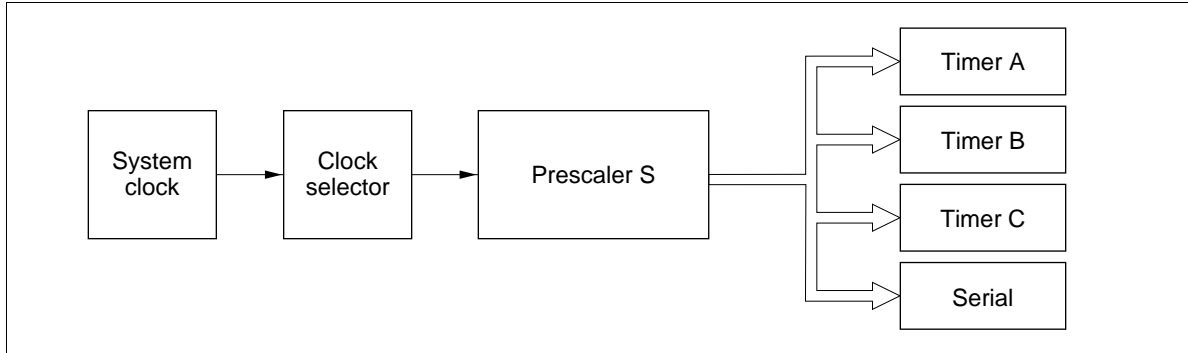
MIS3	Pull-Up MOS On/Off Selection	MIS2	CMOS Buffer On/Off Selection for Pin R0 <sub>2</sub> /SO
0	Pull-up MOS off	0	CMOS on
1	Pull-up MOS on (refer to table 5)	1	CMOS off

Note: The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

**Figure 20 Miscellaneous Register (MIS)**

### **Prescaler**

The MCU has a built-in prescaler labeled as prescaler S (PSS), which divides the system clock and then outputs divided clock signals to the peripheral function modules, as shown in figure21.



**Figure 21 Prescaler Output Supply**

## Timers

The MCU has three built-in timers: A, B, and C. The functions of each timer are listed in table 7.

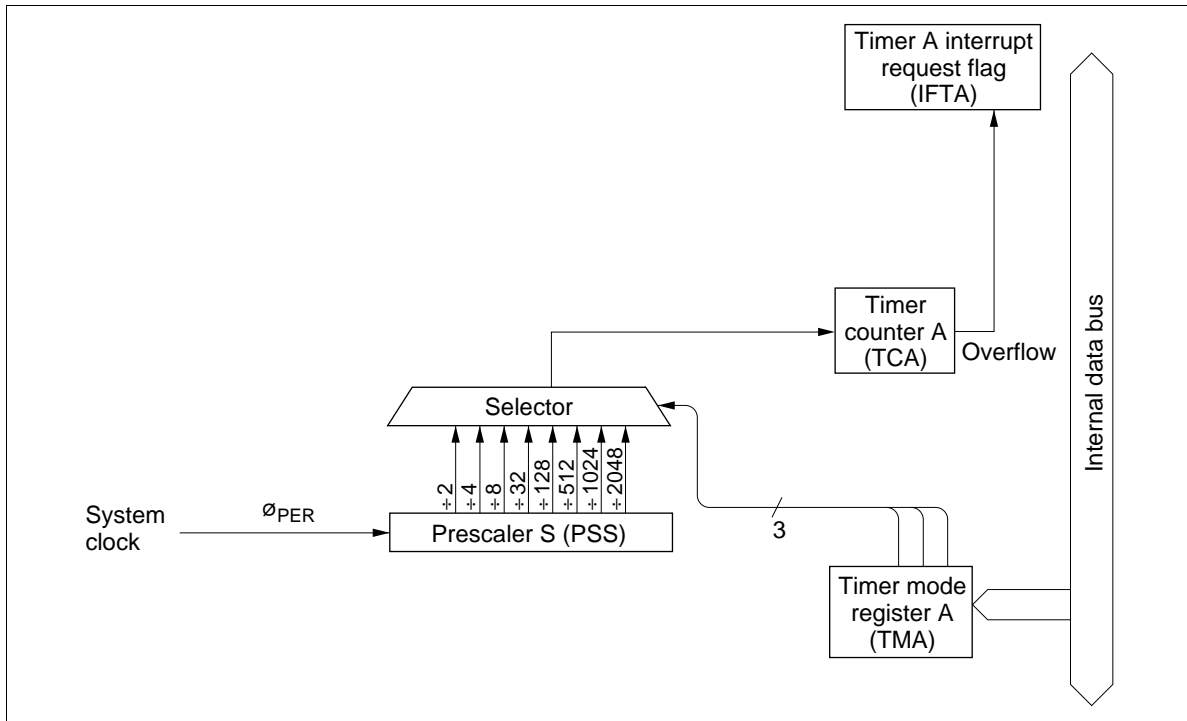
### Timer A

Timer A is an 8-bit free-running timer that has the following features:

- One of eight internal clocks can be selected from prescaler S according to the setting of timer mode register A (TMA: \$008)
- An interrupt request can be generated when timer counter A (TCA) overflows
- Input clock frequency must not be modified during timer A operation

**Table 7     Timer Functions**

Functions		Timer A	Timer B	Timer C
Clock source	Prescaler S	Available	Available	Available
	External event	—	Available	—
Timer functions	Free-running	Available	Available	Available
	Event counter	—	Available	—
	Reload	—	Available	Available
	Watchdog	—	—	Available
	Input capture	—	Available	—
Timer output	PWM	—	—	Available



**Figure 22 Timer A Block Diagram**

**Timer mode register A (TMA: \$008)**

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMA2	TMA1	TMA0

TMA2	TMA1	TMA0	Source Prescaler	Input clock frequency
0	0	0	PSS	2048 $t_{cyc}$
		1	PSS	1024 $t_{cyc}$
	1	0	PSS	512 $t_{cyc}$
		1	PSS	128 $t_{cyc}$
1	0	0	PSS	32 $t_{cyc}$
		1	PSS	8 $t_{cyc}$
	1	0	PSS	4 $t_{cyc}$
		1	PSS	2 $t_{cyc}$

**Figure 23 Timer Mode Register A (TMA)**

**Timer B**

Timer B is an 8-bit multifunction timer that includes free-running, reload, and input capture timer features. These are described as follows.

- By setting timer mode register B1 (TMB1: \$009), one of seven internal clocks supplied from prescaler S can be selected, or timer B can be used as an external event counter
- By setting timer mode register B2 (TMB2: \$026), detection edge type of EVNB can be selected
- By setting timer write register BL, BU (TWBL, BU: \$00A, \$00B), timer counter B (TCB) can be written to during reload timer operation
- By setting timer read register BL, BU (TRBL, BU: \$00A, \$00B), the contents of timer counter B can be read out
- Timer B can be used as an input capture timer to count the clock cycles between trigger edges input as an external event
- An interrupt can be requested when timer counter B overflows or when a trigger input edge is received during input capture operation

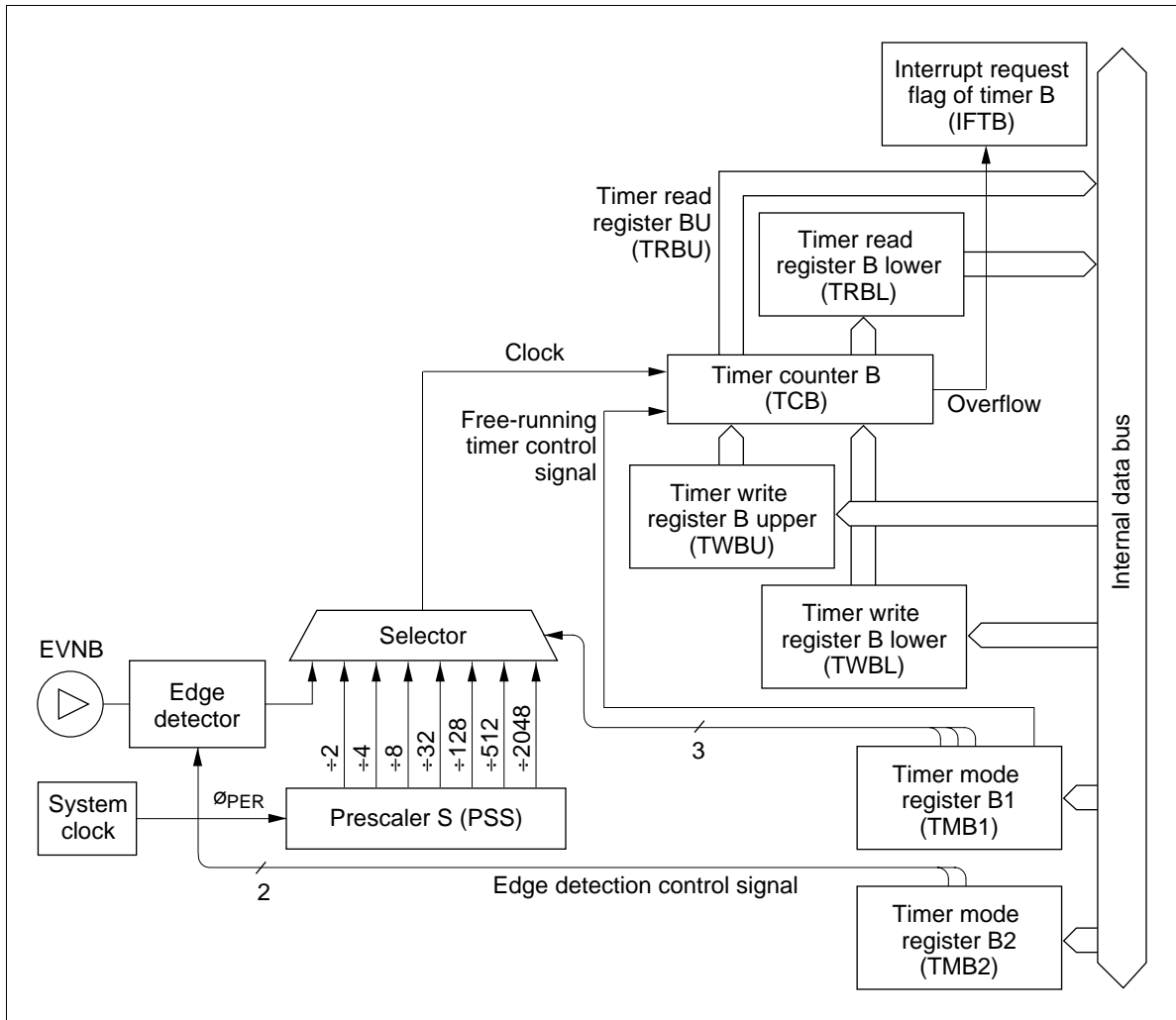


Figure 24 Timer B Free-Running and Reload Operation Block Diagram

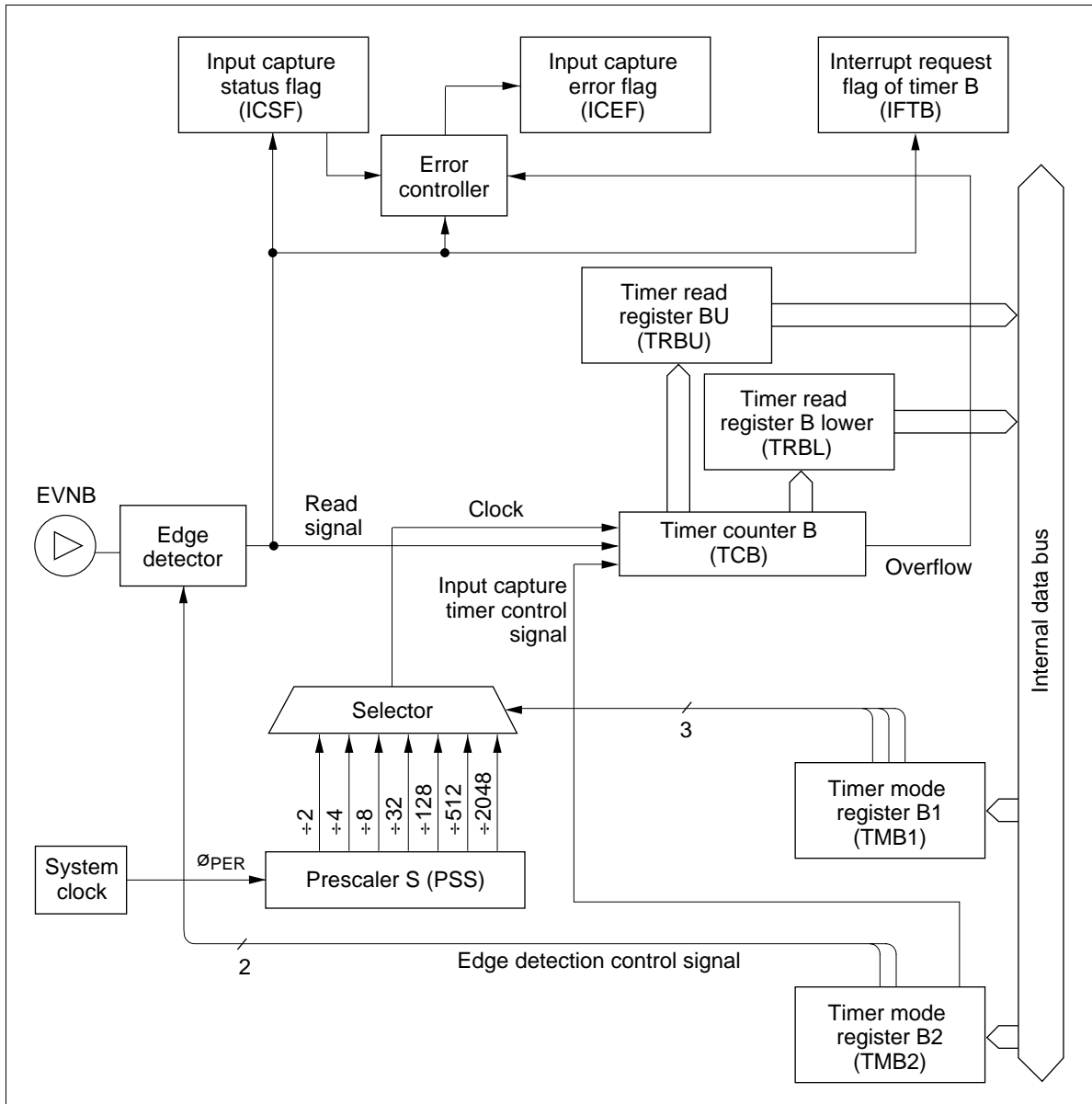


Figure 25 Timer B Input Capture Operation Block Diagram

## HD404318 Series

### Timer mode register B1 (TMB1: \$009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection	TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	Free-running timer	0	0	0	2048 $t_{cyc}$
1	Reload timer	0	0	1	512 $t_{cyc}$
		1	0	0	128 $t_{cyc}$
		1	0	1	32 $t_{cyc}$
		1	1	0	8 $t_{cyc}$
		1	1	1	4 $t_{cyc}$
		1	1	0	2 $t_{cyc}$
		1	1	1	D <sub>2</sub> /EVNB (external event input)

Figure 26 Timer Mode Register B1 (TMB1)

### Timer mode register B2 (TMB2: \$026)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	TMB22	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
0	1	Falling edge detection
1	0	Rising edge detection
1	1	Rising and falling edge detection

TMB22	Free-Running/Reload and Input Capture Selection
0	Free-Running/Reload
1	Input capture

Figure 27 Timer Mode Register B2 (TMB2)

### **Timer C**

Timer C is an 8-bit multifunction timer that includes free-running, reload, and watchdog timer features, which are described as follows.

- By setting timer mode register C (TMC: \$00D), one of eight internal clocks supplied from prescaler S can be selected
- By selecting pin TOC with bit 2 (PMRA2) of port mode register A (PMRA: \$004), timer C output (PWM output) is enabled
- By setting timer write register CL, CU (TWCL, CU: \$00E, \$00F), timer counter C (TCC) can be written to
- By setting timer read register CL, CU (TRCL, CU: \$00E, \$00F), the contents of timer counter C can be read out
- An interrupt can be requested when timer counter C overflows
- Timer counter C can be used as a watchdog timer for detecting runaway program

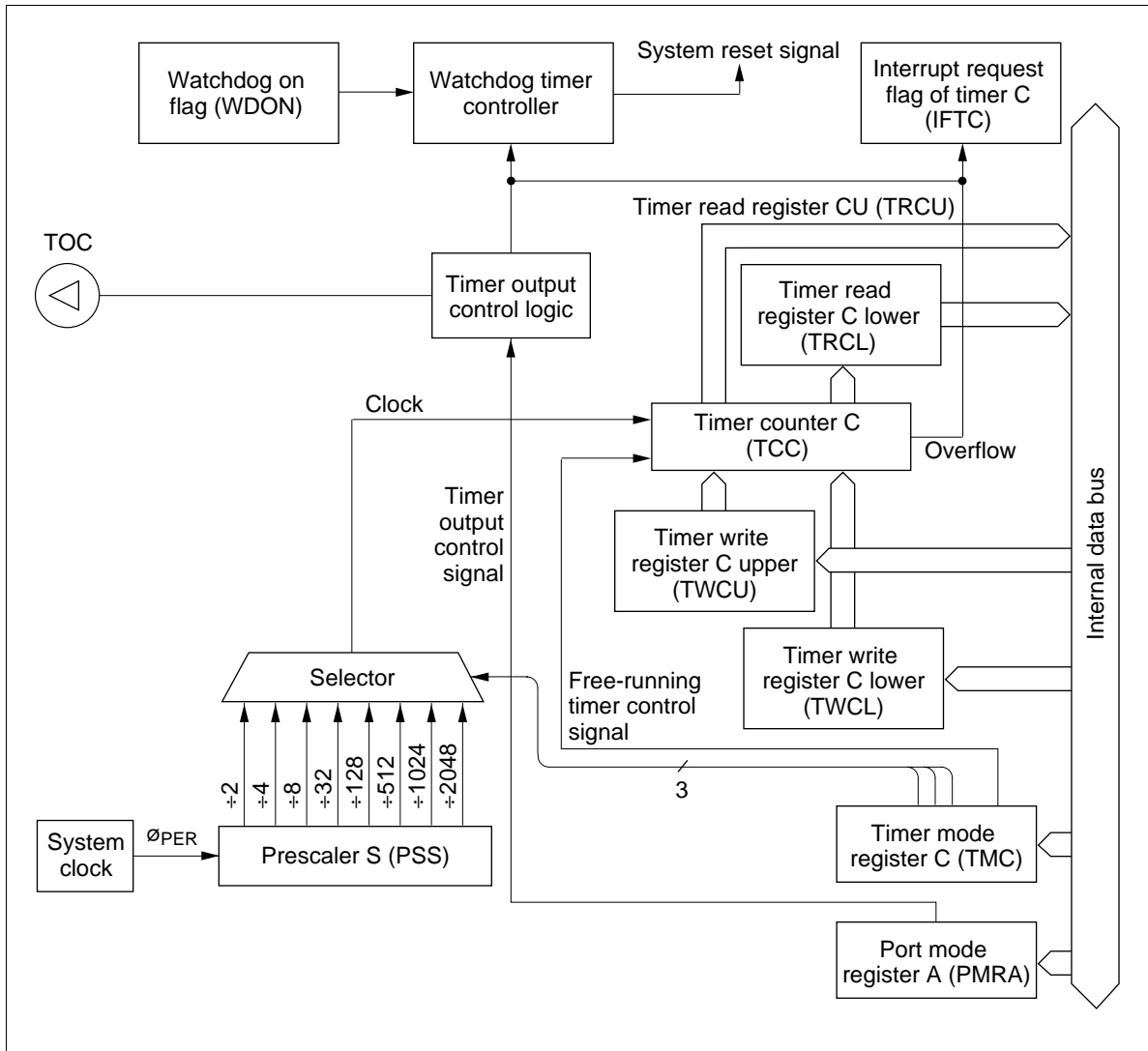


Figure 28 Timer C Block Diagram

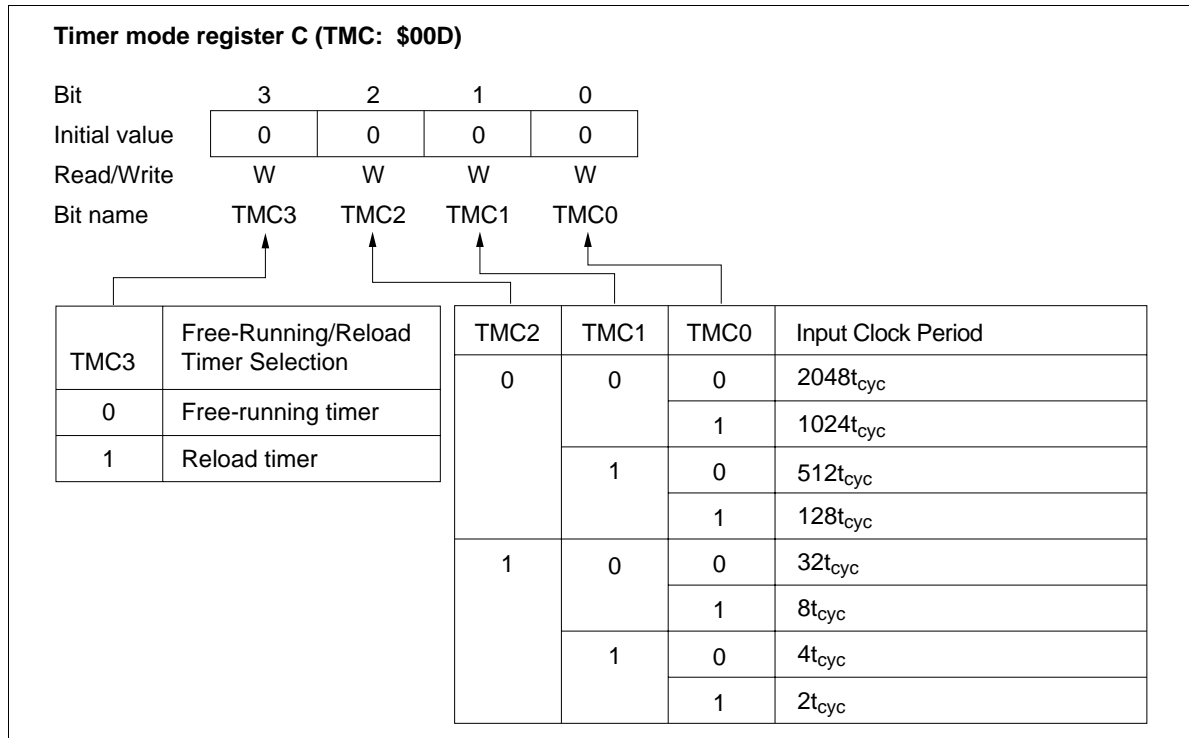


Figure 29 Timer Mode Register C (TMC)

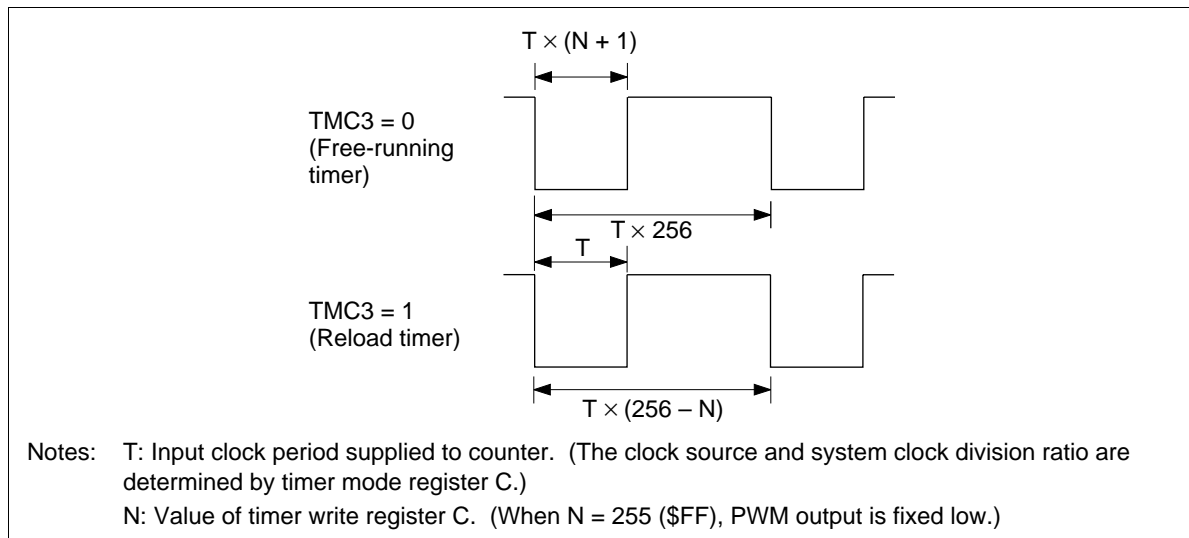


Figure 30 PWM Output Waveform

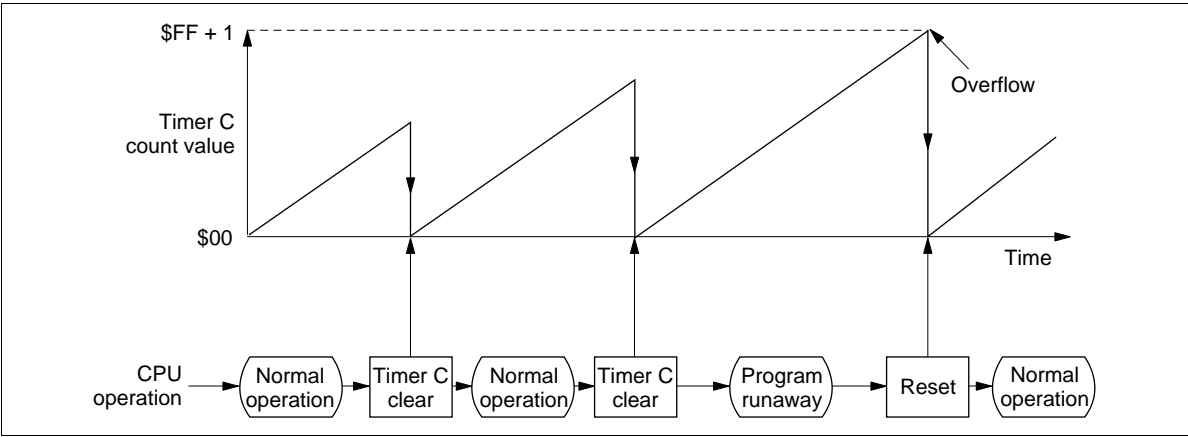


Figure 31 Watchdog Timer Operation Flowchart

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 8. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 8 PWM Output Following Update of Timer Write Register

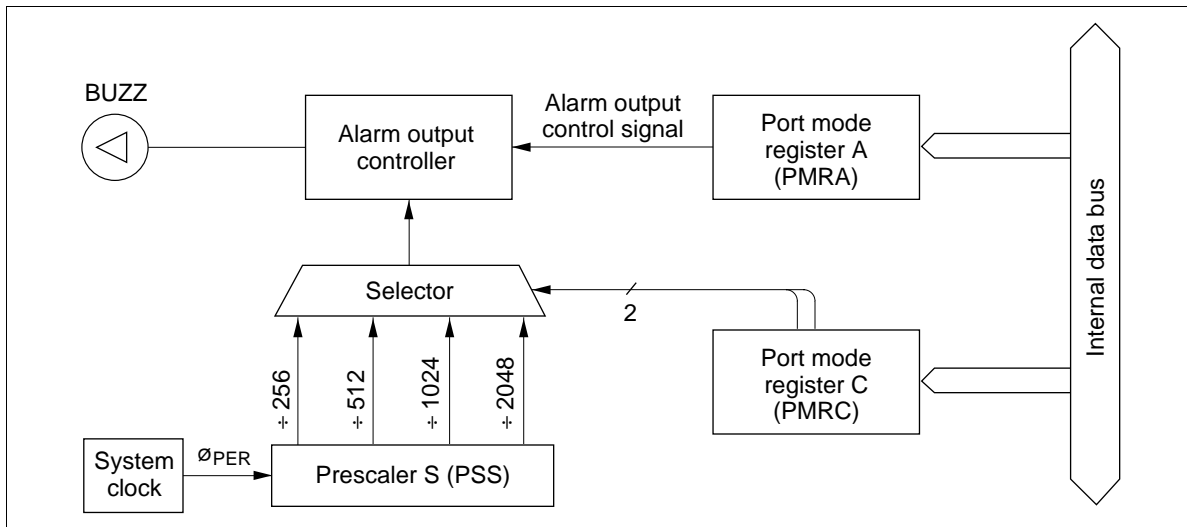
Mode	PWM Output	
	Timer Write Register is Updated during High PWM Output	Timer Write Register is Updated during Low PWM Output
Free running		
Reload		

## Alarm Output Function

The MCU has an alarm output function built in. By setting port mode register C (PMRC: \$025), one of four alarm frequencies supplied from the PSS can be selected.

**Table 9 Port Mode Register C**

PMRC		
Bit 3	Bit 2	System Clock Divisor
0	0	÷ 2048
	1	÷ 1024
1	0	÷ 512
	1	÷ 256



**Figure 32 Alarm Output Function Block Diagram**

---

## HD404318 Series

---

### Serial Interface

The MCU has a one-channel serial interface built in with the following features.

- One of 13 different internal clocks or an external clock can be selected as the transmit clock. The internal clocks include the six prescaler outputs divided by two and by four, and the system clock.
- During idle states, the serial output pin can be controlled to be high or low output
- Transmit clock errors can be detected
- An interrupt request can be generated after transfer has completed when an error occurs

**Table 10    Serial Interface Operating Modes**

SMR		PMRA	
Bit 3	Bit 1	Bit 0	Operating Mode
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

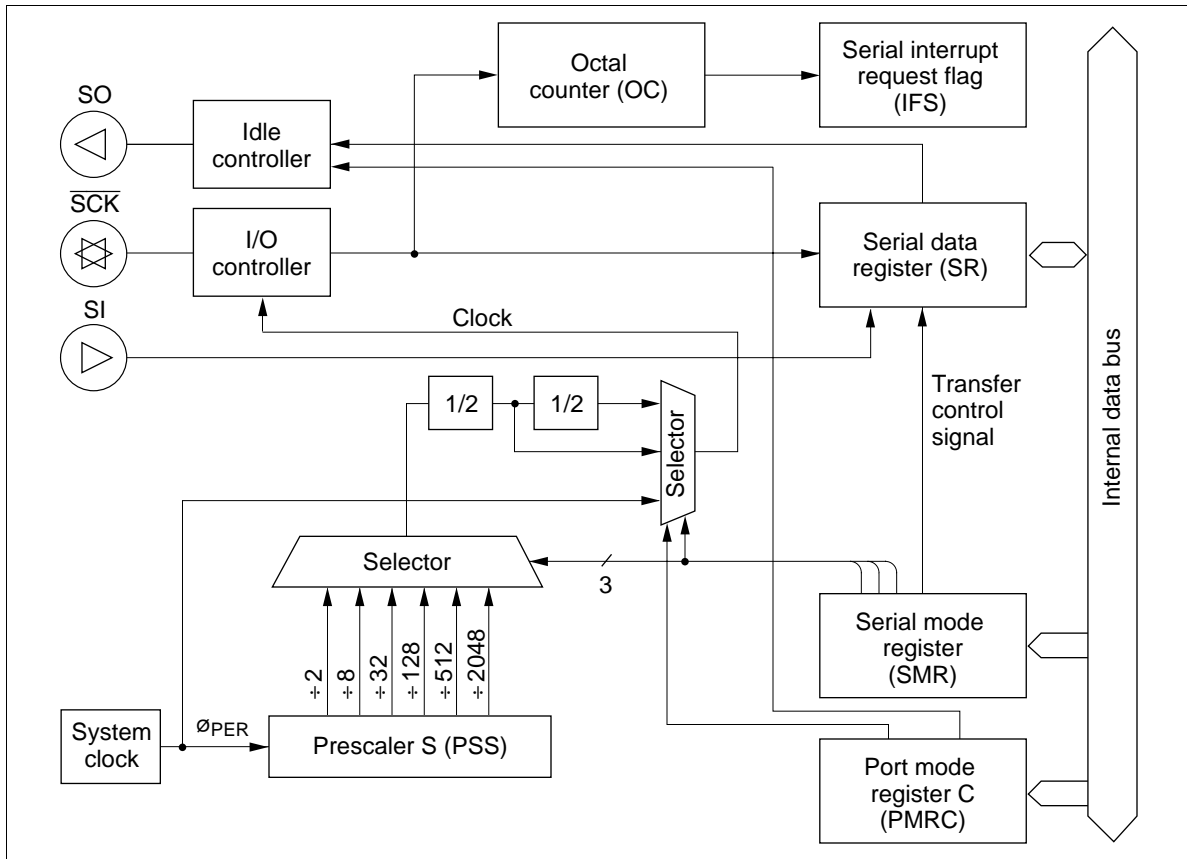
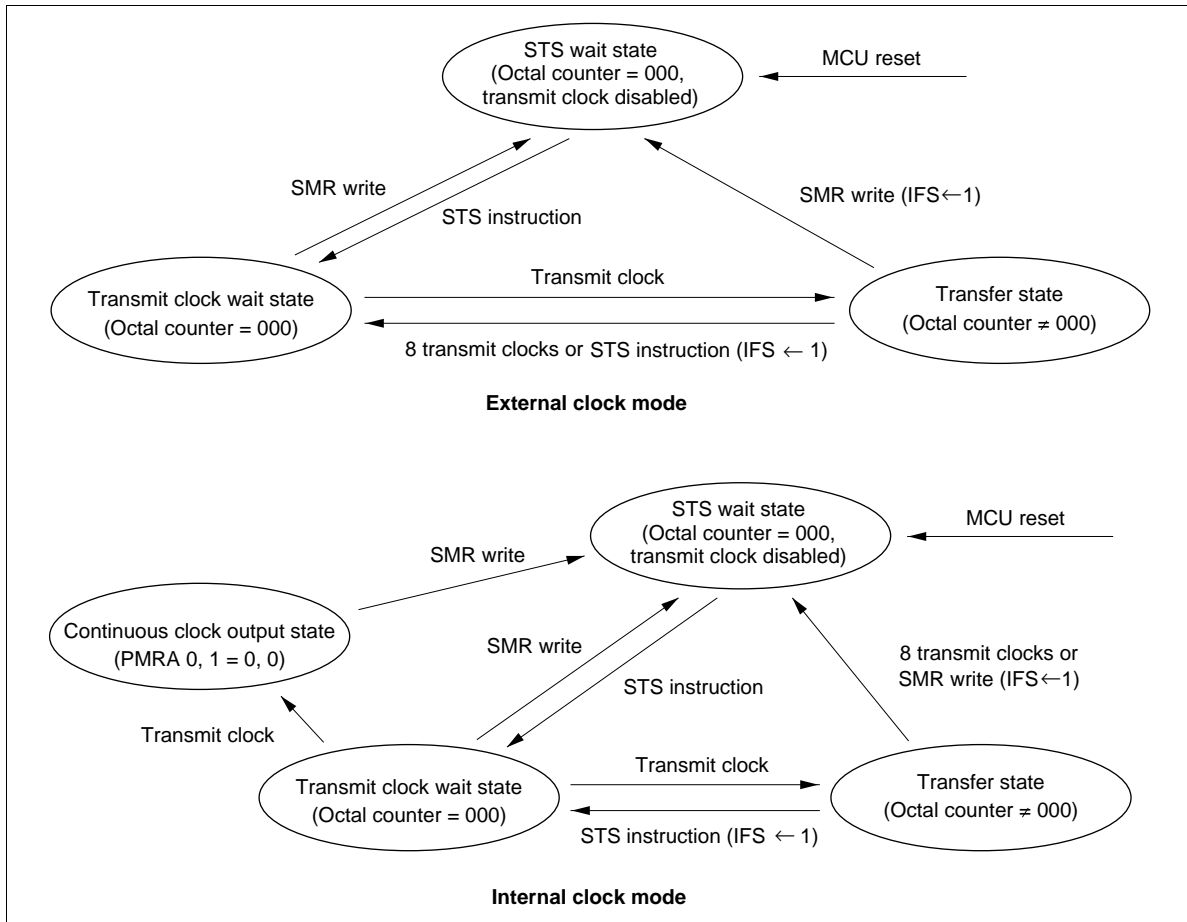
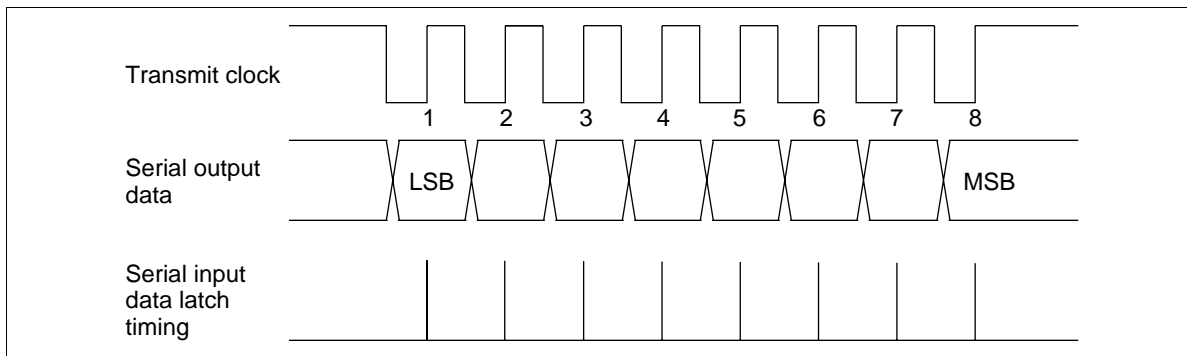


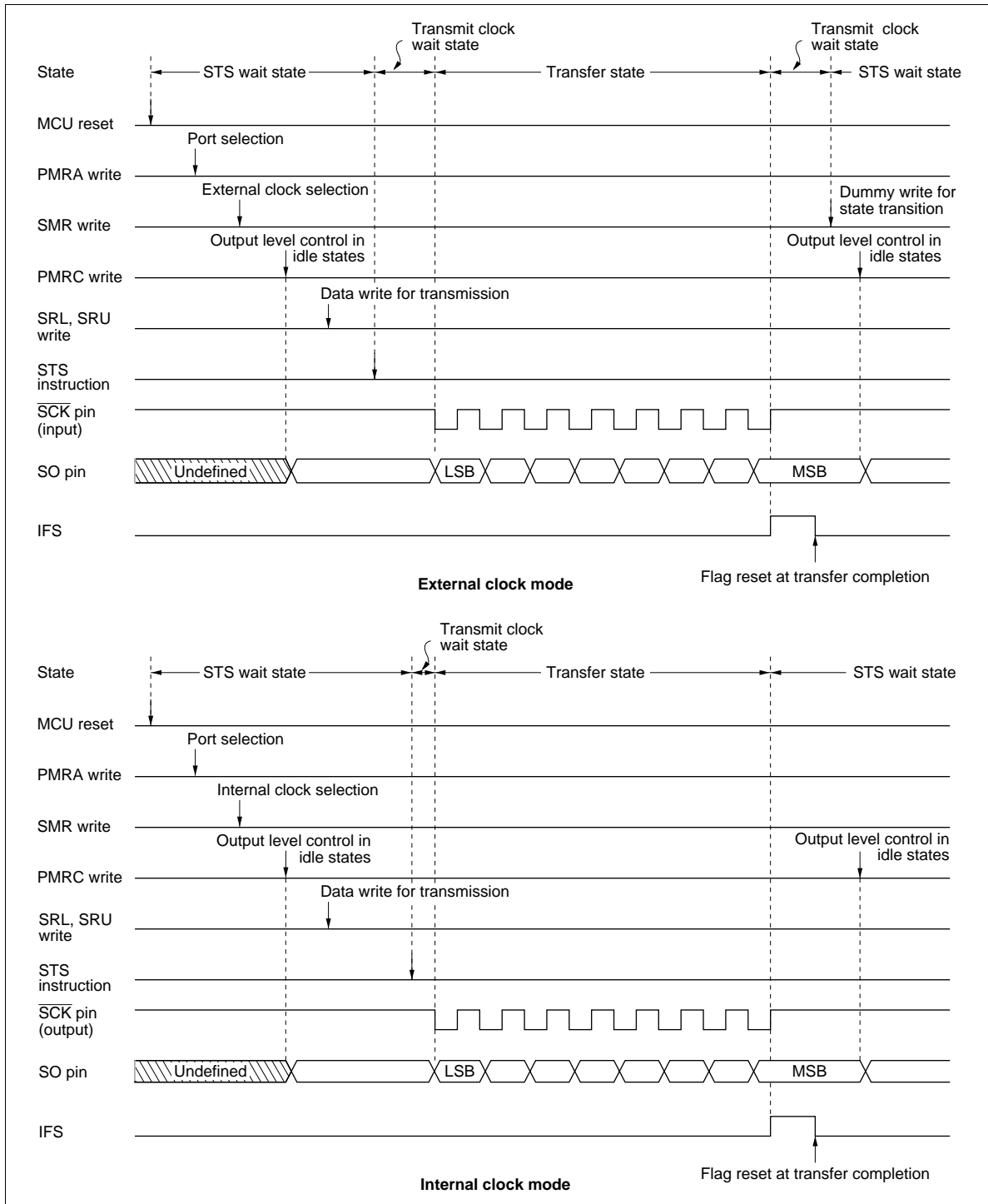
Figure 33 Serial Interface Block Diagram



**Figure 34 Serial Interface State Transitions**



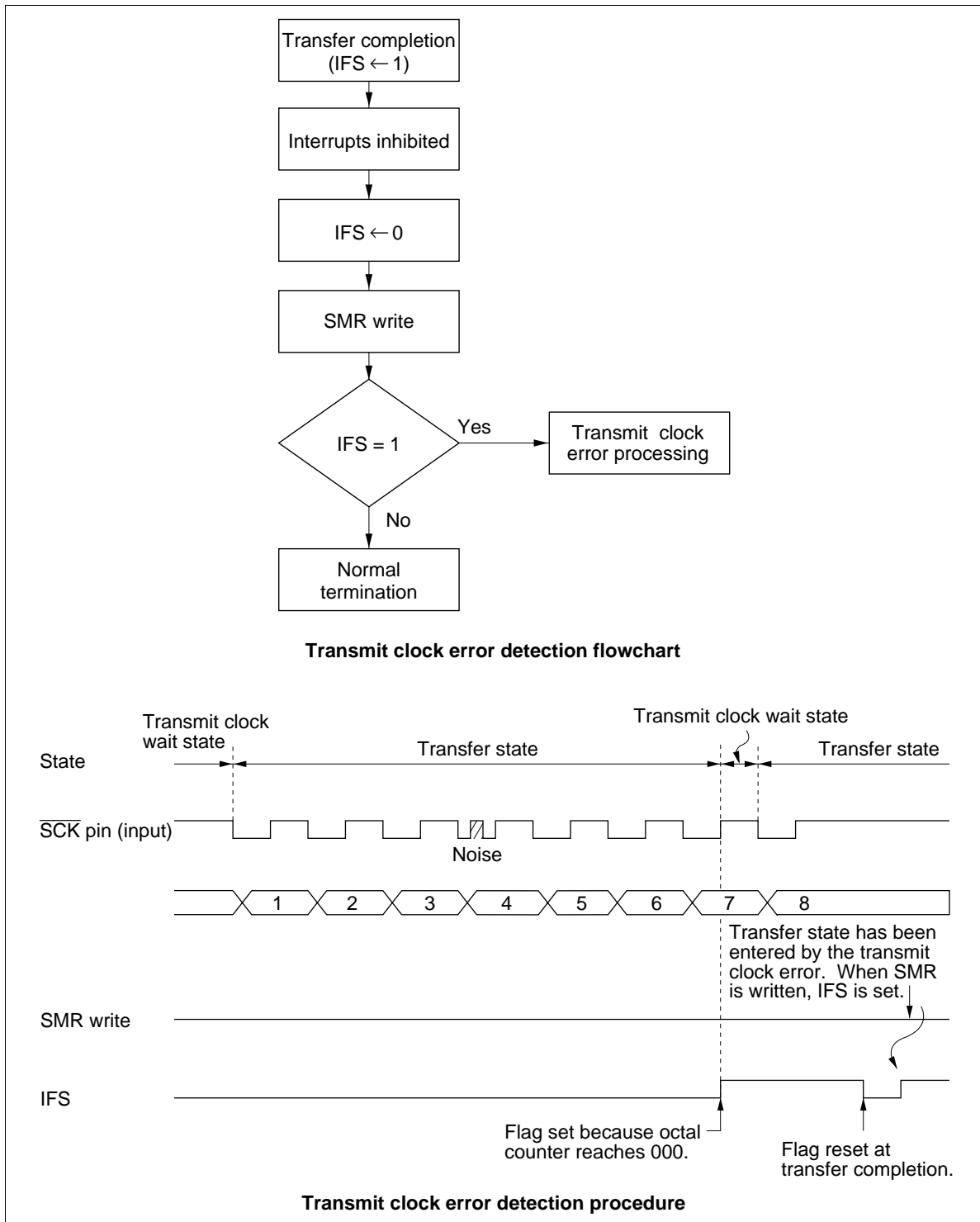
**Figure 35 Serial Interface Timing**



**Figure 36 Example of Serial Interface Operation Sequence**

## HD404318 Series

Transmit clock errors are detected as illustrated in figure 37.



**Figure 37 Transmit Clock Error Detection**

Table 11 Transmit Clock Selection

PMRC	SMR				
Bit 0	Bit 2	Bit 1	Bit 0	System Clock Divisor	Transmit Clock Frequency
0	0	0	0	$\div 2048$	$4096t_{cyc}$
			1	$\div 512$	$1024t_{cyc}$
		1	0	$\div 128$	$256t_{cyc}$
			1	$\div 32$	$64t_{cyc}$
	1	0	0	$\div 8$	$16t_{cyc}$
			1	$\div 2$	$4t_{cyc}$
1	0	0	0	$\div 4096$	$8192t_{cyc}$
			1	$\div 1024$	$2048t_{cyc}$
		1	0	$\div 256$	$512t_{cyc}$
			1	$\div 64$	$128t_{cyc}$
	1	0	0	$\div 16$	$32t_{cyc}$
			1	$\div 4$	$8t_{cyc}$

Serial mode register (SMR: \$005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	R0/ $\overline{SCK}$ Mode Selection	SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	R0	0	0	0	Output	Prescaler	Refer to table 11
				1			
				0			
1	$\overline{SCK}$	1	0	0	Output	System clock	—
				1			
				0			
1	1	1	1	0	Input	External clock	—
				1	Input		

Figure 38 Serial Mode Register (SMR)

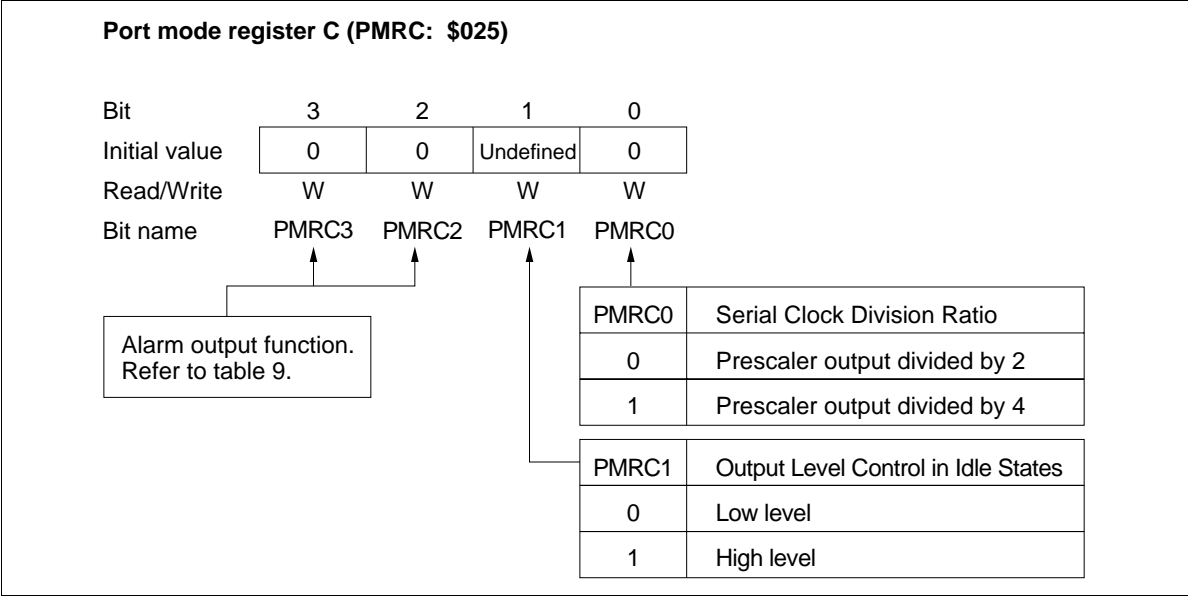


Figure 39 Port Mode Register C (PMRC)

## A/D Converter

The MCU also contains a built-in A/D converter that uses a sequential comparison method with a resistance ladder. It can perform digital conversion of eight analog inputs with 8-bit resolution. The following describes the A/D converter.

- A/D mode register 1 (AMR1: \$019) is used to select digital or analog ports
- A/D mode register 2 (AMR2: \$01A) is used to set the A/D conversion speed and to select digital or analog ports
- The A/D channel register (ACR: \$016) is used to select an analog input channel
- A/D conversion is started by setting the A/D start flag (ADSF: \$020, 2) to 1. After the conversion is completed, converted data is stored in the A/D data register, and at the same time, the A/D start flag is cleared to 0
- By setting the  $I_{AD}$  off flag (IAOF: \$021, 2) to 1, the current flowing through the resistance ladder can be cut off even while operating in standby or active mode

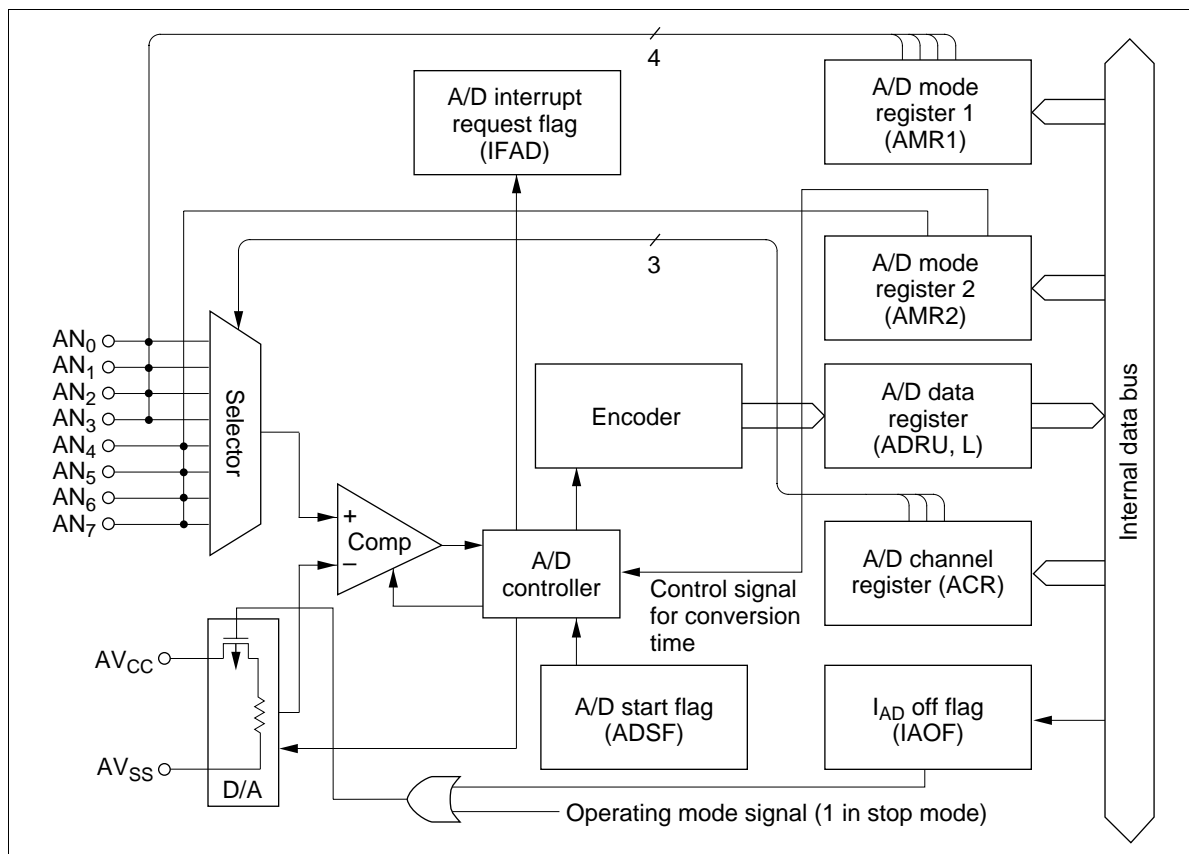
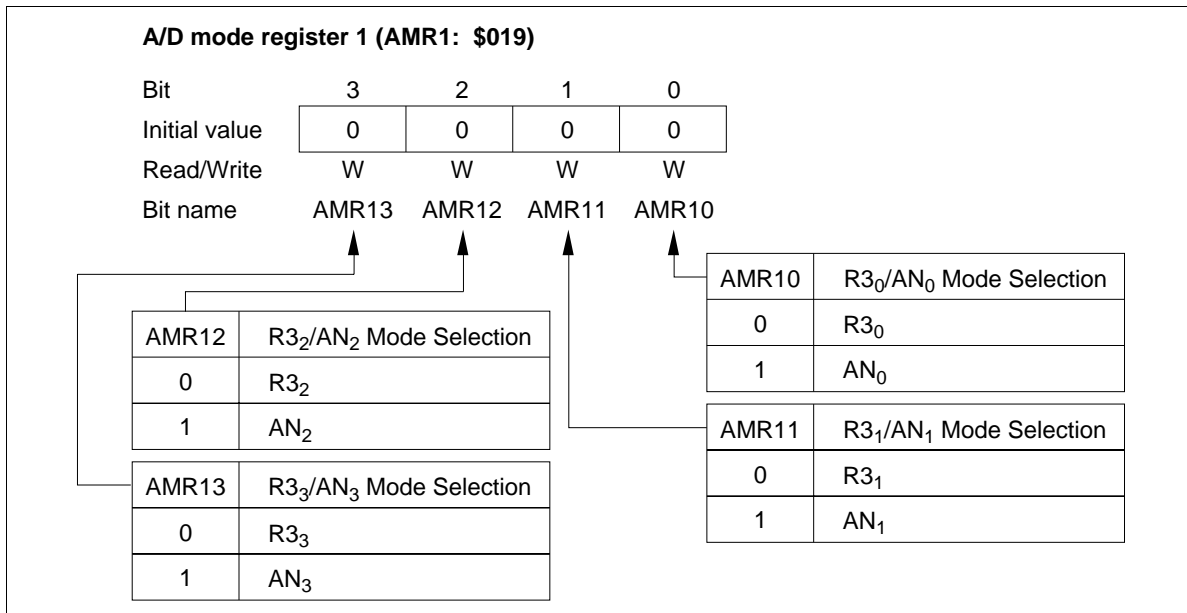


Figure 40 A/D Converter Block Diagram

## HD404318 Series

### Notes on Usage

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF)
- Do not write to the A/D start flag during A/D conversion
- Data in the A/D data register during A/D conversion is undefined
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop mode. In addition, to save power while in stop mode, all current flowing through the converter's resistance ladder is cut off.
- If the power supply for the A/D converter is to be different from  $V_{CC}$ , connect a 0.1- $\mu$ F bypass capacitor between the  $AV_{CC}$  and  $AV_{SS}$  pins. (However, this is not necessary when the  $AV_{CC}$  pin is directly connected to the  $V_{CC}$  pin.)
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to  $V_{CC}$ . When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by bit 1 of the A/D mode register as an analog pin will remain pulled up.



**Figure 41 A/D Mode Register 1 (AMR1)**

**A/D mode register 2 (AMR2: \$01A)**

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	AMR21	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

AMR21	R4/AN <sub>4</sub> –AN <sub>7</sub> Pin Selection
0	R4
1	AN <sub>4</sub> –AN <sub>7</sub>

**Figure 42 A/D Mode Register (AMR2)**

**A/D channel register (ACR: \$016)**

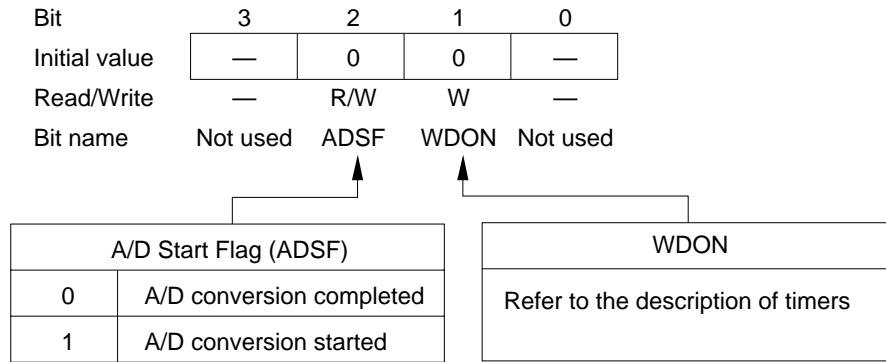
Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	ACR2	ACR1	ACR0

ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	AN <sub>0</sub>
		1	AN <sub>1</sub>
	1	0	AN <sub>2</sub>
		1	AN <sub>3</sub>
1	0	0	AN <sub>4</sub>
		1	AN <sub>5</sub>
	1	0	AN <sub>6</sub>
		1	AN <sub>7</sub>

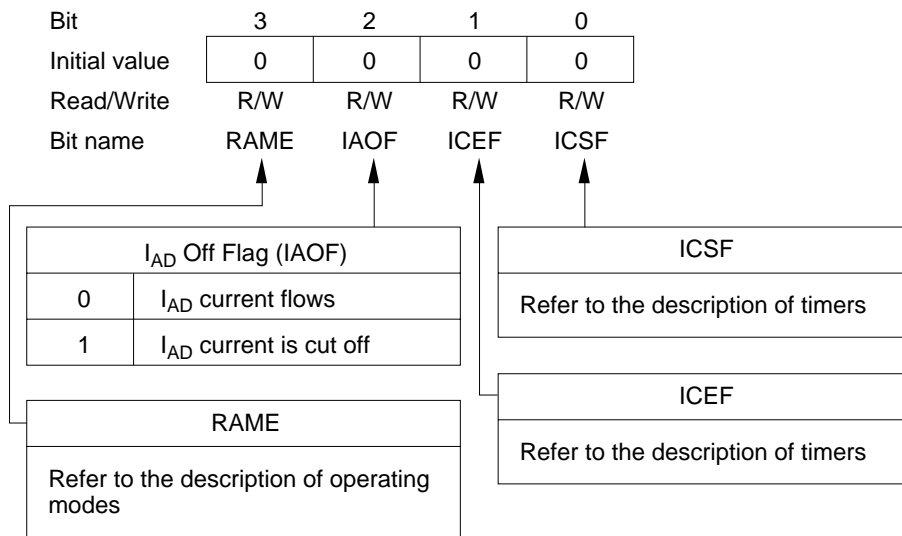
**Figure 43 A/D Channel Register (ACR)**

### A/D start flag (ADSF: \$020, bit 2)

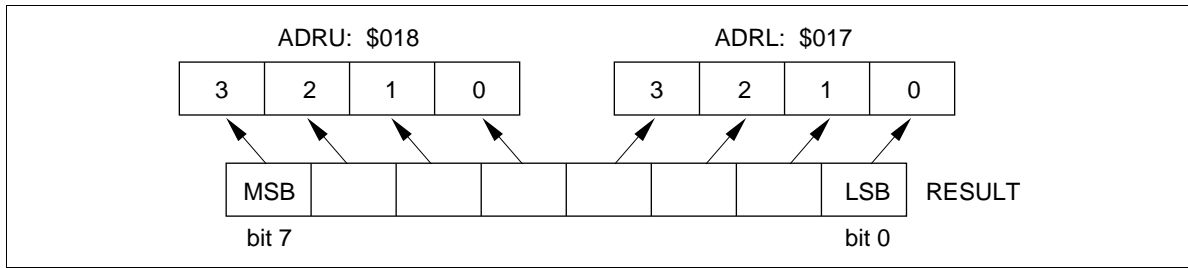


**Figure 44 A/D Start Flag (ADSF)**

### I<sub>AD</sub> off flag (IAOF: \$021, bit 2)



**Figure 45 I<sub>AD</sub> Off Flag (IAOF)**



**Figure 46 A/D Data Registers**

A/D data register (lower digit) (ADRL: \$017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

**Figure 47 A/D Data Register Lower Digit (ADRL)**

A/D data register (upper digit) (ADRU: \$018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

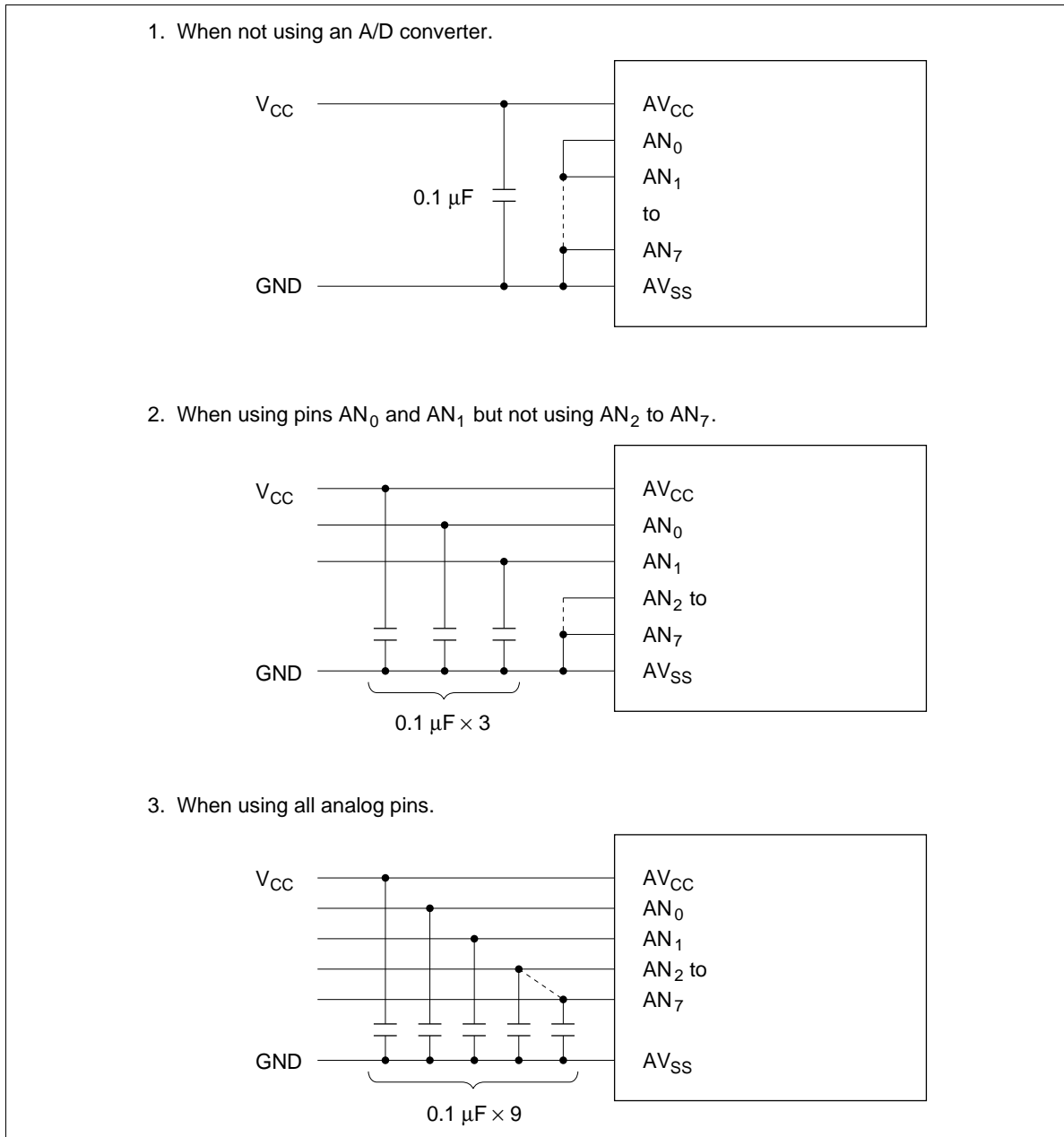
**Figure 48 A/D Data Register Upper Digit (ADRU)**

## HD404318 Series

### Notes on Mounting

Assemble all parts including the HD404318 Series on a board, noting the points described below.

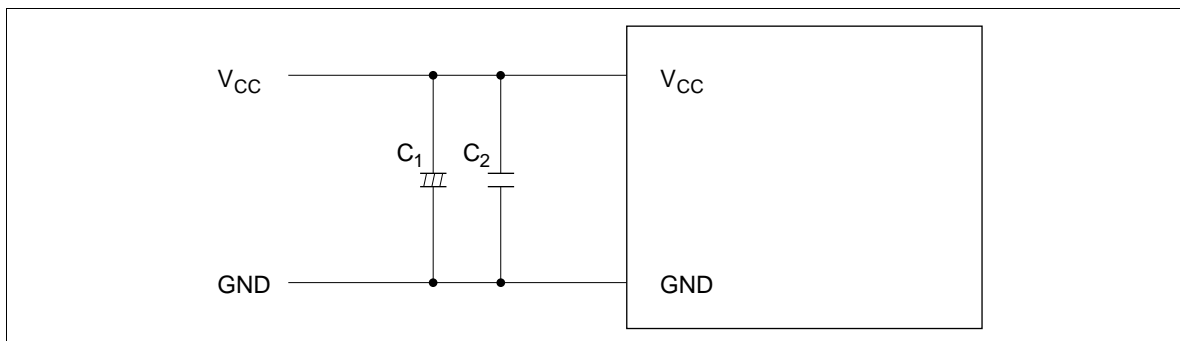
1. Connect layered ceramic type capacitors (about  $0.1\ \mu\text{F}$ ) between  $\text{AV}_{\text{CC}}$  and  $\text{AV}_{\text{SS}}$ , between  $\text{V}_{\text{CC}}$  and  $\text{GND}$ , and between used analog pins and  $\text{AV}_{\text{SS}}$ .
2. Connect unused analog pins to  $\text{AV}_{\text{SS}}$ .



**Figure 49 Example of Connections (1)**

Between the  $V_{CC}$  and GND lines, connect capacitors designed for use in ordinary power supply circuits. An example connection is described in figure 50.

No resistors can be inserted in series in the power supply circuit, so the capacitors should be connected in parallel. The capacitors are a large capacitance  $C_1$  and a small capacitance  $C_2$ .



**Figure 50 Example of Connections (2)**

## HD404318 Series

### Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	$V_{CC}$	−0.3 to +7.0	V	
Programming voltage	$V_{PP}$	−0.3 to +14.0	V	1
Pin voltage	$V_T$	−0.3 to $V_{CC} + 0.3$	V	2
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	3
Total permissible input current	$\sum I_O$	70	mA	4
Total permissible output current	$-\sum I_O$	150	mA	5
Maximum input current	$I_O$	4	mA	6, 7
		20	mA	6, 8
Maximum output current	$-I_O$	4	mA	9, 10
		30	mA	10, 11
Operating temperature	$T_{opr}$	−20 to +75	°C	
Storage temperature	$T_{stg}$	−55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST ( $V_{PP}$ ) of HD4074318.
2. Applies to all standard voltage pins.
3. Applies to high-voltage pins.
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from  $V_{CC}$  to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to ports R3 and R4.
8. Applies to port R0.
9. Applies to ports R0, R3, and R4.
10. The maximum output current is the maximum current flowing from  $V_{CC}$  to each I/O pin.
11. Applies to ports  $D_0$ – $D_8$ , R1, R2, and R8.

**Electrical Characteristics**

**DC Characteristics** ( $V_{CC} = 4.0$  to  $5.5$  V,  $GND = 0$  V,  $V_{disp} = V_{CC} - 40$  V to  $V_{CC}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ , unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	$V_{IH}$	$\overline{RESET}$ , $\overline{SCK}$ , SI, $\overline{INT_0}$ , $\overline{INT_1}$ , $\overline{STOPC}$ , EVNB	$0.8V_{CC}$	—	$V_{CC} + 0.3$	V		
		OSC <sub>1</sub>	$V_{CC} - 0.5$	—	$V_{CC} + 0.3$	V		
Input low voltage	$V_{IL}$	$\overline{RESET}$ , $\overline{SCK}$ , SI	-0.3	—	$0.2V_{CC}$	V		
		$\overline{INT_0}$ , $\overline{INT_1}$ , $\overline{STOPC}$ , EVNB	$V_{CC} - 40$	—	$0.2V_{CC}$	V		
		OSC <sub>1</sub>	-0.3	—	0.5	V		
Output high voltage	$V_{OH}$	$\overline{SCK}$ , SO, TOC	$V_{CC} - 0.5$	—	—	V	$-I_{OH} = 0.5$ mA	
Output low voltage	$V_{OL}$	$\overline{SCK}$ , SO, TOC	—	—	0.4	V	$I_{OL} = 0.4$ mA	
I/O leakage current	$ I_{IL} $	$\overline{RESET}$ , $\overline{SCK}$ , SI, SO, TOC, OSC <sub>1</sub>	—	—	1	μA	$V_{in} = 0$ V to $V_{CC}$	1
		$\overline{INT_0}$ , $\overline{INT_1}$ , $\overline{STOPC}$ , EVNB	—	—	20	μA	$V_{in} = V_{CC} - 40$ to $V_{CC}$	1
Current dissipation in active mode	$I_{CC}$	$V_{CC}$	—	—	5.0	mA	$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	2, 5
			—	—	8.0	mA		2, 6
Current dissipation in standby mode	$I_{SBY}$	$V_{CC}$	—	—	2.0	mA	$V_{CC} = 5$ V, $f_{OSC} = 4$ MHz	3
Current dissipation in stop mode	$I_{STOP}$	$V_{CC}$	—	—	10	μA	$V_{CC} = 5$ V	4, 5
			—	—	20	μA		4, 6
Stop mode retaining voltage	$V_{STOP}$	$V_{CC}$	2	—	—	V		

Notes: 1. Excludes current flowing through pull-up MOS and output buffers.

2.  $I_{CC}$  is the source current when no I/O current is flowing while the MCU is in reset state.

Test conditions:

MCU: Reset

Pins:  $\overline{RESET}$ , TEST at GND

R0, R3, R4 at  $V_{CC}$

D<sub>0</sub>–D<sub>8</sub>, R1, R2, R8, RA<sub>1</sub> at  $V_{disp}$

## HD404318 Series

3.  $I_{SBY}$  is the source current when no I/O current is flowing while the MCU timer is operating.  
 Test conditions:      MCU: I/O reset  
                                  Standby mode  
                                  Pins:  $\overline{RESET}$  at  $V_{CC}$   
                                  TEST at GND  
                                  R0, R3, R4 at  $V_{CC}$   
                                   $D_0-D_8, R1, R2, R8, RA_1$  at  $V_{disp}$
4. This is the source current when no I/O current is flowing.  
 Test conditions:      Pins: R0, R3, R4 at  $V_{CC}$   
                                   $D_0-D_8, R1, R2, R8, RA_1$  at GND
5. Applies to the HD404314, HD404316 and HD404318.
6. Applies to the HD4074318.

**I/O Characteristics for Standard Pins ( $V_{CC} = 4.0$  to  $5.5$  V,  $GND = 0$  V,  $V_{disp} = V_{CC} - 40$  V to  $V_{CC}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ , unless otherwise specified)**

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	$V_{IH}$	R0, R3, R4	$0.7V_{CC}$	—	$V_{CC} + 0.3$	V		
Input low voltage	$V_{IL}$	R0, R3, R4	$-0.3$	—	$0.3V_{CC}$	V		
Output high voltage	$V_{OH}$	R0, R3, R4	$V_{CC} - 0.5$	—	—	V	$-I_{OH} = 0.5$ mA	
Output low voltage	$V_{OL}$	R3, R4	—	—	0.4	V	$I_{OL} = 1.6$ mA	
		R0	—	—	2.0	V	$I_{OL} = 10$ mA	
Input leakage current	$ I_{IL} $	R0, R3, R4	—	—	1	$\mu\text{A}$	$V_{in} = 0$ V to $V_{CC}$	1
Pull-up MOS	$-I_{PU}$	R0, R3, R4	30	150	300	$\mu\text{A}$	$V_{CC} = 5$ V, $V_{in} = 0$ V	2
			30	80	180	$\mu\text{A}$		3

- Notes: 1. Output buffer current is excluded.  
 2. Applies to the HD404314, HD404316, and HD404318.  
 3. Applies to the HD4074318.

## HD404318 Series

**I/O Characteristics for High-Voltage Pins** ( $V_{CC} = 4.0$  to  $5.5$  V,  $GND = 0$  V,  $V_{disp} = V_{CC} - 40$  V to  $V_{CC}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ , unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	$V_{IH}$	$D_0-D_8$ , R1, R2, R8, RA <sub>1</sub>	$0.7V_{CC}$	—	$V_{CC} + 0.3$	V		
Input low voltage	$V_{IL}$	$D_0-D_8$ , R1, R2, R8, RA <sub>1</sub>	$V_{CC} - 40$	—	$0.3V_{CC}$	V		
Output high voltage	$V_{OH}$	$D_0-D_8$ , R1, R2, R8, BUZZ	$V_{CC} - 3.0$	—	—	V	$-I_{OH} = 15$ mA	
			$V_{CC} - 2.0$	—	—	V	$-I_{OH} = 10$ mA	
			$V_{CC} - 1.0$	—	—	V	$-I_{OH} = 4$ mA	
Output low voltage	$V_{OL}$	$D_0-D_8$ , R1, R2, R8, BUZZ	—	—	$V_{CC} - 37$	V	$V_{disp} = V_{CC} - 40$ V	1
			—	—	$V_{CC} - 37$	V	$150\text{ k}\Omega$ at $V_{CC} - 40$ V	2
I/O leakage current	$ I_{IL} $	$D_0-D_8$ , R1, R2, R8, RA <sub>1</sub> , BUZZ	—	—	20	$\mu\text{A}$	$V_{in} = V_{CC} - 40$ V to $V_{CC}$	3
Pull-down MOS current	$I_{PD}$	$D_0-D_8$ , R1, R2, R8, BUZZ	200	600	1000	$\mu\text{A}$	$V_{disp} = V_{CC} - 35$ V, $V_{in} = V_{CC}$	1

Notes: 1. Applies to pins with pull-down MOS as selected by the mask option .  
 2. Applies to pins without pull-down MOS as selected by the mask option.  
 3. Excludes output buffer current.

**A/D Converter Characteristics** ( $V_{CC} = 4.0$  to  $5.5$  V,  $GND = 0$  V,  $V_{disp} = V_{CC} - 40$  V to  $V_{CC}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ , unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog supply voltage	$AV_{CC}$	$AV_{CC}$	$V_{CC} - 0.3$	$V_{CC}$	$V_{CC} + 0.3$	V		1
Analog input voltage	$AV_{in}$	$AN_0-AN_7$	$AV_{SS}$	—	$AV_{CC}$	V		
Current flowing between $AV_{CC}$ and $AV_{SS}$	$I_{AD}$		—	—	200	$\mu\text{A}$	$V_{CC} = AV_{CC} = 5.0$ V	
Analog input capacitance	$CA_{in}$	$AN_0-AN_7$	—	—	30	pF		
Resolution			8	8	8	Bit		
Number of input channels			0	—	8	Chan nel		
Absolute accuracy			—	—	$\pm 2.0$	LSB		
Conversion time			34	—	67	$t_{cyc}$		
Input impedance		$AN_0-AN_7$	1	—	—	$M\Omega$		

Note: 1. Connect this to  $V_{CC}$  if the A/D converter is not used.

## HD404318 Series

AC Characteristics ( $V_{CC} = 4.0$  to  $5.5$  V,  $GND = 0$  V,  $V_{disp} = V_{CC} - 40$  V to  $V_{CC}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ )

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency	$f_{OSC}$	OSC <sub>1</sub> , OSC <sub>2</sub>	0.4	4	4.5	MHz	System clock divided by 4	
Instruction cycle time	$t_{cyc}$		0.89	1	10	$\mu\text{s}$		
Oscillation stabilization time (ceramic oscillator)	$t_{RC}$	OSC <sub>1</sub> , OSC <sub>2</sub>	—	—	7.5	ms		1
Oscillation stabilization time (crystal oscillator)	$t_{RC}$	OSC <sub>1</sub> , OSC <sub>2</sub>	—	—	40	ms		1
External clock high width	$t_{CPH}$	OSC <sub>1</sub>	92	—	—	ns		2
External clock low width	$t_{CPL}$	OSC <sub>1</sub>	92	—	—	ns		2
External clock rise time	$t_{CPr}$	OSC <sub>1</sub>	—	—	20	ns		2
External clock fall time	$t_{CPf}$	OSC <sub>1</sub>	—	—	20	ns		2
$\overline{INT_0}$ , $\overline{INT_1}$ , EVNB high widths	$t_{IH}$	$\overline{INT_0}$ , $\overline{INT_1}$ , EVNB	2	—	—	$t_{cyc}$		3
$\overline{INT_0}$ , $\overline{INT_1}$ , EVNB low widths	$t_{IL}$	$\overline{INT_0}$ , $\overline{INT_1}$ , EVNB	2	—	—	$t_{cyc}$		3
RESET low width	$t_{RSTL}$	$\overline{RESET}$	2	—	—	$t_{cyc}$		4
STOPC low width	$t_{STPL}$	$\overline{STOPC}$	1	—	—	$t_{RC}$		5
RESET rise time	$t_{RSTr}$	$\overline{RESET}$	—	—	20	ms		4
STOPC rise time	$t_{STPr}$	$\overline{STOPC}$	—	—	20	ms		5
Input capacitance	$C_{in}$	All input pins except TEST	—	—	30	pF	$f = 1$ MHz, $V_{in} = 0$ V	
		TEST	—	—	30	pF		6
			—	—	180	pF		7

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

- After  $V_{CC}$  reaches 4.0 V at power-on.
- After  $\overline{RESET}$  input goes low when stop mode is cancelled.
- After  $\overline{STOPC}$  input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled,  $\overline{RESET}$  or  $\overline{STOPC}$  must be input for at least a duration of  $t_{RC}$ .

When using a crystal or ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

- Refer to figure 51.
- Refer to figure 52.
- Refer to figure 53.
- Refer to figure 54.
- Applies to the HD404314, HD404316, and HD404318.
- Applies to the HD4074318.

## HD404318 Series

**Serial Interface Timing Characteristics** ( $V_{CC} = 4.0$  to  $5.5$  V,  $GND = 0$  V,  $V_{disp} = V_{CC} - 40$  V to  $V_{CC}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ , unless otherwise specified)

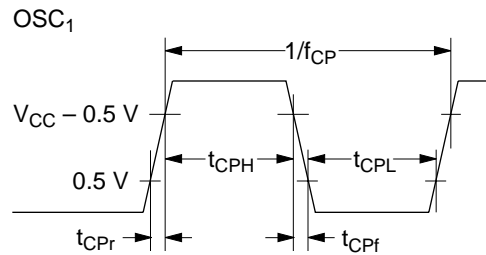
### During Transmit Clock Output

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	$t_{Scyc}$	$\overline{SCK}$	1	—	—	$t_{cyc}$	Load shown in figure 56	1
Transmit clock high width	$t_{SCKH}$	$\overline{SCK}$	0.4	—	—	$t_{Scyc}$	Load shown in figure 56	1
Transmit clock low width	$t_{SCKL}$	$\overline{SCK}$	0.4	—	—	$t_{Scyc}$	Load shown in figure 56	1
Transmit clock rise time	$t_{SCKr}$	$\overline{SCK}$	—	—	80	ns	Load shown in figure 56	1
Transmit clock fall time	$t_{SCKf}$	$\overline{SCK}$	—	—	80	ns	Load shown in figure 56	1
Serial output data delay time	$t_{DSO}$	SO	—	—	300	ns	Load shown in figure 56	1
Serial input data setup time	$t_{SSI}$	SI	100	—	—	ns		1
Serial input data hold time	$t_{HSI}$	SI	200	—	—	ns		1

### During Transmit Clock Input

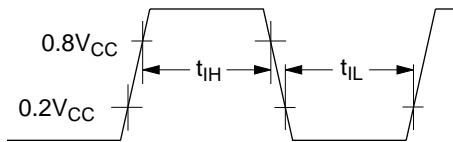
Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transmit clock cycle time	$t_{Scyc}$	$\overline{SCK}$	1	—	—	$t_{cyc}$		1
Transmit clock high width	$t_{SCKH}$	$\overline{SCK}$	0.4	—	—	$t_{Scyc}$		1
Transmit clock low width	$t_{SCKL}$	$\overline{SCK}$	0.4	—	—	$t_{Scyc}$		1
Transmit clock rise time	$t_{SCKr}$	$\overline{SCK}$	—	—	80	ns		1
Transmit clock fall time	$t_{SCKf}$	$\overline{SCK}$	—	—	80	ns		1
Serial output data delay time	$t_{DSO}$	SO	—	—	300	ns	Load shown in figure 56	1
Serial input data setup time	$t_{SSI}$	SI	100	—	—	ns		1
Serial input data hold time	$t_{HSI}$	SI	200	—	—	ns		1

Note: 1. Refer to figure 55.



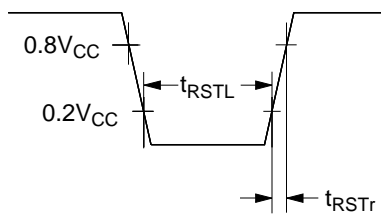
**Figure 51 External Clock Timing**

$\overline{\text{INT}}_0, \overline{\text{INT}}_1, \text{EVNB}$



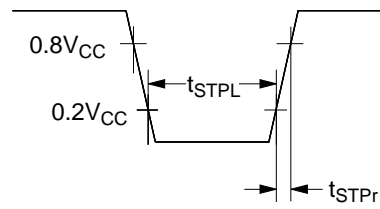
**Figure 52 Interrupt Timing**

$\overline{\text{RESET}}$

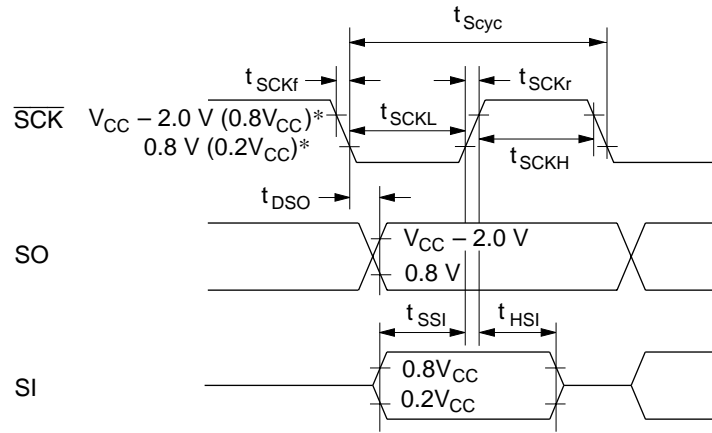


**Figure 53  $\overline{\text{RESET}}$  Timing**

$\overline{\text{STOPC}}$



**Figure 54  $\overline{\text{STOPC}}$  Timing**



Note:  $*V_{\text{CC}} - 2.0\text{ V}$  and  $0.8\text{ V}$  are the threshold voltages for transmit clock output.  
 $0.8V_{\text{CC}}$  and  $0.2V_{\text{CC}}$  are the threshold voltages for transmit clock input.

Figure 55 Serial Interface Timing

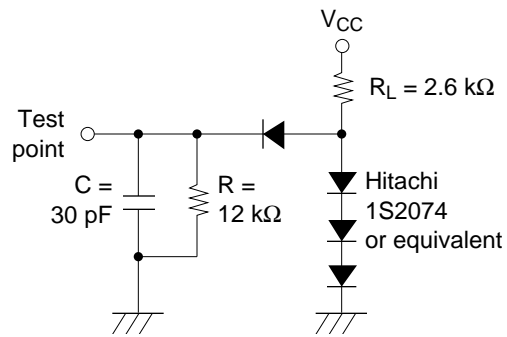


Figure 56 Timing Load Circuit

---

## HD404318 Series

---

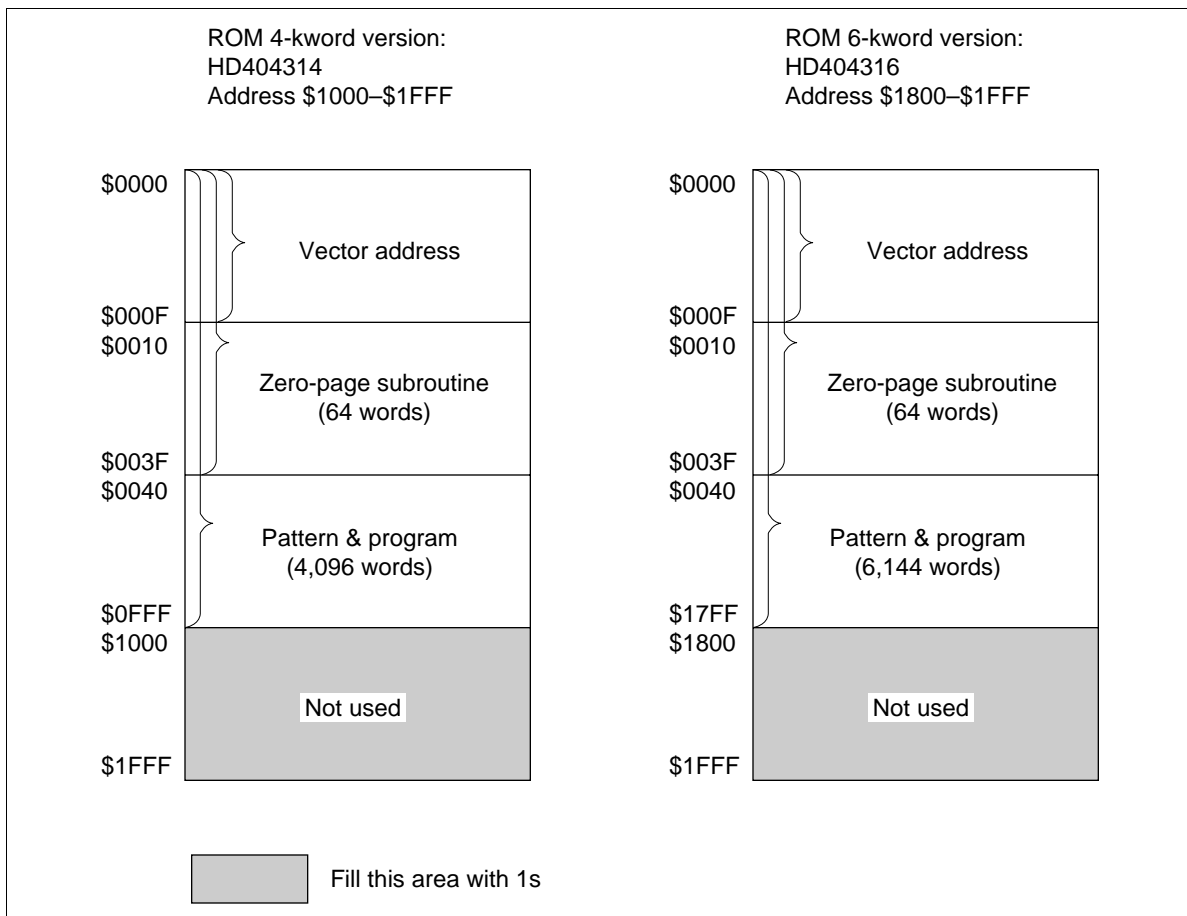
### Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size for the HD404314 and HD404316 as an 8-kword version

(HD404318). An 8-kword data size is required to change ROM data to mask manufacturing data since the program used is for an 8-kword version.

This limitation applies when using an EPROM or a data base.



**HD404314/HD404316/HD404318 Option List**

Please check off the appropriate applications and enter the necessary information.

**1. ROM Size**

<input type="checkbox"/> HD404314	4-kword
<input type="checkbox"/> HD404316	6-kword
<input type="checkbox"/> HD404318	8-kword

**2. I/O Options**

D: Without pull-down resistance

Pin name	I/O	I/O option	
		D	E
D0/INT0	I/O		
D1/INT1	I/O		
D2/EVNB	I/O		
D3/BUZZ	I/O		
D4/STOPC	I/O		
D5	I/O		
D6	I/O		
D7	I/O		
D8	I/O		

**3. RA1/Vdisp**

<input type="checkbox"/> RA1 without pull-down resistance
<input type="checkbox"/> Vdisp

Note: If even only one pin is selected with I/O option E, pin RA1/Vdisp must be selected to function as Vdisp.

**4. ROM Code Media**

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

<input type="checkbox"/> EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
<input type="checkbox"/> EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

**5. System Oscillator for OSC1 and OSC2**

<input type="checkbox"/> Ceramic oscillator	f =	MHz
<input type="checkbox"/> Crystal oscillator	f =	MHz
<input type="checkbox"/> External clock	f =	MHz

**6. Stop mode**

<input type="checkbox"/> Used
<input type="checkbox"/> Not used

**7. Package**

<input type="checkbox"/> DP-42S
<input type="checkbox"/> FP-44A

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

E: With pull-down resistance

Pin name		I/O	I/O option	
			D	E
R1	R10	I/O		
	R11	I/O		
	R12	I/O		
	R13	I/O		
R2	R20	I/O		
	R21	I/O		
	R22	I/O		
	R23	I/O		
R8	R80	I/O		
	R81	I/O		
	R82	I/O		
	R83	I/O		
RA	RA1	I	Selected in option (3)	

### Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.