

1. Overview

The M32C/81 is single-chip microcomputer that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/81 group is available in the 144-pin and 100-pin plastic molded QFP/LQFP package.

With 16-Mbyte address space, this microcomputer combines advanced instructions manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate to office automation, communication devices and industrial equipments and other high-speed processing applications.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Difference between the M32C/81 Group and the M32C/83 Group

The M32C/81 group microcomputer has less peripheral functions than the M32C/83 group microcomputer. The intelligent I/O group 3 and the A-D1 converter are not provided in the M32C/81 group. Consequently, interrupts caused the intelligent I/O group 3 interrupt request, a DMAC operation with the intelligent I/O group 3 and a DMACII operation with the intelligent I/O group 3 are not available in the M32C/81 group.

1.3 Performance Outline

Tables 1.1 and 1.2 list performance outline of the M32C/81 group.

Table 1.1 M32C/81 Group Performance (144-Pin Package)

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, V _{CC} =4.2 V to 5.5 V) 50ns (f(BCLK)=20MHz, V _{CC} =3.0 V to 5.5 V)
	Operation mode	Single-chip, memory expansion and microprocessor modes
	Memory space	16 Mbytes
	Memory capacity	See Table 1.3.
Peripheral function	Port	123 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generation function: 16 bits x 20 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IE bus ⁽¹⁾)
	Serial I/O	5 channels Clock synchronous, Clock asynchronous, IEBus ⁽¹⁾ (option), I ² C bus ⁽²⁾ (option)
	CAN module	1 channel Supporting CAN 2.0B specification
	A-D converter	10-bit A-D converter: 1 circuit Input : 34 channels
	D-A converter	8-bit D-A converter: 2 circuits
	DMAC	4 channels
	DMAC II	Can be activated by all relocatable vector interrupt factors Immediate transfer, arithmetic transfer and chain transfer functions
	CRC calculation circuit	CRC-CCITT
	X-Y converter	16 bits X 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock generation circuit, sub clock generation circuit, ring oscillator, PLL frequency synthesizer The above circuits include an internal feedback resistor and external ceramic resonator/crystal oscillator. Main clock oscillator stop detect function
Electric characteristics	Supply voltage	4.2 V to 5.5 V (f(BCLK)=32 MHz) 3.0 V to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 V to 3.6 V (f(BCLK)=20 MHz, not through VDC)
	Power consumption	28 mA (V _{CC} =5 V, f(BCLK)=32 MHz) 17 mA (V _{CC} =3.3 V, f(BCLK)=20 MHz) 470 μ A (V _{CC} =5 V, f(XCIN)=32 kHz, in wait mode) 340 μ A (V _{CC} =3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 μ A (V _{CC} =3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 μ A (V _{CC} =5 V, f(XCIN)=32 kHz, in stop mode) 0.4 μ A (V _{CC} =3.3 V, f(XCIN)=32 kHz, in stop mode)
Operating ambient temperature		-20 to 85°C, -40 to 85°C (option)
Package		144-pin plastic mold QFP

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
 2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
- All options are on request basis.

Table 1.2 M32C/81 Group Performance (100-Pin Package)

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, V _{CC} =4.2 V to 5.5 V) 50ns (f(BCLK)=20MHz, V _{CC} =3.0 V to 5.5 V)
	Operation mode	Single-chip, memory expansion and microprocessor modes
	Memory space	16 Mbytes
	Memory capacity	See Table 1.3.
Peripheral function	Port	87 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generation function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IE bus ⁽¹⁾)
	Serial I/O	5 channels Clock synchronous, Clock asynchronous, IEBus ⁽¹⁾ (option), I ² C bus ⁽²⁾ (option)
	CAN module	1 channel Supporting CAN 2.0B specification
	A-D converter	10-bit A-D converter: 1 circuit Input : 26 channels
	D-A converter	8-bit D-A converter: 2 circuits
	DMAC	4 channels
	DMAC II	Can be activated by all relocatable vector interrupt factors Immediate transfer, arithmetic transfer and chain transfer functions
	CRC calculation circuit	CRC-CCITT
	X-Y converter	16 bits X 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock generation circuit, sub clock generation circuit, ring oscillator, PLL frequency synthesizer The above circuits include an internal feedback resistor and external ceramic resonator/crystal oscillator. Main clock oscillator stop detect function
Electric characteristics	Supply voltage	4.2 V to 5.5 V (f(XIN)=32 MHz) 3.0 V to 5.5 V (f(XIN)=20 MHz, through VDC) 3.0 V to 3.6 V (f(XIN)=20 MHz, not through VDC)
	Power consumption	28 mA (V _{CC} =5 V, f(BCLK)=32 MHz) 17 mA (V _{CC} =3.3 V, f(BCLK)=20 MHz) 470 μ A (V _{CC} =5 V, f(XCIN)=32 kHz, in wait mode) 340 μ A (V _{CC} =3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 μ A (V _{CC} =3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 μ A (V _{CC} =5 V, f(XCIN)=32 kHz, in stop mode) 0.4 μ A (V _{CC} =3.3 V, f(XCIN)=32 kHz, in stop mode)
Operating ambient temperature		-20 to 85°C -40 to 85°C (option)
Package		100-pin plastic mold QFP

NOTES:

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All options are on request basis.

1.4 Block Diagram

Figure 1.1 shows a block diagram of the M32C/81 group.

The M32C/81 group microcomputer contains ROM and RAM as memory to store instructions and data, CPU to execute calculations and peripheral functions as interrupt, timer, serial I/O, D-A converter, DMAC, CRC calculation circuit, A-D converter, DRAMC, intelligent I/O and I/O ports.

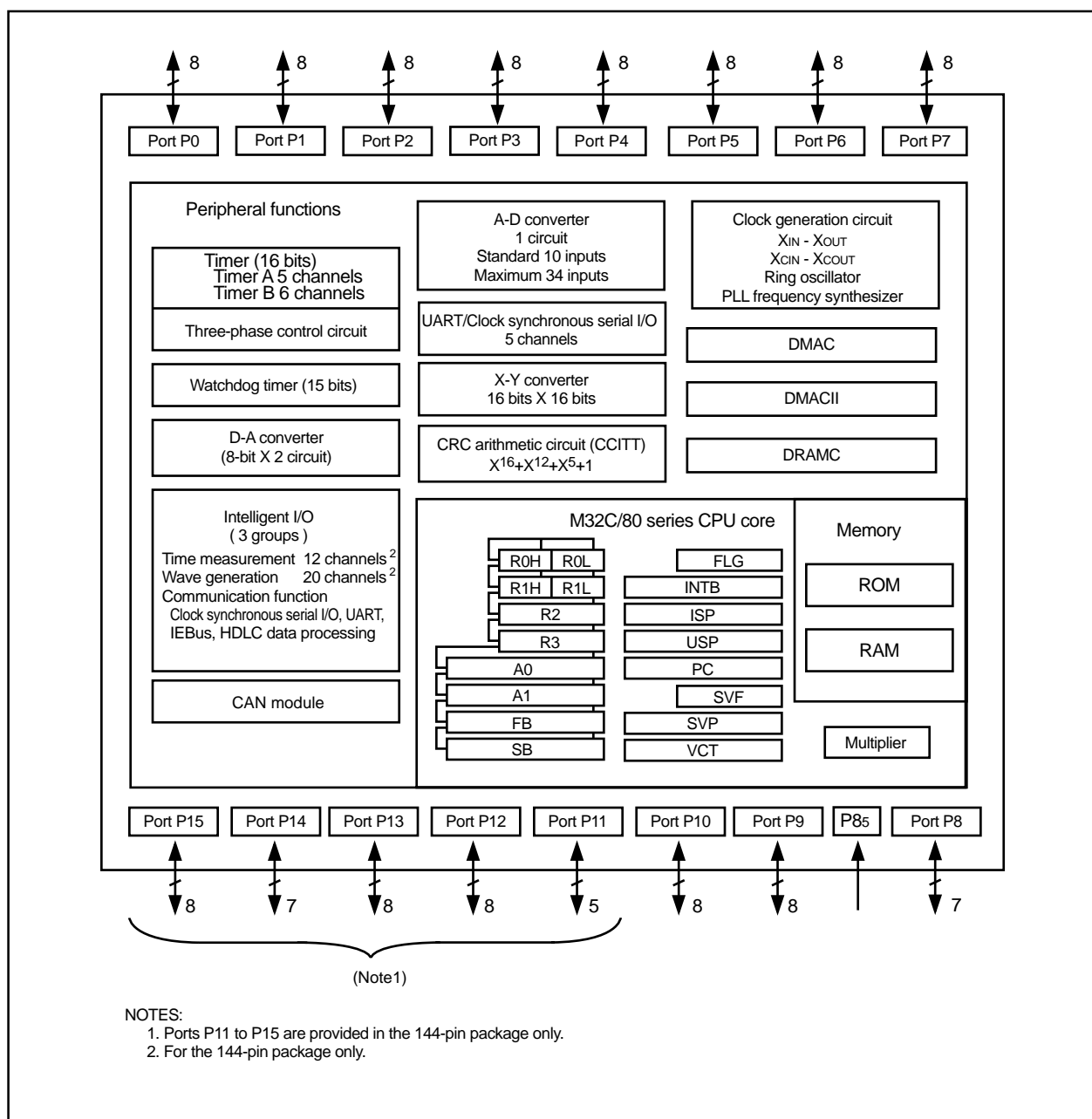


Figure 1.1 M32C/81 Group Block Diagram

1.5 Product Information

Renesas plans to release the following products in the M32C/81 group:

(1) Support for the masked ROM version

(2) ROM/RAM capacity

(3) Package

100P6S-A : Plastic molded QFP

100P6Q-A : Plastic molded QFP

144P6Q-A : Plastic molded QFP

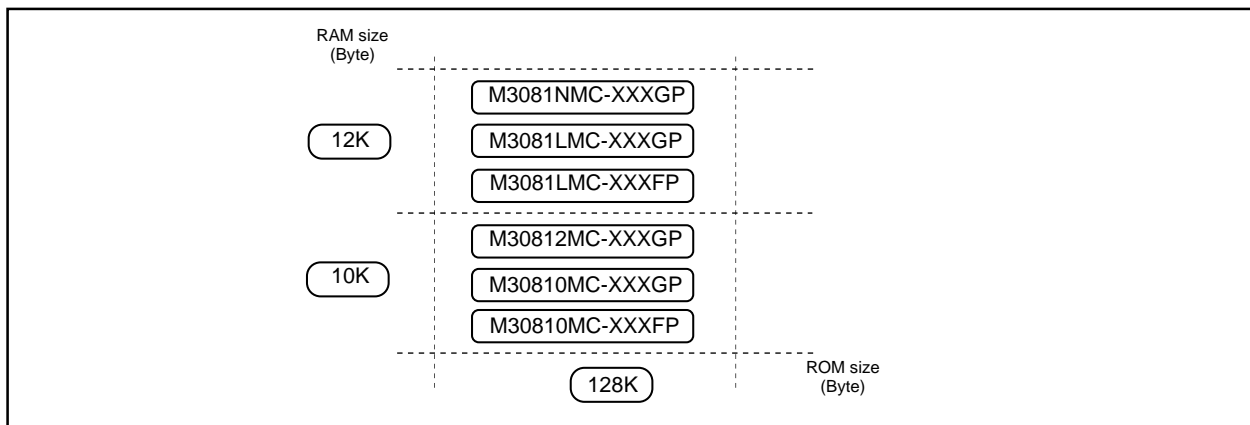


Figure 1.2 ROM/RAM Capacity

Table 1.3 M32C/81 Group

As of January, 2003

Type number	ROM capacity	RAM capacity	Package type	Remarks
M30810MC-XXXFP **	128 Kbytes	10 Kbytes	100P6S-A	Masked ROM
M30810MC-XXXGP **			100P6Q-A	
M30812MC-XXXGP **			144P6Q-A	
M3081LMC-XXXFP **		12 Kbytes	100P6S-A	
M3081LMC-XXXGP **			100P6Q-A	
M3081NMC-XXXGP **			144P6Q-A	

** : Under planning

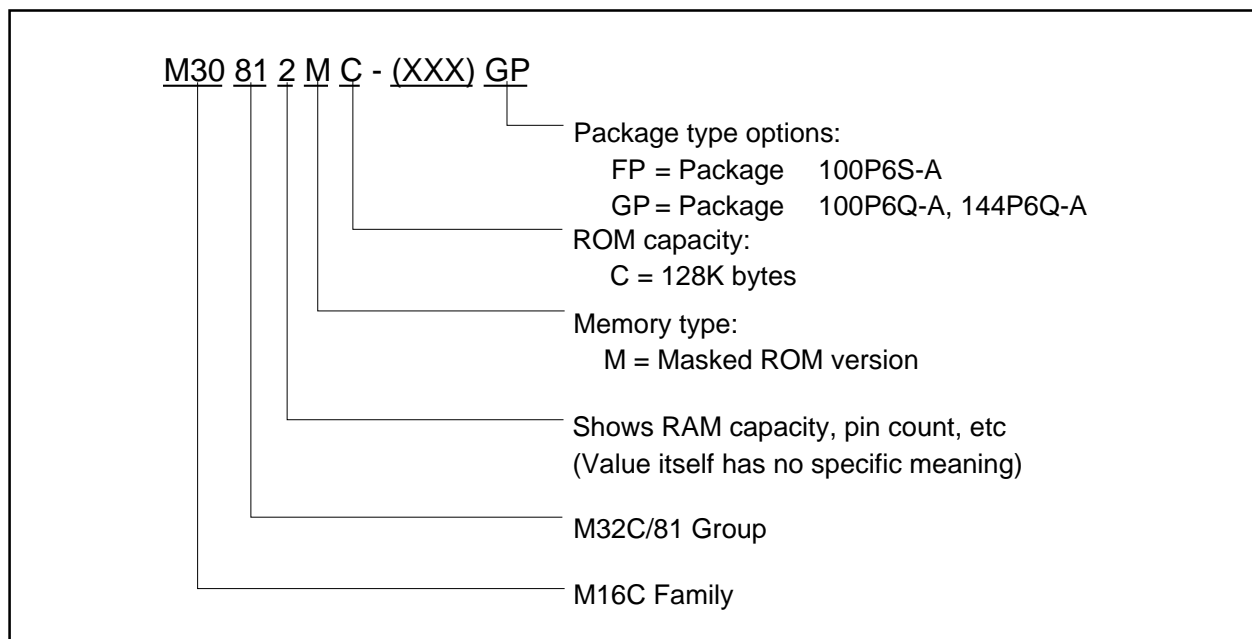


Figure 1.3 Product Numbering System

1.6 Pin Assignments

Figures 1.4 to 1.6 show pin assignments (top view).

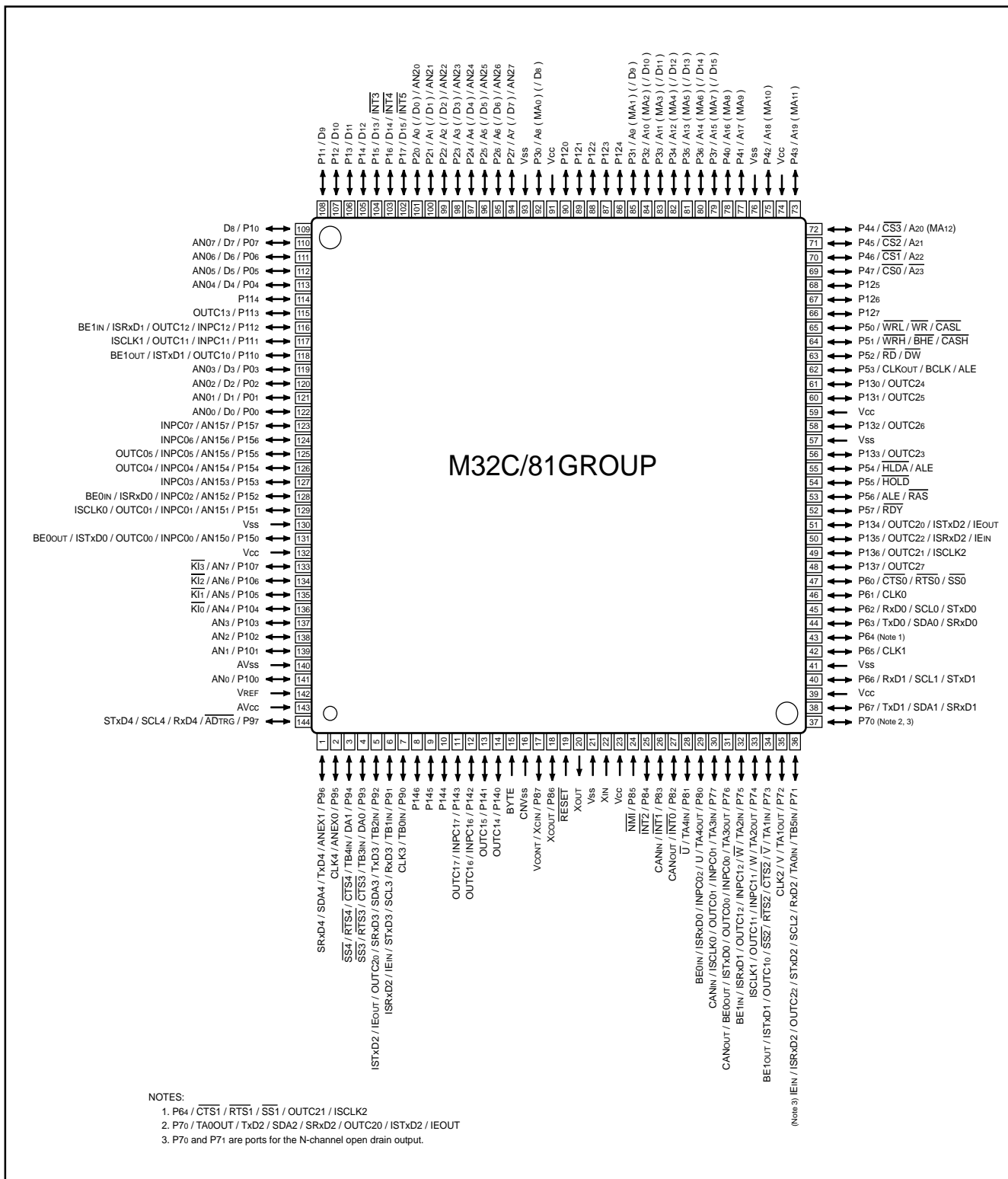


Figure 1.4 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
1		P96			TxD4/SDA4/SRx4		ANEX1	
2		P95			CLK4		ANEX0	
3		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5		P92		TB2IN	TxD3/SDA3/SRx3	OUTC20/IEOUT/ISTxD2		
6		P91		TB1IN	RxD3/SCL3/STxD3	IEIN/ISRxD2		
7		P90		TB0IN	CLK3			
8		P146						
9		P145						
10		P144						
11		P143				INPC17/OUTC17		
12		P142				INPC16/OUTC16		
13		P141				OUTC15		
14		P140				OUTC14		
15	BYTE							
16	CNVSS							
17	XCIN/VCONT	P87						
18	XCOUT	P86						
19	RESET							
20	XOUT							
21	VSS							
22	XIN							
23	VCC							
24		P85	NMI					
25		P84	INT2					
26		P83	INT1		CANIN			
27		P82	INT0		CANOUT			
28		P81		TA4IN/U				
29		P80		TA4OUT/U		INPC02/ISRxD0/BE0IN		
30		P77		TA3IN	CANIN	INPC01/OUTC01/ISCLK0		
31		P76		TA3OUT	CANOUT	INPC00/OUTC00/ISTxD0/BE0OUT		
32		P75		TA2IN/W		INPC12/OUTC12/ISRxD1/BE1IN		
33		P74		TA2OUT/W		INPC11/OUTC11/ISCLK1		
34		P73		TA1IN/V	CTS2/RTS2/SS2	OUTC10/ISTxD1/BE1OUT		
35		P72		TA1OUT/V	CLK2			
36		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	OUTC22/ISRxD2/IEIN		
37		P70		TA0OUT	TxD2/SDA2/SRx2	OUTC20/ISTxD2/IEOUT		
38		P67			TxD1/SDA1/SRx1			
39	VCC							
40		P66			RxD1/SCL1/STxD1			
41	VSS							
42		P65			CLK1			
43		P64			CTS1/RTS1/SS1	OUTC21/ISCLK2		
44		P63			TxD0/SDA0/SRx0			
45		P62			RxD0/SCL0/STxD0			
46		P61			CLK0			
47		P60			CTS0/RTS0/SS0			
48		P137				OUTC27		

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
49		P13 ₆				OUTC2 ₁ /ISCLK2		
50		P13 ₅				OUTC2 ₂ /ISRxD2/IE _{IN}		
51		P13 ₄				OUTC2 ₀ /ISTxD2/IE _{OUT}		
52		P5 ₇						RDY
53		P5 ₆						ALE/RAS
54		P5 ₅						HOLD
55		P5 ₄						HLDA/ALE
56		P13 ₃				OUTC2 ₃		
57	V _{SS}							
58		P13 ₂				OUTC2 ₆		
59	V _{CC}							
60		P13 ₁				OUTC2 ₅		
61		P13 ₀				OUTC2 ₄		
62		P5 ₃						CLK _{OUT} /BCLK/ALE
63		P5 ₂						RD/DW
64		P5 ₁						WRH/BHE/CASH
65		P5 ₀						WRL/WR/CASL
66		P12 ₇						
67		P12 ₆						
68		P12 ₅						
69		P4 ₇						CS ₀ /A ₂₃
70		P4 ₆						CS ₁ /A ₂₂
71		P4 ₅						CS ₂ /A ₂₁
72		P4 ₄						CS ₃ /A ₂₀ (MA ₁₂)
73		P4 ₃						A ₁₉ (MA ₁₁)
74	V _{CC}							
75		P4 ₂						A ₁₈ (MA ₁₀)
76	V _{SS}							
77		P4 ₁						A ₁₇ (MA ₉)
78		P4 ₀						A ₁₆ (MA ₈)
79		P3 ₇						A ₁₅ (MA ₇)/(D ₁₅)
80		P3 ₆						A ₁₄ (MA ₆)/(D ₁₄)
81		P3 ₅						A ₁₃ (MA ₅)/(D ₁₃)
82		P3 ₄						A ₁₂ (MA ₄)/(D ₁₂)
83		P3 ₃						A ₁₁ (MA ₃)/(D ₁₁)
84		P3 ₂						A ₁₀ (MA ₂)/(D ₁₀)
85		P3 ₁						A ₉ (MA ₁)/(D ₉)
86		P12 ₄						
87		P12 ₃						
88		P12 ₂						
89		P12 ₁						
90		P12 ₀						
91	V _{CC}							
92		P3 ₀						A ₈ (MA ₀)/(D ₈)
93	V _{SS}							
94		P2 ₇					AN2 ₇	A ₇ (D ₇)
95		P2 ₆					AN2 ₆	A ₆ (D ₆)
96		P2 ₅					AN2 ₅	A ₅ (D ₅)

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	$\overline{\text{INT5}}$					D15
103		P16	$\overline{\text{INT4}}$					D14
104		P15	$\overline{\text{INT3}}$					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157				INPC07	AN157	
124		P156				INPC06	AN156	
125		P155				INPC05/OUTC05	AN155	
126		P154				INPC04/OUTC04	AN154	
127		P153				INPC03	AN153	
128		P152				INPC02/ISRxD0/BE0IN	AN152	
129		P151				INPC01/OUTC01/ISCLK0	AN151	
130	Vss							
131		P150				INPC00/OUTC00/ISTxD0/BE0OUT	AN150	
132	Vcc							
133		P107	$\overline{\text{KI3}}$				AN7	
134		P106	$\overline{\text{KI2}}$				AN6	
135		P105	$\overline{\text{KI1}}$				AN5	
136		P104	$\overline{\text{KI0}}$				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVss							
141		P100					AN0	
142							VREF	
143	AVcc							
144		P97			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$	

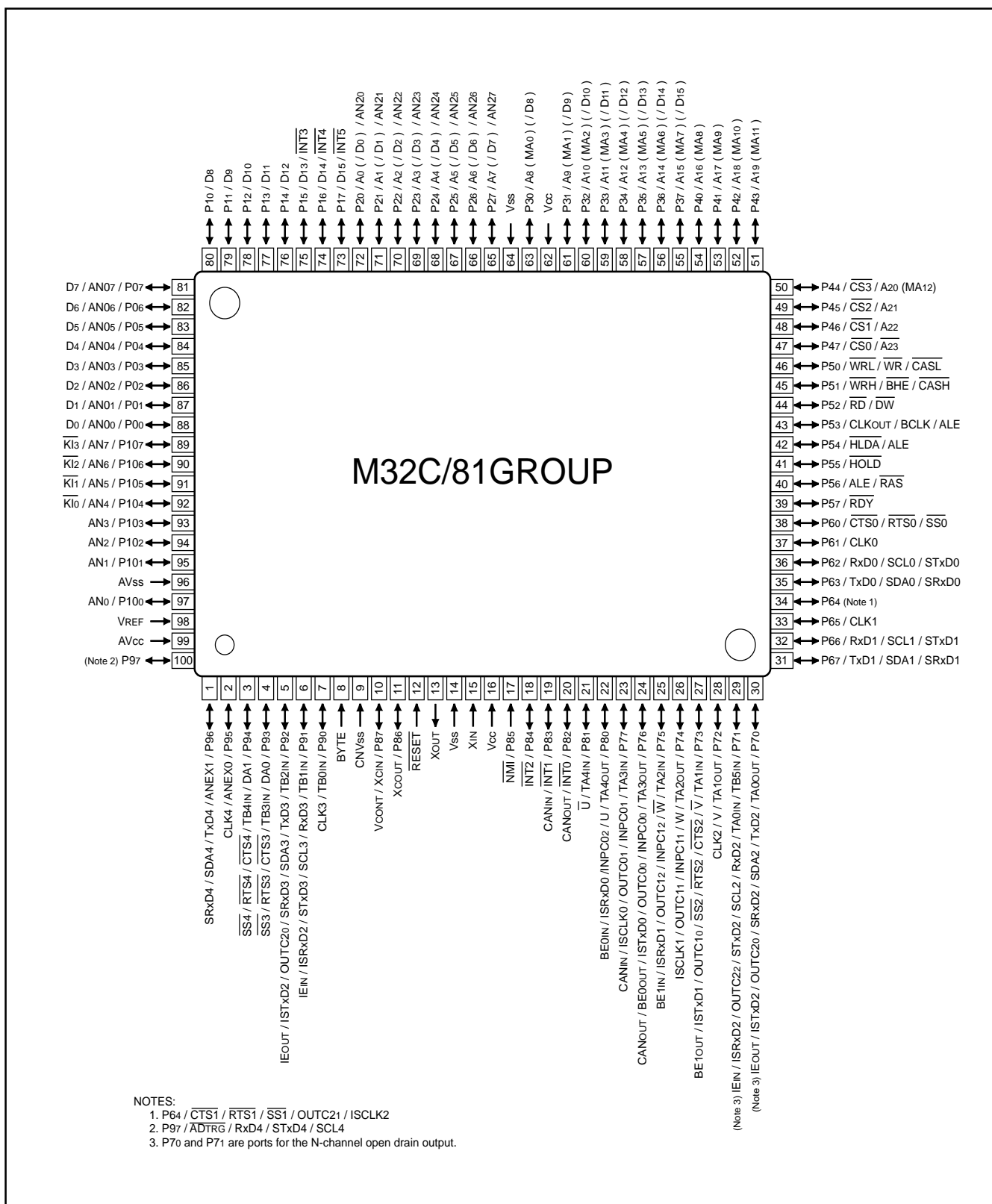


Figure 1.5 Pin assignment for 100-Pin Package

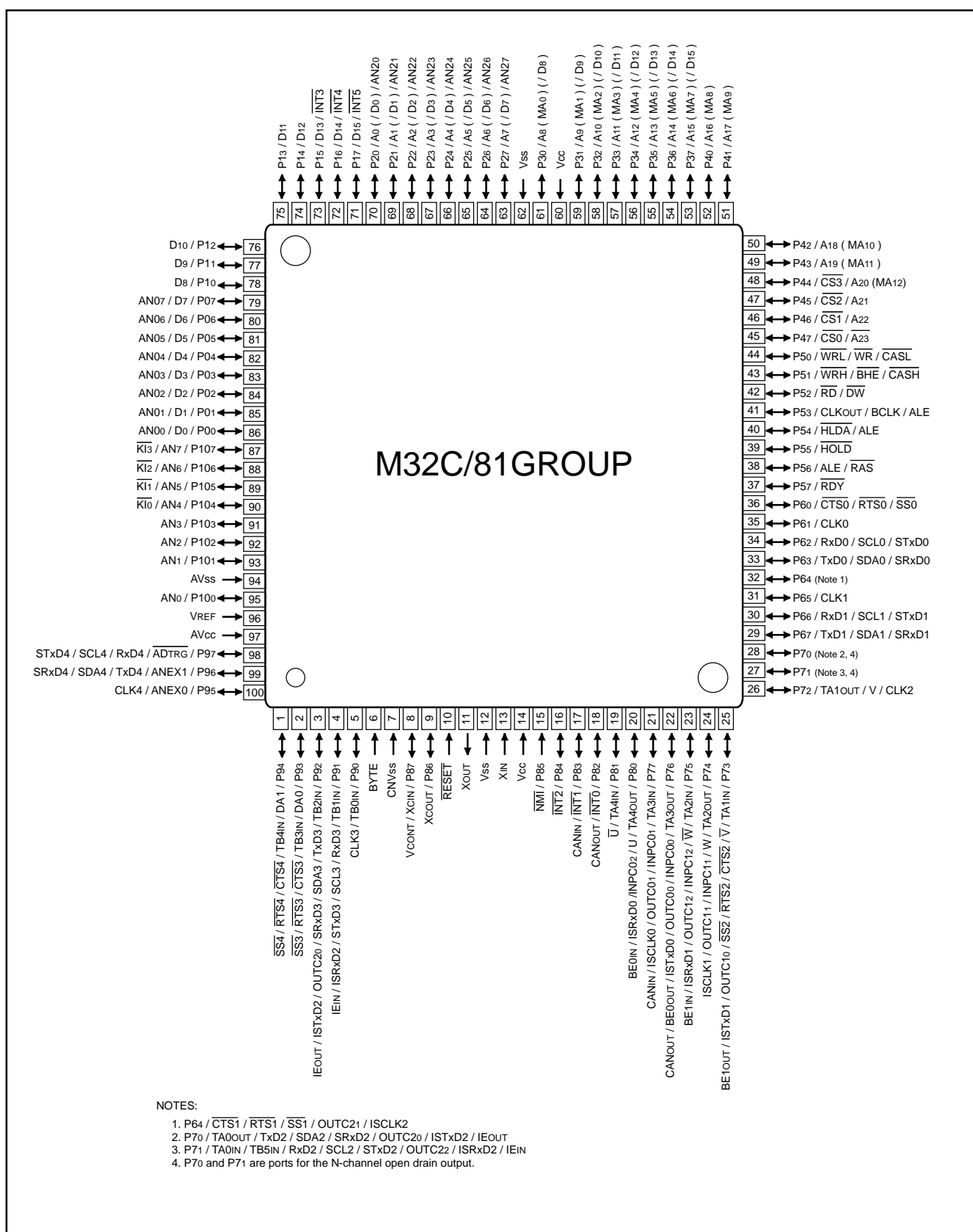


Figure 1.6 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
1	99		P9 ₆			TxD4/SDA4/SRxD4		ANEX1	
2	100		P9 ₅			CLK4		ANEX0	
3	1		P9 ₄		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P9 ₃		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P9 ₂		TB2IN	TxD3/SDA3/SRxD3	OUTC2 ₀ /IE _{OUT} /ISTxD2		
6	4		P9 ₁		TB1IN	RxD3/SCL3/STxD3	IEIN/ISRxD2		
7	5		P9 ₀		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVss							
10	8	X _{CIN} /V _{CONT}	P8 ₇						
11	9	X _{COU} T	P8 ₆						
12	10	RESET							
13	11	X _{OUT}							
14	12	V _{SS}							
15	13	X _{IN}							
16	14	V _{CC}							
17	15		P8 ₅	NMI					
18	16		P8 ₄	INT2					
19	17		P8 ₃	INT1		CANIN			
20	18		P8 ₂	INT0		CANOUT			
21	19		P8 ₁		TA4IN/ \bar{U}				
22	20		P8 ₀		TA4OUT/U		INPC0 ₂ /ISRxD0/BE0IN		
23	21		P7 ₇		TA3IN	CANIN	INPC0 ₁ /OUTC0 ₁ /ISCLK0		
24	22		P7 ₆		TA3OUT	CANOUT	INPC0 ₀ /OUTC0 ₀ /ISTxD0/BE0OUT		
25	23		P7 ₅		TA2IN/ \bar{W}		INPC1 ₂ /OUTC1 ₂ /ISRxD1/BE1IN		
26	24		P7 ₄		TA2OUT/W		INPC1 ₁ /OUTC1 ₁ /ISCLK1		
27	25		P7 ₃		TA1IN/ \bar{V}	CTS2/RTS2/SS2	OUTC1 ₀ /ISTxD1/BE1OUT		
28	26		P7 ₂		TA1OUT/V	CLK2			
29	27		P7 ₁		TB5IN/TA0IN	RxD2/SCL2/STxD2	OUTC2 ₂ /ISRxD2/IEIN		
30	28		P7 ₀		TA0OUT	TxD2/SDA2/SRxD2	OUTC2 ₀ /ISTxD2/IEOUT		
31	29		P6 ₇			TxD1/SDA1/SRxD1			
32	30		P6 ₆			RxD1/SCL1/STxD1			
33	31		P6 ₅			CLK1			
34	32		P6 ₄			CTS1/RTS1/SS1	OUTC2 ₁ /ISCLK2		
35	33		P6 ₃			TxD0/SDA0/SRxD0			
36	34		P6 ₂			RxD0/SCL0/STxD0			
37	35		P6 ₁			CLK0			
38	36		P6 ₀			CTS0/RTS0/SS0			
39	37		P5 ₇						RDY
40	38		P5 ₆						ALE/RAS
41	39		P5 ₅						HOLD
42	40		P5 ₄						HLDA/ALE
43	41		P5 ₃						CLKout/BCLK/ALE
44	42		P5 ₂						RD/DW
45	43		P5 ₁						WRH/BHE/CASH
46	44		P5 ₀						WRL/WR/CASL
47	45		P4 ₇						CS0/A23
48	46		P4 ₆						CS1/A22
49	47		P4 ₅						CS2/A21
50	48		P4 ₄						CS3/A20(MA ₁₂)

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package pin No		Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
51	49		P4 ₃						A19(MA11)
52	50		P4 ₂						A18(MA10)
53	51		P4 ₁						A17(MA9)
54	52		P4 ₀						A16(MA8)
55	53		P3 ₇						A15(MA7)/(D15)
56	54		P3 ₆						A14(MA6)/(D14)
57	55		P3 ₅						A13(MA5)/(D13)
58	56		P3 ₄						A12(MA4)/(D12)
59	57		P3 ₃						A11(MA3)/(D11)
60	58		P3 ₂						A10(MA2)/(D10)
61	59		P3 ₁						A9(MA1)/(D9)
62	60	Vcc							
63	61		P3 ₀						A8(MA0)/(D8)
64	62	Vss							
65	63		P2 ₇					AN2 ₇	A7(/D7)
66	64		P2 ₆					AN2 ₆	A6(/D6)
67	65		P2 ₅					AN2 ₅	A5(/D5)
68	66		P2 ₄					AN2 ₄	A4(/D4)
69	67		P2 ₃					AN2 ₃	A3(/D3)
70	68		P2 ₂					AN2 ₂	A2(/D2)
71	69		P2 ₁					AN2 ₁	A1(/D1)
72	70		P2 ₀					AN2 ₀	A0(/D0)
73	71		P1 ₇	INT5					D15
74	72		P1 ₆	INT4					D14
75	73		P1 ₅	INT3					D13
76	74		P1 ₄						D12
77	75		P1 ₃						D11
78	76		P1 ₂						D10
79	77		P1 ₁						D9
80	78		P1 ₀						D8
81	79		P0 ₇					AN0 ₇	D7
82	80		P0 ₆					AN0 ₆	D6
83	81		P0 ₅					AN0 ₅	D5
84	82		P0 ₄					AN0 ₄	D4
85	83		P0 ₃					AN0 ₃	D3
86	84		P0 ₂					AN0 ₂	D2
87	85		P0 ₁					AN0 ₁	D1
88	86		P0 ₀					AN0 ₀	D0
89	87		P10 ₇	KI ₃				AN7	
90	88		P10 ₆	KI ₂				AN6	
91	89		P10 ₅	KI ₁				AN5	
92	90		P10 ₄	KI ₀				AN4	
93	91		P10 ₃					AN3	
94	92		P10 ₂					AN2	
95	93		P10 ₁					AN1	
96	94	AVss							
97	95		P10 ₀					AN0	
98	96							VREF	
99	97	AVcc							
100	98		P9 ₇			RxD4/SCL4/STxD4		ADTRG	

1.7 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Symbol	Function	I/O type	Description
Vcc	Power supply input	I	Apply 3.0 to 5.5 V to the Vcc pins.
Vss		I	Apply the Vss pin to 0 V.
CNVss	CNVss	I	Switches processor mode. Connect this pin to Vss to start up in single-chip mode (memory expansion mode). Connect this pin to Vcc to start up in microprocessor mode.
RESET	Reset input	I	The microcomputer is in a reset state when applying "L" to the RESET pin.
XIN	Clock input	I	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use an externally generated clock, input the clock to XIN and leave XOUT open.
XOUT	Clock output	O	
BYTE	Input to select external data bus	I	Switches the data bus in external memory space 3. The data bus is 16 bits long when the BYTE pin is held "L" and 8 bits long when the BYTE pin is held "H". Set it to either one. Connect this pin to Vss when an external bus is not used.
AVcc	Analog power supply input	I	Applies the power supply for the A-D converter and D-A converter. Connect this pin to Vcc.
AVss	Analog power supply input	I	Applies the power supply for the A-D converter and D-A converter. Connect this pin to Vss.
VREF	Reference voltage input	I	Applies the reference voltage for the A-D converter.
P00 to P07	I/O port P0	I/O	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port in single-chip mode can be set for a pull-up or for no pull-up in 4-bit unit by program. When these pins are used as bus control pins in memory expansion mode and microprocessor mode, internal pull-up resistor cannot be selected. Ports used as input ports can be set for a pull-up or for no pull-up in these modes above.
D0 to D7	Data bus	I/O	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
AN00 to AN07	Analog input pin	I	Analog input pins for the A-D converter
P10 to P17	I/O port P1	I/O	8-bit I/O ports having equivalent functions to P0
INT3 to INT5	INT interrupt input pin	I	Input pins for the INT interrupt
D8 to D15	Data bus	I/O	Inputs and outputs data (D8 to D15) when these pins are set as the data bus.
P20 to P27	I/O port P2	I/O	8-bit I/O ports having equivalent functions to P0
A0 to A7	Address bus	O	Outputs 8 low-order address bits (A0 to A7).
A0/D0 to A7/D7	Address bus/data bus	I/O	Inputs and outputs data (D0 to D7) and output 8 low-order address bits (A0 to A7) by time-sharing when these pins are set as the multiplexed bus.
AN20 to AN27	Analog input pin	I	Analog input pins for A-D converter
P30 to P37	I/O port P3	I/O	8-bit I/O ports having equivalent functions to P0
A8 to A15	Address bus	O	Outputs 8 middle-order address bits (A8 to A15).
A8/D8 to A15/D15	Address bus/data bus	I/O	Inputs and outputs data (D8 to D15) and output 8 middle-order address bits (A8 to A15) by time-sharing when external 16-bit data bus is set as the multiplexed bus.
MA0 to MA7	Address bus	O	Outputs row addresses and column addresses by time-sharing when accessing the DRAM area.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P40 to P47	I/O port P4	I/O	8-bit I/O ports having equivalent functions to P0
A16 to A22, A23	Address bus	O	Outputs 8 high-order address bits (A16 to A22, A23). The highest-order bit (A23) inverted is also output.
CS0 to CS3	Chip-select signal	O	Outputs CS0 to CS3 signals. CS0 to CS3 are chip-select signals to specify an external space.
MA8 to MA12	Address bus	O	Outputs row addresses and column addresses by time-sharing when accessing the DRAM area.
P50 to P57	I/O port P5	I/O	8-bit I/O ports having equivalent functions to P0
CLKOUT	Clock output	O	Outputs the main clock divided by 8 or divided by 32 or the clock having the same frequency as the sub clock from P53.
WRL WR WRH BHE RD BCLK HLDA HOLD ALE RDY	Bus control pin	O O O O O O O I O I	Outputs WRL, WRH, (WR, BHE), RD, BCLK, HLDA and ALE signals. WRL and WRH or BHE and WR can be switched by program. ■ WRL, WRH and RD are selected The WRL signal becomes "L" by writing data to an even address in an external memory space. The WRH signal becomes "L" by writing data to an odd address in an external memory space. The RD pin signal becomes "L" by reading data in an external memory space. ■ WR, BHE and RD are selected The WR signal becomes "L" by writing data to an external memory space. The RD signal becomes "L" by reading data in an external memory space. The BHE signal becomes "L" by accessing an odd address. Select WR, BHE and RD for an external 8-bit data bus. While the HOLD pin is held "L", the microcomputer is placed in a hold state. In a hold state, HLDA outputs a "L" signal. ALE is a signal to latch the address. While applying a "L" signal to the RDY pin, the microcomputer is placed in a wait state.
DW CASL CASH RAS	DRAM bus control pin	O O O O	The DW signal becomes "L" by writing data to the DRAM area. CASL and CASH are signals to indicate a timing to latch column addresses. The CASL signal becomes "L" by accessing an even address. The CASH signal becomes "L" by accessing an odd address. RAS is a signal to latch row addresses.
P60 to P67	I/O port P6	I/O	8-bit I/O ports having equivalent functions to P0
CTS0, CTS1 RTS0, RTS1 SS0, SS1 CLK0, CLK1 RxD0, RxD1 SCL0, SCL1 STxD0, STxD1 TxD0, TxD1 SDA0, SDA1 SRxD0, SRxD1	UART pin	I O I I/O I I/O O O O O I	I/O pins for UART0 (P60 to P63) and UART1 (P64 to P67)
ISCLK2 OUTC21	Intelligent I/O pin	I/O O	ISCLK2 inputs and outputs the clock for the intelligent I/O communication function. OUTC21 outputs the clock for the waveform generation function.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P70 to P77	I/O port P7	I/O	8-bit I/O ports having equivalent functions to P0 (except P70 and P71 for the N-channel open drain output.)
TA0OUT to TA3OUT TA0IN to TA3IN	Timer A pin	I/O I	I/O ports for the timer A0 to timer A3
TB5IN	Timer B pin	I	Input pin for the timer B5
V, \bar{V}	Three-phase motor	O	V-phase output pin
W, \bar{W}	control output pin		W-phase output pin
CTS2 RTS2 SS2 CLK2 RxD2 SCL2 STxD2 TxD2 SDA2 SRxD2	UART pin	I O I I/O I I/O O O O I	I/O pins for UART2
INPC00, INPC01 INPC11, INPC12 OUTC00, OUTC01 OUTC10 to OUTC12 OUTC20 to OUTC22 ISCLK0, ISCLK1 ISTxD0 to ISTxD2 ISRxD1, ISRxD2 IEOUT IEIN BE0OUT BE1OUT BE1IN	Intelligent I/O pin	I O I/O O I O I O	INPC10 to INPC14, INPC16 and INPC17 are input pins for the time measurement function. OUTC10 to OUTC14, OUTC16 and OUTC17 are output pins for the waveform generation function. ISCLK0 and ISCLK1 input and output the clock for the intelligent I/O communication function. ISRxD1 and BE1IN input received data for the intelligent I/O communication function. ISTxD0 and ISTxD1 and BE1OUT output transmit data for the intelligent I/O communication function.
CAN0OUT CAN0IN	CAN pin	O I	I/O pins for the CAN communication function

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P80 to P84, P86, P87	I/O port P8	I/O	I/O ports having equivalent functions to P0
XCIN	Sub clock	I	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
XCOUT		O	
VCONT	Low-pass filter connect pin for PLL frequency synthesizer pin		Connects the low-pass filter to the VCONT pin to use the PLL frequency synthesizer. Connect P86 to VSS to make a PLL frequency stable.
TA4OUT	Timer A pin	I	I/O pins for the timer A4
TA4IN		O	
U, \bar{U}	Three-phase motor control output pin	O	U-phase output pins
INT0 to INT2	INT interrupt input pin	I	Input pins for INT interrupt
INPC02	Intelligent I/O pin	I	INPC02 is an input pin for the time measurement function.
ISRxD0		I	OUTC30 and OUTC32 are output pins for the waveform generation function.
BE0IN		I	ISRxD0 and BE0IN input received data for the intelligent I/O communication function.
OUTC30		O	ISTxD3 outputs transmit data for the intelligent I/O communication function.
ISTxD3		O	ISRxD3 inputs received data for the intelligent I/O communication function.
OUTC32		O	
ISRxD3		I	
CANOUT	CAN pin	O	I/O pins for CAN communication function
CANIN		I	
P85/NMI	NMI interrupt input pin	I	Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P90 to P97	I/O port P9	I/O	8-bit I/O ports having equivalent functions P0. The PRCR register prevents PD9 and PS3 registers from rewriting.
TB0IN to TB4IN	Timer B pin	I	Input pins for timer B0 to B4
CTS3, CTS4 RTS3, RTS4 SS3, SS4 CLK3, CLK4 RxD3, RxD4 SCL3, SCL4 STxD3, STxD4 TxD3, TxD4 SDA3, SDA4 SRxD3, SRxD4	UART pin	I O I I/O I I/O O O O I	I/O pins for UART3 (P90 to P93) and UART4 (P94 to P97)
DA0, DA1	D-A output pin	O	Input pins for the D-A converter
ANEX0, ANEX1, ADTRG	A-D related pin	I/O I I	ANEX0 and ANEX1 are extended analog I/O pins for the A-D converter. ADTRG is an A-D trigger input pin.
OUTC20 ISTxD2 IEOUT IEIN ISRxD2	Intelligent I/O pin	O O O I I	OUTC20 is an output pin for the waveform generation function. ISTxD2 outputs transmit data for the intelligent I/O communication function. IEOUT outputs transmit data for the intelligent I/O communication function or in IE mode. IEIN outputs transmit data for the intelligent I/O communication function or in IE mode. ISRxD2 inputs received data for the intelligent I/O communication function.
P100 to P107	I/O port P10	I/O	8-bit I/O ports having equivalent functions to P0
KI0 to KI3	Key input interrupt pin	I	Input pins for the key input interrupt
AN0 to AN7	Analog input pin	I	Analog I/O pins for the A-D converter

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Symbol	Function	I/O type	Description
P110 to P117	I/O port P11	I/O	8-bit I/O ports having equivalent functions to P0.
INPC11, INPC12	Intelligent I/O pin	I	INPC11 and INPC12 are input pins for the time measurement function.
OUTC10 to OUTC13		O	OUTC10 to OUTC13 are output pins for the waveform generation function.
ISCLK1		I/O	ISCLK1 inputs and outputs the clock for the intelligent I/O communication
ISRxD1		I	function.
BE1IN		I	ISRxD1 and BE1IN input received data for the intelligent I/O communication
ISTxD1		O	function.
BE1OUT		O	ISTxD1 and BE1OUT output received data for the intelligent I/O communication
			function.
P120 to P127	I/O port P12	I/O	8-bit I/O ports having equivalent functions to P0
OUTC30 to OUTC37	Intelligent I/O pin	O	OUTC30 to OUTC37 are output pins for the waveform generation function.
ISCLK3		I/O	ISCLK3 inputs and outputs the clock for the intelligent I/O communication
ISRxD3		I	function.
ISTxD3		O	ISRxD3 inputs received data for the intelligent I/O communication function.
			ISTxD3 outputs received data for the intelligent I/O communication function.
P130 to P137	I/O port P13	I/O	8-bit I/O ports having equivalent functions to P0
OUTC20 to OUTC27	Intelligent I/O pin	O	OUTC20 to OUTC27 are output pins for the waveform generation function.
ISCLK2		I/O	ISCLK2 inputs and outputs the clock for the intelligent I/O communication
ISRxD2		I	function.
BE1IN		I	ISRxD2 and BE1IN input received data for the intelligent I/O communication
ISTxD2		O	function.
BEOUT		O	ISTxD2 and BE1OUT output received data for the intelligent I/O communication
			function.
P140 to P146	I/O port P14	I/O	7-bit I/O ports having equivalent functions to P0
INPC16, INPC17	Intelligent I/O pin	I	INPC16 and INPC17 are input pins for the time measurement function.
OUTC14 to OUTC17		O	OUTC14 to OUTC17 are output pins for the waveform generation function.
P150 to P157	I/O port P15	I/O	8-bit I/O ports having equivalent functions to P0
INPC00 to INPC07	Intelligent I/O pin	I	INPC00 to INPC07 are input pins for the time measurement function.
OUTC00, OUTC01		O	OUTC00, OUTC01, OUTC04 and OUTC05 are output pins for the waveform
OUTC04, OUTC05			generation function.
ISCLK0		I/O	ISCLK0 inputs and outputs the clock for the intelligent I/O communication
ISRxD0		I	function.
BE0IN		I	ISRxD0 and BE0IN input received data for the intelligent I/O communication
ISTxD0		O	function.
BE0OUT		O	ISTxD0 and BE0OUT output received data for the intelligent I/O communication
			function.
AN150 to AN157	Analog input port	I	Analog I/O pins for the A-D converter

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

Eight registers (R0, R1, R2, R3, A0, A1, SB and FB) out of twenty-eight CPU registers comprise a register bank. Two sets of register banks are provided.

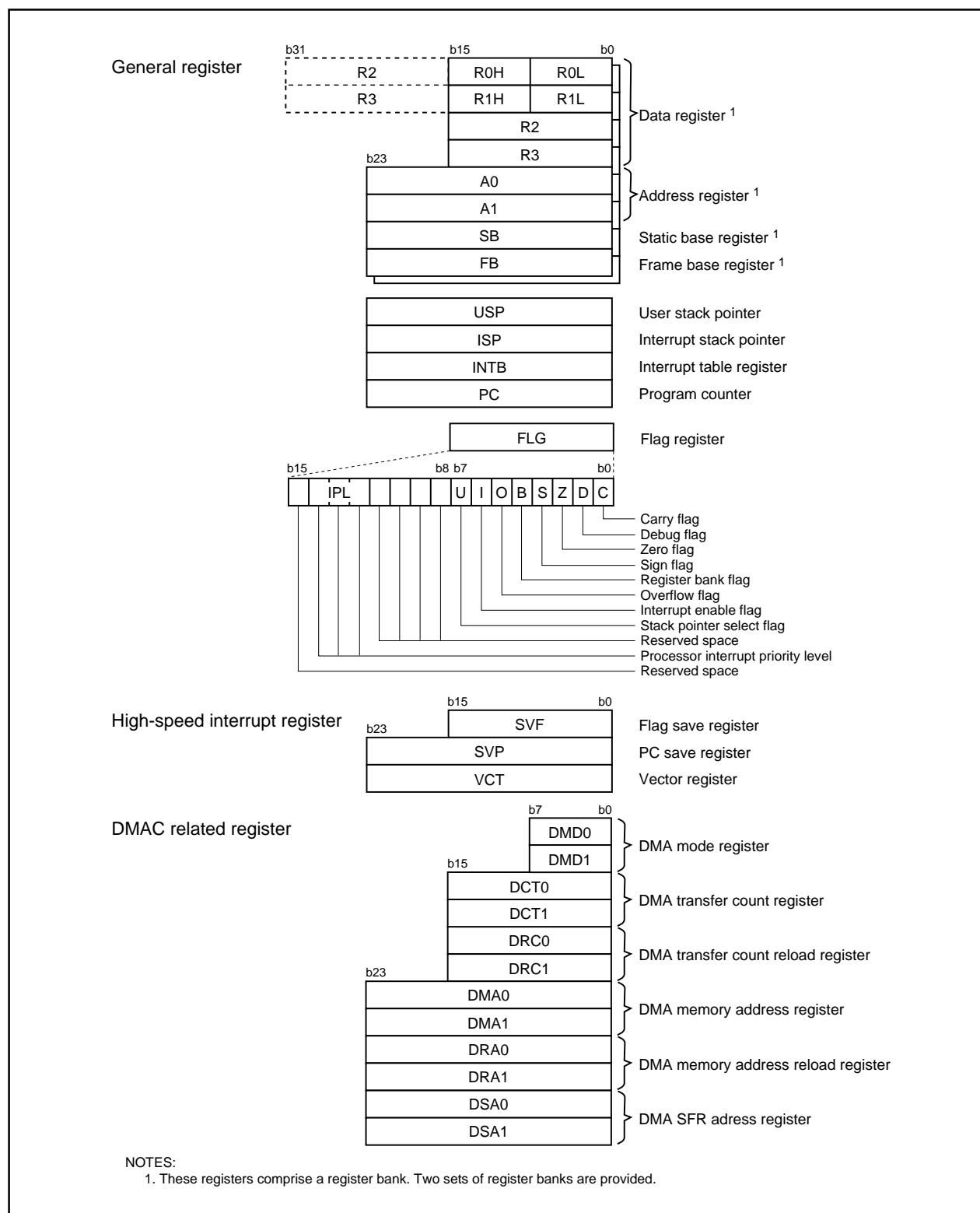


Figure 2.1 CPU Register

2.1 General Register

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to use each as 8-bit data registers.

R0 can be combined with R2 to use the combined one as a 32-bit data register (R2R0) as well as R3R1.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC is 24 bits wide. It indicates an address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register to indicate a starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

USP and ISP as the stack pointer are 24 bits wide. The U flag can switch USP to ISP and vice versa. Refer to "2.1.8 Flag Register (FLG)" about the U flag. Set USP and ISP in even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register to indicate a CPU state.

(1) Carry Flag (C)

The C flag indicates whether carry or borrow occurs after an instruction is executed.

(2) Debug Flag (D)

The D flag is for debug only. Set to "0".

(3) Zero Flag (Z)

The Z flag is set to "1" when a value of zero is obtained from an arithmetic calculation; otherwise "0".

(4) Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

(5) Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

(6) Overflow Flag (O)

The O flag is set to "1" when a result of an arithmetic operation overflows; otherwise "0".

(7) Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0" and is enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

(8) Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when the hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

(9) Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide. It assigns an interrupt priority levels from level 0 to level 7.

If a requested interrupt has a greater priority than IPL, the interrupt is enabled.

(10) Reserved Space

When write, set to "0" for the reserved space. When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated to the high-speed interrupt are as follows.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-associated Registers

Registers associated to DMAC are as follows.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/81 group.

The M32C/81 provides 16-Mbyte address space from addresses 000000₁₆ to FFFFFFF₁₆.

The internal ROM is allocated in lower addresses beginning with address FFFFFFF₁₆. For example, a 64-Kbyte internal ROM is allocated in addresses from FF0000₁₆ to FFFFFFF₁₆.

The fixed interrupt vectors are allocated in addresses from FFFDC₁₆ to FFFFFFF₁₆. It stores the starting address of each interrupt routine.

The internal RAM is allocated in higher addresses beginning with address 000400₁₆. For example, a 10-Kbyte internal RAM are allocated in addresses from 000400₁₆ to 002BFF₁₆. It stores data, calls the subroutine and becomes stacks when an interrupt is acknowledged.

The SFR is allocated in addresses from 000000₁₆ to 0003FF₁₆. The control registers for the peripheral function such as I/O port, A-D conversion, serial I/O, timer are allocated here. All addresses, which have nothing allocated within the SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated in addresses from FFFE00₁₆ to FFFDDB₁₆. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication "Software Manual" for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.

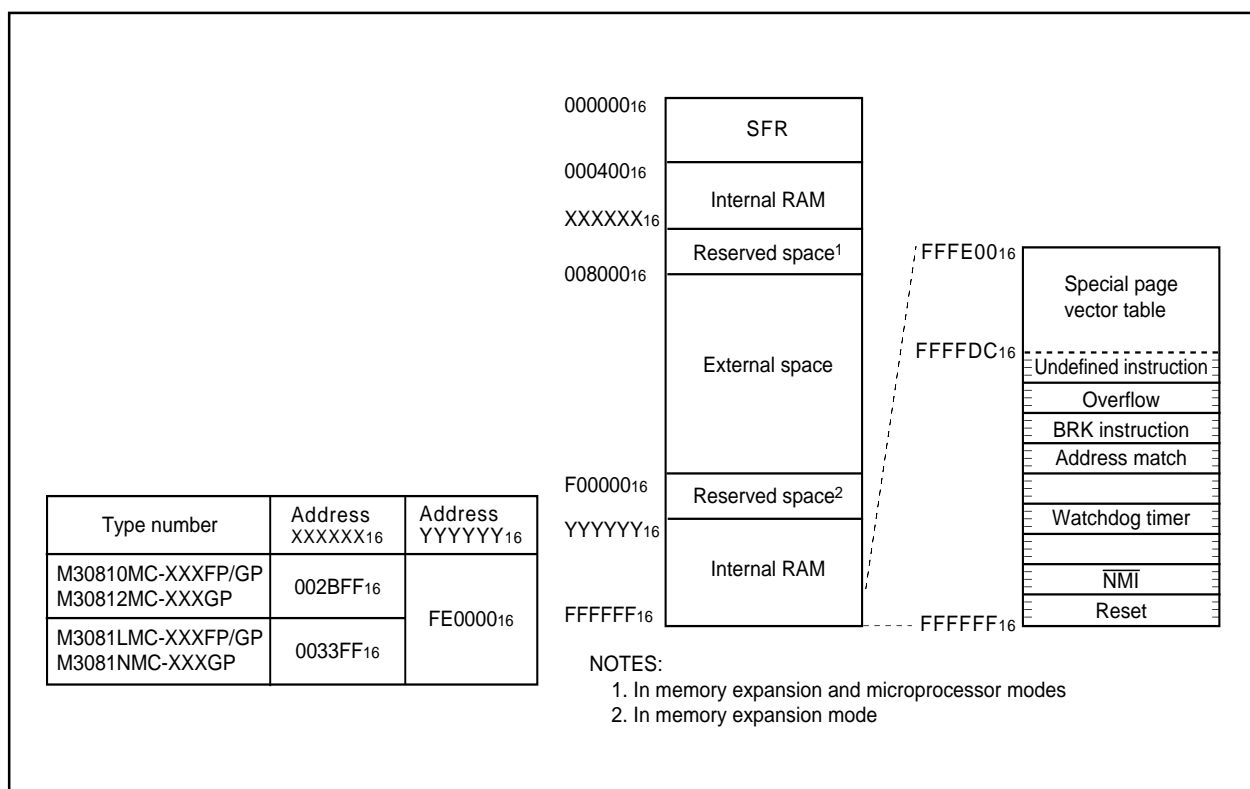


Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	1000 0000 ₂ (CNVss pin ="L") 0000 0011 ₂ (CNVss pin ="H")
0005 ₁₆	Processor mode register 1	PM1	0X00 0000 ₂
0006 ₁₆	System clock control register 0	CM0	0000 X000 ₂
0007 ₁₆	System clock control register 1	CM1	0010 0000 ₂
0008 ₁₆	Wait control register	WCR	1111 1111 ₂
0009 ₁₆	Address match interrupt enable register	AIER	XXXX 0000 ₂
000A ₁₆	Protect register	PRCR	XXXX 0000 ₂
000B ₁₆	External data bus width control register	DS	XXXX 1000 ₂ (BYTE pin ="L") XXXX 0000 ₂ (BYTE pin ="H")
000C ₁₆	Main clock division register	MCD	XXX0 1000 ₂
000D ₁₆	Oscillation stop detect register	CM2	0000 0000 ₂
000E ₁₆	Watchdog timer start register	WDTS	XX ₁₆
000F ₁₆	Watchdog timer control register	WDC	000X XXXX ₂
0010 ₁₆	Address match interrupt register 0	RMAD0	00 ₁₆
0011 ₁₆			00 ₁₆
0012 ₁₆			00 ₁₆
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	00 ₁₆
0015 ₁₆			00 ₁₆
0016 ₁₆			00 ₁₆
0017 ₁₆	VDC control register for PLL	PLV	XXXX XX01 ₂
0018 ₁₆	Address match interrupt register 2	RMAD2	00 ₁₆
0019 ₁₆			00 ₁₆
001A ₁₆			00 ₁₆
001B ₁₆	VDC control register 0	VDC0	0000 0000 ₂
001C ₁₆	Address match interrupt register 3	RMAD3	00 ₁₆
001D ₁₆			00 ₁₆
001E ₁₆			00 ₁₆
001F ₁₆	VDC control register 1	VDC1	0000 0000 ₂
0020 ₁₆	Emulator interrupt vector table register	EIAD	F00000 ₁₆
0021 ₁₆			
0022 ₁₆			
0023 ₁₆	Emulator interrupt detect register	EITD	XXXX XX00 ₂
0024 ₁₆	Emulator protect register	EPRR	XXXX XXX0 ₂
0025 ₁₆	Emulator protect control register	EMU	XXXX X000 ₂
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			

X: Indetermination

Blank columns are all reserved space. No access is allowed.

Users cannot use any symbols with *. No access is allowed.

Address	Register	Symbol	Value after RESET	
0030 ₁₆	ROM area set register	ROA	XXXX X000 ₂	*
0031 ₁₆	Debug monitor space set register	DBA	1111 0000 ₂	*
0032 ₁₆	Expanded space set register 0	EXA0	0000 0000 ₂	*
0033 ₁₆	Expanded space set register 1	EXA1	0000 0000 ₂	*
0034 ₁₆	Expanded space set register 2	EXA2	0000 0000 ₂	*
0035 ₁₆	Expanded space set register 3	EXA3	0000 0000 ₂	*
0036 ₁₆				
0037 ₁₆				
0038 ₁₆				
0039 ₁₆				
003A ₁₆				
003B ₁₆				
003C ₁₆				
003D ₁₆				
003E ₁₆				
003F ₁₆				
0040 ₁₆	DRAM control register	DRAMCONT	XXXX XXXX ₂	
0041 ₁₆	DRAM refresh interval set register	REFCNT	XX ₁₆	
0042 ₁₆				
0043 ₁₆				
0044 ₁₆				
0045 ₁₆				
0046 ₁₆				
0047 ₁₆				
0048 ₁₆				
0049 ₁₆				
004A ₁₆				
004B ₁₆				
004C ₁₆				
004D ₁₆				
004E ₁₆				
004F ₁₆				
0050 ₁₆				
0051 ₁₆				
0052 ₁₆				
0053 ₁₆				
0054 ₁₆				
0055 ₁₆				*
0056 ₁₆				*
0057 ₁₆				
0058 ₁₆				
0059 ₁₆				
005A ₁₆				
005B ₁₆				
005C ₁₆				
005D ₁₆				
005E ₁₆				
005F ₁₆				

X: Indetermination

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Users cannot use any symbols with *. No access is allowed.

Address	Register	Symbol	Value after RESET
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆	DMA0 interrupt control register	DM0IC	XXXX X0002
0069 ₁₆	Timer B5 interrupt control register	TB5IC	XXXX X0002
006A ₁₆	DMA2 interrupt control register	DM2IC	XXXX X0002
006B ₁₆	UART2 receive /ACK interrupt control register	S2RIC	XXXX X0002
006C ₁₆	Timer A0 interrupt control register	TA0IC	XXXX X0002
006D ₁₆	UART3 receive /ACK interrupt control register	S3RIC	XXXX X0002
006E ₁₆	Timer A2 interrupt control register	TA2IC	XXXX X0002
006F ₁₆	UART4 receive /ACK interrupt control register	S4RIC	XXXX X0002
0070 ₁₆	Timer A4 interrupt control register	TA4IC	XXXX X0002
0071 ₁₆	UART0/UART3 bus conflict detect interrupt control register	BCN0IC/BCN3IC	XXXX X0002
0072 ₁₆	UART0 receive/ACK interrupt control register	S0RIC	XXXX X0002
0073 ₁₆	A-D0 conversion interrupt control register	AD0IC	XXXX X0002
0074 ₁₆	UART1 receive/ACK interrupt control register	S1RIC	XXXX X0002
0075 ₁₆	Intelligent I/O interrupt control register 0	IIO0IC	XXXX X0002
0076 ₁₆	Timer B1 interrupt control register	TB1IC	XXXX X0002
0077 ₁₆	Intelligent I/O interrupt control register 2	IIO2IC	XXXX X0002
0078 ₁₆	Timer B3 interrupt control register	TB3IC	XXXX X0002
0079 ₁₆	Intelligent I/O interrupt control register 4	IIO4IC	XXXX X0002
007A ₁₆	INT5 interrupt control register	INT5IC	XX00 X0002
007B ₁₆	Intelligent I/O interrupt control register 6	IIO6IC	XXXX X0002
007C ₁₆	INT3 interrupt control register	INT3IC	XX00 X0002
007D ₁₆	Intelligent I/O interrupt control register 8	IIO8IC	XXXX X0002
007E ₁₆	INT1 interrupt control register	INT1IC	XX00 X0002
007F ₁₆	Intelligent I/O interrupt control register 10/ CAN interrupt 1 control register	IIO10IC CAN1IC	XXXX X0002
0080 ₁₆			
0081 ₁₆	Intelligent I/O interrupt control register 11/ CAN interrupt 2 control register	IIO11IC CAN2IC	XXXX X0002
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆	A-D1 conversion interrupt control register	AD1IC	XXXX X0002
0087 ₁₆			
0088 ₁₆	DMA1 interrupt control register	DM1IC	XXXX X0002
0089 ₁₆	UART2 transmit /NACK interrupt control register	S2TIC	XXXX X0002
008A ₁₆	DMA3 interrupt control register	DM3IC	XXXX X0002
008B ₁₆	UART3 transmit /NACK interrupt control register	S3TIC	XXXX X0002
008C ₁₆	Timer A1 interrupt control register	TA1IC	XXXX X0002
008D ₁₆	UART4 transmit /NACK interrupt control register	S4TIC	XXXX X0002
008E ₁₆	Timer A3 interrupt control register	TA3IC	XXXX X0002
008F ₁₆	UART2 bus conflict detect interrupt control register	BCN2IC	XXXX X0002

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Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 transmit /NACK interrupt control register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 bus conflict detect interrupt control register	BCN1IC/BCN4IC	XXXX X000 ₂
0092 ₁₆	UART1 transmit/NACK interrupt control register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key input interrupt control register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 interrupt control register	TB0IC	XXXX X000 ₂
0095 ₁₆	Intelligent I/O interrupt control register 1	IIO1IC	XXXX X000 ₂
0096 ₁₆	Timer B2 interrupt control register	TB2IC	XXXX X000 ₂
0097 ₁₆	Intelligent I/O interrupt control register 3	IIO3IC	XXXX X000 ₂
0098 ₁₆	Timer B4 interrupt control register	TB4IC	XXXX X000 ₂
0099 ₁₆	Intelligent I/O interrupt control register 5	IIO5IC	XXXX X000 ₂
009A ₁₆	INT4 interrupt control register	INT4IC	XX00 X000 ₂
009B ₁₆	Intelligent I/O interrupt control register 7	IIO7IC	XXXX X000 ₂
009C ₁₆	INT2 interrupt control register	INT2IC	XX00 X000 ₂
009D ₁₆	Intelligent I/O interrupt control register 9/ CAN interrupt 0 control register	IIO9IC CAN0IC	XXXX X000 ₂
009E ₁₆	INT0 interrupt control register	INT0IC	XX00 X000 ₂
009F ₁₆	Exit priority control register	RLVL	XX0X 0000 ₂
00A0 ₁₆	Interrupt request register 0	IIO0IR	0000 000X ₂
00A1 ₁₆	Interrupt request register 1	IIO1IR	0000 000X ₂
00A2 ₁₆	Interrupt request register 2	IIO2IR	0000 000X ₂
00A3 ₁₆	Interrupt request register 3	IIO3IR	0000 000X ₂
00A4 ₁₆	Interrupt request register 4	IIO4IR	0000 000X ₂
00A5 ₁₆	Interrupt request register 5	IIO5IR	0000 000X ₂
00A6 ₁₆	Interrupt request register 6	IIO6IR	0000 000X ₂
00A7 ₁₆	Interrupt request register 7	IIO7IR	0000 000X ₂
00A8 ₁₆	Interrupt request register 8	IIO8IR	0000 000X ₂
00A9 ₁₆	Interrupt request register 9	IIO9IR	0000 000X ₂
00AA ₁₆	Interrupt request register 10	IIO10IR	0000 000X ₂
00AB ₁₆	Interrupt request register 11	IIO11IR	0000 000X ₂
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt enable register 0	IIO0IE	0000 0000 ₂
00B1 ₁₆	Interrupt enable register 1	IIO1IE	0000 0000 ₂
00B2 ₁₆	Interrupt enable register 2	IIO2IE	0000 0000 ₂
00B3 ₁₆	Interrupt enable register 3	IIO3IE	0000 0000 ₂
00B4 ₁₆	Interrupt enable register 4	IIO4IE	0000 0000 ₂
00B5 ₁₆	Interrupt enable register 5	IIO5IE	0000 0000 ₂
00B6 ₁₆	Interrupt enable register 6	IIO6IE	0000 0000 ₂
00B7 ₁₆	Interrupt enable register 7	IIO7IE	0000 0000 ₂
00B8 ₁₆	Interrupt enable register 8	IIO8IE	0000 0000 ₂
00B9 ₁₆	Interrupt enable register 9	IIO9IE	0000 0000 ₂
00BA ₁₆	Interrupt enable register 10	IIO10IE	0000 0000 ₂
00BB ₁₆	Interrupt enable register 11	IIO11IE	0000 0000 ₂
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

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Address	Register	Symbol	Value after RESET
00C0 ₁₆ 00C1 ₁₆	Group 0 time measurement/waveform generation register 0	G0TM0/G0PO0	XX ₁₆ XX ₁₆
00C2 ₁₆ 00C3 ₁₆	Group 0 time measurement/waveform generation register 1	G0TM1/G0PO1	XX ₁₆ XX ₁₆
00C4 ₁₆ 00C5 ₁₆	Group 0 time measurement/waveform generation register 2	G0TM2/G0PO2	XX ₁₆ XX ₁₆
00C6 ₁₆ 00C7 ₁₆	Group 0 time measurement/waveform generation register 3	G0TM3/G0PO3	XX ₁₆ XX ₁₆
00C8 ₁₆ 00C9 ₁₆	Group 0 time measurement/waveform generation register 4	G0TM4/G0PO4	XX ₁₆ XX ₁₆
00CA ₁₆ 00CB ₁₆	Group 0 time measurement/waveform generation register 5	G0TM5/G0PO5	XX ₁₆ XX ₁₆
00CC ₁₆ 00CD ₁₆	Group 0 time measurement/waveform generation register 6	G0TM6/G0PO6	XX ₁₆ XX ₁₆
00CE ₁₆ 00CF ₁₆	Group 0 time measurement/waveform generation register 7	G0TM7/G0PO7	XX ₁₆ XX ₁₆
00D0 ₁₆	Group 0 waveform generation control register 0	G0POCR0	0X00 X0002
00D1 ₁₆	Group 0 waveform generation control register 1	G0POCR1	0X00 X0002
00D2 ₁₆	Group 0 waveform generation control register 2	G0POCR2	0X00 X0002
00D3 ₁₆	Group 0 waveform generation control register 3	G0POCR3	0X00 X0002
00D4 ₁₆	Group 0 waveform generation control register 4	G0POCR4	0X00 X0002
00D5 ₁₆	Group 0 waveform generation control register 5	G0POCR5	0X00 X0002
00D6 ₁₆	Group 0 waveform generation control register 6	G0POCR6	0X00 X0002
00D7 ₁₆	Group 0 waveform generation control register 7	G0POCR7	0X00 X0002
00D8 ₁₆	Group 0 time measurement control register 0	G0TMCR0	0000 00002
00D9 ₁₆	Group 0 time measurement control register 1	G0TMCR1	0000 00002
00DA ₁₆	Group 0 time measurement control register 2	G0TMCR2	0000 00002
00DB ₁₆	Group 0 time measurement control register 3	G0TMCR3	0000 00002
00DC ₁₆	Group 0 time measurement control register 4	G0TMCR4	0000 00002
00DD ₁₆	Group 0 time measurement control register 5	G0TMCR5	0000 00002
00DE ₁₆	Group 0 time measurement control register 6	G0TMCR6	0000 00002
00DF ₁₆	Group 0 time measurement control register 7	G0TMCR7	0000 00002
00E0 ₁₆ 00E1 ₁₆	Group 0 base timer register	G0BT	XX ₁₆ XX ₁₆
00E2 ₁₆	Group 0 base timer control register 0	G0BCR0	0000 00002
00E3 ₁₆	Group 0 base timer control register 1	G0BCR1	0000 00002
00E4 ₁₆	Group 0 time measurement prescaler register 6	G0TPR6	0000 00002
00E5 ₁₆	Group 0 time measurement prescaler register 7	G0TPR7	0000 00002
00E6 ₁₆	Group 0 function enable register	G0FE	0000 00002
00E7 ₁₆	Group 0 function select register	G0FS	0000 00002
00E8 ₁₆ 00E9 ₁₆	Group 0 SI/O receive buffer register	G0RB	XXXX XXXX ₂ XX00 XXXX ₂
00EA ₁₆	Group 0 transmit buffer/receive data register	G0TB/G0DR	XX ₁₆
00EB ₁₆			
00EC ₁₆	Group 0 receive input register	G0RI	XX ₁₆
00ED ₁₆	Group 0 SI/O communication mode register	G0MR	0000 00002
00EE ₁₆	Group 0 transmit output register	G0TO	XX ₁₆
00EF ₁₆	Group 0 SI/O communication control register	G0CR	0000 X0002

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Address	Register	Symbol	Value after RESET
00F0 ₁₆	Group 0 data compare register 0	G0CMP0	XX ₁₆
00F1 ₁₆	Group 0 data compare register 1	G0CMP1	XX ₁₆
00F2 ₁₆	Group 0 data compare register 2	G0CMP2	XX ₁₆
00F3 ₁₆	Group 0 data compare register 3	G0CMP3	XX ₁₆
00F4 ₁₆	Group 0 data mask register 0	G0MSK0	XX ₁₆
00F5 ₁₆	Group 0 data mask register 1	G0MSK1	XX ₁₆
00F6 ₁₆			
00F7 ₁₆			
00F8 ₁₆	Group 0 receive CRC code register	G0RCRC	XX ₁₆
00F9 ₁₆			XX ₁₆
00FA ₁₆	Group 0 transmit CRC code register	G0TCRC	0000 0000 ₂
00FB ₁₆			0000 0000 ₂
00FC ₁₆	Group 0 SI/O extended mode register	G0EMR	0000 0000 ₂
00FD ₁₆	Group 0 SI/O extended receive control register	G0ERC	0000 0000 ₂
00FE ₁₆	Group 0 SI/O special communication interrupt detect register	G0IRF	0000 00XX ₂
00FF ₁₆	Group 0 SI/O extended transmit control register	G0ETC	0000 0XXX ₂
0100 ₁₆	Group 1 time measurement/waveform generation register 0	G1TM0/G1PO0	XX ₁₆
0101 ₁₆			XX ₁₆
0102 ₁₆	Group 1 time measurement/waveform generation register 1	G1TM1/G1PO1	XX ₁₆
0103 ₁₆			XX ₁₆
0104 ₁₆	Group 1 time measurement/waveform generation register 2	G1TM2/G1PO2	XX ₁₆
0105 ₁₆			XX ₁₆
0106 ₁₆	Group 1 time measurement/waveform generation register 3	G1TM3/G1PO3	XX ₁₆
0107 ₁₆			XX ₁₆
0108 ₁₆	Group 1 time measurement/waveform generation register 4	G1TM4/G1PO4	XX ₁₆
0109 ₁₆			XX ₁₆
010A ₁₆	Group 1 time measurement/waveform generation register 5	G1TM5/G1PO5	XX ₁₆
010B ₁₆			XX ₁₆
010C ₁₆	Group 1 time measurement/waveform generation register 6	G1TM6/G1PO6	XX ₁₆
010D ₁₆			XX ₁₆
010E ₁₆	Group 1 time measurement/waveform generation register 7	G1TM7/G1PO7	XX ₁₆
010F ₁₆			XX ₁₆
0110 ₁₆	Group 1 waveform generation control register 0	G1POCR0	0X00 X000 ₂
0111 ₁₆	Group 1 waveform generation control register 1	G1POCR1	0X00 X000 ₂
0112 ₁₆	Group 1 waveform generation control register 2	G1POCR2	0X00 X000 ₂
0113 ₁₆	Group 1 waveform generation control register 3	G1POCR3	0X00 X000 ₂
0114 ₁₆	Group 1 waveform generation control register 4	G1POCR4	0X00 X000 ₂
0115 ₁₆	Group 1 waveform generation control register 5	G1POCR5	0X00 X000 ₂
0116 ₁₆	Group 1 waveform generation control register 6	G1POCR6	0X00 X000 ₂
0117 ₁₆	Group 1 waveform generation control register 7	G1POCR7	0X00 X000 ₂
0118 ₁₆	Group 1 time measurement control register 0	G1TMCR0	0000 0000 ₂
0119 ₁₆	Group 1 time measurement control register 1	G1TMCR1	0000 0000 ₂
011A ₁₆	Group 1 time measurement control register 2	G1TMCR2	0000 0000 ₂
011B ₁₆	Group 1 time measurement control register 3	G1TMCR3	0000 0000 ₂
011C ₁₆	Group 1 time measurement control register 4	G1TMCR4	0000 0000 ₂
011D ₁₆	Group 1 time measurement control register 5	G1TMCR5	0000 0000 ₂
011E ₁₆	Group 1 time measurement control register 6	G1TMCR6	0000 0000 ₂
011F ₁₆	Group 1 time measurement control register 7	G1TMCR7	0000 0000 ₂

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Address	Register	Symbol	Value after RESET
0120 ₁₆ 0121 ₁₆	Group 1 base timer register	G1BT	XX ₁₆ XX ₁₆
0122 ₁₆	Group 1 base timer control register 0	G1BCR0	0000 0000 ₂
0123 ₁₆	Group 1 base timer control register 1	G1BCR1	0000 0000 ₂
0124 ₁₆	Group 1 time measurement prescaler register 6	G1TPR6	0000 0000 ₂
0125 ₁₆	Group 1 time measurement prescaler register 7	G1TPR7	0000 0000 ₂
0126 ₁₆	Group 1 function enable register	G1FE	0000 0000 ₂
0127 ₁₆	Group 1 function select register	G1FS	0000 0000 ₂
0128 ₁₆ 0129 ₁₆	Group 1 SI/O receive buffer register	G1RB	XXXX XXXX ₂ XX00 XXXX ₂
012A ₁₆ 012B ₁₆	Group 1 transmit buffer/receive data register	G1TB/G1DR	XX ₁₆
012C ₁₆	Group 1 receive input register	G1RI	XX ₁₆
012D ₁₆	Group 1 SI/O communication mode register	G1MR	0000 0000 ₂
012E ₁₆	Group 1 transmit output register	G1TO	XX ₁₆
012F ₁₆	Group 1 SI/O communication control register	G1CR	0000 X000 ₂
0130 ₁₆	Group 1 data compare register 0	G1CMP0	XX ₁₆
0131 ₁₆	Group 1 data compare register 1	G1CMP1	XX ₁₆
0132 ₁₆	Group 1 data compare register 2	G1CMP2	XX ₁₆
0133 ₁₆	Group 1 data compare register 3	G1CMP3	XX ₁₆
0134 ₁₆	Group 1 data mask register 0	G1MSK0	XX ₁₆
0135 ₁₆	Group 1 data mask register 1	G1MSK1	XX ₁₆
0136 ₁₆ 0137 ₁₆			
0138 ₁₆ 0139 ₁₆	Group 1 receive CRC code register	G1RCRC	XX ₁₆ XX ₁₆
013A ₁₆ 013B ₁₆	Group 1 transmit CRC code register	G1TCRC	0000 0000 ₂ 0000 0000 ₂
013C ₁₆	Group 1 SI/O extended mode register	G1EMR	0000 0000 ₂
013D ₁₆	Group 1 SI/O extended receive control register	G1ERC	0000 0000 ₂
013E ₁₆	Group 1 SI/O special communication interrupt detect register	G1IRF	0000 00XX ₂
013F ₁₆	Group 1 SI/O extended transmit control register	G1ETC	0000 0XXX ₂
0140 ₁₆ 0141 ₁₆	Group 2 waveform generation register 0	G2PO0	XX ₁₆ XX ₁₆
0142 ₁₆ 0143 ₁₆	Group 2 waveform generation register 1	G2PO1	XX ₁₆ XX ₁₆
0144 ₁₆ 0145 ₁₆	Group 2 waveform generation register 2	G2PO2	XX ₁₆ XX ₁₆
0146 ₁₆ 0147 ₁₆	Group 2 waveform generation register 3	G2PO3	XX ₁₆ XX ₁₆
0148 ₁₆ 0149 ₁₆	Group 2 waveform generation register 4	G2PO4	XX ₁₆ XX ₁₆
014A ₁₆ 014B ₁₆	Group 2 waveform generation register 5	G2PO5	XX ₁₆ XX ₁₆
014C ₁₆ 014D ₁₆	Group 2 waveform generation register 6	G2PO6	XX ₁₆ XX ₁₆
014E ₁₆ 014F ₁₆	Group 2 waveform generation register 7	G2PO7	XX ₁₆ XX ₁₆

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Address	Register	Symbol	Value after RESET
0150 ₁₆	Group 2 waveform generation control register 0	G2POCR0	0000 0000 ₂
0151 ₁₆	Group 2 waveform generation control register 1	G2POCR1	0000 0000 ₂
0152 ₁₆	Group 2 waveform generation control register 2	G2POCR2	0000 0000 ₂
0153 ₁₆	Group 2 waveform generation control register 3	G2POCR3	0000 0000 ₂
0154 ₁₆	Group 2 waveform generation control register 4	G2POCR4	0000 0000 ₂
0155 ₁₆	Group 2 waveform generation control register 5	G2POCR5	0000 0000 ₂
0156 ₁₆	Group 2 waveform generation control register 6	G2POCR6	0000 0000 ₂
0157 ₁₆	Group 2 waveform generation control register 7	G2POCR7	0000 0000 ₂
0158 ₁₆			
0159 ₁₆			
015A ₁₆			
015B ₁₆			
015C ₁₆			
015D ₁₆			
015E ₁₆			
015F ₁₆			
0160 ₁₆ 0161 ₁₆	Group 2 base timer register	G2BT	XX ₁₆ XX ₁₆
0162 ₁₆	Group 2 base timer control register 0	G2BCR0	0000 0000 ₂
0163 ₁₆	Group 2 base timer control register 1	G2BCR1	0000 0000 ₂
0164 ₁₆	Base timer start register	BTSR	XXXX 0000 ₂
0165 ₁₆			
0166 ₁₆	Group 2 function enable register	G2FE	0000 0000 ₂
0167 ₁₆	Group 2 RTP output buffer register	G2RTP	0000 0000 ₂
0168 ₁₆			
0169 ₁₆			
016A ₁₆	Group 2 SI/O communication mode register	G2MR	00XX X000 ₂
016B ₁₆	Group 2 SI/O communication control register	G2CR	0000 X000 ₂
016C ₁₆ 016D ₁₆	Group 2 SI/O transmit buffer register	G2TB	XXXX XXXX ₂ XXXX XXXX ₂
016E ₁₆ 016F ₁₆	Group 2 SI/O receive buffer register	G2RB	XXXX XXXX ₂ XXXX XXXX ₂
0170 ₁₆ 0171 ₁₆	Group 2 IEBus address register	IEAR	XXXX XXXX ₂ XXXX XXXX ₂
0172 ₁₆	Group 2 IEBus control register	IECR	00XX X000 ₂
0173 ₁₆	Group 2 IEBus transmit interrupt cause detect register	IETIF	XXX0 0000 ₂
0174 ₁₆	Group 2 IEBus receive interrupt cause detect register	IERIF	XXX0 0000 ₂
0175 ₁₆			
0176 ₁₆			
0177 ₁₆			
0178 ₁₆	Input function select register	IPS	0000 0000 ₂
0179 ₁₆			
017A ₁₆			
017B ₁₆			
017C ₁₆			
017D ₁₆			
017E ₁₆			
017F ₁₆			

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Address	Register	Symbol	Value after RESET
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆			
01B4 ₁₆			
01B5 ₁₆			
01B6 ₁₆			
01B7 ₁₆			
01B8 ₁₆			
01B9 ₁₆			
01BA ₁₆			
01BB ₁₆			
01BC ₁₆			
01BD ₁₆			
01BE ₁₆			
01BF ₁₆			
01C0 ₁₆ 01C1 ₁₆	A-D1 register 0	AD10	XXXX XXXX ₂ XXXX XXXX ₂
01C2 ₁₆ 01C3 ₁₆	A-D1 register 1	AD11	XXXX XXXX ₂ XXXX XXXX ₂
01C4 ₁₆ 01C5 ₁₆	A-D1 register 2	AD12	XXXX XXXX ₂ XXXX XXXX ₂
01C6 ₁₆ 01C7 ₁₆	A-D1 register 3	AD13	XXXX XXXX ₂ XXXX XXXX ₂
01C8 ₁₆ 01C9 ₁₆	A-D1 register 4	AD14	XXXX XXXX ₂ XXXX XXXX ₂
01CA ₁₆ 01CB ₁₆	A-D1 register 5	AD15	XXXX XXXX ₂ XXXX XXXX ₂
01CC ₁₆ 01CD ₁₆	A-D1 register 6	AD16	XXXX XXXX ₂ XXXX XXXX ₂
01CE ₁₆ 01CF ₁₆	A-D1 register 7	AD17	XXXX XXXX ₂ XXXX XXXX ₂
01D0 ₁₆			
01D1 ₁₆			
01D2 ₁₆			
01D3 ₁₆			
01D4 ₁₆ 01D5 ₁₆	A-D1 control register 2	AD1CON2	X00X X000 ₂
01D6 ₁₆ 01D7 ₁₆	A-D1 control register 0	AD1CON0	0000 0000 ₂
01D8 ₁₆ 01D9 ₁₆	A-D1 control register 1	AD1CON1	XX00 0000 ₂
01DA ₁₆			
01DB ₁₆			
01DC ₁₆			
01DD ₁₆			
01DE ₁₆			
01DF ₁₆			

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Users cannot use any symbols with *. No access is allowed.

Address	Register	Symbol	Value after RESET	
01E0 ₁₆	CAN0 message slot buffer 0 standard ID0	C0SLOT0_0	XXXX XXXX ₂	*
01E1 ₁₆	CAN0 message slot buffer 0 standard ID1	C0SLOT0_1	XXXX XXXX ₂	
01E2 ₁₆	CAN0 message slot buffer 0 extended ID0	C0SLOT0_2	XXXX XXXX ₂	*
01E3 ₁₆	CAN0 message slot buffer 0 extended ID1	C0SLOT0_3	XX ₁₆	
01E4 ₁₆	CAN0 message slot buffer 0 extended ID2	C0SLOT0_4	XXXX XXXX ₂	*
01E5 ₁₆	CAN0 message slot buffer 0 data length code	C0SLOT0_5	XXXX XXXX ₂	
01E6 ₁₆	CAN0 message slot buffer 0 data 0	C0SLOT0_6	XX ₁₆	*
01E7 ₁₆	CAN0 message slot buffer 0 data 1	C0SLOT0_7	XX ₁₆	
01E8 ₁₆	CAN0 message slot buffer 0 data 2	C0SLOT0_8	XX ₁₆	*
01E9 ₁₆	CAN0 message slot buffer 0 data 3	C0SLOT0_9	XX ₁₆	
01EA ₁₆	CAN0 message slot buffer 0 data 4	C0SLOT0_10	XX ₁₆	*
01EB ₁₆	CAN0 message slot buffer 0 data 5	C0SLOT0_11	XX ₁₆	
01EC ₁₆	CAN0 message slot buffer 0 data 6	C0SLOT0_12	XX ₁₆	*
01ED ₁₆	CAN0 message slot buffer 0 data 7	C0SLOT0_13	XX ₁₆	
01EE ₁₆	CAN0 message slot buffer 0 time stamp high-order	C0SLOT0_14	XX ₁₆	*
01EF ₁₆	CAN0 message slot buffer 0 time stamp low-order	C0SLOT0_15	XX ₁₆	
01F0 ₁₆	CAN0 message slot buffer 1 standard ID0	C0SLOT1_0	XXXX XXXX ₂	
01F1 ₁₆	CAN0 message slot buffer 1 standard ID1	C0SLOT1_1	XXXX XXXX ₂	
01F2 ₁₆	CAN0 message slot buffer 1 extended ID0	C0SLOT1_2	XXXX XXXX ₂	
01F3 ₁₆	CAN0 message slot buffer 1 extended ID1	C0SLOT1_3	XX ₁₆	
01F4 ₁₆	CAN0 message slot buffer 1 extended ID2	C0SLOT1_4	XXXX XXXX ₂	
01F5 ₁₆	CAN0 message slot buffer 1 data length code	C0SLOT1_5	XXXX XXXX ₂	
01F6 ₁₆	CAN0 message slot buffer 1 data 0	C0SLOT1_6	XX ₁₆	
01F7 ₁₆	CAN0 message slot buffer 1 data 1	C0SLOT1_7	XX ₁₆	
01F8 ₁₆	CAN0 message slot buffer 1 data 2	C0SLOT1_8	XX ₁₆	
01F9 ₁₆	CAN0 message slot buffer 1 data 3	C0SLOT1_9	XX ₁₆	
01FA ₁₆	CAN0 message slot buffer 1 data 4	C0SLOT1_10	XX ₁₆	
01FB ₁₆	CAN0 message slot buffer 1 data 5	C0SLOT1_11	XX ₁₆	
01FC ₁₆	CAN0 message slot buffer 1 data 6	C0SLOT1_12	XX ₁₆	
01FD ₁₆	CAN0 message slot buffer 1 data 7	C0SLOT1_13	XX ₁₆	
01FE ₁₆	CAN0 message slot buffer 1 time stamp high-order	C0SLOT1_14	XX ₁₆	
01FF ₁₆	CAN0 message slot buffer 1 time stamp low-order	C0SLOT1_15	XX ₁₆	
0200 ₁₆ 0201 ₁₆	CAN0 control register 0	C0CTLR0	XX01 0X01 ₂ ¹ XXXX 0000 ₂ ¹	
0202 ₁₆ 0203 ₁₆	CAN0 status register	C0STR	0000 0000 ₂ ¹ X000 0X01 ₂ ¹	
0204 ₁₆ 0205 ₁₆	CAN0 extended ID register	C0IDR	0000 0000 ₂ ¹ 0000 0000 ₂ ¹	
0206 ₁₆ 0207 ₁₆	CAN0 configuration register	C0CONR	0000 XXXX ₂ ¹ 0000 0000 ₂ ¹	
0208 ₁₆ 0209 ₁₆	CAN0 time stamp register	C0TSR	0000 0000 ₂ ¹ 0000 0000 ₂ ¹	
020A ₁₆	CAN0 transmit error count register	C0TEC	0000 0000 ₂ ¹	
020B ₁₆	CAN0 receive error count register	C0REC	0000 0000 ₂ ¹	
020C ₁₆ 020D ₁₆	CAN0 slot interrupt status register	C0SISTR	0000 0000 ₂ ¹ 0000 0000 ₂ ¹	
020E ₁₆				
020F ₁₆				

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Blank columns are all reserved space. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 slot interrupt mask register	C0SIMKR	0000 0000 ₂ ²
0211 ₁₆			0000 0000 ₂ ²
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 error interrupt mask register	C0EIMKR	XXXX X000 ₂ ²
0215 ₁₆	CAN0 error interrupt status register	C0EISTR	XXXX X000 ₂ ²
0216 ₁₆			
0217 ₁₆	CAN0 baud rate prescaler	C0BRP	0000 0001 ₂ ²
0218 ₁₆			
0219 ₁₆			
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆			
0221 ₁₆			
0222 ₁₆			
0223 ₁₆			
0224 ₁₆			
0225 ₁₆			
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 global mask register standard ID0	C0GMR0	XXX0 0000 ₂ ²
0229 ₁₆	CAN0 global mask register standard ID1	C0GMR1	XX00 0000 ₂ ²
022A ₁₆	CAN0 global mask register extended ID0	C0GMR2	XXXX 0000 ₂ ²
022B ₁₆	CAN0 global mask register extended ID1	C0GMR3	0000 0000 ₂ ²
022C ₁₆	CAN0 global mask register extended ID2	C0GMR4	XX00 0000 ₂ ²
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 message slot 0 control register /	C0MCTL0/	0000 0000 ₂ ²
	CAN0 local mask register A standard ID0	C0LMAR0	XXX0 0000 ₂ ²
0231 ₁₆	CAN0 message slot 1 control register /	C0MCTL1/	0000 0000 ₂ ²
	CAN0 local mask register A standard ID1	C0LMAR1	XX00 0000 ₂ ²
0232 ₁₆	CAN0 message slot 2 control register /	C0MCTL2/	0000 0000 ₂ ²
	CAN0 local mask register A extended ID0	C0LMAR2	XXXX 0000 ₂ ²
0233 ₁₆	CAN0 message slot 3 control register /	C0MCTL3/	0000 0000 ₂ ²
	CAN0 local mask register A extended ID1	C0LMAR3	0000 0000 ₂ ²
0234 ₁₆	CAN0 message slot 4 control register /	C0MCTL4/	0000 0000 ₂ ²
	CAN0 local mask register A extended ID2	C0LMAR4	XX00 0000 ₂ ²
0235 ₁₆	CAN0 message slot 5 control register	C0MCTL5	0000 0000 ₂ ²
0236 ₁₆	CAN0 message slot 6 control register	C0MCTL6	0000 0000 ₂ ²
0237 ₁₆	CAN0 message slot 7 control register	C0MCTL7	0000 0000 ₂ ²
0238 ₁₆	CAN0 message slot 8 control register /	C0MCTL8/	0000 0000 ₂ ²
	CAN0 local mask register B standard ID0	C0LMBR0	XXX0 0000 ₂ ²

(Note 1)

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0230₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

(Note 1)

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1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0230₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02C0 ₁₆ 02C1 ₁₆	X0 register Y0 register	X0R,Y0R	XX ₁₆ XX ₁₆
02C2 ₁₆ 02C3 ₁₆	X1 register Y1 register	X1R,Y1R	XX ₁₆ XX ₁₆
02C4 ₁₆ 02C5 ₁₆	X2 register Y2 register	X2R,Y2R	XX ₁₆ XX ₁₆
02C6 ₁₆ 02C7 ₁₆	X3 register Y3 register	X3R,Y3R	XX ₁₆ XX ₁₆
02C8 ₁₆ 02C9 ₁₆	X4 register Y4 register	X4R,Y4R	XX ₁₆ XX ₁₆
02CA ₁₆ 02CB ₁₆	X5 register Y5 register	X5R,Y5R	XX ₁₆ XX ₁₆
02CC ₁₆ 02CD ₁₆	X6 register Y6 register	X6R,Y6R	XX ₁₆ XX ₁₆
02CE ₁₆ 02CF ₁₆	X7 register Y7 register	X7R,Y7R	XX ₁₆ XX ₁₆
02D0 ₁₆ 02D1 ₁₆	X8 register Y8 register	X8R,Y8R	XX ₁₆ XX ₁₆
02D2 ₁₆ 02D3 ₁₆	X9 register Y9 register	X9R,Y9R	XX ₁₆ XX ₁₆
02D4 ₁₆ 02D5 ₁₆	X10 register Y10 register	X10R,Y10R	XX ₁₆ XX ₁₆
02D6 ₁₆ 02D7 ₁₆	X11 register Y11 register	X11R,Y11R	XX ₁₆ XX ₁₆
02D8 ₁₆ 02D9 ₁₆	X12 register Y12 register	X12R,Y12R	XX ₁₆ XX ₁₆
02DA ₁₆ 02DB ₁₆	X13 register Y13 register	X13R,Y13R	XX ₁₆ XX ₁₆
02DC ₁₆ 02DD ₁₆	X14 register Y14 register	X14R,Y14R	XX ₁₆ XX ₁₆
02DE ₁₆ 02DF ₁₆	X15 register Y15 register	X15R,Y15R	XX ₁₆ XX ₁₆
02E0 ₁₆	XY control register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 special mode register 4	U1SMR4	0000 0000 ₂
02E5 ₁₆	UART1 special mode register 3	U1SMR3	0000 0000 ₂
02E6 ₁₆	UART1 special mode register 2	U1SMR2	0000 0000 ₂
02E7 ₁₆	UART1 special mode register	U1SMR	0000 0000 ₂
02E8 ₁₆	UART1 transmit/receive mode register	U1MR	0000 0000 ₂
02E9 ₁₆	UART1 baud rate register	U1BRG	XX ₁₆
02EA ₁₆ 02EB ₁₆	UART1 transmit buffer register	U1TB	XXXX XXXX ₂ XXXX XXXX ₂
02EC ₁₆	UART1 transmit/receive control register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 transmit/receive control register 1	U1C1	0000 0010 ₂
02EE ₁₆ 02EF ₁₆	UART1 receive buffer register	U1RB	XXXX XXXX ₂ XXXX XXXX ₂

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Address	Register	Symbol	Value after RESET
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 special mode register 4	U4SMR4	0000 0000 ₂
02F5 ₁₆	UART4 special mode register 3	U4SMR3	0000 0000 ₂
02F6 ₁₆	UART4 special mode register 2	U4SMR2	0000 0000 ₂
02F7 ₁₆	UART4 special mode register	U4SMR	0000 0000 ₂
02F8 ₁₆	UART4 transmit/receive mode register	U4MR	0000 0000 ₂
02F9 ₁₆	UART4 baud rate register	U4BRG	XX ₁₆
02FA ₁₆	UART4 transmit buffer register	U4TB	XXXX XXXX ₂
02FB ₁₆			XXXX XXXX ₂
02FC ₁₆	UART4 transmit/receive control register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 transmit/receive control register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 receive buffer register	U4RB	XXXX XXXX ₂
02FF ₁₆			XXXX XXXX ₂
0300 ₁₆	Timer B3,B4,B5 count start flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-phase PWM control register 0	INVC0	0000 0000 ₂
0309 ₁₆	Three-phase PWM control register 1	INVC1	0000 0000 ₂
030A ₁₆	Three-phase output buffer register 0	IDB0	XX11 1111 ₂
030B ₁₆	Three-phase output buffer register 1	IDB1	XX11 1111 ₂
030C ₁₆	Dead time timer	DTT	XX ₁₆
030D ₁₆	Timer B2 interrupt generation frequency set counter	ICTB2	XXXX XXXX ₂
030E ₁₆			
030F ₁₆			
0310 ₁₆	Timer B3 register	TB3	XX ₁₆
0311 ₁₆			XX ₁₆
0312 ₁₆	Timer B4 register	TB4	XX ₁₆
0313 ₁₆			XX ₁₆
0314 ₁₆	Timer B5 register	TB5	XX ₁₆
0315 ₁₆			XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 mode register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 mode register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 mode register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External interrupt cause select register	IFSR	0000 0000 ₂

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Address	Register	Symbol	Value after RESET
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 special mode register 4	U3SMR4	0000 0000 ₂
0325 ₁₆	UART3 special mode register 3	U3SMR3	0000 0000 ₂
0326 ₁₆	UART3 special mode register 2	U3SMR2	0000 0000 ₂
0327 ₁₆	UART3 special mode register	U3SMR	0000 0000 ₂
0328 ₁₆	UART3 transmit/receive mode register	U3MR	0000 0000 ₂
0329 ₁₆	UART3 baud rate register	U3BRG	XX ₁₆
032A ₁₆	UART3 transmit buffer register	U3TB	XXXX XXXX ₂
032B ₁₆			XXXX XXXX ₂
032C ₁₆	UART3 transmit/receive control register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 transmit/receive control register 1	U3C1	0000 0010 ₂
032E ₁₆	UART3 receive buffer register	U3RB	XXXX XXXX ₂
032F ₁₆			XXXX XXXX ₂
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 special mode register 4	U2SMR4	0000 0000 ₂
0335 ₁₆	UART2 special mode register 3	U2SMR3	0000 0000 ₂
0336 ₁₆	UART2 special mode register 2	U2SMR2	0000 0000 ₂
0337 ₁₆	UART2 special mode register	U2SMR	0000 0000 ₂
0338 ₁₆	UART2 transmit/receive mode register	U2MR	0000 0000 ₂
0339 ₁₆	UART2 baud rate register	U2BRG	XX ₁₆
033A ₁₆	UART2 transmit buffer register	U2TB	XXXX XXXX ₂
033B ₁₆			XXXX XXXX ₂
033C ₁₆	UART2 transmit/receive control register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 transmit/receive control register 1	U2C1	0000 0010 ₂
033E ₁₆	UART2 receive buffer register	U2RB	XXXX XXXX ₂
033F ₁₆			XXXX XXXX ₂
0340 ₁₆	Count start flag	TABSR	0000 0000 ₂
0341 ₁₆	Clock prescaler reset flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-shot start flag	ONSF	0000 0000 ₂
0343 ₁₆	Trigger select register	TRGSR	0000 0000 ₂
0344 ₁₆	Up-down flag	UDF	0000 0000 ₂
0345 ₁₆			
0346 ₁₆	Timer A0 register	TA0	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Timer A1 register	TA1	XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆	Timer A2 register	TA2	XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	Timer A3 register	TA3	XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	Timer A4 register	TA4	XX ₁₆
034F ₁₆			XX ₁₆

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Address	Register	Symbol	Value after RESET
0350 ₁₆ 0351 ₁₆	Timer B0 register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 mode register	TA0MR	0000 0X00 ₂
0357 ₁₆	Timer A1 mode register	TA1MR	0000 0X00 ₂
0358 ₁₆	Timer A2 mode register	TA2MR	0000 0X00 ₂
0359 ₁₆	Timer A3 mode register	TA3MR	0000 0X00 ₂
035A ₁₆	Timer A4 mode register	TA4MR	0000 0X00 ₂
035B ₁₆	Timer B0 mode register	TB0MR	00XX 0000 ₂
035C ₁₆	Timer B1 mode register	TB1MR	00XX 0000 ₂
035D ₁₆	Timer B2 mode register	TB2MR	00XX 0000 ₂
035E ₁₆	Timer B2 special mode register	TB2SC	XXXX XXXX ₂
035F ₁₆	Count source prescaler register	TCSPR	0XXX 0000 ₂
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 special mode register 4	U0SMR4	0000 0000 ₂
0365 ₁₆	UART0 special mode register 3	U0SMR3	0000 0000 ₂
0366 ₁₆	UART0 special mode register 2	U0SMR2	0000 0000 ₂
0367 ₁₆	UART0 special mode register	U0SMR	0000 0000 ₂
0368 ₁₆	UART0 transmit/receive mode register	U0MR	0000 0000 ₂
0369 ₁₆	UART0 baud rate register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 transmit buffer register	U0TB	XXXX XXXX ₂ XXXX XXXX ₂
036C ₁₆	UART0 transmit/receive control register 0	U0C0	0000 1000 ₂
036D ₁₆	UART0 transmit/receive control register 1	U0C1	0000 0010 ₂
036E ₁₆ 036F ₁₆	UART0 receive buffer register	U0RB	XXXX XXXX ₂ XXXX XXXX ₂
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆	PLL control register 0	PLC0	0011 X100 ₂
0377 ₁₆	PLL control register 1	PLC1	XXXX 0000 ₂
0378 ₁₆	DMA0 cause select register	DM0SL	0X00 0000 ₂
0379 ₁₆	DMA1 cause select register	DM1SL	0X00 0000 ₂
037A ₁₆	DMA2 cause select register	DM2SL	0X00 0000 ₂
037B ₁₆	DMA3 cause select register	DM3SL	0X00 0000 ₂
037C ₁₆ 037D ₁₆	CRC data register	CRCD	XX ₁₆ XX ₁₆
037E ₁₆	CRC input register	CRCIN	XX ₁₆
037F ₁₆			

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Address	Register	Symbol	Value after RESET
0380 ₁₆ 0381 ₁₆	A-D0 register 0	AD00	XXXX XXXX ₂ XXXX XXXX ₂
0382 ₁₆ 0383 ₁₆	A-D0 register 1	AD01	XXXX XXXX ₂ XXXX XXXX ₂
0384 ₁₆ 0385 ₁₆	A-D0 register 2	AD02	XXXX XXXX ₂ XXXX XXXX ₂
0386 ₁₆ 0387 ₁₆	A-D0 register 3	AD03	XXXX XXXX ₂ XXXX XXXX ₂
0388 ₁₆ 0389 ₁₆	A-D0 register 4	AD04	XXXX XXXX ₂ XXXX XXXX ₂
038A ₁₆ 038B ₁₆	A-D0 register 5	AD05	XXXX XXXX ₂ XXXX XXXX ₂
038C ₁₆ 038D ₁₆	A-D0 register 6	AD06	XXXX XXXX ₂ XXXX XXXX ₂
038E ₁₆ 038F ₁₆	A-D0 register 7	AD07	XXXX XXXX ₂ XXXX XXXX ₂
0390 ₁₆			
0391 ₁₆			
0392 ₁₆			
0393 ₁₆			
0394 ₁₆ 0395 ₁₆	A-D0 control register 2	AD0CON2	X000 0000 ₂
0396 ₁₆	A-D0 control register 0	AD0CON0	0000 0000 ₂
0397 ₁₆	A-D0 control register 1	AD0CON1	0000 0000 ₂
0398 ₁₆ 0399 ₁₆	D-A register 0	DA0	XX ₁₆
039A ₁₆ 039B ₁₆	D-A register 1	DA1	XX ₁₆
039C ₁₆ 039D ₁₆	D-A control register	DACON	XXXX XX00 ₂
039E ₁₆			
039F ₁₆			

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Address	Register	Symbol	Value after RESET
03A0 ₁₆	Function select register A8	PS8	X000 0000 ₂
03A1 ₁₆	Function select register A9	PS9	0000 0000 ₂
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆			
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆			
03AD ₁₆			
03AE ₁₆			
03AF ₁₆	Function select register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function select register A0	PS0	0000 0000 ₂
03B1 ₁₆	Function select register A1	PS1	0000 0000 ₂
03B2 ₁₆	Function select register B0	PSL0	0000 0000 ₂
03B3 ₁₆	Function select register B1	PSL1	0000 0000 ₂
03B4 ₁₆	Function select register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function select register A3	PS3	0000 0000 ₂
03B6 ₁₆	Function select register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function select register B3	PSL3	0000 0000 ₂
03B8 ₁₆			
03B9 ₁₆	Function select register A5	PS5	XXX0 0000 ₂
03BA ₁₆			
03BB ₁₆			
03BC ₁₆	Function select register A6	PS6	0000 0000 ₂
03BD ₁₆	Function select register A7	PS7	0000 0000 ₂
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 register	P6	XX ₁₆
03C1 ₁₆	Port P7 register	P7	XX ₁₆
03C2 ₁₆	Port P6 direction register	PD6	0000 0000 ₂
03C3 ₁₆	Port P7 direction register	PD7	0000 0000 ₂
03C4 ₁₆	Port P8 register	P8	XX ₁₆
03C5 ₁₆	Port P9 register	P9	XX ₁₆
03C6 ₁₆	Port P8 direction register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 direction register	PD9	0000 0000 ₂
03C8 ₁₆	Port P10 register	P10	XX ₁₆
03C9 ₁₆	Port P11 register	P11	XXXX XXXX ₂
03CA ₁₆	Port P10 direction register	PD10	0000 0000 ₂
03CB ₁₆	Port P11 direction register	PD11	XXX0 0000 ₂
03CC ₁₆	Port P12 register	P12	XX ₁₆
03CD ₁₆	Port P13 register	P13	XX ₁₆
03CE ₁₆	Port P12 direction register	PD12	0000 0000 ₂
03CF ₁₆	Port P13 direction register	PD13	0000 0000 ₂

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Address	Register	Symbol	Value after RESET
03D0 ₁₆	Port P14 register	P14	XXXX XXXX ₂
03D1 ₁₆	Port P15 register	P15	XX ₁₆
03D2 ₁₆	Port P14 direction register	PD14	X000 0000 ₂
03D3 ₁₆	Port P15 direction register	PD15	0000 0000 ₂
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-up control register 2	PUR2	0000 0000 ₂
03DB ₁₆	Pull-up control register 3	PUR3	0000 0000 ₂
03DC ₁₆	Pull-up control register 4	PUR4	XXXX 0000 ₂
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 register	P0	XX ₁₆
03E1 ₁₆	Port P1 register	P1	XX ₁₆
03E2 ₁₆	Port P0 direction register	PD0	0000 0000 ₂
03E3 ₁₆	Port P1 direction register	PD1	0000 0000 ₂
03E4 ₁₆	Port P2 register	P2	XX ₁₆
03E5 ₁₆	Port P3 register	P3	XX ₁₆
03E6 ₁₆	Port P2 direction register	PD2	0000 0000 ₂
03E7 ₁₆	Port P3 direction register	PD3	0000 0000 ₂
03E8 ₁₆	Port P4 register	P4	XX ₁₆
03E9 ₁₆	Port P5 register	P5	XX ₁₆
03EA ₁₆	Port P4 direction register	PD4	0000 0000 ₂
03EB ₁₆	Port P5 direction register	PD5	0000 0000 ₂
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-up control register 0	PUR0	0000 0000 ₂
03F1 ₁₆	Pull-up control register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port control register	PCR	XXXX XXX0 ₂

X: Indetermination

Blank columns are all reserved space. No access is allowed.



<100-pin package>

Address	Register	Symbol	Value after RESET
03A0 ₁₆			
03A1 ₁₆			
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆			
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆			
03AD ₁₆			
03AE ₁₆			
03AF ₁₆	Function select register C	PSC	0X00 0000 ₂
03B0 ₁₆	Function select register A0	PS0	0000 0000 ₂
03B1 ₁₆	Function select register A1	PS1	0000 0000 ₂
03B2 ₁₆	Function select register B0	PSL0	0000 0000 ₂
03B3 ₁₆	Function select register B1	PSL1	0000 0000 ₂
03B4 ₁₆	Function select register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function select register A3	PS3	0000 0000 ₂
03B6 ₁₆	Function select register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function select register B3	PSL3	0000 0000 ₂
03B8 ₁₆			
03B9 ₁₆			
03BA ₁₆			
03BB ₁₆			
03BC ₁₆			
03BD ₁₆			
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 register	P6	XX ₁₆
03C1 ₁₆	Port P7 register	P7	XX ₁₆
03C2 ₁₆	Port P6 direction register	PD6	0000 0000 ₂
03C3 ₁₆	Port P7 direction register	PD7	0000 0000 ₂
03C4 ₁₆	Port P8 register	P8	XX ₁₆
03C5 ₁₆	Port P9 register	P9	XX ₁₆
03C6 ₁₆	Port P8 direction register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 direction register	PD9	0000 0000 ₂
03C8 ₁₆	Port P10 register	P10	XX ₁₆
03C9 ₁₆			
03CA ₁₆	Port P10 direction register	PD10	0000 0000 ₂
03CB ₁₆			
03CC ₁₆			
03CD ₁₆			
03CE ₁₆			
03CF ₁₆			

X: Indetermination

Blank columns are all reserved space. No access is allowed.

NOTES:

1.  Set address space 03CB₁₆, 03CE₁₆ and 03CF₁₆ to "FF₁₆" in the 100-pin package.
2.  No address space 03A0₁₆, 03A1₁₆, 03B9₁₆, 03BD₁₆, 03C9₁₆, 03CC₁₆ and 03CD₁₆ is provided in the 100-pin package.




<100-pin package>

Address	Register	Symbol	Value after RESET	
03D0 ₁₆				(Note 2)
03D1 ₁₆				
03D2 ₁₆				
03D3 ₁₆				
03D4 ₁₆				
03D5 ₁₆				
03D6 ₁₆				
03D7 ₁₆				
03D8 ₁₆				
03D9 ₁₆				
03DA ₁₆	Pull-up control register 2	PUR2	0000 0000 ₂	
03DB ₁₆	Pull-up control register 3	PUR3	0000 0000 ₂	
03DC ₁₆				
03DD ₁₆				
03DE ₁₆				
03DF ₁₆				
03E0 ₁₆	Port P0 register	P0	XX ₁₆	
03E1 ₁₆	Port P1 register	P1	XX ₁₆	
03E2 ₁₆	Port P0 direction register	PD0	0000 0000 ₂	
03E3 ₁₆	Port P1 direction register	PD1	0000 0000 ₂	
03E4 ₁₆	Port P2 register	P2	XX ₁₆	
03E5 ₁₆	Port P3 register	P3	XX ₁₆	
03E6 ₁₆	Port P2 direction register	PD2	0000 0000 ₂	
03E7 ₁₆	Port P3 direction register	PD3	0000 0000 ₂	
03E8 ₁₆	Port P4 register	P4	XX ₁₆	
03E9 ₁₆	Port P5 register	P5	XX ₁₆	(Note 2)
03EA ₁₆	Port P4 direction register	PD4	0000 0000 ₂	
03EB ₁₆	Port P5 direction register	PD5	0000 0000 ₂	
03EC ₁₆				(Note 2)
03ED ₁₆				
03EE ₁₆				
03EF ₁₆				
03F0 ₁₆	Pull-up control register 0	PUR0	0000 0000 ₂	
03F1 ₁₆	Pull-up control register 1	PUR1	XXXX 0000 ₂	
03F2 ₁₆				
03F3 ₁₆				
03F4 ₁₆				
03F5 ₁₆				
03F6 ₁₆				
03F7 ₁₆				
03F8 ₁₆				
03F9 ₁₆				(Note 2)
03FA ₁₆				
03FB ₁₆				(Note 1)
03FC ₁₆				(Note 2)
03FD ₁₆				
03FE ₁₆				
03FF ₁₆	Port control register	PCR	XXXX XXX0 ₂	(Note 1)

X: Indetermination

Blank columns are all reserved space. No access is allowed.

NOTES:

1.  Set address space 03D2₁₆ and 03D3₁₆ to "FF₁₆" in the 100-pin package.
2.  Set address space 03DC₁₆ to "00₁₆" in the 100-pin package.
3.  No address space 03D0₁₆ and 03D1₁₆ is provided in the 100-pin package.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V _{CC}	Supply voltage		V _{CC} =AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog supply voltage		V _{CC} =AV _{CC}	-0.3 to 6.0	V
V _I	Input voltage	RESET, CNV _{SS} , BYTE, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , V _{REF} , X _{IN}		-0.3 to V _{CC} +0.3	V
		P7 ₀ , P7 ₁		-0.3 to 6.0	
V _O	Output voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , V _{REF} , X _{IN}		-0.3 to V _{CC} +0.3	V
		P7 ₀ , P7 ₁		-0.3 to 6.0	V
P _d	Power Dissipation		T _{opr} =25° C	500	mW
T _{opr}	Operating ambient temperature			-20 to 85/-40 to 85 ⁽²⁾	° C
T _{stg}	Storage temperature			-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package.
2. This is an option that is on request basis.

Table 5.2 Recommended Operating Conditions ($V_{CC} = 3.0V$ to $5.5V$ at $T_{opr} = -20$ to $85^{\circ}C/-40$ to $85^{\circ}C^{(3)}$)

Symbol	Parameter		Standard			Unit
			Min	Typ	Max	
V _{CC}	Supply voltage (Through VDC)		3.0	5.0	5.5	V
	Supply voltage (Not through VDC)		3.0	3.3	3.6	V
AV _{CC}	Analog supply voltage			V _{CC}		V
V _{SS}	Supply voltage			0		V
AV _{SS}	Analog supply voltage			0		V
V _{IH}	Input high ("H") voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87 ⁽⁴⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾ , X _{IN} , $\overline{\text{RESET}}$, CNV _{SS} , BYTE	0.8V _{CC}		V _{CC}	V
		P70, P71	0.8V _{CC}		6.0	
		P00-P07, P10-P17 (In single-chip mode)	0.8V _{CC}		V _{CC}	V
		P00-P07, P10-P17 (In memory expansion mode and microprocesor mode)	0.5V _{CC}		V _{CC}	V
V _{IL}	Input low ("L") voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 ⁽⁴⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾ , X _{IN} , $\overline{\text{RESET}}$, CNV _{SS} , BYTE	0		0.2V _{CC}	V
		P00-P07, P10-P17 (In single-chip mode)	0		0.2V _{CC}	V
		P00-P07, P10-P17 (In memory expansion mode and microprocesor mode)	0		0.16V _{CC}	V
I _{OH(peak)}	Peak output high ("H") current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾			-10.0	mA
I _{OH(avg)}	Average output high ("H") current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾			-5.0	mA
I _{OL(peak)}	Peak output low ("L") current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾			10.0	mA
I _{OL(avg)}	Average output low ("L") current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾			5.0	mA
f(X _{IN})	Main clock input frequency	Through VDC	V _{CC} =4.2 to 5.5V	0	32	MHz
			V _{CC} =3.0 to 5.5V	0	20	MHz
		Not through VDC	V _{CC} =3.0 to 3.6V	0	20	MHz
f(X _{CIN})	Sub clock oscillation frequency			32.768		kHz

NOTES:

- Output current is averaged with 100ms.
- Total $I_{OL(peak)}$ for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be less than or equal to 80mA.
Total $I_{OH(peak)}$ for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be less than or equal to -80mA.
Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be less than or equal to 80mA.
Total $I_{OH(peak)}$ for P3, P4, P5, P6, P72 to P77, P80 to P84, P12 and P13 must be less than or equal to -80mA.
- This is an option that is on request basis.
- V_{IH} and V_{IL} reference for P87 applies to P87 used as a programmable input ports. It does not apply to P87 used as X_{CIN} .
- P11 to P15 are provided in the 144-pin package only.

V_{CC} = 5V

**Table 5.3 Electrical Characteristics (V_{CC}=4.2 to 5.5V, V_{SS}=0V
at Topr= -20 to 85°C, unless otherwise specified)**

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V _{OH}	Output high ("H") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _{CC} =5V I _{OH} =-5mA	3.0			V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _{CC} =5V I _{OH} =-200μA	4.7			V
		X _{OUT}	V _{CC} =5V I _{OH} =-1mA	3.0			V
		X _{COUT}	No load applied		3.3		V
V _{OL}	Output low ("L") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	V
		X _{OUT}	I _{OL} =1mA			2.0	V
		X _{COUT}	No load applied		0		V
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, K10-K13, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input high ("H") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =V _{CC}			5.0	μA
I _{IL}	Input low ("L") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA
R _{PULLUP}	Pull-up resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	30	50	167	kΩ
R _{fXIN}	Feedback resistance	X _{IN}			1.5		MΩ
R _{fXCIN}	Feedback resistance	X _{CIN}			10		MΩ
V _{RAM}	RAM standby voltage	Through VDC		2.5			V
I _{CC}	Power supply current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(X _{IN})=32 MHz, square wave, no division		28	54	mA
			f(X _{CIN})=32 kHz, with a wait state, Topr=25° C		470		μA
			Topr=25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

V_{CC} = 5V

**Table 5.4 A-D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V
at T_{opr} = –20 to 85°C, unless otherwise specified)**

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution	V _{REF} =V _{CC}			10	Bits
INL	Integral nonlinearity error	V _{REF} =V _{CC} =5V			±3	LSB
						LSB
					±7	LSB
DNL	Differential nonlinearity error				±1	LSB
-	Offset error				±3	LSB
-	Gain error				±3	LSB
R _{LADDER}	Resistor ladder	V _{REF} =V _{CC}	8		40	kΩ
t _{CONV}	10-bit conversion time		2.1			μs
t _{CONV}	8-bit conversion time		1.8			μs
t _{SAMP}	Sample time		0.3			μs
V _{REF}	Reference voltage		2		V _{CC}	V
V _{IA}	Analog input voltage		0		V _{REF}	V

NOTES:

1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency less than or equal to 10 MHz.

**Table 5.5 D-A Conversion Characteristics (V_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V
at T_{opr} = –20 to 85°C, unless otherwise specified)**

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
t _{SU}	Setup time				3	μs
R _O	Output resistance		4	10	20	kΩ
I _{VREF}	Reference power supply input current	(Note 1)			1.5	mA

NOTES:

1. Measurement condition is that one of two D-A converters is used and the DA_i register (i=0, 1) for the unused D-A converter to "0016". The resistor ladder in the A-D converter is excluded.
I_{VREF} flows even if the ADiCON1 register is set to "0" (no V_{REF} connection).

V_{CC} = 5V

Timing Requirements (V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.6 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _c	External clock input cycle time	31.3		ns
t _{w(H)}	External clock input high ("H") pulse width	13		ns
t _{w(L)}	External clock input low ("L") pulse width	13		ns
t _r	External clock rising edge time		5	ns
t _f	External clock falling edge time		5	ns

Table 5.7 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{ac1} (RD-DB)	Data input access time (RD standard, with no wait state)		(Note 1)	ns
t _{ac1} (AD-DB)	Data input access time (AD standard, CS standard, with no wait state)		(Note 1)	ns
t _{ac2} (RD-DB)	Data input access time (RD standard, with a wait state)		(Note 1)	ns
t _{ac2} (AD-DB)	Data input access time (AD standard, CS standard, with a wait state)		(Note 1)	ns
t _{ac3} (RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t _{ac3} (AD-DB)	Data input access time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t _{ac4} (RAS-DB)	Data input access time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
t _{ac4} (CAS-DB)	Data input access time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
t _{ac4} (CAD-DB)	Data input access time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
t _{SU} (DB-BCLK)	Data input setup time	26		ns
t _{SU} (RDY-BCLK)	RDY input setup time	26		ns
t _{SU} (HOLD-BCLK)	HOLD input setup time	30		ns
t _h (RD-DB)	Data input hold time	0		ns
t _h (CAS-DB)	Data input hold time	0		ns
t _h (BCLK-RDY)	RDY input hold time	0		ns
t _h (BCLK-HOLD)	HOLD input hold time	0		ns
t _d (BCLK-HLDA)	HLDA output delay time		25	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency. Insert a wait state or use lower f(BCLK) as an operation frequency if a calculated value is negative.

$$t_{ac1}(RD - DB) = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1}(AD - DB) = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2}(RD - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2}(AD - DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3}(RD - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3}(AD - DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4}(RAS - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4}(CAS - DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ with 2 wait states})$$

$$t_{ac4}(CAD - DB) = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

V_{CC} = 5V

Timing Requirements

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C unless otherwise specified)

Table 5.8 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{in} input cycle time	100		ns
tw(TAH)	TA _{in} input high ("H") pulse width	40		ns
tw(TAL)	TA _{in} input low ("L") pulse width	40		ns

Table 5.9 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{in} input cycle time	400		ns
tw(TAH)	TA _{in} input high ("H") pulse width	200		ns
tw(TAL)	TA _{in} input low ("L") pulse width	200		ns

Table 5.10 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{in} input cycle time	200		ns
tw(TAH)	TA _{in} input high ("H") pulse width	100		ns
tw(TAL)	TA _{in} input low ("L") pulse width	100		ns

Table 5.11 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TA _{in} input high ("H") pulse width	100		ns
tw(TAL)	TA _{in} input low ("L") pulse width	100		ns

Table 5.12 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TA _{IOU} T input cycle time	2000		ns
tw(UPH)	TA _{IOU} T input high ("H") pulse width	1000		ns
tw(UPL)	TA _{IOU} T input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TA _{IOU} T input setup time	400		ns
th(TIN-UP)	TA _{IOU} T input hold time	400		ns

VCC = 5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.13 Timer B Input (Count Source Input in eEvent Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiN input high ("H") pulse width (counted on one edge)	40		ns
tw(TBL)	TBiN input low ("L") pulse width (counted on one edge)	40		ns
tc(TB)	TBiN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiN input high ("H") pulse width (counted on both edges)	80		ns
tw(TBL)	TBiN input low ("L") pulse width (counted on both edges)	80		ns

Table 5.14 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiN input cycle time	400		ns
tw(TBH)	TBiN input high ("H") pulse width	200		ns
tw(TBL)	TBiN input low ("L") pulse width	200		ns

Table 5.15 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiN input cycle time	400		ns
tw(TBH)	TBiN input high ("H") pulse width	200		ns
tw(TBL)	TBiN input low ("L") pulse width	200		ns

Table 5.16 A-D trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(AD)	ADTRG input high ("H") pulse width (trigger available at minimum)	1000		ns
tw(ADL)	ADTRG input low ("L") pulse width	125		ns

Table 5.17 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(CLK)	CLKi input cycle time	200		ns
tw(CLKH)	CLKi input high ("H") pulse width	100		ns
tw(CLKL)	CLKi input low ("L") pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input hold time	30		ns
th(C-Q)	RxDi input hold time	90		ns

Table 5.18 External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(INH)	INTi input high ("H") pulse width	250		ns
tw(INL)	INTi input low ("L") pulse width	250		ns

V_{CC} = 5V

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = –20 to 85°C unless otherwise specified)

Table 5.19 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time			18	ns
th(BCLK-ALE)	ALE signal output hold time		-2		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		-3		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
tw(WR)	Write pulse width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$td(DB - WR) = \frac{10^9}{f(BCLK)} - 20 \quad [ns]$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9}{f(BCLK) \times 2} - 15 \quad [ns]$$

V_{CC} = 5V

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C unless otherwise specified)

**Table 5.20 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time			18	ns
th(BCLK-ALE)	ALE signal output hold time		-2		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		-3		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
tw(WR)	Write pulse width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$td(DB - WR) = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states and } n=3 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=5 \text{ with 3 wait states})$$

V_{CC} = 5V

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C unless otherwise specified)

Table 5.21 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t _d (BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
t _h (BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
t _h (RD-AD)	Address output hold time (RD standard)		(Note 1)		ns
t _h (WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
t _d (BCLK-CS)	Chip-select signal output delay time			18	ns
t _h (BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
t _h (RD-CS)	Chip-select signal output hold time (RD standard)		(Note 1)		ns
t _h (WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
t _d (BCLK-RD)	RD signal output delay time			18	ns
t _h (BCLK-AD)	RD signal output hold time		-5		ns
t _d (BCLK-WR)	WR signal output delay time			18	ns
t _d (BCLK-WR)	WR signal output hold time		-3		ns
t _d (DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
t _h (DB-WR)	Data output hold time (WR standard)		(Note 1)		ns
t _d (BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
t _h (BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
t _d (AD-ALE)	ALE signal output delay time (address standard)		(Note 1)		ns
t _h (ALE-AD)	ALE signal output hold time (address standard)		(Note 1)		ns
t _{dZ} (RD-AD)	Address output high-impedance time			8	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [\text{ns}] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{d(AD-ALE)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [\text{ns}]$$

$$t_{h(ALE-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

V_{CC} = 5V

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Area)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t _d (BCLK-AD)	Row address output delay time	See Figure 5.1		18	ns
t _h (BCLK-AD)	Row address output hold time (BCLK standard)		-3		ns
t _h (BCLK-CAD)	Column address output delay time			18	ns
t _d (BCLK-CAD)	Column address output hold time (BCLK standard)		-3		ns
t _h (RAS-RAD)	Row address output hold time after RAS output		(Note 1)		ns
t _d (BCLK-RAS)	RAS output delay time (BCLK standard)			18	ns
t _h (BCLK-RAS)	RAS output hold time (BCLK standard)		-3		ns
t _{RP}	RAS high ("H") hold time		(Note 1)		ns
t _d (BCLK-CAS)	CAS output delay time (BCLK standard)			18	ns
t _h (BCLK-CAS)	CAS output hold time (BCLK standard)		-3		ns
t _d (BCLK-DW)	DW output delay time (BCLK standard)			18	ns
t _h (BCLK-DW)	DW output hold time (BCLK standard)		-5		ns
t _{su} (DB-CAS)	CAS output setup time after DB output		(Note 1)		ns
t _h (BCLK-DB)	DB signal output hold time (BCLK standard)		-7		ns
t _{su} (CAS-RAS)	CAS output setup time before RAS output (refresh)		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{h(RAS - RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9}{f_{(BCLK)} \times 2} \times 3 - 20 \quad [ns]$$

$$t_{su(DB - CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{su(CAS - RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

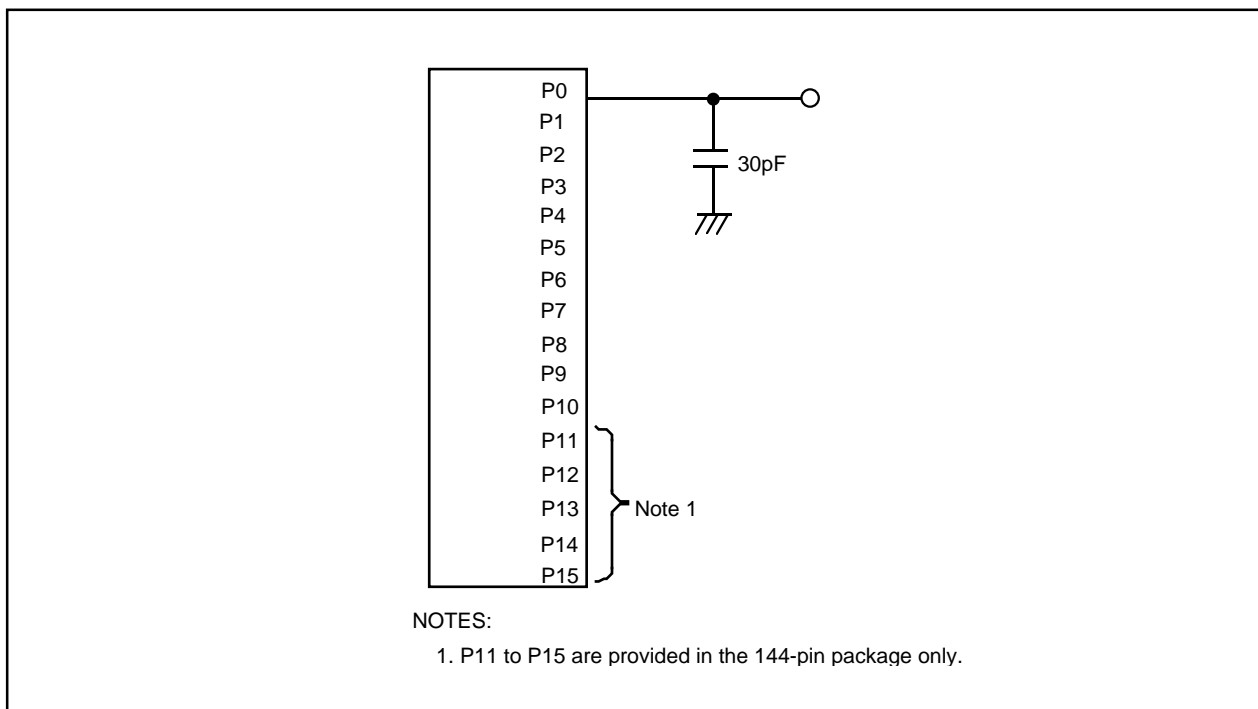


Figure 5.1 P0 to P15 Measurement Circuit

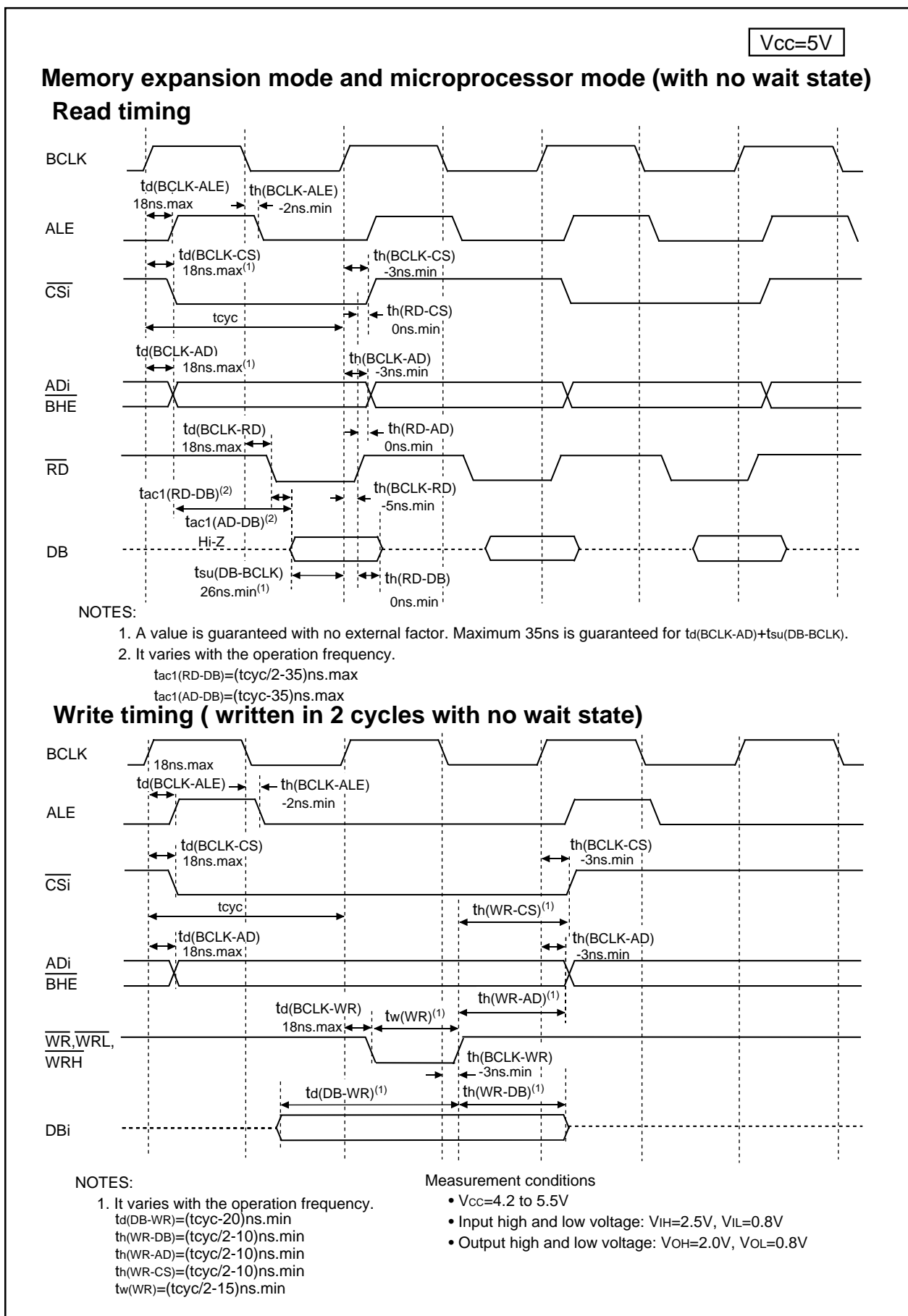


Figure 5.2 V_{CC}=5V Timing Diagram (1)

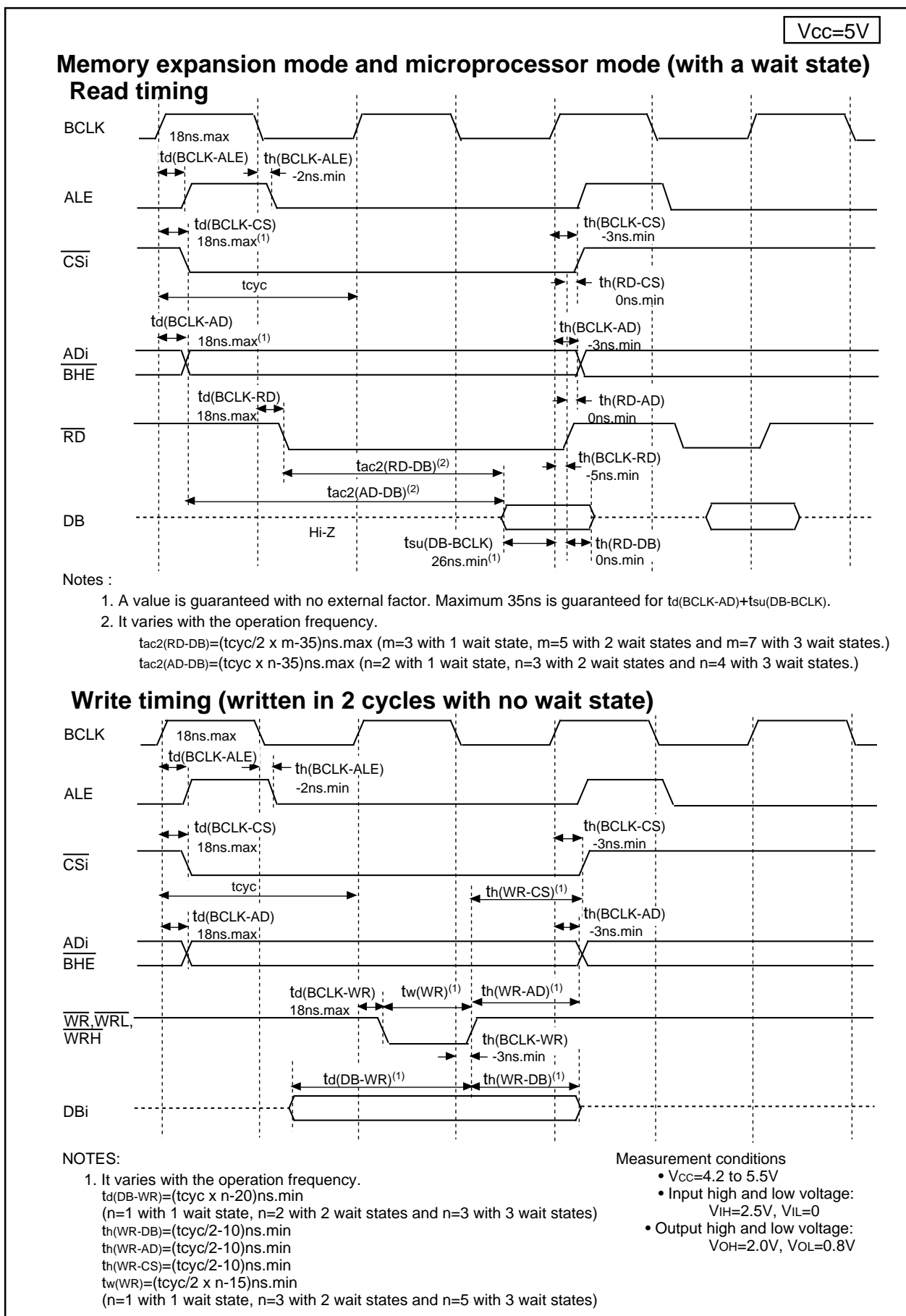


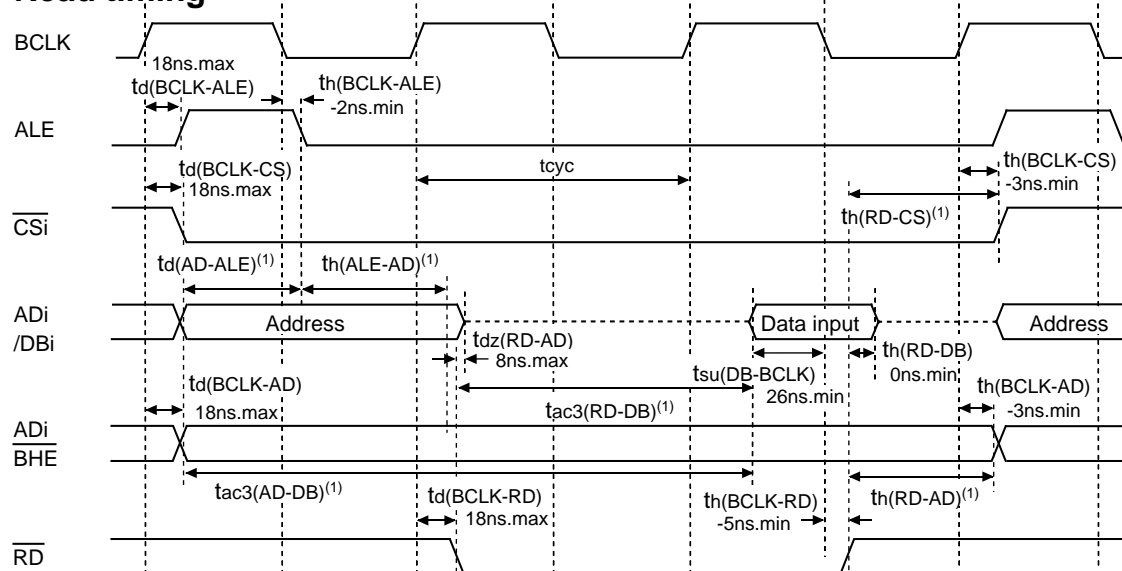
Figure 5.3 $V_{CC}=5V$ Timing Diagram (2)

Memory expansion mode and microprocessor mode

$V_{CC}=5V$

(with a wait state, when accessing an external memory and using the multiplexed bus)

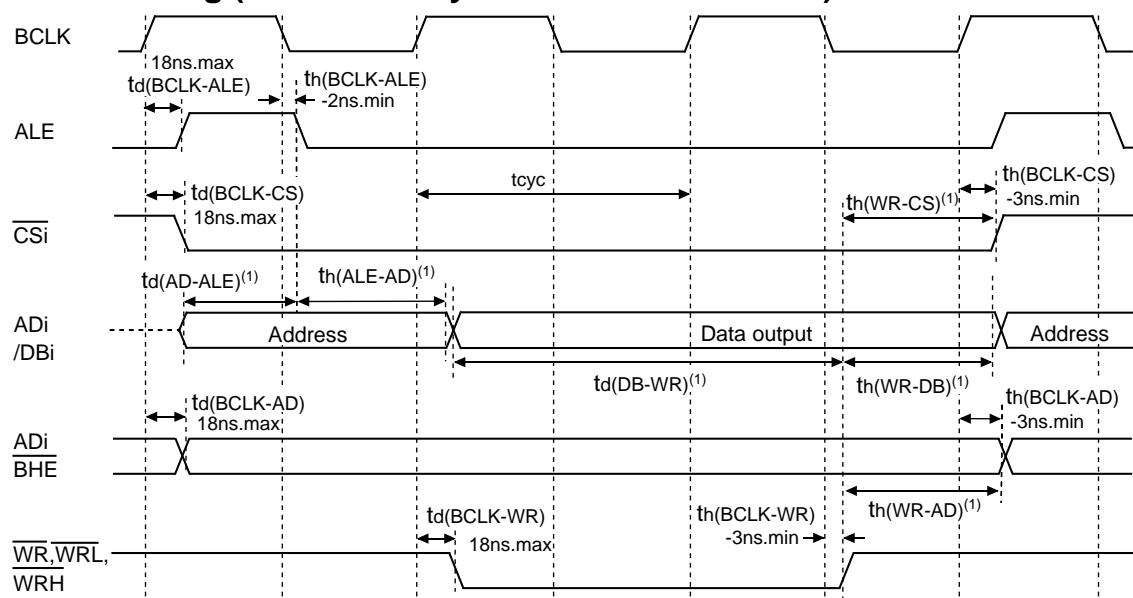
Read timing



NOTES:

- It varies with the operation frequency.
 $t_d(AD-ALE) = (tcyc/2 - 20)ns.min$
 $t_h(ALE-AD) = (tcyc/2 - 10)ns.min$, $t_h(RD-AD) = (tcyc/2 - 10)ns.min$, $t_h(RD-CS) = (tcyc/2 - 10)ns.min$
 $t_{ac3}(RD-DB) = (tcyc/2 \times m - 35)ns.max$ ($m=3$ with 2 wait states and $m=5$ with 3 wait states)
 $t_{ac3}(AD-DB) = (tcyc/2 \times n - 35)ns.max$ ($n=5$ with 2 wait states and $n=7$ with 3 wait states)

Write timing (written in 2 cycles with no wait state)



NOTES:

- It varies with the operation frequency.
 $t_d(AD-ALE) = (tcyc/2 - 20)ns.min$
 $t_h(ALE-AD) = (tcyc/2 - 10)ns.min$, $t_h(WR-AD) = (tcyc/2 - 10)ns.min$
 $t_h(WR-CS) = (tcyc/2 - 10)ns.min$, $t_h(WR-DB) = (tcyc/2 - 10)ns.min$
 $t_d(DB-WR) = (tcyc/2 \times m - 25)ns.min$

Measurement conditions

- $V_{CC}=4.2$ to $5.5V$
- Input high and low voltage:
 $V_{IH}=2.5V$, $V_{IL}=0.8V$
- Output high and low voltage:
 $V_{OH}=2.0V$, $V_{OL}=0.8V$

Figure 5.4 $V_{CC}=5V$ Timing Diagram (3)

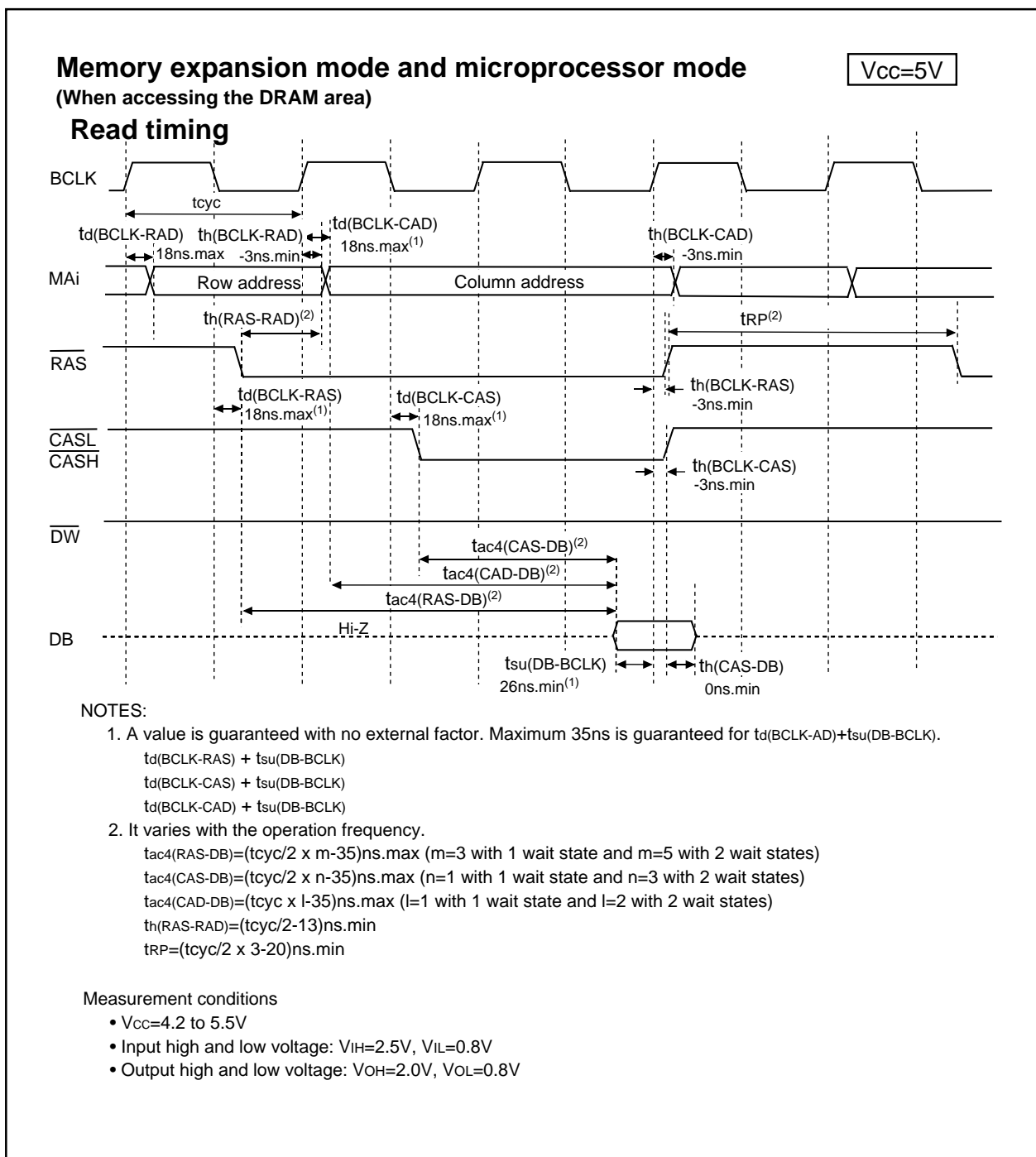


Figure 5.5 $V_{CC}=5V$ Timing Diagram (4)

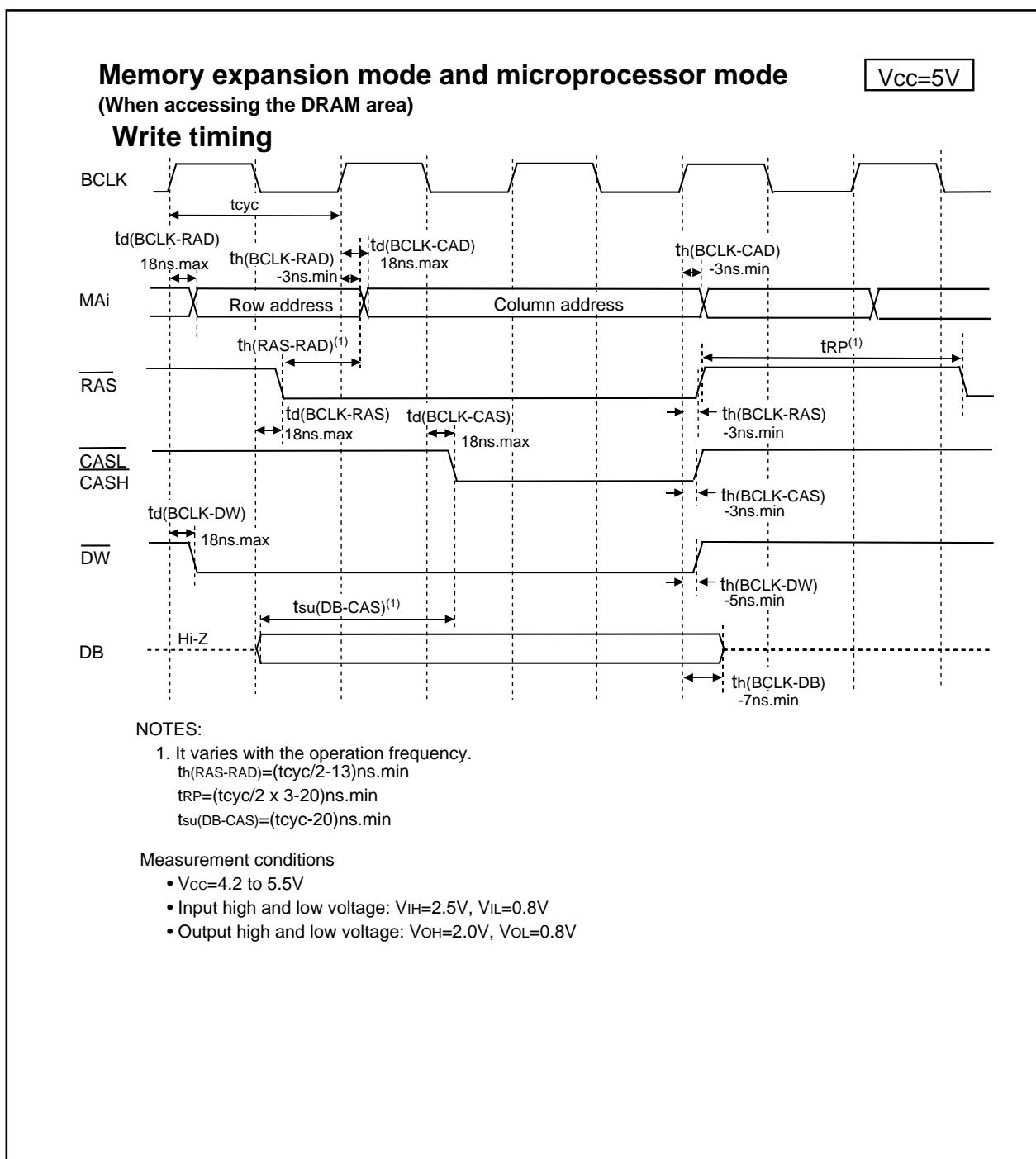
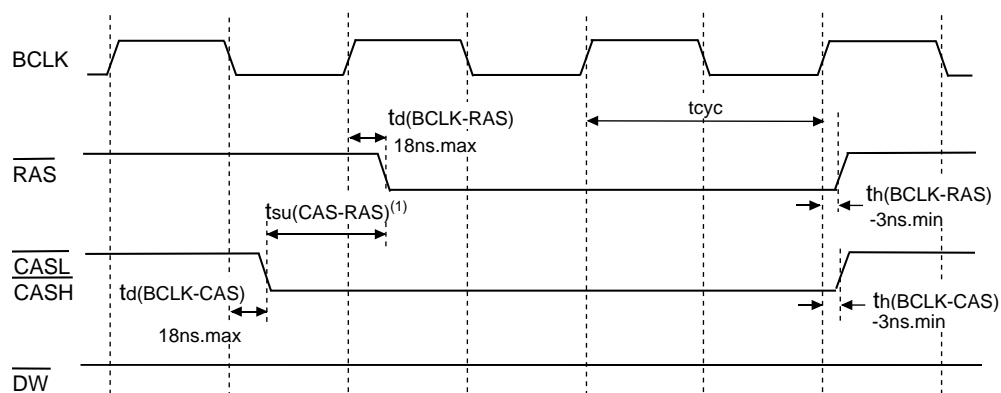


Figure 5.6 $V_{CC}=5V$ Timing Diagram (5)

Memory expansion mode and microprocessor mode Refresh timing (CAS-before-RAS refresh)

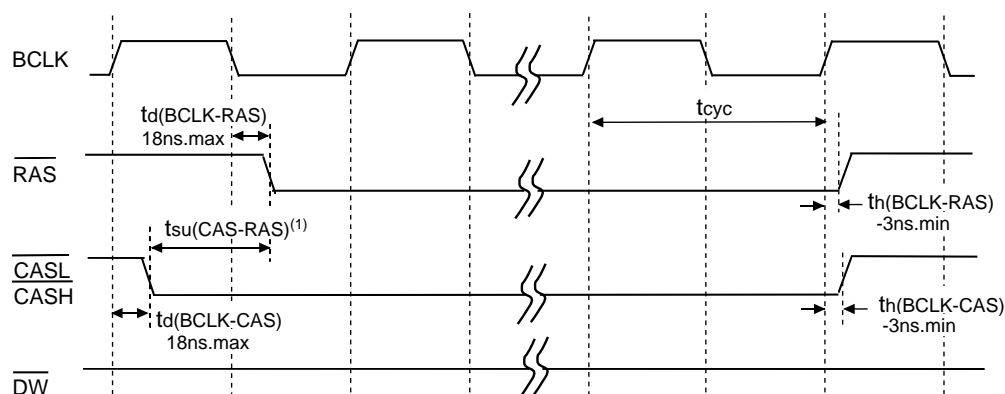
V_{CC}=5V



NOTES :

1. It varies with the operation frequency.
 $t_{su}(CAS-RAS) = (tcyc/2 - 13)ns.min$

Refresh timing (Self-refresh)



NOTES:

1. It varies with the operation frequency.
 $t_{su}(CAS-RAS) = (tcyc/2 - 13)ns.min$

Measurement conditions

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.7 V_{CC}=5V Timing Diagram (6)

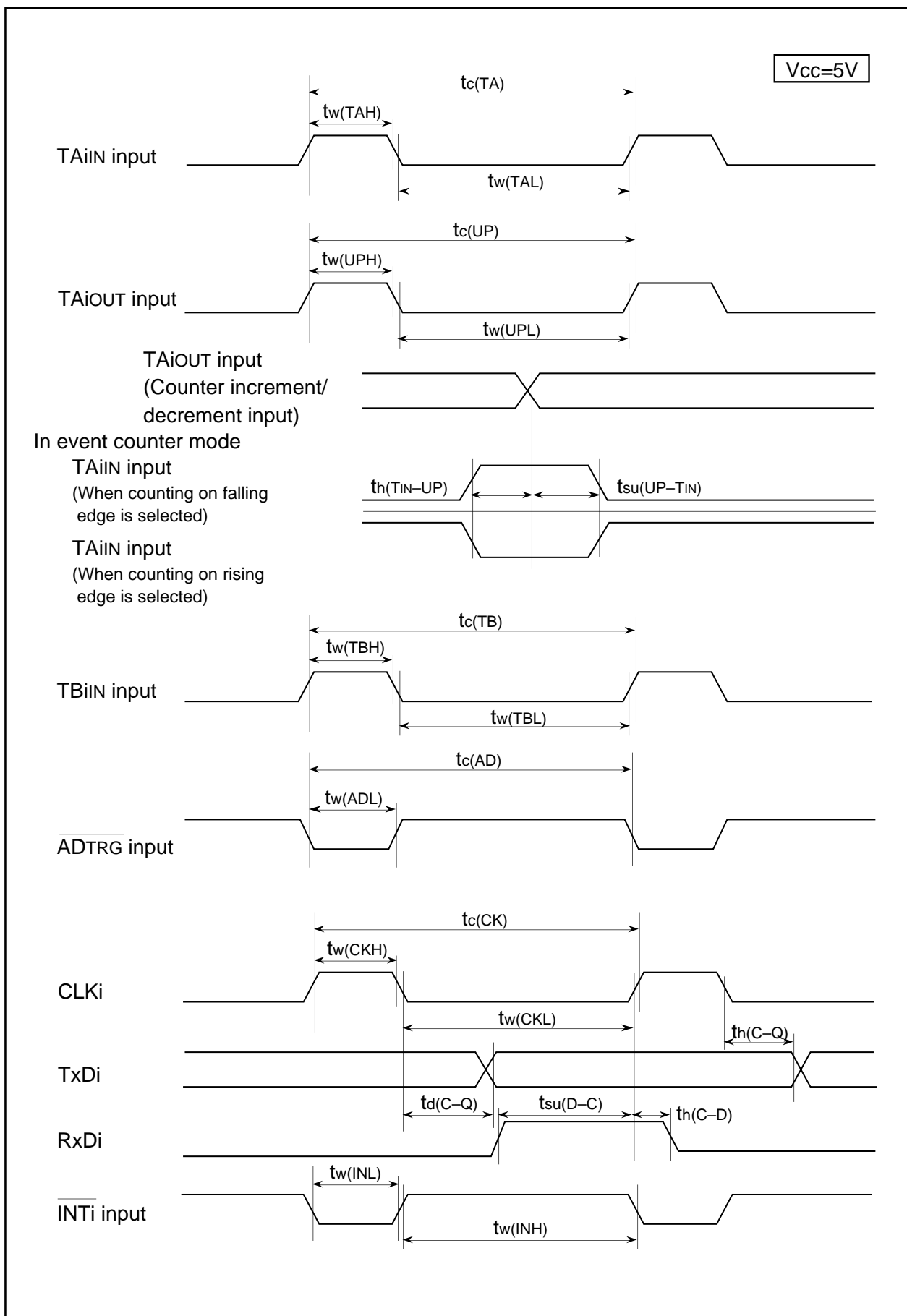


Figure 5.8 $V_{CC}=5V$ Timing Diagram (7)

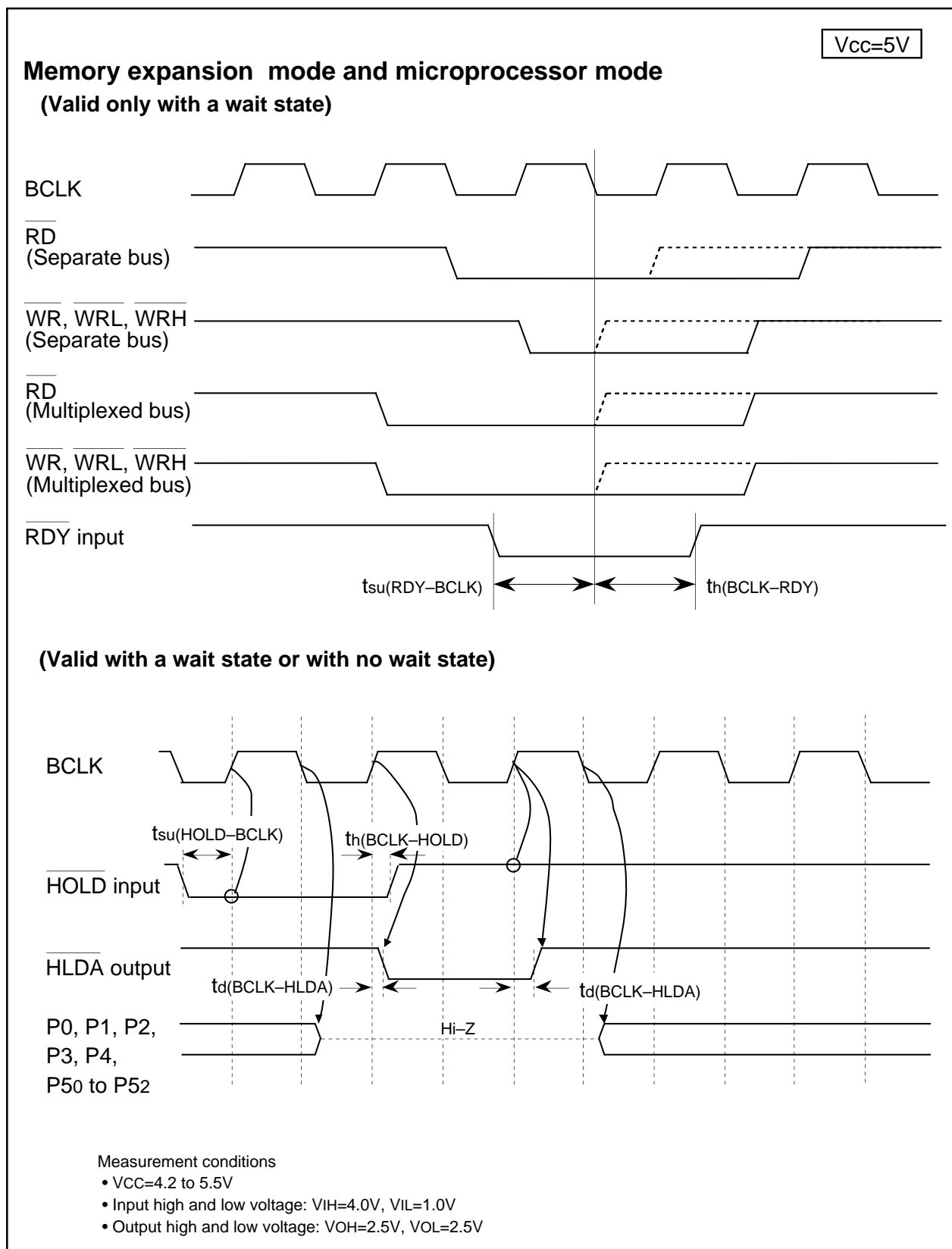


Figure 5.9 $V_{CC}=5V$ Timing Diagram (8)

VCC = 3.3V

Table 5.23 Electrical Characteristics (VCC=3.0 to 3.6V, VSS=0V at Topr = -20 to 85°C, unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
VOH	Output high ("H") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} = -1mA	2.7			V
		X _{OUT}	I _{OH} = -0.1mA	2.7			V
		X _{COU} T	No load applied		3.3		V
VOL	Output low ("L") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} = 1mA			0.5	V
		X _{OUT}	I _{OL} = 0.1mA			0.5	V
		X _{COU} T	No load applied		0		V
VT+ - VT-	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input high ("H") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNVSS, BYTE	V _I = VCC			4.0	μA
I _{IL}	Input low ("L") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNVSS, BYTE	V _I = 0V			-4.0	μA
R _{PULLUP}	Pull-up resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I = 0V	66	120	500	kΩ
R _{fXIN}	Feedback resistance	X _{IN}			3.0		MΩ
R _{fXCIN}	Feedback resistance	X _{CIN}			20.0		MΩ
V _{RAM}	RAM standby voltage	Through VDC		2.5			V
		Not through VDC		2.0			
I _{CC}	Power supply current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to VSS.	f(X _{IN})=20 MHz, square wave, no division		17	38	mA
			f(X _{CIN})=32 kHz, with a wait state, not through VDC, Topr=25° C		5.0		μA
			f(X _{CIN})=32 kHz, with a wait state, through VDC, Topr=25° C		340		μA
			Topr=25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$$V_{CC} = 3.3V$$

$$V_{SS} = AV_{SS} = 0V$$

Table 5.24 A-D Conversion Characteristics (VCC = AVCC = VREF = 3.0 to 3.6V, at Topr = –20 to 85°C, unless otherwise specified)

Symbol	Parameter		Measurement condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		VREF=VCC			10	Bits
INL	Integral nonlinearity error	No S&H function (8-bit)	VCC=VREF=3.3V			±2	LSB
DNL	Differential nonlinearity error	No S&H function (8-bit)				±1	LSB
-	Offset error	No S&H function (8-bit)				±2	LSB
-	Gain error	No S&H function (8-bit)				±2	LSB
RLADDER	Resistor ladder		VREF=VCC	8		40	kΩ
tCONV	8-bit conversion time			1.8			μs
VREF	Reference voltage			3.0		VCC	V
VIA	Analog input voltage			0		VREF	V

S&H: Sample and hold

NOTES:

1. Divide f(XIN), if exceeding 10 MHz, to keep φAD frequency less than or equal to 10 MHz.

Table 5.25 D-A Conversion Characteristics (VCC = VREF = 3.0 to 3.6V, VSS = AVSS = 0V at Topr = –20 to 85°C, unless otherwise specified)

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
tsu	Setup time				3	μs
Ro	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(Note 1)			1.0	mA

NOTES:

1. Measurement condition is that one of two D-A converters is used and the DAi register (i=0, 1) for the unused D-A converter to "0016". The resistor ladder in the A-D converter is excluded.
IVREF flows even if the ADiCON1 register is set to "0" (no VREF connection).

VCC = 3.3V

Timing Requirements (VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.26 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External clock input cycle time	50		ns
tw(H)	External clock input high ("H") pulse width	22		ns
tw(L)	External clock input low ("L") pulse width	22		ns
tr	External clock rising-edge time		5	ns
tf	External clock falling-edge time		5	ns

Table 5.27 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data input access time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data input access time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data input access time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data input access time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data input access time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data input setup time	30		ns
tsu(RDY-BCLK)	RDY input setup time	40		ns
tsu(HOLD-BCLK)	HOLD input setup time	60		ns
th(RD-DB)	Data input hold time	0		ns
th(CAS-DB)	Data input hold time	0		ns
th(BCLK-RDY)	RDY input hold time	0		ns
th(BCLK-HOLD)	HOLD input hold time	0		ns
td(BCLK-HLDA)	HLDA output delay time		25	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency. Insert a wait state or use lower f(BCLK) as an operation frequency if a calculated value is negative.

$$t_{ac1}(RD - DB) = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1}(AD - DB) = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2}(RD - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2}(AD - DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3}(RD - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3}(AD - DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4}(RAS - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4}(CAS - DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ with 2 wait states})$$

$$t_{ac4}(CAD - DB) = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

VCC = 3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin input cycle time	100		ns
tw(TAH)	TAin input high ("H") pulse width	40		ns
tw(TAL)	TAin input low ("L") pulse width	40		ns

Table 5.29 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin input cycle time	400		ns
tw(TAH)	TAin input high ("H") pulse width	200		ns
tw(TAL)	TAin input low ("L") pulse width	200		ns

Table 5.30 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin input cycle time	200		ns
tw(TAH)	TAin input high ("H") pulse width	100		ns
tw(TAL)	TAin input low ("L") pulse width	100		ns

Table 5.31 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TAin input high ("H") pulse width	100		ns
tw(TAL)	TAin input low ("L") pulse width	100		ns

Table 5.32 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high ("H") pulse width	1000		ns
tw(UPL)	TAiOUT input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

VCC = 3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.33 Timer B input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBin input cycle time (counted on one edge)	100		ns
tw(TBH)	TBin input high ("H") pulse width (counted on one edge)	40		ns
tw(TBL)	TBin input low ("L") pulse width (counted on one edge)	40		ns
tc(TB)	TBin input cycle time (counted on both edges)	200		ns
tw(TBH)	TBin input high ("H") pulse width (counted on both edges)	80		ns
tw(TBL)	TBin input low ("L") pulse width (counted on both edges)	80		ns

Table 5.34 Timer B input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBin input cycle time	400		ns
tw(TBH)	TBin input high ("H") pulse width	200		ns
tw(TBL)	TBin input low ("L") pulse width	200		ns

Table 5.35 Timer B input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBin input cycle time	400		ns
tw(TBH)	TBin input high ("H") pulse width	200		ns
tw(TBL)	TBin input low ("L") pulse width	200		ns

Table 5.36 A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(AD)	ADTRG input high ("H") pulse width (trigger available at minimum)	1000		ns
tw(ADL)	ADTRG input low ("L") pulse width	125		ns

Table 5.37 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(CLK)	CLKi input cycle time	200		ns
tw(CLKH)	CLKi input high ("H") pulse width	100		ns
tw(CLKL)	CLKi input low ("L") pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input hold time	30		ns
th(C-Q)	RxDi input hold time	90		ns

Table 5.38 External Interrupt INTi input

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(INH)	INTi input high ("H") pulse width	250		ns
tw(INL)	INTi input low ("L") pulse width	250		ns

V_{CC} = 3.3V

Switching Characteristics

(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at T_{opr} = –20 to 85°C, unless otherwise specified)

Table 5.39 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t _d (BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
t _h (BCLK-AD)	Address output hold time (BCLK standard)		0		ns
t _h (RD-AD)	Address output hold time (RD standard)		0		ns
t _h (WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
t _d (BCLK-CS)	Chip-select signal output delay time			18	ns
t _h (BCLK-CS)	Chip-select signal output hold time (BCLK standard)		0		ns
t _h (RD-CS)	Chip-select signal output hold time (RD standard)		0		ns
t _h (WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
t _d (BCLK-ALE)	ALE signal output delay time			18	ns
t _h (BCLK-ALE)	ALE signal output hold time		-2		ns
t _d (BCLK-RD)	RD signal output delay time			18	ns
t _h (BCLK-RD)	RD signal output hold time		-3		ns
t _d (BCLK-WR)	WR signal output delay time			18	ns
t _d (BCLK-WR)	WR signal output hold time		0		ns
t _d (DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
t _h (WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
t _w (WR)	WR output width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_d(\text{DB} - \text{WR}) = \frac{10^9}{f(\text{BCLK})} - 20 \quad [\text{ns}]$$

$$t_h(\text{WR} - \text{DB}) = \frac{10^9}{f(\text{BCLK}) \times 2} - 10 \quad [\text{ns}]$$

$$t_h(\text{WR} - \text{AD}) = \frac{10^9}{f(\text{BCLK}) \times 2} - 10 \quad [\text{ns}]$$

$$t_h(\text{WR} - \text{CS}) = \frac{10^9}{f(\text{BCLK}) \times 2} - 10 \quad [\text{ns}]$$

$$t_w(\text{WR}) = \frac{10^9}{f(\text{BCLK}) \times 2} - 15 \quad [\text{ns}]$$

V_{CC} = 3.3V

Switching Characteristics

(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at T_{opr} = –20 to 85°C unless otherwise specified)

**Table 5.40 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		0		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		0		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time			18	ns
th(BCLK-ALE)	ALE signal output hold time		-2		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-3		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
tw(WR)	WR output width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$td(DB - WR) = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states and } n=3 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=5 \text{ with 3 wait states})$$

V_{CC} = 3.3V

Switching Characteristics

(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at T_{opr} = -20 to 85°C unless otherwise specified)

Table 5.41 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		0		ns
th(RD-AD)	Address output hold time (RD standard)		(Note 1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		0		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-AD)	RD signal output hold time		-3		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(DB-WR)	Data output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(Note 1)		ns
tdZ(RD-AD)	Address output high-impedance time			8	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD - ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

V_{CC} = 3.3V

Switching Characteristics

(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at T_{opr} = –20 to 85°C unless otherwise specified)

Table 5.42 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Area)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t _d (BCLK-AD)	Row address output delay time	See Figure 5.1		18	ns
t _h (BCLK-AD)	Row address output hold time (BCLK standard)		0		ns
t _h (BCLK-CAD)	Column address output delay time			18	ns
t _d (BCLK-CAD)	Column address output hold time (BCLK standard)		0		ns
t _h (RAS-RAD)	Row address output hold time after RAS output		(Note 1)		ns
t _d (BCLK-RAS)	RAS output delay time (BCLK standard)			18	ns
t _h (BCLK-RAS)	RAS output hold time (BCLK standard)		0		ns
t _{RP}	RAS high ("H") hold time		(Note 1)		ns
t _d (BCLK-CAS)	CAS output delay time (BCLK standard)			18	ns
t _h (BCLK-CAS)	CAS output hold time (BCLK standard)		0		ns
t _d (BCLK-DW)	DW output delay time (BCLK standard)			18	ns
t _h (BCLK-DW)	DW output hold time (BCLK standard)		-3		ns
t _{su} (DB-CAS)	CAS output setup time after DB output		(Note 1)		ns
t _h (BCLK-DB)	DB signal output hold time (BCLK standard)		-7		ns
t _{su} (CAS-RAS)	CAS output setup time before RAS output (refresh)		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_h(\text{RAS} - \text{RAD}) = \frac{10^9}{f(\text{BCLK}) \times 2} - 13 \quad [\text{ns}]$$

$$t_{RP} = \frac{10^9 \times 3}{f(\text{BCLK}) \times 2} - 20 \quad [\text{ns}]$$

$$t_{su}(\text{DB} - \text{CAS}) = \frac{10^9}{f(\text{BCLK})} - 20 \quad [\text{ns}]$$

$$t_{su}(\text{CAS} - \text{RAS}) = \frac{10^9}{f(\text{BCLK}) \times 2} - 13 \quad [\text{ns}]$$

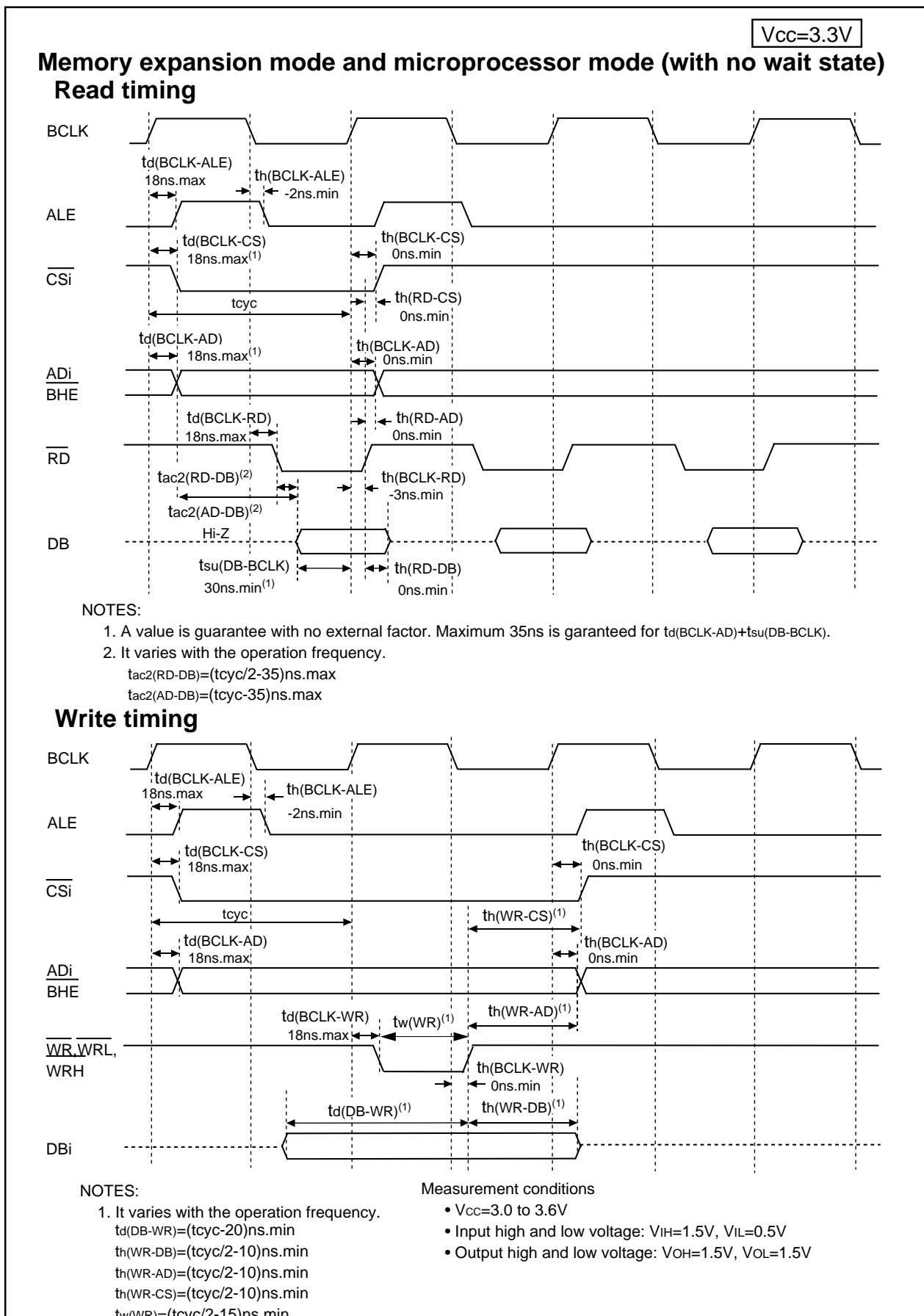


Figure 5.10 V_{CC}=3.3V Timing Diagram (1)

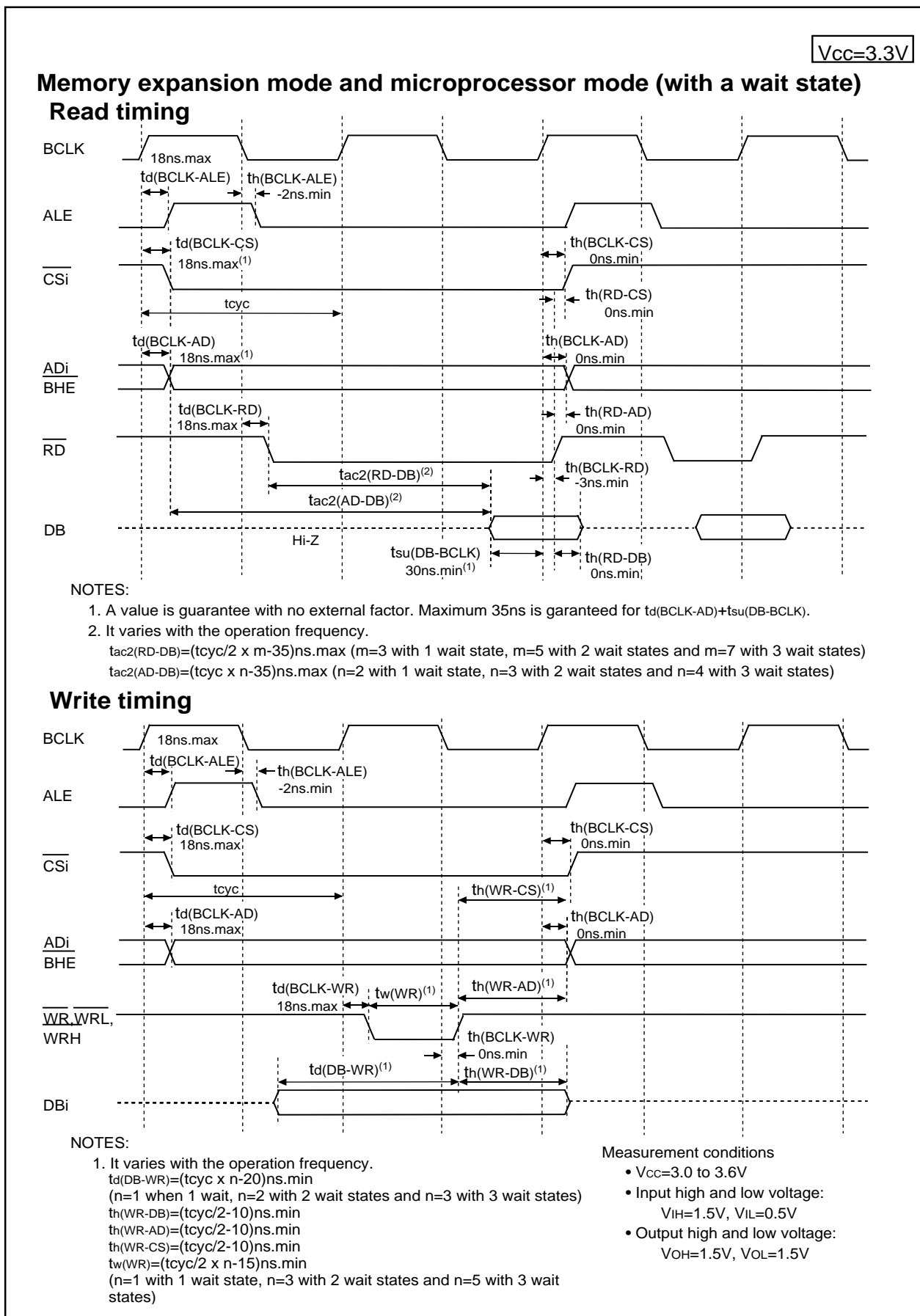


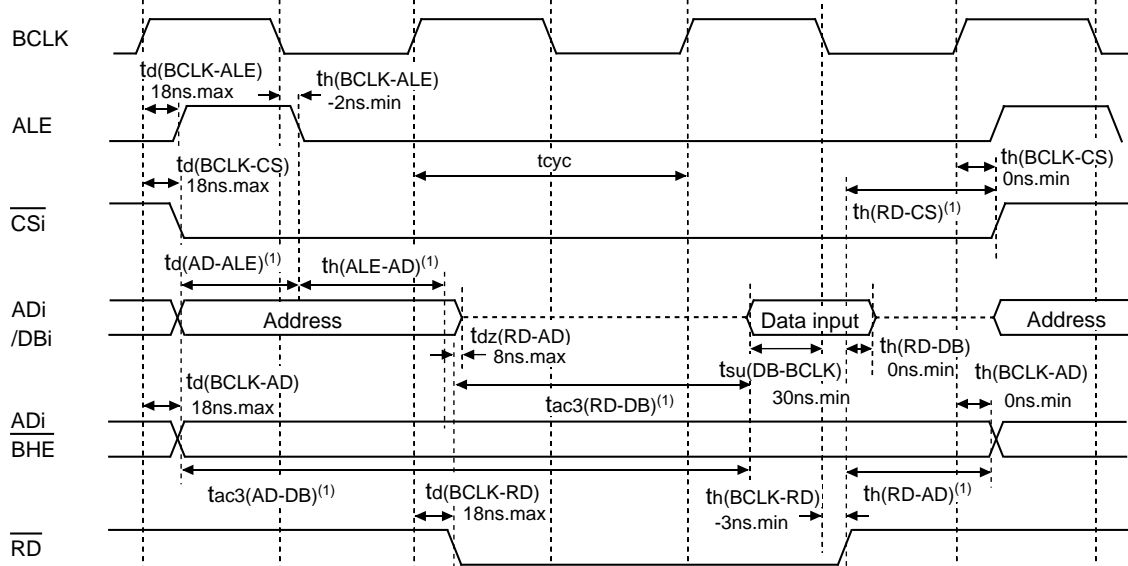
Figure 5.11 V_{CC}=3.3V Timing Diagram (2)

Memory expansion mode and microprocessor mode

$V_{CC}=3.3V$

(with a wait state, when accessing an external memory and using the multiplexed bus)

Read timing



NOTES:

1. It varies with the operation frequency.

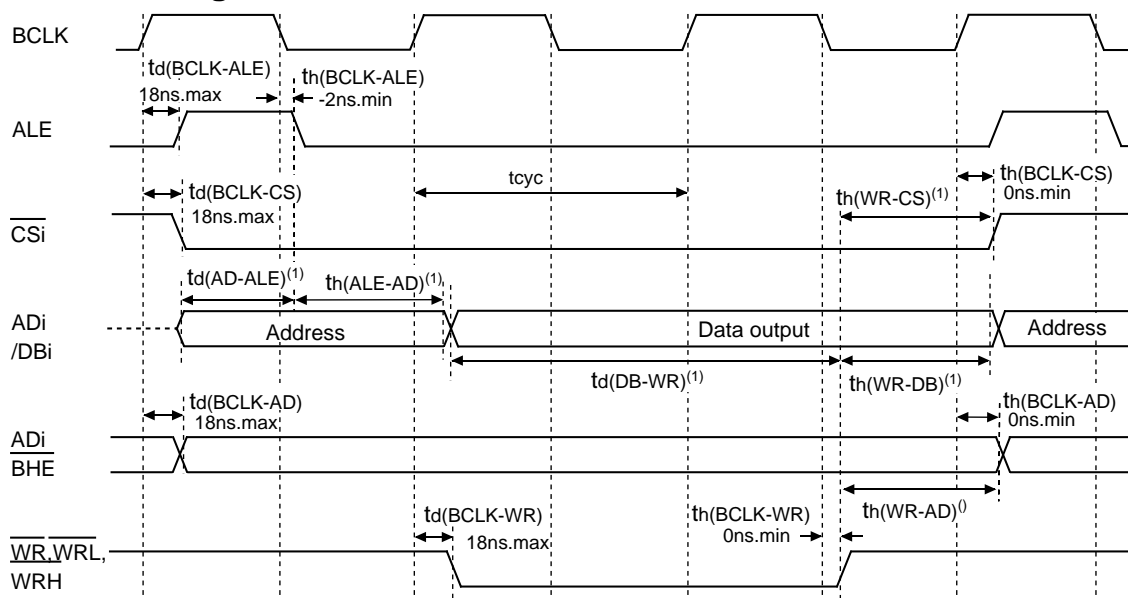
$$t_d(\text{AD-ALE}) = (t_{\text{cyc}}/2 - 20)\text{ns.min}$$

$$t_h(\text{ALE-AD}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}, t_h(\text{RD-AD}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}, t_h(\text{RD-CS}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}$$

$$t_{\text{ac3}}(\text{RD-DB}) = (t_{\text{cyc}}/2 \times m - 35)\text{ns.max} \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{\text{ac3}}(\text{AD-DB}) = (t_{\text{cyc}}/2 \times n - 35)\text{ns.max} \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

Write Timing



NOTES:

1. It varies with the operation frequency.

$$t_d(\text{AD-ALE}) = (t_{\text{cyc}}/2 - 20)\text{ns.min}$$

$$t_h(\text{ALE-AD}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}, t_h(\text{WR-AD}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}$$

$$t_h(\text{WR-CS}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}, t_h(\text{WR-DB}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}$$

$$t_d(\text{DB-WR}) = (t_{\text{cyc}}/2 \times m - 25)\text{ns.min} \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

Measurement conditions

- $V_{CC}=3.0$ to $3.6V$
- Input high and low voltage:
 $V_{IH}=1.5V$, $V_{IL}=0.5V$
- Output high and low voltage:
 $V_{OH}=1.5V$, $V_{OL}=1.5V$

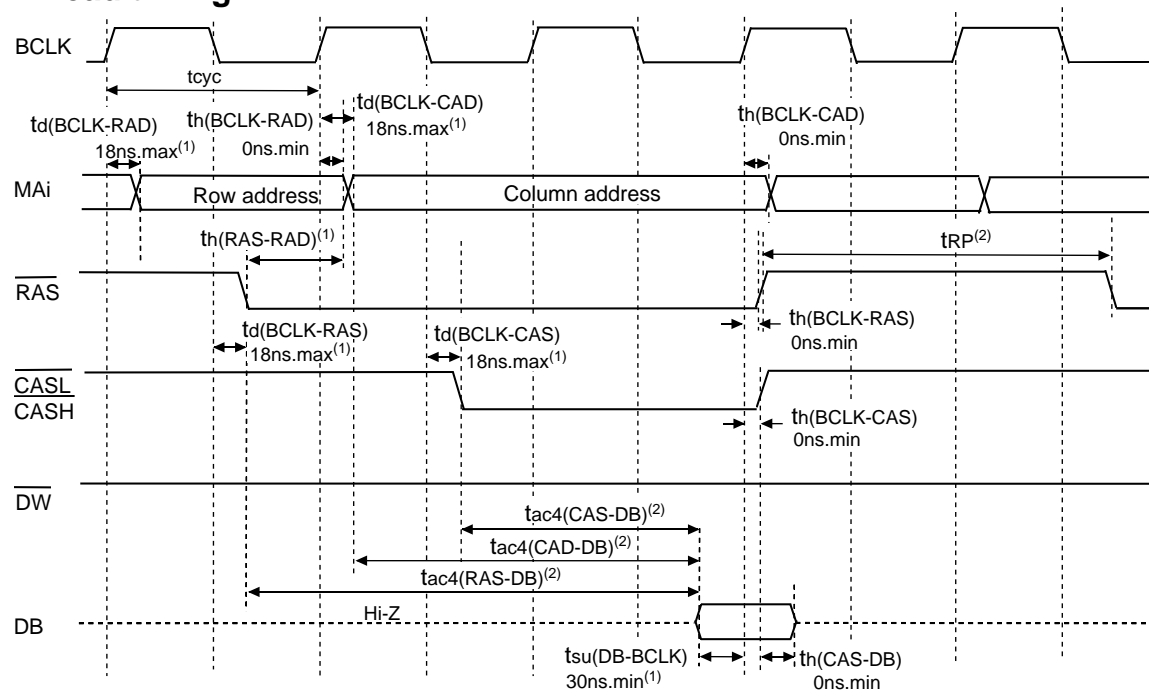
Figure 5.12 $V_{CC}=3.3V$ Timing Diagram (3)

Memory expansion mode and microprocessor mode

$V_{CC}=3.3V$

(With 2 wait states, when accessing the DRAM area)

Read timing



NOTES:

1. A value is guaranteed with no external factor. Maximum 35ns is guaranteed for the followings:

$td(BCLK-RAS) + tsu(DB-BCLK)$
 $td(BCLK-CAS) + tsu(DB-BCLK)$
 $td(BCLK-CAD) + tsu(DB-BCLK)$

2. It varies with the operation frequency.

$tac4(RAS-DB) = (tcyc/2 \times m - 35)ns.max$ ($m=3$ with 1 wait state and $m=5$ with 2 wait states)

$tac4(CAS-DB) = (tcyc/2 \times n - 35)ns.max$ ($n=1$ with 1 wait state and $n=3$ with 2 wait states)

$tac4(CAD-DB) = (tcyc \times l - 35)ns.max$ ($l=1$ with 1 wait state and $l=2$ with 2 wait states)

$th(RAS-RAD) = (tcyc/2 - 13)ns.min$

$tRP = (tcyc/2 \times 3 - 20)ns.min$

Measurement conditions

- $V_{CC}=3.0$ to $3.6V$
- Input high and low voltage: $V_{IH}=1.5V$, $V_{IL}=0.5V$
- Output high and low voltage: $V_{OH}=1.5V$, $V_{OL}=1.5V$

Figure 5.13 $V_{CC}=3.3V$ Timing Diagram (4)

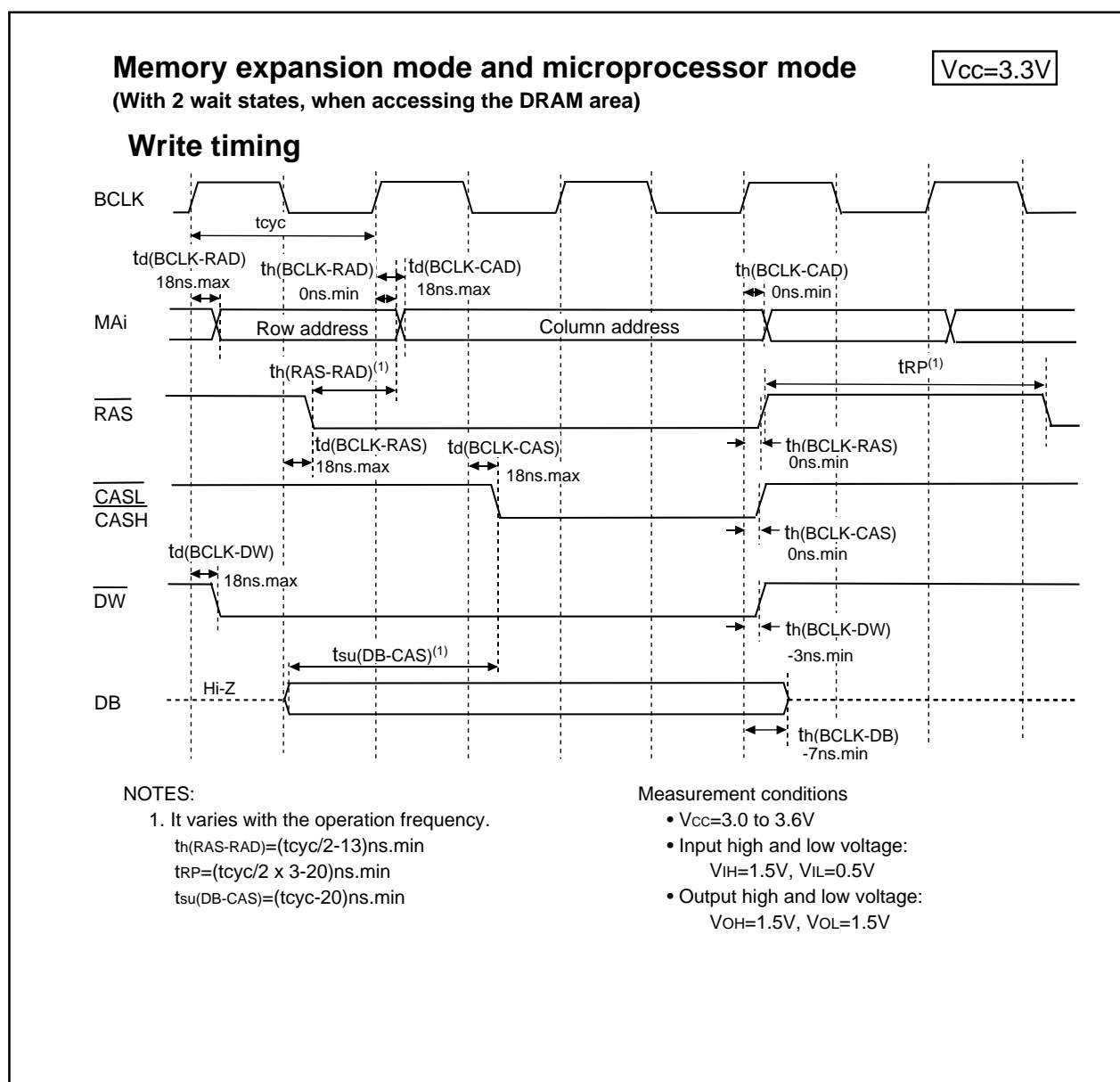
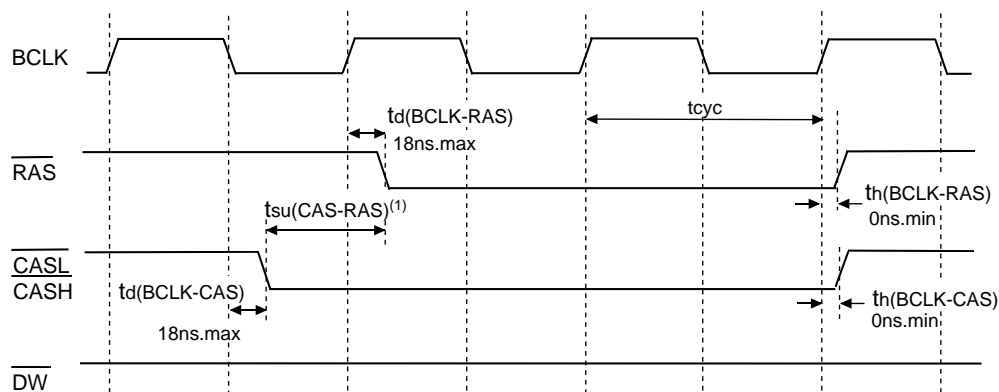


Figure 5.14 $V_{CC}=3.3V$ Timing Diagram (5)

Memory expansion mode and microprocessor mode $V_{CC}=3.3V$ Refresh timing (CAS-before-RAS refresh)

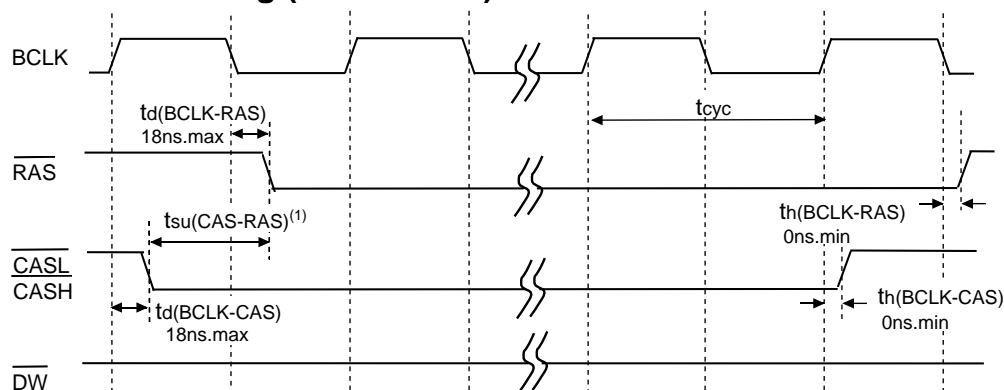


NOTES:

1. It varies with the operation frequency.

$$t_{su}(\text{CAS-RAS}) = (t_{cyc}/2 - 13)\text{ns.min}$$

Refresh timing (Self-refresh)



NOTES:

1. It varies with the operation frequency.

$$t_{su}(\text{CAS-RAS}) = (t_{cyc}/2 - 13)\text{ns.min}$$

Measurement conditions

- $V_{CC}=3.0$ to $3.6V$
- Input high and low voltage: $V_{IH}=1.5V$, $V_{IL}=0.5V$
- Output high and low voltage: $V_{OH}=1.5V$, $V_{OL}=1.5V$

Figure 5.15 $V_{CC}=3.3V$ Timing Diagram (6)

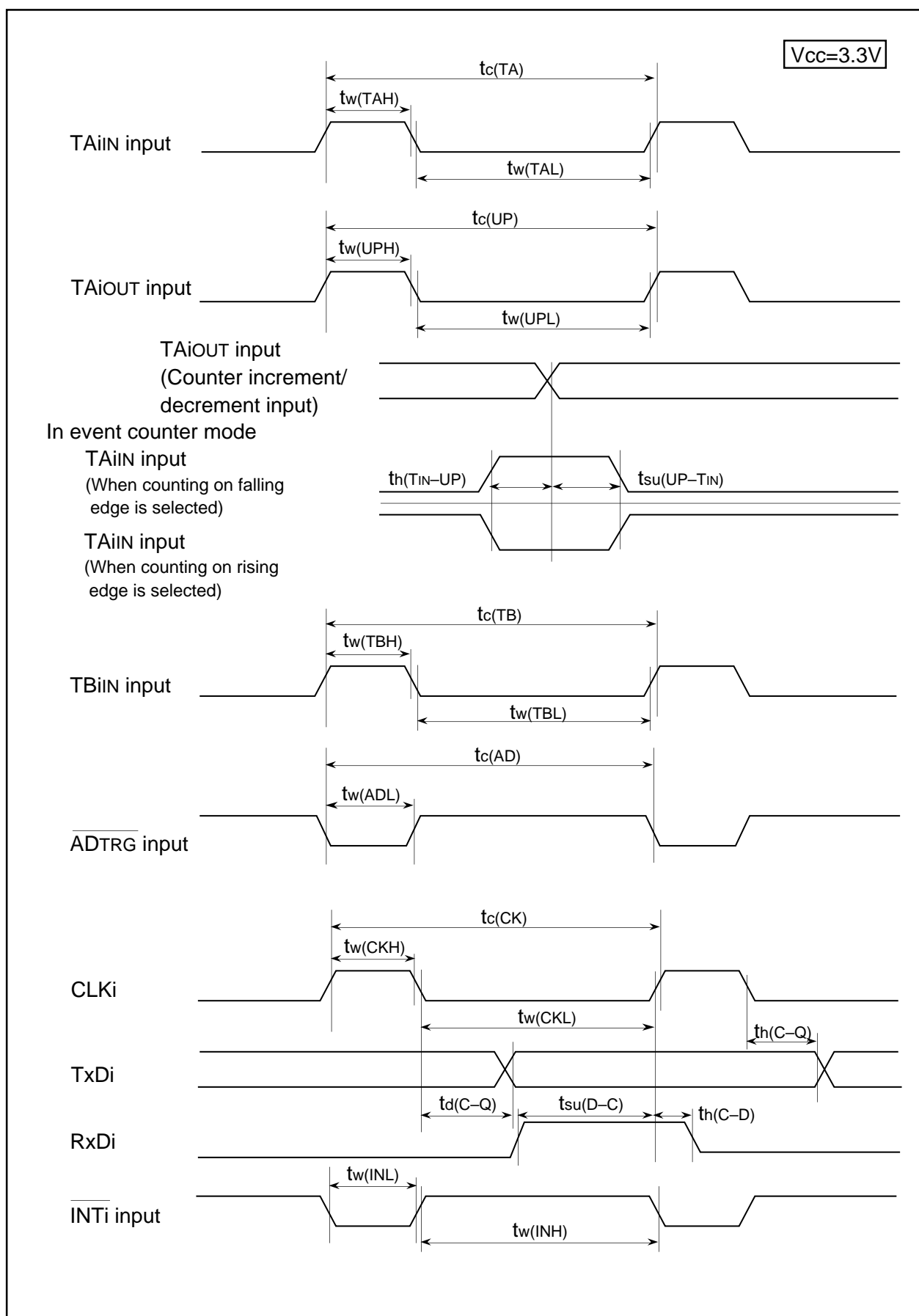


Figure 5.16 $V_{CC}=3.3V$ Timing Diagram (7)

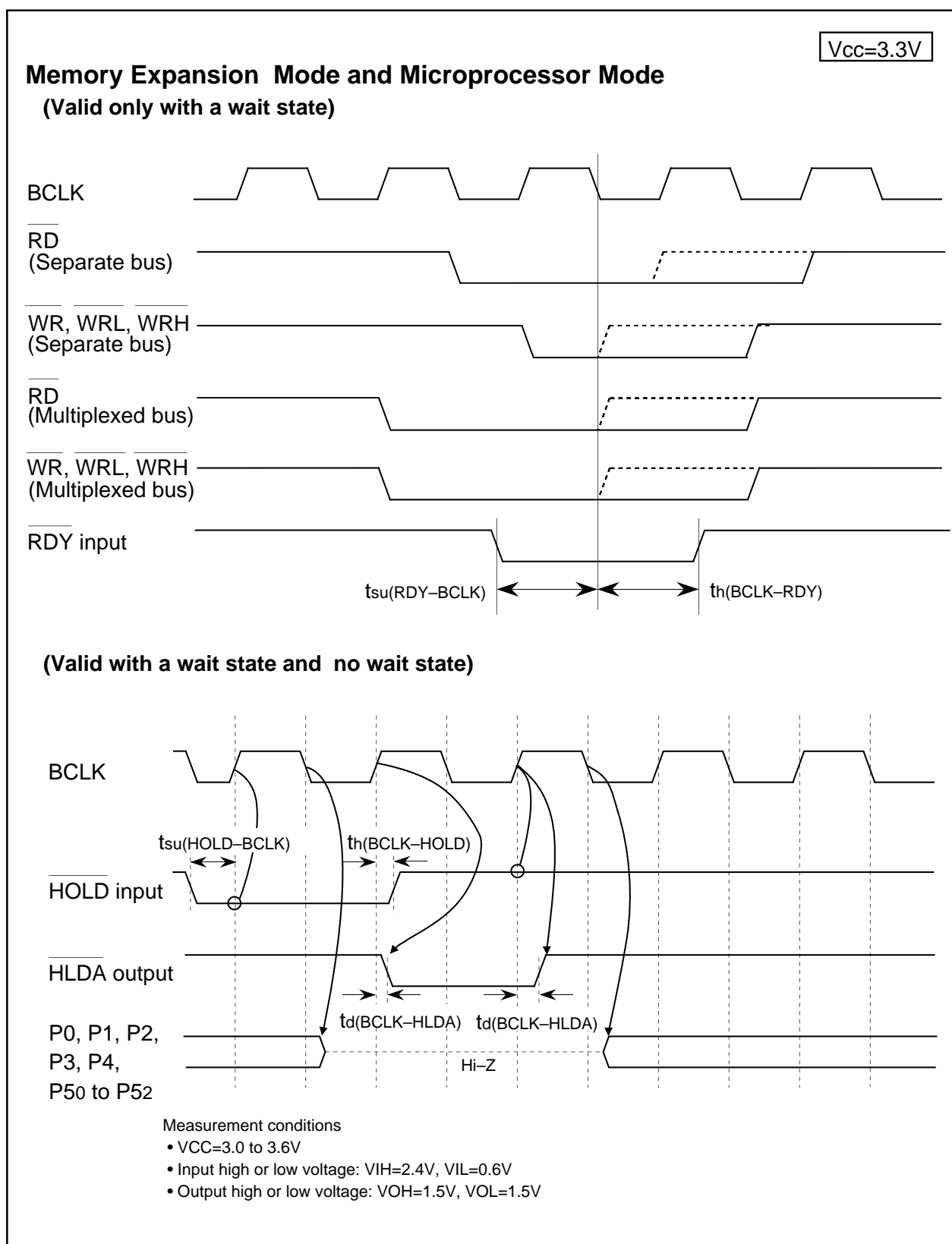
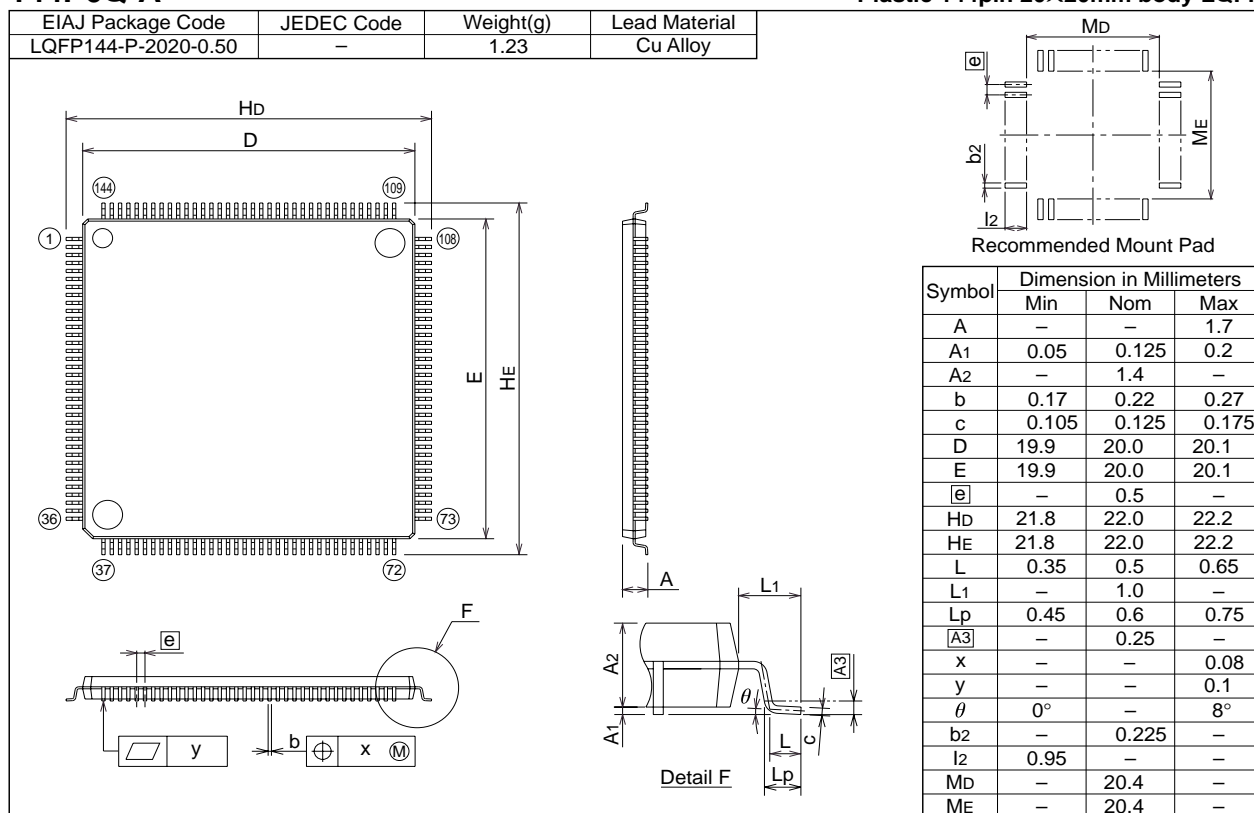


Figure 5.17 $V_{CC}=3.3V$ Timing Diagram (8)

Package Dimensions

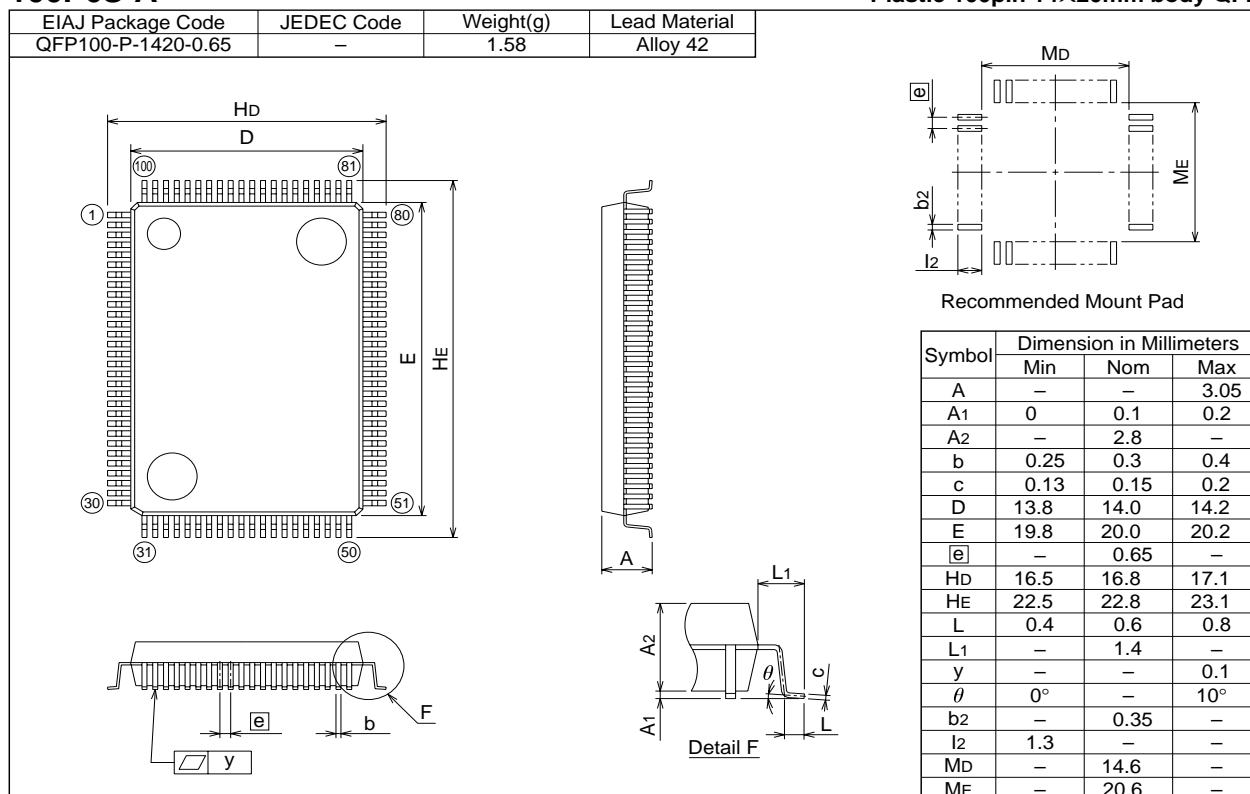
144P6Q-A

Plastic 144pin 20×20mm body LQFP



100P6S-A

Plastic 100pin 14×20mm body QFP

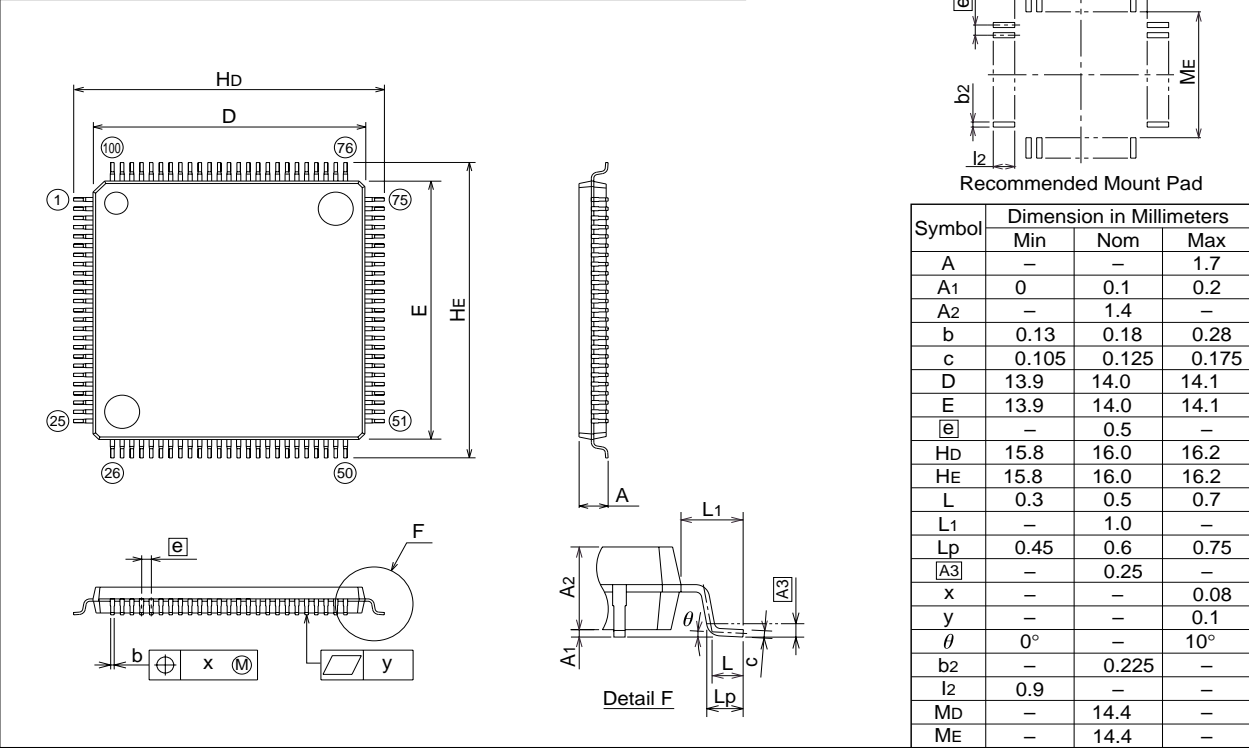


100P6Q-A

(MMP)

Plastic 100pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	—	0.63	Cu Alloy



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