

## 3803 Group (Spec.H) SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0017-0200Z  
Rev.2.00  
2003.05.28

### DESCRIPTION

The 3803 group (Spec. H) is the 8-bit microcomputer based on the 740 family core technology.

The 3803 group (Spec. H) is designed for household products, office automation equipment, and controlling systems that require analog signal processing, including the A-D converter and D-A converters.

### FEATURES

- Basic machine-language instructions ..... 71
- Minimum instruction execution time ..... 0.24  $\mu$ s  
(at 16.8 MHz oscillation frequency)
- Memory size
  - ROM ..... 16 K to 32 K bytes
  - RAM ..... 640 to 1024 bytes
- Programmable input/output ports ..... 56
- Software pull-up resistors ..... Built-in
- Interrupts
  - 21 sources, 16 vectors .....  
(external 8, internal 12, software 1)
- Timers ..... 16-bit  $\times$  1  
8-bit  $\times$  4  
(with 8-bit prescaler)
- Watchdog timer ..... 16-bit  $\times$  1
- Serial I/O ..... 8-bit  $\times$  2 (UART or Clock-synchronized)  
8-bit  $\times$  1 (Clock-synchronized)
- PWM ..... 8-bit  $\times$  1 (with 8-bit prescaler)
- A-D converter ..... 10-bit  $\times$  16 channels  
(8-bit reading enabled)
- D-A converter ..... 8-bit  $\times$  2 channels
- LED direct drive port ..... 8
- Clock generating circuit ..... Built-in 2 circuits  
(connect to external ceramic resonator or quartz-crystal oscillator)

- Power source voltage
  - In high-speed mode
    - At 16.8 MHz oscillation frequency ..... 4.5 to 5.5 V
    - At 12.5 MHz oscillation frequency ..... 4.0 to 5.5 V
    - At 8.4 MHz oscillation frequency) ..... 2.7 to 5.5 V
    - At 4.2 MHz oscillation frequency ..... 2.2 to 5.5 V
    - At 2.1 MHz oscillation frequency) ..... 2.0 to 5.5 V
  - In middle-speed mode
    - At 16.8 MHz oscillation frequency ..... 4.5 to 5.5 V
    - At 12.5 MHz oscillation frequency ..... 2.7 to 5.5 V
    - At 8.4 MHz oscillation frequency) ..... 2.2 to 5.5 V
    - At 6.3 MHz oscillation frequency) ..... 1.8 to 5.5 V
  - In low-speed mode
    - At 32 kHz oscillation frequency ..... 1.8 to 5.5 V
- Power dissipation
  - In high-speed mode ..... 40 mW (typ.)  
(at 16.8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... 45  $\mu$ W (typ.)  
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... -20 to 85°C
- Packages
  - SP ..... 64P4B (64-pin 750 mil SDIP)
  - FP ..... 64P6N-A (64-pin 14  $\times$  14 mm QFP)
  - HP ..... 64P6Q-A (64-pin 10  $\times$  10 mm LQFP)
  - KP ..... 64P6U-A (64-pin 14  $\times$  14 mm LQFP)

Currently support products are listed below.

**Table 1 Support products**

Product name	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38034M4H-XXXSP	16384 (16254)	640	64P4B	Mask ROM version
M38034M4H-XXXFP			64P6N-A	
M38034M4H-XXXHP			64P6Q-A	
M38034M4H-XXXKP			64P6U-A	
M38037M6H-XXXSP	24576 (24446)	1024	64P4B	Mask ROM version
M38037M6H-XXXFP			64P6N-A	
M38037M6H-XXXHP			64P6Q-A	
M38037M6H-XXXKP			64P6U-A	
M38037M8H-XXXSP	32768 (32638)	1024	64P4B	Mask ROM version
M38037M8H-XXXFP			64P6N-A	
M38037M8H-XXXHP			64P6Q-A	
M38037M8H-XXXKP			64P6U-A	

## PIN CONFIGURATION (TOP VIEW)

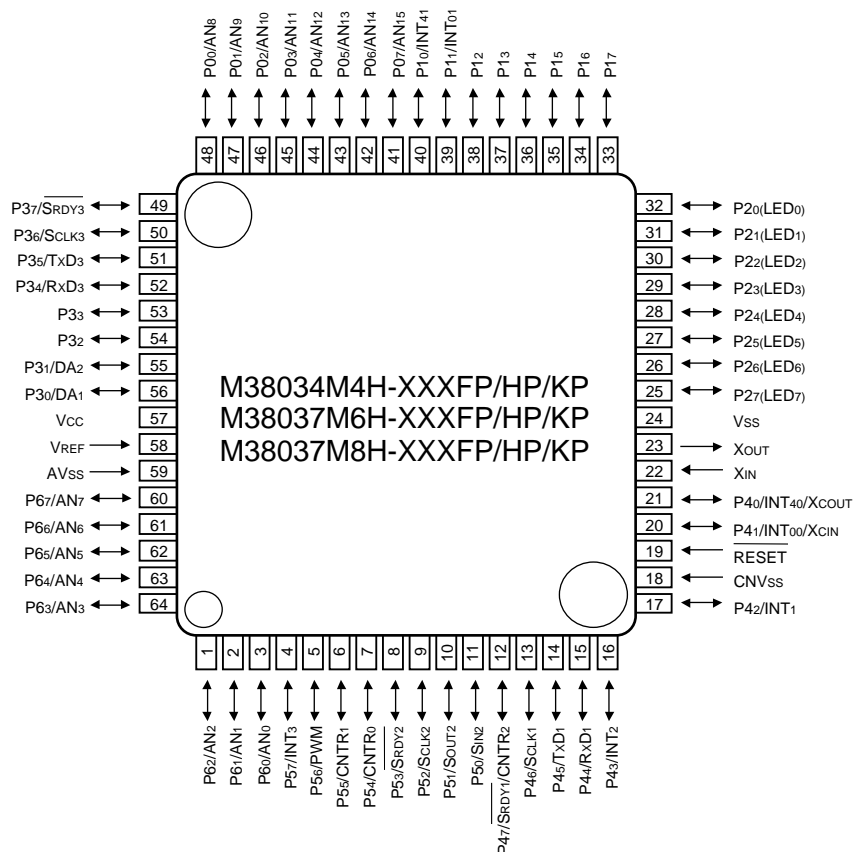
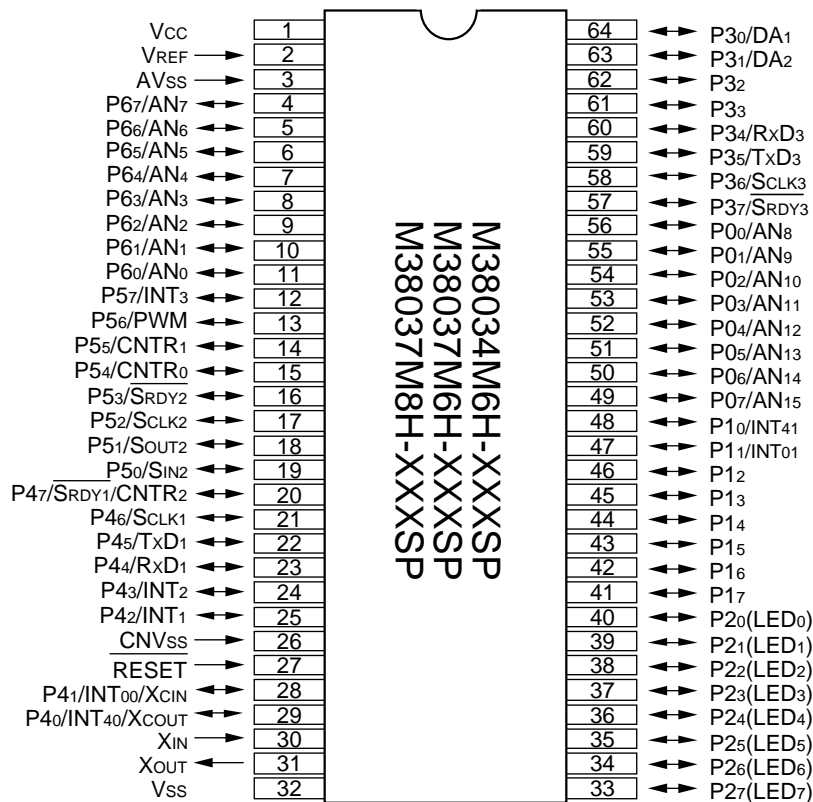


Fig. 1 3803 group (Spec. H) pin configuration

Table 2 List of package (Spec. H)

Package	Product name	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Remarks
64P6N-A	M38034M4H-XXXXFP	16384 (16254)	640	Mask ROM version
	M38037M6H-XXXXFP	24576 (24446)	1024	
	M38037M8H-XXXXFP	32768 (32638)	1024	
64P6Q-A	M38034M4H-XXXXHP	16384 (16254)	640	Mask ROM version
	M38037M6H-XXXXHP	24576 (24446)	1024	
	M38037M8H-XXXXHP	32768 (32638)	1024	
64P6U-A	M38034M4H-XXXXKP	16384 (16254)	640	Mask ROM version
	M38037M6H-XXXXKP	24576 (24446)	1024	
	M38037M8H-XXXXKP	32768 (32638)	1024	

## PIN CONFIGURATION (TOP VIEW)



Package type : 64P4B

Fig. 2 3803 group (Spec. H) pin configuration

Table 3 List of package (Spec. H)

Package	Product name	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Remarks
64P4B	M38034M4H-XXXSP	16384 (16254)	640	Mask ROM version
	M38037M6H-XXXSP	24576 (24446)	1024	
	M38037M8H-XXXSP	32768 (32638)	1024	

## FUNCTIONAL BLOCK

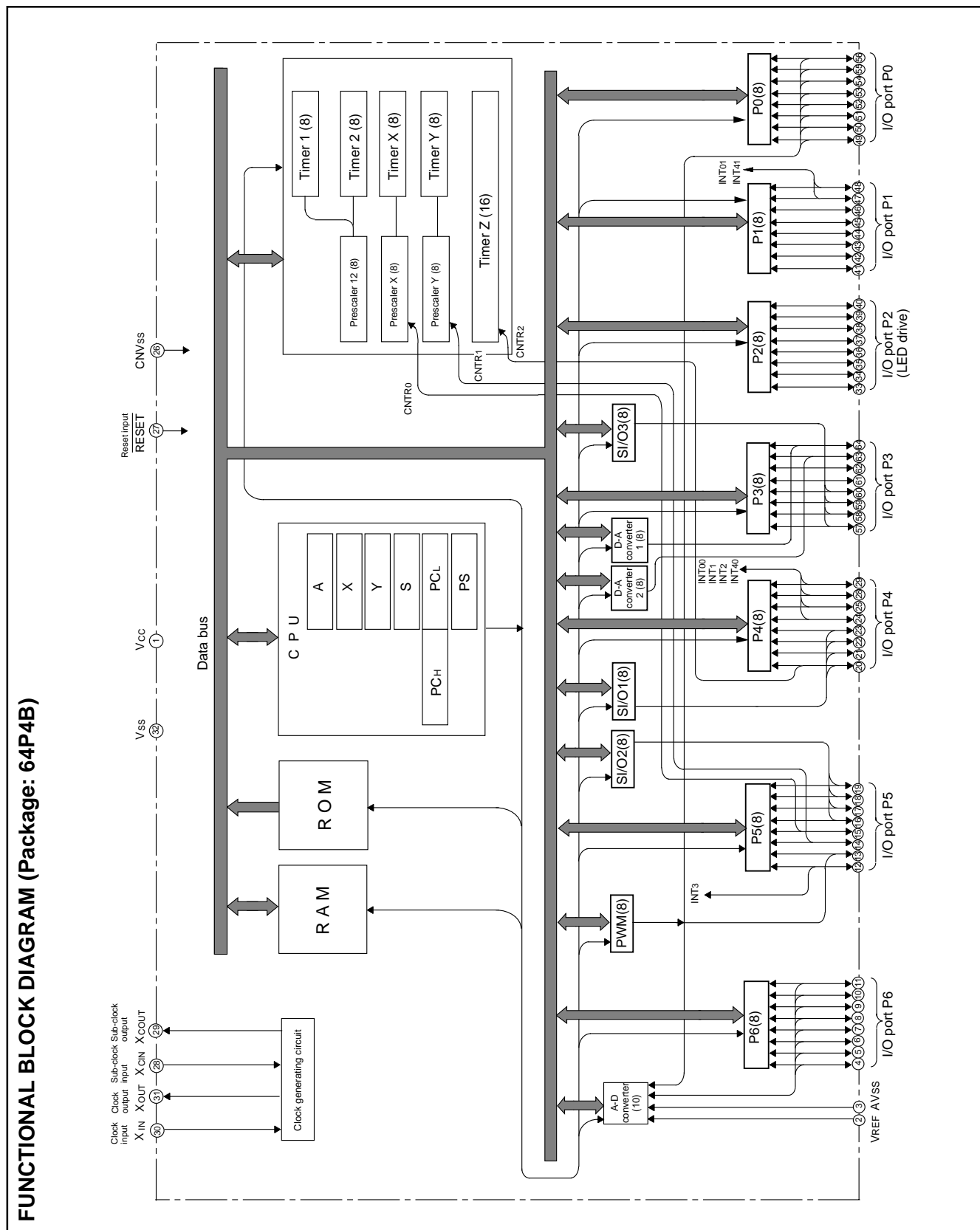


Fig. 3 Functional block diagram

## PIN DESCRIPTION

Table 4 Pin description

Pin	Name	Functions	Function except a port function
VCC, VSS	Power source	•Apply voltage of 1.8 V – 5.5 V to Vcc, and 0 V to Vss.	
CNVSS	CNVss input	•This pin controls the operation mode of the chip. •Normally connected to Vss.	
VREF	Reference voltage	•Reference voltage input pin for A-D and D-A converters.	
AVSS	Analog power source	•Analog power source input pin for A-D and D-A converters. •Connect to Vss.	
RESET	Reset input	•Reset input pin for active “L”.	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.	
XOUT	Clock output	•When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
P00/AN8– P07/AN15	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output.	•A-D converter input pin
P10/INT01 P11/INT41	I/O port P1	•CMOS compatible input level.	•Interrupt input pin
P12–P17		•CMOS 3-state output structure.	
P20–P27	I/O port P2	•Pull-up control is enabled in a bit unit. •P20–P27 are enabled to output large current for LED drive.	
P30/DA1 P31/DA2	I/O port P3	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output.	•D-A converter input pin
P32, P33		•P30, P31, P34–P37 are CMOS 3-state output structure. •P32, P33 are N-channel open-drain output structure.	
P34/RxD3 P35/TxD3 P36/SCLK3 P37/SRDY3		•Pull-up control of P30, P31, P34–P37 is enabled in a bit unit.	•Serial I/O3 function pin
P40/INT40/ XCOUT P41/INT00/ XCIN	I/O port P4	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level.	•Interrupt input pin •Sub-clock generating I/O pin (resonator connected)
P42/INT1 P43/INT2		•CMOS 3-state output structure.	•Interrupt input pin
P44/RxD1 P45/TxD1 P46/SCLK1		•Pull-up control is enabled in a bit unit.	•Serial I/O1 function pin
P47/SRDY1 /CNTR2			•Serial I/O1, timer Z function pin
P50/SIN2 P51/SOUT2 P52/SCLK2 P53/SRDY2	I/O port P5	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level.	•Serial I/O2 function pin
P54/CNTR0		•CMOS 3-state output structure.	•Timer X function pin
P55/CNTR1		•Pull-up control is enabled in a bit unit.	•Timer Y function pin
P56/PWM			•PWM output pin
P57/INT3			•Interrupt input pin
P60/AN0– P67/AN7	I/O port P6		•A-D converter input pin

## PART NUMBERING

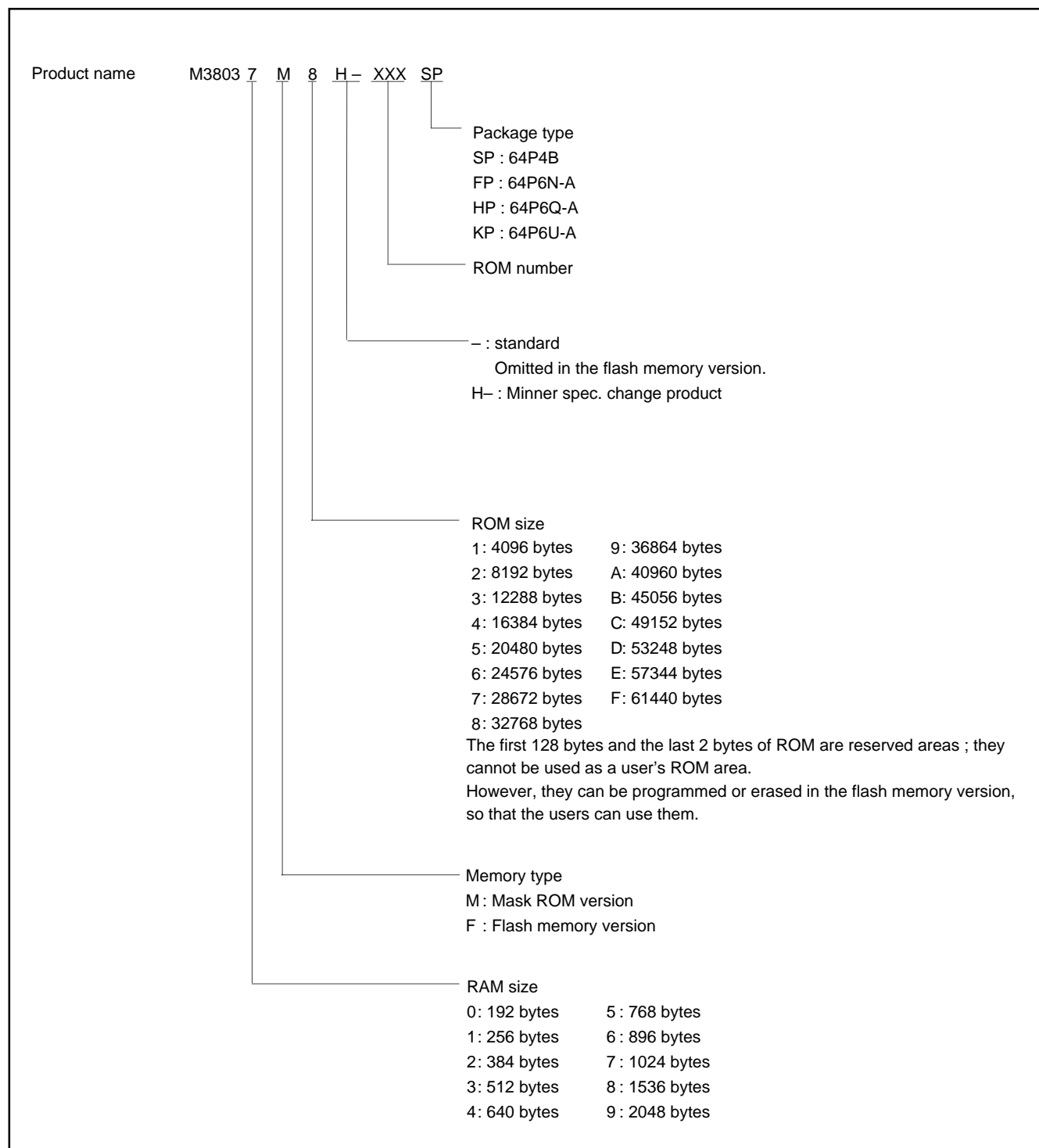


Fig. 4 Part numbering

## GROUP EXPANSION

### GROUP EXPANSION

Mitsubishi plans to expand the 3803 group (Spec. H) as follows.

#### Memory Type

Support for mask ROM version.

#### Memory Size

Mask ROM size ..... 16 K to 32 K bytes

RAM size ..... 640 to 1024 bytes

#### Packages

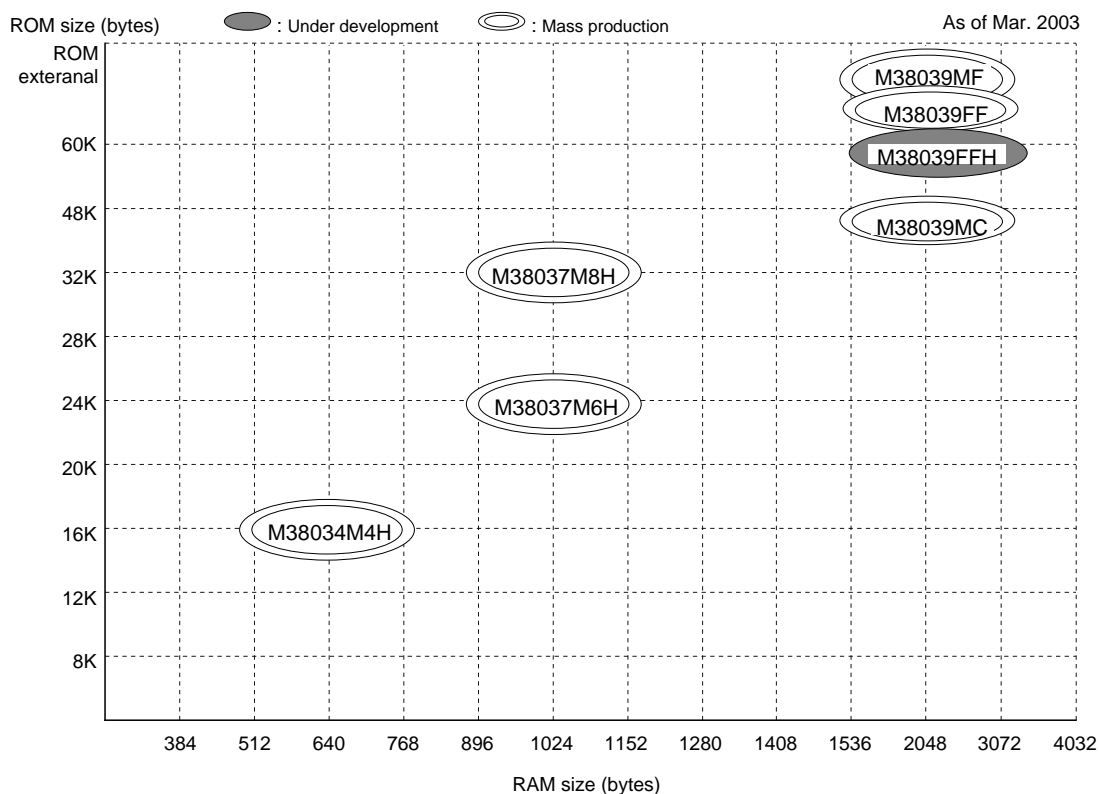
64P4B ..... 64-pin shrink plastic-molded DIP

64P6N-A ..... 0.8 mm-pitch plastic molded QFP

64P6Q-A ..... 0.5 mm-pitch plastic molded LQFP

64P6U-A ..... 0.8 mm-pitch plastic molded LQFP

### Memory Expansion Plan



Note 1: Products under development or planning: the development schedule and specification may be revised without notice. The development of planning products may be stopped.

Note 2: See the 3803/3804 group data sheet about 3803 group products other than 3803 group (spec. H) because there are electrical characteristics differences and so on.

Fig. 5 Memory expansion plan

## FUNCTIONAL DESCRIPTION

### CENTRAL PROCESSING UNIT (CPU)

The 3803 group (Spec. H) uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

### [Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

### [Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

### [Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

### [Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 10.

Store registers other than those described in Figure 10 with program when the user needs them during interrupts or subroutine calls.

### [Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

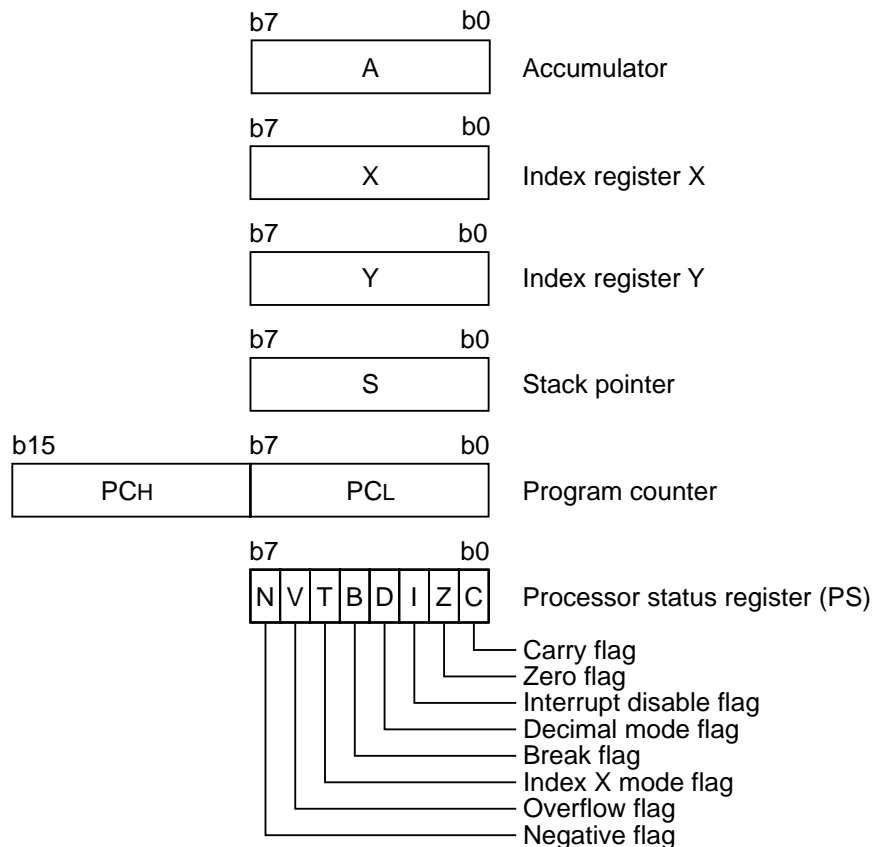


Fig.6 740 Family CPU register structure



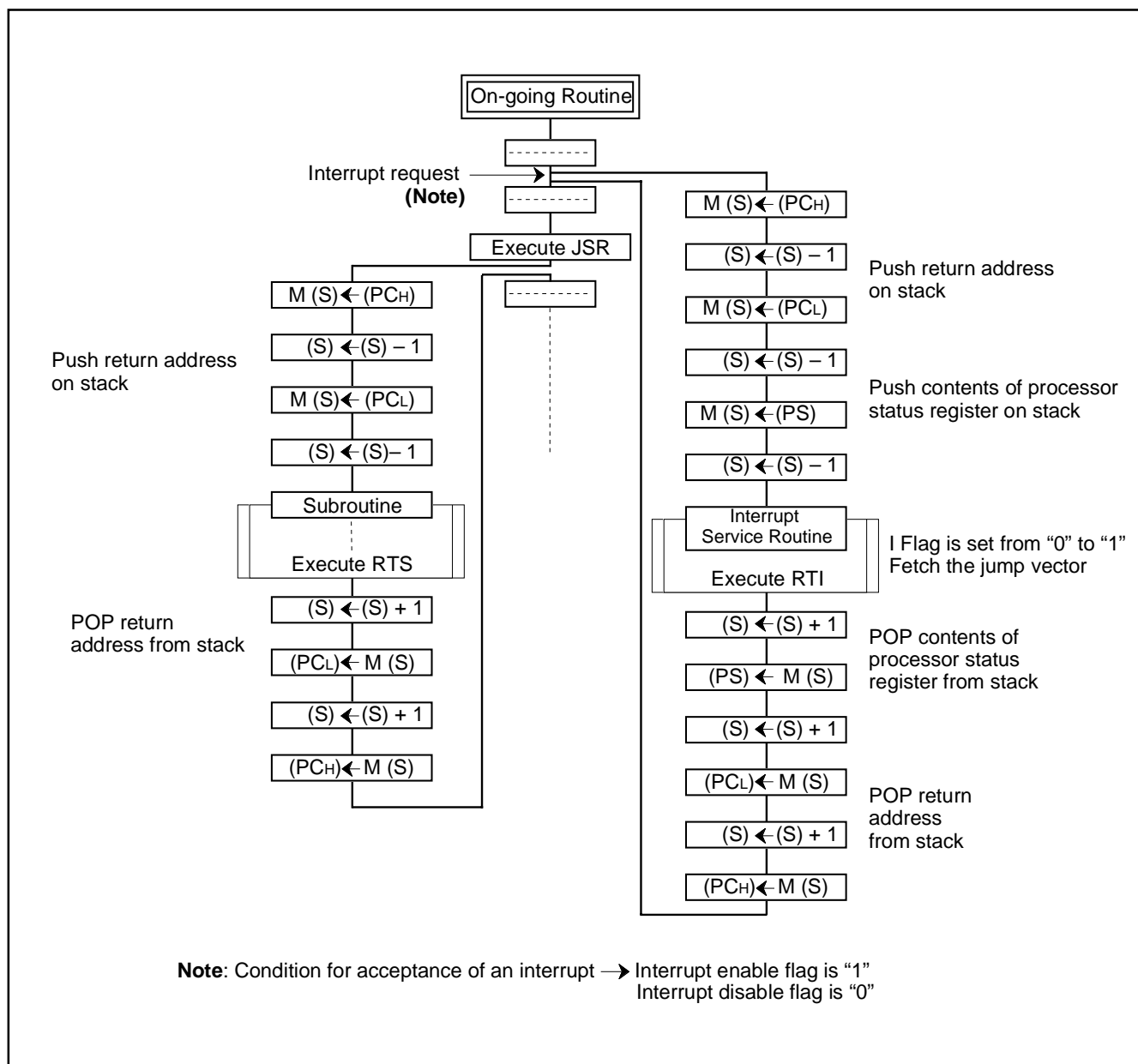


Fig. 7 Register push and pop at interrupt generation and subroutine call

Table 5 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

## [Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can execute decimal arithmetic.

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

•Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

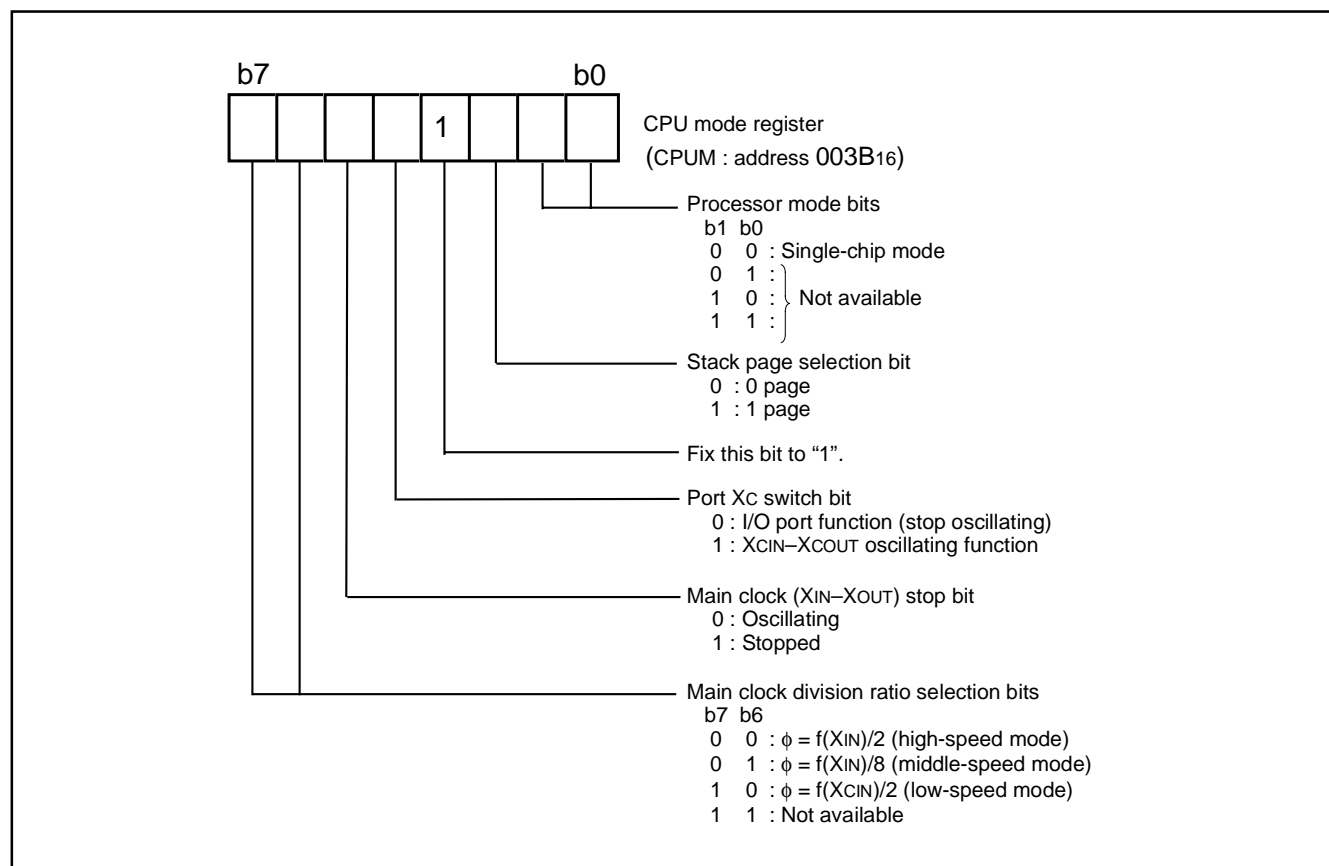
**Table 6 Set and clear instructions of each bit of processor status register**

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

**[CPU Mode Register (CPUM)] 003B16**

The CPU mode register contains the stack page selection bit, etc.

The CPU mode register is allocated at address 003B16.



**Fig.8 Structure of CPU mode register**

## MISRG

### (1) Bit 0 of address 0010<sub>16</sub>: Oscillation stabilizing time set after STP instruction released bit

When the MCU stops the clock oscillation by the STP instruction and the STP instruction has been released by an external interrupt source, usually, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = 01<sub>16</sub>, Prescaler 12 = FF<sub>16</sub>) are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by setting "1" to bit 0 of MISRG (address 0010<sub>16</sub>). However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.

Figure 9 shows the structure of MISRG.

### (2) Bits 1, 2, 3 of address 0010<sub>16</sub>: Middle-speed Mode Automatic Switch Function

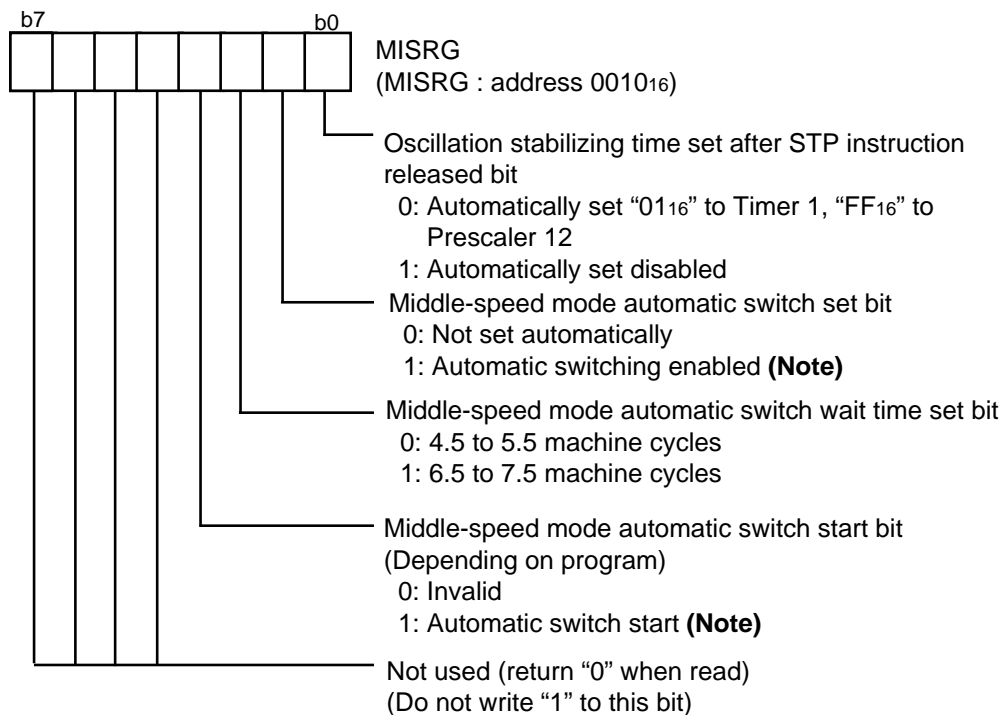
In order to switch the clock mode of an MCU which has a sub-clock, the following procedure is necessary:

set CPU mode register (003B<sub>16</sub>) --> start main clock oscillation --> wait for oscillation stabilization --> switch to middle-speed mode (or high-speed mode).

However, the 3803 group (Spec. H) has the built-in function which automatically switches from low to middle-speed mode by program.

### ●Middle-speed mode automatic switch by program

The middle-speed mode can also be automatically switched by program while operating in low-speed mode. By setting the middle-speed automatic switch start bit (bit 3) of MISRG (address 0010<sub>16</sub>) to "1" in the condition that the middle-speed mode automatic switch set bit is "1" while operating in low-speed mode, the MCU will automatically switch to middle-speed mode. In this case, the oscillation stabilizing time of the main clock can be selected by the middle-speed automatic switch wait time set bit (bit 2) of MISRG (address 0010<sub>16</sub>).



**Note:** When automatic switch to middle-speed mode from low-speed mode occurs, the values of CPU mode register (3B<sub>16</sub>) change.

Fig. 9 Structure of MISRG

## MEMORY

### Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

### RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

### ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

### Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

### Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

### Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

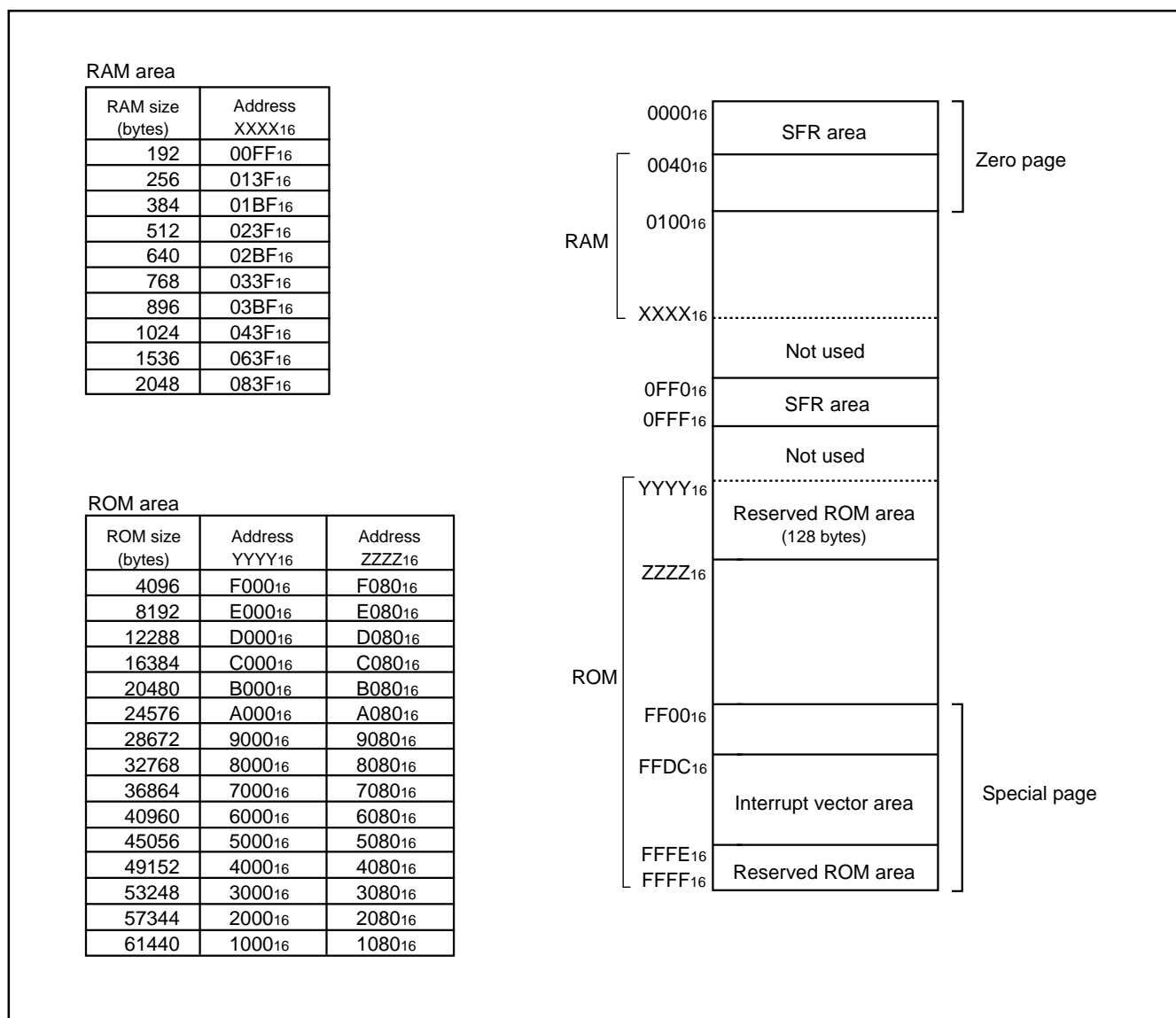


Fig. 10 Memory map diagram

0000 <sub>16</sub>	Port P0 (P0)	0020 <sub>16</sub>	Prescaler 12 (PRE12)
0001 <sub>16</sub>	Port P0 direction register (P0D)	0021 <sub>16</sub>	Timer 1 (T1)
0002 <sub>16</sub>	Port P1 (P1)	0022 <sub>16</sub>	Timer 2 (T2)
0003 <sub>16</sub>	Port P1 direction register (P1D)	0023 <sub>16</sub>	Timer XY mode register (TM)
0004 <sub>16</sub>	Port P2 (P2)	0024 <sub>16</sub>	Prescaler X (PREX)
0005 <sub>16</sub>	Port P2 direction register (P2D)	0025 <sub>16</sub>	Timer X (TX)
0006 <sub>16</sub>	Port P3 (P3)	0026 <sub>16</sub>	Prescaler Y (PREY)
0007 <sub>16</sub>	Port P3 direction register (P3D)	0027 <sub>16</sub>	Timer Y (TY)
0008 <sub>16</sub>	Port P4 (P4)	0028 <sub>16</sub>	Timer Z low-order (TZL)
0009 <sub>16</sub>	Port P4 direction register (P4D)	0029 <sub>16</sub>	Timer Z high-order (TZH)
000A <sub>16</sub>	Port P5 (P5)	002A <sub>16</sub>	Timer Z mode register (TzM)
000B <sub>16</sub>	Port P5 direction register (P5D)	002B <sub>16</sub>	PWM control register (PWMCON)
000C <sub>16</sub>	Port P6 (P6)	002C <sub>16</sub>	PWM prescaler (PREPWM)
000D <sub>16</sub>	Port P6 direction register (P6D)	002D <sub>16</sub>	PWM register (PWM)
000E <sub>16</sub>	Timer 12, X count source selection register (T12XCSS)	002E <sub>16</sub>	
000F <sub>16</sub>	Timer Y, Z count source selection register (TYZCSS)	002F <sub>16</sub>	Baud rate generator 3 (BRG3)
0010 <sub>16</sub>	MISRG	0030 <sub>16</sub>	Transmit/Receive buffer register 3 (TB3/RB3)
0011 <sub>16</sub>	Reserved *	0031 <sub>16</sub>	Serial I/O3 status register (SIO3STS)
0012 <sub>16</sub>	Reserved *	0032 <sub>16</sub>	Serial I/O3 control register (SIO3CON)
0013 <sub>16</sub>	Reserved *	0033 <sub>16</sub>	UART3 control register (UART3CON)
0014 <sub>16</sub>	Reserved *	0034 <sub>16</sub>	AD/DA control register (ADCON)
0015 <sub>16</sub>	Reserved *	0035 <sub>16</sub>	A-D conversion register 1 (AD1)
0016 <sub>16</sub>	Reserved *	0036 <sub>16</sub>	D-A1 conversion register (DA1)
0017 <sub>16</sub>	Reserved *	0037 <sub>16</sub>	D-A2 conversion register (DA2)
0018 <sub>16</sub>	Transmit/Receive buffer register 1 (TB1/RB1)	0038 <sub>16</sub>	A-D conversion register 2 (AD2)
0019 <sub>16</sub>	Serial I/O1 status register (SIO1STS)	0039 <sub>16</sub>	Interrupt source selection register (INTSEL)
001A <sub>16</sub>	Serial I/O1 control register (SIO1CON)	003A <sub>16</sub>	Interrupt edge selection register (INTEDGE)
001B <sub>16</sub>	UART1 control register (UART1CON)	003B <sub>16</sub>	CPU mode register (CPUM)
001C <sub>16</sub>	Baud rate generator (BRG1)	003C <sub>16</sub>	Interrupt request register 1 (IREQ1)
001D <sub>16</sub>	Serial I/O2 control register (SIO2CON)	003D <sub>16</sub>	Interrupt request register 2 (IREQ2)
001E <sub>16</sub>	Watchdog timer control register (WDTCON)	003E <sub>16</sub>	Interrupt control register 1 (ICON1)
001F <sub>16</sub>	Serial I/O2 register (SIO2)	003F <sub>16</sub>	Interrupt control register 2 (ICON2)
		0FF0 <sub>16</sub>	Port P0 pull-up control register (PULL0)
		0FF1 <sub>16</sub>	Port P1 pull-up control register (PULL1)
		0FF2 <sub>16</sub>	Port P2 pull-up control register (PULL2)
		0FF3 <sub>16</sub>	Port P3 pull-up control register (PULL3)
		0FF4 <sub>16</sub>	Port P4 pull-up control register (PULL4)
		0FF5 <sub>16</sub>	Port P5 pull-up control register (PULL5)
		0FF6 <sub>16</sub>	Port P6 pull-up control register (PULL6)

\* Reserved area: Do not write any data to these addresses, because these areas are reserved.

Fig. 11 Memory map of special function register (SFR)

## I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin be-

comes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

**Table 7 I/O port function**

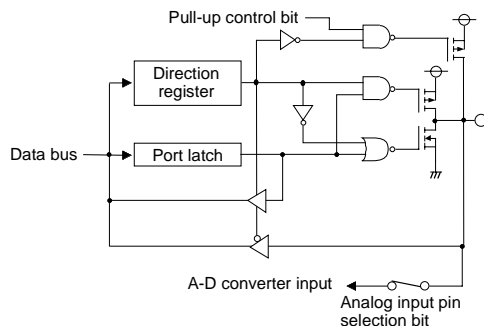
Pin	Name	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P00/AN8–P07/AN15	Port P0	CMOS compatible input level	A-D converter input	AD/DA control register	(1)
P10/INT41 P11/INT01	Port P1	CMOS 3-state output	External interrupt input	Interrupt edge selection register	(2)
P12–P17					(3)
P20/LED0– P27/LED7	Port P2				
P30/DA1 P31/DA2	Port P3	CMOS compatible input level CMOS 3-state output	D-A converter output	AD/DA control register	(4)
P32 P33		CMOS compatible input level N-channel open-drain output			(5)
P34/RxD3 P35/TxD3 P36/SCLK3 P37/SRDY3		CMOS compatible input level CMOS 3-state output	Serial I/O3 function I/O	Serial I/O3 control register UART3 control register	(6) (7) (8) (9)
P40/INT00/XCIN P41/INT40/XCOUT	Port P4	CMOS compatible input level CMOS 3-state output	External interrupt input Sub-clock generating circuit	Interrupt edge selection register CPU mode register	(10) (11)
P42/INT1 P43/INT2			External interrupt input	Interrupt edge selection register	(2)
P44/RxD1 P45/TxD1 P46/SCLK1			Serial I/O1 function I/O	Serial I/O1 control register UART1 control register	(6) (7) (8)
P47/SRDY1/CNTR2			Serial I/O1 function I/O Timer Z function I/O	Serial I/O1 control register Timer Z mode register	(12)
P50/SIN2 P51/SOUT2 P52/SCLK2 P53/SRDY2	Port P5	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(13) (14) (15) (16)
P54/CNTR0 P55/CNTR1			Timer X, Y function I/O	Timer XY mode register	(17)
P56/PWM			PWM output	PWM control register	(18)
P57/INT3			External interrupt input	Interrupt edge selection register	(2)
P60/AN0–P67/AN7	Port P6	CMOS compatible input level CMOS 3-state output	A-D converter input	AD/DA control register	(1)

**Notes 1:** Refer to the applicable sections how to use double-function ports as function I/O ports.

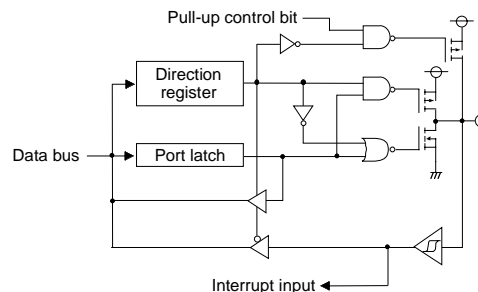
**2:** Make sure that the input level at each pin is either 0 V or V<sub>CC</sub> during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from V<sub>CC</sub> to V<sub>SS</sub> through the input-stage gate.

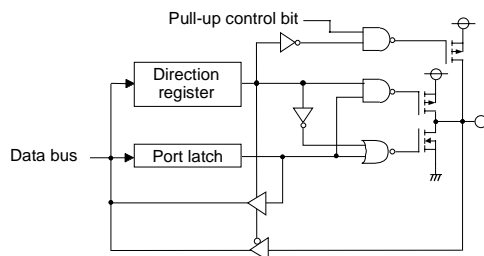
(1) Ports P0, P6



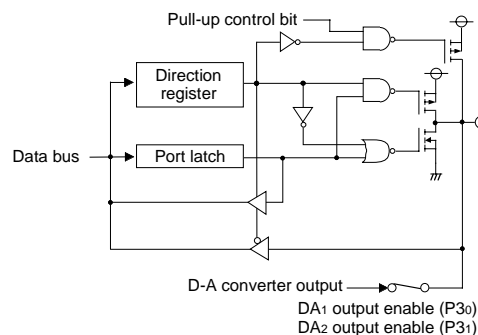
(2) Ports P10, P11, P42, P43, P57



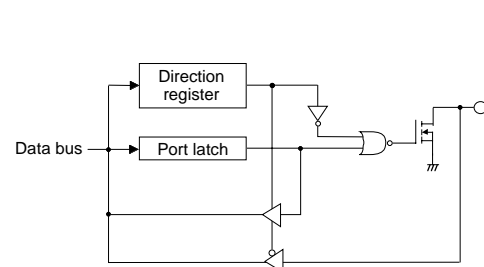
(3) Ports P12 to P17, P2



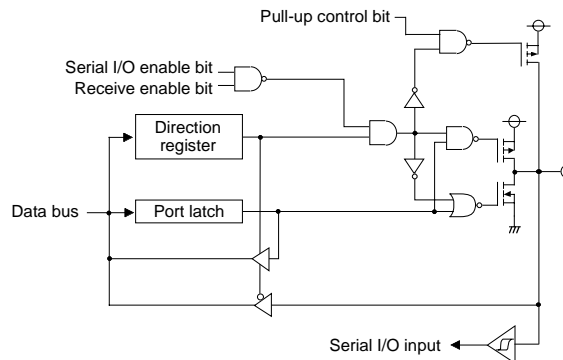
(4) Ports P30, P31



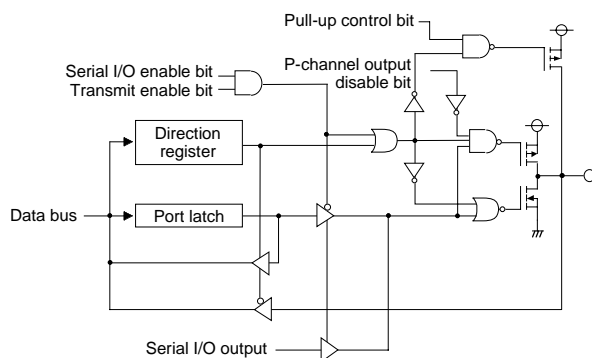
(5) Ports P32, P33



(6) Ports P34, P44



(7) Ports P35, P45



(8) Ports P36, P46

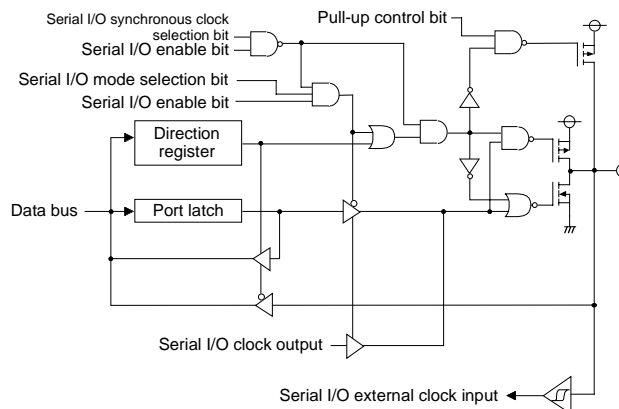
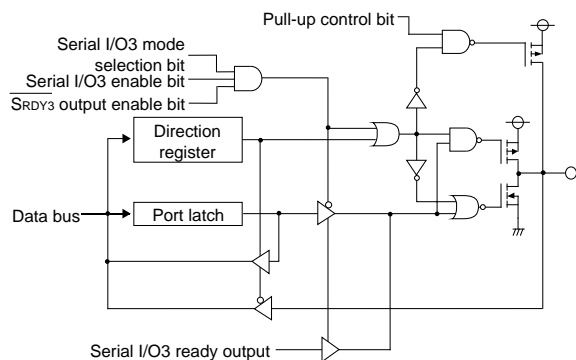


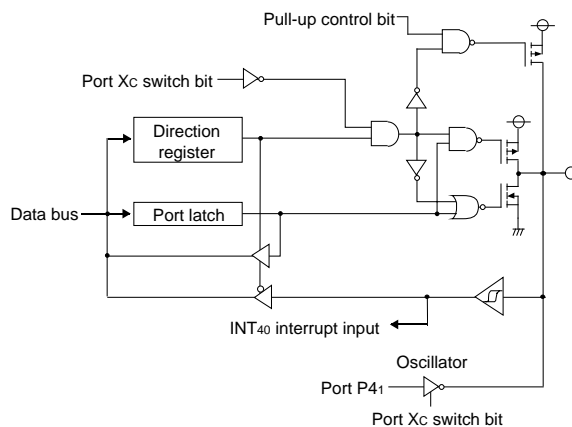
Fig. 12 Port block diagram (1)



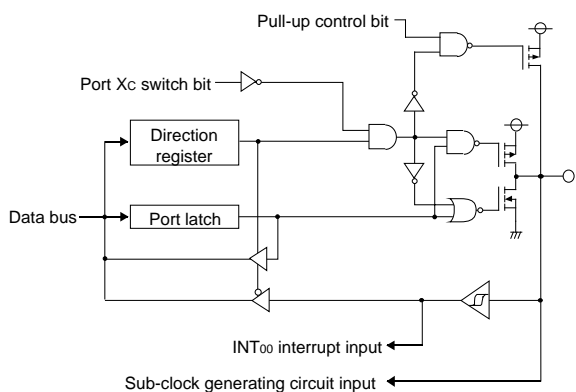
(9) Port P37



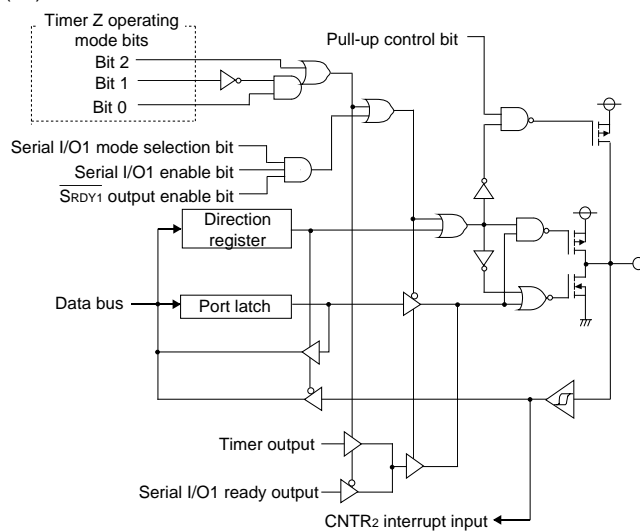
(10) Port P40



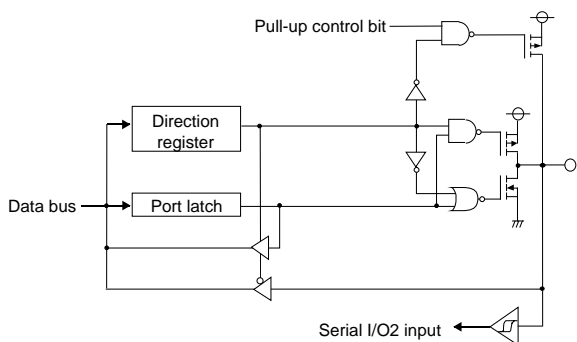
(11) Port P41



(12) Port P47



(13) Port P50



(14) Port P51

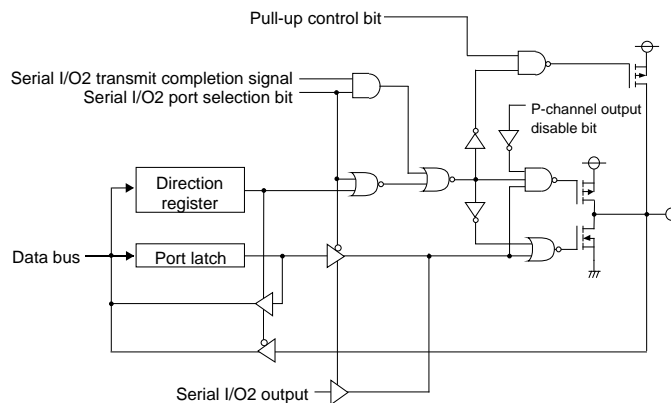
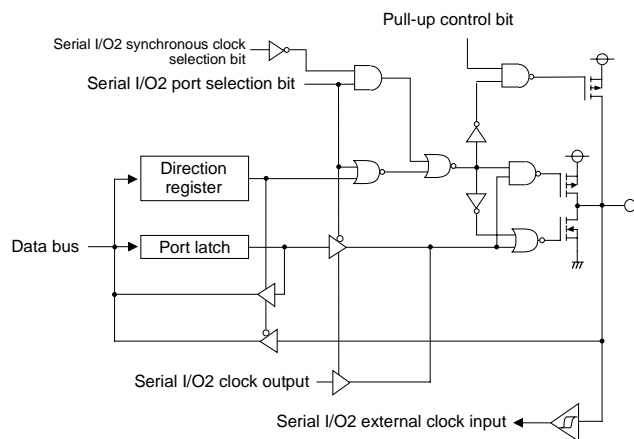
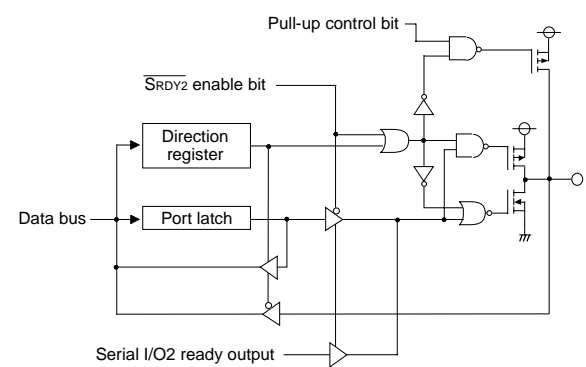


Fig. 13 Port block diagram (2)

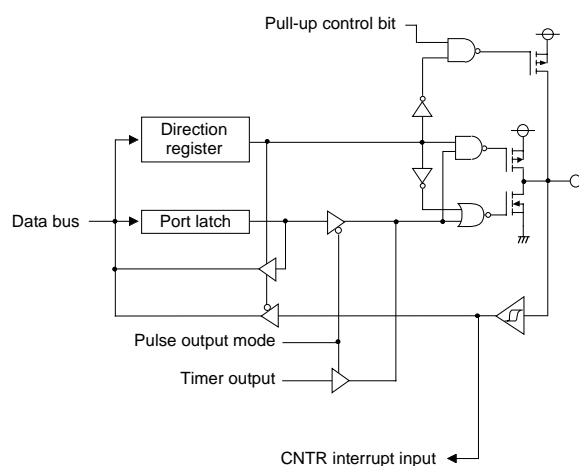
(15) Port P52



(16) Port P53



(17) Ports P54, P55



(18) Port P56

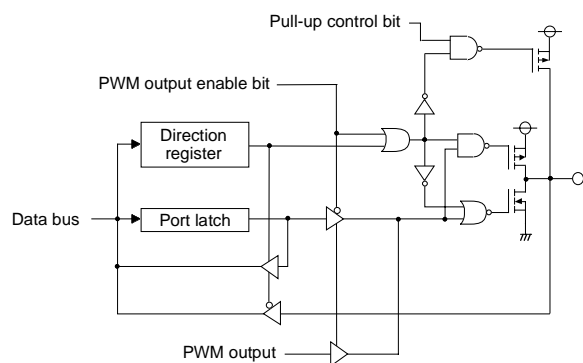


Fig. 14 Port block diagram (3)

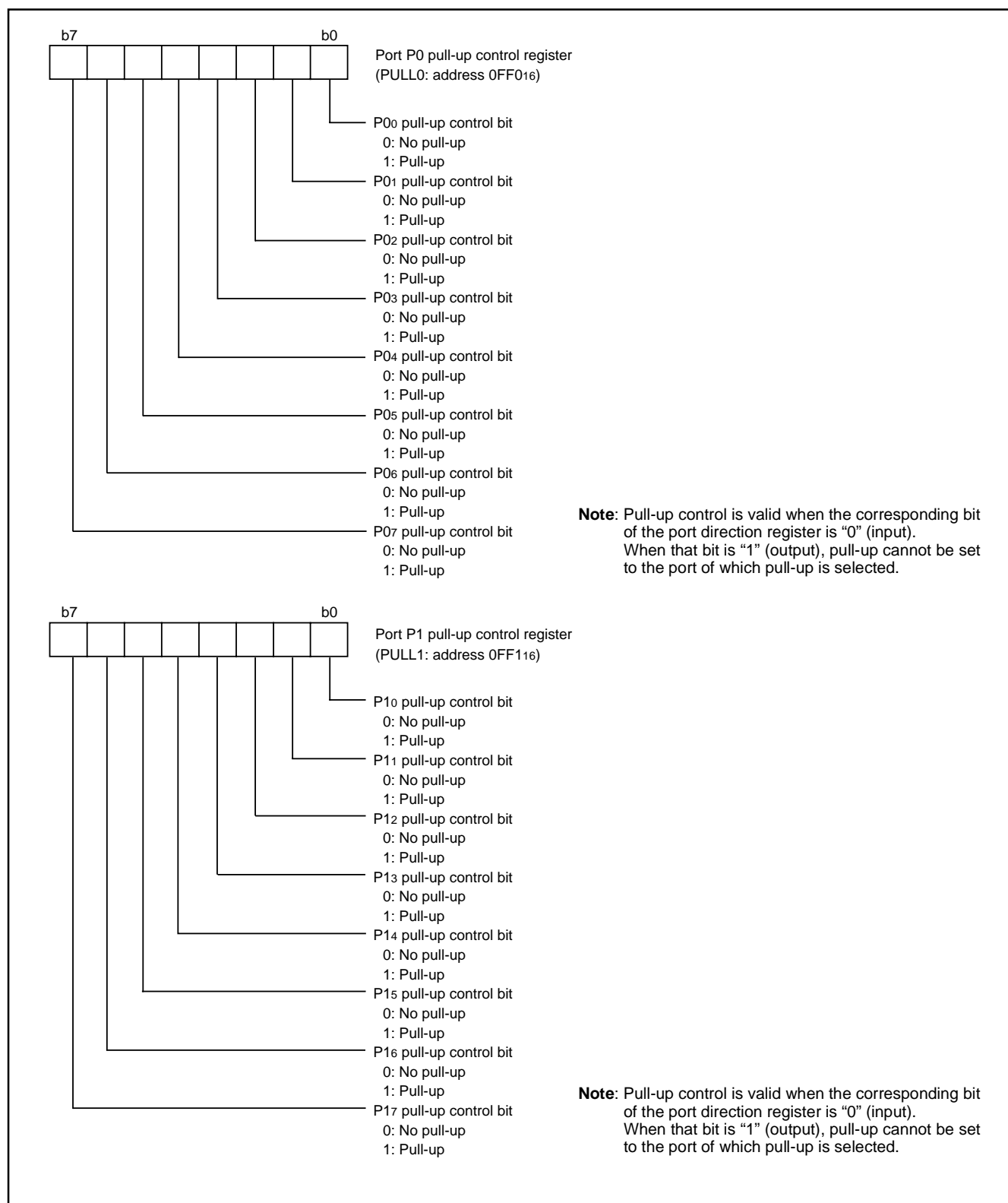


Fig. 15 Structure of port pull-up control register (1)

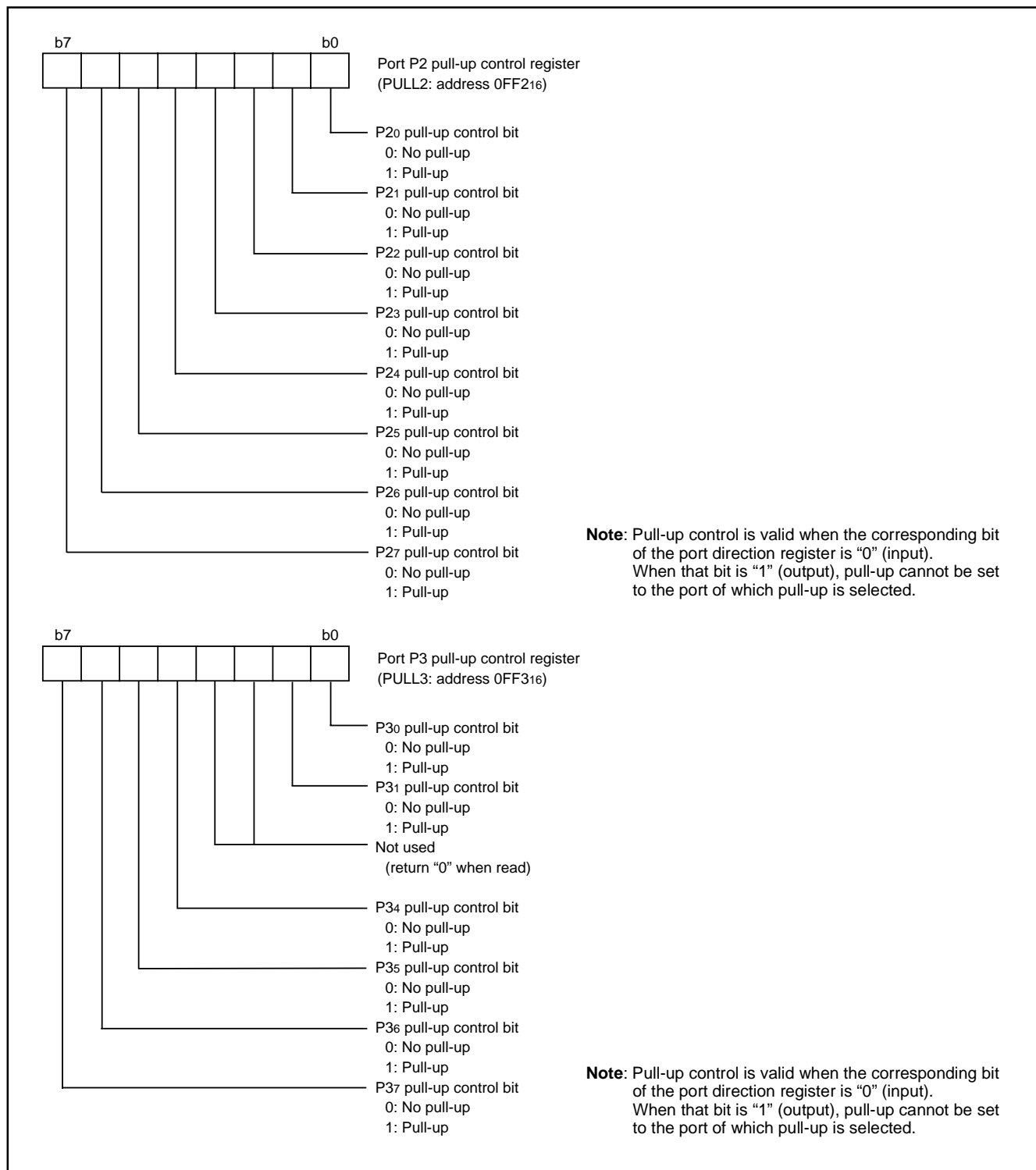


Fig. 16 Structure of port pull-up control register (2)

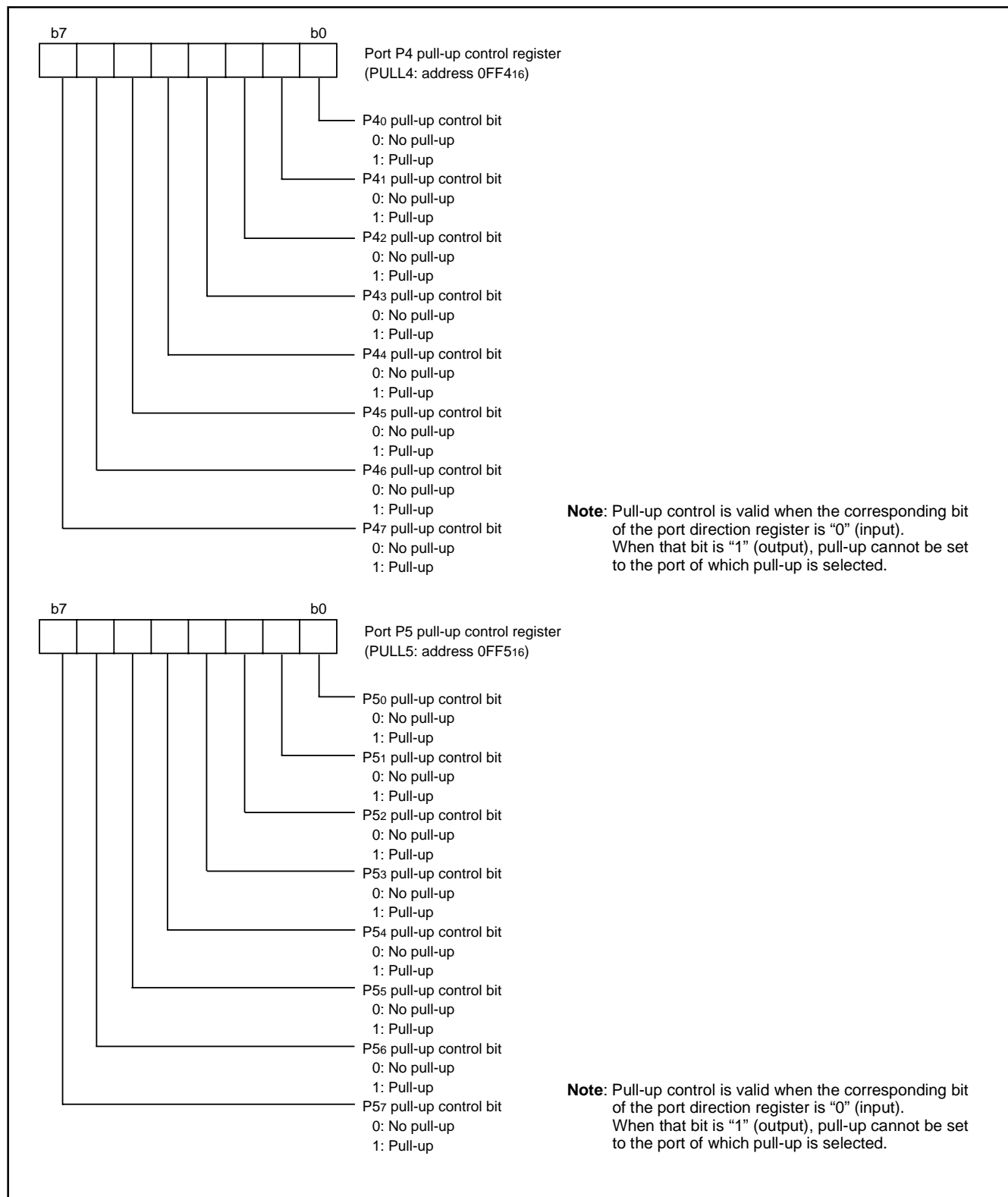


Fig. 17 Structure of port pull-up control register (3)

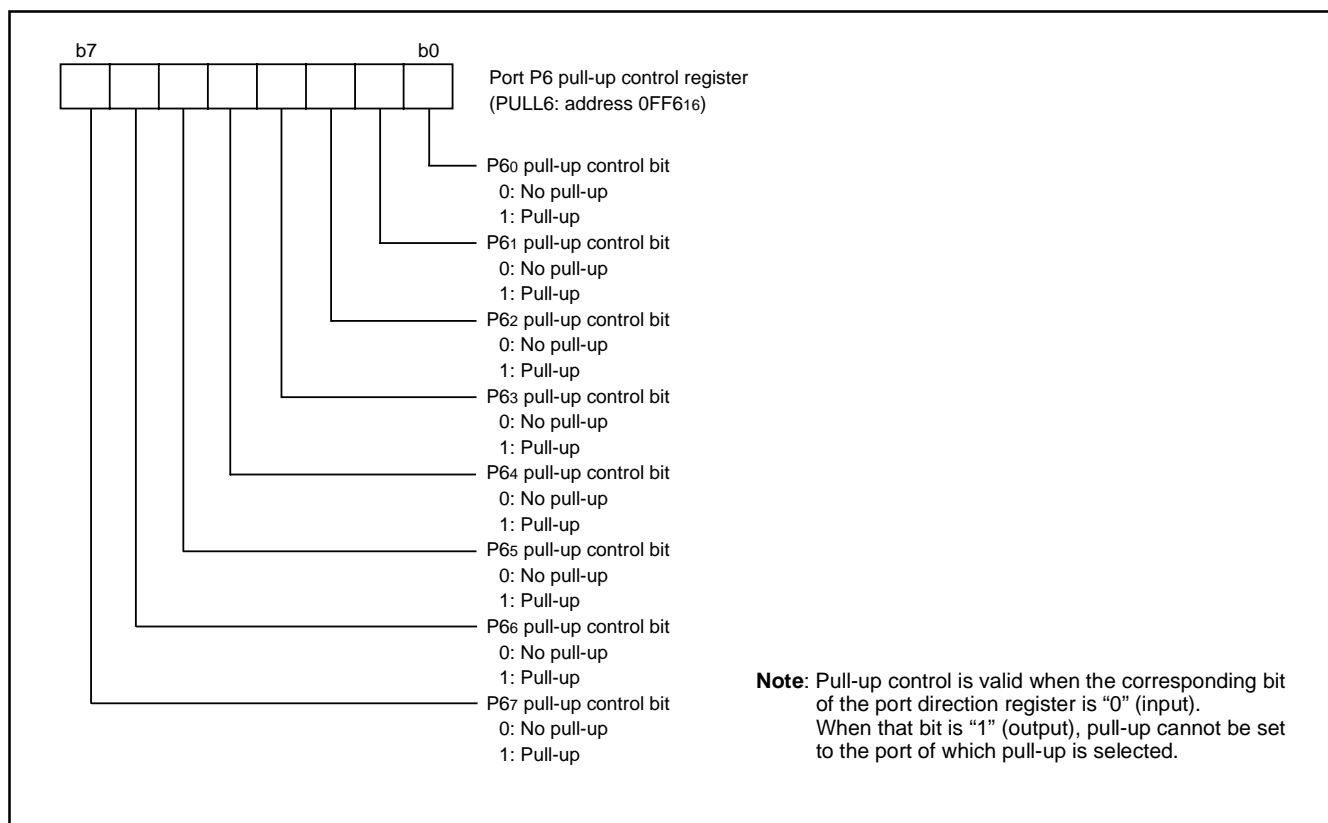


Fig. 18 Structure of port pull-up control register (4)

## INTERRUPTS

The 3803 group (Spec. H)'s interrupts are a type of vector and occur by 16 sources among 21 sources: eight external, twelve internal, and one software.

### Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The reset and the BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the reset and the BRK instruction interrupt.

When several interrupt requests occur at the same time, the interrupts are received according to priority.

### Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

### Interrupt Source Selection

Which of each combination of the following interrupt sources can be selected by the interrupt source selection register (address 003916).

1. INT0 or Timer Z
2. CNTR1 or Serial I/O3 reception
3. Serial I/O2 or Timer Z
7. INT4 or CNTR2
8. A-D converter or serial I/O3 transmission

### External Interrupt Pin Selection

The occurrence sources of the external interrupt INT0 and INT4 can be selected from either input from INT00 and INT40 pin, or input from INT01 and INT41 pin by the INT0, INT4 interrupt switch bit of interrupt edge selection register (bit 6 of address 003A16).

## ■ Notes

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge

Related register: Interrupt edge selection register (address 003A16)

Timer XY mode register (address 002316)

Timer Z mode register (address 002A16)

- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

Related register: Interrupt source selection register

(address 003916)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

- ①Set the corresponding interrupt enable bit to "0" (disabled).
- ②Set the interrupt edge select bit or the interrupt source select bit to "1".
- ③Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④Set the corresponding interrupt enable bit to "1" (enabled).

**Table 8 Interrupt vector addresses and priority**

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD <sub>16</sub>	FFFC <sub>16</sub>	At reset	Non-maskable
INT <sub>0</sub>	2	FFFB <sub>16</sub>	FFFA <sub>16</sub>	At detection of either rising or falling edge of INT <sub>0</sub> input	External interrupt (active edge selectable)
Timer Z				At timer Z underflow	
INT <sub>1</sub>	3	FFF9 <sub>16</sub>	FFF8 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>1</sub> input	External interrupt (active edge selectable)
Serial I/O <sub>1</sub> reception	4	FFF7 <sub>16</sub>	FFF6 <sub>16</sub>	At completion of serial I/O <sub>1</sub> data reception	Valid when serial I/O <sub>1</sub> is selected
Serial I/O <sub>1</sub> transmission	5	FFF5 <sub>16</sub>	FFF4 <sub>16</sub>	At completion of serial I/O <sub>1</sub> transmission shift or when transmission buffer is empty	Valid when serial I/O <sub>1</sub> is selected
Timer X	6	FFF3 <sub>16</sub>	FFF2 <sub>16</sub>	At timer X underflow	
Timer Y	7	FFF1 <sub>16</sub>	FFF0 <sub>16</sub>	At timer Y underflow	
Timer 1	8	FFEF <sub>16</sub>	FFEE <sub>16</sub>	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED <sub>16</sub>	FFEC <sub>16</sub>	At timer 2 underflow	
CNTR <sub>0</sub>	10	FFEB <sub>16</sub>	FFEA <sub>16</sub>	At detection of either rising or falling edge of CNTR <sub>0</sub> input	External interrupt (active edge selectable)
CNTR <sub>1</sub>	11	FFE9 <sub>16</sub>	FFE8 <sub>16</sub>	At detection of either rising or falling edge of CNTR <sub>1</sub> input	External interrupt (active edge selectable)
Serial I/O <sub>3</sub> reception				At completion of serial I/O <sub>3</sub> data reception	Valid when serial I/O <sub>3</sub> is selected
Serial I/O <sub>2</sub>	12	FFE7 <sub>16</sub>	FFE6 <sub>16</sub>	At completion of serial I/O <sub>2</sub> data transmission or reception	Valid when serial I/O <sub>2</sub> is selected
Timer Z				At timer Z underflow	
INT <sub>2</sub>	13	FFE5 <sub>16</sub>	FFE4 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>2</sub> input	External interrupt (active edge selectable)
INT <sub>3</sub>	14	FFE3 <sub>16</sub>	FFE2 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>3</sub> input	External interrupt (active edge selectable)
INT <sub>4</sub>	15	FFE1 <sub>16</sub>	FFE0 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>4</sub> input	External interrupt (active edge selectable)
CNTR <sub>2</sub>				At detection of either rising or falling edge of CNTR <sub>2</sub> input	External interrupt (active edge selectable)
A-D converter	16	FFDF <sub>16</sub>	FFDE <sub>16</sub>	At completion of A-D conversion	
Serial I/O <sub>3</sub> transmission				At completion of serial I/O <sub>3</sub> transmission shift or when transmission buffer is empty	Valid when serial I/O <sub>3</sub> is selected
BRK instruction	17	FFDD <sub>16</sub>	FFDC <sub>16</sub>	At BRK instruction execution	Non-maskable software interrupt

**Notes 1:** Vector addresses contain interrupt jump destination addresses.

**2:** Reset function in the same way as an interrupt with the highest priority.



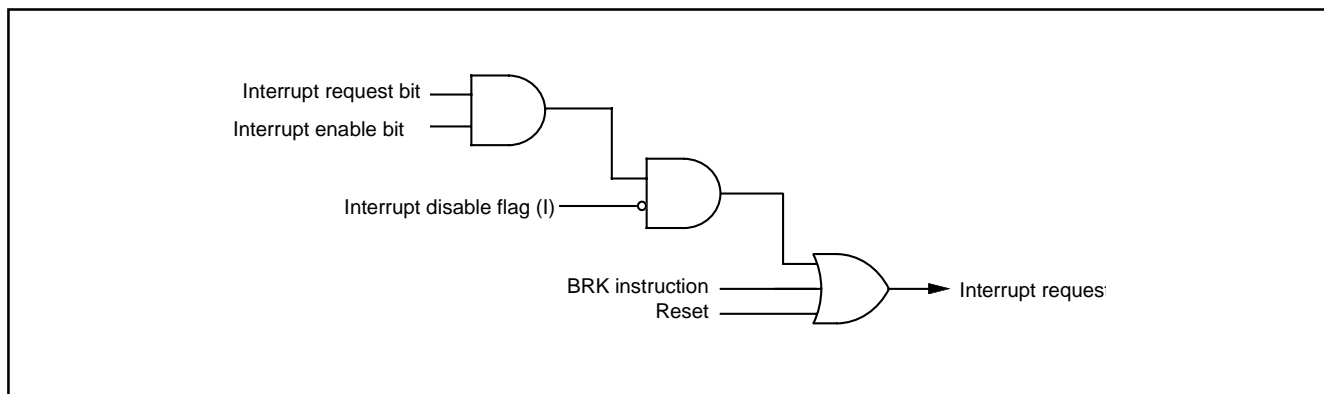


Fig. 19 Interrupt control

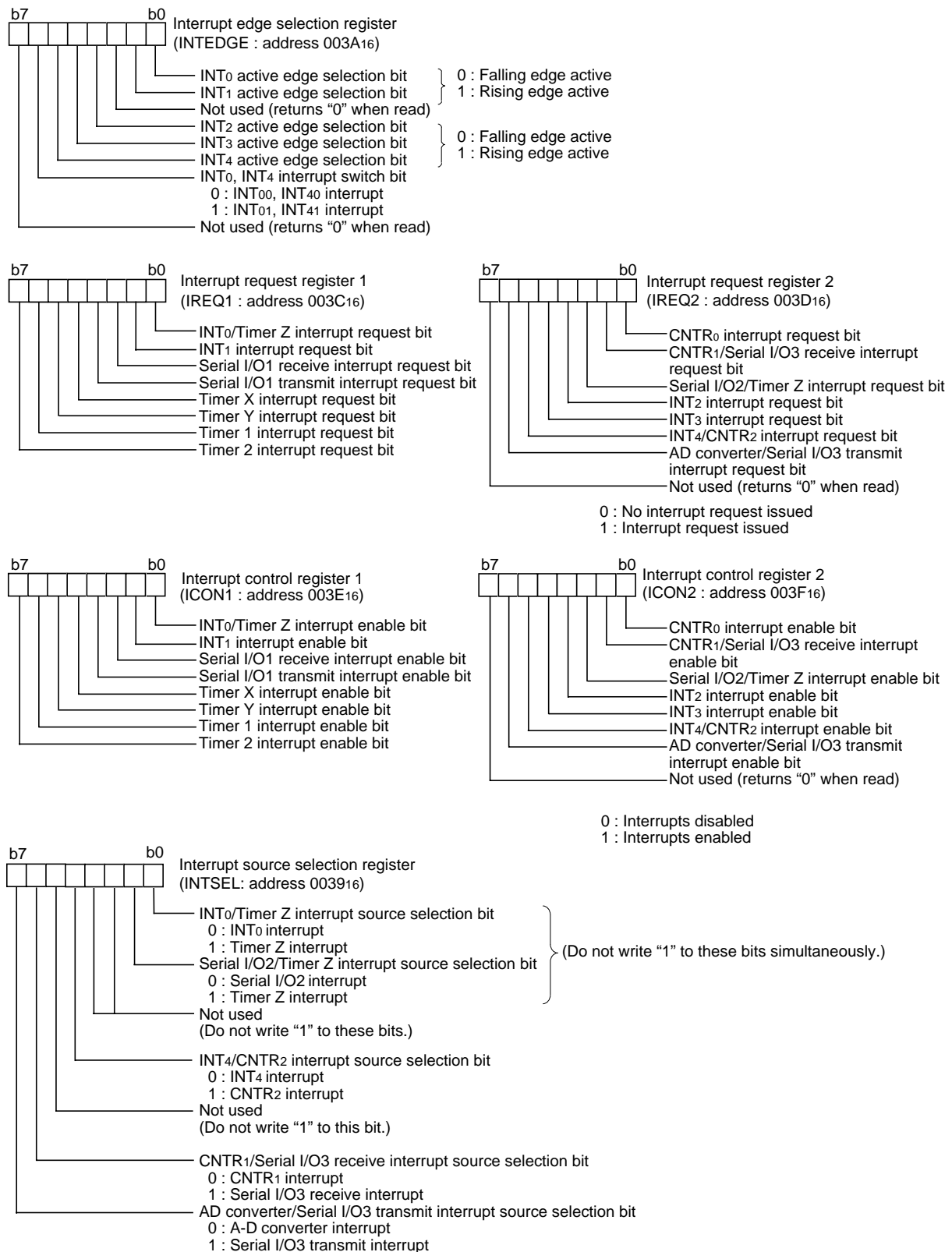


Fig. 20 Structure of interrupt-related registers

## TIMERS

### ●8-bit Timers

The 3803 group (Spec. H) has four 8-bit timers: timer 1, timer 2, timer X, and timer Y.

The timer 1 and timer 2 use one prescaler in common, and the timer X and timer Y use each prescaler. Those are 8-bit prescalers. Each of the timers and prescalers has a timer latch or a prescaler latch.

The division ratio of each timer or prescaler is given by  $1/(n + 1)$ , where  $n$  is the value in the corresponding timer or prescaler latch. All timers are down-counters. When the timer reaches "00<sub>16</sub>", an underflow occurs at the next count pulse and the contents of the corresponding timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

### ●Timer divider

The divider count source is switched by the main clock division ratio selection bits of CPU mode register (bits 7 and 6 at address 003B<sub>16</sub>). When these bits are "00" (high-speed mode) or "01" (middle-speed mode), X<sub>IN</sub> is selected. When these bits are "10" (low-speed mode), X<sub>CIN</sub> is selected.

### ●Prescaler 12

The prescaler 12 counts the output of the timer divider. The count source is selected by the timer 12, X count source selection register among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024 of  $f(X_{IN})$  or  $f(X_{CIN})$ .

## Timer 1 and Timer 2

The timer 1 and timer 2 counts the output of prescaler 12 and periodically set the interrupt request bit.

### ●Prescaler X and prescaler Y

The prescaler X and prescaler Y count the output of the timer divider or  $f(X_{CIN})$ . The count source is selected by the timer 12, X count source selection register (address 000E<sub>16</sub>) and the timer Y, Z count source selection register (address 000F<sub>16</sub>) among 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, and 1/1024 of  $f(X_{IN})$  or  $f(X_{CIN})$ ; and  $f(X_{CIN})$ .

## Timer X and Timer Y

The timer X and timer Y can each select one of four operating modes by setting the timer XY mode register (address 0023<sub>16</sub>).

### (1) Timer mode

#### ●Mode selection

This mode can be selected by setting "00" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023<sub>16</sub>).

#### ●Explanation of operation

The timer count operation is started by setting "0" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023<sub>16</sub>).

When the timer reaches "00<sub>16</sub>", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

### (2) Pulse output mode

#### ●Mode selection

This mode can be selected by setting "01" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023<sub>16</sub>).

#### ●Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from CNTR0/CNTR1 pin. Regardless of the timer counting or not the output of CNTR0/CNTR1 pin is initialized to the level of specified by their active edge switch bits when writing to the timer. When the CNTR0 active edge switch bit (bit 2) and the CNTR1 active edge switch bit (bit 6) of the timer XY mode register (address 0023<sub>16</sub>) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

Switching the CNTR0 or CNTR1 active edge switch bit will reverse the output level of the corresponding CNTR0 or CNTR1 pin.

#### ■Precautions

Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to output in this mode.

### (3) Event counter mode

#### ●Mode selection

This mode can be selected by setting "10" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 002316).

#### ●Explanation of operation

The operation is the same as the timer mode's except that the timer counts signals input from the CNTR0 or CNTR1 pin. The valid edge for the count operation depends on the CNTR0 active edge switch bit (bit 2) or the CNTR1 active edge switch bit (bit 6) of the timer XY mode register (address 002316). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

#### ■Precautions

Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in this mode.

### (4) Pulse width measurement mode

#### ●Mode selection

This mode can be selected by setting "11" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 002316).

#### ●Explanation of operation

When the CNTR0 active edge switch bit (bit 2) or the CNTR1 active edge switch bit (bit 6) of the timer XY mode register (address 002316) is "1", the timer counts during the term of one falling edge of CNTR0/CNTR1 pin input until the next rising edge of input ("L" term). When it is "0", the timer counts during the term of one rising edge input until the next falling edge input ("H" term).

#### ■Precautions

Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in this mode.

The count operation can be stopped by setting "1" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 002316). The interrupt request bit is set to "1" each time the timer underflows.

#### ●Precautions when switching count source

When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in considerable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

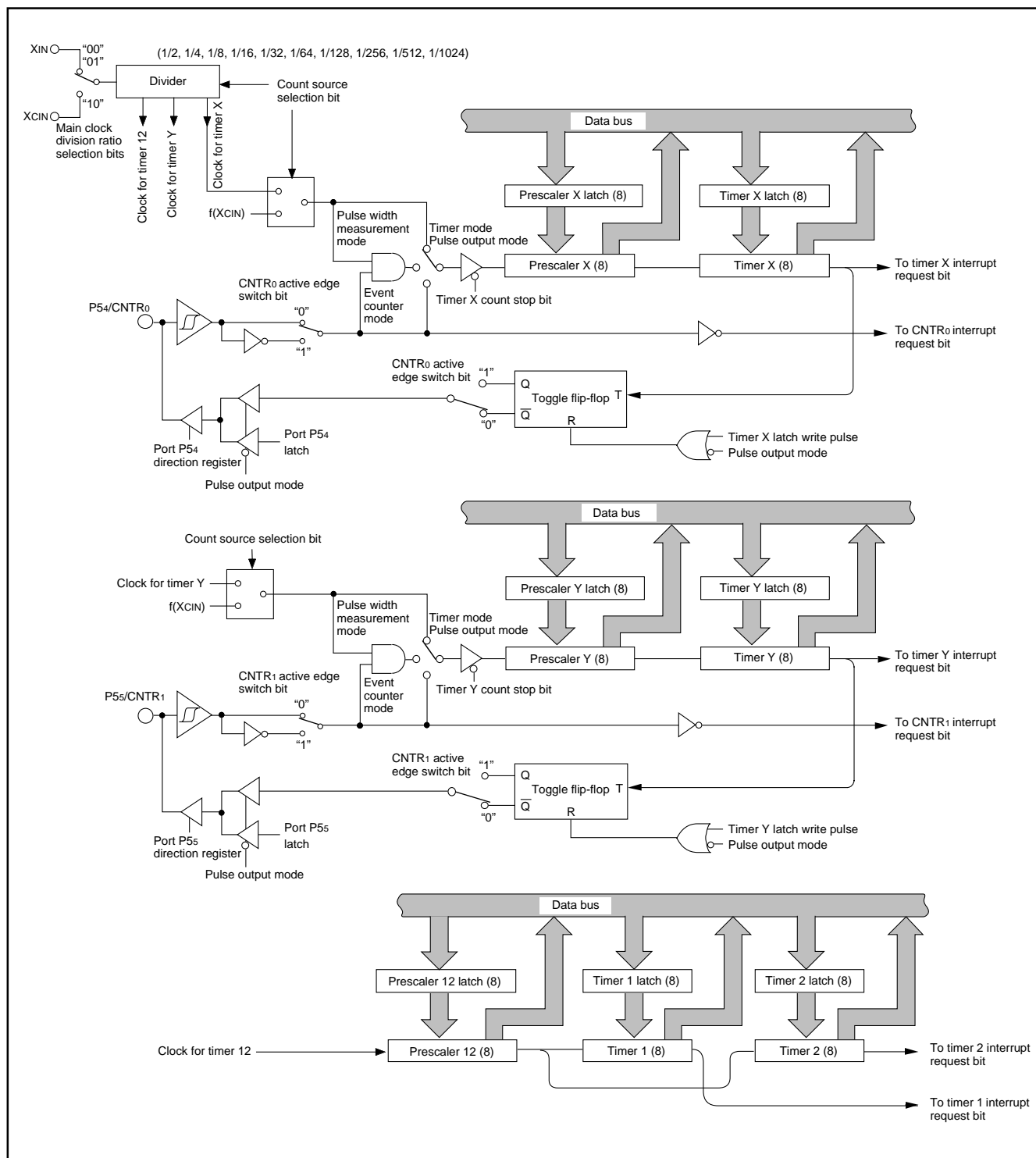


Fig. 21 Block diagram of timer X, timer Y, timer 1, and timer 2

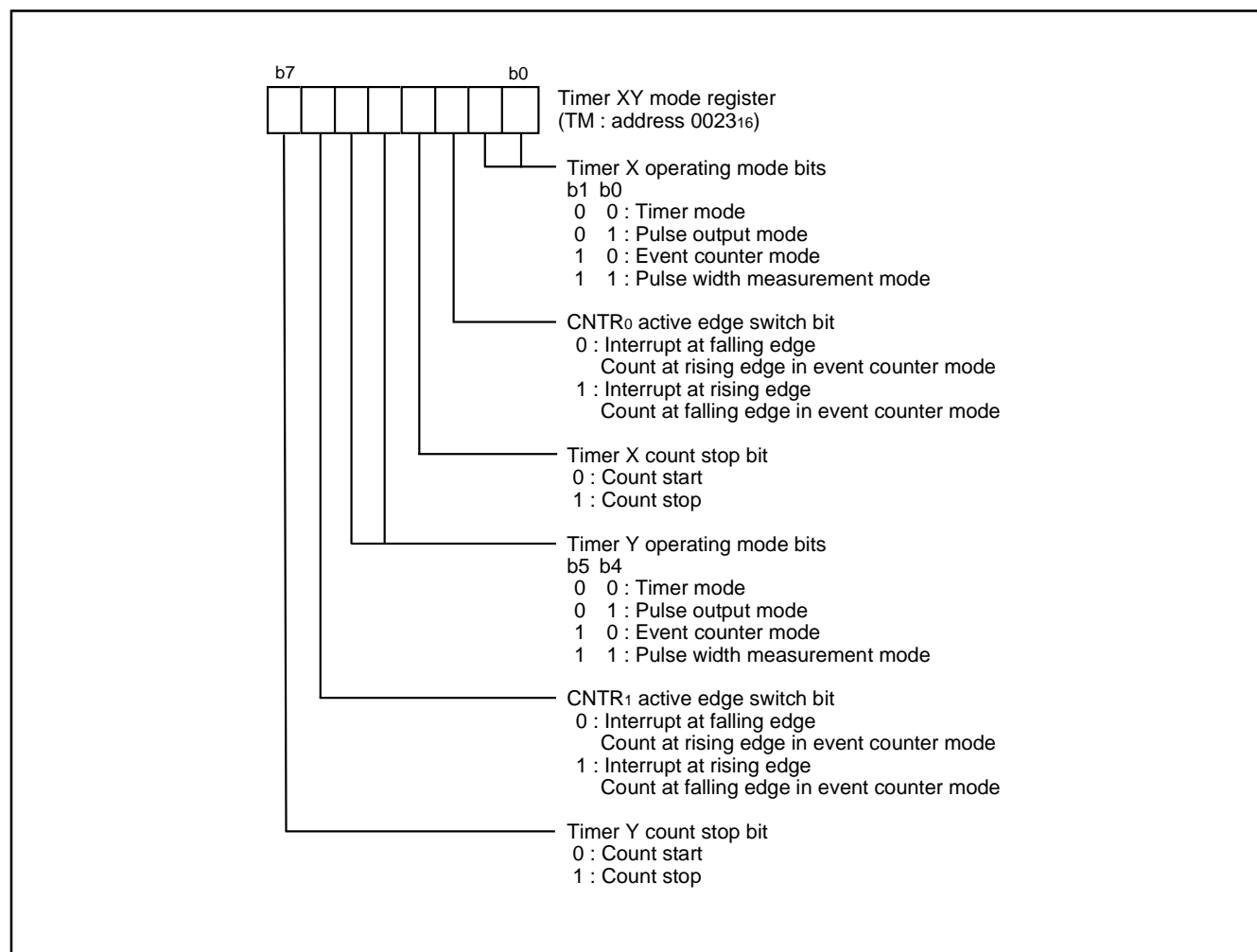


Fig. 22 Structure of timer XY mode register

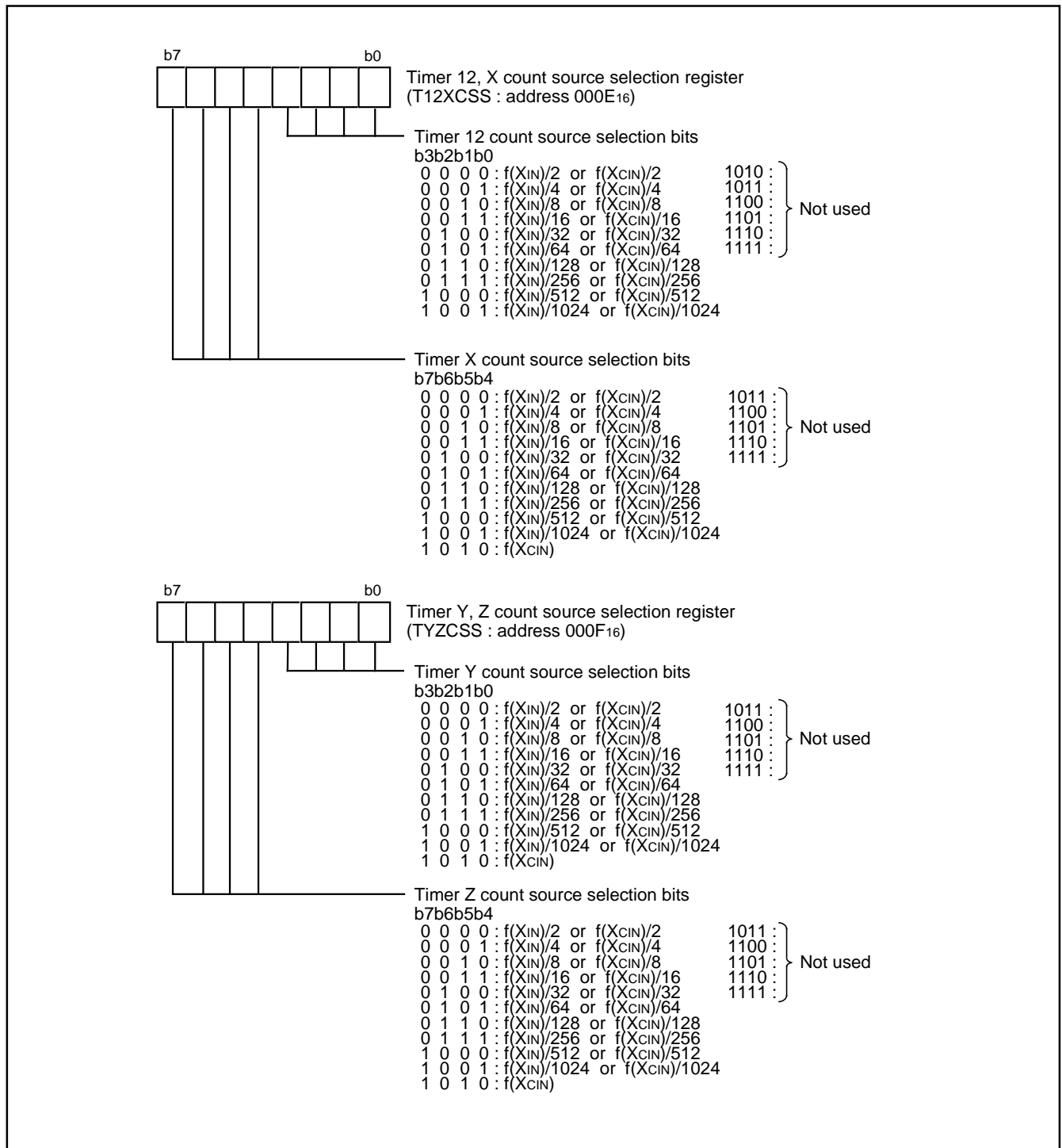


Fig. 23 Structure of timer 12, X and timer Y, Z count source selection registers

## ●16-bit Timer

The timer Z is a 16-bit timer. When the timer reaches "0000<sub>16</sub>", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to the timer Z is set to "1".

When reading/writing to the timer Z, perform reading/writing to both the high-order byte and the low-order byte. When reading the timer Z, read from the high-order byte first, followed by the low-order byte. Do not perform the writing to the timer Z between read operation of the high-order byte and read operation of the low-order byte. When writing to the timer Z, write to the low-order byte first, followed by the high-order byte. Do not perform the reading to the timer Z between write operation of the low-order byte and write operation of the high-order byte.

The timer Z can select the count source by the timer Z count source selection bits of timer Y, Z count source selection register (bits 7 to 4 at address 000F<sub>16</sub>).

Timer Z can select one of seven operating modes by setting the timer Z mode register (address 002A<sub>16</sub>).

## (1) Timer mode

### ●Mode selection

This mode can be selected by setting "000" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A<sub>16</sub>).

### ●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

### ●Interrupt

When an underflow occurs, the INT0/timer Z interrupt request bit (bit 0) of the interrupt request register 1 (address 003C<sub>16</sub>) is set to "1".

### ●Explanation of operation

During timer stop, usually write data to a latch and a timer at the same time to set the timer value.

The timer count operation is started by setting "0" to the timer Z count stop bit (bit 6) of the timer Z mode register (address 002A<sub>16</sub>).

When the timer reaches "0000<sub>16</sub>", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

When writing data to the timer during operation, the data is written only into the latch. Then the new latch value is reloaded into the timer at the next underflow.

## (2) Event counter mode

### ●Mode selection

This mode can be selected by setting "000" to the timer Z operating mode bits (bits 2 to 0) and setting "1" to the timer/event counter mode switch bit (bit 7) of the timer Z mode register (address 002A<sub>16</sub>).

The valid edge for the count operation depends on the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A<sub>16</sub>). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

### ●Interrupt

The interrupt at an underflow is the same as the timer mode's.

### ●Explanation of operation

The operation is the same as the timer mode's.

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

Figure 26 shows the timing chart of the timer/event counter mode.

## (3) Pulse output mode

### ●Mode selection

This mode can be selected by setting "001" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A<sub>16</sub>).

### ●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XIN); or f(XCIN) can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of f(XCIN); or f(XCIN) can be selected as the count source.

### ●Interrupt

The interrupt at an underflow is the same as the timer mode's.

### ●Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from CNTR2 pin. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A<sub>16</sub>) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

### ■Precautions

Set the double-function port of CNTR2 pin and port P47 to output in this mode.

The output from CNTR2 pin is initialized to the level depending on CNTR2 active edge switch bit by writing to the timer.

When the value of the CNTR2 active edge switch bit is changed, the output level of CNTR2 pin is inverted.

Figure 27 shows the timing chart of the pulse output mode.



#### (4) Pulse period measurement mode

##### ●Mode selection

This mode can be selected by setting "010" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

##### ●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of  $f(XIN)$ ; or  $f(XCIN)$  can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of  $f(XCIN)$ ; or  $f(XCIN)$  can be selected as the count source.

##### ●Interrupt

The interrupt at an underflow is the same as the timer mode's. When the pulse period measurement is completed, the INT4/CNTR2 interrupt request bit (bit 5) of the interrupt request register 2 (address 003D16) is set to "1".

##### ●Explanation of operation

The cycle of the pulse which is input from the CNTR2 pin is measured. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A16) is "0", the timer counts during the term from one falling edge of CNTR2 pin input to the next falling edge. When it is "1", the timer counts during the term from one rising edge input to the next rising edge input.

When the valid edge of measurement completion/start is detected, the 1's complement of the timer value is written to the timer latch and "FFFF16" is set to the timer.

Furthermore when the timer underflows, the timer Z interrupt request occurs and "FFFF16" is set to the timer. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

##### ■Precautions

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

"FFFF16" is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse period measurement depends on the timer value just before measurement start.

Figure 28 shows the timing chart of the pulse period measurement mode.

#### (5) Pulse width measurement mode

##### ●Mode selection

This mode can be selected by setting "011" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

##### ●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of  $f(XIN)$ ; or  $f(XCIN)$  can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of  $f(XCIN)$ ; or  $f(XCIN)$  can be selected as the count source.

##### ●Interrupt

The interrupt at an underflow is the same as the timer mode's. When the pulse widths measurement is completed, the INT4/CNTR2 interrupt request bit (bit 5) of the interrupt request register 2 (address 003D16) is set to "1".

##### ●Explanation of operation

The pulse width which is input from the CNTR2 pin is measured. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A16) is "0", the timer counts during the term from one rising edge input to the next falling edge input ("H" term). When it is "1", the timer counts during the term from one falling edge of CNTR2 pin input to the next rising edge of input ("L" term). When the valid edge of measurement completion is detected, the 1's complement of the timer value is written to the timer latch and "FFFF16" is set to the timer.

When the timer Z underflows, the timer Z interrupt occurs and "FFFF16" is set to the timer Z. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

##### ■Precautions

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse widths).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

"FFFF16" is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse width measurement depends on the timer value just before measurement start.

Figure 29 shows the timing chart of the pulse width measurement mode.

## (6) Programmable waveform generating mode

### ●Mode selection

This mode can be selected by setting "100" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

### ●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of  $f(XIN)$ ; or  $f(XCIN)$  can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of  $f(XCIN)$ ; or  $f(XCIN)$  can be selected as the count source.

### ●Interrupt

The interrupt at an underflow is the same as the timer mode's.

### ●Explanation of operation

The operation is the same as the timer mode's. Moreover the timer outputs the data set in the output level latch (bit 4) of the timer Z mode register (address 002A16) from the CNTR2 pin each time the timer underflows.

Changing the value of the output level latch and the timer latch after an underflow makes it possible to output an optional waveform from the CNTR2 pin.

### ■Precautions

Set the double-function port of CNTR2 pin and port P47 to output in this mode.

Figure 30 shows the timing chart of the programmable waveform generating mode.

## (7) Programmable one-shot generating mode

### ●Mode selection

This mode can be selected by setting "101" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

### ●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of  $f(XIN)$ ; or  $f(XCIN)$  can be selected as the count source.

### ●Interrupt

The interrupt at an underflow is the same as the timer mode's.

The trigger to generate one-shot pulse can be selected by the INT1 active edge selection bit (bit 1) of the interrupt edge selection register (address 003A16). When it is "0", the falling edge active is selected; when it is "1", the rising edge active is selected.

When the valid edge of the INT1 pin is detected, the INT1 interrupt request bit (bit 1) of the interrupt request register 1 (address 003C16) is set to "1".

### ●Explanation of operation

•"H" one-shot pulse; Bit 5 of timer Z mode register = "0"

The output level of the CNTR2 pin is initialized to "L" at mode selection. When trigger generation (input signal to INT1 pin) is detected, "H" is output from the CNTR2 pin. When an underflow occurs, "L" is output. The "H" one-shot pulse width is set by the setting value to the timer Z register low-order and high-order. When trigger generating is detected during timer count stop, al-

though "H" is output from the CNTR2 pin, "H" output state continues because an underflow does not occur.

•"L" one-shot pulse; Bit 5 of timer Z mode register = "1"

The output level of the CNTR2 pin is initialized to "H" at mode selection. When trigger generation (input signal to INT1 pin) is detected, "L" is output from the CNTR2 pin. When an underflow occurs, "H" is output. The "L" one-shot pulse width is set by the setting value to the timer Z low-order and high-order. When trigger generating is detected during timer count stop, although "L" is output from the CNTR2 pin, "L" output state continues because an underflow does not occur.

### ■Precautions

Set the double-function port of CNTR2 pin and port P47 to output, and of INT1 pin and port P42 to input in this mode.

This mode cannot be used in low-speed mode.

If the value of the CNTR2 active edge switch bit is changed during one-shot generating enabled or generating one-shot pulse, then the output level from CNTR2 pin changes.

Figure 31 shows the timing chart of the programmable one-shot generating mode.

## ■Notes regarding all modes

### ●Timer Z write control

Which write control can be selected by the timer Z write control bit (bit 3) of the timer Z mode register (address 002A16), writing data to both the latch and the timer at the same time or writing data only to the latch.

When the operation "writing data only to the latch" is selected, the value is set to the timer latch by writing data to the address of timer Z and the timer is updated at next underflow. After reset release, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the latch and the timer at the same time by writing data to the address of timer Z.

In the case of writing data only to the latch, if writing data to the latch and an underflow are performed almost at the same time, the timer value may become undefined.

### ●Timer Z read control

A read-out of timer value is impossible in pulse period measurement mode and pulse width measurement mode. In the other modes, a read-out of timer value is possible regardless of count operating or stopped.

However, a read-out of timer latch value is impossible.

### ●Switch of interrupt active edge of CNTR2 and INT1

Each interrupt active edge depends on setting of the CNTR2 active edge switch bit and the INT1 active edge selection bit.

### ●Switch of count source

When switching the count source by the timer Z count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

### ●Usage of CNTR2 pin as normal I/O port

To use the CNTR2 pin as normal I/O port P47, set timer Z operating mode bits (b2, b1, b0) of timer Z mode register (address 002A16) to "000".

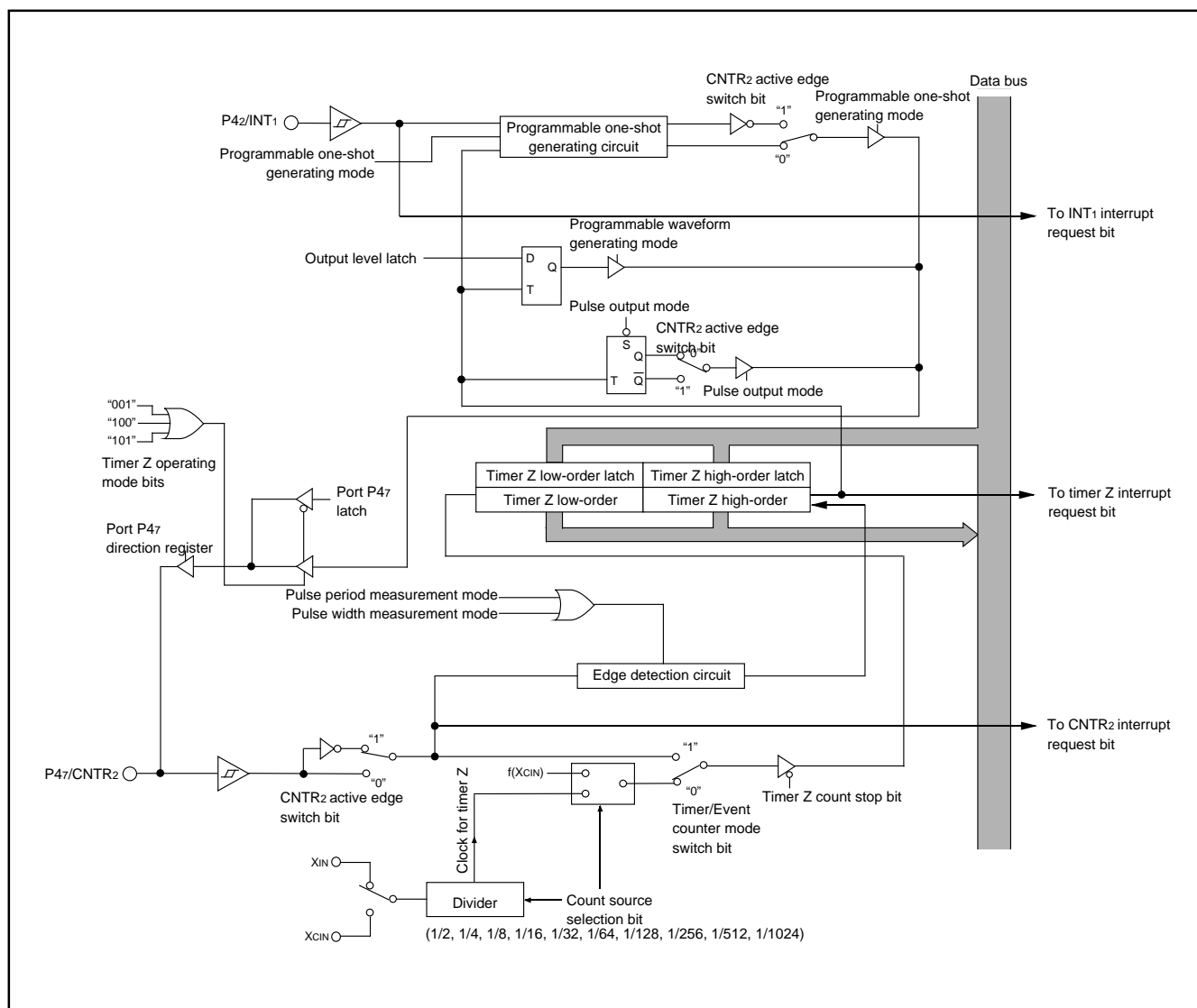


Fig. 24 Block diagram of timer Z

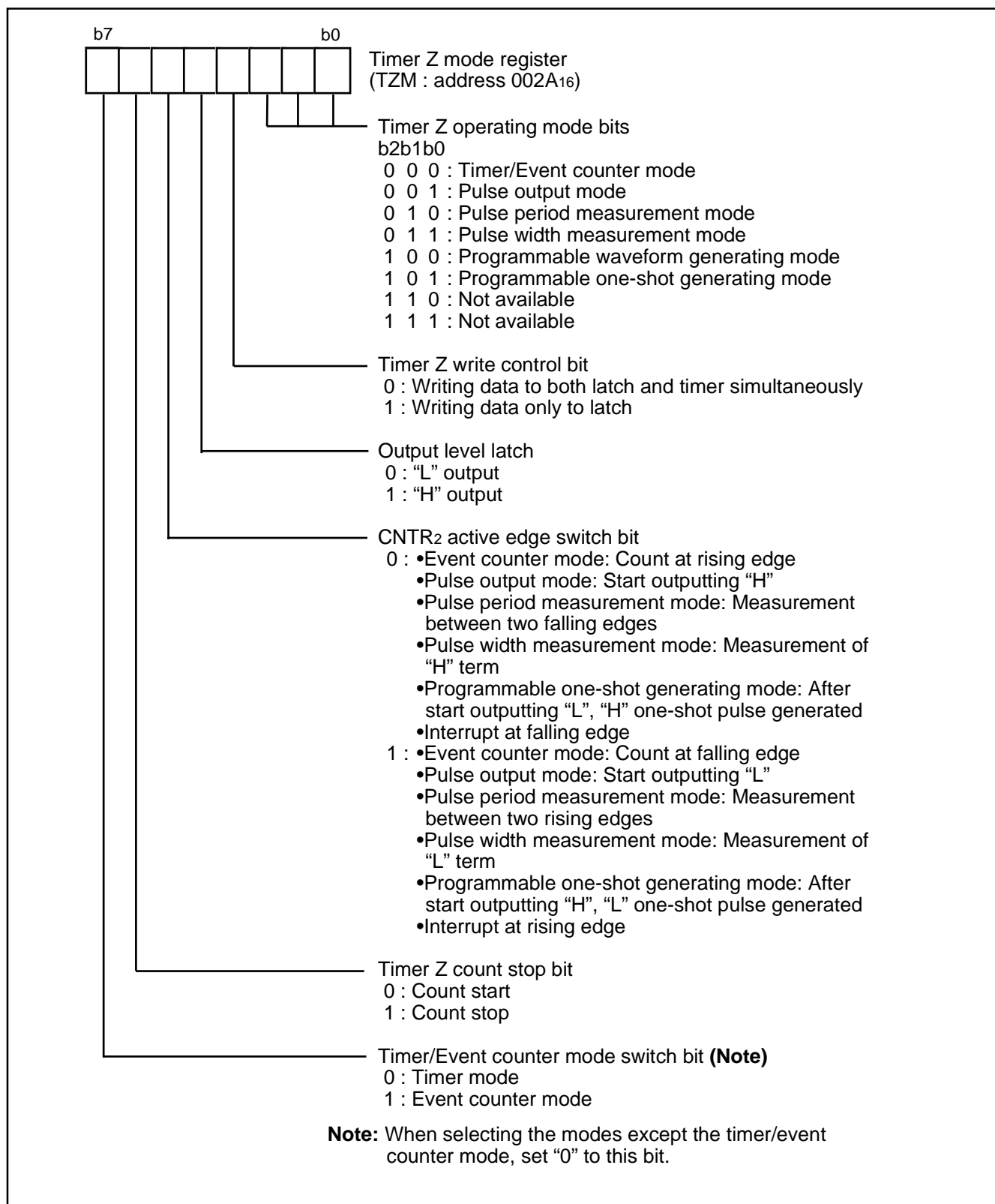


Fig. 25 Structure of timer Z mode register

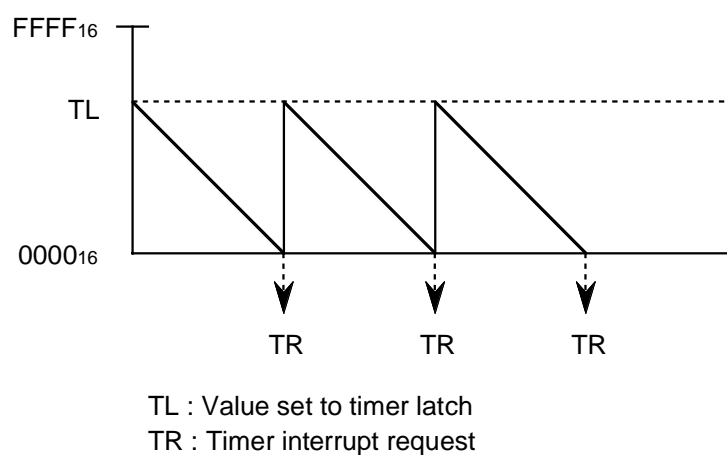


Fig. 26 Timing chart of timer/event counter mode

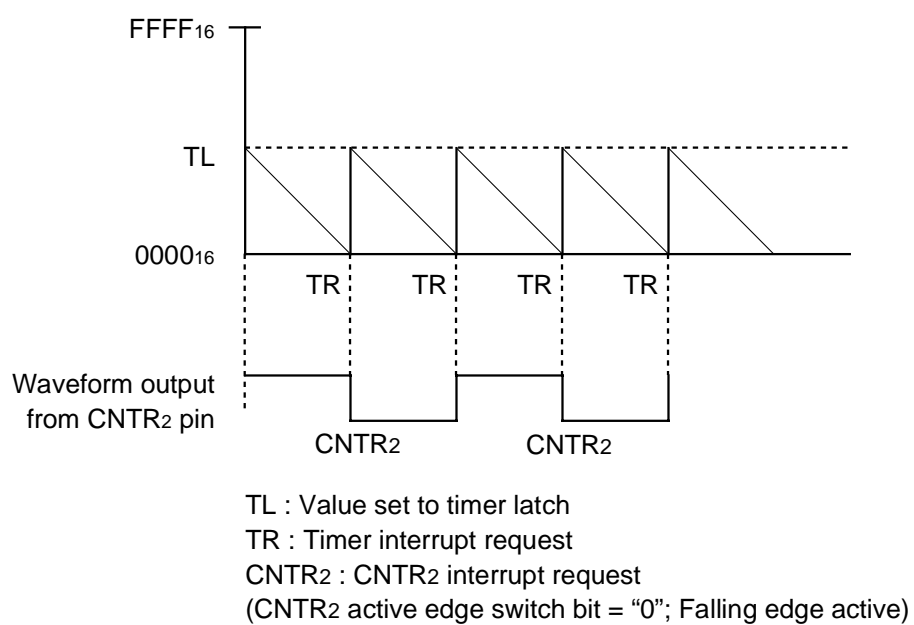


Fig. 27 Timing chart of pulse output mode

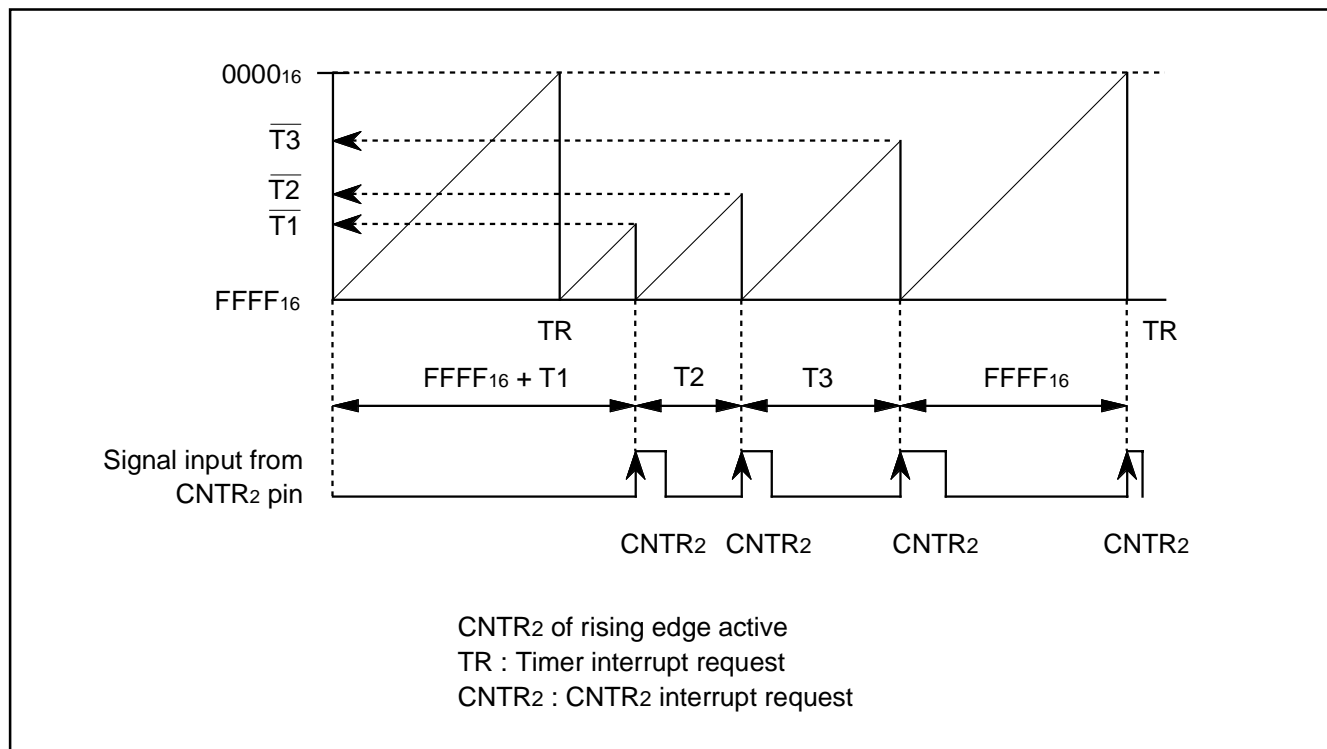


Fig. 28 Timing chart of pulse period measurement mode (Measuring term between two rising edges)

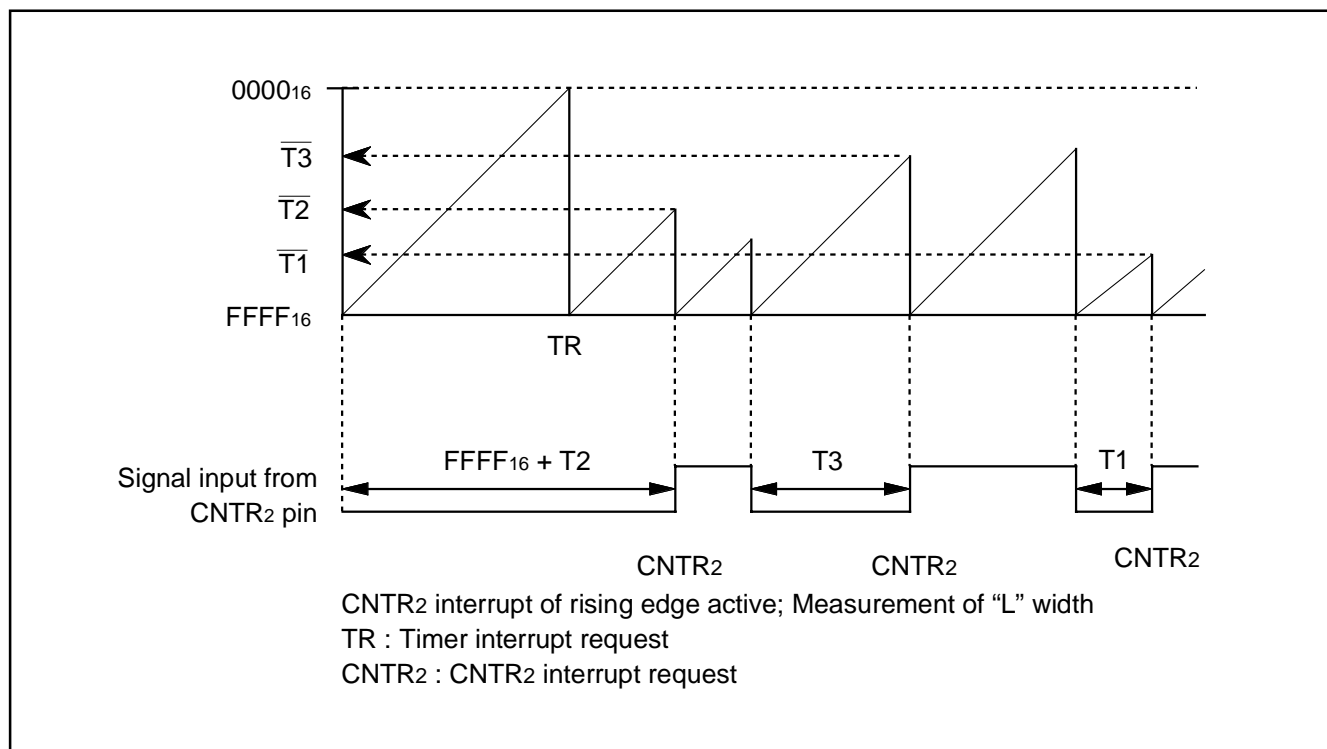


Fig. 29 Timing chart of pulse width measurement mode (Measuring "L" term)

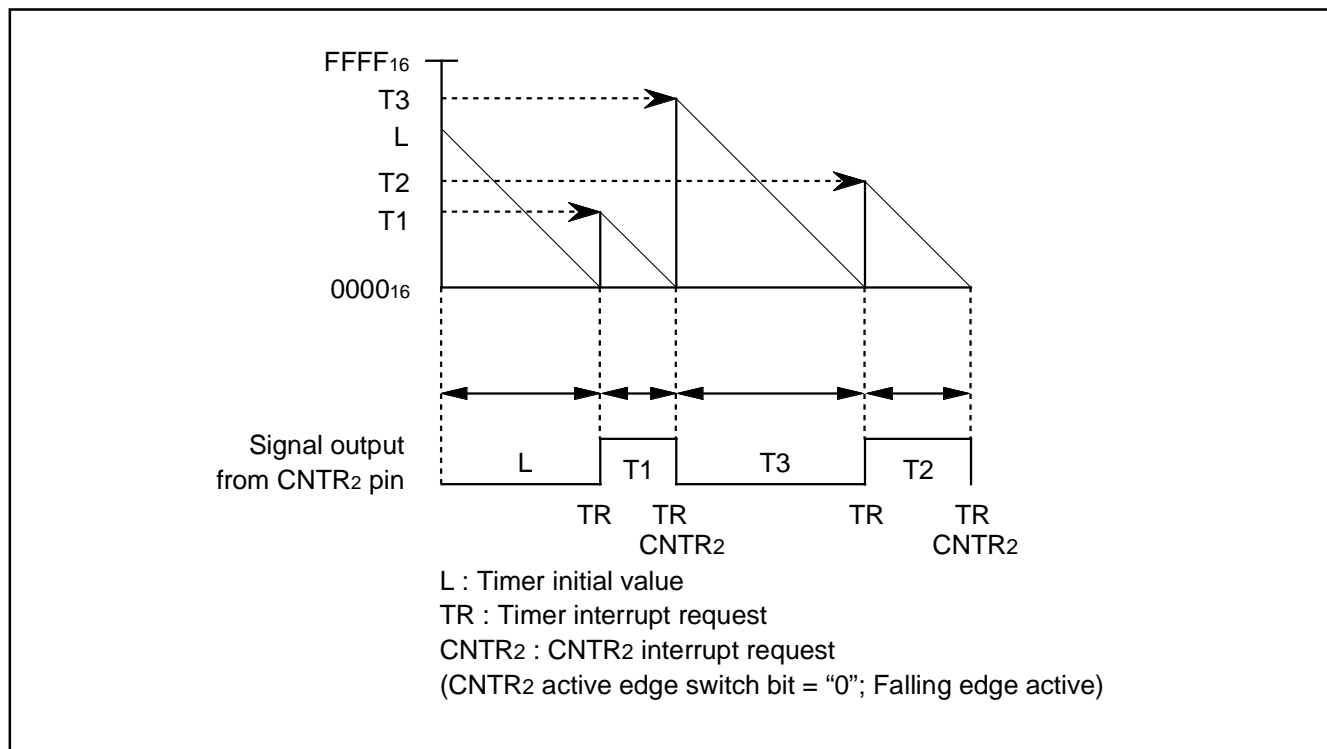


Fig. 30 Timing chart of programmable waveform generating mode

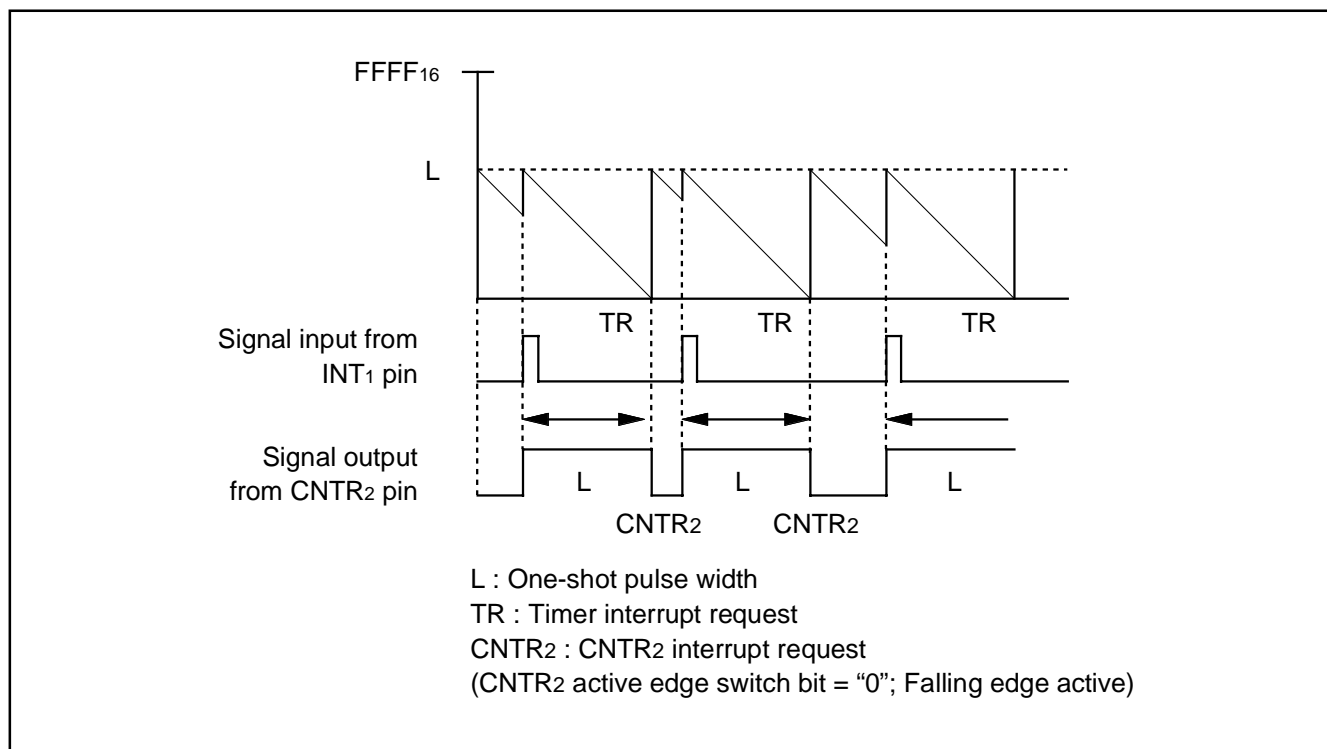


Fig. 31 Timing chart of programmable one-shot generating mode ("H" one-shot pulse generating)

## SERIAL I/O Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

### (1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address 001A<sub>16</sub>) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

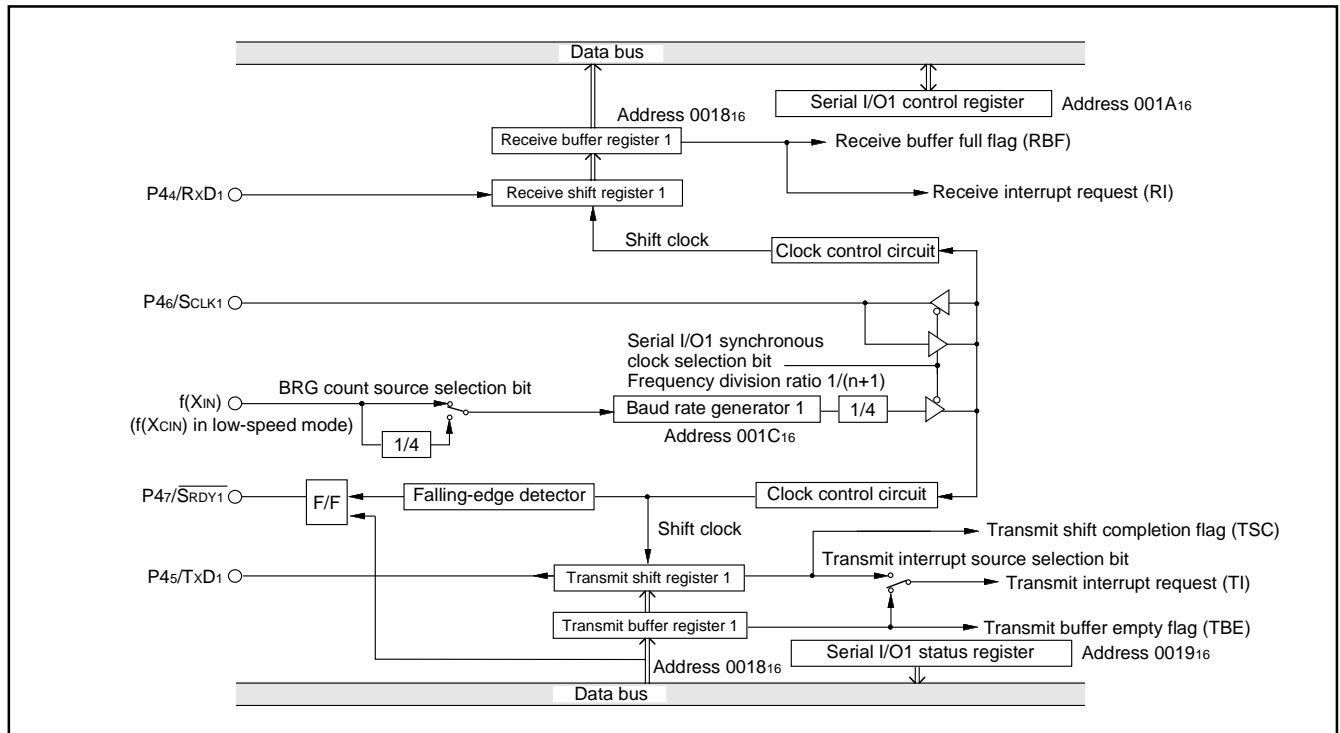


Fig. 32 Block diagram of clock synchronous serial I/O1

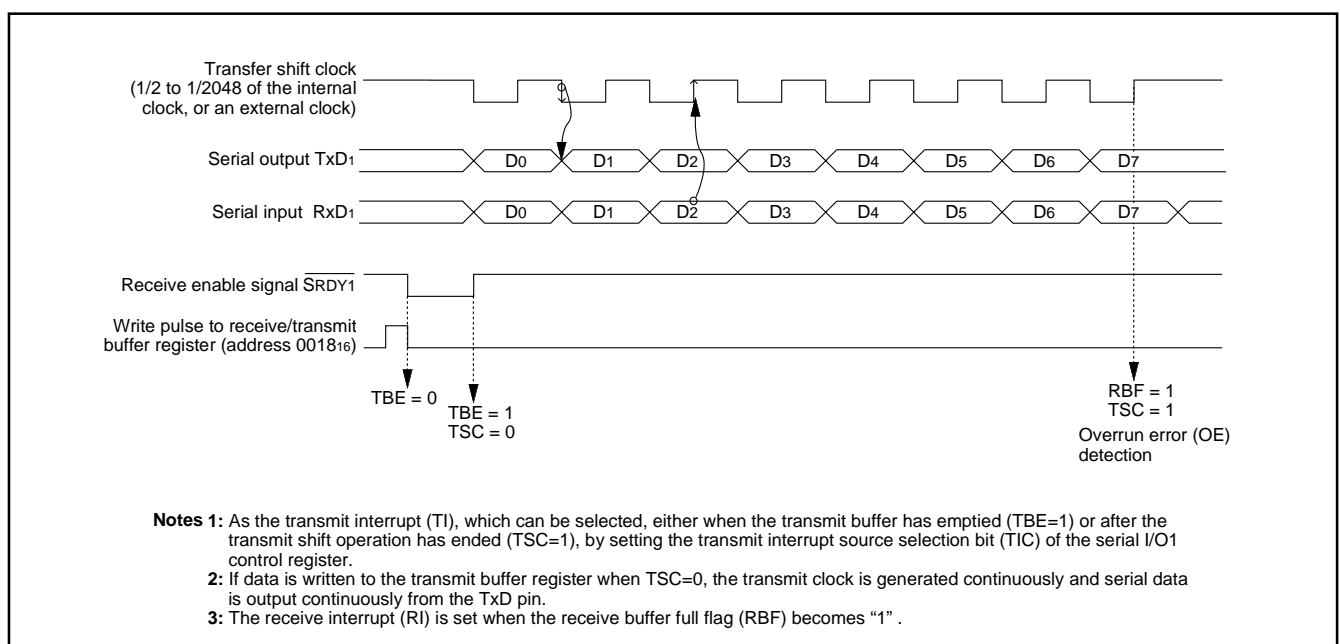


Fig. 33 Operation of clock synchronous serial I/O1



## (2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the

two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

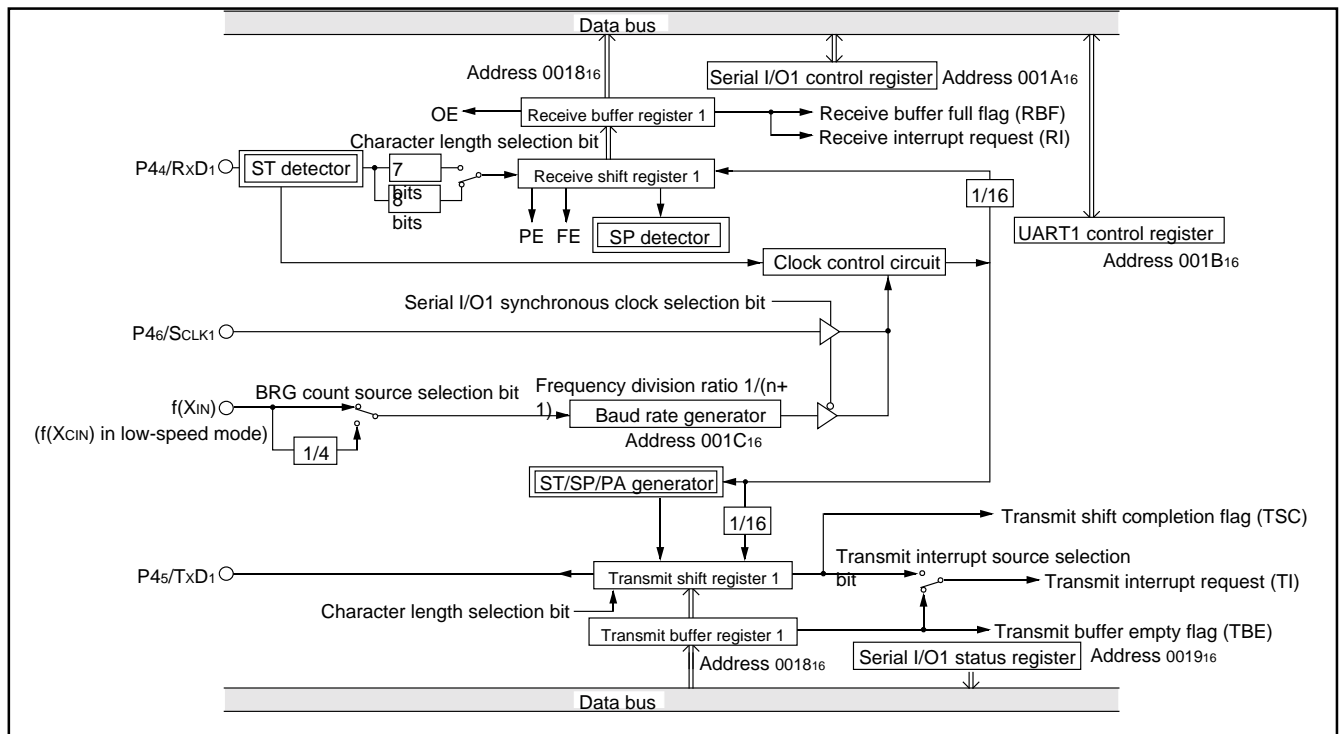


Fig. 34 Block diagram of UART serial I/O1

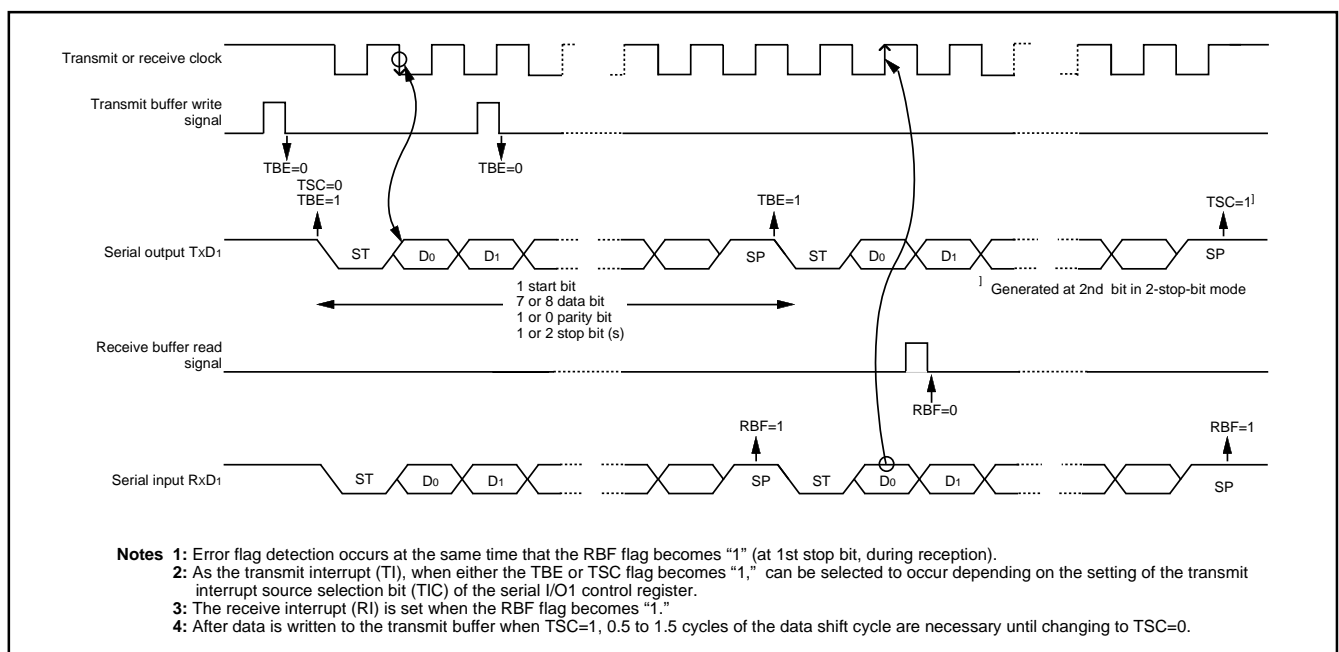


Fig. 35 Operation of UART serial I/O1

**[Serial I/O1 Control Register (SIO1CON)]**  
**001A16**

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

**[UART1 Control Register (UART1CON)]**  
**001B16**

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P45/TxD1 pin.

**[Serial I/O1 Status Register (SIO1STS)]**  
**001916**

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

**[Transmit Buffer Register 1/Receive Buffer Register 1 (TB1/RB1)]** **001816**

The transmit buffer register 1 and the receive buffer register 1 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

**[Baud Rate Generator 1 (BRG1)]** **001C16**

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by  $1/(n + 1)$ , where  $n$  is the value written to the baud rate generator.

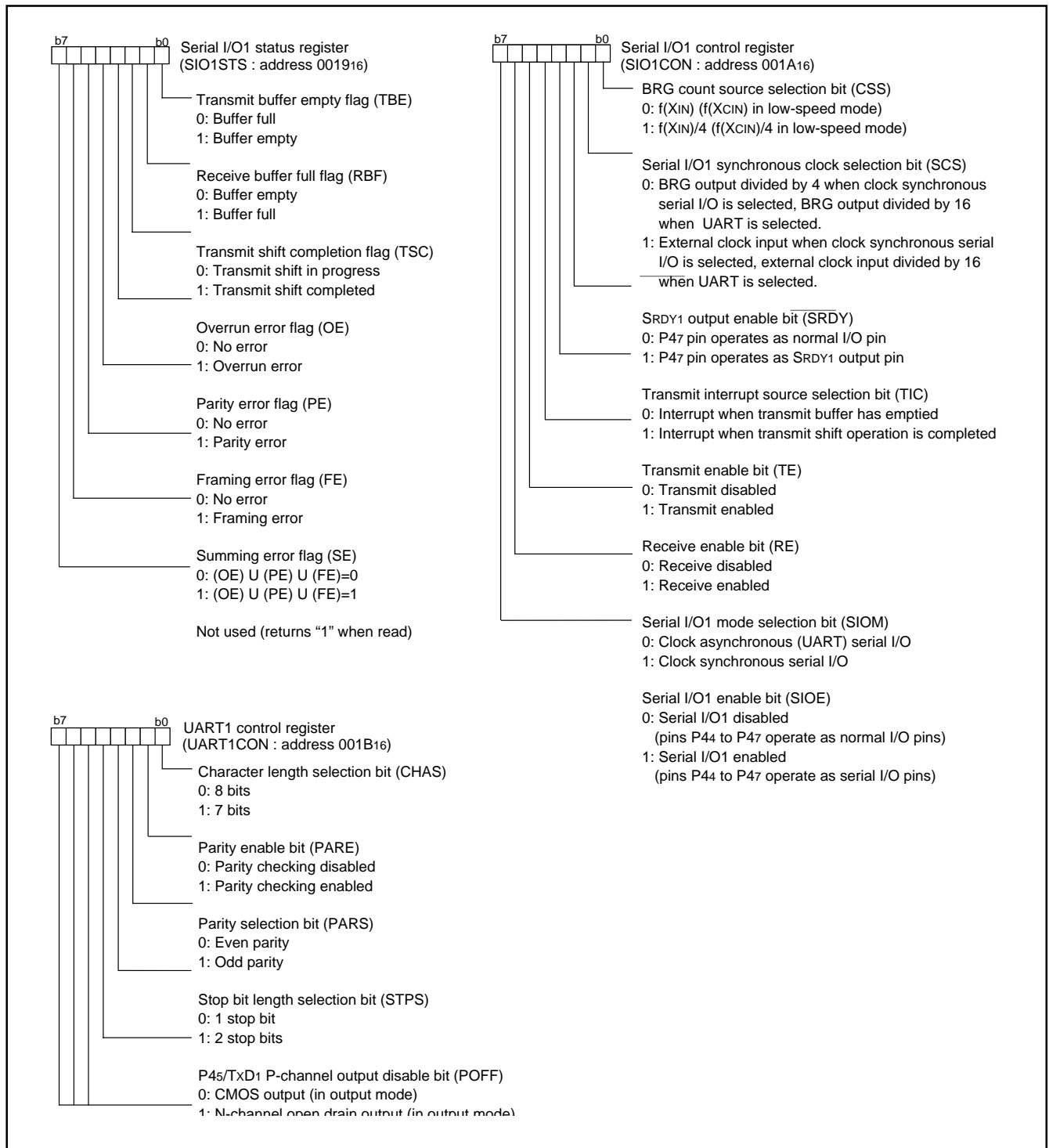


Fig. 36 Structure of serial I/O1 control registers

## ■ Notes concerning serial I/O1

### 1. Notes when selecting clock synchronous serial I/O

#### 1.1 Stop of transmission operation

##### ● Note

Clear the serial I/O1 enable bit and the transmit enable bit to "0" (serial I/O and transmit disabled).

##### ● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and  $\overline{\text{SRDY1}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

#### 1.2 Stop of receive operation

##### ● Note

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O1 enable bit to "0" (serial I/O disabled).

#### 1.3 Stop of transmit/receive operation

##### ● Note

Clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

##### ● Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O1 enable bit to "0" (serial I/O disabled) (refer to 1.1).

### 2. Notes when selecting clock asynchronous serial I/O

#### 2.1 Stop of transmission operation

##### ● Note

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to "0".

##### ● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and  $\overline{\text{SRDY1}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

#### 2.2 Stop of receive operation

##### ● Note

Clear the receive enable bit to "0" (receive disabled).

#### 2.3 Stop of transmit/receive operation

##### ● Note 1 (only transmission operation is stopped)

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to "0".

##### ● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and  $\overline{\text{SRDY1}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

##### ● Note 2 (only receive operation is stopped)

Clear the receive enable bit to "0" (receive disabled).

### 3. SRDY1 output of reception side

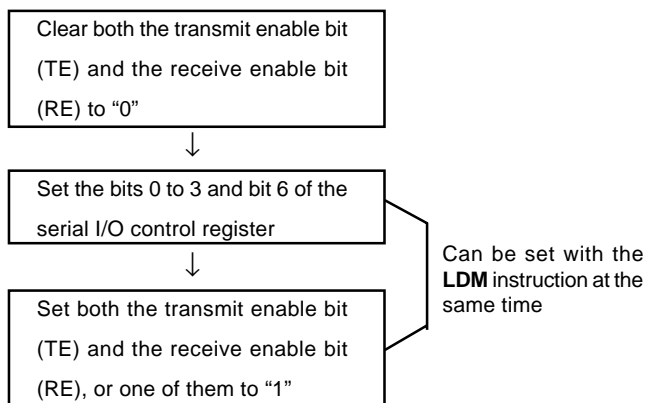
#### ● Note

When signals are output from the SRDY1 pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the SRDY1 output enable bit, and the transmit enable bit to "1" (transmit enabled).

### 4. Setting serial I/O1 control register again

#### ● Note

Set the serial I/O1 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0."



### 5. Data transmission control with referring to transmit shift register completion flag

#### ● Note

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

### 6. Transmission control when external clock is selected

#### ● Note

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK1 input level. Also, write data to the transmit buffer register at "H" of the SCLK1 input level.

### 7. Transmit interrupt request when transmit enable bit is set

#### ● Note

When using the transmit interrupt, take the following sequence.

- ① Set the serial I/O1 transmit interrupt enable bit to "0" (disabled).
  - ② Set the transmit enable bit to "1".
  - ③ Set the serial I/O1 transmit interrupt request bit to "0" after 1 or more instruction has executed.
- √ Set the serial I/O1 transmit interrupt enable bit to "1" (enabled).

#### ● Reason

When the transmit enable bit is set to "1", the transmit buffer empty flag and the transmit shift register shift completion flag are also set to "1". Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

## Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

### [Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains eight bits which control various serial I/O2 functions.

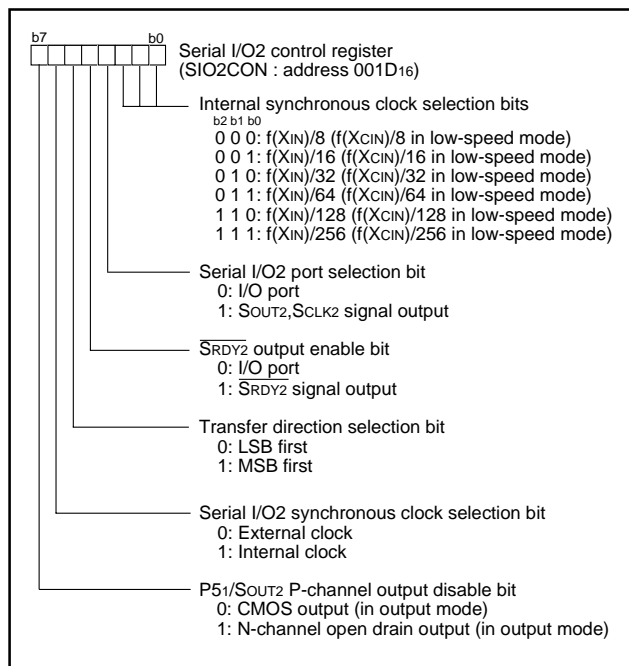


Fig. 37 Structure of serial I/O2 control register

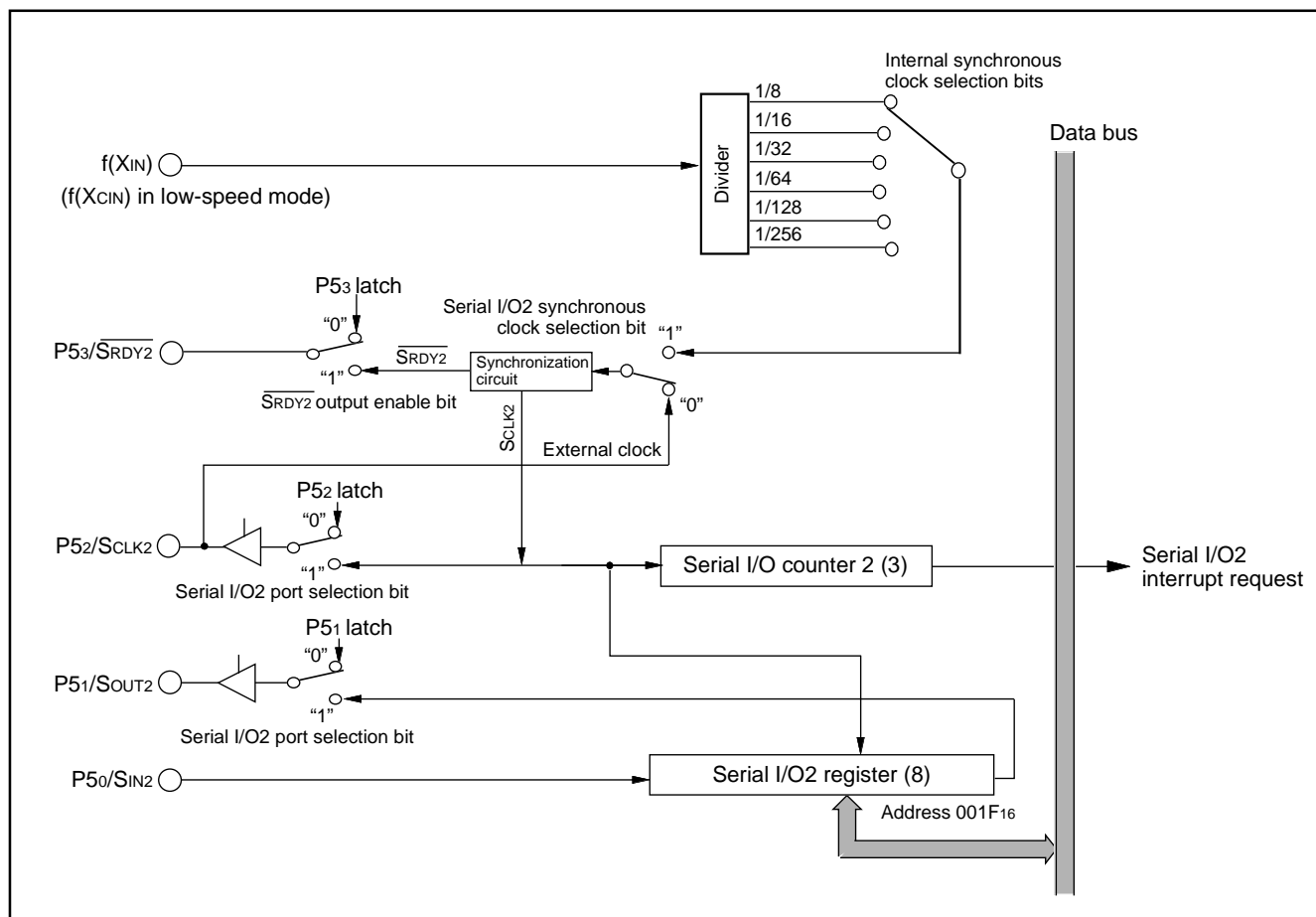


Fig. 38 Block diagram of serial I/O2

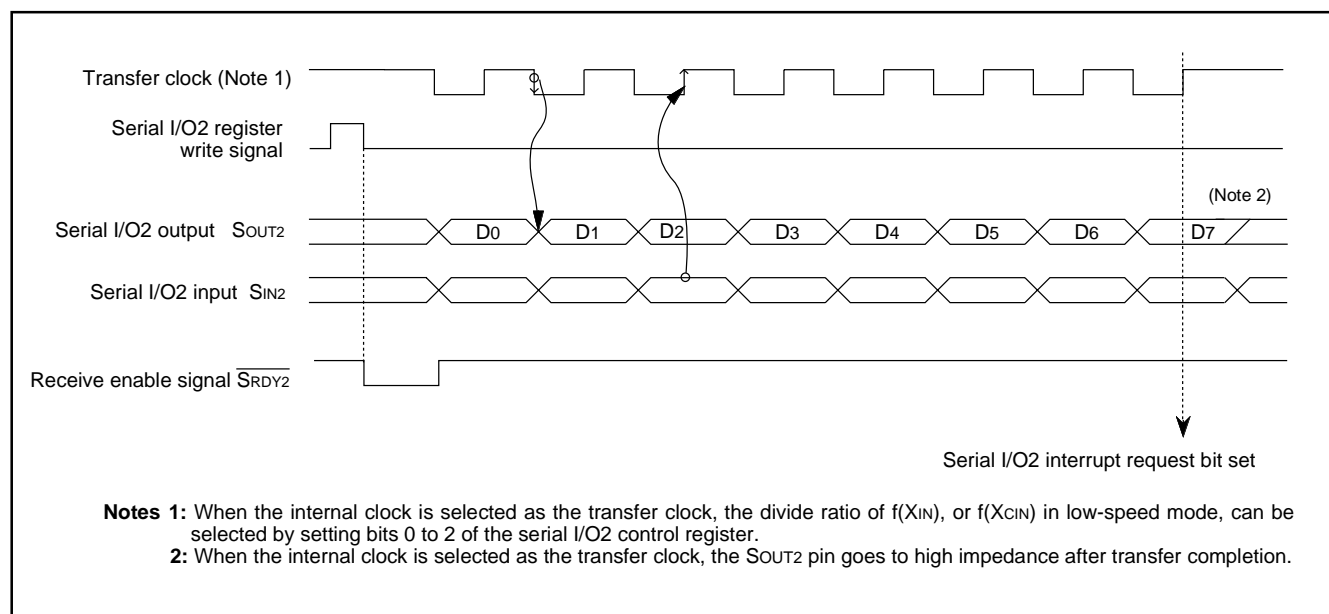


Fig. 39 Timing of serial I/O2

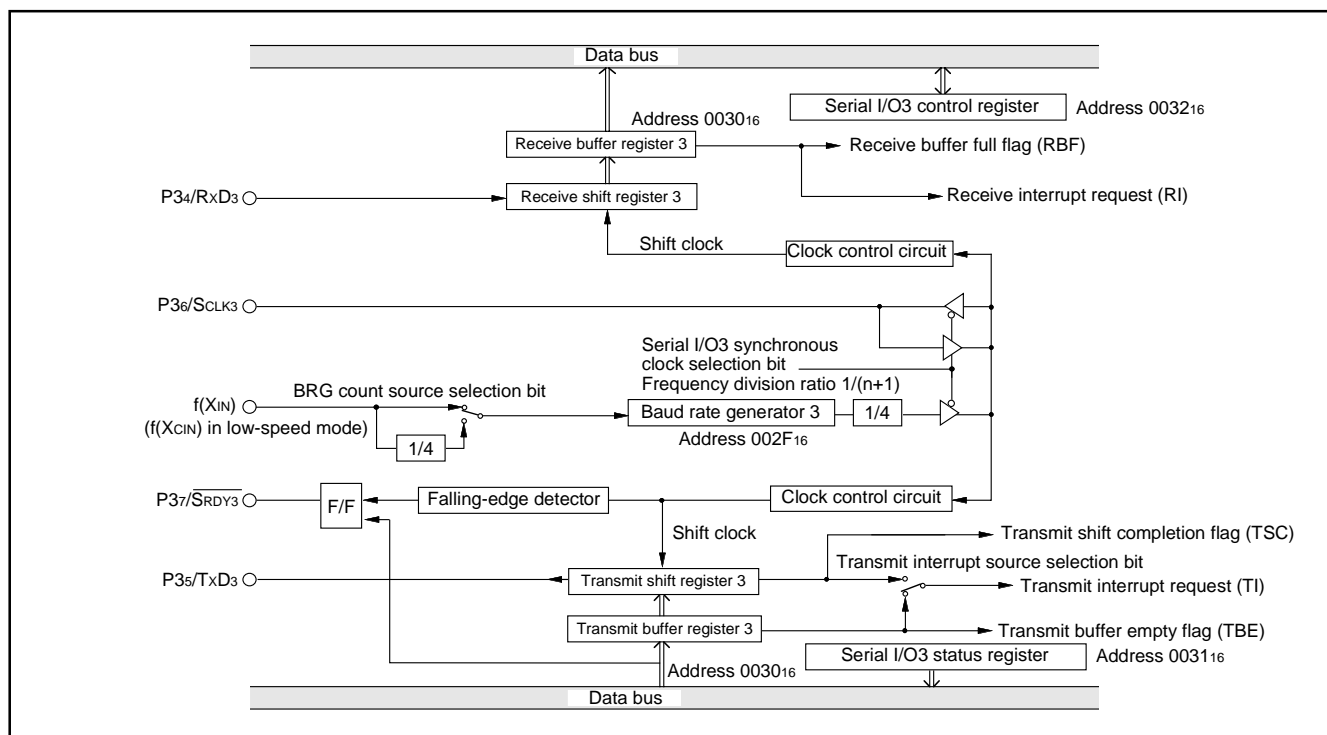
## Serial I/O3

Serial I/O3 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

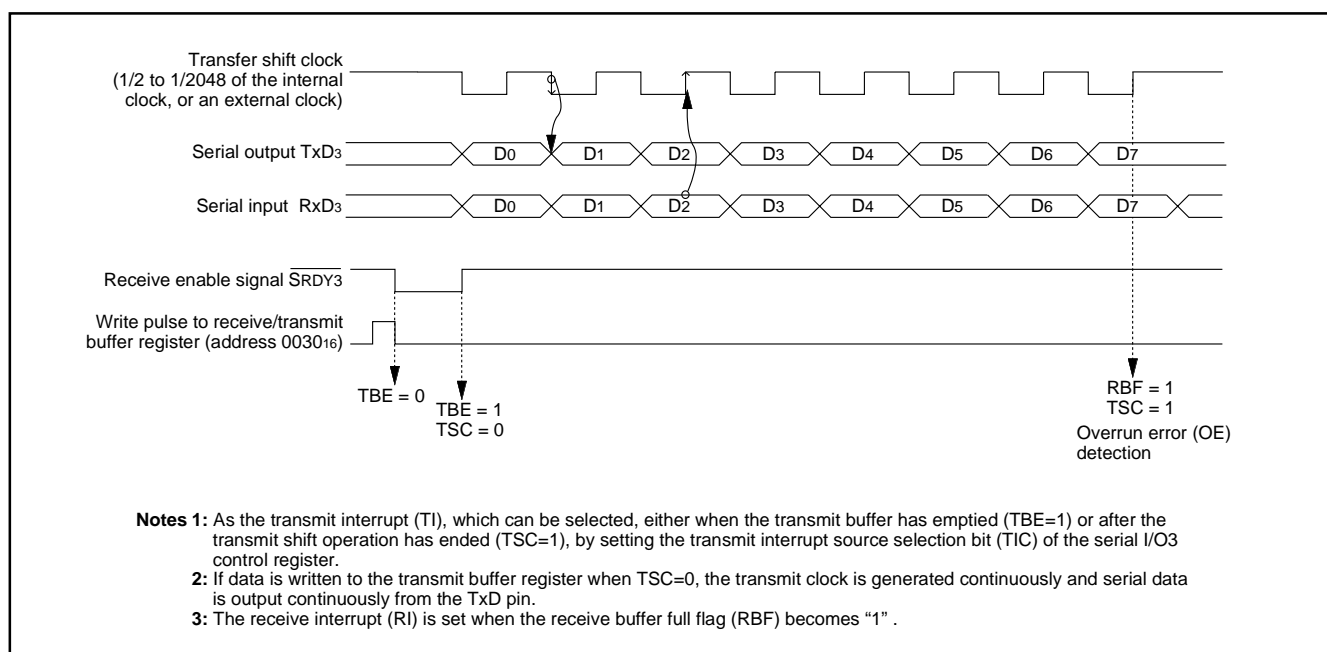
### (1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O3 mode can be selected by setting the serial I/O3 mode selection bit of the serial I/O3 control register (bit 6 of address 003216) to “1”.

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.



**Fig. 40 Block diagram of clock synchronous serial I/O3**



**Fig. 41 Operation of clock synchronous serial I/O3**



## (2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O3 mode selection bit of the serial I/O3 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the

two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

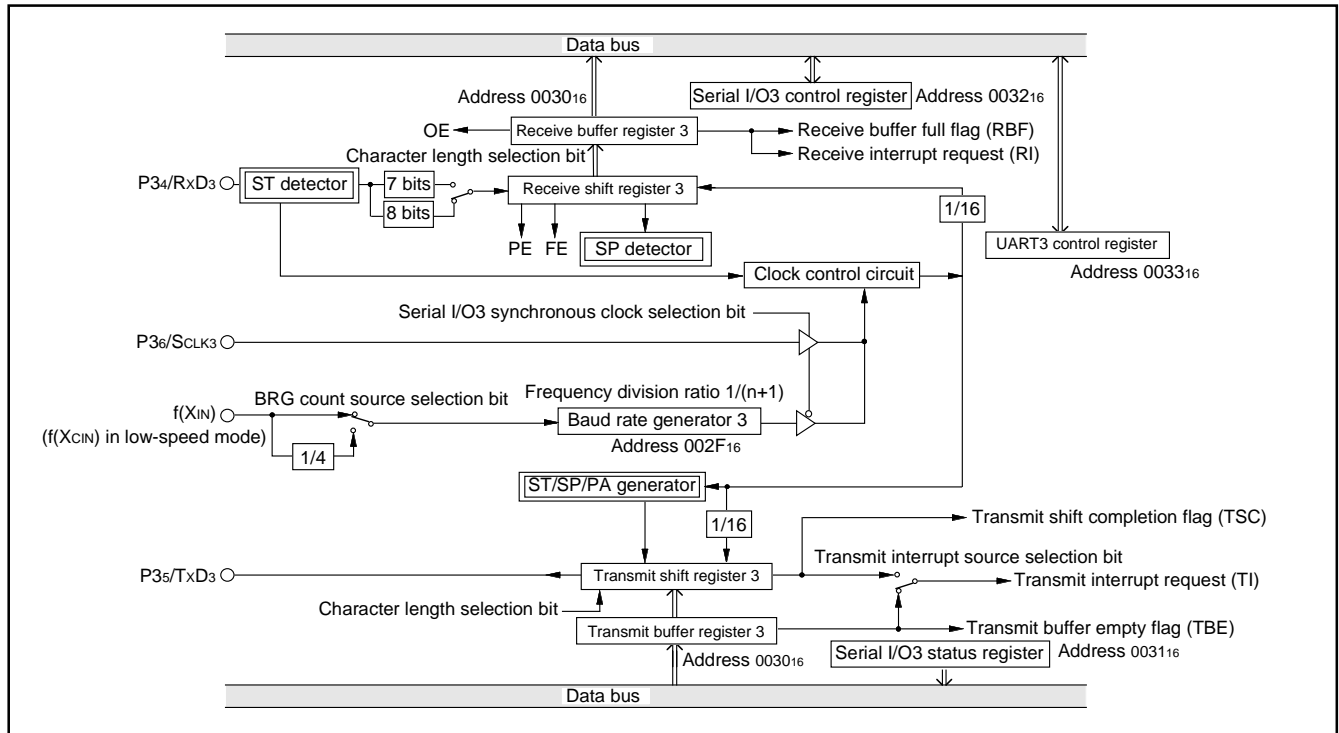


Fig. 42 Block diagram of UART serial I/O3

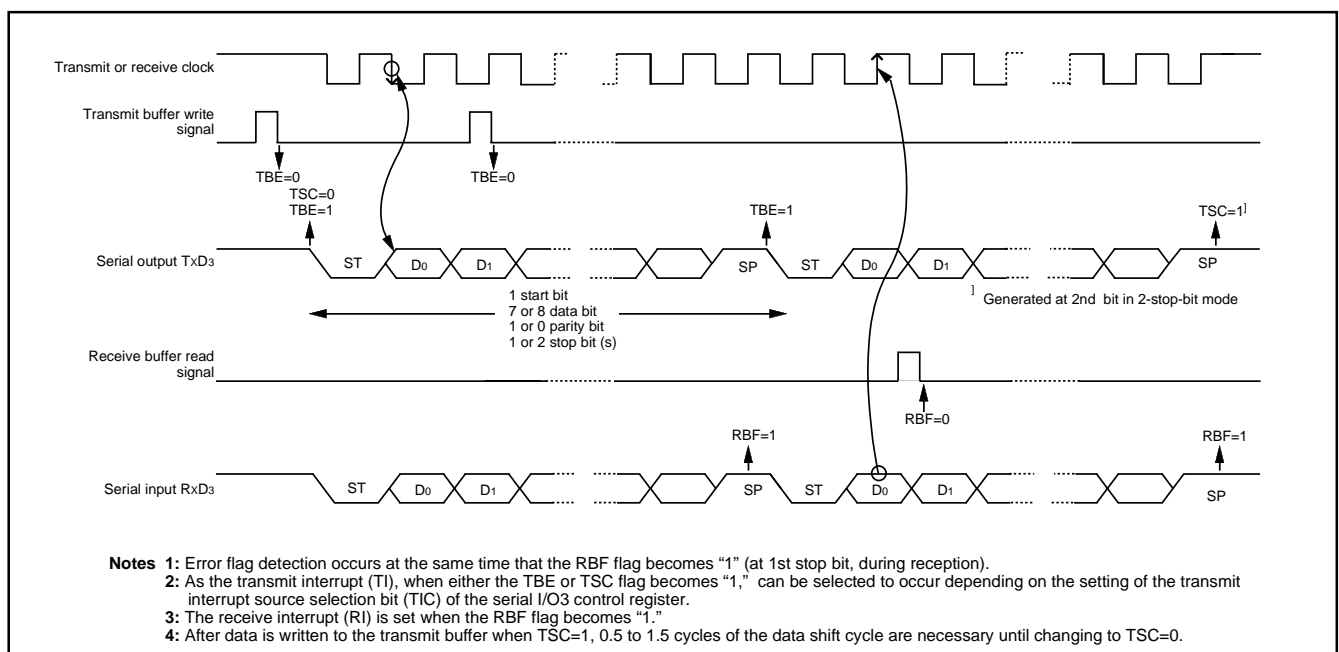


Fig. 43 Operation of UART serial I/O3

**[Serial I/O3 Control Register (SIO3CON)]**  
**0032<sub>16</sub>**

The serial I/O3 control register consists of eight control bits for the serial I/O3 function.

**[UART3 Control Register (UART3CON)]**  
**0033<sub>16</sub>**

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P35/TxD3 pin.

**[Serial I/O3 Status Register (SIO3STS)]** 0031<sub>16</sub>

The read-only serial I/O3 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O3 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O3 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O3 enable bit SIOE (bit 7 of the serial I/O3 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O3 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O3 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

**[Transmit Buffer Register 3/Receive Buffer Register 3 (TB3/RB3)]** 0030<sub>16</sub>

The transmit buffer register 3 and the receive buffer register 3 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

**[Baud Rate Generator 3 (BRG3)]** 002F<sub>16</sub>

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by  $1/(n + 1)$ , where  $n$  is the value written to the baud rate generator.

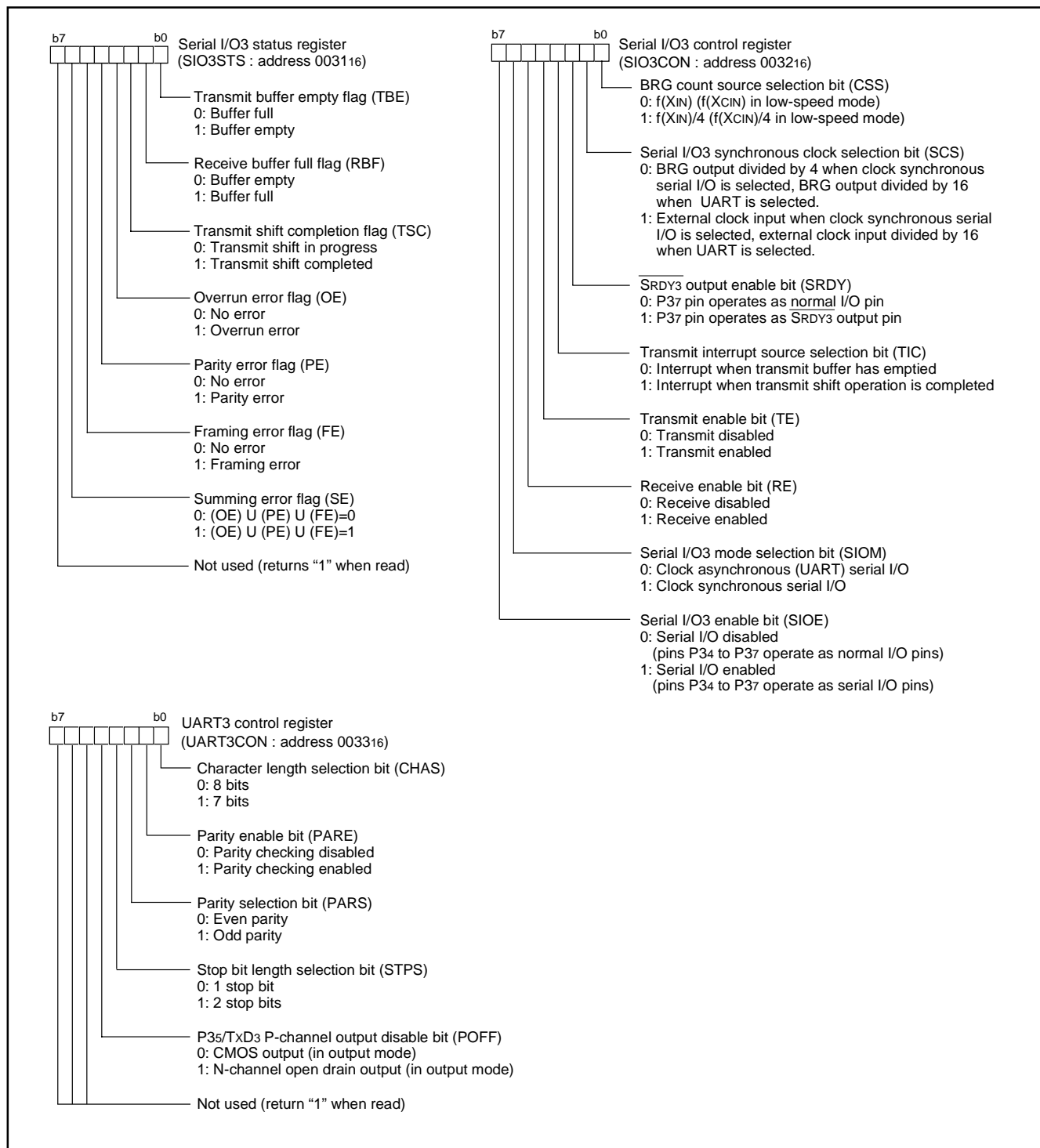


Fig. 44 Structure of serial I/O control registers

## ■ Notes concerning serial I/O3

### 1. Notes when selecting clock synchronous serial I/O

#### 1.1 Stop of transmission operation

##### ● Note

Clear the serial I/O3 enable bit and the transmit enable bit to "0" (serial I/O and transmit disabled).

##### ● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and  $\overline{\text{SRDY3}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to "1" at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

#### 1.2 Stop of receive operation

##### ● Note

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O3 enable bit to "0" (serial I/O disabled).

#### 1.3 Stop of transmit/receive operation

##### ● Note

Clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

##### ● Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O3 enable bit to "0" (serial I/O disabled) (refer to 1.1).

### 2. Notes when selecting clock asynchronous serial I/O

#### 2.1 Stop of transmission operation

##### ● Note

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to "0".

##### ● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and  $\overline{\text{SRDY3}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

#### 2.2 Stop of receive operation

##### ● Note

Clear the receive enable bit to "0" (receive disabled).

#### 2.3 Stop of transmit/receive operation

##### ● Note 1 (only transmission operation is stopped)

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to "0".

##### ● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and  $\overline{\text{SRDY3}}$  function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

##### ● Note 2 (only receive operation is stopped)

Clear the receive enable bit to "0" (receive disabled).

### 3. $\overline{\text{SRDY3}}$ output of reception side

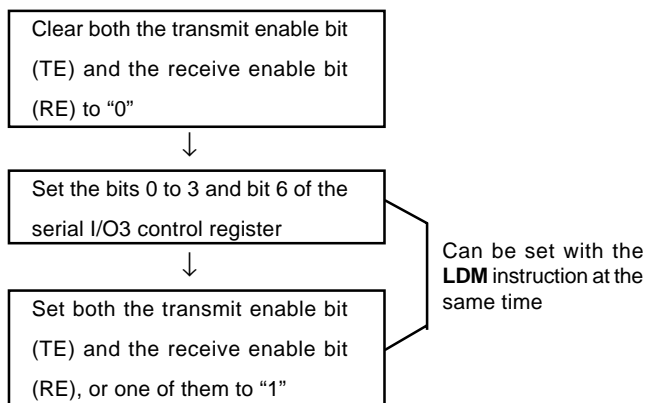
#### ● Note

When signals are output from the  $\overline{\text{SRDY3}}$  pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the  $\overline{\text{SRDY3}}$  output enable bit, and the transmit enable bit to "1" (transmit enabled).

### 4. Setting serial I/O3 control register again

#### ● Note

Set the serial I/O3 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0."



### 5. Data transmission control with referring to transmit shift register completion flag

#### ● Note

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

### 6. Transmission control when external clock is selected

#### ● Note

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK3 input level. Also, write data to the transmit buffer register at "H" of the SCLK input level.

### 7. Transmit interrupt request when transmit enable bit is set

#### ● Note

When using the transmit interrupt, take the following sequence.

- ① Set the serial I/O3 transmit interrupt enable bit to "0" (disabled).
  - ② Set the transmit enable bit to "1".
  - ③ Set the serial I/O3 transmit interrupt request bit to "0" after 1 or more instruction has executed.
- √ Set the serial I/O3 transmit interrupt enable bit to "1" (enabled).

#### ● Reason

When the transmit enable bit is set to "1", the transmit buffer empty flag and the transmit shift register shift completion flag are also set to "1". Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

## PULSE WIDTH MODULATION (PWM)

The 3803 group (Spec. H) has PWM functions with an 8-bit resolution, based on a signal that is the clock input  $X_{IN}$  or that clock input divided by 2 or the clock input  $X_{CIN}$  or that clock input divided by 2 in low-speed mode.

### Data Setting

The PWM output pin also functions as port P56. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.

If the value in the PWM prescaler is  $n$  and the value in the PWM register is  $m$  (where  $n = 0$  to 255 and  $m = 0$  to 255) :

$$\begin{aligned} \text{PWM period} &= 255 \times (n+1) / f(X_{IN}) \\ &= 31.875 \times (n+1) \mu\text{s} \quad (\text{when } f(X_{IN}) = 8 \text{ MHz}) \end{aligned}$$

$$\begin{aligned} \text{Output pulse "H" term} &= \text{PWM period} \times m / 255 \\ &= 0.125 \times (n+1) \times m \mu\text{s} \\ &\quad (\text{when } f(X_{IN}) = 8 \text{ MHz}) \end{aligned}$$

### PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

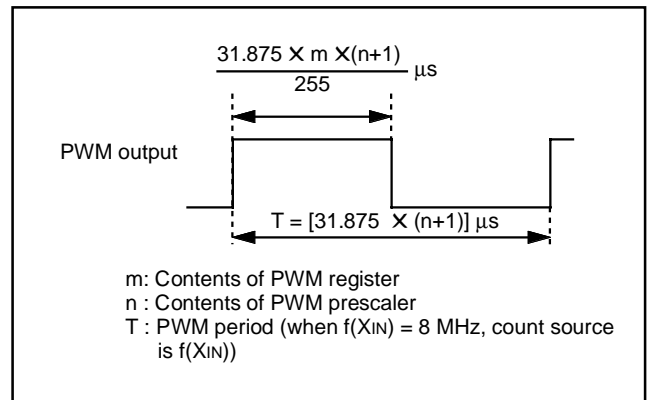


Fig. 45 Timing of PWM period

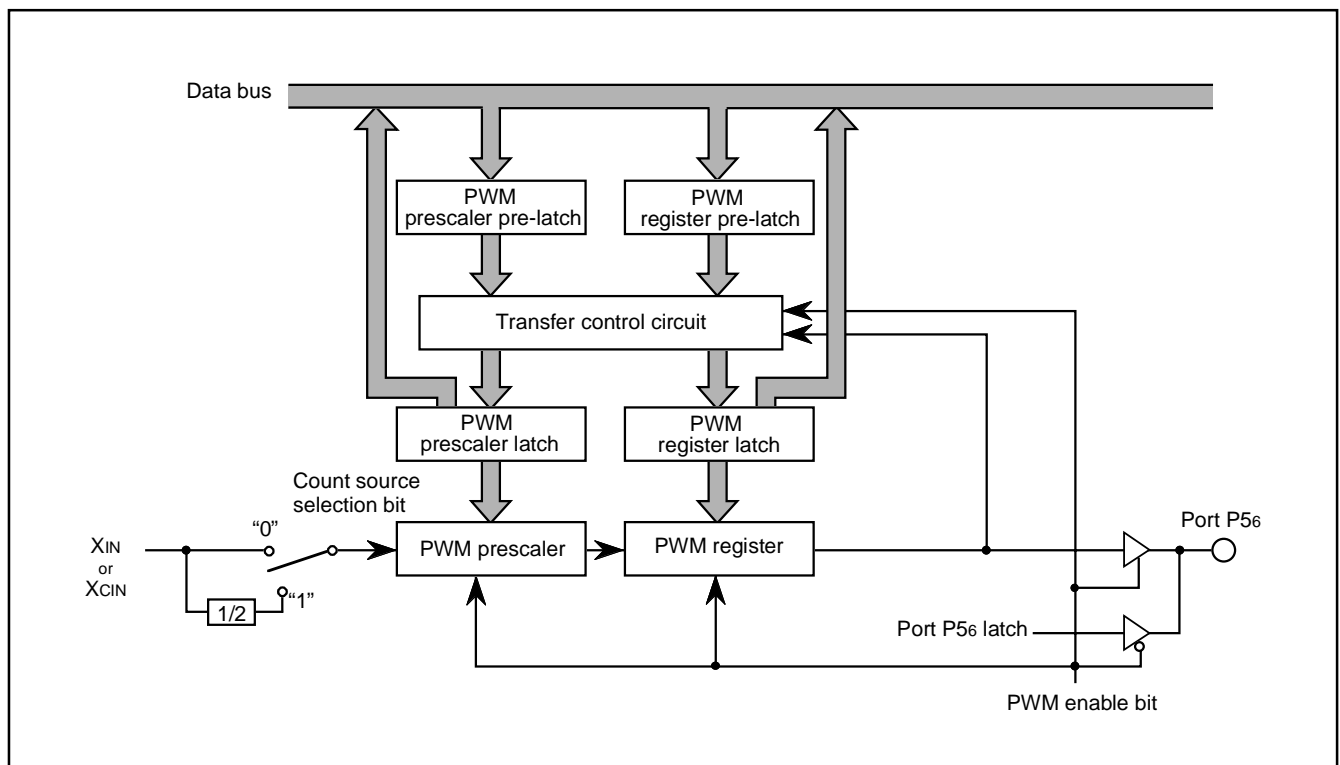


Fig. 46 Block diagram of PWM function

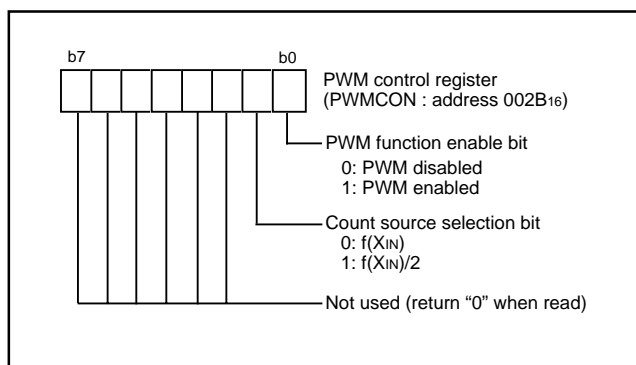


Fig. 47 Structure of PWM control register

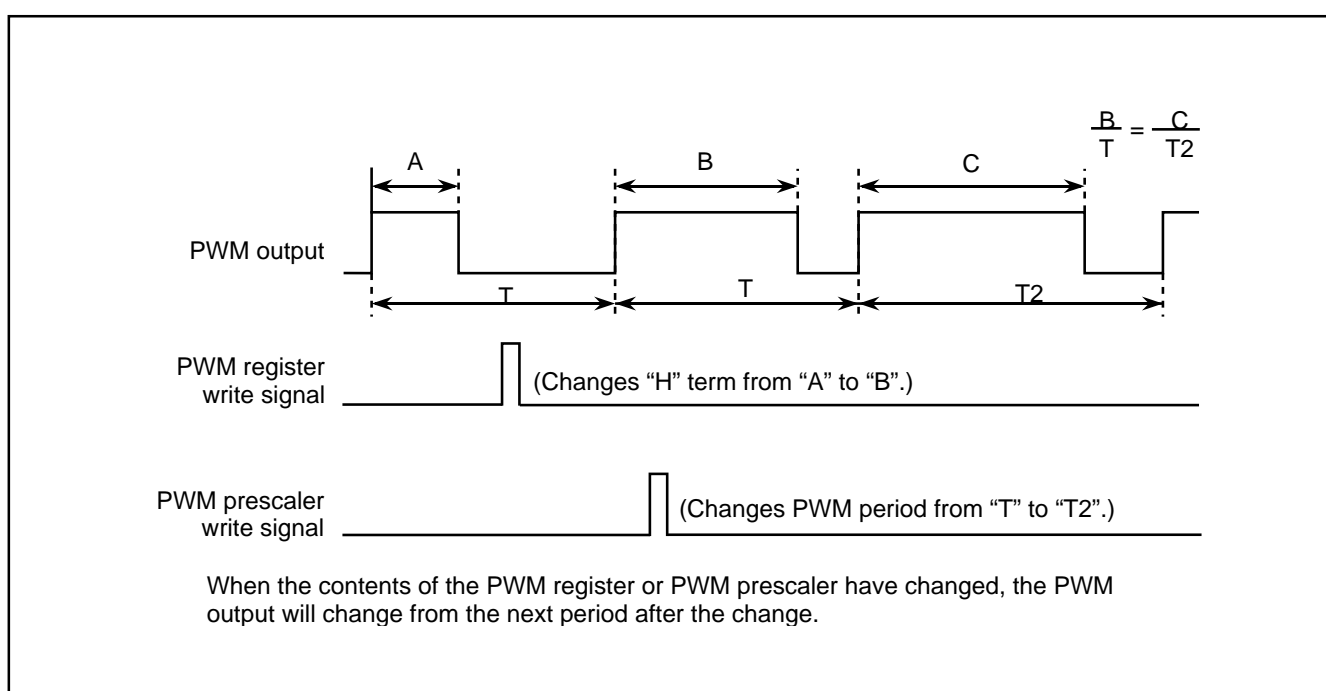


Fig. 48 PWM output timing when PWM register or PWM prescaler is changed

## A-D CONVERTER

### [A-D Conversion Register 1, 2 (AD1, AD2)] 003516, 003816

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

Bit 7 of the A-D conversion register 2 is the conversion mode selection bit. When this bit is set to "0," the A-D converter becomes the 10-bit A-D mode. When this bit is set to "1," that becomes the 8-bit A-D mode. The conversion result of the 8-bit A-D mode is stored in the A-D conversion register 1. As for 10-bit A-D mode, not only 10-bit reading but also only high-order 8-bit reading of conversion result can be performed by selecting the reading procedure of the A-D conversion registers 1, 2 after A-D conversion is completed (in Figure 50).

As for 10-bit A-D mode, the 8-bit reading inclined to MSB is performed when reading the A-D converter register 1 after A-D conversion is started; and when the A-D converter register 1 is read after reading the A-D converter register 2, the 8-bit reading inclined to LSB is performed.

### [AD/DA Control Register (ADCON)] 003416

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 and bit 4 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

## Comparison Voltage Generator

The comparison voltage generator divides the voltage between VREF and AVSS into 1024, and that outputs the comparison voltage in the 10-bit A-D mode (256 division in 8-bit A-D mode).

The A-D converter successively compares the comparison voltage Vref in each mode, dividing the VREF voltage (see below), with the input voltage.

#### •10-bit A-D mode (10-bit reading)

$$V_{ref} = \frac{V_{REF}}{1024} \times n \quad (n = 0-1023)$$

#### •10-bit A-D mode (8-bit reading)

$$V_{ref} = \frac{V_{REF}}{256} \times n \quad (n = 0-255)$$

#### •8-bit A-D mode

$$V_{ref} = \frac{V_{REF}}{256} \times (n-0.5) \quad (n = 1-255)$$

$$=0 \quad (n = 0)$$

## Channel Selector

The channel selector selects one of ports P67/AN7 to P60/AN0 or P07/AN15 to P00/AN8, and inputs the voltage to the comparator.

## Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the A-D conversion registers 1, 2. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A-D conversion.

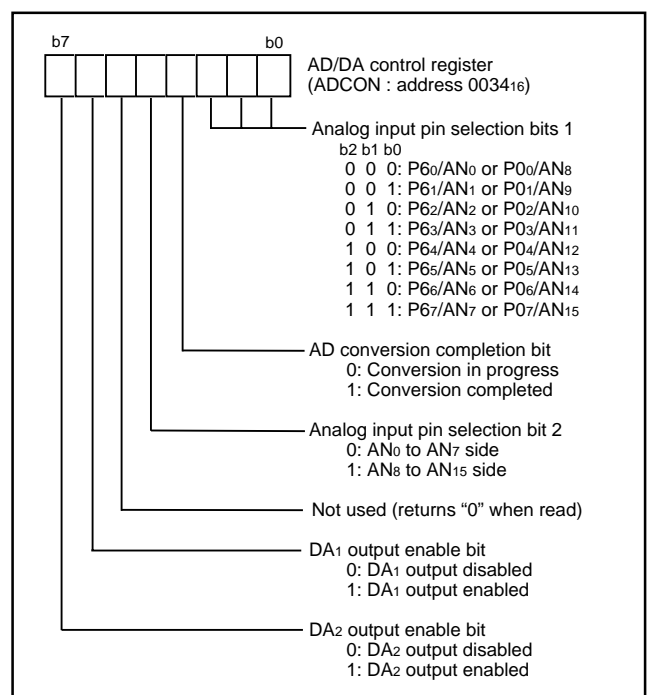


Fig. 49 Structure of AD/DA control register

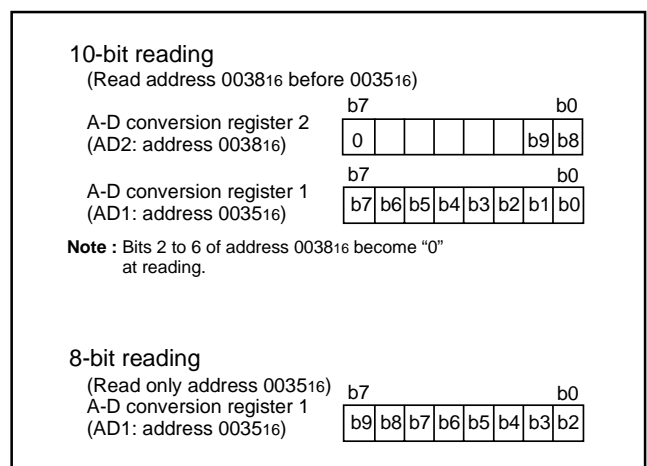


Fig. 50 Structure of 10-bit A-D mode reading



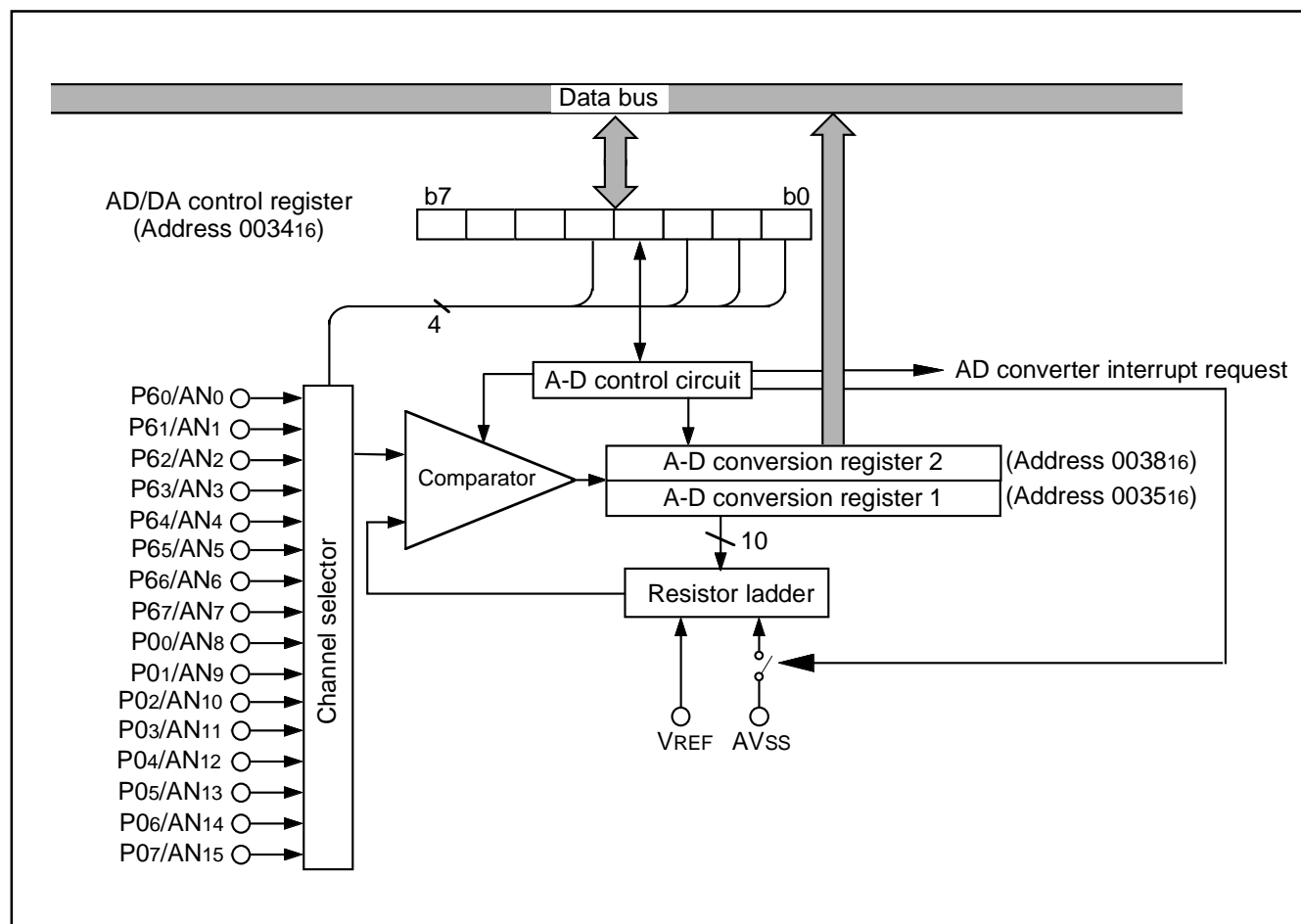


Fig. 51 Block diagram of A-D converter

## D-A CONVERTER

The 3803 group (Spec. H) has two internal D-A converters (DA1 and DA2) with 8-bit resolution.

The D-A conversion is performed by setting the value in each D-A conversion register. The result of D-A conversion is output from the DA1 or DA2 pin by setting the DA output enable bit to "1".

When using the D-A converter, the corresponding port direction register bit (P30/DA1 or P31/DA2) must be set to "0" (input status). The output analog voltage  $V$  is determined by the value  $n$  (decimal notation) in the D-A conversion register as follows:

$$V = V_{REF} \times n/256 \quad (n = 0 \text{ to } 255)$$

Where  $V_{REF}$  is the reference voltage.

At reset, the D-A conversion registers are cleared to "0016", and the DA output enable bits are cleared to "0", and the P30/DA1 and P31/DA2 pins become high impedance.

The DA output does not have buffers. Accordingly, connect an external buffer when driving a low-impedance load.

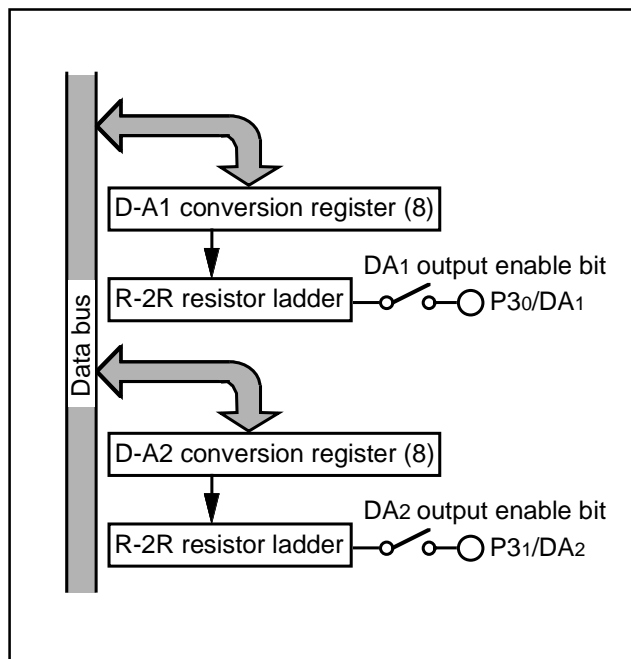


Fig. 52 Block diagram of D-A converter

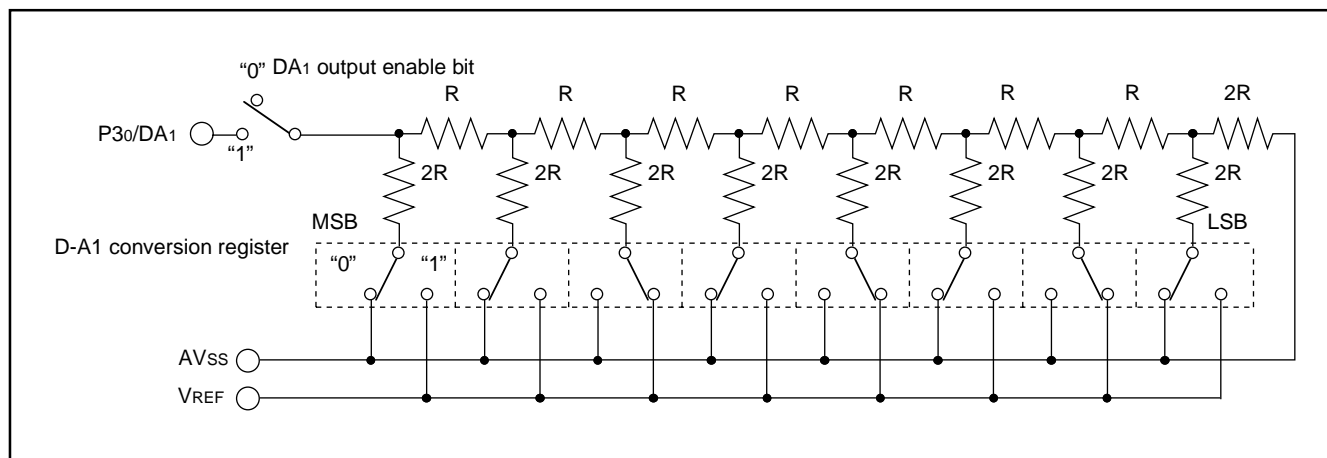


Fig. 53 Equivalent connection circuit of D-A converter (DA1)

## WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

### Watchdog Timer Initial Value

Watchdog timer L is set to "FF<sub>16</sub>" and watchdog timer H is set to "FF<sub>16</sub>" by writing to the watchdog timer control register (address 001E<sub>16</sub>) or at a reset. Any write instruction that causes a write signal can be used, such as the STA, LDM, CLB, etc. Data can only be written to bits 6 and 7 of the watchdog timer control register. Regardless of the value written to bits 0 to 5, the above-mentioned value will be set to each timer.

### Watchdog Timer Operations

The watchdog timer stops at reset and a countdown is started by the writing to the watchdog timer control register. An internal reset occurs when watchdog timer H underflows. The reset is released after its release time. After the release, the program is restarted from the reset vector address. Usually, write to the watchdog timer control register by software before an underflow of the watchdog timer H. The watchdog timer does not function if the watchdog timer control register is not written to at least once.

When bit 6 of the watchdog timer control register is kept at "0", the STP instruction is enabled. When that is executed, both the clock and the watchdog timer stop. Count re-starts at the same time as the release of stop mode (**Note**). The watchdog timer does not stop while a WIT instruction is executed. In addition, the STP instruction is disabled by writing "1" to this bit again. When the STP instruction is executed at this time, it is processed as an undefined instruction, and an internal reset occurs. Once a "1" is written to this bit, it cannot be programmed to "0" again.

The following shows the period between the write execution to the watchdog timer control register and the underflow of watchdog timer H.

Bit 7 of the watchdog timer control register is "0":

when  $X_{CIN} = 32.768 \text{ kHz}$ ; 32 s

when  $X_{IN} = 16 \text{ MHz}$ ; 65.536 ms

Bit 7 of the watchdog timer control register is "1":

when  $X_{CIN} = 32.768 \text{ kHz}$ ; 125 ms

when  $X_{IN} = 16 \text{ MHz}$ ; 256  $\mu\text{s}$

**Note:** The watchdog timer continues to count even while waiting for a stop release. Therefore, make sure that watchdog timer H does not underflow during this period.

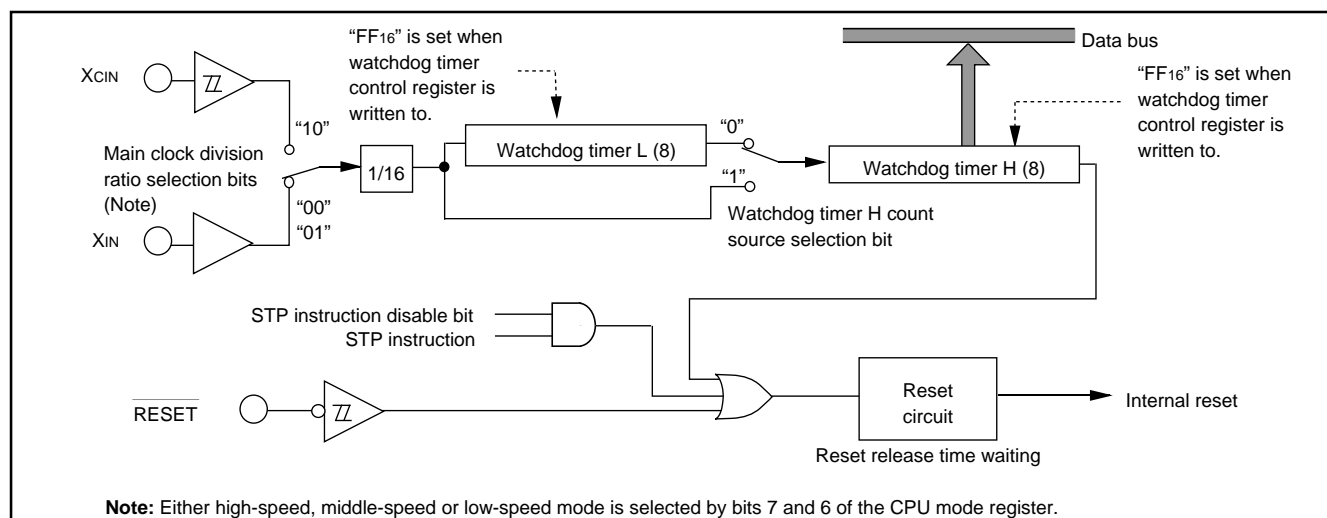


Fig. 54 Block diagram of Watchdog timer

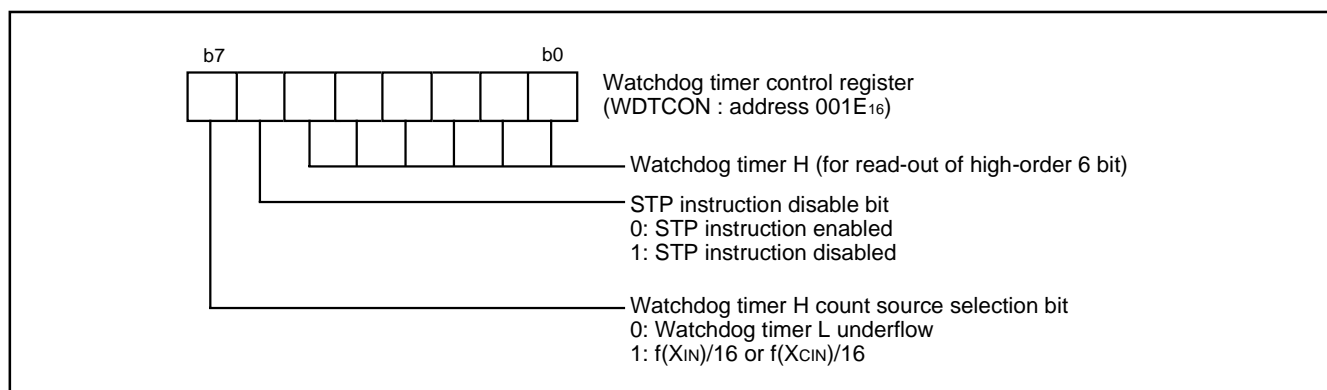


Fig. 55 Structure of Watchdog timer control register

## RESET CIRCUIT

To reset the microcomputer,  $\overline{\text{RESET}}$  pin should be held at an "L" level for 16 cycles or more of  $X_{IN}$ . Then the  $\overline{\text{RESET}}$  pin is returned to an "H" level (the power source voltage should be between 1.8 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address  $\text{FFFD}_{16}$  (high-order byte) and address  $\text{FFFC}_{16}$  (low-order byte). Make sure that the reset input voltage is less than 0.36 V for  $V_{CC}$  of 1.8 V.

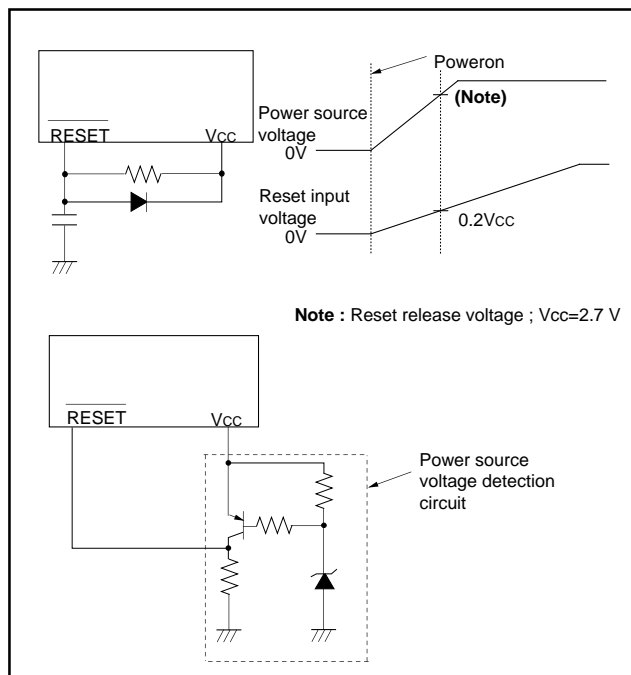


Fig. 56 Reset circuit example

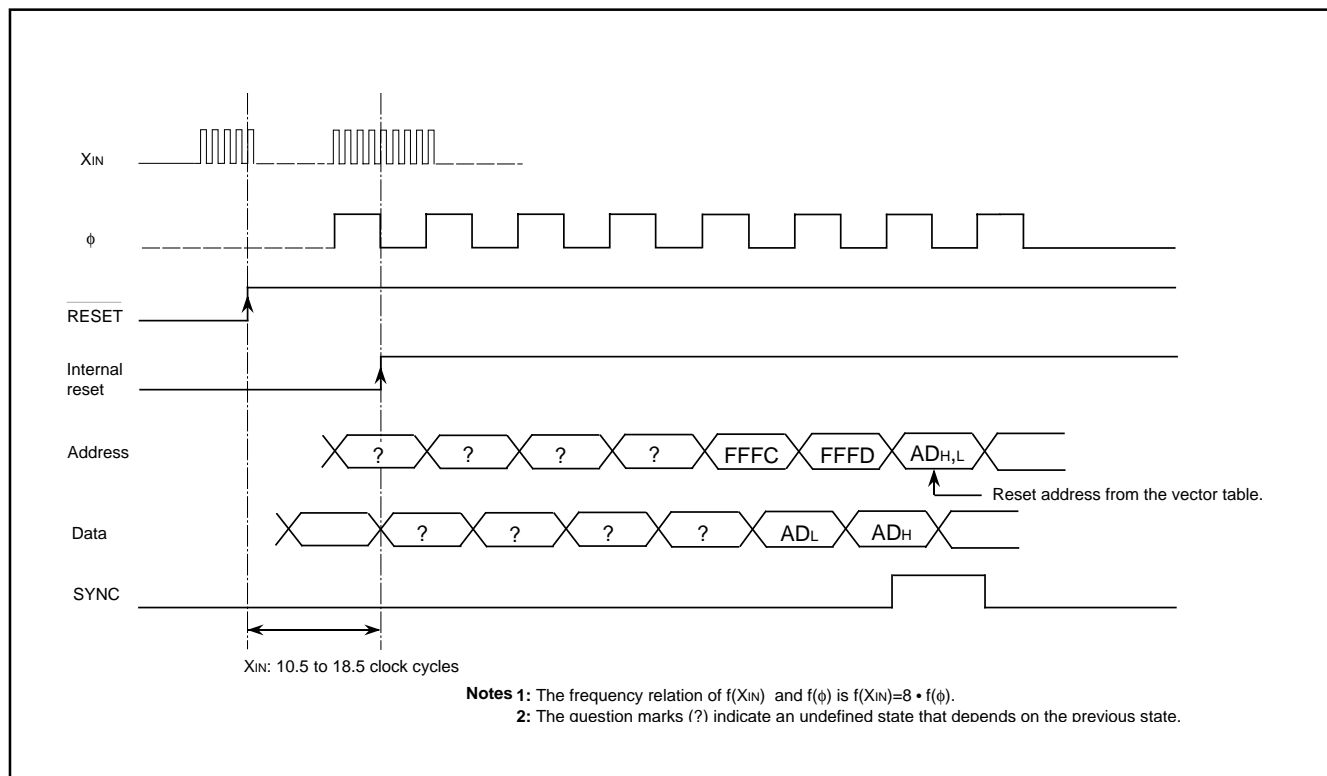


Fig. 57 Reset sequence

Address		Register contents	Address		Register contents
(1)	Port P0 (P0)	0000 <sub>16</sub> 00 <sub>16</sub>	(34)	Timer Z (low-order) (TZL)	0028 <sub>16</sub> FF <sub>16</sub>
(2)	Port P0 direction register (P0D)	0001 <sub>16</sub> 00 <sub>16</sub>	(35)	Timer Z (high-order) (TZH)	0029 <sub>16</sub> FF <sub>16</sub>
(3)	Port P1 (P1)	0002 <sub>16</sub> 00 <sub>16</sub>	(36)	Timer Z mode register (TZM)	002A <sub>16</sub> 00 <sub>16</sub>
(4)	Port P1 direction register (P1D)	0003 <sub>16</sub> 00 <sub>16</sub>	(37)	PWM control register (PWMCON)	002B <sub>16</sub> 00 <sub>16</sub>
(5)	Port P2 (P2)	0004 <sub>16</sub> 00 <sub>16</sub>	(38)	PWM prescaler (PREPWM)	002C <sub>16</sub> XXXXXXXX
(6)	Port P2 direction register (P2D)	0005 <sub>16</sub> 00 <sub>16</sub>	(39)	PWM register (PWM)	002D <sub>16</sub> XXXXXXXX
(7)	Port P3 (P3)	0006 <sub>16</sub> 00 <sub>16</sub>	(40)	Baud rate generator 3 (BRG3)	002F <sub>16</sub> XXXXXXXX
(8)	Port P3 direction register (P3D)	0007 <sub>16</sub> 00 <sub>16</sub>	(41)	Transmit/Receive buffer register 3 (TB3/RB3)	0030 <sub>16</sub> XXXXXXXX
(9)	Port P4 (P4)	0008 <sub>16</sub> 00 <sub>16</sub>	(42)	Serial I/O3 status register (SIO3STS)	0031 <sub>16</sub> 10000000
(10)	Port P4 direction register (P4D)	0009 <sub>16</sub> 00 <sub>16</sub>	(43)	Serial I/O3 control register (SIO3CON)	0032 <sub>16</sub> 00 <sub>16</sub>
(11)	Port P5 (P5)	000A <sub>16</sub> 00 <sub>16</sub>	(44)	UART3 control register (UART3CON)	0033 <sub>16</sub> 11100000
(12)	Port P5 direction register (P5D)	000B <sub>16</sub> 00 <sub>16</sub>	(45)	AD/DA control register (ADCON)	0034 <sub>16</sub> 00001000
(13)	Port P6 (P6)	000C <sub>16</sub> 00 <sub>16</sub>	(46)	A-D conversion register 1 (AD1)	0035 <sub>16</sub> XXXXXXXX
(14)	Port P6 direction register (P6D)	000D <sub>16</sub> 00 <sub>16</sub>	(47)	D-A1 conversion register (DA1)	0036 <sub>16</sub> 00 <sub>16</sub>
(15)	Timer 12, X count source selection register (T12XCSS)	000E <sub>16</sub> 00110011	(48)	D-A2 conversion register (DA2)	0037 <sub>16</sub> 00 <sub>16</sub>
(16)	Timer Y, Z count source selection register (TYZCSS)	000F <sub>16</sub> 00110011	(49)	A-D conversion register 2 (AD2)	0038 <sub>16</sub> 0000000X
(17)	MISRG	0010 <sub>16</sub> 00 <sub>16</sub>	(50)	Interrupt source selection register (INTSEL)	0039 <sub>16</sub> 00 <sub>16</sub>
(18)	Transmit/Receive buffer register 1 (TB1/RB1)	0018 <sub>16</sub> XXXXXXXX	(51)	Interrupt edge selection register (INTEDGE)	003A <sub>16</sub> 00 <sub>16</sub>
(19)	Serial I/O1 status register (SIO1STS)	0019 <sub>16</sub> 10000000	(52)	CPU mode register (CPUM)	003B <sub>16</sub> 01001000
(20)	Serial I/O1 control register (SIO1CON)	001A <sub>16</sub> 00 <sub>16</sub>	(53)	Interrupt request register 1 (IREQ1)	003C <sub>16</sub> 00 <sub>16</sub>
(21)	UART1 control register (UART1CON)	001B <sub>16</sub> 11100000	(54)	Interrupt request register 2 (IREQ2)	003D <sub>16</sub> 00 <sub>16</sub>
(22)	Baud rate generator 1 (BRG1)	001C <sub>16</sub> XXXXXXXX	(55)	Interrupt control register 1 (ICON1)	003E <sub>16</sub> 00 <sub>16</sub>
(23)	Serial I/O2 control register (SIO2CON)	001D <sub>16</sub> 00 <sub>16</sub>	(56)	Interrupt control register 2 (ICON2)	003F <sub>16</sub> 00 <sub>16</sub>
(24)	Watchdog timer control register (WDTCON)	001E <sub>16</sub> 00111111	(57)	Port P0 pull-up control register (PULL0)	0FF0 <sub>16</sub> 00 <sub>16</sub>
(25)	Serial I/O2 register (SIO2)	001F <sub>16</sub> XXXXXXXX	(58)	Port P1 pull-up control register (PULL1)	0FF1 <sub>16</sub> 00 <sub>16</sub>
(26)	Prescaler 12 (PRE12)	0020 <sub>16</sub> FF <sub>16</sub>	(59)	Port P2 pull-up control register (PULL2)	0FF2 <sub>16</sub> 00 <sub>16</sub>
(27)	Timer 1 (T1)	0021 <sub>16</sub> 01 <sub>16</sub>	(60)	Port P3 pull-up control register (PULL3)	0FF3 <sub>16</sub> 00 <sub>16</sub>
(28)	Timer 2 (T2)	0022 <sub>16</sub> FF <sub>16</sub>	(61)	Port P4 pull-up control register (PULL4)	0FF4 <sub>16</sub> 00 <sub>16</sub>
(29)	Timer XY mode register (TM)	0023 <sub>16</sub> 00 <sub>16</sub>	(62)	Port P5 pull-up control register (PULL5)	0FF5 <sub>16</sub> 00 <sub>16</sub>
(30)	Prescaler X (PREX)	0024 <sub>16</sub> FF <sub>16</sub>	(63)	Port P6 pull-up control register (PULL6)	0FF6 <sub>16</sub> 00 <sub>16</sub>
(31)	Timer X (TX)	0025 <sub>16</sub> FF <sub>16</sub>	(64)	Processor status register (PS)	XXXXXXXX1XXX
(32)	Prescaler Y (PREY)	0026 <sub>16</sub> FF <sub>16</sub>	(65)	Program counter (PC <sub>H</sub> )	FFFD <sub>16</sub> contents
(33)	Timer Y (TY)	0027 <sub>16</sub> FF <sub>16</sub>		(PC <sub>L</sub> )	FFFC <sub>16</sub> contents

**Note** : X : Not fixed  
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 58 Internal status at reset

## CLOCK GENERATING CIRCUIT

The 3803 group (Spec. H) has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT. Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

## Frequency Control

### (1) Middle-speed mode

The internal clock  $\phi$  is the frequency of XIN divided by 8. After reset is released, this mode is selected.

### (2) High-speed mode

The internal clock  $\phi$  is half the frequency of XIN.

### (3) Low-speed mode

The internal clock  $\phi$  is half the frequency of XCIN.

### (4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

## Oscillation Control

### (1) Stop mode

If the STP instruction is executed, the internal clock  $\phi$  stops at an "H" level, and XIN and XCIN oscillators stop. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116." When the oscillation stabilizing time set after STP instruction released bit is "1," set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

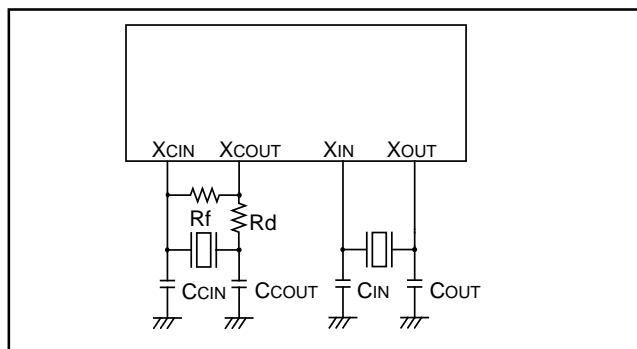
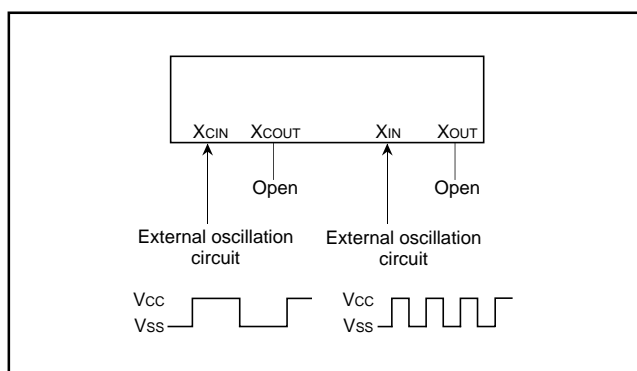
After STP instruction is released, the input of the prescaler 12 is connected to count source which had set at executing the STP instruction, and the output of the prescaler 12 is connected to timer 1. Set the timer 1 interrupt enable bit to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal clock  $\phi$  is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock  $\phi$  is supplied for the first time, when timer 1 underflows. Therefore make sure not to set the timer 1 interrupt request bit to "1" before the STP instruction stops the oscillator. When the oscillator is restarted by reset, apply "L" level to the  $\overline{\text{RESET}}$  pin until the oscillation is stable since a wait time will not be generated.

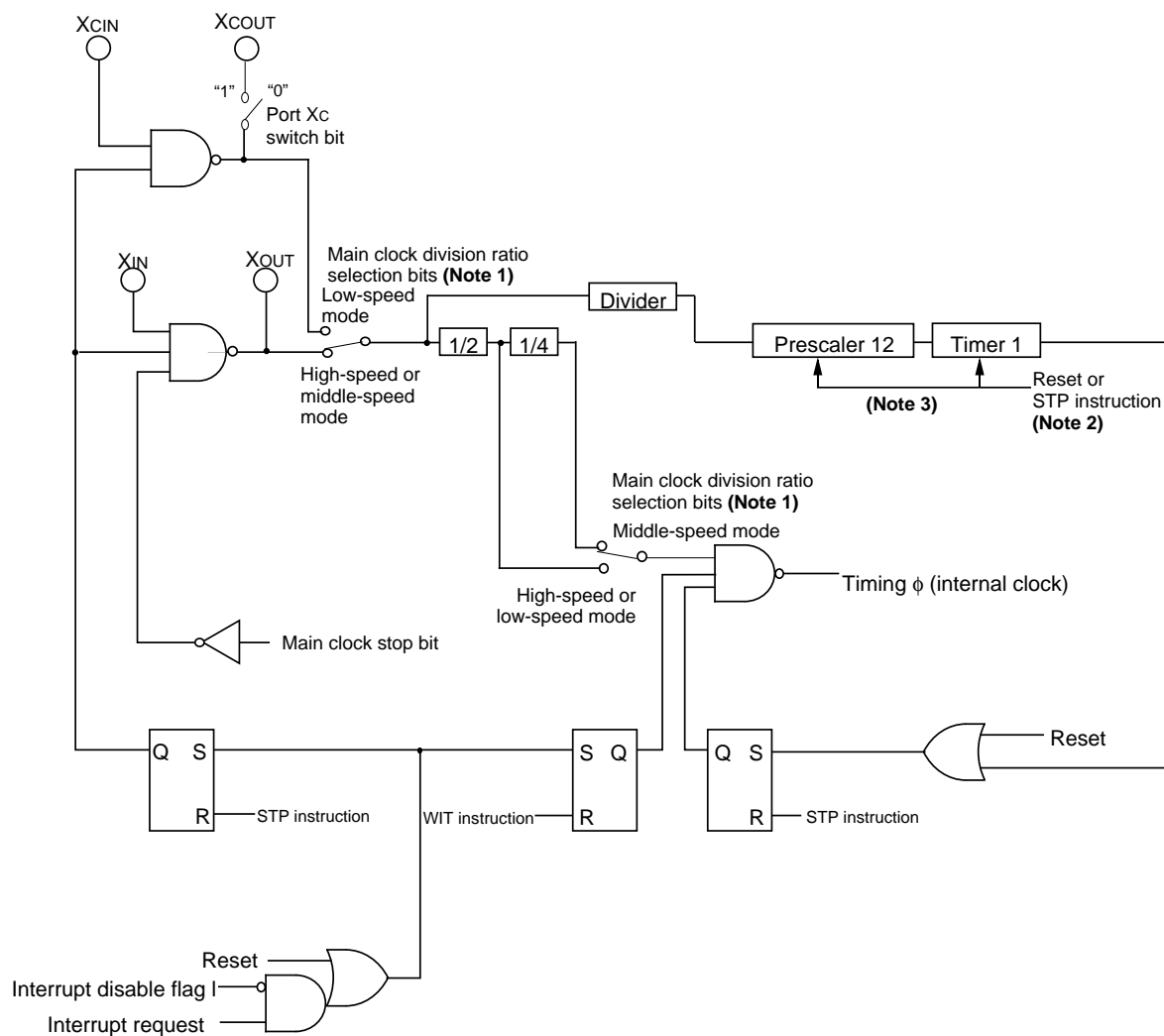
### (2) Wait mode

If the WIT instruction is executed, the internal clock  $\phi$  stops at an "H" level, but the oscillator does not stop. The internal clock  $\phi$  restarts when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

#### ■Note

- If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that  $f(\text{XIN}) > 3f(\text{XCIN})$ .
- When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.

**Fig. 59 Ceramic resonator circuit****Fig. 60 External clock input circuit**



**Notes 1:** Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register.

When low-speed mode is selected, set port Xc switch bit (b4) to “1”.

2: f(XIN)/16 is supplied as the count source to the prescaler 12 at reset. The count source before executing the STP instruction is supplied as the count source at executing STP instruction.

3: When bit 0 of MISRG is "0", timer 1 is set "0116" and prescaler 12 is set "FF16" automatically. When bit 0 of MISRG is "1", set the appropriate value to them in accordance with oscillation stabilizing time required by the using oscillator because nothing is automatically set into timer 1 and prescaler 12.

**Fig. 61 System clock generating circuit block diagram**



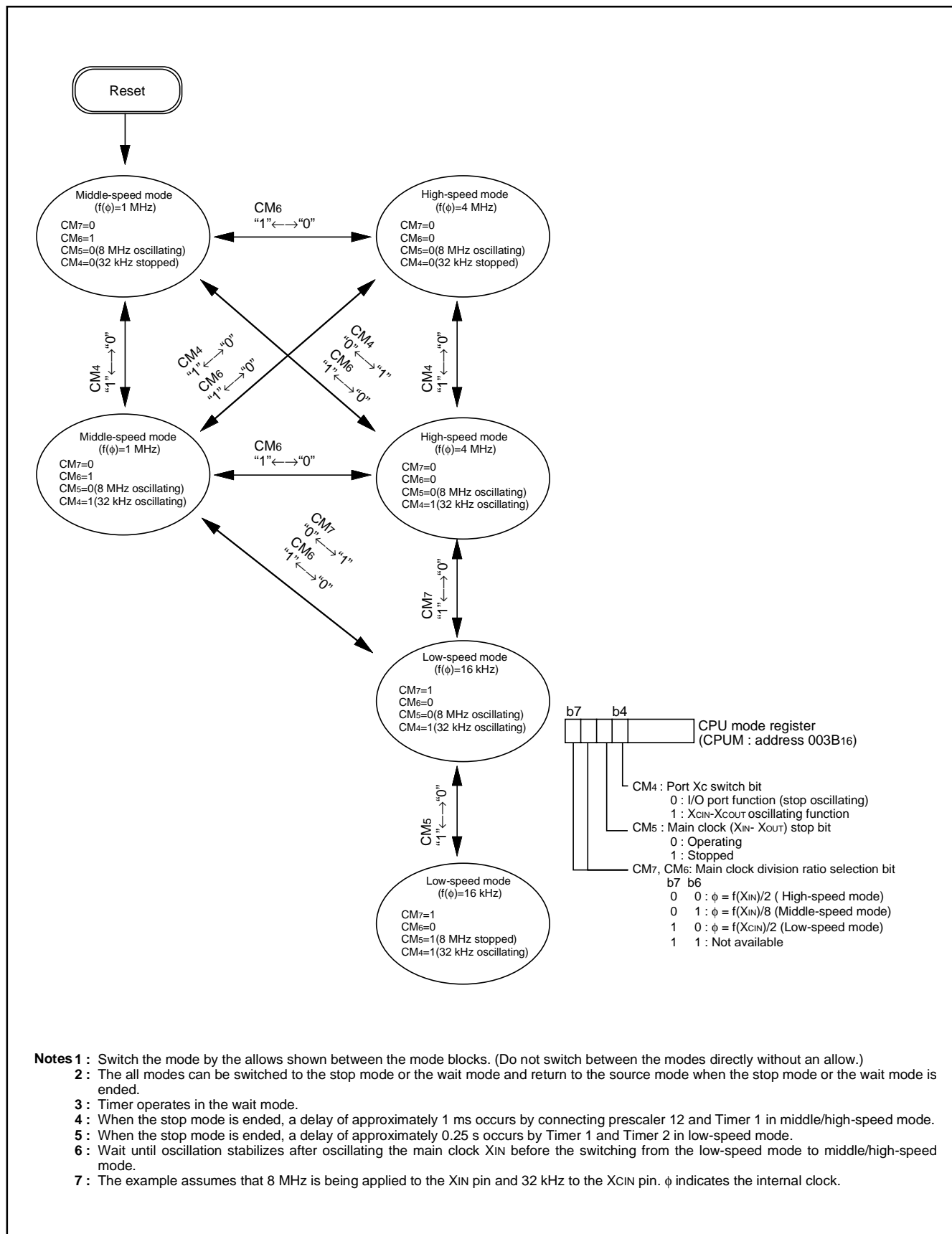


Fig. 62 State transitions of system clock

## NOTES ON USAGE

### Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin), and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01  $\mu$ F–0.1  $\mu$ F is recommended.

## ELECTRICAL CHARACTERISTICS

### Absolute maximum ratings

**Table 9 Absolute maximum ratings**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Power source voltages	All voltages are based on V <sub>SS</sub> . Output transistors are cut off.	−0.3 to 6.5	V
V <sub>I</sub>	Input voltage P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67, V <sub>REF</sub>		−0.3 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage P32, P33		−0.3 to 5.8	V
V <sub>I</sub>	Input voltage RESET, X <sub>IN</sub>		−0.3 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage CNV <sub>SS</sub>		−0.3 to V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67, X <sub>OUT</sub>		−0.3 to V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage P32, P33		−0.3 to 5.8	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	1000 <b>(Note)</b>	mW
T <sub>opr</sub>	Operating temperature		−20 to 85	°C
T <sub>stg</sub>	Storage temperature		−65 to 125	°C

**Note:** In flat package, this value is 300 mW.

## Recommended operating conditions

**Table 10 Recommended operating conditions**

(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	
			Min.	Typ.	Max.		
VCC	Power source voltage (Note 1)	When start oscillating (Note 2)		2.2	5.0	5.5	V
		High-speed mode f(φ) = f(XIN)/2	f(XIN) ≤ 2.1 MHz	2.0	5.0	5.5	V
			f(XIN) ≤ 4.2 MHz	2.2	5.0	5.5	V
			f(XIN) ≤ 8.4 MHz	2.7	5.0	5.5	V
			f(XIN) ≤ 12.5 MHz	4.0	5.0	5.5	V
			f(XIN) ≤ 16.8 MHz	4.5	5.0	5.5	V
		Middle-speed mode f(φ) = f(XIN)/8	f(XIN) ≤ 6.3 MHz	1.8	5.0	5.5	V
			f(XIN) ≤ 8.4 MHz	2.2	5.0	5.5	V
			f(XIN) ≤ 12.5 MHz	2.7	5.0	5.5	V
f(XIN) ≤ 16.8 MHz	4.5		5.0	5.5	V		
VSS	Power source voltage			0		V	
VIH	“H” input voltage P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67	1.8 ≤ VCC < 2.7 V	0.85VCC		VCC	V	
		2.7 ≤ VCC ≤ 5.5 V	0.8VCC		VCC	V	
VIH	“H” input voltage P32, P33	1.8 ≤ VCC < 2.7 V	0.85VCC		5.5	V	
		2.7 ≤ VCC ≤ 5.5 V	0.8VCC		5.5	V	
VIH	“H” input voltage RESET, XIN, XCIN, CNVSS	1.8 ≤ VCC < 2.7 V	0.85VCC		VCC	V	
		2.7 ≤ VCC ≤ 5.5 V	0.8VCC		VCC	V	
VIL	“L” input voltage P00–P07, P10–P17, P20–P27, P30–P37,P40–P47, P50–P57, P60–P67	1.8 ≤ VCC < 2.7 V	0		0.16VCC	V	
		2.7 ≤ VCC ≤ 5.5 V	0		0.2VCC	V	
VIL	“L” input voltage RESET, CNVSS	1.8 ≤ VCC < 2.7 V	0		0.16VCC	V	
		2.7 ≤ VCC ≤ 5.5 V	0		0.2VCC	V	
VIL	“L” input voltage XIN, XCIN	1.8 ≤ VCC ≤ 5.5 V	0		0.16VCC	V	

**Notes 1:** When using A-D converter, see A-D converter recommended operating conditions.

**2:** The start voltage and the start time for oscillation depend on the using oscillator, oscillation circuit constant value and operating temperature range, etc.. Particularly a high-frequency oscillator might require some notes in the low voltage operation.

**Table 11 Recommended operating conditions****(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0V, T<sub>a</sub> = –20 to 85 °C, unless otherwise noted)**

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
f(X <sub>IN</sub> )	Main clock input oscillation frequency ( <b>Note 1</b> )	High-speed mode f(φ) = f(X <sub>IN</sub> )/2	2.0 ≤ V <sub>CC</sub> < 2.2 V			$\frac{(20 \times V_{CC} - 36) \times 1.05}{2}$	MHz
			2.2 ≤ V <sub>CC</sub> < 2.7 V			$\frac{(24 \times V_{CC} - 40.8) \times 1.05}{3}$	MHz
			2.7 ≤ V <sub>CC</sub> < 4.0 V			$\frac{(9 \times V_{CC} - 0.3) \times 1.05}{3}$	MHz
			4.0 ≤ V <sub>CC</sub> < 4.5 V			$\frac{(24 \times V_{CC} - 60) \times 1.05}{3}$	MHz
			4.5 ≤ V <sub>CC</sub> ≤ 5.5 V			16.8	MHz
		Middle-speed mode f(φ) = f(X <sub>IN</sub> )/8	1.8 ≤ V <sub>CC</sub> < 2.2 V			$\frac{(15 \times V_{CC} - 9) \times 1.05}{3}$	MHz
			2.2 ≤ V <sub>CC</sub> < 2.7 V			$\frac{(24 \times V_{CC} - 28.8) \times 1.05}{3}$	MHz
			2.7 ≤ V <sub>CC</sub> < 4.5 V			$\frac{(15 \times V_{CC} + 39) \times 1.1}{7}$	MHz
			4.5 ≤ V <sub>CC</sub> ≤ 5.5 V			16.8	MHz
f(X <sub>CIN</sub> )	Sub-clock input oscillation frequency ( <b>Notes 1, 2</b> )				32.768	50	kHz

**Notes 1:** When the oscillation frequency has a duty cycle of 50%.**2:** When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that f(X<sub>CIN</sub>) < f(X<sub>IN</sub>)/3.

**Table 12 Recommended operating conditions**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0V, T<sub>a</sub> = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	"H" total peak output current P00–P07, P10–P17, P20–P27, P30, P31, P34–P37 <b>(Note 1)</b>			–80	mA
ΣIOH(peak)	"H" total peak output current P40–P47, P50–P57, P60–P67 <b>(Note 1)</b>			–80	mA
ΣIOL(peak)	"L" total peak output current P00–P07, P10–P17, P30–P37 <b>(Note 1)</b>			80	mA
ΣIOL(peak)	"L" total peak output current P20–P27 <b>(Note 1)</b>			80	mA
ΣIOL(peak)	"L" total peak output current P40–P47, P50–P57, P60–P67 <b>(Note 1)</b>			80	mA
ΣIOH(avg)	"H" total average output current P00–P07, P10–P17, P20–P27, P30, P31, P34–P37 <b>(Note 1)</b>			–40	mA
ΣIOH(avg)	"H" total average output current P40–P47, P50–P57, P60–P67 <b>(Note 1)</b>			–40	mA
ΣIOL(avg)	"L" total average output current P00–P07, P10–P17, P30–P37 <b>(Note 1)</b>			40	mA
ΣIOL(avg)	"L" total average output current P20–P27 <b>(Note 1)</b>			40	mA
ΣIOL(avg)	"L" total average output current P40–P47, P50–P57, P60–P67 <b>(Note 1)</b>			40	mA
IOH(peak)	"H" peak output current P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67 <b>(Note 2)</b>			–10	mA
IOL(peak)	"L" peak output current P00–P07, P10–P17, P30–P37, P40–P47, P50–P57, P60–P67 <b>(Note 2)</b>			10	mA
IOL(peak)	"L" peak output current P20–P27 <b>(Note 2)</b>			20	mA
IOH(avg)	"H" average output current P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67 <b>(Note 3)</b>			–5	mA
IOL(avg)	"L" average output current P00–P07, P10–P17, P30–P37, P40–P47, P50–P57, P60–P67 <b>(Note 3)</b>			5	mA
IOL(avg)	"L" average output current P20–P27 <b>(Note 3)</b>			10	mA

**Notes 1:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

**2:** The peak output current is the peak current flowing in each port.

**3:** The average output current IOL(avg), IOH(avg) are average value measured over 100 ms.

## Electrical characteristics

**Table 13 Electrical characteristics (1)**
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	“H” output voltage P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67 <b>(Note 1)</b>	IOH = -10 mA VCC = 4.0 to 5.5 V	VCC-2.0			V
		IOH = -1.0 mA VCC = 1.8 to 5.5 V	VCC-1.0			V
VOL	“L” output voltage P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P67	IOL = 10 mA VCC = 4.0 to 5.5 V			2.0	V
		IOL = 1.6 mA VCC = 1.8 to 5.5 V			1.0	V
VT+–VT–	Hysteresis CNTR0, CNTR1, CNTR2, INT0–INT4			0.4		V
VT+–VT–	Hysteresis RxD1, SCLK1, SIN2, SCLK2, RxD3, SCLK3			0.5		V
VT+–VT–	Hysteresis RESET			0.5		V
IiH	“H” input current P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P67	Vi = VCC (Pin floating. Pull-up transistors “off”)			5.0	μA
IiH	“H” input current RESET, CNVss	Vi = VCC			5.0	μA
IiH	“H” input current XIN	Vi = VCC		4.0		μA
IiL	“L” input current P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P67	Vi = VSS (Pin floating. Pull-up transistors “off”)			-5.0	μA
IiL	“L” input current RESET,CNVss	Vi = VSS			-5.0	μA
IiL	“L” input current XIN	Vi = VSS		-4.0		μA
IiL	“L” input current (at Pull-up) P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67	Vi = VSS VCC = 5.0 V	-80	-210	-420	μA
		Vi = VSS VCC = 3.0 V	-30	-70	-140	μA
VRAM	RAM hold voltage	When clock stopped	1.8		VCC	V

**Note 1:** P35 is measured when the P35/TxD3 P-channel output disable bit of the UART3 control register (bit 4 of address 003316) is “0”.  
P45 is measured when the P45/TxD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is “0”.

**Table 14 Electrical characteristics (2)**

(V<sub>CC</sub> = 1.8 to 5.5 V, T<sub>a</sub> = –20 to 85 °C, f(X<sub>CIN</sub>)=32.768kHz (Stoped in middle-speed mode), Output transistors “off”, AD converter not operated)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
ICC	Power source current	High-speed mode	VCC = 5V	f(XIN) = 16.8 MHz		8.0	15.0	mA
				f(XIN) = 12.5 MHz		6.5	12.0	mA
				f(XIN) = 8.4 MHz		5.0	9.0	mA
				f(XIN) = 4.2 MHz		2.5	5.0	mA
				f(XIN) = 16.8 MHz (in WIT state)		2.0	3.6	mA
			VCC = 3V	f(XIN) = 8.4 MHz		1.9	3.8	mA
				f(XIN) = 4.2 MHz		1.0	2.0	mA
				f(XIN) = 2.1 MHz		0.6	1.2	mA
				Middle-speed mode	VCC = 5V	f(XIN) = 16.8 MHz		4.0
		f(XIN) = 12.5 MHz				3.0	6.0	mA
		f(XIN) = 8.4 MHz				2.5	5.0	mA
		f(XIN) = 16.8 MHz (in WIT state)				1.8	3.3	mA
		VCC = 3V	f(XIN) = 12.5 MHz			1.5	3.0	mA
			f(XIN) = 8.4 MHz			1.2	2.4	mA
			f(XIN) = 6.3 MHz			1.0	2.0	mA
		Low-speed mode	VCC = 5V	f(XIN) = stopped		55	200	μA
				In WIT state		40	70	μA
			VCC = 3V	f(XIN) = stopped		15	40	μA
				In WIT state		8	15	μA
			VCC = 2V	f(XIN) = stopped		6	15	μA
				In WIT state		3	6	μA
				In STP state (All oscillation stopped)		Ta = 25 °C		0.1
		Ta = 85 °C					10	μA
		Increment when A-D conversion is executed		f(XIN) = 16.8 MHz, VCC = 5V In Middle-, high-speed mode			500	



## A-D converter characteristics

**Table 15 A-D converter recommended operating conditions**

(VCC = 2.0 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage (When A-D converter is used)	8-bit A-D mode ( <b>Note 1</b> )	2.0	5.0	5.5	V
		10-bit A-D mode ( <b>Note 2</b> )	2.2	5.0	5.5	
VREF	Analog reference voltage		2.0		VCC	V
AVSS	Analog power source voltage			0		V
VIA	Analog input voltage		0		VCC	V
f(XIN)	Main clock oscillation frequency (When A-D converter is used)	High-speed mode f(φ) = f(XIN)/2	2.0 ≤ VCC < 2.2 V	0.5	$\frac{(20 \times V_{CC} - 36) \times 1.05}{2}$	MHz
			2.2 ≤ VCC < 2.7 V	0.5	$\frac{(24 \times V_{CC} - 40.8) \times 1.05}{3}$	
			2.7 ≤ VCC < 4.0 V	0.5	$\frac{(9 \times V_{CC} - 0.3) \times 1.05}{3}$	
			4.0 ≤ VCC < 4.5 V	0.5	$\frac{(24 \times V_{CC} - 60) \times 1.05}{3}$	
			4.5 ≤ VCC ≤ 5.5 V	0.5	16.8	
		Middle-speed mode f(φ) = f(XIN)/8	2.0 ≤ VCC < 2.2 V	2.0	$\frac{(15 \times V_{CC} - 9) \times 1.05}{3}$	
			2.2 ≤ VCC < 2.7 V	2.0	$\frac{(24 \times V_{CC} - 28.8) \times 1.05}{3}$	
			2.7 ≤ VCC < 4.5 V	2.0	$\frac{(15 \times V_{CC} + 39) \times 1.1}{7}$	
			4.5 ≤ VCC ≤ 5.5 V	2.0	16.8	

**Note 1:** 8-bit A-D mode: When the conversion mode selection bit (bit 7 of address 003816) is "1".

**Note 2:** 10-bit A-D mode: When the conversion mode selection bit (bit 7 of address 003816) is "0".

**Table 16 A-D converter characteristics**

(VCC = 2.0 to 5.5 V, VSS = AVSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution	8-bit A-D mode ( <b>Note 1</b> )			8	bit
		10-bit A-D mode ( <b>Note 2</b> )			10	
–	Absolute accuracy (excluding quantization error)	8-bit A-D mode ( <b>Note 1</b> )	2.0 ≤ VCC < 2.2 V		±3	LSB
			2.2 ≤ VCC ≤ 5.5 V		±2	
		10-bit A-D mode ( <b>Note 2</b> )	2.2 ≤ VCC < 2.7 V		±5	
			2.7 ≤ VCC ≤ 5.5 V		±4	
tCONV	Conversion time	8-bit A-D mode ( <b>Note 1</b> )			50	2tc(XIN)
		10-bit A-D mode ( <b>Note 2</b> )			61	
RLADDER	Ladder resistor		12	35	100	kΩ
IVREF	Reference power	at A-D converter operated	VREF = 5.0 V	50	150	μA
	source input current	at A-D converter operated	VREF = 5.0 V		5	μA
II(AD)	A-D port inout current				5	μA

**Note 1:** 8-bit A-D mode: When the conversion mode selection bit (bit 7 of address 003816) is "1".

**Note 2:** 10-bit A-D mode: When the conversion mode selection bit (bit 7 of address 003816) is "0".

## D-A converter characteristics

**Table 17 D-A converter characteristics**

(VCC = 2.7 to 5.5 V, VREF = 2.7 V to VCC, VSS = AVSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	bit
–	Absolute accuracy	4.0 ≤ VCC ≤ 5.5 V			1.0	%
		2.7 ≤ VCC < 4.0 V			2.5	%
tsu	Setting time				3	μs
RO	Output resistor		2	3.5	5	kΩ
IVREF	Reference power source input current ( <b>Note 1</b> )				3.2	mA

**Note 1:** Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016".

## Timing requirements and switching characteristics

**Table 18 Timing requirements (1) (In high-speed mode)**  
**(V<sub>CC</sub> = 2.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width		16			XIN cycle
tc(XIN)	Main clock XIN input cycle time	4.5≤V <sub>CC</sub> ≤5.5 V	59.5			ns
		4.0≤V <sub>CC</sub> <4.5 V	10000/(86V <sub>CC</sub> -219)			
		2.7≤V <sub>CC</sub> <4.0 V	26×10 <sup>3</sup> /(82V <sub>CC</sub> -3)			
		2.2≤V <sub>CC</sub> <2.7 V	10000/(84V <sub>CC</sub> -143)			
		2.0≤V <sub>CC</sub> <2.2 V	10000/(105V <sub>CC</sub> -189)			
twh(XIN)	Main clock XIN input "H" pulse width	4.5≤V <sub>CC</sub> ≤5.5 V	25			ns
		4.0≤V <sub>CC</sub> <4.5 V	4000/(86V <sub>CC</sub> -219)			
		2.7≤V <sub>CC</sub> <4.0 V	10000/(82V <sub>CC</sub> -3)			
		2.2≤V <sub>CC</sub> <2.7 V	4000/(84V <sub>CC</sub> -143)			
		2.0≤V <sub>CC</sub> <2.2 V	4000/(105V <sub>CC</sub> -189)			
twL(XIN)	Main clock XIN input "L" pulse width	4.5≤V <sub>CC</sub> ≤5.5 V	25			ns
		4.0≤V <sub>CC</sub> <4.5 V	4000/(86V <sub>CC</sub> -219)			
		2.7≤V <sub>CC</sub> <4.0 V	10000/(82V <sub>CC</sub> -3)			
		2.2≤V <sub>CC</sub> <2.7 V	4000/(84V <sub>CC</sub> -143)			
		2.0≤V <sub>CC</sub> <2.2 V	4000/(105V <sub>CC</sub> -189)			
tc(XCIN)	Sub-clock XCIN input cycle time		20			μs
twh(XCIN)	Sub-clock XCIN input "H" pulse width		5			μs
twL(XCIN)	Sub-clock XCIN input "L" pulse width		5			μs
tc(CNTR)	CNTR0–CNTR2 input cycle time	4.5≤V <sub>CC</sub> ≤5.5 V	120			ns
		4.0≤V <sub>CC</sub> <4.5 V	160			
		2.7≤V <sub>CC</sub> <4.0 V	250			
		2.2≤V <sub>CC</sub> <2.7 V	500			
		2.0≤V <sub>CC</sub> <2.2 V	1000			
twh(CNTR)	CNTR0–CNTR2 input "H" pulse width	4.5≤V <sub>CC</sub> ≤5.5 V	48			ns
		4.0≤V <sub>CC</sub> <4.5 V	64			
		2.7≤V <sub>CC</sub> <4.0 V	115			
		2.2≤V <sub>CC</sub> <2.7 V	230			
		2.0≤V <sub>CC</sub> <2.2 V	460			
twL(CNTR)	CNTR0–CNTR2 input "L" pulse width	4.5≤V <sub>CC</sub> ≤5.5 V	48			ns
		4.0≤V <sub>CC</sub> <4.5 V	64			
		2.7≤V <sub>CC</sub> <4.0 V	115			
		2.2≤V <sub>CC</sub> <2.7 V	230			
		2.0≤V <sub>CC</sub> <2.2 V	460			
twh(INT)	INT00, INT01, INT1, INT2, INT3, INT40, INT41 input "H" pulse width	4.5≤V <sub>CC</sub> ≤5.5 V	48			ns
		4.0≤V <sub>CC</sub> <4.5 V	64			
		2.7≤V <sub>CC</sub> <4.0 V	115			
		2.2≤V <sub>CC</sub> <2.7 V	230			
		2.0≤V <sub>CC</sub> <2.2 V	460			
twL(INT)	INT00, INT01, INT1, INT2, INT3, INT40, INT41 input "L" pulse width	4.5≤V <sub>CC</sub> ≤5.5 V	48			ns
		4.0≤V <sub>CC</sub> <4.5 V	64			
		2.7≤V <sub>CC</sub> <4.0 V	115			
		2.2≤V <sub>CC</sub> <2.7 V	230			
		2.0≤V <sub>CC</sub> <2.2 V	460			

**Table 19 Timing requirements (2) (In high-speed mode)**  
**(Vcc = 2.0 to 5.5 V, Vss = 0 V, Ta = -20 to 85 °C, unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tc(SCLK1), tc(SCLK3)	Serial I/O1, serial I/O3 clock input cycle time <b>(Note)</b>	4.5≤Vcc≤5.5 V	250			ns
		4.0≤Vcc<4.5 V	320			
		2.7≤Vcc<4.0 V	500			
		2.2≤Vcc<2.7 V	1000			
		2.0≤Vcc<2.2 V	2000			
tWH(SCLK1), tWH(SCLK3)	Serial I/O1, serial I/O3 clock input "H" pulse width <b>(Note)</b>	4.5≤Vcc≤5.5 V	120			ns
		4.0≤Vcc<4.5 V	150			
		2.7≤Vcc<4.0 V	240			
		2.2≤Vcc<2.7 V	480			
		2.0≤Vcc<2.2 V	950			
tWL(SCLK1), tWL(SCLK3)	Serial I/O1, serial I/O3 clock input "L" pulse width <b>(Note)</b>	4.5≤Vcc≤5.5 V	120			ns
		4.0≤Vcc<4.5 V	150			
		2.7≤Vcc<4.0 V	240			
		2.2≤Vcc<2.7 V	480			
		2.0≤Vcc<2.2 V	950			
tsu(RxD1-SCLK1), tsu(RxD3-SCLK3)	Serial I/O1, serial I/O3 clock input setup time	4.5≤Vcc≤5.5 V	70			ns
		4.0≤Vcc<4.5 V	90			
		2.7≤Vcc<4.0 V	100			
		2.2≤Vcc<2.7 V	200			
		2.0≤Vcc<2.2 V	400			
th(SCLK1-RxD1), th(SCLK3-RxD3)	Serial I/O1, serial I/O3 clock input hold time	4.5≤Vcc≤5.5 V	32			ns
		4.0≤Vcc<4.5 V	40			
		2.7≤Vcc<4.0 V	50			
		2.2≤Vcc<2.7 V	100			
		2.0≤Vcc<2.2 V	200			
tc(SCLK2)	Serial I/O2 clock input cycle time	4.5≤Vcc≤5.5 V	500			ns
		4.0≤Vcc<4.5 V	650			
		2.7≤Vcc<4.0 V	1000			
		2.2≤Vcc<2.7 V	2000			
		2.0≤Vcc<2.2 V	4000			
tWH(SCLK2)	Serial I/O2 clock input "H" pulse width	4.5≤Vcc≤5.5 V	200			ns
		4.0≤Vcc<4.5 V	260			
		2.7≤Vcc<4.0 V	400			
		2.2≤Vcc<2.7 V	950			
		2.0≤Vcc<2.2 V	2000			
tWL(SCLK2)	Serial I/O2 clock input "L" pulse width	4.5≤Vcc≤5.5 V	200			ns
		4.0≤Vcc<4.5 V	260			
		2.7≤Vcc<4.0 V	400			
		2.2≤Vcc<2.7 V	950			
		2.0≤Vcc<2.2 V	2000			
tsu(SIN2-SCLK2)	Serial I/O2 clock input setup time	4.5≤Vcc≤5.5 V	100			ns
		4.0≤Vcc<4.5 V	130			
		2.7≤Vcc<4.0 V	200			
		2.2≤Vcc<2.7 V	400			
		2.0≤Vcc<2.2 V	800			
th(SCLK2-SIN2)	Serial I/O2 clock input hold time	4.5≤Vcc≤5.5 V	100			ns
		4.0≤Vcc<4.5 V	130			
		2.7≤Vcc<4.0 V	150			
		2.2≤Vcc<2.7 V	300			
		2.0≤Vcc<2.2 V	600			

**Note :** When bit 6 of address 001A16 and bit 6 of address 003216 are "1" (clock synchronous).  
Divide this value by four when bit 6 of address 001A16 and bit 6 of address 003216 are "0" (UART).

**Table 20 Timing requirements (3) (In middle-speed mode)****(VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width		16			XIN cycle
tc(XIN)	Main clock XIN input cycle time	4.5 ≤ VCC ≤ 5.5 V	59.5			ns
		2.7 ≤ VCC < 4.5 V	10000/(24VCC+61)			
		2.2 ≤ VCC < 2.7 V	10000/(82VCC-96)			
		1.8 ≤ VCC < 2.2 V	10000/(52VCC-31)			
tWH(XIN)	Main clock XIN input "H" pulse width	4.5 ≤ VCC ≤ 5.5 V	25			ns
		2.7 ≤ VCC < 4.5 V	4000/(24VCC+61)			
		2.2 ≤ VCC < 2.7 V	4000/(82VCC-96)			
		1.8 ≤ VCC < 2.2 V	4000/(52VCC-31)			
tWL(XIN)	Main clock XIN input "L" pulse width	4.5 ≤ VCC ≤ 5.5 V	25			ns
		2.7 ≤ VCC < 4.5 V	4000/(24VCC+61)			
		2.2 ≤ VCC < 2.7 V	4000/(82VCC-96)			
		1.8 ≤ VCC < 2.2 V	4000/(52VCC-31)			
tc(XCIN)	Sub-clock XCIN input cycle time		20			μs
tWH(XCIN)	Sub-clock XCIN input "H" pulse width		5			μs
tWL(XCIN)	Sub-clock XCIN input "L" pulse width		5			μs
tc(CNTR)	CNTR0–CNTR2 input cycle time	4.5 ≤ VCC ≤ 5.5 V	120			ns
		2.7 ≤ VCC < 4.5 V	160			
		2.2 ≤ VCC < 2.7 V	250			
		1.8 ≤ VCC < 2.2 V	320			
tWH(CNTR)	CNTR0–CNTR2 input "H" pulse width	4.5 ≤ VCC ≤ 5.5 V	48			ns
		2.7 ≤ VCC < 4.5 V	64			
		2.2 ≤ VCC < 2.7 V	115			
		1.8 ≤ VCC < 2.2 V	150			
tWL(CNTR)	CNTR0–CNTR2 input "L" pulse width	4.5 ≤ VCC ≤ 5.5 V	48			ns
		2.7 ≤ VCC < 4.5 V	64			
		2.2 ≤ VCC < 2.7 V	115			
		1.8 ≤ VCC < 2.2 V	150			
tWH(INT)	INT00, INT01, INT1, INT2, INT3, INT40, INT41 input "H" pulse width	4.5 ≤ VCC ≤ 5.5 V	48			ns
		2.7 ≤ VCC < 4.5 V	64			
		2.2 ≤ VCC < 2.7 V	115			
		1.8 ≤ VCC < 2.2 V	150			
tWL(INT)	INT00, INT01, INT1, INT2, INT3, INT40, INT41 input "L" pulse width	4.5 ≤ VCC ≤ 5.5 V	48			ns
		2.7 ≤ VCC < 4.5 V	64			
		2.2 ≤ VCC < 2.7 V	115			
		1.8 ≤ VCC < 2.2 V	150			

**Table 21 Timing requirements (4) (In middle-speed mode)**

(VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tc(SCLK1), tc(SCLK3)	Serial I/O1, serial I/O3 clock input cycle time <b>(Note)</b>	4.5≤VCC≤5.5 V	250			ns
		2.7≤VCC<4.5 V	320			
		2.2≤VCC<2.7 V	500			
		1.8≤VCC<2.2 V	650			
tWH(SCLK1), tWH(SCLK3)	Serial I/O1, serial I/O3 clock input "H" pulse width <b>(Note)</b>	4.5≤VCC≤5.5 V	120			ns
		2.7≤VCC<4.5 V	150			
		2.2≤VCC<2.7 V	240			
		1.8≤VCC<2.2 V	310			
tWL(SCLK1), tWL(SCLK3)	Serial I/O1, serial I/O3 clock input "L" pulse width <b>(Note)</b>	4.5≤VCC≤5.5 V	120			ns
		2.7≤VCC<4.5 V	150			
		2.2≤VCC<2.7 V	240			
		1.8≤VCC<2.2 V	310			
tsu(RxD1-SCLK1), tsu(RxD3-SCLK3)	Serial I/O1, serial I/O3 clock input setup time	4.5≤VCC≤5.5 V	70			ns
		2.7≤VCC<4.5 V	90			
		2.2≤VCC<2.7 V	100			
		1.8≤VCC<2.2 V	130			
th(SCLK1-RxD1), th(SCLK3-RxD3)	Serial I/O1, serial I/O3 clock input hold time	4.5≤VCC≤5.5 V	32			ns
		2.7≤VCC<4.5 V	40			
		2.2≤VCC<2.7 V	50			
		1.8≤VCC<2.2 V	65			
tc(SCLK2)	Serial I/O2 clock input cycle time	4.5≤VCC≤5.5 V	500			ns
		2.7≤VCC<4.5 V	650			
		2.2≤VCC<2.7 V	1000			
		1.8≤VCC<2.2 V	1300			
tWH(SCLK2)	Serial I/O2 clock input "H" pulse width	4.5≤VCC≤5.5 V	200			ns
		2.7≤VCC<4.5 V	260			
		2.2≤VCC<2.7 V	400			
		1.8≤VCC<2.2 V	520			
tWL(SCLK2)	Serial I/O2 clock input "L" pulse width	4.5≤VCC≤5.5 V	200			ns
		2.7≤VCC<4.5 V	260			
		2.2≤VCC<2.7 V	400			
		1.8≤VCC<2.2 V	520			
tsu(SIN2-SCLK2)	Serial I/O2 clock input setup time	4.5≤VCC≤5.5 V	100			ns
		2.7≤VCC<4.5 V	130			
		2.2≤VCC<2.7 V	200			
		1.8≤VCC<2.2 V	260			
th(SCLK2-SIN2)	Serial I/O2 clock input hold time	4.5≤VCC≤5.5 V	100			ns
		2.7≤VCC<4.5 V	130			
		2.2≤VCC<2.7 V	150			
		1.8≤VCC<2.2 V	200			

**Note :** When bit 6 of address 001A16 and bit 6 of address 003216 are "1" (clock synchronous).

Divide this value by four when bit 6 of address 001A16 and bit 6 of address 003216 are "0" (UART).

Timing diagram in single-chip mode

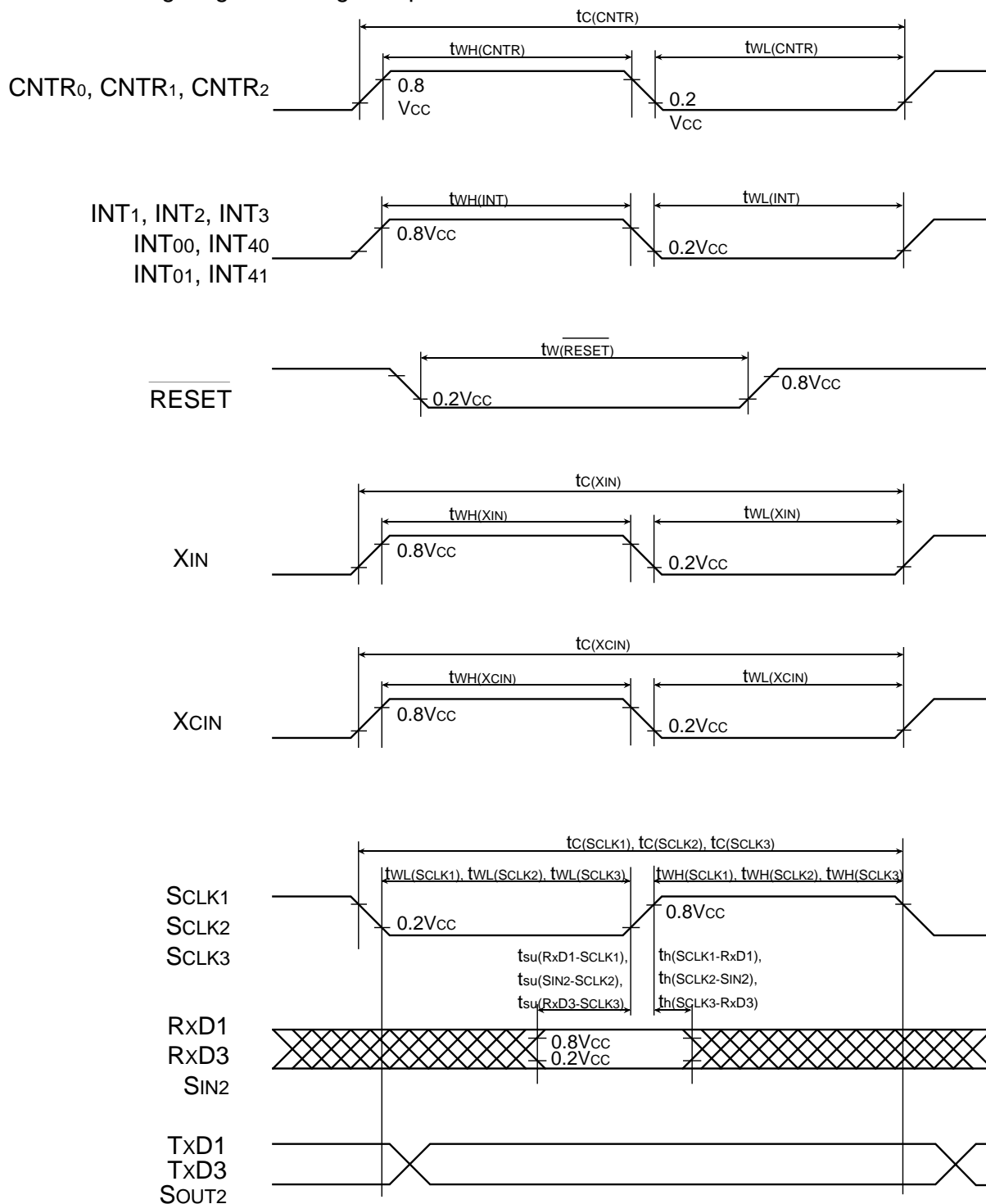


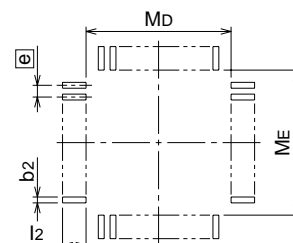
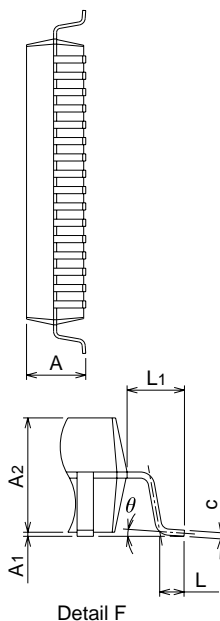
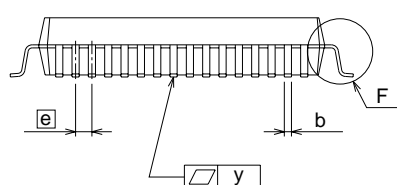
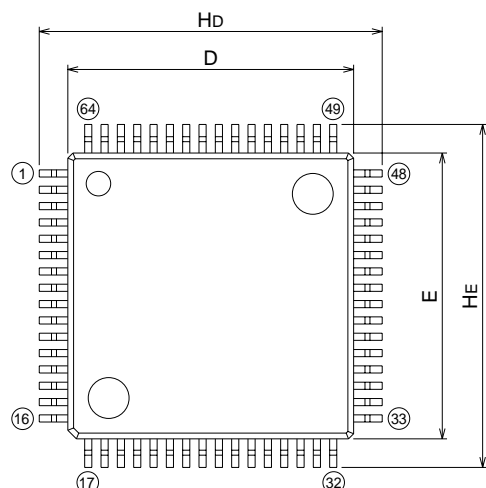
Fig. 63 Timing diagram (in single-chip mode)

## PACKAGE OUTLINE

### 64P6N-A

### Plastic 64pin 14X14mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP64-P-1414-0.80	—	1.11	Alloy 42



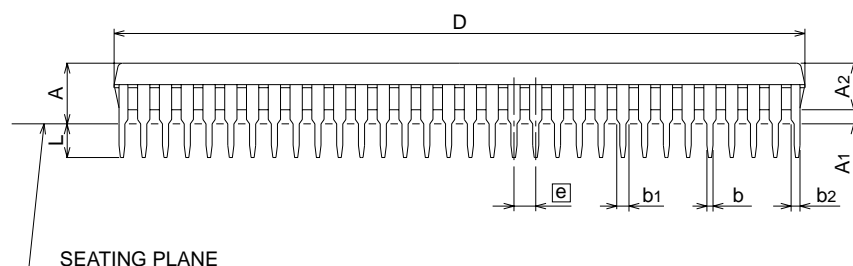
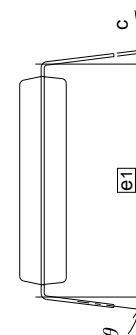
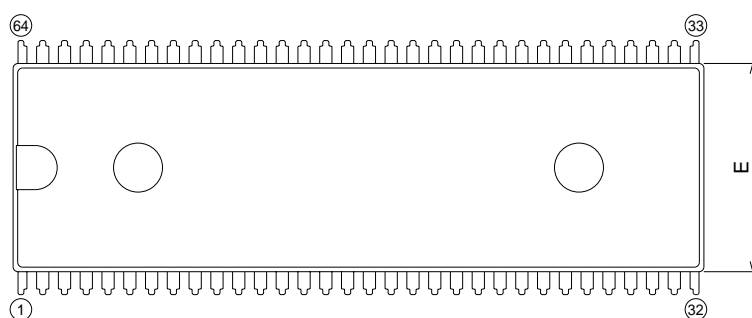
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e	—	0.8	—
HD	16.5	16.8	17.1
HE	16.5	16.8	17.1
L	0.4	0.6	0.8
L1	—	1.4	—
y	—	—	0.1
theta	0°	—	10°
b2	—	0.5	—
l2	1.3	—	—
MD	—	14.6	—
ME	—	14.6	—

### 64P4B

### Plastic 64pin 750mil SDIP

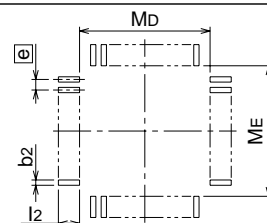
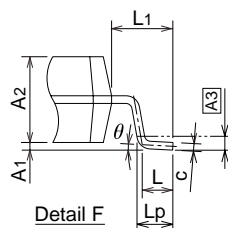
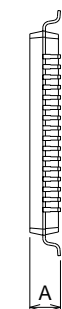
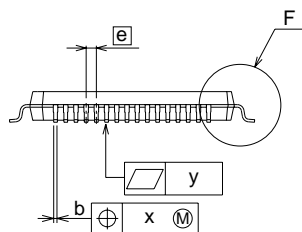
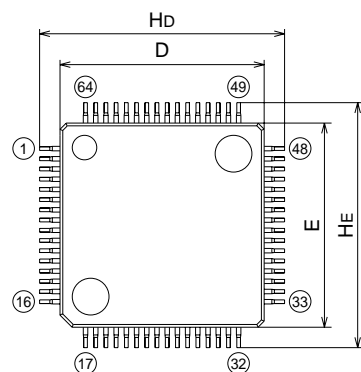
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP64-P-750-1.78	—	7.9	Alloy 42



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.08
A1	0.38	—	—
A2	—	3.8	—
b	0.4	0.5	0.6
b1	0.9	1.0	1.3
b2	0.65	0.75	1.05
c	0.2	0.25	0.32
D	56.2	56.4	56.6
E	16.85	17.0	17.15
e	—	1.778	—
e1	—	19.05	—
L	2.8	—	—
theta	0°	—	15°

**64P6Q-A** (MMP)**Plastic 64pin 10X10mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1010-0.50	—	—	Cu Alloy

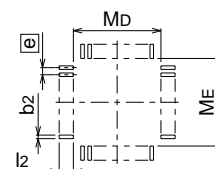
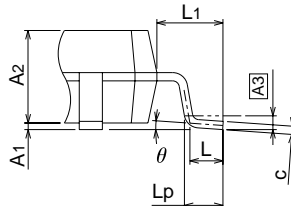
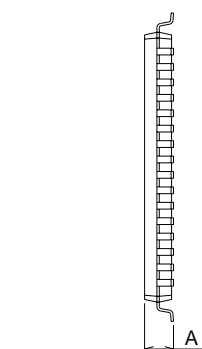
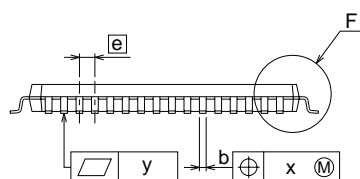
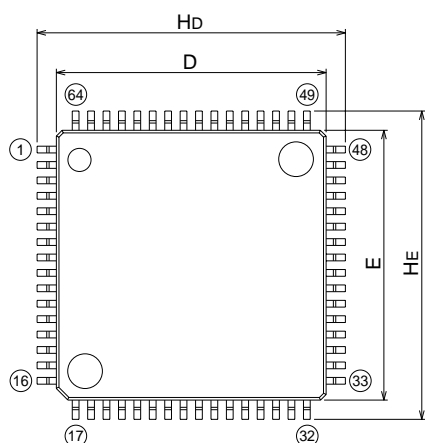


Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	—	0.5	—
Hd	11.8	12.0	12.2
HE	11.8	12.0	12.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
θ	0°	—	10°
b2	—	0.225	—
l2	1.0	—	—
MD	—	10.4	—
ME	—	10.4	—

**64P6U-A** (MMP)**Plastic 64pin 14X14mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP64-P-1414-0.8	—	—	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	—	0.8	—
Hd	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	8°
b2	—	0.225	—
l2	0.95	—	—
MD	—	14.4	—
ME	—	14.4	—



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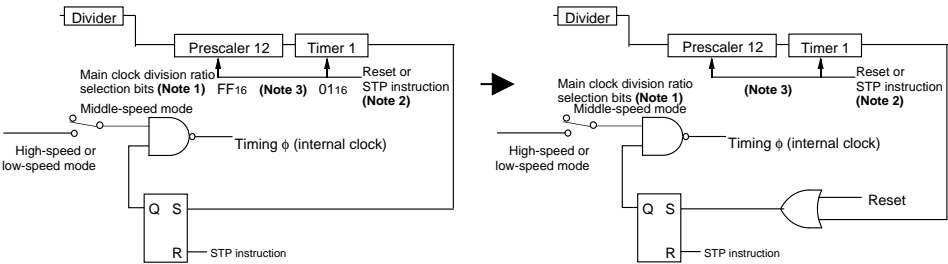


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# REVISION HISTORY

# 3803 Group (Spec.H) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 3, 2001	—	First edition issued
2.00	May. 28, 2003	1,2,6,7 5 7 23 64   68 69 73  75 75,77 76,78 79	<ul style="list-style-type: none"> <li>•Delete the following :“*:KP package is under development.”</li> <li>•Table 4 pin description Vcc,Vss Apply voltage of 2.7–5.5V → 1.8V–5.5V</li> <li>•Fig.5 Memory expansion plan As of Dec. 2002 → As of Mar. 2003</li> <li>•Notes (address 3A16) → (address 003A16), (address 2316) → (address 002316), (address 2A16) → (address 002A16), (address 3916) → (address 003916)</li> <li>•Fig.61 System clock generating circuit block diagram</li> </ul>  <ul style="list-style-type: none"> <li>•Table 10 Recommended operating conditions Add : VIL “L” input voltage XIN, XCIN 1.8≤VCC≤5.5V Min. → 0</li> <li>•Table 11 Recommended operating conditions f(XIN) High-speed mode f(φ)=f(XIN)/2 2.2≤VCC≤4.0V → 2.7≤VCC≤4.0V</li> <li>•Table 16 A-D converter characteristics VCC 8bit A-D mode, 10bit A-D mode Max. 5.0 → 5.5</li> <li>•Table 17 D-A converter characteristics VCC = 4.0 to 5.5V → 4.0≤VCC≤5.5V, VCC = 2.7 to 4.0V → 2.7≤VCC&lt;4.0V</li> <li>•Table 16 A-D converter characteristics, Table 17 D-A converter characteristics Resolution Unit Bits → bit</li> <li>•Table 18 Timing requirements (1) (In high-speed mode) tc(XIN) Main clock XIN input cycle time 2.7≤VCC&lt;4.0 Min. <math>2.6 \times 10^3 / (82V_{CC} - 3) \rightarrow 26 \times 10^3 / (82V_{CC} - 3)</math></li> <li>•Table 18 Timing requirements (1) (In high-speed mode), Table 20 Timing requirements (3) (In middle-speed mode) tWH(XCIN) Sub-clock input “H” pulse width → Sub-clock XCIN input “H” pulse width tWL(XCIN) Sub-clock input “L” pulse width → Sub-clock XCIN input “L” pulse width</li> <li>•Table 19 Timing requirements (2) (In high-speed mode), Table 20 Timing requirements (4) (In middle-speed mode) tCL(SCLK2) → tWL(SCLK2)</li> <li>•Fig.63 Timing diagram (in single-chip mode) Delete the following underline parts : SCLK1 SCLK2 SCLK3 <u>t<sub>f</sub>, t<sub>r</sub></u> TXD1 TXD3 SOUT2 <u>t<sub>d</sub>(SCLK1-TXD1), t<sub>d</sub>(SCLK2-SOUT2), t<sub>d</sub>(SCLK3-TXD3)</u> <u>t<sub>v</sub>(SCLK1-TXD1), t<sub>v</sub>(SCLK2-SOUT2), t<sub>v</sub>(SCLK3-TXD3)</u></li> </ul>