

# R1RW0408D Series

4M High Speed SRAM (512-kword  $\times$  8-bit)

REJ03C0111-0100Z

Rev. 1.00

Mar.12.2004

## Description

The R1RW0408D is a 4-Mbit high speed static RAM organized 512-kword  $\times$  8-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The R1RW0408D is packaged in 400-mil 36-pin SOJ for high density surface mounting.

## Features

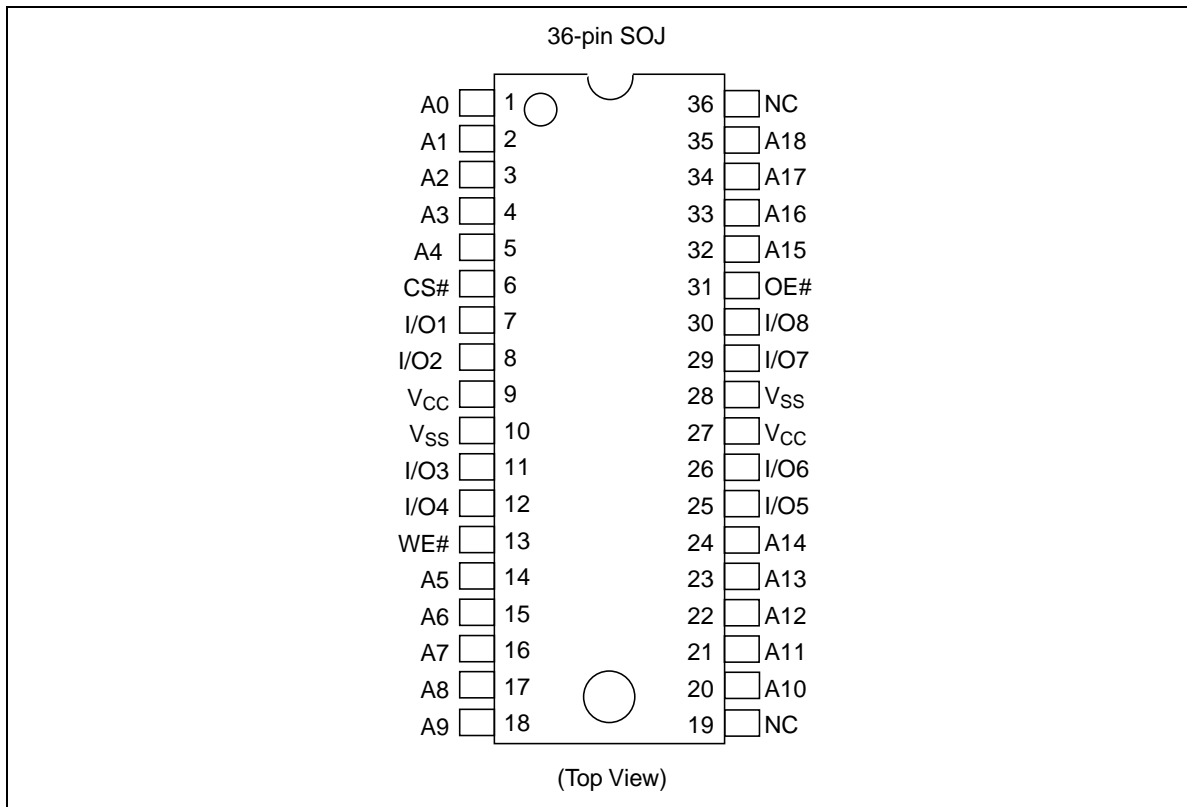
- Single supply: 3.3 V  $\pm$  0.3 V
- Access time: 12 ns (max)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - All inputs and outputs
- Operating current: 100 mA (max)
- TTL standby current: 40 mA (max)
- CMOS standby current: 5 mA (max)
  - : 0.8 mA (max) (L-version)
- Data retention current: 0.4 mA (max) (L-version)
- Data retention voltage: 2 V (min) (L-version)
- Center  $V_{CC}$  and  $V_{SS}$  type pin out

## R1RW0408D Series

### Ordering Information

Type No.	Access time	Package
R1RW0408DGE-2PR	12 ns	400-mil 36-pin plastic SOJ (36P0K)
R1RW0408DGE-2LR	12 ns	

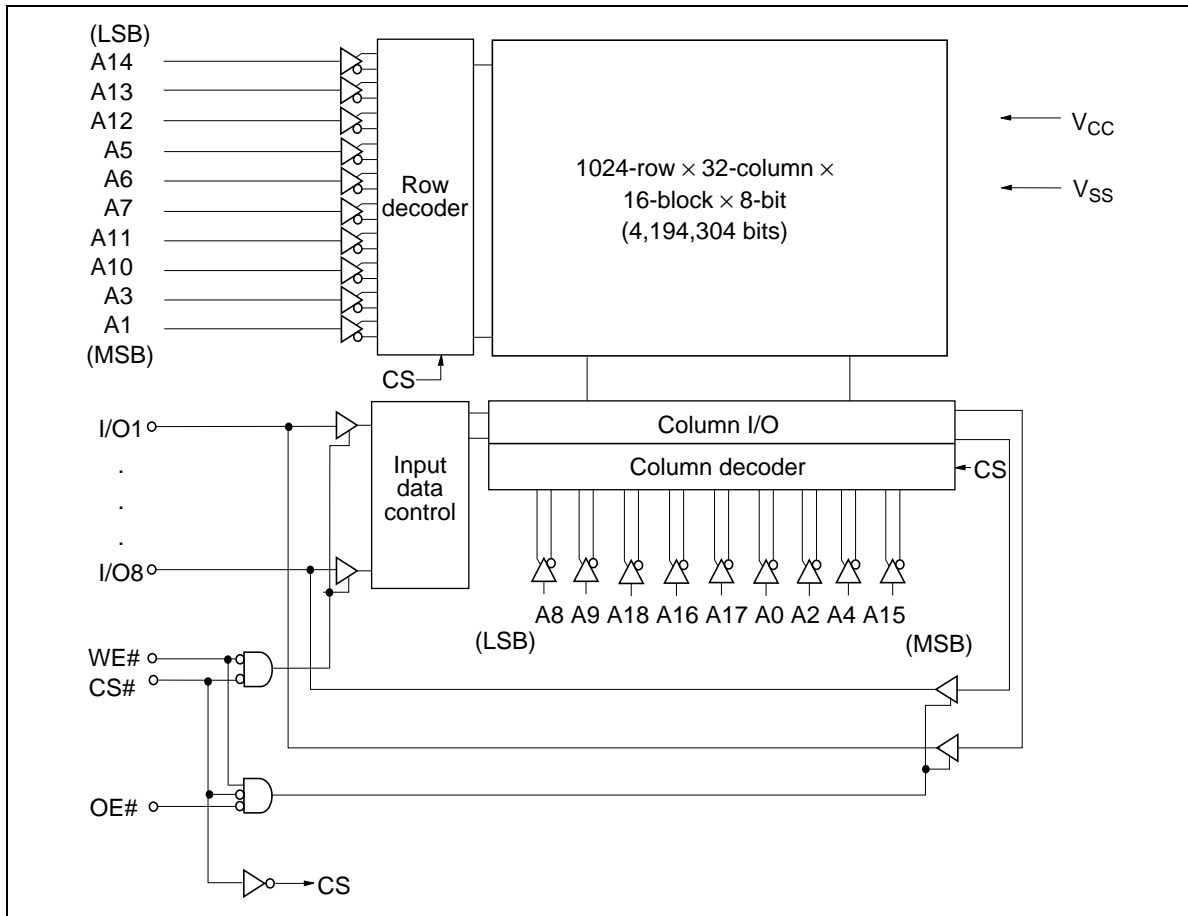
### Pin Arrangement



**Pin Description**

<b>Pin name</b>	<b>Function</b>
A0 to A18	Address input
I/O1 to I/O8	Data input/output
CS#	Chip select
OE#	Output enable
WE#	Write enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground
NC	No connection

## Block Diagram



## Operation Table

CS#	OE#	WE#	Mode	V <sub>CC</sub> current	I/O	Ref. cycle
H	×	×	Standby	I <sub>SB</sub> , I <sub>SB1</sub>	High-Z	—
L	H	H	Output disable	I <sub>CC</sub>	High-Z	—
L	L	H	Read	I <sub>CC</sub>	D <sub>OUT</sub>	Read cycle (1) to (3)
L	H	L	Write	I <sub>CC</sub>	D <sub>IN</sub>	Write cycle (1)
L	L	L	Write	I <sub>CC</sub>	D <sub>IN</sub>	Write cycle (2)

Note: H: V<sub>IH</sub>, L: V<sub>IL</sub>, ×: V<sub>IH</sub> or V<sub>IL</sub>

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V <sub>SS</sub>	V <sub>CC</sub>	−0.5 to +4.6	V
Voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	−0.5* <sup>1</sup> to V <sub>CC</sub> + 0.5* <sup>2</sup>	V
Power dissipation	P <sub>T</sub>	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Notes: 1. V<sub>T</sub> (min) = −2.0 V for pulse width (under shoot) ≤ 6 ns.  
 2. V<sub>T</sub> (max) = V<sub>CC</sub> + 2.0 V for pulse width (over shoot) ≤ 6 ns.

## Recommended DC Operating Conditions

(Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub> * <sup>3</sup>	3.0	3.3	3.6	V
	V <sub>SS</sub> * <sup>4</sup>	0	0	0	V
Input voltage	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> + 0.5* <sup>2</sup>	V
	V <sub>IL</sub>	−0.5* <sup>1</sup>	—	0.8	V

Notes: 1. V<sub>IL</sub> (min) = −2.0 V for pulse width (under shoot) ≤ 6 ns.  
 2. V<sub>IH</sub> (max) = V<sub>CC</sub> + 2.0 V for pulse width (over shoot) ≤ 6 ns.  
 3. The supply voltage with all V<sub>CC</sub> pins must be on the same level.  
 4. The supply voltage with all V<sub>SS</sub> pins must be on the same level.

## DC Characteristics

(Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	2	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	2	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operation power supply current	I <sub>CC</sub>	—	100	mA	Min cycle CS# = V <sub>IL</sub> , I <sub>OUT</sub> = 0 mA Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
Standby power supply current	I <sub>SB</sub>	—	40	mA	Min cycle CS# = V <sub>IH</sub> , Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
	I <sub>SB1</sub>	—	5	mA	f = 0 MHz V <sub>CC</sub> ≥ CS# ≥ V <sub>CC</sub> - 0.2 V, (1) 0 V ≤ V <sub>IN</sub> ≤ 0.2 V or (2) V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V
	—* <sup>1</sup>	—	0.8* <sup>1</sup>	mA	
Output voltage	V <sub>OL</sub>	—	0.4	V	I <sub>OL</sub> = 8 mA
	V <sub>OH</sub>	2.4	—	V	I <sub>OH</sub> = -4 mA

Note: 1. This characteristics is guaranteed only for L-version.

## Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance* <sup>1</sup>	C <sub>IN</sub>	—	6	pF	V <sub>IN</sub> = 0 V
Input/output capacitance* <sup>1</sup>	C <sub>I/O</sub>	—	8	pF	V <sub>I/O</sub> = 0 V

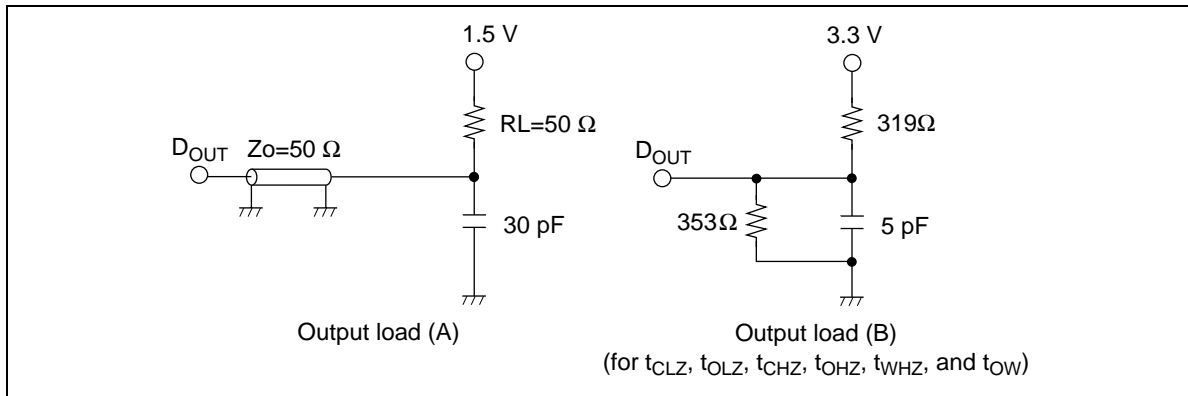
Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ , unless otherwise noted.)

### Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



### Read Cycle

R1RW0408D					
-2					
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	$t_{RC}$	12	—	ns	
Address access time	$t_{AA}$	—	12	ns	
Chip select access time	$t_{ACS}$	—	12	ns	
Output enable to output valid	$t_{OE}$	—	6	ns	
Output hold from address change	$t_{OH}$	3	—	ns	
Chip select to output in low-Z	$t_{CLZ}$	3	—	ns	1
Output enable to output in low-Z	$t_{OLZ}$	0	—	ns	1
Chip deselect to output in high-Z	$t_{CHZ}$	—	6	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	6	ns	1

## Write Cycle

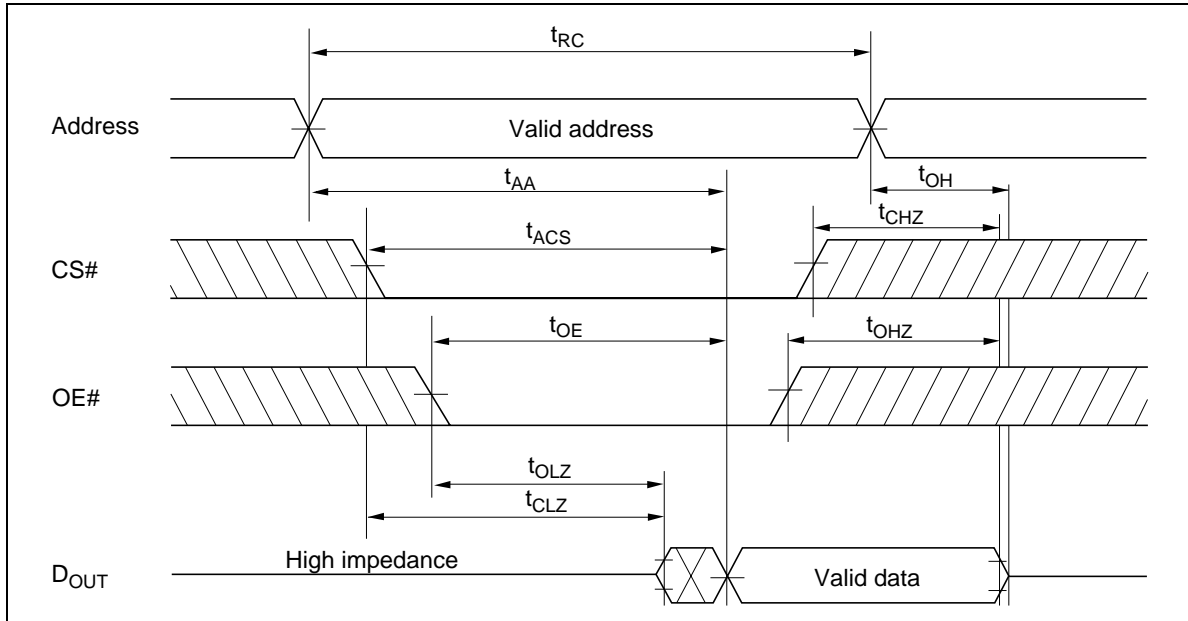
R1RW0408D					
-2					
Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	$t_{WC}$	12	—	ns	
Address valid to end of write	$t_{AW}$	8	—	ns	
Chip select to end of write	$t_{CW}$	8	—	ns	9
Write pulse width	$t_{WP}$	8	—	ns	8
Address setup time	$t_{AS}$	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	ns	7
Data to write time overlap	$t_{DW}$	6	—	ns	
Data hold from write time	$t_{DH}$	0	—	ns	
Write disable to output in low-Z	$t_{OW}$	3	—	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	6	ns	1
Write enable to output in high-Z	$t_{WHZ}$	—	6	ns	1

- Notes:
1. Transition is measured  $\pm 200$  mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.
  2. Address should be valid prior to or coincident with CS# transition low.
  3. WE# and/or CS# must be high during address transition time.
  4. If CS# and OE# are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
  5. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, output remains a high impedance state.
  6.  $t_{AS}$  is measured from the latest address transition to the later of CS# or WE# going low.
  7.  $t_{WR}$  is measured from the earlier of CS# or WE# going high to the first address transition.
  8. A write occurs during the overlap of a low CS# and a low WE#. A write begins at the latest transition among CS# going low and WE# going low. A write ends at the earliest transition among CS# going high and WE# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  9.  $t_{CW}$  is measured from the later of CS# going low to the end of write.

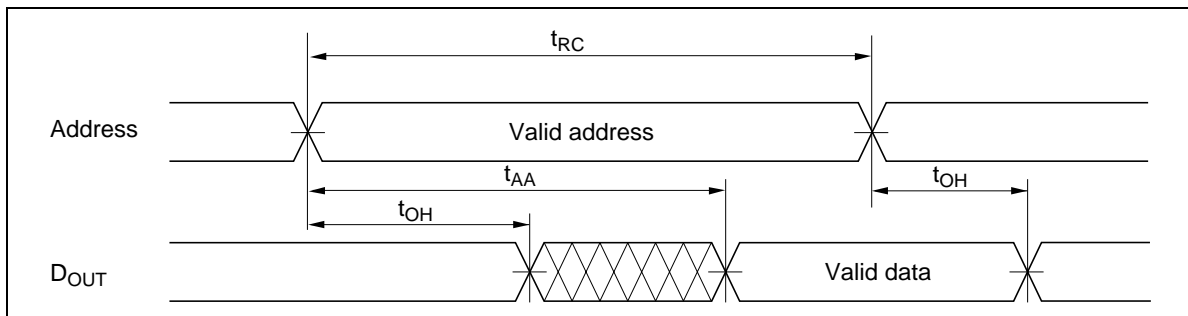


## Timing Waveforms

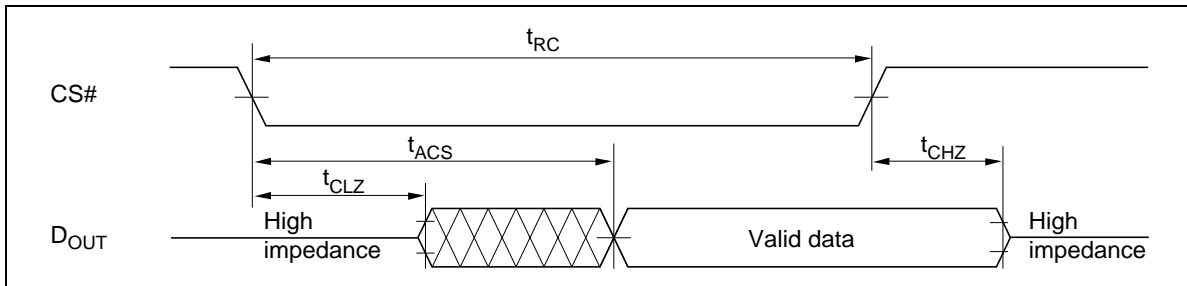
Read Timing Waveform (1) ( $WE\# = V_{IH}$ )



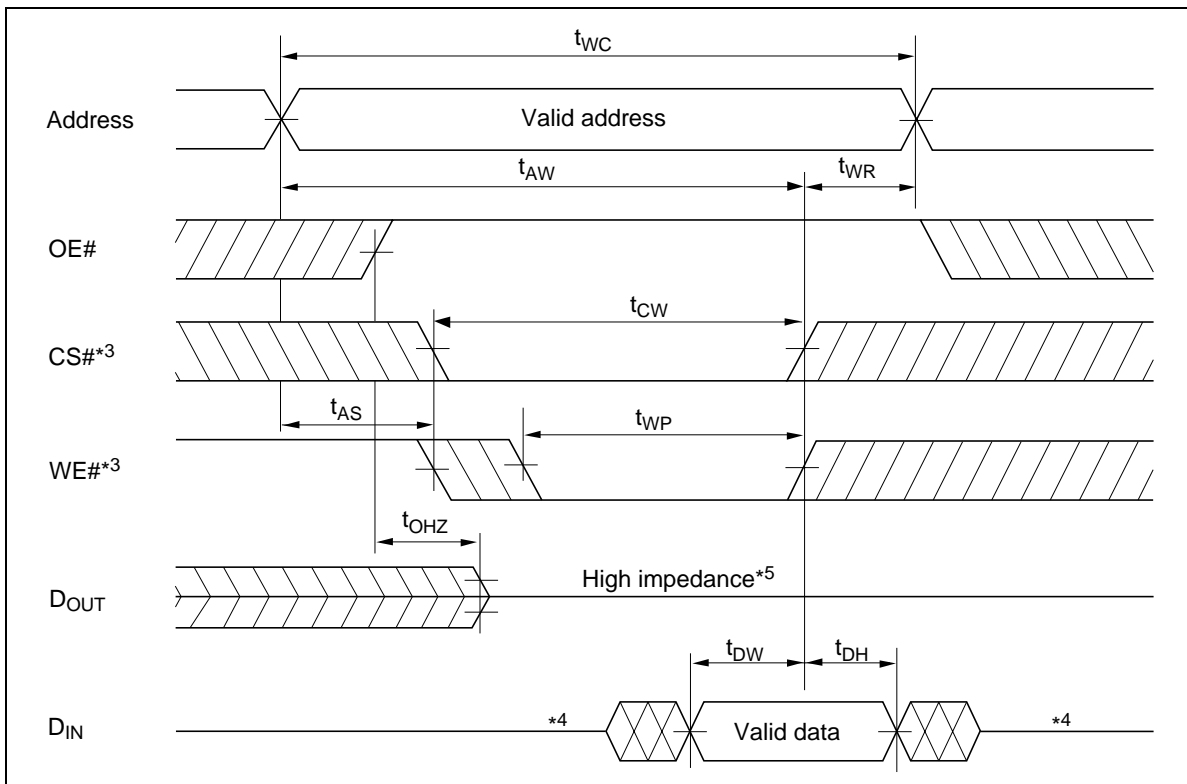
Read Timing Waveform (2) ( $WE\# = V_{IH}$ ,  $CS\# = V_{IL}$ ,  $OE\# = V_{IL}$ )



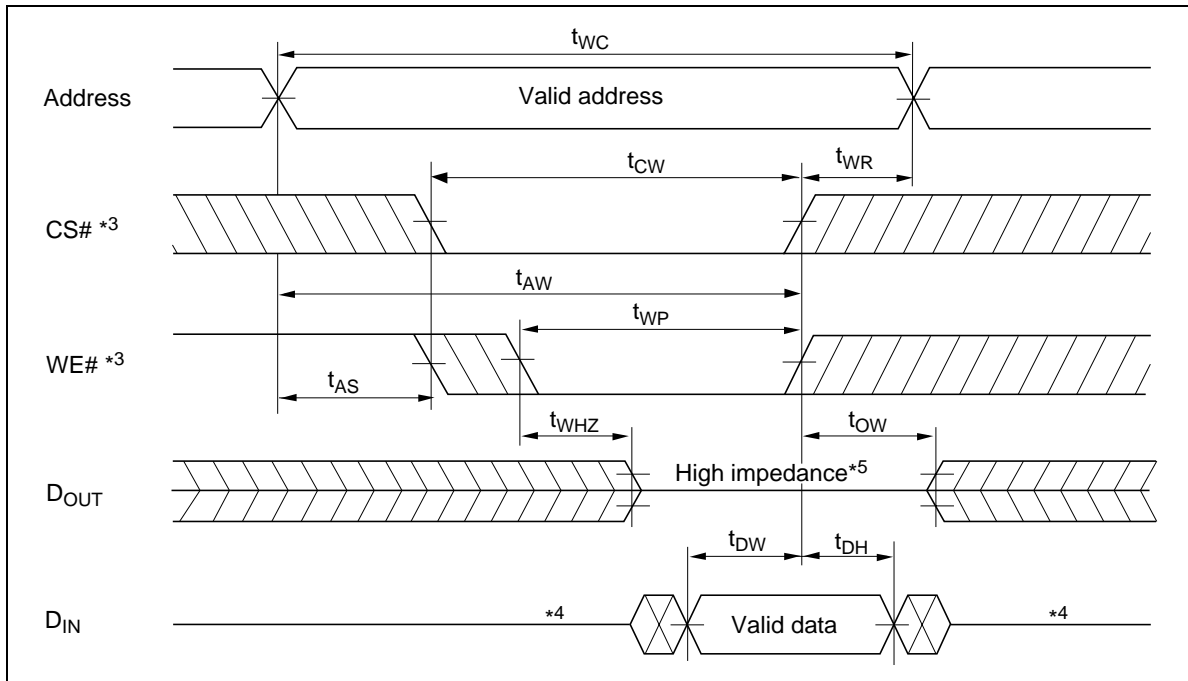
Read Timing Waveform (3) ( $WE\# = V_{IH}$ ,  $CS\# = V_{IL}$ ,  $OE\# = V_{IL}$ )\*<sup>2</sup>



Write Timing Waveform (1) ( $WE\#$  Controlled)



Write Timing Waveform (2) (CS# Controlled)



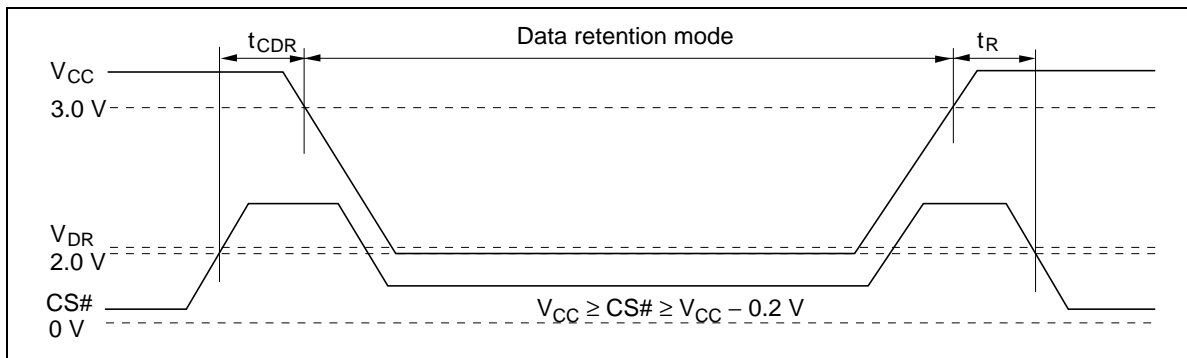
## Low $V_{CC}$ Data Retention Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Max	Unit	Test conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	V	$V_{CC} \geq CS\# \geq V_{CC} - 0.2\text{ V}$ (1) $0\text{ V} \leq V_{IN} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2\text{ V}$
Data retention current	$I_{CCDR}$	—	400	$\mu\text{A}$	$V_{CC} = 3\text{ V}$ , $V_{CC} \geq CS\# \geq V_{CC} - 0.2\text{ V}$ (1) $0\text{ V} \leq V_{IN} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{IN} \geq V_{CC} - 0.2\text{ V}$
Chip deselect to data retention time	$t_{CDR}$	0	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	ms	

## Low $V_{CC}$ Data Retention Timing Waveform



## Revision History

## R1RW0408D Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Sep. 30, 2003	—	Initial issue
1.00	Mar.12.2004	—	Deletion of Preliminary

## Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



### RENESAS SALES OFFICES

<http://www.renesas.com>

#### **Renesas Technology America, Inc.**

450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

#### **Renesas Technology Europe Limited.**

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom  
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

#### **Renesas Technology Europe GmbH**

Dornacher Str. 3, D-85622 Feldkirchen, Germany  
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

#### **Renesas Technology Hong Kong Ltd.**

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2375-6836

#### **Renesas Technology Taiwan Co., Ltd.**

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

#### **Renesas Technology (Shanghai) Co., Ltd.**

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

#### **Renesas Technology Singapore Pte. Ltd.**

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001