

## GENERAL DESCRIPTION

This IP core has been developing for AFE (Analog-front-end) function of voice signal processing with 14bit 8KHz voice codec.

The core consists of 14bit linear monolithic PCM CODEC/transmit and receive band-pass filters utilizing the sigma-delta A/D and D/A conversion architecture.

It offers a number of programmable functions accessed through a serial control channel that easily interfaces to any classical micro controller.

This IP core is suitable for digital mobile phones, as cellular and cordless phones, or any battery powered equipment.

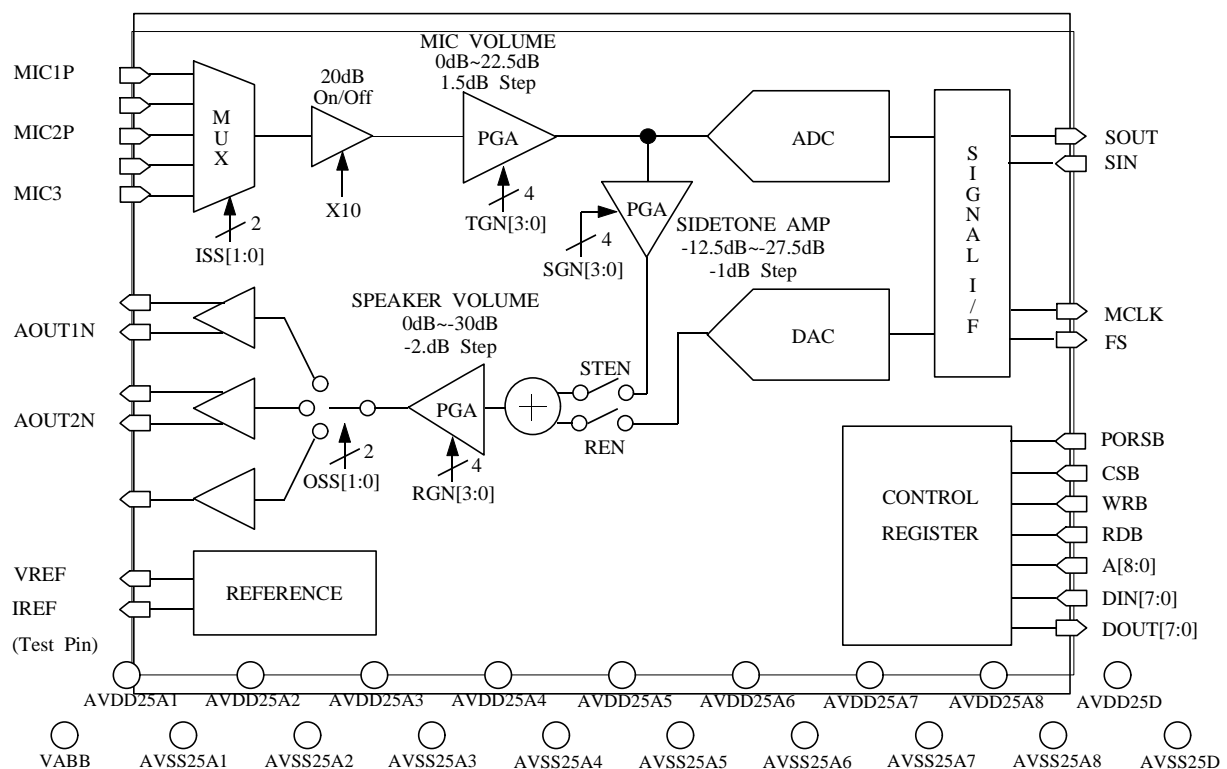
## FEATURES

- Analog 2.5Volt Operation
- Linear 14bit Codec
- 3 Mic Inputs (2 Differential and 1 Single)
- 3 Analog Outputs 32ohm Driver (2 Differential and 1 Single)
- Mic Volume 0dB ~ 22.5dB & 20dB Gain On/Off
- Speaker Volume 0dB ~ -30dB
- Side-tone -12.5dB ~ -27.5dB
- Serial Data Input, Output Format
- Control Register Interface for u-Controller

## APPLICATIONS

- digital mobile phones
- cellular and cordless phones

## FUNCTIONAL BLOCK DIAGRAM



**Ver 1.4 (Apr 2002)**

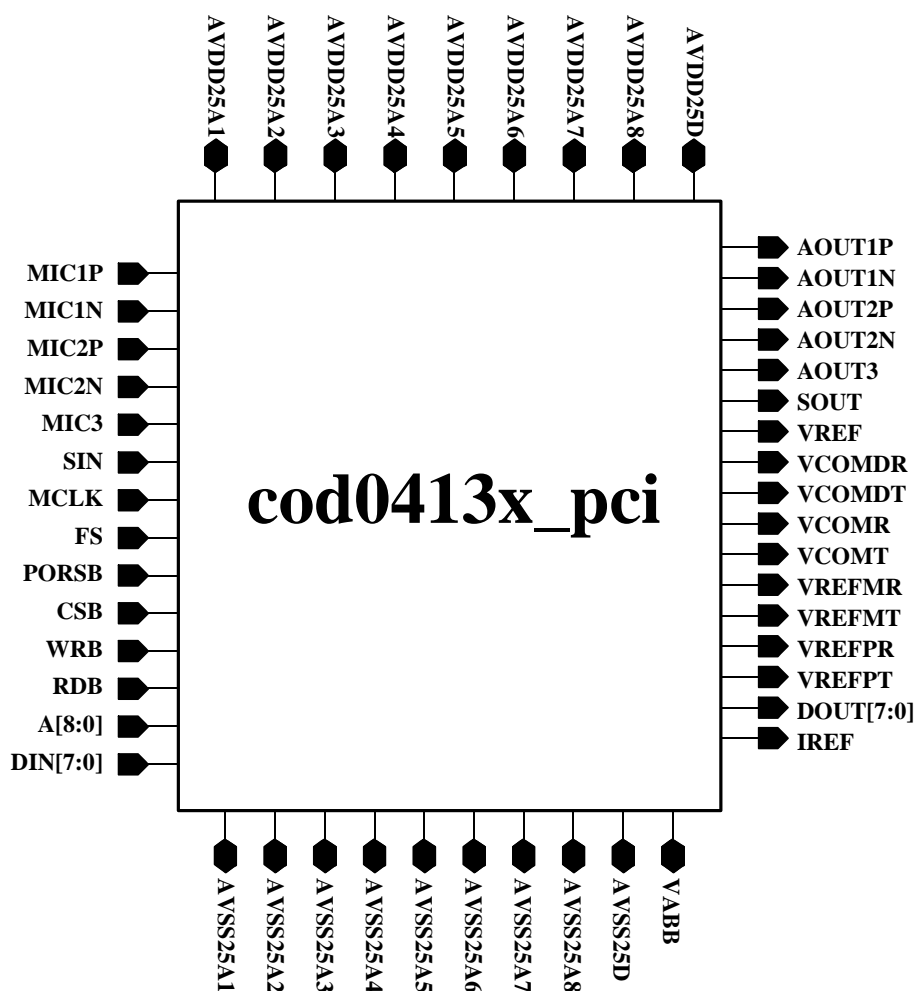
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## CORE PIN DIAGRAM

PIN NAME	Type	I/O Type	FUNCTION		
Power Pins				<b>I/O TYPE ABBR.</b> <ul style="list-style-type: none"><li>• AI : Analog Input</li><li>• DI : Digital Input</li><li>• AO : Analog Output</li><li>• DO : Digital Output</li><li>• AB : Analog Bidirectional</li><li>• DB : Digital Bidirectional</li><li>• AP : Analog Power</li><li>• AG : Analog Ground</li><li>• DP : Digital Power</li><li>• DG : Digital Ground</li></ul>	
AVDD25A1	AP	vdd2t_abb	Analog Power Supply 1 (2.5V)		
AVSS25A1	AG	vss2t_abb	Analog Ground 1		
AVDD25A2	AP	vdd2t_abb	Analog Power Supply 2 (2.5V)		
AVSS25A2	AG	vss2t_abb	Analog Ground 2		
AVDD25A3	AP	vdd2t_abb	Analog Power Supply 3 (2.5V)		
AVSS25A3	AG	vss2t_abb	Analog Ground 3		
AVDD25A4	AP	vdd2t_abb	Analog Power Supply 4 (2.5V)		
AVSS25A4	AG	vss2t_abb	Analog Ground 4		
AVDD25A5	AP	vdd2t_abb	Analog Power Supply 5 (2.5V)		
AVSS25A5	AG	vss2t_abb	Analog Ground 5		
AVDD25A6	DP	vdd2t_abb	Digital Power Supply 6 (2.5V)		
AVSS25A6	DG	vss2t_abb	Digital Ground 6		
AVDD25A7	AP	vdd2t_abb	Analog Power Supply 7 (2.5V)		
AVSS25A7	AG	vss2t_abb	Analog Ground 7		
AVDD25A8	AP	vdd2t_abb	Analog Power Supply 8 (2.5V)		
AVSS25A8	AG	vss2t_abb	Analog Ground 8		
AVDD25D	DP	vdd2t_abb	Digital Power Supply (2.5V)		
AVSS25D	DG	vss2t_abb	Digital Ground		
VABB	AG	vbb_abb	Analog Ground		
Analog Pins					
MIC1P	AI	pia_abb	Mic Input 1 Positive		
MIC1N	AI	pia_abb	Mic Input 1 Negative		
MIC2P	AI	pia_abb	Mic Input 2 Positive		
MIC2N	AI	pia_abb	Mic Input 2 Negative		
MIC3	AI	pia_abb	Mic Input 3 (Single Input)		
AOUT1P	AO	poa_abb	Differential Output 1 Positive		
AOUT1N	AO	poa_abb	Differential Output 1 Negative		
AOUT2P	AO	poa_abb	Differential Output 2 Positive		
AOUT2N	AO	poa_abb	Differential Output 2 Negative		
AOUT3	AO	poa_abb	Single Output		
VREF	AO	poa_abb	Reference Output		
VCOMDR	AO	poa_abb	tied to VREF pin		
VCOMDT	AO	poa_abb	tied to VREF pin		
VCOMR	AO	poa_abb	tied to VREF pin		
VCOMT	AO	poa_abb	tied to VREF pin		
VREFMR	AO	poa_abb	tied to Analog Ground pin		
VREFMT	AO	poa_abb	tied to Analog Ground pin		
VREFPR	AO	poa_abb	tied to VREF pin		
VREFPT	AO	poa_abb	tied to VREF pin		
IREF	AO	poa_abb	Analog Current Control (Test Pin). If this pin is not used, it may be left floating state.		

<i>Digital Pins</i>			
SOUT	DO	pot2_abb	ADC Serial Data Output
SIN	DI	picc_abb	DAC Serial Data Input
MCLK	DI	picc_abb	Master Clock Input
FS	DI	picc_abb	Frame Sync Pulse Input
PORSB	DI	picc_abb	Power-On-Reset and Reset Control Input (Low Active)
CSB	DI	picc_abb	Chip Select (Low Active)
WRB	DI	picc_abb	Write Enable (Low Active)
RDB	DI	picc_abb	Read Enable (Low Active)
A[8:0]	DI	picc_abb	Control Register Address
DIN[7:0]	DI	picc_abb	Control Register Data Input (WR is Enabled)
DOUT[7:0]	DO	pot2_abb	Control Register Data Output (RD is Enabled)

## CORE CONFIGURATION



## Power Group :

AVDD25A1 (AVDD25A1,AVDD25A2,AVDD25A3,AVDD25A4,AVDD25A5,AVDD25A6,AVDD25A8)  
 AVDD25A2 (AVDD25A7)  
 AVDD25D (AVDD25D)

**ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Supply Voltage	AVDD25A1 AVDD25A2 AVDD25D	3.3	V
Analog Input Voltage	-	AVSS25A1 to AVDD25A1 AVSS25A2 to AVDD25A2	V
Digital Input Voltage	-	AVSS25D to AVDD25D	V
Digital Output Voltage	V <sub>OH</sub> , V <sub>OL</sub>	AVSS25D to AVDD25D	V
Storage Temperature Range	T <sub>stg</sub>	-45 to 125	°C

**NOTES**

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5K $\Omega$  resistor (Human body model)
4. This core has initial calibration time for about 3m second from rising edge of PORSB.

**RECOMMENDED OPERATING CONDITIONS**

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	AVDD25A1, AVDD25A2, AVDD25D	2.375	2.5	2.625	V
Supply Voltage Difference	AVDD25A1, AVDD25A2, AVDD25D	-0.1	0.0	0.1	V
Digital Input Voltage		2.25	2.5	2.75	V
Analog Input Voltage		-	1.6	-	V <sub>pp</sub>
Operating Temperature	T <sub>opr</sub>	-40	-	85	°C

**NOTES**

1. It is strongly recommended that all the supply pins (AVDD25A1, AVDD25A2, AVDD25D) be powered from the same source to avoid power latch-up.

**AC ELECTRICAL CHARACTERISTICS**

(Measurement Bandwidth is 20Hz~4KHz. Full scale input sine wave 1KHz, FS=8KHz, @AVDD25A1=2.5V, AVDD25A2=2.5V, AVDD25D=2.5V Ta=55°C, Unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		-	14	-	Bits	-
Sampling rate		-	8	-	KHz	-
ADC Characteristics						
* Signal to Distortion Ratio		-	65	-	dB	0dB Input : Linear
Offset Error		-	-	±20	mV	-
Input Voltage Range		-	1.6	-	V <sub>pp</sub>	-
DAC Characteristics						
* Signal to Distortion Ratio		-	65	-	dB	0dB Input : Linear
Offset Error		-	-	±20	mV	-
Output Voltage Range		-	1.6 3.2	- -	V <sub>pp</sub> V <sub>pp</sub>	- Differential

Power Supply						
Power consumption (Operating Mode)			6.5	-	mA	No load -
			0.5	-	mA	
Power consumption (Power down mode)			50		uA	

## TRANS-MISSION CHARACTERISTICS

(Measurement Bandwidth is 60Hz~4KHz. Full scale, FS=8KHz, @AVDD25A1=2.5V, AVDD25A2=2.5V, AVDD25D=2.5V Ta=55° C., Unless otherwise specified.)

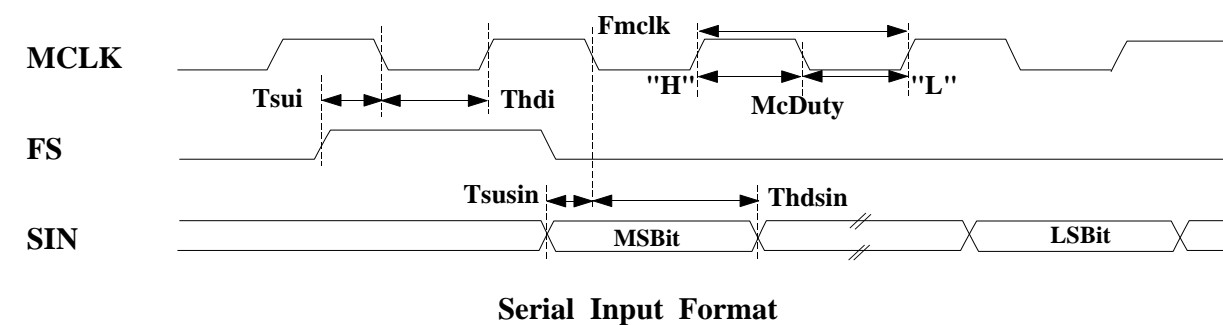
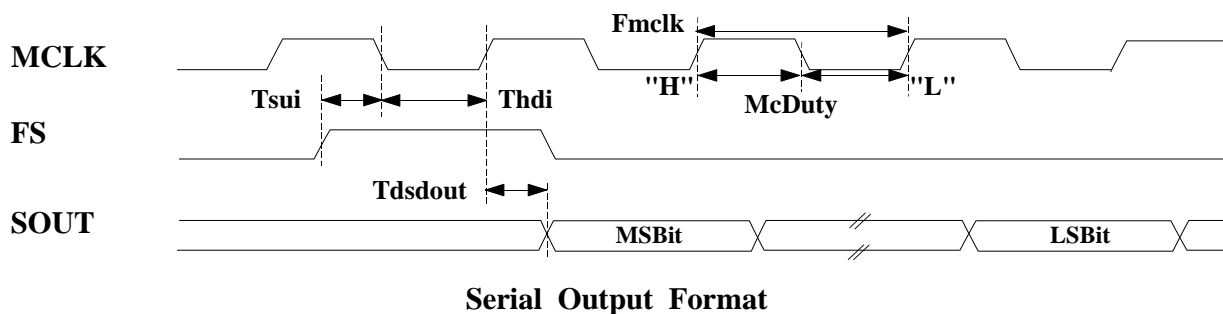
Characteristics	Test Condition	Min	Typ	Max	Unit
Transmit Gain Variation with Frequency	Relative to 1000Hz				
	f = 60Hz	-	-	-7.9	dB
	f = 200Hz	-	-	-1.5	dB
	f = 300Hz	-	-	-0.6	dB
	f = 400Hz ~ 3000Hz	-	-	-0.2	dB
	f = 3400Hz]	-	-	-1.1	dB
	f = 4000Hz	-	-	-17.8	dB
Receive Gain Variation with Frequency	Relative to 1000Hz				
	f = 60Hz	-	-	-8.2	dB
	f = 200Hz	-	-	-1.4	dB
	f = 300Hz	-	-	-0.6	dB
	f = 400Hz ~ 3000Hz	0.6	-	-0.2	dB
	f = 3400Hz]	-	-	-0.7	dB
	f = 4000Hz	-	-	-17.8	dB
Transmit Delay	f = 60hz ~ 3000Hz	-	-	750	us
Receive Delay	f = 60Hz ~ 3000Hz	-	-	750	us

## CONTROL CLOCKS CHARACTERISTICS

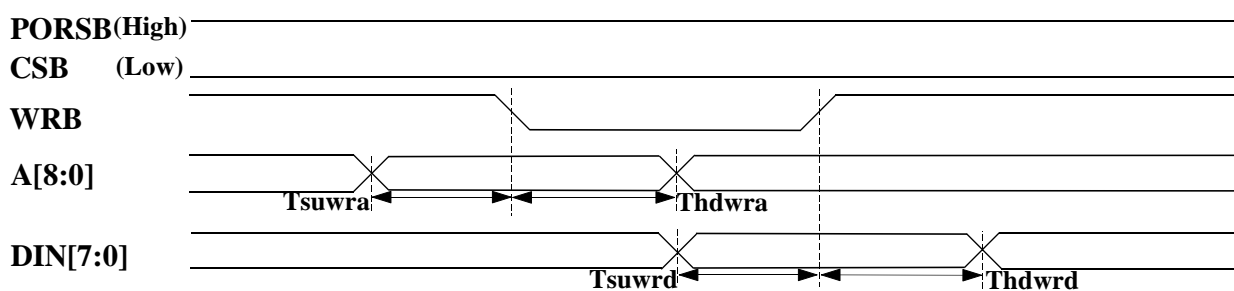
Characteristics	Symbol	Min	Typ	Max	Unit
MCLK Frequency	Fmclk	-	2.048	-	MHz
MCLK Duty Cycle (H/L)	McDuty	-	50:50	-	%
FS Frequency	Fsync	-	8	-	KHz
MCLK Falling and FS SetUp	TsuI	10	-	-	ns
MCLK Falling and FS Hold	ThdI	10	-	-	ns
MCLK Rising and SOUT Delay	Tdsdout	-	-	10	ns
MCLK Falling and SIN SetUp	Tsusin	10	-	-	ns
MCLK Falling and SIN Hold	Thdsin	10	-	-	ns
WR Rising and A[8:0] SetUp	Tsuwra	20	-	-	ns
WR Rising and A[8:0] Hold	Thdwra	20	-	-	ns
WR Rising and DIN[7:0] SetUp	Tsuwrd	10	-	-	ns
WR Rising and DIN[7:0] Hold	Thdwrd	10	-	-	ns
RD Falling and A[8:0] SetUp	Tsurda	10	-	-	ns
RD Rising and A[8:0] Hold	Thdrda	20	-	-	ns
RD Falling and DOUT[8:0] Delay	Tdrdf	-	-	10	ns
RD Rising and DOUT[8:0] Delay	Tdrdr	-	-	10	ns

## Timing Diagram

### Serial Data Interface

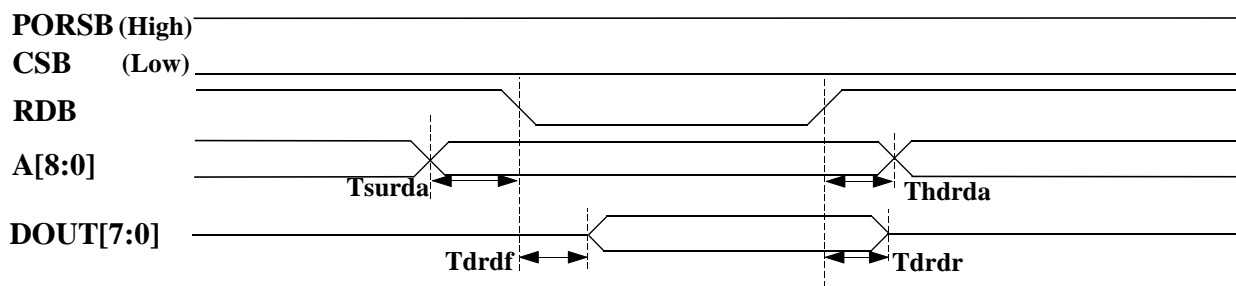


### Control Register Interface



#### Write Mode

Note : Of the data written on the registers, the control signals(OSS, STEN, RGN) for Tx path are assigned at the rising edge of the internal signal RXZC.



#### Read Mode

## Programmable Functions

### Control Register Mapping Table

ADDRESS A[8:0]	FUNCTION	DATA[7:0]							
		7	6	5	4	3	2	1	0
0D0h	Status	X	X	X	X	X	X	X	INIT
0D1h	Power Management	X	X	X	X	X	PW[2]	PW[1]	PW[0]
0D2h	Path Select	ISS[1]	ISS[0]	STEN	OSS[1]	OSS[0]	REN	X	X
0D3h	Mic Volume	T20DB	X	X	X	TGN[3]	TGN[2]	TGN[1]	TGN[0]
0D4h	Speaker Volume	X	X	X	X	RGN[3]	RGN[2]	RGN[1]	RGN[0]
0D5h	Sidetone Volume	X	X	X	X	SGN[3]	SGN[2]	SGN[1]	SGN[0]
0D6h	Miscellaneous	X	X	X	X	X	X	CALDIS	DLB
0D7h	Test Path	X	TLBM	DIBYP	MOBYP	AMOP	ABYP	ALBM	DLBM

### Status Register (0D0H); Read Only

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	X	X	X	INIT	
							0	Under Initializing
							1	Initialize Done

### Power Management (0D1H)

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	X	PW[2]	PW[1]	PW[0]	
					0	0	0	All Power Down (*)
					0	0	1	Standby Mode
					0	1	0	Rx Power Up, Tx Power Down
					0	1	1	Tx Power Up, Rx Power Down
					1	x	x	All Power Up

### Path Selection (0D2H)

7	6	5	4	3	2	1	0	FUNCTION
ISS[1]	ISS[0]	STEN	OSS[1]	OSS[0]	REN	X	X	
0	0							All Muted (*)
0	1							MIC1P, MIC1N Selected
1	0							MIC2P, MICT2N Selected
1	1							MIC3 Selected
		0						Sidetone Disabled (*)
		1						Side Tone Enabled
					0			Receive path Disaable (*)
					1			Receive path Enable
			0	0				All Muted (*)
			0	1				AOUT1P, AOUT1N Selected
			1	0				AOUT2P, AOUT2N Selected
			1	1				AOUT3 Selected

Mic volume control register (0D3H)

7	6	5	4	3	2	1	0	FUNCTION
T20DB	X	X	X	TGN[3]	TGN[2]	TGN[1]	TGN[0]	
0								0dB Selected (*)
1								20dB Selected
				0	0	0	0	0dB Selected (*)
				0	0	0	1	1.5dB Selected
				-	-	-	-	-
				1	1	1	1	22.5dB Selected

Speaker Volume Control Register (0D4H)

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	RGN[3]	RGN[2]	RGN[1]	RGN[0]	
				0	0	0	0	0dB Selected (*)
				0	0	0	1	-2dB Selected
				-	-	-	-	-
				1	1	1	1	-30dB Selected

Sidetone Volume Control Register (0D5H)

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	SGN[3]	SGN[2]	SGN[1]	SGN[0]	
				0	0	0	0	-12.5dB Selected (*)
				0	0	0	1	-13.5dB Selected
				-	-	-	-	-
				1	1	1	1	-27.5dB Selected

Miscellaneous Control Register (0D6H)

7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	X	X	CALDIS	DBYP	
						0		Calibration Function Enabled (*)
						1		Calibration Function Disabled
							0	Serial Data Loop Back Disabled (*)
							1	Serial Data Loop Back Enabled

Test Mode Control Register (0D7H)

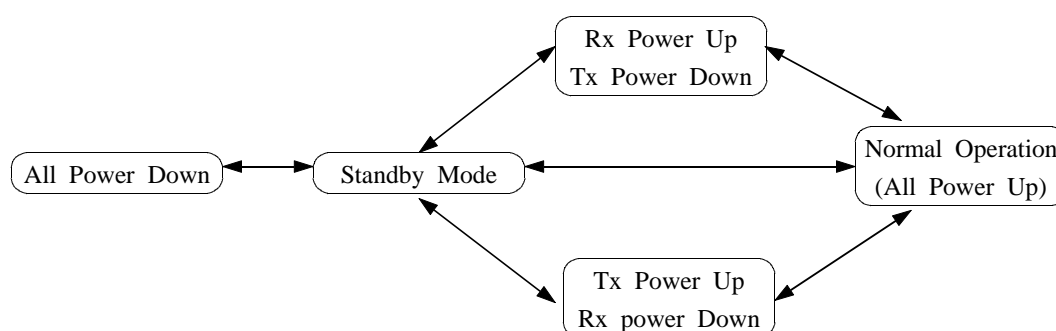
7	6	5	4	3	2	1	0	FUNCTION
X	TLBM	DIBYP	MOBYP	AMOPI	ABYP	ALBM	DLBM	
	0							ADC/DAC Loop Mode disabled (*)
	1							ADC/DAC Loop Mode enabled
		0						Digital Decimator Filter Input Bypass Disabled (*)
		1						Digital Decimator Filter Input Bypass Enabled



			0					Digital Modulator Output Bypass Disabled (*)
			1					Digital Modulator Ourput Bypass Enabled
				0				Analog Moulator Output / Postfilter Input Bypass Disabled (*)
				1				Analog Moulator Output / Postfilter Input Bypass Enabled (*)
					0			Analog Bypass Disabled (*)
					1			Analog Bypass Enabled
						0		Analog Loop Back Disabled (*)
						1		Analog Loop Back Enabled
							0	Digital Loop Back Disabled (*)
							1	Digital Loop Back Enabled

## Power Down/Up Management Guide

cod0413x\_pci is capable of operating at required power when no activity is required. The State of power down/up is controlled by the Power Management Register(0D1H).

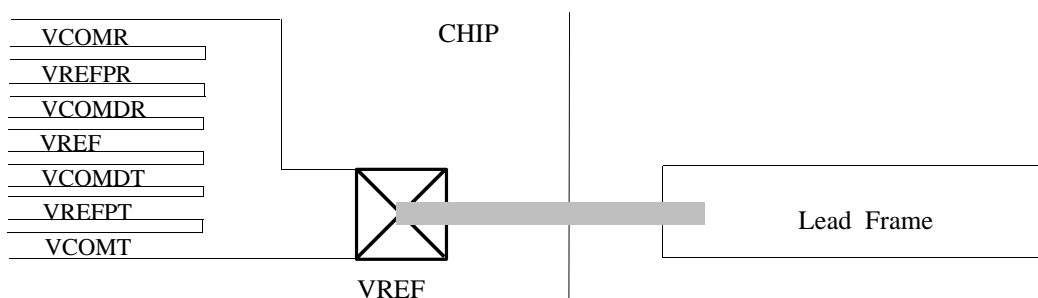


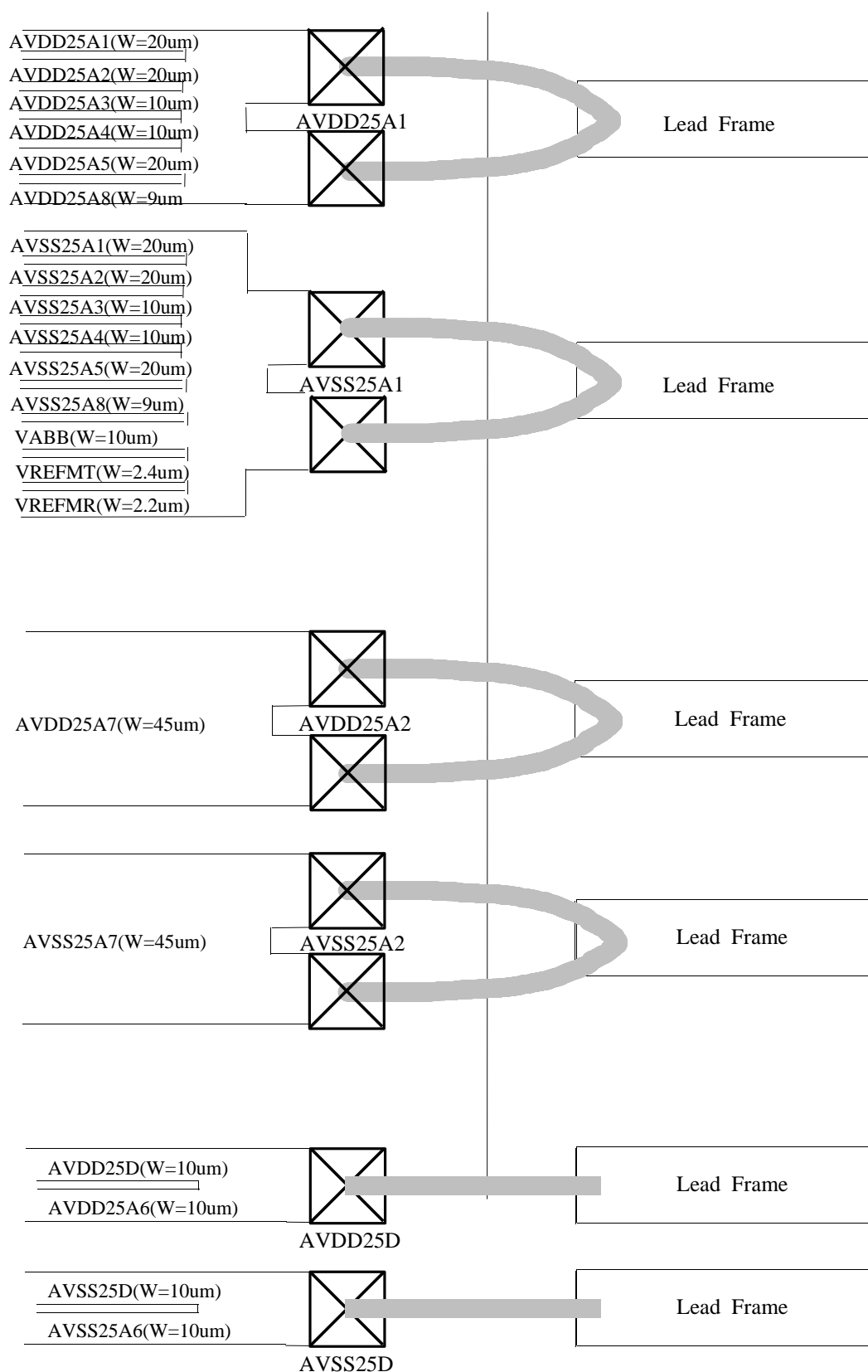
The above figure illustrates one example procedure a complete power down/up of cod0413x\_pci.

From normal operation sequential writes to the Power Management Register are preformed to power down/up cod0413x\_pci a piece at a time

## Layout Guide

### REFERENCE VOLTAGE & POWER LINE CONNECTION





## Phantom cell

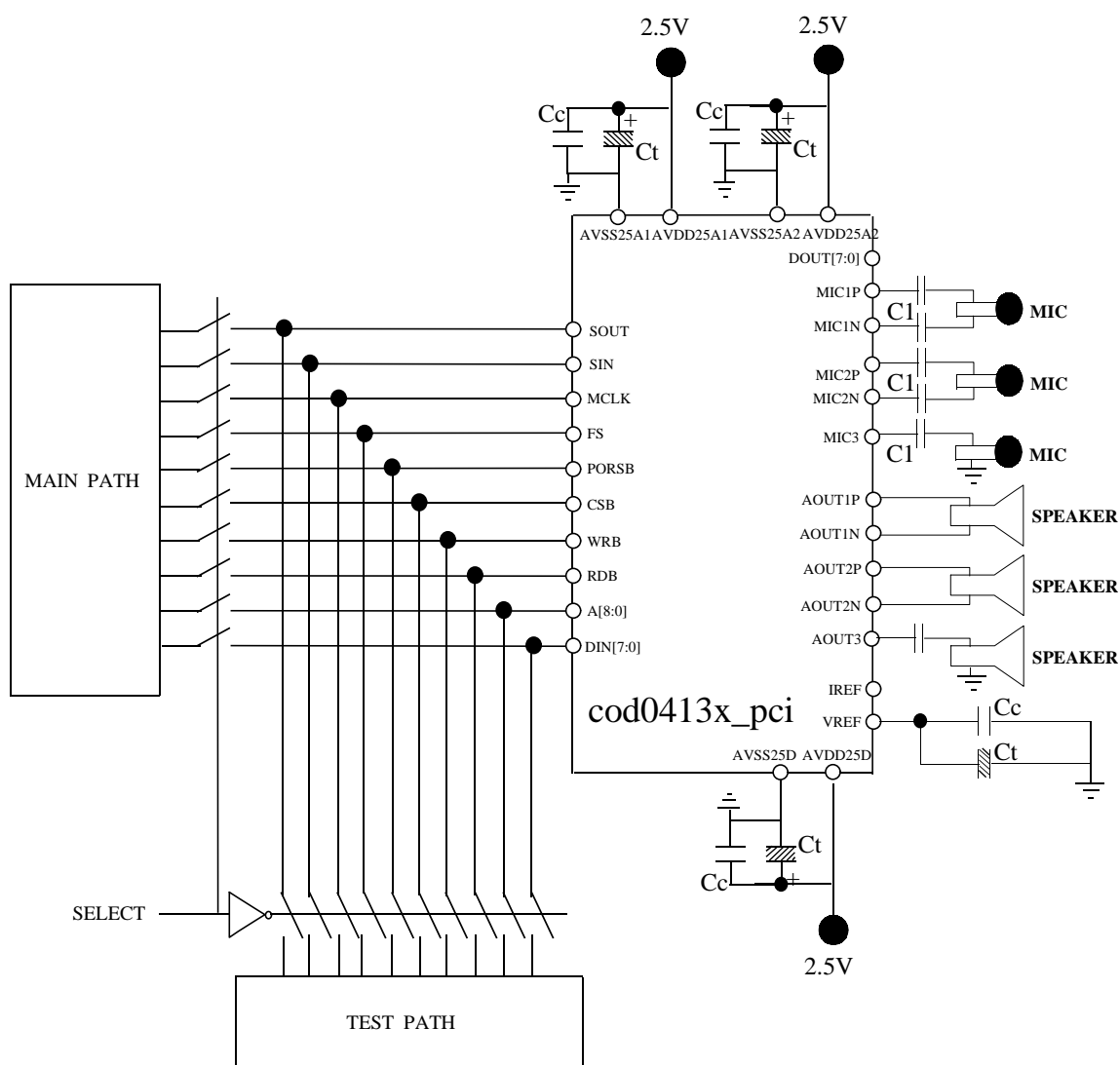
AVSS25A2	AOUT1N
VABB	AOUT1P
AVDD25A2	AOUT2N
AVDD25A7	AOUT2P
AVSS25A7	AOUT3
	VCOMR
	IREF
	VREFMR
	VREFPR
	VCOMDR
AVSS25A4	AOUT1P
VREF	AOUT1N
AVDD25A4	AOUT2P
AVDD25A3	AOUT2N
AVSS25A3	AOUT3
	VREF
	VCOMDR
	VCOMDT
	VREFPT
	VREFMT
	VCOMT
	MIC3
	MIC2P
	MIC1P
	MIC1N
	MIC2N
AVSS25A1	
VABB	
AVDD25A1	
AVSS25A5	
AVDD25A5	
AVSS25A6	
VABB	
AVDD25A6	
AVSS25A8	
AVDD25A8	
AVSS25D	
AVDD25D	
VABB	
MCLK	
CSB	
A[8:0]	
WRB	
RDB	
DIN[7:0]	
DOUT[7:0]	
PORSB	
SIN	
SOUT	
FS	

**cod0413x\_pci**  
**14b 8k voice codec**

Pin Name	Pin Usage	Pin Layout Guide
AVDD25A6	External	<ul style="list-style-type: none"> <li>- Maintain the large width of lines as far as the pads.</li> <li>- Place the port positions to minimize the length of power lines.</li> <li>- Do not merge the analog powers with another power from other blocks.</li> <li>- Use good power and ground source on board.</li> </ul>
AVSS25A6	External	
AVDD25A7	External	
AVSS25A7	External	
AVDD25A8	External	
AVSS25A8	External	
AVDD25D	External	
AVSS25D	External	
VABB	External	<ul style="list-style-type: none"> <li>- Do not overlap with digital lines.</li> <li>- Maintain the shortest path to pads.</li> </ul>
MIC1P	External	
MIC1N	External	
MIC2P	External	
MIC2N	External	
MIC3	External	
AOUT1P	External	
AOUT1N	External	
AOUT2P	External	<ul style="list-style-type: none"> <li>- Maintain the larger width and the shorter length as far as the pads.</li> <li>- Separate from all other digital lines.</li> </ul>
AOUT2N	External	
AOUT3	External	
VREF	External	
VCOMDR	External	
VCOMDT	External	
VCOMR	External	
VCOMT	External	
VREFPR	External	<ul style="list-style-type: none"> <li>- Separate from all other analog signals</li> </ul>
VREFPT	External	
VREFMR	External	
VREFMT	External	
IREF	External	
SOUT	External/Internal	
SIN	External/Internal	
MCLK	External/Internal	
FS	External/Internal	
PORSB	External/Internal	
CSB	External/Internal	
WRB	External/Internal	
RDB	External/Internal	
A[8:0]	External/Internal	
DIN[7:0]	External/Internal	
DOUT[7:0]	External/Internal	

Pin Name	Pin Usage	Pin Layout Guide
AVDD25A1	External	<ul style="list-style-type: none"> <li>- Maintain the large width of lines as far as the pads.</li> <li>- Place the port positions to minimize the length of power lines.</li> <li>- Do not merge the analog powers with another power from other blocks.</li> <li>- Use good power and ground source on board.</li> </ul>
AVSS25A1	External	
AVDD25A2	External	
AVSS25A2	External	
AVDD25A3	External	
AVSS25A3	External	
AVDD25A4	External	
AVSS25A4	External	
AVDD25A5	External	
AVSS25A5	External	

## CORE EVALUATION GUIDE



LOCATION	DESCRIPTION
Ct	0.1uF TANTALUM CAPACITOR
Cc	10uF CERAMIC CAPACITOR
C1	0.47uF CERAMIC CAPACITOR
R1	32Ω RESISTOR

<The Connection User Guide Line for Embedded Core Test>

## NOTES

1. If SOUT is externally shorted with SIN, The CODEC is achieved to loop-back test mode(ADC->DAC).
2. If end users want to test CODEC in integrated chip, The above pin must be extracted to the PAD.
3. The analog power/ground must be separated from digital power/ground.
4. Power typical value :  
 $AVDD25A1 = AVDD25A2 = AVDD25D = 2.5V$ ,  $AVSS25A1 = AVSS25A2 = AVSS25D = 0.0V$

**FEEDBACK REQUEST**

It should be quite helpful to our CODEC core development if you specify your system requirements on CODEC in the following characteristic checking table and fill out the additional questions.

We appreciate your interest in our products. Thank you very much.

Could you explain external/internal pin configurations as required?

Specially requested function list :

1. What is your signal band to use, 3.6KHz? 4KHz? or 4.8KHz?
2. What is your analog in/output signal voltage swing? and what kind of format do you want as analog signal in/output: single or differential format? If you can, Please let us know, what is your exact in/output signal spec.
3. What is your minimum S/N+D spec?
4. Do you want linear phase characteristic or you don't care on digital filter spec?
5. Could you give us exact design spec of speech codec? (For example, A-law, u-law and so on.)

## HISTORY CARD

[illegible]