

GENERAL DESCRIPTION

The COD0418X is Sigma-Delta CODEC for speech and telephony applications. The product contains both digital IIR/FIR filter and smoothing filter. The normal input and output channels have μ /A law format with 38dB signal to distortion ratio. The input and output of this device is compressed form(A-law, μ -law) and 16bit linear which can be easily determined by control select pins. and it has variable gain control block varies from -4dB to +58dB, 2dB steps and input type of AFE is differential and there is another analog bypass mode single input port. An on-chip voltage reference circuit is included to allow the single supply operation.

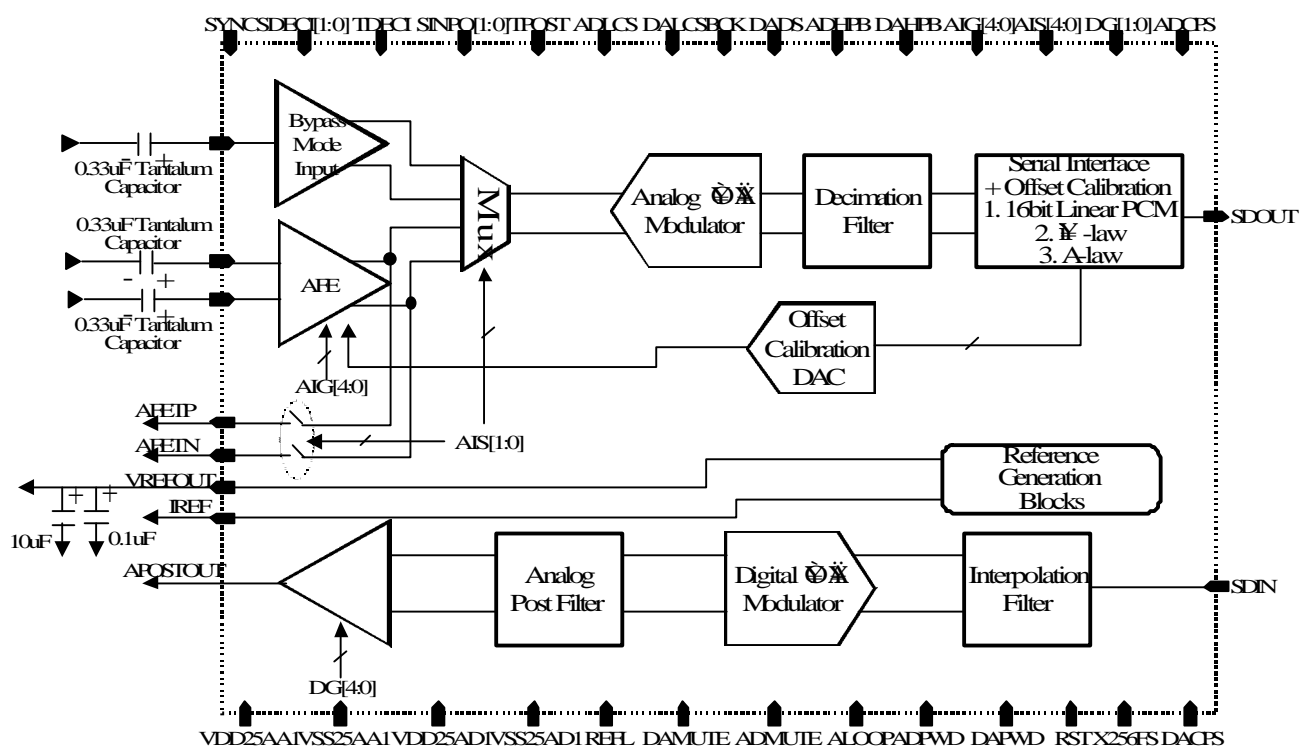
FEATURES

- Single chip voice line Codec (A/D, D/A converter included)
- Over-sampled Sigma Delta modulator/Demodulator
- Input/output format: 8bit μ -law/A-law and linear 16bit
 - * These three types are easily selectable by control pins
 - * When serial interface mode: 16bit linear
- ADC gain block(AFE) range: -4dB to +58dB, 2dB step
- DAC gain block rang: 0,2,3.5dB
- Analog bypass mode for substitution of AFE
- Sigma Delta ADC.
 - * 256X Over-sampling
 - * On chip Decimation Filter
 - * On chip Smoothing Filter
- Sigma Delta DAC.
 - * 256X Over-sampling
 - * On chip 256X Interpolation Filter
 - * On chip Analog Post Filter
- AFE has differential inputs, analog bypass mode has single and analog output is single.
- Sampling Rate: 8kHz
- On chip voltage reference circuitry
- Single +2.5V Power Supply
- 1.6Vpp Input/output signal swing but with signal distortion swings up to 2Vpp.
- Power Consumption
 - * Operating Mode: 17mW Typ(2.5V)
 - * Power-down Mode: 125µW Typ(2.5V)

TYPICAL APPLICATIONS

- Speech Processing
(Recognition, Synthesis, Compression etc.)
- Telephony
- Modem

FUNCTIONAL BLOCK DIAGRAM WITH INPUT/OUTPUT APPLICATION



CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
VDD25AA1	AP	vdd2t_abb	Analog Power (+2.5V): 10uF ceramic and 0.1uF tantalum capacitors should be connected between VDD25AA1 and VSS25AA1 and these two capacitors should be placed as close as possible to two power pads. and the order of two capacitor is described in core evaluation guide.
VSS25AA1	AG	vss2t_abb	Analog Ground (0.0V)
IREF	AO	poa_abb	Current Reference Output: this pin is for test, so normally this pin is float.
REFL	AG	vss2t_abb	Analog Reference Ground (0.0V): for proper operation the end user should supply clean ground level voltage to this pin but if there is no other ground level source, end user can supply analog ground level to this pin. * Note: if there are not enough pins available, end user can connect this pin to VASS25AA1, but in this case REFL should be connected to "VASS25AA1 PAD"
AINP	AI	pia_abb	AFE Analog Positive input: this is positive analog input pin of Analog Front End gain stage. and the input impedance of this pin is 20Kohm.
AINN	AI	pia_abb	AFE Analog Negative input: this is negative analog input pin of Analog Front End gain stage. and the input impedance of this pin is 20Kohm.

NOTES:

1. This pin descriptions are not fixed, but recommended.
2. The Power pin(VDD25AA1,VDD25AD1) must be connected by DIODE_SLOT2.
3. The Ground pin (VSS25AA1, VSS25AD1) must be connected by DIODE_SLOT2.
4. SDECI[1:0], TDECI -> Decimation Filter Block test pin.
5. SINPO[1:0], TPOST -> Post Filter Block test pin.

I/O TYPE ABBR.

- AI: Analog Input
- DI: Digital Input
- AO: Analog Output
- DO: Digital Output
- AB: Analog Bi-directional
- DB: Digital Bi-directional
- AP: Analog Power
- AG: Analog Ground
- DP: Digital Power
- DG: Digital Ground

CORE PIN DESCRIPTION (Cont'd)

Name	I/O Type	I/O Pad	Pin Description
AFETP	AO	poa_abb	AFE Positive Test Output: this is a test pin of AFE block and AFE positive output, the detailed control of this test mode is described in pin description of AIS[1:0]
AFETN	AO	poa_abb	AFE Negative Test Output: this is a test pin of AFE block and AFE negative output, the detailed control of this test mode is described in pin description of AIS[1:0]
DAMUTE	DI	picc_abb	DAC Analog Mute select (High active): when high state DAC mute function activates
ADMUTE	DI	picc_abb	ADC Analog Mute select (High active): when high state ADC mute function activates
ALOOP	DI	picc_abb	Analog loop back select (High active): test pin for internal analog blocks only. and in normal operation, this is LOW state.
VREFOUT	AO	poa_abb	Vref output: voltage reference output of COD0418x and two capacitors should be placed between VREFOUT and analog ground level and one capacitor is 10uF and the other is 0.1uF and detailed capacitor order is described in core evaluation guide and input/output application guide.
ABIN	AI	pia_abb	Bypass Mode Analog Input: analog input of bypass mode and detailed control of bypass mode is described in pin description of AIS[1:0]
APOSTOUT	AO	poa_abb	DAC Analog output: the output load of APOSTOUT is 10Kohm and maximum output of this is 1.6Vp-p but from the request of end user the DAC gain has 3 steps, when 0dB=1.337Vpp, 2dB=1.683Vpp and 3.5dB=2.0Vpp and AC Electrical test of DAC will be performed at 0dB gain and 1.6Vpp input source for core performance test.
ADPWD	DI	picc_abb	ADC Power Down (High active): when high state ADC power down activates
DAPWD	DI	picc_abb	DAC Power Down (High active): when high state DAC power down activates
RST	DI	picc_abb	Digital Reset (High active)
X256FS	DI	picc_abb	256*Sampling Freq.(FS) Clock: main clock of COD0418x and it should be 2.048MHz
SYNC	DI	picc_abb	Sampling Freq.(FS) Clock
SDECI[1:0]	DI	picc_abb	ADC Digital Filter input select: test pin for internal functional blocks, and in normal operation these are LOW states.
TDECI	DI	picc_abb	ADC Digital Filter Test input: test pin for internal functional blocks, and in normal operation, this is LOW state.
SINPO[1:0]	DI	picc_abb	DAC Post Filter input select: test pin for internal functional blocks, and in normal operation these are LOW states.

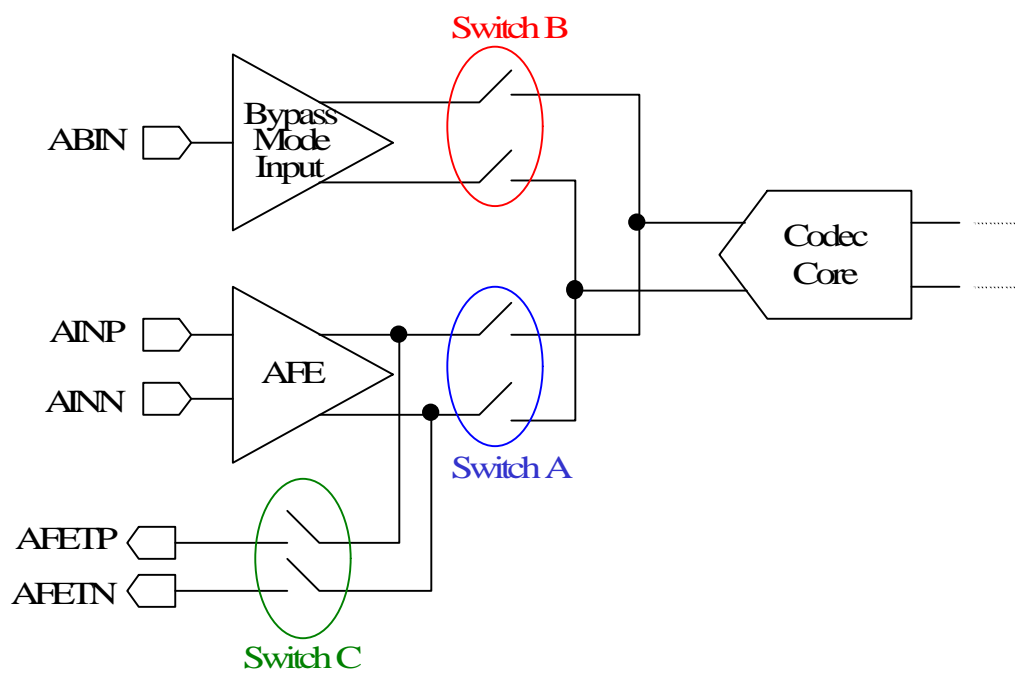
CORE PIN DESCRIPTION (Cont'd)

Name	I/O Type	I/O Pad	Pin Description
SDIN	DI	picc_abb	Serial Data Input: The input of DAC
TPOST	DI	picc_abb	DAC Post Filter Test input: test pin for internal functional blocks, and in normal operation, this is LOW state.
ADLCS	DI	picc_abb	ADC Linear/Command data select (Low/High): when low state ADC Linear mode selected, and high ADC Command mode selected.
DALCS	DI	picc_abb	DAC Linear/Command data select (Low/High): when low state DAC Linear mode selected, and high DAC Command mode selected.
ADCPS	DI	picc_abb	ADC μ -law/A-law select (Low/High): when high state ADC A-law mode selected, and low ADC μ -law mode selected.
DACPS	DI	picc_abb	DAC μ -law/A-law select (Low/High): when high state DAC A-law mode selected, and low DAC μ -law mode selected.
VSS25AD1	DG	vss2t_abb	Digital Ground (0.0V): 10uF ceramic and 0.1uF tantalum capacitors should be connected between VDD25AD1 and VSS25AD1 and these two capacitors should be placed as close as possible to two power pads. and the order of two capacitors is described in core evaluation guide.
VDD25AD1	DP	vdd2t_abb	Digital Power Supply (2.5V)
SDOUT	DO	pot2_abb	Serial Data Output: this is ADC output
BCK	DI	picc_abb	Bit Clock - Serial Interface Clock
DADS	DO	pot2_abb	DAC Modulator output: DAC sigma-delta modulator output and this pin is for internal functional block test, and in normal operation, this pin is floating state, but this should be muxed out for test.
ADHPB	DI	picc_abb	ADC High Pass Filter Enable (Low Active): this pin changes of lower side of base-band frequency response. when high state COD0418X core will transmit very low frequency component (from DC to 300Hz) but when low state, high pass filter function will be enabled, so frequencies below 300Hz will be eliminated. this is only for ADC path.
DAHPB	DI	picc_abb	DAC High Pass Filter Enable (Low Active) : this pin changes of lower side of base-band frequency response. when high state COD0418X core will receive very low frequency component (from DC to 300Hz) but when low state, high pass filter function will be enabled, so frequencies below 300Hz will be eliminated. this is only for DAC path.

CORE PIN DESCRIPTION (Cont'd)

Name	I/O Type	I/O Pad	Pin Description
AIG[4:0]	DI	picc_abb	<p>AFE Gain Control: this will change the AFE gain linearly. and gain step size is 2dB</p> <p>AIG[4:0] = 00000: -4dB</p> <p>AIG[4:0] = 00001: -2dB</p> <p>...</p> <p>AIG[4:0] = 11110: +56dB</p> <p>AIG[4:0] = 11111: +58dB</p>
AIS[1:0]	DI	picc_abb	<p>Analog Input Select: this is for selecting input path and AFE test mode. refer to following description and diagram below.</p> <ol style="list-style-type: none"> 1. when AIS[1:0]=00 then only switch A is on, so end user can use AFE + codec core. 2. when AIS[1:0]=01 then only switch B is on, so end user can use analog bypass mode + codec core 3. when AIS[1:0]=10 then only switch C is on, so end user can test AFE block only. 4. when AIS[1:0]=11 then switch B and C are on, so end user can use analog bypass mode + code core and test AFE block at the same time.
DG[1:0]	DI	picc_abb	<p>DAC Gain Control: dac gain has 3 steps when DG[1:0]=00 0dB will be set, DG[1:0]=01 then 2dB and DG[1:0]=10 then 3.5dB respectively.</p>

AIS[1:0] ANALOG INPUT SELECT DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD25AD1	3.3	V
Digital Input Voltage	D _{IN}	VSS25AD1 to VDD25AD1	V
Storage Temperature Range	T _{stg}	-45 to 125	°C
Operating Temperature Range	T _{opr}	0 to 70	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operations under any of these conditions is not implied.
2. All voltages are measured with respect to VSS(VSS25AA1 or VSS25AD1) unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD25AA1 - VSS25AA1 VDD25AD1 - VSS25AD1	2.375	2.5	2.625	V
Supply Voltage Difference	VDD25AA1 - VDD25AD1	0.1	0.0	0.1	V
Digital Input Voltage Range		2.25	2.5	2.75	V
Analog Input Voltage Range		-	1.6	-	V _{pp}

NOTE: It is strongly recommended that all the supply pins (VDD25AA1, VDD25AD1) be powered from the same source to avoid power latch up.

DIGITAL FILTER CHARACTERISTICS

Characteristics	Ratio	Value (Fs = 8kHz)	Conditions
Filter Pass-band	0 ~ 0.4Fs	0 ~ 3.2kHz	high pass filter off
	0.0375Fs ~ 0.4Fs	300Hz ~ 3.2kHz	high pass filter on
Filter Pass-band ripple	±0.5dB	±0.5dB	-
Filter Stop-band	0.6Fs over	4.8kHz over	high pass filter off
	0.0375Fs under, 0.6Fs over	300Hz under 4.8kHz over	high pass filter on
Filter Stop-band attenuation	-1.2dB(0.425Fs) -40dB (0.6Fs over)	-1.2dB(3.4kHz) -40dB(4.8kHz over)	high pass filter off
	-1.2dB(0.425Fs) -40dB (0.6Fs over) -8dB(0.0075Fs) -25dB (0Fs)	-1.2dB(3.4kHz) -40dB(4.8kHz over) -8dB(60Hz) -25dB(0Hz)	high pass filter on

AC ELECTRICAL CHARACTERISTICS

(Measurement Bandwidth is 20Hz - 4kHz. Full scale input sine wave 1kHz, FS=8kHz, @VDD25AA1, VDD25AD1=2.5V, Ta=25°C ,Unless otherwise specified.)

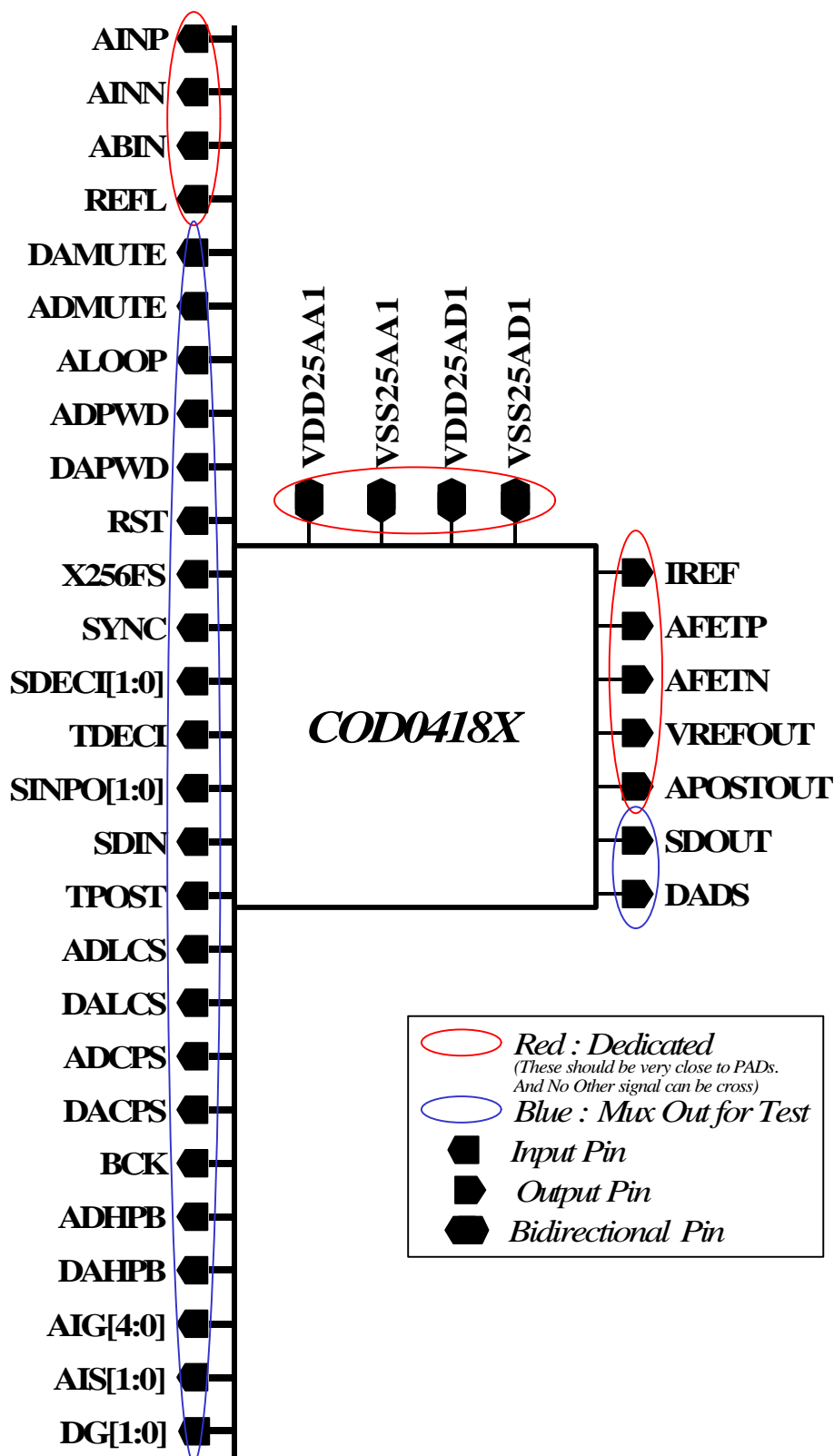
Codec Core Characteristics						
Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		-	16	-	Bits	
Sampling rate		-	8	-	kHz	-
Bypass Mode ADC Analog Characteristics						
Signal to Distortion Ratio		35	38	-	dB	0dB Input: m/A Law command
		-	70	-	dB	0dB Input: Linear
		28	29.5	-	dB	-40dB Input: m-Law command
			29			-40dB Input: A-Law command
		23	25	-	dB	-45dB Input: m-Law command
			24			-45dB Input: A-Law command
Signal to Noise Ratio		80	-	-	dB	0dB Input: Linear
Offset Error		-	-	±20	mV	-
Input Voltage Range		-	1.6	-	Vpp	-
DAC Analog Characteristics With 0dB DAC Gain (Note: The performance over 1.6Vp-p output will be reduced.)						
Signal to Distortion Ratio		35	38	-	dB	0dB Input: m/A Law command
		-	-	80	dB	0dB Input: Linear
		30	33.5	-	dB	-40dB Input: m-Law command
		29	32			-40dB Input: A-Law command
		25	30	-	dB	-45dB Input: m-Law command
		24	27			-45dB Input: A-Law command
Signal to Noise Ratio		80	-	-	dB	0dB Input: Linear
Output Voltage Range		-	1.337	-	Vp-p	0 dB Gain
		-	1.683	-	Vp-p	2 dB Gain
		-	2	-	Vp-p	3.5 dB Gain
Output Current		-	1mA	-		-
Output Load		4.7	10		KΩ	purely resistive load
Offset Error		-	-	±20	mV	-
Power Supply						
Power consumption (2.5v Operating Mode) Analog + Digital		-	- 17 -	- 20 -	mW	-
Power consumption (2.5v Power-down Mode)		-	125	-	uW	This power down current can be measured only when ADPWD and PAPWD activated (both high active) simultaneously

ACELECTRICAL CHARACTERISTICS (CONT'D)

(Measurement Bandwidth is 20Hz - 4KHz. Full scale input sine wave 1KHz, FS=8KHz, @VDD25AA1, VDD25AD1=2.5V, Ta=25°C ,Unless otherwise specified.)

AFE + ADC Analog Characteristics						
* Signal to Distortion Ratio		-	70	-	dB	0dB Input: Linear
		-	70	-	dB	0dB Input: Linear
Offset Error		-	-	±20	mV	-
Input Voltage Range		-	1.6	-	Vpp	-

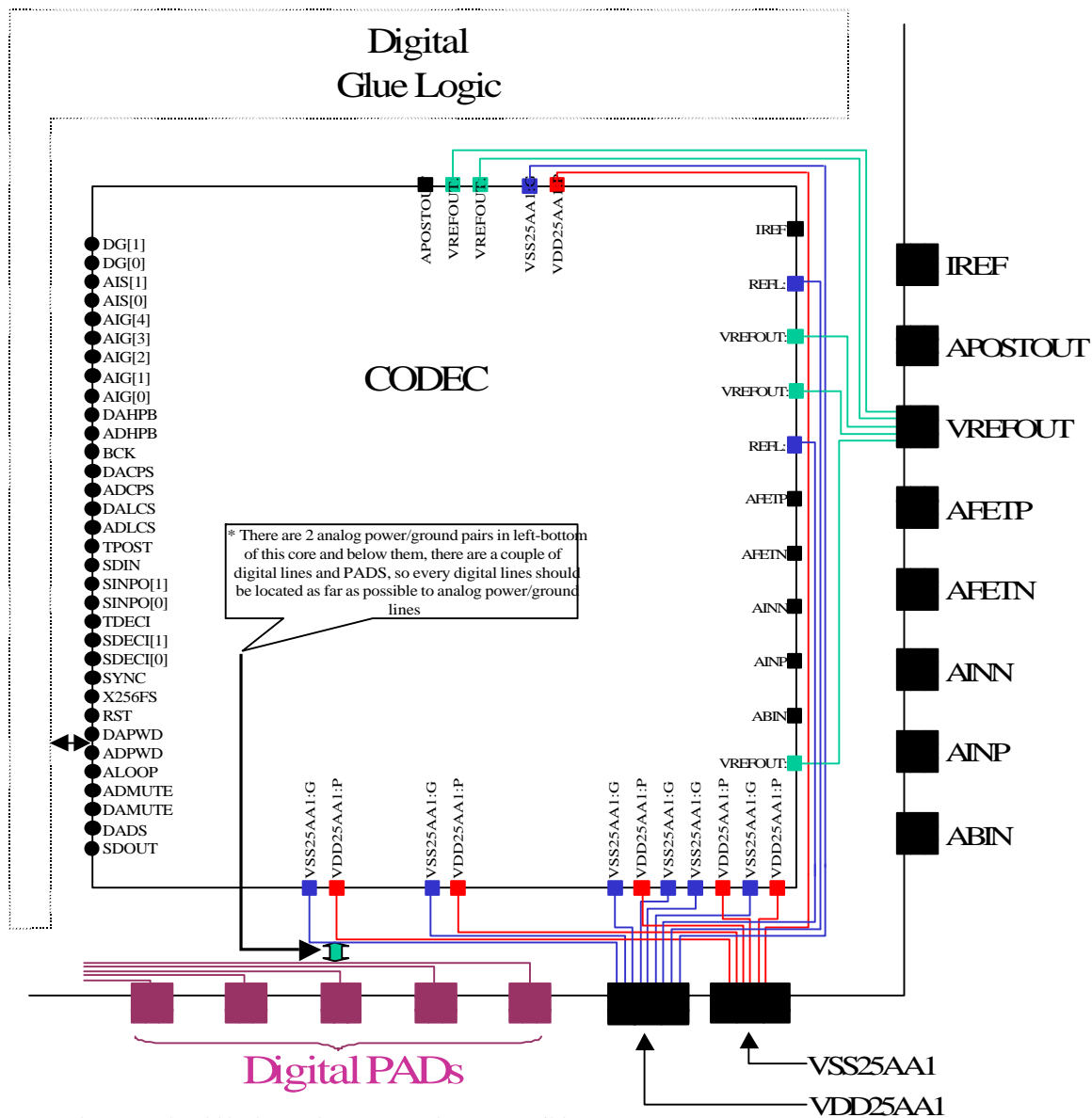
CORE CONFIGURATION AND PIN INFORMATION FOR TEST



Pin Information For Test (Cont'd)

Name	I/O Type	I/O Pad	Pin Type for Test
VDD25AA1	AP	vdd2t_abb	dedicated
VSS25AA1	AG	vss2t_abb	dedicated
IREF	AO	poa_abb	dedicated
REFL	AG	vss1t_abb	dedicated * But if there are not enough pins available, the end user could connect this pin to VSS25AA1, but in this case REFL and VSS25AA1 should be met only at VSS25AA1 PAD
AINP	AI	pia_abb	dedicated
AINN	AI	pia_abb	dedicated
AFETP	AO	poa_abb	dedicated
AFETN	AO	poa_abb	dedicated
DAMUTE	DI	picc_abb	controlled by customer logic
ADMUTE	DI	picc_abb	controlled by customer logic
ALOOP	DI	picc_abb	tied to Ground ("L")
VREFOUT	AO	poa_abb	dedicated
ABIN	AI	pia_abb	dedicated
APOSTOUT	AO	poa_abb	dedicated
AIG[4:0]	DI	picc_abb	accessible for codec test mode, muxed pin
AIS[1:0]	DI	picc_abb	accessible for codec test mode, muxed pin
DG[1:0]	DI	picc_abb	accessible for codec test mode, muxed pin
ADPWD	DI	picc_abb	controlled by customer logic
DAPWD	DI	picc_abb	controlled by customer logic
RST	DI	picc_abb	controlled by customer logic
X256FS	DI	picc_abb	accessible for codec test mode, muxed pin
SYNC	DI	picc_abb	accessible for codec test mode, muxed pin
SDECI[1:0]	DI	picc_abb	tied to Ground ("LL")
TDECI	DI	picc_abb	tied to Ground ("L")
SINPO[1:0]	DI	picc_abb	tied to Ground ("LL")
SDIN	DI	picc_abb	accessible for codec test mode, muxed pin
TPOST	DI	picc_abb	tied to Ground ("L")
ADLCS	DI	picc_abb	controlled by customer logic
DALCS	DI	picc_abb	controlled by customer logic
ADCPS	DI	picc_abb	controlled by customer logic
DACPS	DI	picc_abb	controlled by customer logic
VSS25AD1	DG	vss2t_abb	dedicated
VDD25AD1	DP	vdd2t_abb	dedicated
SDOUT	DO	pot2_abb	accessible for codec test mode, muxed pin
BCK	DI	picc_abb	accessible for codec test mode, muxed pin
DADS	DO	pot2_abb	accessible for codec test mode, muxed pin
ADHPB	DI	picc_abb	controlled by customer logic
DAHBPB	DI	picc_abb	controlled by customer logic

CORE LAYOUT GUIDE

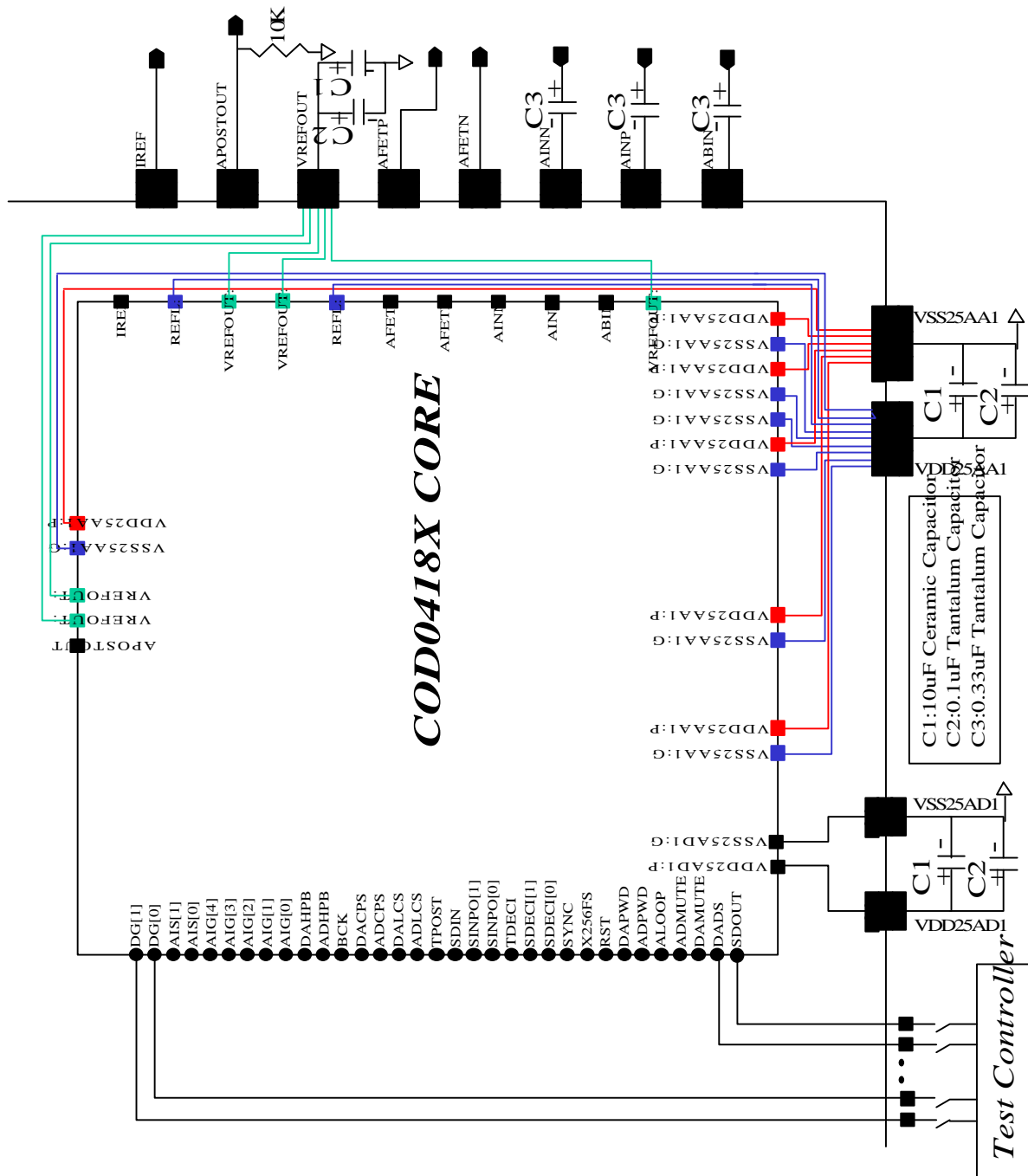


- Analog core should be located to PADS as close as possible.
- Recommended Power/Ground Line Width $\geq 10\mu\text{m}$.
- There are only one Power PAD and only one Ground PAD respectively, but there are 6 Power Ports and 7 Ground Ports on GDS. So each power/ground line should be connected to PADS and merged on the power/ground pad only.
- Similarly, there two REFL ports on GDS, and these two ports should be merged only on analog ground PAD.
- There are also 5 VREFOUT ports on GDS, in similar manner, these should be connect to VREFOUT PAD and merged on that PAD.
- It's good for analog core performance to give some space between analog core and digital glue logic, and recommended space between analog core and digital glue logic is over $100\mu\text{m}$ but if not available space, this should be at least $50\mu\text{m}$.

NOTES:

1. The layout of cod0418x consists of digital part and analog part. The digital part and the analog part should be divided.
2. It is recommended that you use thick analog power metal ($>10\mu\text{m}$). when connecting to PAD, and the path should be as short as possible.
3. Digital power and analog power should be used separately.

CORE EVALUATION GUIDE



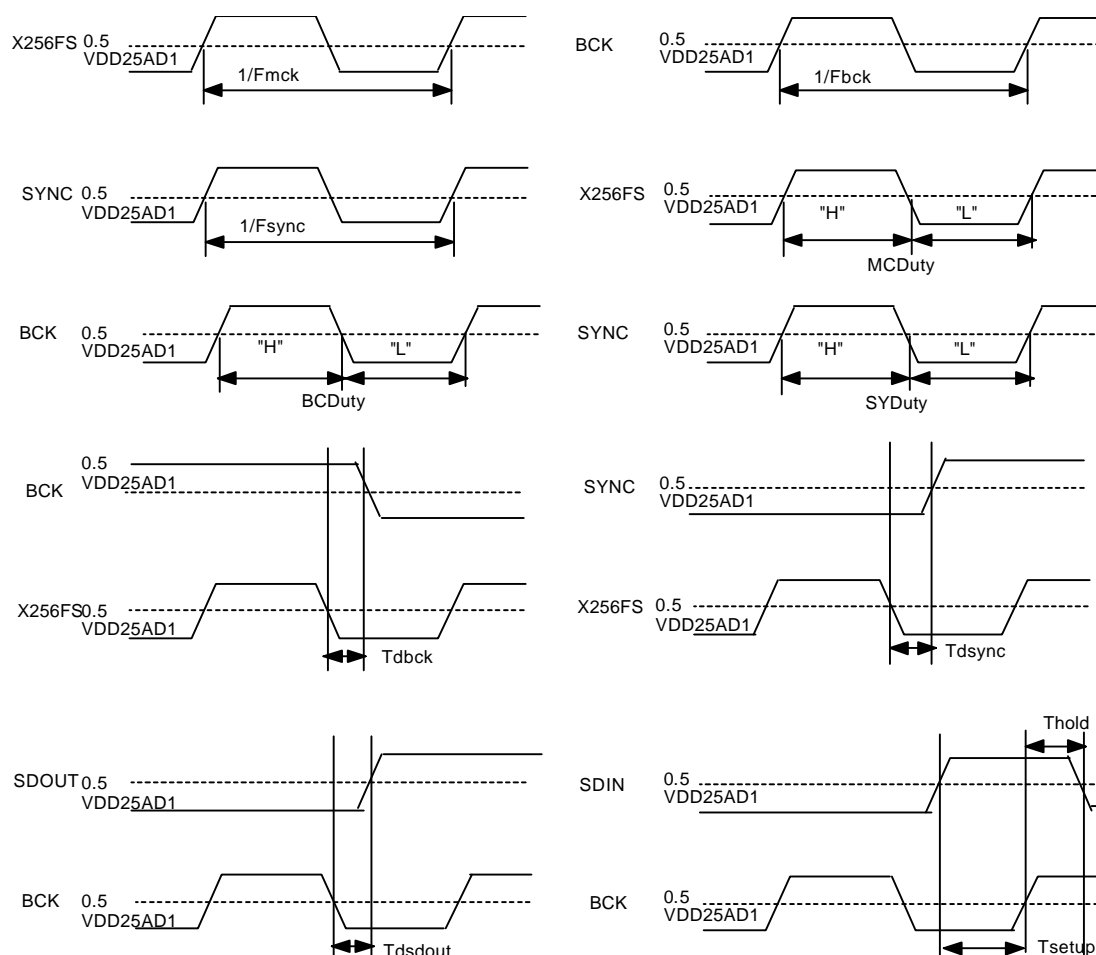
<The Connection User Guide Line for Embedded Core Test>

NOTES:

1. This core configuration is for test of analog and digital characteristics described in page 3-5 and in addition, all digital control pins described in page 10, should be accessible for test of proper functions.
2. The analog power/ground must be separated from digital power/ground.
3. Power typical value: VDD25AA1 = VDD25AD1 = 2.5V, VSS25AA1 = VSS25AD1 = 0.0V

CONTROL CLOCKS CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
X256FS Frequency	Fmck	-	2.048	-	MHz
BCK Frequency	Fbck	-	128	-	kHz
SYNC Frequency	Fsync	-	8	-	kHz
X256FS Duty cycle (H:L)	MCDuty	40:60	50:50	60:40	%
BCK Duty cycle (H:L)	BCDuty	40:60	50:50	60:40	%
SYNC Duty cycle (H:L)	SYDuty	40:60	50:50	60:40	%
X256FS Falling and BCK Edge Delay(Hold)	Tdbck	-	-	15	ns
X256FS Falling and SYNC Edge Delay(Hold)	Tdsync	-	-	15	ns
BCK Falling and SDOUT Delay	Tdsdout	-	-	15	ns
BCK Rising and SDIN Setup	Tsetup	10	15	20	ns
BCK Rising and SDIN Hold	Thold	10	15	20	ns



NOTE: BCK rising edge must NOT occur at the same time as SYNC edge.

TIMING DIAGRAM

The frame of sync clock(SYNC) transitions determine the start of the serial data.

Input data

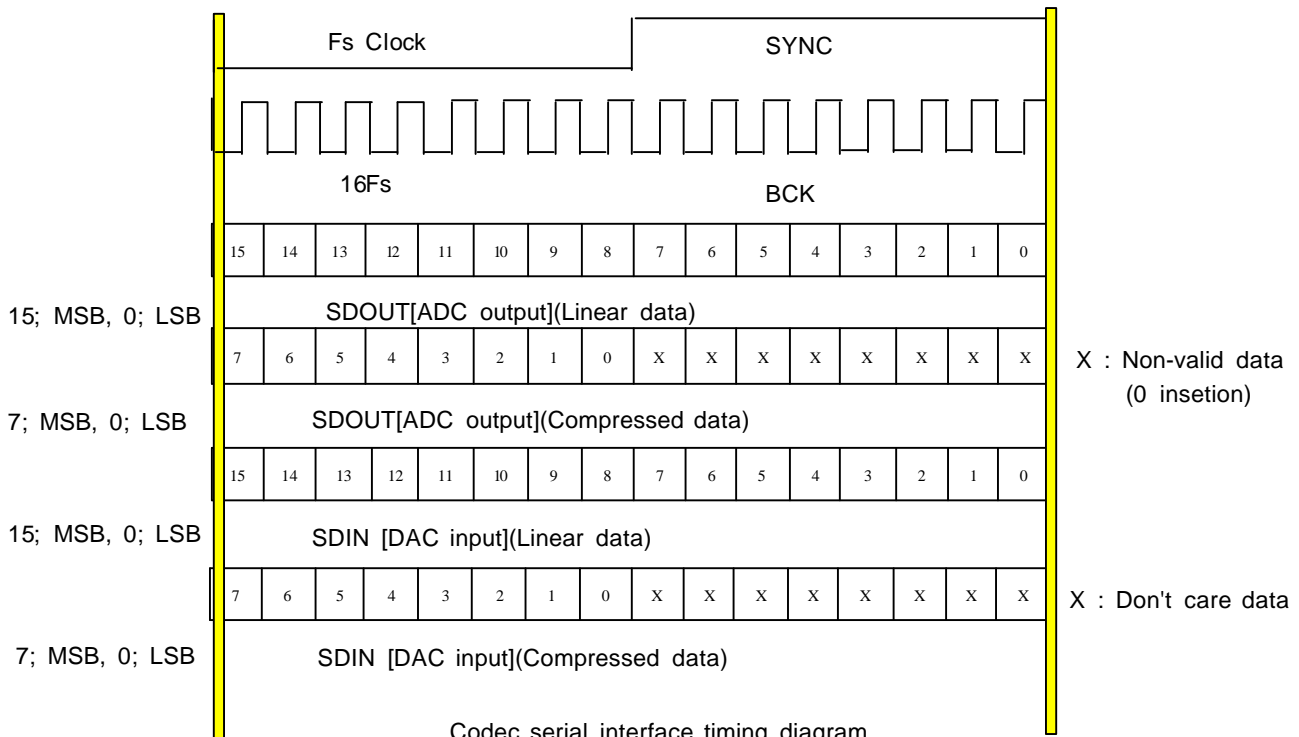
- * All input data are clocked in by the falling edge of BCK.
- * 16bit, 2's complement or 8bit A-law, μ-law data format.

Output data

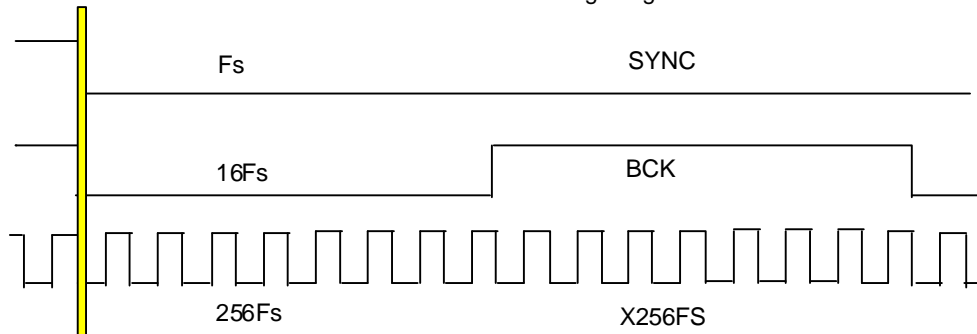
- * All output data are clocked out by the falling edge of BCK.
- * 16bit, 2's complement or 8bit A-law, μ-law data format.

NOTES:

1. SYNC clock is at sampling frequency, F_s .
2. 16-bit linear data has 16-bit serial data format, this is accomplished by $16F_s$ (= F_s clock x 16)

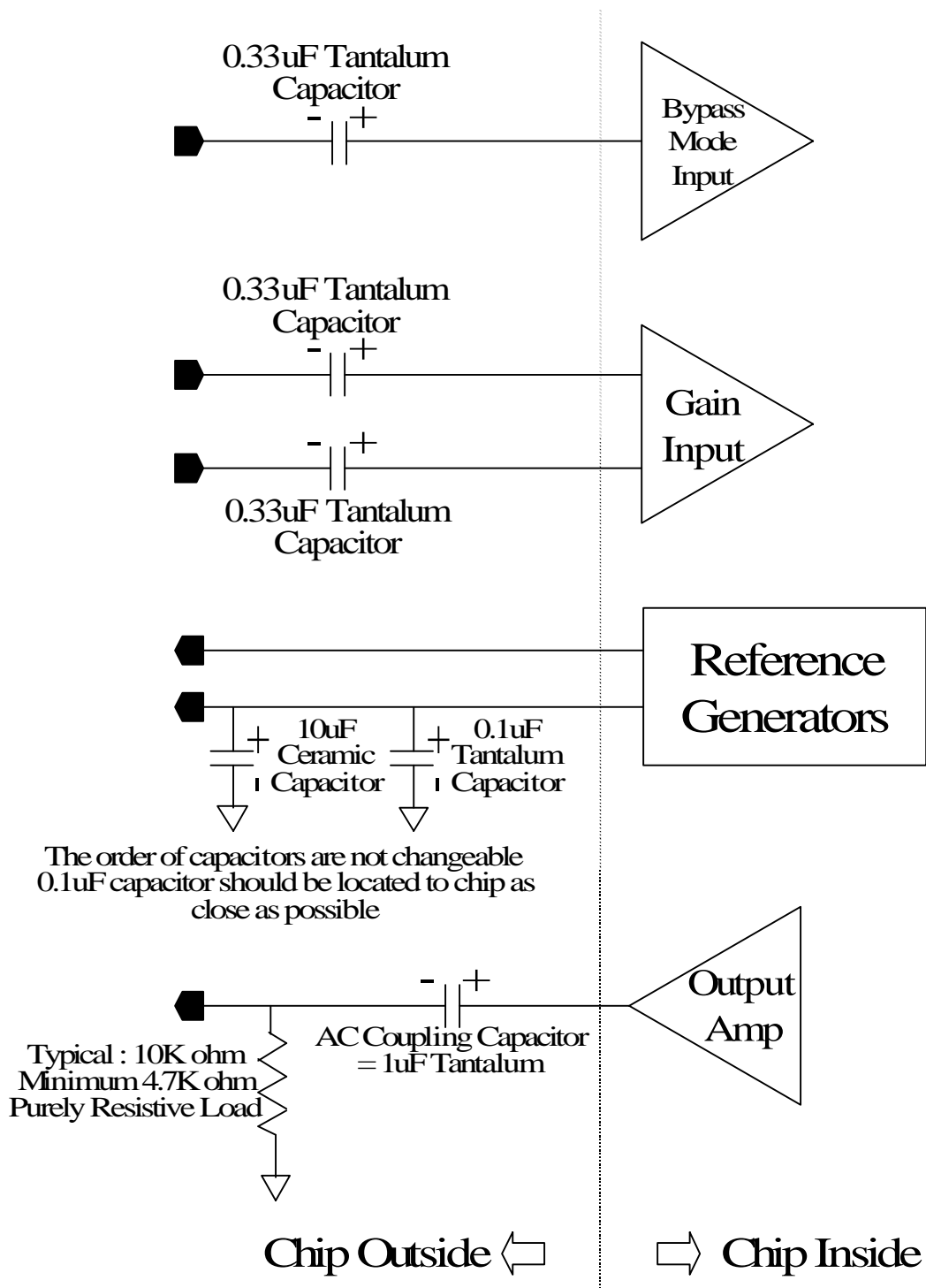


Codec serial interface timing diagram



Codec clock interface timing diagram

INPUT/OUTPUT APPLICATION GUIDE



Core Verilog Modeling Information

COD0418X core modeling file is made by verilog XL. Basically this is a behavioral model and just for checking of connectivity, functions and timing verification only. Because of this is a just behavioral model, the output of this is not exactly same as output of real analog circuit. That means the end user can't measure analog performance from output of this model and output of this model just represents calculated output from logic in model description. And to use this model in design, the end user should refer to annotation in the modeling file and test bench program supplied with this model and modify them to fit their design.

Miscellaneous Information

1. ADC Mute

ADC Mute function will be activated only when ADMUTE (ADC MUTE Pin - High Active) is high. and ADC mute will arise in digital section in ADC.

2. Zero Cross detector in Gain Change.

In DAC gain block, there is a zero cross detector, so only when the analog signal cross the zero range, gain change will arise. and in ADC, no zero cross detector and controller are needed because of cod0418x uses SD modulator in ADC, so every high frequency noise including pop noise in ADC will be eliminated in the digital control blocks in ADC.

3. about ADHPB, DAHPB

ADHPB and DAHPB will change the frequency response of ADC and DAC path respectively.

when ADHPB is low, from 300Hz to 3.2kHz of base-band signal will be transmitted, but when high, from 0Hz to 3.2kHz of signal will be transmitted. and when DAHPB is low, from 300Hz to 3.2KHz of signal will be received, but when high, from 0Hz to 3.2kHz of signal will be received.

DATA SHEET REVISION HISTORY

Version	Date	Modified Items	Comments
Ver 2.0	00.07.31	Core Spec has been completely modified. Every pages has been modified by new specs. So this version is completely irrelevant to previous data sheet.	
Ver 2.1	00.10.23	<p>p1: SDIN pin location of block diagram is corrected. Power consumption changed (15mW → 17mW, 62.5μW → 125μW)</p> <p>p2: REFL and ALOOP pin descriptions are supplemented.</p> <p>p3: Pin descriptions of SDECI[1:0], TDECI, SINPO[1:0], SDIN, TPOST, BCK and DADS are supplemented. ADCPS and DACPS have been corrected in the previous version of data sheet these had been reversed.</p> <p>p6: power consumption changed (15mW → 17mW typical) power down power changed (62.5μW → 125μW)</p> <p>p8: Core configuration page removed and core configuration and pin information for test are merged.</p> <p>p10: Note number 1 is added to "Core Layout Guide".</p> <p>p11: Note number 1 is amended.</p> <p>p12: BCK Frequency changed (256kHz → 128kHz) Typical and minimum values of Tdbck, Tdsync and Tdsdout are removed. Typo of timing diagram corrected (in 4th row of 2nd column BCK→SYNC)</p> <p>p13: Note number 2 is amended (14bit →16bit) and comments about don't care bits are removed. MSB signs of diagram corrected (13 → 15) Comments of diagram concerning don't care bits are removed.</p> <p>p15: Miscellaneous information about ADC mute, zero crossing, ADC and DAC high pass filter functions are supplemented.</p>	
Ver 2.2	00.12.08	<p>p2: I/O Pad changed from vdd1t_abb/vss1t_abb to vdd2t_abb/vss2t_abb</p> <p>p3: - I/O Pad changed from vdd1t_abb/vss1t_abb to vdd2t_abb/vss2t_abb - Typos corrected</p> <p>p6: Minimum output load changed from 10K ohm to 4.7ohm, typical 10k ohm</p> <p>p9: I/O Pad changed from vdd1t_abb/vss1t_abb to vdd2t_abb/vss2t_abb</p> <p>p10: Core layout guide changed</p> <p>p11: Core evaluation guide changed</p> <p>p14: Output application guide added</p> <p>p15: Typos about ADHPB and DAHPB are corrected</p>	
Ver 2.3	00.12.21	<p>all pages; preliminary sign eliminated</p> <p>p7: AFE+ADC performance changed to typical 70dB</p> <p>p7: total harmonic distortion item eliminated</p>	