

64Mbit DDR SDRAM

512K x 32Bit x 4 Banks

Double Data Rate Synchronous DRAM

with Bi-directional Data Strobe and without DLL

Revision 1.2

February 2001

Samsung Electronics reserves the right to change products or specification without notice.

Revision History

Revision 1.2 (February 1, 2001)

- Corrected timing diagram on page 28,32.
- Removed K4D623237A-QC50

Revision 1.1 (July 12, 2000)

- Removed Block Write function. Accordingly pin number 52 must be connected to low (MCL only)
- Removed Write Interrupted by Read function.
- Changed ICC1/ICC2N/ICC3N/ICC5 of K4D623237A-* in "DC Characteristics" table.
- Changed DC operating conditions
 - VREF from 1.15V(min)/1.35V(max) to $0.49 \times V_{DDQ}/0.51 \times V_{DDQ}$
 - VIH/VIL from VREF+0.18(min)/VREF-0.18(max) to VREF+0.15(min)/VREF-0.15(max)

Revision 1.0 (May 16, 2000)

- Changed tCDLR from 1CLK to 2CLK
- Changed tRPST from 0.9/1.1tCK to 0.4/0.5tCK
- Changed tAC(max) and tACS(max) of K4D623237A-QC70 from 5.5ns to 6.0ns

Revision 0.1 (April 24, 2000) - Preliminary

- Changed tCDLR from 2CLK to 1CLK

Revision 0.0 (February 2, 2000) - Target

- Defined Target Specification

**512K x 32Bit x 4 Banks Double Data Rate Synchronous DRAM
with Bi-directional Data Strobe and without DLL****FEATURES**

- 3.3V \pm 5% power supply for device operation
- 2.5V \pm 5% power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
 - Read latency 3 (clock)
 - Burst length (2, 4, 8 and Full page)
 - Burst type (sequential & interleave)
- Full page burst length for sequential burst type only
- Start address of the full page burst should be even
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- Data I/O transactions on both edges of Data strobe
- Data input & output & DM are synchronized with DQS
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 16ms refresh period (2K cycle)
- 100pin TQFP package
- Maximum clock frequency up to 183MHz
- Maximum data rate up to 366Mbps/pin

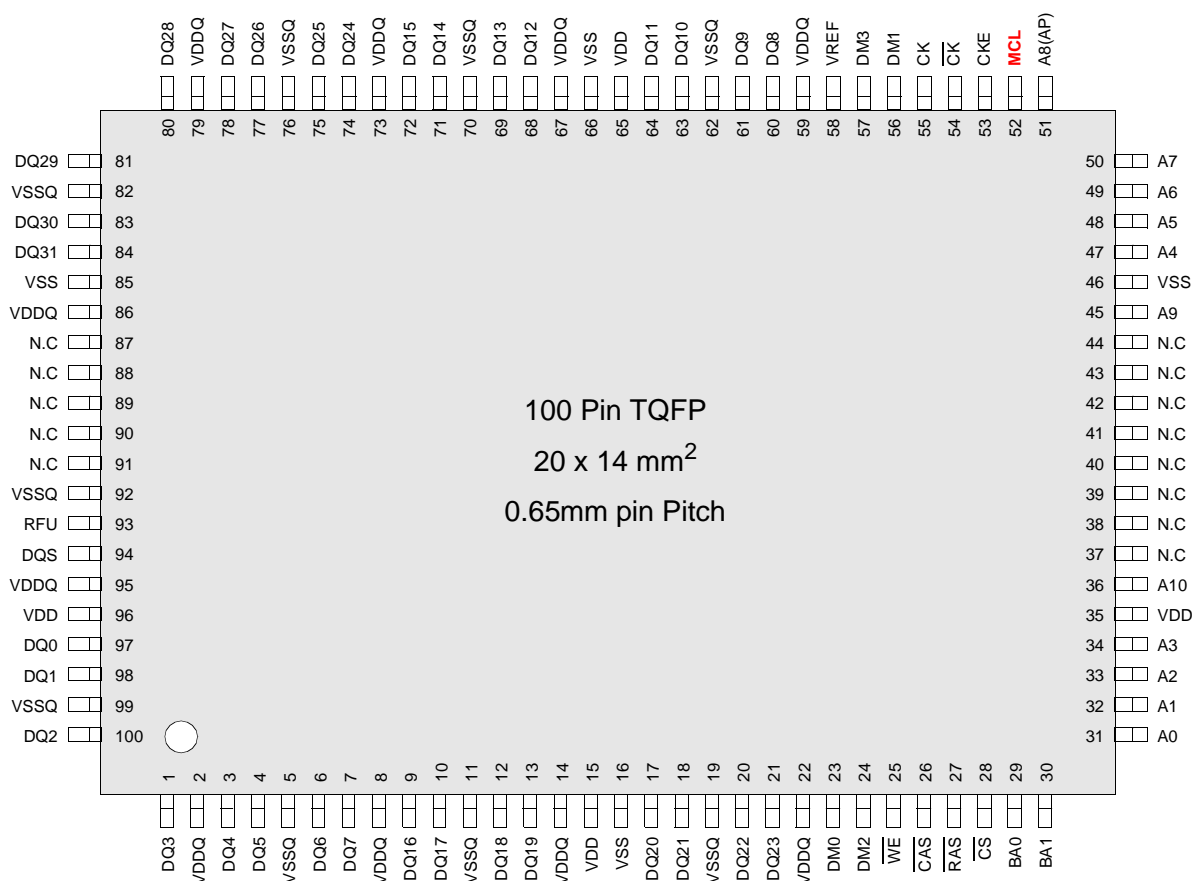
ORDERING INFORMATION

| Part NO. | Max Freq. | Max Data Rate | Interface | Package |
|-----------------|-----------|---------------|-----------|----------|
| K4D623237A-QC55 | 183MHz | 366Mbps/pin | SSTL_2 | 100 TQFP |
| K4D623237A-QC60 | 166MHz | 333Mbps/pin | | |
| K4D623237A-QC70 | 143MHz | 286Mbps/pin | | |

GENERAL DESCRIPTION**FOR 512K x 32Bit x 4 Bank DDR SDRAM**

The K4D623237 is 67,108,864 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 1.5GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

PIN CONFIGURATION (Top View)



PIN DESCRIPTION

| | | | |
|-----------|--------------------------|------------|---------------------|
| CK,CK | Differential Clock Input | BA0, BA1 | Bank Select Address |
| CKE | Clock Enable | A0 ~A10 | Address Input |
| CS | Chip Select | DQ0 ~ DQ31 | Data Input/Output |
| RAS | Row Address Strobe | VDD | Power |
| CAS | Column Address Strobe | VSS | Ground |
| WE | Write Enable | VDDQ | Power for DQ's |
| DQS | Data Strobe | VSSQ | Ground for DQ's |
| DM0 ~ DM3 | Data Mask | MCL | Must Connect Low |
| RFU | Reserved for Future Use | - | - |

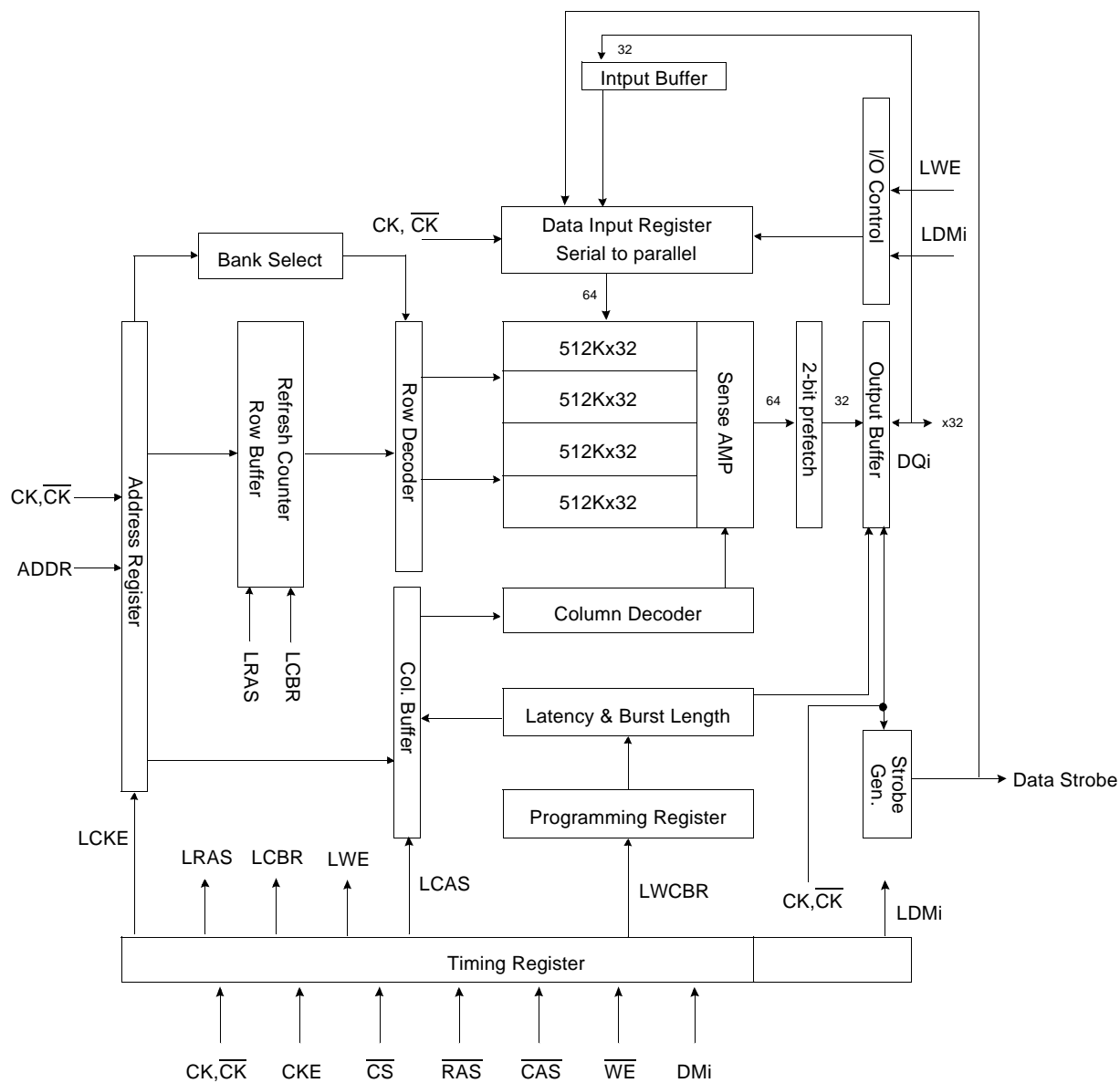
INPUT/OUTPUT FUNCTIONAL DESCRIPTION

| Symbol | Type | Function |
|---------------------------------|--------------|--|
| CK, $\overline{\text{CK}}^{*1}$ | Input | The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS. |
| CKE | Input | Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode. |
| $\overline{\text{CS}}$ | Input | $\overline{\text{CS}}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{\text{RAS}}$ | Input | Latches row addresses on the positive going edge of the CK with $\overline{\text{RAS}}$ low. Enables row access & precharge. |
| $\overline{\text{CAS}}$ | Input | Latches column addresses on the positive going edge of the CK with $\overline{\text{CAS}}$ low. Enables column access. |
| $\overline{\text{WE}}$ | Input | Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active. |
| DQS | Input/Output | Data input and output are synchronized with both edge of DQS. |
| DM0 ~ DM3 | Input | Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM0 for DQ0 ~ DQ7, DM1 for DQ8 ~ DQ15, DM2 for DQ16 ~ DQ23, DM3 for DQ24 ~ DQ31. |
| DQ0 ~ DQ31 | Input/Output | Data inputs/Outputs are multiplexed on the same pins. |
| BA0, BA1 | Input | Selects which bank is to be active. |
| A0 ~ A10 | Input | Row/Column addresses are multiplexed on the same pins. Row addresses : RA0 ~ RA10, Column addresses : CA0 ~ CA7. Column address CA8 is used for auto precharge. |
| VDD/VSS | Power Supply | Power and ground for the input buffers and core logic. |
| VDDQ/VSSQ | Power Supply | Isolated power supply and ground for the output buffers to provide improved noise immunity. |
| VREF | Power Supply | Reference voltage for inputs, used for SSTL interface. |
| MCL | MCL | Must be connected low |

*1 : The timing reference point for the differential clocking is the cross point of CK and $\overline{\text{CK}}$.

For any applications using the single ended clocking, apply VREF to $\overline{\text{CK}}$ pin.

BLOCK DIAGRAM (512Kbit x 32I/O x 4 Bank)



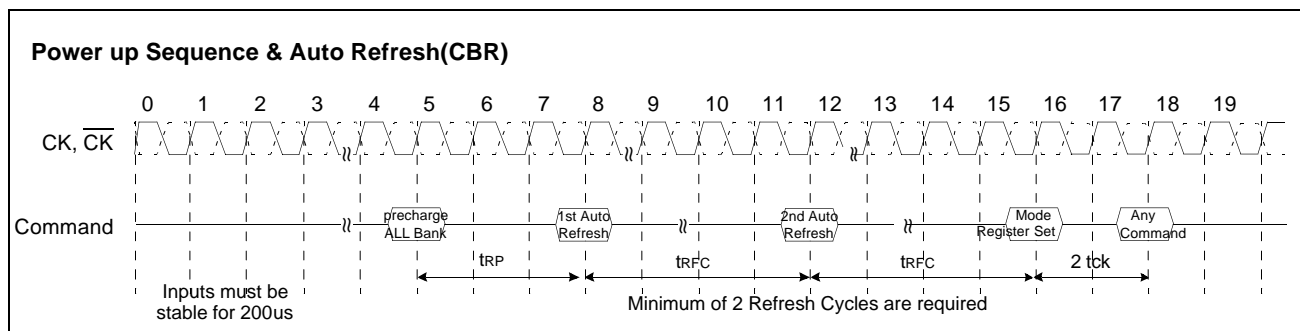
FUNCTIONAL DESCRIPTION

• Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

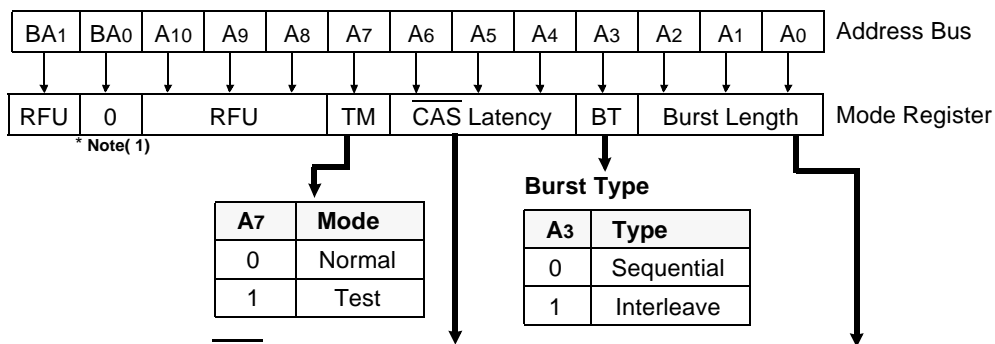
1. Apply power and keep CKE at low state (All other inputs may be undefined)
 - Apply VDD before VDDQ .
 - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock(CK,CK⁻), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue at least 2 or more auto-refresh commands.
6. Issue a mode register set command to initialize the mode register.
- cf) Sequence of 4 & 5 is regardless of the order.

* Mode register must be set just as in spec. Any illegal MRS command can cause unrecoverable malfunction of the device



MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs $\overline{\text{CAS}}$ latency, addressing mode, burst length, test mode and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the DDR SDRAM. The mode register is written by asserting low on $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (The DDR SDRAM should be in active mode with $\overline{\text{CKE}}$ already high prior to writing into the mode register). The state of address pins $\text{A}_0 \sim \text{A}_{10}$ and BA_0 , BA_1 in the same cycle as $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses $\text{A}_0 \sim \text{A}_2$, addressing mode uses A_3 , $\overline{\text{CAS}}$ latency (read latency from column address) uses $\text{A}_4 \sim \text{A}_6$. A_7 is used for test mode. A_7 , A_8 , BA_0 and BA_1 must be set to low for normal DDR SDRAM operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{\text{CAS}}$ latencies.



* RFU(Reserved for future use) should stay "0" during MRS cycle.

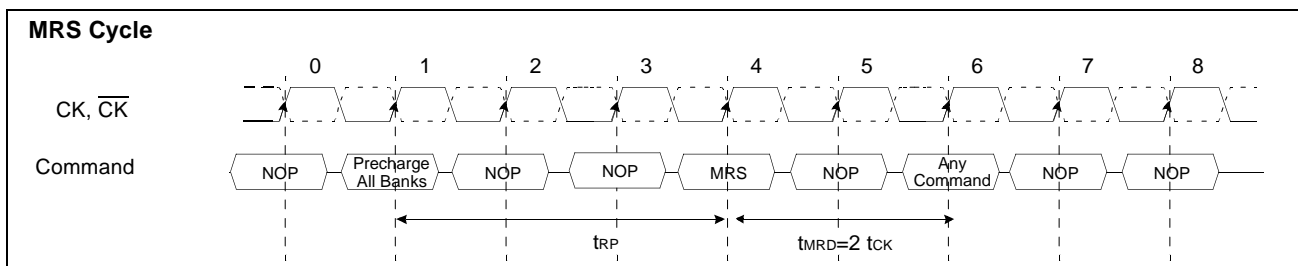
CAS Latency

| A6 | A5 | A4 | Latency |
|----|----|----|---------|
| 0 | 0 | 0 | Reserve |
| 0 | 0 | 1 | Reserve |
| 0 | 1 | 0 | Reserve |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserve |
| 1 | 0 | 1 | Reserve |
| 1 | 1 | 0 | Reserve |
| 1 | 1 | 1 | Reserve |

Burst Length

| A2 | A1 | A0 | Burst Type | |
|----|----|----|------------|------------|
| | | | Sequential | Interleave |
| 0 | 0 | 0 | Reserve | Reserve |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserve | Reserve |
| 1 | 0 | 1 | Reserve | Reserve |
| 1 | 1 | 0 | Reserve | Reserve |
| 1 | 1 | 1 | Full page | Reserve |

Note (1) : BA_0 should be set to "0" during MRS. Otherwise, it will cause malfunction of the device



*1 : MRS can be issued only at all banks precharge state.

*2 : Minimum trp is required to issue MRS command.

BURST MODE OPERATION

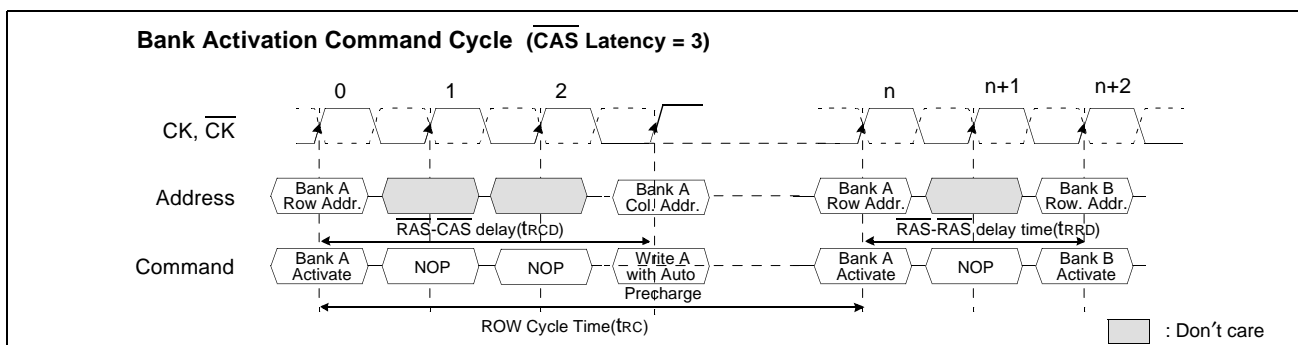
Burst mode operation is used to provide a constant flow of data to memory locations(write cycle), or from memory locations(read cycle). There are two parameters that define how the burst mode operates. These parameters including burst sequence and burst length are programmable and determined by address bits A₀ ~ A₃ during the Mode Register Set command. The burst type is used to define the sequence in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequences are supported, sequential and interleaved. See the below table. The burst length controls the number of bits that will be output after a read command, or the number of bits to be input after a write command. The burst length can be programmed to have values of 2, 4, 8 or Full page. For the full page operation, the starting address must be an even number.

BURST LENGTH AND SEQUENCE

| Burst Length | Starting Address(A ₂ , A ₁ , A ₀) | Sequential Mode | Interleave Mode |
|--------------|---|------------------------|------------------------|
| 2 | xx0 | 0, 1 | 0, 1 |
| | xx1 | 1, 0 | 1, 0 |
| 4 | x00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | x01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | x10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | x11 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 000 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| | 001 | 1, 2, 3, 4, 5, 6, 7, 0 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | 010 | 2, 3, 4, 5, 6, 7, 0, 1 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | 011 | 3, 4, 5, 6, 7, 0, 1, 2 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | 100 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | 101 | 5, 6, 7, 0, 1, 2, 3, 4 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | 110 | 6, 7, 0, 1, 2, 3, 4, 5 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | 111 | 7, 0, 1, 2, 3, 4, 5, 6 | 7, 6, 5, 4, 3, 2, 1, 0 |

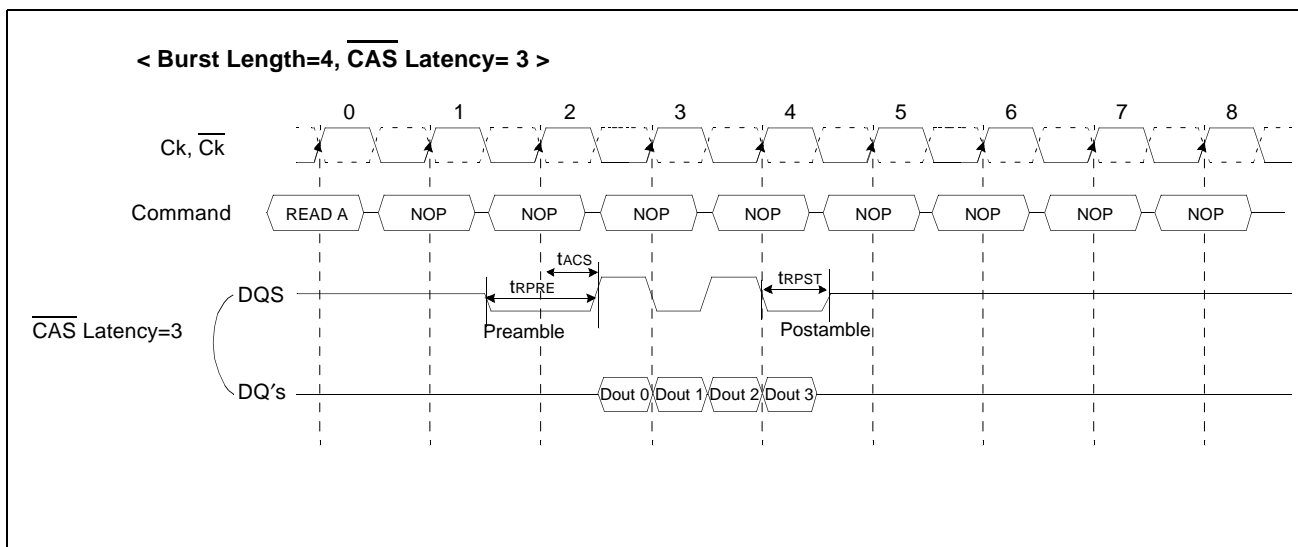
BANK ACTIVATION COMMAND

The Bank Activation command is issued by holding $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ high with $\overline{\text{CS}}$ and $\overline{\text{RAS}}$ low at the rising edge of the clock. The DDR SDRAM has four independent Banks, so two Bank Select addresses(BA₀, BA₁) are supported. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time($t_{\text{RCD min}}$). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time($t_{\text{RRD min}}$).



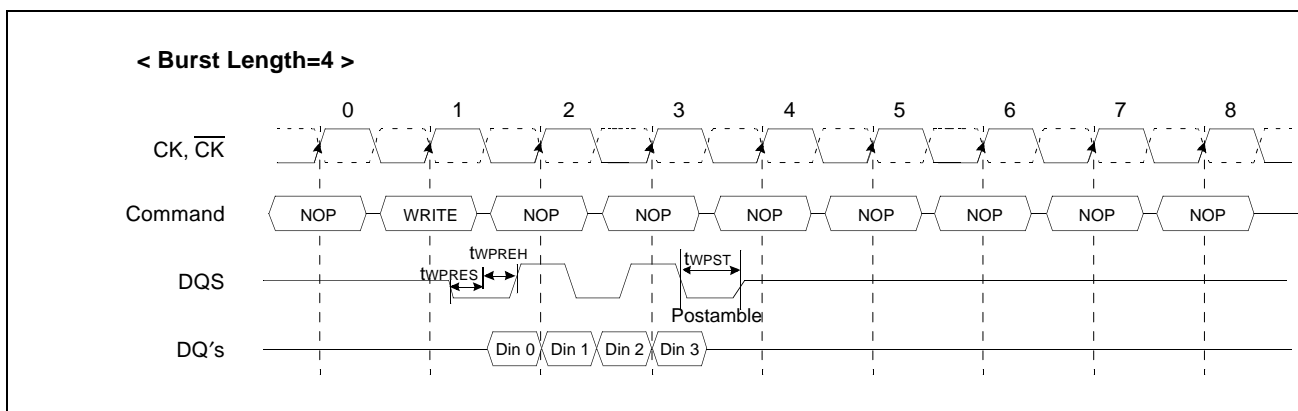
BURST READ OPERATION

Burst Read operation in DDR SDRAM is in the same manner as the current SDRAM such that the Burst read command is issued by asserting \overline{CS} and \overline{CAS} low while holding \overline{RAS} and \overline{WE} high at the rising edge of the clock after t_{RCD} from the bank activation. The address inputs ($A_0 \sim A_7$) determine the starting address for the Burst. The Mode Register sets type of burst (Sequential or interleave) and burst length (2, 4, 8, Full page). The first output data is available after the \overline{CAS} Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe adopted by DDR SDRAM until the burst length is completed.



BURST WRITE OPERATION

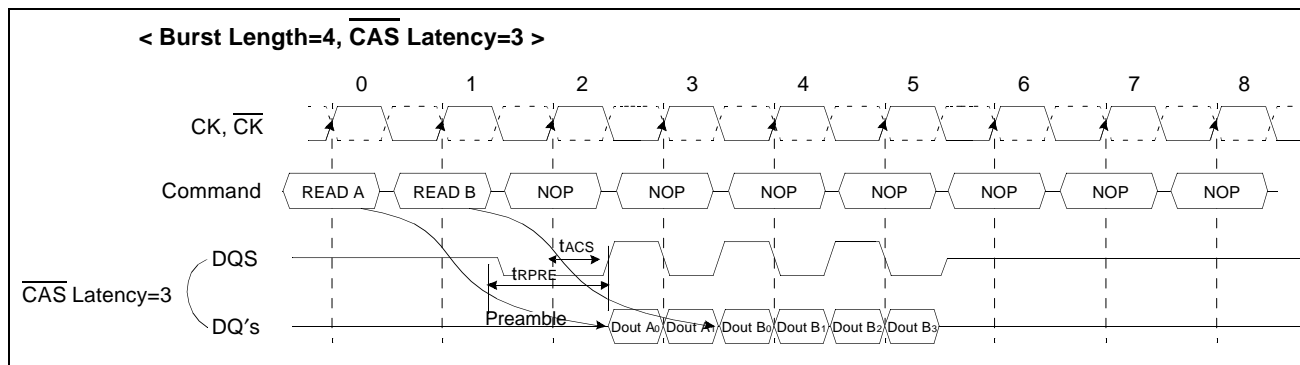
The Burst Write command is issued by having \overline{CS} , \overline{CAS} , and \overline{WE} low while holding \overline{RAS} high at the rising edge of the clock. The address inputs determine the starting column address. There is no real write latency required for burst write cycle. The first data for burst write cycle must be applied at the first rising edge of the data strobe enabled after t_{DQS} from the rising edge of the clock that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.



BURST INTERRUPTION

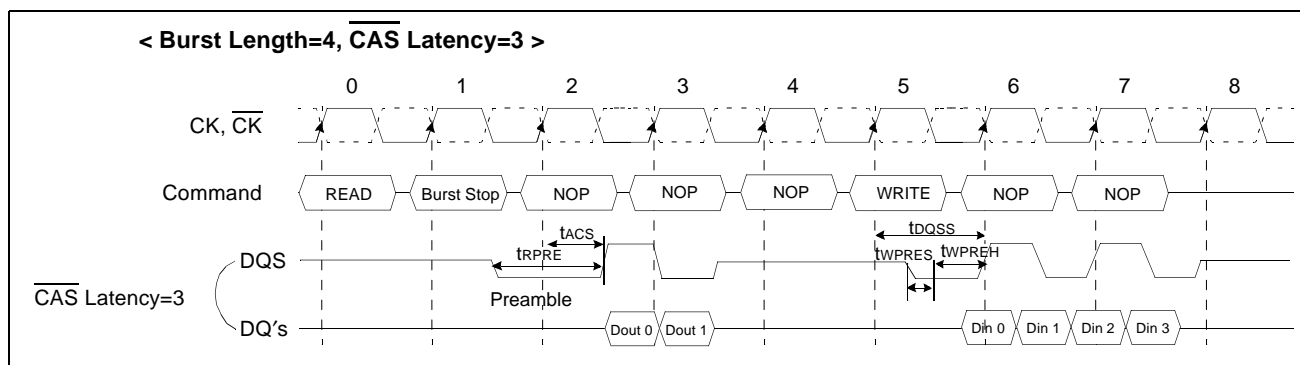
Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 tck.



Read Interrupted by Burst stop & a Write

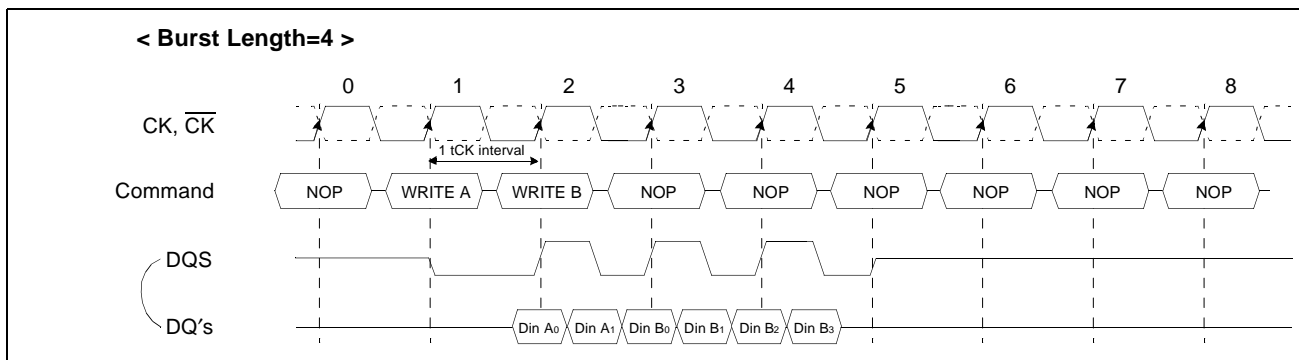
To interrupt a burst read with a write command, Burst stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's (Output drivers) in a high impedance state at least one clock cycle before the Write Command is initiated.



A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the Read to precharge intervals without interrupting a Read burst. A precharge command to output disable latency is equivalent to the CAS latency.

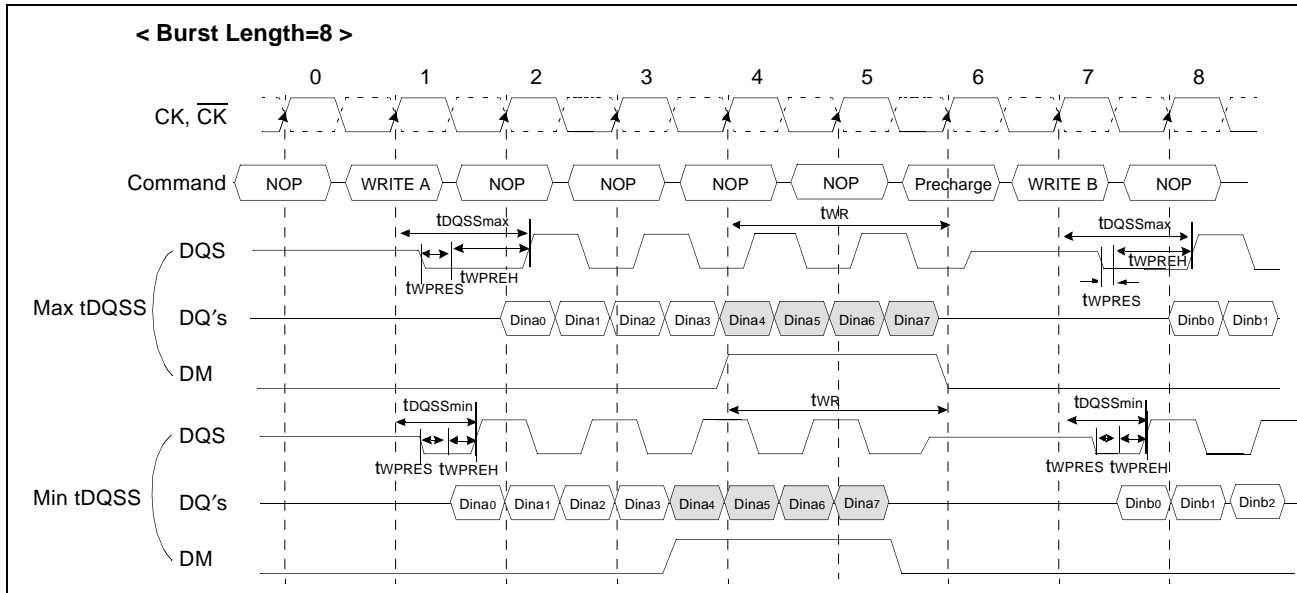


A Burst Write can be interrupted before completion of the burst by the new Write Command, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.



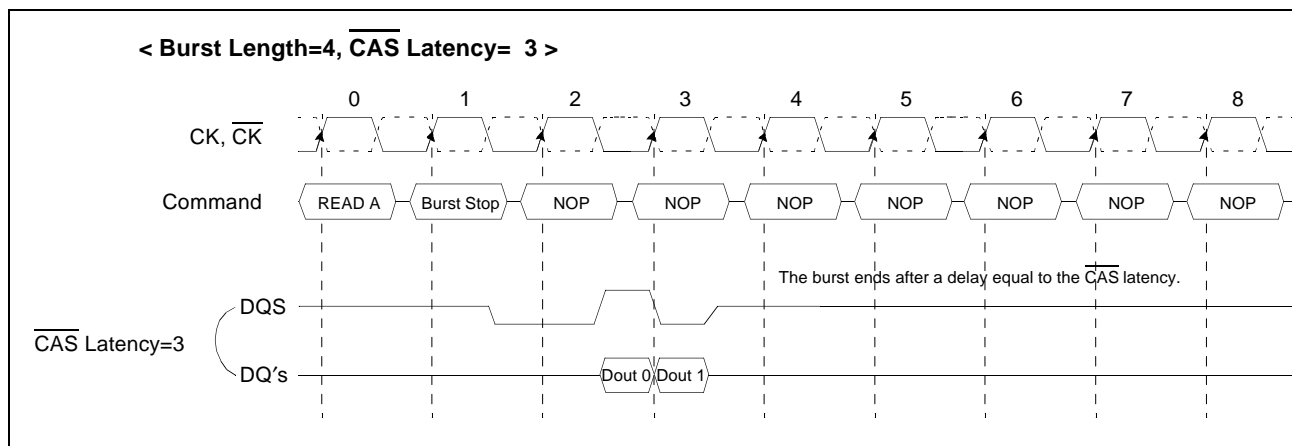
Write Interrupted by a Precharge & DM

A Burst Write operation can be interrupted before completion of the burst by a precharge of the same bank. A Write Recovery time(t_{WR}) is required before a Precharge command to finish the Write operation. When Precharge command is asserted, any residual data from the burst write cycle must be masked by DM.



BURST STOP COMMAND

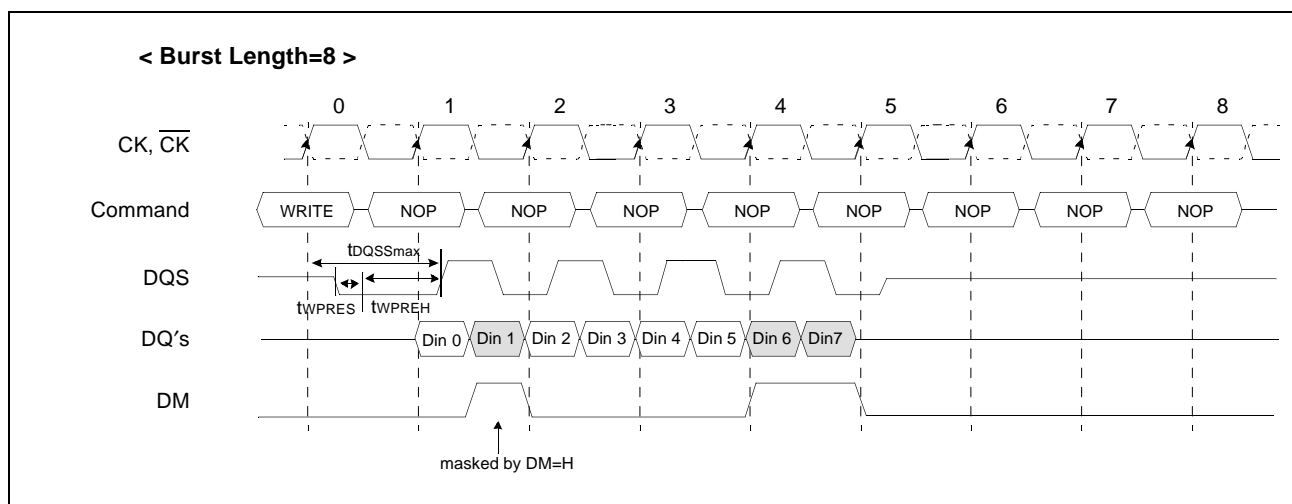
The Burst stop command is initiated by having $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high with $\overline{\text{CS}}$ and $\overline{\text{WE}}$ low at the rising edge of the clock only. The Burst Stop command has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. When the Burst Stop command is issued during a burst read cycle, both the data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the $\overline{\text{CAS}}$ Latency set in the Mode Register. The Burst Stop command, however, is not supported during a write burst operation.



DM FUNCTION

The DDR SDRAM has a Data mask function that can be used in conjunction with data Write cycle only, not Read cycle. When the Data Mask is activated (DM high) during write operation the write data is masked immediately (DM to Data-mask Latency is zero).

DM must be issued at the rising edge or the falling edge of Data Strobe instead of a clock edge.

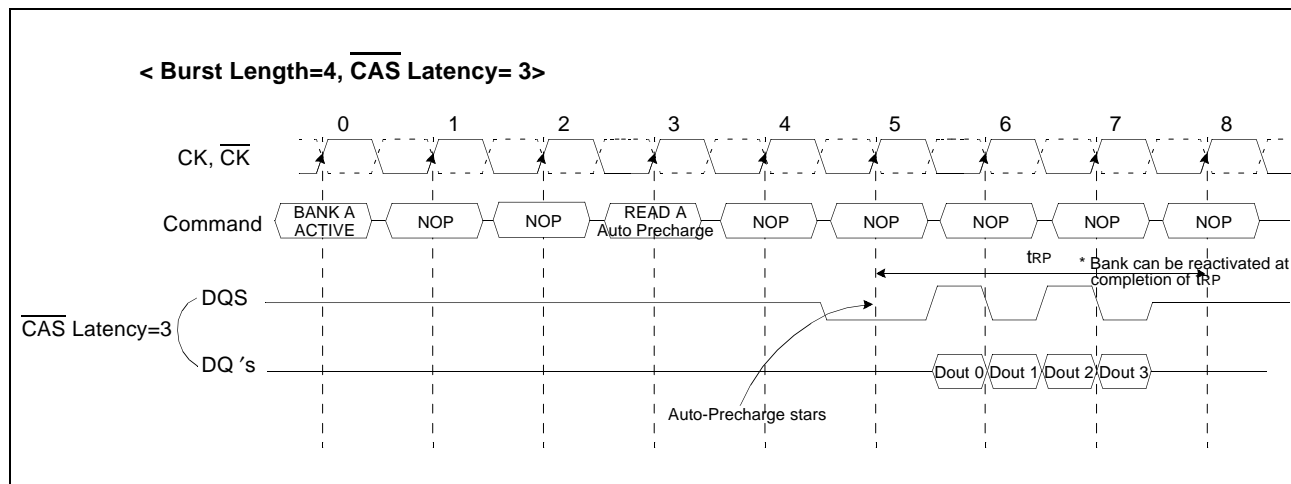


AUTO-PRECHARGE OPERATION

The Auto precharge command can be issued by having column address A8 High when a Read or a Write command is asserted into the DDR SDRAM. If A8 is low when Read or Write command is issued, then normal Read or Write burst operation is asserted and the bank remains active after the completion of the burst sequence. When the Auto precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during read or write cycle after $t_{RAS}(\min)$ is satisfied.

Read with Auto Precharge

If a Read with Auto-precharge command is initiated, the DDR SDRAM automatically starts the precharge operation on $BL/2$ clock later from a Read with Auto-Precharge command when $t_{RAS}(\min)$ is satisfied. If not, the start point of precharge operation will be delayed until $t_{RAS}(\min)$ is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the Precharge time(t_{RP}) has been satisfied.



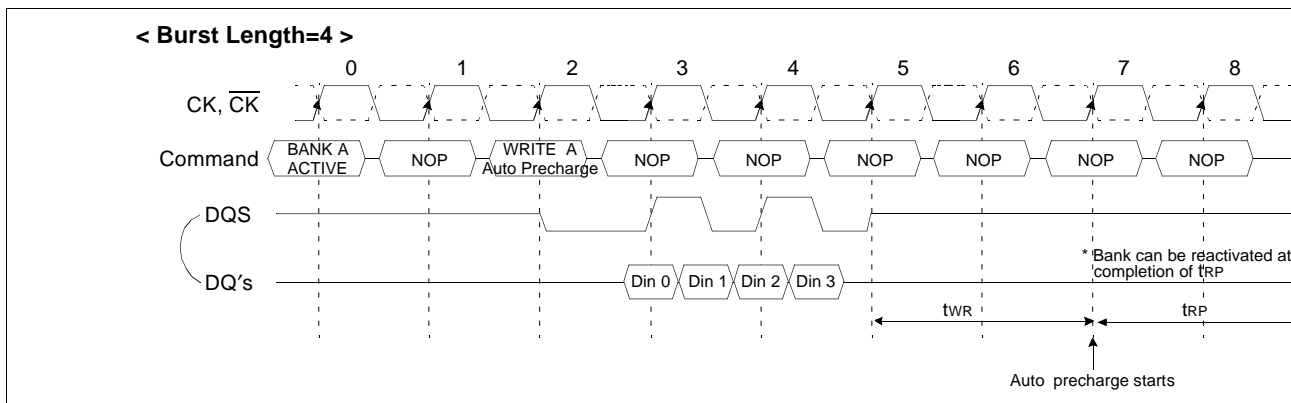
When the Read with Auto precharge command is issued, new command can be asserted at T_4, T_5 and T_6 respectively as follows, even the new command for the same bank is illegal.

| Asserted command | For same Bank | | | For Different Bank | | |
|------------------|----------------|-------------|---------|--------------------|-------|-------|
| | 4 | 5 | 6 | 4 | 5 | 6 |
| Read Interrupt | READ + NO AP*1 | READ+ NO AP | Illegal | Legal | Legal | Legal |
| Active | Illegal | Illegal | Illegal | Legal | Legal | Legal |
| Precharge | Illegal | Illegal | Illegal | Legal | Legal | Legal |

*1 : AP = Auto Precharge

Write with Auto Precharge

If A8 is high when Write command is issued, the write with Auto-Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping $t_{RD}(min)$.



PRECHARGE COMMAND

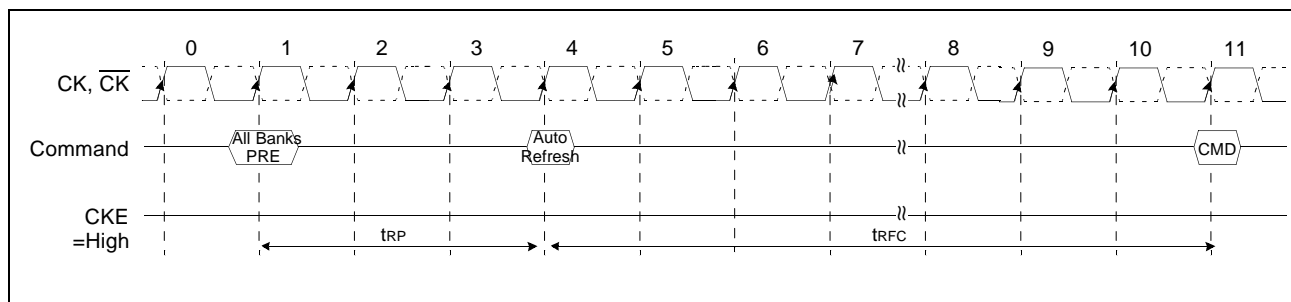
The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when CS, RAS and WE are low and CAS is high at the rising edge of the clock, CK. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The Bank select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, $t_{WR}(min)$ must be satisfied from the start of the last burst write cycle until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

< Bank Selection for Precharge by Bank address bits >

| A8/AP | BA1 | BA0 | Precharge |
|-------|-----|-----|-------------|
| 0 | 0 | 0 | Bank A Only |
| 0 | 0 | 1 | Bank B Only |
| 0 | 1 | 0 | Bank C Only |
| 0 | 1 | 1 | Bank D Only |
| 1 | X | X | All Banks |

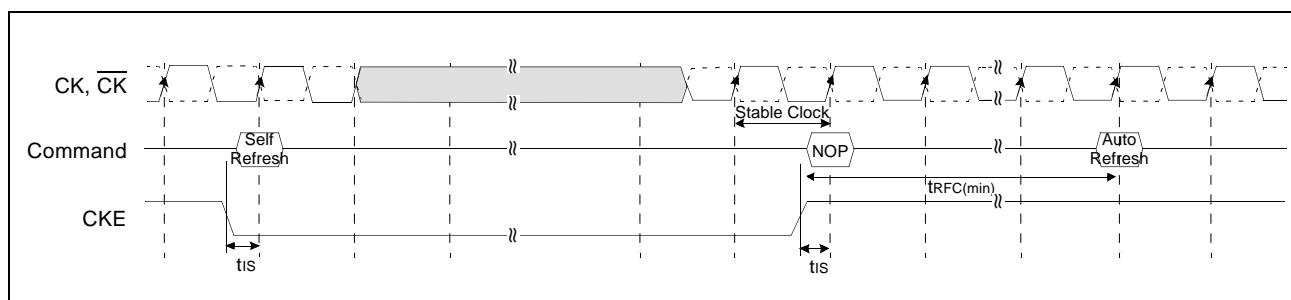
AUTO REFRESH

An Auto Refresh command is issued by having \overline{CS} , \overline{RAS} and \overline{CAS} held low with CKE and \overline{WE} high at the rising edge of the clock, CK. All banks must be precharged and idle for a $t_{RP}(\text{min})$ before the Auto Refresh command is applied. No control of the external address pins is required once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the $t_{RFC}(\text{min})$.



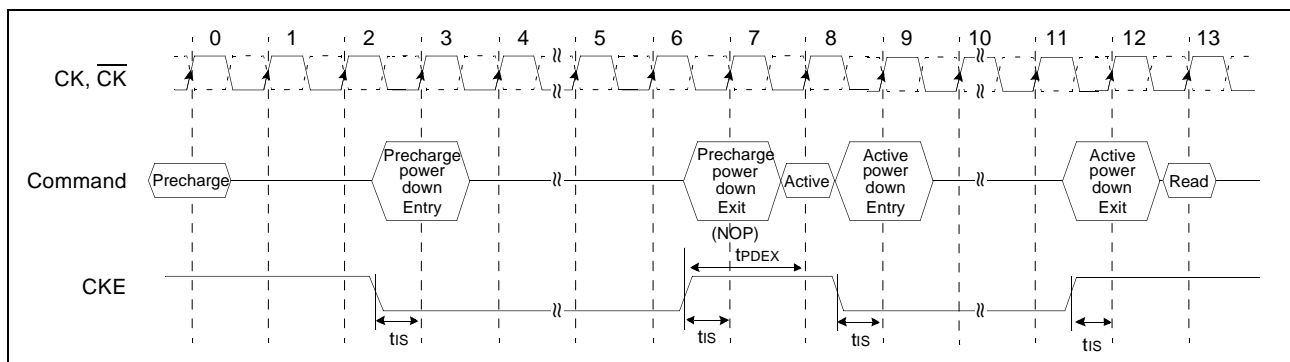
SELF REFRESH

A Self Refresh command is defined by having \overline{CS} , \overline{RAS} , \overline{CAS} and CKE held low with \overline{WE} high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 1 clock cycle from the self refresh command, all of the external control signals including system clock (CK, \overline{CK}) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. To exit the Self Refresh mode, supply stable clock input before returning CKE high, assert deselect or NOP command and then assert CKE high. The Auto Refresh is required before self refresh entry and after self refresh exit.



POWER DOWN MODE

The power down is entered when CKE Low, and exited when CKE High. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. The both bank should be in idle state prior to entering the precharge power down mode and CKE should be set high at least $1 \text{ tCK} + \text{tIS}$ prior to Row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot remain in power down mode longer than the refresh period (t_{REF}) of the device.



SIMPLIFIED TRUTH TABLE

| COMMAND | | | CKEn-1 | CKEn | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | DM | BA0,1 | A8/AP | A10,A9,A7~A0 | Note |
|---------------------------|------------------------|-------|--------|------|-----------------|------------------|------------------|-----------------|----|---------|-------------|----------------|------|
| Register | Mode Register Set | | H | X | L | L | L | L | X | OP CODE | | | 1, 2 |
| Refresh | Auto Refresh | | H | H | L | L | L | H | X | X | | | 3 |
| | Self Refresh | Entry | | L | | | | | | | | | 3 |
| | | Exit | L | H | L | H | H | H | X | X | | | 3 |
| | | | | | H | X | X | X | | | | | 3 |
| Bank Active & Row Addr. | | | H | X | L | L | H | H | X | V | Row Address | | |
| Read & Column Address | Auto Precharge Disable | | H | X | L | H | L | H | X | V | L | Column Address | 4 |
| | Auto Precharge Enable | | | | | | | | | | H | | 4 |
| Write & Column Address | Auto Precharge Disable | | H | X | L | H | L | L | X | V | L | Column Address | 4 |
| | Auto Precharge Enable | | | | | | | | | | H | | 4, 6 |
| Burst Stop | | | H | X | L | H | H | L | X | X | | | 7 |
| Precharge | Bank Selection | | H | X | L | L | H | L | X | V | L | X | |
| | All Banks | | | | | | | | | X | H | | 5 |
| Active Power Down | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | V | V | V | | | | | |
| | | Exit | L | H | X | X | X | X | X | | | | |
| Precharge Power Down Mode | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |
| | | Exit | L | H | H | X | X | X | X | | | | |
| | | | | | L | H | H | H | | | | | |
| DM | | | H | X | | | | | V | X | | | 8 |
| No Operation Command | | | H | X | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code

A0 ~ A10 & BA0 ~ BA1 : Program keys. (@MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.
If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.
If BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank B is selected.
If BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank C is selected.
If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.
5. If A₈/AP is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

FUNCTION TRUTH TABLE

| Current State | CS | RAS | CAS | WE | Address | Command | Action |
|----------------------|----|-----|-----|----|-------------------|--------------|---|
| PRECHARGE STANDBY | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BURST STOP | ILLEGAL*2 |
| | L | H | L | X | BA, CA, A8 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA, RA | ACT | Bank Active, Latch RA |
| | L | L | H | L | BA, A8 | PRE/PREA | NOP*4 |
| | L | L | L | H | X | REFA | AUTO-Refresh*5 |
| | L | L | L | L | Op-Code, Mode-Add | MRS | Mode Register Set*5 |
| ACTIVE STANDBY | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BURST STOP | NOP |
| | L | H | L | H | BA, CA, A8 | READ/READA | Begin Read, Latch CA, Determine Auto-Precharge |
| | L | H | L | L | BA, CA, A8 | WRITE/WRITEA | Begin Write, Latch CA, Determine Auto-Precharge |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA, A8 | PRE/PREA | Precharge/Precharge All |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| READ | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | X | BURST STOP | Terminate Burst |
| | L | H | L | H | BA, CA, A8 | READ/READA | Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3 |
| | L | H | L | L | BA, CA, A8 | WRITE/WRITEA | ILLEGAL |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA, A8 | PRE/PREA | Terminate Burst, Precharge |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

FUNCTION TRUTH TABLE(continued)

| Current State | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Address | Command | Action |
|--------------------------|-----------------|------------------|------------------|-----------------|------------------------|--------------|--|
| WRITE | H | X | X | X | X | DESEL | NOP(Continue Burst END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst END) |
| | L | H | H | L | X | BURST STOP | ILLEGAL |
| | L | H | L | H | BA, CA, A ₈ | READ/READA | Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge*3 |
| | L | H | L | L | BA, CA, A ₈ | WRITE/WRITEA | Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge*3 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA, A ₈ | PRE/PREA | Terminate Burst With DM=High, Precharge |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| READ with AUTO PRECHARGE | H | X | X | X | X | DESEL | NOP(Continue Burst END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst END) |
| | L | H | H | L | X | BURST STOP | ILLEGAL |
| | L | H | L | X | BA, CA, A ₈ | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA, A ₈ | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| WRITE with AUTO RECHARGE | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | X | BURST STOP | ILLEGAL |
| | L | H | L | X | BA, CA, A ₈ | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA, A ₈ | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

FUNCTION TRUTH TABLE(continued)

| Current State | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address | Command | Action |
|----------------|------------------------|-------------------------|-------------------------|------------------------|-------------------|------------|----------------------------|
| PRE-CHARGING | H | X | X | X | X | DESEL | NOP(Idle after tRP) |
| | L | H | H | H | X | NOP | NOP(Idle after tRP) |
| | L | H | H | L | X | BURST STOP | NOP |
| | L | H | L | X | BA, CA, A8 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA, A8 | PRE/PREA | NOP*4(Idle after tRP) |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| ROW ACTIVATING | H | X | X | X | X | DESEL | NOP(ROW Active after tRCD) |
| | L | H | H | H | X | NOP | NOP(ROW Active after tRCD) |
| | L | H | H | L | X | BURST STOP | NOP |
| | L | H | L | X | BA, CA, A8 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA, A8 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

FUNCTION TRUTH TABLE(continued)

| Current State | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Address | Command | Action |
|---------------------|-----------------|------------------|------------------|-----------------|-------------------|--------------|--------------------------|
| WRITE RECOVERING | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | X | BURST STOP | NOP |
| | L | H | L | H | BA, CA, A8 | READ | ILLEGAL*2 |
| | L | H | L | L | BA, CA, A8 | WRITE/WRITEA | New Write, Determine AP. |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA, A8 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| RE- FRESHING | H | X | X | X | X | DESEL | NOP(Idle after trP) |
| | L | H | H | H | X | NOP | NOP(Idle after trP) |
| | L | H | H | L | X | BURST STOP | NOP |
| | L | H | L | X | BA, CA, A8 | READ/WRITE | ILLEGAL |
| | L | L | H | H | BA, RA | ACT | ILLEGAL |
| | L | L | H | L | BA, A8 | PRE/PREA | ILLEGAL |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

ABBREVIATIONS :

H=High Level, L=Low level, V=Valid, X=Don't Care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

Note :

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state ; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Same Bank's previous Auto precharge will not be performed. But if Bank is different, previous Auto precharge will be performed.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

FUNCTION TRUTH TABLE for CKE

| Current State | CKE _{n-1} | CKE _n | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Add | Action |
|-----------------------------------|--------------------|------------------|------------------------|-------------------------|-------------------------|------------------------|---------|-----------------------------------|
| SELF-REFRESHING | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Self-Refresh*1 |
| | L | H | L | H | H | H | X | Exit Self-Refresh*1 |
| | L | H | L | H | H | L | x | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | x | ILLEGAL |
| | L | L | X | X | X | X | X | NOP(Maintain Self-Refresh) |
| PRECHARGE POWER DOWN | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Power Down*2 |
| | L | H | L | H | H | H | X | Exit Power Down*2 |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP(Maintain Power Down) |
| ALL BANKS IDLE | H | H | X | X | X | X | X | Refer to Function True Table |
| | H | L | H | X | X | X | X | Enter Power Down*3 |
| | H | L | L | H | H | H | X | Enter Power Down*3 |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | H | H | RA | Row (& Bank) Active |
| | H | L | L | L | L | H | X | Enter Self-Refresh*3 |
| | H | L | L | L | L | L | OP Code | Mode Register Access |
| | L | X | X | X | X | X | X | Refer to Current State=Power Down |
| Any State other than listed above | H | H | X | X | X | X | X | Refer to Function True Table |
| | H | L | X | X | X | X | X | Begin Clock Suspend next cycle*4 |
| | L | H | X | X | X | X | X | Exit Clock Suspend next cycle*4 |
| | L | L | X | X | X | X | X | Maintain Clock Suspend |

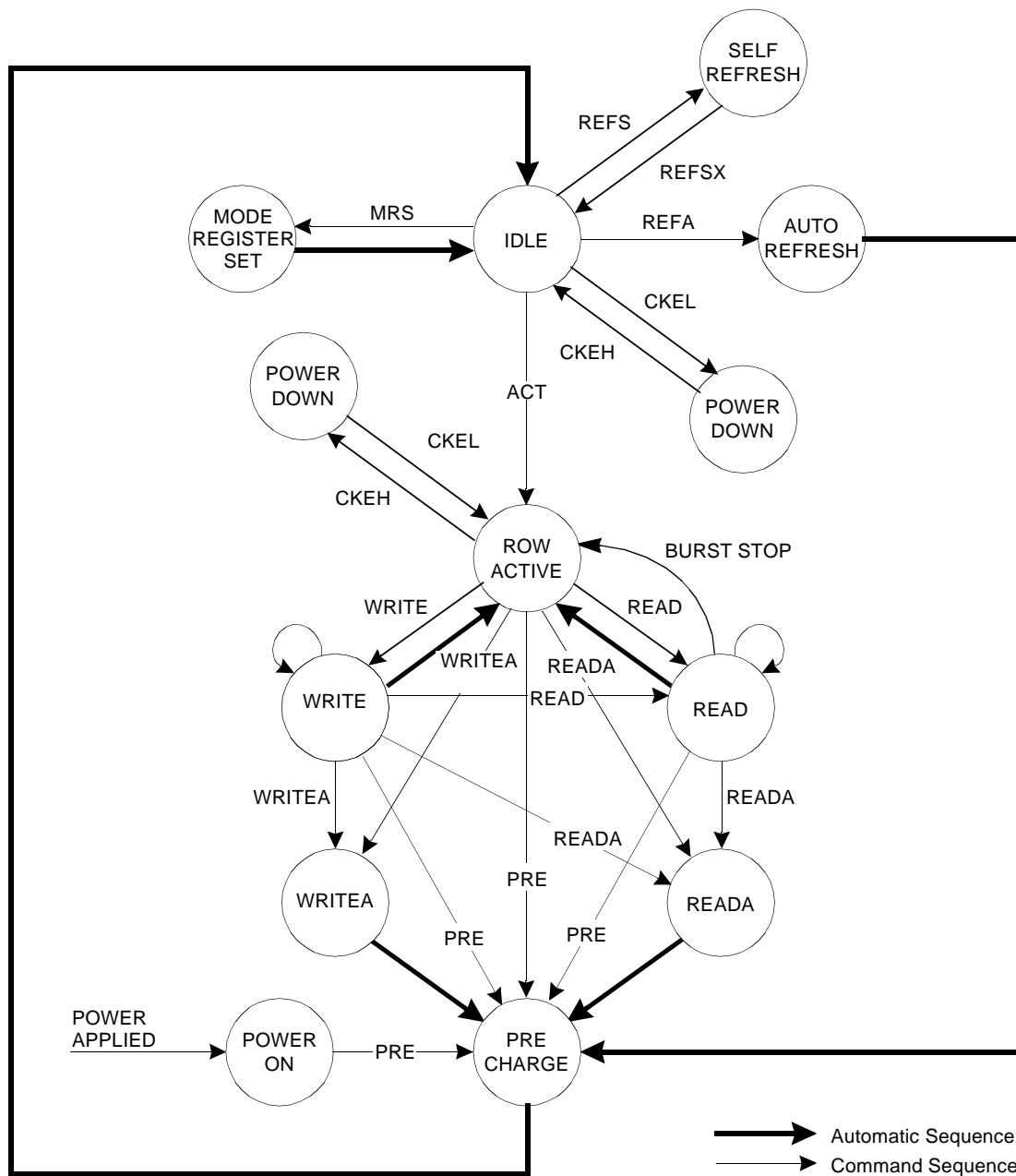
ABBREVIATIONS :

H=High Level, L=Low level, X=Don't Care

Note :

1. After CKE's low to high transition to exist self refresh mode. And a time of tRFC(min) has to be elapse after CKE's low to high transition to issue a new command.
2. CKE low to high transition is asynchronous as if restarts internal clock.
A minimum setup time "tSS + one clock" must be satisfied before any command other than exit.
3. Power-down and self refresh can be entered only from the all banks idle state.
4. Must be a legal command.

SIMPLIFIED STATE DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---------------------------------------|-----------|------------|------|
| Voltage on any pin relative to Vss | VIN, VOUT | -1.0 ~ 4.6 | V |
| Voltage on VDD supply relative to Vss | VDD, VDDQ | -1.0 ~ 4.6 | V |
| Storage temperature | TSTG | -55 ~ +150 | °C |
| Power dissipation | PD | 1.6 | W |
| Short circuit current | Ios | 50 | mA |

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to Vss=0V, TA=0 to 65°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------|--------|-----------|------|-----------|------|-------------|
| Device Supply voltage | VDD | 3.135 | 3.3 | 3.465 | V | 1 |
| Output Supply voltage | VDDQ | 2.375 | 2.50 | 2.625 | V | 1 |
| Reference voltage | VREF | 0.49*VDDQ | - | 0.51*VDDQ | V | 2 |
| Termination voltage | Vtt | VREF-0.04 | VREF | VREF+0.04 | V | 3 |
| Input logic high voltage | VIH | VREF+0.15 | - | VDDQ+0.30 | V | |
| Input logic low voltage | VIL | -0.30 | - | VREF-0.15 | V | 4 |
| Output logic high voltage | VOH | Vtt+0.76 | - | - | V | IOH=-15.2mA |
| Output logic low voltage | VOL | - | - | Vtt-0.76 | V | IOL=+15.2mA |
| Input leakage current | IIL | -5 | - | 5 | uA | 5 |
| Output leakage current | IOL | -5 | - | 5 | uA | 5 |

Note : 1. Under all conditions VDDQ must be less than or equal to VDD.
2. VREF is expected to equal 0.50*VDDQ of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the VREF may not exceed $\pm 2\%$ of the DC value. Thus, from 0.50*VDDQ, VREF is allowed $\pm 25\text{mV}$ for DC error and an additional $\pm 25\text{mV}$ for AC noise.
3. Vtt of the transmitting device must track VREF of the receiving device.
4. VIL(min.)= -1.5V AC(pulse width $\leq 5\text{ns}$).
5. For any pin under test input of $0\text{V} \leq \text{VIN} \leq \text{VDD}+0.3\text{V}$ is acceptable. For all other pins that are not under test VIN=0V.

AC INPUT OPERATING CONDITIONS

Recommended operating conditions(Voltage referenced to Vss=0V, VDD=3.3V $\pm 5\%$, VDDQ=2.5V $\pm 5\%$, TA=0 to 65°C)

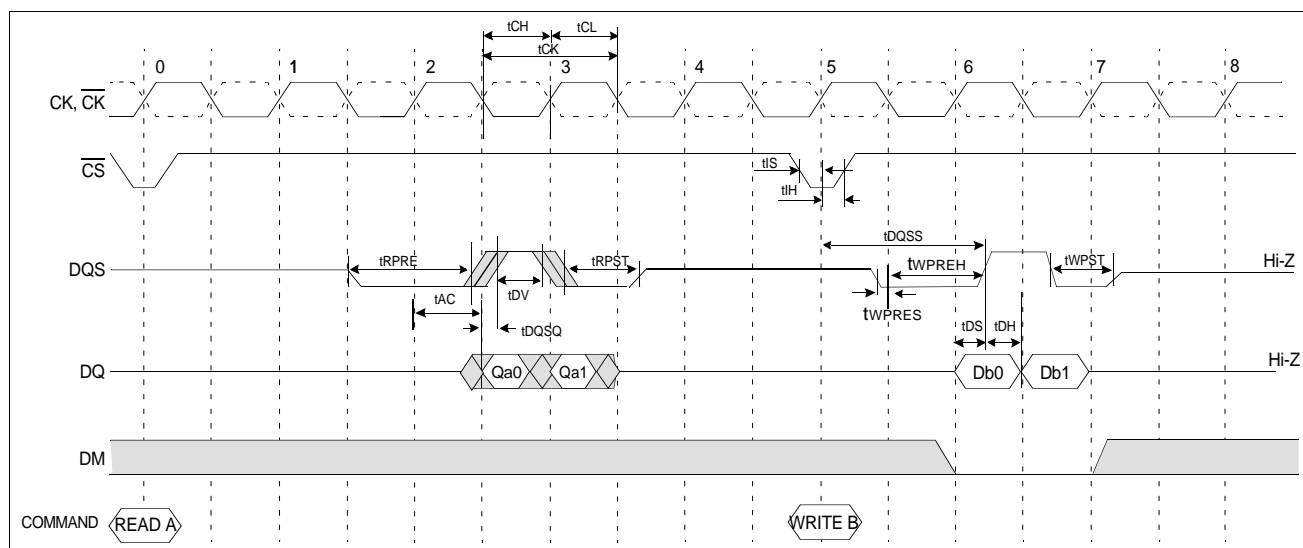
| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|--------|--------------|-----|--------------|------|------|
| Input High (Logic 1) Voltage; DQ | VIH | VREF+0.35 | - | - | V | |
| Input Low (Logic 0) Voltage; DQ | VIL | - | - | VREF-0.35 | V | |
| Clock Input Differential Voltage ; CK and $\overline{\text{CK}}$ | VID | 0.7 | - | VDDQ+0.6 | V | 1 |
| Clock Input Crossing Point Voltage ; CK and $\overline{\text{CK}}$ | VIX | 0.5*VDDQ-0.2 | - | 0.5*VDDQ+0.2 | V | 2 |

Note : 1. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same

AC CHARACTERISTICS

| Parameter | Symbol | -55 | | -60 | | -70 | | Unit | Note |
|--------------------------------------|--------------------|-----------------|------|------|------|------|------|-----------------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| CK cycle time | CL=3 | t _{CK} | 5.5 | 1000 | 6 | 1000 | 7 | 1000 | ns |
| CK high level width | t _{CH} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t _{CK} | |
| CK low level width | t _{CL} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t _{CK} | |
| DQS out access time from CK | t _{ACS} | 2.5 | 5.5 | 2.5 | 5.5 | 2.5 | 6.0 | ns | |
| Output access time from CK | t _{AC} | 2.5 | 5.5 | 2.5 | 5.5 | 2.5 | 6.0 | ns | |
| Data strobe edge to output data edge | t _{DQSQ} | -0.5 | +0.5 | -0.5 | +0.5 | -0.5 | +0.5 | ns | |
| Read preamble | t _{RPRE} | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | t _{CK} | |
| Read postamble | t _{RPST} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} | |
| CK to valid DQS-in | t _{DQSS} | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | t _{CK} | |
| DQS-In setup time | t _{WPRES} | 0 | | 0 | | 0 | | t _{CK} | |
| DQS-in hold time | t _{WPREH} | 0.25 | | 0.25 | | 0.25 | | t _{CK} | |
| DQS-In high level width | t _{DQSH} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} | |
| DQS-In low level width | t _{DQSL} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} | |
| Address and Control input setup time | t _{IS} | 1.2 | | 1.2 | | 1.2 | | ns | |
| Address and Control input hold time | t _{IH} | 0.9 | | 0.9 | | 0.9 | | ns | |
| DQ and DM setup time to DQS | t _{DS} | 0.5 | | 0.5 | | 0.5 | | ns | |
| DQ and DM hold time to DQS | t _{DH} | 0.5 | | 0.5 | | 0.5 | | ns | |
| Output DQS valid window | t _{DV} | 0.35 | | 0.35 | | 0.35 | | t _{CK} | |
| DQS write postamble | t _{WPST} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} | |

Simplified Timing(1) @ BL=2, CL=3

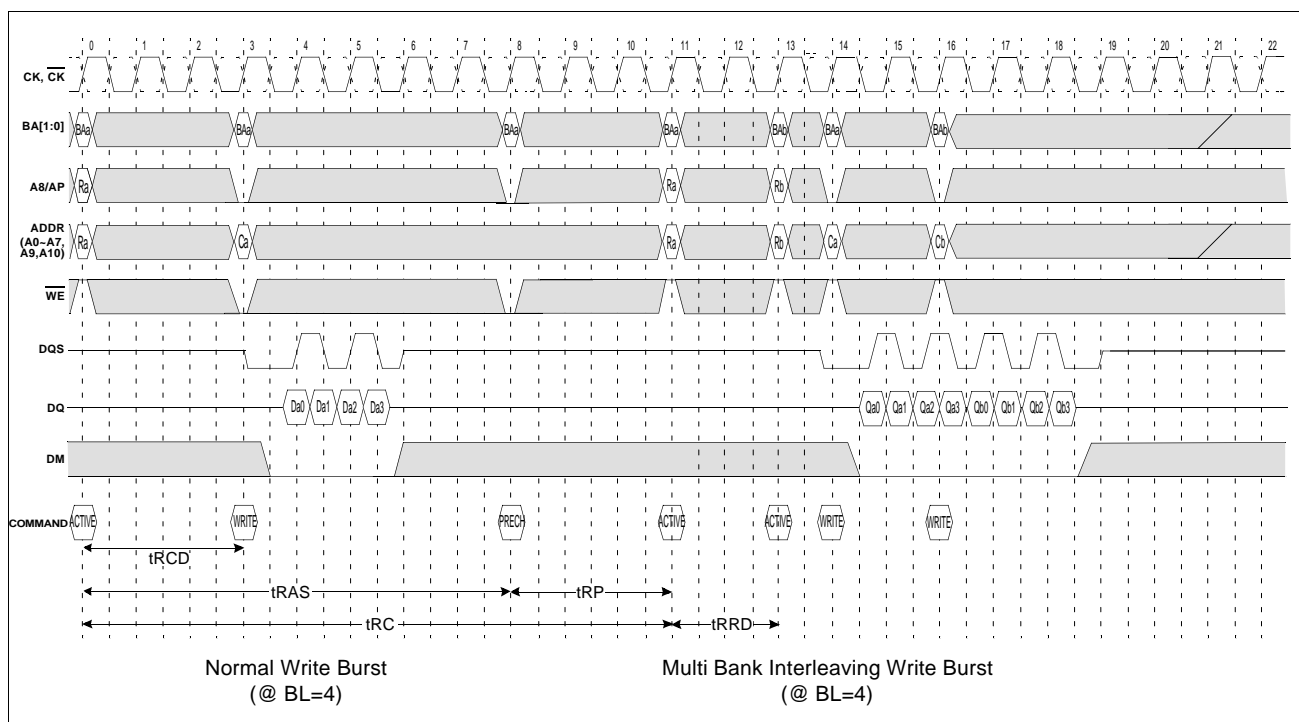


AC CHARACTERISTICS

| Parameter | Symbol | -55 | | -60 | | -70 | | Unit | Note |
|---|-------------------|----------|------|----------|------|----------|------|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| Row cycle time | t _{RC} | 60.5 | | 60 | | 70 | | ns | |
| Refresh row cycle time | t _{RFC} | 71.5 | | 72 | | 84 | | ns | |
| Row active time | t _{RAS} | 44 | 100K | 42 | 100K | 49 | 100K | ns | |
| RAS to CAS delay | t _{RCD} | 22 | | 18 | | 21 | | ns | |
| Row precharge time | t _{RP} | 16.5 | | 18 | | 21 | | ns | |
| Row active to Row active delay | t _{RRD} | 11 | | 12 | | 14 | | ns | |
| Last data in to Row precharge | t _{WR} | 2 | | 2 | | 2 | | tCK | 1 |
| Last data in to Read command delay | t _{CDLR} | 2 | | 2 | | 2 | | tCK | 1 |
| Col. address to Col. address delay | t _{CCD} | 1 | | 1 | | 1 | | tCK | |
| Mode register set cycle time | t _{MRD} | 2 | | 2 | | 2 | | tCK | |
| Power down exit time | t _{PEDX} | 1tCK+tIS | | 1tCK+tIS | | 1tCK+tIS | | ns | |
| Auto precharge write recovery + Precharge | t _{DAL} | 5 | | 5 | | 5 | | tCK | |
| Refresh interval time | t _{REF} | 7.8 | | 7.8 | | 7.8 | | us | |

1. Note : For normal write operation, even numbers of Din are to be written inside DRAM

Simplified Timing(2) @ BL=4, CL=3



DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, TA=0 to 65°C)

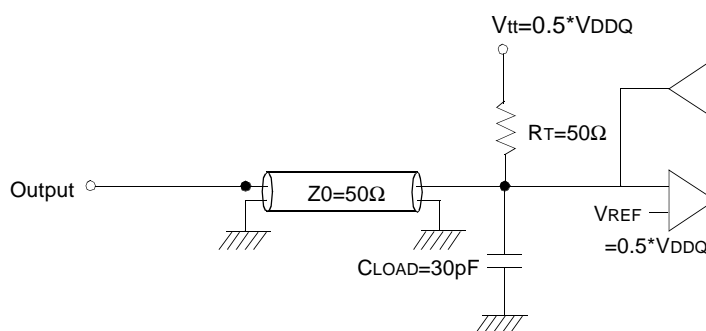
| Parameter | Symbol | Test Condition | Version | | | Unit | Note |
|---|-------------------|--|---------|-----|-----|------|------|
| | | | -55 | -60 | -70 | | |
| Operating Current (One Bank Active) | I _{CC1} | Burst Lenth=2 t _{RC} ≥ t _{RC} (min) I _{OL} =0mA, t _{CC} = t _{CC} (min) | 280 | 280 | 260 | mA | 1 |
| Precharge Standby Current in Power-down mode | I _{CC2P} | CKE ≤ V _{IL} (max), t _{CC} = t _{CC} (min) | 3 | | | mA | |
| Precharge Standby Current in Non Power-down mode | I _{CC2N} | CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(\min)$, t _{CC} = t _{CC} (min) | 125 | 105 | 100 | mA | |
| Active Standby Current power-down mode | I _{CC3P} | CKE ≤ V _{IL} (max), t _{CC} = t _{CC} (min) | 6 | | | mA | |
| Active Standby Current in in Non Power-down mode | I _{CC3N} | CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(\min)$, t _{CC} =t _{CC} (min) | 130 | 120 | 105 | mA | |
| Operating Current (Burst Mode) | I _{CC4} | I _{OL} =0mA ,t _{CC} = t _{CC} (min), Page Burst, All Banks activated | 420 | 400 | 370 | mA | 1 |
| Refresh Current | I _{CC5} | t _{RC} ≥ t _{RFC} (min) | 350 | 340 | 300 | mA | 2 |
| Self Refresh Current | I _{CC6} | CKE ≤ 0.2V | 4 | | | mA | |

Note : 1. Measured with outputs open.

2. Refresh period is 16ms.

AC OPERATING TEST CONDITIONS ($V_{DD}=3.3V\pm0.15V$, $T_A=0$ to 65°C)

| Parameter | Value | Unit | Note |
|--|-----------------------------|------|------|
| Input reference voltage for CK(for single ended) | $0.50 \cdot V_{DDQ}$ | V | |
| CK signal maximum peak swing | 1.5 | V | |
| CK signal minimum slew rate | 1.0 | V/ns | |
| Input Levels(V_{IH}/V_{IL}) | $V_{REF}+0.35/V_{REF}-0.35$ | V | |
| Input timing measurement reference level | V_{REF} | V | |
| Output timing measurement reference level | V_{tt} | V | |
| Output load condition | See Fig.1 | | |



(Fig. 1) Output Load Circuit

CAPACITANCE ($V_{DD}=3.3V$, $T_A=25^\circ\text{C}$, $f=1\text{MHz}$)

| Parameter | Symbol | Min | Max | Unit |
|---|-----------|-----|-----|------|
| Input capacitance($A_0 \sim A_{10}$, $BA_0 \sim BA_1$) | C_{IN1} | 2.5 | 4.5 | pF |
| Input capacitance ($\overline{CK}, \overline{CK}, \overline{CKE}, \overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}$) | C_{IN2} | 2.5 | 5.0 | pF |
| Input/output capacitance($DQ_0 \sim DQ_{31}$ & DQS) | C_{OUT} | 2.5 | 5.5 | pF |
| Input capacitance($DM_0 \sim DM_3$) | C_{IN3} | 2.5 | 5.5 | pF |

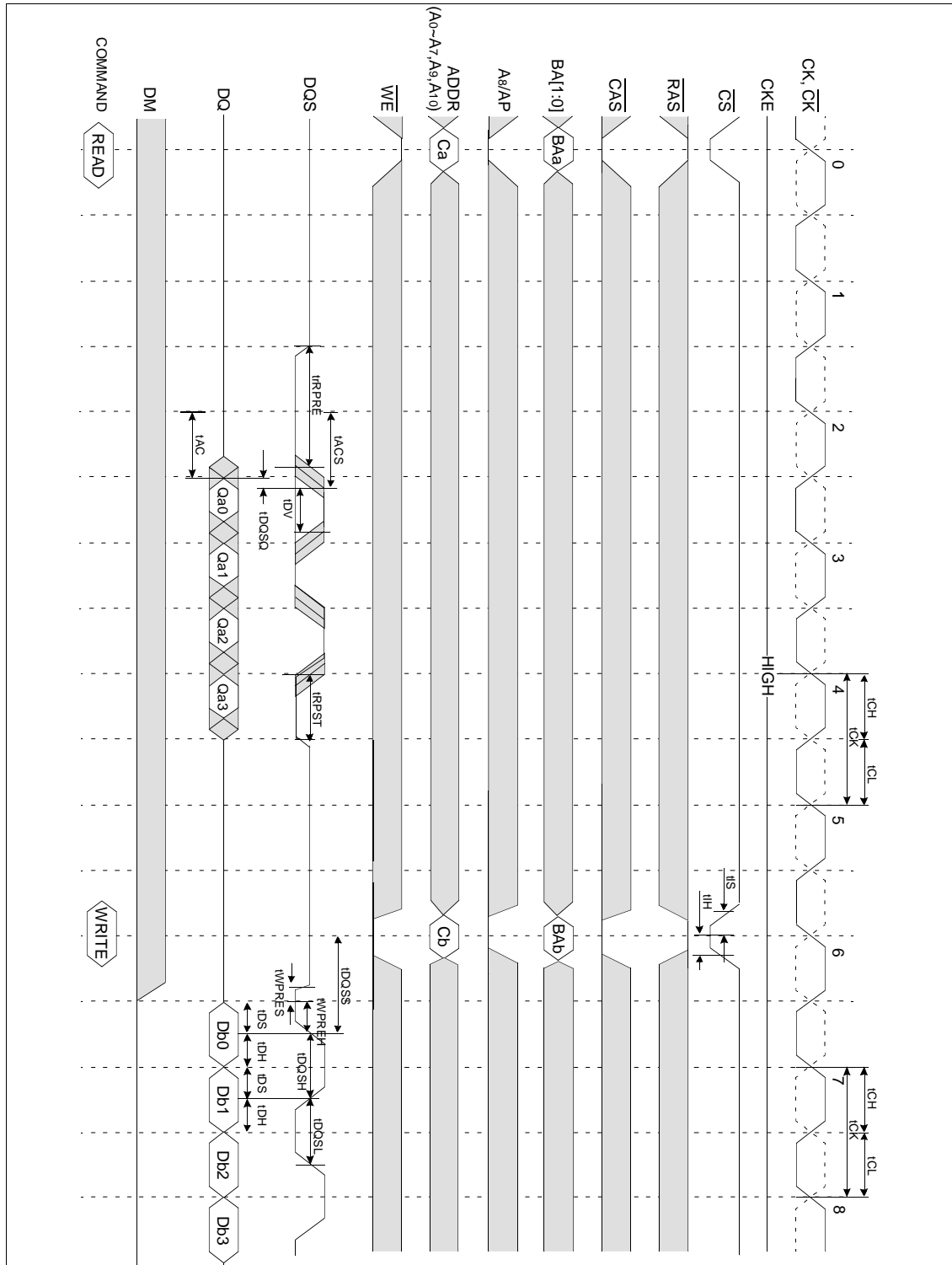
DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

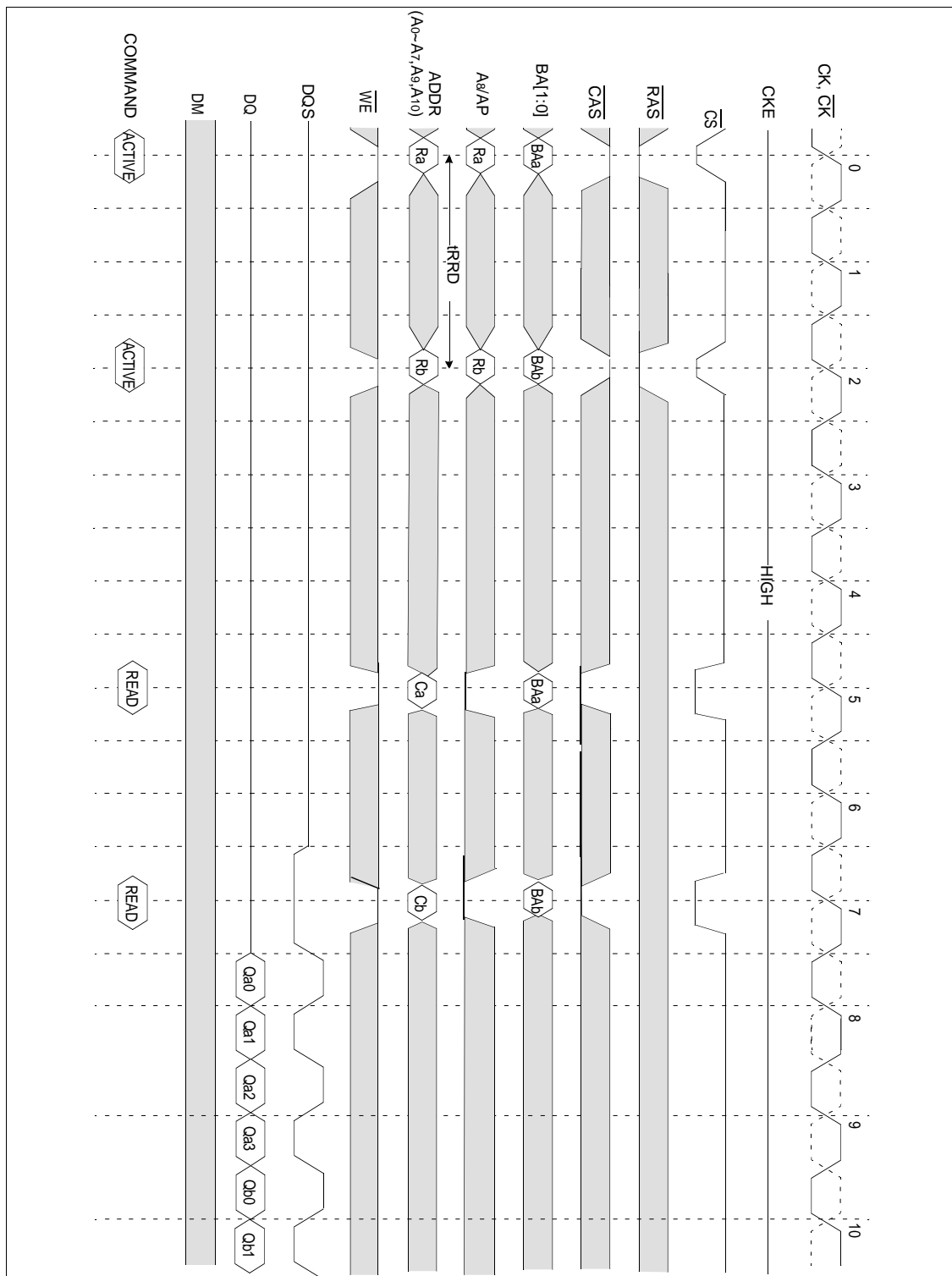
| Parameter | Symbol | Value | Unit |
|--|-----------|--------------|---------------|
| Decoupling Capacitance between V_{DD} and V_{SS} | C_{DC1} | $0.1 + 0.01$ | μF |
| Decoupling Capacitance between V_{DDQ} and V_{SSQ} | C_{DC2} | $0.1 + 0.01$ | μF |

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
 All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
 2. V_{SS} and V_{SSQ} pins are separated each other
 All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

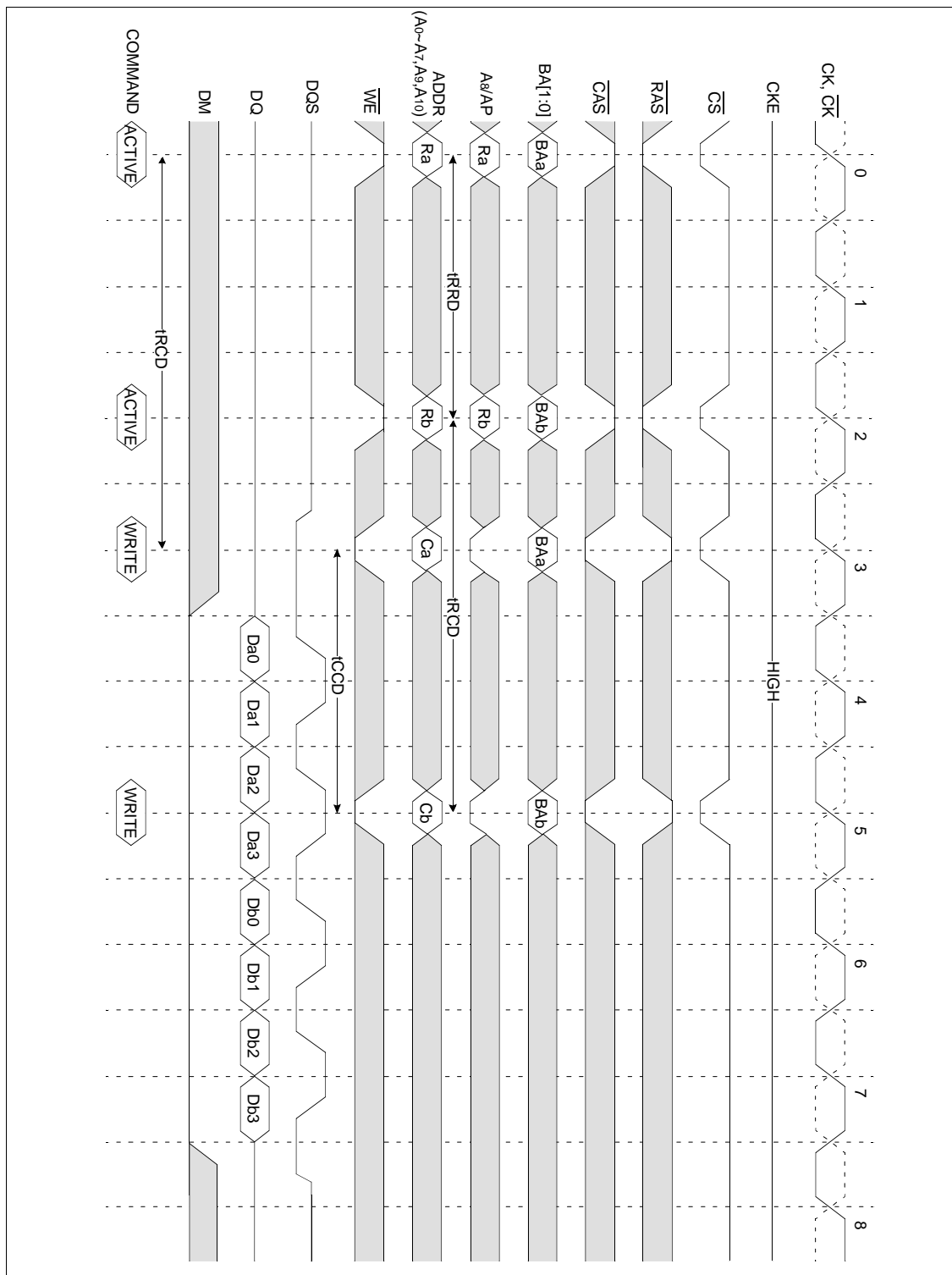
Basic Timing (Setup, Hold and Access Time @BL=4, CL=3)



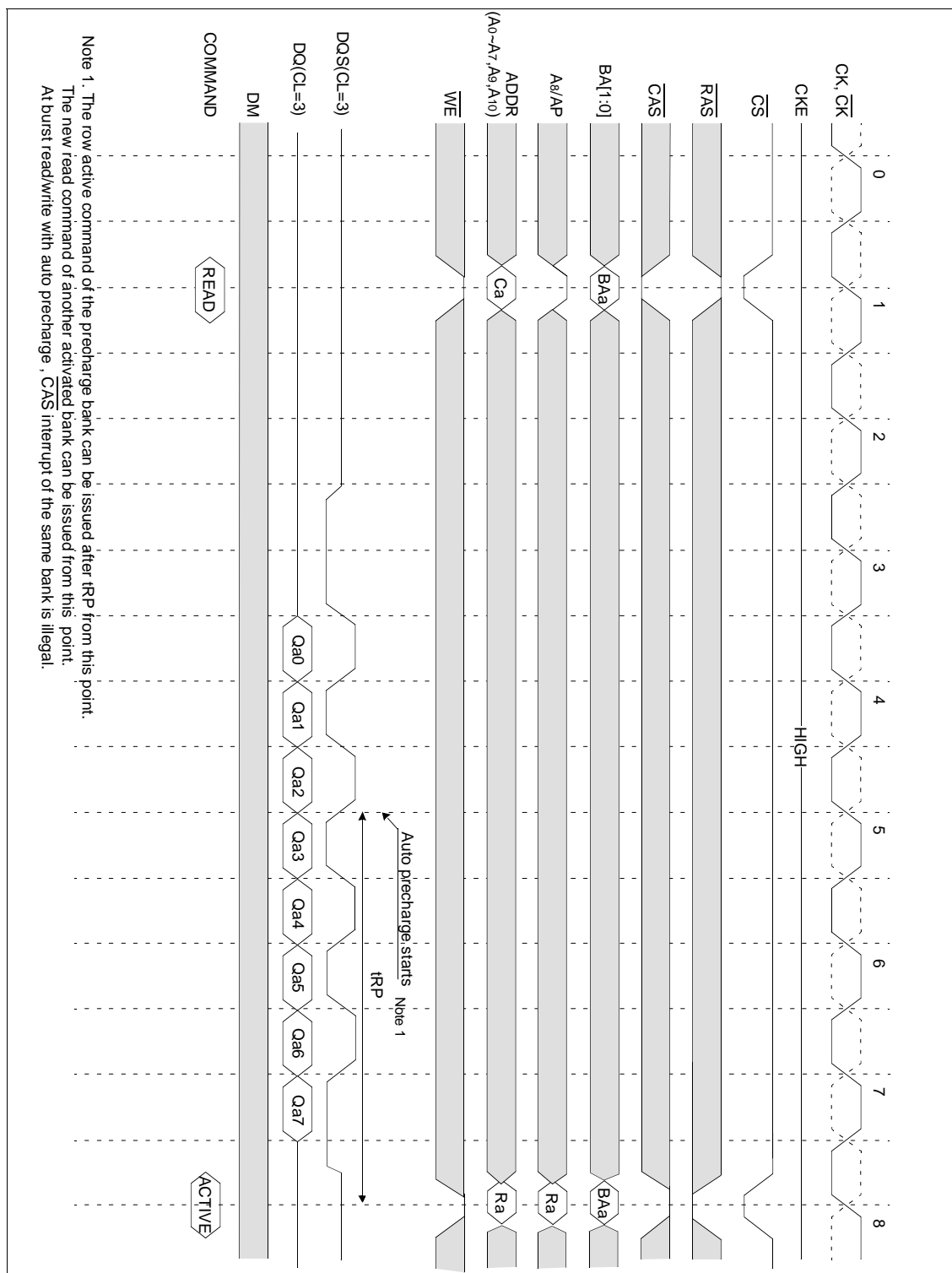
Multi Bank Interleaving READ (@BL=4, CL=3)



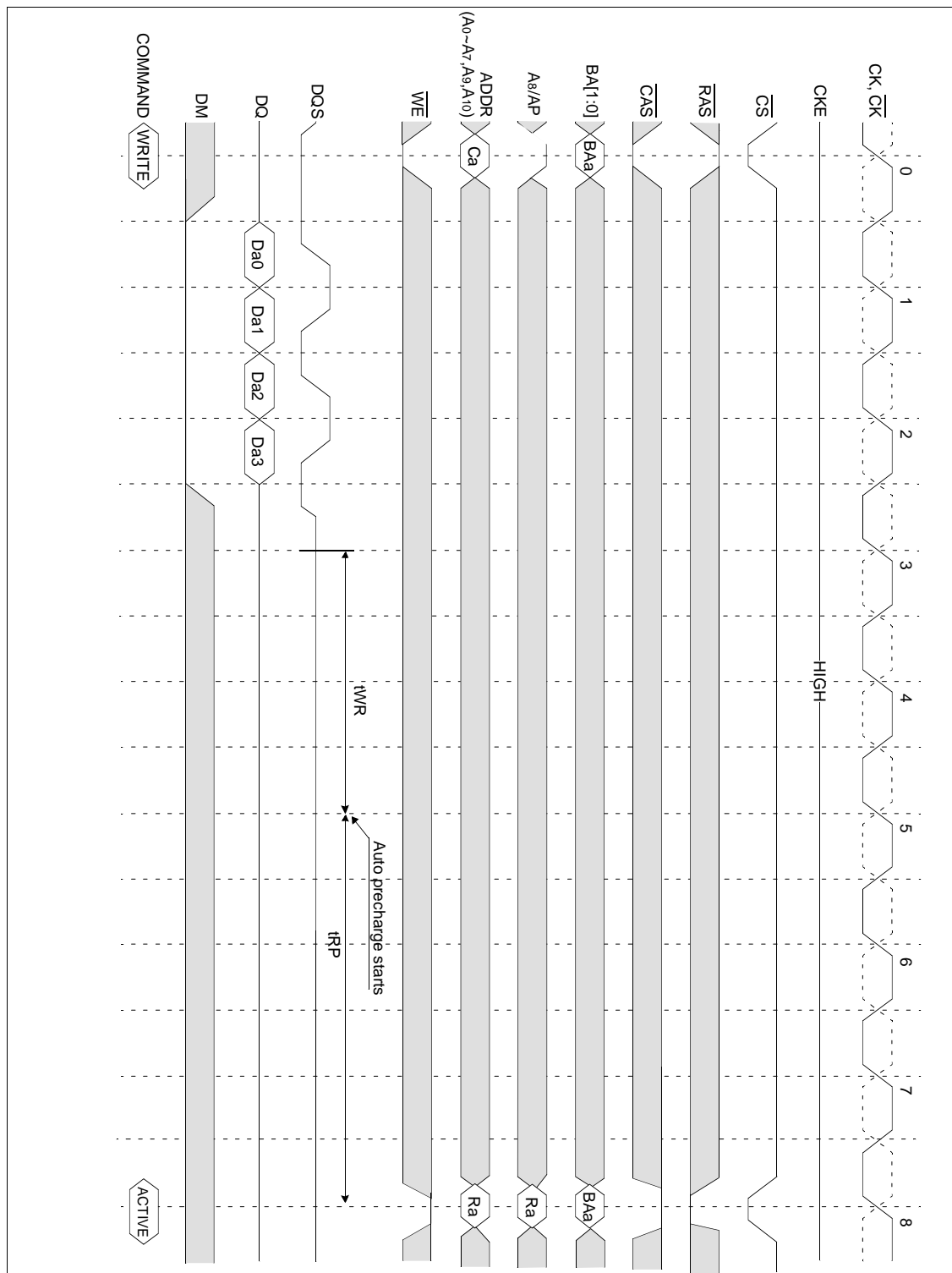
Multi Bank Interleaving WRITE (@BL=4)



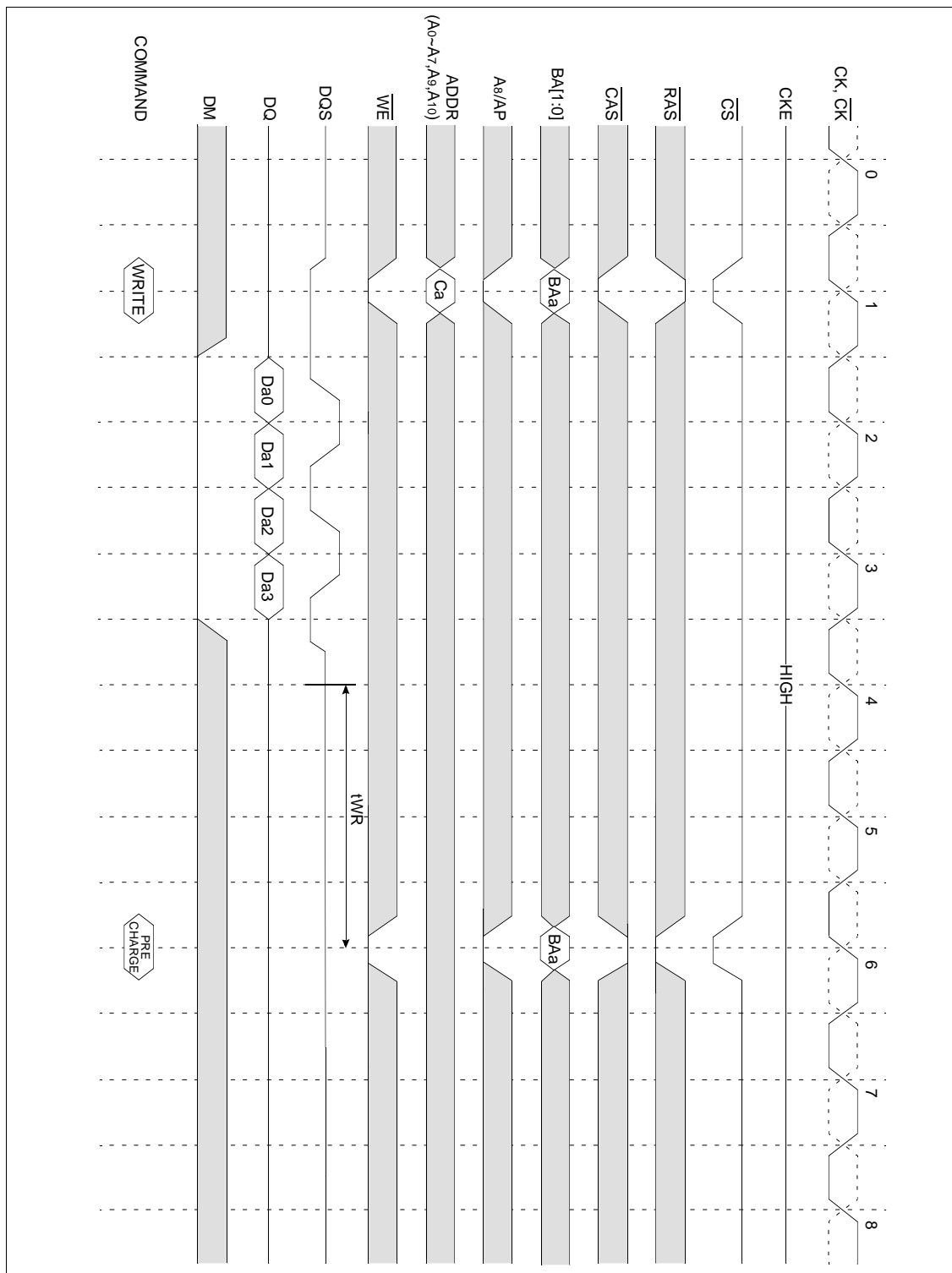
Auto Precharge after READ Burst (@BL=8, CL=3)



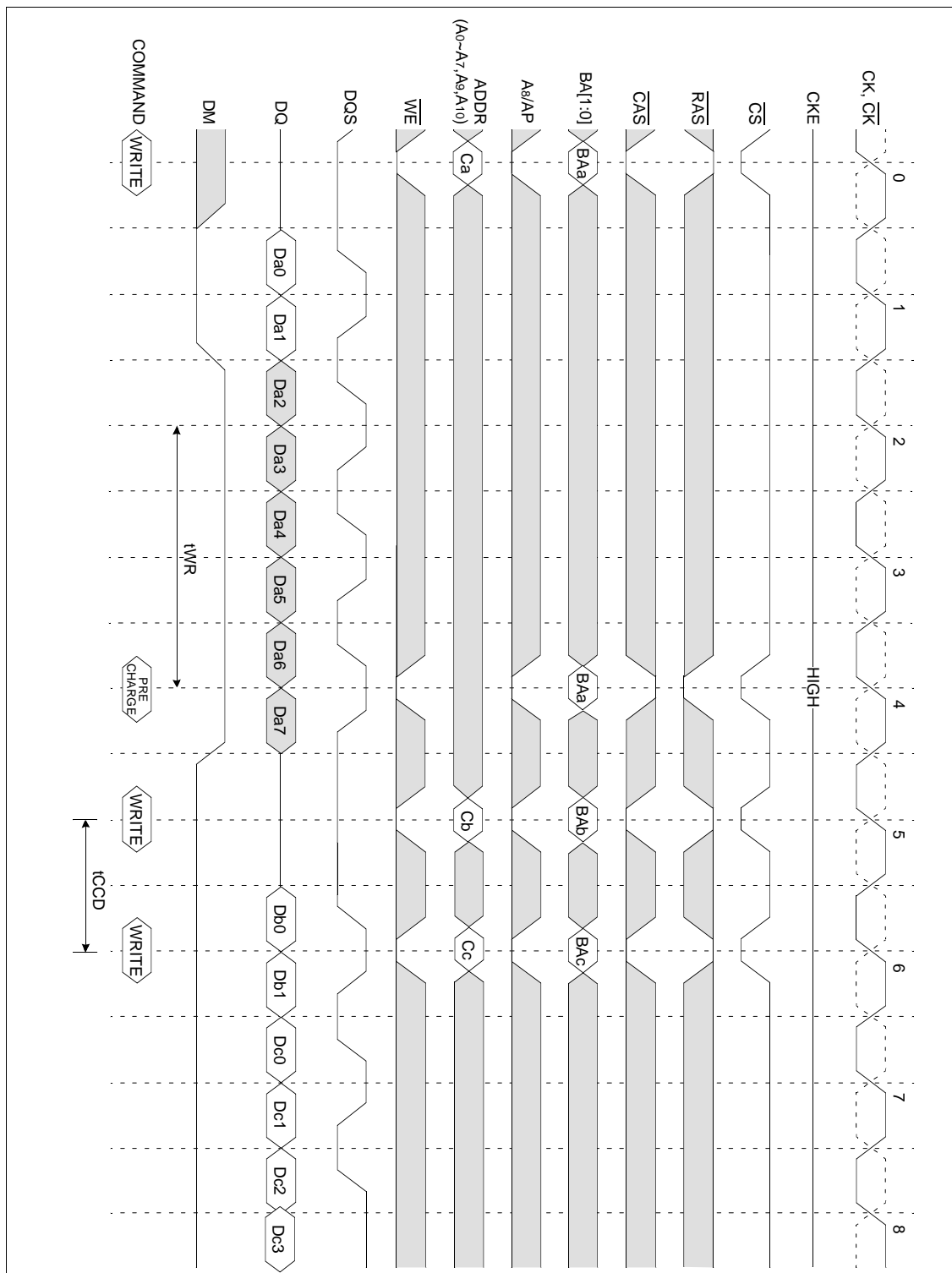
Auto Precharge after WRITE Burst (@BL=4)



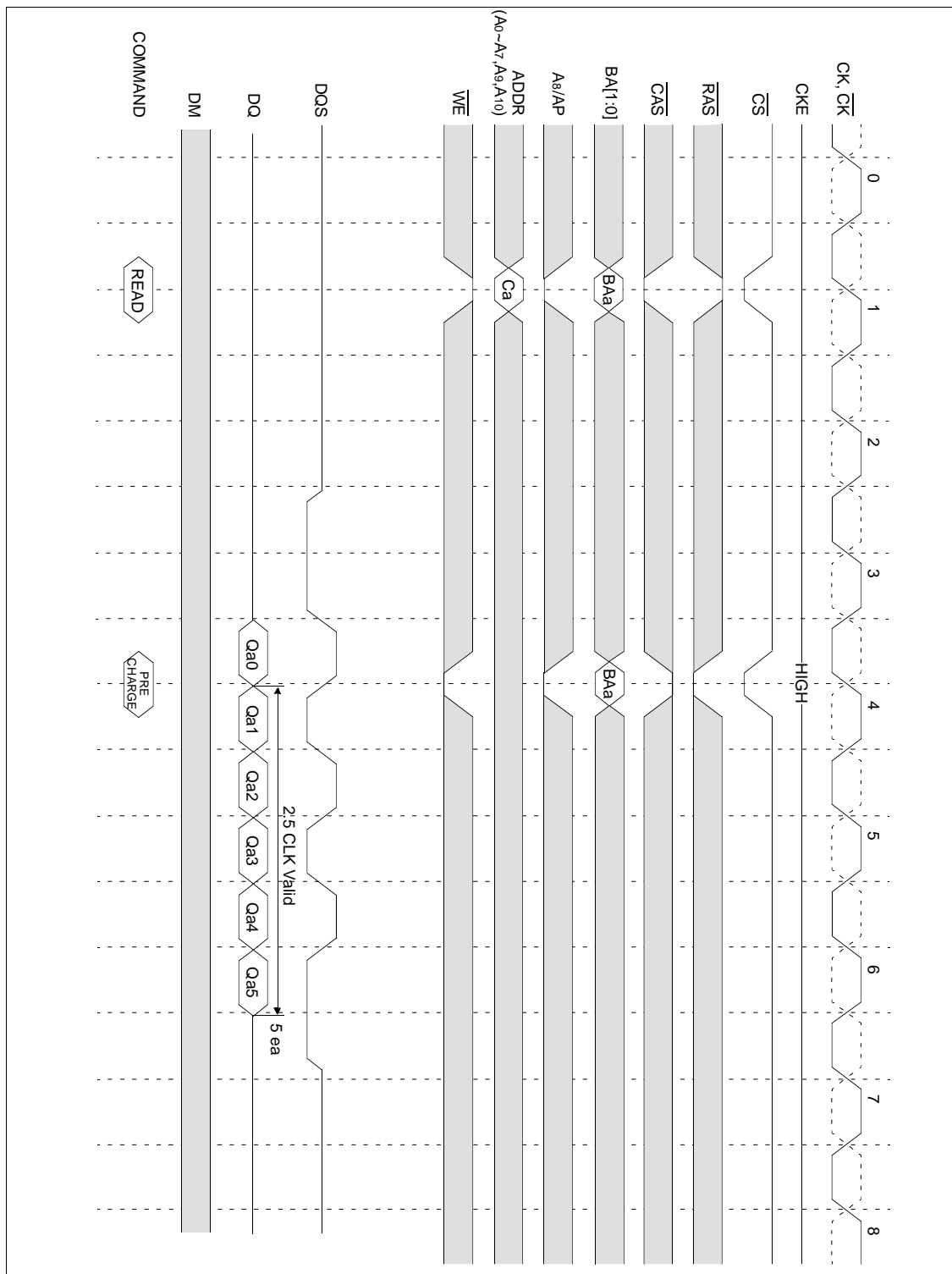
Normal WRITE Burst (@BL=4)



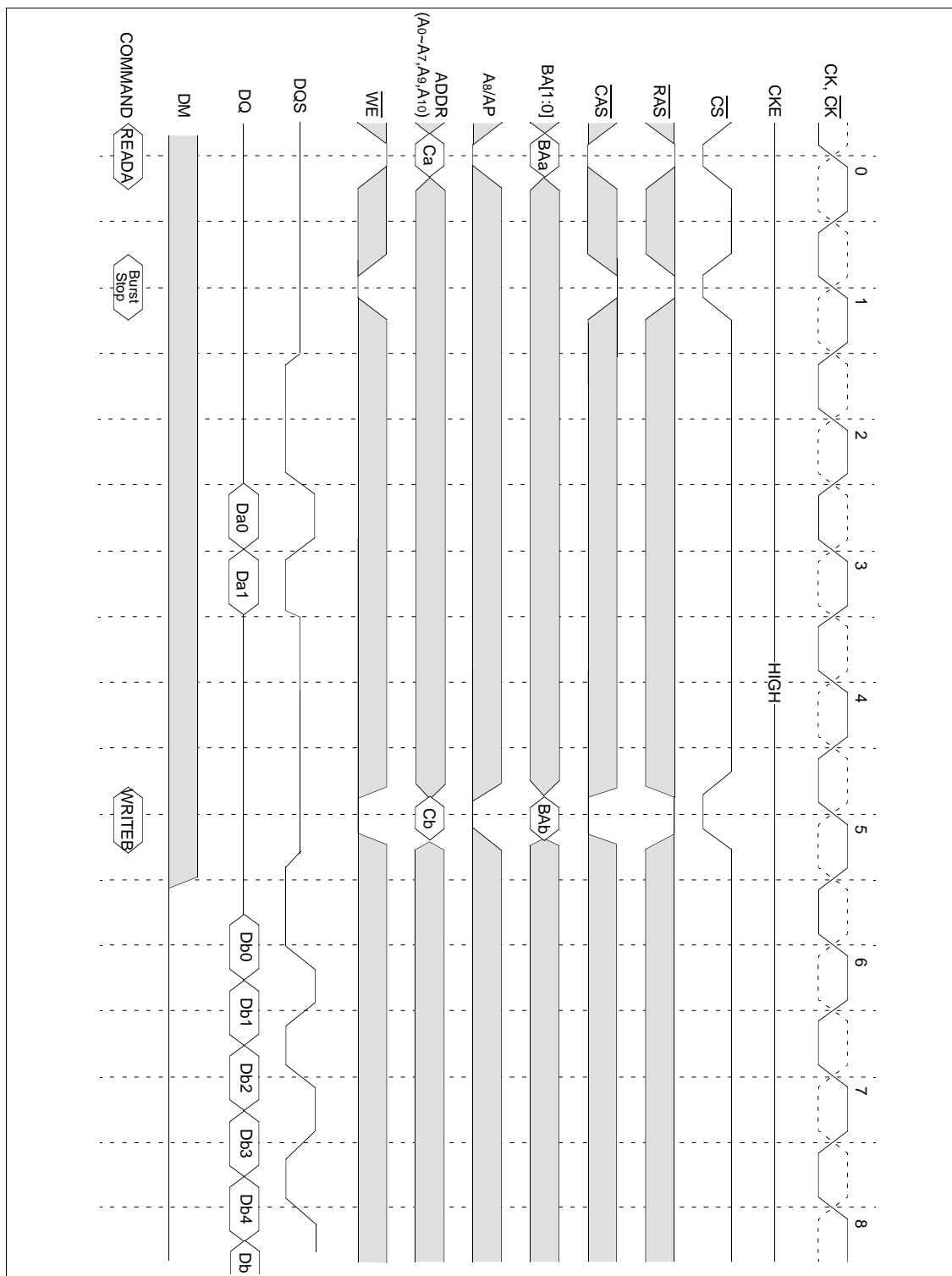
Write Interrupted by Precharge & DM (@BL=8)



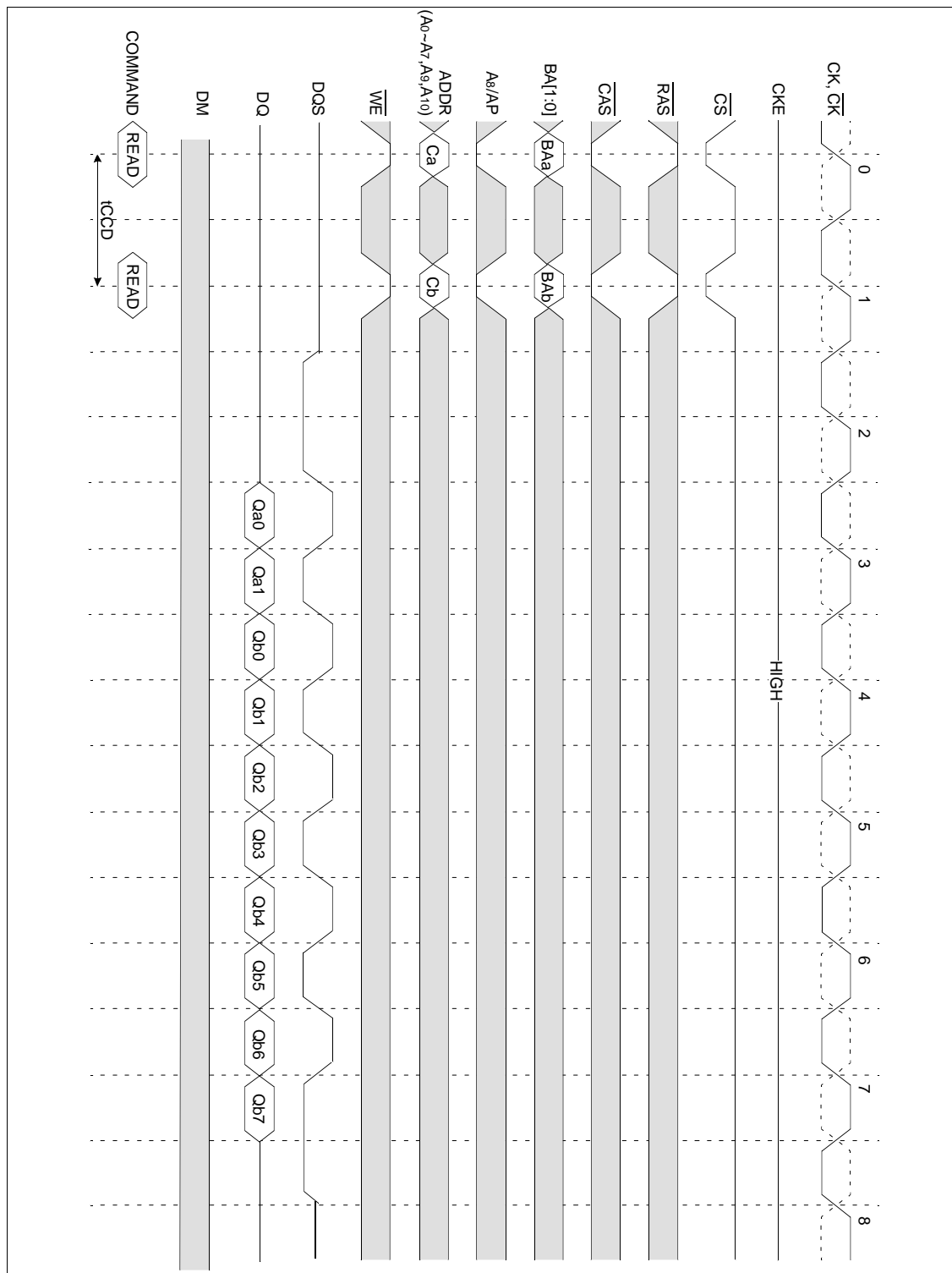
Read Interrupted by Precharge (@BL=8, CL=3)



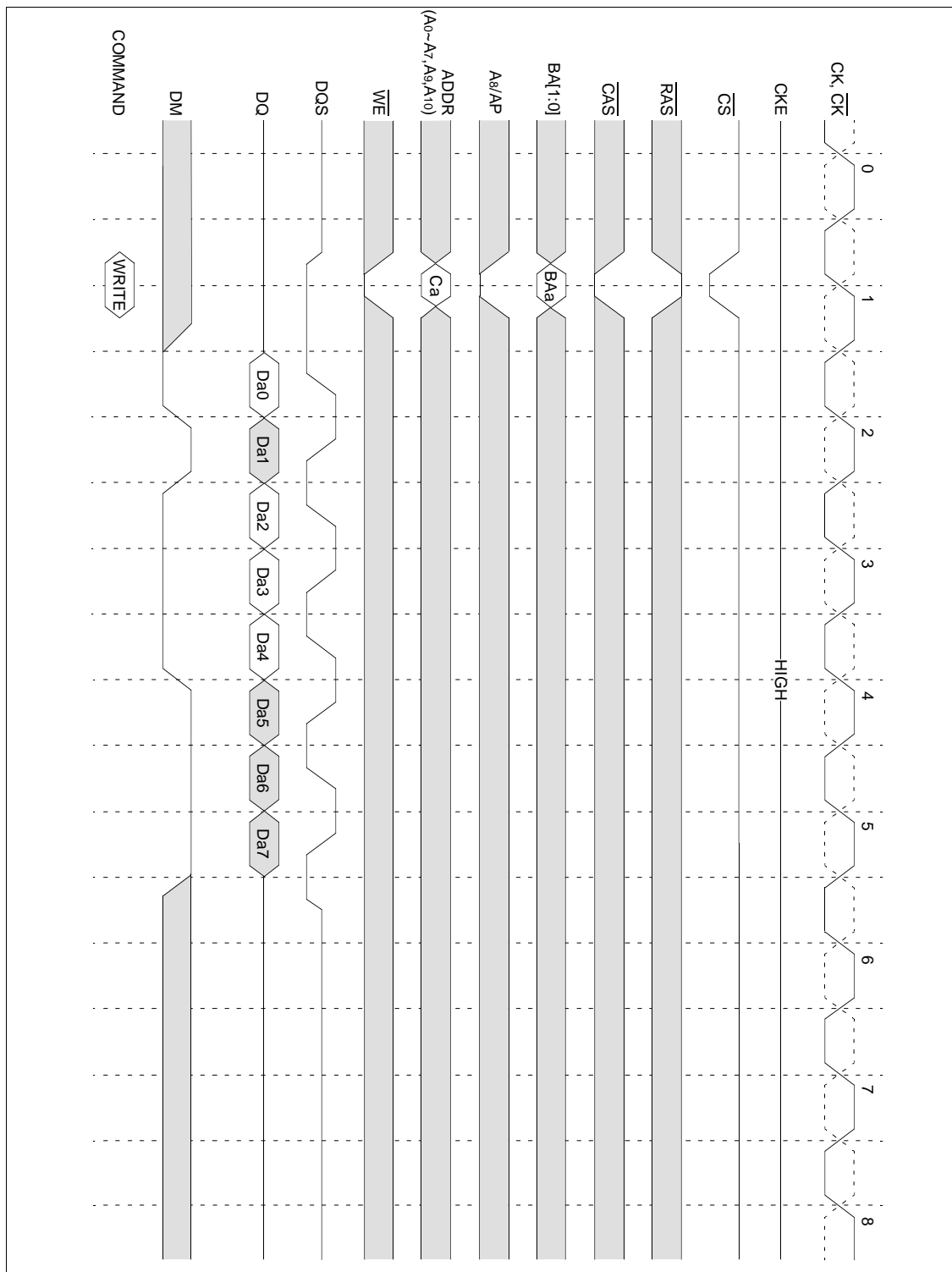
Read Interrupted by Burst stop & Write (@BL=8, CL=3)



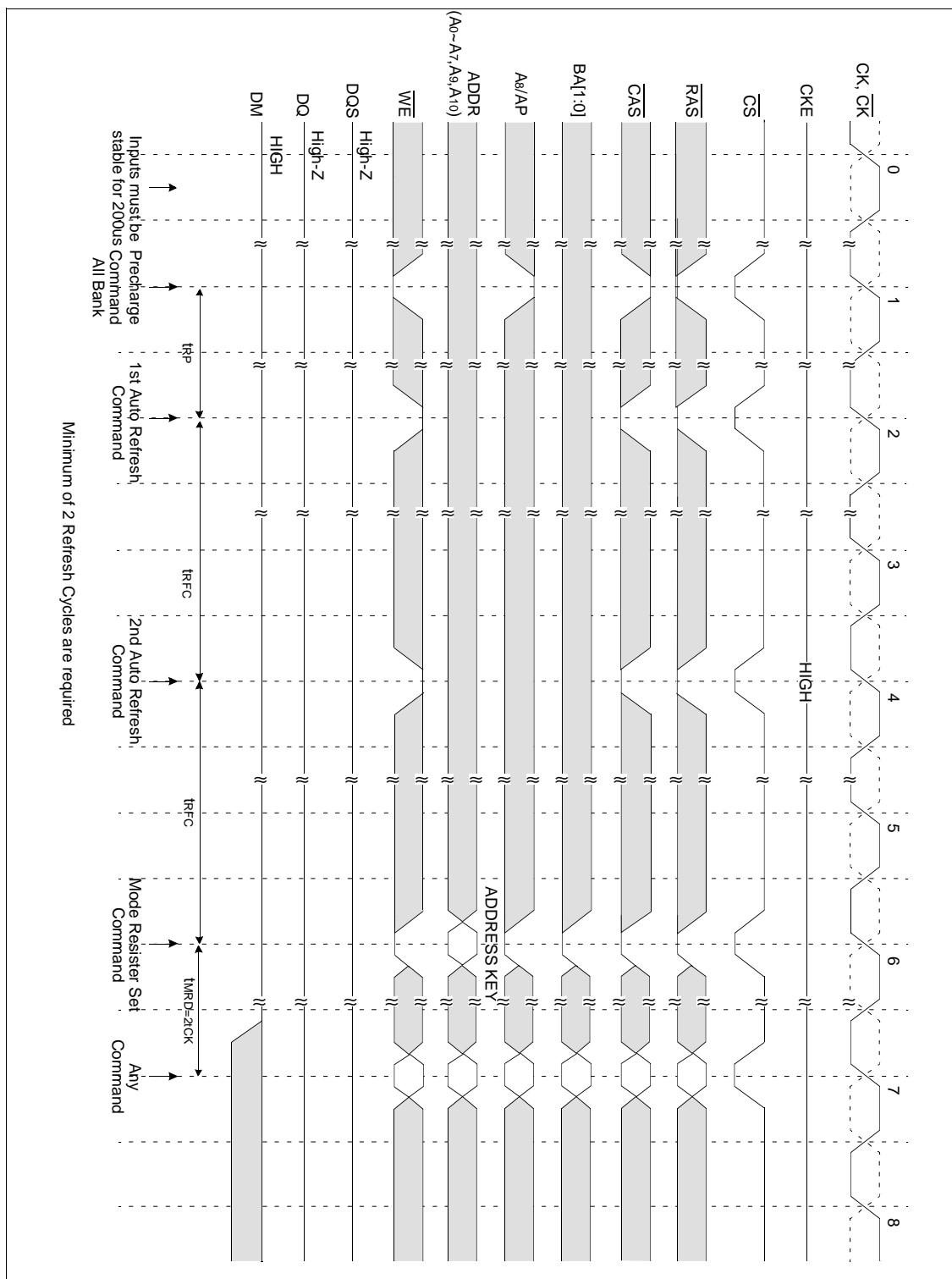
Read Interrupted by a Read (@BL=8, CL=3)



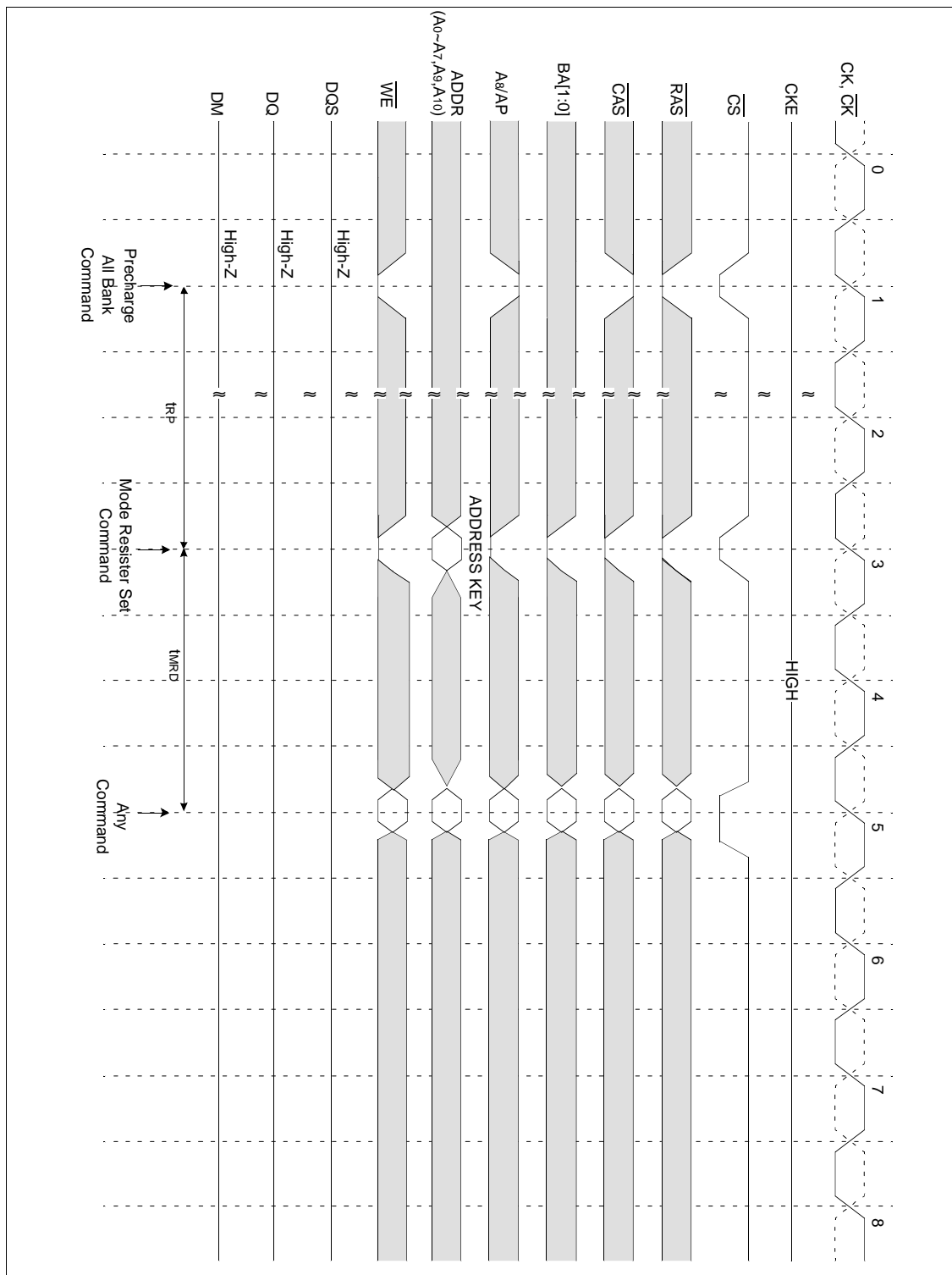
DM Function (@BL=8) only for write



Power up Sequence & Auto Refresh(CBR)



Mode Register Set



PACKAGE DIMENSIONS (TQFP)

Dimensions in Millimeters

