

**Document Title****256Kx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
0.0	Design target	January 30, 1997	Advance
0.1	Initial draft	April 7, 1997	Preliminary
1.0	Finalize - Improved $V_{IL}(\text{Min.})$ : 0.4V $\rightarrow$ 0.6V - Erase reverse type package - Change speed bin KM68V2000: 70/85ns KM68V2000I, KM68U2000, KM68U2000I : 85/100ns - Improved standby current Commercial product: 15 $\mu$ A $\rightarrow$ 10 $\mu$ A Industrial product: 30 $\mu$ A $\rightarrow$ 15 $\mu$ A - Increased Power dissipation: 0.7W $\rightarrow$ 1.0W	November 27, 1997	Final

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## 256Kx8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: TFT
- Organization: 256Kx8
- Power Supply Voltage  
K6T2008V2M Family: 3.0V ~ 3.6V  
K6T2008U2M Family: 2.7V ~ 3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-TSOP1-0820F, 32-TSOP1-0813.4F

### GENERAL DESCRIPTION

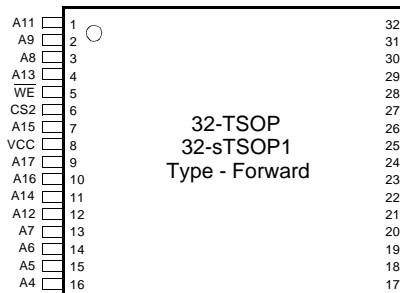
The K6T2008V2M and K6T2008U2M families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2,Max)	
K6T2008V2M-B K6T2008U2M-B	Commercial (0~70°C)	3.0~3.6V 2.7~3.3V	70/85ns 85/100ns	10µA	40mA <sup>1)</sup>	32-TSOP1-0820F 32-TSOP1-0813.4F
K6T2008V2M-F K6T2008U2M-F	Industrial (-40~85°C)	3.0~3.6V 2.7~3.3V	85/100ns 85/100ns	15µA		

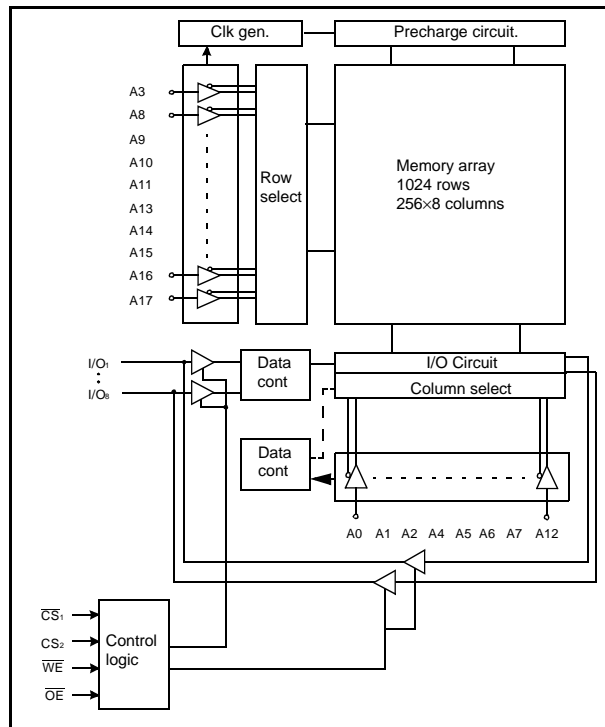
1. K6T2008V2M family = 50mA

### PIN DESCRIPTION



Name	Function
$\overline{CS}_1, \overline{CS}_2$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
A0~A17	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
NC	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T2008V2M-TB70 K6T2008V2M-TB85	32-TSOP1-F, 70ns, 3.3V, LL 32-TSOP1-F, 85ns, 3.3V, LL	K6T2008V2M-TF85 K6T2008V2M-TF10	32-TSOP1-F, 85ns, 3.3V, LL 32-TSOP1-F, 100ns, 3.3V, LL
K6T2008U2M-TB85 K6T2008U2M-TB10	32-TSOP1-F, 85ns, 3.0V, LL 32-TSOP1-F, 100ns, 3.0V, LL	K6T2008U2M-TF85 K6T2008U2M-TF10	32-TSOP1-F, 85ns, 3.0V, LL 32-TSOP1-F, 100ns, 3.0V, LL
K6T2008V2M-YB70 K6T2008V2M-YB85	32-sTSOP1-F, 70ns, 3.3V,LL 32-sTSOP1-F, 85ns, 3.3V,LL	K6T2008V2M-YF85 K6T2008V2M-YF10	32-sTSOP1-F, 85ns, 3.3V,LL 32-sTSOP1-F, 100ns, 3.3V,LL
K6T2008U2M-YB85 K6T2008U2M-YB10	32-sTSOP1-F, 85ns, 3.0V, LL 32-sTSOP1-F, 100ns, 3.0V, LL	K6T2008U2M-YF85 K6T2008U2M-YF10	32-sTSOP1-F, 85ns, 3.0V, LL 32-sTSOP1-F, 100ns, 3.0V, LL

## FUNCTIONAL DESCRIPTION

CS <sub>1</sub>	CS <sub>2</sub>	OE	WE	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	K6T2008V2M-B, K6T2008U2M-B
		-40 to 85	°C	K6T2008V2M-F, K6T2008U2M-F
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec(Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	K6T2008V2M Family K6T2008U2M Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V <sub>SS</sub>	All Family	0	0	0	V
Input high voltage	V <sub>IH</sub>	K6T2008V2M, K6T2008U2M Family	2.2	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	K6T2008V2M, K6T2008U2M Family	-0.3 <sup>3)</sup>	-	0.6	V

Note:

1. Commercial Product: T<sub>A</sub>=0 to 70°C, otherwise specified  
Industrial Product: T<sub>A</sub>=-40 to 85°C, otherwise specified
2. Overshoot: V<sub>CC</sub>+3.0V in case of pulse width≤30ns
3. Undershoot: -3.0V in case of pulse width≤30ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or CS <sub>2</sub> =V <sub>IL</sub> or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Operating power supply	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , Read	-	2	5	mA
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100%duty, I <sub>IO</sub> =0mA, $\overline{CS}_1 \leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	Read	-	2	5
			Write	-	10	15
Average operating current	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	30	40 <sup>1)</sup>	mA
			-	-	-	-
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.2	-	-	V
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.3	mA
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS}_1 \geq V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V or CS <sub>2</sub> ≤0.2V, Other inputs=0~V <sub>CC</sub>	-	0.2	10 <sup>2)</sup>	μA

1. K6T2008V2M Family = 50mA

2. Industrial product = 15μA

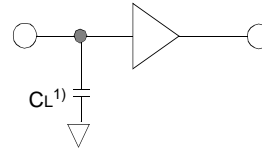
## AC OPERATING CONDITIONS

## TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (see right):  $C_L = 100\text{pF} + 1\text{TTL}$ 

1. Including scope and jig capacitance

**AC CHARACTERISTICS** (K6T2008V2M Family:  $V_{CC} = 3.0 \sim 3.6\text{V}$ , K6T2008U2M Family:  $V_{CC} = 2.7 \sim 3.3\text{V}$   
 Commercial Product:  $T_A = 0$  to  $70^\circ\text{C}$ , Industrial Product:  $T_A = -40$  to  $85^\circ\text{C}$ )

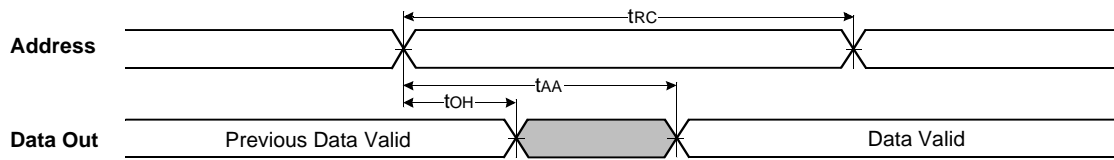
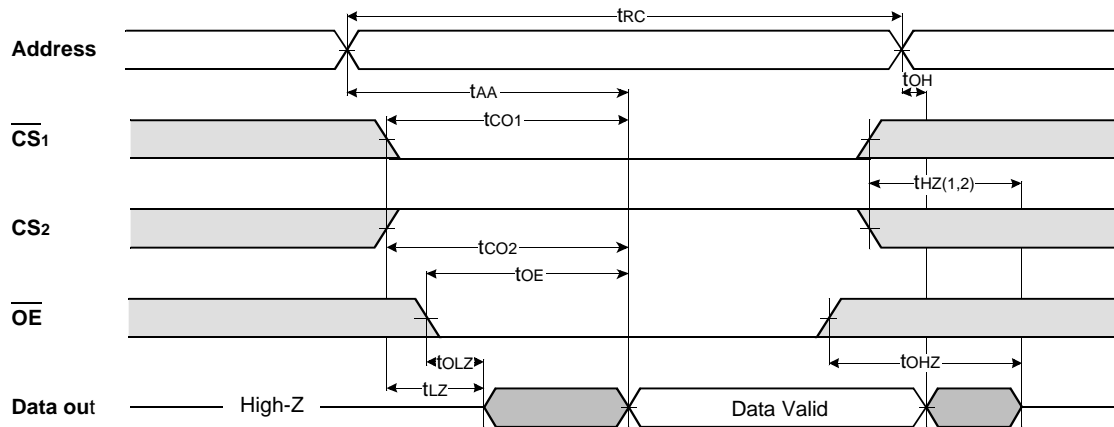
Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO1, tCO2	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

## DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR		$\overline{CS_1} \geq V_{CC} - 0.2V$	2.0	-	3.6	V
Data retention current	IDR	Commercial Industrial	$V_{CC} = 3.0V$ $\overline{CS_1} \geq V_{CC} - 0.2V$ $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$	-	0.2	10 15	$\mu A$
Data retention set-up time	tSDR		See data retention waveform	0	-	-	ms
Recovery time	tRDR			5	-	-	

1.  $\overline{CS_1} \geq V_{CC} - 0.2\text{V}$ ,  $CS_2 \geq V_{CC} - 0.2\text{V}$  ( $\overline{CS_1}$  controlled) or  $CS_2 \leq 0.2\text{V}$  ( $CS_2$  controlled)

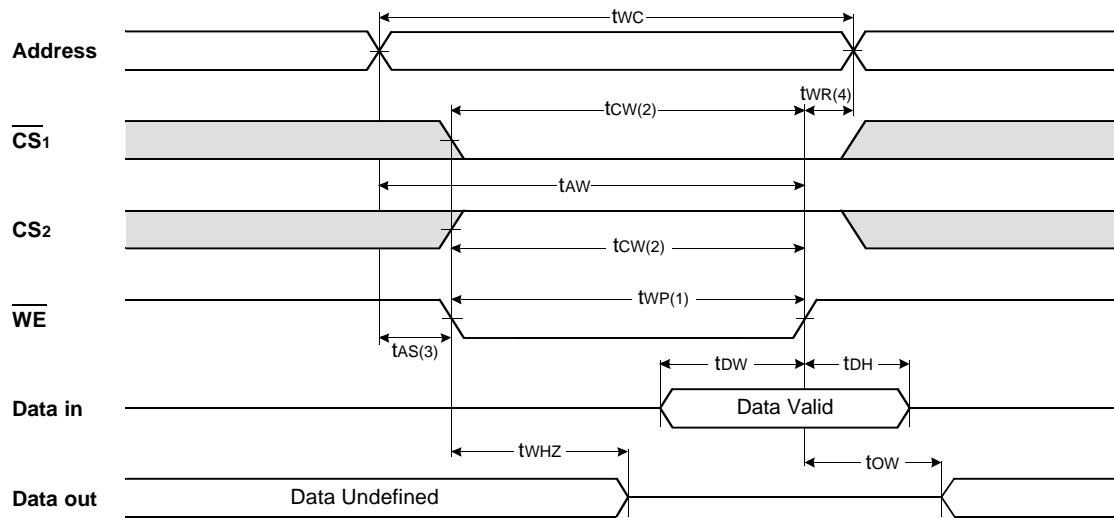
## TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}_1 = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE} = V_{IH}$ )

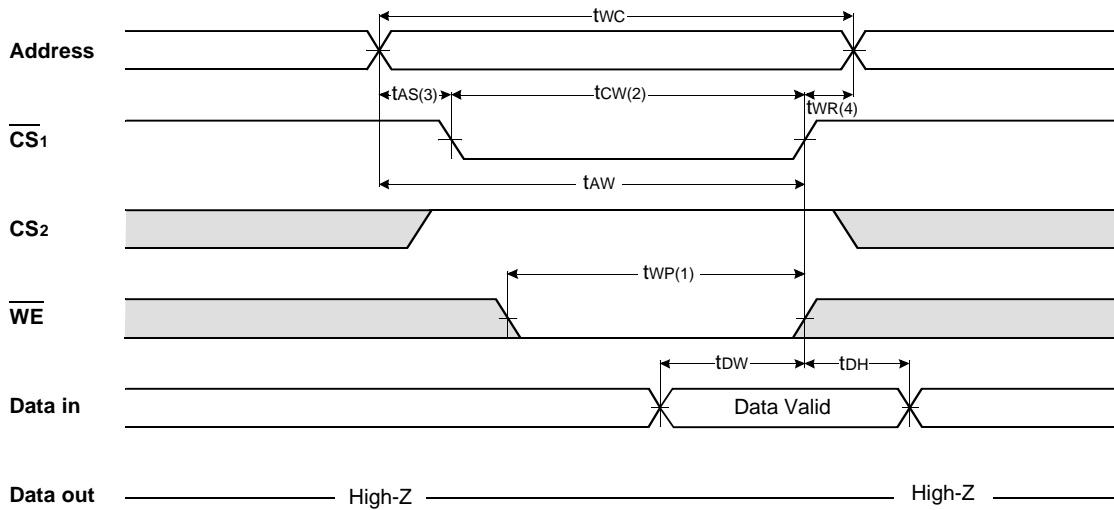
## NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

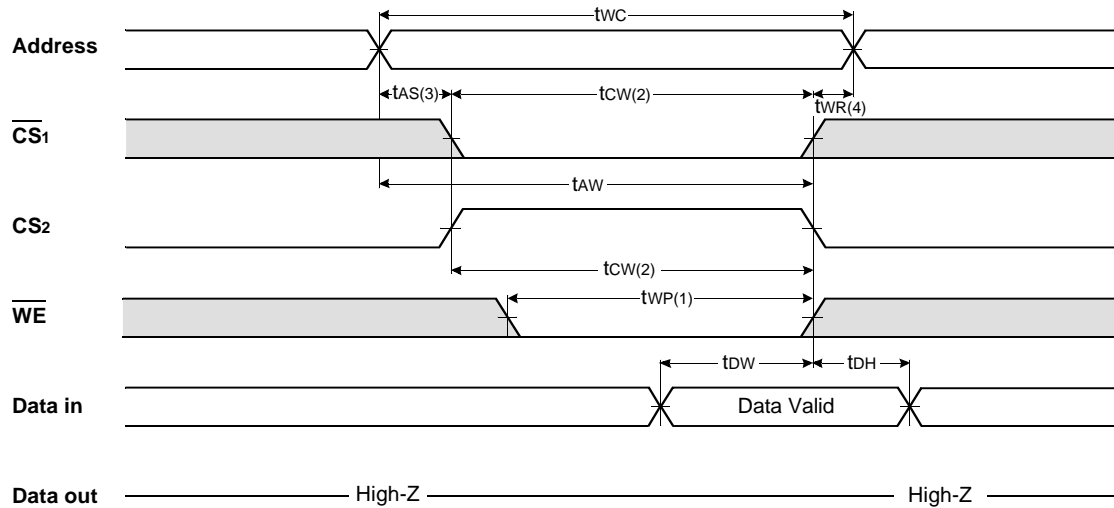
**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS_1}$  Controlled)**



## TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

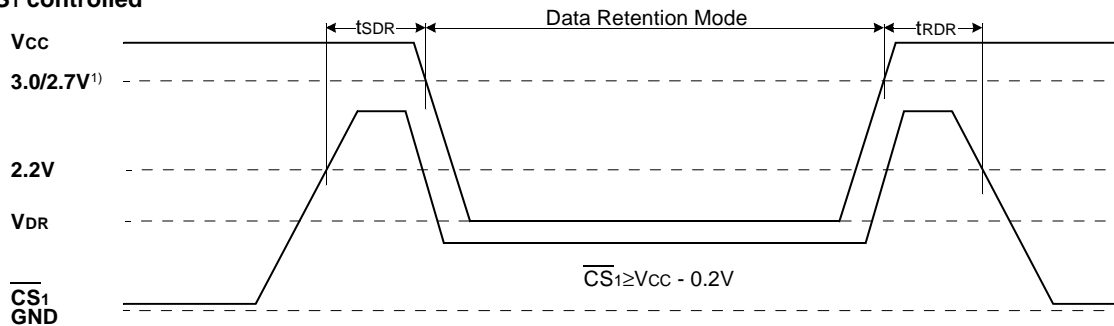


### NOTES (WRITE CYCLE)

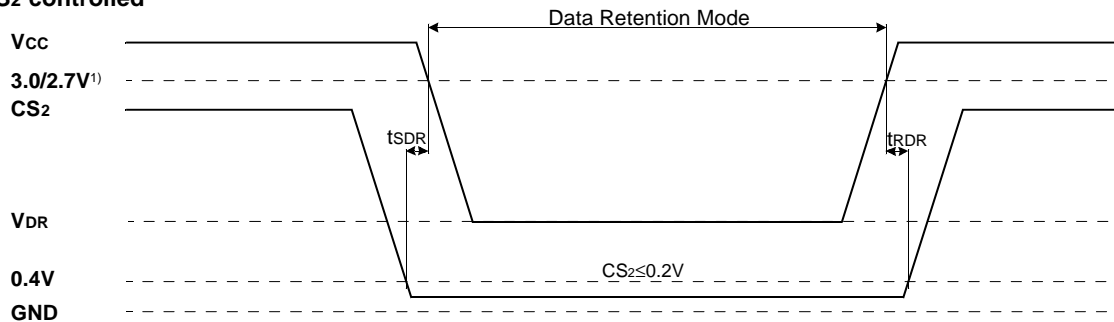
1. A write occurs during the overlap of a low  $\overline{CS_1}$ , a high CS<sub>2</sub> and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS_1}$  goes low, CS<sub>2</sub> going high and  $\overline{WE}$  going low : A write ends at the earliest transition among CS<sub>1</sub> going high, CS<sub>2</sub> going low and  $\overline{WE}$  going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS<sub>1</sub> going low or CS<sub>2</sub> going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as  $\overline{CS_1}$  or  $\overline{WE}$  going high tWR2 applied in case a write ends as CS<sub>2</sub> going to low.

## DATA RETENTION WAVE FORM

### CS<sub>1</sub> controlled



### CS<sub>2</sub> controlled



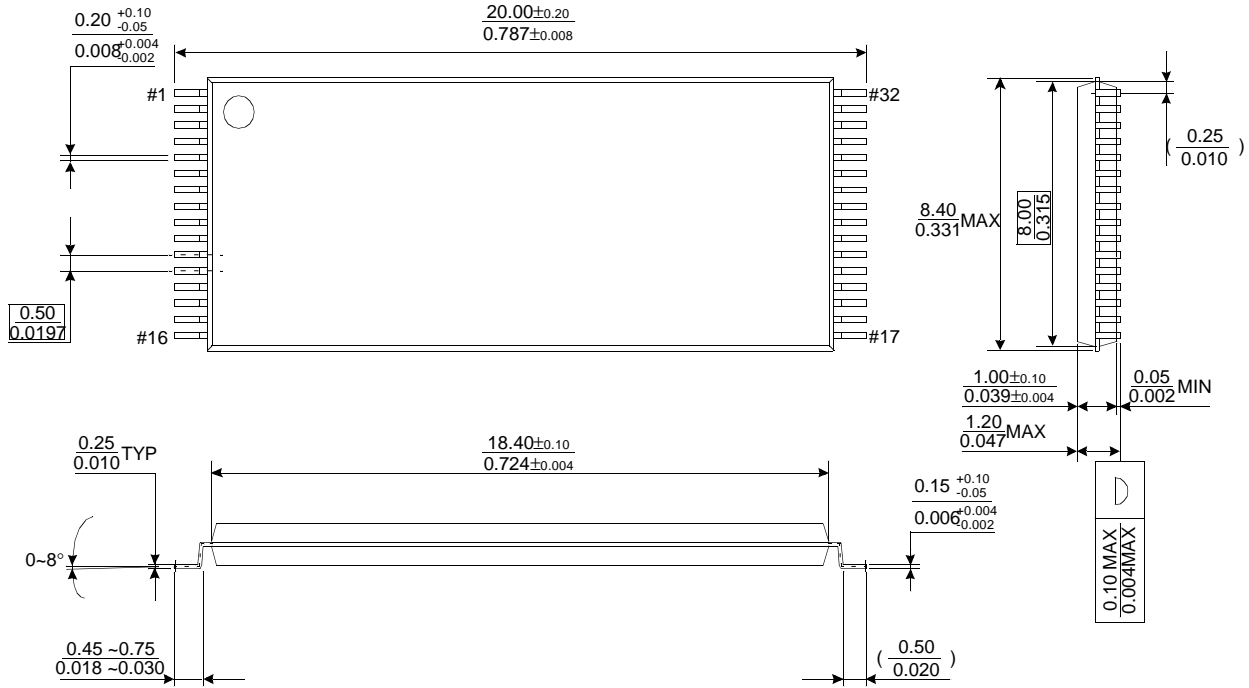
1. 3.0V for K6T2008V2M Family, 2.7V for K6T2008U2M Family.



## PACKAGE DIMENSIONS

Units: millimeters(inches)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



### 32 PIN SMALLER THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

