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KG80/KGM80

0.5μm 5V/3.3V Gate Array Cell Library

April 1997

SAMSUNG

SAMSUNG ASIC

KG80/KGM80
0.5μm 5V/3.3V Gate Array Cell Library
Data Book

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Introduction

This databook contains information about KG80/KGM80, 0.5 μm 5V/3.3V DLM/TLM gate array cell library developed by SEC (Samsung Electronics Corporation).

The “library” basically contains various kinds of internal and I/O cells and soft-macros which are used for developing ASIC (Application Specific Integrated Circuit). It also includes a design kit helping designers to work in a workstation platform, and all sorts of design environments needed for an automatic chip design.

There are six chapters in this databook:

Chapter 1	Introduction to KG80/KGM80
Chapter 2	Electrical Characteristics
Chapter 3	Internal Macrocells
Chapter 4	Input/Output Cells
Chapter 5	Memory Compilers
Chapter 6	JTAG Boundary Scans.

In this databook each cell is followed by its AC electrical characteristics, and these characteristic values are almost equal when the corresponding cell is operated in a real chip.

The purpose of this databook is to prevent any misuse or misapplication of KG80/KGM80 cell library by providing precise information about the cell list, electrical data, directions for use, and matters demanding special attention.

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LIBRARY DESCRIPTION

SEC ASIC offers KG80 5V gate array family and KGM80 3.3V gate array family. KG80 and KGM80 are 0.5μm CMOS processes supporting double-layer or triple-layer metal interconnection options.

The gate array is a kind of design methods. In this design method, all processes before a metal wiring have been completed in a masterslice, and the remaining processes from a metal wiring will be added on the prepared masterslice to form a user-specific circuit. The gate array is used world-widely because of its short period of products development.

With the regard to the mixed using of 5V and 3.3V, 5V-to-3.3V and 3.3V-to-5V convertible cells having level shifters inside themselves are provided in addition to the existing normal input/output cells. Moreover, the other interface cells (CMOS, TTL and Schmitt trigger) are fully equipped for your wide selection.

In order to ensure the product reliability, we efficiently prevent any possible noise, ESD and latch-up. Various kinds of memory compiler, macrofunction and megafunction cells may satisfy the complicated design requirements and offer convenience to users.

There are 14 kinds of masterslices provided (they are preliminary), therefore, you can choose the most appropriate masterslice according to the gate count and pin number of the product.

Every work operation in a design flow has been systematized and automated, and each stage is designed to go through enough reviews and verifications. It makes the design work easier and faster, and prevents any errors or mistakes possible through a design flow.

FEATURES

- ❑ KG80: 5volt gate array library
  KGM80: 3.3volt gate array library
- ❑ Mixed 5V/3.3V I/O interface
- ❑ 0.5μm 5V HCMOS channelless technology
  – Double and Triple layer metal options
- ❑ High basic cell usages
  – 42,400 to 1,250,000 total number of gates
  – Maximum usage: 70% for triple layer metal
  – Maximum usage: 40% for double layer metal
- ❑ High speed
  – 0.2 ns (for KG80) and 0.3ns (for KGM80) delay of 2-input NAND with fanout = 2
- ❑ Fully configurable RAM,ROM and DPRAM
  – Up to 9K-bit RAM available
  – Up to 36K-bit ROM available
  – Up to 9K-bit DPRAM available
- ❑ Configurable FIFO and Multiplier available
- ❑ Operating Temperature (T_A)
  – Commercial range: 0˚C to +70˚C
  – Industrial range: –40˚C to +85˚C
- ❑ ESD and latch-up protection
  – ESD: 2000V (Min.)
  – Latch-up: 300mA (Min.)
- ❑ Selectable output current drive capability
  – 1/2/4/8/12/16/20/24mA available for 5V
  – 1/2/4/6/8/10/12/16mA available for 3.3V
- ❑ TTL, CMOS, LVTTL, LVCMOS and Schmitt trigger I/Os
- ❑ X-tal oscillators
- ❑ PCI, PCMCIA buffers
- ❑ GTL, NTL, CardBus, SCSI, PECL under-developed
- ❑ Various package options
- ❑ Fully integrated CAD software support
  – Verilog, Viewlogic, Mentor and Synopsys

CAE SUPPORT

KG80/KGM80 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor and Synopsys for front-end logic design capture and simulation, and Gate Ensemble and Gards for back-end placement and routing.

For a high simulation accuracy, KG80/KGM80 uses a proprietary delay calculator. Cell delay calculations are based on a matrix of delay parameters for each macrocell, and signal interconnection delay is based on the RC tree analysis.

PRODUCT FAMILY

KG80/KGM80 library include the following design elements:

(a) Internal Macrocells
(b) Input/Output Cells
(c) Macrofunctions
(d) Megafunctions
(e) Memory Compilers
(f) JTAG Boundary Scans.

< Internal Macrocells >

Macrocells are the lowest level of logic functions such as NAND, NOR and flip-flop used for logic designs. There are about 300 different types of internal macrocells. They usually come in two levels of drive strength (1X and 2X).

These macrocells have many levels of representations—logic symbol, logic model, timing model, transistor schematic, HSPICE netlist, physical layout, and placement and routing model.

< Macrofunctions >

Macrofunctions are netlists of logic function which have the complexity of a standard MSI circuit. Macrofunctions are logic building blocks. There are 44 kinds of 74XX (TTL) compatible functions in this library.

< Megafunctions >

Megafunctions are also netlists of logic function, but with a high logic complexity of a standard LSI circuit. Multipliers, barrel shifters, 82XX Intel functions, etc. are supported in this library.

< Memory Compilers>

Memory compilers of KG80/KGM80 consist of asynchronous ROM, single-port RAM, dual-port RAMs, RAM-based FIFO and Multiplier generators. There are two types of dual-port RAMs; one read one write DPRAM and one read/write one read DPRAM.

< Input/Output Cells >

There are about one thousand different I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of the masterslice.

A test logic is provided to enable the efficient parametric (threshold voltage) testing on input buffers including CMOS and TTL level converters, Schmitt trigger input buffers, clock drivers and oscillator buffers. Pull-up and pull-down resistors are optional features.

Three basic types of output buffers (non-inverting, tri-state and open drain) are available in a range of driving capabilities from 1mA to 24mA for 5V drive and 1mA to 16mA for 3.3V drive.Two levels of slew rate controls are provided for each buffer type (except 1mA and 2mA buffers) to reduce output power/ground bus noise and signal ringing, especially in simultaneous switching outputs.

Bi-directional buffers are combinations of input buffers and output buffers (tri-state or open drain) in a single unit. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

For user's convenience, KG80/KGM80 library provides with three options of pull-down and pull-up resistances respectively. They are 50KΩ, 100KΩ, and 200KΩ (The default value is 100KΩ).

I/O Cell Drive Options

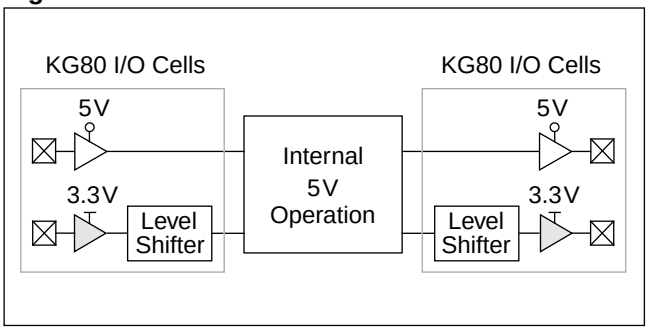
To provide designers with the greater flexibility, each I/O buffer can be selected among various current levels (e.g., 1mA, 2mA, ..., 24mA). The choice of current-level for I/O buffers affects their propagation delay and current noise.

The slew rate control helps decrease the system noise and output signal overshoot/undershoot caused by the switching of output buffers. The output edge rate can be slowed down by selecting the high slew rate control cells. KG80/KGM80 provides three different sets of output slew rate controls. Only one I/O slot is required for any slew rate control options.

5V/3.3V Mixed I/O Cells

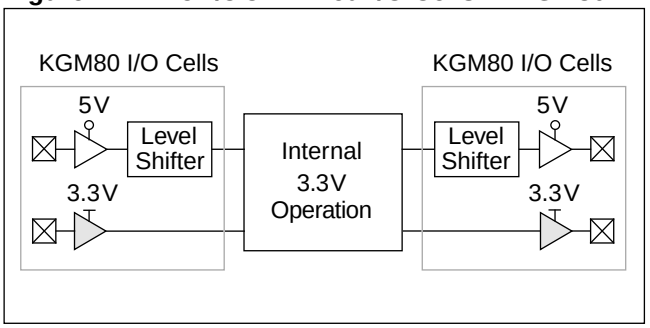
When designers intend to make transitions from 5V supplies to low voltage system, KG80 offers a solution of interfacing problems encountered in mixed 5V/3V environment. This solution provides great flexibility to different devices communicating each other. PCI and PCMCIA buffers are also available in this solution. You can see this in the following figure.

Figure 1-1. 5V/3.3V Mixed I/O Cells in KG80



In KGM80, level shifters are available to provide internal 3V core with great flexibility when it interfaces with a 5V device. Refer to the figure below.

Figure 1-2. 5V/3.3V Mixed I/O Cells in KGM80



PCI Buffers

In addition to input, output, bi-directional, slew rate controlled and Schmitt trigger I/O buffers, SEC ASIC now offers PCI (Peripheral Component Interconnect) I/O buffers. PCI is expected to be better suited to the more complex and feature-rich design than the existing local bus standards. 5V, 3.3V and Universal PCI buffers are included in the library.

CardBus Buffers

CardBus I/O buffers have 3.3V 32-bit bus width and 33MHz of transmission speed. They are for external CardBus type of extension card of notebook PC.

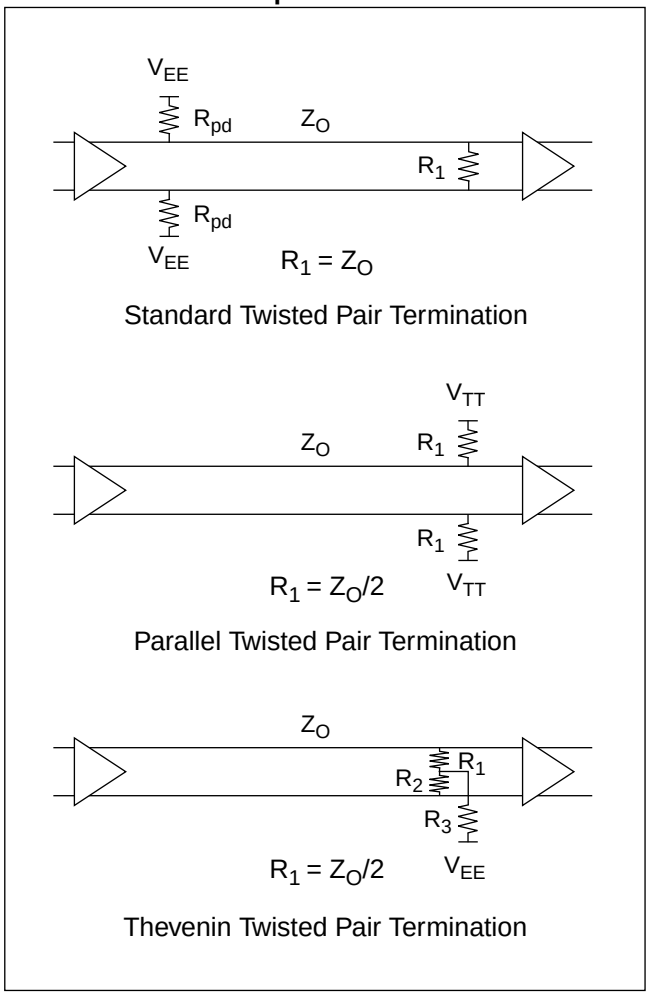
PECL

SEC ASIC's PECL (Positive Emitter Coupled Logic) buffer having 155MHz operating frequency is suited to ATM interface. It supports two voltage source modes; 5V and 3.3V.

The voltage swing level is about 0.8V, being similar to that of ECL, and the external terminator is needed. Its main features are the same as ECL; low noise, high speed and single ended/differential function.

In case of differential transmission, the external terminator is shown in the following figure.

Figure 1-3. Twisted Pair Termination Techniques

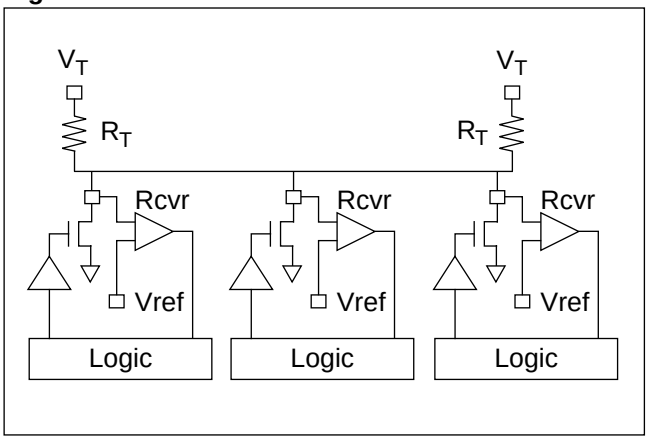


GTL (Gunning Transceiver Logic)

GTL and GTL+ interface I/Os are useful for implementing highly reliable system, satisfying fast and low-powered signal transfers and reducing noise in a switching circuitry.

In all 0.5μm cell libraries in SEC ASIC, GTL interface is fully supported.

Figure 1-4. GTL Interface



LVTTL/LVCMOS

Low Voltage TTL and Low Voltage CMOS I/O buffers have various kinds of applications as normal TTL and CMOS I/O sets. Their key features are low voltage swing and low noise.

Input voltage level is 5V compatible. Output high voltage is 2.4V ~ 3.5V in LVTTL and VDD–0.2V in LVCMOS.

SCSI

SCSI is widely used to extend peripherals, requires external terminator.

SEC ASIC supports SCSI-3 fast-20 parallel interface and SCSI-3 parallel interface only in KG80. Both of them have fail-safe function. SCSI buffer is two times as big as normal buffers.

PCMCIA

PCMCIA (Personnel Computer Memory Card Industry Association) buffers guarantees an accurate logic level even when the internal or external voltage source level of a chip changes between 5V and 3.3V.

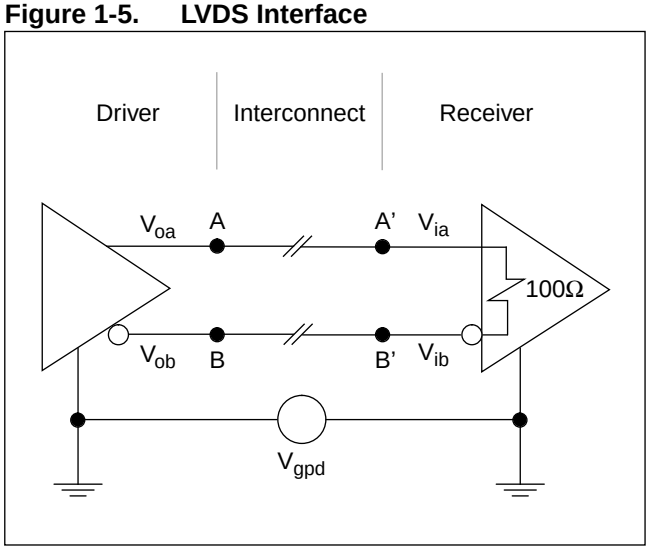
This buffers are designed for 16-bit external extension card of notebook PC.

LVDS

LVDS (Low Voltage Differential Signals) buffer for SCI (Scalable Coherent Interface) system, shown in the following figure, enables high speed I/O interface with SEC ASIC's high frequency PLL.

This structure is designed for high speed point-to-point unidirectional interface. Its main characteristics are much the same as ECL's differential mode; low noise generation, high noise immunity and low level signalling.

Figure 1-5. LVDS Interface



V_{DD}/V_{SS} RULES AND GUIDELINES

There are three types of V_{DD} and V_{SS} in KG80/KGM80, each with its related bus and pad cells. To support the use of mixed voltage, two different V_{DD} types are needed for 5V and 3.3V respectively.

(1) Core logic
  – VSSI, VDD5I (for 5V)
(2) Input buffers (usable when requested)
  – VSSP, VDD5P (for 5V), VDD3P (for 3.3V)
(3) Output buffers
  – VSSO, VDD5O (for 5V), VDD3O (for 3.3V)

The number of V_{DD} and V_{SS} pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching inputs
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency of the design.

Core Logic V_{SS} Bus and VSSI Pad Allocation Guidelines

The purpose of these guidelines is to ensure that V_{DD}/V_{SS} bounce caused by a simultaneous gate switching is kept to minimum. The voltage bounce on the power bus can have a negative impact on a gate-switching speed and even on the functionality of macrocells like flip-flops and latches in an extreme case.

Because of variations in package inductance, the number of V_{DD}/V_{SS} pads required for a specific design is the function of the operating frequency of a chip, i.e., designs operating at high frequency should use more V_{DD}/V_{SS} pads.

- V_{DD} bus width and pad requirements are half of V_{SS}.
- V_{DD}/V_{SS} buses and pads should be distributed evenly in the core and on all sides of the chip.
- Whenever possible, at least one VSSI pad should be used on each side of the chip.
- The total number of core logic V_{DD} pads required is half of VSSI.

The number of VSSI pads required for a design can be calculated from the following expression:

G x S x F x 2.00e−5

,where
G = Total number of used gates,
S = % of simultaneous switching gates,
F = Switching frequency in MHz.

Input Buffer V_{DD}/V_{SS} Pad Allocation Guidelines

These guidelines ensure that an adequate input threshold voltage margin is maintained during a switching.

- One VSSP is required to support 32 input buffers, and one input buffer V_{DD} can support up to 64 inputs.
- For simultaneous switching inputs, one VSSP pad is required for every 20 inputs, and one input buffer V_{DD} pad for every 40 inputs.
- Input buffer V_{SS}/V_{DD} pads should be placed in such a way that they equally divide the input buffers on either side.

Table 1-1. Minimum Input Buffer VSS/VDD for KG80/KGM80 Device Types gives the absolute minimum requirement for each device type.

Table 1-1. Minimum Input Buffer V_{SS}/V_{DD} for KG80/KGM80 Device Types

Devices	Input Buffer V_{SS}	Input Buffer V_{DD}
KG8563D	2	1
KG8144D	3	2
KG8244D	4	2
KG8444D	4	2

Output Buffer V_{DD}/V_{SS} Pad Allocation Guidelines

The number of VSSO pads required for a device can be calculated from the following expressions.

In 5V

$$\Sigma (I_{OL\ Simultaneous\ switching\ outputs}) / 40 + \Sigma (I_{OL\ Normal\ outputs}) / 64$$

In 3.3V

$$\Sigma (I_{OL\ Simultaneous\ switching\ outputs}) / 50 + \Sigma (I_{OL\ Normal\ outputs}) / 80$$

- The total number of output buffer V_{DD} pads required is half of VSSO.
- Output buffer V_{SS}/V_{DD} pads should be placed in such a way that output buffers are equally divided on either side.

POWER DISSIPATION

Estimation of Power Dissipation in CMOS Circuit

CMOS circuits have been traditionally considered to consume low power since they draw very small amount of current in a steady state. However, the recent revolution in a CMOS technology that allows very high gate density has changed the way the power dissipation should be understood. The power dissipation in a CMOS circuit is affected by various factors such as the number of gates, a switching frequency, the loading on the output of a gate, and so on.

Power dissipation is important when designers decide the amount of necessary power supply current for the device to operate in safety. Propagation delays and a reliability of the device also depend on the power dissipation which determines the temperature at which the die operates. To obtain a high speed and a reliability, designers must estimate the power dissipation of the device accurately and determine the appropriate environments including packages and system cooling methods.

This section describes the concept of two types of power dissipation (static and dynamic) in a CMOS circuit, the method of calculating them in the SEC KG80/KGM80 library, and finally their relationship with a temperature.

Static (DC) Power Dissipation

There are two types of static or DC current contributing to the total static power dissipation in CMOS circuits.

One is the leakage current of the gates resulted by a reverse bias between a well and a substrate region. There is no DC current path from power to ground in a CMOS because one of the transistor pair is always off, therefore, no static current except the leakage current flows through the internal gates of the device. The amount of this leakage current is, however, in the range of tens of nano amperes, which is negligible.

The other is DC current that flows through the input and output buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/pull-down transistor included in the input buffers is about 50μA typically, which is also negligible. Therefore, only DC current that the output buffers source or sink has to be counted to estimate the total static power dissipation.

DC power dissipation of TTL output and bi-directional buffers is determined by the following formula:

$$P_{DC_TTL_OUTPUT} = \Sigma(V_{OL} \times I_{OL} \times t_L) + \Sigma((V_{DD} - V_{OH}) \times I_{OH} \times t_H)$$

,where

$t_H = T_{HIGH} / T$,

$t_L + t_H = 1$.

Dynamic (AC) Power Dissipation

When a CMOS gate changes its state, it draws switching current as a result of charging or discharging of a node capacitance, C_L. The energy associated with the switching current for a node capacitance, C_L, is

$$1 / 2 \times (C_L \times V_{DD}^2)$$

,where V_{DD} is a power supply voltage.

The switching occurs twice per cycle for periodic signals: once for charging a capacitance and once for discharging it. Hence, the dynamic power dissipation due to the switching current is the energy divided by the clock period and multiplied by the factor of two, or

$$C_L \times V_{DD} \times V_{DD} / T$$

,where T is a clock period.

As shown above, it is quite straight forward to calculate the dynamic power dissipation for a single gate. The dynamic power dissipation for an entire chip is, however, much more complicated to estimate since it depends on the degree of switching activity of the circuit. SEC has found that the degree of switching activity is 20% on the average and recommends to use this number to estimate the total dynamic power dissipation.

Power Dissipation in KG80/KGM80

This section describes the equations on how to estimate the power dissipation in KG80/KGM80. As explained in the previous section, the total power dissipation (P_{TOTAL}) consists of static power dissipation (P_{DC}) and dynamic power dissipation (P_{AC}).

$$P_{TOTAL} = P_{DC} + P_{AC}$$

Since only output buffers contribute to the static power dissipation,

$$P_{DC} = P_{DC_OUTPUT}$$

,where P_{DC} output is the static power dissipated when output buffers source or sink.

The dynamic power dissipation is caused by three components: input buffers (P_{AC_INPUT}), output buffers (P_{AC_OUTPUT}), and internal cells ($P_{AC_INTERNAL}$).

$$P_{AC} = P_{AC_INPUT} + P_{AC_OUTPUT} + P_{AC_INTERNAL}$$

Each term mentioned above is characterized by the following equations:

In KG80,

$P_{DC_OUTPUT} = 150 \times I_{OL} \times N_output$ [µW]
$P_{AC_INPUT} = 23 \times N_input \times F \times S$ [µW]
$P_{AC_OUTPUT} = 25 \times N_output \times F \times S \times C$ [µW]
$P_{AC_INTERNAL} = 2.3 \times N_internal \times F \times S$ [µW]

In KGM80,

$P_{DC_OUTPUT} = 150 \times I_{OL} \times N_output$ [µW]
$P_{AC_INPUT} = 9.8 \times N_input \times F \times S$ [µW]
$P_{AC_OUTPUT} = 25 \times N_output \times F \times S \times C$ [µW]
$P_{AC_INTERNAL} = 1.2 \times N_internal \times F \times S$ [µW]

,where
I_{OL} is source and sink current of output buffers in mA,
N_output is the number of output buffers used,
N_input is the number of input buffers used,
N_internal is the number of internal cells used,
F is the maximum operation frequency in MHz,
S is the estimated degree of a switching activity (typically 0.2),
C is the output load capacitance in pF.

Temperature and Power Dissipation

The total power dissipation, P_{TOTAL} can be used to find out the device temperature by the following equation:

$$\theta_{JA} = (T_J - T_A) / P_{TOTAL}$$

,where
θ_{JA} is the thermal impedance,
T_J is the junction temperature of the device,
T_A is the ambient temperature.

Thermal impedances of the SEC packages are given in the following table. The junction temperature, obtained by multiplying P_{TOTAL} by the appropriate θ_{JA} and adding T_A, determines the derating factor for the propagation delays and also indicates the reliability measures.

Hence, designers can achieve the desired derating factor and reliability targets by choosing appropriate packages and system cooling methods.

Table 1-2. Thermal Impedances of SEC Packages

	QFP						
Pin Number	**64**	**80**	**100**	**120**	**160**	**208**	**240**
θ_{JA} [°C/W]	60	60	60	50	50	40	40

Maximum Junction Temperature (T_J)

The allowable maximum junction temperatures for plastic and ceramic packages are as follows:

Junction temperature for plastic package ≤ 125°C
Junction temperature for ceramic package ≤ 150°C.

PROPAGATION DELAYS

Interconnection wire length, temperature and supply voltage are the chief factors affecting propagation delays.

Wire Length Load

The loading due to interconnection wire length can be estimated with the following expression. The result is given in terms of number of equivalent standard loads.

$$C_{WL} = C_{FO} \times (0.049 \times \sqrt{A} + 0.48) + 0.079 \times \sqrt{A} + 0.33$$

,where

C_{FO} = Number of fanouts in a standard load,

A = Area of block size in mm^2,

C_{WL} = Number of equivalent standard loads due to an interconnection,

e.g.,

C_{FO} = 7 (standard load),

A = 25mm^2,

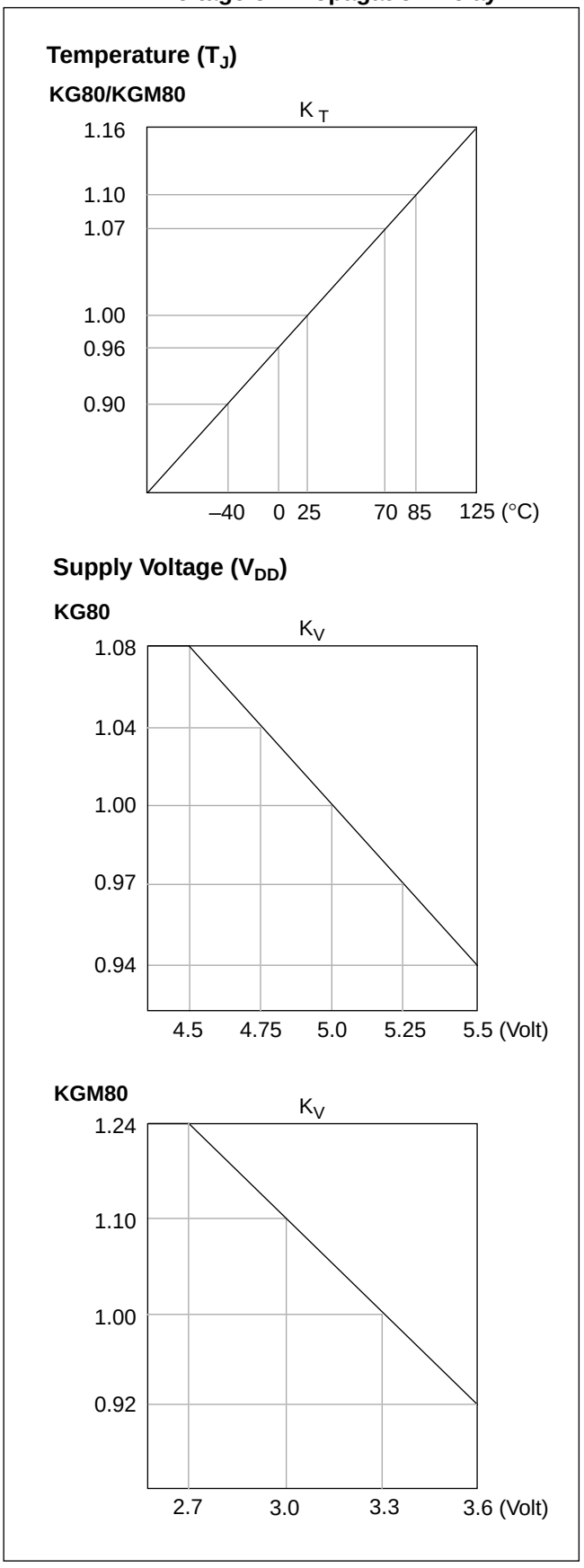
C_{WL} = 5.8 (standard load).

Temperature and Supply Voltage

The next figure describes propagation delay correction factors (K_T, K_V) as a function of on-chip junction temperature (T_J) as well as supply voltage (V_{DD}). As a result of increasing CMOS power dissipation, ambient and junction temperature are generally not the same.

The temperature of the die inside the package (junction temperature, T_J), is calculated using chip power dissipation and the thermal resistance to ambient temperature (θ_{JA}) of the package. Information on package thermal performance can be obtained from SEC application engineers.

Figure 1-6. Effect of Temperature and Supply Voltage on Propagation Delay



Best and Worst Case Conditions

A circuit should be designed to operate properly within a given specification level, either commercial or industrial. It is recommended that circuits be simulated for best case, normal case, and worst case conditions at each specification level.

The following expressions also allow for the effect of process variation on circuit performance.

Best case:

$T_{BC} = K_{PBC} \times K_T \times K_V \times T_{NOM} = K_{BC} \times T_{NOM}$

Worst case:

$T_{WC} = K_{PWC} \times K_T \times K_V \times T_{NOM} = K_{WC} \times T_{NOM}$

,where

T_{BC} = Best case propagation delay

T_{WC} = Worst case propagation delay

T_{NOM} = Normal propagation delay

($T_J = 25^oC$, $V_{DD} = 5V$ and typical process)

K_{PWC} = Worst case process correction factor

K_{PBC} = Best case process correction factor

With above equations, we can calculate the multipliers of K_{WC} and K_{BC} as follows.

Table 1-3. KG80 best case delay

Application	Best case delay			
	Parameter			K_{BC}
	V_{DD}	T_J	Proc.	
Industrial	5.5V	–40 °C	Min.	0.51
Commercial	5.25V	0 °C	Min.	0.56

Table 1-4. KG80 worst case delay

Application	Worst case delay			
	Parameter			K_{WC}
	V_{DD}	T_J	Proc.	
Industrial	4.5V	125 °C	Max.	1.75
Commercial	4.75V	115 °C	Max.	1.66

Table 1-5. KGM80 best case delay

Application	Best case delay			
	Parameter			K_{BC}
	V_{DD}	T_J	Proc.	
Industrial	3.6V	–40 °C	Min.	0.50
Commercial	3.6V	0 °C	Max.	0.53

Table 1-6. KGM80 worst case delay

Application	Worst case delay			
	Parameter			K_{WC}
	V_{DD}	T_J	Proc.	
Industrial	2.7V	125 °C	Max.	2.02
Commercial	3.0V	115 °C	Max.	1.77

Derating factors of KG80/KGM80

The multipliers can be applied to nominal delay data in order to estimate the effects of supply voltage, temperature and process. Nominal data are provided for conditions of $V_{DD} = 5V$, $T_A = 25°C$ and typical process.

The derating factors of KG80/KGM80 are as follows.

Table 1-7. KG80/KGM80 process derating factor

Process Factor (K_P)	Slow	Typ.	Fast
	1.40	1.00	0.60

Table 1-8. KG80 temperature derating factor

Temp. (°C)	125	85	70	25	0	–40
K_T	1.16	1.10	1.07	1.00	0.96	0.90

Table 1-9. KGM80 temperature derating factor

Temp. (°C)	125	85	70	25	0	–40
K_T	1.15	1.09	1.07	1.00	0.96	0.90

Table 1-10. KG80 voltage derating factor (K_V)

Voltage (V)	5.5	5.25	5	4.75	4.5
K_V	0.94	0.97	1.00	1.04	1.08

Table 1-11. KGM80 voltage derating factor (K_V)

Voltage (V)	3.6	3.3	3.0	2.7
K_V	0.92	1.00	1.10	1.24

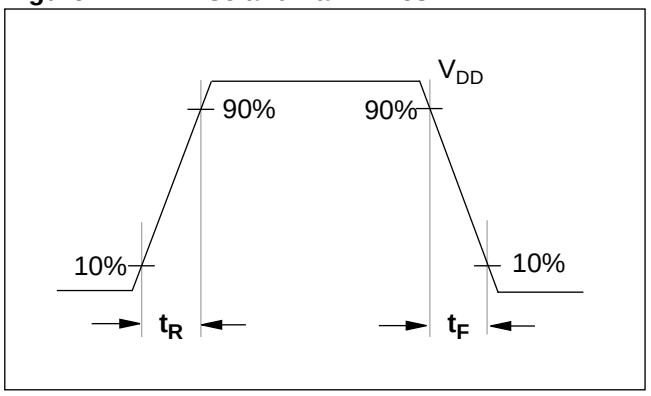
Timing Parameters

This section discusses issues involving timing parameters for primitive cells.

RISE / FALL TIMES

The definition of rise time (t_R) and fall time (t_F) is shown in the following figure.

Figure 1-7. Rise and Fall Times

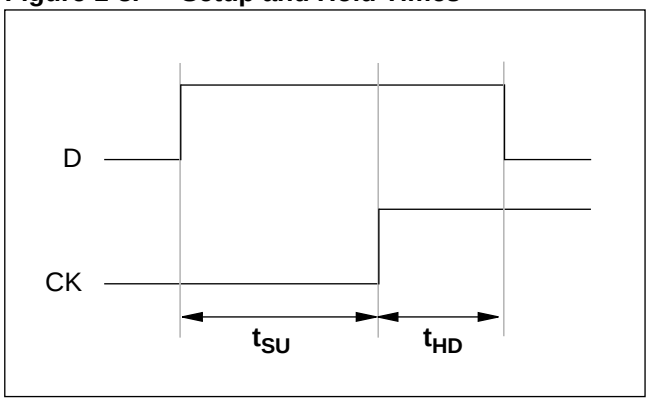


SETUP / HOLD TIMES

Setup time (t_{SU}) is a minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs. Hold time (t_{HD}) is a minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred.

The next figure shows the relationship between setup and hold times for a standard flip-flop triggered on the rising edge of the clock.

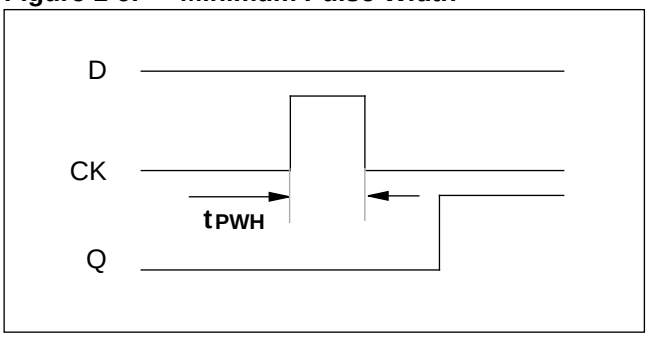
Figure 1-8. Setup and Hold Times



MINIMUM PULSE WIDTHS

Minimum clock pulse widths (t_{PWH}, t_{PWL}) are the time intervals during a clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch.

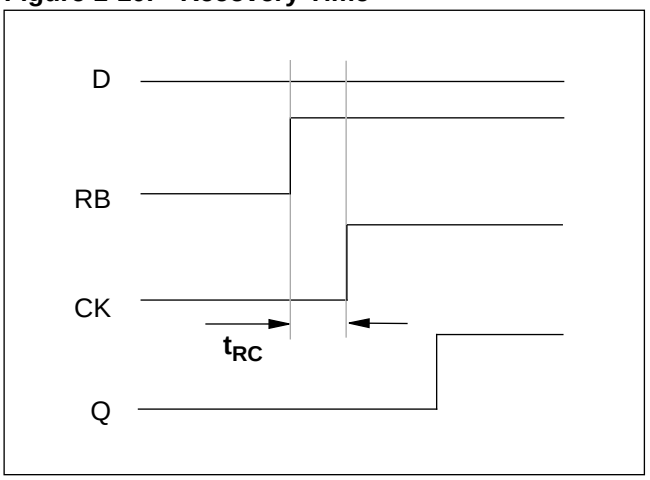
Figure 1-9. Minimum Pulse Width



RECOVERY TIMES

Recovery time (t_{RC}) is the minimum time after an asynchronous pin is disabled that an active clock edge will propagate data from input to output. If the active edge or clock occurs before the specified recovery time, the input data will not propagate.

Figure 1-10. Recovery Time

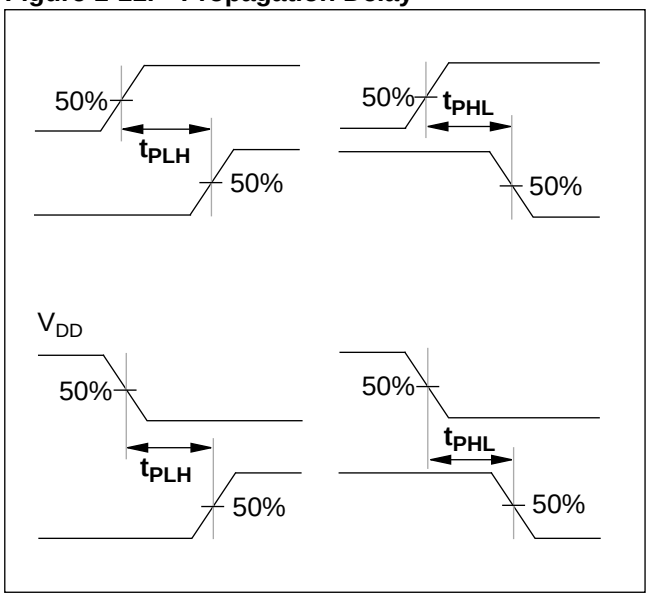


PROPAGATION DELAYS

A delay for a macrocell is considered to be a rising delay (t_{PLH}) if the signal on the output pin is rising. For a rising input and a rising output, the rising delay is the interval between the times the input becomes 50% of supply voltage (V_{DD}) and the output becomes 50% of V_{DD}.

If the input is falling and the output is rising, the rising delay is the interval between the times the input falls to 50% of V_{DD} and the output rises to 50% of V_{DD}. The converse is true for a falling delay (t_{PHL}).

Figure 1-11. Propagation Delay

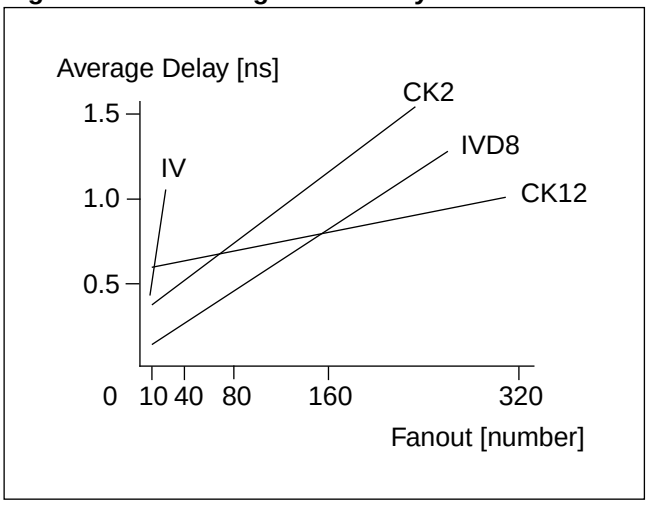


Proper Use of Buffers

Figure 1-12. Average Gate Delay in KG80 shows the average propagation delays of an internal inverter (IV), an 8X inverter (IVD8), a normal clock driver (CK2), and a high clock driver (CK12) in KG80.

Note that transistors uses in I/O slots are larger and have ON channel resistance about one order of magnitude lower than those of the N and P channel transistors in primitive cells. This makes them likely candidates for use as buffers for high fanout signals. For example, CK2 and CK12 buffers require one I/O slot location. Both can be used as high fanout internal buffers.

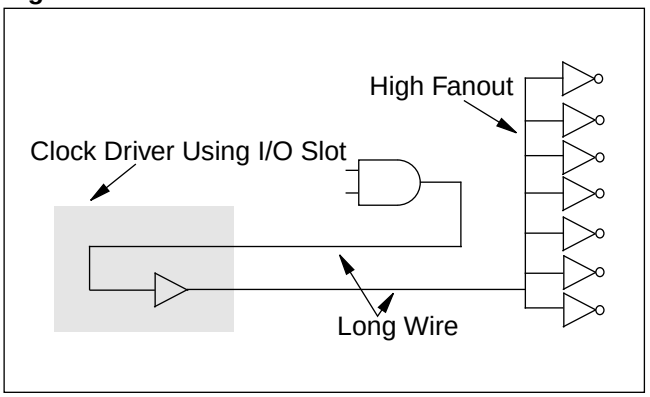
Figure 1-12. Average Gate Delay in KG80



One caution, emphasized in Figure 1-13. Use of I/O Slot for an Internal Buffer, shows that if you route to a buffer that uses an I/O slot from an internal element and back into internal logic, the additional wiring needed could increase propagation delays materially. Higher drive strength internal cells may be more appropriate than I/O slot buffers.

Realize also that using I/O slot cells for internal buffering removes those locations for use as external I/Os and uses two wiring channels, thereby increasing routability congestion on masterslice products.

Figure 1-13. Use of I/O Slot for an Internal Buffer



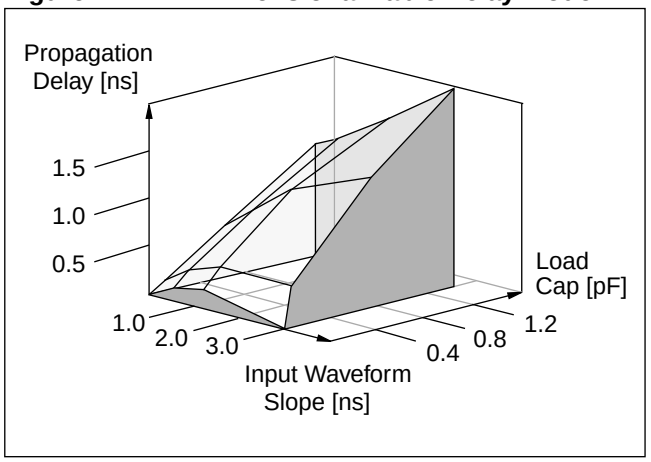
DELAY MODEL

The ASIC timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout loads and distributed interconnection wire resistance and capacitance.
- Interconnection wire delay across the metal lines.
- Timing requirement parameters such as setup time, hold time, recovery time, skew time, minimum pulse width, etc.
- Derating factors for junction temperature, power supply voltage, and process variations.

Timing model for KG80/KGM80 focuses on how to characterize cell propagation delay time accurately. To accomplish this goal, 2-dimensional table look-up delay model has been adopted. The index variables of this table are input waveform slope and output load capacitance. See the figure below. SEC ASIC design automation system supports an n-dimensional table model even though we adopted 2-dimensional model for our 0.5μm cell-based products.

Figure 1-14. 2-Dimensional Table Delay Model



The Table 1-12. Table Delay Model Example shows an example of this model for 2-input NAND cell. The data in this table are high-to-low transition delay times from one of the two input pins to output pin. The number of points and values of the index variables can differ for each cell.

Table 1-12. Table Delay Model Example

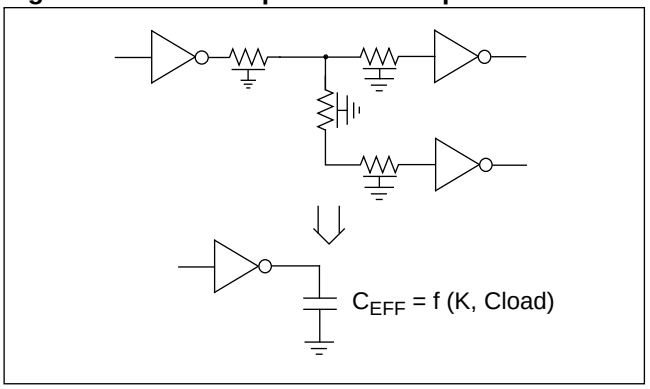
Slope \ Cap.	0.03	0.13	0.53	1.32
0.10	0.07	0.14	0.42	0.97
0.30	0.08	0.17	0.45	1.02
0.80	0.06	0.18	0.51	1.07
1.60	0.01	0.18	0.60	1.18

Notice that 4-by-4 table is used. Delay values between grid points and beyond this table are determined by linear interpolation and extrapolation methods. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a commonly-accepted way in industry.

The delay time due to the interconnection wire can be separated into two components. One is the signal propagation delay time across the metal lines. This delay time component is computed through conventional RC analysis based on $\prod$-model. The other is an additional delay on the driving cell due to the wire load. The traditional way to compute this is based on the lumped capacitance model, ignoring wire resistance.

For sub-micron technology, this approximation cannot be accepted any more. The wire resistance has a shielding effect on the driving cell from load capacitances. An effective capacitance C_{EFF}, a single capacitance approximating distributed interconnection wire resistance and capacitance, is derived, as illustrated in the following figure. The compensation factor K, extracted for each cell, is a function of the length of interconnection wires and the layout topology. All these effects are merged to determine the effective capacitance and this value is used as an index of the table delay model.

Figure 1-15. Concept of Effect Capacitance



The figure below summarizes the features of SEC ASIC's delay model.

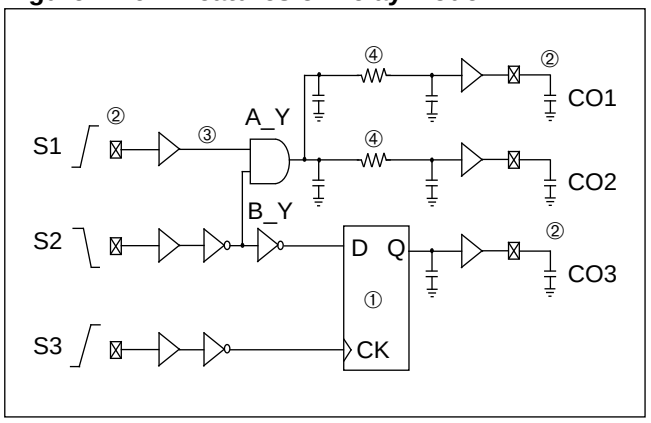
① 2-dimensional table delay model for output loading and input waveform slope effects is used. The slopes (t_R, t_F) and delay times (t_{PLH}, t_{PHL}) of all cell instances are calculated recursively.

② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.

③ Pin to pin delays of cells and interconnection wires are supported.

④ The effect of distributed interconnection wire resistance and capacitance on cell delay is analysed using the effective capacitance concept.

Figure 1-16. Features of Delay Model



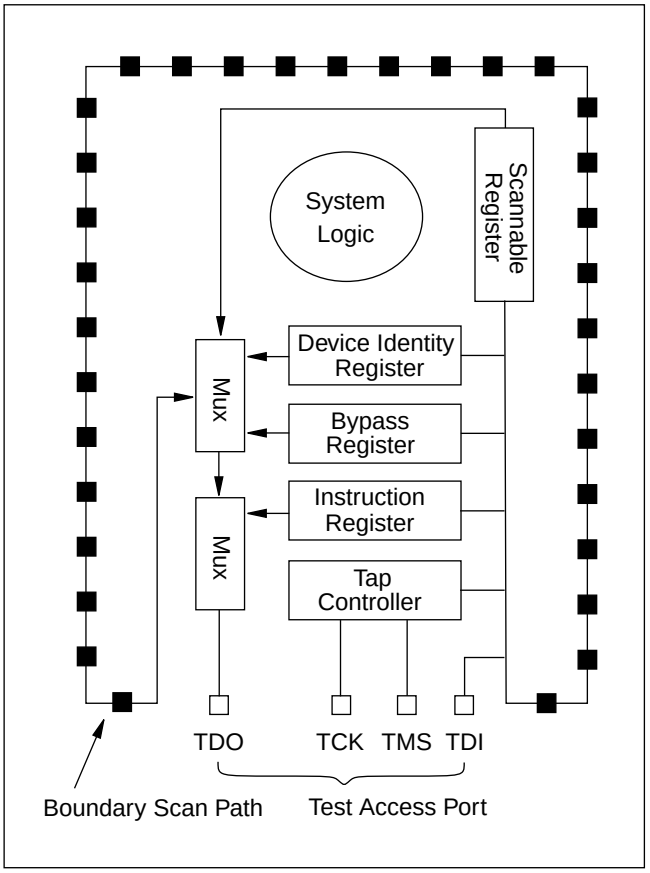
TESTABILITY DESIGN METHODOLOGY

Scan Design

- Multiplexed scan flip-flop that minimizes the area or delay overhead needed to implement scan design
- Automated design rules checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

Boundary-Scan

- IEEE Std 1149.1
- 5 types of JTAG boundary-scan cells
- Boundary-Scan Description Language (BSDL) description for board testing
- Combination with internal scan design



MAXIMUM FANOUTS

Internal Macrocells

The maximum fanouts for KG80/KGM80 primitive cells are as follows. Note that these fanout limitation values are calculated when the rise and fall times of the input signal is 0.40 ns. Depending on the rise and fall times, the maximum fanout limitations can be varied case by case.

In the following table the maximum fanout values for all pins of KG80/KGM80 internal macrocells are listed.

Table 1-13. Maximum Fanouts of Internal Macrocells (When t_R/t_F = 0.40 ns)

Cell Name	Output Pin	Maximum Fanout	
		KG80	KGM80
Logic Cells			
AD2	Y	22	34
AD2D2	Y	46	70
AD3	Y	22	34
AD3D3	Y	69	103
AD4	Y	22	34
AD4D2	Y	44	68
AD5	Y	22	34
AD5D2	Y	44	65
ND2	Y	22	34
ND2D2	Y	48	72
ND3	Y	20	33
ND3D2	Y	44	70
ND4	Y	15	26
ND4D2	Y	32	53
ND5	Y	11	19
ND5D2	Y	23	40
ND6	Y	22	34
ND6D2	Y	45	69
ND8	Y	22	34
ND8D2	Y	45	69
NR2	Y	11	17
NR2D2	Y	24	35
NR3	Y	6	9
NR3D2	Y	14	21
NR4	Y	5	7
NR4D2	Y	10	14
NR5	Y	22	34
NR5D2	Y	45	70
NR6	Y	22	34
NR6D2	Y	70	104
NR8	Y	21	33
NR8D2	Y	46	71
OR2	Y	22	34
OR2D2	Y	45	69
OR3	Y	22	34
OR3D3	Y	71	106
OR4	Y	21	33
OR4D2	Y	45	68
OR5	Y	21	33
OR5D2	Y	45	68
XN2	Y	22	34
XN2D2	Y	46	70
XN3	Y	22	34
XN3D3	Y	69	104
XO2	Y	22	34
XO2D2	Y	46	70
XO3	Y	22	34
XO3D3	Y	70	106
AO21	Y	11	16
AO21D2	Y	22	32
AO211	Y	6	9
AO211D2	Y	13	20
AO22	Y	10	15
AO22D2	Y	45	70
AO22A	Y	10	15
AO22D2A	Y	45	69
AO222	Y	5	8
AO222D2	Y	46	70
AO222A	Y	7	11
AO222D2A	Y	46	70
AO33	Y	9	14
AO33D2	Y	46	70
AO333	Y	2	5
AO333D2	Y	46	71
OA21	Y	11	16
OA21D2	Y	24	34
OA211	Y	11	16
OA211D2	Y	23	34
OA22	Y	10	15
OA22D2	Y	21	32

Cell Name	Output Pin	Maximum Fanout	
		KG80	KGM80
OA22A	Y	11	16
OA22D2A	Y	24	35
OA2222	Y	22	34
OA2222D2	Y	46	71
DL1D2	Y	48	90
DL1D4	Y	103	148
DL2D2	Y	50	90
DL2D4	Y	104	155
DL3D2	Y	49	89
DL3D4	Y	102	177
DL4D2	Y	48	87
DL4D4	Y	98	146
DL5D2	Y	48	87
DL5D4	Y	98	147
DL10D2	Y	50	90
DL10D4	Y	105	154
IV	Y	22	34
IVD2	Y	49	74
IVD3	Y	76	114
IVD4	Y	100	153
IVD6	Y	149	229
IVD8	Y	189	294
IVA	Y	51	76
IVD2A	Y	105	161
IVD3A	Y	152	238
IVD4A	Y	191	296
IVCD11	All Pins	21	34
IVCD13	Y	19	31
	YN	76	114
IVCD22	Y	46	70
	YN	49	74
IVCD26	Y	40	64
	YN	151	229
IVCD44	Y	100	143
	YN	100	153
IVT	Y	29	50
IVTD2	Y	62	105
IVTD4	Y	131	203
IVTD8	Y	259	405
IVTN	Y	28	49
IVTND2	Y	61	103
IVTND4	Y	127	203
IVTND8	Y	252	405

Cell Name	Output Pin	Maximum Fanout	
		KG80	KGM80
NID	Y	22	34
NID2	Y	46	69
NID3	Y	69	107
NID4	Y	97	142
NID6	Y	133	219
NID8	Y	155	301
NIT	Y	29	50
NITD2	Y	62	106
NITD4	Y	129	203
NITD8	Y	259	399
NITN	Y	29	50
NITND2	Y	60	103
NITND4	Y	126	203
NITND8	Y	259	428
Flip-Flops			
FD1	All Pins	22	34
FD1D2	All Pins	46	71
FD1CS	All Pins	22	34
FD1CSD2	Q	45	69
	QN	46	70
FD1S	All Pins	22	34
FD1SD2	All Pins	46	71
FD1Q	Q	22	34
FD1QD2	Q	46	70
FD1X2	All Pins	22	34
FD1X4	All Pins	22	34
YFD1	Q	21	33
	QN	20	32
YFD1D2	Q	43	68
	QN	42	66
FD2	All Pins	22	34
FD2D2	All Pins	46	71
FD2CS	All Pins	22	34
FD2CSD2	Q	45	70
	QN	46	71
FD2S	All Pins	22	34
FD2SD2	All Pins	46	71
FD2Q	Q	22	34
FD2QD2	Q	46	70
FD2X2	All Pins	22	34
FD2X4	All Pins	22	34
YFD2	Q	21	33
	QN	20	32

Cell Name	Output Pin	Maximum Fanout	
		KG80	KGM80
YFD2D2	Q	44	68
	QN	41	65
FD2T	Q	17	33
	Z	17	40
FD2TD2	Q	34	69
	Z	34	76
FD2TCS	Q	21	33
	Z	22	40
FD2TCSD2	Q	43	67
	Z	42	76
FD2TS	Q	21	33
	Z	21	40
FD2TSD2	Q	43	69
	Z	43	76
FD3	All Pins	22	34
FD3D2	All Pins	46	70
FD3CS	All Pins	22	34
FD3CSD2	Q	46	70
	QN	45	69
FD3S	All Pins	22	34
FD3SD2	All Pins	46	71
FD3Q	Q	22	34
FD3QD2	Q	46	70
FD3X2	All Pins	22	34
FD3X4	All Pins	22	34
YFD3	Q	21	33
	QN	19	30
YFD3D2	Q	42	67
	QN	39	62
FD4	All Pins	22	34
FD4D2	All Pins	46	70
FD4CS	All Pins	22	34
FD4CSD2	Q	46	70
	QN	45	69
FD4S	All Pins	22	34
FD4SD2	All Pins	46	70
FD4Q	Q	22	34
FD4QD2	Q	45	70
FD4X2	All Pins	22	34
FD4X4	All Pins	22	34
YFD4	Q	20	32
	QN	19	30

Cell Name	Output Pin	Maximum Fanout	
		KG80	KGM80
YFD4D2	Q	43	68
	QN	38	61
FD5	All Pins	22	34
FD5D2	All Pins	46	70
FD5S	All Pins	22	34
FD5SD2	All Pins	46	70
FD5X4	All Pins	22	34
FD6	All Pins	22	34
FD6D2	All Pins	46	70
FD6S	All Pins	22	34
FD6SD2	All Pins	46	70
FD7	All Pins	22	34
FD7D2	All Pins	46	70
FD7S	All Pins	22	34
FD7SD2	All Pins	46	70
FD8	All Pins	22	34
FD8D2	All Pins	46	70
FD8S	All Pins	22	34
FD8SD2	All Pins	46	70
FDS2	All Pins	22	34
FDS2D2	All Pins	46	70
FDS2CS	All Pins	22	34
FDS2CSD2	All Pins	46	70
FDS2S	All Pins	22	34
FDS2SD2	Q	46	71
	QN	46	70
FDS3	All Pins	22	34
FDS3D2	All Pins	45	70
FG1	All Pins	22	34
FG1X4	All Pins	22	34
FG2	All Pins	22	34
FG2X4	All Pins	22	34
FJ1	All Pins	22	34
FJ1D2	All Pins	46	70
FJ1S	All Pins	22	34
FJ1SD2	All Pins	46	71
FJ2	All Pins	22	34
FJ2D2	All Pins	46	70
FJ2S	All Pins	22	34
FJ2SD2	All Pins	46	70
FJ4	All Pins	22	34
FJ4D2	All Pins	45	70
FJ4S	All Pins	22	34

Cell Name	Output Pin	Maximum Fanout	
		KG80	KGM80
FJ4SD2	All Pins	45	70
FT2	All Pins	22	34
FT2D2	All Pins	46	70
FT3	All Pins	22	34
FT3D2	All Pins	46	70
Latches			
LD1	All Pins	22	34
LD1D2	All Pins	46	71
LD1S	All Pins	22	34
LD1SD2	All Pins	46	71
LD1Q	Q	22	34
LD1QD2	Q	44	70
LD1X4	All Pins	22	34
LD1X4D2	All Pins	46	70
YLD1	Q	20	32
	QN	22	34
YLD1D2	Q	41	66
	QN	44	69
LD1A	Q	22	34
LD1B	All Pins	21	32
LD2	All Pins	22	34
LD2D2	All Pins	46	70
LD2Q	Q	22	34
LD2QD2	Q	45	70
YLD2	Q	19	30
	QN	21	33
YLD2D2	Q	39	62
	QN	44	68
LD3	All Pins	22	34
LD3D2	All Pins	45	70
LD4	All Pins	22	34
LD4D2	Q	45	70
	QN	44	70
LD5	All Pins	22	34
LD5D2	All Pins	46	70
LD5S	All Pins	22	34
LD5SD2	All Pins	46	71
LD5X4	All Pins	22	34
LD5X4D2	All Pins	46	70
LD6	All Pins	22	34
LD6D2	All Pins	46	70
LD7	All Pins	22	34
LD7D2	All Pins	45	70

Cell Name	Output Pin	Maximum Fanout	
		KG80	KGM80
LD8	All Pins	22	34
LD8D2	Q	45	70
	QN	44	70
LDS2	All Pins	22	34
LDS6	All Pins	22	34
LS0	All Pins	21	34
LS0D2	All Pins	46	70
LS1	All Pins	10	15
LS2	All Pins	21	33
Bus Holder			
BUSHOLDER	Y	10,000	10,000
Internal Clock Drivers			
CK2	Y	Fig 1-17 (a)	Fig 1-18 (a)
CK4	Y	Fig 1-17 (b)	Fig 1-18 (b)
CK6	Y	–	Fig 1-18 (c)
CK8	Y	Fig 1-17 (c)	Fig 1-18 (d)
CK12	Y	Fig 1-17 (d)	–
Decoders			
DC4	All Pins	22	34
DC4I	All Pins	22	34
DC8I	All Pins	22	34
Adders			
FA	All Pins	22	34
FAD2	All Pins	46	70
HA	All Pins	22	34
HAD2	All Pins	46	71
Multiplexers			
MX2	Y	22	34
MX2D3	Y	69	106
MX2X4	All Pins	22	34
YMX2	Y	22	34
YMX2D2	Y	44	69
MX2I	YN	11	16
MX2ID2	YN	46	70
MX2IA	YN	11	16
MX2ID2A	YN	46	70
MX2IX4	All Pins	15	22
MX3I	YN	22	34
MX3ID2	YN	46	70
MX4	Y	22	34
MX4D2	Y	45	69
YMX4	Y	22	34
YMX4D2	Y	45	70

Cell Name	Output Pin	Maximum Fanout	
		KG80	KGM80
MX5	Y	22	34
MX5D2	Y	46	70
MX8	Y	22	34
MX8D2	Y	44	67
YMX8	Y	22	34
YMX8D2	Y	45	70

I/O Cells

The maximum fanouts for 5V and 3.3V I/O cells are as follows when the rise and fall times of the input signal is 0.40ns.

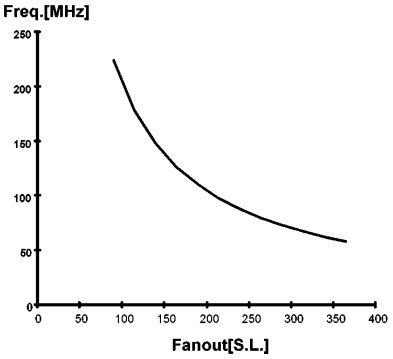
The graphs for fanout vs. frequency curve of KG80/KGM80 internal/input clock drivers are shown in the next page.

Table 1-14. Maximum Fanouts of I/O Cells (When t_R/t_F = 0.40ns)

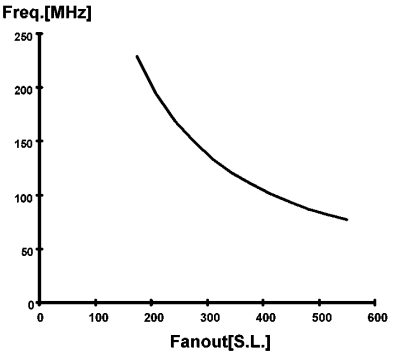
Cell Name	Output Pin	Maximum Fanouts	
		KG80	KGM80
PIC	PO	43	67
	Y	111	216
PICD	PO	43	67
	Y	114	222
PICU	PO	43	67
	Y	115	205
PIL PILD	PO	43	–
	Y	132	–
PILU	PO	43	–
	Y	133	–
PIS	PO	43	67
	Y	88	287
PISD	PO	43	67
	Y	86	237
PISU	PO	43	67
	Y	86	329
PITb	PO	43	–
	Y	87	–
PLIC	PO	32	–
	Y	141	–
PLICD	PO	32	–
	Y	152	–
PLICU	PO	32	–
	Y	145	–
PLIS	PO	32	–
	Y	168	–
PLISD	PO	32	–
	Y	174	–
PLISU	PO	32	–
	Y	118	–
PHIC	PO	–	55
	Y	–	220
PHICD	PO	–	55
	Y	–	223
PHICU	PO	–	55
	Y	–	216
PHIL	PO	–	55
	Y	–	211
PHILD	PO	–	55
	Y	–	244
PHILU	PO	–	55
	Y	–	210
PHIS	PO	–	55
	Y	–	204
PHISD	PO	–	55
	Y	–	225
PHISU	PO	–	55
	Y	–	227
PHIT PHITD	PO	–	55
	Y	–	225
PHITU	PO	–	55
	Y	–	232
PSCKDab2	Y	Fig 1-17 (a)	Fig 1-18 (a)
PSCKDab4	Y	Fig 1-17 (b)	Fig 1-18 (b)
PSCKDab6	Y	–	Fig 1-18 (c)
PSCKDab8	Y	Fig 1-17 (c)	Fig 1-18 (d)
PSCKDab12	Y	Fig 1-17 (d)	–
PSOSCM1 PSOSCM2	PADY	530	1214
	YN	527	1198
PSOSCM3	PADY	1052	2430
	YN	264	600
PSOSCM4	PADY	2022	4850
	YN	2337	5347
PSOSCM5	PADY	3011	7359
	YN	524	1194
PSOSCM6	PADY	4025	9982
	YN	2335	5344

Figure 1-17. Fanout (SL) vs. Frequency Curve of KG80 Clock Drivers

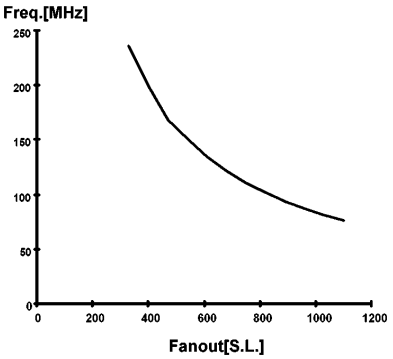
(a) CK2 PSCKDab2



(b) CK4 PSCKDab4



(c) CK8 PSCKDab8



(d) CK12 PSCKDab12

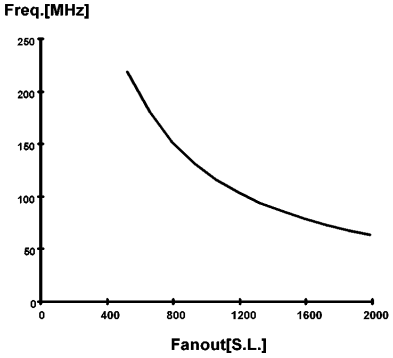
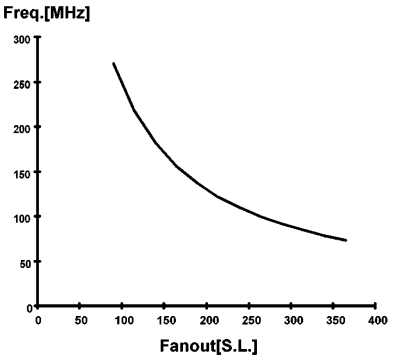
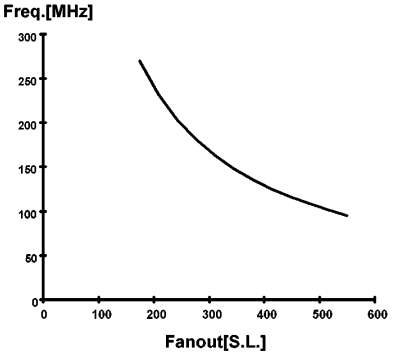


Figure 1-18. Fanout (SL) vs. Frequency Curve of KGM80 Clock Drivers

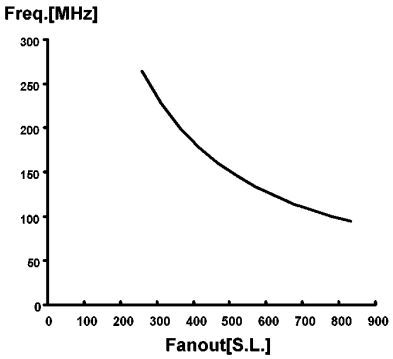
(a) CK2 PSCKDab2



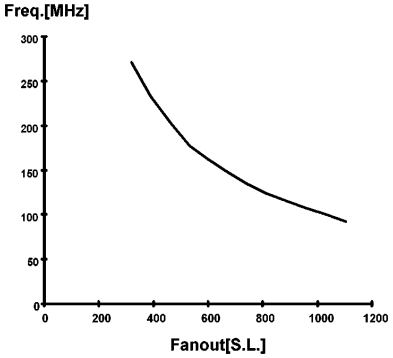
(b) CK4 PSCKDab4



(c) CK6 PSCKDab6



(d) CK8 PSCKDab8



PRODUCT LINE-UP

(The information below is preliminary, and can be changed or added by SEC ASIC.)

Table 1-15. KG80/KGM80 Masterslices (100μm Pad Pitch)

Device	Total Gates	Usable Gates		Total Pads
		DLM	TLM	
KG8563D	56,950	22,800	31,300	100
KG8144D	145,306	51,000	73,000	160
KG8244D	242,604	73,000	109,000	208
KG8444D	443,190	111,000	177,000	280

NOTES:

1. Usable gates are estimated; the actual number of usable gates is design-dependent.
2. I/O pads can be used as V_{DD}/V_{SS} pads.
3. Each clock driver cell occupies one I/O slot.
4. Total pad count includes the corner power pads.

PACKAGES

(The information below is preliminary, therefore, when you choose a package type for your product, or if you want to use the other types of packages, please contact to SEC ASIC.)

Table 1-16. Package Options

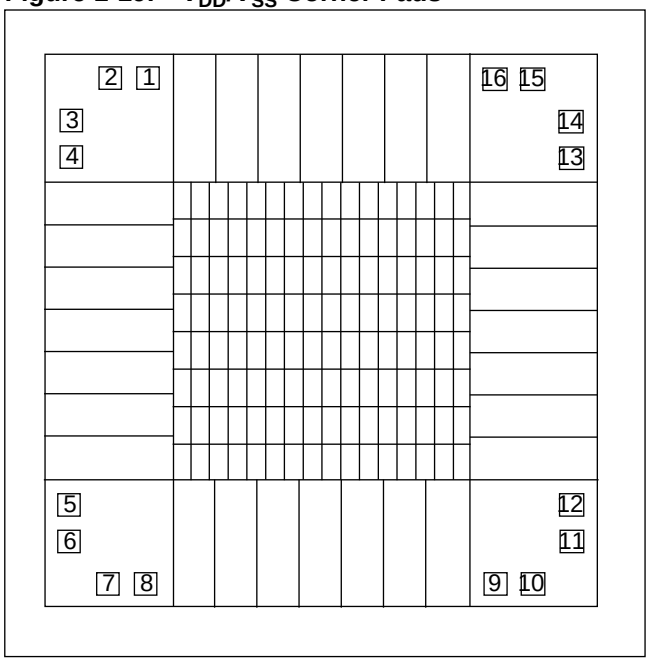
Type	DIP				SDIP									SOP		PLCC					QFP									
Pin / Master	24	28	40	42	24	28	30	32	40	42	48	54	64	28	32	28	32	44	68	84	44	48	60	64	80	100	128	132	160	208	240
KG8563D	A	A	A	o	o	o	o	o	A	A	A	A	A	A	A	o	o	o	A	A	o	o	o	o	o	o	A				
KG8144D		o	A					o		A	A		A			o	A	o	o	o	o	A	o	o	o	o	A		o		
KG8244D										o			A						o	o		A		o	o	o	o	o	o	o	
KG8444D																			o					o		o	o	o	o	o	0

NOTE: “o”-marked packages are fully guaranteed by SEC ASIC, and “A”-marked are available but not guaranteed since they are not completed passed bonding rule test.

DEDICATED CORNER V_{DD}/V_{SS} PADS

The corner pads shown in the following figure are well-suited for double bonding purposes. Pad 1 and pad 2 can be bonded to the same package pin. Unlike normal I/O pads, these pads can only be used for V_{DD}/V_{SS} listed in Table 1-17. Use of Corner Pads.

Figure 1-19. V_{DD}/V_{SS} Corner Pads



NOTES:

1. There is no dedicated corner VSSI pad. Therefore, internal V_{SS} must be supplied using I/O pad type cell.
2. Corner pads are used to reduce the power/ground noise when some parts of the design cause noise problem especially while the other parts keep quiet.

Table 1-17. Use of Corner Pads

1	VSSO
2	VSSO
3	VSSI
4	VSSI
5	VDDI
6	VDDI
7	VDD5O
8	VDD5O
9	VDD3O
10	VDD3O
11	VSSI
12	VSSI
13	VDDI
14	VDDI
15	VSSO
16	VSSO

EXTERNAL DESIGN INTERFACE CONSIDERATIONS

This section briefly describes what you should consider when chips interface with outside world especially for a noise protection.

Input Buffer

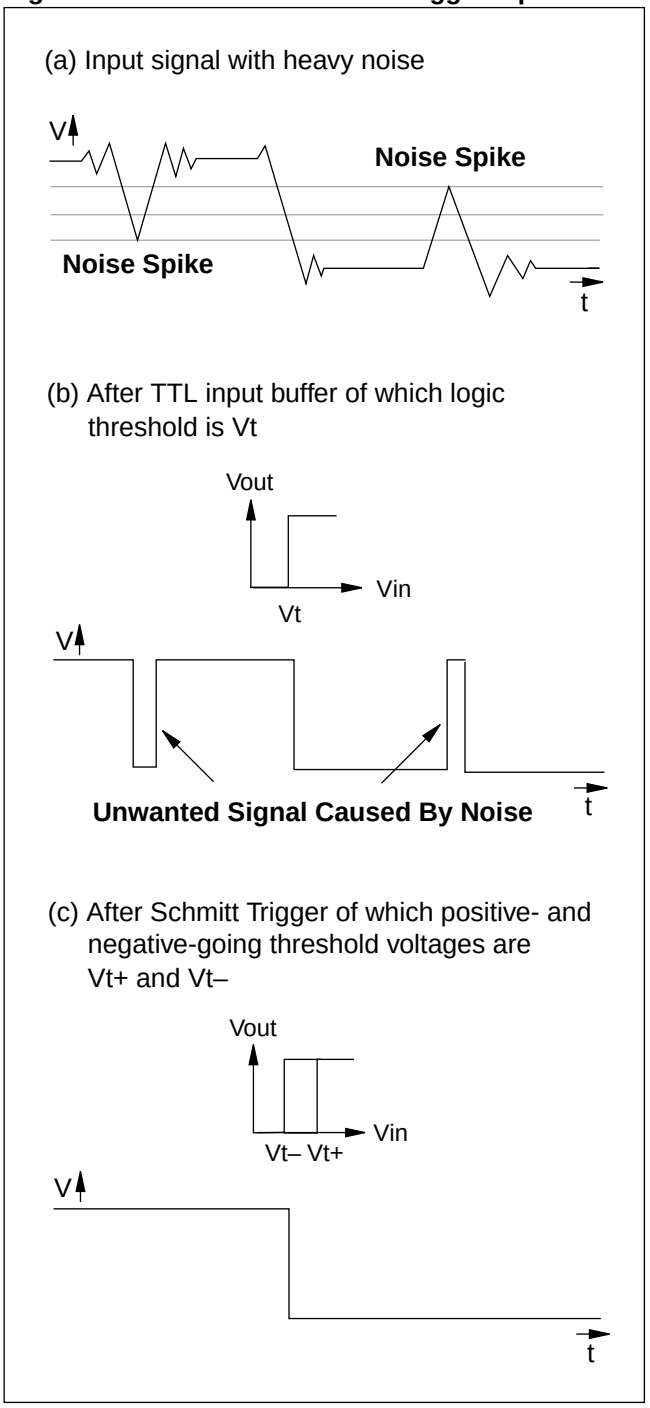
Usually there are three types of input receivers in ASIC libraries; TTL input buffer, CMOS input buffer, and various Schmitt trigger input buffers.

TTL input buffer has relatively poor noise characteristics because of its shifted logic threshold voltage. CMOS input buffer is better than TTL against a noise because the logic threshold voltage is near 2.5volt. If an input signal has relatively large noise spikes, it could cause an unwanted input signal.

When an input signal is very noisy, the noise can be filtered by using a Schmitt trigger input buffer. As shown in Figure 1-20. Effect of Schmitt Trigger Input Buffer, Schmitt trigger input buffers have two different input thresholds for positive- and negative-going signals. This hysteresis between positive- and negative-going voltage signals can filter a noisy signal to a wanted one.

According to applications, the most suitable one can be chosen among the various Schmitt trigger input buffers having different levels of threshold voltage.

Figure 1-20. Effect of Schmitt Trigger Input Buffer



Output Pad Cell

As incoming signals to a chip have a noise, the noise can also be induced by the operation of the chip itself. There are several sources of a noise, but the greatest singular source of a noise is the switching of an output with high capacitive load.

Figure 1-21. Simple Model of Output Pad Cell

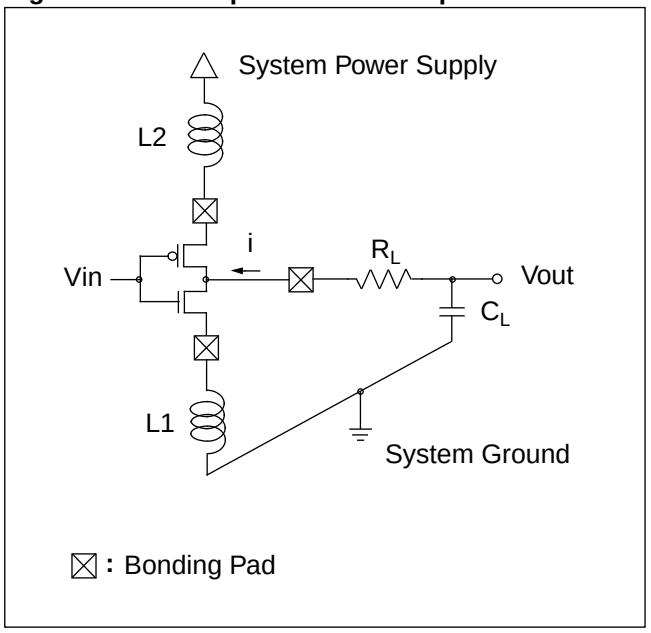


Figure 1-21. Simple Model of Output Pad Cell shows the simple model of an output driver considering the external interface. L1 and L2 are parasitic inductances of the package and C_L is an output load. Vout will fall as Vin rises and the current i flows through n-transistor discharging the loaded charge ($V_{DD} \times C_L$).

The details of this operations are described in Figure 1-22. Ground Bounce Phenomenon.

The important phenomenon which can be observed in this figure is that the voltage level Vn shifts relative to the system ground. Vn is the ground of the chip.

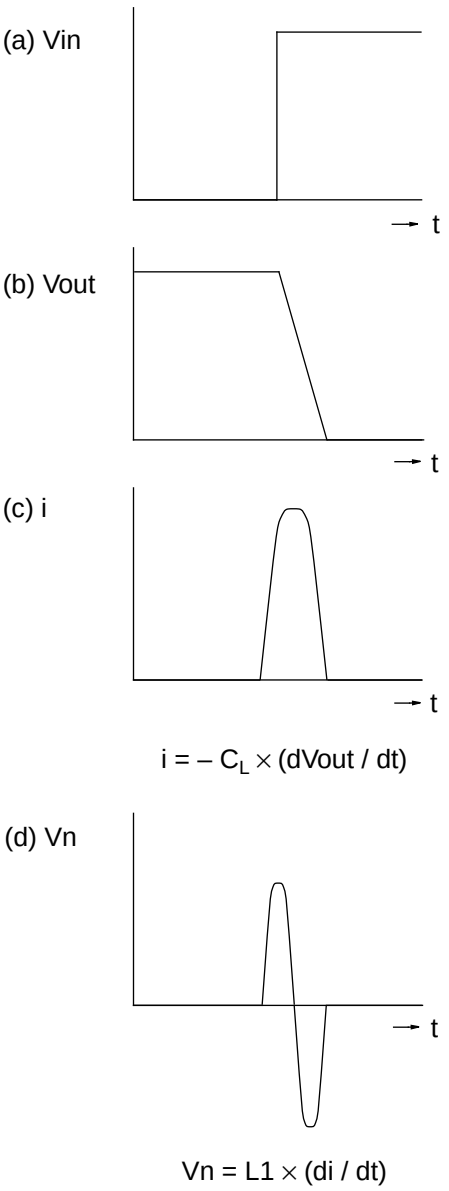
This phenomenon is called as a “ground bounce” that is the chip reference shift caused by the external inductance and the transient current flow to the ground.

The amount of voltage level shifted by the ground bounce is

$$Vn = -L \times (di / dt)$$

When the output driver makes a low-to-high transition, the similar noise problem is generated on the power.

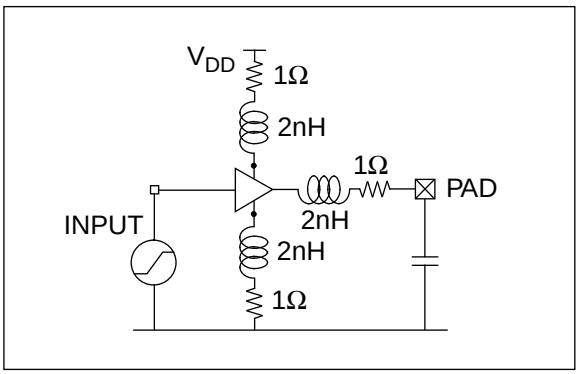
Figure 1-22. Ground Bounce Phenomenon



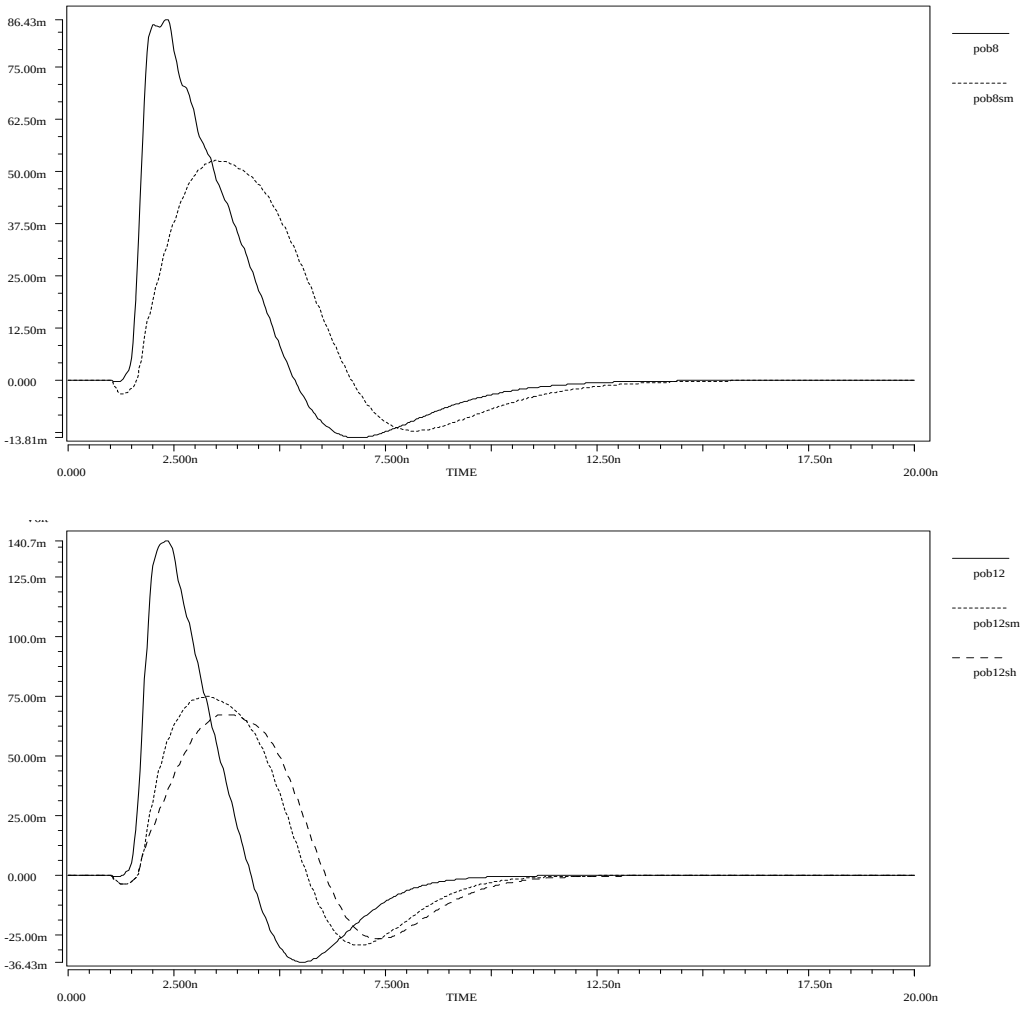
The following graphs show typical AC characteristics of non-slew and slew-rate output drives in KG80/KGM80. Using the slew-rate control, you can reduce the switching noise.

Figure 1-23. AC Characteristics of Non-Slew and Slew Rate Output Drives

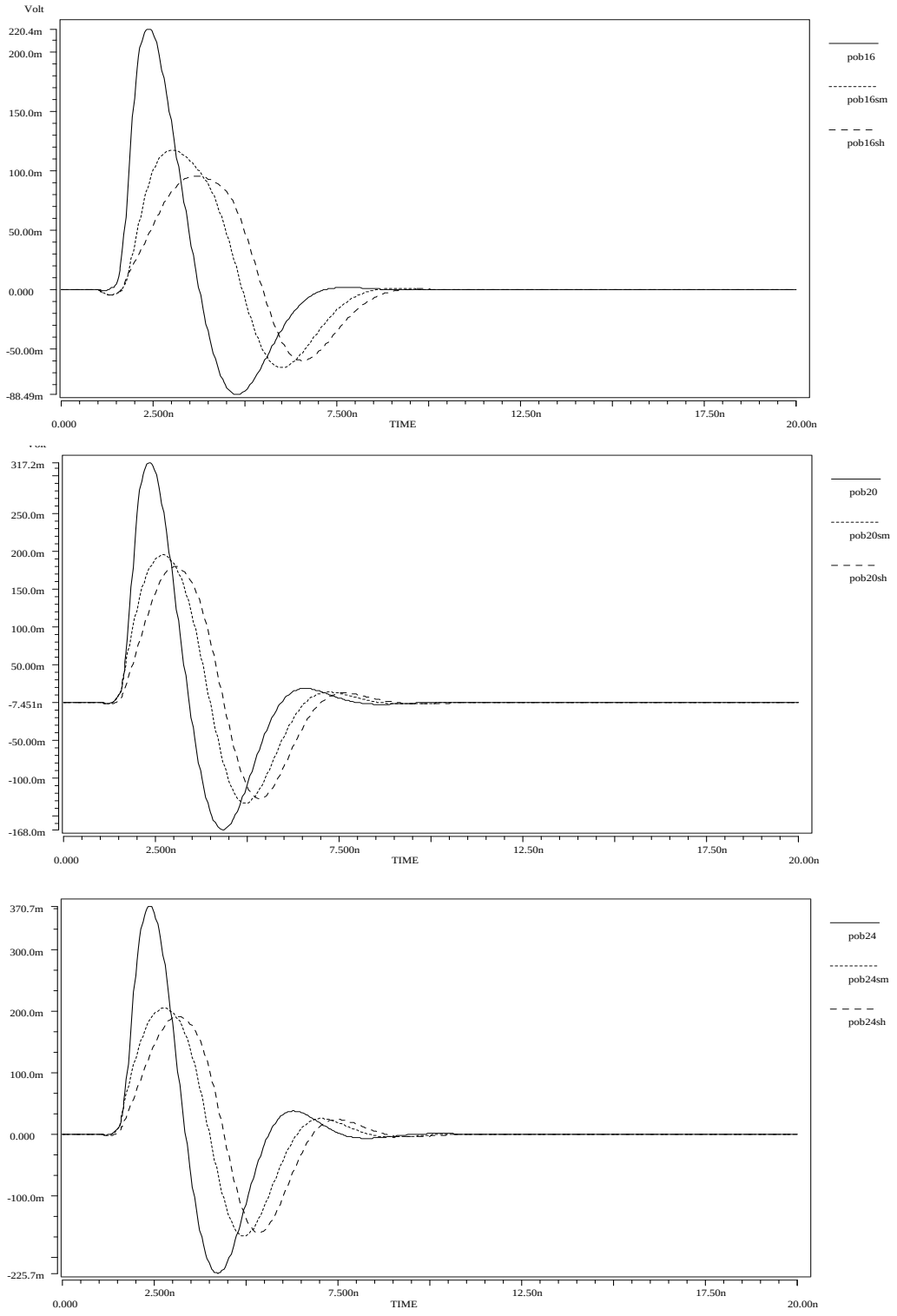
< Test Condition >



Ground Bouncing Voltage vs. Time



Ground Bouncing Voltage vs. Time



Simultaneous Switching Outputs (SSOs)

If several output drivers switch from high to low simultaneously, the ground bouncing level becomes quite large because the current flowing through the inductance L is the total sum of the transient current of each output driver. The amount of total current and the level of ground bounce are proportional to the number of SSOs.

This ground bounce can cause two types of problems, a noise margin reduction and a generation of noise spike on the output pad.

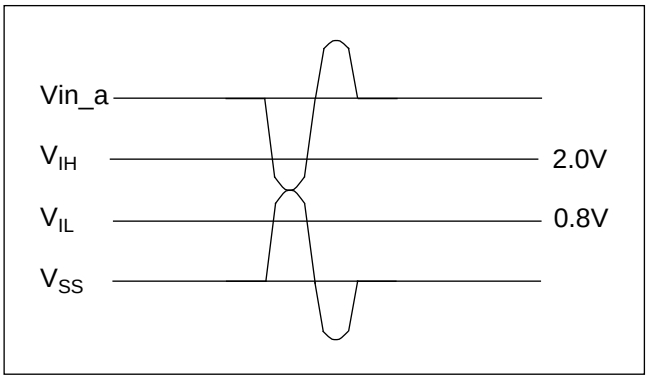
NOISE MARGIN REDUCTION

The ground bounce can cause a noise margin reduction when the same ground bus is used for both input buffers and output drivers as shown in Figure 1-25. The Figure of SSOs. The noise margin reduction can be explained using the circuit in the same figure.

As you can see, if outputs switch from high to low simultaneously, it results in a ground bounce or the rise of the chip ground level relative to system ground. The rise appears as the input voltage Vin_a is below V_{IH} causing false triggering of the input buffer. Vin is, in this case, not the same as Vin_a. Note that Vin is measured relative to the system ground, while Vin_a is measured relative to the local device ground.

This phenomenon is shown in Figure 1-24. Noise Margin Reduction due to SSOs. For a low-to-high transition, it is the low input levels (V_{IL}) that are affected.

Figure 1-24. Noise Margin Reduction due to SSOs

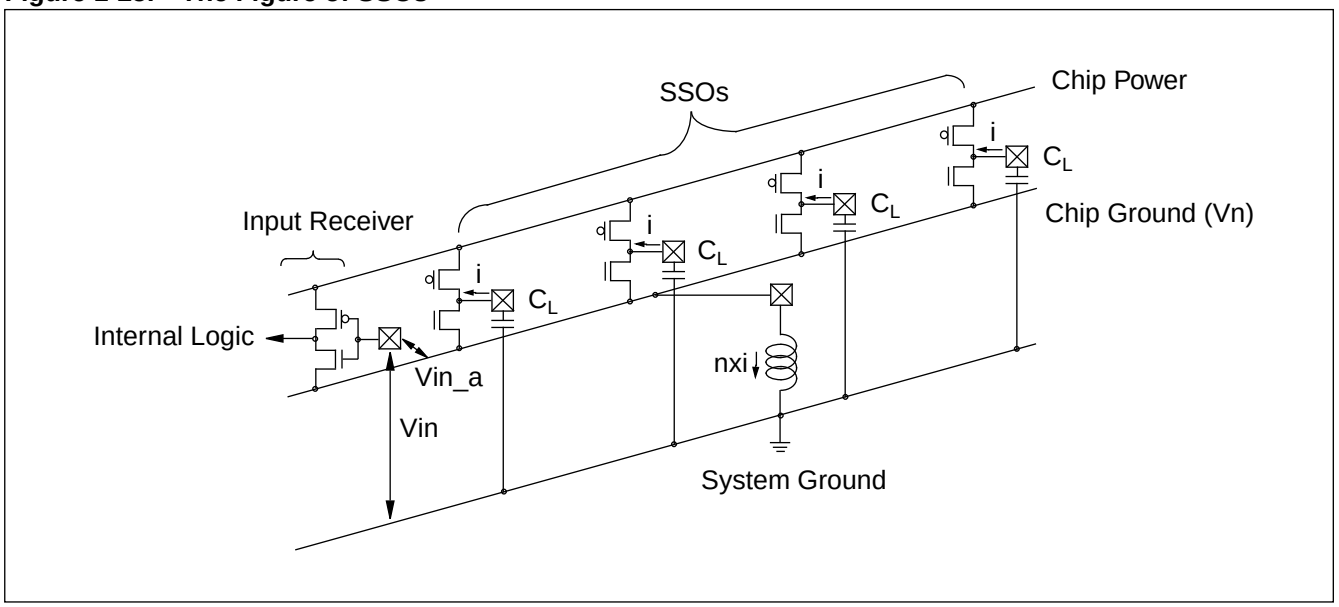


NOISE SPIKE GENERATION ON STABLE OUTPUT

If input and output power buses are separated, the problem of a noise margin reduction in the input buffer can be solved. However, ground bounce can cause another problem in spite of using separated power and ground bus.

The Figure 1-26. Noise Spike Induced by Ground Bounce shows a common octal driver application where ground bounce spikes will be observable on the one stable output. If the spike is considered as high by another chip, this ground bounce may upset that operation of interfacing device or cause system logic errors.

Figure 1-25. The Figure of SSOs



For example, suppose C_L = 100pF, V_{DD} = 3.3Volt, t_F = 5ns. From Figure 1-22. Ground Bounce Phenomenon, the maximum current flow occurs at time $0.5 \times t_F$. Then approximately,

$i = C_L \times (dv / dt) \cong C_L \times (\Delta V / \Delta t)$,
and

$i\ (max) = 100 \times 10^{-12} \times \{5 / (2.5 \times 10^{-9})\} = 200$ [mA].

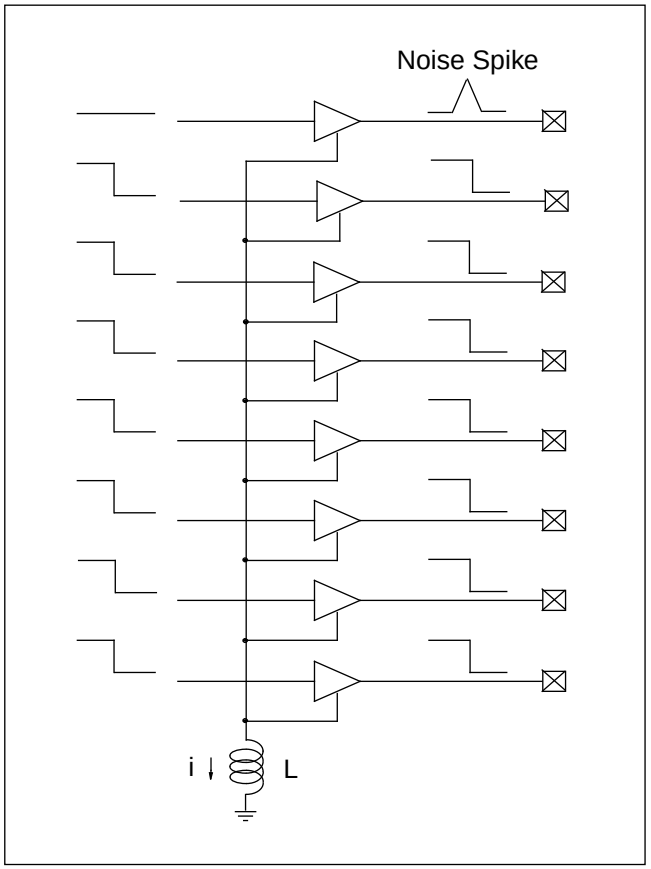
If the number of SSOs is 5, and L is 4nH,

$Vn = L \times (di / dt) \times N \cong L \times (\Delta i / \Delta t) \times N$ by approximation,

$Vn\ (max) = 4 \times 10^{-9} \times \{0.200 / (2.5 \times 10^{-9})\} \times 5 = 1.60$ [Volt].

From this calculation, 1.60V of noise spike is expected. This is about logic threshold voltage of TTL. This numerical estimate clearly shows that power bus noise control is one of the fundamental problems in a high-speed CMOS VLSI design. It is an important design consideration to prevent the noise from affecting the integrity of the logic operation of a chip.

Figure 1-26. Noise Spike Induced by Ground Bounce



How to Protect Ground Bounce?

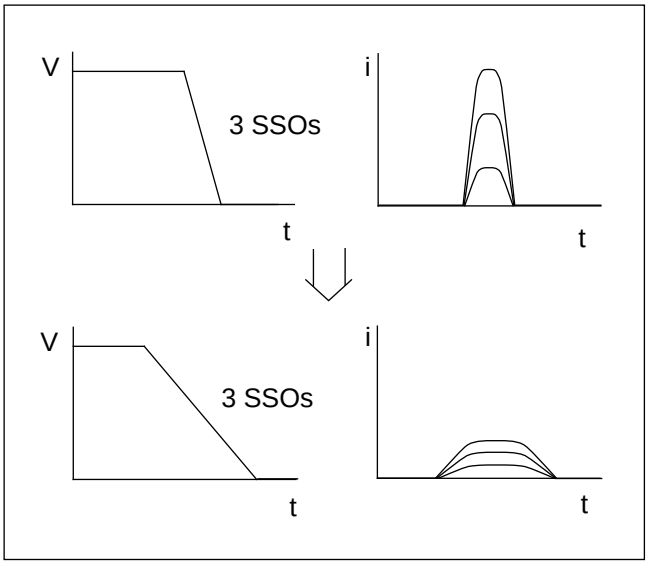
The fundamental solution to the ground bounce problem is to reduce the inductance of the package. However, in the boundary of a given packaging technology, the following guidelines can be used for reducing ground bounce:

(1) If possible, use separate power and ground buses for input buffers and output drivers.

(2) The number of ground and power pads should not be less than the required number of pads.

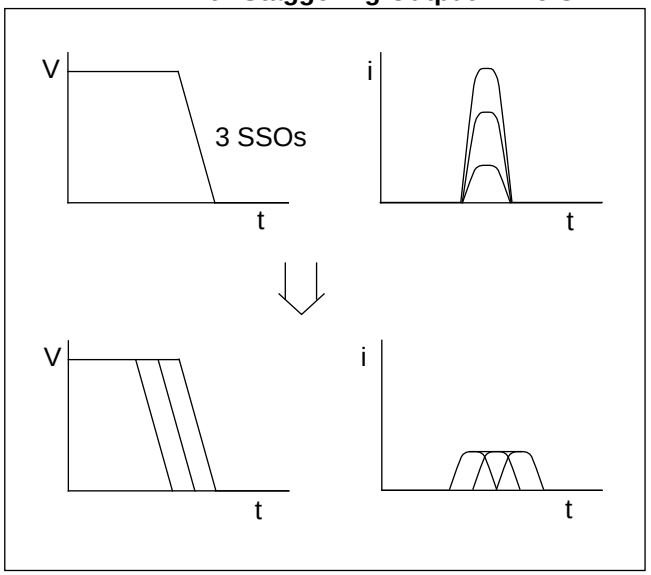
(3) If the design is not so much sensitive to speed, use slew rate control, i.e., increase switching time, to reduce the value of di / dt of an output driver. SEC supports two levels of slew rate controlled output buffers, SM and SH. You can see this effect in the following figure.

Figure 1-27. Effect on Reducing Peak Current with Slew-Rate Control



(4) If you cannot use a slew rate cell because of the speed requirement, you can stagger the output driver as shown in Figure 1-28. Effect on Reducing Peak Current with Staggering Output Drivers. This is not a general-purpose solution. It makes sense only when special relief in timing requirements exists from a system architecture.

Figure 1-28. Effect on Reducing Peak Current with Staggering Output Drivers



(5) High-drive outputs should be close to V_{SS} pins. SSOs should be placed particularly close to V_{SS} pins.

(6) SSOs should be appropriately placed in groups belonging to given V_{SS} pins.

(7) Noise-sensitive signals such as clock, asynchronous clear and preset should be located away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near V_{SS}, if one is available away from SSOs or high-drive outputs.

(8) Place SSOs on low inductance pins, such as those located on the inner rows or middle positions of PGAs.

(9) Clock, preset and clear inputs must not be placed on the corners of a package, especially when the array is packaged in DIP.

(10) Output signals to be used as clock, preset or clear for other devices must be kept away from SSOs and close to V_{SS} pin.

These guidelines assist you in choosing the best package(s) for the application. Furthermore, the recommendations about pinout results in reliable and predictable devices that minimizes harmful DC and AC effects on the system.

CRYSTAL OSCILLATOR CONSIDERATIONS

Overview

KG80/KGM80 contains a circuit commonly referred to as an “on-chip oscillator.” The on-chip circuit itself is not an oscillator but an amplifier which is suitable for being used as the amplifier part of a feedback oscillator. With proper selection of off-chip components, this oscillator circuit performs better than any other types of clock oscillators.

It is very important to select suitable off-chip components to work with the on-chip oscillator circuitry. It should be noted, however, that SEC cannot assume the responsibility of writing specifications for the off-chip components of the complete oscillator circuit, nor of guaranteeing the performance of the finished design in production, anymore than a transistor manufacturer, whose data sheets show a number of suggested amplifier circuits, can assume responsibility for the operation, in production, of any of them.

We are often asked why we don’t publish a list of required crystal or ceramic resonator specifications, and recommend values for the other off-chip components. This has been done in the past, but sometimes with consequences that were not intended.

Suppose we suggest a maximum crystal resistance of 30 ohms for some given frequency. Then your crystal supplier tells you the 30 ohm crystals are going to cost twice as much as 50 ohm crystals. Fearing that SEC will not “guarantee operation” with 50 ohm crystals, you order the expensive ones.

In fact, SEC guarantees only what is embodied within an SEC product. Besides, there is no reason why 50 ohm crystals couldn’t be used, if the other off-chip components are suitably adjusted.

Should we recommend values for the other off-chip components? Should we do for 50 ohm crystals or 30 ohm crystals? With respect to what should we optimize their selection? Should we minimize start-up time or maximize frequency stability?

In many applications, neither start-up time nor frequency stability is particularly critical, and our “recommendations” are only restricting your system to unnecessary tolerances. It all depends on the application.

Oscillator Design Considerations

ASIC designers have a number of options for clocking the system. The main decision is whether to use the “on-chip” oscillator or an external oscillator. If the choice is to use the on-chip oscillator, what kinds of external components are to use an external oscillator, what type of oscillator would it be?

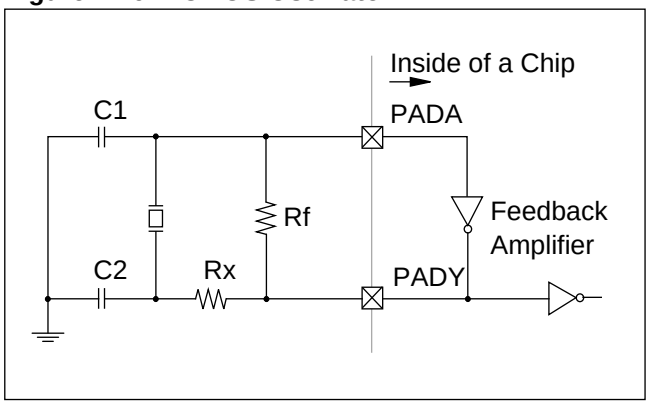
The decisions have to be based on both economic and technical requirements. In this section we will discuss some of the factors that should be considered.

ON-CHIP OSCILLATOR

In most cases, the on-chip amplifier with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components that commonly used for CMOS gate oscillator are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistor Rf and Rx as shown in the figure below.

Figure 1-29. CMOS Oscillator



CRYSTAL SPECIFICATIONS

Specifications for an appropriate crystal are not very critical, unless the frequency is. Any fundamental-mode crystal of medium or better quality can be used.

We are often asked what maximum crystal resistance should be specified. The best answer to that question is the lower the better, but use what is available.

The crystal resistance will have some effect on start-up time and steady-state amplitude, but not so much that it can’t be compensated for by appropriate selection of the capacitances, C1 and C2.

Similar questions are asked about specifications of load capacitance and shunt capacitance. The best advice we can give is to understand what these parameters mean and how they affect the operation of the circuit (that being the purpose of this application note), and then to decide for yourself if such specifications are meaningful in your frequency tolerances are tighter than about 0.1%.

Part of the problem is that crystal manufacturers are accustomed to talking “ppm” tolerances with radio engineers and simply won’t take your order until you’ve filled out their list of frequency tolerance requirements, both for yourself and to the crystal manufacturer. Don’t pay for 0.003% crystals if your actual frequency tolerance is 1%.

OSCILLATION FREQUENCY

The oscillation frequency is determined 99.5% by the crystal and up to about 0.5% by the circuit external to the crystal.

The on-chip amplifier has little effect on the frequency, which is as it should be, since the amplifier parameterizes temperature and process dependent.

The influence of the on-chip amplifier on the frequency is by means of its input and output (pin-to-ground) capacitances, which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance, which parallels the crystal. The input and pin-to-pin capacitances are about 7 pF each.

Internal phase deviations capacitance of 25 to 30 pF. These deviations from the ideal have less effect in the positive reactance oscillator (with the inverting amplifier) than in a comparable series resonant oscillator (with the non-inverting amplifier) for two reasons: first, the effect of the output capacitor; second, the positive reactance oscillator is less sensitive, frequency-wise, to such phase errors.

C1 / C2 SELECTION

Optimal values for the capacitors C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and also on application-specific requirements on start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability, because of various reset and initialization requirements.

Less commonly, accuracy of the oscillator frequency is also critical, for example, when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 20pF. (But they don't have to be either.)

Increasing the value of these capacitances above some 40 or 50pF improves frequency stability. It also tends to increase the start-up time. These is a maximum value (several hundred pH, depending on the value of R1 of the quartz or ceramic resonator) above which the oscillator won't start up at all.

If the on-chip amplifier is a simple inverter, the user can select values for C1 and C2 between some 20 and 100pF, depending on whether start-up time or frequency stability is the more critical parameter in a specific application.

RF / RX SELECTION

A CMOS inverter might work better in this application since a large Rf (1mega-ohm) can be used to hold the inverter in its linear region.

Logic gates tend to have a fairly low output resistance, which testabilizes the oscillator. For that reason a resistor Rx (several k-ohm) is often added to the feedback network, as shown in Figure 1-29. CMOS Oscillator.

At higher frequencies a 20 or 30pF capacitor is sometimes used in the Rx position, to compensate for some of the internal propagation delay.

PIN CAPACITANCE

Internal pin-to-ground and pin-to-pin capacitances, and PADA and PADY have some effect on the oscillator. These capacitances are normally taken to be in the range of 5 to 10pF, but they are extremely difficult to evaluate. Any measurement of one such capacitance necessarily include effects from the others.

One advantage of the positive reactance oscillator is that the pin-to ground cap. is paralleled by an external bulk capacitance, so a precise determination of their value is unnecessary.

We would suggest that there is little justification for more precision than to assign them a value of 7pF (PADA-to-ground and PADA-to-PADY). This value is probably not in error by more than 3 or 4pF.

The PADY-to-ground cap. is not entirely a "pin capacitance", but more like an "equivalent output capacitance" of some 25 to 30pF, having to include the effect of internal phase delays. This value varies to some extent with temperature, process, and frequency.

PLACEMENT OF COMPONENTS

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and V_{SS} pins.

If possible, use dedicated V_{SS} and V_{DD} pin for only crystal feedback amplifier.

Troubleshooting Oscillator Problems

The first thing to consider in case of difficulty is that there may be significant differences in stray caps between the test jig and the actual application, particularly if the actual application is on a multi-layer board.

Noise glitches, that are not present in the test jig but are in the application board, are another possibility. Capacitive coupling between the oscillator circuitry and other signal has already been mentioned as a source of miscounts in the internal clocking circuitry. Inductive coupling is also doubtful, if there is strong current nearby. These problems are a function of the PCB layout.

Surrounding oscillator components with “quit” traces (for example, VCC and ground) will alleviate capacitive coupling to signals having fast transition time. To minimize inductive coupling, the PCB layout should minimize the areas of the loops formed by oscillator components.

The loops demanding to be checked are as follows:

PADA through the resonator to PADY;
PADA through C1 to the V_{SS} pin;
PADY through C2 to the V_{SS} pin.

It is not unusual to find that the ground ends of C1 and C2 eventually connect up to the V_{SS} pin only after looping around the farthest ends of the board. Not good.

Finally, it should not be overlooked that software problems sometimes imitate the symptoms of a slow-starting oscillator or incorrect frequency. Never underestimate the perversity of a software problem.

Electrical Characteristics 2

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DC Electrical Characteristics 2-1
Input Buffer DC Curves 2-3
Output Drive Capabilities 2-5

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 5%, T_A = 0 to 70°C

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage				
	TTL interface		2.0		V
	TTL schmitt trigger			2.1	
	CMOS interface		$0.7V_{DD}$		
	CMOS schmitt trigger			4.0	
V_{IL}	Low level input voltage				
	TTL interface			0.8	V
	TTL schmitt trigger		0.8		
	CMOS interface			$0.3V_{DD}$	
	CMOS schmitt trigger		1.0		
I_{IH}	High level input current				
	Input buffer	$V_{IN} = V_{DD}$	–10	10	µA
	Input buffer with pull-down		10	200	
I_{IL}	Low level input current				
	Input buffer	$V_{IN} = V_{SS}$	–10	10	µA
	Input buffer with pull-up		–200	–10	
V_{OH}	High level output voltage				
	Type B1 to B24[Note1]	I_{OH} = –1µA	V_{DD} – 0.05		V
	Type B1	I_{OH} = –1mA	2.4		
	Type B2	I_{OH} = –2mA			
	Type B4	I_{OH} = –4mA			
	Type B8	I_{OH} = –8mA			
	Type B12	I_{OH} = –12mA			
	Type B16	I_{OH} = –16mA			
	Type B20	I_{OH} = –20mA			
	Type B24	I_{OH} = –24mA			
V_{OL}	Low level output voltage				
	Type B1 to B24	I_{OL} = 1µA		0.05	V
	Type B1	I_{OL} = 1mA		0.4	
	Type B2	I_{OL} = 2mA			
	Type B4	I_{OL} = 4mA			
	Type B8	I_{OL} = 8mA			
	Type B12	I_{OL} = 12mA			
	Type B16	I_{OL} = 16mA			
	Type B20	I_{OL} = 20mA			
	Type B24	I_{OL} = 24mA			
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	–10	10	µA
I_{DD}	Quiescent supply current	$V_{IN} = V_{SS}$ or V_{DD}		100[Note2]	µA

NOTES:

1. Type B1 means 1mA output driver cells, and Type B24 means 24mA output driver cells.
2. This value depends on the customer design.

V_{DD} = 3.3V ± 10%, T_A = 0 to 70°C

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage				V
	CMOS interface		$0.7V_{DD}$		
	CMOS schmitt trigger			2.1	
V_{IL}	Low level input voltage				V
	CMOS interface			$0.3V_{DD}$	
	CMOS schmitt trigger		0.8		
I_{IH}	High level input current				µA
	Input buffer	$V_{IN} = V_{DD}$	–10	10	
	Input buffer with pull-down		10	200	
I_{IL}	Low level input current				µA
	Input buffer	$V_{IN} = V_{SS}$	–10	10	
	Input buffer with pull-up		–200	–10	
V_{OH}	High level output voltage				V
	Type B1 to B16	I_{OH} = –1µA	V_{DD} – 0.05		
	Type B1	I_{OH} = –0.5mA	2.4		
	Type B2	I_{OH} = –1mA			
	Type B4	I_{OH} = –2mA			
	Type B6	I_{OH} = –3mA			
	Type B8	I_{OH} = –4mA			
	Type B10	I_{OH} = –5mA			
	Type B12	I_{OH} = –6mA			
	Type B16	I_{OH} = –8mA			
V_{OL}	Low level output voltage				V
	Type B1 to B16	I_{OL} = 1µA		0.05	
	Type B1	I_{OL} = 1mA		0.4	
	Type B2	I_{OL} = 2mA			
	Type B4	I_{OL} = 4mA			
	Type B6	I_{OL} = 6mA			
	Type B8	I_{OL} = 8mA			
	Type B10	I_{OL} = 10mA			
	Type B12	I_{OL} = 12mA			
	Type B16	I_{OL} = 16mA			

Absolute Maximum Ratings

Symbol	Parameter	Ratingtd	Unit
V_{DD}	DC supply voltage	–0.3 to 7	V
V_{IN}	DC input voltage	–0.3 to V_{DD} + 0.3	
I_{IN}	DC input current	±10	mA
T_{STG}	Storage temperature	–40 to 125	°C

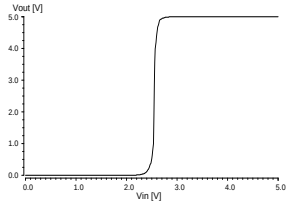
Recommended Operating Conditions

Symbol	Parameter		Rating	Unit
V_{DD}	DC supply voltage	5V	4.75 to 5.25	V
		3.3V	3.0 to 3.6	
T_A	Commercial temperature		0 to 70	°C
	Industrial temperature		–40 to 85	

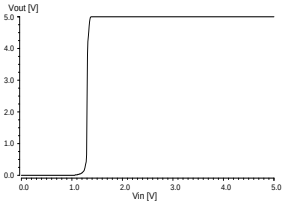
INPUT BUFFER DC CURVES

Input Buffer Transfer Curves

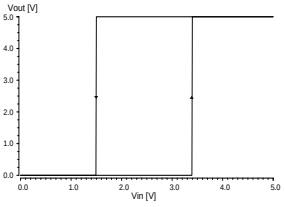
V_{DD} = 5V, T_A = 25°C, Typical Process



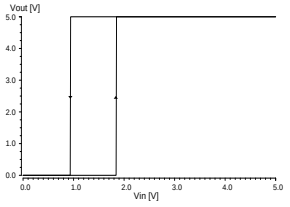
CMOS



TTL

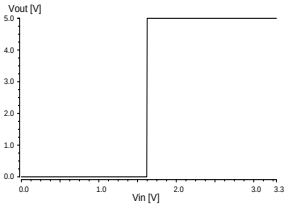


CMOS Schmitt Trigger

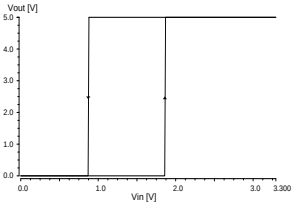


TTL Schmitt Trigger

V_{DD} = 3.3V, T_A = 25°C, Typical Process



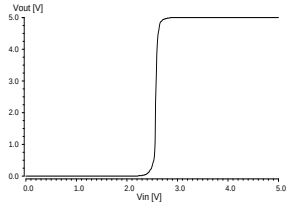
CMOS



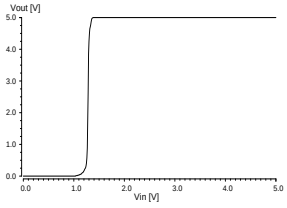
CMOS Schmitt Trigger

Input Clock Drivers Transfer Curves

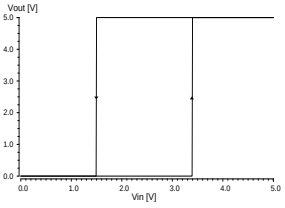
V_{DD} = 5V, T_A = 25°C, Typical Process



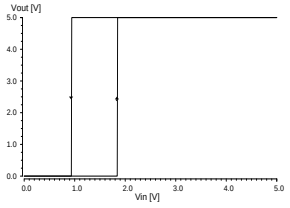
CMOS



TTL

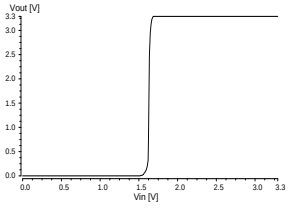


CMOS Schmitt Trigger

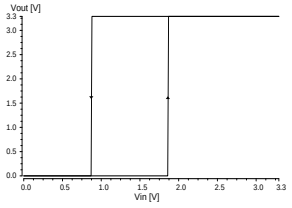


TTL Schmitt Trigger

V_{DD} = 3.3V, T_A = 25°C, Typical Process



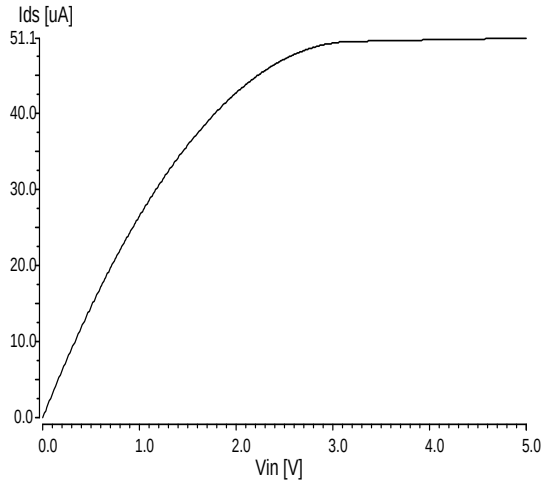
CMOS



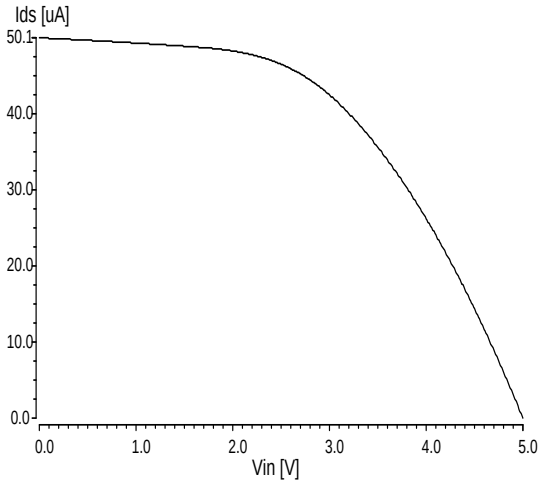
CMOS Schmitt Trigger

Input Buffer Pull-Down/Pull-Up Characteristics

V_{DD} = 5V, T_A = 25°C, Typical Process

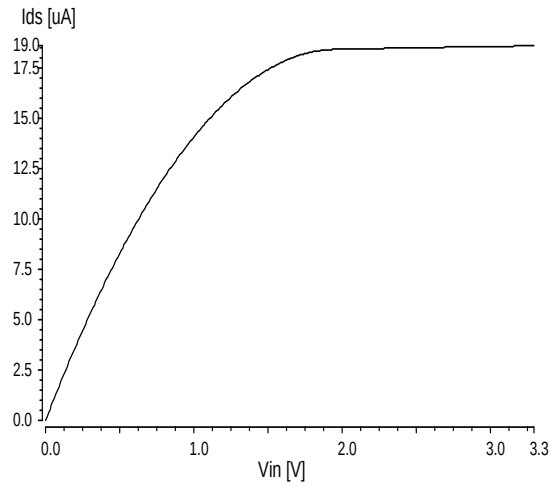


Pull-Down

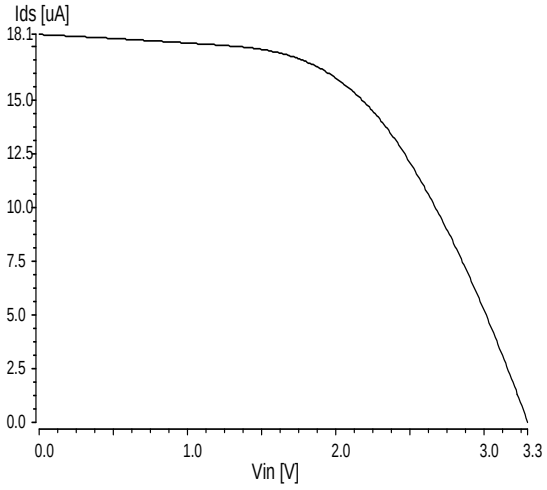


Pull-Up

V_{DD} = 3.3V, T_A = 25°C, Typical Process



Pull-Down

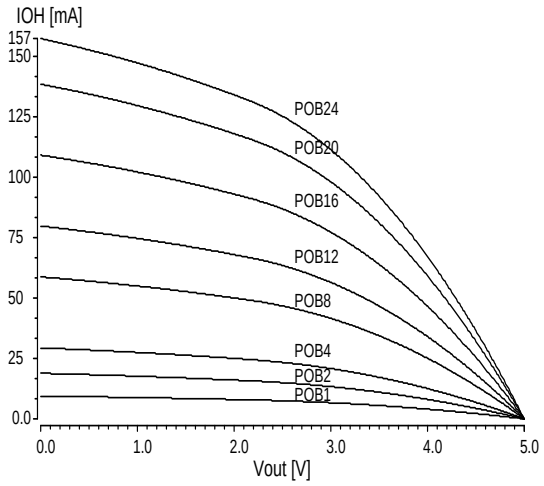


Pull-Up

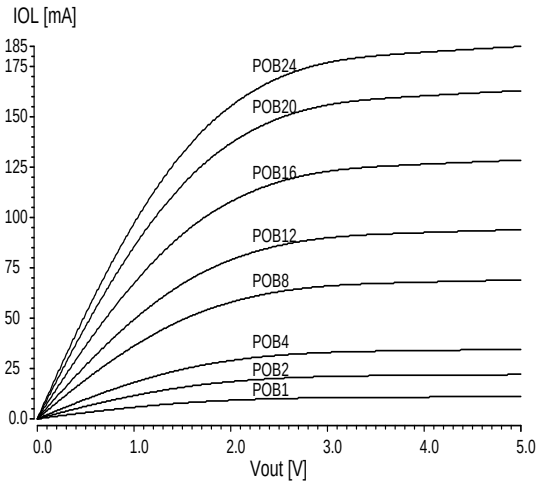
OUTPUT DRIVE CAPABILITIES

IV Characteristics

V_{DD} = 5V, T_A = 25°C, Typical Process



P-TR Characteristics



N-TR Characteristics

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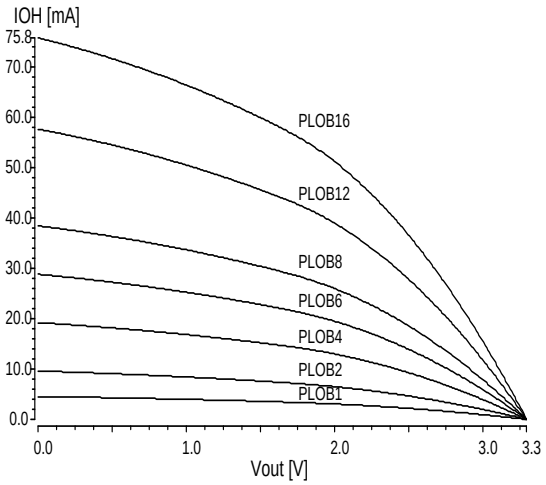
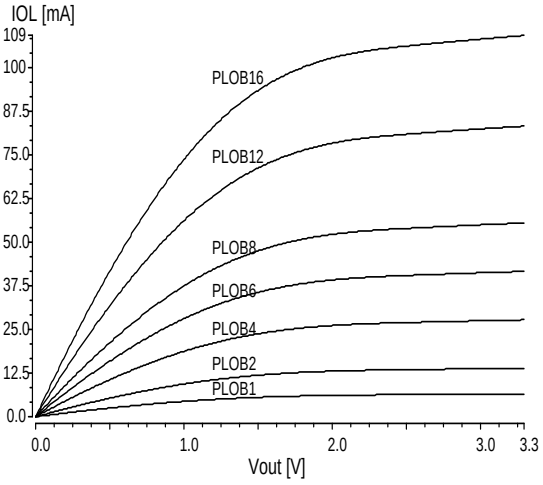


P-TR Characteristics



N-TR Characteristics

Internal Macrocells 3

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OVERVIEW

The third chapter contains data sheets of logic cells, flip-flops, latches, bus holder, internal clock drivers, decoders, adders and multiplexers.

The electrical characteristics of each cell follows its basic cell data.

Summary tables in the following pages list the whole KG80/KGM80 internal macrocells by the type and show their reference page numbers for your convenience. Moreover, you can find the more detailed description tables on the leading pages of each category.

SUMMARY TABLES

Logic Cells

Cell Type	Cell Name	Page
AND Cell	AD2/AD2D2	3-11
	AD3/AD3D3	3-13
	AD4/AD4D2	3-16
	AD5/AD5D2	3-19
NAND Cell	ND2/ND2D2	3-22
	ND3/ND3D2	3-24
	ND4/ND4D2	3-27
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	ND6/ND6D2	3-33
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NOR Cell	NR2/NR2D2	3-43
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	NR4/NR4D2	3-48
	NR5/NR5D2	3-51
	NR6/NR6D2	3-54
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OR Cell	OR2/OR2D2	3-64
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	OR4/OR4D2	3-69
	OR5/OR5D2	3-72
Exclusive-NOR Cell	XN2/XN2D2	3-76
	XN3/XN3D3	3-78
Exclusive-OR Cell	XO2/XO2D2	3-81
	XO3/XO3D3	3-83
Combinational Cell of AND and NOR	AO21/AO21D2	3-86
	AO211/AO211D2	3-89
	AO22/AO22D2	3-92
	AO22A/AO22D2A	3-95
	AO222/AO222D2	3-98
	AO222A/AO222D2A	3-103
	AO33/AO33D2	3-106
	AO333/AO333D2	3-111

Cell Type	Cell Name	Page
Combinational Cell of OR and NAND	OA21/OA21D2	3-116
	OA211/OA211D2	3-119
	OA22/OA22D2	3-122
	OA22A/OA22D2A	3-125
	OA2222/OA2222D2	3-128
Delay Cell	DL(1/2/3/4/5/10)D2/DL(1/2/3/4/5/10)D4	3-133
Inverter	IV/IVD2/IVD3/IVD4/IVD6/IVD8	3-139
	IVA/IVD2A/IVD3A/IVD4A	3-143
	IVCD(11/13)/IVCD(22/26)/IVCD44	3-146
Inverting Tri-State Buffer	IVT/IVTD2/IVTD4/IVTD8	3-150
	IVTN/IVTND2/IVTND4/IVTND8	3-154
Non-Inverting Buffer	NID/NID2/NID3/NID4/NID6/NID8	3-158
	NIT/NITD2/NITD4/NITD8	3-162
	NITN/NITND2/NITND4/NITND8	3-166

Flip-Flops

Cell Type	Cell Name	Page
D Flip-Flop	FD1/FD1D2	3-173
	FD1CS/FD1CSD2	3-176
	FD1S/FD1SD2	3-180
	FD1Q/FD1QD2	3-183
	FD1X2	3-185
	FD1X4	3-187
	YFD1/YFD1D2	3-190
D Flip-Flop with Reset	FD2/FD2D2	3-193
	FD2CS/FD2CSD2	3-196
	FD2S/FD2SD2	3-200
	FD2Q/FD2QD2	3-203
	FD2X2	3-205
	FD2X4	3-208
	YFD2/YFD2D2	3-211
D Flip-Flop with Reset, Tri-State Output	FD2T/FD2TD2	3-214
	FD2TCS/FD2TCSD2	3-217
	FD2TS/FD2TSD2	3-222

Cell Type	Cell Name	Page
D Flip-Flop with Set	FD3/FD3D2	3-226
	FD3CS/FD3CSD2	3-229
	FD3S/FD3SD2	3-233
	FD3Q/FD3QD2	3-236
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D Flip-Flop with Reset, Set	FD4/FD4D2	3-247
	FD4CS/FD4CSD2	3-251
	FD4S/FD4SD2	3-257
	FD4Q/FD4QD2	3-261
	FD4X2	3-264
	FD4X4	3-267
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D Flip-Flop with Negative Edge Trigger	FD5/FD5D2	3-275
	FD5S/FD5SD2	3-278
	FD5X4	3-281
	FD6/FD6D2	3-284
	FD6S/FD6SD2	3-287
	FD7/FD7D2	3-290
	FD7S/FD7SD2	3-293
	FD8/FD8D2	3-296
	FD8S/FD8SD2	3-300
D Flip-Flop with Synchronous Clear	FDS2/FDS2D2	3-304
	FDS2CS/FDS2CSD2	3-307
	FDS2S/FDS2SD2	3-311
	FDS3/FDS3D2	3-314
D Flip-Flop with CK Enable	FG1	3-317
	FG1X4	3-319
	FG2	3-324
	FG2X4	3-327

Cell Type	Cell Name	Page
JK Flip-Flop	FJ1/FJ1D2	3-332
	FJ1S/FJ1SD2	3-335
	FJ2/FJ2D2	3-338
	FJ2S/FJ2SD2	3-341
	FJ4/FJ4D2	3-345
	FJ4S/FJ4SD2	3-349
Toggle Flip-Flop	FT2/FT2D2	3-353
	FT3/FT3D2	3-356

Latches

Cell Type	Cell Name	Page
D Latch with Active High	LD1/LD1D2	3-361
	LD1S/LD1SD2	3-364
	LD1Q/LD1QD2	3-369
	LD1X4/LD1X4D2	3-372
	YLD1/YLD1D2	3-381
	LD1A	3-384
	LD1B	3-386
D Latch with Active High, Reset	LD2/LD2D2	3-389
	LD2Q/LD2QD2	3-394
	YLD2/YLD2D2	3-397
	LD3/LD3D2	3-402
	LD4/LD4D2	3-407
D Latch with Active Low	LD5/LD5D2	3-412
	LD5S/LD5SD2	3-415
	LD5X4/LD5X4D2	3-420
	LD6/LD6D2	3-429
	LD7/LD7D2	3-434
	LD8/LD8D2	3-439
D Latch with Synchronous Clear	LDS2	3-444
	LDS6	3-447
SR Latch	LS0/LS0D2	3-450
	LS1	3-453
	LS2	3-456

Bus Holder

Cell Type	Cell Name	Page
Bus Holder	BUSHOLDER	3-459

Internal Clock Drivers

Cell Type	Cell Name		Page
	KG80	KGM80	
Internal Clock Driver	CK(2/4/8/12)	CK(2/4/6/8)	3-460

Decoders

Cell Type	Cell Name	Page
Non-Inverting Decoder	DC4	3-464
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	DC8I	3-470

Adders

Cell Type	Cell Name	Page
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Multiplexers

Cell Type	Cell Name	Page
2 > 1 Non-Inverting Mux	MX2/MX2D3	3-487
	MX2X4	3-490
	YMX2/YMX2D2	3-495
2 > 1 Inverting Mux	MX2I/MX2ID2	3-498
	MX2IA/MX2ID2A	3-501
	MX2IX4	3-504
3 > 1 Inverting Mux	MX3I/MX3ID2	3-509
4 > 1 Non-Inverting Mux	MX4/MX4D2	3-512
	YMX4/YMX4D2	3-517
5 > 1 Non-Inverting Mux	MX5/MX5D2	3-522
8 > 1 Non-Inverting Mux	MX8/MX8D2	3-527
	YMX8/YMX8D2	3-533

Cell List

Cell Name	Function Description
AD2	2-Input AND
AD2D2	2-Input AND with 2X Drive
AD3	3-Input AND
AD3D3	3-Input AND with 3X Drive
AD4	4-Input AND
AD4D2	4-Input AND with 2X Drive
AD5	5-Input AND
AD5D2	5-Input AND with 2X Drive
ND2	2-Input NAND
ND2D2	2-Input NAND with 2X Drive
ND3	3-Input NAND
ND3D2	3-Input NAND with 2X Drive
ND4	4-Input NAND
ND4D2	4-Input NAND with 2X Drive
ND5	5-Input NAND
ND5D2	5-Input NAND with 2X Drive
ND6	6-Input NAND
ND6D2	6-Input NAND with 2X Drive
ND8	8-Input NAND
ND8D2	8-Input NAND with 2X Drive
NR2	2-Input NOR
NR2D2	2-Input NOR with 2X Drive
NR3	3-Input NOR
NR3D2	3-Input NOR with 2X Drive
NR4	4-Input NOR
NR4D2	4-Input NOR with 2X Drive
NR5	5-Input NOR
NR5D2	5-Input NOR with 2X Drive
NR6	6-Input NOR
NR6D2	6-Input NOR with 2X Drive
NR8	8-Input NOR
NR8D2	8-Input NOR with 2X Drive
OR2	2-Input OR
OR2D2	2-Input OR with 2X Drive

Cell List (Continued)

Cell Name	Function Description
OR3	3-Input OR
OR3D3	3-Input OR with 3X Drive
OR4	4-Input OR
OR4D2	4-Input OR with 2X Drive
OR5	5-Input OR
OR5D2	5-Input OR with 2X Drive
XN2	2-Input Exclusive-NOR
XN2D2	2-Input Exclusive-NOR with 2X Drive
XN3	3-Input Exclusive-NOR
XN3D3	3-Input Exclusive-NOR with 3X Drive
XO2	2-Input Exclusive-OR
XO2D2	2-Input Exclusive-OR with 2X Drive
XO3	3-Input Exclusive-OR
XO3D3	3-Input Exclusive-OR with 3X Drive
AO21	2-AND into 2-NOR
AO21D2	2-AND into 2-NOR with 2X Drive
AO211	2-AND into 3-NOR
AO211D2	2-AND into 3-NOR with 2X Drive
AO22	Two 2-ANDs into 2-NOR
AO22D2	Two 2-ANDs into 2-NOR with 2X Drive
AO22A	2-AND and 2-NOR into 2-NOR
AO22D2A	2-AND and 2-NOR into 2-NOR with 2X Drive
AO222	Three 2-ANDs into 3-NOR
AO222D2	Three 2-ANDs into 3-NOR with 2X Drive
AO222A	Inverting 2-of-3 Majority
AO222D2A	Inverting 2-of-3 Majority with 2X Drive
AO33	Two 3-ANDs into 2-NOR
AO33D2	Two 3-ANDs into 2-NOR with 2X Drive
AO333	Three 3-ANDs into 3-NOR
AO333D2	Three 3-ANDs into 3-NOR with 2X Drive
OA21	2-OR into 2-NAND
OA21D2	2-OR into 2-NAND with 2X Drive
OA211	2-OR into 3-NAND
OA211D2	2-OR into 3-NAND with 2X Drive

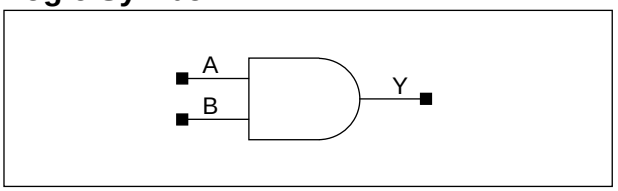
Cell List (Continued)

Cell Name	Function Description
OA22	Two 2-ORs into 2-NAND
OA22D2	Two 2-ORs into 2-NAND with 2X Drive
OA22A	2-OR and 2-NAND into 2-NAND
OA22D2A	2-OR and 2-NAND into 2-NAND with 2X Drive
OA2222	Four 2-ORs into 4-NAND
OA2222D2	Four 2-ORs into 4-NAND with 2X Drive
DL1D2	1ns Delay Cell with 2X Drive
DL1D4	1ns Delay Cell with 4X Drive
DL2D2	2ns Delay Cell with 2X Drive
DL2D4	2ns Delay Cell with 4X Drive
DL3D2	3ns Delay Cell with 2X Drive
DL3D4	3ns Delay Cell with 4X Drive
DL4D2	4ns Delay Cell with 2X Drive
DL4D4	4ns Delay Cell with 4X Drive
DL5D2	5ns Delay Cell with 2X Drive
DL5D4	5ns Delay Cell with 4X Drive
DL10D2	10ns Delay Cell with 2X Drive
DL10D4	10ns Delay Cell with 4X Drive
IV	Inverter
IVD2	Inverter with 2X Drive
IVD3	Inverter with 3X Drive
IVD4	Inverter with 4X Drive
IVD6	Inverter with 6X Drive
IVD8	Inverter with 8X Drive
IVA	Inverter with 2X P-Transistor, 1X N-Transistor
IVD2A	Inverter with 4X P-Transistor, 2X N-Transistor
IVD3A	Inverter with 6X P-Transistor, 3X N-Transistor
IVD4A	Inverter with 8X P-Transistor, 4X N-Transistor
IVCD11	1X Inverter into 1X Inverter
IVCD13	1X Inverter into 3X Inverter
IVCD22	2X Inverter into 2X Inverter
IVCD26	2X Inverter into 6X Inverter
IVCD44	4X Inverter into 4X Inverter
IVT	Inverting Tri-State Buffer with Enable High

Cell List (Continued)

Cell Name	Function Description
IVTD2	Inverting Tri-State Buffer with Enable High, 2X Drive
IVTD4	Inverting Tri-State Buffer with Enable High, 4X Drive
IVTD8	Inverting Tri-State Buffer with Enable High, 8X Drive
IVTN	Inverting Tri-State Buffer with Enable Low
IVTND2	Inverting Tri-State Buffer with Enable Low, 2X Drive
IVTND4	Inverting Tri-State Buffer with Enable Low, 4X Drive
IVTND8	Inverting Tri-State Buffer with Enable Low, 8X Drive
NID	Non-Inverting Buffer
NID2	Non-Inverting Buffer with 2X Drive
NID3	Non-Inverting Buffer with 3X Drive
NID4	Non-Inverting Buffer with 4X Drive
NID6	Non-Inverting Buffer with 6X Drive
NID8	Non-Inverting Buffer with 8X Drive
NIT	Non-Inverting Tri-State Buffer with Enable High
NITD2	Non-Inverting Tri-State Buffer with Enable High, 2X Drive
NITD4	Non-Inverting Tri-State Buffer with Enable High, 4X Drive
NITD8	Non-Inverting Tri-State Buffer with Enable High, 8X Drive
NITN	Non-Inverting Tri-State Buffer with Enable Low
NITND2	Non-Inverting Tri-State Buffer with Enable Low, 2X Drive
NITND4	Non-Inverting Tri-State Buffer with Enable Low, 4X Drive
NITND8	Non-Inverting Tri-State Buffer with Enable Low, 8X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)				Gate Count	
KG80					
AD2		*AD2D2*		*AD2*	*AD2D2*
A	B	A	B		
0.9	0.8	0.9	0.8	2.0	2.0
KGM80					
AD2		*AD2D2*		*AD2*	*AD2D2*
A	B	A	B		
1.0	1.0	1.0	1.0	2.0	2.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.19 + 0.043*SL	0.19 + 0.041*SL	0.19 + 0.042*SL
	t_{PHL}	0.27	0.21 + 0.028*SL	0.22 + 0.025*SL	0.23 + 0.023*SL
	t_R	0.28	0.10 + 0.086*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.16	0.09 + 0.037*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
B to Y	t_{PLH}	0.27	0.18 + 0.043*SL	0.18 + 0.041*SL	0.18 + 0.042*SL
	t_{PHL}	0.30	0.24 + 0.030*SL	0.26 + 0.025*SL	0.27 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.038*SL	0.09 + 0.039*SL	0.08 + 0.041*SL

KG80 AD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.20 + 0.024*SL	0.21 + 0.021*SL	0.22 + 0.020*SL
	t_{PHL}	0.26	0.23 + 0.018*SL	0.24 + 0.014*SL	0.25 + 0.012*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.020*SL
B to Y	t_{PLH}	0.24	0.19 + 0.023*SL	0.20 + 0.021*SL	0.20 + 0.021*SL
	t_{PHL}	0.29	0.25 + 0.020*SL	0.26 + 0.015*SL	0.28 + 0.012*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.042*SL	0.08 + 0.044*SL
	t_F	0.14	0.09 + 0.021*SL	0.10 + 0.019*SL	0.09 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

AD2/AD2D2

2-Input AND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AD2

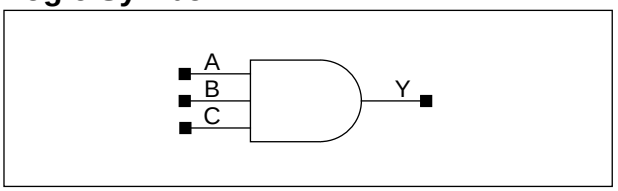
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.36	0.26 + 0.053*SL	0.27 + 0.050*SL	0.27 + 0.050*SL
	t_{PHL}	0.35	0.28 + 0.032*SL	0.30 + 0.025*SL	0.32 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.19	0.11 + 0.042*SL	0.11 + 0.041*SL	0.09 + 0.043*SL
B to Y	t_{PLH}	0.36	0.26 + 0.053*SL	0.26 + 0.050*SL	0.27 + 0.050*SL
	t_{PHL}	0.39	0.32 + 0.033*SL	0.35 + 0.025*SL	0.37 + 0.023*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.041*SL	0.12 + 0.041*SL	0.10 + 0.042*SL

KGM80 AD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.27 + 0.029*SL	0.28 + 0.026*SL	0.29 + 0.025*SL
	t_{PHL}	0.34	0.30 + 0.021*SL	0.31 + 0.015*SL	0.34 + 0.012*SL
	t_R	0.23	0.12 + 0.050*SL	0.12 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.15	0.10 + 0.024*SL	0.11 + 0.021*SL	0.11 + 0.020*SL
B to Y	t_{PLH}	0.32	0.26 + 0.030*SL	0.27 + 0.026*SL	0.28 + 0.025*SL
	t_{PHL}	0.38	0.33 + 0.022*SL	0.35 + 0.015*SL	0.38 + 0.013*SL
	t_R	0.23	0.13 + 0.050*SL	0.12 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.16	0.11 + 0.024*SL	0.12 + 0.020*SL	0.12 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
AD3			*AD3D3*			*AD3*	*AD3D3*
A	B	C	A	B	C		
1.0	0.9	0.9	0.8	0.8	0.9	2.0	3.0
KGM80							
AD3			*AD3D3*			*AD3*	*AD3D3*
A	B	C	A	B	C		
1.0	1.0	1.0	1.0	1.0	1.0	2.0	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.25 + 0.045*SL	0.26 + 0.042*SL	0.26 + 0.042*SL
	t_{PHL}	0.28	0.22 + 0.030*SL	0.23 + 0.025*SL	0.25 + 0.023*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.089*SL
	t_F	0.17	0.10 + 0.037*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
B to Y	t_{PLH}	0.34	0.25 + 0.045*SL	0.26 + 0.042*SL	0.26 + 0.041*SL
	t_{PHL}	0.31	0.25 + 0.032*SL	0.26 + 0.025*SL	0.28 + 0.023*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.088*SL	0.10 + 0.089*SL
	t_F	0.18	0.10 + 0.038*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
C to Y	t_{PLH}	0.34	0.25 + 0.045*SL	0.26 + 0.042*SL	0.27 + 0.041*SL
	t_{PHL}	0.34	0.28 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.089*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.040*SL

KG80 AD3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.38	0.35 + 0.018*SL	0.35 + 0.016*SL	0.36 + 0.015*SL
	t_{PHL}	0.31	0.28 + 0.014*SL	0.29 + 0.011*SL	0.30 + 0.010*SL
	t_R	0.22	0.16 + 0.026*SL	0.16 + 0.028*SL	0.15 + 0.028*SL
	t_F	0.15	0.12 + 0.015*SL	0.12 + 0.013*SL	0.12 + 0.013*SL
B to Y	t_{PLH}	0.38	0.34 + 0.018*SL	0.35 + 0.016*SL	0.36 + 0.015*SL
	t_{PHL}	0.34	0.31 + 0.015*SL	0.31 + 0.012*SL	0.33 + 0.010*SL
	t_R	0.21	0.16 + 0.026*SL	0.16 + 0.028*SL	0.15 + 0.029*SL
	t_F	0.16	0.13 + 0.015*SL	0.13 + 0.014*SL	0.14 + 0.013*SL
C to Y	t_{PLH}	0.38	0.34 + 0.018*SL	0.35 + 0.016*SL	0.36 + 0.015*SL
	t_{PHL}	0.36	0.33 + 0.016*SL	0.34 + 0.012*SL	0.36 + 0.010*SL
	t_R	0.22	0.16 + 0.027*SL	0.16 + 0.027*SL	0.15 + 0.029*SL
	t_F	0.17	0.14 + 0.015*SL	0.15 + 0.014*SL	0.15 + 0.013*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.46	0.34 + 0.057*SL	0.36 + 0.051*SL	0.37 + 0.050*SL
	t_{PHL}	0.37	0.30 + 0.034*SL	0.32 + 0.026*SL	0.35 + 0.023*SL
	t_R	0.38	0.17 + 0.104*SL	0.16 + 0.106*SL	0.14 + 0.108*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.041*SL	0.11 + 0.042*SL
B to Y	t_{PLH}	0.47	0.36 + 0.057*SL	0.37 + 0.051*SL	0.38 + 0.050*SL
	t_{PHL}	0.41	0.34 + 0.035*SL	0.37 + 0.026*SL	0.40 + 0.023*SL
	t_R	0.38	0.17 + 0.103*SL	0.16 + 0.106*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.042*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
C to Y	t_{PLH}	0.48	0.37 + 0.056*SL	0.39 + 0.051*SL	0.40 + 0.050*SL
	t_{PHL}	0.46	0.38 + 0.037*SL	0.41 + 0.027*SL	0.45 + 0.024*SL
	t_R	0.38	0.17 + 0.104*SL	0.16 + 0.106*SL	0.14 + 0.108*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.040*SL	0.13 + 0.042*SL

KGM80 AD3D3

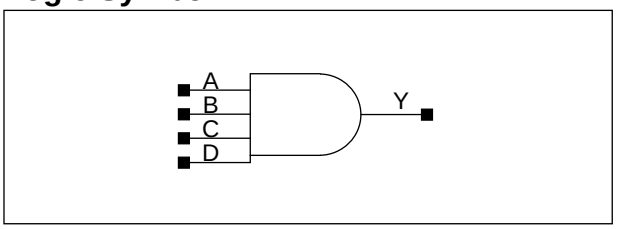
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.51	0.46 + 0.023*SL	0.47 + 0.020*SL	0.49 + 0.018*SL
	t_{PHL}	0.42	0.39 + 0.016*SL	0.40 + 0.012*SL	0.43 + 0.010*SL
	t_R	0.28	0.20 + 0.039*SL	0.21 + 0.035*SL	0.21 + 0.035*SL
	t_F	0.18	0.15 + 0.017*SL	0.15 + 0.015*SL	0.16 + 0.014*SL
B to Y	t_{PLH}	0.52	0.47 + 0.023*SL	0.48 + 0.020*SL	0.50 + 0.018*SL
	t_{PHL}	0.46	0.43 + 0.018*SL	0.44 + 0.013*SL	0.47 + 0.010*SL
	t_R	0.28	0.20 + 0.038*SL	0.21 + 0.035*SL	0.21 + 0.035*SL
	t_F	0.19	0.16 + 0.017*SL	0.16 + 0.015*SL	0.18 + 0.014*SL
C to Y	t_{PLH}	0.53	0.49 + 0.023*SL	0.50 + 0.020*SL	0.52 + 0.018*SL
	t_{PHL}	0.50	0.47 + 0.018*SL	0.48 + 0.013*SL	0.51 + 0.010*SL
	t_R	0.28	0.20 + 0.039*SL	0.21 + 0.035*SL	0.21 + 0.035*SL
	t_F	0.21	0.18 + 0.018*SL	0.18 + 0.015*SL	0.20 + 0.013*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

AD4/AD4D2

4-Input AND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Data

Input Load (SL)								Gate Count	
KG80									
AD4				*AD4D2*				*AD4*	*AD4D2*
A	B	C	D	A	B	C	D		
0.9	0.9	0.9	0.8	0.9	0.9	0.9	0.8	3.0	3.0
KGM80									
AD4				*AD4D2*				*AD4*	*AD4D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	3.0	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.42	0.32 + 0.048*SL	0.33 + 0.043*SL	0.34 + 0.042*SL
	t_{PHL}	0.30	0.24 + 0.031*SL	0.25 + 0.026*SL	0.26 + 0.024*SL
	t_R	0.32	0.15 + 0.085*SL	0.15 + 0.087*SL	0.14 + 0.088*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
B to Y	t_{PLH}	0.43	0.33 + 0.048*SL	0.34 + 0.043*SL	0.36 + 0.042*SL
	t_{PHL}	0.33	0.26 + 0.033*SL	0.28 + 0.026*SL	0.29 + 0.024*SL
	t_R	0.32	0.15 + 0.084*SL	0.15 + 0.086*SL	0.14 + 0.088*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
C to Y	t_{PLH}	0.44	0.35 + 0.048*SL	0.36 + 0.043*SL	0.37 + 0.042*SL
	t_{PHL}	0.36	0.29 + 0.035*SL	0.31 + 0.027*SL	0.32 + 0.024*SL
	t_R	0.32	0.15 + 0.086*SL	0.15 + 0.086*SL	0.14 + 0.088*SL
	t_F	0.20	0.12 + 0.040*SL	0.12 + 0.039*SL	0.11 + 0.040*SL
D to Y	t_{PLH}	0.44	0.34 + 0.048*SL	0.36 + 0.043*SL	0.37 + 0.042*SL
	t_{PHL}	0.37	0.30 + 0.035*SL	0.32 + 0.028*SL	0.34 + 0.024*SL
	t_R	0.32	0.15 + 0.085*SL	0.15 + 0.086*SL	0.14 + 0.088*SL
	t_F	0.21	0.13 + 0.041*SL	0.13 + 0.039*SL	0.13 + 0.040*SL

KG80 AD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.39	0.33 + 0.027*SL	0.34 + 0.023*SL	0.35 + 0.022*SL
	t_{PHL}	0.28	0.25 + 0.018*SL	0.26 + 0.014*SL	0.27 + 0.013*SL
	t_R	0.25	0.17 + 0.039*SL	0.16 + 0.043*SL	0.16 + 0.043*SL
	t_F	0.14	0.10 + 0.020*SL	0.11 + 0.019*SL	0.10 + 0.020*SL
B to Y	t_{PLH}	0.40	0.34 + 0.027*SL	0.35 + 0.023*SL	0.36 + 0.022*SL
	t_{PHL}	0.31	0.27 + 0.020*SL	0.28 + 0.015*SL	0.30 + 0.013*SL
	t_R	0.25	0.17 + 0.039*SL	0.16 + 0.043*SL	0.16 + 0.043*SL
	t_F	0.16	0.11 + 0.022*SL	0.12 + 0.019*SL	0.11 + 0.020*SL
C to Y	t_{PLH}	0.41	0.36 + 0.026*SL	0.37 + 0.023*SL	0.37 + 0.022*SL
	t_{PHL}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.33 + 0.013*SL
	t_R	0.25	0.17 + 0.041*SL	0.16 + 0.043*SL	0.16 + 0.043*SL
	t_F	0.17	0.12 + 0.021*SL	0.13 + 0.019*SL	0.13 + 0.020*SL
D to Y	t_{PLH}	0.41	0.36 + 0.026*SL	0.36 + 0.023*SL	0.37 + 0.022*SL
	t_{PHL}	0.35	0.31 + 0.021*SL	0.32 + 0.016*SL	0.34 + 0.014*SL
	t_R	0.25	0.17 + 0.039*SL	0.16 + 0.043*SL	0.16 + 0.043*SL
	t_F	0.18	0.14 + 0.021*SL	0.14 + 0.020*SL	0.14 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

AD4/AD4D2

4-Input AND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AD4

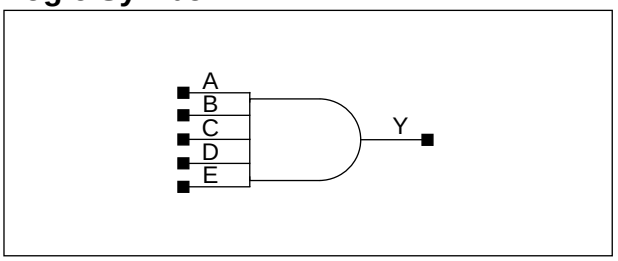
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.56	0.44 + 0.062*SL	0.47 + 0.052*SL	0.49 + 0.050*SL
	t_{PHL}	0.40	0.33 + 0.035*SL	0.35 + 0.027*SL	0.38 + 0.024*SL
	t_R	0.42	0.20 + 0.108*SL	0.21 + 0.105*SL	0.19 + 0.107*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
B to Y	t_{PLH}	0.59	0.47 + 0.062*SL	0.49 + 0.052*SL	0.52 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.036*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.42	0.21 + 0.107*SL	0.21 + 0.105*SL	0.19 + 0.107*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
C to Y	t_{PLH}	0.63	0.50 + 0.061*SL	0.53 + 0.052*SL	0.56 + 0.050*SL
	t_{PHL}	0.49	0.41 + 0.038*SL	0.44 + 0.028*SL	0.48 + 0.024*SL
	t_R	0.42	0.21 + 0.108*SL	0.21 + 0.105*SL	0.19 + 0.107*SL
	t_F	0.24	0.15 + 0.045*SL	0.16 + 0.041*SL	0.15 + 0.041*SL
D to Y	t_{PLH}	0.63	0.51 + 0.062*SL	0.53 + 0.052*SL	0.56 + 0.050*SL
	t_{PHL}	0.51	0.43 + 0.040*SL	0.46 + 0.028*SL	0.51 + 0.024*SL
	t_R	0.42	0.21 + 0.107*SL	0.21 + 0.105*SL	0.19 + 0.107*SL
	t_F	0.25	0.16 + 0.045*SL	0.17 + 0.041*SL	0.16 + 0.041*SL

KGM80 AD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.51	0.44 + 0.033*SL	0.46 + 0.029*SL	0.49 + 0.026*SL
	t_{PHL}	0.38	0.34 + 0.020*SL	0.35 + 0.015*SL	0.38 + 0.013*SL
	t_R	0.32	0.21 + 0.056*SL	0.22 + 0.053*SL	0.22 + 0.052*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
B to Y	t_{PLH}	0.54	0.47 + 0.034*SL	0.49 + 0.029*SL	0.52 + 0.026*SL
	t_{PHL}	0.42	0.38 + 0.022*SL	0.39 + 0.016*SL	0.42 + 0.013*SL
	t_R	0.32	0.21 + 0.057*SL	0.22 + 0.053*SL	0.22 + 0.052*SL
	t_F	0.18	0.14 + 0.023*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
C to Y	t_{PLH}	0.58	0.51 + 0.034*SL	0.52 + 0.029*SL	0.55 + 0.026*SL
	t_{PHL}	0.46	0.42 + 0.023*SL	0.44 + 0.017*SL	0.47 + 0.013*SL
	t_R	0.32	0.21 + 0.056*SL	0.22 + 0.053*SL	0.22 + 0.052*SL
	t_F	0.20	0.15 + 0.024*SL	0.16 + 0.021*SL	0.17 + 0.020*SL
D to Y	t_{PLH}	0.58	0.51 + 0.034*SL	0.53 + 0.029*SL	0.56 + 0.026*SL
	t_{PHL}	0.49	0.44 + 0.024*SL	0.46 + 0.017*SL	0.50 + 0.014*SL
	t_R	0.32	0.21 + 0.057*SL	0.22 + 0.053*SL	0.22 + 0.052*SL
	t_F	0.21	0.16 + 0.024*SL	0.17 + 0.021*SL	0.18 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	1

Cell Data

Input Load (SL)										Gate Count	
KG80											
AD5					*AD5D2*					*AD5*	*AD5D2*
A	B	C	D	E	A	B	C	D	E		
0.5	0.6	0.6	0.8	0.7	0.5	0.6	0.6	0.8	0.7	4.0	5.0
KGM80											
AD5					*AD5D2*					*AD5*	*AD5D2*
A	B	C	D	E	A	B	C	D	E		
0.7	0.8	0.8	0.8	0.9	0.7	0.8	0.8	0.9	0.9	4.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.39 + 0.052*SL	0.40 + 0.045*SL	0.42 + 0.042*SL
	t_{PHL}	0.31	0.24 + 0.033*SL	0.26 + 0.026*SL	0.28 + 0.024*SL
	t_R	0.35	0.18 + 0.086*SL	0.18 + 0.086*SL	0.17 + 0.087*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
B to Y	t_{PLH}	0.51	0.41 + 0.052*SL	0.42 + 0.045*SL	0.44 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.034*SL	0.29 + 0.027*SL	0.31 + 0.024*SL
	t_R	0.35	0.18 + 0.086*SL	0.18 + 0.086*SL	0.17 + 0.087*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.040*SL	0.11 + 0.040*SL
C to Y	t_{PLH}	0.54	0.44 + 0.052*SL	0.45 + 0.045*SL	0.47 + 0.042*SL
	t_{PHL}	0.37	0.30 + 0.036*SL	0.32 + 0.027*SL	0.34 + 0.024*SL
	t_R	0.35	0.18 + 0.086*SL	0.18 + 0.086*SL	0.17 + 0.087*SL
	t_F	0.20	0.12 + 0.041*SL	0.13 + 0.040*SL	0.12 + 0.040*SL
D to Y	t_{PLH}	0.55	0.45 + 0.052*SL	0.47 + 0.045*SL	0.48 + 0.042*SL
	t_{PHL}	0.38	0.31 + 0.037*SL	0.33 + 0.028*SL	0.36 + 0.025*SL
	t_R	0.35	0.18 + 0.085*SL	0.18 + 0.086*SL	0.17 + 0.087*SL
	t_F	0.22	0.13 + 0.042*SL	0.14 + 0.039*SL	0.13 + 0.040*SL
E to Y	t_{PLH}	0.56	0.46 + 0.052*SL	0.48 + 0.045*SL	0.50 + 0.042*SL
	t_{PHL}	0.40	0.32 + 0.038*SL	0.35 + 0.029*SL	0.37 + 0.025*SL
	t_R	0.35	0.18 + 0.086*SL	0.18 + 0.086*SL	0.17 + 0.087*SL
	t_F	0.23	0.14 + 0.043*SL	0.15 + 0.039*SL	0.15 + 0.040*SL

KG80 AD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.51	0.45 + 0.031*SL	0.46 + 0.025*SL	0.48 + 0.023*SL
	t_{PHL}	0.31	0.27 + 0.020*SL	0.28 + 0.016*SL	0.30 + 0.013*SL
	t_R	0.30	0.22 + 0.042*SL	0.22 + 0.042*SL	0.21 + 0.043*SL
	t_F	0.16	0.11 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
B to Y	t_{PLH}	0.53	0.47 + 0.030*SL	0.48 + 0.025*SL	0.50 + 0.023*SL
	t_{PHL}	0.34	0.30 + 0.021*SL	0.31 + 0.016*SL	0.32 + 0.014*SL
	t_R	0.30	0.22 + 0.041*SL	0.22 + 0.042*SL	0.21 + 0.043*SL
	t_F	0.17	0.12 + 0.022*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
C to Y	t_{PLH}	0.56	0.50 + 0.030*SL	0.52 + 0.025*SL	0.53 + 0.023*SL
	t_{PHL}	0.37	0.32 + 0.022*SL	0.33 + 0.017*SL	0.36 + 0.014*SL
	t_R	0.30	0.22 + 0.040*SL	0.22 + 0.042*SL	0.21 + 0.043*SL
	t_F	0.18	0.14 + 0.023*SL	0.14 + 0.020*SL	0.15 + 0.019*SL
D to Y	t_{PLH}	0.57	0.51 + 0.030*SL	0.53 + 0.025*SL	0.54 + 0.022*SL
	t_{PHL}	0.38	0.34 + 0.023*SL	0.35 + 0.017*SL	0.37 + 0.014*SL
	t_R	0.30	0.22 + 0.043*SL	0.22 + 0.042*SL	0.21 + 0.043*SL
	t_F	0.19	0.15 + 0.023*SL	0.15 + 0.020*SL	0.16 + 0.019*SL
E to Y	t_{PLH}	0.59	0.53 + 0.030*SL	0.54 + 0.025*SL	0.56 + 0.023*SL
	t_{PHL}	0.40	0.35 + 0.024*SL	0.36 + 0.018*SL	0.39 + 0.015*SL
	t_R	0.30	0.21 + 0.043*SL	0.22 + 0.042*SL	0.21 + 0.043*SL
	t_F	0.21	0.16 + 0.024*SL	0.17 + 0.020*SL	0.17 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.67	0.53 + 0.067*SL	0.57 + 0.055*SL	0.62 + 0.050*SL
	t_{PHL}	0.42	0.34 + 0.037*SL	0.37 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.46	0.23 + 0.113*SL	0.25 + 0.105*SL	0.24 + 0.106*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
B to Y	t_{PLH}	0.71	0.58 + 0.066*SL	0.61 + 0.055*SL	0.66 + 0.050*SL
	t_{PHL}	0.46	0.38 + 0.038*SL	0.41 + 0.028*SL	0.45 + 0.024*SL
	t_R	0.46	0.23 + 0.112*SL	0.25 + 0.105*SL	0.24 + 0.106*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.041*SL	0.14 + 0.042*SL
C to Y	t_{PLH}	0.77	0.64 + 0.066*SL	0.67 + 0.055*SL	0.72 + 0.050*SL
	t_{PHL}	0.51	0.43 + 0.040*SL	0.46 + 0.029*SL	0.51 + 0.024*SL
	t_R	0.46	0.23 + 0.112*SL	0.25 + 0.105*SL	0.24 + 0.106*SL
	t_F	0.24	0.15 + 0.046*SL	0.16 + 0.041*SL	0.16 + 0.041*SL
D to Y	t_{PLH}	0.79	0.66 + 0.066*SL	0.69 + 0.055*SL	0.74 + 0.050*SL
	t_{PHL}	0.53	0.45 + 0.042*SL	0.48 + 0.029*SL	0.53 + 0.025*SL
	t_R	0.46	0.23 + 0.112*SL	0.25 + 0.105*SL	0.24 + 0.106*SL
	t_F	0.26	0.16 + 0.046*SL	0.18 + 0.041*SL	0.17 + 0.041*SL
E to Y	t_{PLH}	0.82	0.69 + 0.066*SL	0.71 + 0.055*SL	0.76 + 0.050*SL
	t_{PHL}	0.56	0.47 + 0.044*SL	0.51 + 0.030*SL	0.56 + 0.025*SL
	t_R	0.46	0.23 + 0.112*SL	0.25 + 0.105*SL	0.24 + 0.106*SL
	t_F	0.27	0.18 + 0.047*SL	0.19 + 0.041*SL	0.19 + 0.041*SL

KGM80 AD5D2

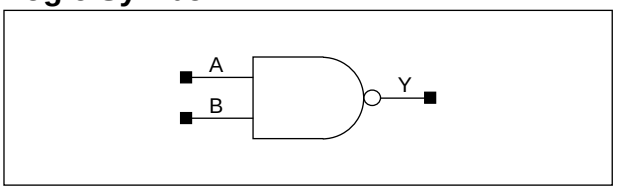
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.70	0.62 + 0.037*SL	0.64 + 0.031*SL	0.68 + 0.027*SL
	t_{PHL}	0.43	0.39 + 0.023*SL	0.40 + 0.017*SL	0.44 + 0.014*SL
	t_R	0.38	0.26 + 0.059*SL	0.28 + 0.054*SL	0.29 + 0.052*SL
	t_F	0.19	0.14 + 0.025*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
B to Y	t_{PLH}	0.74	0.67 + 0.037*SL	0.68 + 0.031*SL	0.73 + 0.027*SL
	t_{PHL}	0.47	0.42 + 0.024*SL	0.44 + 0.017*SL	0.48 + 0.014*SL
	t_R	0.38	0.26 + 0.058*SL	0.27 + 0.054*SL	0.29 + 0.052*SL
	t_F	0.20	0.15 + 0.026*SL	0.16 + 0.022*SL	0.18 + 0.020*SL
C to Y	t_{PLH}	0.80	0.73 + 0.037*SL	0.74 + 0.031*SL	0.79 + 0.027*SL
	t_{PHL}	0.52	0.47 + 0.025*SL	0.49 + 0.018*SL	0.53 + 0.014*SL
	t_R	0.38	0.26 + 0.058*SL	0.27 + 0.054*SL	0.29 + 0.052*SL
	t_F	0.22	0.17 + 0.025*SL	0.18 + 0.022*SL	0.20 + 0.020*SL
D to Y	t_{PLH}	0.82	0.75 + 0.037*SL	0.77 + 0.031*SL	0.81 + 0.027*SL
	t_{PHL}	0.54	0.49 + 0.026*SL	0.51 + 0.019*SL	0.55 + 0.014*SL
	t_R	0.38	0.26 + 0.058*SL	0.27 + 0.054*SL	0.29 + 0.052*SL
	t_F	0.23	0.18 + 0.026*SL	0.19 + 0.022*SL	0.21 + 0.020*SL
E to Y	t_{PLH}	0.85	0.77 + 0.037*SL	0.79 + 0.031*SL	0.83 + 0.027*SL
	t_{PHL}	0.57	0.51 + 0.028*SL	0.54 + 0.019*SL	0.58 + 0.015*SL
	t_R	0.38	0.26 + 0.058*SL	0.27 + 0.054*SL	0.29 + 0.052*SL
	t_F	0.25	0.20 + 0.027*SL	0.21 + 0.022*SL	0.23 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

ND2/ND2D2

2-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)				Gate Count	
KG80					
ND2		*ND2D2*		*ND2*	*ND2D2*
A	B	A	B		
0.9	0.9	1.7	1.7	1.0	2.0
KGM80					
ND2		*ND2D2*		*ND2*	*ND2D2*
A	B	A	B		
1.0	1.0	2.1	2.0	1.0	2.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 ND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.12 + 0.046*SL	0.14 + 0.040*SL	0.13 + 0.041*SL
	t_{PHL}	0.15	0.06 + 0.045*SL	0.08 + 0.034*SL	0.09 + 0.034*SL
	t_R	0.32	0.17 + 0.075*SL	0.15 + 0.084*SL	0.12 + 0.088*SL
	t_F	0.28	0.17 + 0.059*SL	0.16 + 0.061*SL	0.13 + 0.065*SL
B to Y	t_{PLH}	0.24	0.16 + 0.042*SL	0.16 + 0.040*SL	0.16 + 0.041*SL
	t_{PHL}	0.14	0.05 + 0.041*SL	0.07 + 0.035*SL	0.07 + 0.034*SL
	t_R	0.36	0.21 + 0.075*SL	0.19 + 0.083*SL	0.15 + 0.088*SL
	t_F	0.27	0.16 + 0.056*SL	0.14 + 0.062*SL	0.11 + 0.066*SL

KG80 ND2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.17	0.11 + 0.027*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
	t_{PHL}	0.10	0.05 + 0.026*SL	0.06 + 0.021*SL	0.09 + 0.017*SL
	t_R	0.24	0.16 + 0.037*SL	0.16 + 0.039*SL	0.14 + 0.042*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.029*SL	0.15 + 0.031*SL
B to Y	t_{PLH}	0.21	0.16 + 0.023*SL	0.17 + 0.020*SL	0.17 + 0.020*SL
	t_{PHL}	0.10	0.05 + 0.024*SL	0.06 + 0.019*SL	0.07 + 0.017*SL
	t_R	0.29	0.22 + 0.036*SL	0.21 + 0.039*SL	0.19 + 0.042*SL
	t_F	0.21	0.15 + 0.026*SL	0.15 + 0.029*SL	0.13 + 0.031*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 ND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.15 + 0.055*SL	0.16 + 0.049*SL	0.16 + 0.050*SL
	t_{PHL}	0.18	0.08 + 0.048*SL	0.11 + 0.038*SL	0.12 + 0.037*SL
	t_R	0.38	0.19 + 0.097*SL	0.17 + 0.105*SL	0.13 + 0.108*SL
	t_F	0.30	0.17 + 0.068*SL	0.16 + 0.070*SL	0.13 + 0.073*SL
B to Y	t_{PLH}	0.30	0.19 + 0.051*SL	0.20 + 0.049*SL	0.20 + 0.050*SL
	t_{PHL}	0.17	0.09 + 0.044*SL	0.10 + 0.038*SL	0.11 + 0.037*SL
	t_R	0.43	0.23 + 0.098*SL	0.21 + 0.105*SL	0.18 + 0.108*SL
	t_F	0.29	0.15 + 0.067*SL	0.14 + 0.071*SL	0.11 + 0.074*SL

KGM80 ND2D2

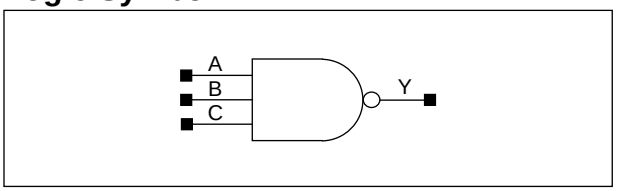
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.13 + 0.031*SL	0.15 + 0.026*SL	0.16 + 0.025*SL
	t_{PHL}	0.12	0.07 + 0.027*SL	0.09 + 0.021*SL	0.12 + 0.018*SL
	t_R	0.28	0.18 + 0.046*SL	0.17 + 0.051*SL	0.15 + 0.053*SL
	t_F	0.23	0.15 + 0.038*SL	0.17 + 0.034*SL	0.15 + 0.035*SL
B to Y	t_{PLH}	0.25	0.20 + 0.028*SL	0.21 + 0.025*SL	0.21 + 0.025*SL
	t_{PHL}	0.14	0.09 + 0.025*SL	0.10 + 0.020*SL	0.12 + 0.019*SL
	t_R	0.34	0.24 + 0.049*SL	0.24 + 0.051*SL	0.21 + 0.053*SL
	t_F	0.21	0.15 + 0.034*SL	0.15 + 0.034*SL	0.12 + 0.036*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

ND3/ND3D2

3-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Data

Input Load (SL)						Gate Count	
KG80							
ND3			*ND3D2*			*ND3*	*ND3D2*
A	B	C	A	B	C		
0.9	0.8	0.8	1.7	1.7	1.7	2.0	3.0
KGM80							
ND3			*ND3D2*			*ND3*	*ND3D2*
A	B	C	A	B	C		
1.0	1.0	1.0	2.0	2.0	1.9	2.0	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 ND3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.15 + 0.044*SL	0.15 + 0.041*SL	0.15 + 0.041*SL
	t_{PHL}	0.22	0.12 + 0.048*SL	0.13 + 0.044*SL	0.13 + 0.045*SL
	t_R	0.37	0.22 + 0.075*SL	0.20 + 0.084*SL	0.17 + 0.088*SL
	t_F	0.40	0.23 + 0.083*SL	0.22 + 0.089*SL	0.19 + 0.092*SL
B to Y	t_{PLH}	0.26	0.18 + 0.041*SL	0.18 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.22	0.12 + 0.048*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.41	0.26 + 0.075*SL	0.24 + 0.084*SL	0.21 + 0.088*SL
	t_F	0.39	0.23 + 0.082*SL	0.21 + 0.090*SL	0.18 + 0.093*SL
C to Y	t_{PLH}	0.29	0.21 + 0.041*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.22	0.12 + 0.047*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.47	0.32 + 0.076*SL	0.30 + 0.083*SL	0.27 + 0.088*SL
	t_F	0.38	0.21 + 0.084*SL	0.19 + 0.091*SL	0.17 + 0.094*SL

KG80 ND3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.17	0.12 + 0.027*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
	t_{PHL}	0.14	0.08 + 0.029*SL	0.10 + 0.024*SL	0.11 + 0.022*SL
	t_R	0.26	0.19 + 0.035*SL	0.18 + 0.039*SL	0.16 + 0.042*SL
	t_F	0.29	0.21 + 0.040*SL	0.20 + 0.041*SL	0.18 + 0.044*SL
B to Y	t_{PLH}	0.21	0.16 + 0.023*SL	0.17 + 0.020*SL	0.17 + 0.020*SL
	t_{PHL}	0.15	0.09 + 0.027*SL	0.10 + 0.024*SL	0.11 + 0.022*SL
	t_R	0.31	0.24 + 0.036*SL	0.23 + 0.039*SL	0.21 + 0.042*SL
	t_F	0.28	0.20 + 0.040*SL	0.20 + 0.041*SL	0.17 + 0.045*SL
C to Y	t_{PLH}	0.23	0.19 + 0.022*SL	0.19 + 0.020*SL	0.19 + 0.020*SL
	t_{PHL}	0.14	0.09 + 0.025*SL	0.10 + 0.023*SL	0.10 + 0.022*SL
	t_R	0.36	0.28 + 0.036*SL	0.28 + 0.039*SL	0.26 + 0.042*SL
	t_F	0.26	0.18 + 0.039*SL	0.17 + 0.043*SL	0.16 + 0.045*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 ND3

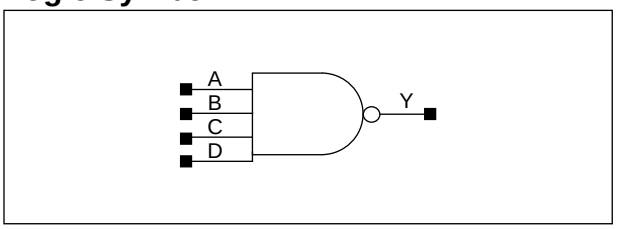
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.19 + 0.052*SL	0.20 + 0.049*SL	0.20 + 0.050*SL
	t_{PHL}	0.27	0.17 + 0.054*SL	0.17 + 0.051*SL	0.17 + 0.051*SL
	t_R	0.47	0.27 + 0.100*SL	0.25 + 0.105*SL	0.22 + 0.108*SL
	t_F	0.47	0.28 + 0.097*SL	0.27 + 0.102*SL	0.23 + 0.105*SL
B to Y	t_{PLH}	0.33	0.23 + 0.050*SL	0.23 + 0.049*SL	0.23 + 0.050*SL
	t_{PHL}	0.28	0.18 + 0.054*SL	0.18 + 0.051*SL	0.18 + 0.051*SL
	t_R	0.51	0.31 + 0.100*SL	0.30 + 0.106*SL	0.27 + 0.109*SL
	t_F	0.46	0.27 + 0.098*SL	0.25 + 0.103*SL	0.23 + 0.105*SL
C to Y	t_{PLH}	0.37	0.27 + 0.051*SL	0.27 + 0.050*SL	0.28 + 0.050*SL
	t_{PHL}	0.30	0.19 + 0.054*SL	0.20 + 0.051*SL	0.20 + 0.051*SL
	t_R	0.59	0.39 + 0.100*SL	0.37 + 0.105*SL	0.34 + 0.108*SL
	t_F	0.45	0.25 + 0.099*SL	0.24 + 0.104*SL	0.22 + 0.105*SL

KGM80 ND3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.15 + 0.031*SL	0.16 + 0.025*SL	0.17 + 0.025*SL
	t_{PHL}	0.17	0.11 + 0.031*SL	0.12 + 0.026*SL	0.13 + 0.025*SL
	t_R	0.30	0.21 + 0.045*SL	0.20 + 0.051*SL	0.17 + 0.053*SL
	t_F	0.32	0.22 + 0.050*SL	0.23 + 0.049*SL	0.20 + 0.051*SL
B to Y	t_{PLH}	0.27	0.21 + 0.027*SL	0.22 + 0.025*SL	0.22 + 0.025*SL
	t_{PHL}	0.20	0.14 + 0.030*SL	0.15 + 0.026*SL	0.16 + 0.026*SL
	t_R	0.37	0.27 + 0.047*SL	0.26 + 0.051*SL	0.24 + 0.053*SL
	t_F	0.31	0.22 + 0.047*SL	0.21 + 0.050*SL	0.19 + 0.052*SL
C to Y	t_{PLH}	0.30	0.24 + 0.027*SL	0.25 + 0.025*SL	0.25 + 0.025*SL
	t_{PHL}	0.20	0.15 + 0.029*SL	0.15 + 0.026*SL	0.16 + 0.026*SL
	t_R	0.43	0.33 + 0.049*SL	0.32 + 0.051*SL	0.30 + 0.053*SL
	t_F	0.30	0.20 + 0.047*SL	0.19 + 0.051*SL	0.18 + 0.052*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
ND4				*ND4D2*				*ND4*	*ND4D2*
A	B	C	D	A	B	C	D		
0.9	0.9	0.8	0.9	1.7	1.7	1.7	1.7	2.0	4.0
KGM80									
ND4				*ND4D2*				*ND4*	*ND4D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	2.1	2.0	1.9	1.9	2.0	4.0

ND4/ND4D2

4-Input NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 ND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.14 + 0.046*SL	0.15 + 0.041*SL	0.15 + 0.041*SL
	t_{PHL}	0.24	0.13 + 0.056*SL	0.13 + 0.054*SL	0.12 + 0.055*SL
	t_R	0.36	0.20 + 0.076*SL	0.18 + 0.084*SL	0.16 + 0.088*SL
	t_F	0.48	0.27 + 0.107*SL	0.25 + 0.115*SL	0.22 + 0.119*SL
B to Y	t_{PLH}	0.25	0.17 + 0.043*SL	0.17 + 0.041*SL	0.17 + 0.041*SL
	t_{PHL}	0.25	0.13 + 0.058*SL	0.14 + 0.055*SL	0.13 + 0.056*SL
	t_R	0.40	0.24 + 0.077*SL	0.23 + 0.084*SL	0.20 + 0.088*SL
	t_F	0.48	0.27 + 0.107*SL	0.25 + 0.116*SL	0.22 + 0.119*SL
C to Y	t_{PLH}	0.28	0.20 + 0.042*SL	0.20 + 0.041*SL	0.20 + 0.042*SL
	t_{PHL}	0.26	0.15 + 0.059*SL	0.15 + 0.056*SL	0.15 + 0.056*SL
	t_R	0.45	0.30 + 0.076*SL	0.28 + 0.083*SL	0.25 + 0.088*SL
	t_F	0.47	0.25 + 0.110*SL	0.23 + 0.117*SL	0.21 + 0.120*SL
D to Y	t_{PLH}	0.30	0.21 + 0.042*SL	0.21 + 0.042*SL	0.22 + 0.042*SL
	t_{PHL}	0.26	0.15 + 0.057*SL	0.15 + 0.056*SL	0.15 + 0.056*SL
	t_R	0.50	0.34 + 0.079*SL	0.33 + 0.083*SL	0.30 + 0.087*SL
	t_F	0.46	0.23 + 0.113*SL	0.22 + 0.118*SL	0.21 + 0.120*SL

KG80 ND4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
	t_{PHL}	0.17	0.11 + 0.031*SL	0.12 + 0.027*SL	0.12 + 0.027*SL
	t_R	0.27	0.20 + 0.037*SL	0.19 + 0.039*SL	0.17 + 0.042*SL
	t_F	0.37	0.26 + 0.053*SL	0.26 + 0.055*SL	0.24 + 0.058*SL
B to Y	t_{PLH}	0.22	0.17 + 0.023*SL	0.18 + 0.020*SL	0.18 + 0.021*SL
	t_{PHL}	0.19	0.13 + 0.031*SL	0.14 + 0.028*SL	0.14 + 0.028*SL
	t_R	0.33	0.25 + 0.035*SL	0.24 + 0.039*SL	0.23 + 0.042*SL
	t_F	0.37	0.26 + 0.051*SL	0.25 + 0.056*SL	0.24 + 0.058*SL
C to Y	t_{PLH}	0.24	0.19 + 0.022*SL	0.20 + 0.021*SL	0.20 + 0.021*SL
	t_{PHL}	0.20	0.14 + 0.031*SL	0.14 + 0.028*SL	0.15 + 0.028*SL
	t_R	0.37	0.30 + 0.037*SL	0.29 + 0.039*SL	0.28 + 0.042*SL
	t_F	0.36	0.25 + 0.052*SL	0.24 + 0.056*SL	0.22 + 0.059*SL
D to Y	t_{PLH}	0.26	0.21 + 0.022*SL	0.21 + 0.021*SL	0.21 + 0.021*SL
	t_{PHL}	0.21	0.15 + 0.030*SL	0.15 + 0.029*SL	0.15 + 0.028*SL
	t_R	0.42	0.35 + 0.038*SL	0.34 + 0.040*SL	0.33 + 0.042*SL
	t_F	0.34	0.23 + 0.054*SL	0.23 + 0.057*SL	0.21 + 0.059*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 ND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.18 + 0.053*SL	0.19 + 0.050*SL	0.19 + 0.050*SL
	t_{PHL}	0.30	0.17 + 0.066*SL	0.17 + 0.065*SL	0.17 + 0.065*SL
	t_R	0.44	0.24 + 0.099*SL	0.23 + 0.105*SL	0.19 + 0.109*SL
	t_F	0.58	0.32 + 0.128*SL	0.31 + 0.133*SL	0.28 + 0.136*SL
B to Y	t_{PLH}	0.32	0.22 + 0.051*SL	0.23 + 0.050*SL	0.23 + 0.050*SL
	t_{PHL}	0.32	0.19 + 0.067*SL	0.20 + 0.065*SL	0.20 + 0.065*SL
	t_R	0.49	0.29 + 0.099*SL	0.27 + 0.106*SL	0.24 + 0.109*SL
	t_F	0.58	0.32 + 0.128*SL	0.31 + 0.134*SL	0.28 + 0.136*SL
C to Y	t_{PLH}	0.37	0.26 + 0.051*SL	0.27 + 0.050*SL	0.27 + 0.050*SL
	t_{PHL}	0.36	0.22 + 0.067*SL	0.23 + 0.065*SL	0.23 + 0.065*SL
	t_R	0.56	0.36 + 0.099*SL	0.35 + 0.105*SL	0.31 + 0.108*SL
	t_F	0.57	0.31 + 0.130*SL	0.30 + 0.135*SL	0.28 + 0.136*SL
D to Y	t_{PLH}	0.39	0.28 + 0.053*SL	0.29 + 0.051*SL	0.30 + 0.050*SL
	t_{PHL}	0.36	0.23 + 0.067*SL	0.24 + 0.065*SL	0.24 + 0.065*SL
	t_R	0.62	0.42 + 0.101*SL	0.41 + 0.105*SL	0.37 + 0.108*SL
	t_F	0.56	0.30 + 0.132*SL	0.29 + 0.135*SL	0.28 + 0.136*SL

KGM80 ND4D2

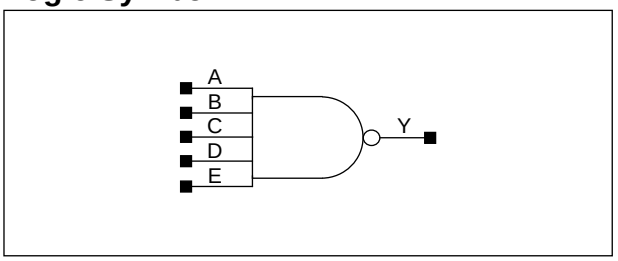
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.16 + 0.030*SL	0.18 + 0.025*SL	0.18 + 0.025*SL
	t_{PHL}	0.22	0.15 + 0.036*SL	0.16 + 0.032*SL	0.15 + 0.032*SL
	t_R	0.33	0.23 + 0.049*SL	0.23 + 0.051*SL	0.20 + 0.053*SL
	t_F	0.44	0.31 + 0.064*SL	0.31 + 0.065*SL	0.29 + 0.067*SL
B to Y	t_{PLH}	0.28	0.23 + 0.027*SL	0.23 + 0.025*SL	0.23 + 0.025*SL
	t_{PHL}	0.26	0.19 + 0.036*SL	0.20 + 0.033*SL	0.20 + 0.033*SL
	t_R	0.40	0.30 + 0.048*SL	0.29 + 0.051*SL	0.27 + 0.053*SL
	t_F	0.44	0.31 + 0.062*SL	0.30 + 0.066*SL	0.29 + 0.067*SL
C to Y	t_{PLH}	0.31	0.26 + 0.026*SL	0.26 + 0.025*SL	0.26 + 0.025*SL
	t_{PHL}	0.28	0.21 + 0.035*SL	0.22 + 0.033*SL	0.22 + 0.033*SL
	t_R	0.45	0.36 + 0.048*SL	0.35 + 0.051*SL	0.33 + 0.053*SL
	t_F	0.43	0.30 + 0.064*SL	0.30 + 0.066*SL	0.28 + 0.067*SL
D to Y	t_{PLH}	0.34	0.28 + 0.027*SL	0.28 + 0.026*SL	0.29 + 0.025*SL
	t_{PHL}	0.30	0.23 + 0.034*SL	0.24 + 0.033*SL	0.24 + 0.033*SL
	t_R	0.52	0.42 + 0.050*SL	0.42 + 0.051*SL	0.40 + 0.053*SL
	t_F	0.42	0.29 + 0.064*SL	0.29 + 0.067*SL	0.28 + 0.068*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

ND5/ND5D2

5-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)										Gate Count	
KG80											
ND5					*ND5D2*					*ND5*	*ND5D2*
A	B	C	D	E	A	B	C	D	E		
0.5	0.6	0.6	0.8	0.7	1.1	1.1	1.3	1.5	1.4	3.0	5.0
KGM80											
ND5					*ND5D2*					*ND5*	*ND5D2*
A	B	C	D	E	A	B	C	D	E		
0.7	0.8	0.8	0.9	0.9	1.3	1.6	1.6	1.7	1.7	3.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 ND5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.17 + 0.043*SL	0.18 + 0.041*SL	0.17 + 0.041*SL
	t_{PHL}	0.33	0.20 + 0.063*SL	0.19 + 0.066*SL	0.19 + 0.066*SL
	t_R	0.42	0.27 + 0.079*SL	0.25 + 0.085*SL	0.23 + 0.089*SL
	t_F	0.69	0.41 + 0.139*SL	0.40 + 0.143*SL	0.37 + 0.147*SL
B to Y	t_{PLH}	0.28	0.20 + 0.041*SL	0.20 + 0.041*SL	0.20 + 0.041*SL
	t_{PHL}	0.35	0.22 + 0.066*SL	0.22 + 0.067*SL	0.21 + 0.067*SL
	t_R	0.47	0.31 + 0.078*SL	0.29 + 0.085*SL	0.27 + 0.088*SL
	t_F	0.69	0.41 + 0.138*SL	0.40 + 0.144*SL	0.39 + 0.146*SL
C to Y	t_{PLH}	0.31	0.23 + 0.042*SL	0.23 + 0.041*SL	0.23 + 0.042*SL
	t_{PHL}	0.38	0.24 + 0.067*SL	0.24 + 0.067*SL	0.24 + 0.067*SL
	t_R	0.52	0.36 + 0.079*SL	0.35 + 0.084*SL	0.32 + 0.088*SL
	t_F	0.69	0.41 + 0.141*SL	0.40 + 0.145*SL	0.39 + 0.146*SL
D to Y	t_{PLH}	0.33	0.24 + 0.043*SL	0.24 + 0.042*SL	0.25 + 0.042*SL
	t_{PHL}	0.39	0.25 + 0.067*SL	0.25 + 0.067*SL	0.26 + 0.067*SL
	t_R	0.57	0.41 + 0.079*SL	0.40 + 0.084*SL	0.37 + 0.088*SL
	t_F	0.68	0.40 + 0.141*SL	0.39 + 0.145*SL	0.38 + 0.147*SL
E to Y	t_{PLH}	0.34	0.25 + 0.045*SL	0.26 + 0.043*SL	0.26 + 0.042*SL
	t_{PHL}	0.40	0.27 + 0.068*SL	0.27 + 0.068*SL	0.27 + 0.067*SL
	t_R	0.62	0.46 + 0.081*SL	0.45 + 0.085*SL	0.43 + 0.088*SL
	t_F	0.68	0.39 + 0.143*SL	0.39 + 0.145*SL	0.38 + 0.147*SL

KG80 ND5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.16 + 0.024*SL	0.17 + 0.021*SL	0.17 + 0.021*SL
	t_{PHL}	0.25	0.19 + 0.031*SL	0.18 + 0.032*SL	0.18 + 0.033*SL
	t_R	0.34	0.27 + 0.031*SL	0.25 + 0.040*SL	0.23 + 0.043*SL
	t_F	0.53	0.40 + 0.067*SL	0.39 + 0.070*SL	0.38 + 0.072*SL
B to Y	t_{PLH}	0.24	0.20 + 0.022*SL	0.20 + 0.020*SL	0.20 + 0.020*SL
	t_{PHL}	0.28	0.21 + 0.033*SL	0.21 + 0.033*SL	0.21 + 0.033*SL
	t_R	0.38	0.31 + 0.038*SL	0.30 + 0.040*SL	0.28 + 0.043*SL
	t_F	0.54	0.40 + 0.069*SL	0.40 + 0.070*SL	0.39 + 0.072*SL
C to Y	t_{PLH}	0.27	0.22 + 0.020*SL	0.22 + 0.021*SL	0.23 + 0.021*SL
	t_{PHL}	0.30	0.23 + 0.034*SL	0.23 + 0.034*SL	0.23 + 0.034*SL
	t_R	0.43	0.36 + 0.038*SL	0.35 + 0.040*SL	0.34 + 0.042*SL
	t_F	0.54	0.40 + 0.069*SL	0.39 + 0.071*SL	0.38 + 0.072*SL
D to Y	t_{PLH}	0.28	0.24 + 0.022*SL	0.24 + 0.021*SL	0.24 + 0.021*SL
	t_{PHL}	0.32	0.25 + 0.034*SL	0.25 + 0.034*SL	0.25 + 0.034*SL
	t_R	0.48	0.41 + 0.039*SL	0.40 + 0.041*SL	0.39 + 0.042*SL
	t_F	0.53	0.39 + 0.070*SL	0.39 + 0.071*SL	0.38 + 0.073*SL
E to Y	t_{PLH}	0.30	0.25 + 0.023*SL	0.25 + 0.022*SL	0.26 + 0.022*SL
	t_{PHL}	0.33	0.26 + 0.035*SL	0.26 + 0.034*SL	0.26 + 0.034*SL
	t_R	0.53	0.45 + 0.040*SL	0.45 + 0.041*SL	0.44 + 0.042*SL
	t_F	0.52	0.38 + 0.071*SL	0.38 + 0.072*SL	0.37 + 0.073*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 ND5

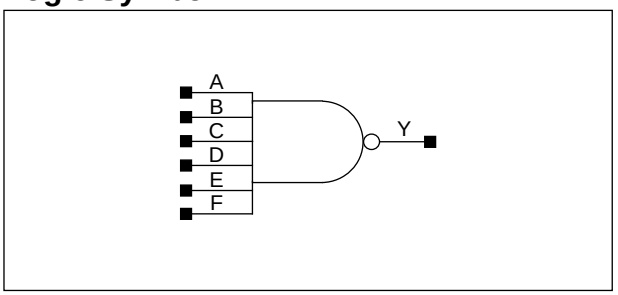
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.23 + 0.050*SL	0.24 + 0.050*SL	0.24 + 0.050*SL
	t_{PHL}	0.43	0.27 + 0.078*SL	0.27 + 0.079*SL	0.27 + 0.079*SL
	t_R	0.56	0.36 + 0.102*SL	0.34 + 0.106*SL	0.32 + 0.109*SL
	t_F	0.88	0.56 + 0.163*SL	0.55 + 0.166*SL	0.53 + 0.168*SL
B to Y	t_{PLH}	0.37	0.27 + 0.050*SL	0.27 + 0.050*SL	0.27 + 0.050*SL
	t_{PHL}	0.47	0.32 + 0.079*SL	0.32 + 0.079*SL	0.32 + 0.079*SL
	t_R	0.61	0.40 + 0.102*SL	0.39 + 0.106*SL	0.36 + 0.109*SL
	t_F	0.89	0.56 + 0.164*SL	0.56 + 0.166*SL	0.54 + 0.167*SL
C to Y	t_{PLH}	0.42	0.31 + 0.051*SL	0.32 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.53	0.37 + 0.080*SL	0.37 + 0.079*SL	0.38 + 0.079*SL
	t_R	0.68	0.48 + 0.101*SL	0.46 + 0.106*SL	0.43 + 0.109*SL
	t_F	0.89	0.56 + 0.164*SL	0.56 + 0.166*SL	0.54 + 0.167*SL
D to Y	t_{PLH}	0.44	0.34 + 0.052*SL	0.34 + 0.051*SL	0.35 + 0.050*SL
	t_{PHL}	0.55	0.39 + 0.080*SL	0.40 + 0.079*SL	0.40 + 0.079*SL
	t_R	0.74	0.54 + 0.101*SL	0.52 + 0.105*SL	0.49 + 0.108*SL
	t_F	0.89	0.56 + 0.164*SL	0.55 + 0.166*SL	0.54 + 0.167*SL
E to Y	t_{PLH}	0.47	0.36 + 0.055*SL	0.36 + 0.052*SL	0.38 + 0.051*SL
	t_{PHL}	0.58	0.42 + 0.080*SL	0.42 + 0.079*SL	0.42 + 0.079*SL
	t_R	0.81	0.61 + 0.102*SL	0.60 + 0.106*SL	0.57 + 0.108*SL
	t_F	0.88	0.55 + 0.165*SL	0.55 + 0.167*SL	0.54 + 0.167*SL

KGM80 ND5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.22 + 0.027*SL	0.23 + 0.025*SL	0.23 + 0.025*SL
	t_{PHL}	0.33	0.26 + 0.037*SL	0.25 + 0.039*SL	0.25 + 0.039*SL
	t_R	0.44	0.34 + 0.050*SL	0.33 + 0.052*SL	0.32 + 0.053*SL
	t_F	0.69	0.53 + 0.082*SL	0.53 + 0.082*SL	0.52 + 0.083*SL
B to Y	t_{PLH}	0.32	0.27 + 0.025*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_{PHL}	0.39	0.31 + 0.040*SL	0.31 + 0.040*SL	0.31 + 0.039*SL
	t_R	0.49	0.39 + 0.050*SL	0.39 + 0.052*SL	0.37 + 0.053*SL
	t_F	0.71	0.54 + 0.081*SL	0.54 + 0.082*SL	0.53 + 0.083*SL
C to Y	t_{PLH}	0.36	0.31 + 0.026*SL	0.31 + 0.025*SL	0.31 + 0.025*SL
	t_{PHL}	0.43	0.35 + 0.040*SL	0.36 + 0.040*SL	0.36 + 0.040*SL
	t_R	0.56	0.46 + 0.050*SL	0.46 + 0.051*SL	0.44 + 0.053*SL
	t_F	0.71	0.54 + 0.081*SL	0.54 + 0.082*SL	0.53 + 0.083*SL
D to Y	t_{PLH}	0.39	0.33 + 0.027*SL	0.34 + 0.026*SL	0.34 + 0.025*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.39 + 0.040*SL	0.39 + 0.040*SL
	t_R	0.63	0.53 + 0.050*SL	0.53 + 0.052*SL	0.51 + 0.053*SL
	t_F	0.70	0.54 + 0.081*SL	0.54 + 0.083*SL	0.53 + 0.083*SL
E to Y	t_{PLH}	0.41	0.35 + 0.028*SL	0.35 + 0.027*SL	0.37 + 0.026*SL
	t_{PHL}	0.49	0.41 + 0.040*SL	0.41 + 0.040*SL	0.41 + 0.040*SL
	t_R	0.70	0.59 + 0.051*SL	0.59 + 0.052*SL	0.58 + 0.053*SL
	t_F	0.70	0.53 + 0.082*SL	0.53 + 0.083*SL	0.52 + 0.083*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	x	x	x	x	x	1
x	0	x	x	x	x	1
x	x	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
1	1	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
KG80													
ND6						*ND6D2*						*ND6*	*ND6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.5	0.5	0.7	0.8	0.8	0.5	0.5	0.5	0.7	0.8	0.8	0.5	5.0	5.0
KGM80													
ND6						*ND6D2*						*ND6*	*ND6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
1.0	1.0	1.0	0.9	0.9	0.7	1.0	1.0	1.0	0.9	0.9	0.7	5.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 ND6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.39	0.31 + 0.043*SL	0.31 + 0.042*SL	0.31 + 0.041*SL
	t_{PHL}	0.45	0.38 + 0.033*SL	0.40 + 0.026*SL	0.42 + 0.024*SL
	t_R	0.26	0.09 + 0.089*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.19	0.10 + 0.042*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
B to Y	t_{PLH}	0.42	0.34 + 0.041*SL	0.34 + 0.042*SL	0.34 + 0.042*SL
	t_{PHL}	0.45	0.38 + 0.033*SL	0.40 + 0.027*SL	0.42 + 0.024*SL
	t_R	0.26	0.08 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.19	0.10 + 0.042*SL	0.11 + 0.040*SL	0.11 + 0.041*SL
C to Y	t_{PLH}	0.45	0.37 + 0.041*SL	0.37 + 0.042*SL	0.37 + 0.042*SL
	t_{PHL}	0.45	0.39 + 0.033*SL	0.40 + 0.027*SL	0.42 + 0.024*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.041*SL	0.10 + 0.041*SL
D to Y	t_{PLH}	0.48	0.39 + 0.041*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_{PHL}	0.47	0.41 + 0.033*SL	0.42 + 0.027*SL	0.44 + 0.024*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.10 + 0.042*SL	0.10 + 0.041*SL	0.10 + 0.041*SL
E to Y	t_{PLH}	0.45	0.36 + 0.042*SL	0.36 + 0.041*SL	0.36 + 0.042*SL
	t_{PHL}	0.47	0.41 + 0.033*SL	0.42 + 0.027*SL	0.44 + 0.024*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.10 + 0.042*SL	0.11 + 0.041*SL	0.10 + 0.041*SL
F to Y	t_{PLH}	0.42	0.33 + 0.041*SL	0.33 + 0.041*SL	0.33 + 0.042*SL
	t_{PHL}	0.47	0.41 + 0.033*SL	0.42 + 0.027*SL	0.44 + 0.024*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.040*SL	0.10 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 ND6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.38	0.34 + 0.021*SL	0.34 + 0.021*SL	0.34 + 0.021*SL
	t_{PHL}	0.48	0.44 + 0.021*SL	0.45 + 0.016*SL	0.46 + 0.014*SL
	t_R	0.18	0.09 + 0.041*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
B to Y	t_{PLH}	0.41	0.37 + 0.021*SL	0.37 + 0.021*SL	0.37 + 0.021*SL
	t_{PHL}	0.48	0.44 + 0.021*SL	0.45 + 0.016*SL	0.46 + 0.014*SL
	t_R	0.18	0.10 + 0.040*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.18	0.13 + 0.022*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
C to Y	t_{PLH}	0.44	0.40 + 0.021*SL	0.40 + 0.021*SL	0.40 + 0.021*SL
	t_{PHL}	0.48	0.44 + 0.021*SL	0.45 + 0.016*SL	0.47 + 0.014*SL
	t_R	0.18	0.10 + 0.040*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.18	0.13 + 0.022*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
D to Y	t_{PLH}	0.47	0.43 + 0.021*SL	0.43 + 0.021*SL	0.43 + 0.021*SL
	t_{PHL}	0.50	0.46 + 0.021*SL	0.47 + 0.016*SL	0.49 + 0.014*SL
	t_R	0.18	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
E to Y	t_{PLH}	0.44	0.39 + 0.021*SL	0.40 + 0.021*SL	0.39 + 0.021*SL
	t_{PHL}	0.50	0.46 + 0.021*SL	0.47 + 0.016*SL	0.49 + 0.014*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.043*SL	0.08 + 0.045*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
F to Y	t_{PLH}	0.40	0.36 + 0.021*SL	0.36 + 0.021*SL	0.36 + 0.021*SL
	t_{PHL}	0.50	0.46 + 0.021*SL	0.47 + 0.016*SL	0.49 + 0.014*SL
	t_R	0.18	0.10 + 0.039*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.14 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 ND6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.53	0.43 + 0.050*SL	0.43 + 0.050*SL	0.43 + 0.050*SL
	t_{PHL}	0.63	0.56 + 0.038*SL	0.59 + 0.028*SL	0.63 + 0.024*SL
	t_R	0.33	0.12 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.13 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
B to Y	t_{PLH}	0.57	0.47 + 0.050*SL	0.47 + 0.050*SL	0.47 + 0.050*SL
	t_{PHL}	0.65	0.57 + 0.038*SL	0.60 + 0.028*SL	0.64 + 0.024*SL
	t_R	0.34	0.12 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
C to Y	t_{PLH}	0.62	0.51 + 0.051*SL	0.52 + 0.050*SL	0.52 + 0.050*SL
	t_{PHL}	0.66	0.58 + 0.037*SL	0.61 + 0.028*SL	0.65 + 0.024*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.13 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
D to Y	t_{PLH}	0.65	0.55 + 0.051*SL	0.55 + 0.050*SL	0.55 + 0.050*SL
	t_{PHL}	0.70	0.63 + 0.038*SL	0.66 + 0.028*SL	0.70 + 0.024*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.23	0.13 + 0.047*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
E to Y	t_{PLH}	0.60	0.50 + 0.051*SL	0.50 + 0.050*SL	0.51 + 0.050*SL
	t_{PHL}	0.69	0.61 + 0.038*SL	0.64 + 0.028*SL	0.68 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
F to Y	t_{PLH}	0.56	0.46 + 0.051*SL	0.46 + 0.050*SL	0.46 + 0.050*SL
	t_{PHL}	0.68	0.60 + 0.038*SL	0.63 + 0.028*SL	0.67 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.14 + 0.047*SL	0.15 + 0.042*SL	0.15 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 ND6D2

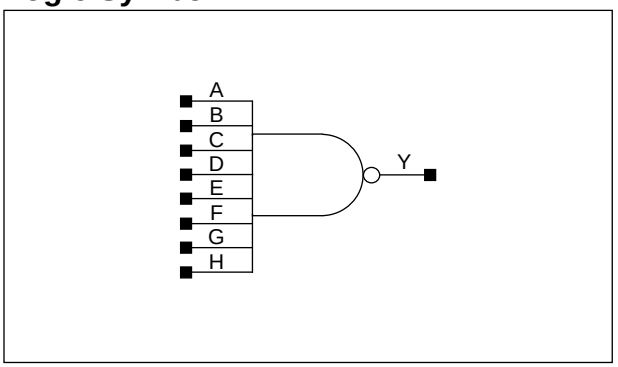
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.52	0.47 + 0.026*SL	0.47 + 0.025*SL	0.47 + 0.025*SL
	t_{PHL}	0.69	0.64 + 0.024*SL	0.66 + 0.018*SL	0.70 + 0.014*SL
	t_R	0.24	0.13 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.22	0.17 + 0.025*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
B to Y	t_{PLH}	0.56	0.51 + 0.026*SL	0.51 + 0.025*SL	0.51 + 0.025*SL
	t_{PHL}	0.70	0.65 + 0.024*SL	0.67 + 0.018*SL	0.71 + 0.014*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.22	0.17 + 0.027*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
C to Y	t_{PLH}	0.61	0.56 + 0.026*SL	0.56 + 0.025*SL	0.56 + 0.025*SL
	t_{PHL}	0.72	0.67 + 0.025*SL	0.68 + 0.018*SL	0.72 + 0.014*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.22	0.17 + 0.026*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
D to Y	t_{PLH}	0.64	0.59 + 0.026*SL	0.59 + 0.025*SL	0.59 + 0.025*SL
	t_{PHL}	0.76	0.71 + 0.025*SL	0.73 + 0.018*SL	0.77 + 0.014*SL
	t_R	0.24	0.14 + 0.052*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.22	0.17 + 0.025*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
E to Y	t_{PLH}	0.59	0.54 + 0.026*SL	0.54 + 0.025*SL	0.54 + 0.025*SL
	t_{PHL}	0.75	0.70 + 0.024*SL	0.72 + 0.018*SL	0.76 + 0.014*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.22	0.17 + 0.025*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
F to Y	t_{PLH}	0.55	0.50 + 0.026*SL	0.50 + 0.025*SL	0.50 + 0.025*SL
	t_{PHL}	0.74	0.69 + 0.024*SL	0.70 + 0.018*SL	0.74 + 0.014*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.22	0.17 + 0.025*SL	0.18 + 0.022*SL	0.20 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

ND8/ND8D2

8-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	x	x	x	x	x	x	x	1
x	0	x	x	x	x	x	x	1
x	x	0	x	x	x	x	x	1
x	x	x	0	x	x	x	x	1
x	x	x	x	0	x	x	x	1
x	x	x	x	x	0	x	x	1
x	x	x	x	x	x	0	x	1
x	x	x	x	x	x	x	0	1
1	1	1	1	1	1	1	1	0

Cell Data

Input Load (SL)																Gate Count	
KG80																	
ND8								*ND8D2*								*ND8*	*ND8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.5	0.6	0.6	0.8	0.7	0.6	0.7	0.5	0.5	0.6	0.6	0.8	0.7	0.6	0.6	0.5	6.0	6.0
KGM80																	
ND8								*ND8D2*								*ND8*	*ND8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
1.0	1.0	1.0	1.0	0.9	0.8	0.8	0.7	1.0	1.0	1.0	1.0	0.9	0.8	0.8	0.7	6.0	6.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 ND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.38	0.30 + 0.041*SL	0.30 + 0.042*SL	0.30 + 0.042*SL
	t_{PHL}	0.48	0.41 + 0.033*SL	0.43 + 0.027*SL	0.45 + 0.024*SL
	t_R	0.26	0.10 + 0.081*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.11 + 0.041*SL	0.11 + 0.041*SL	0.10 + 0.041*SL
B to Y	t_{PLH}	0.41	0.33 + 0.041*SL	0.33 + 0.042*SL	0.33 + 0.042*SL
	t_{PHL}	0.49	0.43 + 0.033*SL	0.44 + 0.027*SL	0.46 + 0.024*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.11 + 0.042*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
C to Y	t_{PLH}	0.44	0.36 + 0.041*SL	0.36 + 0.042*SL	0.36 + 0.042*SL
	t_{PHL}	0.51	0.44 + 0.033*SL	0.46 + 0.027*SL	0.47 + 0.024*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.19	0.10 + 0.042*SL	0.11 + 0.041*SL	0.11 + 0.041*SL
D to Y	t_{PLH}	0.46	0.38 + 0.042*SL	0.38 + 0.041*SL	0.37 + 0.042*SL
	t_{PHL}	0.50	0.44 + 0.033*SL	0.45 + 0.027*SL	0.47 + 0.024*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
E to Y	t_{PLH}	0.49	0.41 + 0.041*SL	0.41 + 0.041*SL	0.41 + 0.042*SL
	t_{PHL}	0.54	0.47 + 0.033*SL	0.49 + 0.027*SL	0.51 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.19	0.11 + 0.042*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
F to Y	t_{PLH}	0.48	0.39 + 0.041*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_{PHL}	0.54	0.48 + 0.033*SL	0.49 + 0.027*SL	0.51 + 0.024*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.11 + 0.041*SL	0.11 + 0.040*SL	0.11 + 0.041*SL
G to Y	t_{PLH}	0.45	0.36 + 0.041*SL	0.36 + 0.041*SL	0.36 + 0.042*SL
	t_{PHL}	0.53	0.46 + 0.033*SL	0.48 + 0.027*SL	0.50 + 0.024*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.11 + 0.041*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
H to Y	t_{PLH}	0.42	0.33 + 0.041*SL	0.33 + 0.042*SL	0.33 + 0.042*SL
	t_{PHL}	0.52	0.45 + 0.033*SL	0.47 + 0.027*SL	0.48 + 0.024*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.11 + 0.041*SL	0.11 + 0.040*SL	0.10 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 ND8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.33 + 0.021*SL	0.33 + 0.021*SL	0.33 + 0.021*SL
	t_{PHL}	0.51	0.46 + 0.021*SL	0.47 + 0.016*SL	0.49 + 0.014*SL
	t_R	0.18	0.10 + 0.040*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
B to Y	t_{PLH}	0.40	0.36 + 0.021*SL	0.36 + 0.021*SL	0.36 + 0.021*SL
	t_{PHL}	0.52	0.48 + 0.021*SL	0.49 + 0.016*SL	0.51 + 0.014*SL
	t_R	0.18	0.09 + 0.041*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.18	0.14 + 0.023*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
C to Y	t_{PLH}	0.43	0.39 + 0.021*SL	0.39 + 0.021*SL	0.39 + 0.021*SL
	t_{PHL}	0.53	0.49 + 0.021*SL	0.50 + 0.016*SL	0.52 + 0.014*SL
	t_R	0.18	0.10 + 0.040*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
D to Y	t_{PLH}	0.45	0.41 + 0.021*SL	0.41 + 0.021*SL	0.41 + 0.021*SL
	t_{PHL}	0.53	0.49 + 0.021*SL	0.50 + 0.016*SL	0.52 + 0.014*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.043*SL	0.08 + 0.045*SL
	t_F	0.18	0.13 + 0.022*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
E to Y	t_{PLH}	0.48	0.44 + 0.021*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.57	0.52 + 0.021*SL	0.53 + 0.017*SL	0.55 + 0.014*SL
	t_R	0.18	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.18	0.14 + 0.022*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
F to Y	t_{PLH}	0.47	0.42 + 0.021*SL	0.43 + 0.020*SL	0.42 + 0.021*SL
	t_{PHL}	0.57	0.52 + 0.021*SL	0.54 + 0.017*SL	0.55 + 0.014*SL
	t_R	0.18	0.10 + 0.043*SL	0.10 + 0.043*SL	0.09 + 0.045*SL
	t_F	0.18	0.14 + 0.022*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
G to Y	t_{PLH}	0.43	0.39 + 0.021*SL	0.39 + 0.021*SL	0.39 + 0.021*SL
	t_{PHL}	0.55	0.51 + 0.021*SL	0.52 + 0.016*SL	0.54 + 0.014*SL
	t_R	0.18	0.10 + 0.042*SL	0.09 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.18	0.14 + 0.023*SL	0.14 + 0.020*SL	0.15 + 0.020*SL
H to Y	t_{PLH}	0.40	0.36 + 0.021*SL	0.36 + 0.021*SL	0.36 + 0.021*SL
	t_{PHL}	0.54	0.50 + 0.021*SL	0.51 + 0.016*SL	0.53 + 0.014*SL
	t_R	0.18	0.10 + 0.040*SL	0.09 + 0.043*SL	0.08 + 0.045*SL
	t_F	0.18	0.14 + 0.022*SL	0.14 + 0.021*SL	0.14 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 ND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.52	0.42 + 0.051*SL	0.42 + 0.050*SL	0.42 + 0.050*SL
	t_{PHL}	0.67	0.59 + 0.037*SL	0.62 + 0.028*SL	0.66 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
B to Y	t_{PLH}	0.56	0.46 + 0.050*SL	0.46 + 0.050*SL	0.46 + 0.050*SL
	t_{PHL}	0.70	0.62 + 0.038*SL	0.65 + 0.028*SL	0.69 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.14 + 0.045*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
C to Y	t_{PLH}	0.61	0.51 + 0.051*SL	0.51 + 0.050*SL	0.51 + 0.050*SL
	t_{PHL}	0.73	0.66 + 0.038*SL	0.68 + 0.028*SL	0.72 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
D to Y	t_{PLH}	0.63	0.53 + 0.050*SL	0.53 + 0.050*SL	0.53 + 0.050*SL
	t_{PHL}	0.74	0.66 + 0.038*SL	0.69 + 0.028*SL	0.73 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
E to Y	t_{PLH}	0.68	0.58 + 0.050*SL	0.58 + 0.050*SL	0.58 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.038*SL	0.76 + 0.028*SL	0.80 + 0.024*SL
	t_R	0.34	0.14 + 0.105*SL	0.12 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.23	0.15 + 0.045*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
F to Y	t_{PLH}	0.66	0.55 + 0.050*SL	0.55 + 0.050*SL	0.56 + 0.050*SL
	t_{PHL}	0.80	0.72 + 0.038*SL	0.75 + 0.028*SL	0.79 + 0.024*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.24	0.14 + 0.046*SL	0.16 + 0.042*SL	0.15 + 0.042*SL
G to Y	t_{PLH}	0.61	0.51 + 0.051*SL	0.51 + 0.050*SL	0.51 + 0.050*SL
	t_{PHL}	0.76	0.69 + 0.038*SL	0.72 + 0.028*SL	0.76 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
H to Y	t_{PLH}	0.57	0.46 + 0.051*SL	0.47 + 0.050*SL	0.47 + 0.050*SL
	t_{PHL}	0.74	0.66 + 0.038*SL	0.69 + 0.028*SL	0.73 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.042*SL	0.15 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Switching Characteristics

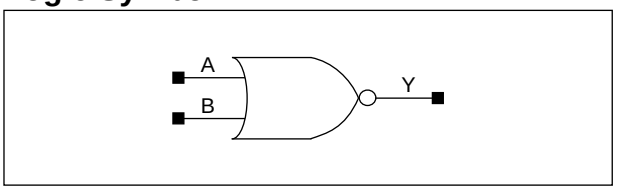
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 ND8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.50	0.45 + 0.026*SL	0.45 + 0.025*SL	0.46 + 0.025*SL
	t_{PHL}	0.72	0.68 + 0.025*SL	0.69 + 0.018*SL	0.73 + 0.014*SL
	t_R	0.24	0.13 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.23	0.17 + 0.025*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
B to Y	t_{PLH}	0.55	0.50 + 0.026*SL	0.50 + 0.025*SL	0.50 + 0.025*SL
	t_{PHL}	0.75	0.70 + 0.025*SL	0.72 + 0.018*SL	0.76 + 0.014*SL
	t_R	0.24	0.14 + 0.050*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.23	0.17 + 0.026*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
C to Y	t_{PLH}	0.60	0.55 + 0.026*SL	0.55 + 0.025*SL	0.55 + 0.025*SL
	t_{PHL}	0.79	0.74 + 0.024*SL	0.76 + 0.018*SL	0.80 + 0.014*SL
	t_R	0.24	0.13 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.23	0.17 + 0.025*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
D to Y	t_{PLH}	0.62	0.57 + 0.026*SL	0.57 + 0.025*SL	0.57 + 0.025*SL
	t_{PHL}	0.79	0.74 + 0.025*SL	0.76 + 0.018*SL	0.80 + 0.014*SL
	t_R	0.24	0.14 + 0.050*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.23	0.18 + 0.025*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
E to Y	t_{PLH}	0.67	0.62 + 0.026*SL	0.62 + 0.025*SL	0.62 + 0.025*SL
	t_{PHL}	0.86	0.81 + 0.025*SL	0.83 + 0.018*SL	0.87 + 0.014*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.23	0.18 + 0.026*SL	0.19 + 0.022*SL	0.21 + 0.021*SL
F to Y	t_{PLH}	0.64	0.59 + 0.026*SL	0.59 + 0.025*SL	0.60 + 0.025*SL
	t_{PHL}	0.86	0.81 + 0.025*SL	0.83 + 0.018*SL	0.87 + 0.014*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.23	0.18 + 0.026*SL	0.19 + 0.022*SL	0.21 + 0.021*SL
G to Y	t_{PLH}	0.59	0.54 + 0.026*SL	0.55 + 0.025*SL	0.55 + 0.025*SL
	t_{PHL}	0.82	0.77 + 0.025*SL	0.79 + 0.018*SL	0.83 + 0.014*SL
	t_R	0.24	0.14 + 0.052*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.23	0.18 + 0.026*SL	0.19 + 0.022*SL	0.21 + 0.021*SL
H to Y	t_{PLH}	0.55	0.50 + 0.026*SL	0.50 + 0.025*SL	0.50 + 0.025*SL
	t_{PHL}	0.79	0.74 + 0.025*SL	0.76 + 0.018*SL	0.80 + 0.014*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.23	0.18 + 0.026*SL	0.19 + 0.022*SL	0.21 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Cell Data

Input Load (SL)				Gate Count	
KG80					
NR2		*NR2D2*		*NR2*	*NR2D2*
A	B	A	B		
0.5	0.7	1.1	1.5	1.0	2.0
KGM80					
NR2		*NR2D2*		*NR2*	*NR2D2*
A	B	A	B		
1.0	1.0	2.1	1.9	1.0	2.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.17 + 0.068*SL	0.17 + 0.069*SL	0.16 + 0.070*SL
	t_{PHL}	0.10	0.02 + 0.040*SL	0.05 + 0.027*SL	0.08 + 0.023*SL
	t_R	0.51	0.20 + 0.154*SL	0.19 + 0.159*SL	0.16 + 0.163*SL
	t_F	0.22	0.14 + 0.040*SL	0.15 + 0.036*SL	0.13 + 0.038*SL
B to Y	t_{PLH}	0.31	0.17 + 0.068*SL	0.17 + 0.069*SL	0.16 + 0.071*SL
	t_{PHL}	0.12	0.05 + 0.037*SL	0.07 + 0.026*SL	0.09 + 0.023*SL
	t_R	0.51	0.21 + 0.152*SL	0.19 + 0.159*SL	0.17 + 0.162*SL
	t_F	0.25	0.18 + 0.036*SL	0.17 + 0.037*SL	0.17 + 0.038*SL

KG80 NR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.16 + 0.036*SL	0.17 + 0.033*SL	0.16 + 0.034*SL
	t_{PHL}	0.06	0.01 + 0.024*SL	0.03 + 0.017*SL	0.05 + 0.014*SL
	t_R	0.34	0.19 + 0.074*SL	0.19 + 0.077*SL	0.17 + 0.080*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.020*SL	0.16 + 0.017*SL
B to Y	t_{PLH}	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.035*SL
	t_{PHL}	0.08	0.04 + 0.022*SL	0.06 + 0.016*SL	0.07 + 0.013*SL
	t_R	0.35	0.20 + 0.073*SL	0.19 + 0.077*SL	0.17 + 0.080*SL
	t_F	0.22	0.17 + 0.022*SL	0.17 + 0.021*SL	0.21 + 0.015*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NR2

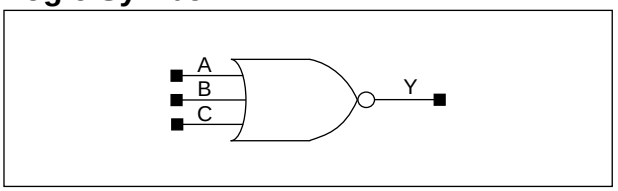
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.39	0.21 + 0.092*SL	0.21 + 0.093*SL	0.20 + 0.094*SL
	t_{PHL}	0.13	0.05 + 0.037*SL	0.08 + 0.026*SL	0.11 + 0.023*SL
	t_R	0.69	0.28 + 0.201*SL	0.27 + 0.206*SL	0.24 + 0.208*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.039*SL	0.12 + 0.041*SL
B to Y	t_{PLH}	0.42	0.23 + 0.094*SL	0.23 + 0.094*SL	0.23 + 0.094*SL
	t_{PHL}	0.15	0.08 + 0.035*SL	0.10 + 0.025*SL	0.13 + 0.023*SL
	t_R	0.69	0.29 + 0.200*SL	0.27 + 0.206*SL	0.25 + 0.208*SL
	t_F	0.25	0.17 + 0.041*SL	0.17 + 0.039*SL	0.14 + 0.041*SL

KGM80 NR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.18 + 0.049*SL	0.19 + 0.046*SL	0.18 + 0.047*SL
	t_{PHL}	0.08	0.04 + 0.023*SL	0.05 + 0.016*SL	0.09 + 0.012*SL
	t_R	0.46	0.26 + 0.099*SL	0.25 + 0.102*SL	0.24 + 0.103*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.020*SL	0.13 + 0.019*SL
B to Y	t_{PLH}	0.33	0.23 + 0.050*SL	0.24 + 0.047*SL	0.24 + 0.047*SL
	t_{PHL}	0.11	0.07 + 0.021*SL	0.08 + 0.015*SL	0.12 + 0.012*SL
	t_R	0.47	0.27 + 0.096*SL	0.26 + 0.101*SL	0.24 + 0.103*SL
	t_F	0.21	0.17 + 0.022*SL	0.18 + 0.019*SL	0.17 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
1	x	x	0
x	1	x	0
x	x	1	0

Cell Data

Input Load (SL)						Gate Count	
KG80							
NR3			*NR3D2*			*NR3*	*NR3D2*
A	B	C	A	B	C		
0.5	0.7	0.7	1.0	1.4	0.14	2.0	3.0
KGM80							
NR3			*NR3D2*			*NR3*	*NR3D2*
A	B	C	A	B	C		
1.0	1.0	1.0	2.1	2.0	1.9	2.0	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.47	0.28 + 0.097*SL	0.27 + 0.100*SL	0.26 + 0.101*SL
	t_{PHL}	0.13	0.07 + 0.033*SL	0.09 + 0.025*SL	0.10 + 0.023*SL
	t_R	0.97	0.51 + 0.232*SL	0.50 + 0.236*SL	0.49 + 0.238*SL
	t_F	0.25	0.18 + 0.036*SL	0.17 + 0.038*SL	0.16 + 0.039*SL
B to Y	t_{PLH}	0.52	0.32 + 0.100*SL	0.32 + 0.101*SL	0.31 + 0.102*SL
	t_{PHL}	0.16	0.09 + 0.032*SL	0.11 + 0.024*SL	0.12 + 0.023*SL
	t_R	0.99	0.53 + 0.230*SL	0.52 + 0.235*SL	0.50 + 0.236*SL
	t_F	0.28	0.21 + 0.034*SL	0.21 + 0.038*SL	0.20 + 0.039*SL
C to Y	t_{PLH}	0.53	0.32 + 0.102*SL	0.32 + 0.102*SL	0.32 + 0.102*SL
	t_{PHL}	0.16	0.10 + 0.030*SL	0.11 + 0.026*SL	0.12 + 0.024*SL
	t_R	0.99	0.52 + 0.231*SL	0.51 + 0.235*SL	0.50 + 0.236*SL
	t_F	0.31	0.23 + 0.041*SL	0.24 + 0.036*SL	0.22 + 0.039*SL

KG80 NR3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.22 + 0.046*SL	0.22 + 0.049*SL	0.21 + 0.050*SL
	t_{PHL}	0.07	0.03 + 0.022*SL	0.04 + 0.017*SL	0.07 + 0.013*SL
	t_R	0.58	0.35 + 0.114*SL	0.35 + 0.116*SL	0.34 + 0.118*SL
	t_F	0.19	0.15 + 0.022*SL	0.15 + 0.018*SL	0.15 + 0.019*SL
B to Y	t_{PLH}	0.35	0.25 + 0.050*SL	0.25 + 0.050*SL	0.24 + 0.051*SL
	t_{PHL}	0.09	0.05 + 0.020*SL	0.06 + 0.016*SL	0.09 + 0.013*SL
	t_R	0.60	0.37 + 0.113*SL	0.37 + 0.115*SL	0.35 + 0.117*SL
	t_F	0.22	0.19 + 0.019*SL	0.19 + 0.018*SL	0.19 + 0.018*SL
C to Y	t_{PLH}	0.37	0.27 + 0.051*SL	0.27 + 0.051*SL	0.27 + 0.051*SL
	t_{PHL}	0.10	0.06 + 0.022*SL	0.07 + 0.016*SL	0.09 + 0.013*SL
	t_R	0.59	0.37 + 0.114*SL	0.36 + 0.116*SL	0.35 + 0.118*SL
	t_F	0.25	0.21 + 0.020*SL	0.21 + 0.019*SL	0.22 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.38 + 0.138*SL	0.38 + 0.138*SL	0.38 + 0.139*SL
	t_{PHL}	0.17	0.10 + 0.032*SL	0.13 + 0.024*SL	0.14 + 0.023*SL
	t_R	1.43	0.82 + 0.307*SL	0.81 + 0.309*SL	0.82 + 0.308*SL
	t_F	0.26	0.19 + 0.039*SL	0.18 + 0.040*SL	0.16 + 0.042*SL
B to Y	t_{PLH}	0.78	0.50 + 0.140*SL	0.51 + 0.140*SL	0.51 + 0.139*SL
	t_{PHL}	0.19	0.13 + 0.031*SL	0.15 + 0.024*SL	0.16 + 0.023*SL
	t_R	1.45	0.85 + 0.302*SL	0.83 + 0.307*SL	0.82 + 0.308*SL
	t_F	0.30	0.22 + 0.039*SL	0.22 + 0.039*SL	0.20 + 0.042*SL
C to Y	t_{PLH}	0.82	0.54 + 0.141*SL	0.54 + 0.140*SL	0.55 + 0.139*SL
	t_{PHL}	0.20	0.14 + 0.031*SL	0.15 + 0.025*SL	0.17 + 0.024*SL
	t_R	1.45	0.84 + 0.303*SL	0.83 + 0.307*SL	0.82 + 0.308*SL
	t_F	0.32	0.25 + 0.038*SL	0.24 + 0.040*SL	0.22 + 0.042*SL

KGM80 NR3D2

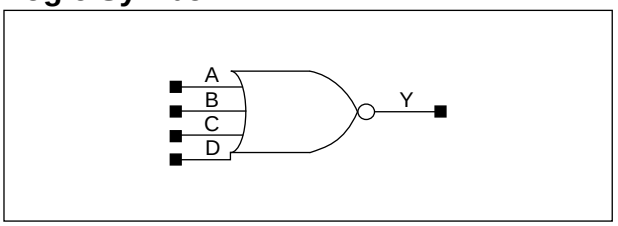
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.28 + 0.067*SL	0.27 + 0.069*SL	0.27 + 0.069*SL
	t_{PHL}	0.10	0.06 + 0.020*SL	0.07 + 0.015*SL	0.11 + 0.012*SL
	t_R	0.84	0.53 + 0.152*SL	0.53 + 0.154*SL	0.52 + 0.155*SL
	t_F	0.19	0.14 + 0.023*SL	0.15 + 0.019*SL	0.15 + 0.020*SL
B to Y	t_{PLH}	0.51	0.37 + 0.070*SL	0.37 + 0.070*SL	0.37 + 0.070*SL
	t_{PHL}	0.13	0.09 + 0.019*SL	0.10 + 0.015*SL	0.13 + 0.012*SL
	t_R	0.87	0.57 + 0.149*SL	0.56 + 0.152*SL	0.54 + 0.154*SL
	t_F	0.23	0.18 + 0.022*SL	0.19 + 0.019*SL	0.18 + 0.020*SL
C to Y	t_{PLH}	0.58	0.44 + 0.072*SL	0.44 + 0.070*SL	0.45 + 0.070*SL
	t_{PHL}	0.13	0.09 + 0.020*SL	0.10 + 0.015*SL	0.14 + 0.012*SL
	t_R	0.86	0.57 + 0.149*SL	0.56 + 0.152*SL	0.54 + 0.154*SL
	t_F	0.25	0.21 + 0.022*SL	0.22 + 0.020*SL	0.21 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

NR4/NR4D2

4-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
NR4				*NR4D2*				*NR4*	*NR4D2*
A	B	C	D	A	B	C	D		
0.5	0.7	0.7	0.7	1.1	1.3	1.4	1.5	2.0	4.0
KGM80									
NR4				*NR4D2*				*NR4*	*NR4D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	2.1	1.9	1.9	1.9	2.0	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.50	0.24 + 0.126*SL	0.23 + 0.130*SL	0.22 + 0.132*SL
	t_{PHL}	0.11	0.04 + 0.037*SL	0.07 + 0.026*SL	0.09 + 0.023*SL
	t_R	1.12	0.51 + 0.308*SL	0.50 + 0.312*SL	0.50 + 0.312*SL
	t_F	0.23	0.15 + 0.040*SL	0.16 + 0.037*SL	0.15 + 0.039*SL
B to Y	t_{PLH}	0.55	0.29 + 0.130*SL	0.29 + 0.132*SL	0.28 + 0.133*SL
	t_{PHL}	0.13	0.06 + 0.035*SL	0.08 + 0.025*SL	0.10 + 0.023*SL
	t_R	1.15	0.54 + 0.304*SL	0.53 + 0.309*SL	0.52 + 0.310*SL
	t_F	0.26	0.18 + 0.036*SL	0.18 + 0.037*SL	0.17 + 0.039*SL
C to Y	t_{PLH}	0.61	0.35 + 0.134*SL	0.35 + 0.134*SL	0.35 + 0.134*SL
	t_{PHL}	0.14	0.07 + 0.036*SL	0.09 + 0.026*SL	0.11 + 0.024*SL
	t_R	1.16	0.55 + 0.302*SL	0.54 + 0.308*SL	0.52 + 0.310*SL
	t_F	0.28	0.21 + 0.036*SL	0.21 + 0.038*SL	0.20 + 0.039*SL
D to Y	t_{PLH}	0.63	0.36 + 0.135*SL	0.36 + 0.135*SL	0.37 + 0.134*SL
	t_{PHL}	0.14	0.06 + 0.037*SL	0.09 + 0.026*SL	0.11 + 0.024*SL
	t_R	1.15	0.55 + 0.303*SL	0.53 + 0.309*SL	0.52 + 0.310*SL
	t_F	0.30	0.22 + 0.038*SL	0.22 + 0.039*SL	0.21 + 0.039*SL

KG80 NR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.23 + 0.059*SL	0.22 + 0.064*SL	0.21 + 0.065*SL
	t_{PHL}	0.07	0.03 + 0.022*SL	0.04 + 0.017*SL	0.07 + 0.013*SL
	t_R	0.80	0.50 + 0.152*SL	0.49 + 0.155*SL	0.48 + 0.157*SL
	t_F	0.19	0.14 + 0.021*SL	0.15 + 0.019*SL	0.16 + 0.018*SL
B to Y	t_{PLH}	0.43	0.29 + 0.066*SL	0.29 + 0.066*SL	0.29 + 0.066*SL
	t_{PHL}	0.10	0.06 + 0.021*SL	0.07 + 0.016*SL	0.09 + 0.012*SL
	t_R	0.85	0.55 + 0.149*SL	0.54 + 0.153*SL	0.53 + 0.155*SL
	t_F	0.22	0.19 + 0.019*SL	0.19 + 0.017*SL	0.18 + 0.020*SL
C to Y	t_{PLH}	0.48	0.34 + 0.068*SL	0.35 + 0.067*SL	0.35 + 0.067*SL
	t_{PHL}	0.10	0.06 + 0.021*SL	0.07 + 0.017*SL	0.10 + 0.012*SL
	t_R	0.85	0.56 + 0.148*SL	0.55 + 0.152*SL	0.53 + 0.154*SL
	t_F	0.25	0.21 + 0.020*SL	0.21 + 0.018*SL	0.20 + 0.019*SL
D to Y	t_{PLH}	0.50	0.36 + 0.068*SL	0.36 + 0.068*SL	0.37 + 0.067*SL
	t_{PHL}	0.10	0.06 + 0.022*SL	0.07 + 0.016*SL	0.09 + 0.013*SL
	t_R	0.85	0.55 + 0.148*SL	0.54 + 0.153*SL	0.53 + 0.154*SL
	t_F	0.26	0.21 + 0.022*SL	0.22 + 0.020*SL	0.23 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

NR4/NR4D2

4-Input NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NR4

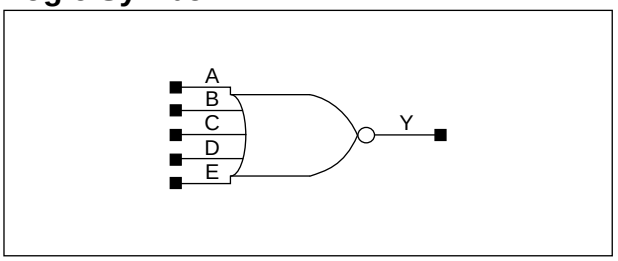
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.68	0.31 + 0.182*SL	0.31 + 0.184*SL	0.30 + 0.184*SL
	t_{PHL}	0.14	0.07 + 0.035*SL	0.10 + 0.025*SL	0.12 + 0.023*SL
	t_R	1.61	0.79 + 0.411*SL	0.79 + 0.412*SL	0.82 + 0.408*SL
	t_F	0.24	0.15 + 0.042*SL	0.16 + 0.039*SL	0.13 + 0.042*SL
B to Y	t_{PLH}	0.81	0.43 + 0.186*SL	0.43 + 0.185*SL	0.44 + 0.185*SL
	t_{PHL}	0.16	0.10 + 0.033*SL	0.12 + 0.025*SL	0.14 + 0.023*SL
	t_R	1.66	0.85 + 0.402*SL	0.84 + 0.407*SL	0.83 + 0.408*SL
	t_F	0.27	0.19 + 0.039*SL	0.19 + 0.039*SL	0.16 + 0.042*SL
C to Y	t_{PLH}	0.96	0.58 + 0.189*SL	0.59 + 0.186*SL	0.59 + 0.185*SL
	t_{PHL}	0.17	0.10 + 0.035*SL	0.13 + 0.025*SL	0.15 + 0.024*SL
	t_R	1.66	0.86 + 0.401*SL	0.85 + 0.407*SL	0.83 + 0.408*SL
	t_F	0.29	0.21 + 0.042*SL	0.22 + 0.039*SL	0.19 + 0.042*SL
D to Y	t_{PLH}	1.00	0.62 + 0.189*SL	0.63 + 0.186*SL	0.64 + 0.185*SL
	t_{PHL}	0.17	0.10 + 0.035*SL	0.12 + 0.026*SL	0.14 + 0.024*SL
	t_R	1.66	0.86 + 0.402*SL	0.85 + 0.407*SL	0.83 + 0.408*SL
	t_F	0.30	0.22 + 0.042*SL	0.22 + 0.041*SL	0.21 + 0.042*SL

KGM80 NR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.45	0.28 + 0.085*SL	0.26 + 0.091*SL	0.25 + 0.092*SL
	t_{PHL}	0.10	0.06 + 0.020*SL	0.07 + 0.015*SL	0.11 + 0.012*SL
	t_R	1.16	0.75 + 0.206*SL	0.75 + 0.207*SL	0.75 + 0.207*SL
	t_F	0.19	0.14 + 0.023*SL	0.15 + 0.020*SL	0.15 + 0.020*SL
B to Y	t_{PLH}	0.64	0.45 + 0.095*SL	0.46 + 0.093*SL	0.46 + 0.093*SL
	t_{PHL}	0.13	0.09 + 0.019*SL	0.10 + 0.015*SL	0.13 + 0.012*SL
	t_R	1.25	0.85 + 0.198*SL	0.84 + 0.202*SL	0.83 + 0.204*SL
	t_F	0.23	0.19 + 0.022*SL	0.19 + 0.019*SL	0.19 + 0.020*SL
C to Y	t_{PLH}	0.77	0.58 + 0.096*SL	0.58 + 0.094*SL	0.59 + 0.093*SL
	t_{PHL}	0.13	0.09 + 0.020*SL	0.11 + 0.015*SL	0.14 + 0.012*SL
	t_R	1.26	0.86 + 0.198*SL	0.85 + 0.202*SL	0.83 + 0.204*SL
	t_F	0.25	0.21 + 0.022*SL	0.22 + 0.020*SL	0.21 + 0.020*SL
D to Y	t_{PLH}	0.82	0.62 + 0.096*SL	0.63 + 0.094*SL	0.64 + 0.093*SL
	t_{PHL}	0.13	0.09 + 0.020*SL	0.10 + 0.015*SL	0.14 + 0.012*SL
	t_R	1.25	0.86 + 0.198*SL	0.85 + 0.202*SL	0.83 + 0.204*SL
	t_F	0.26	0.22 + 0.022*SL	0.22 + 0.020*SL	0.22 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	1
1	x	x	x	x	0
x	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0

Cell Data

Input Load (SL)										Gate Count	
KG80											
NR5					*NR5D2*					*NR5*	*NR5D2*
A	B	C	D	E	A	B	C	D	E		
0.5	0.7	0.7	0.6	0.8	0.5	08	0.9	0.9	0.9	4.0	5.0
KGM80											
NR5					*NR5D2*					*NR5*	*NR5D2*
A	B	C	D	E	A	B	C	D	E		
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	4.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.49 + 0.043*SL	0.49 + 0.041*SL	0.49 + 0.042*SL
	t_{PHL}	0.27	0.21 + 0.028*SL	0.22 + 0.024*SL	0.23 + 0.023*SL
	t_R	0.28	0.11 + 0.087*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.15	0.08 + 0.038*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
B to Y	t_{PLH}	0.60	0.51 + 0.043*SL	0.51 + 0.042*SL	0.51 + 0.042*SL
	t_{PHL}	0.29	0.24 + 0.028*SL	0.25 + 0.024*SL	0.25 + 0.023*SL
	t_R	0.28	0.11 + 0.087*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.15	0.08 + 0.037*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
C to Y	t_{PLH}	0.62	0.53 + 0.043*SL	0.54 + 0.041*SL	0.53 + 0.042*SL
	t_{PHL}	0.31	0.25 + 0.028*SL	0.26 + 0.024*SL	0.27 + 0.023*SL
	t_R	0.28	0.10 + 0.087*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.15	0.07 + 0.039*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
D to Y	t_{PLH}	0.49	0.40 + 0.043*SL	0.40 + 0.042*SL	0.40 + 0.042*SL
	t_{PHL}	0.28	0.22 + 0.030*SL	0.23 + 0.024*SL	0.24 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to Y	t_{PLH}	0.48	0.40 + 0.043*SL	0.40 + 0.042*SL	0.40 + 0.042*SL
	t_{PHL}	0.31	0.25 + 0.030*SL	0.26 + 0.024*SL	0.27 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 NR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.54	0.49 + 0.026*SL	0.50 + 0.022*SL	0.51 + 0.021*SL
	t_{PHL}	0.27	0.23 + 0.019*SL	0.24 + 0.015*SL	0.26 + 0.013*SL
	t_R	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.043*SL
	t_F	0.12	0.08 + 0.022*SL	0.08 + 0.020*SL	0.08 + 0.020*SL
B to Y	t_{PLH}	0.54	0.49 + 0.026*SL	0.50 + 0.022*SL	0.51 + 0.021*SL
	t_{PHL}	0.29	0.26 + 0.019*SL	0.27 + 0.015*SL	0.28 + 0.013*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.13	0.08 + 0.021*SL	0.09 + 0.020*SL	0.08 + 0.020*SL
C to Y	t_{PLH}	0.55	0.50 + 0.026*SL	0.51 + 0.022*SL	0.52 + 0.021*SL
	t_{PHL}	0.29	0.25 + 0.021*SL	0.27 + 0.015*SL	0.28 + 0.013*SL
	t_R	0.20	0.12 + 0.041*SL	0.12 + 0.043*SL	0.11 + 0.043*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
D to Y	t_{PLH}	0.55	0.50 + 0.026*SL	0.51 + 0.022*SL	0.52 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.020*SL	0.29 + 0.015*SL	0.31 + 0.013*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.043*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
E to Y	t_{PLH}	0.49	0.44 + 0.026*SL	0.45 + 0.023*SL	0.46 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.022*SL	0.29 + 0.016*SL	0.31 + 0.014*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.042*SL	0.11 + 0.044*SL
	t_F	0.15	0.11 + 0.023*SL	0.11 + 0.020*SL	0.12 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.80	0.69 + 0.052*SL	0.70 + 0.050*SL	0.70 + 0.050*SL
	t_{PHL}	0.38	0.32 + 0.030*SL	0.33 + 0.024*SL	0.34 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.18	0.09 + 0.043*SL	0.09 + 0.042*SL	0.08 + 0.043*SL
B to Y	t_{PLH}	0.87	0.77 + 0.052*SL	0.77 + 0.050*SL	0.78 + 0.050*SL
	t_{PHL}	0.40	0.34 + 0.030*SL	0.36 + 0.024*SL	0.37 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.18	0.09 + 0.042*SL	0.09 + 0.042*SL	0.08 + 0.043*SL
C to Y	t_{PLH}	0.94	0.83 + 0.052*SL	0.84 + 0.050*SL	0.84 + 0.050*SL
	t_{PHL}	0.41	0.35 + 0.030*SL	0.37 + 0.024*SL	0.38 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.042*SL	0.08 + 0.043*SL
D to Y	t_{PLH}	0.65	0.55 + 0.052*SL	0.55 + 0.050*SL	0.56 + 0.050*SL
	t_{PHL}	0.40	0.33 + 0.031*SL	0.35 + 0.025*SL	0.37 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.19	0.11 + 0.041*SL	0.10 + 0.041*SL	0.09 + 0.043*SL
E to Y	t_{PLH}	0.67	0.57 + 0.053*SL	0.58 + 0.050*SL	0.58 + 0.050*SL
	t_{PHL}	0.42	0.36 + 0.031*SL	0.38 + 0.025*SL	0.39 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.19	0.10 + 0.041*SL	0.11 + 0.041*SL	0.09 + 0.043*SL

KGM80 NR5D2

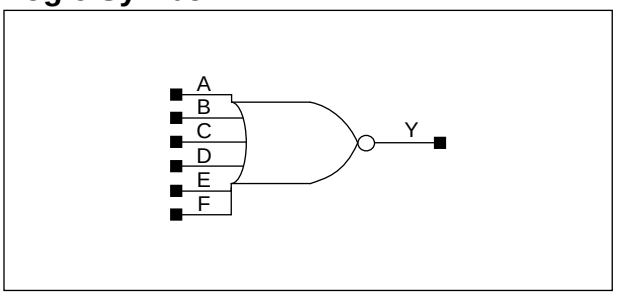
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.74	0.67 + 0.033*SL	0.69 + 0.027*SL	0.71 + 0.025*SL
	t_{PHL}	0.39	0.35 + 0.022*SL	0.36 + 0.016*SL	0.40 + 0.013*SL
	t_R	0.26	0.15 + 0.055*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.021*SL	0.12 + 0.021*SL
B to Y	t_{PLH}	0.76	0.69 + 0.033*SL	0.71 + 0.027*SL	0.73 + 0.025*SL
	t_{PHL}	0.42	0.37 + 0.022*SL	0.39 + 0.016*SL	0.42 + 0.013*SL
	t_R	0.26	0.15 + 0.054*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.15	0.10 + 0.026*SL	0.11 + 0.021*SL	0.12 + 0.021*SL
C to Y	t_{PLH}	0.75	0.69 + 0.033*SL	0.70 + 0.027*SL	0.73 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.024*SL	0.40 + 0.016*SL	0.44 + 0.013*SL
	t_R	0.26	0.15 + 0.056*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.16	0.12 + 0.024*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
D to Y	t_{PLH}	0.78	0.71 + 0.033*SL	0.72 + 0.028*SL	0.75 + 0.025*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.43 + 0.016*SL	0.46 + 0.013*SL
	t_R	0.26	0.15 + 0.056*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
E to Y	t_{PLH}	0.66	0.59 + 0.033*SL	0.61 + 0.028*SL	0.63 + 0.025*SL
	t_{PHL}	0.46	0.41 + 0.025*SL	0.43 + 0.017*SL	0.47 + 0.013*SL
	t_R	0.26	0.15 + 0.056*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

NR6/NR6D2

6-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
1	x	x	x	x	x	0
x	1	x	x	x	x	0
x	x	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0

Cell Data

Input Load (SL)												Gate Count	
KG80													
NR6						*NR6D2*						*NR6*	*NR6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.6	0.8	0.9	0.9	0.9	0.9	0.6	0.8	0.9	0.9	0.9	0.9	5.0	6.0
KGM80													
NR6						*NR6D2*						*NR6*	*NR6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	5.0	6.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NR6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.54	0.45 + 0.045*SL	0.46 + 0.042*SL	0.46 + 0.042*SL
	t_{PHL}	0.27	0.22 + 0.028*SL	0.22 + 0.025*SL	0.23 + 0.023*SL
	t_R	0.29	0.12 + 0.086*SL	0.12 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.16	0.08 + 0.039*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
B to Y	t_{PLH}	0.54	0.45 + 0.045*SL	0.46 + 0.042*SL	0.46 + 0.042*SL
	t_{PHL}	0.30	0.24 + 0.030*SL	0.25 + 0.025*SL	0.26 + 0.023*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.16	0.08 + 0.039*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
C to Y	t_{PLH}	0.56	0.47 + 0.045*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.30	0.24 + 0.031*SL	0.25 + 0.025*SL	0.27 + 0.023*SL
	t_R	0.29	0.12 + 0.086*SL	0.12 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
D to Y	t_{PLH}	0.56	0.47 + 0.045*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.33	0.26 + 0.031*SL	0.28 + 0.025*SL	0.29 + 0.023*SL
	t_R	0.29	0.12 + 0.086*SL	0.12 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.17	0.09 + 0.038*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
E to Y	t_{PLH}	0.57	0.48 + 0.045*SL	0.49 + 0.042*SL	0.49 + 0.041*SL
	t_{PHL}	0.33	0.26 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.023*SL
	t_R	0.29	0.12 + 0.086*SL	0.11 + 0.088*SL	0.11 + 0.089*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.10 + 0.041*SL
F to Y	t_{PLH}	0.57	0.48 + 0.045*SL	0.49 + 0.042*SL	0.49 + 0.041*SL
	t_{PHL}	0.35	0.29 + 0.033*SL	0.30 + 0.026*SL	0.32 + 0.024*SL
	t_R	0.29	0.12 + 0.086*SL	0.12 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.11 + 0.040*SL	0.10 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NR6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.56	0.52 + 0.021*SL	0.53 + 0.017*SL	0.54 + 0.015*SL
	t_{PHL}	0.32	0.28 + 0.018*SL	0.29 + 0.015*SL	0.31 + 0.013*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.028*SL	0.14 + 0.028*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
B to Y	t_{PLH}	0.56	0.51 + 0.021*SL	0.52 + 0.017*SL	0.54 + 0.015*SL
	t_{PHL}	0.35	0.31 + 0.019*SL	0.32 + 0.015*SL	0.33 + 0.013*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
C to Y	t_{PLH}	0.57	0.53 + 0.021*SL	0.54 + 0.017*SL	0.55 + 0.015*SL
	t_{PHL}	0.35	0.31 + 0.019*SL	0.32 + 0.015*SL	0.34 + 0.013*SL
	t_R	0.20	0.15 + 0.028*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.16	0.12 + 0.021*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
D to Y	t_{PLH}	0.57	0.53 + 0.021*SL	0.54 + 0.017*SL	0.55 + 0.015*SL
	t_{PHL}	0.37	0.33 + 0.019*SL	0.34 + 0.015*SL	0.36 + 0.013*SL
	t_R	0.20	0.15 + 0.027*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.019*SL	0.12 + 0.020*SL
E to Y	t_{PLH}	0.59	0.54 + 0.021*SL	0.55 + 0.017*SL	0.56 + 0.015*SL
	t_{PHL}	0.38	0.34 + 0.021*SL	0.35 + 0.016*SL	0.37 + 0.014*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.028*SL	0.14 + 0.028*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.019*SL	0.14 + 0.019*SL
F to Y	t_{PLH}	0.58	0.54 + 0.021*SL	0.55 + 0.017*SL	0.56 + 0.015*SL
	t_{PHL}	0.40	0.36 + 0.021*SL	0.37 + 0.016*SL	0.39 + 0.014*SL
	t_R	0.20	0.15 + 0.027*SL	0.14 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.18	0.14 + 0.022*SL	0.14 + 0.019*SL	0.14 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NR6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.74	0.63 + 0.056*SL	0.64 + 0.051*SL	0.65 + 0.050*SL
	t_{PHL}	0.38	0.32 + 0.032*SL	0.34 + 0.025*SL	0.36 + 0.023*SL
	t_R	0.38	0.17 + 0.104*SL	0.17 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.19	0.10 + 0.044*SL	0.10 + 0.042*SL	0.09 + 0.043*SL
B to Y	t_{PLH}	0.76	0.65 + 0.056*SL	0.66 + 0.051*SL	0.68 + 0.050*SL
	t_{PHL}	0.41	0.35 + 0.032*SL	0.36 + 0.025*SL	0.39 + 0.023*SL
	t_R	0.38	0.17 + 0.105*SL	0.17 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.19	0.10 + 0.042*SL	0.10 + 0.042*SL	0.09 + 0.043*SL
C to Y	t_{PLH}	0.76	0.65 + 0.056*SL	0.67 + 0.051*SL	0.68 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.034*SL	0.38 + 0.026*SL	0.41 + 0.023*SL
	t_R	0.38	0.18 + 0.104*SL	0.17 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.10 + 0.042*SL
D to Y	t_{PLH}	0.79	0.67 + 0.056*SL	0.69 + 0.051*SL	0.70 + 0.050*SL
	t_{PHL}	0.45	0.39 + 0.034*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.38	0.18 + 0.103*SL	0.17 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.10 + 0.042*SL
E to Y	t_{PLH}	0.78	0.67 + 0.056*SL	0.68 + 0.051*SL	0.69 + 0.050*SL
	t_{PHL}	0.47	0.40 + 0.036*SL	0.42 + 0.026*SL	0.46 + 0.023*SL
	t_R	0.38	0.18 + 0.104*SL	0.17 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.040*SL	0.12 + 0.042*SL
F to Y	t_{PLH}	0.80	0.69 + 0.057*SL	0.71 + 0.051*SL	0.72 + 0.050*SL
	t_{PHL}	0.50	0.42 + 0.036*SL	0.45 + 0.026*SL	0.48 + 0.023*SL
	t_R	0.38	0.18 + 0.104*SL	0.17 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.040*SL	0.13 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Switching Characteristics

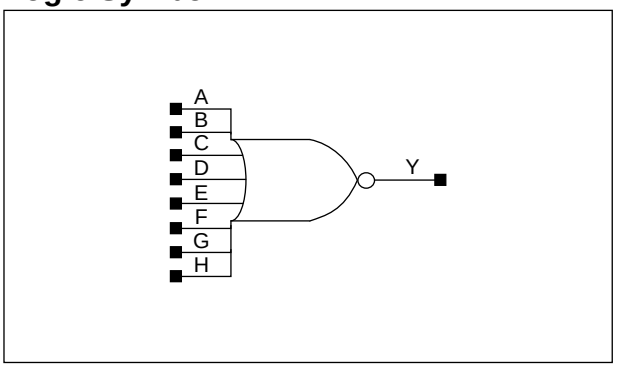
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NR6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.76	0.71 + 0.025*SL	0.73 + 0.020*SL	0.76 + 0.018*SL
	t_{PHL}	0.46	0.42 + 0.022*SL	0.43 + 0.016*SL	0.46 + 0.013*SL
	t_R	0.25	0.17 + 0.037*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
B to Y	t_{PLH}	0.79	0.74 + 0.025*SL	0.75 + 0.020*SL	0.78 + 0.018*SL
	t_{PHL}	0.48	0.44 + 0.022*SL	0.46 + 0.016*SL	0.49 + 0.013*SL
	t_R	0.25	0.17 + 0.037*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
C to Y	t_{PLH}	0.78	0.73 + 0.025*SL	0.75 + 0.020*SL	0.78 + 0.018*SL
	t_{PHL}	0.50	0.46 + 0.023*SL	0.47 + 0.017*SL	0.51 + 0.013*SL
	t_R	0.25	0.18 + 0.037*SL	0.18 + 0.035*SL	0.19 + 0.034*SL
	t_F	0.19	0.15 + 0.025*SL	0.15 + 0.021*SL	0.17 + 0.020*SL
D to Y	t_{PLH}	0.81	0.76 + 0.025*SL	0.77 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.53	0.48 + 0.023*SL	0.50 + 0.017*SL	0.53 + 0.013*SL
	t_R	0.25	0.18 + 0.037*SL	0.18 + 0.035*SL	0.19 + 0.034*SL
	t_F	0.19	0.15 + 0.025*SL	0.15 + 0.021*SL	0.17 + 0.020*SL
E to Y	t_{PLH}	0.80	0.75 + 0.025*SL	0.77 + 0.020*SL	0.80 + 0.018*SL
	t_{PHL}	0.54	0.50 + 0.024*SL	0.51 + 0.017*SL	0.55 + 0.014*SL
	t_R	0.25	0.18 + 0.037*SL	0.18 + 0.035*SL	0.19 + 0.035*SL
	t_F	0.21	0.16 + 0.025*SL	0.17 + 0.021*SL	0.19 + 0.020*SL
F to Y	t_{PLH}	0.83	0.78 + 0.025*SL	0.79 + 0.020*SL	0.82 + 0.018*SL
	t_{PHL}	0.57	0.52 + 0.024*SL	0.54 + 0.017*SL	0.58 + 0.014*SL
	t_R	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.19 + 0.034*SL
	t_F	0.21	0.16 + 0.025*SL	0.17 + 0.021*SL	0.19 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	0
x	x	x	1	x	x	x	x	0
x	x	x	x	1	x	x	x	0
x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	1	0

Cell Data

Input Load (SL)																Gate Count	
KG80																	
NR8								*NR8D2*								*NR8*	*NR8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.6	0.7	0.7	0.7	0.9	0.9	0.9	0.8	0.6	0.8	0.8	0.7	0.9	0.9	0.9	0.8	6.0	6.0
KGM80																	
NR8								*NR8D2*								*NR8*	*NR8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	6.0	6.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NR8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.58 + 0.042*SL	0.58 + 0.042*SL	0.58 + 0.042*SL
	t_{PHL}	0.29	0.24 + 0.026*SL	0.25 + 0.024*SL	0.25 + 0.023*SL
	t_R	0.34	0.17 + 0.086*SL	0.16 + 0.089*SL	0.15 + 0.090*SL
	t_F	0.18	0.09 + 0.041*SL	0.09 + 0.041*SL	0.08 + 0.042*SL
B to Y	t_{PLH}	0.71	0.63 + 0.043*SL	0.63 + 0.041*SL	0.63 + 0.042*SL
	t_{PHL}	0.31	0.26 + 0.026*SL	0.27 + 0.024*SL	0.27 + 0.023*SL
	t_R	0.34	0.17 + 0.086*SL	0.16 + 0.089*SL	0.15 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.042*SL	0.09 + 0.042*SL
C to Y	t_{PLH}	0.77	0.68 + 0.042*SL	0.68 + 0.042*SL	0.69 + 0.041*SL
	t_{PHL}	0.33	0.28 + 0.026*SL	0.28 + 0.024*SL	0.29 + 0.023*SL
	t_R	0.34	0.17 + 0.086*SL	0.16 + 0.089*SL	0.15 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.09 + 0.042*SL	0.09 + 0.042*SL
D to Y	t_{PLH}	0.78	0.70 + 0.042*SL	0.70 + 0.042*SL	0.70 + 0.042*SL
	t_{PHL}	0.33	0.28 + 0.026*SL	0.28 + 0.024*SL	0.29 + 0.023*SL
	t_R	0.34	0.17 + 0.086*SL	0.16 + 0.089*SL	0.15 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.09 + 0.041*SL	0.09 + 0.042*SL
E to Y	t_{PLH}	0.65	0.56 + 0.043*SL	0.57 + 0.041*SL	0.56 + 0.042*SL
	t_{PHL}	0.31	0.26 + 0.028*SL	0.27 + 0.024*SL	0.27 + 0.023*SL
	t_R	0.34	0.17 + 0.086*SL	0.16 + 0.089*SL	0.15 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.09 + 0.042*SL
F to Y	t_{PLH}	0.69	0.61 + 0.043*SL	0.61 + 0.042*SL	0.61 + 0.041*SL
	t_{PHL}	0.34	0.28 + 0.028*SL	0.29 + 0.024*SL	0.30 + 0.023*SL
	t_R	0.34	0.17 + 0.086*SL	0.16 + 0.088*SL	0.15 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.10 + 0.042*SL
G to Y	t_{PLH}	0.75	0.66 + 0.043*SL	0.67 + 0.041*SL	0.67 + 0.042*SL
	t_{PHL}	0.35	0.30 + 0.027*SL	0.31 + 0.024*SL	0.31 + 0.023*SL
	t_R	0.34	0.17 + 0.086*SL	0.16 + 0.089*SL	0.15 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.10 + 0.041*SL	0.10 + 0.042*SL
H to Y	t_{PLH}	0.77	0.68 + 0.043*SL	0.68 + 0.041*SL	0.68 + 0.042*SL
	t_{PHL}	0.35	0.30 + 0.027*SL	0.31 + 0.024*SL	0.31 + 0.023*SL
	t_R	0.34	0.17 + 0.087*SL	0.16 + 0.088*SL	0.15 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.040*SL	0.09 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NR8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.64	0.59 + 0.024*SL	0.60 + 0.021*SL	0.60 + 0.021*SL
	t_{PHL}	0.28	0.24 + 0.018*SL	0.25 + 0.014*SL	0.26 + 0.012*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
	t_F	0.12	0.08 + 0.021*SL	0.08 + 0.020*SL	0.08 + 0.020*SL
B to Y	t_{PLH}	0.69	0.64 + 0.023*SL	0.65 + 0.021*SL	0.65 + 0.021*SL
	t_{PHL}	0.30	0.26 + 0.018*SL	0.27 + 0.014*SL	0.28 + 0.012*SL
	t_R	0.19	0.11 + 0.041*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
	t_F	0.12	0.08 + 0.021*SL	0.08 + 0.020*SL	0.08 + 0.020*SL
C to Y	t_{PLH}	0.75	0.70 + 0.024*SL	0.70 + 0.021*SL	0.71 + 0.021*SL
	t_{PHL}	0.31	0.28 + 0.018*SL	0.29 + 0.014*SL	0.30 + 0.012*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
	t_F	0.12	0.08 + 0.021*SL	0.08 + 0.020*SL	0.08 + 0.020*SL
D to Y	t_{PLH}	0.76	0.71 + 0.024*SL	0.72 + 0.021*SL	0.73 + 0.021*SL
	t_{PHL}	0.31	0.28 + 0.018*SL	0.29 + 0.014*SL	0.30 + 0.012*SL
	t_R	0.19	0.11 + 0.041*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.12	0.08 + 0.022*SL	0.08 + 0.020*SL	0.09 + 0.019*SL
E to Y	t_{PLH}	0.62	0.57 + 0.024*SL	0.57 + 0.022*SL	0.58 + 0.021*SL
	t_{PHL}	0.29	0.26 + 0.019*SL	0.27 + 0.015*SL	0.28 + 0.013*SL
	t_R	0.19	0.11 + 0.041*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
F to Y	t_{PLH}	0.66	0.61 + 0.025*SL	0.62 + 0.022*SL	0.63 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.020*SL	0.29 + 0.015*SL	0.31 + 0.013*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.042*SL	0.10 + 0.044*SL
	t_F	0.13	0.09 + 0.023*SL	0.09 + 0.019*SL	0.09 + 0.020*SL
G to Y	t_{PLH}	0.72	0.67 + 0.024*SL	0.68 + 0.022*SL	0.68 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.019*SL	0.30 + 0.015*SL	0.32 + 0.013*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.042*SL	0.10 + 0.043*SL
	t_F	0.13	0.09 + 0.022*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
H to Y	t_{PLH}	0.73	0.69 + 0.024*SL	0.69 + 0.022*SL	0.70 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.019*SL	0.31 + 0.015*SL	0.32 + 0.013*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.042*SL	0.10 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NR8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.94	0.84 + 0.051*SL	0.84 + 0.050*SL	0.84 + 0.050*SL
	t_{PHL}	0.41	0.35 + 0.027*SL	0.36 + 0.024*SL	0.37 + 0.023*SL
	t_R	0.46	0.25 + 0.103*SL	0.24 + 0.107*SL	0.22 + 0.109*SL
	t_F	0.21	0.13 + 0.040*SL	0.13 + 0.042*SL	0.11 + 0.043*SL
B to Y	t_{PLH}	1.06	0.96 + 0.051*SL	0.96 + 0.050*SL	0.96 + 0.050*SL
	t_{PHL}	0.43	0.38 + 0.027*SL	0.39 + 0.024*SL	0.40 + 0.023*SL
	t_R	0.46	0.25 + 0.104*SL	0.24 + 0.107*SL	0.22 + 0.109*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.042*SL	0.11 + 0.043*SL
C to Y	t_{PLH}	1.21	1.11 + 0.051*SL	1.11 + 0.050*SL	1.11 + 0.050*SL
	t_{PHL}	0.45	0.39 + 0.028*SL	0.40 + 0.024*SL	0.41 + 0.023*SL
	t_R	0.46	0.25 + 0.104*SL	0.24 + 0.107*SL	0.22 + 0.109*SL
	t_F	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.11 + 0.043*SL
D to Y	t_{PLH}	1.25	1.15 + 0.051*SL	1.15 + 0.050*SL	1.15 + 0.050*SL
	t_{PHL}	0.45	0.39 + 0.028*SL	0.40 + 0.024*SL	0.41 + 0.023*SL
	t_R	0.46	0.25 + 0.104*SL	0.24 + 0.107*SL	0.22 + 0.109*SL
	t_F	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
E to Y	t_{PLH}	0.91	0.81 + 0.051*SL	0.82 + 0.050*SL	0.82 + 0.050*SL
	t_{PHL}	0.44	0.39 + 0.029*SL	0.40 + 0.024*SL	0.41 + 0.023*SL
	t_R	0.46	0.25 + 0.104*SL	0.24 + 0.107*SL	0.22 + 0.109*SL
	t_F	0.22	0.14 + 0.042*SL	0.14 + 0.041*SL	0.12 + 0.043*SL
F to Y	t_{PLH}	1.03	0.93 + 0.052*SL	0.93 + 0.050*SL	0.94 + 0.050*SL
	t_{PHL}	0.47	0.41 + 0.029*SL	0.42 + 0.024*SL	0.44 + 0.023*SL
	t_R	0.46	0.25 + 0.104*SL	0.24 + 0.107*SL	0.22 + 0.109*SL
	t_F	0.22	0.14 + 0.041*SL	0.14 + 0.041*SL	0.12 + 0.043*SL
G to Y	t_{PLH}	1.18	1.08 + 0.052*SL	1.08 + 0.050*SL	1.08 + 0.050*SL
	t_{PHL}	0.48	0.43 + 0.029*SL	0.44 + 0.024*SL	0.45 + 0.023*SL
	t_R	0.46	0.25 + 0.103*SL	0.24 + 0.107*SL	0.23 + 0.109*SL
	t_F	0.22	0.14 + 0.041*SL	0.14 + 0.041*SL	0.13 + 0.043*SL
H to Y	t_{PLH}	1.22	1.12 + 0.052*SL	1.12 + 0.050*SL	1.12 + 0.050*SL
	t_{PHL}	0.49	0.43 + 0.029*SL	0.44 + 0.024*SL	0.45 + 0.023*SL
	t_R	0.46	0.25 + 0.104*SL	0.24 + 0.107*SL	0.23 + 0.109*SL
	t_F	0.22	0.14 + 0.041*SL	0.14 + 0.041*SL	0.12 + 0.043*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NR8D2

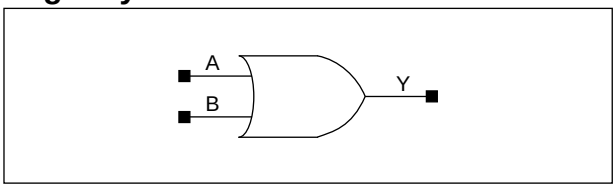
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.91	0.84 + 0.030*SL	0.86 + 0.026*SL	0.87 + 0.025*SL
	t_{PHL}	0.39	0.35 + 0.020*SL	0.37 + 0.015*SL	0.39 + 0.012*SL
	t_R	0.24	0.14 + 0.051*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.14	0.09 + 0.025*SL	0.10 + 0.021*SL	0.11 + 0.021*SL
B to Y	t_{PLH}	1.03	0.97 + 0.030*SL	0.98 + 0.026*SL	0.99 + 0.025*SL
	t_{PHL}	0.42	0.38 + 0.021*SL	0.39 + 0.015*SL	0.42 + 0.012*SL
	t_R	0.24	0.14 + 0.051*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.14	0.09 + 0.024*SL	0.10 + 0.021*SL	0.11 + 0.021*SL
C to Y	t_{PLH}	1.17	1.11 + 0.030*SL	1.13 + 0.026*SL	1.14 + 0.025*SL
	t_{PHL}	0.43	0.39 + 0.021*SL	0.41 + 0.015*SL	0.44 + 0.012*SL
	t_R	0.24	0.14 + 0.051*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.15	0.10 + 0.025*SL	0.11 + 0.021*SL	0.11 + 0.020*SL
D to Y	t_{PLH}	1.22	1.16 + 0.030*SL	1.17 + 0.026*SL	1.18 + 0.025*SL
	t_{PHL}	0.43	0.39 + 0.021*SL	0.41 + 0.015*SL	0.44 + 0.012*SL
	t_R	0.24	0.14 + 0.051*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.15	0.10 + 0.025*SL	0.11 + 0.021*SL	0.11 + 0.021*SL
E to Y	t_{PLH}	0.86	0.80 + 0.031*SL	0.82 + 0.026*SL	0.83 + 0.025*SL
	t_{PHL}	0.42	0.38 + 0.023*SL	0.40 + 0.016*SL	0.43 + 0.013*SL
	t_R	0.24	0.14 + 0.052*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.12 + 0.020*SL
F to Y	t_{PLH}	0.98	0.92 + 0.031*SL	0.94 + 0.026*SL	0.95 + 0.025*SL
	t_{PHL}	0.45	0.40 + 0.023*SL	0.42 + 0.016*SL	0.46 + 0.013*SL
	t_R	0.24	0.14 + 0.052*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.16	0.11 + 0.024*SL	0.12 + 0.021*SL	0.12 + 0.020*SL
G to Y	t_{PLH}	1.13	1.07 + 0.031*SL	1.08 + 0.026*SL	1.09 + 0.025*SL
	t_{PHL}	0.47	0.42 + 0.023*SL	0.44 + 0.016*SL	0.47 + 0.013*SL
	t_R	0.24	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
H to Y	t_{PLH}	1.17	1.11 + 0.031*SL	1.12 + 0.026*SL	1.14 + 0.025*SL
	t_{PHL}	0.47	0.42 + 0.023*SL	0.44 + 0.016*SL	0.48 + 0.013*SL
	t_R	0.24	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.16	0.11 + 0.024*SL	0.12 + 0.020*SL	0.13 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

OR2/OR2D2

2-Input OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Cell Data

Input Load (SL)				Gate Count	
KG80					
OR2		*OR2D2*		*OR2*	*OR2D2*
A	B	A	B		
0.5	0.7	0.5	0.7	2.0	2.0
KGM80					
OR2		*OR2D2*		*OR2*	*OR2D2*
A	B	A	B		
1.0	1.0	1.0	1.0	2.0	2.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.13 + 0.041*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.032*SL	0.29 + 0.027*SL	0.31 + 0.024*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.19	0.10 + 0.041*SL	0.10 + 0.041*SL	0.10 + 0.041*SL
B to Y	t_{PLH}	0.23	0.15 + 0.042*SL	0.15 + 0.041*SL	0.15 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.27	0.10 + 0.083*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.19	0.10 + 0.041*SL	0.10 + 0.041*SL	0.10 + 0.041*SL

KG80 OR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.16 + 0.021*SL	0.16 + 0.021*SL	0.16 + 0.021*SL
	t_{PHL}	0.36	0.32 + 0.020*SL	0.33 + 0.016*SL	0.34 + 0.014*SL
	t_R	0.18	0.10 + 0.043*SL	0.10 + 0.043*SL	0.09 + 0.045*SL
	t_F	0.17	0.13 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
B to Y	t_{PLH}	0.22	0.18 + 0.021*SL	0.18 + 0.021*SL	0.18 + 0.021*SL
	t_{PHL}	0.36	0.32 + 0.020*SL	0.32 + 0.016*SL	0.34 + 0.014*SL
	t_R	0.18	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.045*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.14 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

LSwitching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.18 + 0.050*SL	0.18 + 0.050*SL	0.18 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.028*SL	0.43 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.23	0.13 + 0.047*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
B to Y	t_{PLH}	0.31	0.21 + 0.051*SL	0.21 + 0.050*SL	0.21 + 0.050*SL
	t_{PHL}	0.46	0.39 + 0.037*SL	0.41 + 0.028*SL	0.45 + 0.024*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.23	0.13 + 0.047*SL	0.15 + 0.042*SL	0.15 + 0.042*SL

KGM80 OR2D2

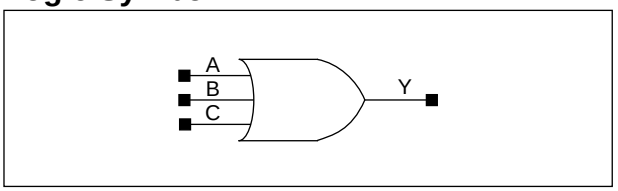
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.22 + 0.026*SL	0.22 + 0.025*SL	0.22 + 0.025*SL
	t_{PHL}	0.49	0.44 + 0.024*SL	0.46 + 0.018*SL	0.50 + 0.014*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.22	0.17 + 0.026*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
B to Y	t_{PLH}	0.29	0.24 + 0.026*SL	0.24 + 0.025*SL	0.25 + 0.025*SL
	t_{PHL}	0.51	0.46 + 0.024*SL	0.48 + 0.018*SL	0.52 + 0.014*SL
	t_R	0.24	0.14 + 0.050*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.22	0.17 + 0.025*SL	0.18 + 0.022*SL	0.19 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

OR3/OR3D3

3-Input OR with 1X/3X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
1	x	x	1
x	1	x	1
x	x	1	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
OR3			*OR3D3*			*OR3*	*OR3D3*
A	B	C	A	B	C		
0.5	0.7	0.7	0.5	0.7	0.7	2.0	3.0
KGM80							
OR3			*OR3D3*			*OR3*	*OR3D3*
A	B	C	A	B	C		
1.0	1.0	1.0	1.0	1.0	1.0	2.0	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.14 + 0.041*SL	0.14 + 0.041*SL	0.14 + 0.042*SL
	t_{PHL}	0.42	0.34 + 0.039*SL	0.36 + 0.030*SL	0.39 + 0.026*SL
	t_R	0.27	0.10 + 0.084*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.23	0.14 + 0.045*SL	0.15 + 0.042*SL	0.16 + 0.041*SL
B to Y	t_{PLH}	0.25	0.16 + 0.042*SL	0.16 + 0.041*SL	0.16 + 0.042*SL
	t_{PHL}	0.44	0.36 + 0.040*SL	0.39 + 0.030*SL	0.42 + 0.026*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.24	0.15 + 0.043*SL	0.15 + 0.042*SL	0.17 + 0.041*SL
C to Y	t_{PLH}	0.26	0.18 + 0.042*SL	0.18 + 0.041*SL	0.17 + 0.042*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.41 + 0.030*SL	0.44 + 0.026*SL
	t_R	0.27	0.11 + 0.083*SL	0.09 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.24	0.15 + 0.044*SL	0.15 + 0.042*SL	0.16 + 0.041*SL

KG80 OR3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.20 + 0.015*SL	0.20 + 0.014*SL	0.21 + 0.014*SL
	t_{PHL}	0.51	0.47 + 0.019*SL	0.48 + 0.015*SL	0.50 + 0.013*SL
	t_R	0.17	0.11 + 0.029*SL	0.11 + 0.027*SL	0.10 + 0.029*SL
	t_F	0.27	0.23 + 0.018*SL	0.23 + 0.016*SL	0.25 + 0.014*SL
B to Y	t_{PLH}	0.25	0.22 + 0.015*SL	0.23 + 0.014*SL	0.23 + 0.014*SL
	t_{PHL}	0.54	0.50 + 0.019*SL	0.51 + 0.015*SL	0.53 + 0.013*SL
	t_R	0.17	0.11 + 0.027*SL	0.11 + 0.028*SL	0.10 + 0.029*SL
	t_F	0.27	0.23 + 0.018*SL	0.24 + 0.016*SL	0.25 + 0.015*SL
C to Y	t_{PLH}	0.27	0.24 + 0.015*SL	0.24 + 0.014*SL	0.24 + 0.014*SL
	t_{PHL}	0.56	0.52 + 0.019*SL	0.53 + 0.015*SL	0.55 + 0.013*SL
	t_R	0.17	0.12 + 0.026*SL	0.12 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.27	0.23 + 0.018*SL	0.24 + 0.016*SL	0.25 + 0.014*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OR3

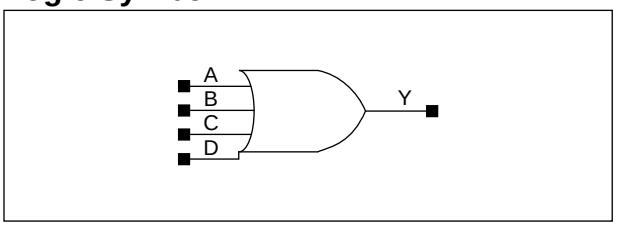
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.20 + 0.051*SL	0.20 + 0.050*SL	0.20 + 0.050*SL
	t_{PHL}	0.58	0.49 + 0.046*SL	0.52 + 0.033*SL	0.59 + 0.027*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.30	0.19 + 0.051*SL	0.21 + 0.045*SL	0.24 + 0.042*SL
B to Y	t_{PLH}	0.33	0.23 + 0.051*SL	0.23 + 0.050*SL	0.23 + 0.050*SL
	t_{PHL}	0.65	0.56 + 0.047*SL	0.60 + 0.033*SL	0.66 + 0.027*SL
	t_R	0.34	0.14 + 0.104*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.30	0.20 + 0.052*SL	0.22 + 0.044*SL	0.24 + 0.042*SL
C to Y	t_{PLH}	0.34	0.24 + 0.052*SL	0.24 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.72	0.63 + 0.046*SL	0.67 + 0.033*SL	0.73 + 0.027*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.30	0.20 + 0.052*SL	0.22 + 0.044*SL	0.24 + 0.042*SL

KGM80 OR3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.27 + 0.018*SL	0.27 + 0.017*SL	0.28 + 0.017*SL
	t_{PHL}	0.76	0.71 + 0.023*SL	0.73 + 0.018*SL	0.77 + 0.014*SL
	t_R	0.21	0.15 + 0.034*SL	0.14 + 0.035*SL	0.13 + 0.036*SL
	t_F	0.35	0.31 + 0.022*SL	0.32 + 0.018*SL	0.34 + 0.016*SL
B to Y	t_{PLH}	0.33	0.29 + 0.019*SL	0.30 + 0.017*SL	0.30 + 0.017*SL
	t_{PHL}	0.83	0.79 + 0.023*SL	0.80 + 0.018*SL	0.85 + 0.014*SL
	t_R	0.22	0.15 + 0.033*SL	0.15 + 0.035*SL	0.13 + 0.036*SL
	t_F	0.35	0.31 + 0.023*SL	0.32 + 0.018*SL	0.34 + 0.016*SL
C to Y	t_{PLH}	0.34	0.30 + 0.019*SL	0.31 + 0.017*SL	0.32 + 0.017*SL
	t_{PHL}	0.91	0.86 + 0.023*SL	0.87 + 0.018*SL	0.92 + 0.014*SL
	t_R	0.22	0.15 + 0.034*SL	0.15 + 0.035*SL	0.14 + 0.036*SL
	t_F	0.35	0.31 + 0.021*SL	0.32 + 0.018*SL	0.34 + 0.016*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Cell Data

Input Load (SL)								Gate Count	
KG80									
OR4				*OR4D2*				*OR4*	*OR4D2*
A	B	C	D	A	B	C	D		
0.6	0.7	0.6	0.8	0.6	0.7	0.6	0.8	3.0	4.0
KGM80									
OR4				*OR4D2*				*OR4*	*OR4D2*
A	B	C	D	A	B	C	D		
1.1	1.0	1.0	1.1	1.0	1.0	1.0	1.0	3.0	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
	t_{PHL}	0.38	0.29 + 0.042*SL	0.31 + 0.036*SL	0.32 + 0.034*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.25	0.12 + 0.065*SL	0.12 + 0.066*SL	0.11 + 0.067*SL
B to Y	t_{PLH}	0.24	0.15 + 0.042*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
	t_{PHL}	0.38	0.29 + 0.042*SL	0.31 + 0.036*SL	0.32 + 0.035*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.26	0.13 + 0.065*SL	0.12 + 0.066*SL	0.11 + 0.067*SL
C to Y	t_{PLH}	0.23	0.15 + 0.041*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
	t_{PHL}	0.37	0.30 + 0.039*SL	0.30 + 0.036*SL	0.31 + 0.034*SL
	t_R	0.31	0.14 + 0.085*SL	0.13 + 0.089*SL	0.12 + 0.091*SL
	t_F	0.25	0.11 + 0.066*SL	0.11 + 0.066*SL	0.10 + 0.068*SL
D to Y	t_{PLH}	0.26	0.17 + 0.041*SL	0.17 + 0.042*SL	0.17 + 0.042*SL
	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.036*SL	0.31 + 0.035*SL
	t_R	0.31	0.14 + 0.084*SL	0.13 + 0.089*SL	0.12 + 0.090*SL
	t_F	0.25	0.12 + 0.065*SL	0.11 + 0.066*SL	0.10 + 0.068*SL

KG80 OR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.17 + 0.021*SL	0.17 + 0.021*SL	0.17 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.025*SL	0.36 + 0.021*SL	0.37 + 0.019*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.043*SL	0.09 + 0.045*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.033*SL	0.16 + 0.032*SL
B to Y	t_{PLH}	0.23	0.19 + 0.021*SL	0.19 + 0.021*SL	0.19 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.025*SL	0.36 + 0.021*SL	0.37 + 0.019*SL
	t_R	0.20	0.11 + 0.041*SL	0.11 + 0.042*SL	0.09 + 0.045*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.032*SL	0.16 + 0.032*SL
C to Y	t_{PLH}	0.23	0.19 + 0.021*SL	0.19 + 0.021*SL	0.19 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.023*SL	0.36 + 0.020*SL	0.37 + 0.018*SL
	t_R	0.24	0.16 + 0.041*SL	0.16 + 0.042*SL	0.15 + 0.044*SL
	t_F	0.21	0.15 + 0.030*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
D to Y	t_{PLH}	0.26	0.21 + 0.021*SL	0.21 + 0.021*SL	0.22 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.024*SL	0.36 + 0.020*SL	0.37 + 0.018*SL
	t_R	0.25	0.16 + 0.041*SL	0.16 + 0.042*SL	0.15 + 0.044*SL
	t_F	0.22	0.15 + 0.032*SL	0.15 + 0.031*SL	0.14 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.19 + 0.051*SL	0.19 + 0.050*SL	0.19 + 0.050*SL
	t_{PHL}	0.50	0.40 + 0.050*SL	0.42 + 0.040*SL	0.45 + 0.037*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.109*SL	0.12 + 0.109*SL
	t_F	0.31	0.16 + 0.075*SL	0.17 + 0.072*SL	0.16 + 0.073*SL
B to Y	t_{PLH}	0.32	0.21 + 0.051*SL	0.22 + 0.050*SL	0.22 + 0.050*SL
	t_{PHL}	0.52	0.42 + 0.050*SL	0.45 + 0.040*SL	0.48 + 0.038*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.32	0.17 + 0.074*SL	0.17 + 0.072*SL	0.16 + 0.073*SL
C to Y	t_{PLH}	0.32	0.22 + 0.051*SL	0.22 + 0.050*SL	0.23 + 0.050*SL
	t_{PHL}	0.49	0.40 + 0.046*SL	0.42 + 0.039*SL	0.44 + 0.038*SL
	t_R	0.40	0.19 + 0.104*SL	0.18 + 0.108*SL	0.17 + 0.109*SL
	t_F	0.30	0.15 + 0.071*SL	0.15 + 0.073*SL	0.14 + 0.074*SL
D to Y	t_{PLH}	0.35	0.24 + 0.051*SL	0.25 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.046*SL	0.44 + 0.039*SL	0.46 + 0.038*SL
	t_R	0.40	0.19 + 0.104*SL	0.18 + 0.108*SL	0.17 + 0.109*SL
	t_F	0.30	0.16 + 0.071*SL	0.15 + 0.073*SL	0.14 + 0.074*SL

KGM80 OR4D2

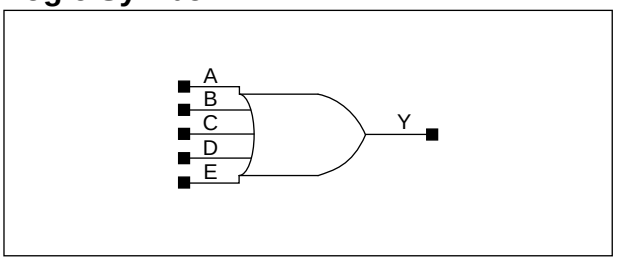
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.23 + 0.026*SL	0.23 + 0.025*SL	0.23 + 0.025*SL
	t_{PHL}	0.54	0.48 + 0.030*SL	0.50 + 0.024*SL	0.54 + 0.020*SL
	t_R	0.25	0.15 + 0.051*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.28	0.20 + 0.039*SL	0.21 + 0.036*SL	0.22 + 0.036*SL
B to Y	t_{PLH}	0.31	0.25 + 0.027*SL	0.26 + 0.025*SL	0.26 + 0.025*SL
	t_{PHL}	0.57	0.51 + 0.030*SL	0.53 + 0.024*SL	0.56 + 0.020*SL
	t_R	0.25	0.15 + 0.050*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.28	0.21 + 0.039*SL	0.21 + 0.036*SL	0.22 + 0.036*SL
C to Y	t_{PLH}	0.32	0.27 + 0.026*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_{PHL}	0.55	0.49 + 0.028*SL	0.51 + 0.023*SL	0.53 + 0.020*SL
	t_R	0.31	0.21 + 0.051*SL	0.21 + 0.053*SL	0.19 + 0.054*SL
	t_F	0.26	0.19 + 0.036*SL	0.19 + 0.036*SL	0.19 + 0.036*SL
D to Y	t_{PLH}	0.34	0.29 + 0.026*SL	0.29 + 0.025*SL	0.30 + 0.025*SL
	t_{PHL}	0.57	0.52 + 0.028*SL	0.53 + 0.023*SL	0.56 + 0.020*SL
	t_R	0.32	0.22 + 0.051*SL	0.21 + 0.053*SL	0.20 + 0.054*SL
	t_F	0.26	0.19 + 0.037*SL	0.19 + 0.036*SL	0.19 + 0.036*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

OR5/OR5D2

5-Input OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Cell Data

Input Load (SL)										Gate Count	
KG80											
OR5					*OR5D2*					*OR5*	*OR5D2*
A	B	C	D	E	A	B	C	D	E		
0.6	0.7	0.7	0.6	0.7	0.6	0.7	0.7	0.6	0.7	4.0	5.0
KGM80											
OR5					*OR5D2*					*OR5*	*OR5D2*
A	B	C	D	E	A	B	C	D	E		
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	4.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.18 + 0.042*SL	0.18 + 0.041*SL	0.17 + 0.042*SL
	t_{PHL}	0.52	0.41 + 0.053*SL	0.44 + 0.042*SL	0.47 + 0.038*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.34	0.20 + 0.069*SL	0.21 + 0.066*SL	0.21 + 0.066*SL
B to Y	t_{PLH}	0.29	0.20 + 0.043*SL	0.21 + 0.041*SL	0.20 + 0.042*SL
	t_{PHL}	0.56	0.45 + 0.053*SL	0.48 + 0.042*SL	0.51 + 0.037*SL
	t_R	0.28	0.11 + 0.087*SL	0.10 + 0.088*SL	0.08 + 0.091*SL
	t_F	0.34	0.21 + 0.067*SL	0.21 + 0.066*SL	0.21 + 0.066*SL
C to Y	t_{PLH}	0.29	0.21 + 0.042*SL	0.21 + 0.042*SL	0.21 + 0.042*SL
	t_{PHL}	0.57	0.46 + 0.053*SL	0.49 + 0.042*SL	0.52 + 0.038*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.34	0.21 + 0.067*SL	0.21 + 0.066*SL	0.21 + 0.066*SL
D to Y	t_{PLH}	0.23	0.15 + 0.042*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
	t_{PHL}	0.37	0.30 + 0.039*SL	0.30 + 0.036*SL	0.31 + 0.035*SL
	t_R	0.31	0.14 + 0.085*SL	0.13 + 0.089*SL	0.12 + 0.091*SL
	t_F	0.24	0.11 + 0.066*SL	0.11 + 0.067*SL	0.10 + 0.068*SL
E to Y	t_{PLH}	0.26	0.17 + 0.041*SL	0.17 + 0.041*SL	0.17 + 0.042*SL
	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.036*SL	0.31 + 0.035*SL
	t_R	0.31	0.14 + 0.084*SL	0.13 + 0.089*SL	0.12 + 0.090*SL
	t_F	0.25	0.12 + 0.065*SL	0.11 + 0.066*SL	0.10 + 0.068*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.21 + 0.022*SL	0.21 + 0.021*SL	0.21 + 0.021*SL
	t_{PHL}	0.54	0.48 + 0.032*SL	0.49 + 0.026*SL	0.52 + 0.022*SL
	t_R	0.20	0.11 + 0.040*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.32	0.25 + 0.036*SL	0.26 + 0.033*SL	0.26 + 0.032*SL
B to Y	t_{PLH}	0.28	0.23 + 0.022*SL	0.23 + 0.021*SL	0.24 + 0.021*SL
	t_{PHL}	0.59	0.53 + 0.032*SL	0.54 + 0.025*SL	0.57 + 0.022*SL
	t_R	0.20	0.12 + 0.041*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.33	0.26 + 0.035*SL	0.26 + 0.033*SL	0.27 + 0.032*SL
C to Y	t_{PLH}	0.28	0.24 + 0.023*SL	0.24 + 0.021*SL	0.24 + 0.021*SL
	t_{PHL}	0.60	0.53 + 0.031*SL	0.55 + 0.026*SL	0.57 + 0.022*SL
	t_R	0.20	0.12 + 0.039*SL	0.11 + 0.043*SL	0.10 + 0.045*SL
	t_F	0.33	0.25 + 0.036*SL	0.26 + 0.033*SL	0.27 + 0.032*SL
D to Y	t_{PLH}	0.23	0.19 + 0.021*SL	0.19 + 0.021*SL	0.19 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.023*SL	0.36 + 0.020*SL	0.37 + 0.018*SL
	t_R	0.24	0.16 + 0.041*SL	0.16 + 0.043*SL	0.14 + 0.044*SL
	t_F	0.21	0.15 + 0.029*SL	0.15 + 0.032*SL	0.14 + 0.033*SL
E to Y	t_{PLH}	0.26	0.21 + 0.021*SL	0.21 + 0.021*SL	0.22 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.024*SL	0.36 + 0.020*SL	0.37 + 0.018*SL
	t_R	0.25	0.16 + 0.041*SL	0.16 + 0.043*SL	0.15 + 0.044*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.032*SL	0.14 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.24 + 0.051*SL	0.25 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.72	0.59 + 0.065*SL	0.63 + 0.049*SL	0.72 + 0.041*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.43	0.27 + 0.080*SL	0.29 + 0.074*SL	0.32 + 0.072*SL
B to Y	t_{PLH}	0.38	0.28 + 0.051*SL	0.28 + 0.050*SL	0.28 + 0.050*SL
	t_{PHL}	0.84	0.71 + 0.065*SL	0.75 + 0.049*SL	0.84 + 0.041*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.44	0.27 + 0.081*SL	0.29 + 0.074*SL	0.32 + 0.072*SL
C to Y	t_{PLH}	0.39	0.28 + 0.053*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.88	0.75 + 0.065*SL	0.79 + 0.049*SL	0.87 + 0.041*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.44	0.27 + 0.081*SL	0.29 + 0.074*SL	0.32 + 0.072*SL
D to Y	t_{PLH}	0.32	0.22 + 0.051*SL	0.22 + 0.050*SL	0.22 + 0.050*SL
	t_{PHL}	0.49	0.40 + 0.046*SL	0.42 + 0.040*SL	0.44 + 0.038*SL
	t_R	0.40	0.19 + 0.105*SL	0.18 + 0.109*SL	0.17 + 0.109*SL
	t_F	0.29	0.15 + 0.072*SL	0.15 + 0.073*SL	0.14 + 0.074*SL
E to Y	t_{PLH}	0.35	0.24 + 0.051*SL	0.25 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.046*SL	0.44 + 0.040*SL	0.46 + 0.038*SL
	t_R	0.40	0.19 + 0.104*SL	0.18 + 0.108*SL	0.17 + 0.109*SL
	t_F	0.30	0.15 + 0.071*SL	0.15 + 0.073*SL	0.14 + 0.074*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OR5D2

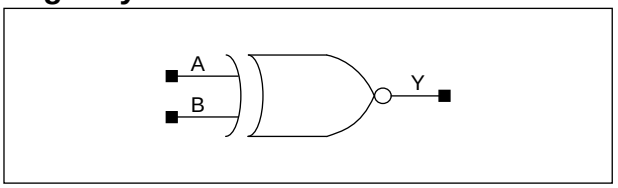
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.28 + 0.028*SL	0.28 + 0.025*SL	0.29 + 0.025*SL
	t_{PHL}	0.79	0.71 + 0.040*SL	0.73 + 0.030*SL	0.79 + 0.024*SL
	t_R	0.25	0.15 + 0.051*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.42	0.33 + 0.043*SL	0.34 + 0.039*SL	0.37 + 0.037*SL
B to Y	t_{PLH}	0.36	0.31 + 0.027*SL	0.31 + 0.025*SL	0.32 + 0.025*SL
	t_{PHL}	0.91	0.83 + 0.040*SL	0.86 + 0.030*SL	0.92 + 0.024*SL
	t_R	0.26	0.16 + 0.050*SL	0.15 + 0.053*SL	0.14 + 0.054*SL
	t_F	0.42	0.33 + 0.043*SL	0.35 + 0.038*SL	0.37 + 0.037*SL
C to Y	t_{PLH}	0.37	0.32 + 0.028*SL	0.32 + 0.026*SL	0.33 + 0.025*SL
	t_{PHL}	0.95	0.87 + 0.040*SL	0.89 + 0.030*SL	0.95 + 0.024*SL
	t_R	0.26	0.17 + 0.047*SL	0.15 + 0.053*SL	0.14 + 0.054*SL
	t_F	0.42	0.33 + 0.043*SL	0.35 + 0.038*SL	0.37 + 0.037*SL
D to Y	t_{PLH}	0.32	0.27 + 0.026*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_{PHL}	0.55	0.49 + 0.027*SL	0.50 + 0.023*SL	0.53 + 0.020*SL
	t_R	0.31	0.21 + 0.052*SL	0.21 + 0.053*SL	0.19 + 0.054*SL
	t_F	0.26	0.19 + 0.037*SL	0.19 + 0.036*SL	0.19 + 0.037*SL
E to Y	t_{PLH}	0.34	0.29 + 0.026*SL	0.29 + 0.025*SL	0.30 + 0.025*SL
	t_{PHL}	0.57	0.51 + 0.027*SL	0.53 + 0.023*SL	0.55 + 0.020*SL
	t_R	0.32	0.21 + 0.051*SL	0.21 + 0.053*SL	0.20 + 0.054*SL
	t_F	0.26	0.19 + 0.036*SL	0.19 + 0.036*SL	0.19 + 0.037*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

XN2/XN2D2

2-Input Exclusive-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)				Gate Count	
KG80					
XN2		*XN2D2*		*XN2*	*XN2D2*
A	B	A	B		
0.9	1.7	0.9	1.7	3.0	4.0
KGM80					
XN2		*XN2D2*		*XN2*	*XN2D2*
A	B	A	B		
1.0	2.0	1.0	2.0	3.0	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 XN2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.50	0.41 + 0.043*SL	0.41 + 0.041*SL	0.41 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.039*SL	0.36 + 0.030*SL	0.39 + 0.025*SL
	t_R	0.27	0.11 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.040*SL	0.15 + 0.040*SL
B to Y	t_{PLH}	0.37	0.29 + 0.043*SL	0.29 + 0.041*SL	0.29 + 0.042*SL
	t_{PHL}	0.31	0.24 + 0.033*SL	0.26 + 0.027*SL	0.28 + 0.025*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.09 + 0.044*SL	0.10 + 0.042*SL	0.10 + 0.041*SL

KG80 XN2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.44 + 0.023*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.42	0.37 + 0.024*SL	0.38 + 0.019*SL	0.40 + 0.016*SL
	t_R	0.20	0.11 + 0.042*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.21	0.15 + 0.026*SL	0.16 + 0.022*SL	0.17 + 0.020*SL
B to Y	t_{PLH}	0.36	0.32 + 0.023*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.31	0.27 + 0.021*SL	0.28 + 0.017*SL	0.30 + 0.015*SL
	t_R	0.20	0.11 + 0.042*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.16	0.11 + 0.026*SL	0.12 + 0.022*SL	0.12 + 0.021*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 XN2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.56 + 0.053*SL	0.57 + 0.050*SL	0.57 + 0.050*SL
	t_{PHL}	0.56	0.47 + 0.047*SL	0.51 + 0.031*SL	0.58 + 0.025*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.28	0.19 + 0.050*SL	0.21 + 0.042*SL	0.22 + 0.040*SL
B to Y	t_{PLH}	0.49	0.38 + 0.052*SL	0.39 + 0.050*SL	0.39 + 0.050*SL
	t_{PHL}	0.41	0.33 + 0.038*SL	0.36 + 0.029*SL	0.40 + 0.025*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.22	0.13 + 0.049*SL	0.14 + 0.043*SL	0.15 + 0.042*SL

KGM80 XN2D2

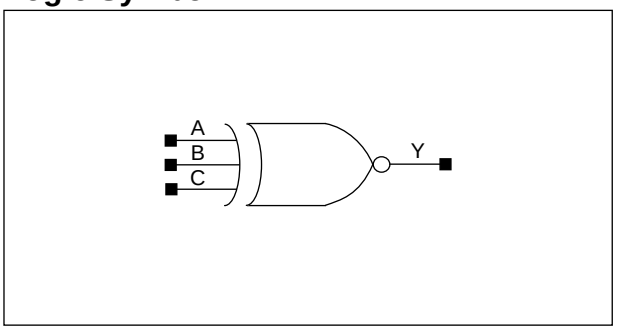
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.60 + 0.029*SL	0.61 + 0.026*SL	0.62 + 0.025*SL
	t_{PHL}	0.58	0.52 + 0.030*SL	0.54 + 0.021*SL	0.60 + 0.016*SL
	t_R	0.26	0.16 + 0.052*SL	0.15 + 0.052*SL	0.14 + 0.054*SL
	t_F	0.27	0.20 + 0.031*SL	0.22 + 0.024*SL	0.25 + 0.021*SL
B to Y	t_{PLH}	0.47	0.42 + 0.029*SL	0.43 + 0.026*SL	0.44 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.40 + 0.019*SL	0.44 + 0.015*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.052*SL	0.14 + 0.054*SL
	t_F	0.21	0.15 + 0.030*SL	0.17 + 0.024*SL	0.19 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

XN3/XN3D3

3-Input Exclusive-NOR with 1X/3X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Data

Input Load (SL)						Gate Count	
KG80							
XN3			*XN3D3*			*XN3*	*XN3D3*
A	B	C	A	B	C		
1.2	0.8	1.8	1.2	0.8	1.8	5.0	6.0
KGM80							
XN3			*XN3D3*			*XN3*	*XN3D3*
A	B	C	A	B	C		
2.1	1.0	2.2	2.2	1.0	2.2	5.0	6.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 XN3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.31 + 0.047*SL	0.32 + 0.043*SL	0.33 + 0.042*SL
	t_{PHL}	0.33	0.25 + 0.037*SL	0.27 + 0.031*SL	0.29 + 0.027*SL
	t_R	0.29	0.12 + 0.089*SL	0.12 + 0.088*SL	0.11 + 0.089*SL
	t_F	0.20	0.10 + 0.051*SL	0.11 + 0.046*SL	0.13 + 0.043*SL
B to Y	t_{PLH}	0.67	0.58 + 0.043*SL	0.59 + 0.041*SL	0.59 + 0.041*SL
	t_{PHL}	0.69	0.61 + 0.037*SL	0.63 + 0.028*SL	0.66 + 0.025*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.040*SL	0.13 + 0.040*SL
C to Y	t_{PLH}	0.56	0.47 + 0.043*SL	0.48 + 0.041*SL	0.48 + 0.041*SL
	t_{PHL}	0.56	0.49 + 0.037*SL	0.51 + 0.028*SL	0.54 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.040*SL	0.13 + 0.040*SL

KG80 XN3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.37 + 0.021*SL	0.38 + 0.016*SL	0.39 + 0.015*SL
	t_{PHL}	0.33	0.30 + 0.018*SL	0.30 + 0.016*SL	0.32 + 0.013*SL
	t_R	0.21	0.16 + 0.026*SL	0.15 + 0.028*SL	0.15 + 0.029*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.15 + 0.018*SL
B to Y	t_{PLH}	0.68	0.65 + 0.018*SL	0.65 + 0.015*SL	0.66 + 0.014*SL
	t_{PHL}	0.71	0.67 + 0.018*SL	0.68 + 0.014*SL	0.70 + 0.012*SL
	t_R	0.18	0.13 + 0.026*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_F	0.18	0.15 + 0.019*SL	0.15 + 0.016*SL	0.16 + 0.014*SL
C to Y	t_{PLH}	0.57	0.53 + 0.018*SL	0.54 + 0.015*SL	0.55 + 0.014*SL
	t_{PHL}	0.58	0.55 + 0.018*SL	0.55 + 0.014*SL	0.57 + 0.012*SL
	t_R	0.18	0.13 + 0.026*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_F	0.18	0.15 + 0.019*SL	0.15 + 0.016*SL	0.16 + 0.014*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 XN3

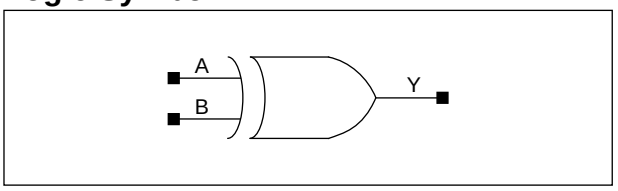
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.53	0.41 + 0.059*SL	0.43 + 0.051*SL	0.45 + 0.050*SL
	t_{PHL}	0.43	0.34 + 0.044*SL	0.37 + 0.033*SL	0.43 + 0.028*SL
	t_R	0.38	0.16 + 0.108*SL	0.17 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.25	0.14 + 0.057*SL	0.16 + 0.049*SL	0.21 + 0.044*SL
B to Y	t_{PLH}	0.95	0.84 + 0.053*SL	0.85 + 0.050*SL	0.85 + 0.050*SL
	t_{PHL}	0.97	0.88 + 0.044*SL	0.92 + 0.030*SL	0.97 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
C to Y	t_{PLH}	0.78	0.68 + 0.053*SL	0.69 + 0.050*SL	0.69 + 0.050*SL
	t_{PHL}	0.79	0.70 + 0.044*SL	0.74 + 0.030*SL	0.80 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL

KGM80 XN3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.54	0.49 + 0.024*SL	0.50 + 0.020*SL	0.53 + 0.018*SL
	t_{PHL}	0.48	0.43 + 0.024*SL	0.44 + 0.019*SL	0.49 + 0.015*SL
	t_R	0.26	0.18 + 0.038*SL	0.19 + 0.036*SL	0.20 + 0.035*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.023*SL	0.25 + 0.019*SL
B to Y	t_{PLH}	0.97	0.92 + 0.022*SL	0.93 + 0.018*SL	0.95 + 0.017*SL
	t_{PHL}	1.01	0.96 + 0.023*SL	0.98 + 0.016*SL	1.02 + 0.012*SL
	t_R	0.23	0.16 + 0.036*SL	0.16 + 0.034*SL	0.16 + 0.035*SL
	t_F	0.24	0.20 + 0.023*SL	0.21 + 0.018*SL	0.24 + 0.015*SL
C to Y	t_{PLH}	0.80	0.75 + 0.022*SL	0.76 + 0.018*SL	0.78 + 0.017*SL
	t_{PHL}	0.83	0.79 + 0.023*SL	0.80 + 0.017*SL	0.85 + 0.012*SL
	t_R	0.23	0.15 + 0.036*SL	0.16 + 0.034*SL	0.15 + 0.035*SL
	t_F	0.24	0.19 + 0.023*SL	0.21 + 0.018*SL	0.24 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)				Gate Count	
KG80					
XO2		*XO2D2*		*XO2*	*XO2D2*
A	B	A	B		
0.9	1.2	0.9	1.1	3.0	4.0
KGM80					
XO2		*XO2D2*		*XO2*	*XO2D2*
A	B	A	B		
1.0	2.0	1.0	2.0	3.0	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 XO2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.50	0.41 + 0.043*SL	0.41 + 0.041*SL	0.41 + 0.042*SL
	t_{PHL}	0.41	0.33 + 0.040*SL	0.36 + 0.030*SL	0.39 + 0.025*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.23	0.14 + 0.045*SL	0.15 + 0.040*SL	0.15 + 0.040*SL
B to Y	t_{PLH}	0.37	0.28 + 0.043*SL	0.29 + 0.042*SL	0.29 + 0.042*SL
	t_{PHL}	0.30	0.24 + 0.033*SL	0.25 + 0.028*SL	0.27 + 0.025*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.09 + 0.045*SL	0.10 + 0.042*SL	0.10 + 0.041*SL

KG80 XO2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.44 + 0.023*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.41	0.36 + 0.024*SL	0.38 + 0.019*SL	0.40 + 0.015*SL
	t_R	0.20	0.12 + 0.040*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.20	0.15 + 0.026*SL	0.16 + 0.022*SL	0.17 + 0.020*SL
B to Y	t_{PLH}	0.36	0.31 + 0.023*SL	0.32 + 0.022*SL	0.32 + 0.021*SL
	t_{PHL}	0.30	0.26 + 0.021*SL	0.27 + 0.017*SL	0.29 + 0.015*SL
	t_R	0.20	0.11 + 0.043*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.16	0.11 + 0.026*SL	0.11 + 0.023*SL	0.12 + 0.022*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 XO2

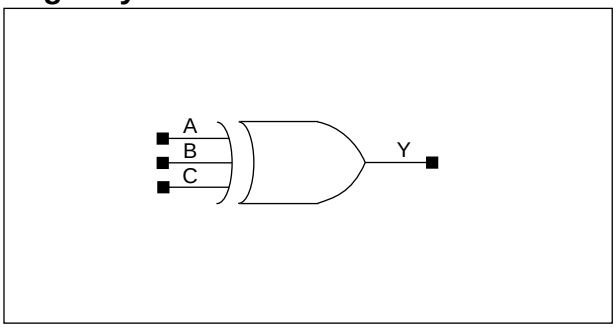
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.56 + 0.053*SL	0.56 + 0.050*SL	0.57 + 0.050*SL
	t_{PHL}	0.56	0.46 + 0.048*SL	0.51 + 0.032*SL	0.58 + 0.025*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.28	0.18 + 0.050*SL	0.21 + 0.042*SL	0.22 + 0.040*SL
B to Y	t_{PLH}	0.48	0.38 + 0.053*SL	0.39 + 0.050*SL	0.39 + 0.050*SL
	t_{PHL}	0.40	0.32 + 0.038*SL	0.35 + 0.029*SL	0.39 + 0.025*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.22	0.12 + 0.050*SL	0.14 + 0.043*SL	0.15 + 0.042*SL

KGM80 XO2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.65	0.59 + 0.029*SL	0.60 + 0.026*SL	0.61 + 0.025*SL
	t_{PHL}	0.57	0.51 + 0.030*SL	0.53 + 0.021*SL	0.59 + 0.016*SL
	t_R	0.26	0.15 + 0.052*SL	0.15 + 0.052*SL	0.14 + 0.054*SL
	t_F	0.26	0.20 + 0.031*SL	0.22 + 0.024*SL	0.25 + 0.021*SL
B to Y	t_{PLH}	0.47	0.41 + 0.030*SL	0.42 + 0.026*SL	0.43 + 0.025*SL
	t_{PHL}	0.42	0.37 + 0.025*SL	0.39 + 0.019*SL	0.43 + 0.015*SL
	t_R	0.26	0.15 + 0.053*SL	0.16 + 0.052*SL	0.14 + 0.054*SL
	t_F	0.21	0.15 + 0.030*SL	0.16 + 0.024*SL	0.19 + 0.022*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

ICell Data

Input Load (SL)						Gate Count	
KG80							
XO3			*XO3D3*			*XO3*	*XO3D3*
A	B	C	A	B	C		
1.7	0.9	1.7	1.7	0.9	1.7	5.0	6.0
KGM80							
XO3			*XO3D3*			*XO3*	*XO3D3*
A	B	C	A	B	C		
2.0	1.0	2.0	2.0	1.0	2.0	5.0	6.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 XO3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.28 + 0.043*SL	0.29 + 0.041*SL	0.29 + 0.042*SL
	t_{PHL}	0.31	0.24 + 0.034*SL	0.25 + 0.027*SL	0.27 + 0.025*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.09 + 0.043*SL	0.10 + 0.042*SL	0.10 + 0.041*SL
B to Y	t_{PLH}	0.67	0.58 + 0.043*SL	0.59 + 0.041*SL	0.59 + 0.041*SL
	t_{PHL}	0.68	0.61 + 0.036*SL	0.63 + 0.028*SL	0.65 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.041*SL	0.13 + 0.040*SL
C to Y	t_{PLH}	0.55	0.47 + 0.043*SL	0.47 + 0.041*SL	0.47 + 0.042*SL
	t_{PHL}	0.56	0.48 + 0.036*SL	0.50 + 0.028*SL	0.53 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.040*SL	0.12 + 0.041*SL

KG80 XO3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.33 + 0.018*SL	0.34 + 0.015*SL	0.35 + 0.014*SL
	t_{PHL}	0.32	0.29 + 0.017*SL	0.29 + 0.014*SL	0.31 + 0.011*SL
	t_R	0.17	0.12 + 0.027*SL	0.12 + 0.028*SL	0.11 + 0.029*SL
	t_F	0.16	0.12 + 0.019*SL	0.13 + 0.016*SL	0.14 + 0.015*SL
B to Y	t_{PLH}	0.68	0.65 + 0.017*SL	0.65 + 0.015*SL	0.66 + 0.014*SL
	t_{PHL}	0.70	0.67 + 0.018*SL	0.68 + 0.014*SL	0.69 + 0.012*SL
	t_R	0.18	0.13 + 0.026*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_F	0.18	0.15 + 0.019*SL	0.15 + 0.016*SL	0.16 + 0.014*SL
C to Y	t_{PLH}	0.57	0.53 + 0.018*SL	0.54 + 0.015*SL	0.54 + 0.014*SL
	t_{PHL}	0.58	0.54 + 0.018*SL	0.55 + 0.014*SL	0.57 + 0.012*SL
	t_R	0.18	0.12 + 0.026*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_F	0.18	0.15 + 0.019*SL	0.15 + 0.016*SL	0.16 + 0.014*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 XO3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.48	0.38 + 0.053*SL	0.39 + 0.050*SL	0.39 + 0.050*SL
	t_{PHL}	0.41	0.33 + 0.038*SL	0.36 + 0.029*SL	0.40 + 0.025*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.22	0.12 + 0.049*SL	0.14 + 0.043*SL	0.15 + 0.042*SL
B to Y	t_{PLH}	0.95	0.84 + 0.053*SL	0.85 + 0.050*SL	0.85 + 0.050*SL
	t_{PHL}	0.96	0.87 + 0.043*SL	0.91 + 0.030*SL	0.97 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.18 + 0.041*SL
C to Y	t_{PLH}	0.78	0.67 + 0.053*SL	0.68 + 0.050*SL	0.68 + 0.050*SL
	t_{PHL}	0.78	0.69 + 0.043*SL	0.73 + 0.030*SL	0.78 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.050*SL	0.18 + 0.042*SL	0.19 + 0.041*SL

KGM80 XO3D3

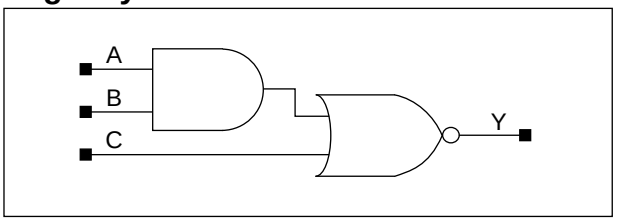
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.48	0.44 + 0.022*SL	0.45 + 0.018*SL	0.47 + 0.017*SL
	t_{PHL}	0.45	0.41 + 0.021*SL	0.42 + 0.016*SL	0.46 + 0.012*SL
	t_R	0.22	0.15 + 0.034*SL	0.15 + 0.035*SL	0.15 + 0.035*SL
	t_F	0.21	0.16 + 0.023*SL	0.18 + 0.018*SL	0.21 + 0.016*SL
B to Y	t_{PLH}	0.97	0.92 + 0.022*SL	0.93 + 0.018*SL	0.95 + 0.017*SL
	t_{PHL}	1.00	0.96 + 0.023*SL	0.98 + 0.016*SL	1.02 + 0.012*SL
	t_R	0.23	0.16 + 0.035*SL	0.16 + 0.035*SL	0.16 + 0.035*SL
	t_F	0.24	0.19 + 0.023*SL	0.21 + 0.018*SL	0.24 + 0.015*SL
C to Y	t_{PLH}	0.79	0.75 + 0.022*SL	0.76 + 0.018*SL	0.78 + 0.017*SL
	t_{PHL}	0.82	0.77 + 0.023*SL	0.79 + 0.016*SL	0.83 + 0.012*SL
	t_R	0.23	0.16 + 0.036*SL	0.16 + 0.034*SL	0.16 + 0.035*SL
	t_F	0.24	0.19 + 0.023*SL	0.21 + 0.018*SL	0.24 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

AO21/AO21D2

2-AND into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
x	x	1	0
0	x	0	1
x	0	0	1
1	1	x	0

Cell Data

Input Load (SL)						Gate Count	
KG80							
AO21			*AO21D2*			*AO21*	*AO21D2*
A	B	C	A	B	C		
0.5	0.5	0.7	1.1	1.1	1.5	2.0	2.0
KGM80							
AO21			*AO21D2*			*AO21*	*AO21D2*
A	B	C	A	B	C		
1.0	1.0	1.0	2.0	2.0	1.9	2.0	2.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.18 + 0.067*SL	0.18 + 0.070*SL	0.17 + 0.071*SL
	t_{PHL}	0.16	0.07 + 0.045*SL	0.09 + 0.034*SL	0.10 + 0.034*SL
	t_R	0.57	0.27 + 0.152*SL	0.25 + 0.159*SL	0.22 + 0.163*SL
	t_F	0.30	0.18 + 0.059*SL	0.18 + 0.062*SL	0.15 + 0.065*SL
B to Y	t_{PLH}	0.36	0.23 + 0.067*SL	0.22 + 0.069*SL	0.21 + 0.070*SL
	t_{PHL}	0.15	0.06 + 0.041*SL	0.08 + 0.035*SL	0.08 + 0.034*SL
	t_R	0.64	0.33 + 0.152*SL	0.32 + 0.159*SL	0.29 + 0.163*SL
	t_F	0.28	0.17 + 0.056*SL	0.15 + 0.063*SL	0.13 + 0.066*SL
C to Y	t_{PLH}	0.40	0.26 + 0.070*SL	0.26 + 0.071*SL	0.25 + 0.071*SL
	t_{PHL}	0.15	0.09 + 0.030*SL	0.11 + 0.025*SL	0.12 + 0.023*SL
	t_R	0.63	0.32 + 0.156*SL	0.31 + 0.160*SL	0.29 + 0.163*SL
	t_F	0.29	0.20 + 0.044*SL	0.22 + 0.035*SL	0.19 + 0.039*SL

KG80 AO21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.20 + 0.034*SL	0.19 + 0.034*SL	0.19 + 0.035*SL
	t_{PHL}	0.12	0.07 + 0.025*SL	0.09 + 0.020*SL	0.11 + 0.016*SL
	t_R	0.43	0.28 + 0.075*SL	0.28 + 0.078*SL	0.26 + 0.080*SL
	t_F	0.25	0.19 + 0.030*SL	0.19 + 0.029*SL	0.18 + 0.031*SL
B to Y	t_{PLH}	0.31	0.25 + 0.033*SL	0.25 + 0.034*SL	0.24 + 0.035*SL
	t_{PHL}	0.12	0.07 + 0.022*SL	0.08 + 0.019*SL	0.09 + 0.017*SL
	t_R	0.52	0.37 + 0.074*SL	0.36 + 0.077*SL	0.34 + 0.080*SL
	t_F	0.23	0.18 + 0.028*SL	0.17 + 0.030*SL	0.16 + 0.032*SL
C to Y	t_{PLH}	0.34	0.27 + 0.035*SL	0.27 + 0.035*SL	0.26 + 0.035*SL
	t_{PHL}	0.13	0.09 + 0.018*SL	0.10 + 0.014*SL	0.11 + 0.012*SL
	t_R	0.51	0.36 + 0.077*SL	0.35 + 0.079*SL	0.34 + 0.080*SL
	t_F	0.24	0.20 + 0.018*SL	0.20 + 0.019*SL	0.21 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

AO21/AO21D2

2-AND into 2-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO21

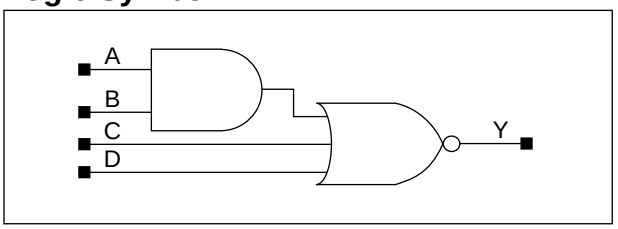
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.42	0.23 + 0.092*SL	0.23 + 0.094*SL	0.23 + 0.094*SL
	t_{PHL}	0.20	0.10 + 0.046*SL	0.13 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.78	0.37 + 0.202*SL	0.36 + 0.207*SL	0.34 + 0.208*SL
	t_F	0.33	0.19 + 0.067*SL	0.19 + 0.070*SL	0.15 + 0.073*SL
B to Y	t_{PLH}	0.49	0.30 + 0.093*SL	0.30 + 0.093*SL	0.30 + 0.094*SL
	t_{PHL}	0.19	0.10 + 0.043*SL	0.12 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.87	0.46 + 0.202*SL	0.45 + 0.207*SL	0.44 + 0.209*SL
	t_F	0.31	0.17 + 0.067*SL	0.16 + 0.071*SL	0.14 + 0.074*SL
C to Y	t_{PLH}	0.58	0.39 + 0.095*SL	0.39 + 0.094*SL	0.39 + 0.094*SL
	t_{PHL}	0.19	0.13 + 0.031*SL	0.15 + 0.025*SL	0.16 + 0.023*SL
	t_R	0.88	0.47 + 0.202*SL	0.46 + 0.207*SL	0.44 + 0.208*SL
	t_F	0.29	0.21 + 0.039*SL	0.21 + 0.039*SL	0.18 + 0.042*SL

KGM80 AO21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.25 + 0.046*SL	0.25 + 0.047*SL	0.25 + 0.047*SL
	t_{PHL}	0.16	0.11 + 0.025*SL	0.12 + 0.020*SL	0.14 + 0.018*SL
	t_R	0.61	0.41 + 0.100*SL	0.41 + 0.102*SL	0.39 + 0.104*SL
	t_F	0.27	0.20 + 0.036*SL	0.21 + 0.034*SL	0.19 + 0.035*SL
B to Y	t_{PLH}	0.43	0.34 + 0.047*SL	0.34 + 0.047*SL	0.33 + 0.047*SL
	t_{PHL}	0.16	0.12 + 0.022*SL	0.13 + 0.020*SL	0.14 + 0.019*SL
	t_R	0.72	0.52 + 0.100*SL	0.52 + 0.102*SL	0.50 + 0.104*SL
	t_F	0.26	0.19 + 0.034*SL	0.19 + 0.034*SL	0.17 + 0.036*SL
C to Y	t_{PLH}	0.50	0.40 + 0.048*SL	0.40 + 0.047*SL	0.40 + 0.047*SL
	t_{PHL}	0.16	0.13 + 0.017*SL	0.13 + 0.014*SL	0.16 + 0.012*SL
	t_R	0.72	0.52 + 0.100*SL	0.52 + 0.102*SL	0.50 + 0.104*SL
	t_F	0.25	0.21 + 0.020*SL	0.21 + 0.019*SL	0.20 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	x	0
x	x	x	1	0
x	0	0	0	1
0	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
KG80									
AO211				*AO211D2*				*AO211*	*AO211D2*
A	B	C	D	A	B	C	D		
0.5	0.5	0.6	0.7	1.1	1.1	1.3	1.5	2.0	4.0
KGM80									
AO211				*AO211D2*				*AO211*	*AO211D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	2.0	2.0	1.9	1.9	2.0	4.0

AO211/AO211D2

2-AND into 3-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.42	0.23 + 0.097*SL	0.22 + 0.100*SL	0.21 + 0.101*SL
	t_{PHL}	0.17	0.08 + 0.043*SL	0.10 + 0.034*SL	0.11 + 0.034*SL
	t_R	0.90	0.44 + 0.229*SL	0.43 + 0.237*SL	0.41 + 0.238*SL
	t_F	0.31	0.20 + 0.058*SL	0.19 + 0.062*SL	0.17 + 0.065*SL
B to Y	t_{PLH}	0.48	0.29 + 0.097*SL	0.28 + 0.100*SL	0.27 + 0.101*SL
	t_{PHL}	0.15	0.07 + 0.040*SL	0.09 + 0.035*SL	0.09 + 0.034*SL
	t_R	1.00	0.54 + 0.231*SL	0.52 + 0.237*SL	0.51 + 0.238*SL
	t_F	0.30	0.18 + 0.059*SL	0.17 + 0.063*SL	0.15 + 0.066*SL
C to Y	t_{PLH}	0.57	0.37 + 0.101*SL	0.36 + 0.102*SL	0.36 + 0.102*SL
	t_{PHL}	0.16	0.10 + 0.031*SL	0.12 + 0.025*SL	0.13 + 0.023*SL
	t_R	1.02	0.56 + 0.231*SL	0.55 + 0.235*SL	0.53 + 0.236*SL
	t_F	0.28	0.21 + 0.035*SL	0.21 + 0.037*SL	0.19 + 0.040*SL
D to Y	t_{PLH}	0.58	0.37 + 0.102*SL	0.37 + 0.102*SL	0.37 + 0.102*SL
	t_{PHL}	0.17	0.11 + 0.029*SL	0.12 + 0.025*SL	0.13 + 0.024*SL
	t_R	1.02	0.55 + 0.232*SL	0.54 + 0.235*SL	0.53 + 0.236*SL
	t_F	0.31	0.23 + 0.041*SL	0.24 + 0.037*SL	0.22 + 0.039*SL

KG80 AO211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.21 + 0.045*SL	0.20 + 0.049*SL	0.19 + 0.050*SL
	t_{PHL}	0.12	0.06 + 0.026*SL	0.08 + 0.020*SL	0.10 + 0.016*SL
	t_R	0.62	0.40 + 0.114*SL	0.39 + 0.115*SL	0.37 + 0.118*SL
	t_F	0.24	0.18 + 0.032*SL	0.18 + 0.030*SL	0.17 + 0.032*SL
B to Y	t_{PLH}	0.37	0.27 + 0.048*SL	0.27 + 0.049*SL	0.26 + 0.050*SL
	t_{PHL}	0.11	0.07 + 0.022*SL	0.07 + 0.019*SL	0.09 + 0.017*SL
	t_R	0.74	0.51 + 0.112*SL	0.51 + 0.116*SL	0.49 + 0.118*SL
	t_F	0.22	0.17 + 0.028*SL	0.16 + 0.030*SL	0.15 + 0.032*SL
C to Y	t_{PLH}	0.45	0.35 + 0.051*SL	0.35 + 0.051*SL	0.35 + 0.051*SL
	t_{PHL}	0.13	0.09 + 0.019*SL	0.10 + 0.015*SL	0.12 + 0.012*SL
	t_R	0.76	0.53 + 0.114*SL	0.53 + 0.116*SL	0.51 + 0.117*SL
	t_F	0.24	0.20 + 0.020*SL	0.20 + 0.017*SL	0.20 + 0.019*SL
D to Y	t_{PLH}	0.46	0.36 + 0.051*SL	0.36 + 0.051*SL	0.36 + 0.051*SL
	t_{PHL}	0.13	0.10 + 0.018*SL	0.11 + 0.014*SL	0.12 + 0.012*SL
	t_R	0.76	0.53 + 0.114*SL	0.52 + 0.116*SL	0.51 + 0.118*SL
	t_F	0.26	0.22 + 0.019*SL	0.22 + 0.019*SL	0.23 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.30 + 0.138*SL	0.29 + 0.139*SL	0.29 + 0.139*SL
	t_{PHL}	0.21	0.12 + 0.045*SL	0.14 + 0.037*SL	0.15 + 0.037*SL
	t_R	1.29	0.68 + 0.308*SL	0.67 + 0.310*SL	0.69 + 0.308*SL
	t_F	0.35	0.22 + 0.066*SL	0.21 + 0.070*SL	0.17 + 0.073*SL
B to Y	t_{PLH}	0.68	0.40 + 0.138*SL	0.40 + 0.139*SL	0.40 + 0.139*SL
	t_{PHL}	0.20	0.12 + 0.042*SL	0.13 + 0.038*SL	0.14 + 0.037*SL
	t_R	1.43	0.81 + 0.308*SL	0.81 + 0.310*SL	0.83 + 0.309*SL
	t_F	0.33	0.20 + 0.067*SL	0.18 + 0.072*SL	0.16 + 0.074*SL
C to Y	t_{PLH}	0.87	0.59 + 0.141*SL	0.59 + 0.140*SL	0.60 + 0.139*SL
	t_{PHL}	0.20	0.14 + 0.030*SL	0.16 + 0.024*SL	0.17 + 0.023*SL
	t_R	1.47	0.86 + 0.303*SL	0.85 + 0.307*SL	0.84 + 0.308*SL
	t_F	0.30	0.22 + 0.039*SL	0.22 + 0.039*SL	0.20 + 0.042*SL
D to Y	t_{PLH}	0.91	0.63 + 0.142*SL	0.63 + 0.140*SL	0.64 + 0.139*SL
	t_{PHL}	0.21	0.14 + 0.031*SL	0.16 + 0.025*SL	0.18 + 0.023*SL
	t_R	1.46	0.86 + 0.304*SL	0.85 + 0.307*SL	0.84 + 0.308*SL
	t_F	0.32	0.25 + 0.038*SL	0.24 + 0.040*SL	0.22 + 0.042*SL

KGM80 AO211D2

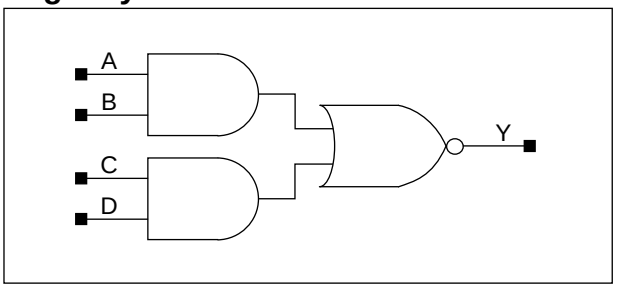
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.38	0.26 + 0.064*SL	0.24 + 0.069*SL	0.24 + 0.070*SL
	t_{PHL}	0.15	0.10 + 0.026*SL	0.11 + 0.021*SL	0.14 + 0.018*SL
	t_R	0.89	0.58 + 0.154*SL	0.58 + 0.154*SL	0.57 + 0.155*SL
	t_F	0.26	0.19 + 0.036*SL	0.19 + 0.034*SL	0.17 + 0.035*SL
B to Y	t_{PLH}	0.51	0.37 + 0.069*SL	0.37 + 0.069*SL	0.37 + 0.069*SL
	t_{PHL}	0.15	0.11 + 0.023*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
	t_R	1.06	0.75 + 0.153*SL	0.75 + 0.155*SL	0.74 + 0.155*SL
	t_F	0.24	0.17 + 0.034*SL	0.17 + 0.034*SL	0.15 + 0.036*SL
C to Y	t_{PLH}	0.71	0.56 + 0.072*SL	0.57 + 0.070*SL	0.57 + 0.070*SL
	t_{PHL}	0.16	0.13 + 0.017*SL	0.14 + 0.014*SL	0.16 + 0.012*SL
	t_R	1.10	0.81 + 0.149*SL	0.80 + 0.152*SL	0.78 + 0.154*SL
	t_F	0.25	0.21 + 0.020*SL	0.21 + 0.019*SL	0.20 + 0.020*SL
D to Y	t_{PLH}	0.75	0.60 + 0.072*SL	0.61 + 0.071*SL	0.61 + 0.070*SL
	t_{PHL}	0.17	0.13 + 0.018*SL	0.14 + 0.014*SL	0.17 + 0.012*SL
	t_R	1.10	0.80 + 0.150*SL	0.80 + 0.152*SL	0.78 + 0.154*SL
	t_F	0.27	0.23 + 0.021*SL	0.23 + 0.020*SL	0.23 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

AO22/AO22D2

Two 2-ANDs into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

Cell Data

Input Load (SL)								Gate Count	
KG80									
AO22				*AO22D2*				*AO22*	*AO22D2*
A	B	C	D	A	B	C	D		
0.5	0.5	0.7	0.7	0.6	0.5	0.7	0.7	2.0	4.0
KGM80									
AO22				*AO22D2*				*AO22*	*AO22D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	2.0	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.36	0.22 + 0.068*SL	0.22 + 0.070*SL	0.21 + 0.071*SL
	t_{PHL}	0.17	0.08 + 0.043*SL	0.11 + 0.034*SL	0.11 + 0.034*SL
	t_R	0.63	0.32 + 0.155*SL	0.31 + 0.160*SL	0.29 + 0.163*SL
	t_F	0.34	0.23 + 0.056*SL	0.21 + 0.062*SL	0.19 + 0.065*SL
B to Y	t_{PLH}	0.40	0.26 + 0.068*SL	0.26 + 0.070*SL	0.25 + 0.070*SL
	t_{PHL}	0.16	0.08 + 0.040*SL	0.09 + 0.035*SL	0.09 + 0.034*SL
	t_R	0.70	0.40 + 0.153*SL	0.38 + 0.160*SL	0.36 + 0.164*SL
	t_F	0.32	0.21 + 0.056*SL	0.19 + 0.063*SL	0.17 + 0.066*SL
C to Y	t_{PLH}	0.41	0.27 + 0.072*SL	0.27 + 0.071*SL	0.27 + 0.072*SL
	t_{PHL}	0.22	0.15 + 0.036*SL	0.15 + 0.035*SL	0.16 + 0.034*SL
	t_R	0.64	0.33 + 0.155*SL	0.32 + 0.160*SL	0.30 + 0.163*SL
	t_F	0.39	0.26 + 0.062*SL	0.27 + 0.062*SL	0.24 + 0.065*SL
D to Y	t_{PLH}	0.45	0.31 + 0.071*SL	0.31 + 0.071*SL	0.31 + 0.071*SL
	t_{PHL}	0.21	0.13 + 0.038*SL	0.14 + 0.035*SL	0.14 + 0.034*SL
	t_R	0.71	0.39 + 0.157*SL	0.39 + 0.160*SL	0.37 + 0.163*SL
	t_F	0.37	0.25 + 0.061*SL	0.24 + 0.064*SL	0.22 + 0.067*SL

KG80 AO22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.45 + 0.022*SL	0.45 + 0.020*SL	0.45 + 0.021*SL
	t_{PHL}	0.35	0.32 + 0.017*SL	0.33 + 0.014*SL	0.34 + 0.012*SL
	t_R	0.18	0.10 + 0.041*SL	0.09 + 0.043*SL	0.08 + 0.045*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.020*SL
B to Y	t_{PLH}	0.54	0.49 + 0.021*SL	0.50 + 0.021*SL	0.49 + 0.021*SL
	t_{PHL}	0.34	0.31 + 0.018*SL	0.31 + 0.014*SL	0.32 + 0.012*SL
	t_R	0.18	0.10 + 0.039*SL	0.09 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
C to Y	t_{PLH}	0.54	0.50 + 0.021*SL	0.50 + 0.020*SL	0.50 + 0.021*SL
	t_{PHL}	0.42	0.38 + 0.017*SL	0.39 + 0.014*SL	0.40 + 0.012*SL
	t_R	0.18	0.11 + 0.038*SL	0.09 + 0.044*SL	0.09 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.020*SL
D to Y	t_{PLH}	0.59	0.55 + 0.021*SL	0.55 + 0.021*SL	0.55 + 0.020*SL
	t_{PHL}	0.40	0.37 + 0.017*SL	0.38 + 0.014*SL	0.38 + 0.012*SL
	t_R	0.18	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

AO22/AO22D2

Two 2-ANDs into 2-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO22

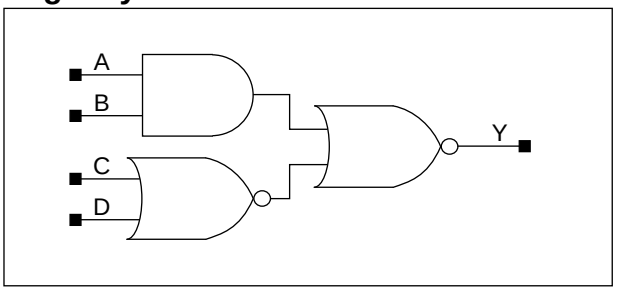
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.48	0.29 + 0.094*SL	0.29 + 0.094*SL	0.29 + 0.094*SL
	t_{PHL}	0.21	0.11 + 0.046*SL	0.14 + 0.038*SL	0.14 + 0.037*SL
	t_R	0.87	0.46 + 0.204*SL	0.45 + 0.208*SL	0.44 + 0.209*SL
	t_F	0.38	0.25 + 0.064*SL	0.23 + 0.070*SL	0.20 + 0.073*SL
B to Y	t_{PLH}	0.55	0.36 + 0.093*SL	0.36 + 0.094*SL	0.36 + 0.094*SL
	t_{PHL}	0.20	0.11 + 0.043*SL	0.13 + 0.038*SL	0.14 + 0.037*SL
	t_R	0.96	0.56 + 0.204*SL	0.55 + 0.208*SL	0.54 + 0.209*SL
	t_F	0.36	0.23 + 0.066*SL	0.21 + 0.071*SL	0.19 + 0.074*SL
C to Y	t_{PLH}	0.61	0.41 + 0.096*SL	0.42 + 0.095*SL	0.42 + 0.094*SL
	t_{PHL}	0.28	0.20 + 0.042*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_R	0.89	0.49 + 0.201*SL	0.47 + 0.207*SL	0.46 + 0.208*SL
	t_F	0.44	0.30 + 0.067*SL	0.30 + 0.071*SL	0.27 + 0.073*SL
D to Y	t_{PLH}	0.68	0.49 + 0.096*SL	0.49 + 0.094*SL	0.49 + 0.094*SL
	t_{PHL}	0.27	0.19 + 0.042*SL	0.20 + 0.038*SL	0.21 + 0.037*SL
	t_R	0.98	0.57 + 0.203*SL	0.56 + 0.207*SL	0.55 + 0.208*SL
	t_F	0.42	0.28 + 0.070*SL	0.28 + 0.072*SL	0.26 + 0.074*SL

KGM80 AO22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.69	0.63 + 0.026*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.019*SL	0.46 + 0.015*SL	0.48 + 0.012*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.022*SL	0.12 + 0.021*SL	0.12 + 0.020*SL
B to Y	t_{PLH}	0.76	0.71 + 0.026*SL	0.71 + 0.025*SL	0.71 + 0.025*SL
	t_{PHL}	0.48	0.44 + 0.019*SL	0.45 + 0.015*SL	0.48 + 0.012*SL
	t_R	0.24	0.14 + 0.050*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.024*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
C to Y	t_{PLH}	0.81	0.76 + 0.026*SL	0.76 + 0.025*SL	0.77 + 0.025*SL
	t_{PHL}	0.57	0.53 + 0.020*SL	0.54 + 0.015*SL	0.57 + 0.012*SL
	t_R	0.24	0.14 + 0.050*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.020*SL	0.12 + 0.021*SL
D to Y	t_{PLH}	0.89	0.84 + 0.026*SL	0.84 + 0.025*SL	0.84 + 0.025*SL
	t_{PHL}	0.56	0.52 + 0.020*SL	0.53 + 0.015*SL	0.56 + 0.012*SL
	t_R	0.24	0.14 + 0.050*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.020*SL	0.12 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
KG80									
AO22A				*AO22D2A*				*AO22A*	*AO22D2A*
A	B	C	D	A	B	C	D		
0.9	0.8	0.9	0.9	0.9	0.9	0.9	0.9	4.0	5.0
KGM80									
AO22A				*AO22D2A*				*AO22A*	*AO22D2A*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	4.0	5.0

AO22A/AO22D2A

2-AND and 2-NOR into 2-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.36	0.22 + 0.068*SL	0.22 + 0.070*SL	0.21 + 0.071*SL
	t_{PHL}	0.17	0.09 + 0.043*SL	0.11 + 0.035*SL	0.11 + 0.034*SL
	t_R	0.64	0.33 + 0.155*SL	0.32 + 0.160*SL	0.30 + 0.163*SL
	t_F	0.34	0.23 + 0.056*SL	0.22 + 0.061*SL	0.18 + 0.066*SL
B to Y	t_{PLH}	0.40	0.27 + 0.068*SL	0.26 + 0.070*SL	0.25 + 0.071*SL
	t_{PHL}	0.16	0.08 + 0.040*SL	0.09 + 0.035*SL	0.09 + 0.034*SL
	t_R	0.71	0.40 + 0.154*SL	0.39 + 0.160*SL	0.36 + 0.164*SL
	t_F	0.32	0.21 + 0.055*SL	0.19 + 0.063*SL	0.17 + 0.066*SL
C to Y	t_{PLH}	0.43	0.29 + 0.074*SL	0.29 + 0.072*SL	0.29 + 0.072*SL
	t_{PHL}	0.37	0.29 + 0.037*SL	0.30 + 0.035*SL	0.30 + 0.034*SL
	t_R	0.63	0.32 + 0.160*SL	0.31 + 0.162*SL	0.31 + 0.163*SL
	t_F	0.34	0.21 + 0.067*SL	0.21 + 0.067*SL	0.20 + 0.068*SL
D to Y	t_{PLH}	0.48	0.33 + 0.073*SL	0.33 + 0.072*SL	0.34 + 0.071*SL
	t_{PHL}	0.38	0.30 + 0.037*SL	0.31 + 0.035*SL	0.31 + 0.035*SL
	t_R	0.70	0.38 + 0.160*SL	0.38 + 0.162*SL	0.37 + 0.163*SL
	t_F	0.34	0.21 + 0.066*SL	0.20 + 0.068*SL	0.20 + 0.069*SL

KG80 AO22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.45 + 0.021*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.35	0.32 + 0.017*SL	0.33 + 0.014*SL	0.34 + 0.012*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.043*SL	0.08 + 0.045*SL
	t_F	0.13	0.09 + 0.020*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
B to Y	t_{PLH}	0.54	0.49 + 0.022*SL	0.50 + 0.021*SL	0.50 + 0.020*SL
	t_{PHL}	0.34	0.31 + 0.017*SL	0.31 + 0.014*SL	0.33 + 0.012*SL
	t_R	0.18	0.11 + 0.039*SL	0.10 + 0.043*SL	0.09 + 0.045*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.020*SL
C to Y	t_{PLH}	0.56	0.51 + 0.022*SL	0.52 + 0.020*SL	0.52 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.018*SL	0.53 + 0.014*SL	0.54 + 0.012*SL
	t_R	0.18	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.13	0.10 + 0.018*SL	0.09 + 0.019*SL	0.09 + 0.020*SL
D to Y	t_{PLH}	0.61	0.57 + 0.021*SL	0.57 + 0.020*SL	0.57 + 0.021*SL
	t_{PHL}	0.57	0.53 + 0.018*SL	0.54 + 0.014*SL	0.55 + 0.012*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.13	0.09 + 0.020*SL	0.09 + 0.019*SL	0.09 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.30 + 0.094*SL	0.30 + 0.094*SL	0.30 + 0.094*SL
	t_{PHL}	0.21	0.12 + 0.046*SL	0.14 + 0.038*SL	0.14 + 0.037*SL
	t_R	0.89	0.48 + 0.204*SL	0.47 + 0.208*SL	0.46 + 0.209*SL
	t_F	0.38	0.25 + 0.065*SL	0.24 + 0.070*SL	0.20 + 0.073*SL
B to Y	t_{PLH}	0.55	0.37 + 0.093*SL	0.37 + 0.094*SL	0.37 + 0.094*SL
	t_{PHL}	0.20	0.11 + 0.043*SL	0.13 + 0.038*SL	0.14 + 0.037*SL
	t_R	0.98	0.57 + 0.204*SL	0.56 + 0.208*SL	0.55 + 0.209*SL
	t_F	0.36	0.23 + 0.066*SL	0.22 + 0.071*SL	0.19 + 0.074*SL
C to Y	t_{PLH}	0.65	0.46 + 0.097*SL	0.46 + 0.095*SL	0.47 + 0.094*SL
	t_{PHL}	0.46	0.38 + 0.041*SL	0.38 + 0.038*SL	0.39 + 0.038*SL
	t_R	0.89	0.48 + 0.205*SL	0.47 + 0.208*SL	0.47 + 0.208*SL
	t_F	0.41	0.27 + 0.071*SL	0.27 + 0.073*SL	0.25 + 0.074*SL
D to Y	t_{PLH}	0.73	0.53 + 0.096*SL	0.54 + 0.094*SL	0.54 + 0.094*SL
	t_{PHL}	0.47	0.39 + 0.042*SL	0.40 + 0.039*SL	0.41 + 0.037*SL
	t_R	0.98	0.57 + 0.206*SL	0.57 + 0.208*SL	0.56 + 0.208*SL
	t_F	0.41	0.27 + 0.073*SL	0.26 + 0.074*SL	0.25 + 0.074*SL

KGM80 AO22D2A

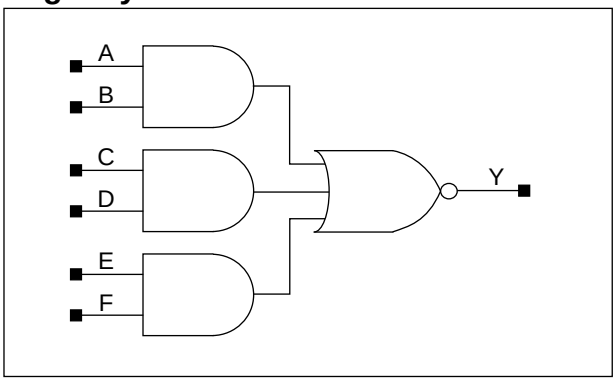
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.69	0.64 + 0.026*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.019*SL	0.46 + 0.015*SL	0.49 + 0.012*SL
	t_R	0.24	0.14 + 0.049*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.021*SL
B to Y	t_{PLH}	0.77	0.71 + 0.026*SL	0.72 + 0.025*SL	0.72 + 0.025*SL
	t_{PHL}	0.48	0.44 + 0.019*SL	0.45 + 0.015*SL	0.48 + 0.012*SL
	t_R	0.24	0.14 + 0.050*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.021*SL	0.12 + 0.020*SL
C to Y	t_{PLH}	0.86	0.80 + 0.026*SL	0.81 + 0.025*SL	0.81 + 0.025*SL
	t_{PHL}	0.74	0.70 + 0.020*SL	0.72 + 0.015*SL	0.74 + 0.012*SL
	t_R	0.24	0.14 + 0.050*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.12 + 0.022*SL	0.12 + 0.021*SL	0.12 + 0.021*SL
D to Y	t_{PLH}	0.93	0.88 + 0.026*SL	0.89 + 0.025*SL	0.89 + 0.025*SL
	t_{PHL}	0.76	0.72 + 0.019*SL	0.73 + 0.015*SL	0.76 + 0.012*SL
	t_R	0.24	0.14 + 0.050*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.020*SL	0.12 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

AO222/AO222D2

Three 2-ANDs into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
Other States						1

Cell Data

Input Load (SL)												Gate Count	
KG80													
AO222						*AO222D2*						*AO222*	*AO222D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	0.9	0.5	0.8	0.5	0.8	0.9	0.9	0.5	0.8	0.5	0.8	3.0	5.0
KGM80													
AO222						*AO222D2*						*AO222*	*AO222D2*
A	B	C	D	E	F	A	B	C	D	E	F		
1.0	1.0	1.0	1.0	0.9	0.9	1.0	1.0	1.0	1.0	0.9	0.9	3.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.54	0.34 + 0.100*SL	0.33 + 0.101*SL	0.33 + 0.102*SL
	t_{PHL}	0.20	0.12 + 0.040*SL	0.13 + 0.034*SL	0.13 + 0.034*SL
	t_R	1.13	0.66 + 0.235*SL	0.65 + 0.238*SL	0.64 + 0.239*SL
	t_F	0.40	0.28 + 0.057*SL	0.27 + 0.062*SL	0.25 + 0.065*SL
B to Y	t_{PLH}	0.60	0.40 + 0.100*SL	0.40 + 0.100*SL	0.39 + 0.101*SL
	t_{PHL}	0.18	0.10 + 0.038*SL	0.11 + 0.034*SL	0.11 + 0.034*SL
	t_R	1.22	0.75 + 0.235*SL	0.75 + 0.238*SL	0.74 + 0.239*SL
	t_F	0.38	0.26 + 0.057*SL	0.25 + 0.064*SL	0.23 + 0.066*SL
C to Y	t_{PLH}	0.66	0.46 + 0.104*SL	0.46 + 0.103*SL	0.46 + 0.103*SL
	t_{PHL}	0.25	0.18 + 0.036*SL	0.18 + 0.034*SL	0.18 + 0.034*SL
	t_R	1.16	0.70 + 0.232*SL	0.69 + 0.235*SL	0.68 + 0.236*SL
	t_F	0.44	0.32 + 0.060*SL	0.32 + 0.063*SL	0.30 + 0.066*SL
D to Y	t_{PLH}	0.73	0.52 + 0.103*SL	0.52 + 0.102*SL	0.52 + 0.102*SL
	t_{PHL}	0.23	0.16 + 0.037*SL	0.16 + 0.035*SL	0.17 + 0.034*SL
	t_R	1.26	0.79 + 0.233*SL	0.79 + 0.235*SL	0.78 + 0.237*SL
	t_F	0.43	0.30 + 0.062*SL	0.30 + 0.064*SL	0.28 + 0.067*SL
E to Y	t_{PLH}	0.71	0.50 + 0.105*SL	0.50 + 0.104*SL	0.51 + 0.103*SL
	t_{PHL}	0.27	0.19 + 0.038*SL	0.20 + 0.036*SL	0.20 + 0.035*SL
	t_R	1.16	0.70 + 0.232*SL	0.69 + 0.235*SL	0.68 + 0.236*SL
	t_F	0.51	0.39 + 0.060*SL	0.38 + 0.063*SL	0.36 + 0.066*SL
F to Y	t_{PLH}	0.77	0.56 + 0.103*SL	0.56 + 0.103*SL	0.57 + 0.102*SL
	t_{PHL}	0.25	0.18 + 0.039*SL	0.18 + 0.036*SL	0.19 + 0.035*SL
	t_R	1.26	0.79 + 0.234*SL	0.78 + 0.235*SL	0.78 + 0.236*SL
	t_F	0.48	0.36 + 0.063*SL	0.35 + 0.065*SL	0.34 + 0.067*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

AO222/AO222D2

Three 2-ANDs into 3-NOR with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.65	0.60 + 0.023*SL	0.61 + 0.020*SL	0.61 + 0.021*SL
	t_{PHL}	0.39	0.35 + 0.017*SL	0.36 + 0.014*SL	0.37 + 0.012*SL
	t_R	0.19	0.11 + 0.039*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
B to Y	t_{PLH}	0.71	0.66 + 0.022*SL	0.67 + 0.021*SL	0.67 + 0.020*SL
	t_{PHL}	0.38	0.34 + 0.017*SL	0.35 + 0.014*SL	0.36 + 0.012*SL
	t_R	0.20	0.12 + 0.039*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.08 + 0.021*SL
C to Y	t_{PLH}	0.74	0.70 + 0.023*SL	0.70 + 0.020*SL	0.70 + 0.021*SL
	t_{PHL}	0.45	0.41 + 0.018*SL	0.42 + 0.014*SL	0.43 + 0.012*SL
	t_R	0.19	0.12 + 0.039*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.13	0.10 + 0.019*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
D to Y	t_{PLH}	0.80	0.76 + 0.023*SL	0.76 + 0.021*SL	0.76 + 0.020*SL
	t_{PHL}	0.43	0.40 + 0.018*SL	0.40 + 0.014*SL	0.41 + 0.012*SL
	t_R	0.20	0.12 + 0.039*SL	0.11 + 0.042*SL	0.10 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
E to Y	t_{PLH}	0.82	0.77 + 0.022*SL	0.78 + 0.021*SL	0.78 + 0.020*SL
	t_{PHL}	0.49	0.45 + 0.018*SL	0.46 + 0.014*SL	0.47 + 0.012*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.042*SL	0.10 + 0.044*SL
	t_F	0.13	0.10 + 0.020*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
F to Y	t_{PLH}	0.88	0.84 + 0.022*SL	0.84 + 0.021*SL	0.84 + 0.020*SL
	t_{PHL}	0.47	0.43 + 0.018*SL	0.44 + 0.014*SL	0.45 + 0.012*SL
	t_R	0.20	0.12 + 0.041*SL	0.11 + 0.042*SL	0.10 + 0.044*SL
	t_F	0.13	0.10 + 0.019*SL	0.10 + 0.019*SL	0.09 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.78	0.50 + 0.140*SL	0.50 + 0.139*SL	0.50 + 0.139*SL
	t_{PHL}	0.23	0.15 + 0.044*SL	0.16 + 0.038*SL	0.17 + 0.037*SL
	t_R	1.62	1.00 + 0.311*SL	0.99 + 0.312*SL	1.03 + 0.309*SL
	t_F	0.45	0.32 + 0.066*SL	0.31 + 0.070*SL	0.28 + 0.073*SL
B to Y	t_{PLH}	0.88	0.60 + 0.139*SL	0.60 + 0.139*SL	0.60 + 0.139*SL
	t_{PHL}	0.23	0.14 + 0.042*SL	0.15 + 0.038*SL	0.16 + 0.037*SL
	t_R	1.76	1.13 + 0.312*SL	1.13 + 0.312*SL	1.17 + 0.309*SL
	t_F	0.44	0.30 + 0.066*SL	0.29 + 0.072*SL	0.27 + 0.074*SL
C to Y	t_{PLH}	1.04	0.76 + 0.143*SL	0.76 + 0.140*SL	0.77 + 0.140*SL
	t_{PHL}	0.31	0.23 + 0.040*SL	0.24 + 0.038*SL	0.25 + 0.037*SL
	t_R	1.68	1.07 + 0.304*SL	1.07 + 0.307*SL	1.06 + 0.308*SL
	t_F	0.52	0.38 + 0.067*SL	0.37 + 0.071*SL	0.35 + 0.073*SL
D to Y	t_{PLH}	1.15	0.87 + 0.141*SL	0.87 + 0.140*SL	0.88 + 0.139*SL
	t_{PHL}	0.30	0.22 + 0.041*SL	0.23 + 0.038*SL	0.24 + 0.037*SL
	t_R	1.82	1.21 + 0.305*SL	1.20 + 0.307*SL	1.19 + 0.308*SL
	t_F	0.50	0.36 + 0.069*SL	0.36 + 0.072*SL	0.34 + 0.074*SL
E to Y	t_{PLH}	1.13	0.85 + 0.143*SL	0.85 + 0.141*SL	0.86 + 0.139*SL
	t_{PHL}	0.33	0.25 + 0.042*SL	0.26 + 0.040*SL	0.27 + 0.038*SL
	t_R	1.68	1.07 + 0.304*SL	1.07 + 0.307*SL	1.06 + 0.308*SL
	t_F	0.59	0.45 + 0.069*SL	0.44 + 0.071*SL	0.42 + 0.073*SL
F to Y	t_{PLH}	1.24	0.95 + 0.141*SL	0.96 + 0.140*SL	0.96 + 0.139*SL
	t_{PHL}	0.32	0.24 + 0.043*SL	0.25 + 0.040*SL	0.26 + 0.038*SL
	t_R	1.82	1.20 + 0.306*SL	1.20 + 0.307*SL	1.19 + 0.308*SL
	t_F	0.57	0.43 + 0.071*SL	0.43 + 0.072*SL	0.41 + 0.074*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

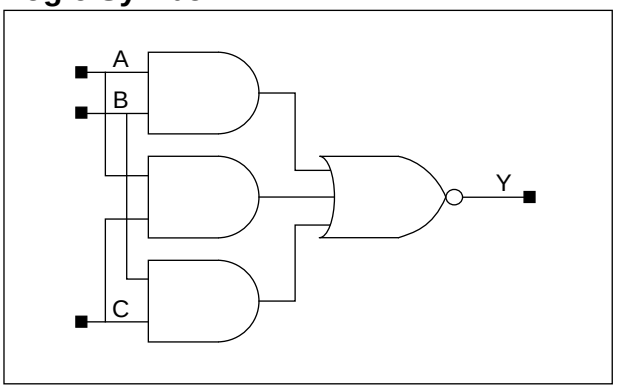
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.96	0.91 + 0.027*SL	0.91 + 0.025*SL	0.91 + 0.025*SL
	t_{PHL}	0.54	0.50 + 0.020*SL	0.51 + 0.015*SL	0.54 + 0.012*SL
	t_R	0.26	0.16 + 0.049*SL	0.15 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.16	0.12 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
B to Y	t_{PLH}	1.07	1.01 + 0.027*SL	1.02 + 0.025*SL	1.02 + 0.025*SL
	t_{PHL}	0.53	0.49 + 0.019*SL	0.50 + 0.015*SL	0.53 + 0.012*SL
	t_R	0.26	0.16 + 0.051*SL	0.16 + 0.052*SL	0.14 + 0.054*SL
	t_F	0.16	0.11 + 0.024*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
C to Y	t_{PLH}	1.17	1.12 + 0.027*SL	1.13 + 0.025*SL	1.13 + 0.025*SL
	t_{PHL}	0.61	0.57 + 0.020*SL	0.58 + 0.015*SL	0.61 + 0.012*SL
	t_R	0.26	0.16 + 0.049*SL	0.15 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.16	0.12 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.021*SL
D to Y	t_{PLH}	1.28	1.23 + 0.028*SL	1.23 + 0.025*SL	1.24 + 0.025*SL
	t_{PHL}	0.60	0.56 + 0.020*SL	0.57 + 0.015*SL	0.59 + 0.012*SL
	t_R	0.26	0.16 + 0.051*SL	0.16 + 0.051*SL	0.14 + 0.054*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
E to Y	t_{PLH}	1.32	1.27 + 0.028*SL	1.27 + 0.025*SL	1.27 + 0.025*SL
	t_{PHL}	0.65	0.61 + 0.020*SL	0.63 + 0.015*SL	0.65 + 0.012*SL
	t_R	0.26	0.16 + 0.049*SL	0.15 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
F to Y	t_{PLH}	1.43	1.38 + 0.027*SL	1.38 + 0.025*SL	1.38 + 0.025*SL
	t_{PHL}	0.64	0.60 + 0.020*SL	0.62 + 0.015*SL	0.64 + 0.012*SL
	t_R	0.26	0.16 + 0.049*SL	0.16 + 0.052*SL	0.14 + 0.054*SL
	t_F	0.16	0.12 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
AO222A			*AO222D2A*			*AO222A*	*AO222D2A*
A	B	C	A	B	C		
1.1	1.4	1.5	1.2	1.4	1.5	3.0	5.0
KGM80							
AO222A			*AO222D2A*			*AO222A*	*AO222D2A*
A	B	C	A	B	C		
2.1	2.0	2.0	2.1	2.1	2.0	3.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO222A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.31 + 0.090*SL	0.31 + 0.089*SL	0.32 + 0.088*SL
	t_{PHL}	0.23	0.15 + 0.042*SL	0.17 + 0.035*SL	0.17 + 0.035*SL
	t_R	0.90	0.51 + 0.195*SL	0.50 + 0.198*SL	0.49 + 0.199*SL
	t_F	0.40	0.28 + 0.061*SL	0.28 + 0.064*SL	0.26 + 0.066*SL
B to Y	t_{PLH}	0.52	0.35 + 0.085*SL	0.34 + 0.085*SL	0.34 + 0.086*SL
	t_{PHL}	0.24	0.16 + 0.041*SL	0.17 + 0.038*SL	0.18 + 0.036*SL
	t_R	0.91	0.52 + 0.196*SL	0.52 + 0.198*SL	0.51 + 0.199*SL
	t_F	0.44	0.31 + 0.063*SL	0.31 + 0.065*SL	0.29 + 0.067*SL
C to Y	t_{PLH}	0.58	0.41 + 0.087*SL	0.41 + 0.086*SL	0.41 + 0.086*SL
	t_{PHL}	0.22	0.13 + 0.043*SL	0.15 + 0.038*SL	0.16 + 0.036*SL
	t_R	0.89	0.51 + 0.192*SL	0.50 + 0.196*SL	0.49 + 0.198*SL
	t_F	0.44	0.31 + 0.063*SL	0.30 + 0.065*SL	0.29 + 0.067*SL

KG80 AO222D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.60	0.56 + 0.022*SL	0.56 + 0.020*SL	0.56 + 0.021*SL
	t_{PHL}	0.43	0.40 + 0.018*SL	0.41 + 0.014*SL	0.42 + 0.012*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.020*SL
B to Y	t_{PLH}	0.63	0.59 + 0.023*SL	0.59 + 0.020*SL	0.59 + 0.020*SL
	t_{PHL}	0.45	0.41 + 0.017*SL	0.42 + 0.014*SL	0.43 + 0.012*SL
	t_R	0.19	0.11 + 0.038*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
C to Y	t_{PLH}	0.71	0.67 + 0.022*SL	0.67 + 0.021*SL	0.67 + 0.020*SL
	t_{PHL}	0.42	0.39 + 0.018*SL	0.40 + 0.014*SL	0.41 + 0.012*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.13	0.09 + 0.019*SL	0.09 + 0.019*SL	0.09 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO222A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.73	0.48 + 0.126*SL	0.49 + 0.121*SL	0.51 + 0.119*SL
	t_{PHL}	0.29	0.20 + 0.044*SL	0.22 + 0.039*SL	0.23 + 0.038*SL
	t_R	1.30	0.78 + 0.256*SL	0.78 + 0.258*SL	0.78 + 0.258*SL
	t_F	0.47	0.34 + 0.068*SL	0.33 + 0.071*SL	0.30 + 0.074*SL
B to Y	t_{PLH}	0.81	0.57 + 0.122*SL	0.58 + 0.120*SL	0.59 + 0.118*SL
	t_{PHL}	0.30	0.21 + 0.045*SL	0.22 + 0.041*SL	0.25 + 0.039*SL
	t_R	1.30	0.80 + 0.253*SL	0.79 + 0.257*SL	0.78 + 0.258*SL
	t_F	0.51	0.36 + 0.072*SL	0.36 + 0.073*SL	0.35 + 0.074*SL
C to Y	t_{PLH}	0.90	0.66 + 0.118*SL	0.67 + 0.117*SL	0.67 + 0.116*SL
	t_{PHL}	0.28	0.19 + 0.047*SL	0.21 + 0.041*SL	0.23 + 0.039*SL
	t_R	1.28	0.77 + 0.251*SL	0.76 + 0.255*SL	0.75 + 0.257*SL
	t_F	0.51	0.36 + 0.073*SL	0.36 + 0.073*SL	0.36 + 0.074*SL

KGM80 AO222D2A

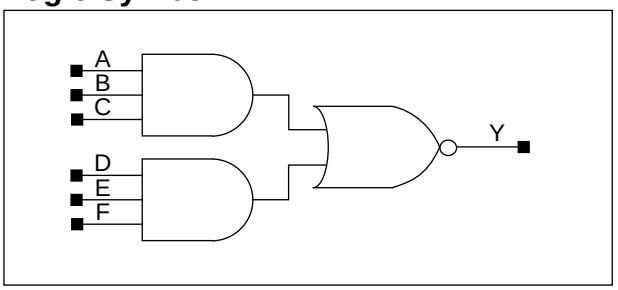
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.91	0.86 + 0.027*SL	0.86 + 0.025*SL	0.86 + 0.025*SL
	t_{PHL}	0.59	0.55 + 0.020*SL	0.57 + 0.015*SL	0.59 + 0.012*SL
	t_R	0.25	0.15 + 0.050*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
B to Y	t_{PLH}	1.03	0.98 + 0.026*SL	0.98 + 0.025*SL	0.98 + 0.025*SL
	t_{PHL}	0.60	0.56 + 0.020*SL	0.57 + 0.015*SL	0.60 + 0.012*SL
	t_R	0.25	0.15 + 0.050*SL	0.14 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.16	0.12 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.021*SL
C to Y	t_{PLH}	1.11	1.06 + 0.026*SL	1.07 + 0.025*SL	1.07 + 0.025*SL
	t_{PHL}	0.58	0.55 + 0.020*SL	0.56 + 0.015*SL	0.58 + 0.012*SL
	t_R	0.25	0.15 + 0.049*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.020*SL	0.12 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

AO33/AO33D2

Two 3-ANDs into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
Other States						1

Cell Data

Input Load (SL)												Gate Count	
KG80													
AO33						*AO33D2*						*AO33*	*AO33D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.5	0.5	0.8	0.5	0.5	0.8	0.5	0.6	0.8	0.5	0.6	0.8	3.0	5.0
KGM80													
AO33						*AO33D2*						*AO33*	*AO33D2*
A	B	C	D	E	F	A	B	C	D	E	F		
1.0	1.0	1.0	0.9	0.8	0.9	1.0	1.0	1.0	0.9	0.8	0.9	3.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.43	0.29 + 0.071*SL	0.29 + 0.071*SL	0.29 + 0.071*SL
	t_{PHL}	0.24	0.15 + 0.048*SL	0.15 + 0.045*SL	0.15 + 0.045*SL
	t_R	0.79	0.48 + 0.156*SL	0.47 + 0.161*SL	0.45 + 0.163*SL
	t_F	0.53	0.37 + 0.081*SL	0.35 + 0.089*SL	0.33 + 0.092*SL
B to Y	t_{PLH}	0.49	0.35 + 0.071*SL	0.35 + 0.071*SL	0.35 + 0.071*SL
	t_{PHL}	0.25	0.15 + 0.049*SL	0.16 + 0.046*SL	0.17 + 0.045*SL
	t_R	0.88	0.57 + 0.157*SL	0.56 + 0.161*SL	0.54 + 0.163*SL
	t_F	0.53	0.36 + 0.085*SL	0.34 + 0.090*SL	0.32 + 0.093*SL
C to Y	t_{PLH}	0.53	0.39 + 0.070*SL	0.39 + 0.071*SL	0.38 + 0.071*SL
	t_{PHL}	0.24	0.15 + 0.049*SL	0.15 + 0.047*SL	0.16 + 0.045*SL
	t_R	0.95	0.64 + 0.155*SL	0.63 + 0.160*SL	0.61 + 0.163*SL
	t_F	0.51	0.34 + 0.085*SL	0.33 + 0.091*SL	0.31 + 0.094*SL
D to Y	t_{PLH}	0.49	0.34 + 0.073*SL	0.35 + 0.072*SL	0.35 + 0.072*SL
	t_{PHL}	0.32	0.23 + 0.044*SL	0.23 + 0.045*SL	0.23 + 0.045*SL
	t_R	0.80	0.49 + 0.156*SL	0.48 + 0.160*SL	0.47 + 0.162*SL
	t_F	0.60	0.43 + 0.086*SL	0.42 + 0.089*SL	0.40 + 0.093*SL
E to Y	t_{PLH}	0.55	0.40 + 0.072*SL	0.40 + 0.072*SL	0.41 + 0.071*SL
	t_{PHL}	0.33	0.23 + 0.047*SL	0.24 + 0.046*SL	0.24 + 0.045*SL
	t_R	0.89	0.57 + 0.157*SL	0.56 + 0.161*SL	0.55 + 0.163*SL
	t_F	0.59	0.42 + 0.087*SL	0.41 + 0.091*SL	0.39 + 0.093*SL
F to Y	t_{PLH}	0.59	0.44 + 0.072*SL	0.44 + 0.072*SL	0.44 + 0.071*SL
	t_{PHL}	0.32	0.23 + 0.047*SL	0.23 + 0.046*SL	0.23 + 0.045*SL
	t_R	0.95	0.64 + 0.158*SL	0.63 + 0.160*SL	0.62 + 0.163*SL
	t_F	0.58	0.41 + 0.089*SL	0.40 + 0.092*SL	0.39 + 0.094*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO33D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.52 + 0.021*SL	0.53 + 0.020*SL	0.52 + 0.021*SL
	t_{PHL}	0.46	0.43 + 0.018*SL	0.44 + 0.014*SL	0.45 + 0.012*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.019*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
B to Y	t_{PLH}	0.61	0.57 + 0.022*SL	0.57 + 0.020*SL	0.57 + 0.021*SL
	t_{PHL}	0.46	0.43 + 0.018*SL	0.44 + 0.014*SL	0.45 + 0.012*SL
	t_R	0.19	0.11 + 0.038*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.019*SL	0.10 + 0.019*SL	0.10 + 0.019*SL
C to Y	t_{PLH}	0.67	0.62 + 0.022*SL	0.63 + 0.020*SL	0.62 + 0.020*SL
	t_{PHL}	0.47	0.43 + 0.018*SL	0.44 + 0.014*SL	0.45 + 0.012*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.14	0.10 + 0.020*SL	0.10 + 0.019*SL	0.10 + 0.019*SL
D to Y	t_{PLH}	0.65	0.61 + 0.022*SL	0.61 + 0.020*SL	0.61 + 0.021*SL
	t_{PHL}	0.57	0.54 + 0.018*SL	0.54 + 0.014*SL	0.56 + 0.012*SL
	t_R	0.19	0.11 + 0.039*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.018*SL	0.11 + 0.019*SL	0.10 + 0.020*SL
E to Y	t_{PLH}	0.70	0.65 + 0.023*SL	0.66 + 0.020*SL	0.66 + 0.020*SL
	t_{PHL}	0.57	0.53 + 0.018*SL	0.54 + 0.014*SL	0.56 + 0.012*SL
	t_R	0.19	0.11 + 0.038*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.10 + 0.020*SL
F to Y	t_{PLH}	0.75	0.71 + 0.022*SL	0.71 + 0.020*SL	0.71 + 0.020*SL
	t_{PHL}	0.57	0.54 + 0.018*SL	0.54 + 0.014*SL	0.56 + 0.012*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.15	0.11 + 0.019*SL	0.11 + 0.019*SL	0.11 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.62	0.43 + 0.096*SL	0.43 + 0.095*SL	0.44 + 0.094*SL
	t_{PHL}	0.29	0.19 + 0.054*SL	0.19 + 0.052*SL	0.20 + 0.051*SL
	t_R	1.12	0.72 + 0.204*SL	0.71 + 0.207*SL	0.70 + 0.208*SL
	t_F	0.58	0.39 + 0.097*SL	0.38 + 0.102*SL	0.34 + 0.105*SL
B to Y	t_{PLH}	0.72	0.53 + 0.095*SL	0.53 + 0.094*SL	0.53 + 0.094*SL
	t_{PHL}	0.32	0.21 + 0.055*SL	0.22 + 0.052*SL	0.22 + 0.052*SL
	t_R	1.24	0.83 + 0.205*SL	0.83 + 0.208*SL	0.82 + 0.208*SL
	t_F	0.65	0.45 + 0.099*SL	0.44 + 0.103*SL	0.41 + 0.105*SL
C to Y	t_{PLH}	0.78	0.59 + 0.096*SL	0.59 + 0.094*SL	0.60 + 0.094*SL
	t_{PHL}	0.32	0.21 + 0.055*SL	0.21 + 0.053*SL	0.22 + 0.052*SL
	t_R	1.34	0.93 + 0.204*SL	0.92 + 0.208*SL	0.91 + 0.208*SL
	t_F	0.64	0.44 + 0.100*SL	0.43 + 0.104*SL	0.41 + 0.105*SL
D to Y	t_{PLH}	0.74	0.54 + 0.097*SL	0.55 + 0.095*SL	0.56 + 0.094*SL
	t_{PHL}	0.41	0.30 + 0.054*SL	0.31 + 0.052*SL	0.31 + 0.051*SL
	t_R	1.13	0.73 + 0.202*SL	0.72 + 0.207*SL	0.70 + 0.208*SL
	t_F	0.66	0.46 + 0.100*SL	0.45 + 0.103*SL	0.43 + 0.105*SL
E to Y	t_{PLH}	0.84	0.64 + 0.096*SL	0.65 + 0.095*SL	0.66 + 0.094*SL
	t_{PHL}	0.44	0.33 + 0.053*SL	0.33 + 0.052*SL	0.34 + 0.051*SL
	t_R	1.25	0.84 + 0.204*SL	0.83 + 0.207*SL	0.82 + 0.208*SL
	t_F	0.65	0.45 + 0.102*SL	0.44 + 0.104*SL	0.43 + 0.105*SL
F to Y	t_{PLH}	0.90	0.71 + 0.097*SL	0.71 + 0.095*SL	0.72 + 0.094*SL
	t_{PHL}	0.44	0.33 + 0.054*SL	0.33 + 0.052*SL	0.34 + 0.051*SL
	t_R	1.35	0.94 + 0.203*SL	0.93 + 0.207*SL	0.92 + 0.208*SL
	t_F	0.64	0.44 + 0.103*SL	0.43 + 0.104*SL	0.42 + 0.105*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

AO33/AO33D2

Two 3-ANDs into 2-NOR with 1X/2X Drive

Switching Characteristics

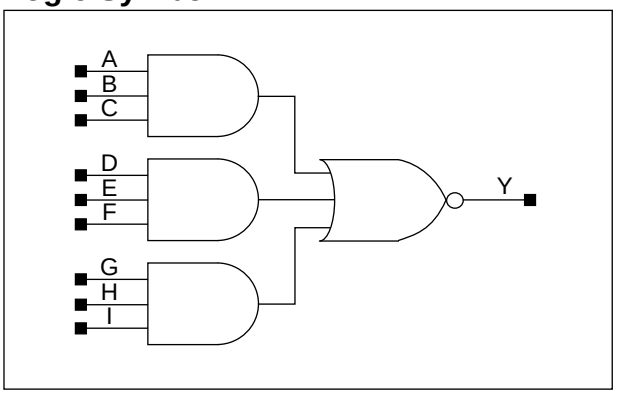
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO33D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.83	0.77 + 0.026*SL	0.78 + 0.025*SL	0.78 + 0.025*SL
	t_{PHL}	0.63	0.59 + 0.020*SL	0.60 + 0.015*SL	0.63 + 0.012*SL
	t_R	0.25	0.15 + 0.050*SL	0.14 + 0.052*SL	0.12 + 0.054*SL
	t_F	0.17	0.13 + 0.023*SL	0.13 + 0.020*SL	0.14 + 0.020*SL
B to Y	t_{PLH}	0.90	0.85 + 0.026*SL	0.85 + 0.025*SL	0.85 + 0.025*SL
	t_{PHL}	0.64	0.60 + 0.020*SL	0.61 + 0.015*SL	0.64 + 0.012*SL
	t_R	0.25	0.15 + 0.050*SL	0.14 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.17	0.13 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
C to Y	t_{PLH}	1.00	0.94 + 0.027*SL	0.95 + 0.025*SL	0.95 + 0.025*SL
	t_{PHL}	0.65	0.61 + 0.020*SL	0.63 + 0.015*SL	0.66 + 0.012*SL
	t_R	0.25	0.16 + 0.049*SL	0.15 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.17	0.13 + 0.022*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
D to Y	t_{PLH}	1.00	0.94 + 0.026*SL	0.95 + 0.025*SL	0.95 + 0.025*SL
	t_{PHL}	0.77	0.73 + 0.020*SL	0.74 + 0.015*SL	0.77 + 0.013*SL
	t_R	0.25	0.15 + 0.050*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
E to Y	t_{PLH}	1.08	1.02 + 0.026*SL	1.03 + 0.025*SL	1.03 + 0.025*SL
	t_{PHL}	0.78	0.74 + 0.021*SL	0.76 + 0.015*SL	0.79 + 0.012*SL
	t_R	0.25	0.15 + 0.049*SL	0.14 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
F to Y	t_{PLH}	1.17	1.12 + 0.027*SL	1.12 + 0.025*SL	1.12 + 0.025*SL
	t_{PHL}	0.80	0.76 + 0.020*SL	0.77 + 0.015*SL	0.80 + 0.012*SL
	t_R	0.25	0.15 + 0.049*SL	0.15 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.020*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Y
1	1	1	x	x	x	x	x	x	0
x	x	x	1	1	1	x	x	x	0
x	x	x	x	x	x	1	1	1	0
Other States									1

Cell Data

Input Load (SL)									Gate Count
KG80									
AO333									*AO333*
A	B	C	D	E	F	G	H	I	
0.5	0.5	0.8	0.5	0.5	0.8	0.5	0.6	0.7	5.0
AO333D2									*AO333D2*
A	B	C	D	E	F	G	H	I	
0.5	0.5	0.7	0.5	0.5	0.8	0.5	0.6	0.7	7.0
KGM80									
AO333									*AO333*
A	B	C	D	E	F	G	H	I	
1.0	1.0	1.0	0.9	0.8	0.9	0.9	0.8	0.9	5.0
AO333D2									*AO333D2*
A	B	C	D	E	F	G	H	I	
1.0	1.0	1.0	0.9	0.8	0.9	0.9	0.8	0.9	7.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO333

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.74	0.53 + 0.102*SL	0.53 + 0.102*SL	0.53 + 0.102*SL
	t_{PHL}	0.31	0.22 + 0.047*SL	0.22 + 0.046*SL	0.22 + 0.045*SL
	t_R	1.64	1.16 + 0.237*SL	1.15 + 0.240*SL	1.16 + 0.240*SL
	t_F	0.71	0.55 + 0.084*SL	0.53 + 0.090*SL	0.51 + 0.093*SL
B to Y	t_{PLH}	0.79	0.59 + 0.102*SL	0.59 + 0.102*SL	0.59 + 0.102*SL
	t_{PHL}	0.31	0.22 + 0.047*SL	0.22 + 0.046*SL	0.22 + 0.046*SL
	t_R	1.73	1.25 + 0.238*SL	1.25 + 0.240*SL	1.25 + 0.239*SL
	t_F	0.71	0.53 + 0.086*SL	0.52 + 0.091*SL	0.50 + 0.094*SL
C to Y	t_{PLH}	0.87	0.67 + 0.102*SL	0.67 + 0.102*SL	0.67 + 0.102*SL
	t_{PHL}	0.31	0.22 + 0.048*SL	0.22 + 0.047*SL	0.23 + 0.045*SL
	t_R	1.86	1.38 + 0.238*SL	1.38 + 0.240*SL	1.38 + 0.239*SL
	t_F	0.69	0.52 + 0.088*SL	0.51 + 0.092*SL	0.49 + 0.094*SL
D to Y	t_{PLH}	0.94	0.73 + 0.105*SL	0.73 + 0.104*SL	0.74 + 0.103*SL
	t_{PHL}	0.40	0.31 + 0.049*SL	0.31 + 0.047*SL	0.32 + 0.046*SL
	t_R	1.69	1.22 + 0.233*SL	1.22 + 0.235*SL	1.21 + 0.236*SL
	t_F	0.89	0.72 + 0.085*SL	0.71 + 0.089*SL	0.68 + 0.093*SL
E to Y	t_{PLH}	1.03	0.82 + 0.104*SL	0.82 + 0.103*SL	0.83 + 0.103*SL
	t_{PHL}	0.42	0.32 + 0.049*SL	0.32 + 0.047*SL	0.33 + 0.046*SL
	t_R	1.81	1.35 + 0.233*SL	1.34 + 0.235*SL	1.34 + 0.236*SL
	t_F	0.87	0.70 + 0.088*SL	0.69 + 0.091*SL	0.68 + 0.093*SL
F to Y	t_{PLH}	1.09	0.88 + 0.104*SL	0.88 + 0.103*SL	0.88 + 0.103*SL
	t_{PHL}	0.41	0.31 + 0.049*SL	0.32 + 0.047*SL	0.32 + 0.046*SL
	t_R	1.91	1.44 + 0.234*SL	1.44 + 0.235*SL	1.43 + 0.236*SL
	t_F	0.87	0.69 + 0.089*SL	0.68 + 0.092*SL	0.67 + 0.093*SL
G to Y	t_{PLH}	1.02	0.81 + 0.106*SL	0.81 + 0.104*SL	0.82 + 0.103*SL
	t_{PHL}	0.44	0.34 + 0.051*SL	0.34 + 0.049*SL	0.35 + 0.047*SL
	t_R	1.69	1.23 + 0.232*SL	1.22 + 0.235*SL	1.21 + 0.236*SL
	t_F	1.00	0.82 + 0.086*SL	0.82 + 0.090*SL	0.80 + 0.093*SL
H to Y	t_{PLH}	1.10	0.89 + 0.104*SL	0.90 + 0.104*SL	0.90 + 0.103*SL
	t_{PHL}	0.45	0.35 + 0.052*SL	0.36 + 0.049*SL	0.37 + 0.047*SL
	t_R	1.82	1.35 + 0.234*SL	1.34 + 0.235*SL	1.34 + 0.236*SL
	t_F	0.99	0.81 + 0.089*SL	0.80 + 0.092*SL	0.79 + 0.094*SL
I to Y	t_{PLH}	1.16	0.95 + 0.104*SL	0.96 + 0.103*SL	0.96 + 0.103*SL
	t_{PHL}	0.44	0.34 + 0.051*SL	0.35 + 0.049*SL	0.36 + 0.047*SL
	t_R	1.91	1.44 + 0.233*SL	1.44 + 0.235*SL	1.43 + 0.236*SL
	t_F	0.98	0.80 + 0.090*SL	0.79 + 0.093*SL	0.78 + 0.094*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 AO333D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.77	0.73 + 0.022*SL	0.73 + 0.021*SL	0.73 + 0.021*SL
	t_{PHL}	0.52	0.49 + 0.018*SL	0.50 + 0.014*SL	0.51 + 0.012*SL
	t_R	0.20	0.12 + 0.040*SL	0.12 + 0.042*SL	0.11 + 0.044*SL
	t_F	0.15	0.10 + 0.022*SL	0.11 + 0.019*SL	0.11 + 0.019*SL
B to Y	t_{PLH}	0.83	0.78 + 0.023*SL	0.79 + 0.021*SL	0.79 + 0.021*SL
	t_{PHL}	0.52	0.49 + 0.018*SL	0.49 + 0.014*SL	0.51 + 0.012*SL
	t_R	0.21	0.13 + 0.040*SL	0.12 + 0.042*SL	0.11 + 0.044*SL
	t_F	0.15	0.11 + 0.018*SL	0.11 + 0.019*SL	0.11 + 0.019*SL
C to Y	t_{PLH}	0.90	0.85 + 0.023*SL	0.85 + 0.021*SL	0.86 + 0.021*SL
	t_{PHL}	0.52	0.48 + 0.018*SL	0.49 + 0.014*SL	0.51 + 0.012*SL
	t_R	0.21	0.13 + 0.040*SL	0.13 + 0.042*SL	0.12 + 0.044*SL
	t_F	0.15	0.11 + 0.018*SL	0.11 + 0.019*SL	0.11 + 0.019*SL
D to Y	t_{PLH}	0.97	0.92 + 0.023*SL	0.93 + 0.021*SL	0.93 + 0.020*SL
	t_{PHL}	0.64	0.60 + 0.018*SL	0.61 + 0.014*SL	0.63 + 0.012*SL
	t_R	0.20	0.13 + 0.040*SL	0.12 + 0.042*SL	0.11 + 0.044*SL
	t_F	0.15	0.12 + 0.018*SL	0.12 + 0.019*SL	0.12 + 0.019*SL
E to Y	t_{PLH}	1.05	1.00 + 0.023*SL	1.01 + 0.021*SL	1.01 + 0.021*SL
	t_{PHL}	0.65	0.61 + 0.018*SL	0.62 + 0.014*SL	0.64 + 0.012*SL
	t_R	0.21	0.13 + 0.040*SL	0.12 + 0.043*SL	0.12 + 0.043*SL
	t_F	0.15	0.12 + 0.020*SL	0.12 + 0.019*SL	0.12 + 0.019*SL
F to Y	t_{PLH}	1.10	1.06 + 0.023*SL	1.06 + 0.021*SL	1.06 + 0.021*SL
	t_{PHL}	0.64	0.61 + 0.018*SL	0.62 + 0.015*SL	0.63 + 0.012*SL
	t_R	0.21	0.13 + 0.040*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.15	0.11 + 0.020*SL	0.12 + 0.019*SL	0.12 + 0.019*SL
G to Y	t_{PLH}	1.04	1.00 + 0.022*SL	1.00 + 0.021*SL	1.00 + 0.020*SL
	t_{PHL}	0.69	0.66 + 0.018*SL	0.67 + 0.015*SL	0.68 + 0.012*SL
	t_R	0.21	0.13 + 0.038*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.16	0.12 + 0.019*SL	0.12 + 0.019*SL	0.12 + 0.019*SL
H to Y	t_{PLH}	1.12	1.08 + 0.023*SL	1.08 + 0.021*SL	1.08 + 0.021*SL
	t_{PHL}	0.70	0.67 + 0.019*SL	0.68 + 0.015*SL	0.69 + 0.012*SL
	t_R	0.21	0.13 + 0.041*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.16	0.12 + 0.020*SL	0.12 + 0.018*SL	0.12 + 0.019*SL
I to Y	t_{PLH}	1.18	1.13 + 0.023*SL	1.14 + 0.021*SL	1.14 + 0.021*SL
	t_{PHL}	0.70	0.66 + 0.018*SL	0.67 + 0.015*SL	0.68 + 0.013*SL
	t_R	0.21	0.13 + 0.040*SL	0.13 + 0.042*SL	0.12 + 0.044*SL
	t_F	0.16	0.12 + 0.018*SL	0.12 + 0.019*SL	0.12 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO333

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.12	0.83 + 0.142*SL	0.84 + 0.140*SL	0.85 + 0.139*SL
	t_{PHL}	0.37	0.26 + 0.054*SL	0.26 + 0.054*SL	0.28 + 0.052*SL
	t_R	2.39	1.76 + 0.314*SL	1.76 + 0.314*SL	1.80 + 0.310*SL
	t_F	0.90	0.70 + 0.098*SL	0.69 + 0.102*SL	0.66 + 0.105*SL
B to Y	t_{PLH}	1.22	0.94 + 0.141*SL	0.94 + 0.140*SL	0.95 + 0.139*SL
	t_{PHL}	0.38	0.27 + 0.054*SL	0.27 + 0.054*SL	0.29 + 0.052*SL
	t_R	2.53	1.90 + 0.314*SL	1.90 + 0.314*SL	1.94 + 0.310*SL
	t_F	0.89	0.69 + 0.099*SL	0.68 + 0.103*SL	0.66 + 0.105*SL
C to Y	t_{PLH}	1.36	1.08 + 0.141*SL	1.08 + 0.140*SL	1.09 + 0.139*SL
	t_{PHL}	0.39	0.28 + 0.054*SL	0.28 + 0.054*SL	0.30 + 0.052*SL
	t_R	2.72	2.09 + 0.314*SL	2.09 + 0.313*SL	2.13 + 0.310*SL
	t_F	0.88	0.68 + 0.101*SL	0.67 + 0.104*SL	0.66 + 0.105*SL
D to Y	t_{PLH}	1.52	1.23 + 0.143*SL	1.24 + 0.141*SL	1.25 + 0.140*SL
	t_{PHL}	0.49	0.38 + 0.058*SL	0.38 + 0.055*SL	0.41 + 0.053*SL
	t_R	2.48	1.87 + 0.304*SL	1.87 + 0.306*SL	1.85 + 0.308*SL
	t_F	1.12	0.92 + 0.098*SL	0.91 + 0.102*SL	0.88 + 0.105*SL
E to Y	t_{PLH}	1.67	1.38 + 0.142*SL	1.39 + 0.141*SL	1.40 + 0.140*SL
	t_{PHL}	0.52	0.41 + 0.059*SL	0.42 + 0.055*SL	0.44 + 0.053*SL
	t_R	2.66	2.05 + 0.305*SL	2.05 + 0.307*SL	2.04 + 0.308*SL
	t_F	1.11	0.91 + 0.099*SL	0.91 + 0.103*SL	0.89 + 0.105*SL
F to Y	t_{PLH}	1.77	1.49 + 0.142*SL	1.49 + 0.140*SL	1.50 + 0.139*SL
	t_{PHL}	0.52	0.41 + 0.058*SL	0.41 + 0.055*SL	0.44 + 0.053*SL
	t_R	2.80	2.19 + 0.305*SL	2.18 + 0.307*SL	2.17 + 0.308*SL
	t_F	1.11	0.90 + 0.101*SL	0.90 + 0.103*SL	0.88 + 0.105*SL
G to Y	t_{PLH}	1.65	1.37 + 0.143*SL	1.37 + 0.141*SL	1.39 + 0.140*SL
	t_{PHL}	0.53	0.41 + 0.062*SL	0.42 + 0.058*SL	0.46 + 0.054*SL
	t_R	2.49	1.88 + 0.303*SL	1.87 + 0.306*SL	1.86 + 0.308*SL
	t_F	1.27	1.07 + 0.099*SL	1.06 + 0.103*SL	1.03 + 0.105*SL
H to Y	t_{PLH}	1.80	1.52 + 0.143*SL	1.52 + 0.141*SL	1.53 + 0.140*SL
	t_{PHL}	0.56	0.44 + 0.062*SL	0.45 + 0.058*SL	0.49 + 0.054*SL
	t_R	2.67	2.06 + 0.305*SL	2.05 + 0.307*SL	2.04 + 0.308*SL
	t_F	1.26	1.06 + 0.101*SL	1.05 + 0.103*SL	1.04 + 0.105*SL
I to Y	t_{PLH}	1.90	1.62 + 0.142*SL	1.62 + 0.140*SL	1.63 + 0.140*SL
	t_{PHL}	0.56	0.44 + 0.062*SL	0.45 + 0.058*SL	0.49 + 0.054*SL
	t_R	2.80	2.19 + 0.305*SL	2.19 + 0.307*SL	2.17 + 0.308*SL
	t_F	1.25	1.05 + 0.103*SL	1.04 + 0.104*SL	1.04 + 0.105*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 AO333D2

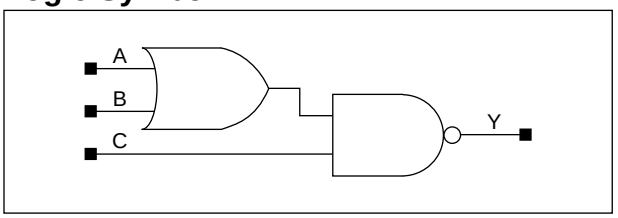
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.19	1.13 + 0.028*SL	1.14 + 0.025*SL	1.15 + 0.025*SL
	t_{PHL}	0.70	0.66 + 0.020*SL	0.67 + 0.015*SL	0.70 + 0.012*SL
	t_R	0.27	0.17 + 0.051*SL	0.17 + 0.051*SL	0.15 + 0.053*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
B to Y	t_{PLH}	1.29	1.24 + 0.028*SL	1.25 + 0.025*SL	1.25 + 0.025*SL
	t_{PHL}	0.71	0.67 + 0.021*SL	0.68 + 0.015*SL	0.71 + 0.013*SL
	t_R	0.28	0.18 + 0.049*SL	0.17 + 0.051*SL	0.15 + 0.053*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
C to Y	t_{PLH}	1.41	1.36 + 0.029*SL	1.36 + 0.025*SL	1.37 + 0.025*SL
	t_{PHL}	0.72	0.68 + 0.021*SL	0.69 + 0.015*SL	0.72 + 0.013*SL
	t_R	0.28	0.18 + 0.050*SL	0.18 + 0.051*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
D to Y	t_{PLH}	1.57	1.52 + 0.028*SL	1.52 + 0.025*SL	1.53 + 0.025*SL
	t_{PHL}	0.86	0.81 + 0.021*SL	0.83 + 0.015*SL	0.86 + 0.013*SL
	t_R	0.27	0.17 + 0.050*SL	0.17 + 0.051*SL	0.14 + 0.053*SL
	t_F	0.19	0.14 + 0.024*SL	0.15 + 0.020*SL	0.15 + 0.020*SL
E to Y	t_{PLH}	1.72	1.66 + 0.028*SL	1.67 + 0.025*SL	1.68 + 0.025*SL
	t_{PHL}	0.89	0.84 + 0.021*SL	0.86 + 0.015*SL	0.89 + 0.013*SL
	t_R	0.28	0.18 + 0.050*SL	0.17 + 0.051*SL	0.15 + 0.053*SL
	t_F	0.18	0.14 + 0.025*SL	0.15 + 0.020*SL	0.15 + 0.020*SL
F to Y	t_{PLH}	1.82	1.76 + 0.028*SL	1.77 + 0.025*SL	1.78 + 0.025*SL
	t_{PHL}	0.88	0.84 + 0.021*SL	0.86 + 0.015*SL	0.89 + 0.013*SL
	t_R	0.28	0.18 + 0.051*SL	0.18 + 0.051*SL	0.16 + 0.053*SL
	t_F	0.18	0.14 + 0.024*SL	0.15 + 0.020*SL	0.15 + 0.020*SL
G to Y	t_{PLH}	1.71	1.65 + 0.028*SL	1.66 + 0.025*SL	1.66 + 0.025*SL
	t_{PHL}	0.92	0.88 + 0.021*SL	0.89 + 0.016*SL	0.92 + 0.013*SL
	t_R	0.27	0.17 + 0.049*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.14 + 0.023*SL	0.15 + 0.020*SL	0.15 + 0.020*SL
H to Y	t_{PLH}	1.85	1.80 + 0.028*SL	1.81 + 0.025*SL	1.81 + 0.025*SL
	t_{PHL}	0.95	0.90 + 0.021*SL	0.92 + 0.015*SL	0.95 + 0.013*SL
	t_R	0.28	0.18 + 0.050*SL	0.17 + 0.051*SL	0.15 + 0.053*SL
	t_F	0.19	0.15 + 0.021*SL	0.15 + 0.020*SL	0.16 + 0.020*SL
I to Y	t_{PLH}	1.95	1.89 + 0.028*SL	1.90 + 0.025*SL	1.91 + 0.025*SL
	t_{PHL}	0.95	0.90 + 0.021*SL	0.92 + 0.015*SL	0.95 + 0.013*SL
	t_R	0.28	0.18 + 0.050*SL	0.18 + 0.051*SL	0.16 + 0.053*SL
	t_F	0.19	0.15 + 0.022*SL	0.15 + 0.020*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

OA21/OA21D2

2-OR into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	x	1	0
x	1	1	0
0	0	x	1
x	x	0	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
OA21			*OA21D2*			*OA21*	*OA21D2*
A	B	C	A	B	C		
0.5	0.7	0.8	1.1	1.4	1.7	2.0	3.0
KGM80							
OA21			*OA21D2*			*OA21*	*OA21D2*
A	B	C	A	B	C		
1.0	1.0	1.0	2.0	1.9	2.0	2.0	3.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OA21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.19 + 0.068*SL	0.18 + 0.069*SL	0.18 + 0.071*SL
	t_{PHL}	0.16	0.07 + 0.044*SL	0.10 + 0.034*SL	0.10 + 0.034*SL
	t_R	0.56	0.26 + 0.152*SL	0.24 + 0.159*SL	0.22 + 0.163*SL
	t_F	0.30	0.19 + 0.058*SL	0.18 + 0.062*SL	0.15 + 0.065*SL
B to Y	t_{PLH}	0.32	0.19 + 0.069*SL	0.18 + 0.070*SL	0.18 + 0.071*SL
	t_{PHL}	0.18	0.10 + 0.040*SL	0.11 + 0.034*SL	0.12 + 0.034*SL
	t_R	0.56	0.26 + 0.152*SL	0.24 + 0.159*SL	0.22 + 0.162*SL
	t_F	0.35	0.23 + 0.059*SL	0.22 + 0.061*SL	0.20 + 0.065*SL
C to Y	t_{PLH}	0.29	0.21 + 0.039*SL	0.21 + 0.040*SL	0.20 + 0.041*SL
	t_{PHL}	0.19	0.11 + 0.038*SL	0.12 + 0.035*SL	0.13 + 0.034*SL
	t_R	0.42	0.26 + 0.080*SL	0.25 + 0.085*SL	0.22 + 0.089*SL
	t_F	0.31	0.20 + 0.058*SL	0.18 + 0.064*SL	0.16 + 0.067*SL

KG80 OA21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.035*SL
	t_{PHL}	0.11	0.05 + 0.027*SL	0.07 + 0.020*SL	0.09 + 0.017*SL
	t_R	0.38	0.24 + 0.073*SL	0.23 + 0.077*SL	0.21 + 0.080*SL
	t_F	0.23	0.16 + 0.034*SL	0.17 + 0.029*SL	0.16 + 0.031*SL
B to Y	t_{PLH}	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.14	0.09 + 0.024*SL	0.10 + 0.019*SL	0.11 + 0.017*SL
	t_R	0.38	0.24 + 0.073*SL	0.23 + 0.078*SL	0.21 + 0.080*SL
	t_F	0.28	0.23 + 0.029*SL	0.22 + 0.030*SL	0.22 + 0.030*SL
C to Y	t_{PLH}	0.24	0.20 + 0.021*SL	0.20 + 0.020*SL	0.20 + 0.020*SL
	t_{PHL}	0.14	0.10 + 0.021*SL	0.11 + 0.019*SL	0.12 + 0.017*SL
	t_R	0.32	0.24 + 0.038*SL	0.23 + 0.041*SL	0.22 + 0.042*SL
	t_F	0.26	0.18 + 0.036*SL	0.20 + 0.028*SL	0.17 + 0.032*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

OA21/OA21D2

2-OR into 2-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OA21

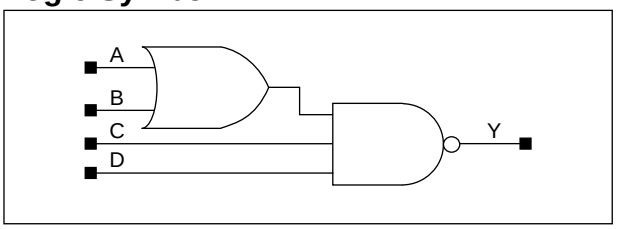
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.43	0.24 + 0.093*SL	0.24 + 0.094*SL	0.24 + 0.094*SL
	t_{PHL}	0.20	0.11 + 0.046*SL	0.13 + 0.038*SL	0.14 + 0.037*SL
	t_R	0.77	0.37 + 0.201*SL	0.36 + 0.206*SL	0.33 + 0.208*SL
	t_F	0.33	0.20 + 0.067*SL	0.19 + 0.070*SL	0.16 + 0.073*SL
B to Y	t_{PLH}	0.45	0.27 + 0.094*SL	0.26 + 0.094*SL	0.27 + 0.094*SL
	t_{PHL}	0.23	0.14 + 0.043*SL	0.16 + 0.037*SL	0.16 + 0.037*SL
	t_R	0.77	0.37 + 0.201*SL	0.36 + 0.206*SL	0.34 + 0.208*SL
	t_F	0.38	0.25 + 0.066*SL	0.24 + 0.070*SL	0.20 + 0.073*SL
C to Y	t_{PLH}	0.37	0.27 + 0.049*SL	0.27 + 0.050*SL	0.27 + 0.050*SL
	t_{PHL}	0.25	0.16 + 0.042*SL	0.18 + 0.038*SL	0.18 + 0.037*SL
	t_R	0.53	0.32 + 0.102*SL	0.31 + 0.106*SL	0.28 + 0.109*SL
	t_F	0.35	0.22 + 0.067*SL	0.20 + 0.072*SL	0.19 + 0.074*SL

KGM80 OA21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.21 + 0.048*SL	0.22 + 0.047*SL	0.21 + 0.047*SL
	t_{PHL}	0.14	0.08 + 0.027*SL	0.10 + 0.021*SL	0.12 + 0.018*SL
	t_R	0.52	0.32 + 0.099*SL	0.31 + 0.102*SL	0.29 + 0.103*SL
	t_F	0.25	0.17 + 0.037*SL	0.18 + 0.034*SL	0.16 + 0.035*SL
B to Y	t_{PLH}	0.35	0.25 + 0.049*SL	0.26 + 0.047*SL	0.26 + 0.047*SL
	t_{PHL}	0.18	0.12 + 0.025*SL	0.14 + 0.020*SL	0.15 + 0.019*SL
	t_R	0.52	0.32 + 0.098*SL	0.31 + 0.102*SL	0.30 + 0.103*SL
	t_F	0.31	0.24 + 0.032*SL	0.24 + 0.034*SL	0.22 + 0.035*SL
C to Y	t_{PLH}	0.30	0.25 + 0.025*SL	0.25 + 0.025*SL	0.25 + 0.025*SL
	t_{PHL}	0.19	0.15 + 0.023*SL	0.16 + 0.020*SL	0.17 + 0.019*SL
	t_R	0.39	0.29 + 0.049*SL	0.28 + 0.052*SL	0.27 + 0.053*SL
	t_F	0.27	0.21 + 0.034*SL	0.20 + 0.035*SL	0.19 + 0.036*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	x	1	1	0
x	1	1	1	0
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1

Cell Data

Input Load (SL)								Gate Count	
KG80									
OA211				*OA211D2*				*OA211*	*OA211D2*
A	B	C	D	A	B	C	D		
0.5	0.7	0.8	0.9	1.1	1.4	1.7	1.7	2.0	4.0
KGM80									
OA211				*OA211D2*				*OA211*	*OA211D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	2.0	1.9	2.0	1.9	2.0	4.0

OA211/OA211D2

2-OR into 3-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OA211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.19 + 0.068*SL	0.19 + 0.070*SL	0.18 + 0.071*SL
	t_{PHL}	0.20	0.10 + 0.050*SL	0.12 + 0.044*SL	0.11 + 0.045*SL
	t_R	0.58	0.27 + 0.152*SL	0.26 + 0.159*SL	0.23 + 0.163*SL
	t_F	0.39	0.23 + 0.083*SL	0.22 + 0.088*SL	0.19 + 0.092*SL
B to Y	t_{PLH}	0.33	0.19 + 0.070*SL	0.19 + 0.071*SL	0.19 + 0.071*SL
	t_{PHL}	0.23	0.13 + 0.047*SL	0.14 + 0.044*SL	0.13 + 0.045*SL
	t_R	0.58	0.27 + 0.153*SL	0.26 + 0.159*SL	0.24 + 0.162*SL
	t_F	0.45	0.28 + 0.084*SL	0.28 + 0.087*SL	0.24 + 0.092*SL
C to Y	t_{PLH}	0.29	0.21 + 0.041*SL	0.21 + 0.041*SL	0.20 + 0.041*SL
	t_{PHL}	0.25	0.16 + 0.047*SL	0.16 + 0.045*SL	0.16 + 0.045*SL
	t_R	0.43	0.27 + 0.078*SL	0.26 + 0.085*SL	0.23 + 0.089*SL
	t_F	0.42	0.26 + 0.084*SL	0.24 + 0.091*SL	0.22 + 0.093*SL
D to Y	t_{PLH}	0.31	0.23 + 0.041*SL	0.23 + 0.041*SL	0.23 + 0.041*SL
	t_{PHL}	0.24	0.15 + 0.047*SL	0.15 + 0.045*SL	0.16 + 0.045*SL
	t_R	0.47	0.31 + 0.079*SL	0.30 + 0.084*SL	0.27 + 0.089*SL
	t_F	0.41	0.24 + 0.086*SL	0.23 + 0.092*SL	0.21 + 0.094*SL

KG80 OA211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.15	0.09 + 0.028*SL	0.10 + 0.024*SL	0.12 + 0.022*SL
	t_R	0.43	0.28 + 0.073*SL	0.27 + 0.078*SL	0.26 + 0.080*SL
	t_F	0.31	0.23 + 0.039*SL	0.22 + 0.042*SL	0.21 + 0.045*SL
B to Y	t_{PLH}	0.27	0.20 + 0.037*SL	0.20 + 0.035*SL	0.20 + 0.035*SL
	t_{PHL}	0.19	0.14 + 0.026*SL	0.14 + 0.022*SL	0.14 + 0.023*SL
	t_R	0.43	0.28 + 0.074*SL	0.27 + 0.078*SL	0.26 + 0.080*SL
	t_F	0.38	0.31 + 0.039*SL	0.30 + 0.042*SL	0.29 + 0.044*SL
C to Y	t_{PLH}	0.25	0.20 + 0.021*SL	0.21 + 0.020*SL	0.20 + 0.020*SL
	t_{PHL}	0.21	0.16 + 0.025*SL	0.17 + 0.023*SL	0.17 + 0.023*SL
	t_R	0.34	0.27 + 0.038*SL	0.26 + 0.041*SL	0.25 + 0.042*SL
	t_F	0.36	0.27 + 0.042*SL	0.27 + 0.044*SL	0.26 + 0.046*SL
D to Y	t_{PLH}	0.27	0.23 + 0.020*SL	0.23 + 0.020*SL	0.23 + 0.021*SL
	t_{PHL}	0.21	0.16 + 0.025*SL	0.16 + 0.023*SL	0.17 + 0.023*SL
	t_R	0.39	0.31 + 0.039*SL	0.31 + 0.040*SL	0.30 + 0.042*SL
	t_F	0.34	0.26 + 0.041*SL	0.25 + 0.045*SL	0.24 + 0.046*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OA211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.25 + 0.094*SL	0.25 + 0.094*SL	0.25 + 0.094*SL
	t_{PHL}	0.25	0.14 + 0.055*SL	0.15 + 0.051*SL	0.15 + 0.051*SL
	t_R	0.80	0.39 + 0.201*SL	0.38 + 0.206*SL	0.36 + 0.208*SL
	t_F	0.46	0.26 + 0.098*SL	0.25 + 0.102*SL	0.22 + 0.105*SL
B to Y	t_{PLH}	0.47	0.28 + 0.095*SL	0.28 + 0.094*SL	0.28 + 0.094*SL
	t_{PHL}	0.29	0.18 + 0.053*SL	0.19 + 0.051*SL	0.19 + 0.051*SL
	t_R	0.80	0.39 + 0.201*SL	0.38 + 0.206*SL	0.36 + 0.208*SL
	t_F	0.52	0.33 + 0.096*SL	0.32 + 0.101*SL	0.28 + 0.105*SL
C to Y	t_{PLH}	0.37	0.27 + 0.050*SL	0.27 + 0.050*SL	0.28 + 0.050*SL
	t_{PHL}	0.34	0.23 + 0.054*SL	0.23 + 0.052*SL	0.24 + 0.051*SL
	t_R	0.54	0.34 + 0.101*SL	0.32 + 0.106*SL	0.30 + 0.109*SL
	t_F	0.50	0.30 + 0.100*SL	0.30 + 0.103*SL	0.28 + 0.105*SL
D to Y	t_{PLH}	0.40	0.30 + 0.051*SL	0.31 + 0.050*SL	0.31 + 0.050*SL
	t_{PHL}	0.33	0.23 + 0.054*SL	0.23 + 0.052*SL	0.24 + 0.051*SL
	t_R	0.59	0.39 + 0.101*SL	0.38 + 0.106*SL	0.35 + 0.109*SL
	t_F	0.50	0.29 + 0.101*SL	0.29 + 0.104*SL	0.27 + 0.105*SL

KGM80 OA211D2

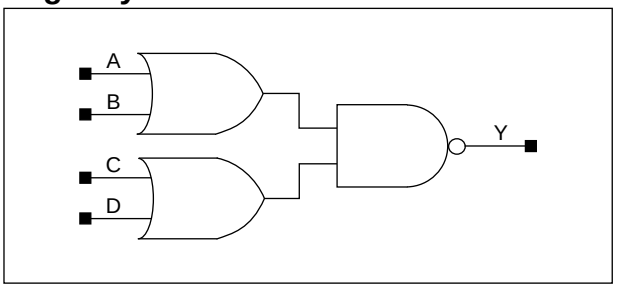
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.25 + 0.047*SL	0.25 + 0.047*SL	0.24 + 0.047*SL
	t_{PHL}	0.19	0.13 + 0.030*SL	0.14 + 0.026*SL	0.15 + 0.026*SL
	t_R	0.60	0.40 + 0.100*SL	0.39 + 0.102*SL	0.37 + 0.104*SL
	t_F	0.36	0.26 + 0.048*SL	0.26 + 0.050*SL	0.24 + 0.051*SL
B to Y	t_{PLH}	0.39	0.30 + 0.048*SL	0.30 + 0.047*SL	0.30 + 0.047*SL
	t_{PHL}	0.25	0.19 + 0.029*SL	0.19 + 0.026*SL	0.20 + 0.026*SL
	t_R	0.60	0.40 + 0.099*SL	0.39 + 0.102*SL	0.37 + 0.104*SL
	t_F	0.45	0.36 + 0.047*SL	0.35 + 0.049*SL	0.33 + 0.051*SL
C to Y	t_{PLH}	0.32	0.27 + 0.025*SL	0.27 + 0.025*SL	0.27 + 0.025*SL
	t_{PHL}	0.29	0.23 + 0.029*SL	0.24 + 0.027*SL	0.24 + 0.026*SL
	t_R	0.43	0.32 + 0.050*SL	0.32 + 0.052*SL	0.30 + 0.053*SL
	t_F	0.43	0.33 + 0.048*SL	0.33 + 0.051*SL	0.31 + 0.052*SL
D to Y	t_{PLH}	0.36	0.31 + 0.025*SL	0.31 + 0.025*SL	0.31 + 0.025*SL
	t_{PHL}	0.29	0.24 + 0.028*SL	0.24 + 0.027*SL	0.25 + 0.026*SL
	t_R	0.49	0.39 + 0.050*SL	0.38 + 0.052*SL	0.37 + 0.053*SL
	t_F	0.42	0.32 + 0.050*SL	0.32 + 0.051*SL	0.31 + 0.052*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

OA22/OA22D2

Two 2-ORs into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
1	x	x	1	0
x	1	x	1	0
1	x	1	x	0
x	1	1	x	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
OA22				*OA22D2*				*OA22*	*OA22D2*
A	B	C	D	A	B	C	D		
0.5	0.7	0.5	0.7	1.0	1.4	1.1	1.5	2.0	4.0
KGM80									
OA22				*OA22D2*				*OA22*	*OA22D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	2.0	1.9	2.0	1.9	2.0	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OA22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.21 + 0.069*SL	0.20 + 0.071*SL	0.20 + 0.071*SL
	t_{PHL}	0.19	0.11 + 0.041*SL	0.12 + 0.034*SL	0.12 + 0.034*SL
	t_R	0.68	0.37 + 0.152*SL	0.36 + 0.159*SL	0.33 + 0.163*SL
	t_F	0.33	0.21 + 0.061*SL	0.20 + 0.063*SL	0.18 + 0.066*SL
B to Y	t_{PLH}	0.35	0.21 + 0.070*SL	0.20 + 0.071*SL	0.21 + 0.071*SL
	t_{PHL}	0.21	0.13 + 0.037*SL	0.14 + 0.034*SL	0.14 + 0.034*SL
	t_R	0.68	0.37 + 0.152*SL	0.36 + 0.159*SL	0.33 + 0.162*SL
	t_F	0.38	0.26 + 0.057*SL	0.25 + 0.061*SL	0.22 + 0.065*SL
C to Y	t_{PLH}	0.43	0.29 + 0.068*SL	0.29 + 0.070*SL	0.29 + 0.070*SL
	t_{PHL}	0.19	0.12 + 0.038*SL	0.13 + 0.035*SL	0.13 + 0.034*SL
	t_R	0.72	0.40 + 0.156*SL	0.39 + 0.160*SL	0.38 + 0.163*SL
	t_F	0.31	0.19 + 0.059*SL	0.18 + 0.064*SL	0.16 + 0.067*SL
D to Y	t_{PLH}	0.43	0.29 + 0.069*SL	0.29 + 0.070*SL	0.29 + 0.071*SL
	t_{PHL}	0.21	0.14 + 0.037*SL	0.15 + 0.035*SL	0.15 + 0.034*SL
	t_R	0.72	0.41 + 0.156*SL	0.40 + 0.160*SL	0.38 + 0.163*SL
	t_F	0.35	0.24 + 0.054*SL	0.22 + 0.064*SL	0.20 + 0.067*SL

KG80 OA22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.19 + 0.035*SL	0.19 + 0.035*SL	0.19 + 0.036*SL
	t_{PHL}	0.14	0.09 + 0.024*SL	0.10 + 0.019*SL	0.13 + 0.016*SL
	t_R	0.52	0.37 + 0.072*SL	0.36 + 0.077*SL	0.34 + 0.079*SL
	t_F	0.27	0.21 + 0.030*SL	0.21 + 0.030*SL	0.19 + 0.032*SL
B to Y	t_{PLH}	0.27	0.19 + 0.038*SL	0.20 + 0.035*SL	0.20 + 0.036*SL
	t_{PHL}	0.17	0.13 + 0.022*SL	0.14 + 0.018*SL	0.14 + 0.017*SL
	t_R	0.52	0.37 + 0.074*SL	0.37 + 0.076*SL	0.34 + 0.080*SL
	t_F	0.31	0.26 + 0.028*SL	0.25 + 0.030*SL	0.25 + 0.031*SL
C to Y	t_{PLH}	0.35	0.28 + 0.035*SL	0.28 + 0.034*SL	0.28 + 0.035*SL
	t_{PHL}	0.15	0.11 + 0.022*SL	0.11 + 0.019*SL	0.12 + 0.017*SL
	t_R	0.53	0.37 + 0.077*SL	0.37 + 0.078*SL	0.36 + 0.080*SL
	t_F	0.25	0.19 + 0.033*SL	0.19 + 0.029*SL	0.17 + 0.032*SL
D to Y	t_{PLH}	0.36	0.29 + 0.035*SL	0.29 + 0.035*SL	0.28 + 0.035*SL
	t_{PHL}	0.18	0.14 + 0.020*SL	0.14 + 0.018*SL	0.15 + 0.017*SL
	t_R	0.53	0.38 + 0.076*SL	0.37 + 0.079*SL	0.36 + 0.080*SL
	t_F	0.29	0.23 + 0.028*SL	0.23 + 0.031*SL	0.21 + 0.032*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

OA22/OA22D2

Two 2-ORs into 2-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OA22

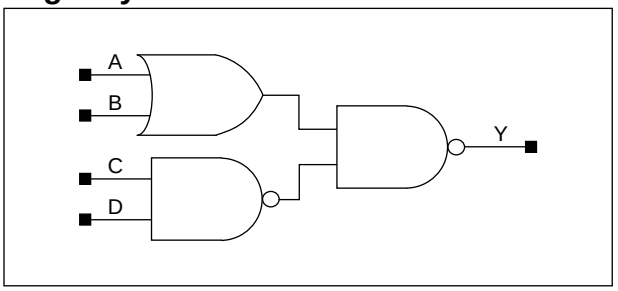
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.45	0.26 + 0.095*SL	0.26 + 0.095*SL	0.27 + 0.094*SL
	t_{PHL}	0.24	0.15 + 0.043*SL	0.17 + 0.037*SL	0.17 + 0.037*SL
	t_R	0.95	0.55 + 0.199*SL	0.53 + 0.206*SL	0.51 + 0.208*SL
	t_F	0.37	0.24 + 0.066*SL	0.23 + 0.071*SL	0.20 + 0.073*SL
B to Y	t_{PLH}	0.48	0.28 + 0.096*SL	0.29 + 0.095*SL	0.29 + 0.095*SL
	t_{PHL}	0.26	0.18 + 0.042*SL	0.19 + 0.038*SL	0.20 + 0.037*SL
	t_R	0.95	0.55 + 0.200*SL	0.53 + 0.206*SL	0.51 + 0.208*SL
	t_F	0.42	0.28 + 0.067*SL	0.27 + 0.070*SL	0.24 + 0.073*SL
C to Y	t_{PLH}	0.61	0.42 + 0.094*SL	0.42 + 0.094*SL	0.42 + 0.094*SL
	t_{PHL}	0.26	0.17 + 0.041*SL	0.18 + 0.038*SL	0.19 + 0.037*SL
	t_R	0.99	0.59 + 0.203*SL	0.58 + 0.207*SL	0.57 + 0.208*SL
	t_F	0.35	0.21 + 0.068*SL	0.20 + 0.072*SL	0.19 + 0.074*SL
D to Y	t_{PLH}	0.63	0.45 + 0.094*SL	0.45 + 0.094*SL	0.45 + 0.094*SL
	t_{PHL}	0.28	0.20 + 0.041*SL	0.21 + 0.038*SL	0.21 + 0.037*SL
	t_R	1.00	0.59 + 0.204*SL	0.58 + 0.207*SL	0.57 + 0.208*SL
	t_F	0.39	0.26 + 0.068*SL	0.25 + 0.072*SL	0.23 + 0.074*SL

KGM80 OA22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.23 + 0.048*SL	0.23 + 0.048*SL	0.23 + 0.048*SL
	t_{PHL}	0.18	0.13 + 0.025*SL	0.14 + 0.020*SL	0.16 + 0.019*SL
	t_R	0.73	0.54 + 0.097*SL	0.53 + 0.101*SL	0.50 + 0.103*SL
	t_F	0.29	0.22 + 0.035*SL	0.23 + 0.034*SL	0.21 + 0.036*SL
B to Y	t_{PLH}	0.36	0.27 + 0.049*SL	0.27 + 0.048*SL	0.27 + 0.048*SL
	t_{PHL}	0.22	0.17 + 0.023*SL	0.18 + 0.020*SL	0.19 + 0.019*SL
	t_R	0.73	0.54 + 0.097*SL	0.53 + 0.101*SL	0.51 + 0.103*SL
	t_F	0.35	0.28 + 0.034*SL	0.28 + 0.034*SL	0.27 + 0.035*SL
C to Y	t_{PLH}	0.49	0.39 + 0.047*SL	0.39 + 0.047*SL	0.39 + 0.047*SL
	t_{PHL}	0.20	0.16 + 0.023*SL	0.16 + 0.020*SL	0.18 + 0.019*SL
	t_R	0.73	0.53 + 0.101*SL	0.52 + 0.103*SL	0.51 + 0.104*SL
	t_F	0.27	0.21 + 0.033*SL	0.20 + 0.035*SL	0.19 + 0.036*SL
D to Y	t_{PLH}	0.53	0.43 + 0.047*SL	0.43 + 0.047*SL	0.44 + 0.047*SL
	t_{PHL}	0.24	0.19 + 0.022*SL	0.20 + 0.020*SL	0.21 + 0.019*SL
	t_R	0.73	0.53 + 0.101*SL	0.53 + 0.102*SL	0.51 + 0.104*SL
	t_F	0.33	0.26 + 0.032*SL	0.25 + 0.035*SL	0.24 + 0.036*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
1	x	0	x	0
1	x	x	0	0
x	1	0	x	0
x	1	x	0	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
OA22A				*OA22D2A*				*OA22*	*OA22D2*
A	B	C	D	A	B	C	D		
0.6	0.5	0.9	0.9	1.1	1.1	0.9	0.8	3.0	4.0
KGM80									
OA22A				*OA22D2A*				*OA22*	*OA22D2*
A	B	C	D	A	B	C	D		
1.0	1.0	1.0	1.0	2.0	1.9	1.0	1.0	3.0	4.0

OA22A/OA22D2A

2-OR and 2-NAND into 2-NAND with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OA22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.19 + 0.068*SL	0.19 + 0.070*SL	0.18 + 0.071*SL
	t_{PHL}	0.16	0.08 + 0.043*SL	0.10 + 0.034*SL	0.10 + 0.034*SL
	t_R	0.57	0.27 + 0.152*SL	0.25 + 0.159*SL	0.23 + 0.163*SL
	t_F	0.31	0.19 + 0.058*SL	0.18 + 0.062*SL	0.16 + 0.065*SL
B to Y	t_{PLH}	0.33	0.19 + 0.069*SL	0.19 + 0.070*SL	0.18 + 0.071*SL
	t_{PHL}	0.18	0.10 + 0.040*SL	0.12 + 0.034*SL	0.12 + 0.034*SL
	t_R	0.58	0.27 + 0.153*SL	0.25 + 0.159*SL	0.23 + 0.162*SL
	t_F	0.35	0.23 + 0.059*SL	0.23 + 0.061*SL	0.20 + 0.065*SL
C to Y	t_{PLH}	0.33	0.25 + 0.042*SL	0.25 + 0.042*SL	0.25 + 0.042*SL
	t_{PHL}	0.35	0.28 + 0.036*SL	0.28 + 0.035*SL	0.28 + 0.034*SL
	t_R	0.40	0.22 + 0.087*SL	0.22 + 0.089*SL	0.21 + 0.090*SL
	t_F	0.28	0.15 + 0.066*SL	0.14 + 0.068*SL	0.14 + 0.069*SL
D to Y	t_{PLH}	0.32	0.24 + 0.042*SL	0.24 + 0.042*SL	0.24 + 0.042*SL
	t_{PHL}	0.38	0.31 + 0.036*SL	0.31 + 0.034*SL	0.31 + 0.034*SL
	t_R	0.40	0.23 + 0.086*SL	0.22 + 0.089*SL	0.21 + 0.090*SL
	t_F	0.28	0.15 + 0.065*SL	0.15 + 0.067*SL	0.14 + 0.069*SL

KG80 OA22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.17 + 0.035*SL
	t_{PHL}	0.11	0.05 + 0.027*SL	0.07 + 0.021*SL	0.10 + 0.016*SL
	t_R	0.38	0.23 + 0.073*SL	0.22 + 0.077*SL	0.20 + 0.080*SL
	t_F	0.23	0.16 + 0.034*SL	0.17 + 0.029*SL	0.16 + 0.031*SL
B to Y	t_{PLH}	0.25	0.17 + 0.037*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.13	0.09 + 0.024*SL	0.10 + 0.019*SL	0.11 + 0.017*SL
	t_R	0.38	0.24 + 0.071*SL	0.22 + 0.078*SL	0.21 + 0.080*SL
	t_F	0.28	0.22 + 0.030*SL	0.23 + 0.029*SL	0.22 + 0.030*SL
C to Y	t_{PLH}	0.33	0.28 + 0.021*SL	0.28 + 0.021*SL	0.28 + 0.021*SL
	t_{PHL}	0.34	0.30 + 0.019*SL	0.31 + 0.018*SL	0.31 + 0.017*SL
	t_R	0.29	0.22 + 0.036*SL	0.20 + 0.043*SL	0.19 + 0.044*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.033*SL	0.14 + 0.033*SL
D to Y	t_{PLH}	0.31	0.27 + 0.021*SL	0.27 + 0.021*SL	0.27 + 0.021*SL
	t_{PHL}	0.37	0.33 + 0.020*SL	0.34 + 0.018*SL	0.34 + 0.017*SL
	t_R	0.29	0.20 + 0.043*SL	0.20 + 0.043*SL	0.19 + 0.044*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.032*SL	0.15 + 0.033*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OA22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.25 + 0.093*SL	0.25 + 0.094*SL	0.25 + 0.094*SL
	t_{PHL}	0.20	0.11 + 0.045*SL	0.14 + 0.037*SL	0.14 + 0.037*SL
	t_R	0.79	0.39 + 0.201*SL	0.37 + 0.206*SL	0.35 + 0.208*SL
	t_F	0.34	0.21 + 0.066*SL	0.20 + 0.070*SL	0.16 + 0.073*SL
B to Y	t_{PLH}	0.46	0.27 + 0.094*SL	0.27 + 0.094*SL	0.27 + 0.094*SL
	t_{PHL}	0.23	0.15 + 0.043*SL	0.16 + 0.037*SL	0.17 + 0.037*SL
	t_R	0.79	0.39 + 0.202*SL	0.38 + 0.206*SL	0.35 + 0.208*SL
	t_F	0.39	0.26 + 0.066*SL	0.24 + 0.070*SL	0.21 + 0.073*SL
C to Y	t_{PLH}	0.45	0.35 + 0.051*SL	0.35 + 0.050*SL	0.36 + 0.050*SL
	t_{PHL}	0.45	0.37 + 0.040*SL	0.37 + 0.038*SL	0.38 + 0.037*SL
	t_R	0.52	0.31 + 0.106*SL	0.30 + 0.108*SL	0.29 + 0.109*SL
	t_F	0.34	0.19 + 0.072*SL	0.19 + 0.074*SL	0.18 + 0.075*SL
D to Y	t_{PLH}	0.45	0.35 + 0.051*SL	0.35 + 0.050*SL	0.36 + 0.050*SL
	t_{PHL}	0.49	0.41 + 0.040*SL	0.42 + 0.038*SL	0.42 + 0.037*SL
	t_R	0.52	0.31 + 0.106*SL	0.30 + 0.108*SL	0.29 + 0.109*SL
	t_F	0.34	0.20 + 0.071*SL	0.19 + 0.073*SL	0.18 + 0.074*SL

KGM80 OA22D2A

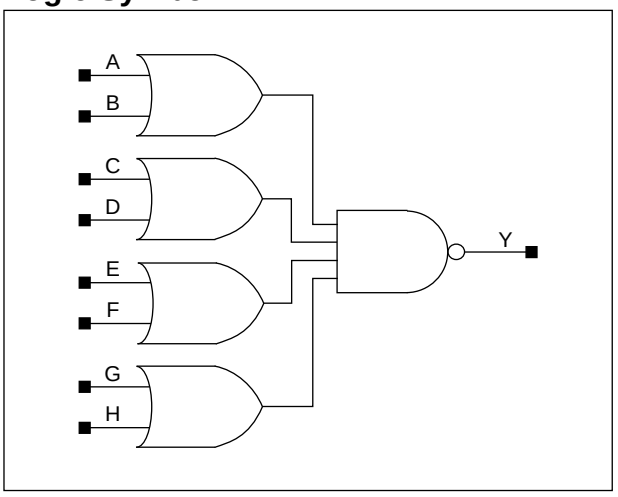
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.31	0.21 + 0.048*SL	0.21 + 0.047*SL	0.21 + 0.047*SL
	t_{PHL}	0.14	0.08 + 0.026*SL	0.10 + 0.021*SL	0.12 + 0.018*SL
	t_R	0.51	0.32 + 0.099*SL	0.31 + 0.102*SL	0.29 + 0.103*SL
	t_F	0.24	0.17 + 0.038*SL	0.18 + 0.034*SL	0.16 + 0.035*SL
B to Y	t_{PLH}	0.35	0.25 + 0.049*SL	0.25 + 0.047*SL	0.25 + 0.047*SL
	t_{PHL}	0.17	0.12 + 0.025*SL	0.14 + 0.020*SL	0.15 + 0.019*SL
	t_R	0.52	0.32 + 0.099*SL	0.31 + 0.101*SL	0.29 + 0.103*SL
	t_F	0.31	0.24 + 0.033*SL	0.24 + 0.034*SL	0.22 + 0.035*SL
C to Y	t_{PLH}	0.44	0.39 + 0.026*SL	0.39 + 0.025*SL	0.40 + 0.025*SL
	t_{PHL}	0.45	0.41 + 0.022*SL	0.41 + 0.020*SL	0.42 + 0.019*SL
	t_R	0.38	0.27 + 0.051*SL	0.27 + 0.053*SL	0.26 + 0.054*SL
	t_F	0.26	0.20 + 0.034*SL	0.19 + 0.036*SL	0.18 + 0.037*SL
D to Y	t_{PLH}	0.44	0.39 + 0.026*SL	0.39 + 0.025*SL	0.39 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.023*SL	0.46 + 0.020*SL	0.47 + 0.019*SL
	t_R	0.37	0.27 + 0.052*SL	0.27 + 0.053*SL	0.26 + 0.054*SL
	t_F	0.27	0.20 + 0.034*SL	0.20 + 0.036*SL	0.19 + 0.036*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

OA2222/OA2222D2

Four 2-ORs into 4-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

Cell Data

Input Load (SL)																Gate Count	
KG80																	
OA2222								*OA2222D2*								*OA2222*	*OA2222 D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.5	0.6	0.8	0.8	0.6	0.6	0.8	0.8	0.5	0.6	0.8	0.8	0.6	0.6	0.8	0.8	6.0	6.0
KGM80																	
OA2222								*OA2222D2*								*OA2222*	*OA2222 D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
1.0	1.0	1.0	1.0	0.7	0.7	0.9	0.9	1.0	1.0	1.0	1.0	0.7	0.7	0.9	0.9	6.0	6.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OA2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.41 + 0.042*SL	0.41 + 0.041*SL	0.40 + 0.042*SL
	t_{PHL}	0.42	0.36 + 0.033*SL	0.37 + 0.027*SL	0.39 + 0.024*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.18	0.10 + 0.043*SL	0.10 + 0.041*SL	0.10 + 0.041*SL
B to Y	t_{PLH}	0.49	0.40 + 0.041*SL	0.40 + 0.041*SL	0.40 + 0.042*SL
	t_{PHL}	0.45	0.39 + 0.033*SL	0.40 + 0.026*SL	0.42 + 0.024*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.18	0.10 + 0.043*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
C to Y	t_{PLH}	0.56	0.48 + 0.042*SL	0.48 + 0.041*SL	0.47 + 0.042*SL
	t_{PHL}	0.43	0.37 + 0.033*SL	0.38 + 0.026*SL	0.40 + 0.024*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.041*SL	0.10 + 0.041*SL
D to Y	t_{PLH}	0.56	0.47 + 0.042*SL	0.47 + 0.041*SL	0.47 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.033*SL	0.35 + 0.026*SL	0.37 + 0.024*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.041*SL	0.10 + 0.041*SL
E to Y	t_{PLH}	0.51	0.42 + 0.041*SL	0.42 + 0.041*SL	0.42 + 0.042*SL
	t_{PHL}	0.43	0.37 + 0.033*SL	0.38 + 0.026*SL	0.40 + 0.024*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.10 + 0.041*SL
F to Y	t_{PLH}	0.51	0.42 + 0.041*SL	0.42 + 0.041*SL	0.42 + 0.042*SL
	t_{PHL}	0.46	0.40 + 0.033*SL	0.41 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.18	0.10 + 0.043*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
G to Y	t_{PLH}	0.58	0.50 + 0.041*SL	0.50 + 0.041*SL	0.49 + 0.042*SL
	t_{PHL}	0.44	0.38 + 0.032*SL	0.39 + 0.026*SL	0.41 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.19	0.10 + 0.044*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
H to Y	t_{PLH}	0.58	0.50 + 0.041*SL	0.50 + 0.041*SL	0.49 + 0.042*SL
	t_{PHL}	0.42	0.35 + 0.033*SL	0.37 + 0.027*SL	0.39 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.10 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 OA2222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.48	0.43 + 0.023*SL	0.44 + 0.020*SL	0.44 + 0.021*SL
	t_{PHL}	0.44	0.40 + 0.022*SL	0.41 + 0.017*SL	0.43 + 0.014*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
B to Y	t_{PLH}	0.48	0.43 + 0.022*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.47	0.42 + 0.022*SL	0.44 + 0.017*SL	0.46 + 0.014*SL
	t_R	0.16	0.09 + 0.037*SL	0.07 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
C to Y	t_{PLH}	0.55	0.50 + 0.022*SL	0.51 + 0.021*SL	0.51 + 0.021*SL
	t_{PHL}	0.45	0.41 + 0.022*SL	0.42 + 0.017*SL	0.44 + 0.014*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
D to Y	t_{PLH}	0.55	0.50 + 0.023*SL	0.51 + 0.020*SL	0.51 + 0.021*SL
	t_{PHL}	0.42	0.38 + 0.022*SL	0.39 + 0.017*SL	0.41 + 0.014*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
E to Y	t_{PLH}	0.49	0.45 + 0.022*SL	0.45 + 0.021*SL	0.45 + 0.020*SL
	t_{PHL}	0.45	0.41 + 0.023*SL	0.42 + 0.017*SL	0.44 + 0.014*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
F to Y	t_{PLH}	0.49	0.45 + 0.022*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.48	0.43 + 0.023*SL	0.45 + 0.017*SL	0.47 + 0.014*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.042*SL	0.07 + 0.044*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
G to Y	t_{PLH}	0.57	0.52 + 0.022*SL	0.53 + 0.021*SL	0.53 + 0.020*SL
	t_{PHL}	0.46	0.42 + 0.022*SL	0.43 + 0.017*SL	0.45 + 0.014*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.16	0.12 + 0.024*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
H to Y	t_{PLH}	0.57	0.52 + 0.023*SL	0.53 + 0.020*SL	0.53 + 0.020*SL
	t_{PHL}	0.44	0.39 + 0.022*SL	0.41 + 0.017*SL	0.42 + 0.014*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.020*SL	0.13 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OA2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.67	0.57 + 0.050*SL	0.57 + 0.050*SL	0.58 + 0.050*SL
	t_{PHL}	0.59	0.52 + 0.037*SL	0.54 + 0.028*SL	0.58 + 0.024*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.23	0.13 + 0.047*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
B to Y	t_{PLH}	0.70	0.60 + 0.050*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.63	0.55 + 0.037*SL	0.58 + 0.028*SL	0.62 + 0.024*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.22	0.13 + 0.046*SL	0.14 + 0.042*SL	0.15 + 0.042*SL
C to Y	t_{PLH}	0.84	0.74 + 0.050*SL	0.74 + 0.050*SL	0.74 + 0.050*SL
	t_{PHL}	0.62	0.54 + 0.037*SL	0.57 + 0.028*SL	0.61 + 0.024*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.23	0.13 + 0.047*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
D to Y	t_{PLH}	0.81	0.71 + 0.050*SL	0.71 + 0.050*SL	0.71 + 0.050*SL
	t_{PHL}	0.58	0.51 + 0.037*SL	0.54 + 0.028*SL	0.58 + 0.024*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.22	0.13 + 0.047*SL	0.14 + 0.042*SL	0.15 + 0.042*SL
E to Y	t_{PLH}	0.70	0.60 + 0.050*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.63	0.55 + 0.037*SL	0.58 + 0.028*SL	0.62 + 0.024*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.23	0.13 + 0.047*SL	0.14 + 0.042*SL	0.15 + 0.042*SL
F to Y	t_{PLH}	0.72	0.62 + 0.051*SL	0.62 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.66	0.58 + 0.037*SL	0.61 + 0.028*SL	0.65 + 0.024*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.23	0.13 + 0.047*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
G to Y	t_{PLH}	0.86	0.76 + 0.050*SL	0.76 + 0.050*SL	0.76 + 0.050*SL
	t_{PHL}	0.65	0.58 + 0.037*SL	0.61 + 0.028*SL	0.65 + 0.024*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.23	0.13 + 0.047*SL	0.15 + 0.042*SL	0.14 + 0.042*SL
H to Y	t_{PLH}	0.83	0.73 + 0.050*SL	0.74 + 0.050*SL	0.74 + 0.050*SL
	t_{PHL}	0.62	0.55 + 0.037*SL	0.57 + 0.028*SL	0.61 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.23	0.13 + 0.046*SL	0.14 + 0.042*SL	0.15 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

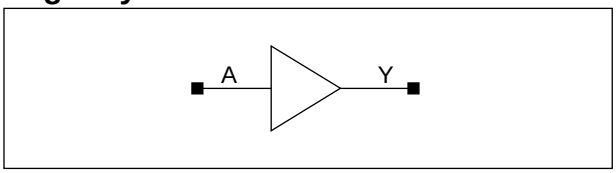
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 OA2222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.61 + 0.027*SL	0.61 + 0.025*SL	0.61 + 0.025*SL
	t_{PHL}	0.63	0.58 + 0.026*SL	0.60 + 0.019*SL	0.64 + 0.015*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.21	0.15 + 0.027*SL	0.17 + 0.023*SL	0.18 + 0.021*SL
B to Y	t_{PLH}	0.69	0.63 + 0.027*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.67	0.62 + 0.027*SL	0.64 + 0.019*SL	0.68 + 0.015*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.21	0.15 + 0.027*SL	0.16 + 0.023*SL	0.18 + 0.021*SL
C to Y	t_{PLH}	0.82	0.77 + 0.028*SL	0.78 + 0.025*SL	0.78 + 0.025*SL
	t_{PHL}	0.66	0.61 + 0.026*SL	0.63 + 0.019*SL	0.67 + 0.015*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.21	0.15 + 0.028*SL	0.17 + 0.022*SL	0.18 + 0.021*SL
D to Y	t_{PLH}	0.80	0.74 + 0.028*SL	0.75 + 0.025*SL	0.75 + 0.025*SL
	t_{PHL}	0.63	0.57 + 0.027*SL	0.59 + 0.019*SL	0.64 + 0.015*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.21	0.15 + 0.028*SL	0.16 + 0.022*SL	0.18 + 0.021*SL
E to Y	t_{PLH}	0.68	0.63 + 0.027*SL	0.63 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.67	0.61 + 0.027*SL	0.64 + 0.019*SL	0.68 + 0.015*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.21	0.15 + 0.027*SL	0.16 + 0.023*SL	0.19 + 0.021*SL
F to Y	t_{PLH}	0.71	0.65 + 0.028*SL	0.66 + 0.025*SL	0.66 + 0.025*SL
	t_{PHL}	0.70	0.65 + 0.027*SL	0.67 + 0.019*SL	0.71 + 0.015*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.21	0.15 + 0.028*SL	0.17 + 0.023*SL	0.18 + 0.021*SL
G to Y	t_{PLH}	0.84	0.79 + 0.028*SL	0.80 + 0.025*SL	0.80 + 0.025*SL
	t_{PHL}	0.70	0.64 + 0.026*SL	0.66 + 0.019*SL	0.71 + 0.015*SL
	t_R	0.22	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.21	0.15 + 0.028*SL	0.16 + 0.023*SL	0.19 + 0.021*SL
H to Y	t_{PLH}	0.82	0.76 + 0.028*SL	0.77 + 0.025*SL	0.77 + 0.025*SL
	t_{PHL}	0.66	0.61 + 0.026*SL	0.63 + 0.019*SL	0.68 + 0.015*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.21	0.15 + 0.027*SL	0.16 + 0.023*SL	0.19 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)											
KG80											
DL1D2	*DL1D4*	*DL2D2*	*DL2D4*	*DL3D2*	*DL3D4*	*DL4D2*	*DL4D4*	*DL5D2*	*DL5D4*	*DL10D2*	*DL10D4*
A	A	A	A	A	A	A	A	A	A	A	A
0.8	0.8	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9
KGM80											
DL1D2	*DL1D4*	*DL2D2*	*DL2D4*	*DL3D2*	*DL3D4*	*DL4D2*	*DL4D4*	*DL5D2*	*DL5D4*	*DL10D2*	*DL10D4*
A	A	A	A	A	A	A	A	A	A	A	A
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Gate Count											
KGD80/KGM80											
DL1D2	*DL1D4*	*DL2D2*	*DL2D4*	*DL3D2*	*DL3D4*	*DL4D2*	*DL4D4*	*DL5D2*	*DL5D4*	*DL10D2*	*DL10D4*
7.0	7.0	11.0	12.0	15.0	16.0	20.0	20.0	24.0	24.0	43.0	44.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 DL1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.76	0.72 + 0.020*SL	0.73 + 0.016*SL	0.74 + 0.015*SL
	t_{PHL}	0.80	0.74 + 0.026*SL	0.75 + 0.024*SL	0.76 + 0.023*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.026*SL	0.13 + 0.027*SL
	t_F	0.18	0.11 + 0.038*SL	0.10 + 0.041*SL	0.10 + 0.041*SL

KG80 DL1D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.81	0.78 + 0.016*SL	0.78 + 0.012*SL	0.79 + 0.011*SL
	t_{PHL}	0.79	0.76 + 0.016*SL	0.77 + 0.014*SL	0.78 + 0.012*SL
	t_R	0.19	0.15 + 0.020*SL	0.15 + 0.019*SL	0.14 + 0.020*SL
	t_F	0.16	0.12 + 0.019*SL	0.12 + 0.019*SL	0.12 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 DL2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.44	1.40 + 0.021*SL	1.41 + 0.016*SL	1.42 + 0.014*SL
	t_{PHL}	1.52	1.46 + 0.026*SL	1.47 + 0.024*SL	1.47 + 0.023*SL
	t_R	0.20	0.16 + 0.024*SL	0.16 + 0.025*SL	0.14 + 0.027*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.040*SL	0.09 + 0.042*SL

KG80 DL2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.50	1.47 + 0.016*SL	1.47 + 0.012*SL	1.48 + 0.011*SL
	t_{PHL}	1.52	1.48 + 0.016*SL	1.49 + 0.014*SL	1.50 + 0.012*SL
	t_R	0.20	0.17 + 0.017*SL	0.17 + 0.018*SL	0.16 + 0.020*SL
	t_F	0.17	0.13 + 0.019*SL	0.13 + 0.019*SL	0.13 + 0.019*SL

KG80 DL3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.63	2.59 + 0.019*SL	2.60 + 0.015*SL	2.61 + 0.014*SL
	t_{PHL}	2.59	2.53 + 0.026*SL	2.54 + 0.024*SL	2.55 + 0.023*SL
	t_R	0.17	0.13 + 0.023*SL	0.12 + 0.026*SL	0.10 + 0.028*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.042*SL

KG80 DL3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.68	2.65 + 0.013*SL	2.66 + 0.010*SL	2.67 + 0.009*SL
	t_{PHL}	2.62	2.59 + 0.016*SL	2.59 + 0.014*SL	2.60 + 0.012*SL
	t_R	0.17	0.14 + 0.013*SL	0.14 + 0.015*SL	0.13 + 0.016*SL
	t_F	0.17	0.13 + 0.019*SL	0.13 + 0.019*SL	0.13 + 0.019*SL

KG80 DL4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.14	3.09 + 0.025*SL	3.11 + 0.018*SL	3.13 + 0.015*SL
	t_{PHL}	3.28	3.22 + 0.030*SL	3.23 + 0.026*SL	3.24 + 0.024*SL
	t_R	0.27	0.22 + 0.023*SL	0.22 + 0.024*SL	0.20 + 0.027*SL
	t_F	0.25	0.17 + 0.040*SL	0.17 + 0.039*SL	0.17 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 DL4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.23	3.20 + 0.019*SL	3.21 + 0.015*SL	3.22 + 0.012*SL
	t_{PHL}	3.29	3.25 + 0.020*SL	3.26 + 0.016*SL	3.28 + 0.014*SL
	t_R	0.27	0.23 + 0.016*SL	0.23 + 0.018*SL	0.22 + 0.020*SL
	t_F	0.24	0.19 + 0.023*SL	0.20 + 0.019*SL	0.20 + 0.019*SL

KG80 DL5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.90	3.86 + 0.021*SL	3.87 + 0.017*SL	3.89 + 0.015*SL
	t_{PHL}	3.88	3.82 + 0.030*SL	3.83 + 0.026*SL	3.85 + 0.024*SL
	t_R	0.21	0.16 + 0.024*SL	0.16 + 0.026*SL	0.15 + 0.027*SL
	t_F	0.24	0.16 + 0.038*SL	0.16 + 0.040*SL	0.15 + 0.040*SL

KG80 DL5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.97	3.94 + 0.018*SL	3.95 + 0.013*SL	3.96 + 0.011*SL
	t_{PHL}	3.89	3.85 + 0.020*SL	3.86 + 0.016*SL	3.88 + 0.014*SL
	t_R	0.21	0.17 + 0.018*SL	0.17 + 0.019*SL	0.17 + 0.020*SL
	t_F	0.23	0.18 + 0.023*SL	0.19 + 0.019*SL	0.19 + 0.020*SL

KG80 DL10D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	7.50	7.45 + 0.024*SL	7.47 + 0.017*SL	7.49 + 0.015*SL
	t_{PHL}	7.60	7.55 + 0.027*SL	7.56 + 0.024*SL	7.56 + 0.023*SL
	t_R	0.24	0.20 + 0.023*SL	0.19 + 0.024*SL	0.17 + 0.027*SL
	t_F	0.20	0.13 + 0.037*SL	0.13 + 0.039*SL	0.11 + 0.041*SL

KG80 DL10D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	7.57	7.54 + 0.017*SL	7.55 + 0.013*SL	7.56 + 0.011*SL
	t_{PHL}	7.61	7.57 + 0.017*SL	7.58 + 0.014*SL	7.59 + 0.012*SL
	t_R	0.24	0.21 + 0.016*SL	0.20 + 0.018*SL	0.19 + 0.019*SL
	t_F	0.19	0.15 + 0.020*SL	0.15 + 0.018*SL	0.15 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 DL1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.18	1.13 + 0.024*SL	1.14 + 0.019*SL	1.16 + 0.017*SL
	t_{PHL}	1.09	1.03 + 0.030*SL	1.04 + 0.025*SL	1.06 + 0.023*SL
	t_R	0.24	0.18 + 0.033*SL	0.18 + 0.032*SL	0.16 + 0.034*SL
	t_F	0.22	0.14 + 0.043*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

KGM80 DL1D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.25	1.21 + 0.019*SL	1.22 + 0.015*SL	1.24 + 0.013*SL
	t_{PHL}	1.10	1.06 + 0.019*SL	1.07 + 0.015*SL	1.09 + 0.013*SL
	t_R	0.23	0.18 + 0.026*SL	0.18 + 0.025*SL	0.18 + 0.025*SL
	t_F	0.19	0.15 + 0.022*SL	0.15 + 0.021*SL	0.15 + 0.020*SL

KGM80 DL2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.25	2.20 + 0.026*SL	2.22 + 0.019*SL	2.24 + 0.017*SL
	t_{PHL}	2.26	2.20 + 0.031*SL	2.21 + 0.025*SL	2.23 + 0.023*SL
	t_R	0.27	0.21 + 0.030*SL	0.21 + 0.031*SL	0.18 + 0.034*SL
	t_F	0.23	0.14 + 0.043*SL	0.15 + 0.041*SL	0.13 + 0.042*SL

KGM80 DL2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.33	2.29 + 0.019*SL	2.31 + 0.015*SL	2.33 + 0.013*SL
	t_{PHL}	2.27	2.23 + 0.019*SL	2.24 + 0.015*SL	2.27 + 0.013*SL
	t_R	0.27	0.22 + 0.023*SL	0.22 + 0.023*SL	0.21 + 0.025*SL
	t_F	0.21	0.16 + 0.022*SL	0.17 + 0.020*SL	0.17 + 0.020*SL

KGM80 DL3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	4.15	4.10 + 0.023*SL	4.11 + 0.018*SL	4.13 + 0.017*SL
	t_{PHL}	4.02	3.96 + 0.030*SL	3.97 + 0.025*SL	3.99 + 0.023*SL
	t_R	0.22	0.17 + 0.030*SL	0.16 + 0.032*SL	0.13 + 0.034*SL
	t_F	0.22	0.13 + 0.042*SL	0.13 + 0.041*SL	0.12 + 0.043*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 DL3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	4.22	4.18 + 0.016*SL	4.20 + 0.012*SL	4.22 + 0.010*SL
	t_{PHL}	4.07	4.03 + 0.018*SL	4.04 + 0.015*SL	4.07 + 0.013*SL
	t_R	0.22	0.18 + 0.019*SL	0.18 + 0.018*SL	0.17 + 0.020*SL
	t_F	0.20	0.16 + 0.022*SL	0.16 + 0.021*SL	0.17 + 0.020*SL

KGM80 DL4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	5.02	4.96 + 0.031*SL	4.98 + 0.022*SL	5.02 + 0.018*SL
	t_{PHL}	5.10	5.03 + 0.035*SL	5.04 + 0.028*SL	5.09 + 0.025*SL
	t_R	0.35	0.28 + 0.032*SL	0.28 + 0.031*SL	0.27 + 0.033*SL
	t_F	0.30	0.21 + 0.045*SL	0.23 + 0.041*SL	0.23 + 0.041*SL

KGM80 DL4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	5.16	5.11 + 0.025*SL	5.13 + 0.018*SL	5.16 + 0.015*SL
	t_{PHL}	5.14	5.09 + 0.024*SL	5.11 + 0.018*SL	5.14 + 0.015*SL
	t_R	0.34	0.30 + 0.023*SL	0.29 + 0.024*SL	0.29 + 0.024*SL
	t_F	0.29	0.24 + 0.025*SL	0.25 + 0.022*SL	0.27 + 0.020*SL

KGM80 DL5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	6.23	6.18 + 0.027*SL	6.19 + 0.020*SL	6.23 + 0.017*SL
	t_{PHL}	6.06	5.99 + 0.035*SL	6.01 + 0.028*SL	6.05 + 0.025*SL
	t_R	0.28	0.22 + 0.032*SL	0.22 + 0.032*SL	0.20 + 0.033*SL
	t_F	0.29	0.20 + 0.045*SL	0.21 + 0.042*SL	0.21 + 0.041*SL

KGM80 DL5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	6.33	6.29 + 0.021*SL	6.30 + 0.016*SL	6.33 + 0.014*SL
	t_{PHL}	6.10	6.05 + 0.024*SL	6.06 + 0.018*SL	6.10 + 0.015*SL
	t_R	0.27	0.22 + 0.024*SL	0.22 + 0.024*SL	0.22 + 0.024*SL
	t_F	0.27	0.22 + 0.025*SL	0.23 + 0.022*SL	0.25 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 DL10D2

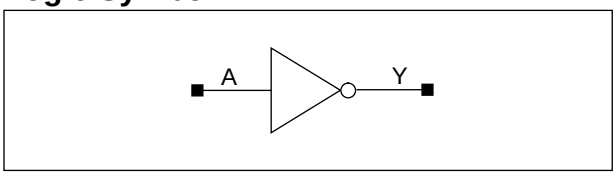
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	12.10	12.04 + 0.030*SL	12.07 + 0.021*SL	12.10 + 0.017*SL
	t_{PHL}	12.04	11.98 + 0.032*SL	12.00 + 0.025*SL	12.02 + 0.023*SL
	t_R	0.32	0.26 + 0.033*SL	0.26 + 0.031*SL	0.24 + 0.033*SL
	t_F	0.24	0.16 + 0.043*SL	0.16 + 0.040*SL	0.15 + 0.042*SL

KGM80 DL10D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	12.21	12.16 + 0.022*SL	12.18 + 0.016*SL	12.21 + 0.014*SL
	t_{PHL}	12.06	12.02 + 0.019*SL	12.03 + 0.016*SL	12.06 + 0.013*SL
	t_R	0.32	0.27 + 0.024*SL	0.28 + 0.023*SL	0.27 + 0.024*SL
	t_F	0.22	0.18 + 0.022*SL	0.18 + 0.020*SL	0.19 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)						Gate Count					
KG80											
IV	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*	*IV*	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*
A	A	A	A	A	A						
1.0	1.7	2.5	3.4	5.1	6.9	1.0	1.0	2.0	2.0	3.0	4.0
KGM80											
IV	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*	*IV*	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*
A	A	A	A	A	A						
1.0	2.0	2.9	4.0	6.0	8.0	1.0	1.0	2.0	2.0	3.0	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IV

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.16 + 0.042*SL	0.17 + 0.040*SL	0.16 + 0.041*SL
	t_{PHL}	0.13	0.06 + 0.034*SL	0.08 + 0.025*SL	0.09 + 0.023*SL
	t_R	0.36	0.20 + 0.079*SL	0.18 + 0.085*SL	0.16 + 0.089*SL
	t_F	0.24	0.16 + 0.039*SL	0.17 + 0.036*SL	0.15 + 0.038*SL

KG80 IVD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.16	0.11 + 0.027*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
	t_{PHL}	0.06	0.01 + 0.025*SL	0.02 + 0.017*SL	0.05 + 0.013*SL
	t_R	0.21	0.13 + 0.040*SL	0.13 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.17	0.12 + 0.025*SL	0.14 + 0.018*SL	0.14 + 0.018*SL

KG80 IVD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.15	0.11 + 0.019*SL	0.12 + 0.015*SL	0.14 + 0.013*SL
	t_{PHL}	0.04	0.01 + 0.017*SL	0.02 + 0.013*SL	0.04 + 0.010*SL
	t_R	0.19	0.14 + 0.028*SL	0.14 + 0.026*SL	0.13 + 0.027*SL
	t_F	0.16	0.12 + 0.018*SL	0.14 + 0.013*SL	0.14 + 0.013*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IVD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.14	0.11 + 0.015*SL	0.11 + 0.012*SL	0.13 + 0.010*SL
	t_{PHL}	0.03	0.00 + 0.015*SL	0.01 + 0.011*SL	0.03 + 0.009*SL
	t_R	0.17	0.13 + 0.021*SL	0.13 + 0.020*SL	0.14 + 0.019*SL
	t_F	0.15	0.12 + 0.014*SL	0.13 + 0.011*SL	0.14 + 0.009*SL

KG80 IVD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.13	0.11 + 0.011*SL	0.11 + 0.009*SL	0.12 + 0.008*SL
	t_{PHL}	0.02	0.00 + 0.011*SL	0.01 + 0.008*SL	0.02 + 0.007*SL
	t_R	0.16	0.13 + 0.014*SL	0.13 + 0.013*SL	0.14 + 0.013*SL
	t_F	0.14	0.12 + 0.008*SL	0.12 + 0.008*SL	0.14 + 0.006*SL

KG80 IVD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.12	0.10 + 0.008*SL	0.11 + 0.007*SL	0.12 + 0.006*SL
	t_{PHL}	0.02	-0.00 + 0.009*SL	0.00 + 0.007*SL	0.01 + 0.005*SL
	t_R	0.15	0.13 + 0.011*SL	0.13 + 0.010*SL	0.13 + 0.010*SL
	t_F	0.13	0.12 + 0.007*SL	0.12 + 0.007*SL	0.13 + 0.005*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IV

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.20 + 0.051*SL	0.20 + 0.049*SL	0.20 + 0.049*SL
	t_{PHL}	0.15	0.09 + 0.033*SL	0.11 + 0.025*SL	0.13 + 0.023*SL
	t_R	0.46	0.25 + 0.102*SL	0.24 + 0.106*SL	0.21 + 0.108*SL
	t_F	0.25	0.17 + 0.040*SL	0.17 + 0.039*SL	0.14 + 0.042*SL

KGM80 IVD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.12 + 0.032*SL	0.14 + 0.025*SL	0.14 + 0.025*SL
	t_{PHL}	0.07	0.02 + 0.023*SL	0.04 + 0.016*SL	0.08 + 0.012*SL
	t_R	0.24	0.14 + 0.052*SL	0.14 + 0.050*SL	0.12 + 0.053*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.020*SL	0.13 + 0.019*SL

KGM80 IVD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.17	0.12 + 0.022*SL	0.14 + 0.018*SL	0.15 + 0.016*SL
	t_{PHL}	0.06	0.03 + 0.016*SL	0.04 + 0.012*SL	0.07 + 0.009*SL
	t_R	0.22	0.15 + 0.036*SL	0.16 + 0.033*SL	0.14 + 0.035*SL
	t_F	0.15	0.12 + 0.016*SL	0.12 + 0.014*SL	0.14 + 0.013*SL

KGM80 IVD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.15	0.12 + 0.017*SL	0.12 + 0.014*SL	0.15 + 0.012*SL
	t_{PHL}	0.05	0.02 + 0.014*SL	0.03 + 0.010*SL	0.06 + 0.008*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.025*SL	0.14 + 0.026*SL
	t_F	0.14	0.11 + 0.013*SL	0.12 + 0.011*SL	0.13 + 0.010*SL

KGM80 IVD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.14	0.11 + 0.012*SL	0.12 + 0.010*SL	0.14 + 0.009*SL
	t_{PHL}	0.04	0.02 + 0.009*SL	0.03 + 0.007*SL	0.04 + 0.006*SL
	t_R	0.17	0.13 + 0.020*SL	0.14 + 0.017*SL	0.14 + 0.017*SL
	t_F	0.13	0.11 + 0.009*SL	0.11 + 0.008*SL	0.12 + 0.007*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

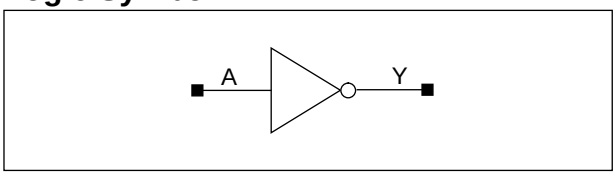
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IVD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.13	0.11 + 0.010*SL	0.12 + 0.008*SL	0.13 + 0.007*SL
	t_{PHL}	0.03	0.02 + 0.008*SL	0.02 + 0.006*SL	0.04 + 0.005*SL
	t_R	0.16	0.13 + 0.015*SL	0.14 + 0.013*SL	0.15 + 0.012*SL
	t_F	0.12	0.11 + 0.007*SL	0.11 + 0.006*SL	0.12 + 0.006*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)				Gate Count			
KG80							
IVA	*IVD2A*	*IVD3A*	*IVD4A*	*IVA*	*IVD2A*	*IVD3A*	*IVD4A*
A	A	A	A				
1.3	3.3	4.9	6.7	1.0	2.0	3.0	4.0
KGM80							
IVA	*IVD2A*	*IVD3A*	*IVD4A*	*IVA*	*IVD2A*	*IVD3A*	*IVD4A*
A	A	A	A				
1.6	3.8	5.8	7.8	1.0	2.0	3.0	4.0

IVA/IVD2A/IVD3A/IVD4A

Inverter with (2X/4X/6X/8X) P-Transistor, (1X/2X/3X/4X) N-Transistor

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IVA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.13	0.07 + 0.032*SL	0.09 + 0.023*SL	0.11 + 0.020*SL
	t_{PHL}	0.12	0.06 + 0.034*SL	0.08 + 0.025*SL	0.09 + 0.023*SL
	t_R	0.23	0.15 + 0.039*SL	0.15 + 0.038*SL	0.13 + 0.041*SL
	t_F	0.21	0.13 + 0.037*SL	0.14 + 0.037*SL	0.12 + 0.039*SL

KG80 IVD2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.10	0.07 + 0.019*SL	0.08 + 0.014*SL	0.10 + 0.011*SL
	t_{PHL}	0.09	0.05 + 0.019*SL	0.06 + 0.015*SL	0.08 + 0.012*SL
	t_R	0.19	0.15 + 0.021*SL	0.15 + 0.019*SL	0.15 + 0.019*SL
	t_F	0.17	0.13 + 0.020*SL	0.14 + 0.018*SL	0.13 + 0.019*SL

KG80 IVD3A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.09	0.07 + 0.013*SL	0.08 + 0.010*SL	0.09 + 0.008*SL
	t_{PHL}	0.08	0.06 + 0.013*SL	0.06 + 0.011*SL	0.08 + 0.009*SL
	t_R	0.18	0.15 + 0.013*SL	0.15 + 0.013*SL	0.16 + 0.012*SL
	t_F	0.16	0.13 + 0.015*SL	0.14 + 0.013*SL	0.15 + 0.011*SL

KG80 IVD4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.08	0.06 + 0.011*SL	0.07 + 0.009*SL	0.08 + 0.007*SL
	t_{PHL}	0.07	0.05 + 0.011*SL	0.06 + 0.009*SL	0.07 + 0.008*SL
	t_R	0.17	0.15 + 0.011*SL	0.15 + 0.010*SL	0.16 + 0.009*SL
	t_F	0.15	0.13 + 0.012*SL	0.13 + 0.010*SL	0.14 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IVA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.16	0.09 + 0.035*SL	0.11 + 0.026*SL	0.13 + 0.025*SL
	t_{PHL}	0.14	0.07 + 0.034*SL	0.09 + 0.025*SL	0.12 + 0.023*SL
	t_R	0.25	0.15 + 0.049*SL	0.15 + 0.050*SL	0.12 + 0.052*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.039*SL	0.10 + 0.042*SL

KGM80 IVD2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.12	0.08 + 0.020*SL	0.10 + 0.015*SL	0.13 + 0.012*SL
	t_{PHL}	0.10	0.06 + 0.019*SL	0.08 + 0.015*SL	0.11 + 0.012*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.024*SL	0.14 + 0.025*SL
	t_F	0.16	0.12 + 0.024*SL	0.13 + 0.020*SL	0.13 + 0.020*SL

KGM80 IVD3A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.12	0.09 + 0.013*SL	0.10 + 0.011*SL	0.12 + 0.009*SL
	t_{PHL}	0.10	0.07 + 0.013*SL	0.08 + 0.011*SL	0.10 + 0.009*SL
	t_R	0.19	0.16 + 0.017*SL	0.16 + 0.016*SL	0.16 + 0.016*SL
	t_F	0.15	0.12 + 0.017*SL	0.13 + 0.014*SL	0.14 + 0.013*SL

KGM80 IVD4A

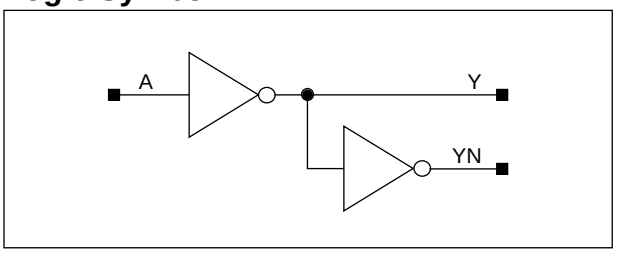
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.10	0.08 + 0.011*SL	0.09 + 0.009*SL	0.10 + 0.007*SL
	t_{PHL}	0.08	0.06 + 0.011*SL	0.07 + 0.009*SL	0.08 + 0.007*SL
	t_R	0.17	0.15 + 0.012*SL	0.15 + 0.013*SL	0.15 + 0.012*SL
	t_F	0.14	0.11 + 0.013*SL	0.12 + 0.011*SL	0.13 + 0.010*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

IVCD(11/13)/IVCD(22/26)/IVCD44

1X IV into (1X/3X) IV/2X IV into (2X/6X) IV/4X IV into 4X IV

Logic Symbol



Truth Table

A	Y	YN
1	0	1
0	1	0

Cell Data

Input Load (SL)					Gate Count				
KG80									
IVCD11	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*	*IVCD11*	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*
A	A	A	A	A					
0.9	0.8	1.7	1.7	3.4	2.0	2.0	2.0	4.0	4.0
KGM80									
IVCD11	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*	*IVCD11*	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*
A	A	A	A	A					
1.0	1.0	2.1	2.0	4.0	2.0	2.0	2.0	4.0	4.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IVCD11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.20 + 0.039*SL	0.20 + 0.040*SL	0.19 + 0.041*SL
	t_{PHL}	0.15	0.09 + 0.031*SL	0.10 + 0.024*SL	0.12 + 0.022*SL
	t_R	0.44	0.28 + 0.082*SL	0.27 + 0.086*SL	0.25 + 0.089*SL
	t_F	0.27	0.20 + 0.035*SL	0.20 + 0.036*SL	0.17 + 0.040*SL
Y to YN	t_{PLH}	0.24	0.16 + 0.041*SL	0.16 + 0.040*SL	0.16 + 0.041*SL
	t_{PHL}	0.13	0.06 + 0.034*SL	0.08 + 0.025*SL	0.10 + 0.023*SL
	t_R	0.36	0.20 + 0.080*SL	0.19 + 0.085*SL	0.16 + 0.089*SL
	t_F	0.24	0.16 + 0.039*SL	0.17 + 0.036*SL	0.15 + 0.038*SL

KG80 IVCD13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.25 + 0.038*SL	0.24 + 0.040*SL	0.24 + 0.041*SL
	t_{PHL}	0.17	0.12 + 0.028*SL	0.13 + 0.024*SL	0.14 + 0.022*SL
	t_R	0.54	0.37 + 0.084*SL	0.37 + 0.087*SL	0.35 + 0.089*SL
	t_F	0.33	0.26 + 0.034*SL	0.26 + 0.034*SL	0.22 + 0.040*SL
Y to YN	t_{PLH}	0.15	0.11 + 0.019*SL	0.12 + 0.015*SL	0.14 + 0.013*SL
	t_{PHL}	0.04	0.01 + 0.017*SL	0.02 + 0.013*SL	0.04 + 0.010*SL
	t_R	0.19	0.14 + 0.028*SL	0.14 + 0.026*SL	0.13 + 0.027*SL
	t_F	0.16	0.13 + 0.017*SL	0.13 + 0.013*SL	0.14 + 0.013*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IVCD22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.16 + 0.022*SL	0.16 + 0.020*SL	0.16 + 0.020*SL
	t_{PHL}	0.09	0.05 + 0.019*SL	0.06 + 0.016*SL	0.08 + 0.013*SL
	t_R	0.29	0.21 + 0.040*SL	0.21 + 0.041*SL	0.20 + 0.042*SL
	t_F	0.21	0.17 + 0.018*SL	0.17 + 0.017*SL	0.17 + 0.018*SL
Y to YN	t_{PLH}	0.16	0.11 + 0.027*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
	t_{PHL}	0.06	0.01 + 0.025*SL	0.02 + 0.017*SL	0.05 + 0.013*SL
	t_R	0.21	0.13 + 0.040*SL	0.13 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.17	0.12 + 0.024*SL	0.14 + 0.019*SL	0.15 + 0.017*SL

KG80 IVCD26

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.24 + 0.018*SL	0.24 + 0.019*SL	0.23 + 0.020*SL
	t_{PHL}	0.14	0.11 + 0.015*SL	0.11 + 0.014*SL	0.12 + 0.012*SL
	t_R	0.43	0.35 + 0.041*SL	0.35 + 0.043*SL	0.34 + 0.043*SL
	t_F	0.29	0.26 + 0.015*SL	0.26 + 0.015*SL	0.24 + 0.018*SL
Y to YN	t_{PLH}	0.13	0.11 + 0.011*SL	0.11 + 0.009*SL	0.12 + 0.008*SL
	t_{PHL}	0.02	0.00 + 0.011*SL	0.01 + 0.008*SL	0.02 + 0.007*SL
	t_R	0.16	0.13 + 0.014*SL	0.13 + 0.013*SL	0.14 + 0.013*SL
	t_F	0.14	0.12 + 0.008*SL	0.12 + 0.008*SL	0.14 + 0.006*SL

KG80 IVCD44

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.16 + 0.011*SL	0.16 + 0.011*SL	0.17 + 0.010*SL
	t_{PHL}	0.07	0.05 + 0.011*SL	0.05 + 0.009*SL	0.06 + 0.008*SL
	t_R	0.26	0.21 + 0.024*SL	0.22 + 0.018*SL	0.21 + 0.021*SL
	t_F	0.19	0.17 + 0.009*SL	0.17 + 0.009*SL	0.16 + 0.010*SL
Y to YN	t_{PLH}	0.14	0.11 + 0.015*SL	0.11 + 0.012*SL	0.13 + 0.010*SL
	t_{PHL}	0.03	0.00 + 0.014*SL	0.01 + 0.011*SL	0.03 + 0.009*SL
	t_R	0.17	0.13 + 0.021*SL	0.13 + 0.020*SL	0.14 + 0.019*SL
	t_F	0.15	0.12 + 0.015*SL	0.13 + 0.010*SL	0.14 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IVCD11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.25 + 0.049*SL	0.25 + 0.049*SL	0.24 + 0.050*SL
	t_{PHL}	0.18	0.12 + 0.030*SL	0.14 + 0.024*SL	0.15 + 0.023*SL
	t_R	0.58	0.38 + 0.103*SL	0.37 + 0.106*SL	0.34 + 0.108*SL
	t_F	0.28	0.21 + 0.038*SL	0.20 + 0.040*SL	0.18 + 0.042*SL
Y to YN	t_{PLH}	0.30	0.20 + 0.051*SL	0.20 + 0.049*SL	0.20 + 0.050*SL
	t_{PHL}	0.15	0.09 + 0.033*SL	0.11 + 0.025*SL	0.13 + 0.023*SL
	t_R	0.46	0.26 + 0.101*SL	0.24 + 0.106*SL	0.22 + 0.108*SL
	t_F	0.25	0.17 + 0.040*SL	0.17 + 0.039*SL	0.14 + 0.042*SL

KGM80 IVCD13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.31 + 0.048*SL	0.31 + 0.049*SL	0.30 + 0.049*SL
	t_{PHL}	0.20	0.15 + 0.028*SL	0.16 + 0.024*SL	0.17 + 0.023*SL
	t_R	0.70	0.49 + 0.105*SL	0.49 + 0.107*SL	0.47 + 0.109*SL
	t_F	0.34	0.27 + 0.033*SL	0.26 + 0.039*SL	0.23 + 0.042*SL
Y to YN	t_{PLH}	0.17	0.12 + 0.022*SL	0.14 + 0.018*SL	0.15 + 0.016*SL
	t_{PHL}	0.06	0.03 + 0.016*SL	0.04 + 0.012*SL	0.07 + 0.009*SL
	t_R	0.22	0.15 + 0.036*SL	0.16 + 0.033*SL	0.14 + 0.035*SL
	t_F	0.15	0.12 + 0.016*SL	0.12 + 0.014*SL	0.14 + 0.013*SL

KGM80 IVCD22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.18 + 0.027*SL	0.19 + 0.025*SL	0.19 + 0.025*SL
	t_{PHL}	0.11	0.07 + 0.020*SL	0.08 + 0.015*SL	0.11 + 0.012*SL
	t_R	0.36	0.26 + 0.048*SL	0.26 + 0.051*SL	0.24 + 0.053*SL
	t_F	0.20	0.16 + 0.022*SL	0.17 + 0.019*SL	0.16 + 0.020*SL
Y to YN	t_{PLH}	0.18	0.12 + 0.032*SL	0.14 + 0.025*SL	0.14 + 0.025*SL
	t_{PHL}	0.07	0.03 + 0.023*SL	0.04 + 0.016*SL	0.09 + 0.012*SL
	t_R	0.24	0.14 + 0.052*SL	0.14 + 0.050*SL	0.12 + 0.053*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.020*SL	0.13 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IVCD26

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.30 + 0.023*SL	0.29 + 0.024*SL	0.29 + 0.025*SL
	t_{PHL}	0.17	0.13 + 0.016*SL	0.14 + 0.013*SL	0.16 + 0.012*SL
	t_R	0.56	0.46 + 0.051*SL	0.46 + 0.053*SL	0.45 + 0.054*SL
	t_F	0.30	0.27 + 0.014*SL	0.26 + 0.018*SL	0.24 + 0.020*SL
Y to YN	t_{PLH}	0.14	0.11 + 0.013*SL	0.12 + 0.010*SL	0.14 + 0.009*SL
	t_{PHL}	0.04	0.02 + 0.009*SL	0.03 + 0.007*SL	0.04 + 0.006*SL
	t_R	0.17	0.14 + 0.019*SL	0.14 + 0.017*SL	0.14 + 0.017*SL
	t_F	0.13	0.11 + 0.009*SL	0.11 + 0.008*SL	0.13 + 0.007*SL

KGM80 IVCD44

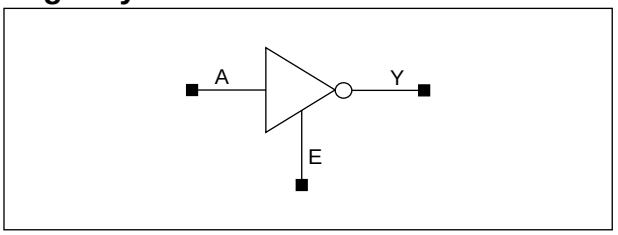
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.18 + 0.015*SL	0.19 + 0.013*SL	0.19 + 0.012*SL
	t_{PHL}	0.09	0.07 + 0.010*SL	0.07 + 0.008*SL	0.09 + 0.007*SL
	t_R	0.31	0.26 + 0.026*SL	0.26 + 0.025*SL	0.25 + 0.026*SL
	t_F	0.18	0.16 + 0.009*SL	0.16 + 0.010*SL	0.17 + 0.009*SL
Y to YN	t_{PLH}	0.15	0.11 + 0.018*SL	0.12 + 0.014*SL	0.15 + 0.012*SL
	t_{PHL}	0.05	0.02 + 0.014*SL	0.03 + 0.010*SL	0.06 + 0.008*SL
	t_R	0.19	0.14 + 0.028*SL	0.15 + 0.025*SL	0.14 + 0.026*SL
	t_F	0.14	0.11 + 0.013*SL	0.11 + 0.011*SL	0.13 + 0.009*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

IVT/IVTD2/IVTD4/IVTD8

Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	1
1	1	0

Cell Data

Input Load (SL)								Output Load (SL)				Gate Count			
KG80															
IVT		*IVTD2*		*IVTD4*		*IVTD8*		*IVT*	IVTD2	*IVTD4*	IVTD8	*IVT*	*IVTD2*	*IVTD4*	*IVTD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
0.9	1.5	0.8	2.4	0.8	2.1	0.8	2.1	0.8	1.2	6.1	11.6	4.0	5.0	8.0	14.0
KGM80															
IVT		*IVTD2*		*IVTD4*		*IVTD8*		*IVT*	IVTD2	*IVTD4*	IVTD8	*IVT*	*IVTD2*	*IVTD4*	*IVTD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
1.0	1.8	1.0	2.7	0.9	2.5	0.9	4.1	1.1	1.6	7.7	14.5	4.0	5.0	8.0	14.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IVT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.38	0.34 + 0.024*SL	0.34 + 0.021*SL	0.34 + 0.021*SL
	t_{PHL}	0.34	0.27 + 0.036*SL	0.27 + 0.035*SL	0.28 + 0.034*SL
	t_R	0.21	0.13 + 0.040*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.068*SL	0.09 + 0.068*SL
E to Y	t_{PLH}	0.22	0.17 + 0.024*SL	0.18 + 0.022*SL	0.19 + 0.021*SL
	t_{PHL}	0.14	0.04 + 0.051*SL	0.07 + 0.037*SL	0.09 + 0.035*SL
	t_R	0.22	0.14 + 0.039*SL	0.13 + 0.041*SL	0.12 + 0.044*SL
	t_F	0.28	0.15 + 0.066*SL	0.16 + 0.062*SL	0.13 + 0.066*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.37	0.37 + 0.000*SL	0.37 + 0.000*SL	0.37 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IVTD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.43	0.40 + 0.014*SL	0.40 + 0.012*SL	0.41 + 0.011*SL
	t_{PHL}	0.37	0.33 + 0.021*SL	0.34 + 0.018*SL	0.34 + 0.017*SL
	t_R	0.19	0.15 + 0.018*SL	0.15 + 0.020*SL	0.14 + 0.021*SL
	t_F	0.19	0.13 + 0.029*SL	0.13 + 0.030*SL	0.11 + 0.033*SL
E to Y	t_{PLH}	0.27	0.24 + 0.014*SL	0.24 + 0.013*SL	0.25 + 0.011*SL
	t_{PHL}	0.07	-0.00 + 0.034*SL	0.02 + 0.024*SL	0.06 + 0.018*SL
	t_R	0.20	0.16 + 0.022*SL	0.17 + 0.018*SL	0.16 + 0.020*SL
	t_F	0.20	0.13 + 0.039*SL	0.14 + 0.031*SL	0.15 + 0.031*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.53	0.53 + 0.000*SL	0.53 + 0.000*SL	0.53 + 0.000*SL

KG80 IVTD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.43 + 0.009*SL	0.43 + 0.008*SL	0.44 + 0.007*SL
	t_{PHL}	0.44	0.42 + 0.011*SL	0.42 + 0.010*SL	0.43 + 0.009*SL
	t_R	0.19	0.17 + 0.011*SL	0.17 + 0.009*SL	0.17 + 0.010*SL
	t_F	0.23	0.20 + 0.013*SL	0.20 + 0.014*SL	0.19 + 0.016*SL
E to Y	t_{PLH}	0.31	0.29 + 0.007*SL	0.29 + 0.008*SL	0.30 + 0.007*SL
	t_{PHL}	0.05	0.02 + 0.015*SL	0.02 + 0.012*SL	0.04 + 0.011*SL
	t_R	0.20	0.18 + 0.010*SL	0.18 + 0.009*SL	0.18 + 0.009*SL
	t_F	0.21	0.19 + 0.013*SL	0.18 + 0.014*SL	0.18 + 0.015*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.59	0.59 + 0.000*SL	0.59 + 0.000*SL	0.59 + 0.000*SL

KG80 IVTD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.59	0.58 + 0.006*SL	0.58 + 0.005*SL	0.58 + 0.005*SL
	t_{PHL}	0.65	0.63 + 0.008*SL	0.64 + 0.006*SL	0.64 + 0.006*SL
	t_R	0.28	0.27 + 0.004*SL	0.27 + 0.004*SL	0.27 + 0.005*SL
	t_F	0.34	0.33 + 0.006*SL	0.33 + 0.006*SL	0.33 + 0.006*SL
E to Y	t_{PLH}	0.45	0.44 + 0.006*SL	0.44 + 0.005*SL	0.45 + 0.005*SL
	t_{PHL}	0.02	0.01 + 0.008*SL	0.01 + 0.007*SL	0.02 + 0.006*SL
	t_R	0.28	0.27 + 0.004*SL	0.27 + 0.005*SL	0.28 + 0.004*SL
	t_F	0.19	0.17 + 0.007*SL	0.17 + 0.007*SL	0.17 + 0.008*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.90	0.90 + 0.000*SL	0.90 + 0.000*SL	0.90 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IVT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.51	0.45 + 0.028*SL	0.46 + 0.026*SL	0.46 + 0.025*SL
	t_{PHL}	0.47	0.39 + 0.041*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.27	0.17 + 0.050*SL	0.16 + 0.053*SL	0.15 + 0.054*SL
	t_F	0.28	0.14 + 0.071*SL	0.13 + 0.073*SL	0.12 + 0.074*SL
E to Y	t_{PLH}	0.31	0.26 + 0.029*SL	0.26 + 0.026*SL	0.27 + 0.025*SL
	t_{PHL}	0.19	0.09 + 0.049*SL	0.12 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.27	0.18 + 0.048*SL	0.17 + 0.052*SL	0.15 + 0.054*SL
	t_F	0.32	0.18 + 0.070*SL	0.17 + 0.070*SL	0.14 + 0.073*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.48	0.48 + 0.000*SL	0.48 + 0.000*SL	0.48 + 0.000*SL

KGM80 IVTD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.56	0.53 + 0.018*SL	0.54 + 0.015*SL	0.55 + 0.013*SL
	t_{PHL}	0.52	0.47 + 0.024*SL	0.48 + 0.021*SL	0.50 + 0.019*SL
	t_R	0.23	0.19 + 0.025*SL	0.18 + 0.025*SL	0.18 + 0.026*SL
	t_F	0.22	0.16 + 0.034*SL	0.15 + 0.035*SL	0.14 + 0.036*SL
E to Y	t_{PLH}	0.38	0.34 + 0.018*SL	0.35 + 0.015*SL	0.37 + 0.013*SL
	t_{PHL}	0.11	0.05 + 0.031*SL	0.07 + 0.022*SL	0.11 + 0.019*SL
	t_R	0.24	0.19 + 0.024*SL	0.19 + 0.025*SL	0.18 + 0.026*SL
	t_F	0.22	0.14 + 0.041*SL	0.16 + 0.034*SL	0.15 + 0.035*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.70	0.70 + 0.000*SL	0.70 + 0.000*SL	0.70 + 0.000*SL

KGM80 IVTD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.59	0.57 + 0.011*SL	0.57 + 0.009*SL	0.58 + 0.008*SL
	t_{PHL}	0.62	0.60 + 0.013*SL	0.60 + 0.012*SL	0.62 + 0.011*SL
	t_R	0.23	0.20 + 0.013*SL	0.21 + 0.013*SL	0.20 + 0.013*SL
	t_F	0.28	0.24 + 0.019*SL	0.24 + 0.018*SL	0.25 + 0.017*SL
E to Y	t_{PLH}	0.43	0.41 + 0.011*SL	0.41 + 0.009*SL	0.43 + 0.008*SL
	t_{PHL}	0.10	0.07 + 0.015*SL	0.07 + 0.012*SL	0.09 + 0.011*SL
	t_R	0.23	0.21 + 0.012*SL	0.21 + 0.013*SL	0.21 + 0.013*SL
	t_F	0.26	0.25 + 0.006*SL	0.23 + 0.015*SL	0.21 + 0.017*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.80	0.80 + -0.001*SL	0.80 + 0.000*SL	0.79 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IVTD8

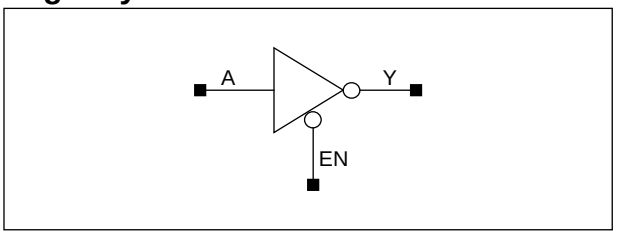
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.77	0.76 + 0.007*SL	0.76 + 0.006*SL	0.77 + 0.005*SL
	t_{PHL}	0.90	0.89 + 0.008*SL	0.89 + 0.007*SL	0.90 + 0.006*SL
	t_R	0.31	0.30 + 0.006*SL	0.30 + 0.006*SL	0.30 + 0.006*SL
	t_F	0.39	0.38 + 0.008*SL	0.37 + 0.009*SL	0.38 + 0.008*SL
E to Y	t_{PLH}	0.62	0.61 + 0.006*SL	0.61 + 0.006*SL	0.62 + 0.005*SL
	t_{PHL}	0.07	0.06 + 0.008*SL	0.06 + 0.007*SL	0.07 + 0.006*SL
	t_R	0.31	0.30 + 0.006*SL	0.30 + 0.006*SL	0.30 + 0.006*SL
	t_F	0.23	0.22 + 0.005*SL	0.21 + 0.008*SL	0.20 + 0.009*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	1.22	1.22 + 0.000*SL	1.22 + 0.000*SL	1.22 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

IVTN/IVTND2/IVTND4/IVTND8

Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	1
1	0	0

Cell Data

Input Load (SL)								Output Load (SL)			
KG80											
IVTN		*IVTND2*		*IVTND4*		*IVTND8*		*IVTN*	*IVTND2*	*IVTND4*	*IVTND8*
A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y
0.9	0.9	0.9	0.9	0.8	0.8	0.8	0.8	1.3	1.1	6.1	11.6
KGM80											
IVTN		*IVTND2*		*IVTND4*		*IVTND8*		*IVTN*	*IVTND2*	*IVTND4*	*IVTND8*
A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y
1.0	1.0	1.0	1.0	0.9	0.9	0.9	0.9	1.7	1.5	7.7	14.5

KG80/KGM80			
Gate Count			
IVTN	*IVTND2*	*IVTND4*	*IVTND8*
4.0	5.0	8.0	14.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IVTN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.35 + 0.023*SL	0.36 + 0.021*SL	0.36 + 0.021*SL
	t_{PHL}	0.35	0.28 + 0.036*SL	0.29 + 0.035*SL	0.29 + 0.034*SL
	t_R	0.22	0.14 + 0.041*SL	0.13 + 0.043*SL	0.13 + 0.044*SL
	t_F	0.27	0.14 + 0.065*SL	0.13 + 0.068*SL	0.13 + 0.069*SL
EN to Y	t_{PLH}	0.42	0.38 + 0.023*SL	0.38 + 0.021*SL	0.38 + 0.021*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.28 + 0.036*SL	0.28 + 0.035*SL
	t_R	0.22	0.14 + 0.041*SL	0.14 + 0.043*SL	0.13 + 0.044*SL
	t_F	0.28	0.15 + 0.065*SL	0.15 + 0.067*SL	0.14 + 0.068*SL
	t_{PLZ}	0.16	0.16 + 0.000*SL	0.16 + 0.000*SL	0.16 + 0.000*SL
	t_{PHZ}	0.37	0.37 + 0.000*SL	0.37 + 0.000*SL	0.37 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 IVTND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.41 + 0.015*SL	0.41 + 0.013*SL	0.42 + 0.011*SL
	t_{PHL}	0.39	0.35 + 0.021*SL	0.35 + 0.018*SL	0.36 + 0.018*SL
	t_R	0.19	0.15 + 0.019*SL	0.15 + 0.020*SL	0.15 + 0.020*SL
	t_F	0.20	0.14 + 0.028*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
EN to Y	t_{PLH}	0.50	0.47 + 0.015*SL	0.48 + 0.013*SL	0.49 + 0.011*SL
	t_{PHL}	0.30	0.25 + 0.027*SL	0.26 + 0.021*SL	0.28 + 0.018*SL
	t_R	0.20	0.16 + 0.019*SL	0.16 + 0.020*SL	0.16 + 0.020*SL
	t_F	0.17	0.10 + 0.036*SL	0.11 + 0.032*SL	0.10 + 0.033*SL
	t_{PLZ}	0.21	0.20 + 0.001*SL	0.21 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.59	0.58 + 0.001*SL	0.59 + 0.000*SL	0.59 + 0.000*SL

KG80 IVTND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.43 + 0.009*SL	0.43 + 0.008*SL	0.44 + 0.007*SL
	t_{PHL}	0.44	0.42 + 0.011*SL	0.42 + 0.010*SL	0.43 + 0.009*SL
	t_R	0.19	0.17 + 0.011*SL	0.17 + 0.009*SL	0.17 + 0.010*SL
	t_F	0.23	0.20 + 0.014*SL	0.20 + 0.015*SL	0.19 + 0.016*SL
EN to Y	t_{PLH}	0.52	0.51 + 0.009*SL	0.51 + 0.008*SL	0.52 + 0.007*SL
	t_{PHL}	0.29	0.26 + 0.013*SL	0.26 + 0.011*SL	0.27 + 0.010*SL
	t_R	0.19	0.17 + 0.012*SL	0.18 + 0.009*SL	0.17 + 0.010*SL
	t_F	0.18	0.16 + 0.011*SL	0.15 + 0.015*SL	0.14 + 0.016*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.64	0.64 + 0.000*SL	0.64 + 0.000*SL	0.64 + 0.000*SL

KG80 IVTND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.59	0.58 + 0.006*SL	0.58 + 0.005*SL	0.58 + 0.005*SL
	t_{PHL}	0.65	0.63 + 0.008*SL	0.64 + 0.006*SL	0.64 + 0.006*SL
	t_R	0.28	0.27 + 0.004*SL	0.27 + 0.004*SL	0.27 + 0.005*SL
	t_F	0.34	0.33 + 0.007*SL	0.33 + 0.006*SL	0.33 + 0.006*SL
EN to Y	t_{PLH}	0.73	0.72 + 0.006*SL	0.72 + 0.005*SL	0.73 + 0.005*SL
	t_{PHL}	0.31	0.29 + 0.008*SL	0.29 + 0.007*SL	0.30 + 0.006*SL
	t_R	0.29	0.28 + 0.005*SL	0.28 + 0.004*SL	0.28 + 0.004*SL
	t_F	0.18	0.16 + 0.007*SL	0.16 + 0.008*SL	0.16 + 0.008*SL
	t_{PLZ}	0.27	0.27 + 0.000*SL	0.28 + -0.001*SL	0.27 + 0.001*SL
	t_{PHZ}	1.01	1.01 + 0.000*SL	1.01 + 0.000*SL	1.01 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IVTN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.53	0.47 + 0.027*SL	0.48 + 0.025*SL	0.48 + 0.025*SL
	t_{PHL}	0.48	0.40 + 0.041*SL	0.41 + 0.038*SL	0.42 + 0.037*SL
	t_R	0.29	0.19 + 0.051*SL	0.18 + 0.053*SL	0.17 + 0.054*SL
	t_F	0.33	0.19 + 0.071*SL	0.18 + 0.073*SL	0.17 + 0.074*SL
EN to Y	t_{PLH}	0.57	0.51 + 0.028*SL	0.52 + 0.026*SL	0.53 + 0.025*SL
	t_{PHL}	0.44	0.36 + 0.043*SL	0.37 + 0.038*SL	0.38 + 0.037*SL
	t_R	0.29	0.19 + 0.051*SL	0.18 + 0.053*SL	0.17 + 0.054*SL
	t_F	0.34	0.20 + 0.070*SL	0.20 + 0.072*SL	0.18 + 0.074*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.52	0.52 + 0.000*SL	0.52 + 0.000*SL	0.51 + 0.000*SL

KGM80 IVTND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.58	0.55 + 0.018*SL	0.55 + 0.015*SL	0.57 + 0.013*SL
	t_{PHL}	0.54	0.49 + 0.025*SL	0.50 + 0.021*SL	0.52 + 0.019*SL
	t_R	0.24	0.19 + 0.024*SL	0.19 + 0.025*SL	0.18 + 0.026*SL
	t_F	0.23	0.16 + 0.035*SL	0.16 + 0.035*SL	0.15 + 0.036*SL
EN to Y	t_{PLH}	0.68	0.64 + 0.018*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_{PHL}	0.40	0.35 + 0.029*SL	0.37 + 0.022*SL	0.40 + 0.019*SL
	t_R	0.24	0.19 + 0.026*SL	0.20 + 0.025*SL	0.19 + 0.025*SL
	t_F	0.21	0.14 + 0.039*SL	0.15 + 0.036*SL	0.14 + 0.036*SL
	t_{PLZ}	0.25	0.25 + 0.000*SL	0.25 + 0.000*SL	0.25 + 0.000*SL
	t_{PHZ}	0.81	0.81 + 0.001*SL	0.81 + 0.000*SL	0.81 + 0.000*SL

KGM80 IVTND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.59	0.57 + 0.011*SL	0.57 + 0.009*SL	0.58 + 0.008*SL
	t_{PHL}	0.62	0.60 + 0.013*SL	0.60 + 0.012*SL	0.62 + 0.011*SL
	t_R	0.23	0.20 + 0.013*SL	0.21 + 0.013*SL	0.20 + 0.013*SL
	t_F	0.28	0.24 + 0.019*SL	0.24 + 0.018*SL	0.24 + 0.018*SL
EN to Y	t_{PLH}	0.70	0.68 + 0.011*SL	0.69 + 0.009*SL	0.70 + 0.008*SL
	t_{PHL}	0.37	0.35 + 0.014*SL	0.35 + 0.012*SL	0.37 + 0.011*SL
	t_R	0.24	0.21 + 0.013*SL	0.21 + 0.013*SL	0.21 + 0.013*SL
	t_F	0.26	0.25 + 0.004*SL	0.22 + 0.016*SL	0.20 + 0.018*SL
	t_{PLZ}	0.24	0.24 + 0.000*SL	0.24 + 0.000*SL	0.25 + 0.000*SL
	t_{PHZ}	0.89	0.89 + -0.001*SL	0.89 + 0.000*SL	0.89 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 IVTND8

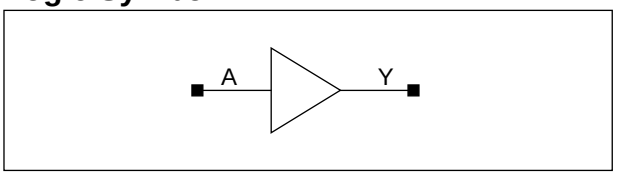
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.77	0.76 + 0.007*SL	0.76 + 0.006*SL	0.77 + 0.005*SL
	t_{PHL}	0.90	0.89 + 0.008*SL	0.89 + 0.007*SL	0.90 + 0.007*SL
	t_R	0.31	0.30 + 0.006*SL	0.30 + 0.006*SL	0.30 + 0.006*SL
	t_F	0.39	0.38 + 0.008*SL	0.37 + 0.009*SL	0.38 + 0.008*SL
EN to Y	t_{PLH}	0.99	0.97 + 0.007*SL	0.98 + 0.006*SL	0.99 + 0.005*SL
	t_{PHL}	0.42	0.40 + 0.008*SL	0.40 + 0.007*SL	0.41 + 0.006*SL
	t_R	0.32	0.31 + 0.006*SL	0.31 + 0.006*SL	0.31 + 0.006*SL
	t_F	0.25	0.24 + 0.005*SL	0.23 + 0.009*SL	0.22 + 0.009*SL
	t_{PLZ}	0.33	0.33 + -0.001*SL	0.33 + 0.000*SL	0.33 + 0.000*SL
	t_{PHZ}	1.39	1.39 + -0.001*SL	1.39 + 0.000*SL	1.39 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

NID/NID2/NID3/NID4/NID6/NID8

Non-Inverting Buffer with 1X/2X/3X/4X/6X/8X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)						Gate Count					
KG80											
NID	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*	*NID*	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*
A	A	A	A	A	A						
0.9	0.9	0.8	1.7	1.7	1.7	1.0	2.0	2.0	3.0	4.0	5.0
KGM80											
NID	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*	*NID*	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*
A	A	A	A	A	A						
1.0	1.0	1.0	1.9	1.9	2.0	1.0	2.0	2.0	3.0	4.0	5.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NID

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.13 + 0.041*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
	t_{PHL}	0.26	0.21 + 0.028*SL	0.22 + 0.024*SL	0.22 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.16	0.09 + 0.035*SL	0.07 + 0.041*SL	0.06 + 0.042*SL

KG80 NID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.16 + 0.021*SL	0.16 + 0.020*SL	0.16 + 0.021*SL
	t_{PHL}	0.27	0.24 + 0.016*SL	0.25 + 0.014*SL	0.26 + 0.012*SL
	t_R	0.18	0.10 + 0.043*SL	0.10 + 0.043*SL	0.08 + 0.045*SL
	t_F	0.13	0.09 + 0.019*SL	0.09 + 0.019*SL	0.09 + 0.020*SL

KG80 NID3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.19 + 0.015*SL	0.19 + 0.014*SL	0.20 + 0.014*SL
	t_{PHL}	0.29	0.27 + 0.013*SL	0.27 + 0.011*SL	0.28 + 0.009*SL
	t_R	0.16	0.11 + 0.023*SL	0.10 + 0.029*SL	0.10 + 0.029*SL
	t_F	0.14	0.11 + 0.013*SL	0.11 + 0.013*SL	0.11 + 0.013*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NID4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.18	0.16 + 0.011*SL	0.16 + 0.010*SL	0.16 + 0.010*SL
	t_{PHL}	0.25	0.24 + 0.009*SL	0.24 + 0.008*SL	0.25 + 0.007*SL
	t_R	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.09 + 0.022*SL
	t_F	0.11	0.09 + 0.010*SL	0.09 + 0.010*SL	0.09 + 0.010*SL

KG80 NID6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.19 + 0.008*SL	0.19 + 0.007*SL	0.19 + 0.007*SL
	t_{PHL}	0.28	0.27 + 0.007*SL	0.27 + 0.006*SL	0.28 + 0.005*SL
	t_R	0.14	0.10 + 0.016*SL	0.11 + 0.012*SL	0.10 + 0.015*SL
	t_F	0.12	0.11 + 0.008*SL	0.11 + 0.006*SL	0.11 + 0.007*SL

KG80 NID8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.22 + 0.006*SL	0.22 + 0.006*SL	0.23 + 0.005*SL
	t_{PHL}	0.31	0.30 + 0.006*SL	0.30 + 0.005*SL	0.31 + 0.004*SL
	t_R	0.14	0.11 + 0.011*SL	0.11 + 0.013*SL	0.15 + 0.007*SL
	t_F	0.14	0.12 + 0.006*SL	0.13 + 0.005*SL	0.13 + 0.005*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NID

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.18 + 0.051*SL	0.18 + 0.050*SL	0.18 + 0.050*SL
	t_{PHL}	0.32	0.26 + 0.030*SL	0.27 + 0.024*SL	0.29 + 0.023*SL
	t_R	0.34	0.13 + 0.106*SL	0.12 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.18	0.11 + 0.036*SL	0.10 + 0.041*SL	0.08 + 0.043*SL

KGM80 NID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.21 + 0.026*SL	0.22 + 0.025*SL	0.22 + 0.025*SL
	t_{PHL}	0.35	0.31 + 0.019*SL	0.32 + 0.014*SL	0.34 + 0.012*SL
	t_R	0.24	0.13 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.16	0.11 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.021*SL

KGM80 NID3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.25 + 0.018*SL	0.25 + 0.017*SL	0.26 + 0.017*SL
	t_{PHL}	0.38	0.35 + 0.015*SL	0.36 + 0.011*SL	0.38 + 0.009*SL
	t_R	0.21	0.14 + 0.033*SL	0.14 + 0.035*SL	0.13 + 0.036*SL
	t_F	0.16	0.13 + 0.016*SL	0.14 + 0.014*SL	0.14 + 0.014*SL

KGM80 NID4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.21 + 0.014*SL	0.21 + 0.013*SL	0.22 + 0.012*SL
	t_{PHL}	0.32	0.30 + 0.011*SL	0.31 + 0.008*SL	0.33 + 0.007*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.026*SL	0.13 + 0.027*SL
	t_F	0.13	0.11 + 0.012*SL	0.11 + 0.011*SL	0.12 + 0.010*SL

KGM80 NID6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.25 + 0.010*SL	0.25 + 0.009*SL	0.25 + 0.008*SL
	t_{PHL}	0.37	0.35 + 0.008*SL	0.35 + 0.007*SL	0.37 + 0.005*SL
	t_R	0.18	0.14 + 0.017*SL	0.14 + 0.017*SL	0.14 + 0.017*SL
	t_F	0.15	0.13 + 0.008*SL	0.13 + 0.008*SL	0.14 + 0.007*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NID8

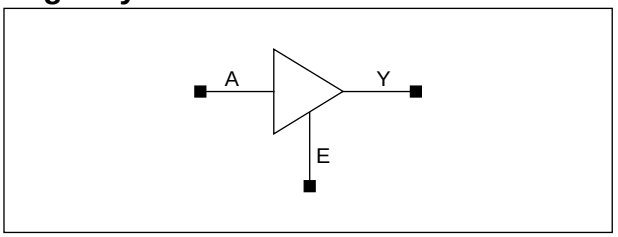
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.28 + 0.008*SL	0.28 + 0.007*SL	0.29 + 0.006*SL
	t_{PHL}	0.41	0.40 + 0.007*SL	0.40 + 0.006*SL	0.41 + 0.005*SL
	t_R	0.18	0.15 + 0.013*SL	0.15 + 0.012*SL	0.15 + 0.013*SL
	t_F	0.17	0.15 + 0.007*SL	0.15 + 0.006*SL	0.16 + 0.006*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

NIT/NITD2/NITD4/NITD8

Non-Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	0
1	1	1

Cell Data

Input Load (SL)								Output Load (SL)				Gate Count			
KG80															
NIT		*NITD2*		*NITD4*		*NITD8*		*NIT*	*NITD2*	*NITD4*	*NITD8*	*NIT*	*NITD2*	*NITD4*	*NITD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
0.9	1.6	0.9	2.4	0.9	2.2	0.9	3.6	0.8	1.3	5.8	11.6	3.0	4.0	7.0	13.0
KGM80															
NIT		*NITD2*		*NITD4*		*NITD8*		*NIT*	*NITD2*	*NITD4*	*NITD8*	*NIT*	*NITD2*	*NITD4*	*NITD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
1.0	1.9	1.1	2.8	0.9	2.5	0.9	4.1	1.1	1.8	7.2	14.3	3.0	4.0	7.0	13.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.19 + 0.024*SL	0.19 + 0.022*SL	0.20 + 0.021*SL
	t_{PHL}	0.34	0.27 + 0.036*SL	0.28 + 0.034*SL	0.28 + 0.034*SL
	t_R	0.22	0.14 + 0.038*SL	0.13 + 0.042*SL	0.12 + 0.044*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.067*SL	0.09 + 0.068*SL
E to Y	t_{PLH}	0.22	0.17 + 0.023*SL	0.18 + 0.022*SL	0.18 + 0.021*SL
	t_{PHL}	0.14	0.04 + 0.051*SL	0.07 + 0.037*SL	0.09 + 0.035*SL
	t_R	0.21	0.14 + 0.037*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.28	0.15 + 0.066*SL	0.16 + 0.062*SL	0.13 + 0.066*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.36	0.36 + 0.000*SL	0.36 + 0.000*SL	0.36 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NITD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.27 + 0.015*SL	0.28 + 0.013*SL	0.29 + 0.011*SL
	t_{PHL}	0.39	0.35 + 0.020*SL	0.36 + 0.018*SL	0.36 + 0.017*SL
	t_R	0.21	0.17 + 0.015*SL	0.17 + 0.018*SL	0.15 + 0.020*SL
	t_F	0.20	0.15 + 0.027*SL	0.14 + 0.030*SL	0.13 + 0.032*SL
E to Y	t_{PLH}	0.28	0.25 + 0.015*SL	0.25 + 0.013*SL	0.27 + 0.011*SL
	t_{PHL}	0.07	0.01 + 0.033*SL	0.03 + 0.024*SL	0.07 + 0.018*SL
	t_R	0.21	0.18 + 0.018*SL	0.18 + 0.018*SL	0.16 + 0.020*SL
	t_F	0.21	0.13 + 0.038*SL	0.15 + 0.031*SL	0.15 + 0.031*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.55	0.55 + 0.000*SL	0.55 + 0.000*SL	0.55 + 0.000*SL

KG80 NITD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.29 + 0.011*SL	0.30 + 0.008*SL	0.31 + 0.007*SL
	t_{PHL}	0.45	0.42 + 0.012*SL	0.43 + 0.010*SL	0.44 + 0.009*SL
	t_R	0.19	0.18 + 0.005*SL	0.17 + 0.009*SL	0.17 + 0.010*SL
	t_F	0.22	0.19 + 0.014*SL	0.19 + 0.015*SL	0.19 + 0.015*SL
E to Y	t_{PLH}	0.31	0.28 + 0.011*SL	0.29 + 0.008*SL	0.30 + 0.007*SL
	t_{PHL}	0.04	0.01 + 0.015*SL	0.02 + 0.013*SL	0.03 + 0.011*SL
	t_R	0.19	0.18 + 0.008*SL	0.17 + 0.009*SL	0.17 + 0.010*SL
	t_F	0.20	0.18 + 0.013*SL	0.17 + 0.014*SL	0.17 + 0.015*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.58	0.58 + 0.000*SL	0.58 + 0.000*SL	0.58 + 0.000*SL

KG80 NITD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.46	0.45 + 0.006*SL	0.45 + 0.005*SL	0.45 + 0.005*SL
	t_{PHL}	0.66	0.64 + 0.007*SL	0.64 + 0.006*SL	0.65 + 0.006*SL
	t_R	0.28	0.27 + 0.004*SL	0.27 + 0.005*SL	0.27 + 0.005*SL
	t_F	0.34	0.33 + 0.006*SL	0.33 + 0.006*SL	0.33 + 0.007*SL
E to Y	t_{PLH}	0.45	0.44 + 0.006*SL	0.44 + 0.005*SL	0.44 + 0.005*SL
	t_{PHL}	0.02	0.01 + 0.008*SL	0.01 + 0.007*SL	0.02 + 0.006*SL
	t_R	0.28	0.27 + 0.004*SL	0.27 + 0.004*SL	0.27 + 0.005*SL
	t_F	0.19	0.17 + 0.007*SL	0.17 + 0.007*SL	0.17 + 0.008*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.90	0.90 + 0.000*SL	0.90 + 0.000*SL	0.90 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.26 + 0.029*SL	0.27 + 0.026*SL	0.28 + 0.025*SL
	t_{PHL}	0.44	0.36 + 0.041*SL	0.37 + 0.038*SL	0.38 + 0.037*SL
	t_R	0.27	0.17 + 0.049*SL	0.16 + 0.052*SL	0.15 + 0.054*SL
	t_F	0.28	0.14 + 0.070*SL	0.13 + 0.073*SL	0.12 + 0.074*SL
E to Y	t_{PLH}	0.31	0.25 + 0.028*SL	0.26 + 0.026*SL	0.27 + 0.025*SL
	t_{PHL}	0.19	0.09 + 0.050*SL	0.12 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.27	0.17 + 0.049*SL	0.16 + 0.052*SL	0.14 + 0.054*SL
	t_F	0.31	0.17 + 0.070*SL	0.17 + 0.070*SL	0.14 + 0.073*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.47	0.47 + 0.000*SL	0.47 + 0.000*SL	0.47 + 0.000*SL

KGM80 NITD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.37 + 0.018*SL	0.38 + 0.015*SL	0.39 + 0.013*SL
	t_{PHL}	0.52	0.47 + 0.024*SL	0.48 + 0.021*SL	0.49 + 0.019*SL
	t_R	0.24	0.19 + 0.025*SL	0.19 + 0.025*SL	0.18 + 0.025*SL
	t_F	0.24	0.17 + 0.034*SL	0.17 + 0.034*SL	0.16 + 0.036*SL
E to Y	t_{PLH}	0.39	0.35 + 0.018*SL	0.36 + 0.015*SL	0.38 + 0.013*SL
	t_{PHL}	0.12	0.06 + 0.031*SL	0.08 + 0.022*SL	0.12 + 0.019*SL
	t_R	0.24	0.19 + 0.026*SL	0.19 + 0.025*SL	0.18 + 0.026*SL
	t_F	0.23	0.15 + 0.039*SL	0.17 + 0.034*SL	0.15 + 0.035*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.74	0.74 + 0.000*SL	0.74 + 0.000*SL	0.74 + 0.000*SL

KGM80 NITD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.42	0.40 + 0.011*SL	0.41 + 0.009*SL	0.42 + 0.008*SL
	t_{PHL}	0.60	0.57 + 0.014*SL	0.58 + 0.012*SL	0.59 + 0.010*SL
	t_R	0.22	0.20 + 0.013*SL	0.20 + 0.013*SL	0.20 + 0.013*SL
	t_F	0.27	0.23 + 0.017*SL	0.23 + 0.018*SL	0.24 + 0.017*SL
E to Y	t_{PLH}	0.42	0.40 + 0.010*SL	0.41 + 0.009*SL	0.42 + 0.008*SL
	t_{PHL}	0.09	0.06 + 0.015*SL	0.06 + 0.012*SL	0.08 + 0.010*SL
	t_R	0.22	0.20 + 0.012*SL	0.20 + 0.013*SL	0.20 + 0.013*SL
	t_F	0.25	0.23 + 0.008*SL	0.21 + 0.016*SL	0.20 + 0.017*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.79	0.79 + -0.001*SL	0.79 + 0.000*SL	0.79 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NITD8

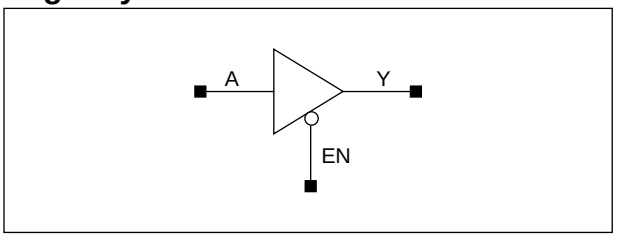
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.61	0.60 + 0.007*SL	0.60 + 0.006*SL	0.61 + 0.005*SL
	t_{PHL}	0.89	0.87 + 0.008*SL	0.88 + 0.007*SL	0.89 + 0.006*SL
	t_R	0.31	0.30 + 0.007*SL	0.30 + 0.006*SL	0.30 + 0.006*SL
	t_F	0.39	0.38 + 0.008*SL	0.37 + 0.009*SL	0.38 + 0.008*SL
E to Y	t_{PLH}	0.61	0.60 + 0.006*SL	0.60 + 0.006*SL	0.61 + 0.005*SL
	t_{PHL}	0.07	0.06 + 0.008*SL	0.06 + 0.007*SL	0.07 + 0.006*SL
	t_R	0.31	0.30 + 0.006*SL	0.30 + 0.006*SL	0.30 + 0.006*SL
	t_F	0.23	0.22 + 0.004*SL	0.21 + 0.008*SL	0.20 + 0.009*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	1.22	1.23 + -0.001*SL	1.22 + 0.000*SL	1.22 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

NITN/NITND2/NITND4/NITND8

Non-Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	0
1	0	1

Cell Data

Input Load (SL)								Output Load (SL)			
KG80											
NITN		*NITND2*		*NITND4*		*NITND8*		*NITN*	*NITND2*	*NITND4*	*NITND8*
A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y
0.9	0.9	0.9	0.9	0.8	0.8	0.9	0.8	0.9	1.1	5.8	11.6
KGM80											
NITN		*NITND2*		*NITND4*		*NITND8*		*NITN*	*NITND2*	*NITND4*	*NITND8*
A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y
0.7	1.0	0.7	1.0	0.6	0.9	0.6	0.9	1.2	1.5	7.2	14.3

KG80/KGM80			
Gate Count			
NITN	*NITND2*	*NITND4*	*NITND8*
3.0	5.0	8.0	14.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NITN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.19 + 0.023*SL	0.19 + 0.022*SL	0.20 + 0.021*SL
	t_{PHL}	0.35	0.27 + 0.036*SL	0.28 + 0.035*SL	0.28 + 0.034*SL
	t_R	0.22	0.14 + 0.037*SL	0.13 + 0.042*SL	0.12 + 0.044*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.09 + 0.069*SL
EN to Y	t_{PLH}	0.41	0.36 + 0.024*SL	0.36 + 0.021*SL	0.37 + 0.021*SL
	t_{PHL}	0.33	0.25 + 0.041*SL	0.26 + 0.036*SL	0.27 + 0.034*SL
	t_R	0.21	0.13 + 0.041*SL	0.12 + 0.042*SL	0.11 + 0.044*SL
	t_F	0.25	0.11 + 0.065*SL	0.11 + 0.067*SL	0.10 + 0.068*SL
	t_{PLZ}	0.16	0.16 + 0.000*SL	0.16 + 0.000*SL	0.16 + 0.000*SL
	t_{PHZ}	0.36	0.36 + 0.001*SL	0.36 + 0.000*SL	0.37 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 NITND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.27 + 0.015*SL	0.27 + 0.013*SL	0.29 + 0.011*SL
	t_{PHL}	0.39	0.35 + 0.021*SL	0.36 + 0.018*SL	0.36 + 0.017*SL
	t_R	0.20	0.17 + 0.016*SL	0.16 + 0.019*SL	0.15 + 0.020*SL
	t_F	0.20	0.14 + 0.028*SL	0.14 + 0.030*SL	0.12 + 0.032*SL
EN to Y	t_{PLH}	0.50	0.47 + 0.016*SL	0.48 + 0.013*SL	0.48 + 0.011*SL
	t_{PHL}	0.30	0.24 + 0.027*SL	0.26 + 0.021*SL	0.28 + 0.018*SL
	t_R	0.20	0.17 + 0.017*SL	0.16 + 0.020*SL	0.16 + 0.020*SL
	t_F	0.17	0.10 + 0.036*SL	0.11 + 0.033*SL	0.10 + 0.033*SL
	t_{PLZ}	0.20	0.20 + 0.001*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.59	0.59 + 0.001*SL	0.59 + 0.000*SL	0.59 + 0.000*SL

KG80 NITND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.29 + 0.011*SL	0.30 + 0.008*SL	0.31 + 0.007*SL
	t_{PHL}	0.45	0.42 + 0.012*SL	0.43 + 0.010*SL	0.44 + 0.009*SL
	t_R	0.19	0.18 + 0.005*SL	0.17 + 0.009*SL	0.17 + 0.010*SL
	t_F	0.22	0.19 + 0.014*SL	0.19 + 0.014*SL	0.19 + 0.015*SL
EN to Y	t_{PLH}	0.52	0.50 + 0.009*SL	0.50 + 0.008*SL	0.51 + 0.007*SL
	t_{PHL}	0.28	0.25 + 0.012*SL	0.26 + 0.011*SL	0.26 + 0.010*SL
	t_R	0.19	0.17 + 0.010*SL	0.17 + 0.009*SL	0.16 + 0.010*SL
	t_F	0.17	0.16 + 0.005*SL	0.14 + 0.015*SL	0.14 + 0.016*SL
	t_{PLZ}	0.20	0.20 + -0.001*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.64	0.64 + -0.001*SL	0.64 + 0.000*SL	0.64 + 0.000*SL

KG80 NITND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.46	0.45 + 0.006*SL	0.45 + 0.005*SL	0.45 + 0.005*SL
	t_{PHL}	0.66	0.64 + 0.007*SL	0.64 + 0.006*SL	0.65 + 0.006*SL
	t_R	0.28	0.27 + 0.004*SL	0.27 + 0.004*SL	0.27 + 0.005*SL
	t_F	0.34	0.33 + 0.006*SL	0.33 + 0.006*SL	0.33 + 0.007*SL
EN to Y	t_{PLH}	0.73	0.72 + 0.006*SL	0.72 + 0.005*SL	0.72 + 0.005*SL
	t_{PHL}	0.31	0.29 + 0.008*SL	0.29 + 0.007*SL	0.30 + 0.006*SL
	t_R	0.28	0.28 + 0.004*SL	0.28 + 0.004*SL	0.27 + 0.005*SL
	t_F	0.18	0.16 + 0.007*SL	0.16 + 0.007*SL	0.16 + 0.008*SL
	t_{PLZ}	0.28	0.27 + 0.001*SL	0.28 + 0.000*SL	0.28 + -0.001*SL
	t_{PHZ}	1.01	1.01 + 0.000*SL	1.01 + 0.000*SL	1.01 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NITN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.26 + 0.028*SL	0.27 + 0.026*SL	0.28 + 0.025*SL
	t_{PHL}	0.45	0.36 + 0.041*SL	0.37 + 0.038*SL	0.38 + 0.037*SL
	t_R	0.27	0.17 + 0.049*SL	0.16 + 0.052*SL	0.15 + 0.054*SL
	t_F	0.29	0.15 + 0.072*SL	0.14 + 0.073*SL	0.13 + 0.074*SL
EN to Y	t_{PLH}	0.54	0.48 + 0.029*SL	0.49 + 0.026*SL	0.50 + 0.025*SL
	t_{PHL}	0.42	0.34 + 0.044*SL	0.35 + 0.038*SL	0.36 + 0.037*SL
	t_R	0.27	0.17 + 0.050*SL	0.16 + 0.052*SL	0.15 + 0.054*SL
	t_F	0.30	0.16 + 0.072*SL	0.15 + 0.073*SL	0.14 + 0.074*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.51	0.51 + 0.000*SL	0.51 + 0.000*SL	0.51 + 0.000*SL

KGM80 NITND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.37 + 0.018*SL	0.38 + 0.015*SL	0.40 + 0.013*SL
	t_{PHL}	0.52	0.47 + 0.025*SL	0.48 + 0.021*SL	0.50 + 0.019*SL
	t_R	0.24	0.19 + 0.025*SL	0.19 + 0.025*SL	0.18 + 0.025*SL
	t_F	0.23	0.16 + 0.034*SL	0.16 + 0.035*SL	0.15 + 0.036*SL
EN to Y	t_{PLH}	0.67	0.64 + 0.018*SL	0.65 + 0.015*SL	0.66 + 0.013*SL
	t_{PHL}	0.40	0.34 + 0.029*SL	0.36 + 0.022*SL	0.39 + 0.019*SL
	t_R	0.24	0.19 + 0.025*SL	0.19 + 0.025*SL	0.18 + 0.025*SL
	t_F	0.21	0.14 + 0.038*SL	0.14 + 0.036*SL	0.14 + 0.036*SL
	t_{PLZ}	0.25	0.25 + 0.000*SL	0.25 + 0.000*SL	0.25 + 0.000*SL
	t_{PHZ}	0.82	0.82 + -0.001*SL	0.82 + 0.000*SL	0.81 + 0.000*SL

KGM80 NITND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.42	0.40 + 0.011*SL	0.41 + 0.009*SL	0.42 + 0.008*SL
	t_{PHL}	0.60	0.57 + 0.014*SL	0.58 + 0.012*SL	0.59 + 0.010*SL
	t_R	0.22	0.20 + 0.013*SL	0.20 + 0.013*SL	0.20 + 0.013*SL
	t_F	0.27	0.23 + 0.017*SL	0.23 + 0.018*SL	0.24 + 0.017*SL
EN to Y	t_{PLH}	0.70	0.68 + 0.010*SL	0.68 + 0.009*SL	0.70 + 0.008*SL
	t_{PHL}	0.37	0.34 + 0.014*SL	0.34 + 0.012*SL	0.36 + 0.010*SL
	t_R	0.23	0.20 + 0.013*SL	0.20 + 0.013*SL	0.20 + 0.013*SL
	t_F	0.24	0.22 + 0.010*SL	0.20 + 0.016*SL	0.19 + 0.017*SL
	t_{PLZ}	0.24	0.25 + -0.001*SL	0.24 + 0.000*SL	0.25 + 0.000*SL
	t_{PHZ}	0.88	0.89 + -0.001*SL	0.88 + 0.000*SL	0.88 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 NITND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.61	0.60 + 0.007*SL	0.60 + 0.006*SL	0.61 + 0.005*SL
	t_{PHL}	0.89	0.87 + 0.008*SL	0.88 + 0.007*SL	0.88 + 0.006*SL
	t_R	0.31	0.30 + 0.006*SL	0.30 + 0.006*SL	0.30 + 0.006*SL
	t_F	0.39	0.37 + 0.009*SL	0.38 + 0.008*SL	0.38 + 0.008*SL
EN to Y	t_{PLH}	0.98	0.97 + 0.007*SL	0.97 + 0.006*SL	0.98 + 0.005*SL
	t_{PHL}	0.41	0.40 + 0.009*SL	0.40 + 0.007*SL	0.41 + 0.006*SL
	t_R	0.32	0.31 + 0.006*SL	0.31 + 0.006*SL	0.30 + 0.006*SL
	t_F	0.25	0.24 + 0.005*SL	0.23 + 0.008*SL	0.22 + 0.009*SL
	t_{PLZ}	0.33	0.33 + 0.000*SL	0.33 + 0.000*SL	0.33 + 0.000*SL
	t_{PHZ}	1.39	1.39 + -0.001*SL	1.39 + 0.000*SL	1.39 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FLIP-FLOPS

Cell List

Cell Name	Function Description
FD1	D Flip-Flop
FD1D2	D Flip-Flop with 2X Drive
FD1CS	D Flip-Flop with Scan Clock
FD1CSD2	D Flip-Flop with Scan Clock, 2X Drive
FD1S	D Flip-Flop with Scan
FD1SD2	D Flip-Flop with Scan, 2X Drive
FD1Q	D Flip-Flop with Q Output Only
FD1QD2	D Flip-Flop with Q Output Only, 2X Drive
FD1X2	2-Bit D Flip-Flop
FD1X4	4-Bit D Flip-Flop
YFD1	Fast D Flip-Flop
YFD1D2	Fast D Flip-Flop with 2X Drive
FD2	D Flip-Flop with Reset
FD2D2	D Flip-Flop with Reset, 2X Drive
FD2CS	D Flip-Flop with Reset, Scan Clock
FD2CSD2	D Flip-Flop with Reset, Scan Clock, 2X Drive
FD2S	D Flip-Flop with Reset, Scan
FD2SD2	D Flip-Flop with Reset, Scan, 2X Drive
FD2Q	D Flip-Flop with Reset, Q Output Only
FD2QD2	D Flip-Flop with Reset, Q Output Only, 2X Drive
FD2X2	2-Bit D Flip-Flop with Reset
FD2X4	4-Bit D Flip-Flop with Reset
YFD2	Fast D Flip-Flop with Reset
YFD2D2	Fast D Flip-Flop with Reset, 2X Drive
FD2T	D Flip-Flop with Reset, Tri-State Output
FD2TD2	D Flip-Flop with Reset, Tri-State Output, 2X Drive
FD2TCS	D Flip-Flop with Reset, Scan Clock, Tri-State Output
FD2TCSD2	D Flip-Flop with Reset, Scan Clock, Tri-State Output, 2X Drive
FD2TS	D Flip-Flop with Reset, Scan, Tri-State Output
FD2TSD2	D Flip-Flop with Reset, Scan, Tri-State Output, 2X Drive
FD3	D Flip-Flop with Set
FD3D2	D Flip-Flop with Set, 2X Drive
FD3CS	D Flip-Flop with Set, Scan Clock
FD3CSD2	D Flip-Flop with Set, Scan Clock, 2X Drive

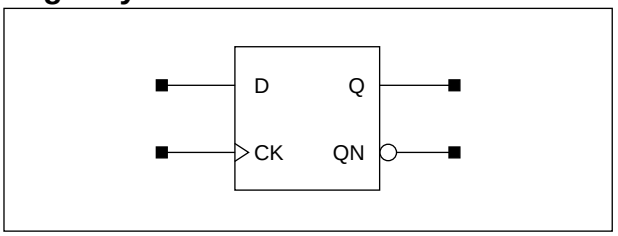
Cell List (Continued)

Cell Name	Function Description
FD3S	D Flip-Flop with Set, Scan
FD3SD2	D Flip-Flop with Set, Scan, 2X Drive
FD3Q	D Flip-Flop with Set, Q Output Only
FD3QD2	D Flip-Flop with Set, Q Output Only, 2X Drive
FD3X2	2-Bit D Flip-Flop with Set
FD3X4	4-Bit D Flip-Flop with Set
YFD3	Fast D Flip-Flop with Set
YFD3D2	Fast D Flip-Flop with Set, 2X Drive
FD4	D Flip-Flop with Reset, Set
FD4D2	D Flip-Flop with Reset, Set, 2X Drive
FD4CS	D Flip-Flop with Reset, Set, Scan Clock
FD4CSD2	D Flip-Flop with Reset, Set, Scan Clock, 2X Drive
FD4S	D Flip-Flop with Reset, Set, Scan
FD4SD2	D Flip-Flop with Reset, Set, Scan, 2X Drive
FD4Q	D Flip-Flop with Reset, Set, Q Output Only
FD4QD2	D Flip-Flop with Reset, Set, Q Output Only, 2X Drive
FD4X2	2-Bit D Flip-Flop with Reset, Set
FD4X4	4-Bit D Flip-Flop with Reset, Set
YFD4	Fast D Flip-Flop with Reset, Set
YFD4D2	Fast D Flip-Flop with Reset, Set, 2X Drive
FD5	D Flip-Flop with Negative Edge Trigger
FD5D2	D Flip-Flop with Negative Edge Trigger, 2X Drive
FD5S	D Flip-Flop with Negative Edge Trigger, Scan
FD5SD2	D Flip-Flop with Negative Edge Trigger, Scan, 2X Drive
FD5X4	4-Bit Flip-Flop with Negative Edge Trigger
FD6	D Flip-Flop with Negative Edge Trigger, Reset
FD6D2	D Flip-Flop with Negative Edge Trigger, Reset, 2X Drive
FD6S	D Flip-Flop with Negative Edge Trigger, Reset, Scan
FD6SD2	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 2X Drive
FD7	D Flip-Flop with Negative Edge Trigger, Set
FD7D2	D Flip-Flop with Negative Edge Trigger, Set, 2X Drive
FD7S	D Flip-Flop with Negative Edge Trigger, Set, Scan
FD7SD2	D Flip-Flop with Negative Edge Trigger, Set, Scan, 2X Drive
FD8	D Flip-Flop with Negative Edge Trigger, Reset, Set

Cell List (Continued)

Cell Name	Function Description
FD8D2	D Flip-Flop with Negative Edge Trigger, Reset, Set, 2X Drive
FD8S	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan
FD8SD2	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 2X Drive
FDS2	D Flip-Flop with Synchronous Clear
FDS2D2	D Flip-Flop with Synchronous Clear, 2X Drive
FDS2CS	D Flip-Flop with Synchronous Clear, Scan Clock
FDS2CSD2	D Flip-Flop with Synchronous Clear, Scan Clock, 2X Drive
FDS2S	D Flip-Flop with Synchronous Clear, Scan
FDS2SD2	D Flip-Flop with Synchronous Clear, Scan, 2X Drive
FDS3	D Flip-Flop with Synchronous Set
FDS3D2	D Flip-Flop with Synchronous Set, 2X Drive
FG1	D Flip-Flop with CK Enable
FG1X4	4-Bit D Flip-Flop with CK Enable
FG2	D Flip-Flop with CK Enable, Reset
FG2X4	4-Bit D Flip-Flop with CK Enable, Reset
FJ1	JK Flip-Flop
FJ1D2	JK Flip-Flop with 2X Drive
FJ1S	JK Flip-Flop with Scan
FJ1SD2	JK Flip-Flop with Scan, 2X Drive
FJ2	JK Flip-Flop with Reset
FJ2D2	JK Flip-Flop with Reset, 2X Drive
FJ2S	JK Flip-Flop with Reset, Scan
FJ2SD2	JK Flip-Flop with Reset, Scan, 2X Drive
FJ4	JK Flip-Flop with Reset, Set
FJ4D2	JK Flip-Flop with Reset, Set, 2X Drive
FJ4S	JK Flip-Flop with Reset, Set, Scan
FJ4SD2	JK Flip-Flop with Reset, Set, Scan, 2X Drive
FT2	Toggle Flip-Flop with Reset
FT2D2	Toggle Flip-Flop with Reset, 2X Drive
FT3	Toggle Flip-Flop with Set
FT3D2	Toggle Flip-Flop with Set, 2X Drive

Logic Symbol



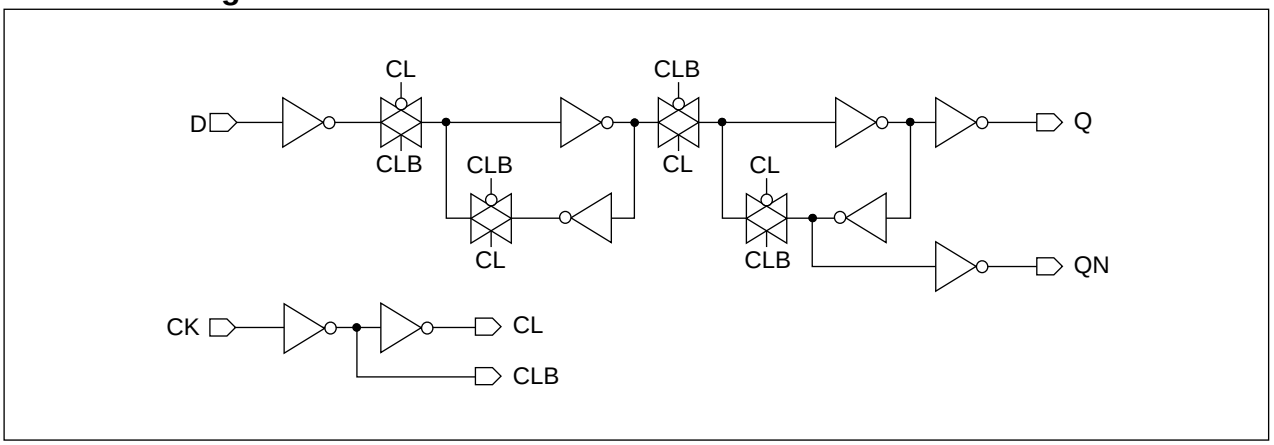
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
FD1		*FD1D2*		*FD1*	*FD1D2*
D	CK	D	CK		
0.9	0.9	0.9	0.9	7.0	8.0
KGM80					
FD1		*FD1D2*		*FD1*	*FD1D2*
D	CK	D	CK		
1.0	1.0	1.0	1.0	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD1	FD1D2	FD1	FD1D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.37	0.37	0.64	0.64
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40, SL: Standard Load)

KG80 FD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.53	0.47 + 0.030*SL	0.49 + 0.026*SL	0.50 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CK to QN	t_{PLH}	0.67	0.59 + 0.040*SL	0.59 + 0.041*SL	0.58 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.030*SL	0.54 + 0.025*SL	0.55 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.07 + 0.042*SL

KG80 FD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.49	0.44 + 0.023*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.53	0.49 + 0.021*SL	0.50 + 0.015*SL	0.52 + 0.013*SL
	t_R	0.17	0.09 + 0.039*SL	0.08 + 0.044*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
CK to QN	t_{PLH}	0.70	0.66 + 0.019*SL	0.66 + 0.019*SL	0.65 + 0.020*SL
	t_{PHL}	0.62	0.58 + 0.019*SL	0.59 + 0.015*SL	0.61 + 0.013*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40, SL: Standard Load)

KGM80 FD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.60 + 0.051*SL	0.61 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.75	0.68 + 0.034*SL	0.70 + 0.026*SL	0.73 + 0.024*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CK to QN	t_{PLH}	0.94	0.85 + 0.049*SL	0.84 + 0.050*SL	0.84 + 0.050*SL
	t_{PHL}	0.83	0.76 + 0.033*SL	0.78 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

KGM80 FD1D2

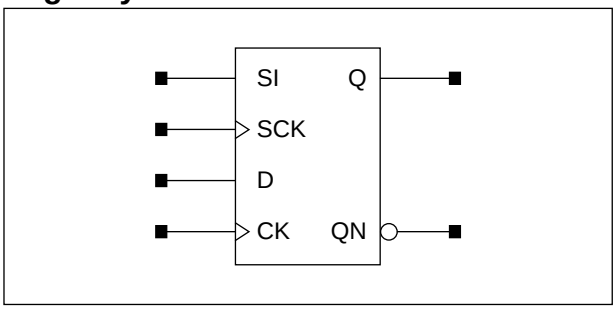
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.62 + 0.028*SL	0.63 + 0.025*SL	0.63 + 0.025*SL
	t_{PHL}	0.75	0.70 + 0.023*SL	0.72 + 0.017*SL	0.76 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.021*SL
CK to QN	t_{PLH}	0.99	0.94 + 0.025*SL	0.94 + 0.024*SL	0.93 + 0.025*SL
	t_{PHL}	0.88	0.84 + 0.022*SL	0.85 + 0.016*SL	0.88 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FD1CS/FD1CSD2

D Flip-Flop with Scan Clock, 1X/2X Drive

Logic Symbol



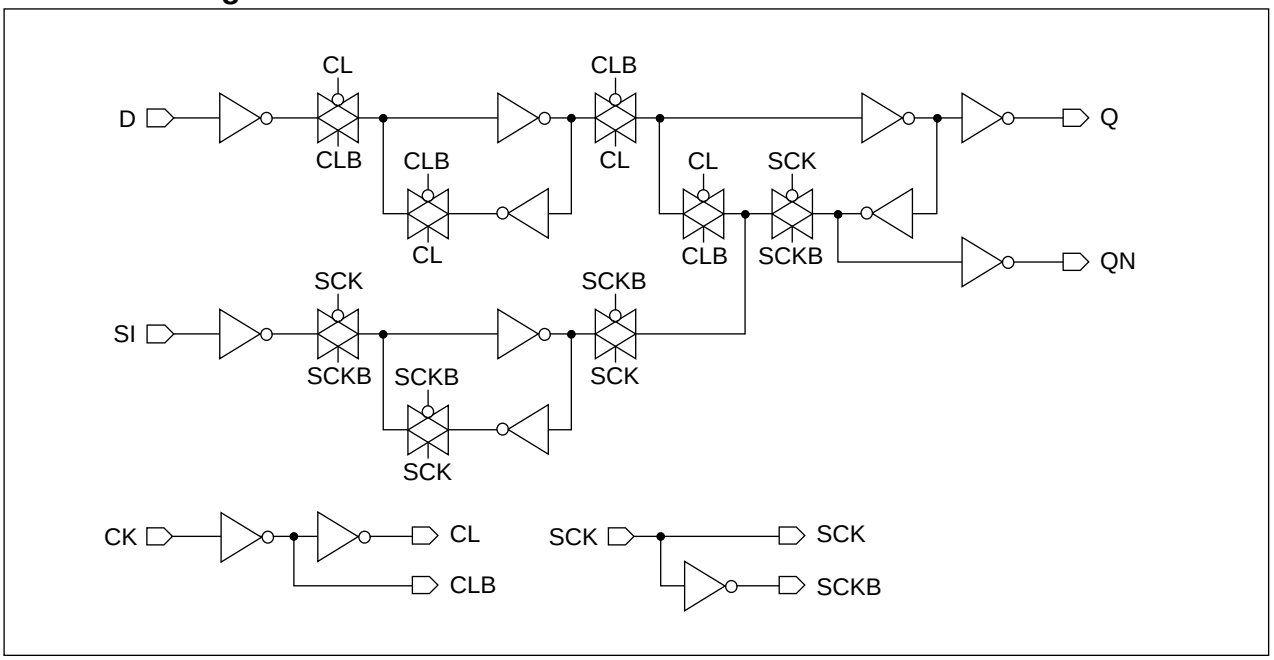
Truth Table

SI	SCK	D	CK	Q (n+1)	QN (n+1)
x	0	0	⎍	0	1
x	0	1	⎍	1	0
0	⎍	x	0	0	1
1	⎍	x	0	1	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
FD1CS				*FD1CSD2*				*FD1CS*	*FD1CSD2*
SI	SCK	D	CK	SI	SCK	D	CK		
0.9	2.1	0.9	0.9	0.9	2.1	0.9	0.9	11.0	12.0
KGM80									
FD1CS				*FD1CSD2*				*FD1CS*	*FD1CSD2*
SI	SCK	D	CK	SI	SCK	D	CK		
1.0	2.1	1.0	1.0	1.0	2.1	1.0	1.0	11.0	12.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD1CS	FD1CSD2	FD1CS	FD1CSD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SCK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (SCK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.15	0.15	0.64	0.64
Input Hold Time (D to CK)	t_{HD}	0.37	0.37	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.15	0.15	0.96	0.96
Input Hold Time (SI to SCK)	t_{HD}	0.56	0.56	0.33	0.33

FD1CS/FD1CSD2

D Flip-Flop with Scan Clock, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD1CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.52	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.54	0.48 + 0.030*SL	0.49 + 0.025*SL	0.50 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SCK to Q	t_{PLH}	0.55	0.46 + 0.042*SL	0.47 + 0.041*SL	0.47 + 0.042*SL
	t_{PHL}	0.47	0.41 + 0.031*SL	0.42 + 0.026*SL	0.44 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
CK to QN	t_{PLH}	0.74	0.65 + 0.042*SL	0.66 + 0.041*SL	0.65 + 0.041*SL
	t_{PHL}	0.67	0.60 + 0.035*SL	0.62 + 0.028*SL	0.64 + 0.025*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.21	0.12 + 0.042*SL	0.13 + 0.040*SL	0.12 + 0.041*SL
SCK to QN	t_{PLH}	0.61	0.53 + 0.040*SL	0.53 + 0.041*SL	0.52 + 0.042*SL
	t_{PHL}	0.62	0.56 + 0.029*SL	0.57 + 0.025*SL	0.58 + 0.023*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 FD1CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.51	0.46 + 0.022*SL	0.47 + 0.021*SL	0.47 + 0.021*SL
	t_{PHL}	0.54	0.51 + 0.019*SL	0.51 + 0.015*SL	0.53 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.045*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
SCK to Q	t_{PLH}	0.55	0.51 + 0.023*SL	0.51 + 0.021*SL	0.51 + 0.020*SL
	t_{PHL}	0.48	0.45 + 0.019*SL	0.46 + 0.015*SL	0.47 + 0.013*SL
	t_R	0.20	0.12 + 0.040*SL	0.11 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.16	0.11 + 0.021*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
CK to QN	t_{PLH}	0.78	0.73 + 0.021*SL	0.74 + 0.020*SL	0.74 + 0.020*SL
	t_{PHL}	0.71	0.67 + 0.021*SL	0.68 + 0.017*SL	0.70 + 0.014*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.042*SL	0.11 + 0.043*SL
	t_F	0.18	0.14 + 0.024*SL	0.14 + 0.020*SL	0.15 + 0.020*SL
SCK to QN	t_{PLH}	0.65	0.61 + 0.019*SL	0.61 + 0.019*SL	0.60 + 0.020*SL
	t_{PHL}	0.68	0.64 + 0.017*SL	0.65 + 0.014*SL	0.66 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD1CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.72	0.61 + 0.051*SL	0.62 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.75	0.68 + 0.034*SL	0.70 + 0.026*SL	0.73 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SCK to Q	t_{PLH}	0.81	0.70 + 0.052*SL	0.71 + 0.050*SL	0.71 + 0.050*SL
	t_{PHL}	0.66	0.59 + 0.035*SL	0.61 + 0.026*SL	0.65 + 0.023*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CK to QN	t_{PLH}	1.03	0.92 + 0.053*SL	0.93 + 0.050*SL	0.93 + 0.050*SL
	t_{PHL}	0.95	0.88 + 0.040*SL	0.90 + 0.029*SL	0.95 + 0.025*SL
	t_R	0.38	0.17 + 0.102*SL	0.16 + 0.106*SL	0.14 + 0.108*SL
	t_F	0.25	0.15 + 0.047*SL	0.16 + 0.043*SL	0.17 + 0.042*SL
SCK to QN	t_{PLH}	0.85	0.76 + 0.049*SL	0.75 + 0.050*SL	0.75 + 0.050*SL
	t_{PHL}	0.92	0.86 + 0.032*SL	0.88 + 0.025*SL	0.90 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.043*SL

KGM80 FD1CSD2

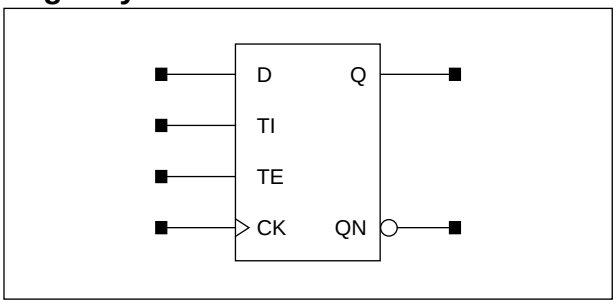
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.65 + 0.027*SL	0.66 + 0.025*SL	0.66 + 0.025*SL
	t_{PHL}	0.77	0.73 + 0.021*SL	0.74 + 0.016*SL	0.77 + 0.013*SL
	t_R	0.25	0.15 + 0.051*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
SCK to Q	t_{PLH}	0.82	0.76 + 0.028*SL	0.77 + 0.025*SL	0.77 + 0.025*SL
	t_{PHL}	0.69	0.64 + 0.022*SL	0.66 + 0.016*SL	0.69 + 0.013*SL
	t_R	0.27	0.17 + 0.050*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.14 + 0.023*SL	0.15 + 0.021*SL	0.16 + 0.020*SL
CK to QN	t_{PLH}	1.09	1.03 + 0.028*SL	1.04 + 0.025*SL	1.04 + 0.025*SL
	t_{PHL}	1.02	0.97 + 0.025*SL	0.99 + 0.018*SL	1.02 + 0.015*SL
	t_R	0.28	0.17 + 0.052*SL	0.18 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.22	0.17 + 0.027*SL	0.18 + 0.022*SL	0.20 + 0.021*SL
SCK to QN	t_{PLH}	0.92	0.87 + 0.023*SL	0.87 + 0.024*SL	0.86 + 0.025*SL
	t_{PHL}	1.01	0.97 + 0.019*SL	0.98 + 0.015*SL	1.01 + 0.013*SL
	t_R	0.25	0.15 + 0.051*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FD1S/FD1SD2

D Flip-Flop with Scan, 1X/2X Drive

Logic Symbol



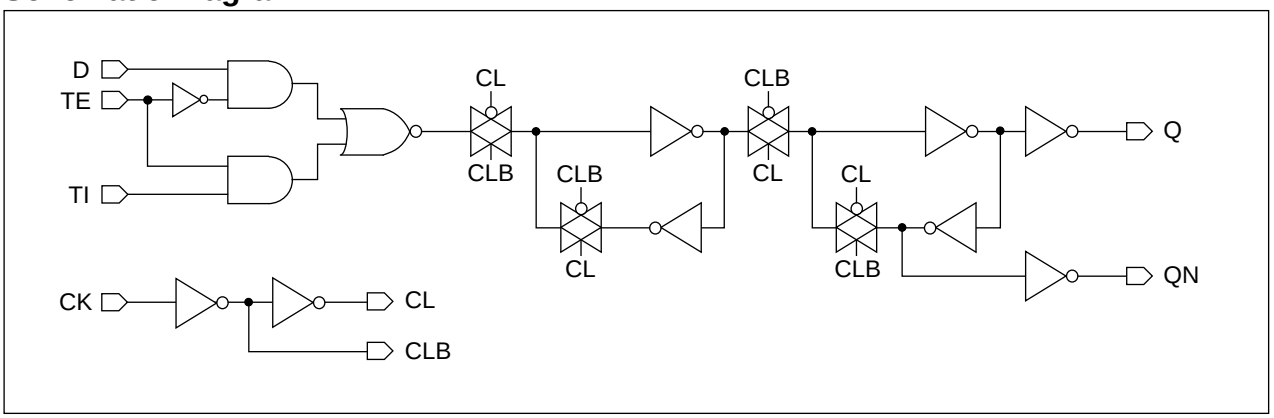
Truth Table

D	TI	TE	CK	Q (n+1)	QN (n+1)
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
FD1S				*FD1SD2*				*FD1S*	*FD1SD2*
D	TI	TE	CK	D	TI	TE	CK		
0.6	0.8	1.6	0.9	0.6	0.8	1.6	0.9	9.0	10.0
KGM80									
FD1S				*FD1SD2*				*FD1S*	*FD1SD2*
D	TI	TE	CK	D	TI	TE	CK		
1.0	1.0	2.0	1.1	1.0	1.0	2.0	1.1	9.0	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD1S	FD1SD2	FD1S	FD1SD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.47	0.47	0.86	0.86
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.50	0.53	0.96	0.96
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.56	0.56	0.96	0.99
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.53	0.47 + 0.030*SL	0.48 + 0.026*SL	0.50 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CK to QN	t_{PLH}	0.67	0.59 + 0.040*SL	0.58 + 0.041*SL	0.58 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.030*SL	0.54 + 0.025*SL	0.55 + 0.023*SL
	t_R	0.26	0.09 + 0.085*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 FD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.49	0.44 + 0.022*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.53	0.49 + 0.021*SL	0.50 + 0.015*SL	0.51 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
CK to QN	t_{PLH}	0.69	0.66 + 0.019*SL	0.66 + 0.019*SL	0.65 + 0.020*SL
	t_{PHL}	0.62	0.58 + 0.018*SL	0.59 + 0.015*SL	0.61 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD1S/FD1SD2

D Flip-Flop with Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD1S

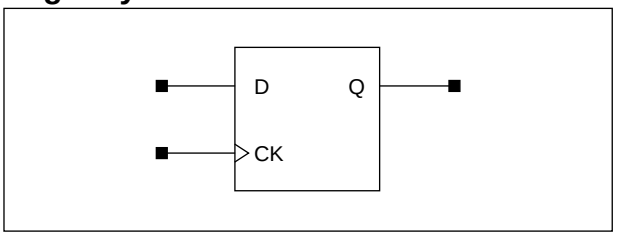
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.60 + 0.051*SL	0.60 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.74	0.67 + 0.034*SL	0.70 + 0.026*SL	0.73 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CK to QN	t_{PLH}	0.94	0.84 + 0.049*SL	0.84 + 0.050*SL	0.84 + 0.050*SL
	t_{PHL}	0.82	0.76 + 0.033*SL	0.78 + 0.026*SL	0.80 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.044*SL	0.11 + 0.041*SL	0.10 + 0.042*SL

KGM80 FD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.67	0.62 + 0.028*SL	0.62 + 0.025*SL	0.63 + 0.025*SL
	t_{PHL}	0.75	0.70 + 0.023*SL	0.72 + 0.016*SL	0.75 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.021*SL
CK to QN	t_{PLH}	0.98	0.93 + 0.024*SL	0.93 + 0.024*SL	0.93 + 0.025*SL
	t_{PHL}	0.88	0.83 + 0.022*SL	0.85 + 0.016*SL	0.88 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



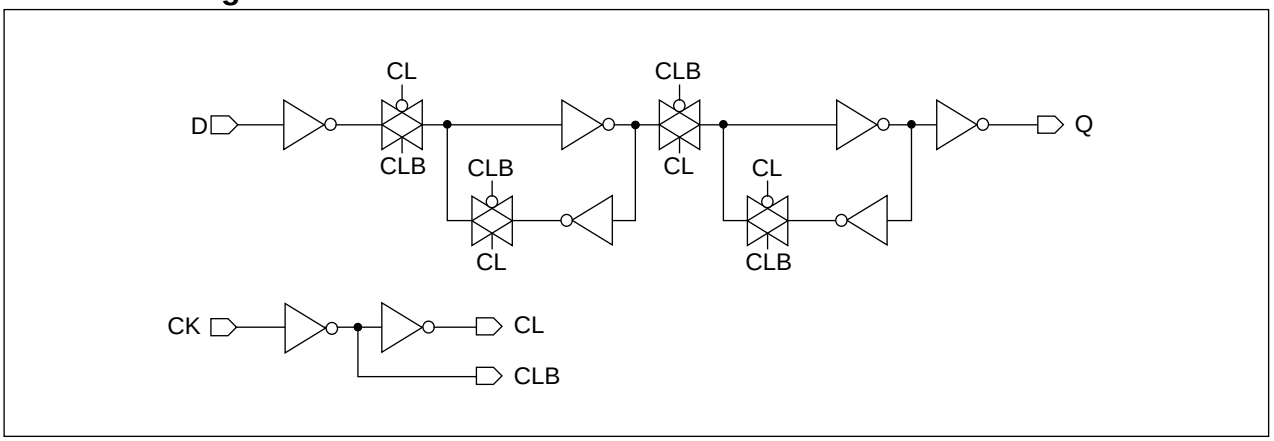
Truth Table

D	CK	Q (n+1)
0	↑	0
1	↑	1
x	↓	Q (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
FD1Q		*FD1QD2*		*FD1Q*	*FD1QD2*
D	CK	D	CK		
0.8	0.8	0.8	0.8	8.0	9.0
KGM80					
FD1Q		*FD1QD2*		*FD1Q*	*FD1QD2*
D	CK	D	CK		
0.9	0.9	0.9	0.9	8.0	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD1Q	FD1QD2	FD1Q	FD1QD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.39	0.39	0.71	0.71
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33

FD1Q/FD1QD2

D Flip-Flop with Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.49	0.41 + 0.043*SL	0.41 + 0.042*SL	0.41 + 0.042*SL
	t_{PHL}	0.50	0.44 + 0.031*SL	0.45 + 0.025*SL	0.46 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.041*SL

KG80 FD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.48	0.44 + 0.022*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.50	0.46 + 0.019*SL	0.47 + 0.015*SL	0.49 + 0.013*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD1Q

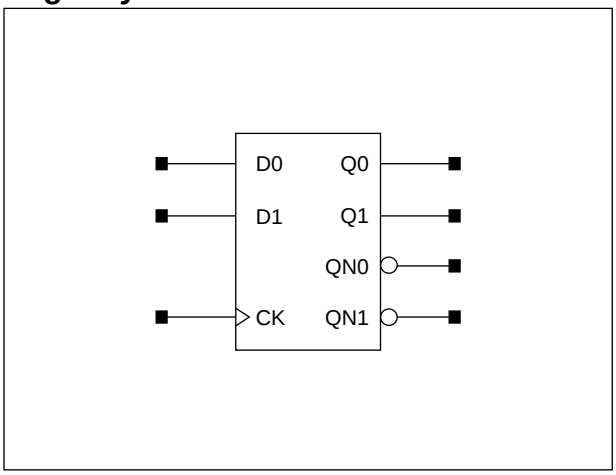
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.60 + 0.052*SL	0.60 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.70	0.63 + 0.034*SL	0.65 + 0.026*SL	0.68 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.044*SL	0.11 + 0.041*SL	0.10 + 0.042*SL

KGM80 FD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.63 + 0.027*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.71	0.67 + 0.021*SL	0.69 + 0.016*SL	0.72 + 0.013*SL
	t_R	0.24	0.14 + 0.051*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

Dn	CK	Qn (n+1)	QNn (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
KG80		
Dn	CK	
1.0	0.9	12.0
KGM80		
Dn	CK	
1.0	1.1	12.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.61	1.02
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Input Setup Time (D0 to CK)	t_{SU}	0.15	0.58
Input Hold Time (D0 to CK)	t_{HD}	0.28	0.33
Input Setup Time (D1 to CK)	t_{SU}	0.31	0.58
Input Hold Time (D1 to CK)	t_{HD}	0.15	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD1X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.57	0.48 + 0.042*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.64	0.57 + 0.031*SL	0.59 + 0.026*SL	0.60 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
CK to Q1	t_{PLH}	0.57	0.48 + 0.042*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.64	0.57 + 0.031*SL	0.59 + 0.026*SL	0.60 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
CK to QN0	t_{PLH}	0.77	0.69 + 0.040*SL	0.69 + 0.041*SL	0.68 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.030*SL	0.59 + 0.025*SL	0.61 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CK to QN1	t_{PLH}	0.77	0.69 + 0.040*SL	0.69 + 0.041*SL	0.68 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.030*SL	0.59 + 0.025*SL	0.61 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD1X2

2-Bit D Flip-Flop

Switching Characteristics

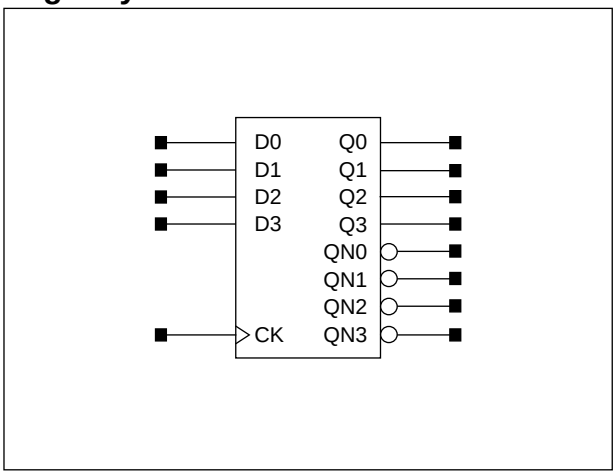
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD1X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.77	0.67 + 0.051*SL	0.67 + 0.050*SL	0.68 + 0.050*SL
	t_{PHL}	0.89	0.82 + 0.034*SL	0.84 + 0.026*SL	0.87 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
CK to Q1	t_{PLH}	0.77	0.67 + 0.051*SL	0.67 + 0.050*SL	0.68 + 0.050*SL
	t_{PHL}	0.89	0.82 + 0.034*SL	0.84 + 0.026*SL	0.87 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
CK to QN0	t_{PLH}	1.08	0.98 + 0.049*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.89	0.83 + 0.033*SL	0.85 + 0.026*SL	0.87 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
CK to QN1	t_{PLH}	1.08	0.98 + 0.049*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.89	0.82 + 0.033*SL	0.84 + 0.026*SL	0.87 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

Dn	CK	Qn (n+1)	QNn (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
KG80		
Dn	CK	
1.0	0.9	24.0
KGM80		
Dn	CK	
1.0	1.1	24.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.80	1.27
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Input Setup Time (D0 to CK)	t_{SU}	0.17	0.46
Input Hold Time (D0 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D1 to CK)	t_{SU}	0.17	0.46
Input Hold Time (D1 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D2 to CK)	t_{SU}	0.17	0.46
Input Hold Time (D2 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D3 to CK)	t_{SU}	0.17	0.46
Input Hold Time (D3 to CK)	t_{HD}	0.26	0.43

FD1X4

4-Bit D Flip-Flop

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.67	0.59 + 0.042*SL	0.59 + 0.042*SL	0.59 + 0.042*SL
	t_{PHL}	0.83	0.77 + 0.031*SL	0.78 + 0.026*SL	0.80 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.10 + 0.040*SL	0.08 + 0.041*SL
CK to Q1	t_{PLH}	0.68	0.59 + 0.042*SL	0.59 + 0.042*SL	0.59 + 0.042*SL
	t_{PHL}	0.84	0.77 + 0.031*SL	0.79 + 0.026*SL	0.80 + 0.024*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
CK to Q2	t_{PLH}	0.68	0.59 + 0.042*SL	0.59 + 0.042*SL	0.59 + 0.042*SL
	t_{PHL}	0.84	0.77 + 0.031*SL	0.79 + 0.026*SL	0.80 + 0.024*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
CK to Q3	t_{PLH}	0.67	0.59 + 0.042*SL	0.59 + 0.042*SL	0.59 + 0.042*SL
	t_{PHL}	0.83	0.77 + 0.031*SL	0.78 + 0.026*SL	0.80 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.10 + 0.040*SL	0.08 + 0.041*SL
CK to QN0	t_{PLH}	0.96	0.88 + 0.040*SL	0.88 + 0.041*SL	0.88 + 0.042*SL
	t_{PHL}	0.74	0.68 + 0.030*SL	0.69 + 0.025*SL	0.71 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CK to QN1	t_{PLH}	0.97	0.89 + 0.040*SL	0.89 + 0.041*SL	0.88 + 0.042*SL
	t_{PHL}	0.75	0.69 + 0.029*SL	0.70 + 0.025*SL	0.71 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CK to QN2	t_{PLH}	0.97	0.89 + 0.040*SL	0.89 + 0.041*SL	0.88 + 0.042*SL
	t_{PHL}	0.75	0.69 + 0.030*SL	0.70 + 0.025*SL	0.71 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
CK to QN3	t_{PLH}	0.96	0.88 + 0.040*SL	0.88 + 0.041*SL	0.88 + 0.042*SL
	t_{PHL}	0.74	0.68 + 0.030*SL	0.69 + 0.025*SL	0.71 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD1X4

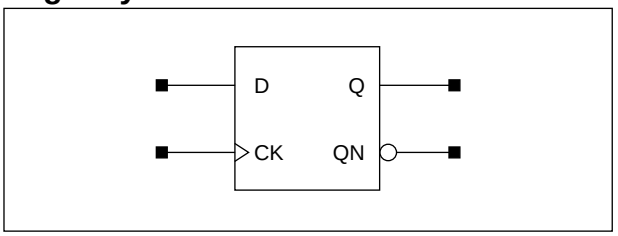
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.89	0.79 + 0.051*SL	0.79 + 0.050*SL	0.80 + 0.050*SL
	t_{PHL}	1.16	1.09 + 0.034*SL	1.11 + 0.026*SL	1.14 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CK to Q1	t_{PLH}	0.90	0.80 + 0.050*SL	0.80 + 0.050*SL	0.81 + 0.050*SL
	t_{PHL}	1.17	1.10 + 0.034*SL	1.12 + 0.026*SL	1.15 + 0.023*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CK to Q2	t_{PLH}	0.90	0.80 + 0.051*SL	0.80 + 0.050*SL	0.81 + 0.050*SL
	t_{PHL}	1.17	1.10 + 0.034*SL	1.12 + 0.026*SL	1.15 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CK to Q3	t_{PLH}	0.89	0.79 + 0.051*SL	0.79 + 0.050*SL	0.80 + 0.050*SL
	t_{PHL}	1.16	1.09 + 0.034*SL	1.11 + 0.026*SL	1.14 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CK to QN0	t_{PLH}	1.35	1.25 + 0.049*SL	1.25 + 0.050*SL	1.25 + 0.050*SL
	t_{PHL}	1.01	0.95 + 0.033*SL	0.97 + 0.026*SL	0.99 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
CK to QN1	t_{PLH}	1.36	1.26 + 0.050*SL	1.26 + 0.050*SL	1.26 + 0.050*SL
	t_{PHL}	1.02	0.96 + 0.032*SL	0.98 + 0.026*SL	1.00 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
CK to QN2	t_{PLH}	1.36	1.26 + 0.049*SL	1.26 + 0.050*SL	1.26 + 0.050*SL
	t_{PHL}	1.02	0.96 + 0.032*SL	0.98 + 0.026*SL	1.00 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
CK to QN3	t_{PLH}	1.35	1.25 + 0.049*SL	1.25 + 0.050*SL	1.25 + 0.050*SL
	t_{PHL}	1.01	0.95 + 0.033*SL	0.97 + 0.026*SL	0.99 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

YFD1/YFD1D2

Fast D Flip-Flop with 1X/2X Drive

Logic Symbol



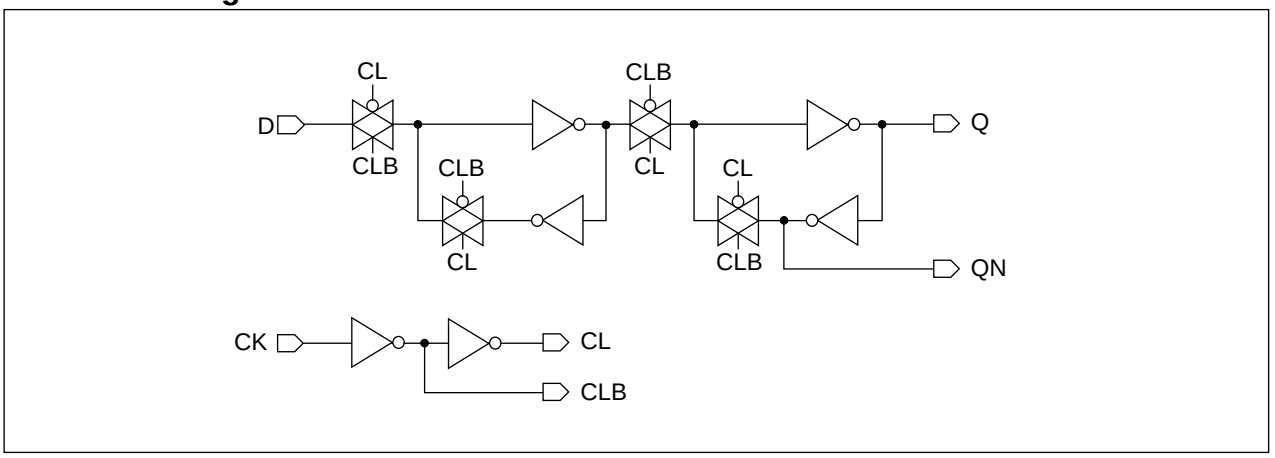
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
YFD1		*YFD1D2*		*YFD1*	*YFD1D2*
D	CK	D	CK		
2.9	0.8	2.9	0.8	5.0	6.0
KGM80					
YFD1		*YFD1D2*		*YFD1*	*YFD1D2*
D	CK	D	CK		
3.7	0.9	3.7	0.9	5.0	6.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		YFD1	YFD1D2	YFD1	YFD1D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.26	0.26	0.52	0.49
Input Hold Time (D to CK)	t_{HD}	0.26	0.26	0.46	0.46

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40, SL: Standard Load)

KG80 YFD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.45	0.37 + 0.043*SL	0.37 + 0.042*SL	0.37 + 0.042*SL
	t_{PHL}	0.38	0.32 + 0.033*SL	0.33 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.35	0.18 + 0.086*SL	0.18 + 0.088*SL	0.16 + 0.090*SL
	t_F	0.22	0.13 + 0.043*SL	0.13 + 0.042*SL	0.14 + 0.042*SL
CK to QN	t_{PLH}	0.57	0.40 + 0.086*SL	0.42 + 0.080*SL	0.44 + 0.077*SL
	t_{PHL}	0.58	0.42 + 0.078*SL	0.42 + 0.077*SL	0.42 + 0.077*SL
	t_R	0.32	0.13 + 0.094*SL	0.13 + 0.094*SL	0.13 + 0.094*SL
	t_F	0.21	0.09 + 0.061*SL	0.08 + 0.063*SL	0.08 + 0.063*SL

KG80 YFD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.44	0.40 + 0.023*SL	0.40 + 0.021*SL	0.40 + 0.021*SL
	t_{PHL}	0.38	0.34 + 0.019*SL	0.35 + 0.016*SL	0.37 + 0.014*SL
	t_R	0.28	0.19 + 0.042*SL	0.19 + 0.044*SL	0.18 + 0.045*SL
	t_F	0.20	0.15 + 0.023*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
CK to QN	t_{PLH}	0.51	0.42 + 0.047*SL	0.43 + 0.043*SL	0.44 + 0.041*SL
	t_{PHL}	0.52	0.44 + 0.040*SL	0.44 + 0.039*SL	0.45 + 0.038*SL
	t_R	0.21	0.11 + 0.048*SL	0.11 + 0.047*SL	0.11 + 0.048*SL
	t_F	0.14	0.08 + 0.031*SL	0.08 + 0.031*SL	0.07 + 0.031*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40, SL: Standard Load)

KGM80 YFD1

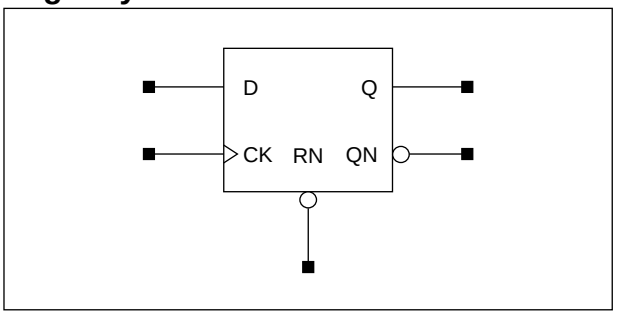
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.53 + 0.052*SL	0.53 + 0.050*SL	0.54 + 0.050*SL
	t_{PHL}	0.55	0.47 + 0.037*SL	0.49 + 0.029*SL	0.54 + 0.025*SL
	t_R	0.47	0.26 + 0.103*SL	0.25 + 0.107*SL	0.23 + 0.109*SL
	t_F	0.27	0.18 + 0.048*SL	0.19 + 0.044*SL	0.21 + 0.042*SL
CK to QN	t_{PLH}	0.80	0.60 + 0.101*SL	0.63 + 0.091*SL	0.67 + 0.087*SL
	t_{PHL}	0.80	0.61 + 0.094*SL	0.62 + 0.092*SL	0.62 + 0.092*SL
	t_R	0.43	0.20 + 0.112*SL	0.20 + 0.112*SL	0.20 + 0.112*SL
	t_F	0.25	0.11 + 0.067*SL	0.11 + 0.068*SL	0.11 + 0.068*SL

KGM80 YFD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.62	0.56 + 0.028*SL	0.57 + 0.026*SL	0.58 + 0.025*SL
	t_{PHL}	0.56	0.52 + 0.023*SL	0.53 + 0.018*SL	0.57 + 0.015*SL
	t_R	0.37	0.27 + 0.052*SL	0.27 + 0.052*SL	0.25 + 0.053*SL
	t_F	0.26	0.21 + 0.025*SL	0.22 + 0.023*SL	0.24 + 0.021*SL
CK to QN	t_{PLH}	0.74	0.63 + 0.055*SL	0.64 + 0.050*SL	0.69 + 0.046*SL
	t_{PHL}	0.73	0.63 + 0.048*SL	0.64 + 0.046*SL	0.64 + 0.046*SL
	t_R	0.27	0.16 + 0.055*SL	0.16 + 0.056*SL	0.16 + 0.056*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.033*SL	0.09 + 0.033*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Logic Symbol



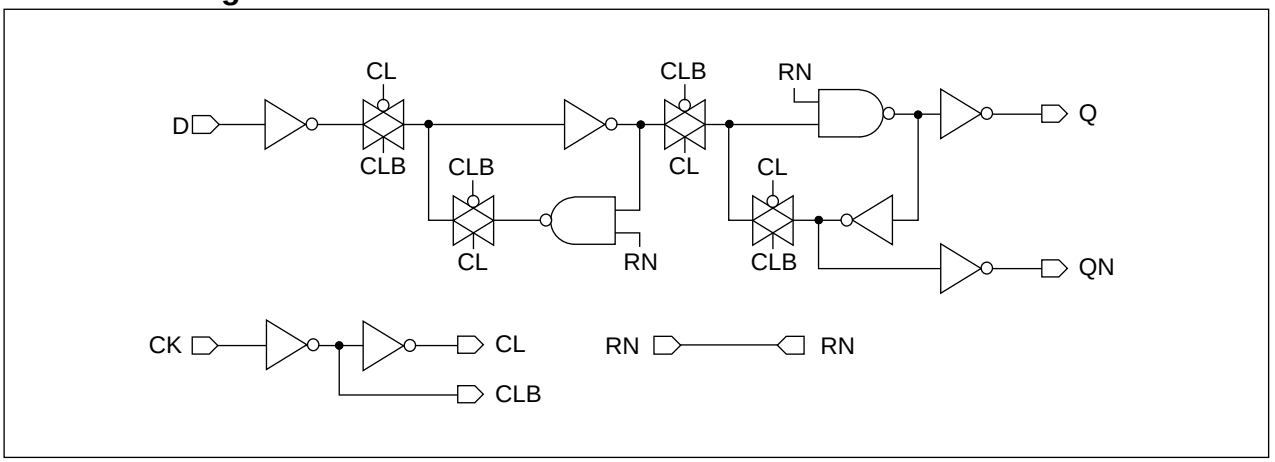
Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FD2			*FD2D2*			*FD2*	*FD2D2*
D	CK	RN	D	CK	RN		
0.9	0.9	1.7	0.9	0.9	1.6	8.0	9.0
KGM80							
FD2			*FD2D2*			*FD2*	*FD2D2*
D	CK	RN	D	CK	RN		
1.1	1.0	2.0	1.1	1.0	2.0	8.0	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD2	FD2D2	FD2	FD2D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.37	0.37	0.68	0.68
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.37	0.37	0.63	0.63

FD2/FD2D2

D Flip-Flop with Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.49 + 0.045*SL	0.50 + 0.042*SL	0.50 + 0.042*SL
	t_{PHL}	0.55	0.48 + 0.032*SL	0.50 + 0.026*SL	0.52 + 0.024*SL
	t_R	0.29	0.12 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.043*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q	t_{PHL}	0.35	0.28 + 0.033*SL	0.29 + 0.027*SL	0.31 + 0.024*SL
	t_F	0.20	0.11 + 0.041*SL	0.12 + 0.039*SL	0.11 + 0.040*SL
CK to QN	t_{PLH}	0.69	0.61 + 0.040*SL	0.61 + 0.041*SL	0.60 + 0.042*SL
	t_{PHL}	0.66	0.60 + 0.030*SL	0.61 + 0.025*SL	0.62 + 0.023*SL
	t_R	0.26	0.09 + 0.085*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN	t_{PLH}	0.49	0.41 + 0.040*SL	0.41 + 0.041*SL	0.40 + 0.042*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL

KG80 FD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.56	0.51 + 0.025*SL	0.52 + 0.022*SL	0.53 + 0.021*SL
	t_{PHL}	0.54	0.50 + 0.021*SL	0.51 + 0.016*SL	0.53 + 0.014*SL
	t_R	0.19	0.11 + 0.043*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PHL}	0.33	0.29 + 0.022*SL	0.30 + 0.017*SL	0.33 + 0.014*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
CK to QN	t_{PLH}	0.72	0.68 + 0.020*SL	0.68 + 0.019*SL	0.67 + 0.020*SL
	t_{PHL}	0.71	0.67 + 0.018*SL	0.68 + 0.015*SL	0.69 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
RN to QN	t_{PLH}	0.51	0.48 + 0.020*SL	0.48 + 0.019*SL	0.47 + 0.020*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.80	0.70 + 0.054*SL	0.71 + 0.051*SL	0.72 + 0.050*SL
	t_{PHL}	0.77	0.70 + 0.036*SL	0.73 + 0.027*SL	0.76 + 0.024*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.22	0.13 + 0.045*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
RN to Q	t_{PHL}	0.45	0.38 + 0.037*SL	0.40 + 0.028*SL	0.44 + 0.024*SL
	t_F	0.23	0.14 + 0.044*SL	0.15 + 0.041*SL	0.14 + 0.041*SL
CK to QN	t_{PLH}	0.98	0.88 + 0.049*SL	0.88 + 0.050*SL	0.87 + 0.050*SL
	t_{PHL}	0.93	0.87 + 0.033*SL	0.89 + 0.026*SL	0.92 + 0.023*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.66	0.56 + 0.049*SL	0.56 + 0.050*SL	0.55 + 0.050*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL

KGM80 FD2D2

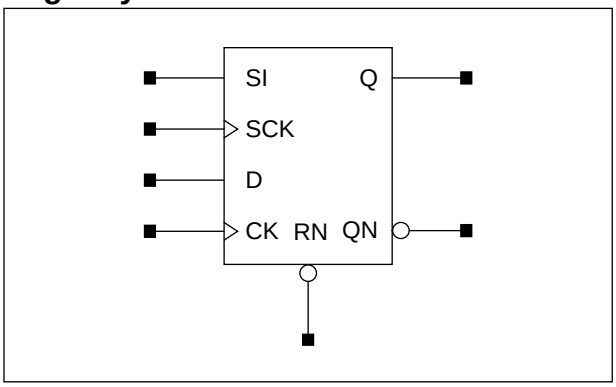
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.78	0.72 + 0.031*SL	0.73 + 0.027*SL	0.75 + 0.025*SL
	t_{PHL}	0.77	0.72 + 0.024*SL	0.74 + 0.017*SL	0.78 + 0.014*SL
	t_R	0.25	0.14 + 0.053*SL	0.14 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.17	0.12 + 0.026*SL	0.13 + 0.022*SL	0.15 + 0.021*SL
RN to Q	t_{PHL}	0.45	0.39 + 0.026*SL	0.42 + 0.018*SL	0.46 + 0.014*SL
	t_F	0.19	0.13 + 0.027*SL	0.15 + 0.022*SL	0.17 + 0.020*SL
CK to QN	t_{PLH}	1.02	0.97 + 0.025*SL	0.97 + 0.024*SL	0.96 + 0.025*SL
	t_{PHL}	1.01	0.96 + 0.021*SL	0.98 + 0.016*SL	1.01 + 0.013*SL
	t_R	0.22	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
RN to QN	t_{PLH}	0.70	0.65 + 0.025*SL	0.65 + 0.024*SL	0.64 + 0.025*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.052*SL	0.10 + 0.054*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FD2CS/FD2CSD2

D Flip-Flop with Reset, Scan Clock, 1X/2X Drive

Logic Symbol



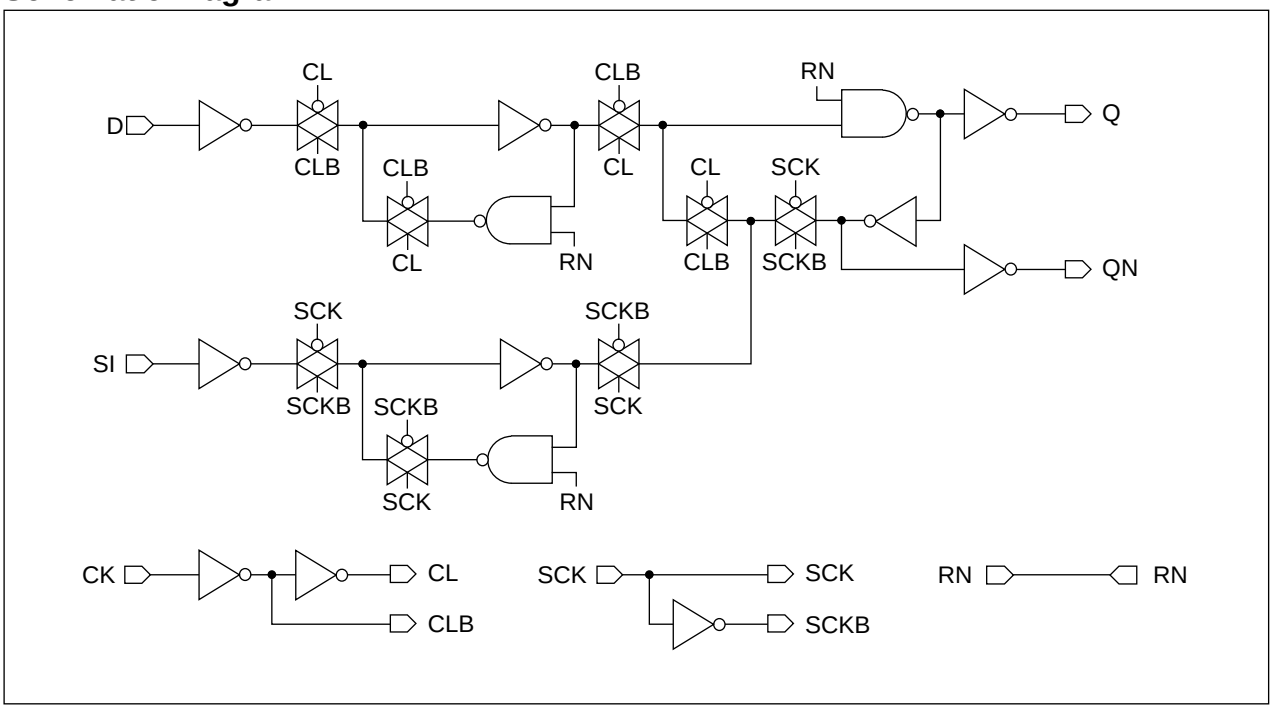
Truth Table

SI	SCK	D	CK	RN	Q (n+1)	QN (n+1)
x	0	0	↑	1	0	1
x	0	1	↑	1	1	0
0	↑	x	0	1	0	1
1	↑	x	0	1	1	0
x	x	x	x	0	0	1

Cell Data

Input Load (SL)										Gate Count	
KG80											
FD2CS					*FD2CSD2*					*FD2CS*	*FD2CSD2*
SI	SCK	D	CK	RN	SI	SCK	D	CK	RN		
0.9	2.1	0.9	0.9	2.7	0.9	2.1	0.9	0.9	2.7	12.0	13.0
KGM80											
FD2CS					*FD2CSD2*					*FD2CS*	*FD2CSD2*
SI	SCK	D	CK	RN	SI	SCK	D	CK	RN		
1.0	2.9	1.1	1.0	3.2	1.0	2.9	1.1	1.0	3.2	12.0	13.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD2CS	FD2CSD2	FD2CS	FD2CSD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SCK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (SCK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.37	0.37	0.68	0.68
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.56	0.56	0.96	0.96
Input Hold Time (SI to SCK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.37	0.37	0.63	0.63
Recovery Time (RN to SCK)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to SCK)	t_{HD}	0.26	0.26	0.63	0.63

FD2CS/FD2CSD2

D Flip-Flop with Reset, Scan Clock, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.56	0.47 + 0.044*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.53	0.47 + 0.031*SL	0.49 + 0.026*SL	0.50 + 0.024*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.089*SL	0.10 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SCK to Q	t_{PLH}	0.62	0.53 + 0.044*SL	0.54 + 0.042*SL	0.54 + 0.042*SL
	t_{PHL}	0.47	0.41 + 0.031*SL	0.43 + 0.026*SL	0.44 + 0.024*SL
	t_R	0.30	0.13 + 0.085*SL	0.12 + 0.088*SL	0.11 + 0.089*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
RN to Q	t_{PHL}	0.33	0.27 + 0.032*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to QN	t_{PLH}	0.74	0.66 + 0.042*SL	0.66 + 0.041*SL	0.66 + 0.041*SL
	t_{PHL}	0.73	0.66 + 0.036*SL	0.68 + 0.028*SL	0.70 + 0.025*SL
	t_R	0.29	0.12 + 0.083*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.21	0.13 + 0.043*SL	0.14 + 0.040*SL	0.13 + 0.041*SL
SCK to QN	t_{PLH}	0.62	0.54 + 0.040*SL	0.53 + 0.041*SL	0.53 + 0.042*SL
	t_{PHL}	0.70	0.64 + 0.030*SL	0.65 + 0.025*SL	0.67 + 0.023*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.039*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to QN	t_{PLH}	0.55	0.47 + 0.042*SL	0.47 + 0.041*SL	0.47 + 0.041*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.088*SL	0.10 + 0.090*SL

KG80 FD2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.56	0.52 + 0.024*SL	0.52 + 0.022*SL	0.53 + 0.021*SL
	t_{PHL}	0.54	0.50 + 0.019*SL	0.51 + 0.015*SL	0.53 + 0.013*SL
	t_R	0.21	0.13 + 0.042*SL	0.12 + 0.043*SL	0.12 + 0.044*SL
	t_F	0.15	0.11 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
SCK to Q	t_{PLH}	0.63	0.58 + 0.024*SL	0.59 + 0.022*SL	0.60 + 0.021*SL
	t_{PHL}	0.48	0.45 + 0.019*SL	0.46 + 0.015*SL	0.47 + 0.013*SL
	t_R	0.22	0.14 + 0.042*SL	0.14 + 0.042*SL	0.13 + 0.044*SL
	t_F	0.16	0.12 + 0.021*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
RN to Q	t_{PHL}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.33 + 0.013*SL
	t_F	0.17	0.12 + 0.022*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
CK to QN	t_{PLH}	0.79	0.74 + 0.022*SL	0.75 + 0.020*SL	0.75 + 0.020*SL
	t_{PHL}	0.78	0.74 + 0.021*SL	0.75 + 0.017*SL	0.77 + 0.014*SL
	t_R	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.20	0.15 + 0.025*SL	0.16 + 0.020*SL	0.16 + 0.020*SL
SCK to QN	t_{PLH}	0.66	0.62 + 0.019*SL	0.62 + 0.019*SL	0.61 + 0.020*SL
	t_{PHL}	0.77	0.74 + 0.017*SL	0.74 + 0.014*SL	0.75 + 0.013*SL
	t_R	0.19	0.10 + 0.043*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.020*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
RN to QN	t_{PLH}	0.59	0.55 + 0.021*SL	0.55 + 0.020*SL	0.55 + 0.020*SL
	t_R	0.21	0.13 + 0.041*SL	0.13 + 0.042*SL	0.12 + 0.043*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.78	0.67 + 0.054*SL	0.68 + 0.051*SL	0.69 + 0.050*SL
	t_{PHL}	0.75	0.68 + 0.034*SL	0.71 + 0.026*SL	0.74 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SCK to Q	t_{PLH}	0.90	0.79 + 0.055*SL	0.81 + 0.051*SL	0.82 + 0.050*SL
	t_{PHL}	0.67	0.59 + 0.035*SL	0.62 + 0.027*SL	0.65 + 0.023*SL
	t_R	0.39	0.18 + 0.105*SL	0.18 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.12 + 0.042*SL
RN to Q	t_{PHL}	0.43	0.36 + 0.036*SL	0.39 + 0.027*SL	0.41 + 0.024*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN	t_{PLH}	1.04	0.93 + 0.053*SL	0.94 + 0.050*SL	0.94 + 0.050*SL
	t_{PHL}	1.04	0.96 + 0.040*SL	0.99 + 0.030*SL	1.03 + 0.025*SL
	t_R	0.38	0.17 + 0.103*SL	0.16 + 0.106*SL	0.14 + 0.108*SL
	t_F	0.25	0.16 + 0.047*SL	0.17 + 0.043*SL	0.18 + 0.042*SL
SCK to QN	t_{PLH}	0.87	0.77 + 0.049*SL	0.77 + 0.050*SL	0.77 + 0.050*SL
	t_{PHL}	1.03	0.97 + 0.033*SL	0.99 + 0.026*SL	1.02 + 0.023*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.73	0.62 + 0.053*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_R	0.38	0.17 + 0.102*SL	0.16 + 0.106*SL	0.14 + 0.108*SL

KGM80 FD2CSD2

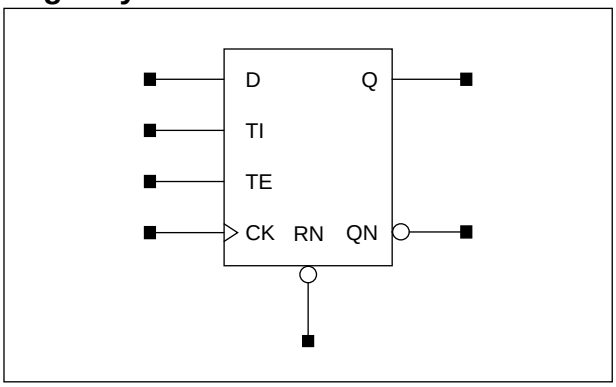
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.73 + 0.030*SL	0.74 + 0.026*SL	0.75 + 0.025*SL
	t_{PHL}	0.77	0.73 + 0.022*SL	0.75 + 0.016*SL	0.78 + 0.013*SL
	t_R	0.28	0.18 + 0.052*SL	0.18 + 0.052*SL	0.16 + 0.054*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
SCK to Q	t_{PLH}	0.93	0.87 + 0.031*SL	0.88 + 0.026*SL	0.89 + 0.025*SL
	t_{PHL}	0.69	0.65 + 0.022*SL	0.66 + 0.016*SL	0.69 + 0.013*SL
	t_R	0.30	0.19 + 0.052*SL	0.19 + 0.052*SL	0.18 + 0.053*SL
	t_F	0.19	0.14 + 0.025*SL	0.15 + 0.021*SL	0.16 + 0.020*SL
RN to Q	t_{PHL}	0.45	0.40 + 0.023*SL	0.42 + 0.016*SL	0.45 + 0.013*SL
	t_F	0.20	0.15 + 0.025*SL	0.16 + 0.021*SL	0.17 + 0.020*SL
CK to QN	t_{PLH}	1.10	1.05 + 0.028*SL	1.06 + 0.025*SL	1.06 + 0.025*SL
	t_{PHL}	1.13	1.08 + 0.024*SL	1.09 + 0.018*SL	1.13 + 0.015*SL
	t_R	0.28	0.18 + 0.052*SL	0.18 + 0.052*SL	0.17 + 0.053*SL
	t_F	0.23	0.18 + 0.027*SL	0.19 + 0.022*SL	0.21 + 0.021*SL
SCK to QN	t_{PLH}	0.94	0.89 + 0.024*SL	0.89 + 0.024*SL	0.88 + 0.025*SL
	t_{PHL}	1.14	1.11 + 0.019*SL	1.12 + 0.015*SL	1.14 + 0.013*SL
	t_R	0.25	0.15 + 0.051*SL	0.15 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.19	0.14 + 0.023*SL	0.15 + 0.021*SL	0.15 + 0.020*SL
RN to QN	t_{PLH}	0.79	0.73 + 0.028*SL	0.74 + 0.025*SL	0.74 + 0.024*SL
	t_R	0.28	0.18 + 0.052*SL	0.18 + 0.052*SL	0.17 + 0.053*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

FD2S/FD2SD2

D Flip-Flop with Reset, Scan, 1X/2X Drive

Logic Symbol



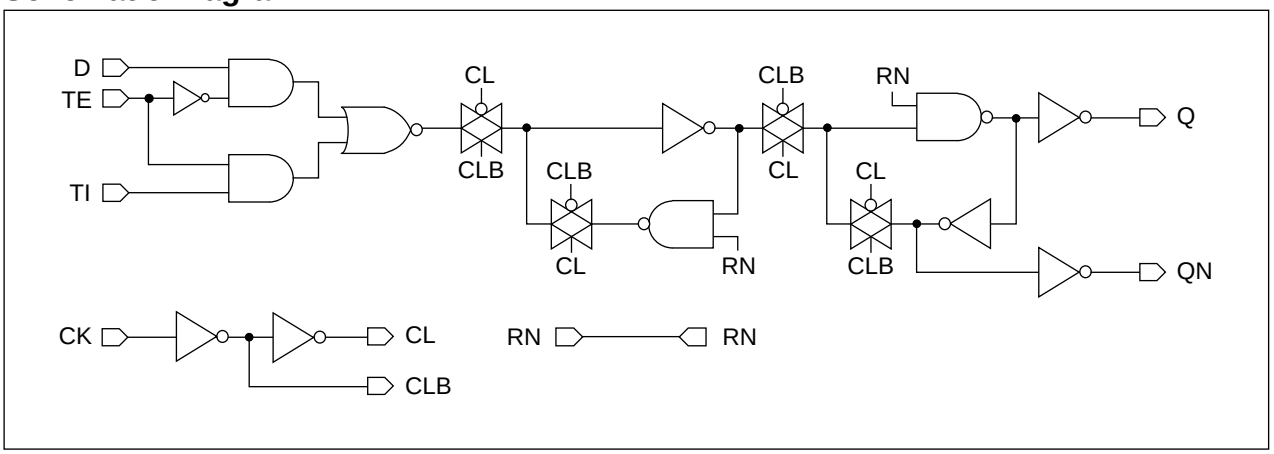
Truth Table

D	TI	TE	CK	RN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1

Cell Data

Input Load (SL)										Gate Count	
KG80											
FD2S					*FD2SD2*					*FD2S*	*FD2SD2*
D	TI	TE	CK	RN	D	TI	TE	CK	RN		
0.5	0.9	1.7	0.9	1.7	0.5	0.9	1.7	0.9	1.7	10.0	11.0
KGM80											
FD2S					*FD2SD2*					*FD2S*	*FD2SD2*
D	TI	TE	CK	RN	D	TI	TE	CK	RN		
1.0	1.0	2.1	1.0	2.0	1.0	1.0	2.1	1.0	2.0	10.0	11.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD2S	FD2SD2	FD2S	FD2SD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.47	0.47	0.86	0.86
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.53	0.53	0.96	0.96
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.58	0.58	0.96	1.02
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.63	0.63

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.49 + 0.044*SL	0.50 + 0.042*SL	0.50 + 0.042*SL
	t_{PHL}	0.55	0.49 + 0.032*SL	0.50 + 0.026*SL	0.52 + 0.024*SL
	t_R	0.29	0.12 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q	t_{PHL}	0.35	0.28 + 0.033*SL	0.30 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.12 + 0.039*SL	0.11 + 0.040*SL
CK to QN	t_{PLH}	0.69	0.61 + 0.041*SL	0.61 + 0.041*SL	0.61 + 0.042*SL
	t_{PHL}	0.66	0.60 + 0.030*SL	0.61 + 0.025*SL	0.63 + 0.023*SL
	t_R	0.26	0.09 + 0.085*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN	t_{PLH}	0.49	0.41 + 0.040*SL	0.41 + 0.041*SL	0.40 + 0.042*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL

KG80 FD2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.52 + 0.025*SL	0.52 + 0.022*SL	0.53 + 0.021*SL
	t_{PHL}	0.55	0.50 + 0.021*SL	0.52 + 0.016*SL	0.53 + 0.014*SL
	t_R	0.19	0.11 + 0.042*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PHL}	0.33	0.29 + 0.022*SL	0.30 + 0.017*SL	0.32 + 0.014*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
CK to QN	t_{PLH}	0.72	0.68 + 0.019*SL	0.68 + 0.019*SL	0.68 + 0.020*SL
	t_{PHL}	0.71	0.67 + 0.018*SL	0.68 + 0.015*SL	0.69 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.11 + 0.019*SL
RN to QN	t_{PLH}	0.51	0.47 + 0.019*SL	0.48 + 0.019*SL	0.47 + 0.020*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD2S/FD2SD2

D Flip-Flop with Reset, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2S

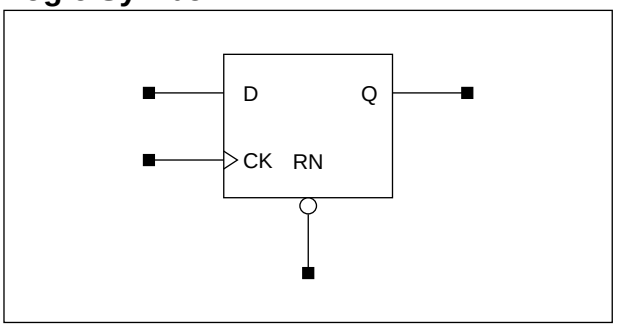
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.81	0.70 + 0.054*SL	0.71 + 0.051*SL	0.72 + 0.050*SL
	t_{PHL}	0.78	0.71 + 0.036*SL	0.73 + 0.027*SL	0.77 + 0.024*SL
	t_R	0.38	0.17 + 0.104*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.13 + 0.042*SL
RN to Q	t_{PHL}	0.45	0.38 + 0.037*SL	0.40 + 0.028*SL	0.44 + 0.024*SL
	t_F	0.23	0.14 + 0.045*SL	0.15 + 0.041*SL	0.14 + 0.041*SL
CK to QN	t_{PLH}	0.98	0.89 + 0.049*SL	0.88 + 0.050*SL	0.88 + 0.050*SL
	t_{PHL}	0.94	0.87 + 0.034*SL	0.89 + 0.026*SL	0.92 + 0.023*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.66	0.56 + 0.049*SL	0.56 + 0.050*SL	0.56 + 0.050*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL

KGM80 FD2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.72 + 0.032*SL	0.74 + 0.027*SL	0.75 + 0.025*SL
	t_{PHL}	0.78	0.73 + 0.024*SL	0.75 + 0.017*SL	0.79 + 0.014*SL
	t_R	0.25	0.14 + 0.054*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.026*SL	0.13 + 0.022*SL	0.15 + 0.021*SL
RN to Q	t_{PHL}	0.45	0.39 + 0.026*SL	0.42 + 0.018*SL	0.46 + 0.014*SL
	t_F	0.19	0.13 + 0.027*SL	0.15 + 0.022*SL	0.17 + 0.020*SL
CK to QN	t_{PLH}	1.03	0.98 + 0.025*SL	0.98 + 0.024*SL	0.97 + 0.025*SL
	t_{PHL}	1.01	0.96 + 0.021*SL	0.98 + 0.016*SL	1.01 + 0.013*SL
	t_R	0.22	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
RN to QN	t_{PLH}	0.70	0.65 + 0.025*SL	0.65 + 0.024*SL	0.64 + 0.025*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



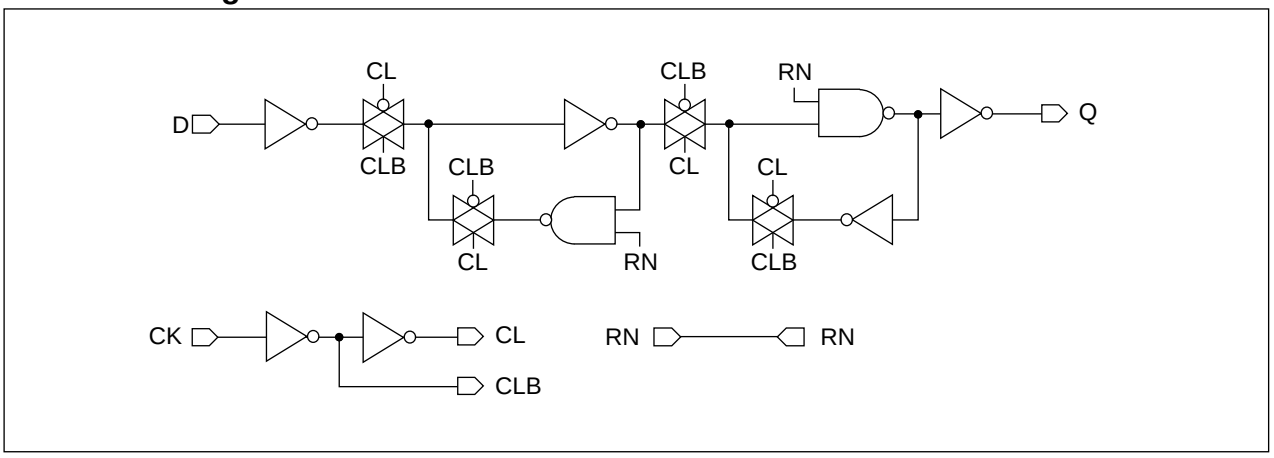
Truth Table

D	CK	RN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	0
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FD2Q			*FD2QD2*			*FD2Q*	*FD2QD2*
D	CK	RN	D	CK	RN		
0.8	0.8	1.4	0.8	0.8	1.4	7.0	8.0
KGM80							
FD2Q			*FD2QD2*			*FD2Q*	*FD2QD2*
D	CK	RN	D	CK	RN		
0.9	0.9	1.6	0.9	0.9	1.6	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD2Q	FD2QD2	FD2Q	FD2QD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.39	0.39	0.71	0.71
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.37	0.37	0.63	0.63

FD2Q/FD2QD2

D Flip-Flop with Reset, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.56	0.47 + 0.045*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.51	0.45 + 0.031*SL	0.46 + 0.026*SL	0.48 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.043*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to Q	t_{PHL}	0.34	0.27 + 0.034*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.040*SL

KG80 FD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.55	0.51 + 0.023*SL	0.51 + 0.022*SL	0.52 + 0.021*SL
	t_{PHL}	0.51	0.47 + 0.019*SL	0.48 + 0.015*SL	0.50 + 0.013*SL
	t_R	0.21	0.12 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.044*SL
	t_F	0.15	0.10 + 0.024*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PHL}	0.34	0.29 + 0.021*SL	0.31 + 0.016*SL	0.33 + 0.013*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.019*SL	0.13 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2Q

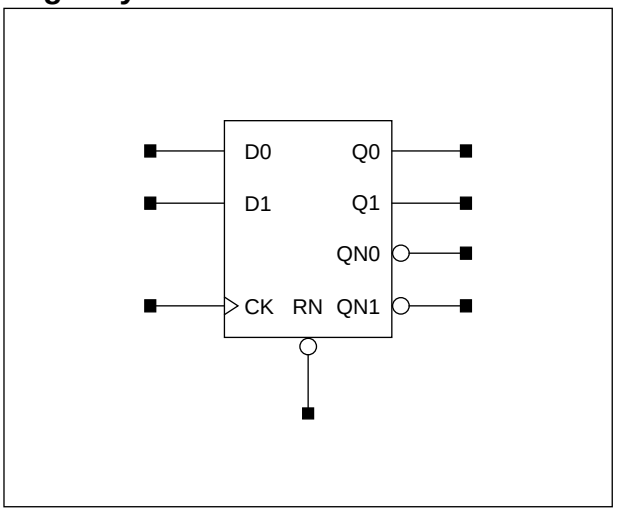
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.80	0.69 + 0.056*SL	0.70 + 0.050*SL	0.71 + 0.050*SL
	t_{PHL}	0.73	0.65 + 0.036*SL	0.68 + 0.027*SL	0.71 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.106*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q	t_{PHL}	0.44	0.37 + 0.038*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.045*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

KGM80 FD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.80	0.74 + 0.030*SL	0.75 + 0.027*SL	0.76 + 0.025*SL
	t_{PHL}	0.74	0.69 + 0.022*SL	0.71 + 0.016*SL	0.74 + 0.013*SL
	t_R	0.28	0.17 + 0.054*SL	0.17 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
RN to Q	t_{PHL}	0.45	0.40 + 0.023*SL	0.42 + 0.017*SL	0.46 + 0.013*SL
	t_F	0.20	0.15 + 0.027*SL	0.16 + 0.021*SL	0.17 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

Dn	CK	RN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
KG80			
Dn	CK	RN	
1.0	0.9	3.6	14.0
KGM80			
Dn	CK	RN	
1.0	1.0	4.4	14.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.61	1.02
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.99
Input Setup Time (D0 to CK)	t_{SU}	0.31	0.58
Input Hold Time (D0 to CK)	t_{HD}	0.15	0.33
Input Setup Time (D1 to CK)	t_{SU}	0.31	0.58
Input Hold Time (D1 to CK)	t_{HD}	0.15	0.33
Recovery Time (RN)	t_{RC}	0.15	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.62	0.53 + 0.044*SL	0.54 + 0.042*SL	0.54 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.031*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.089*SL	0.10 + 0.090*SL
	t_F	0.17	0.10 + 0.040*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to Q0	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to Q1	t_{PLH}	0.62	0.53 + 0.044*SL	0.54 + 0.042*SL	0.54 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.031*SL	0.59 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.089*SL	0.10 + 0.090*SL
	t_F	0.17	0.10 + 0.040*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to Q1	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to QN0	t_{PLH}	0.78	0.70 + 0.040*SL	0.70 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.70	0.64 + 0.030*SL	0.66 + 0.025*SL	0.67 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to QN0	t_{PLH}	0.48	0.40 + 0.040*SL	0.40 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.26	0.09 + 0.086*SL	0.09 + 0.089*SL	0.07 + 0.091*SL
CK to QN1	t_{PLH}	0.78	0.70 + 0.040*SL	0.70 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.70	0.64 + 0.030*SL	0.66 + 0.025*SL	0.67 + 0.024*SL
	t_R	0.26	0.09 + 0.085*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to QN1	t_{PLH}	0.48	0.40 + 0.040*SL	0.40 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.26	0.09 + 0.086*SL	0.09 + 0.089*SL	0.07 + 0.091*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2X2

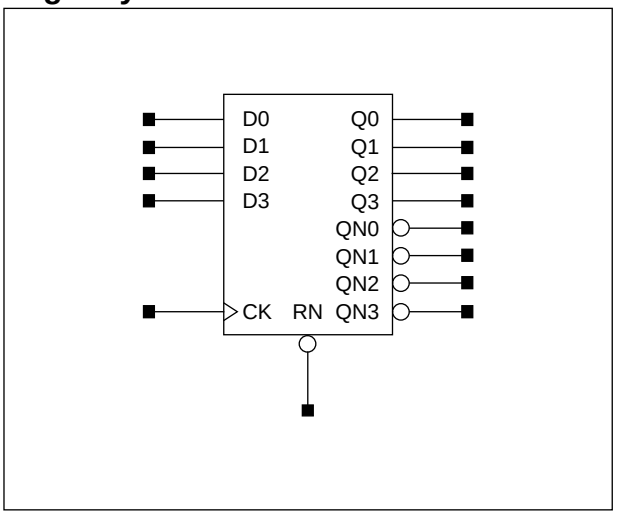
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.85	0.75 + 0.054*SL	0.75 + 0.051*SL	0.76 + 0.050*SL
	t_{PHL}	0.90	0.83 + 0.034*SL	0.85 + 0.026*SL	0.88 + 0.023*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q0	t_{PHL}	0.43	0.36 + 0.036*SL	0.39 + 0.027*SL	0.42 + 0.024*SL
	t_F	0.22	0.14 + 0.042*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to Q1	t_{PLH}	0.85	0.74 + 0.054*SL	0.75 + 0.051*SL	0.76 + 0.050*SL
	t_{PHL}	0.90	0.83 + 0.034*SL	0.85 + 0.026*SL	0.88 + 0.023*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q1	t_{PHL}	0.43	0.36 + 0.036*SL	0.39 + 0.027*SL	0.42 + 0.024*SL
	t_F	0.22	0.14 + 0.042*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN0	t_{PLH}	1.10	1.00 + 0.049*SL	1.00 + 0.049*SL	1.00 + 0.050*SL
	t_{PHL}	0.98	0.92 + 0.034*SL	0.94 + 0.026*SL	0.97 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN0	t_{PLH}	0.64	0.54 + 0.049*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
CK to QN1	t_{PLH}	1.10	1.00 + 0.049*SL	1.00 + 0.050*SL	1.00 + 0.050*SL
	t_{PHL}	0.98	0.92 + 0.033*SL	0.94 + 0.026*SL	0.96 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN1	t_{PLH}	0.64	0.54 + 0.049*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FD2X4

4-Bit D Flip-Flop with Reset

Logic Symbol



Truth Table

Dn	CK	RN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
KG80			
Dn	CK	RN	
1.0	0.9	7.5	28.0
KGM80			
Dn	CK	RN	
1.0	1.1	8.9	28.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.80	1.27
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.99
Input Setup Time (D0 to CK)	t_{SU}	0.20	0.46
Input Hold Time (D0 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D1 to CK)	t_{SU}	0.20	0.46
Input Hold Time (D1 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D2 to CK)	t_{SU}	0.20	0.46
Input Hold Time (D2 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D3 to CK)	t_{SU}	0.20	0.46
Input Hold Time (D3 to CK)	t_{HD}	0.26	0.43
Recovery Time (RN)	t_{RC}	0.15	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load

KG80 FD2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.73	0.64 + 0.043*SL	0.64 + 0.042*SL	0.65 + 0.042*SL
	t_{PHL}	0.84	0.77 + 0.031*SL	0.79 + 0.026*SL	0.80 + 0.024*SL
	t_R	0.29	0.12 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q0	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to Q1	t_{PLH}	0.74	0.65 + 0.044*SL	0.65 + 0.042*SL	0.66 + 0.042*SL
	t_{PHL}	0.84	0.78 + 0.031*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.29	0.12 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
RN to Q1	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to Q2	t_{PLH}	0.74	0.65 + 0.045*SL	0.65 + 0.042*SL	0.66 + 0.042*SL
	t_{PHL}	0.84	0.78 + 0.031*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.29	0.12 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
RN to Q2	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CK to Q3	t_{PLH}	0.73	0.64 + 0.043*SL	0.64 + 0.042*SL	0.65 + 0.042*SL
	t_{PHL}	0.84	0.77 + 0.031*SL	0.79 + 0.026*SL	0.80 + 0.024*SL
	t_R	0.29	0.12 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q3	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to QN0	t_{PLH}	0.97	0.89 + 0.040*SL	0.89 + 0.041*SL	0.89 + 0.042*SL
	t_{PHL}	0.81	0.75 + 0.030*SL	0.76 + 0.025*SL	0.77 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.09 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to QN0	t_{PLH}	0.48	0.40 + 0.040*SL	0.40 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.089*SL	0.07 + 0.091*SL
CK to QN1	t_{PLH}	0.98	0.90 + 0.040*SL	0.90 + 0.041*SL	0.89 + 0.042*SL
	t_{PHL}	0.82	0.76 + 0.030*SL	0.77 + 0.025*SL	0.78 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN1	t_{PLH}	0.48	0.40 + 0.040*SL	0.40 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
CK to QN2	t_{PLH}	0.98	0.90 + 0.040*SL	0.90 + 0.041*SL	0.90 + 0.041*SL
	t_{PHL}	0.82	0.76 + 0.030*SL	0.77 + 0.025*SL	0.78 + 0.023*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

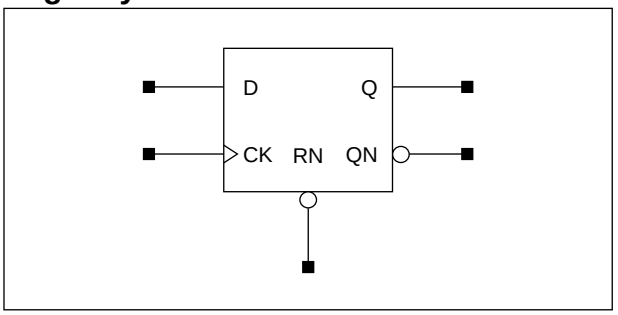
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.97	0.87 + 0.054*SL	0.88 + 0.051*SL	0.88 + 0.050*SL
	t_{PHL}	1.18	1.11 + 0.034*SL	1.13 + 0.027*SL	1.16 + 0.023*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q0	t_{PHL}	0.43	0.36 + 0.035*SL	0.39 + 0.027*SL	0.42 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to Q1	t_{PLH}	0.99	0.88 + 0.054*SL	0.89 + 0.051*SL	0.90 + 0.050*SL
	t_{PHL}	1.19	1.12 + 0.035*SL	1.14 + 0.027*SL	1.17 + 0.023*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q1	t_{PHL}	0.44	0.37 + 0.036*SL	0.39 + 0.027*SL	0.42 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to Q2	t_{PLH}	0.99	0.88 + 0.054*SL	0.89 + 0.051*SL	0.90 + 0.050*SL
	t_{PHL}	1.18	1.11 + 0.035*SL	1.14 + 0.027*SL	1.17 + 0.023*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q2	t_{PHL}	0.44	0.36 + 0.036*SL	0.39 + 0.027*SL	0.42 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to Q3	t_{PLH}	0.97	0.87 + 0.054*SL	0.88 + 0.051*SL	0.88 + 0.050*SL
	t_{PHL}	1.18	1.11 + 0.034*SL	1.13 + 0.027*SL	1.16 + 0.023*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q3	t_{PHL}	0.43	0.36 + 0.035*SL	0.39 + 0.027*SL	0.42 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN0	t_{PLH}	1.38	1.28 + 0.049*SL	1.28 + 0.050*SL	1.28 + 0.050*SL
	t_{PHL}	1.10	1.04 + 0.033*SL	1.06 + 0.026*SL	1.08 + 0.023*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN0	t_{PLH}	0.64	0.54 + 0.049*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
CK to QN1	t_{PLH}	1.39	1.29 + 0.049*SL	1.29 + 0.050*SL	1.28 + 0.050*SL
	t_{PHL}	1.12	1.05 + 0.033*SL	1.07 + 0.026*SL	1.10 + 0.023*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN1	t_{PLH}	0.64	0.54 + 0.049*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
CK to QN2	t_{PLH}	1.39	1.29 + 0.050*SL	1.29 + 0.050*SL	1.29 + 0.050*SL
	t_{PHL}	1.12	1.05 + 0.033*SL	1.07 + 0.026*SL	1.10 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Logic Symbol



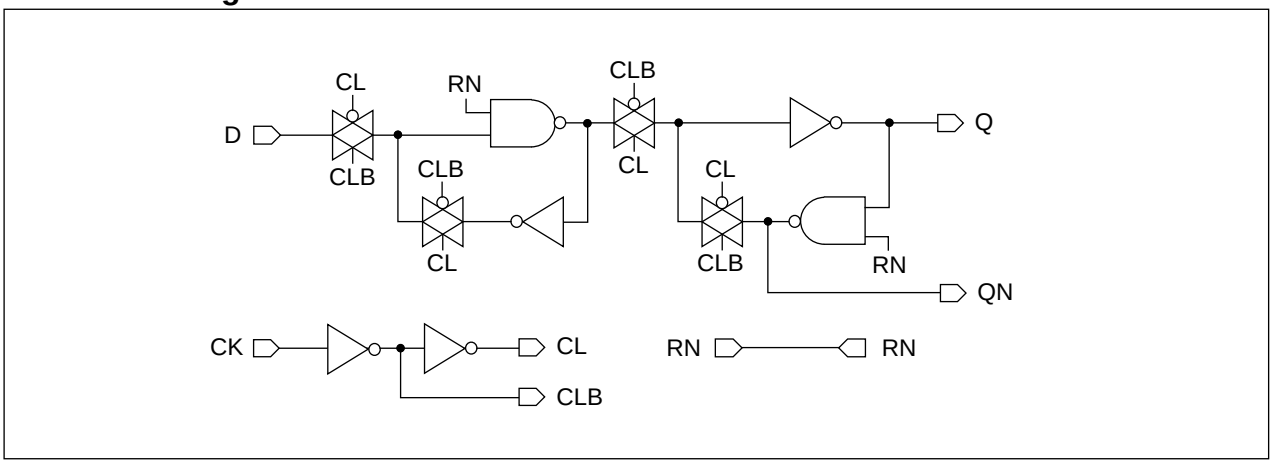
Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
YFD2			*YFD2D2*			*YFD2*	*YFD2D2*
D	CK	RN	D	CK	RN		
2.9	0.8	1.4	2.9	0.8	2.1	6.0	8.0
KGM80							
YFD2			*YFD2D2*			*YFD2*	*YFD2D2*
D	CK	RN	D	CK	RN		
3.7	0.9	1.7	3.7	0.9	2.4	6.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		YFD2	YFD2D2	YFD2	YFD2D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	1.02	1.02
Input Setup Time (D to CK)	t_{SU}	0.26	0.26	0.55	0.52
Input Hold Time (D to CK)	t_{HD}	0.26	0.26	0.46	0.46
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.15	0.15	0.41	0.41

YFD2/YFD2D2

Fast D Flip-Flop with Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YFD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.48	0.39 + 0.046*SL	0.40 + 0.043*SL	0.41 + 0.042*SL
	t_{PHL}	0.38	0.32 + 0.033*SL	0.33 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.36	0.19 + 0.086*SL	0.19 + 0.088*SL	0.17 + 0.089*SL
	t_F	0.22	0.13 + 0.044*SL	0.13 + 0.043*SL	0.14 + 0.042*SL
RN to Q	t_{PHL}	0.48	0.41 + 0.040*SL	0.43 + 0.029*SL	0.46 + 0.025*SL
	t_F	0.26	0.17 + 0.042*SL	0.18 + 0.040*SL	0.18 + 0.039*SL
CK to QN	t_{PLH}	0.58	0.41 + 0.085*SL	0.43 + 0.080*SL	0.45 + 0.077*SL
	t_{PHL}	0.67	0.48 + 0.092*SL	0.49 + 0.090*SL	0.49 + 0.089*SL
	t_R	0.35	0.16 + 0.094*SL	0.16 + 0.094*SL	0.16 + 0.095*SL
	t_F	0.31	0.14 + 0.086*SL	0.14 + 0.086*SL	0.14 + 0.086*SL
RN to QN	t_{PLH}	0.28	0.20 + 0.041*SL	0.20 + 0.041*SL	0.22 + 0.039*SL
	t_R	0.42	0.29 + 0.064*SL	0.31 + 0.056*SL	0.31 + 0.055*SL

KG80 YFD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.48	0.43 + 0.025*SL	0.44 + 0.023*SL	0.44 + 0.022*SL
	t_{PHL}	0.38	0.34 + 0.019*SL	0.35 + 0.016*SL	0.36 + 0.015*SL
	t_R	0.30	0.22 + 0.040*SL	0.22 + 0.042*SL	0.20 + 0.044*SL
	t_F	0.20	0.15 + 0.023*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
RN to Q	t_{PHL}	0.48	0.43 + 0.024*SL	0.44 + 0.019*SL	0.47 + 0.015*SL
	t_F	0.23	0.19 + 0.023*SL	0.19 + 0.020*SL	0.19 + 0.021*SL
CK to QN	t_{PLH}	0.52	0.43 + 0.047*SL	0.44 + 0.043*SL	0.46 + 0.041*SL
	t_{PHL}	0.60	0.51 + 0.048*SL	0.51 + 0.046*SL	0.52 + 0.045*SL
	t_R	0.23	0.14 + 0.047*SL	0.14 + 0.047*SL	0.13 + 0.048*SL
	t_F	0.21	0.12 + 0.042*SL	0.12 + 0.043*SL	0.12 + 0.043*SL
RN to QN	t_{PLH}	0.23	0.19 + 0.022*SL	0.19 + 0.020*SL	0.19 + 0.021*SL
	t_R	0.33	0.26 + 0.036*SL	0.27 + 0.034*SL	0.30 + 0.029*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YFD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.56 + 0.057*SL	0.58 + 0.051*SL	0.59 + 0.050*SL
	t_{PHL}	0.54	0.47 + 0.038*SL	0.49 + 0.029*SL	0.53 + 0.025*SL
	t_R	0.47	0.27 + 0.105*SL	0.26 + 0.106*SL	0.24 + 0.108*SL
	t_F	0.27	0.18 + 0.049*SL	0.19 + 0.044*SL	0.21 + 0.042*SL
RN to Q	t_{PHL}	0.68	0.58 + 0.048*SL	0.63 + 0.031*SL	0.70 + 0.025*SL
	t_F	0.33	0.23 + 0.047*SL	0.25 + 0.041*SL	0.26 + 0.040*SL
CK to QN	t_{PLH}	0.82	0.62 + 0.100*SL	0.64 + 0.091*SL	0.69 + 0.087*SL
	t_{PHL}	0.93	0.70 + 0.113*SL	0.71 + 0.108*SL	0.72 + 0.107*SL
	t_R	0.47	0.25 + 0.112*SL	0.25 + 0.112*SL	0.25 + 0.112*SL
	t_F	0.39	0.20 + 0.093*SL	0.20 + 0.094*SL	0.19 + 0.095*SL
RN to QN	t_{PLH}	0.36	0.26 + 0.050*SL	0.26 + 0.050*SL	0.31 + 0.046*SL
	t_R	0.55	0.37 + 0.092*SL	0.43 + 0.070*SL	0.46 + 0.067*SL

KGM80 YFD2D2

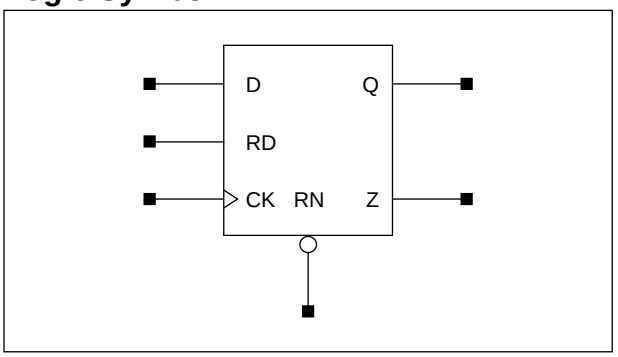
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.67	0.61 + 0.031*SL	0.62 + 0.027*SL	0.64 + 0.026*SL
	t_{PHL}	0.56	0.51 + 0.023*SL	0.52 + 0.018*SL	0.56 + 0.015*SL
	t_R	0.40	0.30 + 0.050*SL	0.29 + 0.051*SL	0.28 + 0.052*SL
	t_F	0.26	0.21 + 0.026*SL	0.21 + 0.024*SL	0.24 + 0.021*SL
RN to Q	t_{PHL}	0.68	0.62 + 0.030*SL	0.64 + 0.021*SL	0.71 + 0.015*SL
	t_F	0.31	0.26 + 0.024*SL	0.27 + 0.021*SL	0.29 + 0.020*SL
CK to QN	t_{PLH}	0.76	0.65 + 0.055*SL	0.66 + 0.050*SL	0.70 + 0.046*SL
	t_{PHL}	0.84	0.73 + 0.058*SL	0.73 + 0.055*SL	0.75 + 0.054*SL
	t_R	0.32	0.21 + 0.056*SL	0.21 + 0.056*SL	0.21 + 0.056*SL
	t_F	0.26	0.17 + 0.045*SL	0.17 + 0.046*SL	0.16 + 0.047*SL
RN to QN	t_{PLH}	0.29	0.24 + 0.026*SL	0.24 + 0.025*SL	0.24 + 0.025*SL
	t_R	0.42	0.32 + 0.050*SL	0.33 + 0.044*SL	0.44 + 0.035*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FD2T/FD2TD2

D Flip-Flop with Reset, Tri-State Output, 1X/2X Drive

Logic Symbol



Truth Table

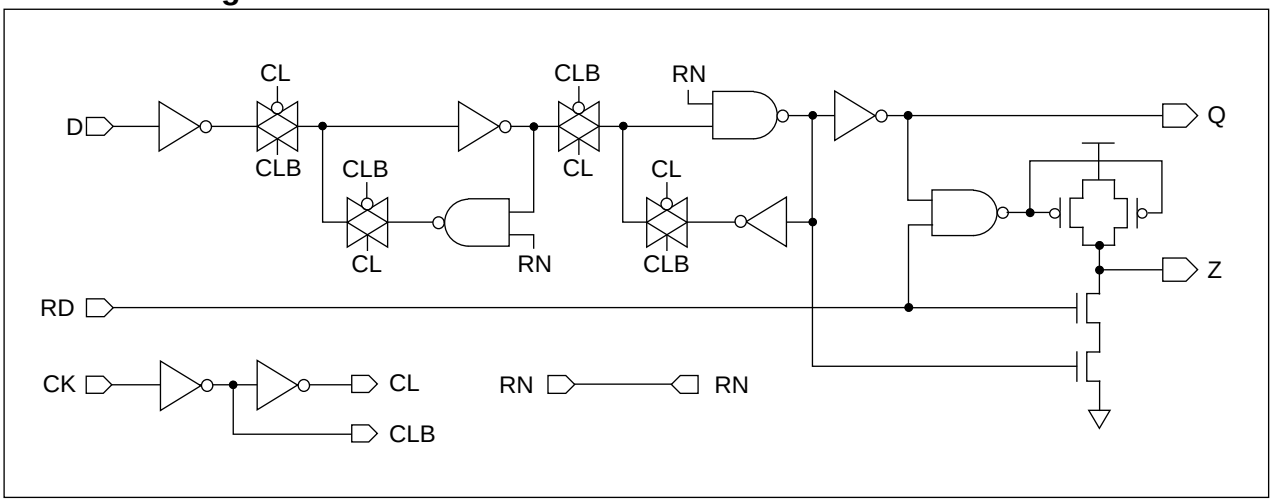
D	RD*	CK	RN	Q (n+1)	Z (n+1)
0	1	↑	1	0	0
1	1	↑	1	1	1
x	1	x	0	0	0
x	0	x	1	x	Hi-Z
x	1	↓	1	Q (n)	Z (n)

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)								Output Load (SL)		Gate Count	
KG80											
FD2T				*FD2TD2*				*FD2T*	*FD2TD2*	*FD2T*	*FD2TD2*
D	RD	CK	RN	D	RD	CK	RN	Z	Z		
0.9	1.4	0.9	1.7	0.9	2.0	0.9	1.7	0.7	1.4	10.0	13.0
KGM80											
FD2T				*FD2TD2*				*FD2T*	*FD2TD2*	*FD2T*	*FD2TD2*
D	RD	CK	RN	D	RD	CK	RN	Z	Z		
1.1	1.7	1.0	2.0	1.1	2.6	1.0	2.0	0.9	1.8	10.0	13.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD2T	FD2TD2	FD2T	FD2TD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.64	1.02	1.05
Input Setup Time (D to CK)	t_{SU}	0.37	0.37	0.64	0.64
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.37	0.37	0.63	0.63

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2T

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.58 + 0.053*SL	0.58 + 0.052*SL	0.60 + 0.049*SL
	t_{PHL}	0.63	0.56 + 0.038*SL	0.57 + 0.032*SL	0.60 + 0.028*SL
	t_R	0.41	0.20 + 0.103*SL	0.18 + 0.110*SL	0.21 + 0.105*SL
	t_F	0.25	0.15 + 0.048*SL	0.15 + 0.049*SL	0.16 + 0.048*SL
RN to Q	t_{PHL}	0.45	0.37 + 0.038*SL	0.39 + 0.032*SL	0.42 + 0.027*SL
	t_F	0.27	0.18 + 0.045*SL	0.17 + 0.047*SL	0.17 + 0.047*SL
CK to Z	t_{PLH}	0.93	0.75 + 0.088*SL	0.77 + 0.081*SL	0.83 + 0.072*SL
	t_{PHL}	0.87	0.72 + 0.074*SL	0.74 + 0.066*SL	0.78 + 0.059*SL
	t_R	0.22	0.11 + 0.053*SL	0.10 + 0.057*SL	0.12 + 0.054*SL
	t_F	0.48	0.28 + 0.099*SL	0.27 + 0.103*SL	0.31 + 0.097*SL
RN to Z	t_{PHL}	0.69	0.54 + 0.074*SL	0.56 + 0.065*SL	0.60 + 0.059*SL
	t_F	0.48	0.28 + 0.098*SL	0.27 + 0.102*SL	0.31 + 0.097*SL
RD to Z	t_{PLH}	0.24	0.17 + 0.035*SL	0.19 + 0.028*SL	0.21 + 0.025*SL
	t_{PHL}	0.13	-0.01 + 0.069*SL	0.04 + 0.048*SL	0.10 + 0.040*SL
	t_R	0.24	0.16 + 0.042*SL	0.14 + 0.050*SL	0.14 + 0.051*SL
	t_F	0.34	0.18 + 0.081*SL	0.20 + 0.076*SL	0.20 + 0.075*SL
	t_{PLZ}	0.25	0.25 + 0.000*SL	0.25 + 0.000*SL	0.25 + 0.000*SL
	t_{PHZ}	0.38	0.38 + 0.000*SL	0.38 + 0.000*SL	0.38 + 0.000*SL

KG80 FD2TD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.63 + 0.030*SL	0.63 + 0.028*SL	0.66 + 0.025*SL
	t_{PHL}	0.64	0.59 + 0.026*SL	0.60 + 0.021*SL	0.63 + 0.016*SL
	t_R	0.27	0.17 + 0.052*SL	0.17 + 0.052*SL	0.18 + 0.051*SL
	t_F	0.21	0.16 + 0.026*SL	0.16 + 0.025*SL	0.18 + 0.023*SL
RN to Q	t_{PHL}	0.46	0.40 + 0.026*SL	0.42 + 0.020*SL	0.45 + 0.015*SL
	t_F	0.23	0.18 + 0.025*SL	0.18 + 0.023*SL	0.20 + 0.021*SL
CK to Z	t_{PLH}	0.95	0.84 + 0.053*SL	0.86 + 0.047*SL	0.91 + 0.040*SL
	t_{PHL}	0.90	0.81 + 0.046*SL	0.82 + 0.040*SL	0.87 + 0.033*SL
	t_R	0.19	0.13 + 0.030*SL	0.14 + 0.028*SL	0.15 + 0.026*SL
	t_F	0.44	0.34 + 0.052*SL	0.34 + 0.052*SL	0.36 + 0.049*SL
RN to Z	t_{PHL}	0.71	0.62 + 0.045*SL	0.64 + 0.039*SL	0.68 + 0.032*SL
	t_F	0.44	0.33 + 0.052*SL	0.34 + 0.051*SL	0.36 + 0.048*SL
RD to Z	t_{PLH}	0.27	0.22 + 0.025*SL	0.24 + 0.019*SL	0.27 + 0.014*SL
	t_{PHL}	0.06	-0.02 + 0.042*SL	0.01 + 0.031*SL	0.07 + 0.022*SL
	t_R	0.25	0.22 + 0.014*SL	0.20 + 0.022*SL	0.19 + 0.023*SL
	t_F	0.27	0.17 + 0.047*SL	0.19 + 0.039*SL	0.21 + 0.036*SL
	t_{PLZ}	0.25	0.25 + 0.000*SL	0.25 + 0.000*SL	0.25 + 0.000*SL
	t_{PHZ}	0.54	0.54 + 0.001*SL	0.54 + 0.000*SL	0.54 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD2T/FD2TD2

D Flip-Flop with Reset, Tri-State Output, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2T

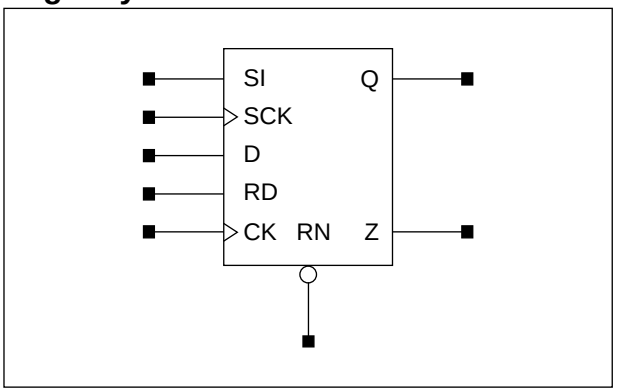
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.91	0.81 + 0.054*SL	0.82 + 0.050*SL	0.82 + 0.050*SL
	t_{PHL}	0.86	0.79 + 0.036*SL	0.81 + 0.027*SL	0.85 + 0.024*SL
	t_R	0.49	0.28 + 0.103*SL	0.27 + 0.106*SL	0.25 + 0.108*SL
	t_F	0.28	0.19 + 0.043*SL	0.20 + 0.041*SL	0.20 + 0.041*SL
RN to Q	t_{PHL}	0.54	0.47 + 0.037*SL	0.49 + 0.028*SL	0.54 + 0.024*SL
	t_F	0.30	0.21 + 0.044*SL	0.22 + 0.040*SL	0.21 + 0.041*SL
CK to Z	t_{PLH}	1.25	1.07 + 0.091*SL	1.10 + 0.080*SL	1.16 + 0.075*SL
	t_{PHL}	1.13	1.00 + 0.068*SL	1.03 + 0.055*SL	1.07 + 0.051*SL
	t_R	0.25	0.15 + 0.054*SL	0.15 + 0.053*SL	0.13 + 0.055*SL
	t_F	0.53	0.35 + 0.088*SL	0.36 + 0.086*SL	0.36 + 0.086*SL
RN to Z	t_{PHL}	0.81	0.68 + 0.068*SL	0.71 + 0.055*SL	0.75 + 0.051*SL
	t_F	0.53	0.36 + 0.087*SL	0.36 + 0.086*SL	0.36 + 0.086*SL
RD to Z	t_{PLH}	0.31	0.25 + 0.033*SL	0.26 + 0.026*SL	0.28 + 0.025*SL
	t_{PHL}	0.16	0.05 + 0.052*SL	0.09 + 0.038*SL	0.11 + 0.037*SL
	t_R	0.29	0.23 + 0.029*SL	0.17 + 0.050*SL	0.14 + 0.053*SL
	t_F	0.32	0.18 + 0.070*SL	0.18 + 0.069*SL	0.14 + 0.073*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.47	0.47 + 0.000*SL	0.47 + 0.000*SL	0.47 + 0.000*SL

KGM80 FD2TD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.92	0.86 + 0.032*SL	0.87 + 0.028*SL	0.90 + 0.025*SL
	t_{PHL}	0.90	0.84 + 0.026*SL	0.86 + 0.019*SL	0.91 + 0.015*SL
	t_R	0.33	0.22 + 0.054*SL	0.22 + 0.052*SL	0.22 + 0.052*SL
	t_F	0.24	0.19 + 0.027*SL	0.20 + 0.022*SL	0.22 + 0.020*SL
RN to Q	t_{PHL}	0.57	0.51 + 0.027*SL	0.53 + 0.019*SL	0.59 + 0.014*SL
	t_F	0.26	0.21 + 0.025*SL	0.22 + 0.021*SL	0.24 + 0.019*SL
CK to Z	t_{PLH}	1.31	1.19 + 0.057*SL	1.22 + 0.047*SL	1.28 + 0.042*SL
	t_{PHL}	1.20	1.12 + 0.043*SL	1.14 + 0.034*SL	1.20 + 0.029*SL
	t_R	0.23	0.18 + 0.027*SL	0.18 + 0.026*SL	0.18 + 0.027*SL
	t_F	0.51	0.41 + 0.048*SL	0.42 + 0.045*SL	0.43 + 0.044*SL
RN to Z	t_{PHL}	0.88	0.79 + 0.042*SL	0.81 + 0.034*SL	0.88 + 0.028*SL
	t_F	0.50	0.40 + 0.049*SL	0.42 + 0.044*SL	0.43 + 0.043*SL
RD to Z	t_{PLH}	0.37	0.32 + 0.023*SL	0.34 + 0.016*SL	0.37 + 0.013*SL
	t_{PHL}	0.11	0.05 + 0.030*SL	0.07 + 0.022*SL	0.11 + 0.018*SL
	t_R	0.33	0.30 + 0.016*SL	0.29 + 0.018*SL	0.22 + 0.025*SL
	t_F	0.25	0.17 + 0.039*SL	0.19 + 0.033*SL	0.17 + 0.035*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.69	0.69 + 0.000*SL	0.69 + 0.000*SL	0.69 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

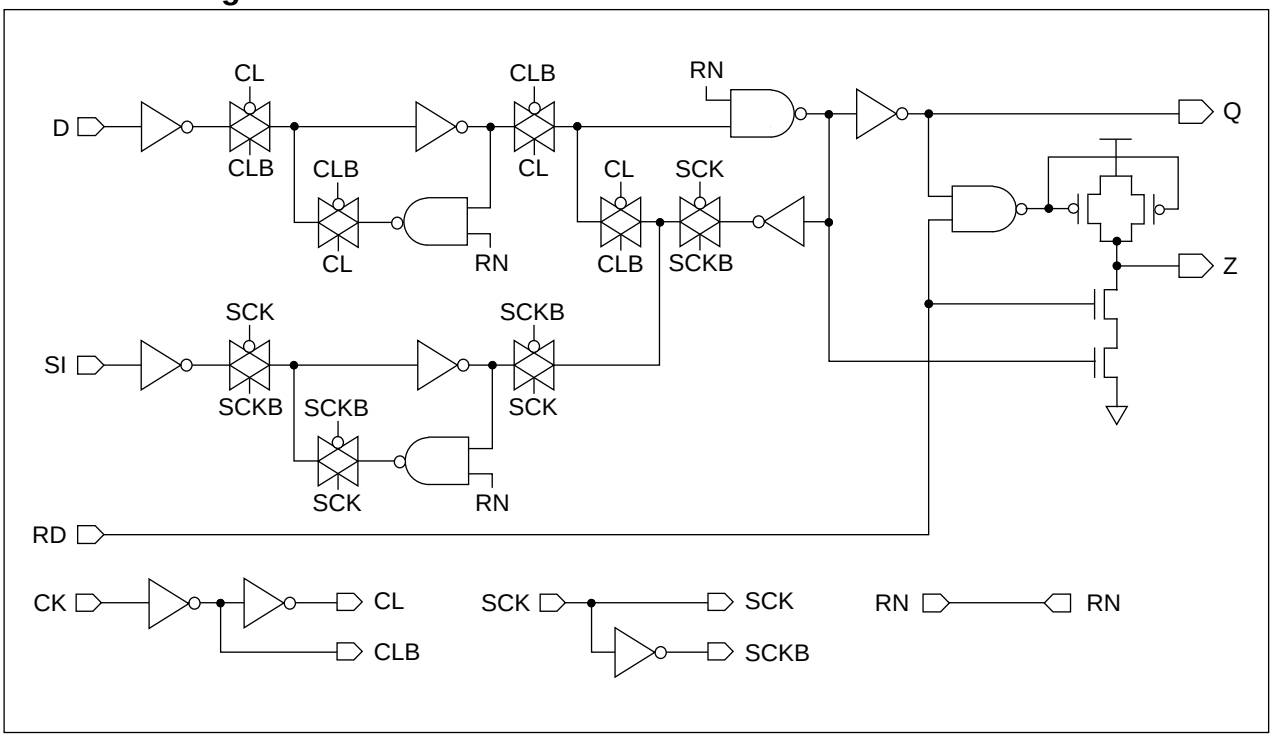
SI	SCK	D	RD	CK	RN	Q (n+1)	Z (n+1)
x	0	0	1	⎍	1	0	0
x	0	1	1	⎍	1	1	1
0	⎍	x	1	0	1	0	0
1	⎍	x	1	0	1	1	1
x	x	x	1	x	0	0	0
x	x	x	0	x	1	x	Hi-Z

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)												Output Load (SL)		Gate Count	
KG80															
FD2TCS						*FD2TCSD2*						*FD2TCS*	*FD2TCSD2*	*FD2TCS*	*FD2TCSD2*
SI	SCK	D	RD	CK	RN	SI	SCK	D	RD	CK	RN	Z	Z		
0.8	2.1	0.9	1.6	0.9	2.9	0.8	2.5	0.9	2.4	0.9	3.0	0.9	1.5	15.0	17.0
KGM80															
FD2TCS						*FD2TCSD2*						*FD2TCS*	*FD2TCSD2*	*FD2TCS*	*FD2TCSD2*
SI	SCK	D	RD	CK	RN	SI	SCK	D	RD	CK	RN	Z	Z		
1.0	2.9	1.0	1.9	1.0	3.4	1.0	2.9	1.0	2.8	1.0	3.6	1.3	2.0	15.0	17.0

Schematic Diagram



FD2TCS/FD2TCSD2

D Flip-Flop with Reset, Scan Clock, Tri-State Output, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD2TCS	FD2TCSD2	FD2TCS	FD2TCSD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SCK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (SCK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	1.02
Input Setup Time (D to CK)	t_{SU}	0.37	0.37	0.64	0.64
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.56	0.56	0.96	0.96
Input Hold Time (SI to SCK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.63	0.63
Recovery Time (RN to SCK)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to SCK)	t_{HD}	0.26	0.26	0.63	0.63

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2TCS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.56 + 0.044*SL	0.56 + 0.042*SL	0.57 + 0.042*SL
	t_{PHL}	0.60	0.53 + 0.031*SL	0.55 + 0.026*SL	0.56 + 0.024*SL
	t_R	0.38	0.19 + 0.094*SL	0.21 + 0.087*SL	0.20 + 0.089*SL
	t_F	0.22	0.14 + 0.040*SL	0.14 + 0.040*SL	0.14 + 0.040*SL
SCK to Q	t_{PLH}	0.72	0.63 + 0.045*SL	0.63 + 0.042*SL	0.64 + 0.041*SL
	t_{PHL}	0.54	0.48 + 0.033*SL	0.49 + 0.026*SL	0.51 + 0.024*SL
	t_R	0.39	0.21 + 0.091*SL	0.22 + 0.086*SL	0.21 + 0.089*SL
	t_F	0.23	0.15 + 0.039*SL	0.15 + 0.039*SL	0.14 + 0.040*SL
RN to Q	t_{PHL}	0.39	0.33 + 0.032*SL	0.34 + 0.026*SL	0.36 + 0.024*SL
	t_F	0.24	0.16 + 0.040*SL	0.16 + 0.039*SL	0.15 + 0.041*SL
CK to Z	t_{PLH}	0.90	0.74 + 0.077*SL	0.76 + 0.069*SL	0.79 + 0.065*SL
	t_{PHL}	0.82	0.70 + 0.060*SL	0.71 + 0.052*SL	0.73 + 0.050*SL
	t_R	0.21	0.12 + 0.045*SL	0.13 + 0.044*SL	0.12 + 0.046*SL
	t_F	0.43	0.26 + 0.083*SL	0.26 + 0.082*SL	0.26 + 0.082*SL
SCK to Z	t_{PLH}	0.96	0.81 + 0.077*SL	0.83 + 0.069*SL	0.86 + 0.065*SL
	t_{PHL}	0.76	0.64 + 0.060*SL	0.66 + 0.052*SL	0.68 + 0.050*SL
	t_R	0.21	0.13 + 0.043*SL	0.12 + 0.045*SL	0.12 + 0.046*SL
	t_F	0.43	0.26 + 0.083*SL	0.27 + 0.082*SL	0.27 + 0.082*SL
RN to Z	t_{PHL}	0.61	0.49 + 0.060*SL	0.51 + 0.052*SL	0.53 + 0.050*SL
	t_F	0.43	0.26 + 0.084*SL	0.27 + 0.082*SL	0.27 + 0.082*SL
RD to Z	t_{PLH}	0.22	0.16 + 0.029*SL	0.18 + 0.023*SL	0.19 + 0.021*SL
	t_{PHL}	0.13	0.03 + 0.050*SL	0.06 + 0.037*SL	0.08 + 0.034*SL
	t_R	0.23	0.17 + 0.035*SL	0.15 + 0.040*SL	0.13 + 0.043*SL
	t_F	0.31	0.18 + 0.063*SL	0.18 + 0.061*SL	0.16 + 0.065*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.40	0.40 + -0.001*SL	0.40 + 0.000*SL	0.40 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2TCSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.67	0.62 + 0.026*SL	0.63 + 0.022*SL	0.64 + 0.021*SL
	t_{PHL}	0.63	0.58 + 0.023*SL	0.60 + 0.017*SL	0.62 + 0.015*SL
	t_R	0.25	0.17 + 0.042*SL	0.16 + 0.044*SL	0.17 + 0.044*SL
	t_F	0.20	0.16 + 0.023*SL	0.16 + 0.020*SL	0.17 + 0.020*SL
SCK to Q	t_{PLH}	0.76	0.71 + 0.026*SL	0.71 + 0.023*SL	0.73 + 0.021*SL
	t_{PHL}	0.58	0.53 + 0.023*SL	0.54 + 0.018*SL	0.57 + 0.015*SL
	t_R	0.27	0.18 + 0.043*SL	0.18 + 0.043*SL	0.18 + 0.043*SL
	t_F	0.21	0.16 + 0.023*SL	0.17 + 0.020*SL	0.18 + 0.019*SL
RN to Q	t_{PHL}	0.42	0.37 + 0.023*SL	0.38 + 0.018*SL	0.41 + 0.014*SL
	t_F	0.21	0.17 + 0.022*SL	0.18 + 0.019*SL	0.18 + 0.018*SL
CK to Z	t_{PLH}	0.93	0.84 + 0.047*SL	0.85 + 0.041*SL	0.88 + 0.037*SL
	t_{PHL}	0.87	0.79 + 0.037*SL	0.80 + 0.032*SL	0.83 + 0.028*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.022*SL	0.15 + 0.022*SL
	t_F	0.39	0.30 + 0.044*SL	0.30 + 0.042*SL	0.30 + 0.042*SL
SCK to Z	t_{PLH}	1.02	0.92 + 0.048*SL	0.94 + 0.041*SL	0.97 + 0.036*SL
	t_{PHL}	0.82	0.74 + 0.038*SL	0.75 + 0.032*SL	0.78 + 0.028*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.022*SL	0.15 + 0.022*SL
	t_F	0.39	0.30 + 0.045*SL	0.30 + 0.042*SL	0.31 + 0.042*SL
RN to Z	t_{PHL}	0.65	0.58 + 0.037*SL	0.59 + 0.031*SL	0.62 + 0.027*SL
	t_F	0.38	0.29 + 0.043*SL	0.30 + 0.041*SL	0.30 + 0.041*SL
RD to Z	t_{PLH}	0.24	0.20 + 0.018*SL	0.21 + 0.015*SL	0.23 + 0.012*SL
	t_{PHL}	0.07	0.01 + 0.031*SL	0.03 + 0.023*SL	0.06 + 0.018*SL
	t_R	0.23	0.20 + 0.014*SL	0.19 + 0.018*SL	0.18 + 0.020*SL
	t_F	0.23	0.15 + 0.038*SL	0.17 + 0.031*SL	0.17 + 0.031*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.53	0.53 + -0.001*SL	0.53 + 0.000*SL	0.53 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD2TCS/FD2TCSD2

D Flip-Flop with Reset, Scan Clock, Tri-State Output, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2TCS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.90	0.79 + 0.054*SL	0.80 + 0.051*SL	0.81 + 0.050*SL
	t_{PHL}	0.84	0.77 + 0.035*SL	0.79 + 0.027*SL	0.83 + 0.024*SL
	t_R	0.50	0.27 + 0.114*SL	0.29 + 0.106*SL	0.27 + 0.108*SL
	t_F	0.26	0.18 + 0.043*SL	0.18 + 0.041*SL	0.18 + 0.042*SL
SCK to Q	t_{PLH}	1.04	0.93 + 0.055*SL	0.94 + 0.051*SL	0.95 + 0.050*SL
	t_{PHL}	0.76	0.69 + 0.036*SL	0.71 + 0.027*SL	0.75 + 0.024*SL
	t_R	0.52	0.29 + 0.111*SL	0.31 + 0.105*SL	0.28 + 0.108*SL
	t_F	0.27	0.19 + 0.043*SL	0.20 + 0.040*SL	0.19 + 0.041*SL
RN to Q	t_{PHL}	0.52	0.45 + 0.036*SL	0.47 + 0.028*SL	0.51 + 0.024*SL
	t_F	0.28	0.20 + 0.043*SL	0.20 + 0.041*SL	0.20 + 0.042*SL
CK to Z	t_{PLH}	1.26	1.07 + 0.095*SL	1.10 + 0.083*SL	1.16 + 0.078*SL
	t_{PHL}	1.11	0.98 + 0.064*SL	1.01 + 0.054*SL	1.04 + 0.051*SL
	t_R	0.28	0.17 + 0.053*SL	0.17 + 0.053*SL	0.16 + 0.054*SL
	t_F	0.51	0.33 + 0.090*SL	0.34 + 0.087*SL	0.35 + 0.086*SL
SCK to Z	t_{PLH}	1.40	1.21 + 0.095*SL	1.25 + 0.083*SL	1.30 + 0.078*SL
	t_{PHL}	1.03	0.90 + 0.064*SL	0.93 + 0.054*SL	0.96 + 0.051*SL
	t_R	0.28	0.17 + 0.053*SL	0.17 + 0.053*SL	0.16 + 0.054*SL
	t_F	0.51	0.33 + 0.091*SL	0.34 + 0.086*SL	0.35 + 0.085*SL
RN to Z	t_{PHL}	0.78	0.65 + 0.064*SL	0.68 + 0.054*SL	0.72 + 0.051*SL
	t_F	0.51	0.33 + 0.089*SL	0.34 + 0.087*SL	0.35 + 0.085*SL
RD to Z	t_{PLH}	0.32	0.26 + 0.031*SL	0.27 + 0.026*SL	0.28 + 0.025*SL
	t_{PHL}	0.18	0.09 + 0.048*SL	0.11 + 0.038*SL	0.12 + 0.037*SL
	t_R	0.31	0.26 + 0.027*SL	0.19 + 0.050*SL	0.16 + 0.053*SL
	t_F	0.34	0.21 + 0.068*SL	0.20 + 0.069*SL	0.17 + 0.073*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.53	0.53 + 0.000*SL	0.53 + 0.000*SL	0.53 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2TCSD2

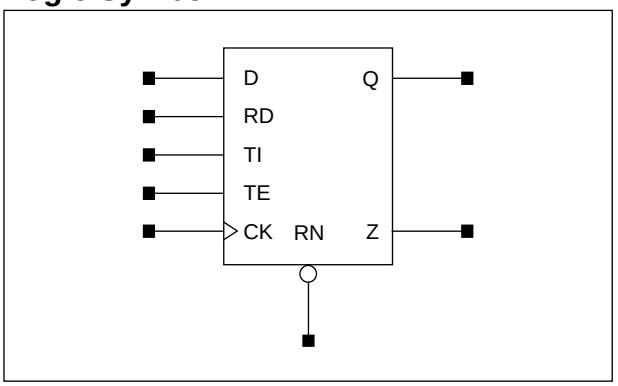
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.93	0.86 + 0.032*SL	0.88 + 0.028*SL	0.90 + 0.025*SL
	t_{PHL}	0.90	0.84 + 0.026*SL	0.86 + 0.019*SL	0.91 + 0.015*SL
	t_R	0.32	0.22 + 0.055*SL	0.22 + 0.054*SL	0.23 + 0.053*SL
	t_F	0.24	0.19 + 0.026*SL	0.20 + 0.022*SL	0.22 + 0.020*SL
SCK to Q	t_{PLH}	1.10	1.03 + 0.032*SL	1.05 + 0.028*SL	1.07 + 0.025*SL
	t_{PHL}	0.82	0.77 + 0.027*SL	0.79 + 0.020*SL	0.84 + 0.015*SL
	t_R	0.34	0.23 + 0.055*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.25	0.20 + 0.025*SL	0.21 + 0.022*SL	0.23 + 0.020*SL
RN to Q	t_{PHL}	0.56	0.51 + 0.027*SL	0.53 + 0.019*SL	0.58 + 0.014*SL
	t_F	0.26	0.20 + 0.026*SL	0.22 + 0.021*SL	0.24 + 0.019*SL
CK to Z	t_{PLH}	1.31	1.19 + 0.060*SL	1.22 + 0.049*SL	1.29 + 0.043*SL
	t_{PHL}	1.19	1.11 + 0.042*SL	1.13 + 0.033*SL	1.19 + 0.028*SL
	t_R	0.24	0.19 + 0.027*SL	0.19 + 0.027*SL	0.19 + 0.027*SL
	t_F	0.46	0.36 + 0.049*SL	0.37 + 0.046*SL	0.39 + 0.044*SL
SCK to Z	t_{PLH}	1.48	1.36 + 0.061*SL	1.39 + 0.049*SL	1.46 + 0.043*SL
	t_{PHL}	1.12	1.04 + 0.042*SL	1.06 + 0.033*SL	1.12 + 0.028*SL
	t_R	0.25	0.19 + 0.026*SL	0.19 + 0.027*SL	0.19 + 0.027*SL
	t_F	0.46	0.36 + 0.050*SL	0.37 + 0.046*SL	0.39 + 0.044*SL
RN to Z	t_{PHL}	0.86	0.78 + 0.041*SL	0.80 + 0.033*SL	0.86 + 0.028*SL
	t_F	0.45	0.35 + 0.050*SL	0.37 + 0.045*SL	0.38 + 0.043*SL
RD to Z	t_{PLH}	0.35	0.31 + 0.021*SL	0.33 + 0.016*SL	0.35 + 0.013*SL
	t_{PHL}	0.11	0.06 + 0.029*SL	0.08 + 0.022*SL	0.11 + 0.019*SL
	t_R	0.30	0.30 + 0.000*SL	0.24 + 0.023*SL	0.22 + 0.025*SL
	t_F	0.25	0.18 + 0.039*SL	0.19 + 0.034*SL	0.18 + 0.035*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.70	0.70 + 0.000*SL	0.70 + 0.000*SL	0.70 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FD2TS/FD2TSD2

D Flip-Flop with Reset, Scan, Tri-State Output, 1X/2X Drive

Logic Symbol



Truth Table

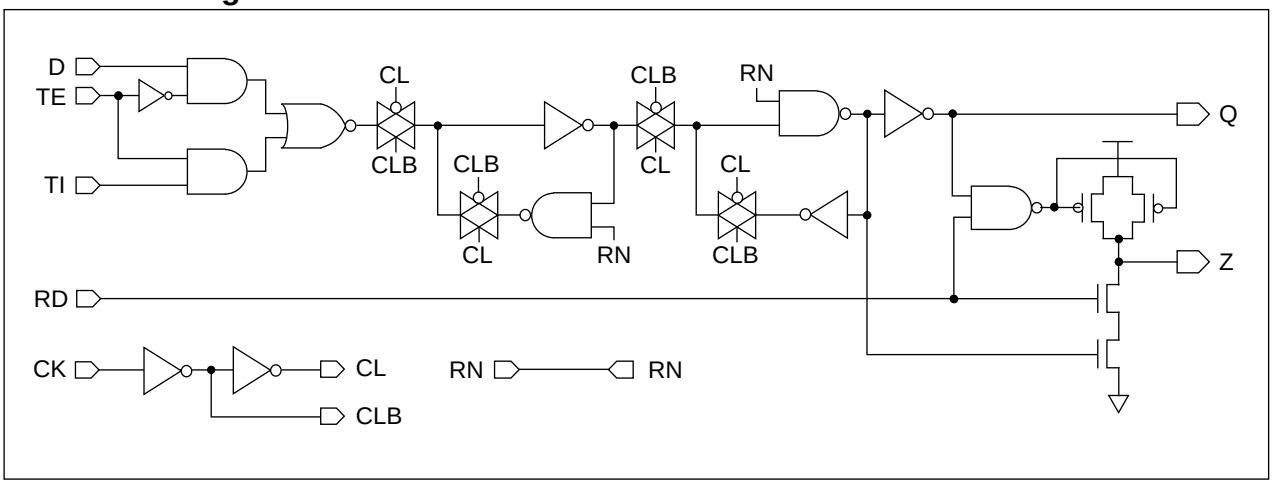
D	RD	TI	TE	CK	RN	Q (n+1)	Z (n+1)
0	1	x	0	↑	1	0	0
1	1	x	0	↑	1	1	1
x	1	0	1	↑	1	0	0
x	1	1	1	↑	1	1	1
x	1	x	x	x	0	0	0
x	0	x	x	x	1	x	Hi-Z
x	1	x	x	↓	1	Q (n)	Z (n)

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)												Output Load (SL)		Gate Count	
KG80															
FD2TS						*FD2TSD2*						*FD2TS*	*FD2TSD2*	*FD2TS*	*FD2TSD2*
D	RD	TI	TE	CK	RN	D	RD	TI	TE	CK	RN	Z	Z		
0.9	1.3	0.8	1.7	0.9	1.7	0.9	2.2	0.8	1.7	0.9	1.7	0.7	1.2	12.0	15.0
KGM80															
FD2TS						*FD2TSD2*						*FD2TS*	*FD2TSD2*	*FD2TS*	*FD2TSD2*
D	RD	TI	TE	CK	RN	D	RD	TI	TE	CK	RN	Z	Z		
1.0	1.7	0.9	2.0	1.0	2.0	1.0	2.6	0.9	2.0	1.0	2.0	0.9	1.6	12.0	15.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD2TS	FD2TSD2	FD2TS	FD2TSD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.64	0.99	1.05
Input Setup Time (D to CK)	t_{SU}	0.47	0.47	0.86	0.86
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.50	0.50	0.93	0.93
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.15	0.15	0.33	0.33
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.63	0.63

FD2TS/FD2TSD2

D Flip-Flop with Reset, Scan, Tri-State Output, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD2TS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.66	0.57 + 0.045*SL	0.58 + 0.042*SL	0.58 + 0.041*SL
	t_{PHL}	0.62	0.55 + 0.032*SL	0.57 + 0.026*SL	0.58 + 0.024*SL
	t_R	0.37	0.20 + 0.084*SL	0.19 + 0.087*SL	0.18 + 0.089*SL
	t_F	0.23	0.15 + 0.041*SL	0.16 + 0.039*SL	0.15 + 0.041*SL
RN to Q	t_{PHL}	0.41	0.34 + 0.033*SL	0.36 + 0.027*SL	0.38 + 0.023*SL
	t_F	0.25	0.17 + 0.040*SL	0.17 + 0.038*SL	0.16 + 0.039*SL
CK to Z	t_{PLH}	0.89	0.74 + 0.075*SL	0.77 + 0.066*SL	0.79 + 0.063*SL
	t_{PHL}	0.84	0.72 + 0.062*SL	0.74 + 0.054*SL	0.76 + 0.051*SL
	t_R	0.20	0.11 + 0.044*SL	0.11 + 0.045*SL	0.10 + 0.046*SL
	t_F	0.44	0.28 + 0.082*SL	0.28 + 0.083*SL	0.28 + 0.083*SL
RN to Z	t_{PHL}	0.63	0.51 + 0.063*SL	0.53 + 0.053*SL	0.55 + 0.051*SL
	t_F	0.44	0.28 + 0.082*SL	0.28 + 0.082*SL	0.28 + 0.082*SL
RD to Z	t_{PLH}	0.22	0.16 + 0.030*SL	0.18 + 0.023*SL	0.20 + 0.021*SL
	t_{PHL}	0.12	0.01 + 0.054*SL	0.05 + 0.036*SL	0.05 + 0.036*SL
	t_R	0.22	0.16 + 0.031*SL	0.14 + 0.040*SL	0.12 + 0.043*SL
	t_F	0.29	0.16 + 0.066*SL	0.17 + 0.062*SL	0.16 + 0.064*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.36	0.36 + 0.001*SL	0.36 + 0.000*SL	0.36 + 0.000*SL

KG80 FD2TSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.67	0.62 + 0.025*SL	0.63 + 0.023*SL	0.64 + 0.021*SL
	t_{PHL}	0.63	0.59 + 0.022*SL	0.60 + 0.018*SL	0.62 + 0.015*SL
	t_R	0.26	0.17 + 0.043*SL	0.17 + 0.042*SL	0.17 + 0.043*SL
	t_F	0.20	0.16 + 0.023*SL	0.16 + 0.021*SL	0.17 + 0.020*SL
RN to Q	t_{PHL}	0.42	0.37 + 0.023*SL	0.38 + 0.018*SL	0.41 + 0.014*SL
	t_F	0.22	0.17 + 0.022*SL	0.18 + 0.018*SL	0.18 + 0.018*SL
CK to Z	t_{PLH}	0.93	0.84 + 0.045*SL	0.85 + 0.039*SL	0.88 + 0.035*SL
	t_{PHL}	0.88	0.80 + 0.039*SL	0.82 + 0.033*SL	0.85 + 0.029*SL
	t_R	0.18	0.13 + 0.024*SL	0.14 + 0.023*SL	0.14 + 0.022*SL
	t_F	0.42	0.33 + 0.043*SL	0.34 + 0.041*SL	0.34 + 0.041*SL
RN to Z	t_{PHL}	0.66	0.59 + 0.038*SL	0.60 + 0.032*SL	0.63 + 0.028*SL
	t_F	0.41	0.33 + 0.043*SL	0.33 + 0.040*SL	0.33 + 0.041*SL
RD to Z	t_{PLH}	0.25	0.21 + 0.021*SL	0.22 + 0.016*SL	0.25 + 0.013*SL
	t_{PHL}	0.06	-0.01 + 0.033*SL	0.01 + 0.024*SL	0.05 + 0.018*SL
	t_R	0.23	0.21 + 0.012*SL	0.20 + 0.017*SL	0.18 + 0.019*SL
	t_F	0.22	0.14 + 0.039*SL	0.16 + 0.031*SL	0.16 + 0.031*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.51	0.51 + 0.000*SL	0.51 + 0.000*SL	0.51 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD2TS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.92	0.81 + 0.054*SL	0.82 + 0.050*SL	0.83 + 0.050*SL
	t_{PHL}	0.87	0.80 + 0.036*SL	0.82 + 0.027*SL	0.86 + 0.024*SL
	t_R	0.49	0.28 + 0.103*SL	0.27 + 0.106*SL	0.25 + 0.108*SL
	t_F	0.28	0.19 + 0.044*SL	0.20 + 0.041*SL	0.20 + 0.041*SL
RN to Q	t_{PHL}	0.54	0.47 + 0.037*SL	0.49 + 0.028*SL	0.54 + 0.024*SL
	t_F	0.30	0.21 + 0.044*SL	0.22 + 0.040*SL	0.21 + 0.041*SL
CK to Z	t_{PLH}	1.26	1.08 + 0.092*SL	1.11 + 0.080*SL	1.16 + 0.075*SL
	t_{PHL}	1.14	1.00 + 0.068*SL	1.04 + 0.055*SL	1.08 + 0.051*SL
	t_R	0.25	0.15 + 0.053*SL	0.15 + 0.053*SL	0.13 + 0.055*SL
	t_F	0.53	0.35 + 0.088*SL	0.36 + 0.086*SL	0.36 + 0.086*SL
RN to Z	t_{PHL}	0.81	0.67 + 0.068*SL	0.71 + 0.055*SL	0.75 + 0.051*SL
	t_F	0.53	0.36 + 0.087*SL	0.36 + 0.086*SL	0.37 + 0.086*SL
RD to Z	t_{PLH}	0.31	0.25 + 0.033*SL	0.26 + 0.026*SL	0.28 + 0.025*SL
	t_{PHL}	0.16	0.05 + 0.052*SL	0.09 + 0.038*SL	0.11 + 0.037*SL
	t_R	0.29	0.23 + 0.029*SL	0.17 + 0.050*SL	0.14 + 0.053*SL
	t_F	0.32	0.18 + 0.069*SL	0.18 + 0.069*SL	0.14 + 0.073*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.47	0.47 + 0.000*SL	0.47 + 0.000*SL	0.47 + 0.000*SL

KGM80 FD2TSD2

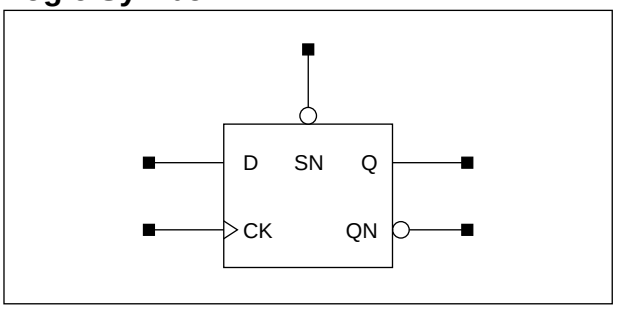
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.93	0.86 + 0.032*SL	0.87 + 0.028*SL	0.90 + 0.025*SL
	t_{PHL}	0.90	0.85 + 0.025*SL	0.87 + 0.019*SL	0.91 + 0.015*SL
	t_R	0.33	0.22 + 0.053*SL	0.23 + 0.052*SL	0.22 + 0.052*SL
	t_F	0.24	0.19 + 0.026*SL	0.20 + 0.022*SL	0.22 + 0.020*SL
RN to Q	t_{PHL}	0.57	0.51 + 0.027*SL	0.53 + 0.019*SL	0.59 + 0.014*SL
	t_F	0.26	0.20 + 0.027*SL	0.22 + 0.020*SL	0.24 + 0.019*SL
CK to Z	t_{PLH}	1.31	1.19 + 0.057*SL	1.22 + 0.047*SL	1.28 + 0.042*SL
	t_{PHL}	1.21	1.12 + 0.044*SL	1.14 + 0.035*SL	1.21 + 0.029*SL
	t_R	0.23	0.18 + 0.027*SL	0.18 + 0.027*SL	0.18 + 0.026*SL
	t_F	0.50	0.40 + 0.048*SL	0.41 + 0.045*SL	0.42 + 0.044*SL
RN to Z	t_{PHL}	0.87	0.79 + 0.043*SL	0.81 + 0.034*SL	0.87 + 0.028*SL
	t_F	0.49	0.40 + 0.048*SL	0.41 + 0.044*SL	0.42 + 0.043*SL
RD to Z	t_{PLH}	0.36	0.32 + 0.023*SL	0.34 + 0.016*SL	0.37 + 0.013*SL
	t_{PHL}	0.10	0.04 + 0.031*SL	0.06 + 0.022*SL	0.10 + 0.018*SL
	t_R	0.31	0.30 + 0.002*SL	0.25 + 0.021*SL	0.21 + 0.025*SL
	t_F	0.24	0.16 + 0.041*SL	0.18 + 0.034*SL	0.16 + 0.035*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.69	0.69 + 0.000*SL	0.69 + 0.000*SL	0.69 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FD3/FD3D2

D Flip-Flop with Set, 1X/2X Drive

Logic Symbol



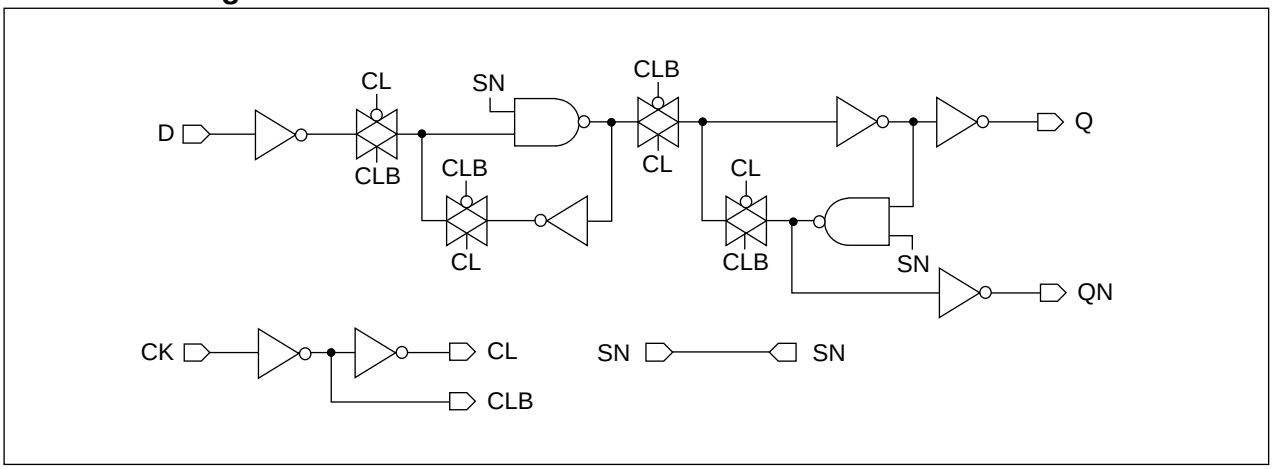
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FD3			*FD3D2*			*FD3*	*FD3D2*
D	CK	SN	D	CK	SN		
0.9	0.9	1.6	0.9	0.9	1.6	8.0	9.0
KGM80							
FD3			*FD3D2*			*FD3*	*FD3D2*
D	CK	SN	D	CK	SN		
1.0	1.0	1.9	1.0	1.0	1.9	8.0	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD3	FD3D2	FD3	FD3D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.42	0.42	0.74	0.74
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.56	0.50 + 0.031*SL	0.51 + 0.026*SL	0.52 + 0.024*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to Q	t_{PLH}	0.59	0.50 + 0.041*SL	0.50 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to QN	t_{PLH}	0.76	0.68 + 0.042*SL	0.68 + 0.041*SL	0.68 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.026*SL	0.57 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to QN	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.09 + 0.040*SL

KG80 FD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.49	0.45 + 0.023*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.020*SL	0.53 + 0.015*SL	0.54 + 0.013*SL
	t_R	0.17	0.09 + 0.037*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SN to Q	t_{PLH}	0.57	0.53 + 0.023*SL	0.53 + 0.021*SL	0.53 + 0.021*SL
	t_R	0.17	0.09 + 0.040*SL	0.09 + 0.042*SL	0.07 + 0.044*SL
CK to QN	t_{PLH}	0.81	0.76 + 0.022*SL	0.77 + 0.020*SL	0.77 + 0.020*SL
	t_{PHL}	0.64	0.60 + 0.019*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.11 + 0.019*SL
SN to QN	t_{PHL}	0.33	0.29 + 0.022*SL	0.30 + 0.016*SL	0.32 + 0.013*SL
	t_F	0.16	0.11 + 0.021*SL	0.12 + 0.019*SL	0.12 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD3/FD3D2

D Flip-Flop with Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD3

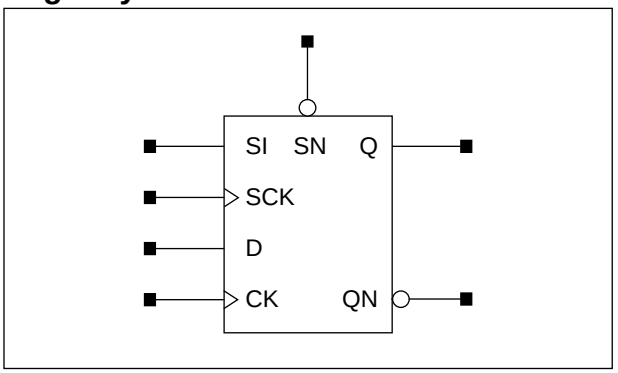
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.60 + 0.051*SL	0.61 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.78	0.71 + 0.034*SL	0.74 + 0.026*SL	0.76 + 0.024*SL
	t_R	0.34	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SN to Q	t_{PLH}	0.82	0.72 + 0.051*SL	0.72 + 0.050*SL	0.72 + 0.050*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
CK to QN	t_{PLH}	1.08	0.97 + 0.052*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.85	0.78 + 0.034*SL	0.81 + 0.026*SL	0.84 + 0.024*SL
	t_R	0.36	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to QN	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

KGM80 FD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.62 + 0.028*SL	0.63 + 0.025*SL	0.63 + 0.025*SL
	t_{PHL}	0.79	0.74 + 0.024*SL	0.76 + 0.016*SL	0.80 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
SN to Q	t_{PLH}	0.80	0.75 + 0.028*SL	0.75 + 0.025*SL	0.76 + 0.025*SL
	t_R	0.22	0.12 + 0.050*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
CK to QN	t_{PLH}	1.14	1.08 + 0.029*SL	1.09 + 0.025*SL	1.10 + 0.025*SL
	t_{PHL}	0.90	0.86 + 0.022*SL	0.88 + 0.016*SL	0.91 + 0.013*SL
	t_R	0.24	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.026*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
SN to QN	t_{PHL}	0.44	0.39 + 0.025*SL	0.41 + 0.017*SL	0.45 + 0.014*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.16 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



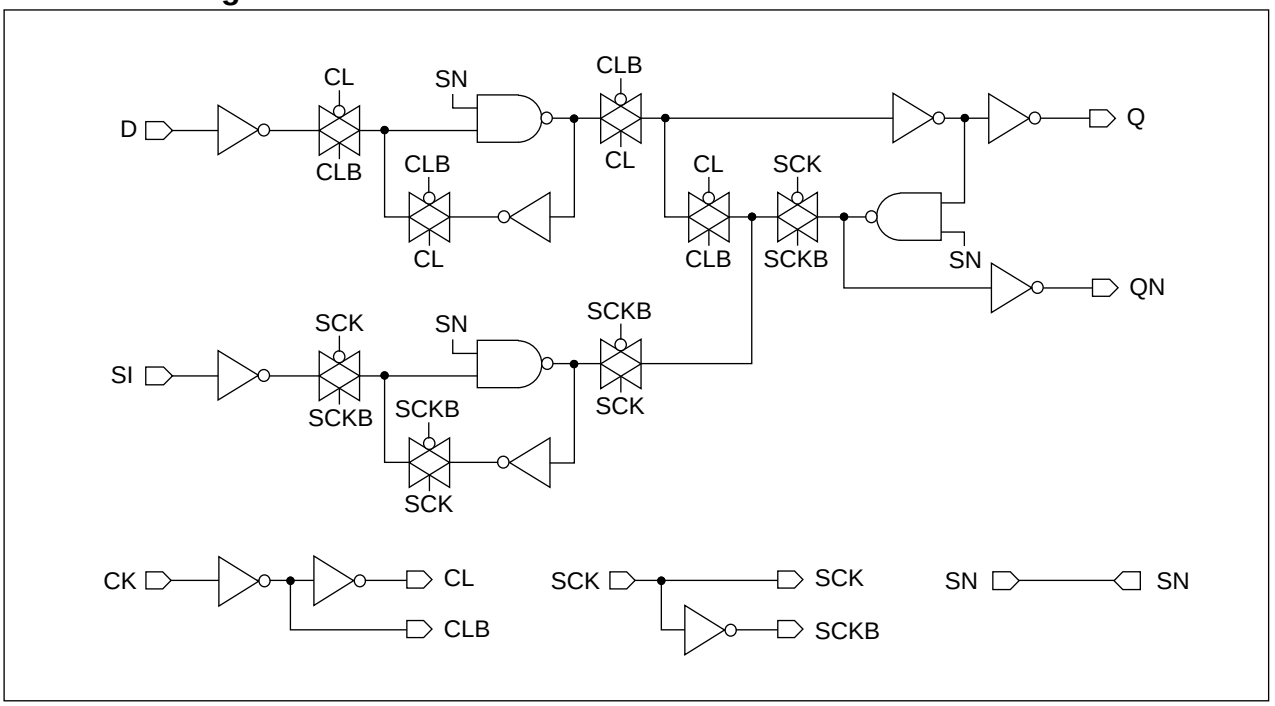
Truth Table

SI	SCK	D	CK	SN	Q (n+1)	QN (n+1)
x	0	0	↑	1	0	1
x	0	1	↑	1	1	0
0	↑	x	0	1	0	1
1	↑	x	0	1	1	0
x	x	x	x	0	1	0

Cell Data

Input Load (SL)										Gate Count	
KG80											
FD3CS					*FD3CSD2*					*FD3CS*	*FD3CSD2*
SI	SCK	D	CK	SN	SI	SCK	D	CK	SN		
0.8	2.1	0.9	0.9	2.7	0.8	2.1	0.9	0.9	2.7	12.0	13.0
KGM80											
FD3CS					*FD3CSD2*					*FD3CS*	*FD3CSD2*
SI	SCK	D	CK	SN	SI	SCK	D	CK	SN		
1.0	2.8	1.0	1.0	3.1	1.0	2.8	1.0	1.0	3.1	12.0	13.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD3CS	FD3CSD2	FD3CS	FD3CSD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SCK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (SCK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.67	0.69	1.11	1.14
Input Setup Time (D to CK)	t_{SU}	0.42	0.42	0.74	0.74
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.61	0.61	1.02	1.02
Input Hold Time (SI to SCK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (SN to CK)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41
Recovery Time (SN to SCK)	t_{RC}	0.31	0.31	0.55	0.55
Input Hold Time (SN to SCK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD3CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.51	0.43 + 0.041*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.56	0.50 + 0.030*SL	0.51 + 0.025*SL	0.52 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SCK to Q	t_{PLH}	0.54	0.46 + 0.043*SL	0.46 + 0.041*SL	0.46 + 0.041*SL
	t_{PHL}	0.53	0.46 + 0.031*SL	0.48 + 0.026*SL	0.49 + 0.024*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
SN to Q	t_{PLH}	0.59	0.51 + 0.041*SL	0.51 + 0.041*SL	0.51 + 0.042*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to QN	t_{PLH}	0.85	0.76 + 0.045*SL	0.77 + 0.042*SL	0.77 + 0.041*SL
	t_{PHL}	0.68	0.61 + 0.036*SL	0.63 + 0.028*SL	0.65 + 0.025*SL
	t_R	0.32	0.15 + 0.085*SL	0.14 + 0.086*SL	0.12 + 0.089*SL
	t_F	0.21	0.13 + 0.042*SL	0.13 + 0.040*SL	0.13 + 0.041*SL
SCK to QN	t_{PLH}	0.72	0.64 + 0.042*SL	0.64 + 0.041*SL	0.64 + 0.041*SL
	t_{PHL}	0.63	0.57 + 0.030*SL	0.58 + 0.025*SL	0.59 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SN to QN	t_{PHL}	0.41	0.34 + 0.037*SL	0.36 + 0.027*SL	0.38 + 0.024*SL
	t_F	0.22	0.14 + 0.039*SL	0.15 + 0.037*SL	0.13 + 0.039*SL

KG80 FD3CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.50	0.45 + 0.023*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.021*SL	0.53 + 0.015*SL	0.55 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SCK to Q	t_{PLH}	0.54	0.49 + 0.023*SL	0.50 + 0.021*SL	0.50 + 0.021*SL
	t_{PHL}	0.53	0.49 + 0.021*SL	0.50 + 0.016*SL	0.52 + 0.013*SL
	t_R	0.18	0.11 + 0.038*SL	0.10 + 0.042*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
SN to Q	t_{PLH}	0.58	0.53 + 0.023*SL	0.54 + 0.021*SL	0.54 + 0.020*SL
	t_R	0.17	0.09 + 0.042*SL	0.09 + 0.042*SL	0.08 + 0.044*SL
CK to QN	t_{PLH}	0.91	0.86 + 0.024*SL	0.86 + 0.021*SL	0.87 + 0.021*SL
	t_{PHL}	0.72	0.68 + 0.021*SL	0.69 + 0.017*SL	0.71 + 0.014*SL
	t_R	0.24	0.16 + 0.041*SL	0.16 + 0.042*SL	0.15 + 0.043*SL
	t_F	0.19	0.14 + 0.025*SL	0.15 + 0.020*SL	0.15 + 0.020*SL
SCK to QN	t_{PLH}	0.78	0.74 + 0.021*SL	0.74 + 0.020*SL	0.74 + 0.020*SL
	t_{PHL}	0.68	0.65 + 0.017*SL	0.65 + 0.014*SL	0.66 + 0.013*SL
	t_R	0.21	0.12 + 0.043*SL	0.12 + 0.043*SL	0.12 + 0.044*SL
	t_F	0.15	0.11 + 0.020*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
SN to QN	t_{PHL}	0.41	0.36 + 0.023*SL	0.38 + 0.017*SL	0.40 + 0.014*SL
	t_F	0.20	0.16 + 0.021*SL	0.16 + 0.019*SL	0.17 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

FD3CS/FD3CSD2

D Flip-Flop with Set, Scan Clock, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD3CS

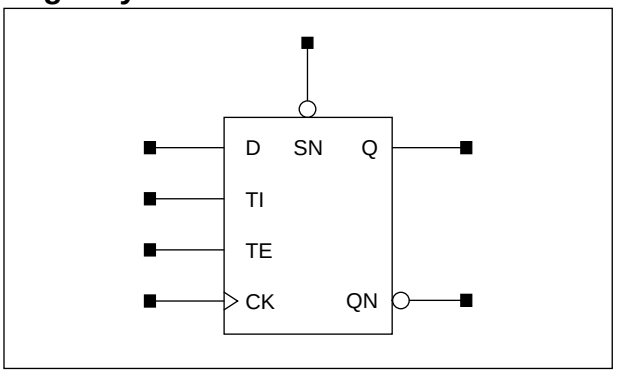
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.78	0.71 + 0.034*SL	0.74 + 0.026*SL	0.76 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.042*SL	0.11 + 0.043*SL
SCK to Q	t_{PLH}	0.80	0.69 + 0.052*SL	0.70 + 0.050*SL	0.70 + 0.050*SL
	t_{PHL}	0.73	0.66 + 0.036*SL	0.69 + 0.027*SL	0.72 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.042*SL
SN to Q	t_{PLH}	0.82	0.72 + 0.051*SL	0.72 + 0.050*SL	0.73 + 0.050*SL
	t_R	0.35	0.15 + 0.103*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
CK to QN	t_{PLH}	1.19	1.08 + 0.059*SL	1.10 + 0.051*SL	1.11 + 0.050*SL
	t_{PHL}	0.97	0.89 + 0.040*SL	0.92 + 0.030*SL	0.96 + 0.025*SL
	t_R	0.42	0.21 + 0.104*SL	0.21 + 0.104*SL	0.18 + 0.107*SL
	t_F	0.25	0.16 + 0.048*SL	0.17 + 0.043*SL	0.18 + 0.042*SL
SCK to QN	t_{PLH}	1.01	0.91 + 0.051*SL	0.92 + 0.050*SL	0.92 + 0.050*SL
	t_{PHL}	0.93	0.86 + 0.033*SL	0.88 + 0.026*SL	0.91 + 0.023*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
SN to QN	t_{PHL}	0.55	0.47 + 0.042*SL	0.50 + 0.029*SL	0.56 + 0.024*SL
	t_F	0.26	0.17 + 0.044*SL	0.19 + 0.039*SL	0.17 + 0.041*SL

KGM80 FD3CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.80	0.75 + 0.023*SL	0.77 + 0.016*SL	0.80 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.021*SL
SCK to Q	t_{PLH}	0.80	0.74 + 0.029*SL	0.75 + 0.025*SL	0.75 + 0.025*SL
	t_{PHL}	0.75	0.71 + 0.024*SL	0.73 + 0.017*SL	0.76 + 0.014*SL
	t_R	0.24	0.14 + 0.050*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
SN to Q	t_{PLH}	0.81	0.75 + 0.028*SL	0.76 + 0.025*SL	0.77 + 0.025*SL
	t_R	0.23	0.13 + 0.050*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
CK to QN	t_{PLH}	1.27	1.21 + 0.031*SL	1.22 + 0.027*SL	1.24 + 0.025*SL
	t_{PHL}	1.03	0.98 + 0.025*SL	1.00 + 0.018*SL	1.04 + 0.015*SL
	t_R	0.32	0.21 + 0.054*SL	0.22 + 0.052*SL	0.22 + 0.052*SL
	t_F	0.23	0.18 + 0.026*SL	0.19 + 0.023*SL	0.20 + 0.021*SL
SCK to QN	t_{PLH}	1.11	1.06 + 0.027*SL	1.06 + 0.024*SL	1.06 + 0.025*SL
	t_{PHL}	1.02	0.98 + 0.019*SL	1.00 + 0.015*SL	1.02 + 0.013*SL
	t_R	0.28	0.17 + 0.053*SL	0.17 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
SN to QN	t_{PHL}	0.56	0.51 + 0.027*SL	0.53 + 0.018*SL	0.58 + 0.014*SL
	t_F	0.24	0.19 + 0.025*SL	0.20 + 0.020*SL	0.22 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Logic Symbol



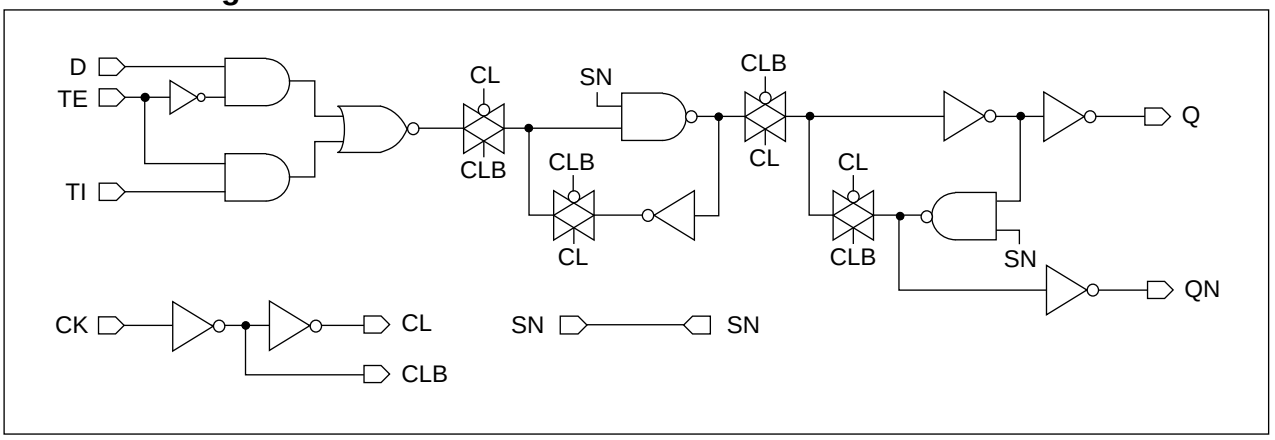
Truth Table

D	TI	TE	CK	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0
x	x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
KG80											
FD3S					*FD3SD2*					*FD3S*	*FD3S D2*
D	TI	TE	CK	SN	D	TI	TE	CK	SN		
0.5	0.8	1.7	0.9	1.7	0.5	0.8	1.7	0.9	1.7	10.0	11.0
KGM80											
FD3S					*FD3SD2*					*FD3S*	*FD3S D2*
D	TI	TE	CK	SN	D	TI	TE	CK	SN		
1.0	1.0	2.1	1.0	1.9	1.0	1.0	2.1	1.0	1.9	10.0	11.0

Schematic Diagram



FD3S/FD3SD2

D Flip-Flop with Set, Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD3S	FD3SD2	FD3S	FD3SD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.53	0.53	0.93	0.93
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.58	0.58	1.02	1.02
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.53	0.53	0.96	0.96
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD3S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.56	0.50 + 0.031*SL	0.51 + 0.026*SL	0.52 + 0.024*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to Q	t_{PLH}	0.59	0.51 + 0.041*SL	0.51 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to QN	t_{PLH}	0.76	0.68 + 0.042*SL	0.68 + 0.041*SL	0.68 + 0.041*SL
	t_{PHL}	0.60	0.54 + 0.031*SL	0.55 + 0.026*SL	0.57 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.08 + 0.041*SL	0.08 + 0.041*SL
SN to QN	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.09 + 0.041*SL

KG80 FD3SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.49	0.45 + 0.023*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.021*SL	0.53 + 0.015*SL	0.55 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.11 + 0.019*SL	0.10 + 0.020*SL
SN to Q	t_{PLH}	0.58	0.53 + 0.023*SL	0.53 + 0.021*SL	0.54 + 0.020*SL
	t_R	0.17	0.09 + 0.043*SL	0.09 + 0.042*SL	0.07 + 0.044*SL
CK to QN	t_{PLH}	0.81	0.76 + 0.022*SL	0.77 + 0.020*SL	0.76 + 0.020*SL
	t_{PHL}	0.64	0.60 + 0.019*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SN to QN	t_{PHL}	0.33	0.29 + 0.021*SL	0.30 + 0.016*SL	0.32 + 0.013*SL
	t_F	0.16	0.11 + 0.022*SL	0.12 + 0.019*SL	0.12 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD3S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.60 + 0.051*SL	0.61 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.78	0.71 + 0.034*SL	0.73 + 0.026*SL	0.77 + 0.024*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to Q	t_{PLH}	0.82	0.72 + 0.051*SL	0.72 + 0.050*SL	0.72 + 0.050*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
CK to QN	t_{PLH}	1.08	0.97 + 0.052*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.85	0.79 + 0.034*SL	0.81 + 0.026*SL	0.84 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to QN	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

KGM80 FD3SD2

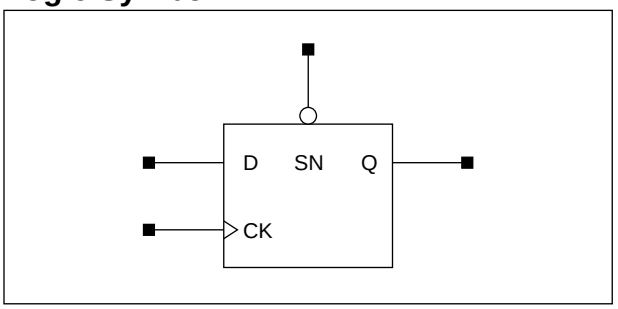
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.62 + 0.028*SL	0.63 + 0.025*SL	0.63 + 0.025*SL
	t_{PHL}	0.79	0.74 + 0.024*SL	0.76 + 0.017*SL	0.80 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
SN to Q	t_{PLH}	0.81	0.75 + 0.028*SL	0.76 + 0.025*SL	0.76 + 0.025*SL
	t_R	0.22	0.12 + 0.051*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
CK to QN	t_{PLH}	1.14	1.08 + 0.029*SL	1.09 + 0.025*SL	1.10 + 0.025*SL
	t_{PHL}	0.91	0.86 + 0.023*SL	0.88 + 0.016*SL	0.91 + 0.013*SL
	t_R	0.24	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.021*SL
SN to QN	t_{PHL}	0.44	0.39 + 0.025*SL	0.41 + 0.017*SL	0.45 + 0.014*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.16 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FD3Q/FD3QD2

D Flip-Flop with Set, Q Output Only, 1X/2X Drive

Logic Symbol



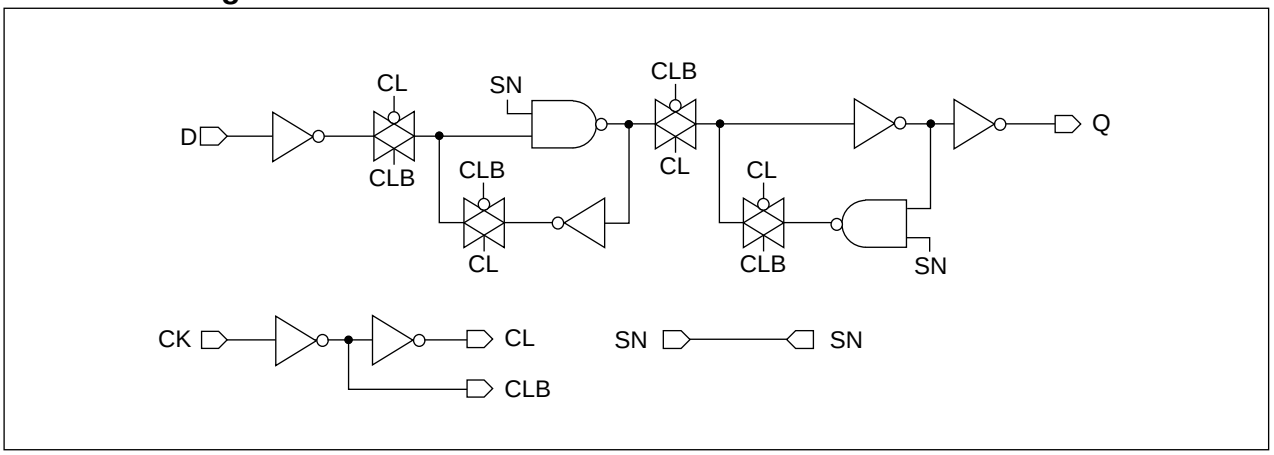
Truth Table

D	CK	SN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	1
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FD3Q			*FD3QD2*			*FD3Q*	*FD3QD2*
D	CK	SN	D	CK	SN		
0.8	0.8	1.4	0.8	0.8	1.4	7.0	8.0
KGM80							
FD3Q			*FD3QD2*			*FD3Q*	*FD3QD2*
D	CK	SN	D	CK	SN		
0.9	0.9	1.7	0.9	0.9	1.7	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD3Q	FD3QD2	FD3Q	FD3QD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	1.02	1.02
Input Setup Time (D to CK)	t_{SU}	0.15	0.15	0.80	0.80
Input Hold Time (D to CK)	t_{HD}	0.45	0.45	0.33	0.33
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD3Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.49	0.40 + 0.043*SL	0.41 + 0.042*SL	0.41 + 0.042*SL
	t_{PHL}	0.52	0.46 + 0.030*SL	0.47 + 0.026*SL	0.49 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.17	0.08 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SN to Q	t_{PLH}	0.59	0.50 + 0.042*SL	0.50 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.083*SL	0.08 + 0.089*SL	0.07 + 0.091*SL

KG80 FD3QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.48	0.43 + 0.022*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.53	0.49 + 0.018*SL	0.50 + 0.015*SL	0.51 + 0.013*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SN to Q	t_{PLH}	0.58	0.54 + 0.022*SL	0.54 + 0.020*SL	0.54 + 0.021*SL
	t_R	0.18	0.10 + 0.040*SL	0.10 + 0.043*SL	0.09 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD3Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.59 + 0.051*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.74	0.67 + 0.034*SL	0.69 + 0.026*SL	0.72 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SN to Q	t_{PLH}	0.83	0.73 + 0.051*SL	0.73 + 0.050*SL	0.73 + 0.050*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL

KGM80 FD3QD2

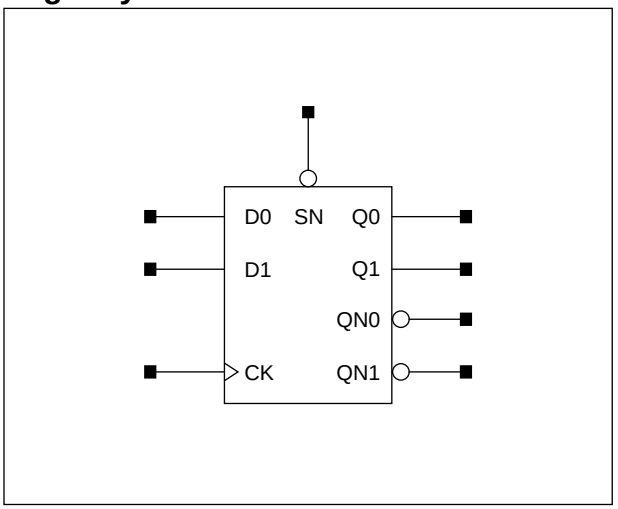
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.63 + 0.027*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.76	0.71 + 0.021*SL	0.73 + 0.016*SL	0.76 + 0.013*SL
	t_R	0.24	0.14 + 0.052*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.18	0.13 + 0.023*SL	0.13 + 0.021*SL	0.14 + 0.021*SL
SN to Q	t_{PLH}	0.83	0.77 + 0.026*SL	0.78 + 0.025*SL	0.78 + 0.025*SL
	t_R	0.25	0.15 + 0.050*SL	0.14 + 0.052*SL	0.13 + 0.054*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

FD3X2

2-Bit D Flip-Flop with Set

Logic Symbol



Truth Table

Dn	CK	SN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
KG80			
Dn	CK	SN	
1.0	0.9	3.4	15.0
KGM80			
Dn	CK	SN	
1.0	1.0	4.2	15.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.67	1.05
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.99
Input Setup Time (D0 to CK)	t_{SU}	0.37	0.64
Input Hold Time (D0 to CK)	t_{HD}	0.15	0.33
Input Setup Time (D1 to CK)	t_{SU}	0.37	0.64
Input Hold Time (D1 to CK)	t_{HD}	0.15	0.33
Recovery Time (SN)	t_{RC}	0.15	0.33
Input Hold Time (SN to CK)	t_{HD}	0.20	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD3X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.57	0.48 + 0.042*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.67	0.60 + 0.031*SL	0.62 + 0.026*SL	0.63 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to Q0	t_{PLH}	0.59	0.50 + 0.042*SL	0.50 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to Q1	t_{PLH}	0.57	0.48 + 0.042*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.67	0.60 + 0.031*SL	0.62 + 0.026*SL	0.63 + 0.024*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.090*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to Q1	t_{PLH}	0.59	0.50 + 0.042*SL	0.50 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to QN0	t_{PLH}	0.87	0.79 + 0.042*SL	0.79 + 0.041*SL	0.79 + 0.041*SL
	t_{PHL}	0.66	0.60 + 0.031*SL	0.61 + 0.025*SL	0.62 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SN to QN0	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CK to QN1	t_{PLH}	0.87	0.79 + 0.042*SL	0.79 + 0.041*SL	0.79 + 0.041*SL
	t_{PHL}	0.66	0.60 + 0.031*SL	0.61 + 0.025*SL	0.62 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to QN1	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD3X2

2-Bit D Flip-Flop with Set

Switching Characteristics

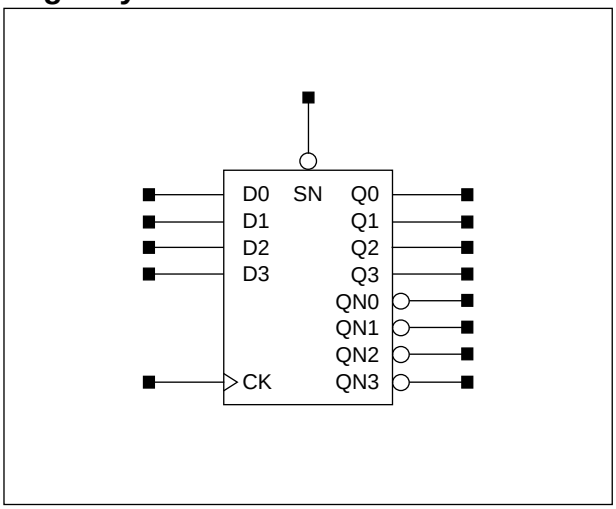
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD3X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.77	0.67 + 0.051*SL	0.67 + 0.050*SL	0.68 + 0.050*SL
	t_{PHL}	0.93	0.86 + 0.034*SL	0.88 + 0.026*SL	0.91 + 0.024*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SN to Q0	t_{PLH}	0.81	0.71 + 0.051*SL	0.71 + 0.050*SL	0.72 + 0.050*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
CK to Q1	t_{PLH}	0.78	0.67 + 0.051*SL	0.68 + 0.050*SL	0.68 + 0.050*SL
	t_{PHL}	0.93	0.86 + 0.034*SL	0.88 + 0.026*SL	0.91 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SN to Q1	t_{PLH}	0.81	0.71 + 0.051*SL	0.71 + 0.050*SL	0.72 + 0.050*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
CK to QN0	t_{PLH}	1.23	1.12 + 0.052*SL	1.13 + 0.050*SL	1.13 + 0.050*SL
	t_{PHL}	0.92	0.85 + 0.034*SL	0.88 + 0.026*SL	0.91 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to QN0	t_{PHL}	0.44	0.37 + 0.037*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.046*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN1	t_{PLH}	1.23	1.12 + 0.052*SL	1.13 + 0.050*SL	1.13 + 0.050*SL
	t_{PHL}	0.92	0.86 + 0.034*SL	0.88 + 0.026*SL	0.91 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to QN1	t_{PHL}	0.44	0.37 + 0.037*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.046*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

Dn	CK	SN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
KG80			
Dn	CK	SN	
1.0	0.9	7.2	30.0
KGM80			
Dn	CK	SN	
1.0	1.0	8.6	30.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.83	1.33
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.99
Input Setup Time (D0 to CK)	t_{SU}	0.23	0.49
Input Hold Time (D0 to CK)	t_{HD}	0.23	0.39
Input Setup Time (D1 to CK)	t_{SU}	0.23	0.49
Input Hold Time (D1 to CK)	t_{HD}	0.23	0.39
Input Setup Time (D2 to CK)	t_{SU}	0.23	0.49
Input Hold Time (D2 to CK)	t_{HD}	0.23	0.39
Input Setup Time (D3 to CK)	t_{SU}	0.23	0.49
Input Hold Time (D3 to CK)	t_{HD}	0.23	0.39
Recovery Time (SN)	t_{RC}	0.15	0.33
Input Hold Time (SN to CK)	t_{HD}	0.37	0.63

FD3X4

4-Bit D Flip-Flop with Set

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD3X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.67	0.59 + 0.042*SL	0.59 + 0.042*SL	0.59 + 0.042*SL
	t_{PHL}	0.87	0.81 + 0.030*SL	0.82 + 0.026*SL	0.84 + 0.024*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to Q0	t_{PLH}	0.58	0.50 + 0.041*SL	0.50 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to Q1	t_{PLH}	0.68	0.60 + 0.042*SL	0.60 + 0.042*SL	0.60 + 0.042*SL
	t_{PHL}	0.88	0.82 + 0.031*SL	0.83 + 0.026*SL	0.85 + 0.024*SL
	t_R	0.27	0.11 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
SN to Q1	t_{PLH}	0.59	0.51 + 0.041*SL	0.51 + 0.041*SL	0.51 + 0.041*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to Q2	t_{PLH}	0.68	0.60 + 0.042*SL	0.60 + 0.042*SL	0.60 + 0.042*SL
	t_{PHL}	0.88	0.82 + 0.031*SL	0.83 + 0.026*SL	0.85 + 0.024*SL
	t_R	0.27	0.11 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
SN to Q2	t_{PLH}	0.59	0.51 + 0.041*SL	0.51 + 0.041*SL	0.51 + 0.041*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to Q3	t_{PLH}	0.67	0.59 + 0.042*SL	0.59 + 0.042*SL	0.59 + 0.042*SL
	t_{PHL}	0.87	0.81 + 0.030*SL	0.82 + 0.026*SL	0.84 + 0.024*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to Q3	t_{PLH}	0.58	0.50 + 0.041*SL	0.50 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
CK to QN0	t_{PLH}	1.08	0.99 + 0.042*SL	0.99 + 0.041*SL	0.99 + 0.041*SL
	t_{PHL}	0.76	0.70 + 0.030*SL	0.71 + 0.026*SL	0.73 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to QN0	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.023*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.09 + 0.040*SL
CK to QN1	t_{PLH}	1.08	0.99 + 0.042*SL	0.99 + 0.041*SL	0.99 + 0.041*SL
	t_{PHL}	0.77	0.71 + 0.030*SL	0.72 + 0.025*SL	0.73 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SN to QN1	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.023*SL
	t_F	0.18	0.10 + 0.039*SL	0.10 + 0.039*SL	0.09 + 0.040*SL
CK to QN2	t_{PLH}	1.08	0.99 + 0.042*SL	0.99 + 0.041*SL	0.99 + 0.041*SL
	t_{PHL}	0.77	0.71 + 0.030*SL	0.72 + 0.025*SL	0.73 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD3X4

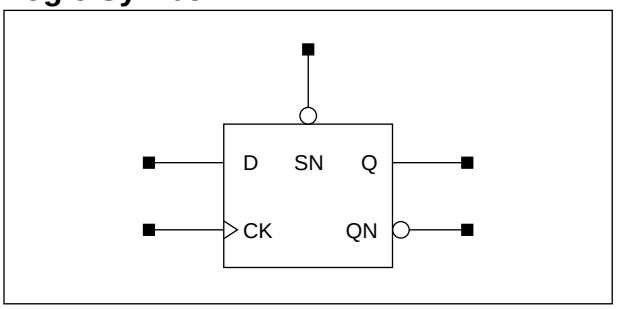
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.90	0.80 + 0.051*SL	0.80 + 0.050*SL	0.81 + 0.050*SL
	t_{PHL}	1.22	1.15 + 0.035*SL	1.17 + 0.026*SL	1.20 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to Q0	t_{PLH}	0.81	0.71 + 0.050*SL	0.71 + 0.050*SL	0.71 + 0.050*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
CK to Q1	t_{PLH}	0.92	0.82 + 0.051*SL	0.82 + 0.050*SL	0.82 + 0.050*SL
	t_{PHL}	1.23	1.16 + 0.035*SL	1.18 + 0.027*SL	1.21 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
SN to Q1	t_{PLH}	0.82	0.72 + 0.051*SL	0.72 + 0.050*SL	0.72 + 0.050*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
CK to Q2	t_{PLH}	0.92	0.82 + 0.051*SL	0.82 + 0.050*SL	0.82 + 0.050*SL
	t_{PHL}	1.23	1.16 + 0.035*SL	1.18 + 0.027*SL	1.21 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
SN to Q2	t_{PLH}	0.82	0.72 + 0.051*SL	0.72 + 0.050*SL	0.72 + 0.050*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
CK to Q3	t_{PLH}	0.90	0.80 + 0.051*SL	0.80 + 0.050*SL	0.81 + 0.050*SL
	t_{PHL}	1.22	1.15 + 0.035*SL	1.17 + 0.026*SL	1.20 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to Q3	t_{PLH}	0.81	0.71 + 0.050*SL	0.71 + 0.050*SL	0.71 + 0.050*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
CK to QN0	t_{PLH}	1.51	1.41 + 0.052*SL	1.41 + 0.050*SL	1.41 + 0.050*SL
	t_{PHL}	1.05	0.98 + 0.034*SL	1.00 + 0.026*SL	1.03 + 0.024*SL
	t_R	0.36	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SN to QN0	t_{PHL}	0.44	0.37 + 0.037*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN1	t_{PLH}	1.51	1.41 + 0.052*SL	1.41 + 0.050*SL	1.41 + 0.050*SL
	t_{PHL}	1.05	0.99 + 0.034*SL	1.01 + 0.026*SL	1.03 + 0.023*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SN to QN1	t_{PHL}	0.43	0.36 + 0.036*SL	0.39 + 0.027*SL	0.42 + 0.024*SL
	t_F	0.21	0.13 + 0.044*SL	0.14 + 0.041*SL	0.12 + 0.042*SL
CK to QN2	t_{PLH}	1.51	1.41 + 0.052*SL	1.41 + 0.050*SL	1.41 + 0.050*SL
	t_{PHL}	1.05	0.99 + 0.033*SL	1.01 + 0.026*SL	1.03 + 0.023*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

YFD3/YFD3D2

Fast D Flip-Flop with Set, 1X/2X Drive

Logic Symbol



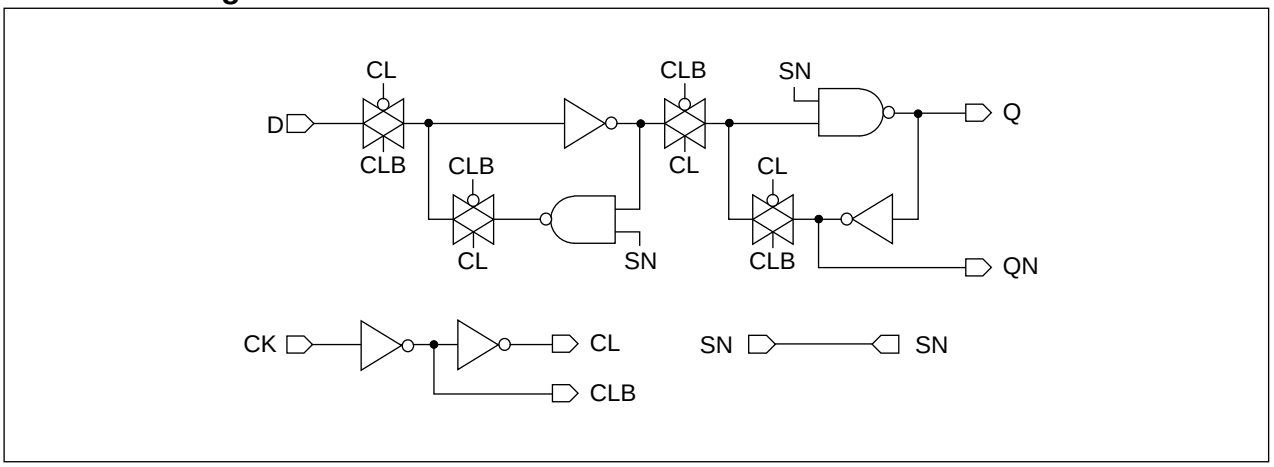
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
YFD3			*YFD3D2*			*YFD3*	*YFD3D2*
D	CK	SN	D	CK	SN		
2.9	0.8	1.4	2.9	0.8	2.1	6.0	8.0
KGM80							
YFD3			*YFD3D2*			*YFD3*	*YFD3D2*
D	CK	SN	D	CK	SN		
3.7	0.9	1.6	3.7	0.9	2.4	6.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		YFD3	YFD3D2	YFD3	YFD3D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.26	0.26	0.46	0.46
Input Hold Time (D to CK)	t_{HD}	0.26	0.26	0.52	0.52
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.42	0.42	0.85	0.63

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YFD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.47	0.38 + 0.043*SL	0.38 + 0.042*SL	0.39 + 0.042*SL
	t_{PHL}	0.44	0.36 + 0.041*SL	0.37 + 0.037*SL	0.38 + 0.035*SL
	t_R	0.38	0.21 + 0.085*SL	0.21 + 0.088*SL	0.19 + 0.090*SL
	t_F	0.32	0.19 + 0.068*SL	0.19 + 0.067*SL	0.19 + 0.067*SL
SN to Q	t_{PLH}	0.29	0.21 + 0.040*SL	0.21 + 0.040*SL	0.30 + 0.027*SL
	t_R	0.44	0.32 + 0.061*SL	0.38 + 0.038*SL	0.37 + 0.039*SL
CK to QN	t_{PLH}	0.66	0.46 + 0.102*SL	0.47 + 0.098*SL	0.48 + 0.095*SL
	t_{PHL}	0.59	0.44 + 0.078*SL	0.44 + 0.077*SL	0.44 + 0.077*SL
	t_R	0.34	0.15 + 0.099*SL	0.14 + 0.100*SL	0.14 + 0.100*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.09 + 0.063*SL
SN to QN	t_{PHL}	0.41	0.26 + 0.076*SL	0.28 + 0.068*SL	0.36 + 0.056*SL
	t_F	0.23	0.11 + 0.060*SL	0.14 + 0.048*SL	0.16 + 0.045*SL

KG80 YFD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.45	0.41 + 0.023*SL	0.41 + 0.022*SL	0.41 + 0.021*SL
	t_{PHL}	0.44	0.39 + 0.023*SL	0.40 + 0.021*SL	0.41 + 0.019*SL
	t_R	0.31	0.22 + 0.043*SL	0.22 + 0.044*SL	0.21 + 0.045*SL
	t_F	0.28	0.21 + 0.032*SL	0.21 + 0.033*SL	0.21 + 0.033*SL
SN to Q	t_{PLH}	0.25	0.21 + 0.020*SL	0.21 + 0.020*SL	0.20 + 0.021*SL
	t_R	0.39	0.31 + 0.040*SL	0.34 + 0.027*SL	0.40 + 0.019*SL
CK to QN	t_{PLH}	0.58	0.48 + 0.055*SL	0.48 + 0.051*SL	0.50 + 0.049*SL
	t_{PHL}	0.53	0.45 + 0.040*SL	0.45 + 0.039*SL	0.46 + 0.039*SL
	t_R	0.22	0.13 + 0.048*SL	0.12 + 0.050*SL	0.12 + 0.051*SL
	t_F	0.14	0.08 + 0.031*SL	0.08 + 0.031*SL	0.08 + 0.032*SL
SN to QN	t_{PHL}	0.32	0.25 + 0.040*SL	0.25 + 0.038*SL	0.27 + 0.035*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.030*SL	0.13 + 0.025*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YFD3

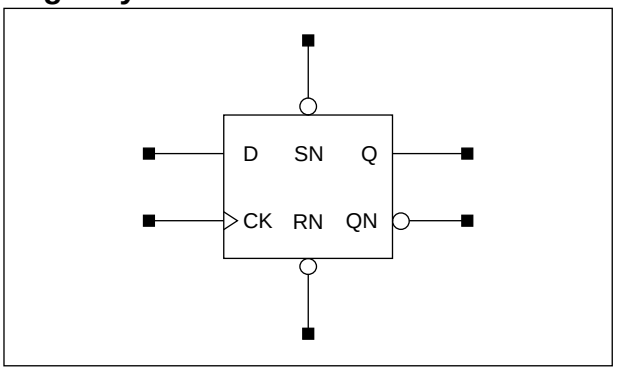
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.55 + 0.052*SL	0.55 + 0.050*SL	0.56 + 0.050*SL
	t_{PHL}	0.63	0.53 + 0.049*SL	0.55 + 0.041*SL	0.59 + 0.038*SL
	t_R	0.51	0.30 + 0.105*SL	0.30 + 0.107*SL	0.28 + 0.109*SL
	t_F	0.41	0.26 + 0.076*SL	0.27 + 0.073*SL	0.27 + 0.073*SL
SN to Q	t_{PLH}	0.36	0.26 + 0.049*SL	0.27 + 0.048*SL	0.48 + 0.028*SL
	t_R	0.59	0.40 + 0.095*SL	0.52 + 0.049*SL	0.52 + 0.049*SL
CK to QN	t_{PLH}	0.92	0.68 + 0.121*SL	0.70 + 0.113*SL	0.74 + 0.110*SL
	t_{PHL}	0.82	0.64 + 0.094*SL	0.64 + 0.092*SL	0.65 + 0.092*SL
	t_R	0.46	0.22 + 0.118*SL	0.22 + 0.119*SL	0.22 + 0.119*SL
	t_F	0.26	0.12 + 0.067*SL	0.12 + 0.068*SL	0.12 + 0.068*SL
SN to QN	t_{PHL}	0.54	0.35 + 0.092*SL	0.39 + 0.079*SL	0.56 + 0.063*SL
	t_F	0.27	0.14 + 0.065*SL	0.19 + 0.049*SL	0.18 + 0.050*SL

KGM80 YFD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.59 + 0.028*SL	0.59 + 0.026*SL	0.60 + 0.025*SL
	t_{PHL}	0.64	0.58 + 0.028*SL	0.60 + 0.023*SL	0.63 + 0.020*SL
	t_R	0.41	0.31 + 0.053*SL	0.31 + 0.052*SL	0.30 + 0.053*SL
	t_F	0.37	0.29 + 0.038*SL	0.29 + 0.037*SL	0.31 + 0.036*SL
SN to Q	t_{PLH}	0.31	0.26 + 0.025*SL	0.26 + 0.025*SL	0.26 + 0.025*SL
	t_R	0.48	0.38 + 0.051*SL	0.42 + 0.036*SL	0.56 + 0.023*SL
CK to QN	t_{PLH}	0.84	0.71 + 0.065*SL	0.73 + 0.059*SL	0.76 + 0.056*SL
	t_{PHL}	0.75	0.66 + 0.048*SL	0.66 + 0.046*SL	0.67 + 0.046*SL
	t_R	0.30	0.18 + 0.059*SL	0.18 + 0.059*SL	0.18 + 0.059*SL
	t_F	0.17	0.11 + 0.032*SL	0.10 + 0.033*SL	0.10 + 0.033*SL
SN to QN	t_{PHL}	0.42	0.33 + 0.047*SL	0.33 + 0.046*SL	0.40 + 0.039*SL
	t_F	0.19	0.12 + 0.034*SL	0.13 + 0.031*SL	0.22 + 0.023*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



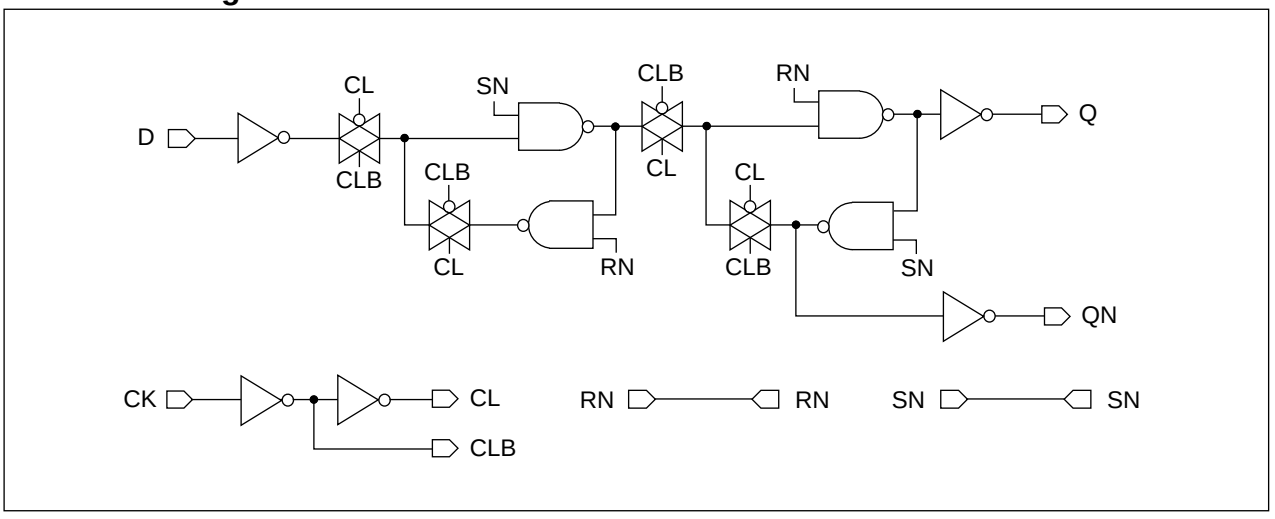
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
KG80									
FD4				*FD4D2*				*FD4*	*FD4D2*
D	CK	RN	SN	D	CK	RN	SN		
0.9	0.9	1.7	1.6	0.9	0.9	1.7	1.6	9.0	10.0
KGM80									
FD4				*FD4D2*				*FD4*	*FD4D2*
D	CK	RN	SN	D	CK	RN	SN		
1.0	1.0	2.2	2.1	1.0	1.0	2.2	2.1	9.0	10.0

Schematic Diagram



FD4/FD4D2

D Flip-Flop with Reset, Set, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD4	FD4D2	FD4	FD4D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.64	1.02	1.02
Input Setup Time (D to CK)	t_{SU}	0.42	0.42	0.74	0.74
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.63	0.63
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.48 + 0.044*SL	0.48 + 0.042*SL	0.49 + 0.042*SL
	t_{PHL}	0.57	0.51 + 0.031*SL	0.52 + 0.026*SL	0.53 + 0.024*SL
	t_R	0.29	0.11 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q	t_{PLH}	0.29	0.20 + 0.043*SL	0.21 + 0.041*SL	0.21 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.12 + 0.084*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q	t_{PLH}	0.65	0.56 + 0.043*SL	0.57 + 0.041*SL	0.57 + 0.041*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
CK to QN	t_{PLH}	0.76	0.67 + 0.042*SL	0.67 + 0.041*SL	0.67 + 0.042*SL
	t_{PHL}	0.65	0.58 + 0.030*SL	0.60 + 0.025*SL	0.61 + 0.023*SL
	t_R	0.28	0.10 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.041*SL	0.09 + 0.040*SL	0.07 + 0.042*SL
RN to QN	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.041*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
SN to QN	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.32	0.26 + 0.032*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.039*SL	0.09 + 0.041*SL

KG80 FD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.52 + 0.024*SL	0.52 + 0.022*SL	0.53 + 0.021*SL
	t_{PHL}	0.58	0.54 + 0.019*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_R	0.21	0.13 + 0.042*SL	0.12 + 0.043*SL	0.12 + 0.044*SL
	t_F	0.16	0.11 + 0.022*SL	0.12 + 0.019*SL	0.11 + 0.020*SL
RN to Q	t_{PLH}	0.29	0.24 + 0.023*SL	0.24 + 0.022*SL	0.25 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.020*SL	0.30 + 0.016*SL	0.32 + 0.013*SL
	t_R	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.044*SL
	t_F	0.16	0.12 + 0.021*SL	0.13 + 0.019*SL	0.12 + 0.020*SL
SN to Q	t_{PLH}	0.65	0.61 + 0.023*SL	0.61 + 0.022*SL	0.62 + 0.021*SL
	t_R	0.21	0.13 + 0.042*SL	0.13 + 0.043*SL	0.12 + 0.044*SL
CK to QN	t_{PLH}	0.80	0.76 + 0.021*SL	0.76 + 0.020*SL	0.76 + 0.020*SL
	t_{PHL}	0.69	0.65 + 0.019*SL	0.66 + 0.015*SL	0.68 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
RN to QN	t_{PLH}	0.56	0.52 + 0.022*SL	0.52 + 0.020*SL	0.52 + 0.020*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
SN to QN	t_{PLH}	0.28	0.23 + 0.025*SL	0.24 + 0.022*SL	0.24 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.042*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD4/FD4D2

D Flip-Flop with Reset, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD4

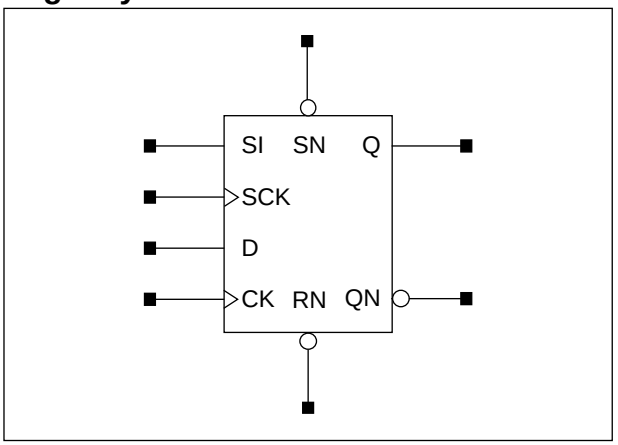
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.68 + 0.054*SL	0.69 + 0.051*SL	0.70 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.034*SL	0.75 + 0.027*SL	0.79 + 0.024*SL
	t_R	0.37	0.16 + 0.106*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q	t_{PLH}	0.39	0.28 + 0.054*SL	0.29 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.035*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.042*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q	t_{PLH}	0.90	0.80 + 0.054*SL	0.81 + 0.050*SL	0.81 + 0.050*SL
	t_R	0.37	0.17 + 0.103*SL	0.16 + 0.106*SL	0.14 + 0.109*SL
CK to QN	t_{PLH}	1.07	0.97 + 0.052*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.91	0.85 + 0.034*SL	0.87 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.70	0.60 + 0.051*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
SN to QN	t_{PLH}	0.40	0.29 + 0.054*SL	0.30 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.42	0.35 + 0.035*SL	0.38 + 0.026*SL	0.41 + 0.024*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL

KGM80 FD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.73 + 0.030*SL	0.74 + 0.026*SL	0.75 + 0.025*SL
	t_{PHL}	0.82	0.78 + 0.022*SL	0.80 + 0.016*SL	0.83 + 0.013*SL
	t_R	0.28	0.18 + 0.053*SL	0.18 + 0.052*SL	0.17 + 0.053*SL
	t_F	0.19	0.14 + 0.025*SL	0.15 + 0.021*SL	0.15 + 0.021*SL
RN to Q	t_{PLH}	0.39	0.33 + 0.030*SL	0.34 + 0.026*SL	0.35 + 0.025*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.42 + 0.016*SL	0.45 + 0.013*SL
	t_R	0.28	0.18 + 0.049*SL	0.17 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.20	0.15 + 0.025*SL	0.16 + 0.021*SL	0.16 + 0.020*SL
SN to Q	t_{PLH}	0.92	0.86 + 0.030*SL	0.87 + 0.026*SL	0.88 + 0.025*SL
	t_R	0.28	0.18 + 0.053*SL	0.18 + 0.052*SL	0.16 + 0.053*SL
CK to QN	t_{PLH}	1.13	1.08 + 0.029*SL	1.09 + 0.025*SL	1.09 + 0.025*SL
	t_{PHL}	0.99	0.94 + 0.022*SL	0.96 + 0.016*SL	0.99 + 0.013*SL
	t_R	0.24	0.13 + 0.054*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
RN to QN	t_{PLH}	0.76	0.70 + 0.029*SL	0.71 + 0.025*SL	0.71 + 0.025*SL
	t_R	0.24	0.13 + 0.055*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
SN to QN	t_{PLH}	0.38	0.32 + 0.031*SL	0.33 + 0.026*SL	0.35 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.40 + 0.017*SL	0.44 + 0.013*SL
	t_R	0.24	0.13 + 0.055*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



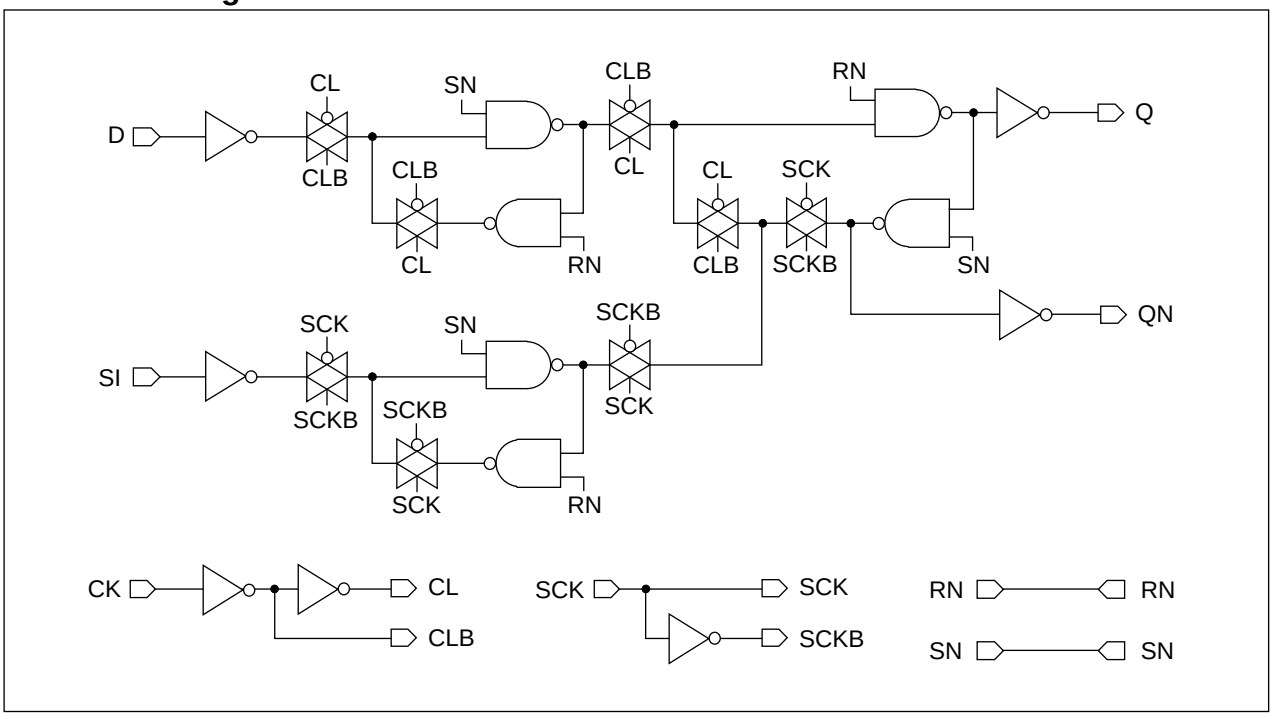
Truth Table

SI	SCK	D	CK	RN	SN	Q (n+1)	QN (n+1)
x	0	0	↑	1	1	0	1
x	0	1	↑	1	1	1	0
0	↑	x	0	1	1	0	1
1	↑	x	0	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0

Cell Data

Input Load (SL)												Gate Count	
KG80													
FD4CS						*FD4CSD2*						*FD4CS*	*FD4CSD2*
SI	SCK	D	CK	RN	SN	SI	SCK	D	CK	RN	SN		
0.8	2.1	0.9	0.9	3.0	2.6	0.8	2.1	0.9	0.9	3.0	2.7	14.0	15.0
KGM80													
FD4CS						*FD4CSD2*						*FD4CS*	*FD4CSD2*
SI	SCK	D	CK	RN	SN	SI	SCK	D	CK	RN	SN		
1.0	2.6	1.0	1.0	3.5	3.1	1.0	2.5	1.0	1.0	3.6	3.1	14.0	15.0

Schematic Diagram



FD4CS/FD4CSD2

D Flip-Flop with Reset, Set, Scan Clock, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD4CS	FD4CSD2	FD4CS	FD4CSD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SCK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (SCK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.72	0.75	1.18	1.24
Input Setup Time (D to CK)	t_{SU}	0.42	0.42	0.74	0.74
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.61	0.61	1.02	1.05
Input Hold Time (SI to SCK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.85	0.85
Recovery Time (RN to SCK)	t_{RC}	0.15	0.15	0.55	0.58
Input Hold Time (RN to SCK)	t_{HD}	0.31	0.31	0.63	0.63
Recovery Time (SN to CK)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41
Recovery Time (SN to SCK)	t_{RC}	0.31	0.31	0.33	0.52
Input Hold Time (sN to SCK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD4CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.59	0.50 + 0.044*SL	0.51 + 0.042*SL	0.51 + 0.042*SL
	t_{PHL}	0.58	0.52 + 0.032*SL	0.53 + 0.026*SL	0.55 + 0.024*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.040*SL	0.10 + 0.041*SL
SCK to Q	t_{PLH}	0.65	0.56 + 0.045*SL	0.57 + 0.042*SL	0.57 + 0.041*SL
	t_{PHL}	0.55	0.49 + 0.033*SL	0.50 + 0.027*SL	0.52 + 0.024*SL
	t_R	0.30	0.13 + 0.085*SL	0.13 + 0.087*SL	0.11 + 0.089*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.040*SL	0.11 + 0.040*SL
SN to Q	t_{PLH}	0.69	0.60 + 0.044*SL	0.60 + 0.041*SL	0.61 + 0.041*SL
	t_R	0.29	0.12 + 0.086*SL	0.12 + 0.088*SL	0.10 + 0.090*SL
RN to Q	t_{PLH}	0.31	0.22 + 0.044*SL	0.23 + 0.041*SL	0.23 + 0.042*SL
	t_{PHL}	0.34	0.28 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
CK to QN	t_{PLH}	0.89	0.79 + 0.045*SL	0.80 + 0.042*SL	0.81 + 0.041*SL
	t_{PHL}	0.76	0.69 + 0.036*SL	0.71 + 0.028*SL	0.73 + 0.025*SL
	t_R	0.32	0.15 + 0.084*SL	0.15 + 0.086*SL	0.13 + 0.089*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.040*SL	0.13 + 0.041*SL
SCK to QN	t_{PLH}	0.75	0.66 + 0.042*SL	0.66 + 0.041*SL	0.66 + 0.041*SL
	t_{PHL}	0.73	0.67 + 0.030*SL	0.68 + 0.025*SL	0.69 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to QN	t_{PLH}	0.40	0.31 + 0.047*SL	0.32 + 0.043*SL	0.33 + 0.041*SL
	t_{PHL}	0.41	0.34 + 0.038*SL	0.36 + 0.028*SL	0.39 + 0.024*SL
	t_R	0.32	0.15 + 0.085*SL	0.15 + 0.086*SL	0.13 + 0.088*SL
	t_F	0.23	0.14 + 0.041*SL	0.15 + 0.038*SL	0.14 + 0.039*SL
RN to QN	t_{PLH}	0.65	0.56 + 0.045*SL	0.57 + 0.042*SL	0.57 + 0.041*SL
	t_R	0.32	0.15 + 0.084*SL	0.15 + 0.086*SL	0.13 + 0.088*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD4CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.53 + 0.025*SL	0.54 + 0.022*SL	0.55 + 0.021*SL
	t_{PHL}	0.58	0.54 + 0.021*SL	0.55 + 0.016*SL	0.57 + 0.014*SL
	t_R	0.20	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.044*SL
	t_F	0.15	0.11 + 0.022*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
SCK to Q	t_{PLH}	0.65	0.60 + 0.025*SL	0.61 + 0.022*SL	0.62 + 0.021*SL
	t_{PHL}	0.56	0.51 + 0.021*SL	0.53 + 0.016*SL	0.54 + 0.014*SL
	t_R	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.17	0.12 + 0.021*SL	0.13 + 0.020*SL	0.13 + 0.019*SL
SN to Q	t_{PLH}	0.68	0.63 + 0.025*SL	0.64 + 0.022*SL	0.65 + 0.021*SL
	t_R	0.20	0.11 + 0.042*SL	0.11 + 0.042*SL	0.11 + 0.043*SL
RN to Q	t_{PLH}	0.30	0.25 + 0.025*SL	0.25 + 0.022*SL	0.26 + 0.021*SL
	t_{PHL}	0.34	0.29 + 0.023*SL	0.31 + 0.017*SL	0.33 + 0.014*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.041*SL	0.10 + 0.044*SL
	t_F	0.16	0.12 + 0.023*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
CK to QN	t_{PLH}	0.94	0.89 + 0.026*SL	0.90 + 0.022*SL	0.91 + 0.021*SL
	t_{PHL}	0.82	0.77 + 0.023*SL	0.78 + 0.017*SL	0.80 + 0.015*SL
	t_R	0.23	0.15 + 0.042*SL	0.15 + 0.042*SL	0.14 + 0.043*SL
	t_F	0.19	0.14 + 0.026*SL	0.16 + 0.020*SL	0.16 + 0.020*SL
SCK to QN	t_{PLH}	0.81	0.77 + 0.022*SL	0.78 + 0.020*SL	0.77 + 0.020*SL
	t_{PHL}	0.80	0.76 + 0.018*SL	0.77 + 0.015*SL	0.78 + 0.013*SL
	t_R	0.19	0.11 + 0.042*SL	0.11 + 0.043*SL	0.10 + 0.043*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
SN to QN	t_{PLH}	0.40	0.34 + 0.028*SL	0.36 + 0.023*SL	0.37 + 0.021*SL
	t_{PHL}	0.41	0.36 + 0.026*SL	0.38 + 0.018*SL	0.40 + 0.015*SL
	t_R	0.23	0.15 + 0.043*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
	t_F	0.20	0.15 + 0.026*SL	0.16 + 0.019*SL	0.17 + 0.018*SL
RN to QN	t_{PLH}	0.71	0.65 + 0.026*SL	0.67 + 0.022*SL	0.67 + 0.021*SL
	t_R	0.23	0.15 + 0.041*SL	0.15 + 0.043*SL	0.15 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD4CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.71 + 0.054*SL	0.72 + 0.051*SL	0.73 + 0.050*SL
	t_{PHL}	0.83	0.76 + 0.036*SL	0.78 + 0.027*SL	0.81 + 0.024*SL
	t_R	0.38	0.17 + 0.104*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.042*SL	0.13 + 0.042*SL
SCK to Q	t_{PLH}	0.96	0.84 + 0.056*SL	0.86 + 0.051*SL	0.87 + 0.050*SL
	t_{PHL}	0.78	0.71 + 0.037*SL	0.73 + 0.028*SL	0.77 + 0.024*SL
	t_R	0.39	0.18 + 0.104*SL	0.18 + 0.106*SL	0.16 + 0.108*SL
	t_F	0.23	0.14 + 0.044*SL	0.15 + 0.041*SL	0.15 + 0.042*SL
SN to Q	t_{PLH}	0.97	0.86 + 0.054*SL	0.87 + 0.050*SL	0.88 + 0.050*SL
	t_R	0.38	0.17 + 0.104*SL	0.17 + 0.106*SL	0.14 + 0.108*SL
RN to Q	t_{PLH}	0.42	0.31 + 0.054*SL	0.32 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.45	0.38 + 0.036*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.37	0.17 + 0.104*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.22	0.14 + 0.043*SL	0.14 + 0.042*SL	0.14 + 0.042*SL
CK to QN	t_{PLH}	1.25	1.13 + 0.059*SL	1.16 + 0.051*SL	1.17 + 0.050*SL
	t_{PHL}	1.09	1.01 + 0.040*SL	1.04 + 0.030*SL	1.08 + 0.026*SL
	t_R	0.42	0.22 + 0.105*SL	0.22 + 0.104*SL	0.18 + 0.107*SL
	t_F	0.26	0.17 + 0.045*SL	0.17 + 0.043*SL	0.18 + 0.042*SL
SCK to QN	t_{PLH}	1.06	0.96 + 0.051*SL	0.97 + 0.050*SL	0.96 + 0.050*SL
	t_{PHL}	1.08	1.02 + 0.033*SL	1.04 + 0.026*SL	1.06 + 0.023*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
SN to QN	t_{PLH}	0.54	0.42 + 0.061*SL	0.44 + 0.052*SL	0.46 + 0.050*SL
	t_{PHL}	0.55	0.47 + 0.042*SL	0.50 + 0.030*SL	0.56 + 0.025*SL
	t_R	0.42	0.22 + 0.104*SL	0.21 + 0.104*SL	0.18 + 0.107*SL
	t_F	0.27	0.17 + 0.047*SL	0.19 + 0.041*SL	0.19 + 0.041*SL
RN to QN	t_{PLH}	0.88	0.76 + 0.059*SL	0.78 + 0.051*SL	0.80 + 0.050*SL
	t_R	0.42	0.21 + 0.105*SL	0.22 + 0.104*SL	0.18 + 0.107*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FD4CS/FD4CSD2

D Flip-Flop with Reset, Set, Scan Clock, 1X/2X Drive

Switching Characteristics

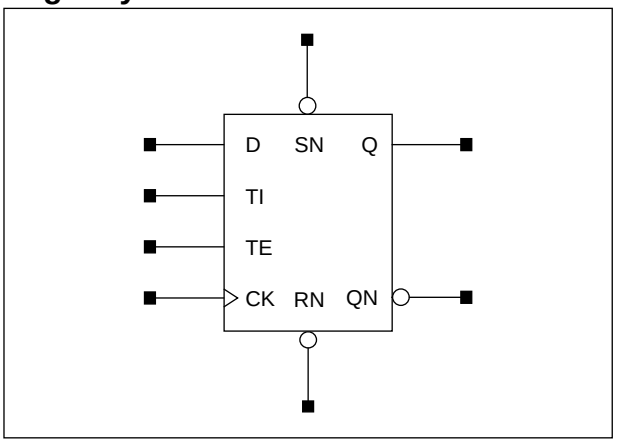
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD4CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.81	0.75 + 0.032*SL	0.76 + 0.027*SL	0.78 + 0.025*SL
	t_{PHL}	0.84	0.79 + 0.025*SL	0.81 + 0.017*SL	0.85 + 0.014*SL
	t_R	0.26	0.15 + 0.053*SL	0.15 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.15 + 0.021*SL	0.15 + 0.021*SL
SCK to Q	t_{PLH}	0.96	0.90 + 0.032*SL	0.91 + 0.027*SL	0.93 + 0.025*SL
	t_{PHL}	0.80	0.75 + 0.025*SL	0.77 + 0.018*SL	0.81 + 0.014*SL
	t_R	0.27	0.17 + 0.053*SL	0.17 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.20	0.15 + 0.026*SL	0.16 + 0.021*SL	0.17 + 0.021*SL
SN to Q	t_{PLH}	0.96	0.90 + 0.031*SL	0.91 + 0.027*SL	0.93 + 0.025*SL
	t_R	0.26	0.15 + 0.054*SL	0.16 + 0.052*SL	0.14 + 0.053*SL
RN to Q	t_{PLH}	0.40	0.34 + 0.032*SL	0.35 + 0.027*SL	0.37 + 0.025*SL
	t_{PHL}	0.45	0.40 + 0.026*SL	0.42 + 0.018*SL	0.47 + 0.014*SL
	t_R	0.25	0.14 + 0.054*SL	0.15 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.19	0.14 + 0.025*SL	0.15 + 0.022*SL	0.17 + 0.020*SL
CK to QN	t_{PLH}	1.34	1.27 + 0.033*SL	1.28 + 0.028*SL	1.31 + 0.025*SL
	t_{PHL}	1.17	1.12 + 0.027*SL	1.14 + 0.019*SL	1.18 + 0.015*SL
	t_R	0.30	0.19 + 0.056*SL	0.20 + 0.052*SL	0.20 + 0.052*SL
	t_F	0.23	0.17 + 0.029*SL	0.19 + 0.023*SL	0.21 + 0.021*SL
SCK to QN	t_{PLH}	1.17	1.11 + 0.028*SL	1.12 + 0.025*SL	1.12 + 0.025*SL
	t_{PHL}	1.20	1.16 + 0.021*SL	1.17 + 0.016*SL	1.20 + 0.013*SL
	t_R	0.25	0.14 + 0.054*SL	0.15 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
SN to QN	t_{PLH}	0.53	0.46 + 0.035*SL	0.48 + 0.029*SL	0.52 + 0.026*SL
	t_{PHL}	0.56	0.50 + 0.030*SL	0.53 + 0.020*SL	0.59 + 0.015*SL
	t_R	0.30	0.19 + 0.056*SL	0.20 + 0.052*SL	0.20 + 0.052*SL
	t_F	0.24	0.18 + 0.028*SL	0.20 + 0.022*SL	0.22 + 0.020*SL
RN to QN	t_{PLH}	0.96	0.89 + 0.034*SL	0.91 + 0.028*SL	0.94 + 0.025*SL
	t_R	0.30	0.19 + 0.057*SL	0.20 + 0.052*SL	0.20 + 0.052*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



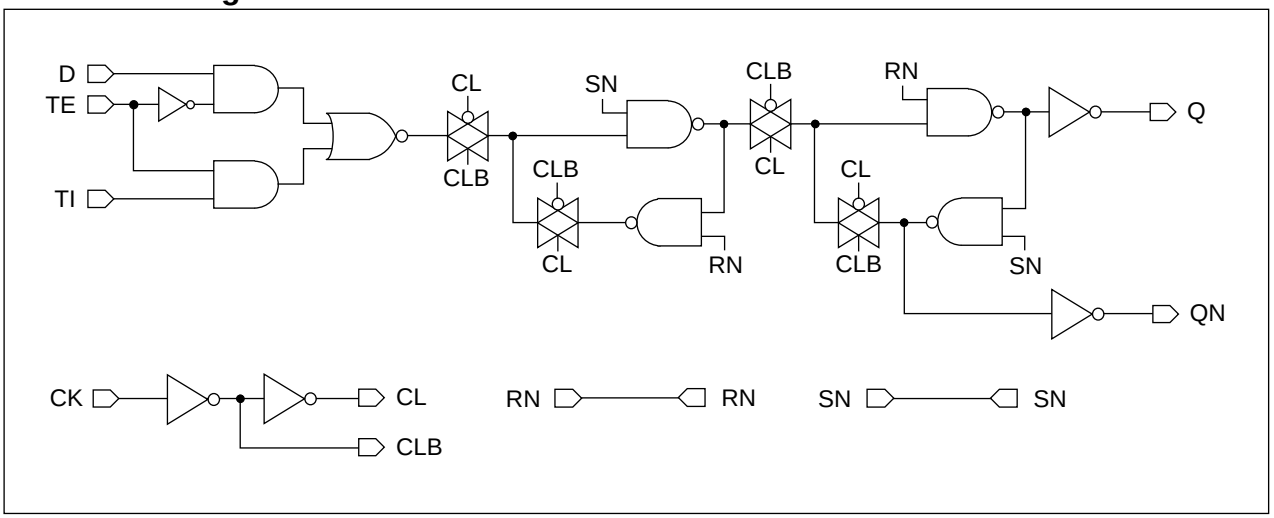
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	1	0	1
1	x	0	↑	1	1	1	0
x	0	1	↑	1	1	0	1
x	1	1	↑	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
KG80													
FD4S						*FD4SD2*						*FD4S*	*FD4SD2*
D	TI	TE	CK	RN	SN	D	TI	TE	CK	RN	SN		
0.9	0.7	1.6	0.9	1.9	1.7	0.9	0.7	1.6	0.9	1.9	1.7	11.0	12.0
KGM80													
FD4S						*FD4SD2*						*FD4S*	*FD4SD2*
D	TI	TE	CK	RN	SN	D	TI	TE	CK	RN	SN		
1.0	0.9	1.9	1.1	2.3	2.1	1.0	0.9	1.9	1.1	2.3	2.1	11.0	12.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD4S	FD4SD2	FD4S	FD4SD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	1.02	1.02
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.64	0.64	1.05	1.05
Input Setup Time (D to CK)	t_{SU}	0.53	0.53	0.93	0.93
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.58	0.58	1.05	1.05
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.56	0.56	0.99	0.99
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.85	0.85
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.57	0.48 + 0.044*SL	0.49 + 0.042*SL	0.49 + 0.042*SL
	t_{PHL}	0.57	0.51 + 0.031*SL	0.52 + 0.026*SL	0.54 + 0.024*SL
	t_R	0.29	0.11 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.041*SL	0.09 + 0.041*SL	0.09 + 0.041*SL
RN to Q	t_{PLH}	0.29	0.20 + 0.043*SL	0.21 + 0.041*SL	0.21 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q	t_{PLH}	0.66	0.58 + 0.043*SL	0.58 + 0.041*SL	0.58 + 0.041*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
CK to QN	t_{PLH}	0.78	0.69 + 0.042*SL	0.69 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.66	0.60 + 0.030*SL	0.61 + 0.025*SL	0.62 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN	t_{PLH}	0.54	0.45 + 0.042*SL	0.45 + 0.041*SL	0.45 + 0.041*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
SN to QN	t_{PLH}	0.31	0.22 + 0.044*SL	0.22 + 0.041*SL	0.22 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.29	0.11 + 0.088*SL	0.12 + 0.086*SL	0.09 + 0.090*SL
	t_F	0.18	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL

KG80 FD4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.56	0.51 + 0.025*SL	0.52 + 0.022*SL	0.52 + 0.021*SL
	t_{PHL}	0.57	0.53 + 0.021*SL	0.54 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.19	0.11 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.15	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PLH}	0.28	0.23 + 0.024*SL	0.23 + 0.022*SL	0.24 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
	t_F	0.15	0.11 + 0.023*SL	0.12 + 0.020*SL	0.11 + 0.020*SL
SN to Q	t_{PLH}	0.66	0.61 + 0.024*SL	0.61 + 0.022*SL	0.62 + 0.021*SL
	t_R	0.19	0.11 + 0.042*SL	0.11 + 0.043*SL	0.10 + 0.043*SL
CK to QN	t_{PLH}	0.82	0.77 + 0.023*SL	0.78 + 0.020*SL	0.78 + 0.020*SL
	t_{PHL}	0.71	0.67 + 0.019*SL	0.68 + 0.015*SL	0.69 + 0.013*SL
	t_R	0.19	0.11 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.10 + 0.022*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
RN to QN	t_{PLH}	0.58	0.53 + 0.023*SL	0.54 + 0.020*SL	0.53 + 0.020*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
SN to QN	t_{PLH}	0.29	0.24 + 0.024*SL	0.25 + 0.022*SL	0.26 + 0.021*SL
	t_{PHL}	0.33	0.28 + 0.022*SL	0.30 + 0.016*SL	0.32 + 0.014*SL
	t_R	0.19	0.11 + 0.040*SL	0.11 + 0.041*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

FD4S/FD4SD2

D Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD4S

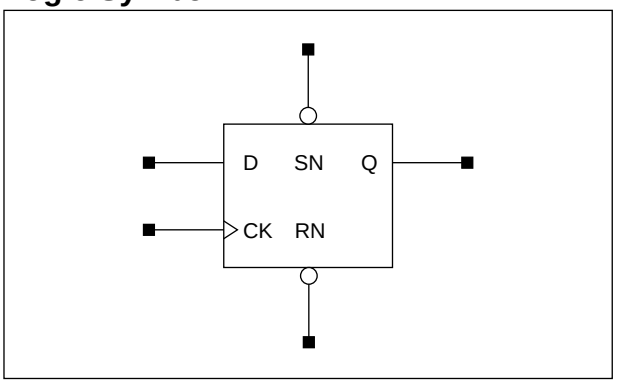
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.68 + 0.055*SL	0.70 + 0.051*SL	0.70 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.76 + 0.027*SL	0.79 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q	t_{PLH}	0.39	0.28 + 0.054*SL	0.30 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.035*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q	t_{PLH}	0.93	0.82 + 0.054*SL	0.83 + 0.050*SL	0.84 + 0.050*SL
	t_R	0.37	0.17 + 0.103*SL	0.16 + 0.106*SL	0.13 + 0.109*SL
CK to QN	t_{PLH}	1.10	1.00 + 0.052*SL	1.00 + 0.050*SL	1.00 + 0.050*SL
	t_{PHL}	0.94	0.87 + 0.034*SL	0.89 + 0.026*SL	0.92 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to QN	t_{PLH}	0.73	0.62 + 0.052*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.12 + 0.109*SL
SN to QN	t_{PLH}	0.42	0.31 + 0.055*SL	0.32 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.045*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

KGM80 FD4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.78	0.71 + 0.031*SL	0.73 + 0.027*SL	0.74 + 0.025*SL
	t_{PHL}	0.81	0.76 + 0.024*SL	0.78 + 0.017*SL	0.82 + 0.013*SL
	t_R	0.24	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.14 + 0.021*SL
RN to Q	t_{PLH}	0.37	0.31 + 0.031*SL	0.32 + 0.026*SL	0.34 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.40 + 0.017*SL	0.44 + 0.013*SL
	t_R	0.24	0.14 + 0.053*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
SN to Q	t_{PLH}	0.92	0.86 + 0.031*SL	0.87 + 0.026*SL	0.89 + 0.025*SL
	t_R	0.25	0.14 + 0.053*SL	0.15 + 0.052*SL	0.13 + 0.053*SL
CK to QN	t_{PLH}	1.16	1.10 + 0.029*SL	1.11 + 0.025*SL	1.12 + 0.025*SL
	t_{PHL}	1.01	0.97 + 0.022*SL	0.98 + 0.016*SL	1.01 + 0.013*SL
	t_R	0.24	0.14 + 0.054*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.18	0.13 + 0.024*SL	0.13 + 0.021*SL	0.15 + 0.020*SL
RN to QN	t_{PLH}	0.78	0.72 + 0.029*SL	0.74 + 0.025*SL	0.74 + 0.025*SL
	t_R	0.24	0.14 + 0.054*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
SN to QN	t_{PLH}	0.40	0.34 + 0.031*SL	0.35 + 0.027*SL	0.37 + 0.025*SL
	t_{PHL}	0.44	0.39 + 0.026*SL	0.41 + 0.017*SL	0.45 + 0.014*SL
	t_R	0.24	0.13 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Logic Symbol



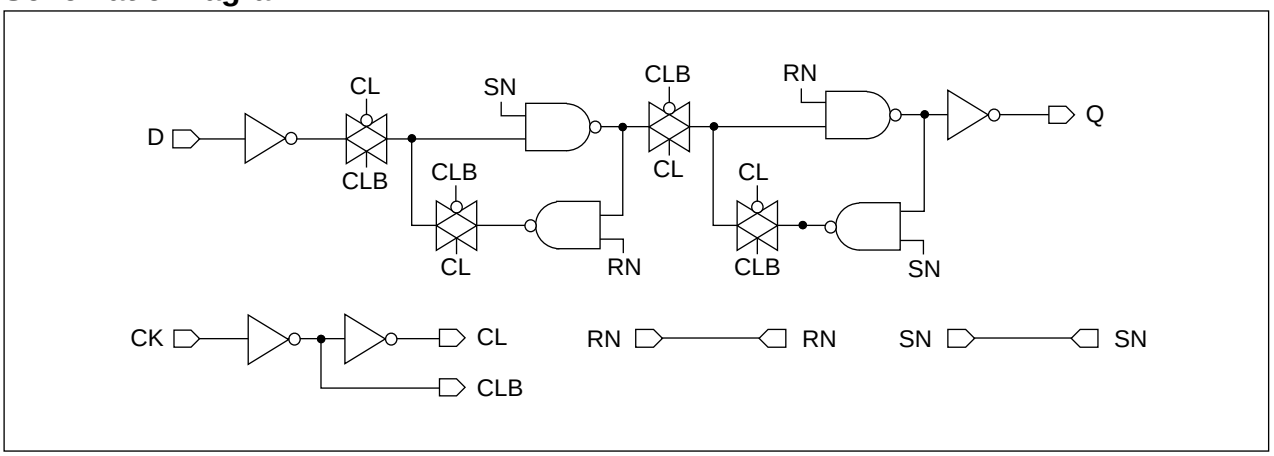
Truth Table

D	CK	RN	SN	Q (n+1)
0	↑	1	1	0
1	↑	1	1	1
x	x	1	0	1
x	x	0	1	0
x	x	0	0	0
x	↓	1	1	Q (n)

Cell Data

Input Load (SL)								Gate Count	
KG80									
FD4Q				*FD4QD2*				*FD4Q*	*FD4QD2*
D	CK	RN	SN	D	CK	RN	SN		
0.8	0.8	1.5	1.5	0.8	0.8	1.5	1.5	8.0	9.0
KGM80									
FD4Q				*FD4QD2*				*FD4Q*	*FD4QD2*
D	CK	RN	SN	D	CK	RN	SN		
0.9	0.9	1.7	1.7	0.9	0.9	1.7	1.7	8.0	9.0

Schematic Diagram



FD4Q/FD4QD2

D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD4Q	FD4QD2	FD4Q	FD4QD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.64	0.64	1.05	1.05
Input Setup Time (D to CK)	t_{SU}	0.45	0.45.	0.80	0.80
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.63	0.63
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD4Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.56	0.47 + 0.045*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.54	0.47 + 0.031*SL	0.49 + 0.026*SL	0.50 + 0.024*SL
	t_R	0.28	0.11 + 0.087*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to Q	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.33	0.27 + 0.033*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.040*SL	0.10 + 0.040*SL
SN to Q	t_{PLH}	0.66	0.57 + 0.043*SL	0.58 + 0.041*SL	0.58 + 0.042*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL

KG80 FD4QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.55	0.51 + 0.024*SL	0.51 + 0.022*SL	0.52 + 0.021*SL
	t_{PHL}	0.54	0.50 + 0.019*SL	0.51 + 0.015*SL	0.52 + 0.013*SL
	t_R	0.21	0.12 + 0.044*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.15	0.11 + 0.022*SL	0.11 + 0.020*SL	0.12 + 0.019*SL
RN to Q	t_{PLH}	0.28	0.24 + 0.023*SL	0.24 + 0.022*SL	0.25 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.020*SL	0.30 + 0.016*SL	0.32 + 0.013*SL
	t_R	0.20	0.11 + 0.043*SL	0.11 + 0.043*SL	0.11 + 0.045*SL
	t_F	0.16	0.12 + 0.021*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
SN to Q	t_{PLH}	0.66	0.61 + 0.024*SL	0.62 + 0.021*SL	0.62 + 0.021*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.044*SL	0.11 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD4Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.80	0.69 + 0.055*SL	0.70 + 0.051*SL	0.71 + 0.050*SL
	t_{PHL}	0.77	0.69 + 0.035*SL	0.72 + 0.027*SL	0.75 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q	t_{PLH}	0.40	0.29 + 0.054*SL	0.30 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.44	0.36 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.22	0.13 + 0.045*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
SN to Q	t_{PLH}	0.94	0.83 + 0.054*SL	0.84 + 0.050*SL	0.84 + 0.050*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.108*SL

KGM80 FD4QD2

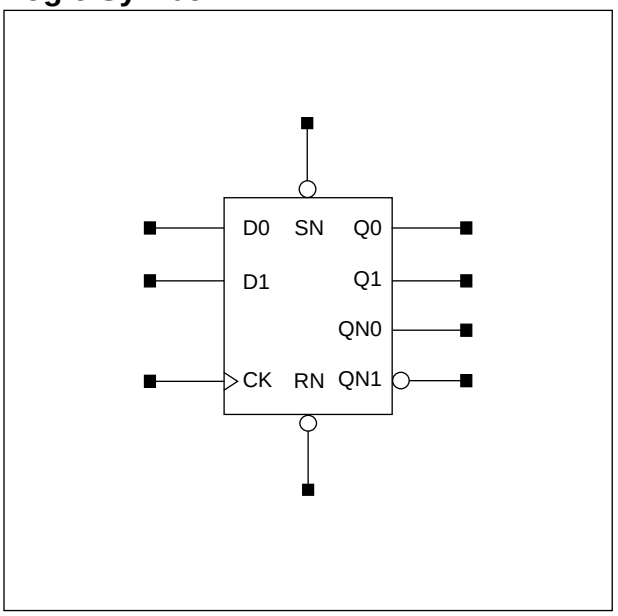
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.73 + 0.030*SL	0.74 + 0.027*SL	0.76 + 0.025*SL
	t_{PHL}	0.78	0.73 + 0.022*SL	0.75 + 0.016*SL	0.78 + 0.013*SL
	t_R	0.27	0.16 + 0.053*SL	0.16 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
RN to Q	t_{PLH}	0.39	0.33 + 0.030*SL	0.34 + 0.026*SL	0.35 + 0.025*SL
	t_{PHL}	0.44	0.39 + 0.023*SL	0.41 + 0.017*SL	0.45 + 0.013*SL
	t_R	0.26	0.16 + 0.053*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.14 + 0.025*SL	0.15 + 0.021*SL	0.16 + 0.020*SL
SN to Q	t_{PLH}	0.94	0.88 + 0.030*SL	0.89 + 0.026*SL	0.90 + 0.025*SL
	t_R	0.27	0.16 + 0.052*SL	0.17 + 0.052*SL	0.15 + 0.053*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

FD4X2

2-Bit D Flip-Flop with Reset, Set

Logic Symbol



Truth Table

Dn	CK	RN	SN	Qn (n+1)	QNn (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
KG80				
Dn	CK	RN	SN	
0.9	0.9	3.9	3.8	16.0
KGM80				
Dn	CK	RN	SN	
1.0	1.0	4.9	4.7	16.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.64	1.05
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	1.02
Input Setup Time (D0 to CK)	t_{SU}	0.34	0.64
Input Hold Time (D0 to CK)	t_{HD}	0.15	0.33
Input Setup Time (D1 to CK)	t_{SU}	0.34	0.64
Input Hold Time (D1 to CK)	t_{HD}	0.15	0.33
Recovery Time (RN)	t_{RC}	0.15	0.33
Input Hold Time (RN to CK)	t_{HD}	0.48	0.85
Recovery Time (SN)	t_{RC}	0.15	0.33
Input Hold Time (SN to CK)	t_{HD}	0.26	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD4X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.63	0.54 + 0.043*SL	0.54 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.68	0.62 + 0.031*SL	0.63 + 0.026*SL	0.65 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.089*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q0	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
SN to Q0	t_{PLH}	0.65	0.57 + 0.043*SL	0.57 + 0.041*SL	0.57 + 0.041*SL
	t_R	0.29	0.11 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
CK to Q1	t_{PLH}	0.63	0.54 + 0.044*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.68	0.62 + 0.031*SL	0.63 + 0.026*SL	0.65 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.089*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q1	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
SN to Q1	t_{PLH}	0.65	0.56 + 0.043*SL	0.57 + 0.041*SL	0.57 + 0.042*SL
	t_R	0.29	0.11 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
CK to QN0	t_{PLH}	0.89	0.80 + 0.042*SL	0.81 + 0.041*SL	0.80 + 0.041*SL
	t_{PHL}	0.72	0.66 + 0.030*SL	0.67 + 0.026*SL	0.68 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to QN0	t_{PLH}	0.54	0.45 + 0.042*SL	0.46 + 0.041*SL	0.45 + 0.041*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
SN to QN0	t_{PLH}	0.31	0.22 + 0.043*SL	0.22 + 0.042*SL	0.23 + 0.041*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to QN1	t_{PLH}	0.89	0.80 + 0.043*SL	0.81 + 0.041*SL	0.80 + 0.041*SL
	t_{PHL}	0.72	0.66 + 0.030*SL	0.67 + 0.026*SL	0.68 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to QN1	t_{PLH}	0.54	0.45 + 0.042*SL	0.46 + 0.041*SL	0.45 + 0.041*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
SN to QN1	t_{PLH}	0.31	0.22 + 0.043*SL	0.22 + 0.042*SL	0.23 + 0.041*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD4X2

2-Bit D Flip-Flop with Reset, Set

Switching Characteristics

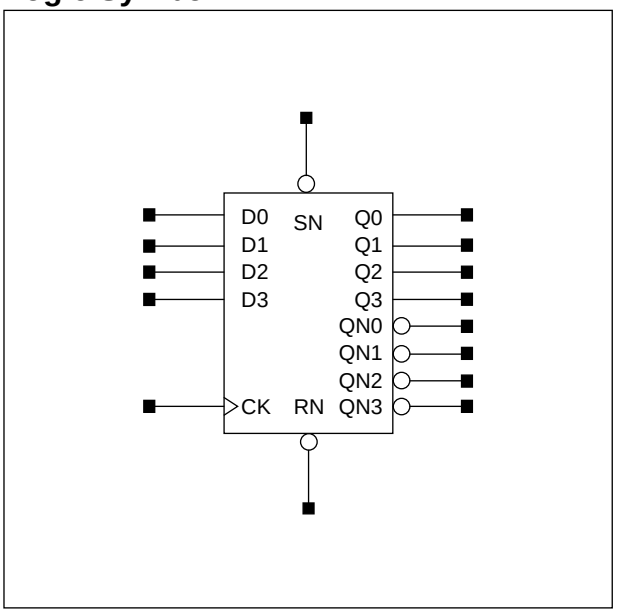
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD4X2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.87	0.76 + 0.054*SL	0.77 + 0.051*SL	0.78 + 0.050*SL
	t_{PHL}	0.96	0.89 + 0.035*SL	0.91 + 0.027*SL	0.94 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q0	t_{PLH}	0.39	0.28 + 0.054*SL	0.30 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.035*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q0	t_{PLH}	0.91	0.80 + 0.053*SL	0.81 + 0.050*SL	0.82 + 0.050*SL
	t_R	0.37	0.17 + 0.103*SL	0.16 + 0.106*SL	0.13 + 0.109*SL
CK to Q1	t_{PLH}	0.87	0.76 + 0.054*SL	0.77 + 0.051*SL	0.78 + 0.050*SL
	t_{PHL}	0.96	0.89 + 0.035*SL	0.91 + 0.027*SL	0.94 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q1	t_{PLH}	0.39	0.28 + 0.054*SL	0.30 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.035*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q1	t_{PLH}	0.91	0.80 + 0.054*SL	0.81 + 0.050*SL	0.82 + 0.050*SL
	t_R	0.37	0.17 + 0.103*SL	0.16 + 0.106*SL	0.13 + 0.109*SL
CK to QN0	t_{PLH}	1.26	1.15 + 0.053*SL	1.16 + 0.050*SL	1.16 + 0.050*SL
	t_{PHL}	1.01	0.94 + 0.034*SL	0.96 + 0.026*SL	1.00 + 0.024*SL
	t_R	0.36	0.16 + 0.104*SL	0.15 + 0.106*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.042*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
RN to QN0	t_{PLH}	0.73	0.62 + 0.052*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
SN to QN0	t_{PLH}	0.42	0.31 + 0.054*SL	0.32 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.036*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN1	t_{PLH}	1.26	1.15 + 0.052*SL	1.16 + 0.050*SL	1.16 + 0.050*SL
	t_{PHL}	1.01	0.94 + 0.034*SL	0.96 + 0.026*SL	1.00 + 0.024*SL
	t_R	0.36	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
RN to QN1	t_{PLH}	0.73	0.62 + 0.052*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
SN to QN1	t_{PLH}	0.42	0.31 + 0.054*SL	0.32 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.036*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

Dn	CK	RN	SN	Qn (n+1)	QNn (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
KG80				
Dn	CK	RN	SN	
1.0	1.1	8.3	8.0	32.0
KGM80				
Dn	CK	RN	SN	
1.0	1.0	9.7	9.6	32.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.83	1.30
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	1.02
Input Setup Time (D0 to CK)	t_{SU}	0.23	0.46
Input Hold Time (D0 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D1 to CK)	t_{SU}	0.23	0.46
Input Hold Time (D1 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D2 to CK)	t_{SU}	0.23	0.46
Input Hold Time (D2 to CK)	t_{HD}	0.26	0.43
Input Setup Time (D3 to CK)	t_{SU}	0.23	0.46
Input Hold Time (D3 to CK)	t_{HD}	0.26	0.43
Recovery Time (RN)	t_{RC}	0.15	0.33
Input Hold Time (RN to CK)	t_{HD}	0.59	1.07
Recovery Time (SN)	t_{RC}	0.15	0.33
Input Hold Time (RN to CK)	t_{HD}	0.37	0.63

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD4X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.74	0.65 + 0.045*SL	0.65 + 0.042*SL	0.66 + 0.042*SL
	t_{PHL}	0.89	0.83 + 0.031*SL	0.84 + 0.026*SL	0.85 + 0.024*SL
	t_R	0.29	0.11 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.039*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q0	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.12 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q0	t_{PLH}	0.65	0.56 + 0.044*SL	0.57 + 0.041*SL	0.56 + 0.042*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
CK to Q1	t_{PLH}	0.73	0.64 + 0.044*SL	0.65 + 0.042*SL	0.65 + 0.042*SL
	t_{PHL}	0.88	0.82 + 0.031*SL	0.83 + 0.026*SL	0.85 + 0.024*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q1	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.29 + 0.024*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q1	t_{PLH}	0.65	0.56 + 0.043*SL	0.56 + 0.041*SL	0.56 + 0.041*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
CK to Q2	t_{PLH}	0.73	0.64 + 0.044*SL	0.65 + 0.042*SL	0.65 + 0.042*SL
	t_{PHL}	0.88	0.82 + 0.031*SL	0.83 + 0.026*SL	0.85 + 0.024*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.089*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q2	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.29 + 0.024*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q2	t_{PLH}	0.64	0.56 + 0.043*SL	0.56 + 0.041*SL	0.56 + 0.042*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
CK to Q3	t_{PLH}	0.74	0.65 + 0.045*SL	0.65 + 0.042*SL	0.66 + 0.042*SL
	t_{PHL}	0.89	0.83 + 0.031*SL	0.84 + 0.026*SL	0.85 + 0.024*SL
	t_R	0.29	0.11 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.039*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q3	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.12 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q3	t_{PLH}	0.65	0.56 + 0.044*SL	0.57 + 0.041*SL	0.56 + 0.042*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.088*SL	0.09 + 0.090*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD4X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.09	1.01 + 0.042*SL	1.01 + 0.041*SL	1.01 + 0.041*SL
	t_{PHL}	0.82	0.76 + 0.031*SL	0.77 + 0.025*SL	0.79 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN0	t_{PLH}	0.54	0.45 + 0.042*SL	0.46 + 0.041*SL	0.45 + 0.042*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
SN to QN0	t_{PLH}	0.31	0.22 + 0.044*SL	0.22 + 0.041*SL	0.22 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CK to QN1	t_{PLH}	1.09	1.00 + 0.042*SL	1.01 + 0.041*SL	1.01 + 0.041*SL
	t_{PHL}	0.82	0.76 + 0.031*SL	0.77 + 0.025*SL	0.78 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.040*SL	0.08 + 0.041*SL
RN to QN1	t_{PLH}	0.54	0.46 + 0.042*SL	0.46 + 0.041*SL	0.46 + 0.042*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
SN to QN1	t_{PLH}	0.31	0.22 + 0.043*SL	0.23 + 0.042*SL	0.23 + 0.041*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_R	0.28	0.12 + 0.085*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to QN2	t_{PLH}	1.09	1.01 + 0.042*SL	1.01 + 0.041*SL	1.01 + 0.041*SL
	t_{PHL}	0.82	0.76 + 0.030*SL	0.77 + 0.025*SL	0.78 + 0.024*SL
	t_R	0.29	0.12 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to QN2	t_{PLH}	0.54	0.46 + 0.042*SL	0.46 + 0.041*SL	0.46 + 0.041*SL
	t_R	0.29	0.12 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
SN to QN2	t_{PLH}	0.31	0.23 + 0.044*SL	0.23 + 0.041*SL	0.23 + 0.041*SL
	t_{PHL}	0.34	0.28 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
CK to QN3	t_{PLH}	1.09	1.01 + 0.042*SL	1.01 + 0.041*SL	1.01 + 0.041*SL
	t_{PHL}	0.82	0.76 + 0.031*SL	0.77 + 0.025*SL	0.79 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN3	t_{PLH}	0.54	0.45 + 0.042*SL	0.46 + 0.041*SL	0.45 + 0.042*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
SN to QN3	t_{PLH}	0.31	0.22 + 0.044*SL	0.22 + 0.041*SL	0.22 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD4X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.99	0.88 + 0.054*SL	0.89 + 0.051*SL	0.90 + 0.050*SL
	t_{PHL}	1.24	1.17 + 0.035*SL	1.20 + 0.027*SL	1.23 + 0.024*SL
	t_R	0.37	0.16 + 0.106*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q0	t_{PLH}	0.39	0.28 + 0.054*SL	0.29 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.036*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q0	t_{PLH}	0.90	0.79 + 0.054*SL	0.80 + 0.050*SL	0.81 + 0.050*SL
	t_R	0.37	0.16 + 0.103*SL	0.16 + 0.106*SL	0.13 + 0.109*SL
CK to Q1	t_{PLH}	0.98	0.87 + 0.054*SL	0.88 + 0.051*SL	0.89 + 0.050*SL
	t_{PHL}	1.24	1.17 + 0.034*SL	1.19 + 0.027*SL	1.22 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q1	t_{PLH}	0.39	0.28 + 0.054*SL	0.29 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.036*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q1	t_{PLH}	0.90	0.79 + 0.054*SL	0.80 + 0.050*SL	0.80 + 0.050*SL
	t_R	0.37	0.17 + 0.103*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
CK to Q2	t_{PLH}	0.98	0.87 + 0.054*SL	0.88 + 0.051*SL	0.89 + 0.050*SL
	t_{PHL}	1.24	1.17 + 0.034*SL	1.19 + 0.027*SL	1.22 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q2	t_{PLH}	0.39	0.28 + 0.054*SL	0.29 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.035*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.042*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q2	t_{PLH}	0.90	0.79 + 0.054*SL	0.80 + 0.050*SL	0.80 + 0.050*SL
	t_R	0.37	0.17 + 0.104*SL	0.16 + 0.106*SL	0.14 + 0.109*SL
CK to Q3	t_{PLH}	0.99	0.88 + 0.054*SL	0.89 + 0.051*SL	0.90 + 0.050*SL
	t_{PHL}	1.24	1.17 + 0.035*SL	1.20 + 0.027*SL	1.23 + 0.024*SL
	t_R	0.37	0.16 + 0.106*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q3	t_{PLH}	0.39	0.28 + 0.054*SL	0.29 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.036*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q3	t_{PLH}	0.90	0.79 + 0.054*SL	0.80 + 0.050*SL	0.81 + 0.050*SL
	t_R	0.37	0.16 + 0.103*SL	0.16 + 0.106*SL	0.13 + 0.109*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD4X4

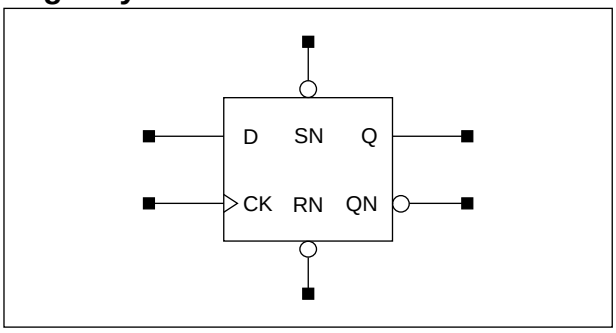
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.54	1.43 + 0.052*SL	1.44 + 0.050*SL	1.44 + 0.050*SL
	t_{PHL}	1.14	1.07 + 0.034*SL	1.09 + 0.026*SL	1.12 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
RN to QN0	t_{PLH}	0.73	0.62 + 0.052*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
SN to QN0	t_{PLH}	0.42	0.31 + 0.055*SL	0.32 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN1	t_{PLH}	1.54	1.44 + 0.052*SL	1.44 + 0.050*SL	1.44 + 0.050*SL
	t_{PHL}	1.13	1.06 + 0.034*SL	1.09 + 0.026*SL	1.12 + 0.024*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.106*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to QN1	t_{PLH}	0.73	0.63 + 0.053*SL	0.64 + 0.050*SL	0.64 + 0.050*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.106*SL	0.13 + 0.109*SL
SN to QN1	t_{PLH}	0.43	0.32 + 0.054*SL	0.33 + 0.050*SL	0.34 + 0.050*SL
	t_{PHL}	0.45	0.37 + 0.037*SL	0.40 + 0.027*SL	0.44 + 0.024*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN2	t_{PLH}	1.54	1.44 + 0.052*SL	1.44 + 0.050*SL	1.44 + 0.050*SL
	t_{PHL}	1.13	1.07 + 0.034*SL	1.09 + 0.026*SL	1.12 + 0.024*SL
	t_R	0.38	0.17 + 0.104*SL	0.16 + 0.106*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
RN to QN2	t_{PLH}	0.74	0.63 + 0.052*SL	0.64 + 0.050*SL	0.64 + 0.050*SL
	t_R	0.38	0.17 + 0.104*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
SN to QN2	t_{PLH}	0.43	0.32 + 0.054*SL	0.33 + 0.050*SL	0.34 + 0.050*SL
	t_{PHL}	0.45	0.38 + 0.037*SL	0.40 + 0.027*SL	0.44 + 0.024*SL
	t_R	0.38	0.17 + 0.103*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.22	0.14 + 0.044*SL	0.14 + 0.041*SL	0.14 + 0.042*SL
CK to QN3	t_{PLH}	1.54	1.43 + 0.052*SL	1.44 + 0.050*SL	1.44 + 0.050*SL
	t_{PHL}	1.14	1.07 + 0.034*SL	1.09 + 0.026*SL	1.12 + 0.024*SL
	t_R	0.36	0.16 + 0.104*SL	0.15 + 0.106*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
RN to QN3	t_{PLH}	0.73	0.62 + 0.052*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
SN to QN3	t_{PLH}	0.42	0.31 + 0.055*SL	0.32 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

YFD4/YFD4D2

Fast D Flip-Flop with Reset, Set, 1X/2X Drive

Logic Symbol



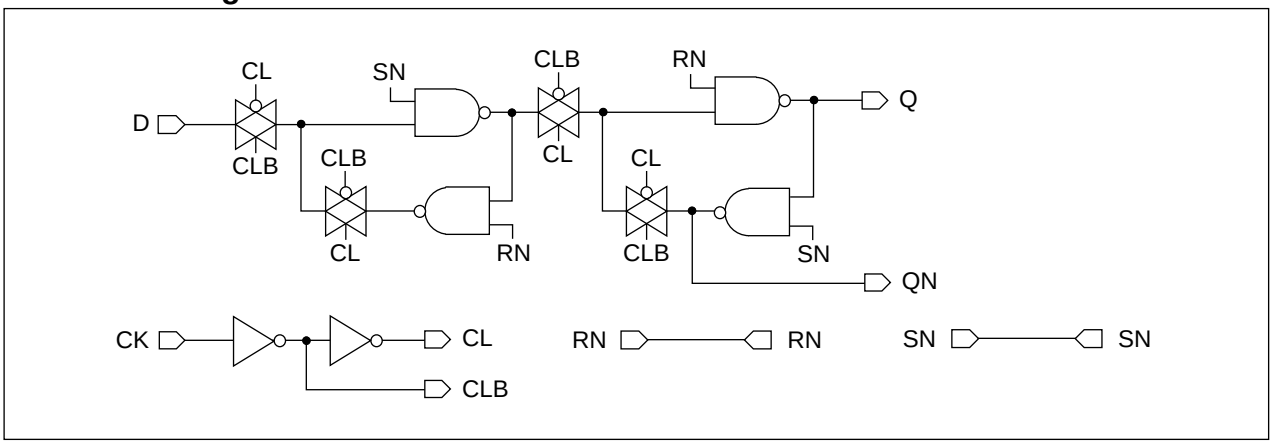
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	1
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
KG80									
YFD4				*YFD4D2*				*YFD4*	*YFD4D2*
D	CK	RN	SN	D	CK	RN	SN		
2.8	0.8	1.2	1.5	2.8	0.8	1.9	2.3	7.0	9.0
KGM80									
YFD4				*YFD4D2*				*YFD4*	*YFD4D2*
D	CK	RN	SN	D	CK	RN	SN		
3.5	0.9	1.4	1.8	3.6	0.9	2.3	2.6	7.0	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		YFD4	YFD4D2	YFD4	YFD4D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	1.02
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.28	0.31	0.61	0.58
Input Hold Time (D to CK)	t_{HD}	0.26	0.26	0.46	0.46
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.20	0.20	0.41	0.41
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.85	0.85

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YFD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.53	0.44 + 0.045*SL	0.45 + 0.043*SL	0.45 + 0.042*SL
	t_{PHL}	0.44	0.36 + 0.038*SL	0.37 + 0.036*SL	0.38 + 0.035*SL
	t_R	0.45	0.29 + 0.081*SL	0.28 + 0.087*SL	0.26 + 0.089*SL
	t_F	0.31	0.18 + 0.065*SL	0.17 + 0.067*SL	0.16 + 0.068*SL
RN to Q	t_{PHL}	0.50	0.42 + 0.042*SL	0.43 + 0.036*SL	0.44 + 0.035*SL
	t_F	0.32	0.19 + 0.062*SL	0.18 + 0.067*SL	0.18 + 0.067*SL
SN to Q	t_{PLH}	0.25	0.17 + 0.042*SL	0.17 + 0.041*SL	0.22 + 0.034*SL
	t_{PHL}	0.18	0.10 + 0.041*SL	0.11 + 0.034*SL	0.12 + 0.034*SL
	t_R	0.40	0.25 + 0.076*SL	0.31 + 0.049*SL	0.37 + 0.041*SL
	t_F	0.33	0.22 + 0.056*SL	0.20 + 0.062*SL	0.18 + 0.065*SL
CK to QN	t_{PLH}	0.67	0.48 + 0.097*SL	0.48 + 0.095*SL	0.49 + 0.094*SL
	t_{PHL}	0.72	0.54 + 0.092*SL	0.54 + 0.090*SL	0.55 + 0.089*SL
	t_R	0.37	0.18 + 0.099*SL	0.17 + 0.100*SL	0.17 + 0.100*SL
	t_F	0.33	0.16 + 0.086*SL	0.16 + 0.086*SL	0.16 + 0.086*SL
RN to QN	t_{PLH}	0.28	0.20 + 0.041*SL	0.20 + 0.041*SL	0.21 + 0.040*SL
	t_{PHL}	0.18	0.10 + 0.038*SL	0.11 + 0.034*SL	0.11 + 0.034*SL
	t_R	0.42	0.29 + 0.064*SL	0.30 + 0.061*SL	0.29 + 0.062*SL
	t_F	0.31	0.20 + 0.060*SL	0.18 + 0.064*SL	0.16 + 0.067*SL
SN to QN	t_{PHL}	0.44	0.26 + 0.089*SL	0.27 + 0.083*SL	0.36 + 0.071*SL
	t_F	0.32	0.15 + 0.084*SL	0.17 + 0.076*SL	0.21 + 0.070*SL

KG80 YFD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.49	0.44 + 0.024*SL	0.45 + 0.023*SL	0.46 + 0.022*SL
	t_{PHL}	0.43	0.39 + 0.023*SL	0.39 + 0.021*SL	0.41 + 0.019*SL
	t_R	0.34	0.26 + 0.040*SL	0.25 + 0.042*SL	0.24 + 0.044*SL
	t_F	0.28	0.21 + 0.033*SL	0.21 + 0.033*SL	0.21 + 0.033*SL
RN to Q	t_{PHL}	0.50	0.45 + 0.027*SL	0.46 + 0.022*SL	0.48 + 0.019*SL
	t_F	0.29	0.22 + 0.032*SL	0.22 + 0.032*SL	0.22 + 0.033*SL
SN to Q	t_{PLH}	0.24	0.20 + 0.020*SL	0.20 + 0.020*SL	0.20 + 0.021*SL
	t_{PHL}	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.10 + 0.018*SL
	t_R	0.39	0.32 + 0.036*SL	0.33 + 0.031*SL	0.39 + 0.022*SL
	t_F	0.26	0.20 + 0.030*SL	0.19 + 0.031*SL	0.18 + 0.032*SL
CK to QN	t_{PLH}	0.59	0.49 + 0.054*SL	0.49 + 0.051*SL	0.50 + 0.049*SL
	t_{PHL}	0.62	0.52 + 0.048*SL	0.52 + 0.047*SL	0.53 + 0.045*SL
	t_R	0.25	0.16 + 0.048*SL	0.15 + 0.050*SL	0.15 + 0.051*SL
	t_F	0.21	0.13 + 0.041*SL	0.13 + 0.043*SL	0.13 + 0.042*SL
RN to QN	t_{PLH}	0.23	0.19 + 0.022*SL	0.19 + 0.020*SL	0.19 + 0.021*SL
	t_{PHL}	0.12	0.08 + 0.022*SL	0.09 + 0.018*SL	0.10 + 0.017*SL
	t_R	0.33	0.26 + 0.038*SL	0.27 + 0.035*SL	0.29 + 0.032*SL
	t_F	0.24	0.18 + 0.027*SL	0.18 + 0.030*SL	0.16 + 0.032*SL
SN to QN	t_{PHL}	0.37	0.28 + 0.045*SL	0.28 + 0.044*SL	0.30 + 0.041*SL
	t_F	0.22	0.14 + 0.042*SL	0.14 + 0.042*SL	0.17 + 0.038*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YFD4

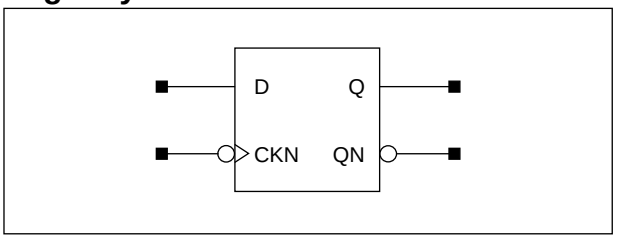
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.75	0.64 + 0.054*SL	0.65 + 0.051*SL	0.67 + 0.050*SL
	t_{PHL}	0.62	0.53 + 0.044*SL	0.55 + 0.039*SL	0.56 + 0.038*SL
	t_R	0.60	0.40 + 0.101*SL	0.38 + 0.106*SL	0.36 + 0.108*SL
	t_F	0.38	0.24 + 0.073*SL	0.24 + 0.073*SL	0.23 + 0.073*SL
RN to Q	t_{PHL}	0.71	0.61 + 0.049*SL	0.63 + 0.041*SL	0.67 + 0.037*SL
	t_F	0.40	0.26 + 0.070*SL	0.26 + 0.072*SL	0.24 + 0.073*SL
SN to Q	t_{PLH}	0.31	0.21 + 0.051*SL	0.21 + 0.050*SL	0.37 + 0.036*SL
	t_{PHL}	0.22	0.13 + 0.044*SL	0.15 + 0.038*SL	0.15 + 0.037*SL
	t_R	0.51	0.31 + 0.102*SL	0.41 + 0.062*SL	0.55 + 0.050*SL
	t_F	0.37	0.24 + 0.067*SL	0.23 + 0.071*SL	0.20 + 0.073*SL
CK to QN	t_{PLH}	0.94	0.71 + 0.115*SL	0.72 + 0.111*SL	0.73 + 0.109*SL
	t_{PHL}	1.01	0.79 + 0.112*SL	0.80 + 0.108*SL	0.81 + 0.107*SL
	t_R	0.51	0.27 + 0.118*SL	0.27 + 0.119*SL	0.26 + 0.119*SL
	t_F	0.41	0.22 + 0.094*SL	0.22 + 0.094*SL	0.21 + 0.095*SL
RN to QN	t_{PLH}	0.36	0.26 + 0.050*SL	0.26 + 0.050*SL	0.28 + 0.048*SL
	t_{PHL}	0.23	0.15 + 0.041*SL	0.16 + 0.038*SL	0.17 + 0.037*SL
	t_R	0.56	0.37 + 0.094*SL	0.42 + 0.077*SL	0.42 + 0.077*SL
	t_F	0.36	0.23 + 0.068*SL	0.22 + 0.072*SL	0.20 + 0.074*SL
SN to QN	t_{PHL}	0.57	0.35 + 0.108*SL	0.38 + 0.098*SL	0.57 + 0.081*SL
	t_F	0.39	0.20 + 0.093*SL	0.23 + 0.082*SL	0.28 + 0.078*SL

KGM80 YFD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.63 + 0.030*SL	0.64 + 0.027*SL	0.66 + 0.026*SL
	t_{PHL}	0.63	0.58 + 0.028*SL	0.59 + 0.023*SL	0.62 + 0.021*SL
	t_R	0.45	0.35 + 0.049*SL	0.35 + 0.051*SL	0.33 + 0.053*SL
	t_F	0.37	0.29 + 0.039*SL	0.29 + 0.037*SL	0.31 + 0.036*SL
RN to Q	t_{PHL}	0.71	0.65 + 0.033*SL	0.67 + 0.025*SL	0.72 + 0.020*SL
	t_F	0.39	0.31 + 0.037*SL	0.32 + 0.035*SL	0.32 + 0.035*SL
SN to Q	t_{PLH}	0.31	0.26 + 0.025*SL	0.26 + 0.025*SL	0.25 + 0.026*SL
	t_{PHL}	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.15 + 0.019*SL
	t_R	0.49	0.39 + 0.047*SL	0.41 + 0.041*SL	0.57 + 0.026*SL
	t_F	0.29	0.22 + 0.034*SL	0.22 + 0.036*SL	0.21 + 0.036*SL
CK to QN	t_{PLH}	0.86	0.73 + 0.064*SL	0.74 + 0.059*SL	0.78 + 0.056*SL
	t_{PHL}	0.87	0.75 + 0.058*SL	0.76 + 0.055*SL	0.78 + 0.054*SL
	t_R	0.34	0.22 + 0.059*SL	0.22 + 0.059*SL	0.22 + 0.059*SL
	t_F	0.27	0.18 + 0.046*SL	0.18 + 0.046*SL	0.17 + 0.047*SL
RN to QN	t_{PLH}	0.29	0.24 + 0.026*SL	0.24 + 0.025*SL	0.24 + 0.025*SL
	t_{PHL}	0.17	0.12 + 0.022*SL	0.13 + 0.020*SL	0.14 + 0.018*SL
	t_R	0.41	0.32 + 0.049*SL	0.32 + 0.047*SL	0.40 + 0.039*SL
	t_F	0.26	0.20 + 0.033*SL	0.19 + 0.034*SL	0.18 + 0.036*SL
SN to QN	t_{PHL}	0.48	0.38 + 0.054*SL	0.38 + 0.053*SL	0.44 + 0.048*SL
	t_F	0.28	0.18 + 0.047*SL	0.19 + 0.045*SL	0.26 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



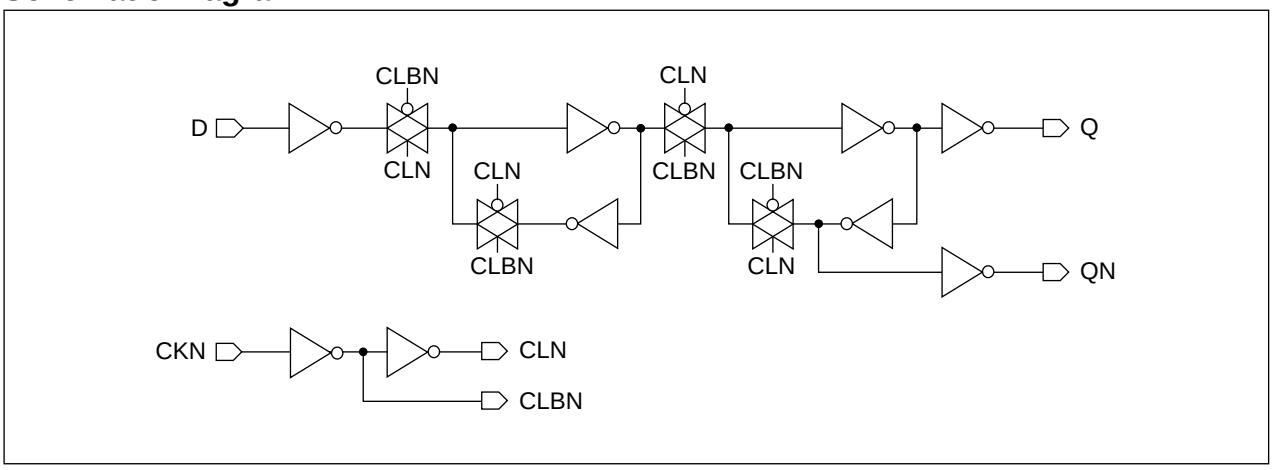
Truth Table

D	CKN	Q (n+1)	QN (n+1)
0	↓	0	1
1	↓	1	0
x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
FD5		*FD5D2*		*FD5*	*FD5D2*
D	CKN	D	CKN		
0.9	0.9	0.9	0.9	7.0	8.0
KGM80					
FD5		*FD5D2*		*FD5*	*FD5D2*
D	CKN	D	CKN		
1.0	1.0	1.0	1.0	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD5	FD5D2	FD5	FD5D2
Pulse Width Low (CKN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CKN)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CKN)	t_{SU}	0.31	0.31	0.58	0.58
Input Hold Time (D to CKN)	t_{HD}	0.26	0.26	0.49	0.49

FD5/FD5D2

D Flip-Flop with Negative Edge Trigger, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.64	0.56 + 0.042*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.56	0.50 + 0.031*SL	0.51 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CKN to QN	t_{PLH}	0.70	0.62 + 0.040*SL	0.61 + 0.041*SL	0.61 + 0.042*SL
	t_{PHL}	0.71	0.66 + 0.029*SL	0.67 + 0.025*SL	0.68 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 FD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.62	0.58 + 0.023*SL	0.58 + 0.021*SL	0.58 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.021*SL	0.53 + 0.015*SL	0.54 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.045*SL
	t_F	0.14	0.09 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
CKN to QN	t_{PLH}	0.73	0.69 + 0.019*SL	0.69 + 0.019*SL	0.68 + 0.020*SL
	t_{PHL}	0.75	0.72 + 0.018*SL	0.73 + 0.015*SL	0.74 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.88	0.78 + 0.051*SL	0.78 + 0.050*SL	0.79 + 0.050*SL
	t_{PHL}	0.76	0.69 + 0.034*SL	0.71 + 0.026*SL	0.74 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CKN to QN	t_{PLH}	0.95	0.86 + 0.049*SL	0.85 + 0.050*SL	0.85 + 0.050*SL
	t_{PHL}	1.00	0.94 + 0.033*SL	0.96 + 0.026*SL	0.98 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

KGM80 FD5D2

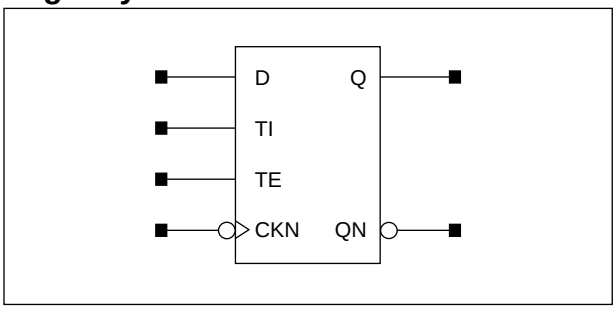
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.86	0.80 + 0.028*SL	0.81 + 0.025*SL	0.81 + 0.025*SL
	t_{PHL}	0.77	0.72 + 0.023*SL	0.74 + 0.016*SL	0.77 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.14 + 0.020*SL
CKN to QN	t_{PLH}	1.00	0.95 + 0.024*SL	0.95 + 0.024*SL	0.95 + 0.025*SL
	t_{PHL}	1.06	1.02 + 0.021*SL	1.03 + 0.016*SL	1.06 + 0.013*SL
	t_R	0.22	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FD5S/FD5SD2

D Flip-Flop with Negative Edge Trigger, Scan, 1X/2X Drive

Logic Symbol



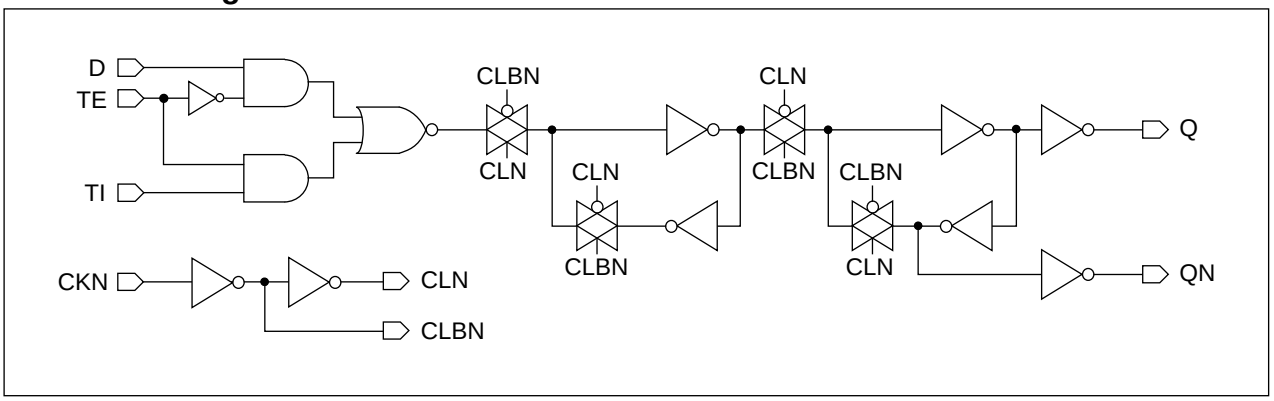
Truth Table

D	TI	TE	CKN	Q (n+1)	QN (n+1)
0	x	0	↓	0	1
1	x	0	↓	1	0
x	0	1	↓	0	1
x	1	1	↓	1	0
x	x	x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
KG80									
FD5S				*FD5SD2*				*FD5S*	*FD5SD2*
D	TI	TE	CKN	D	TI	TE	CKN		
0.6	0.8	1.7	0.9	0.6	0.8	1.7	0.9	9.0	10.0
KGM80									
FD5S				*FD5SD2*				*FD5S*	*FD5SD2*
D	TI	TE	CKN	D	TI	TE	CKN		
1.0	1.0	2.1	1.0	1.0	1.0	2.1	1.0	9.0	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD5S	FD5SD2	FD5S	FD5SD2
Pulse Width Low (CKN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CKN)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CKN)	t_{SU}	0.39	0.39	0.74	0.74
Input Hold Time (D to CKN)	t_{HD}	0.17	0.17	0.36	0.36
Input Setup Time (TI to CKN)	t_{SU}	0.45	0.45	0.83	0.83
Input Hold Time (TI to CKN)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CKN)	t_{SU}	0.45	0.45	0.77	0.77
Input Hold Time (TE to CKN)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.63	0.55 + 0.042*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.56	0.50 + 0.031*SL	0.51 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CKN to QN	t_{PLH}	0.69	0.61 + 0.040*SL	0.61 + 0.041*SL	0.61 + 0.042*SL
	t_{PHL}	0.71	0.65 + 0.030*SL	0.66 + 0.025*SL	0.68 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 FD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.62	0.57 + 0.023*SL	0.58 + 0.021*SL	0.58 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.020*SL	0.53 + 0.015*SL	0.54 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
CKN to QN	t_{PLH}	0.73	0.69 + 0.019*SL	0.69 + 0.019*SL	0.68 + 0.020*SL
	t_{PHL}	0.75	0.71 + 0.019*SL	0.72 + 0.015*SL	0.73 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD5S

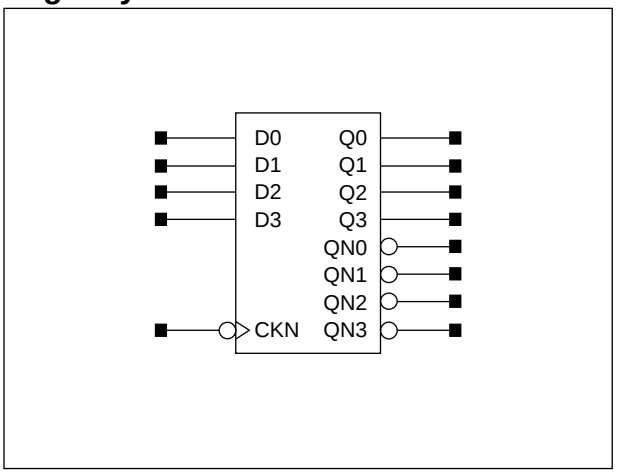
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.88	0.77 + 0.051*SL	0.78 + 0.050*SL	0.78 + 0.050*SL
	t_{PHL}	0.76	0.69 + 0.034*SL	0.71 + 0.026*SL	0.74 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CKN to QN	t_{PLH}	0.95	0.85 + 0.049*SL	0.85 + 0.050*SL	0.85 + 0.050*SL
	t_{PHL}	1.00	0.93 + 0.033*SL	0.95 + 0.026*SL	0.98 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

KGM80 FD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.85	0.79 + 0.028*SL	0.80 + 0.025*SL	0.80 + 0.025*SL
	t_{PHL}	0.76	0.72 + 0.023*SL	0.74 + 0.016*SL	0.77 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.14 + 0.021*SL
CKN to QN	t_{PLH}	1.00	0.95 + 0.024*SL	0.95 + 0.024*SL	0.94 + 0.025*SL
	t_{PHL}	1.05	1.01 + 0.021*SL	1.03 + 0.016*SL	1.06 + 0.013*SL
	t_R	0.22	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

Dn	CKN	Qn (n+1)	QNn (n+1)
0	↓	0	1
1	↓	1	0
x	↑	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
KG80		
Dn	CKN	
0.9	0.9	24.0
KGM80		
Dn	CKN	
1.0	1.1	24.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CKN)	t_{PWL}	0.80	1.27
Pulse Width High (CKN)	t_{PWH}	0.61	0.99
Input Setup Time (D0 to CKN)	t_{SU}	0.17	0.39
Input Hold Time (D0 to CKN)	t_{HD}	0.47	0.83
Input Setup Time (D1 to CKN)	t_{SU}	0.17	0.39
Input Hold Time (D1 to CKN)	t_{HD}	0.47	0.83
Input Setup Time (D2 to CKN)	t_{SU}	0.17	0.39
Input Hold Time (D2 to CKN)	t_{HD}	0.47	0.83
Input Setup Time (D3 to CKN)	t_{SU}	0.17	0.39
Input Hold Time (D3 to CKN)	t_{HD}	0.47	0.83

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q0	t_{PLH}	0.98	0.89 + 0.042*SL	0.89 + 0.041*SL	0.89 + 0.042*SL
	t_{PHL}	0.76	0.69 + 0.031*SL	0.71 + 0.026*SL	0.72 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CKN to Q1	t_{PLH}	0.98	0.90 + 0.042*SL	0.90 + 0.041*SL	0.90 + 0.042*SL
	t_{PHL}	0.76	0.70 + 0.031*SL	0.71 + 0.026*SL	0.73 + 0.023*SL
	t_R	0.28	0.10 + 0.085*SL	0.10 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
CKN to Q2	t_{PLH}	0.98	0.90 + 0.042*SL	0.90 + 0.041*SL	0.90 + 0.042*SL
	t_{PHL}	0.76	0.70 + 0.031*SL	0.71 + 0.026*SL	0.73 + 0.023*SL
	t_R	0.28	0.10 + 0.086*SL	0.10 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
CKN to Q3	t_{PLH}	0.98	0.89 + 0.042*SL	0.89 + 0.041*SL	0.89 + 0.042*SL
	t_{PHL}	0.76	0.69 + 0.031*SL	0.71 + 0.026*SL	0.72 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CKN to QN0	t_{PLH}	0.87	0.79 + 0.040*SL	0.79 + 0.041*SL	0.79 + 0.041*SL
	t_{PHL}	1.05	1.00 + 0.029*SL	1.01 + 0.025*SL	1.02 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CKN to QN1	t_{PLH}	0.88	0.80 + 0.040*SL	0.80 + 0.041*SL	0.79 + 0.042*SL
	t_{PHL}	1.06	1.00 + 0.030*SL	1.01 + 0.025*SL	1.02 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CKN to QN2	t_{PLH}	0.88	0.80 + 0.040*SL	0.80 + 0.041*SL	0.79 + 0.042*SL
	t_{PHL}	1.06	1.00 + 0.030*SL	1.01 + 0.025*SL	1.02 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CKN to QN3	t_{PLH}	0.87	0.79 + 0.040*SL	0.79 + 0.041*SL	0.79 + 0.041*SL
	t_{PHL}	1.05	1.00 + 0.029*SL	1.01 + 0.025*SL	1.02 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD5X4

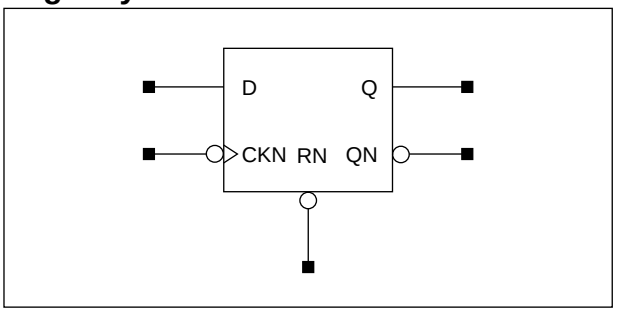
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q0	t_{PLH}	1.37	1.27 + 0.051*SL	1.27 + 0.050*SL	1.28 + 0.050*SL
	t_{PHL}	1.04	0.97 + 0.034*SL	0.99 + 0.026*SL	1.02 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CKN to Q1	t_{PLH}	1.38	1.28 + 0.051*SL	1.28 + 0.050*SL	1.28 + 0.050*SL
	t_{PHL}	1.05	0.98 + 0.034*SL	1.00 + 0.026*SL	1.03 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CKN to Q2	t_{PLH}	1.38	1.28 + 0.051*SL	1.28 + 0.050*SL	1.28 + 0.050*SL
	t_{PHL}	1.05	0.98 + 0.034*SL	1.00 + 0.026*SL	1.03 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CKN to Q3	t_{PLH}	1.37	1.27 + 0.051*SL	1.27 + 0.050*SL	1.28 + 0.050*SL
	t_{PHL}	1.04	0.97 + 0.034*SL	0.99 + 0.026*SL	1.03 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CKN to QN0	t_{PLH}	1.22	1.12 + 0.049*SL	1.12 + 0.050*SL	1.12 + 0.050*SL
	t_{PHL}	1.49	1.43 + 0.033*SL	1.45 + 0.026*SL	1.47 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
CKN to QN1	t_{PLH}	1.23	1.13 + 0.049*SL	1.13 + 0.050*SL	1.13 + 0.050*SL
	t_{PHL}	1.50	1.44 + 0.033*SL	1.46 + 0.026*SL	1.48 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.11 + 0.042*SL	0.11 + 0.042*SL
CKN to QN2	t_{PLH}	1.23	1.13 + 0.049*SL	1.13 + 0.050*SL	1.13 + 0.050*SL
	t_{PHL}	1.50	1.44 + 0.033*SL	1.46 + 0.026*SL	1.48 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
CKN to QN3	t_{PLH}	1.22	1.12 + 0.049*SL	1.12 + 0.050*SL	1.12 + 0.050*SL
	t_{PHL}	1.49	1.43 + 0.033*SL	1.45 + 0.026*SL	1.47 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FD6/FD6D2

D Flip-Flop with Negative Edge Trigger, Reset, 1X/2X Drive

Logic Symbol



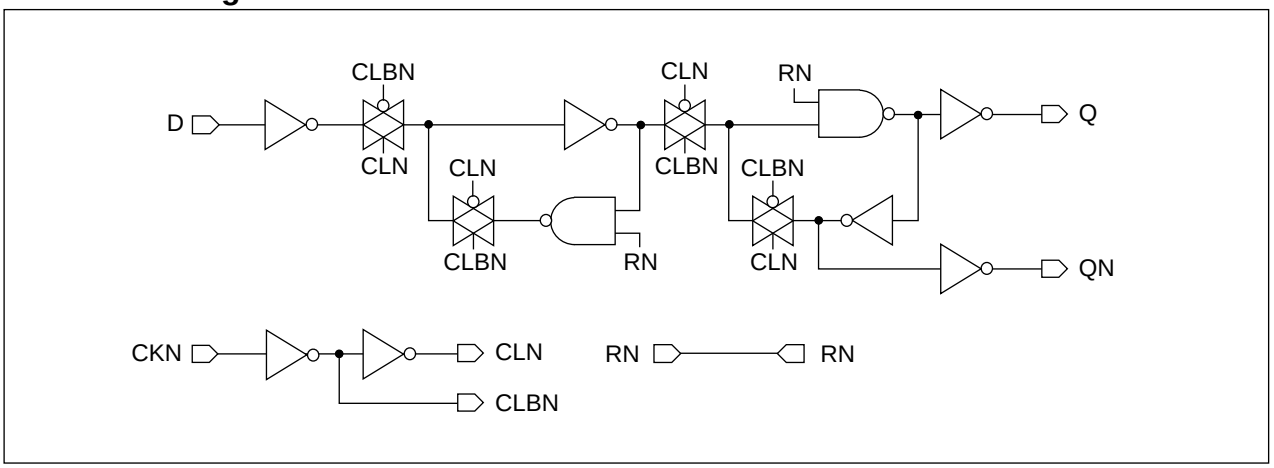
Truth Table

D	CKN	RN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	0	1
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FD6			*FD6D2*			*FD6*	*FD6D2*
D	CKN	RN	D	CKN	RN		
0.9	0.9	1.6	0.9	0.9	1.6	8.0	9.0
KGM80							
FD6			*FD6D2*			*FD6*	*FD6D2*
D	CKN	RN	D	CKN	RN		
1.0	1.0	1.9	1.0	1.0	1.9	8.0	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD6	FD6D2	FD6	FD6D2
Pulse Width Low (CKN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CKN)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CKN)	t_{SU}	0.31	0.31	0.58	0.58
Input Hold Time (D to CKN)	t_{HD}	0.26	0.26	0.49	0.49
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.53	0.53	0.85	0.85

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.70	0.61 + 0.044*SL	0.61 + 0.042*SL	0.62 + 0.042*SL
	t_{PHL}	0.57	0.51 + 0.031*SL	0.52 + 0.026*SL	0.54 + 0.023*SL
	t_R	0.28	0.11 + 0.087*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to Q	t_{PHL}	0.33	0.27 + 0.033*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CKN to QN	t_{PLH}	0.70	0.62 + 0.040*SL	0.62 + 0.041*SL	0.62 + 0.042*SL
	t_{PHL}	0.77	0.71 + 0.029*SL	0.72 + 0.025*SL	0.73 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
RN to QN	t_{PLH}	0.47	0.38 + 0.040*SL	0.38 + 0.041*SL	0.38 + 0.042*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL

KG80 FD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.70	0.65 + 0.023*SL	0.66 + 0.022*SL	0.66 + 0.021*SL
	t_{PHL}	0.58	0.54 + 0.019*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_R	0.21	0.13 + 0.043*SL	0.12 + 0.043*SL	0.12 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PHL}	0.34	0.29 + 0.020*SL	0.31 + 0.016*SL	0.32 + 0.013*SL
	t_F	0.17	0.12 + 0.021*SL	0.13 + 0.020*SL	0.13 + 0.019*SL
CKN to QN	t_{PLH}	0.73	0.69 + 0.020*SL	0.69 + 0.019*SL	0.69 + 0.020*SL
	t_{PHL}	0.82	0.78 + 0.018*SL	0.79 + 0.015*SL	0.81 + 0.013*SL
	t_R	0.16	0.08 + 0.042*SL	0.08 + 0.043*SL	0.06 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
RN to QN	t_{PLH}	0.49	0.45 + 0.019*SL	0.45 + 0.019*SL	0.45 + 0.020*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD6

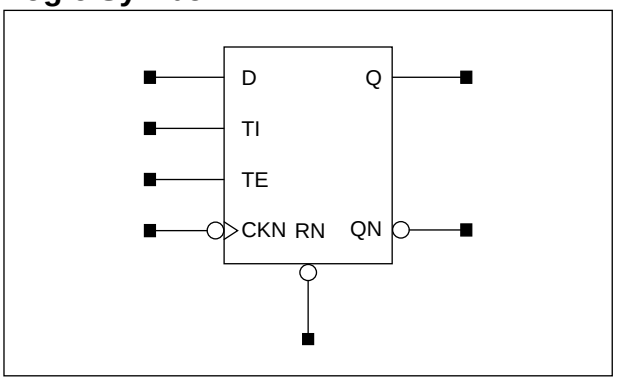
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.97	0.86 + 0.054*SL	0.87 + 0.051*SL	0.88 + 0.050*SL
	t_{PHL}	0.78	0.71 + 0.035*SL	0.73 + 0.027*SL	0.76 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to Q	t_{PHL}	0.43	0.36 + 0.036*SL	0.38 + 0.027*SL	0.42 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CKN to QN	t_{PLH}	0.97	0.87 + 0.049*SL	0.87 + 0.050*SL	0.87 + 0.050*SL
	t_{PHL}	1.08	1.02 + 0.032*SL	1.04 + 0.025*SL	1.06 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
RN to QN	t_{PLH}	0.62	0.52 + 0.049*SL	0.52 + 0.050*SL	0.52 + 0.050*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL

KGM80 FD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.97	0.91 + 0.030*SL	0.92 + 0.026*SL	0.93 + 0.025*SL
	t_{PHL}	0.80	0.75 + 0.022*SL	0.77 + 0.016*SL	0.80 + 0.013*SL
	t_R	0.28	0.17 + 0.053*SL	0.18 + 0.052*SL	0.17 + 0.053*SL
	t_F	0.18	0.14 + 0.023*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
RN to Q	t_{PHL}	0.44	0.40 + 0.023*SL	0.42 + 0.017*SL	0.45 + 0.013*SL
	t_F	0.20	0.15 + 0.024*SL	0.16 + 0.021*SL	0.17 + 0.020*SL
CKN to QN	t_{PLH}	1.01	0.96 + 0.025*SL	0.96 + 0.024*SL	0.96 + 0.025*SL
	t_{PHL}	1.16	1.12 + 0.021*SL	1.13 + 0.016*SL	1.16 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
RN to QN	t_{PLH}	0.66	0.61 + 0.025*SL	0.61 + 0.024*SL	0.61 + 0.025*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



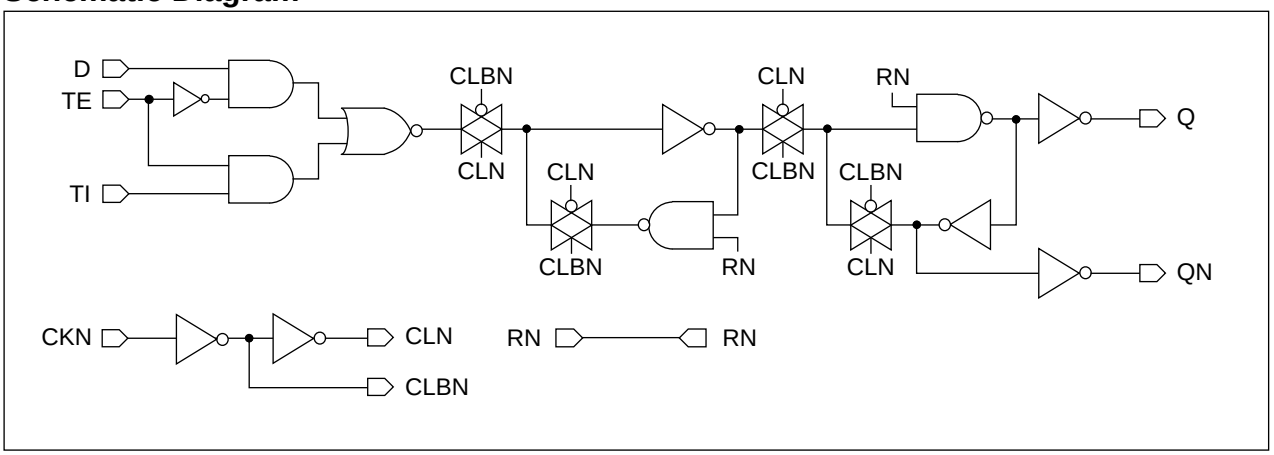
Truth Table

D	TI	TE	CKN	RN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	0	1
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
KG80											
FD6S					*FD6SD2*					*FD6S*	*FD6SD2*
D	TI	TE	CKN	RN	D	TI	TE	CKN	RN		
0.6	0.9	1.7	0.9	1.5	0.6	0.9	1.7	0.9	1.5	10.0	11.0
KGM80											
FD6S					*FD6SD2*					*FD6S*	*FD6SD2*
D	TI	TE	CKN	RN	D	TI	TE	CKN	RN		
1.1	1.0	2.1	1.0	1.9	1.1	1.0	2.1	1.0	1.9	10.0	11.0

Schematic Diagram



FD6S/FD6SD2

D Flip-Flop with Negative Edge Trigger, Reset, Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD6S	FD6SD2	FD6S	FD6SD2
Pulse Width Low (CKN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CKN)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to CKN)	t_{SU}	0.39	0.37	0.74	0.74
Input Hold Time (D to CKN)	t_{HD}	0.17	0.17	0.36	0.36
Input Setup Time (TI to CKN)	t_{SU}	0.45	0.45	0.86	0.86
Input Hold Time (TI to CKN)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CKN)	t_{SU}	0.45	0.45	0.77	0.80
Input Hold Time (TE to CKN)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.0.53	0.53	0.85	0.85

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD6S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.72	0.63 + 0.044*SL	0.64 + 0.042*SL	0.64 + 0.042*SL
	t_{PHL}	0.59	0.52 + 0.031*SL	0.54 + 0.026*SL	0.55 + 0.024*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.10 + 0.040*SL	0.08 + 0.041*SL
RN to Q	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CKN to QN	t_{PLH}	0.72	0.64 + 0.040*SL	0.64 + 0.041*SL	0.64 + 0.042*SL
	t_{PHL}	0.79	0.74 + 0.029*SL	0.75 + 0.025*SL	0.76 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
RN to QN	t_{PLH}	0.47	0.40 + 0.040*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL

KG80 FD6SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.71	0.66 + 0.025*SL	0.67 + 0.022*SL	0.67 + 0.021*SL
	t_{PHL}	0.58	0.54 + 0.021*SL	0.55 + 0.016*SL	0.57 + 0.014*SL
	t_R	0.19	0.11 + 0.043*SL	0.11 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.14	0.10 + 0.023*SL	0.10 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PHL}	0.33	0.29 + 0.022*SL	0.30 + 0.016*SL	0.32 + 0.014*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
CKN to QN	t_{PLH}	0.76	0.72 + 0.018*SL	0.72 + 0.019*SL	0.71 + 0.020*SL
	t_{PHL}	0.85	0.82 + 0.016*SL	0.83 + 0.014*SL	0.84 + 0.013*SL
	t_R	0.19	0.11 + 0.039*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.019*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
RN to QN	t_{PLH}	0.51	0.47 + 0.019*SL	0.47 + 0.019*SL	0.47 + 0.020*SL
	t_R	0.19	0.10 + 0.044*SL	0.10 + 0.043*SL	0.09 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD6S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	1.00	0.89 + 0.055*SL	0.90 + 0.051*SL	0.91 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.036*SL	0.75 + 0.027*SL	0.79 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.045*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CKN to QN	t_{PLH}	0.99	0.90 + 0.049*SL	0.89 + 0.050*SL	0.89 + 0.050*SL
	t_{PHL}	1.12	1.05 + 0.032*SL	1.07 + 0.025*SL	1.09 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.042*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
RN to QN	t_{PLH}	0.64	0.54 + 0.048*SL	0.53 + 0.050*SL	0.53 + 0.050*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL

KGM80 FD6SD2

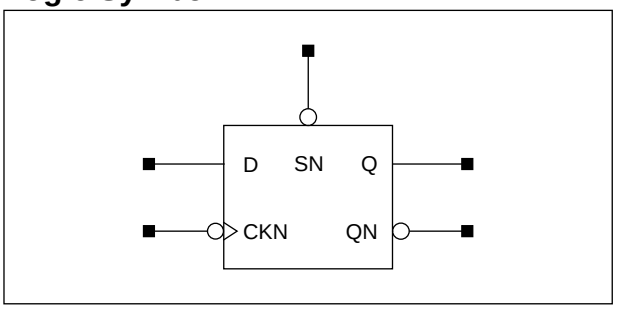
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.98	0.92 + 0.031*SL	0.93 + 0.027*SL	0.95 + 0.025*SL
	t_{PHL}	0.80	0.75 + 0.024*SL	0.77 + 0.017*SL	0.81 + 0.014*SL
	t_R	0.25	0.14 + 0.054*SL	0.14 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
RN to Q	t_{PHL}	0.44	0.39 + 0.025*SL	0.41 + 0.017*SL	0.45 + 0.014*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.16 + 0.020*SL
CKN to QN	t_{PLH}	1.05	1.01 + 0.023*SL	1.01 + 0.024*SL	1.00 + 0.025*SL
	t_{PHL}	1.21	1.17 + 0.019*SL	1.18 + 0.015*SL	1.21 + 0.013*SL
	t_R	0.25	0.14 + 0.051*SL	0.14 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
RN to QN	t_{PLH}	0.69	0.65 + 0.023*SL	0.65 + 0.024*SL	0.64 + 0.025*SL
	t_R	0.25	0.15 + 0.051*SL	0.14 + 0.053*SL	0.12 + 0.054*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FD7/FD7D2

D Flip-Flop with Negative Edge Trigger, Set, 1X/2X Drive

Logic Symbol



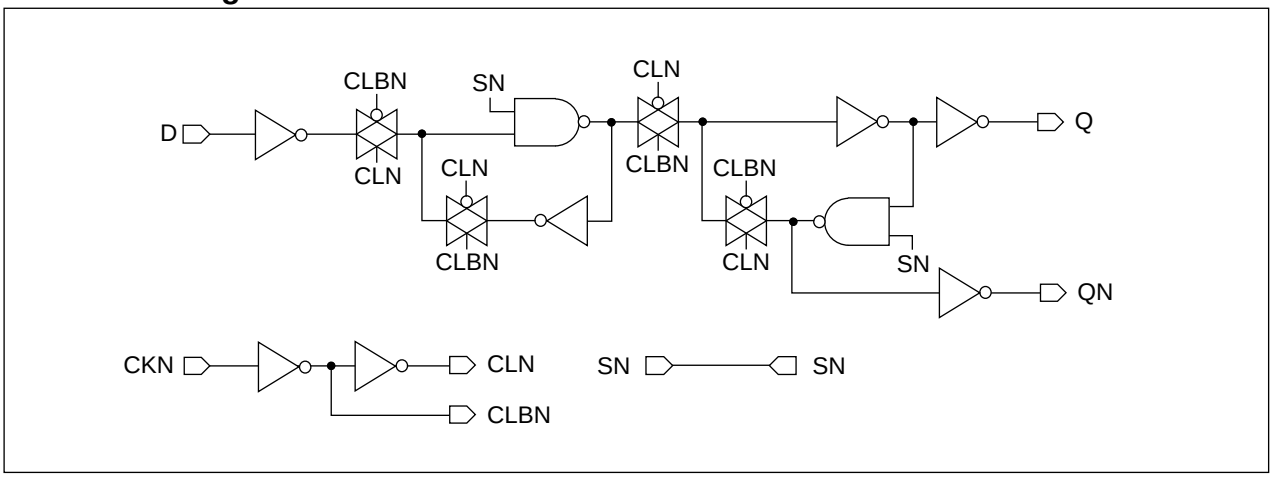
Truth Table

D	CKN	SN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	1	0
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FD7			*FD7D2*			*FD7*	*FD7D2*
D	CKN	SN	D	CKN	SN		
0.9	0.9	1.6	0.9	0.9	1.6	8.0	9.0
KGM80							
FD7			*FD7D2*			*FD7*	*FD7D2*
D	CKN	SN	D	CKN	SN		
1.0	1.0	2.0	1.0	1.0	2.0	8.0	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD7	FD7D2	FD7	FD7D2
Pulse Width Low (CKN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CKN)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	1.02
Input Setup Time (D to CKN)	t_{SU}	0.37	0.37	0.68	0.68
Input Hold Time (D to CKN)	t_{HD}	0.26	0.26	0.46	0.46
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.26	0.26	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.63	0.55 + 0.042*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.031*SL	0.54 + 0.026*SL	0.55 + 0.024*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to Q	t_{PLH}	0.59	0.50 + 0.041*SL	0.50 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
CKN to QN	t_{PLH}	0.79	0.71 + 0.042*SL	0.71 + 0.041*SL	0.71 + 0.042*SL
	t_{PHL}	0.73	0.67 + 0.030*SL	0.68 + 0.026*SL	0.69 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SN to QN	t_{PHL}	0.34	0.27 + 0.032*SL	0.29 + 0.026*SL	0.30 + 0.023*SL
	t_F	0.18	0.11 + 0.038*SL	0.11 + 0.039*SL	0.09 + 0.041*SL

KG80 FD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.62	0.57 + 0.022*SL	0.58 + 0.021*SL	0.58 + 0.021*SL
	t_{PHL}	0.59	0.55 + 0.021*SL	0.56 + 0.015*SL	0.58 + 0.013*SL
	t_R	0.17	0.09 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SN to Q	t_{PLH}	0.57	0.53 + 0.023*SL	0.53 + 0.021*SL	0.53 + 0.020*SL
	t_R	0.17	0.09 + 0.041*SL	0.09 + 0.043*SL	0.07 + 0.044*SL
CKN to QN	t_{PLH}	0.84	0.79 + 0.022*SL	0.80 + 0.020*SL	0.80 + 0.020*SL
	t_{PHL}	0.76	0.72 + 0.019*SL	0.73 + 0.015*SL	0.75 + 0.013*SL
	t_R	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.044*SL
	t_F	0.14	0.09 + 0.023*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SN to QN	t_{PHL}	0.33	0.29 + 0.022*SL	0.30 + 0.016*SL	0.32 + 0.013*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.019*SL	0.12 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FD7/FD7D2

D Flip-Flop with Negative Edge Trigger, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD7

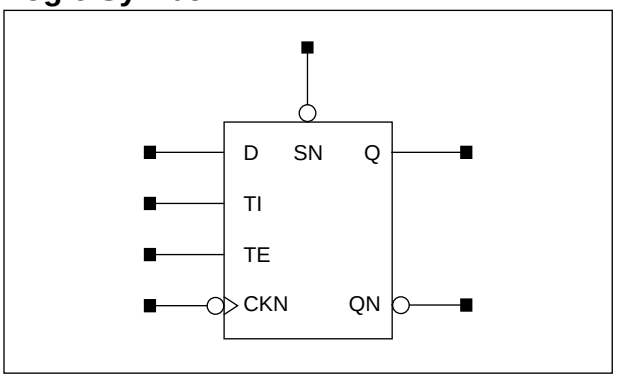
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.88	0.78 + 0.051*SL	0.78 + 0.050*SL	0.78 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.034*SL	0.75 + 0.026*SL	0.78 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SN to Q	t_{PLH}	0.82	0.71 + 0.051*SL	0.72 + 0.050*SL	0.72 + 0.050*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
CKN to QN	t_{PLH}	1.10	0.99 + 0.052*SL	1.00 + 0.050*SL	1.00 + 0.050*SL
	t_{PHL}	1.03	0.96 + 0.034*SL	0.98 + 0.026*SL	1.01 + 0.024*SL
	t_R	0.36	0.16 + 0.104*SL	0.15 + 0.106*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to QN	t_{PHL}	0.44	0.37 + 0.037*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

FDM80 FD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.86	0.80 + 0.028*SL	0.81 + 0.025*SL	0.81 + 0.025*SL
	t_{PHL}	0.81	0.76 + 0.024*SL	0.78 + 0.016*SL	0.82 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
SN to Q	t_{PLH}	0.80	0.74 + 0.029*SL	0.75 + 0.025*SL	0.75 + 0.025*SL
	t_R	0.22	0.12 + 0.051*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
CKN to QN	t_{PLH}	1.16	1.11 + 0.029*SL	1.12 + 0.025*SL	1.12 + 0.025*SL
	t_{PHL}	1.08	1.04 + 0.023*SL	1.05 + 0.016*SL	1.09 + 0.013*SL
	t_R	0.25	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
SN to QN	t_{PHL}	0.44	0.39 + 0.025*SL	0.42 + 0.017*SL	0.46 + 0.014*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.16 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



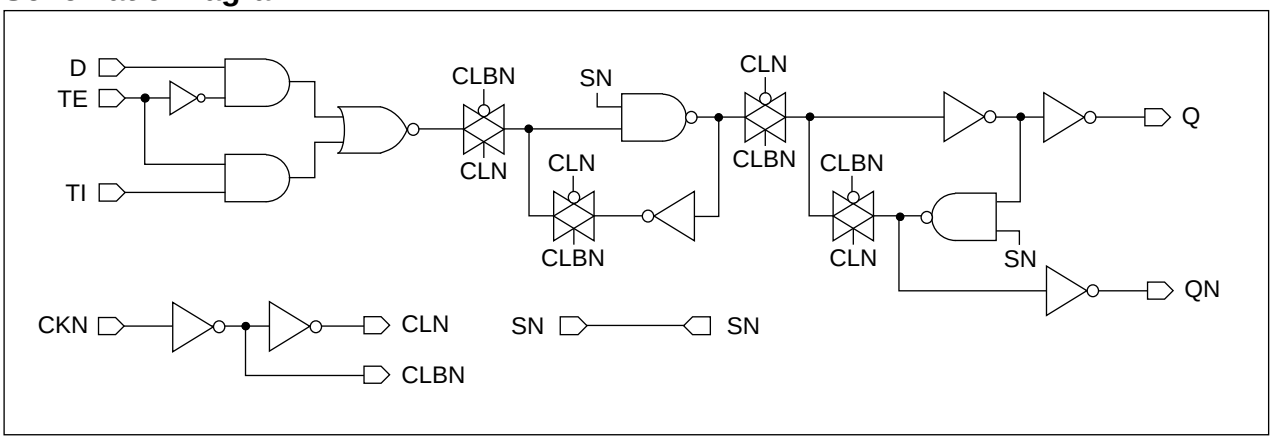
Truth Table

D	TI	TE	CKN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	1	0
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
KG80											
FD7S					*FD7SD2*					*FD7S*	*FD7SD2*
D	TI	TE	CKN	SN	D	TI	TE	CKN	SN		
0.5	0.8	1.7	0.9	1./6	0.5	0.8	1.7	0.9	1.6	10.0	11.0
KGM80											
FD7S					*FD7SD2*					*FD7S*	*FD7SD2*
D	TI	TE	CKN	SN	D	TI	TE	CKN	SN		
1.0	1.0	2.1	1.0	1.9	1.0	1.0	2.1	1.0	1.9	10.0	11.0

Schematic Diagram



FD7S/FD7SD2

D Flip-Flop with Negative Edge Trigger, Set, Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD7S	FD7SD2	FD7S	FD7SD2
Pulse Width Low (CKN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CKN)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	1.02
Input Setup Time (D to CKN)	t_{SU}	0.45	0.45	0.83	0.83
Input Hold Time (D to CKN)	t_{HD}	0.17	0.17	0.33	0.33
Input Setup Time (TI to CKN)	t_{SU}	0.50	0.50	0.93	0.93
Input Hold Time (TI to CKN)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CKN)	t_{SU}	0.45	0.45	0.83	0.83
Input Hold Time (TE to CKN)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.26	0.26	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD7S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.64	0.55 + 0.042*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.030*SL	0.54 + 0.026*SL	0.55 + 0.024*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.041*SL	0.08 + 0.041*SL
SN to Q	t_{PLH}	0.59	0.51 + 0.041*SL	0.51 + 0.041*SL	0.50 + 0.042*SL
	t_R	0.27	0.10 + 0.083*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
CKN to QN	t_{PLH}	0.79	0.71 + 0.042*SL	0.71 + 0.041*SL	0.71 + 0.042*SL
	t_{PHL}	0.73	0.67 + 0.030*SL	0.68 + 0.026*SL	0.69 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SN to QN	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_F	0.18	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.040*SL

KG80 FD7SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.62	0.57 + 0.023*SL	0.58 + 0.021*SL	0.58 + 0.021*SL
	t_{PHL}	0.59	0.55 + 0.021*SL	0.56 + 0.015*SL	0.58 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SN to Q	t_{PLH}	0.58	0.53 + 0.023*SL	0.54 + 0.021*SL	0.54 + 0.020*SL
	t_R	0.17	0.09 + 0.042*SL	0.09 + 0.042*SL	0.07 + 0.044*SL
CKN to QN	t_{PLH}	0.84	0.79 + 0.023*SL	0.80 + 0.020*SL	0.80 + 0.020*SL
	t_{PHL}	0.76	0.73 + 0.019*SL	0.73 + 0.015*SL	0.75 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SN to QN	t_{PHL}	0.33	0.29 + 0.022*SL	0.30 + 0.016*SL	0.32 + 0.013*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.019*SL	0.12 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD7S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.88	0.78 + 0.051*SL	0.78 + 0.050*SL	0.78 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.76 + 0.026*SL	0.78 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SN to Q	t_{PLH}	0.82	0.72 + 0.051*SL	0.72 + 0.050*SL	0.72 + 0.050*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
CKN to QN	t_{PLH}	1.10	0.99 + 0.053*SL	1.00 + 0.050*SL	1.00 + 0.050*SL
	t_{PHL}	1.03	0.96 + 0.034*SL	0.98 + 0.026*SL	1.01 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SN to QN	t_{PHL}	0.44	0.37 + 0.037*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

KGM80 FD7SD2

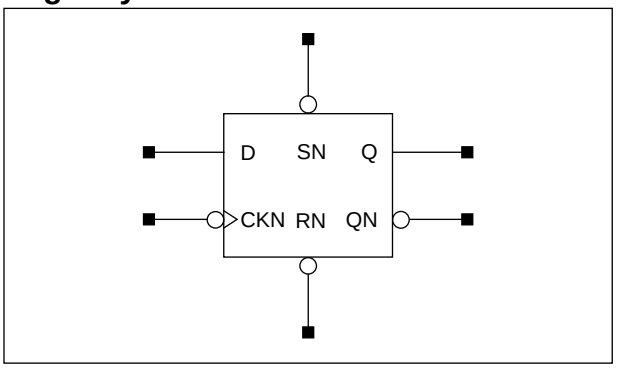
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.86	0.80 + 0.028*SL	0.81 + 0.025*SL	0.81 + 0.025*SL
	t_{PHL}	0.81	0.76 + 0.024*SL	0.78 + 0.016*SL	0.82 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
SN to Q	t_{PLH}	0.80	0.75 + 0.028*SL	0.76 + 0.025*SL	0.76 + 0.025*SL
	t_R	0.22	0.12 + 0.050*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
CKN to QN	t_{PLH}	1.16	1.11 + 0.029*SL	1.12 + 0.025*SL	1.12 + 0.025*SL
	t_{PHL}	1.08	1.04 + 0.023*SL	1.05 + 0.016*SL	1.09 + 0.013*SL
	t_R	0.25	0.14 + 0.054*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.026*SL	0.13 + 0.021*SL	0.14 + 0.021*SL
SN to QN	t_{PHL}	0.44	0.39 + 0.025*SL	0.41 + 0.017*SL	0.46 + 0.014*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.16 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FD8/FD8D2

D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X/2X Drive

Logic Symbol



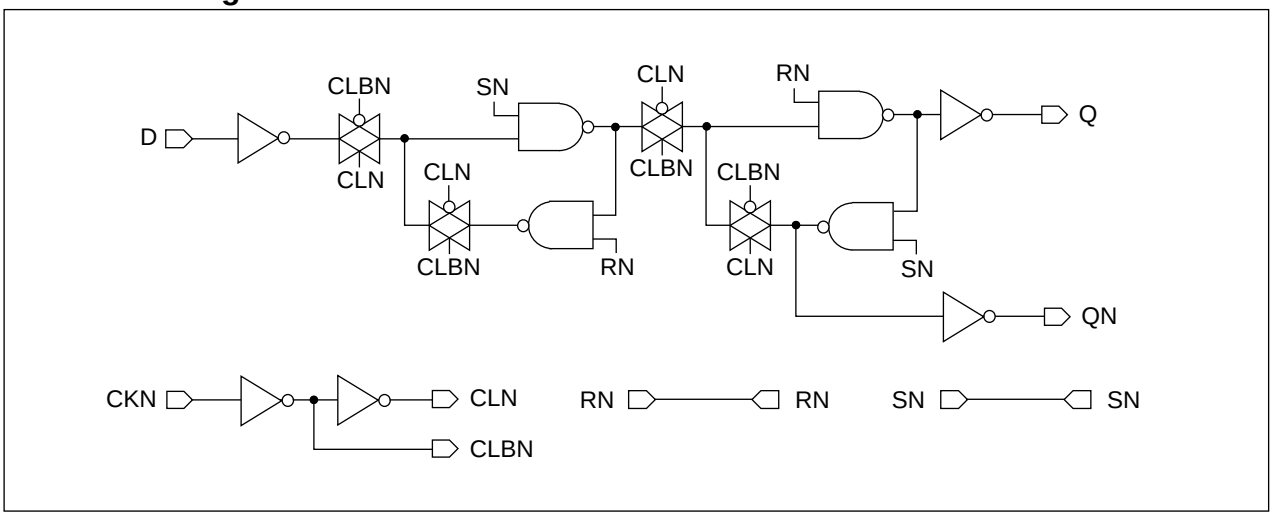
Truth Table

D	CKN	RN	SN	Q (n+1)	QN (n+1)
0	↓	1	1	0	1
1	↓	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
KG80									
FD8				*FD8D2*				*FD8*	*FD8D2*
D	CKN	RN	SN	D	CKN	RN	SN		
0.9	0.9	1.8	1.6	0.9	0.9	1.8	1.6	9.0	10.0
KGM80									
FD8				*FD8D2*				*FD8*	*FD8D2*
D	CKN	RN	SN	D	CKN	RN	SN		
1.0	1.0	2.2	2.1	1.0	1.0	2.2	2.1	9.0	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD8	FD8D2	FD8	FD8D2
Pulse Width Low (CKN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CKN)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.64	0.64	1.05	1.08
Input Setup Time (D to CKN)	t_{SU}	0.37	0.37	0.68	0.68
Input Hold Time (D to CKN)	t_{HD}	0.26	0.26	0.49	0.49
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.53	0.53	0.85	0.85
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.26	0.26	0.49	0.49

FD8/FD8D2

D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.71	0.62 + 0.045*SL	0.62 + 0.042*SL	0.63 + 0.042*SL
	t_{PHL}	0.61	0.54 + 0.031*SL	0.56 + 0.026*SL	0.57 + 0.024*SL
	t_R	0.29	0.11 + 0.086*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to Q	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q	t_{PLH}	0.66	0.57 + 0.043*SL	0.58 + 0.041*SL	0.58 + 0.041*SL
	t_R	0.28	0.11 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
CKN to QN	t_{PLH}	0.80	0.71 + 0.042*SL	0.71 + 0.041*SL	0.71 + 0.041*SL
	t_{PHL}	0.79	0.73 + 0.030*SL	0.74 + 0.025*SL	0.75 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to QN	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.041*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
SN to QN	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.33	0.26 + 0.032*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.039*SL	0.09 + 0.041*SL

KG80 FD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.70	0.65 + 0.025*SL	0.66 + 0.022*SL	0.66 + 0.021*SL
	t_{PHL}	0.61	0.56 + 0.021*SL	0.58 + 0.016*SL	0.59 + 0.013*SL
	t_R	0.19	0.11 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.14	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PLH}	0.27	0.23 + 0.023*SL	0.23 + 0.022*SL	0.24 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_R	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.043*SL
	t_F	0.15	0.11 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
SN to Q	t_{PLH}	0.66	0.61 + 0.025*SL	0.61 + 0.022*SL	0.62 + 0.021*SL
	t_R	0.19	0.11 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
CKN to QN	t_{PLH}	0.84	0.80 + 0.021*SL	0.80 + 0.020*SL	0.80 + 0.020*SL
	t_{PHL}	0.84	0.80 + 0.018*SL	0.81 + 0.015*SL	0.82 + 0.013*SL
	t_R	0.19	0.10 + 0.043*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
RN to QN	t_{PLH}	0.56	0.52 + 0.022*SL	0.52 + 0.020*SL	0.52 + 0.020*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
SN to QN	t_{PLH}	0.28	0.23 + 0.025*SL	0.24 + 0.022*SL	0.25 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.98	0.87 + 0.054*SL	0.88 + 0.051*SL	0.89 + 0.050*SL
	t_{PHL}	0.83	0.76 + 0.035*SL	0.78 + 0.027*SL	0.81 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
RN to Q	t_{PLH}	0.39	0.28 + 0.054*SL	0.29 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.036*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.36	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q	t_{PLH}	0.93	0.82 + 0.054*SL	0.83 + 0.050*SL	0.83 + 0.050*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
CKN to QN	t_{PLH}	1.11	1.00 + 0.052*SL	1.01 + 0.050*SL	1.01 + 0.050*SL
	t_{PHL}	1.11	1.05 + 0.033*SL	1.07 + 0.026*SL	1.09 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.70	0.60 + 0.052*SL	0.61 + 0.050*SL	0.61 + 0.050*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
SN to QN	t_{PLH}	0.40	0.29 + 0.054*SL	0.30 + 0.050*SL	0.31 + 0.050*SL
	t_{PHL}	0.43	0.35 + 0.036*SL	0.38 + 0.026*SL	0.41 + 0.024*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL

KGM80 FD8D2

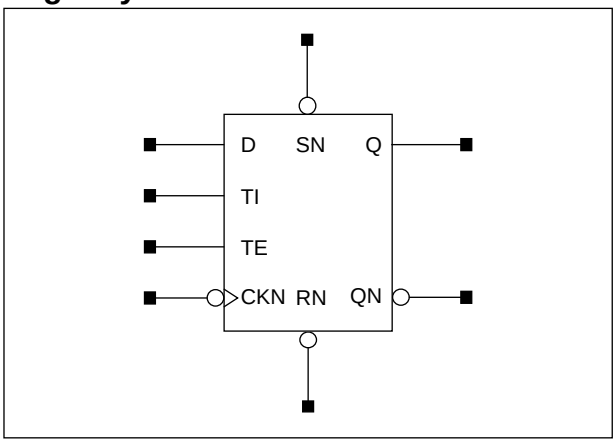
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.97	0.90 + 0.031*SL	0.92 + 0.027*SL	0.93 + 0.025*SL
	t_{PHL}	0.84	0.79 + 0.024*SL	0.81 + 0.017*SL	0.84 + 0.013*SL
	t_R	0.25	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
RN to Q	t_{PLH}	0.37	0.31 + 0.032*SL	0.32 + 0.026*SL	0.34 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.40 + 0.017*SL	0.44 + 0.014*SL
	t_R	0.24	0.14 + 0.052*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
SN to Q	t_{PLH}	0.92	0.86 + 0.031*SL	0.87 + 0.026*SL	0.89 + 0.025*SL
	t_R	0.25	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
CKN to QN	t_{PLH}	1.17	1.11 + 0.028*SL	1.12 + 0.025*SL	1.12 + 0.025*SL
	t_{PHL}	1.19	1.15 + 0.021*SL	1.16 + 0.016*SL	1.19 + 0.013*SL
	t_R	0.24	0.13 + 0.053*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
RN to QN	t_{PLH}	0.76	0.70 + 0.029*SL	0.71 + 0.025*SL	0.72 + 0.025*SL
	t_R	0.24	0.13 + 0.055*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
SN to QN	t_{PLH}	0.38	0.32 + 0.032*SL	0.33 + 0.026*SL	0.34 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.40 + 0.017*SL	0.44 + 0.013*SL
	t_R	0.24	0.13 + 0.053*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

FD8S/FD8SD2

D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

Logic Symbol



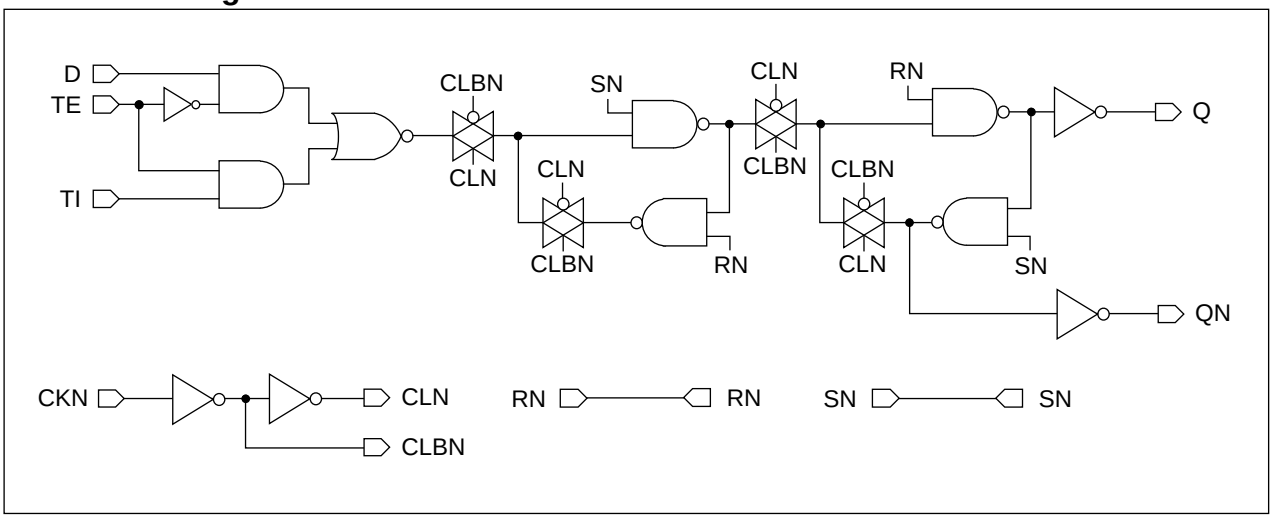
Truth Table

D	TI	TE	CKN	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	1	0	1
1	x	0	↓	1	1	1	0
x	0	1	↓	1	1	0	1
x	1	1	↓	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
KG80													
FD8S						*FD8SD2*						*FD8S*	*FD8SD2*
D	TI	TE	CKN	RN	SN	D	TI	TE	CKN	RN	SN		
0.9	0.8	1.6	0.9	1.9	1.8	0.9	0.8	1.6	0.9	1.9	1.8	11.0	12.0
KGM80													
FD8S						*FD8SD2*						*FD8S*	*FD8SD2*
D	TI	TE	CKN	RN	SN	D	TI	TE	CKN	RN	SN		
1.1	0.9	2.0	1.0	2.2	2.1	1.1	0.9	2.0	1.0	2.2	2.1	11.0	12.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FD8S	FD8SD2	FD8S	FD8SD2
Pulse Width Low (CKN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CKN)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.64	1.02	1.05
Input Setup Time (D to CKN)	t_{SU}	0.42	0.42	0.80	0.80
Input Hold Time (D to CKN)	t_{HD}	0.20	0.20	0.39	0.39
Input Setup Time (TI to CKN)	t_{SU}	0.47	0.47	0.93	0.93
Input Hold Time (TI to CKN)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CKN)	t_{SU}	0.42	0.45	0.77	0.77
Input Hold Time (TE to CKN)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.53	0.53	0.85	0.85
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.26	0.26	0.63	0.63

FD8S/FD8SD2

D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FD8S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.71	0.63 + 0.044*SL	0.63 + 0.042*SL	0.63 + 0.042*SL
	t_{PHL}	0.61	0.55 + 0.031*SL	0.56 + 0.026*SL	0.57 + 0.024*SL
	t_R	0.29	0.11 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to Q	t_{PLH}	0.29	0.20 + 0.044*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.33	0.27 + 0.032*SL	0.28 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.11 + 0.040*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q	t_{PLH}	0.65	0.56 + 0.043*SL	0.57 + 0.041*SL	0.57 + 0.041*SL
	t_R	0.28	0.11 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
CKN to QN	t_{PLH}	0.80	0.72 + 0.042*SL	0.72 + 0.041*SL	0.71 + 0.042*SL
	t_{PHL}	0.79	0.73 + 0.030*SL	0.75 + 0.025*SL	0.76 + 0.023*SL
	t_R	0.28	0.10 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.041*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
SN to QN	t_{PLH}	0.29	0.20 + 0.043*SL	0.21 + 0.041*SL	0.21 + 0.042*SL
	t_{PHL}	0.33	0.26 + 0.032*SL	0.28 + 0.025*SL	0.29 + 0.024*SL
	t_R	0.28	0.10 + 0.087*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.039*SL	0.10 + 0.039*SL	0.09 + 0.041*SL

KG80 FD8SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.70	0.65 + 0.025*SL	0.66 + 0.022*SL	0.67 + 0.021*SL
	t_{PHL}	0.61	0.57 + 0.021*SL	0.58 + 0.016*SL	0.60 + 0.013*SL
	t_R	0.19	0.11 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PLH}	0.27	0.23 + 0.023*SL	0.23 + 0.022*SL	0.24 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
SN to Q	t_{PLH}	0.64	0.59 + 0.025*SL	0.60 + 0.022*SL	0.61 + 0.021*SL
	t_R	0.19	0.11 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
CKN to QN	t_{PLH}	0.84	0.80 + 0.021*SL	0.80 + 0.020*SL	0.80 + 0.020*SL
	t_{PHL}	0.84	0.81 + 0.018*SL	0.81 + 0.015*SL	0.83 + 0.013*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
RN to QN	t_{PLH}	0.56	0.52 + 0.022*SL	0.52 + 0.020*SL	0.52 + 0.020*SL
	t_R	0.19	0.10 + 0.043*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
SN to QN	t_{PLH}	0.28	0.23 + 0.024*SL	0.24 + 0.022*SL	0.24 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_R	0.19	0.11 + 0.036*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FD8S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.99	0.88 + 0.054*SL	0.89 + 0.051*SL	0.90 + 0.050*SL
	t_{PHL}	0.84	0.76 + 0.035*SL	0.79 + 0.027*SL	0.82 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.043*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
RN to Q	t_{PLH}	0.39	0.28 + 0.054*SL	0.29 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.036*SL	0.38 + 0.027*SL	0.41 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
SN to Q	t_{PLH}	0.91	0.80 + 0.054*SL	0.81 + 0.050*SL	0.81 + 0.050*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.106*SL	0.13 + 0.108*SL
CKN to QN	t_{PLH}	1.11	1.01 + 0.052*SL	1.01 + 0.050*SL	1.01 + 0.050*SL
	t_{PHL}	1.12	1.05 + 0.034*SL	1.08 + 0.026*SL	1.10 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.70	0.60 + 0.052*SL	0.60 + 0.050*SL	0.61 + 0.050*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
SN to QN	t_{PLH}	0.40	0.29 + 0.054*SL	0.30 + 0.050*SL	0.30 + 0.050*SL
	t_{PHL}	0.42	0.35 + 0.035*SL	0.38 + 0.026*SL	0.41 + 0.024*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL

KGM80 FD8SD2

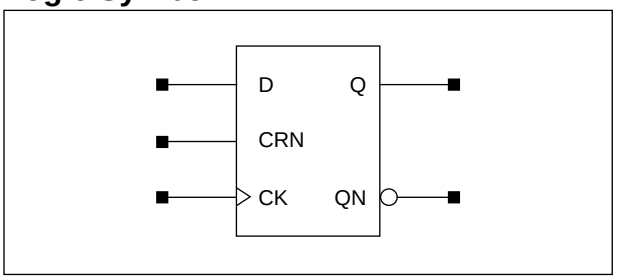
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.98	0.92 + 0.031*SL	0.93 + 0.027*SL	0.94 + 0.025*SL
	t_{PHL}	0.84	0.79 + 0.024*SL	0.81 + 0.017*SL	0.85 + 0.013*SL
	t_R	0.25	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.14 + 0.021*SL
RN to Q	t_{PLH}	0.37	0.31 + 0.031*SL	0.32 + 0.026*SL	0.34 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.40 + 0.017*SL	0.44 + 0.013*SL
	t_R	0.24	0.14 + 0.052*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
SN to Q	t_{PLH}	0.90	0.84 + 0.031*SL	0.85 + 0.026*SL	0.87 + 0.025*SL
	t_R	0.25	0.14 + 0.054*SL	0.15 + 0.052*SL	0.13 + 0.053*SL
CKN to QN	t_{PLH}	1.17	1.12 + 0.028*SL	1.12 + 0.025*SL	1.13 + 0.025*SL
	t_{PHL}	1.20	1.15 + 0.021*SL	1.17 + 0.016*SL	1.20 + 0.013*SL
	t_R	0.24	0.13 + 0.054*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
RN to QN	t_{PLH}	0.76	0.70 + 0.029*SL	0.71 + 0.025*SL	0.72 + 0.025*SL
	t_R	0.24	0.13 + 0.054*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
SN to QN	t_{PLH}	0.38	0.32 + 0.031*SL	0.33 + 0.026*SL	0.35 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.40 + 0.017*SL	0.44 + 0.013*SL
	t_R	0.24	0.13 + 0.055*SL	0.14 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FDS2/FDS2D2

D Flip-Flop with Synchronous Clear, 1X/2X Drive

Logic Symbol



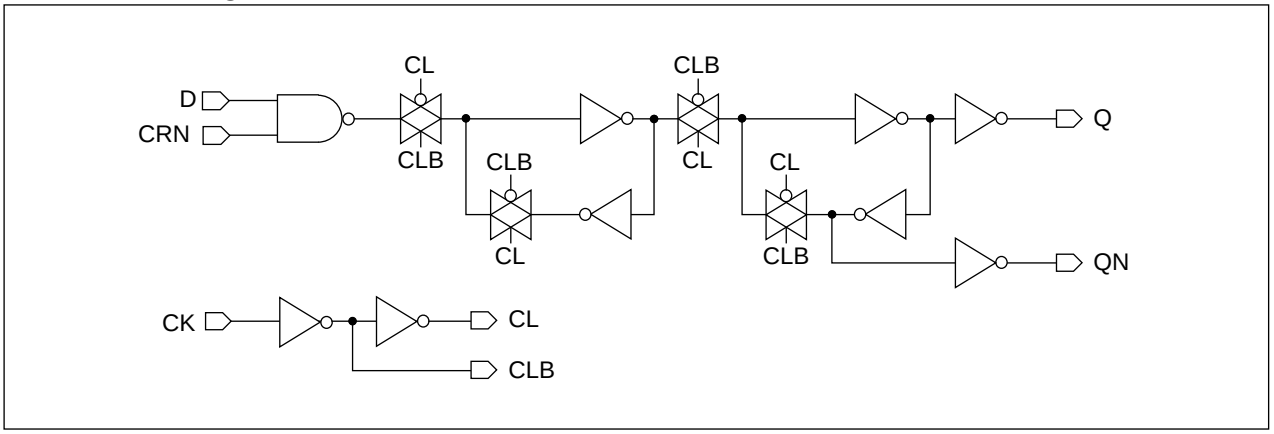
Truth Table

D	CRN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	0	1
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FDS2			*FDS2D2*			*FDS2*	*FDS2D2*
D	CRN	CK	D	CRN	CK		
0.9	0.8	0.9	0.9	0.8	0.9	7.0	8.0
KGM80							
FDS2			*FDS2D2*			*FDS2*	*FDS2D2*
D	CRN	CK	D	CRN	CK		
1.0	1.0	1.0	1.0	1.0	1.0	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FDS2	FDS2D2	FDS2	FDS2D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.42	0.42	0.77	0.80
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.42	0.42	0.77	0.80
Input Hold Time (CRN to CK)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.50	0.42 + 0.042*SL	0.42 + 0.042*SL	0.42 + 0.042*SL
	t_{PHL}	0.52	0.46 + 0.030*SL	0.48 + 0.026*SL	0.49 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CK to QN	t_{PLH}	0.66	0.58 + 0.040*SL	0.58 + 0.041*SL	0.57 + 0.042*SL
	t_{PHL}	0.58	0.52 + 0.030*SL	0.53 + 0.025*SL	0.54 + 0.023*SL
	t_R	0.26	0.09 + 0.085*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 FDS2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.48	0.44 + 0.022*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.52	0.48 + 0.021*SL	0.49 + 0.015*SL	0.51 + 0.013*SL
	t_R	0.17	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
CK to QN	t_{PLH}	0.69	0.65 + 0.019*SL	0.65 + 0.019*SL	0.65 + 0.020*SL
	t_{PHL}	0.61	0.58 + 0.018*SL	0.59 + 0.015*SL	0.60 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.09 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FDS2/FDS2D2

D Flip-Flop with Synchronous Clear, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FDS2

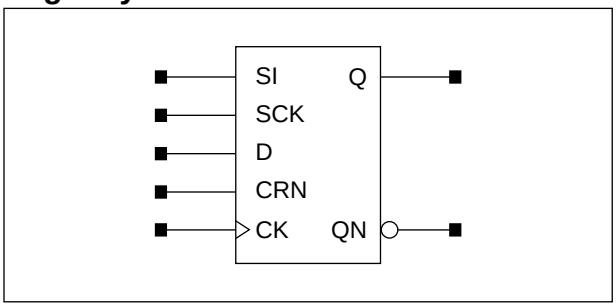
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.59 + 0.051*SL	0.59 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.74	0.67 + 0.034*SL	0.69 + 0.026*SL	0.72 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CK to QN	t_{PLH}	0.93	0.83 + 0.049*SL	0.83 + 0.050*SL	0.83 + 0.050*SL
	t_{PHL}	0.81	0.75 + 0.033*SL	0.77 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

KGM80 FDS2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.67	0.61 + 0.028*SL	0.62 + 0.025*SL	0.62 + 0.025*SL
	t_{PHL}	0.74	0.69 + 0.023*SL	0.71 + 0.016*SL	0.75 + 0.013*SL
	t_R	0.22	0.11 + 0.051*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.021*SL
CK to QN	t_{PLH}	0.98	0.93 + 0.024*SL	0.93 + 0.024*SL	0.92 + 0.025*SL
	t_{PHL}	0.87	0.83 + 0.021*SL	0.84 + 0.016*SL	0.87 + 0.013*SL
	t_R	0.22	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



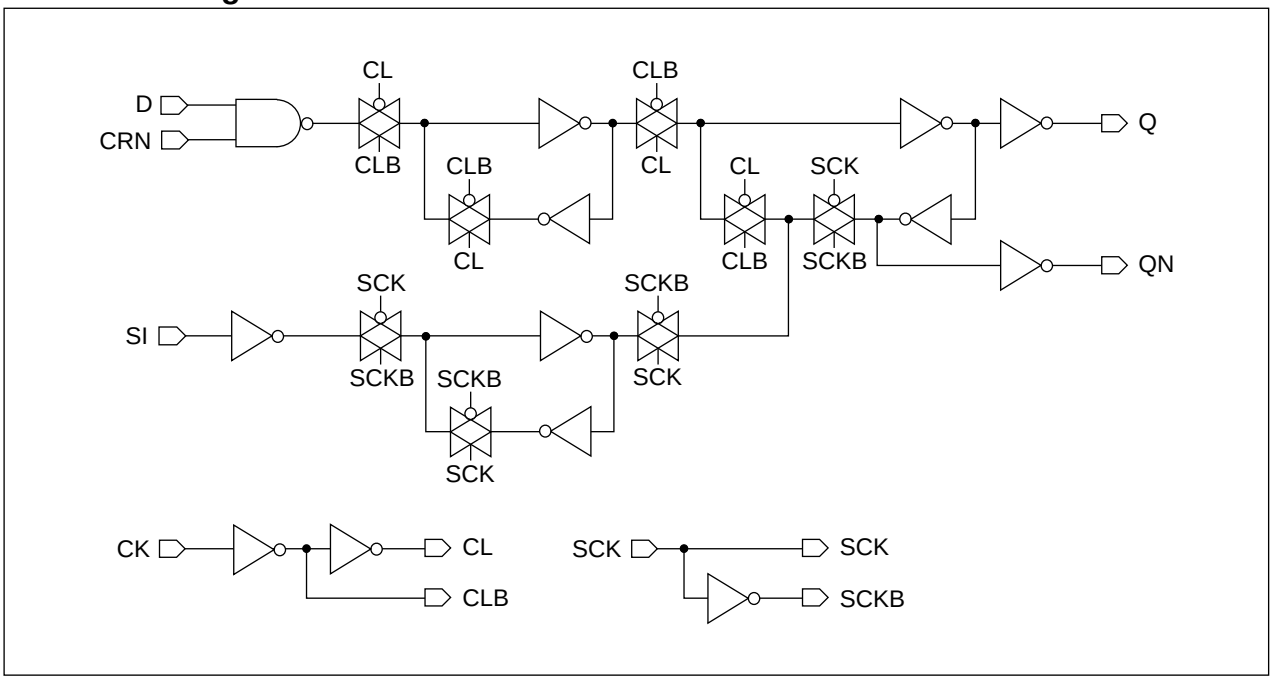
Truth Table

SI	SCK	D	CRN	CK	Q (n+1)	QN (n+1)
x	0	0	1	↑	0	1
x	0	1	1	↑	1	0
0	↑	x	1	0	0	1
1	↑	x	1	0	1	0
x	x	x	0	↑	0	1

Cell Data

Input Load (SL)										Gate Count	
KG80											
FDS2CS					*FDS2CSD2*					*FDS2CS*	*FDS2CSD2*
SI	SCK	D	CRN	CK	SI	SCK	D	CRN	CK		
0.9	2.1	0.9	0.8	0.9	0.9	2.1	0.9	0.8	0.9	11.0	12.0
KGM80											
FDS2CS					*FDS2CSD2*					*FDS2CS*	*FDS2CSD2*
SI	SCK	D	CRN	CK	SI	SCK	D	CRN	CK		
1.0	2.4	1.0	1.0	1.0	1.0	2.5	1.0	1.0	1.0	11.0	12.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FDS2CS	FDS2CSD2	FDS2CS	FDS2CSD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SCK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (SCK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.42	0.42	0.77	0.77
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.56	0.56	0.96	0.96
Input Hold Time (SI to SCK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.42	0.42	0.33	0.33
Input Hold Time (CRN to CK)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FDS2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.51	0.42 + 0.041*SL	0.42 + 0.042*SL	0.42 + 0.042*SL
	t_{PHL}	0.52	0.46 + 0.030*SL	0.48 + 0.025*SL	0.49 + 0.024*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SCK to Q	t_{PLH}	0.54	0.46 + 0.042*SL	0.46 + 0.042*SL	0.46 + 0.041*SL
	t_{PHL}	0.47	0.41 + 0.031*SL	0.42 + 0.026*SL	0.44 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
CK to QN	t_{PLH}	0.73	0.64 + 0.042*SL	0.65 + 0.041*SL	0.64 + 0.041*SL
	t_{PHL}	0.67	0.60 + 0.035*SL	0.61 + 0.028*SL	0.64 + 0.025*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.040*SL	0.13 + 0.041*SL
SCK to QN	t_{PLH}	0.61	0.53 + 0.040*SL	0.52 + 0.041*SL	0.52 + 0.042*SL
	t_{PHL}	0.62	0.56 + 0.029*SL	0.57 + 0.025*SL	0.58 + 0.023*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 FDS2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.49	0.44 + 0.022*SL	0.45 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.52	0.48 + 0.020*SL	0.49 + 0.015*SL	0.51 + 0.013*SL
	t_R	0.17	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SCK to Q	t_{PLH}	0.53	0.49 + 0.023*SL	0.49 + 0.021*SL	0.50 + 0.020*SL
	t_{PHL}	0.47	0.43 + 0.020*SL	0.44 + 0.016*SL	0.46 + 0.013*SL
	t_R	0.18	0.10 + 0.039*SL	0.10 + 0.042*SL	0.08 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
CK to QN	t_{PLH}	0.76	0.71 + 0.022*SL	0.72 + 0.020*SL	0.72 + 0.020*SL
	t_{PHL}	0.69	0.65 + 0.023*SL	0.66 + 0.017*SL	0.68 + 0.014*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.042*SL	0.10 + 0.043*SL
	t_F	0.18	0.12 + 0.026*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
SCK to QN	t_{PLH}	0.64	0.60 + 0.019*SL	0.60 + 0.019*SL	0.59 + 0.020*SL
	t_{PHL}	0.67	0.63 + 0.018*SL	0.64 + 0.014*SL	0.65 + 0.013*SL
	t_R	0.17	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.045*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.019*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FDS2CS/FDS2CSD2

D Flip-Flop with Synchronous Clear, Scan Clock, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FDS2CS

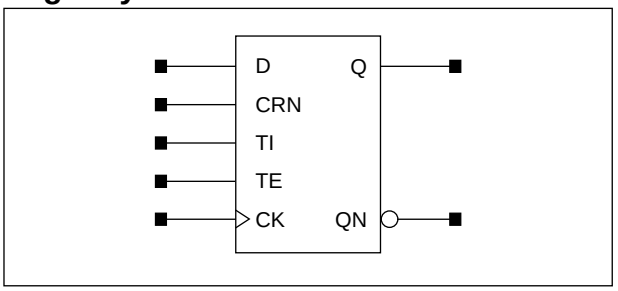
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.60 + 0.051*SL	0.60 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.74	0.67 + 0.034*SL	0.69 + 0.026*SL	0.72 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
SCK to Q	t_{PLH}	0.80	0.69 + 0.052*SL	0.70 + 0.050*SL	0.70 + 0.050*SL
	t_{PHL}	0.65	0.58 + 0.035*SL	0.61 + 0.026*SL	0.64 + 0.023*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CK to QN	t_{PLH}	1.02	0.91 + 0.053*SL	0.92 + 0.050*SL	0.92 + 0.050*SL
	t_{PHL}	0.95	0.87 + 0.040*SL	0.89 + 0.030*SL	0.94 + 0.025*SL
	t_R	0.38	0.17 + 0.102*SL	0.16 + 0.106*SL	0.13 + 0.108*SL
	t_F	0.25	0.15 + 0.048*SL	0.17 + 0.043*SL	0.18 + 0.042*SL
SCK to QN	t_{PLH}	0.85	0.75 + 0.049*SL	0.75 + 0.050*SL	0.75 + 0.050*SL
	t_{PHL}	0.92	0.85 + 0.032*SL	0.87 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.042*SL	0.11 + 0.042*SL

KGM80 FDS2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.67	0.62 + 0.028*SL	0.63 + 0.025*SL	0.63 + 0.025*SL
	t_{PHL}	0.74	0.69 + 0.023*SL	0.71 + 0.016*SL	0.75 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
SCK to Q	t_{PLH}	0.79	0.73 + 0.029*SL	0.74 + 0.025*SL	0.74 + 0.025*SL
	t_{PHL}	0.66	0.62 + 0.024*SL	0.63 + 0.017*SL	0.67 + 0.013*SL
	t_R	0.24	0.14 + 0.050*SL	0.13 + 0.052*SL	0.11 + 0.053*SL
	t_F	0.17	0.12 + 0.026*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
CK to QN	t_{PLH}	1.06	1.00 + 0.030*SL	1.01 + 0.025*SL	1.02 + 0.024*SL
	t_{PHL}	0.99	0.94 + 0.027*SL	0.96 + 0.019*SL	1.00 + 0.015*SL
	t_R	0.25	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.21	0.16 + 0.028*SL	0.17 + 0.023*SL	0.19 + 0.021*SL
SCK to QN	t_{PLH}	0.90	0.85 + 0.024*SL	0.85 + 0.024*SL	0.84 + 0.025*SL
	t_{PHL}	0.99	0.95 + 0.020*SL	0.97 + 0.016*SL	1.00 + 0.013*SL
	t_R	0.22	0.11 + 0.052*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



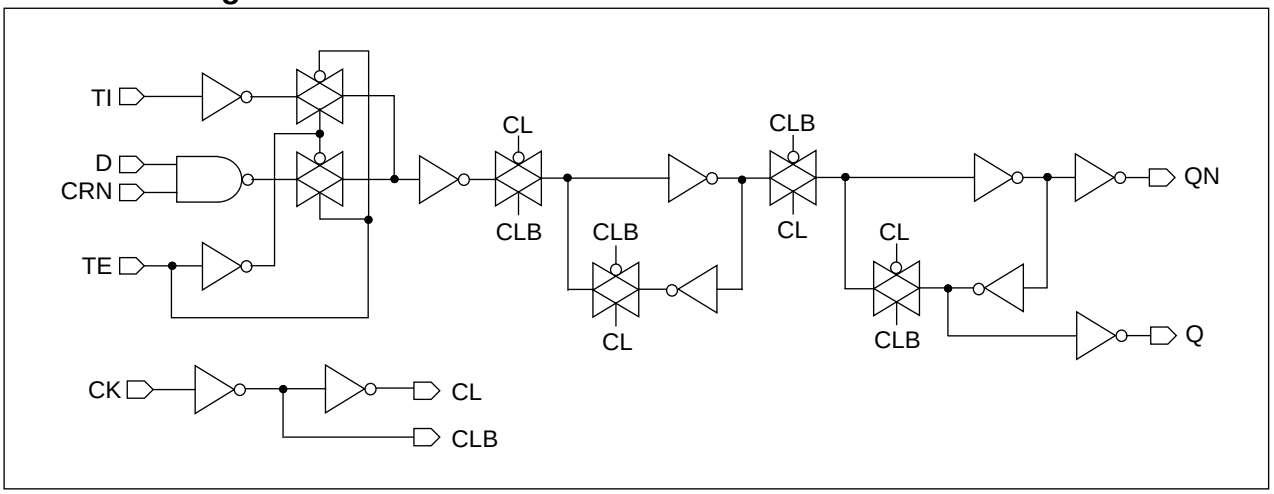
Truth Table

D	CRN	TI	TE	CK	Q (n+1)	QN (n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	0	x	0	↑	0	1
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	x	x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
KG80											
FDS2S					*FDS2SD2*					*FDS2S*	*FDS2SD2*
D	CRN	TI	TE	CK	D	CRN	TI	TE	CK		
0.9	0.8	0.9	1.7	0.9	0.9	0.8	0.9	1.7	0.9	10.0	11.0
KGM80											
FDS2S					*FDS2SD2*					*FDS2S*	*FDS2SD2*
D	CRN	TI	TE	CK	D	CRN	TI	TE	CK		
1.0	1.0	1.0	2.0	1.0	1.0	1.0	1.0	2.0	1.0	10.0	11.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FDS2S	FDS2SD2	FDS2S	FDS2SD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.58	0.58	0.99	0.99
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.58	0.58	0.99	0.99
Input Hold Time (CRN to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.56	0.56	1.02	0.99
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.47	0.47	0.83	0.83
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33

FDS2S/FDS2SD2

D Flip-Flop with Synchronous Clear, Scan, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FDS2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.66	0.58 + 0.040*SL	0.58 + 0.041*SL	0.57 + 0.042*SL
	t_{PHL}	0.58	0.52 + 0.030*SL	0.53 + 0.025*SL	0.54 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CK to QN	t_{PLH}	0.50	0.42 + 0.042*SL	0.42 + 0.042*SL	0.42 + 0.042*SL
	t_{PHL}	0.53	0.46 + 0.031*SL	0.48 + 0.026*SL	0.49 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL

KG80 FDS2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.65 + 0.019*SL	0.65 + 0.019*SL	0.64 + 0.020*SL
	t_{PHL}	0.62	0.58 + 0.018*SL	0.59 + 0.015*SL	0.60 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.10 + 0.020*SL
CK to QN	t_{PLH}	0.48	0.44 + 0.022*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.52	0.48 + 0.020*SL	0.49 + 0.015*SL	0.51 + 0.013*SL
	t_R	0.17	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FDS2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.93	0.83 + 0.049*SL	0.83 + 0.050*SL	0.83 + 0.050*SL
	t_{PHL}	0.81	0.75 + 0.033*SL	0.77 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
CK to QN	t_{PLH}	0.69	0.59 + 0.051*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.74	0.67 + 0.034*SL	0.69 + 0.026*SL	0.72 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

KGM80 FDS2SD2

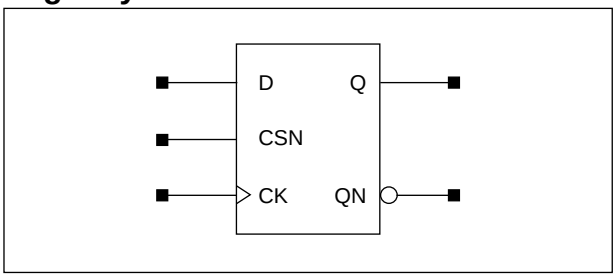
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.98	0.93 + 0.025*SL	0.93 + 0.024*SL	0.92 + 0.025*SL
	t_{PHL}	0.87	0.83 + 0.021*SL	0.84 + 0.016*SL	0.87 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.026*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
CK to QN	t_{PLH}	0.67	0.61 + 0.028*SL	0.62 + 0.025*SL	0.62 + 0.025*SL
	t_{PHL}	0.74	0.69 + 0.023*SL	0.71 + 0.016*SL	0.75 + 0.013*SL
	t_R	0.22	0.11 + 0.051*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FDS3/FDS3D2

D Flip-Flop with Synchronous Set, 1X/2X Drive

Logic Symbol



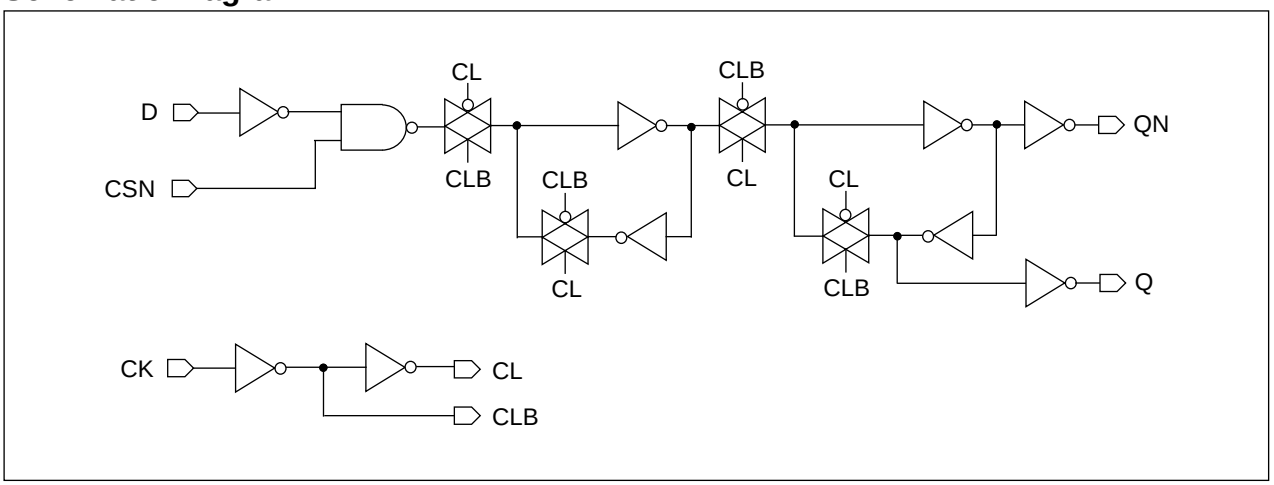
Truth Table

D	CSN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	1	0
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FDS3			*FDS3D2*			*FDS3*	*FDS3D2*
D	CSN	CK	D	CSN	CK		
0.8	0.8	0.8	0.8	0.8	0.8	8.0	9.0
KGM80							
FDS3			*FDS3D2*			*FDS3*	*FDS3D2*
D	CSN	CK	D	CSN	CK		
0.9	0.9	0.9	0.9	0.9	0.9	8.0	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FDS2	FDS2D2	FDS2	FDS2D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to CK)	t_{SU}	0.15	0.15	0.33	0.33
Input Hold Time (D to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (CSN to CK)	t_{SU}	0.45	0.45	0.77	0.77
Input Hold Time (CSN to CK)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FDS3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.62	0.54 + 0.040*SL	0.54 + 0.041*SL	0.54 + 0.042*SL
	t_{PHL}	0.56	0.50 + 0.028*SL	0.51 + 0.025*SL	0.52 + 0.023*SL
	t_R	0.26	0.08 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.15	0.07 + 0.040*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
CK to QN	t_{PLH}	0.49	0.41 + 0.042*SL	0.41 + 0.042*SL	0.41 + 0.042*SL
	t_{PHL}	0.50	0.44 + 0.030*SL	0.45 + 0.025*SL	0.46 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 FDS3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.65	0.61 + 0.019*SL	0.61 + 0.020*SL	0.60 + 0.021*SL
	t_{PHL}	0.59	0.55 + 0.017*SL	0.56 + 0.014*SL	0.57 + 0.012*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.020*SL
CK to QN	t_{PLH}	0.48	0.44 + 0.021*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.50	0.46 + 0.018*SL	0.47 + 0.015*SL	0.48 + 0.013*SL
	t_R	0.18	0.10 + 0.044*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FDS3/FDS3D2

D Flip-Flop with Synchronous Clear, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FDS3

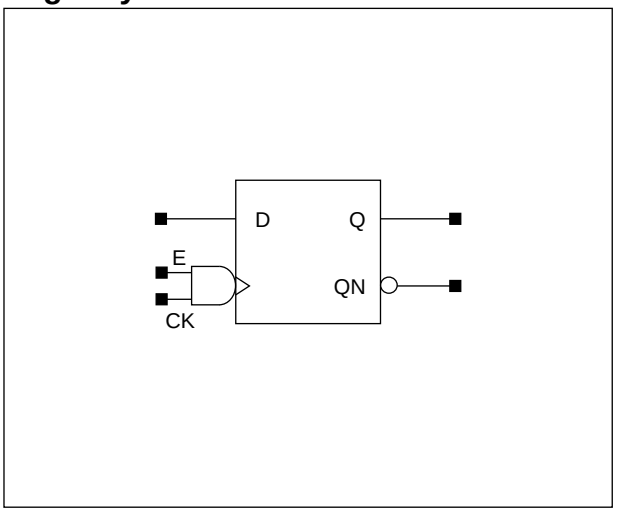
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.88	0.78 + 0.049*SL	0.78 + 0.050*SL	0.78 + 0.050*SL
	t_{PHL}	0.80	0.74 + 0.031*SL	0.76 + 0.025*SL	0.78 + 0.023*SL
	t_R	0.33	0.12 + 0.105*SL	0.11 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.18	0.10 + 0.043*SL	0.10 + 0.042*SL	0.09 + 0.043*SL
CK to QN	t_{PLH}	0.70	0.60 + 0.051*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.70	0.63 + 0.034*SL	0.65 + 0.026*SL	0.68 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.044*SL	0.11 + 0.041*SL	0.10 + 0.042*SL

KGM80 FDS3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.92	0.87 + 0.023*SL	0.87 + 0.024*SL	0.86 + 0.025*SL
	t_{PHL}	0.86	0.82 + 0.019*SL	0.83 + 0.015*SL	0.85 + 0.012*SL
	t_R	0.23	0.13 + 0.051*SL	0.13 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.021*SL	0.12 + 0.020*SL
CK to QN	t_{PLH}	0.69	0.63 + 0.027*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.71	0.67 + 0.021*SL	0.68 + 0.015*SL	0.71 + 0.013*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.021*SL	0.13 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



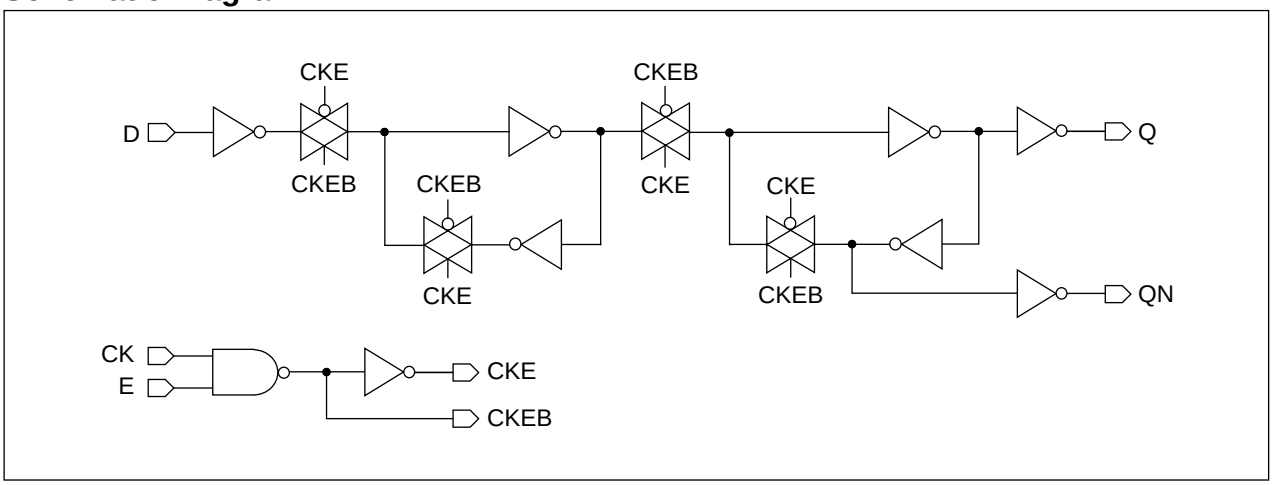
Truth Table

D	E	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	x	Q (n)	QN (n)
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)			Gate Count
KG80			
D	E	CK	
1.0	0.9	0.9	7.0
KGM80			
D	E	CK	
1.0	1.0	1.0	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.61	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Pulse Width Low (E)	t_{PWL}	0.61	0.99
Pulse Width High (E)	t_{PWH}	0.61	0.99
Input Setup Time (D to CK)	t_{SU}	0.31	0.58
Input Hold Time (D to CK)	t_{HD}	0.15	0.33
Input Setup Time (D to E)	t_{SU}	0.31	0.58
Input Hold Time (D to E)	t_{HD}	0.15	0.33

FG1

D Flip-Flop with CK Enable

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FG1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.49 + 0.042*SL	0.49 + 0.042*SL	0.50 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.026*SL	0.56 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
E to Q	t_{PLH}	0.56	0.48 + 0.042*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.58	0.52 + 0.031*SL	0.53 + 0.026*SL	0.55 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CK to QN	t_{PLH}	0.73	0.65 + 0.040*SL	0.65 + 0.041*SL	0.65 + 0.042*SL
	t_{PHL}	0.65	0.60 + 0.029*SL	0.61 + 0.025*SL	0.62 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to QN	t_{PLH}	0.72	0.64 + 0.040*SL	0.63 + 0.041*SL	0.63 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.030*SL	0.59 + 0.025*SL	0.60 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

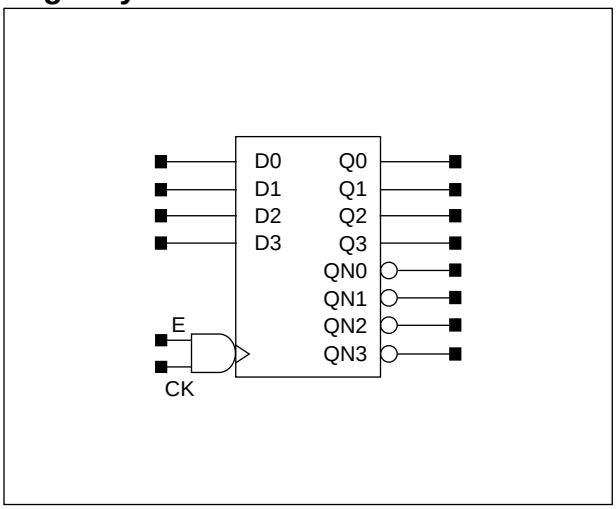
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FG1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.80	0.70 + 0.051*SL	0.70 + 0.050*SL	0.70 + 0.050*SL
	t_{PHL}	0.83	0.77 + 0.033*SL	0.79 + 0.026*SL	0.82 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
E to Q	t_{PLH}	0.79	0.69 + 0.051*SL	0.69 + 0.050*SL	0.69 + 0.050*SL
	t_{PHL}	0.82	0.76 + 0.034*SL	0.78 + 0.026*SL	0.81 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
CK to QN	t_{PLH}	1.03	0.93 + 0.048*SL	0.93 + 0.050*SL	0.93 + 0.050*SL
	t_{PHL}	0.92	0.85 + 0.033*SL	0.87 + 0.026*SL	0.90 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
E to QN	t_{PLH}	1.02	0.92 + 0.049*SL	0.92 + 0.050*SL	0.92 + 0.050*SL
	t_{PHL}	0.91	0.84 + 0.033*SL	0.86 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

Dn	E	CK	Qn (n+1)	QNn (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	x	Qn (n)	QNn (n)
x	x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
KG80			
Dn	E	CK	
0.9	0.8	0.6	25.0
KGM80			
Dn	E	CK	
1.0	0.9	0.7	25.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.78	1.24
Pulse Width High (CK)	t_{PWH}	0.69	1.11
Pulse Width Low (E)	t_{PWL}	0.80	1.30
Pulse Width High (E)	t_{PWH}	0.67	1.08
Input Setup Time (D0 to CK)	t_{SU}	0.15	0.33
Input Hold Time (D0 to CK)	t_{HD}	0.37	0.58
Input Setup Time (D0 to E)	t_{SU}	0.15	0.33
Input Hold Time (D0 to E)	t_{HD}	0.34	0.58
Input Setup Time (D1 to CK)	t_{SU}	0.15	0.33
Input Hold Time (D1 to CK)	t_{HD}	0.37	0.58
Input Setup Time (D1 to E)	t_{SU}	0.15	0.33
Input Hold Time (D1 to E)	t_{HD}	0.34	0.55
Input Setup Time (D2 to CK)	t_{SU}	0.15	0.33
Input Hold Time (D2 to CK)	t_{HD}	0.37	0.58
Input Setup Time (D2 to E)	t_{SU}	0.15	0.33
Input Hold Time (D2 to E)	t_{HD}	0.34	0.55
Input Setup Time (D3 to CK)	t_{SU}	0.15	0.33
Input Hold Time (D3 to CK)	t_{HD}	0.37	0.58
Input Setup Time (D3 to E)	t_{SU}	0.15	0.33
Input Hold Time (D3 to E)	t_{HD}	0.34	0.55

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FG1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.80	0.71 + 0.042*SL	0.71 + 0.042*SL	0.71 + 0.042*SL
	t_{PHL}	0.97	0.90 + 0.030*SL	0.92 + 0.026*SL	0.93 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
E to Q0	t_{PLH}	0.78	0.70 + 0.042*SL	0.70 + 0.042*SL	0.70 + 0.042*SL
	t_{PHL}	0.95	0.89 + 0.031*SL	0.90 + 0.026*SL	0.91 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CK to Q1	t_{PLH}	0.80	0.72 + 0.042*SL	0.72 + 0.041*SL	0.72 + 0.042*SL
	t_{PHL}	0.97	0.91 + 0.030*SL	0.92 + 0.026*SL	0.94 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.18	0.09 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
E to Q1	t_{PLH}	0.79	0.70 + 0.042*SL	0.70 + 0.042*SL	0.70 + 0.042*SL
	t_{PHL}	0.95	0.89 + 0.031*SL	0.90 + 0.026*SL	0.92 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
CK to Q2	t_{PLH}	0.80	0.72 + 0.042*SL	0.72 + 0.041*SL	0.72 + 0.042*SL
	t_{PHL}	0.97	0.91 + 0.030*SL	0.92 + 0.026*SL	0.94 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.18	0.09 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
E to Q2	t_{PLH}	0.79	0.70 + 0.042*SL	0.70 + 0.042*SL	0.70 + 0.042*SL
	t_{PHL}	0.95	0.89 + 0.031*SL	0.90 + 0.026*SL	0.92 + 0.024*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
CK to Q3	t_{PLH}	0.80	0.71 + 0.042*SL	0.71 + 0.042*SL	0.71 + 0.042*SL
	t_{PHL}	0.97	0.90 + 0.030*SL	0.92 + 0.026*SL	0.93 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
E to Q3	t_{PLH}	0.78	0.70 + 0.042*SL	0.70 + 0.042*SL	0.70 + 0.042*SL
	t_{PHL}	0.95	0.89 + 0.031*SL	0.90 + 0.026*SL	0.91 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CK to QN0	t_{PLH}	1.10	1.02 + 0.040*SL	1.01 + 0.041*SL	1.01 + 0.042*SL
	t_{PHL}	0.87	0.81 + 0.030*SL	0.82 + 0.025*SL	0.83 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to QN0	t_{PLH}	1.08	1.00 + 0.041*SL	1.00 + 0.041*SL	1.00 + 0.041*SL
	t_{PHL}	0.85	0.79 + 0.030*SL	0.80 + 0.025*SL	0.82 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FG1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN1	t_{PLH}	1.10	1.02 + 0.040*SL	1.02 + 0.041*SL	1.02 + 0.042*SL
	t_{PHL}	0.88	0.82 + 0.029*SL	0.83 + 0.025*SL	0.84 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to QN1	t_{PLH}	1.09	1.01 + 0.040*SL	1.00 + 0.041*SL	1.00 + 0.042*SL
	t_{PHL}	0.86	0.80 + 0.030*SL	0.81 + 0.025*SL	0.82 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CK to QN2	t_{PLH}	1.10	1.02 + 0.040*SL	1.02 + 0.041*SL	1.02 + 0.042*SL
	t_{PHL}	0.88	0.82 + 0.029*SL	0.83 + 0.025*SL	0.84 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to QN2	t_{PLH}	1.09	1.01 + 0.040*SL	1.00 + 0.041*SL	1.00 + 0.042*SL
	t_{PHL}	0.86	0.80 + 0.030*SL	0.81 + 0.025*SL	0.82 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CK to QN3	t_{PLH}	1.10	1.02 + 0.040*SL	1.01 + 0.041*SL	1.01 + 0.042*SL
	t_{PHL}	0.87	0.81 + 0.030*SL	0.82 + 0.025*SL	0.83 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to QN3	t_{PLH}	1.08	1.00 + 0.041*SL	1.00 + 0.041*SL	1.00 + 0.041*SL
	t_{PHL}	0.85	0.79 + 0.030*SL	0.80 + 0.025*SL	0.82 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FG1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.08	0.97 + 0.051*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	1.36	1.29 + 0.034*SL	1.31 + 0.026*SL	1.34 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
E to Q0	t_{PLH}	1.07	0.96 + 0.051*SL	0.97 + 0.050*SL	0.97 + 0.050*SL
	t_{PHL}	1.35	1.28 + 0.034*SL	1.30 + 0.026*SL	1.33 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.11 + 0.042*SL
CK to Q1	t_{PLH}	1.09	0.98 + 0.051*SL	0.99 + 0.050*SL	0.99 + 0.050*SL
	t_{PHL}	1.36	1.30 + 0.034*SL	1.32 + 0.026*SL	1.35 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
E to Q1	t_{PLH}	1.08	0.97 + 0.051*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	1.36	1.29 + 0.034*SL	1.31 + 0.026*SL	1.34 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CK to Q2	t_{PLH}	1.09	0.98 + 0.051*SL	0.99 + 0.050*SL	0.99 + 0.050*SL
	t_{PHL}	1.36	1.30 + 0.034*SL	1.32 + 0.026*SL	1.35 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
E to Q2	t_{PLH}	1.08	0.97 + 0.051*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	1.36	1.29 + 0.034*SL	1.31 + 0.026*SL	1.34 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CK to Q3	t_{PLH}	1.08	0.97 + 0.051*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	1.36	1.29 + 0.034*SL	1.31 + 0.026*SL	1.34 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
E to Q3	t_{PLH}	1.07	0.96 + 0.051*SL	0.97 + 0.050*SL	0.97 + 0.050*SL
	t_{PHL}	1.35	1.28 + 0.034*SL	1.30 + 0.026*SL	1.33 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.11 + 0.042*SL
CK to QN0	t_{PLH}	1.55	1.45 + 0.049*SL	1.45 + 0.050*SL	1.45 + 0.050*SL
	t_{PHL}	1.20	1.13 + 0.033*SL	1.15 + 0.026*SL	1.17 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
E to QN0	t_{PLH}	1.54	1.44 + 0.049*SL	1.44 + 0.050*SL	1.44 + 0.050*SL
	t_{PHL}	1.19	1.12 + 0.033*SL	1.14 + 0.026*SL	1.16 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 KG1X4

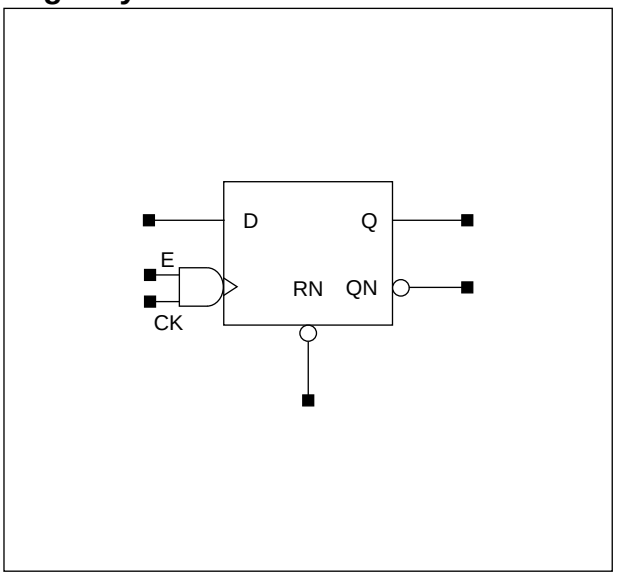
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN1	t_{PLH}	1.56	1.46 + 0.049*SL	1.46 + 0.050*SL	1.46 + 0.050*SL
	t_{PHL}	1.21	1.14 + 0.033*SL	1.16 + 0.026*SL	1.19 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
E to QN1	t_{PLH}	1.55	1.45 + 0.049*SL	1.45 + 0.050*SL	1.45 + 0.050*SL
	t_{PHL}	1.20	1.13 + 0.032*SL	1.15 + 0.026*SL	1.18 + 0.023*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
CK to QN2	t_{PLH}	1.56	1.46 + 0.049*SL	1.46 + 0.050*SL	1.46 + 0.050*SL
	t_{PHL}	1.21	1.14 + 0.033*SL	1.16 + 0.026*SL	1.19 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
E to QN2	t_{PLH}	1.55	1.45 + 0.049*SL	1.45 + 0.050*SL	1.45 + 0.050*SL
	t_{PHL}	1.20	1.13 + 0.033*SL	1.15 + 0.026*SL	1.18 + 0.023*SL
	t_R	0.34	0.14 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
CK to QN3	t_{PLH}	1.55	1.45 + 0.049*SL	1.45 + 0.050*SL	1.45 + 0.050*SL
	t_{PHL}	1.20	1.13 + 0.033*SL	1.15 + 0.026*SL	1.17 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
E to QN3	t_{PLH}	1.54	1.44 + 0.049*SL	1.44 + 0.050*SL	1.44 + 0.050*SL
	t_{PHL}	1.19	1.12 + 0.033*SL	1.14 + 0.026*SL	1.16 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

FG2

D Flip-Flop with CK Enable, Reset

Logic Symbol



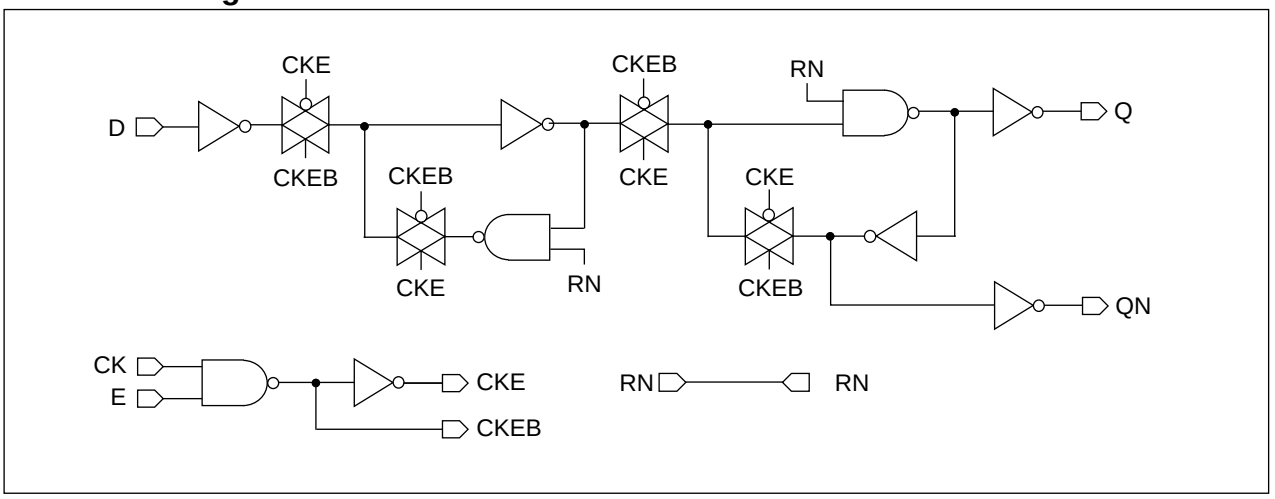
Truth Table

D	E	CK	RN	Q (n+1)	QN (n+1)
0	1	↑	1	0	1
1	1	↑	1	1	0
x	0	x	1	Q (n)	QN (n)
x	x	x	0	0	1
x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count
KG80				
D	E	CK	RN	
1.0	0.9	0.9	1.5	8.0
KGM80				
D	E	CK	RN	
1.0	1.0	1.1	1.9	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.61	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.99
Pulse Width Low (E)	t_{PWL}	0.61	0.99
Pulse Width High (E)	t_{PWH}	0.61	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.99
Input Setup Time (D to CK)	t_{SU}	0.31	0.58
Input Hold Time (D to CK)	t_{HD}	0.15	0.33
Input Setup Time (D to E)	t_{SU}	0.31	0.58
Input Hold Time (D to E)	t_{HD}	0.15	0.33
Recovery Time (RN to CK)	t_{RC}	0.15	0.33
Input Hold Time (RN to CK)	t_{HD}	0.48	0.85
Recovery Time (RN to E)	t_{RC}	0.15	0.33
Input Hold Time (RN to E)	t_{HD}	0.48	0.85

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FG2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.55 + 0.044*SL	0.56 + 0.042*SL	0.57 + 0.041*SL
	t_{PHL}	0.62	0.55 + 0.031*SL	0.57 + 0.026*SL	0.58 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
E to Q	t_{PLH}	0.63	0.54 + 0.045*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.031*SL	0.55 + 0.026*SL	0.57 + 0.024*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to Q	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.041*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CK to QN	t_{PLH}	0.75	0.67 + 0.040*SL	0.67 + 0.041*SL	0.67 + 0.042*SL
	t_{PHL}	0.72	0.66 + 0.030*SL	0.67 + 0.025*SL	0.68 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.16	0.09 + 0.039*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to QN	t_{PLH}	0.74	0.66 + 0.040*SL	0.65 + 0.041*SL	0.65 + 0.042*SL
	t_{PHL}	0.71	0.65 + 0.030*SL	0.66 + 0.025*SL	0.67 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.16	0.09 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
RN to QN	t_{PLH}	0.48	0.40 + 0.040*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FG2

D Flip-Flop with CK Enable, Reset

Switching Characteristics

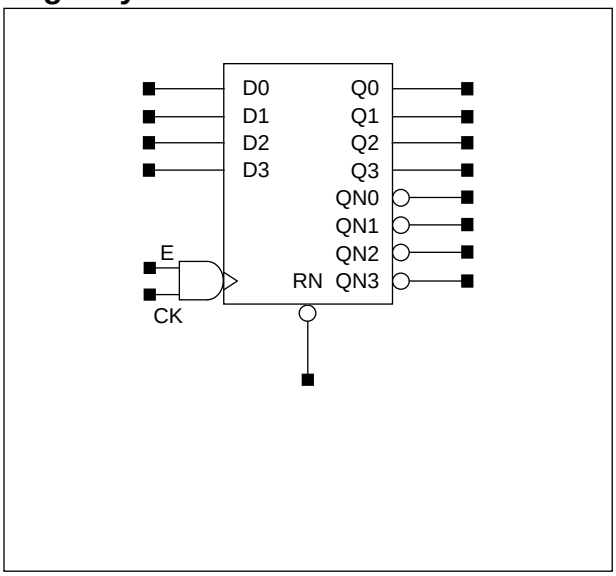
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FG2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.89	0.78 + 0.055*SL	0.80 + 0.051*SL	0.81 + 0.050*SL
	t_{PHL}	0.86	0.79 + 0.036*SL	0.82 + 0.027*SL	0.85 + 0.023*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
E to Q	t_{PLH}	0.88	0.77 + 0.055*SL	0.79 + 0.051*SL	0.80 + 0.050*SL
	t_{PHL}	0.86	0.78 + 0.036*SL	0.81 + 0.027*SL	0.84 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to QN	t_{PLH}	1.06	0.96 + 0.049*SL	0.96 + 0.050*SL	0.96 + 0.050*SL
	t_{PHL}	1.02	0.95 + 0.033*SL	0.97 + 0.026*SL	0.99 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
E to QN	t_{PLH}	1.05	0.95 + 0.049*SL	0.95 + 0.050*SL	0.95 + 0.050*SL
	t_{PHL}	1.01	0.94 + 0.033*SL	0.96 + 0.025*SL	0.98 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.042*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
RN to QN	t_{PLH}	0.64	0.54 + 0.049*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

Dn	E	CK	RN	Qn (n+1)	QNn (n+1)
0	1	↑	1	0	1
1	1	↑	1	1	0
x	0	x	1	Qn (n)	QNn (n)
x	x	x	0	0	1
x	x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
KG80				
Dn	E	CK	RN	
0.9	0.8	0.6	7.0	29.0
KGM80				
Dn	E	CK	RN	
1.0	0.9	0.7	8.3	29.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (CK)	t_{PWL}	0.78	1.27
Pulse Width High (CK)	t_{PWH}	0.72	1.14
Pulse Width Low (E)	t_{PWL}	0.83	1.30
Pulse Width High (E)	t_{PWH}	0.69	1.11
Pulse Width Low (RN)	t_{PWL}	0.61	0.99
Input Setup Time (D0 to CK)	t_{SU}	0.15	0.33
Input Hold Time (D0 to CK)	t_{HD}	0.37	0.58
Input Setup Time (D0 to E)	t_{SU}	0.15	0.36
Input Hold Time (D0 to E)	t_{HD}	0.37	0.58
Input Setup Time (D1 to CK)	t_{SU}	0.15	0.33
Input Hold Time (D1 to CK)	t_{HD}	0.39	0.61
Input Setup Time (D1 to E)	t_{SU}	0.15	0.36
Input Hold Time (D1 to E)	t_{HD}	0.37	0.58
Input Setup Time (D2 to CK)	t_{SU}	0.15	0.33
Input Hold Time (D2 to CK)	t_{HD}	0.39	0.61
Input Setup Time (D2 to E)	t_{SU}	0.15	0.36
Input Hold Time (D2 to E)	t_{HD}	0.37	0.58
Input Setup Time (D3 to CK)	t_{SU}	0.15	0.33
Input Hold Time (D3 to CK)	t_{HD}	0.37	0.58
Input Setup Time (D3 to E)	t_{SU}	0.15	0.36
Input Hold Time (D3 to E)	t_{HD}	0.37	0.58
Recovery Time (RN to CK)	t_{RC}	0.15	0.33
Input Hold Time (RN to CK)	t_{HD}	0.75	1.07
Recovery Time (RN to E)	t_{RC}	0.15	0.33
Input Hold Time (RN to E)	t_{HD}	0.69	1.07

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FG2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.87	0.78 + 0.045*SL	0.79 + 0.042*SL	0.80 + 0.041*SL
	t_{PHL}	0.99	0.93 + 0.031*SL	0.94 + 0.026*SL	0.96 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
E to Q0	t_{PLH}	0.86	0.77 + 0.045*SL	0.77 + 0.042*SL	0.78 + 0.042*SL
	t_{PHL}	0.98	0.91 + 0.032*SL	0.93 + 0.026*SL	0.94 + 0.024*SL
	t_R	0.28	0.11 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
RN to Q0	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CK to Q1	t_{PLH}	0.88	0.79 + 0.044*SL	0.79 + 0.042*SL	0.80 + 0.042*SL
	t_{PHL}	1.00	0.93 + 0.031*SL	0.95 + 0.026*SL	0.96 + 0.024*SL
	t_R	0.29	0.12 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
E to Q1	t_{PLH}	0.86	0.77 + 0.044*SL	0.78 + 0.042*SL	0.78 + 0.042*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.93 + 0.026*SL	0.95 + 0.024*SL
	t_R	0.29	0.12 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q1	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CK to Q2	t_{PLH}	0.88	0.79 + 0.044*SL	0.79 + 0.042*SL	0.80 + 0.042*SL
	t_{PHL}	1.00	0.93 + 0.031*SL	0.95 + 0.026*SL	0.96 + 0.024*SL
	t_R	0.29	0.11 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
E to Q2	t_{PLH}	0.86	0.77 + 0.044*SL	0.78 + 0.042*SL	0.78 + 0.042*SL
	t_{PHL}	0.98	0.92 + 0.031*SL	0.93 + 0.026*SL	0.95 + 0.024*SL
	t_R	0.29	0.12 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
RN to Q2	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.040*SL
CK to Q3	t_{PLH}	0.87	0.78 + 0.045*SL	0.79 + 0.042*SL	0.80 + 0.041*SL
	t_{PHL}	0.99	0.93 + 0.031*SL	0.94 + 0.026*SL	0.96 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
E to Q3	t_{PLH}	0.86	0.77 + 0.045*SL	0.77 + 0.042*SL	0.78 + 0.042*SL
	t_{PHL}	0.98	0.91 + 0.032*SL	0.93 + 0.026*SL	0.94 + 0.024*SL
	t_R	0.28	0.11 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
RN to Q3	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FG2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.13	1.05 + 0.040*SL	1.05 + 0.041*SL	1.04 + 0.042*SL
	t_{PHL}	0.95	0.89 + 0.030*SL	0.90 + 0.025*SL	0.91 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.09 + 0.039*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to QN0	t_{PLH}	1.11	1.03 + 0.040*SL	1.03 + 0.041*SL	1.02 + 0.042*SL
	t_{PHL}	0.93	0.87 + 0.029*SL	0.88 + 0.025*SL	0.89 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.16	0.09 + 0.039*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
RN to QN0	t_{PLH}	0.47	0.40 + 0.040*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
CK to QN1	t_{PLH}	1.13	1.05 + 0.040*SL	1.05 + 0.041*SL	1.05 + 0.042*SL
	t_{PHL}	0.95	0.90 + 0.029*SL	0.91 + 0.025*SL	0.92 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
E to QN1	t_{PLH}	1.12	1.04 + 0.040*SL	1.03 + 0.041*SL	1.03 + 0.041*SL
	t_{PHL}	0.94	0.88 + 0.029*SL	0.89 + 0.025*SL	0.90 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN1	t_{PLH}	0.48	0.40 + 0.040*SL	0.40 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
CK to QN2	t_{PLH}	1.13	1.05 + 0.040*SL	1.05 + 0.041*SL	1.05 + 0.042*SL
	t_{PHL}	0.95	0.89 + 0.030*SL	0.91 + 0.025*SL	0.92 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
E to QN2	t_{PLH}	1.12	1.04 + 0.040*SL	1.03 + 0.041*SL	1.03 + 0.041*SL
	t_{PHL}	0.94	0.88 + 0.030*SL	0.89 + 0.025*SL	0.90 + 0.023*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN2	t_{PLH}	0.48	0.40 + 0.040*SL	0.40 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.27	0.09 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
CK to QN3	t_{PLH}	1.13	1.05 + 0.040*SL	1.05 + 0.041*SL	1.04 + 0.042*SL
	t_{PHL}	0.95	0.89 + 0.030*SL	0.90 + 0.025*SL	0.91 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.09 + 0.039*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
E to QN3	t_{PLH}	1.11	1.03 + 0.040*SL	1.03 + 0.041*SL	1.02 + 0.042*SL
	t_{PHL}	0.93	0.87 + 0.029*SL	0.88 + 0.025*SL	0.89 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.16	0.09 + 0.039*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
RN to QN3	t_{PLH}	0.47	0.40 + 0.040*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FG2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.18	1.07 + 0.055*SL	1.08 + 0.051*SL	1.09 + 0.050*SL
	t_{PHL}	1.41	1.33 + 0.036*SL	1.36 + 0.027*SL	1.39 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
E to Q0	t_{PLH}	1.17	1.06 + 0.055*SL	1.07 + 0.051*SL	1.08 + 0.050*SL
	t_{PHL}	1.40	1.32 + 0.036*SL	1.35 + 0.027*SL	1.39 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q0	t_{PHL}	0.44	0.36 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.045*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to Q1	t_{PLH}	1.19	1.08 + 0.054*SL	1.09 + 0.051*SL	1.10 + 0.050*SL
	t_{PHL}	1.41	1.34 + 0.035*SL	1.36 + 0.027*SL	1.40 + 0.023*SL
	t_R	0.37	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
E to Q1	t_{PLH}	1.18	1.07 + 0.055*SL	1.08 + 0.051*SL	1.09 + 0.050*SL
	t_{PHL}	1.40	1.33 + 0.035*SL	1.35 + 0.027*SL	1.39 + 0.024*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q1	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to Q2	t_{PLH}	1.19	1.08 + 0.054*SL	1.09 + 0.051*SL	1.10 + 0.050*SL
	t_{PHL}	1.41	1.34 + 0.035*SL	1.36 + 0.027*SL	1.40 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
E to Q2	t_{PLH}	1.18	1.07 + 0.054*SL	1.08 + 0.051*SL	1.09 + 0.050*SL
	t_{PHL}	1.40	1.33 + 0.035*SL	1.35 + 0.027*SL	1.39 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q2	t_{PHL}	0.44	0.37 + 0.036*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.045*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
CK to Q3	t_{PLH}	1.18	1.07 + 0.055*SL	1.08 + 0.051*SL	1.09 + 0.050*SL
	t_{PHL}	1.41	1.33 + 0.036*SL	1.36 + 0.027*SL	1.39 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
E to Q3	t_{PLH}	1.17	1.06 + 0.055*SL	1.07 + 0.051*SL	1.08 + 0.050*SL
	t_{PHL}	1.40	1.32 + 0.036*SL	1.35 + 0.027*SL	1.39 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q3	t_{PHL}	0.44	0.36 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_F	0.22	0.13 + 0.045*SL	0.14 + 0.041*SL	0.13 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FG2X4

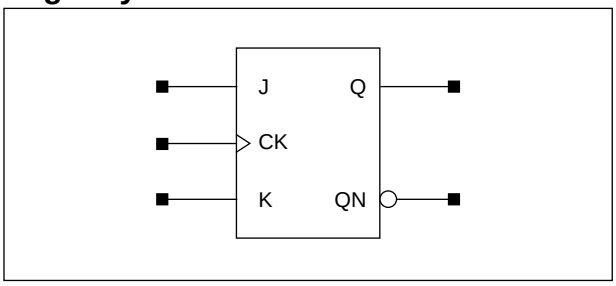
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.60	1.50 + 0.049*SL	1.50 + 0.050*SL	1.50 + 0.050*SL
	t_{PHL}	1.30	1.24 + 0.032*SL	1.26 + 0.026*SL	1.28 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.042*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
E to QN0	t_{PLH}	1.59	1.49 + 0.049*SL	1.49 + 0.050*SL	1.49 + 0.050*SL
	t_{PHL}	1.29	1.23 + 0.032*SL	1.25 + 0.026*SL	1.27 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.042*SL	0.11 + 0.041*SL	0.10 + 0.043*SL
RN to QN0	t_{PLH}	0.64	0.54 + 0.048*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
CK to QN1	t_{PLH}	1.61	1.51 + 0.049*SL	1.51 + 0.050*SL	1.51 + 0.050*SL
	t_{PHL}	1.32	1.25 + 0.033*SL	1.27 + 0.026*SL	1.29 + 0.023*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
E to QN1	t_{PLH}	1.60	1.50 + 0.049*SL	1.50 + 0.050*SL	1.50 + 0.050*SL
	t_{PHL}	1.31	1.24 + 0.033*SL	1.26 + 0.026*SL	1.29 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN1	t_{PLH}	0.64	0.54 + 0.049*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
CK to QN2	t_{PLH}	1.61	1.51 + 0.049*SL	1.51 + 0.050*SL	1.51 + 0.050*SL
	t_{PHL}	1.31	1.25 + 0.033*SL	1.27 + 0.026*SL	1.29 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
E to QN2	t_{PLH}	1.60	1.50 + 0.049*SL	1.50 + 0.050*SL	1.50 + 0.050*SL
	t_{PHL}	1.30	1.24 + 0.033*SL	1.26 + 0.026*SL	1.28 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN2	t_{PLH}	0.64	0.54 + 0.049*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
CK to QN3	t_{PLH}	1.60	1.50 + 0.049*SL	1.50 + 0.050*SL	1.50 + 0.050*SL
	t_{PHL}	1.30	1.24 + 0.032*SL	1.26 + 0.026*SL	1.28 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.042*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
E to QN3	t_{PLH}	1.59	1.49 + 0.049*SL	1.49 + 0.050*SL	1.49 + 0.050*SL
	t_{PHL}	1.29	1.23 + 0.032*SL	1.25 + 0.026*SL	1.27 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.042*SL	0.11 + 0.041*SL	0.10 + 0.043*SL
RN to QN3	t_{PLH}	0.64	0.54 + 0.048*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FJ1/FJ1D2

JK Flip-Flop with 1X/2X Drive

Logic Symbol



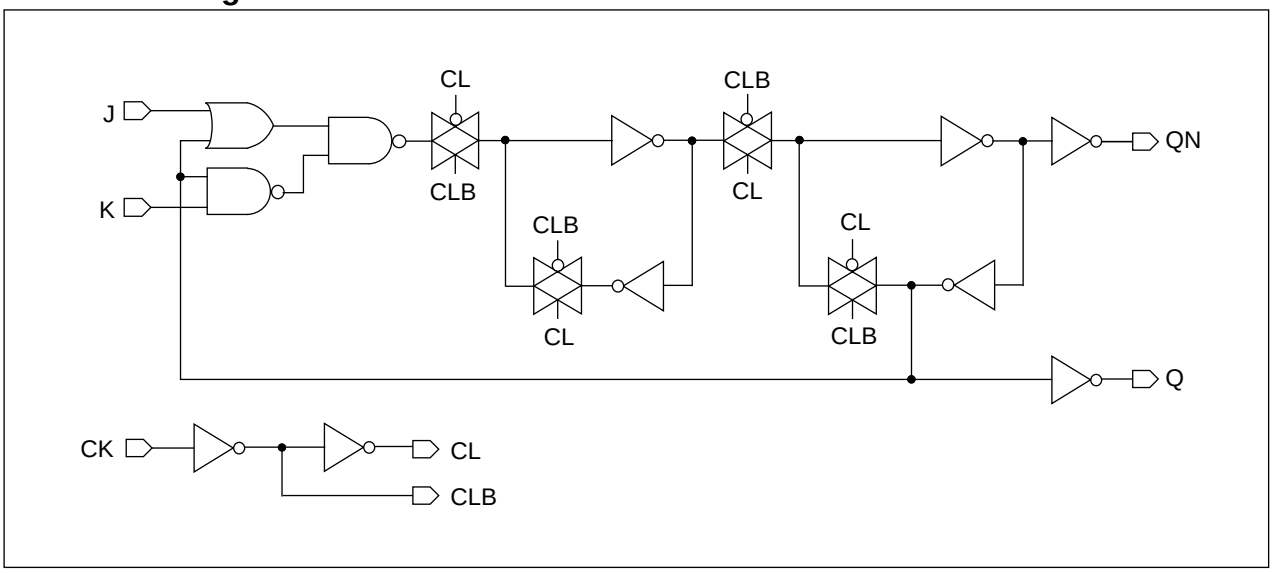
Truth Table

J	CK	K	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	0	1	0
0	↑	0	Q (n)	QN (n)
1	↑	1	QN (n)	Q (n)
x	↓	x	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
KG80							
FJ1			*FJ1D2*			*FJ1*	*FJ1D2*
J	CK	K	J	CK	K		
0.5	0.9	0.9	0.5	0.9	0.9	9.0	12.0
KGM80							
FJ1			*FJ1D2*			*FJ1*	*FJ1D2*
J	CK	K	J	CK	K		
1.0	1.0	1.0	1.0	1.0	1.0	9.0	12.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FJ1	FJ1D2	FJ1	FJ1D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (J to CK)	t_{SU}	0.42	0.42	0.77	0.77
Input Hold Time (J to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.42	0.42	0.77	0.77
Input Hold Time (K to CK)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FJ1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.73	0.65 + 0.041*SL	0.65 + 0.041*SL	0.64 + 0.041*SL
	t_{PHL}	0.66	0.59 + 0.035*SL	0.61 + 0.028*SL	0.63 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.039*SL	0.12 + 0.040*SL
CK to QN	t_{PLH}	0.50	0.42 + 0.042*SL	0.42 + 0.042*SL	0.42 + 0.042*SL
	t_{PHL}	0.53	0.47 + 0.030*SL	0.48 + 0.025*SL	0.49 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.041*SL	0.08 + 0.042*SL

KG80 FJ1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.71 + 0.022*SL	0.72 + 0.020*SL	0.72 + 0.020*SL
	t_{PHL}	0.69	0.64 + 0.023*SL	0.66 + 0.017*SL	0.68 + 0.014*SL
	t_R	0.18	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.020*SL	0.14 + 0.020*SL
CK to QN	t_{PLH}	0.48	0.44 + 0.023*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.53	0.48 + 0.021*SL	0.50 + 0.015*SL	0.51 + 0.013*SL
	t_R	0.17	0.09 + 0.039*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FJ1

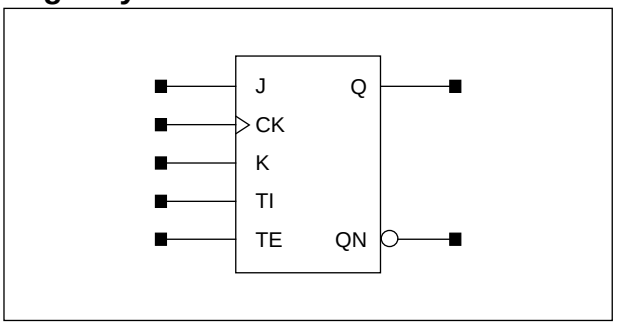
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.02	0.92 + 0.050*SL	0.92 + 0.050*SL	0.92 + 0.050*SL
	t_{PHL}	0.93	0.85 + 0.040*SL	0.88 + 0.029*SL	0.93 + 0.024*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.24	0.15 + 0.047*SL	0.17 + 0.041*SL	0.16 + 0.041*SL
CK to QN	t_{PLH}	0.70	0.59 + 0.051*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.74	0.67 + 0.034*SL	0.69 + 0.026*SL	0.72 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL

KGM80 FJ1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.06	1.01 + 0.027*SL	1.01 + 0.024*SL	1.01 + 0.025*SL
	t_{PHL}	0.98	0.92 + 0.027*SL	0.94 + 0.019*SL	0.99 + 0.014*SL
	t_R	0.23	0.13 + 0.052*SL	0.13 + 0.052*SL	0.11 + 0.053*SL
	t_F	0.21	0.15 + 0.029*SL	0.17 + 0.022*SL	0.19 + 0.020*SL
CK to QN	t_{PLH}	0.67	0.61 + 0.028*SL	0.62 + 0.025*SL	0.62 + 0.025*SL
	t_{PHL}	0.74	0.70 + 0.023*SL	0.72 + 0.016*SL	0.75 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



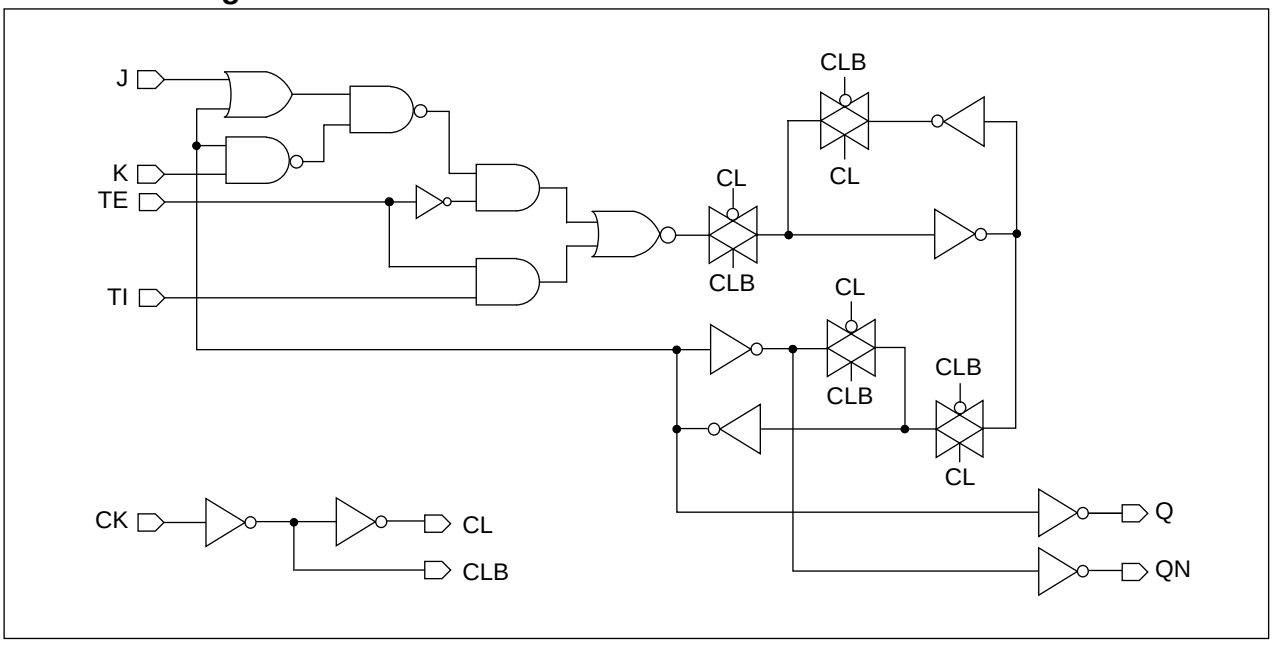
Truth Table

J	CK	K	TI	TE	Q (n+1)	QN (n+1)
0	↑	1	x	0	0	1
1	↑	0	x	0	1	0
0	↑	0	x	0	Q (n)	QN (n)
1	↑	1	x	0	QN (n)	Q (n)
x	↓	x	x	x	Q (n)	QN (n)
x	↑	x	0	1	0	1
x	↑	x	1	1	1	0

Cell Data

Input Load (SL)										Gate Count	
KG80											
FJ1S					*FJ1SD2*					*FJ1S*	*FJ1SD2*
J	CK	K	TI	TE	J	CK	K	TI	TE		
0.9	0.9	0.8	0.9	1.6	0.9	0.9	0.8	0.9	1.6	11.0	12.0
KGM80											
FJ1S					*FJ1SD2*					*FJ1S*	*FJ1SD2*
J	CK	K	TI	TE	J	CK	K	TI	TE		
1.0	1.0	1.0	1.0	2.0	1.0	1.0	1.0	1.0	2.0	11.0	12.0

Schematic Diagram



FJ1S/FJ1SD2

JK Flip-Flop with Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FJ1S	FJ1SD2	FJ1S	FJ1SD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (J to CK)	t_{SU}	0.64	0.64	1.14	1.14
Input Hold Time (J to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.64	0.64	1.14	1.14
Input Hold Time (K to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.50	0.50	0.93	0.93
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.47	0.50	0.86	0.86
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FJ1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.50 + 0.043*SL	0.50 + 0.042*SL	0.50 + 0.042*SL
	t_{PHL}	0.62	0.55 + 0.036*SL	0.57 + 0.028*SL	0.59 + 0.025*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.040*SL	0.13 + 0.040*SL
CK to QN	t_{PLH}	0.76	0.68 + 0.040*SL	0.67 + 0.041*SL	0.67 + 0.042*SL
	t_{PHL}	0.66	0.60 + 0.030*SL	0.61 + 0.025*SL	0.62 + 0.023*SL
	t_R	0.26	0.09 + 0.085*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL

KG80 FJ1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.56	0.51 + 0.025*SL	0.51 + 0.021*SL	0.52 + 0.021*SL
	t_{PHL}	0.61	0.56 + 0.025*SL	0.57 + 0.018*SL	0.59 + 0.015*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.042*SL	0.09 + 0.044*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
CK to QN	t_{PLH}	0.79	0.75 + 0.020*SL	0.75 + 0.019*SL	0.74 + 0.020*SL
	t_{PHL}	0.69	0.65 + 0.019*SL	0.66 + 0.015*SL	0.68 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.020*SL	0.10 + 0.019*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FJ1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.80	0.69 + 0.053*SL	0.70 + 0.050*SL	0.71 + 0.050*SL
	t_{PHL}	0.87	0.79 + 0.042*SL	0.82 + 0.030*SL	0.88 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.25	0.16 + 0.048*SL	0.18 + 0.041*SL	0.18 + 0.041*SL
CK to QN	t_{PLH}	1.07	0.97 + 0.050*SL	0.97 + 0.050*SL	0.97 + 0.050*SL
	t_{PHL}	0.92	0.85 + 0.033*SL	0.87 + 0.026*SL	0.90 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL

KGM80 FJ1SD2

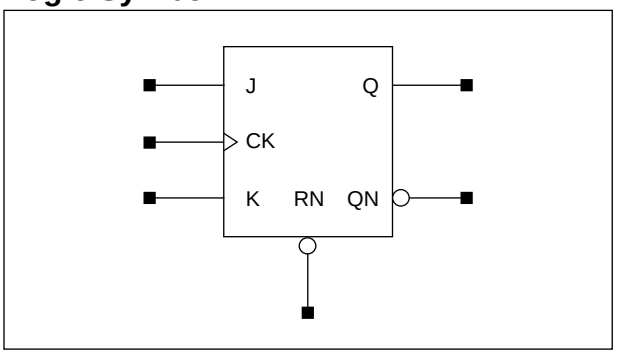
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.70 + 0.030*SL	0.71 + 0.026*SL	0.72 + 0.025*SL
	t_{PHL}	0.86	0.80 + 0.029*SL	0.83 + 0.019*SL	0.88 + 0.015*SL
	t_R	0.24	0.13 + 0.051*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.21	0.16 + 0.027*SL	0.17 + 0.023*SL	0.19 + 0.020*SL
CK to QN	t_{PLH}	1.12	1.07 + 0.025*SL	1.07 + 0.024*SL	1.06 + 0.025*SL
	t_{PHL}	0.97	0.93 + 0.021*SL	0.94 + 0.016*SL	0.97 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.17	0.11 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

FJ2/FJ2D2

JK Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



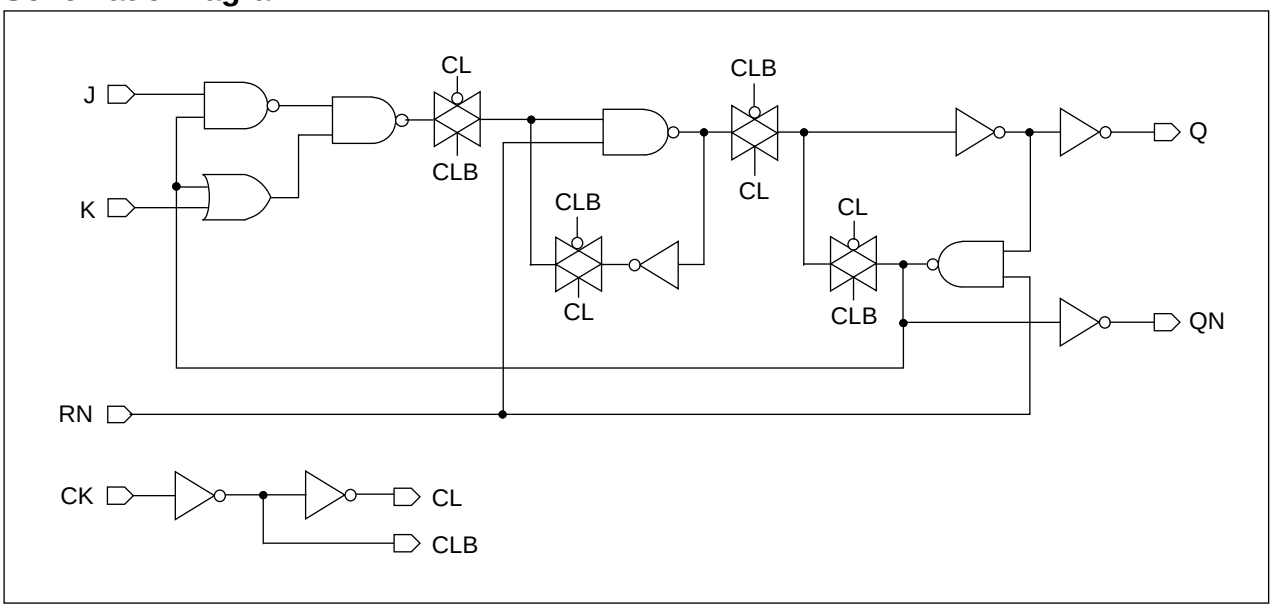
Truth Table

J	CK	K	RN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	0	1	1	0
0	↑	0	1	Q (n)	QN (n)
1	↑	1	1	QN (n)	Q (n)
x	↓	x	1	Q (n)	QN (n)
x	x	x	0	0	1

Cell DataCell Data

Input Load (SL)								Gate Count	
KG80									
FJ2				*FJ2D2*				*FJ2*	*FJ2D2*
J	CK	K	RN	J	CK	K	RN		
0.5	0.9	0.9	1.6	0.5	0.9	0.9	1.6	10.0	11.0
KGM80									
FJ2				*FJ2D2*				*FJ2*	*FJ2D2*
J	CK	K	RN	J	CK	K	RN		
1.0	1.0	1.0	1.9	1.0	1.0	1.0	1.9	10.0	11.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FJ2	FJ2D2	FJ2	FJ2D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (J to CK)	t_{SU}	0.50	0.50	0.83	0.83
Input Hold Time (J to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.50	0.50	0.83	0.83
Input Hold Time (K to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FJ2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.86	0.77 + 0.045*SL	0.78 + 0.042*SL	0.78 + 0.041*SL
	t_{PHL}	0.69	0.62 + 0.035*SL	0.64 + 0.028*SL	0.66 + 0.025*SL
	t_R	0.31	0.14 + 0.086*SL	0.14 + 0.087*SL	0.12 + 0.089*SL
	t_F	0.21	0.12 + 0.042*SL	0.13 + 0.040*SL	0.13 + 0.040*SL
RN to Q	t_{PHL}	0.42	0.34 + 0.038*SL	0.37 + 0.027*SL	0.39 + 0.023*SL
	t_F	0.22	0.15 + 0.039*SL	0.15 + 0.036*SL	0.14 + 0.038*SL
CK to QN	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.57	0.51 + 0.031*SL	0.52 + 0.025*SL	0.53 + 0.024*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN	t_{PLH}	0.60	0.52 + 0.042*SL	0.52 + 0.041*SL	0.52 + 0.042*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.090*SL

KG80 FJ2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.90	0.85 + 0.026*SL	0.86 + 0.022*SL	0.86 + 0.021*SL
	t_{PHL}	0.71	0.66 + 0.023*SL	0.68 + 0.017*SL	0.70 + 0.014*SL
	t_R	0.22	0.13 + 0.042*SL	0.13 + 0.043*SL	0.13 + 0.043*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
RN to Q	t_{PHL}	0.40	0.35 + 0.026*SL	0.37 + 0.018*SL	0.40 + 0.014*SL
	t_F	0.19	0.15 + 0.023*SL	0.16 + 0.019*SL	0.17 + 0.018*SL
CK to QN	t_{PLH}	0.49	0.45 + 0.023*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.57	0.53 + 0.021*SL	0.54 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.020*SL	0.10 + 0.020*SL
RN to QN	t_{PLH}	0.58	0.54 + 0.023*SL	0.54 + 0.021*SL	0.55 + 0.020*SL
	t_R	0.17	0.10 + 0.039*SL	0.09 + 0.043*SL	0.08 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FJ2

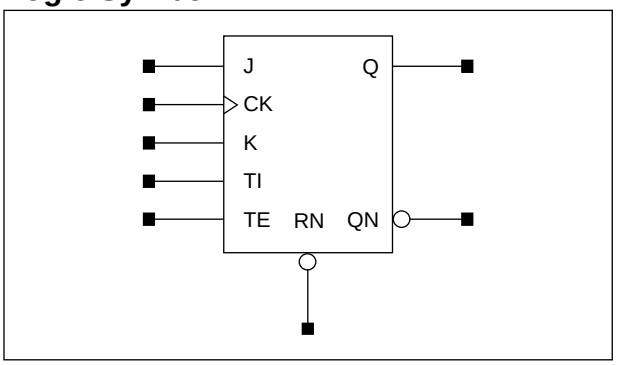
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.21	1.09 + 0.057*SL	1.11 + 0.051*SL	1.12 + 0.050*SL
	t_{PHL}	0.97	0.89 + 0.041*SL	0.92 + 0.029*SL	0.98 + 0.024*SL
	t_R	0.40	0.19 + 0.105*SL	0.19 + 0.105*SL	0.17 + 0.107*SL
	t_F	0.25	0.16 + 0.047*SL	0.17 + 0.041*SL	0.18 + 0.041*SL
RN to Q	t_{PHL}	0.56	0.47 + 0.044*SL	0.51 + 0.029*SL	0.57 + 0.024*SL
	t_F	0.27	0.18 + 0.045*SL	0.20 + 0.038*SL	0.18 + 0.040*SL
CK to QN	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.75 + 0.026*SL	0.77 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
RN to QN	t_{PLH}	0.84	0.74 + 0.050*SL	0.74 + 0.050*SL	0.74 + 0.050*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.108*SL	0.12 + 0.109*SL

KGM80 FJ2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.26	1.19 + 0.032*SL	1.21 + 0.027*SL	1.23 + 0.025*SL
	t_{PHL}	1.01	0.95 + 0.028*SL	0.98 + 0.019*SL	1.02 + 0.015*SL
	t_R	0.27	0.16 + 0.056*SL	0.17 + 0.052*SL	0.17 + 0.052*SL
	t_F	0.21	0.15 + 0.028*SL	0.17 + 0.022*SL	0.19 + 0.020*SL
RN to Q	t_{PHL}	0.54	0.48 + 0.030*SL	0.51 + 0.020*SL	0.57 + 0.014*SL
	t_F	0.23	0.17 + 0.029*SL	0.20 + 0.021*SL	0.22 + 0.019*SL
CK to QN	t_{PLH}	0.68	0.62 + 0.029*SL	0.63 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.80	0.76 + 0.023*SL	0.77 + 0.017*SL	0.81 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.14 + 0.021*SL
RN to QN	t_{PLH}	0.82	0.76 + 0.028*SL	0.77 + 0.025*SL	0.77 + 0.025*SL
	t_R	0.22	0.13 + 0.049*SL	0.12 + 0.052*SL	0.10 + 0.054*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



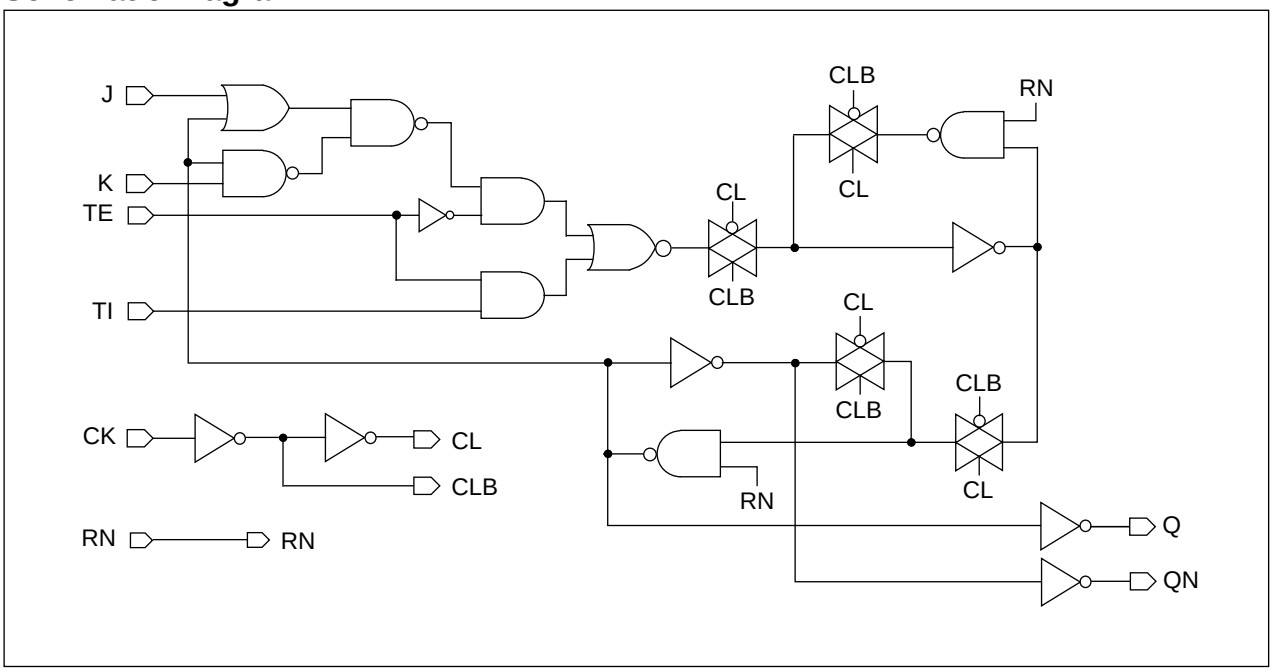
Truth Table

J	CK	K	TI	TE	RN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	0	1
1	↑	0	x	0	1	1	0
0	↑	0	x	0	1	Q (n)	QN (n)
1	↑	1	x	0	1	QN (n)	Q (n)
x	↓	x	x	0	1	Q (n)	QN (n)
x	x	x	x	x	0	0	1
x	↑	x	0	1	1	0	1
x	↑	x	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
KG80													
FJ2S						*FJ2SD2*						*FJ2S*	*FJ2S D2*
J	CK	K	TI	TE	RN	J	CK	K	TI	TE	RN		
0.9	0.9	0.8	0.8	1.6	1.9	0.9	0.9	0.8	0.8	1.6	1.8	12.0	13.0
KGM80													
FJ2S						*FJ2SD2*						*FJ2S*	*FJ2S D2*
J	CK	K	TI	TE	RN	J	CK	K	TI	TE	RN		
1.0	1.0	1.0	0.9	2.0	2.2	1.0	1.0	1.0	0.9	2.0	2.1	12.0	13.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FJ2S	FJ2SD2	FJ2S	FJ2SD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width High (RN)	t_{PWH}	0.61	0.61	0.99	1.02
Input Setup Time (J to CK)	t_{SU}	0.64	0.64	1.14	1.14
Input Hold Time (J to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.64	0.64	1.14	1.14
Input Hold Time (K to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.50	0.50	0.93	0.93
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.50	0.50	0.86	0.86
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.63	0.63

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FJ2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.58 + 0.047*SL	0.59 + 0.043*SL	0.60 + 0.041*SL
	t_{PHL}	0.63	0.56 + 0.038*SL	0.58 + 0.029*SL	0.61 + 0.025*SL
	t_R	0.31	0.14 + 0.086*SL	0.14 + 0.087*SL	0.13 + 0.089*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.040*SL	0.14 + 0.040*SL
RN to Q	t_{PHL}	0.43	0.34 + 0.041*SL	0.37 + 0.029*SL	0.41 + 0.024*SL
	t_F	0.24	0.15 + 0.042*SL	0.17 + 0.037*SL	0.15 + 0.038*SL
CK to QN	t_{PLH}	0.77	0.69 + 0.040*SL	0.69 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.75	0.69 + 0.030*SL	0.70 + 0.025*SL	0.72 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.039*SL	0.08 + 0.042*SL
RN to QN	t_{PLH}	0.57	0.49 + 0.040*SL	0.48 + 0.041*SL	0.48 + 0.042*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL

KG80 FJ2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.66	0.60 + 0.028*SL	0.61 + 0.023*SL	0.62 + 0.022*SL
	t_{PHL}	0.62	0.57 + 0.025*SL	0.58 + 0.018*SL	0.61 + 0.015*SL
	t_R	0.22	0.14 + 0.042*SL	0.14 + 0.043*SL	0.13 + 0.043*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
RN to Q	t_{PHL}	0.41	0.35 + 0.027*SL	0.37 + 0.019*SL	0.40 + 0.014*SL
	t_F	0.20	0.15 + 0.025*SL	0.16 + 0.019*SL	0.18 + 0.018*SL
CK to QN	t_{PLH}	0.80	0.76 + 0.020*SL	0.76 + 0.019*SL	0.76 + 0.020*SL
	t_{PHL}	0.80	0.76 + 0.018*SL	0.77 + 0.015*SL	0.78 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
RN to QN	t_{PLH}	0.59	0.55 + 0.019*SL	0.55 + 0.019*SL	0.55 + 0.020*SL
	t_R	0.17	0.09 + 0.040*SL	0.09 + 0.042*SL	0.07 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FJ2S

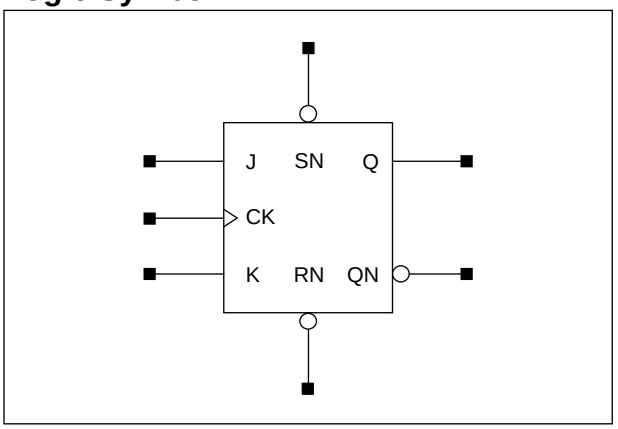
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.93	0.81 + 0.059*SL	0.83 + 0.052*SL	0.85 + 0.050*SL
	t_{PHL}	0.90	0.81 + 0.043*SL	0.84 + 0.030*SL	0.91 + 0.025*SL
	t_R	0.41	0.19 + 0.106*SL	0.20 + 0.105*SL	0.17 + 0.107*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.041*SL	0.19 + 0.041*SL
RN to Q	t_{PHL}	0.57	0.47 + 0.046*SL	0.52 + 0.031*SL	0.59 + 0.024*SL
	t_F	0.28	0.18 + 0.050*SL	0.21 + 0.039*SL	0.20 + 0.040*SL
CK to QN	t_{PLH}	1.10	1.00 + 0.049*SL	1.00 + 0.050*SL	1.00 + 0.050*SL
	t_{PHL}	1.05	0.99 + 0.033*SL	1.01 + 0.026*SL	1.03 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.041*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.77	0.67 + 0.049*SL	0.67 + 0.049*SL	0.67 + 0.050*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.12 + 0.109*SL

KGM80 FJ2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.90	0.83 + 0.034*SL	0.85 + 0.029*SL	0.87 + 0.026*SL
	t_{PHL}	0.88	0.82 + 0.030*SL	0.85 + 0.020*SL	0.90 + 0.015*SL
	t_R	0.28	0.16 + 0.056*SL	0.17 + 0.053*SL	0.17 + 0.053*SL
	t_F	0.22	0.16 + 0.029*SL	0.18 + 0.023*SL	0.20 + 0.021*SL
RN to Q	t_{PHL}	0.55	0.48 + 0.031*SL	0.51 + 0.021*SL	0.58 + 0.015*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.022*SL	0.23 + 0.019*SL
CK to QN	t_{PLH}	1.14	1.09 + 0.025*SL	1.09 + 0.024*SL	1.08 + 0.025*SL
	t_{PHL}	1.12	1.08 + 0.021*SL	1.09 + 0.016*SL	1.12 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.18	0.12 + 0.025*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
RN to QN	t_{PLH}	0.81	0.77 + 0.024*SL	0.77 + 0.024*SL	0.76 + 0.025*SL
	t_R	0.22	0.12 + 0.051*SL	0.12 + 0.052*SL	0.10 + 0.054*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



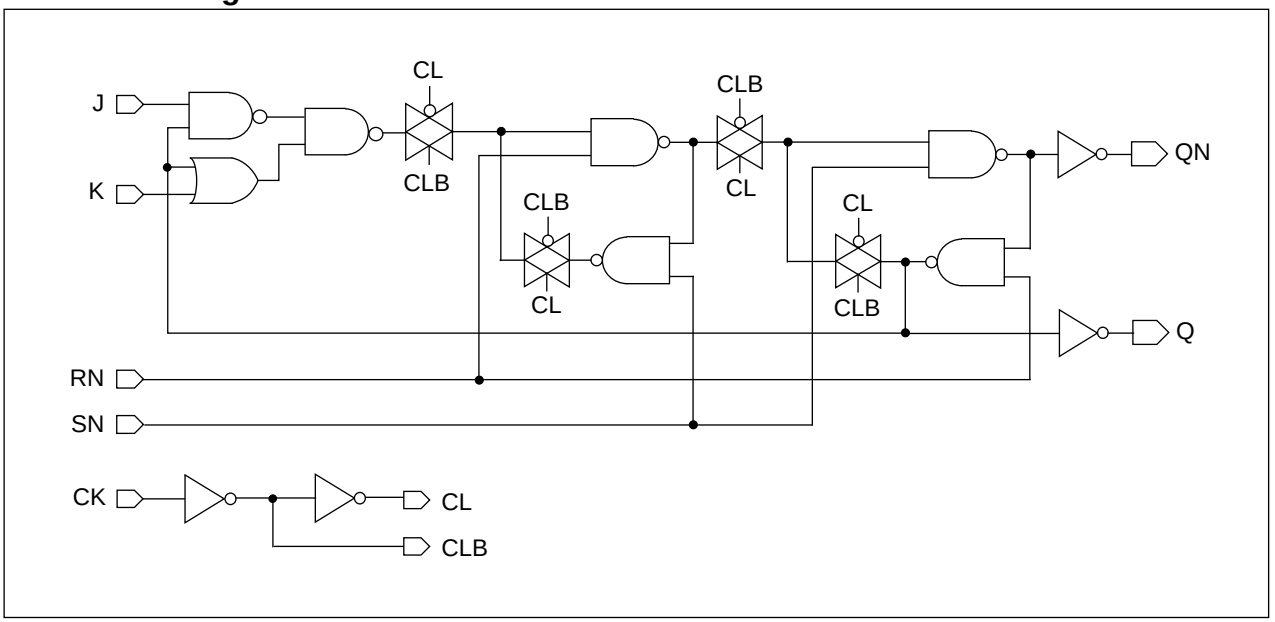
Truth Table

J	CK	K	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	1	0	1
1	↑	0	1	1	1	0
0	↑	0	1	1	Q (n)	QN (n)
1	↑	1	1	1	QN (n)	Q (n)
x	↓	x	1	1	Q (n)	QN (n)
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

Cell Data

Input Load (SL)										Gate Count	
KG80											
FJ4					*FJ4D2*					*FJ4*	*FJ4D2*
J	CK	K	RN	SN	J	CK	K	RN	SN		
0.9	0.9	0.8	1.8	1.7	0.9	0.9	0.7	1.7	1.7	11.0	12.0
KGM80											
FJ4					*FJ4D2*					*FJ4*	*FJ4D2*
J	CK	K	RN	SN	J	CK	K	RN	SN		
1.0	1.0	1.0	2.2	2.2	1.0	1.0	1.0	2.2	2.2	11.0	12.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FJ4	FJ4D2	FJ4	FJ4D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0;64	1.05	0.79
Input Setup Time (J to CK)	t_{SU}	0.47	0.47	0.83	0.83
Input Hold Time (J to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.47	0.47	0.83	0.83
Input Hold Time (K to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.15	0.15	0.41	0.41
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.42	0.42	0.85	0.85

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FJ4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.87	0.78 + 0.045*SL	0.79 + 0.042*SL	0.79 + 0.041*SL
	t_{PHL}	0.76	0.68 + 0.035*SL	0.70 + 0.028*SL	0.73 + 0.025*SL
	t_R	0.31	0.14 + 0.086*SL	0.13 + 0.087*SL	0.12 + 0.089*SL
	t_F	0.21	0.13 + 0.041*SL	0.13 + 0.039*SL	0.13 + 0.040*SL
RN to Q	t_{PLH}	0.39	0.29 + 0.048*SL	0.31 + 0.042*SL	0.31 + 0.041*SL
	t_{PHL}	0.41	0.34 + 0.038*SL	0.36 + 0.028*SL	0.39 + 0.024*SL
	t_R	0.31	0.14 + 0.084*SL	0.13 + 0.086*SL	0.12 + 0.089*SL
	t_F	0.23	0.14 + 0.043*SL	0.16 + 0.037*SL	0.14 + 0.039*SL
SN to Q	t_{PLH}	0.64	0.55 + 0.045*SL	0.55 + 0.041*SL	0.56 + 0.041*SL
	t_R	0.31	0.14 + 0.085*SL	0.13 + 0.086*SL	0.11 + 0.089*SL
CK to QN	t_{PLH}	0.58	0.49 + 0.044*SL	0.50 + 0.042*SL	0.50 + 0.042*SL
	t_{PHL}	0.58	0.52 + 0.031*SL	0.53 + 0.026*SL	0.54 + 0.024*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.089*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to QN	t_{PLH}	0.67	0.58 + 0.044*SL	0.59 + 0.041*SL	0.59 + 0.041*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
SN to QN	t_{PLH}	0.30	0.22 + 0.044*SL	0.22 + 0.041*SL	0.22 + 0.041*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.024*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.040*SL	0.10 + 0.040*SL

KG80 FJ4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.91	0.85 + 0.026*SL	0.86 + 0.022*SL	0.87 + 0.021*SL
	t_{PHL}	0.79	0.75 + 0.023*SL	0.76 + 0.017*SL	0.78 + 0.014*SL
	t_R	0.21	0.13 + 0.042*SL	0.13 + 0.043*SL	0.13 + 0.043*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.020*SL	0.15 + 0.020*SL
RN to Q	t_{PLH}	0.37	0.32 + 0.027*SL	0.33 + 0.023*SL	0.34 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.026*SL	0.36 + 0.019*SL	0.39 + 0.014*SL
	t_R	0.21	0.13 + 0.043*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.19	0.14 + 0.026*SL	0.16 + 0.019*SL	0.17 + 0.018*SL
SN to Q	t_{PLH}	0.67	0.62 + 0.025*SL	0.63 + 0.022*SL	0.63 + 0.020*SL
	t_R	0.21	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.043*SL
CK to QN	t_{PLH}	0.58	0.53 + 0.024*SL	0.54 + 0.022*SL	0.54 + 0.021*SL
	t_{PHL}	0.59	0.55 + 0.020*SL	0.56 + 0.015*SL	0.57 + 0.013*SL
	t_R	0.21	0.13 + 0.042*SL	0.13 + 0.043*SL	0.12 + 0.044*SL
	t_F	0.16	0.12 + 0.022*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
RN to QN	t_{PLH}	0.67	0.63 + 0.024*SL	0.63 + 0.022*SL	0.64 + 0.021*SL
	t_R	0.22	0.13 + 0.042*SL	0.13 + 0.042*SL	0.12 + 0.044*SL
SN to QN	t_{PLH}	0.30	0.25 + 0.023*SL	0.26 + 0.022*SL	0.26 + 0.021*SL
	t_{PHL}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.33 + 0.013*SL
	t_R	0.22	0.15 + 0.032*SL	0.13 + 0.042*SL	0.12 + 0.044*SL
	t_F	0.17	0.13 + 0.021*SL	0.13 + 0.020*SL	0.13 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FJ4

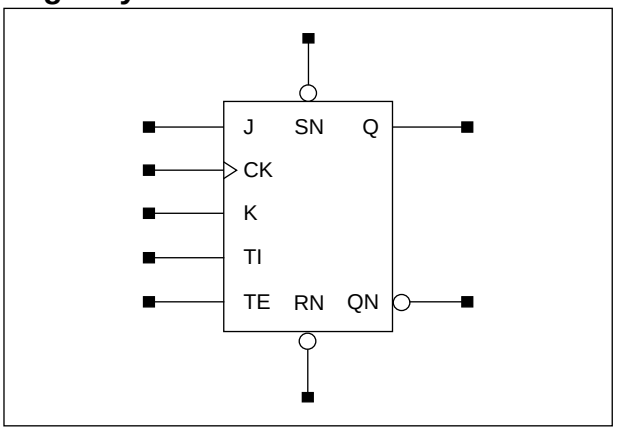
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.23	1.11 + 0.057*SL	1.13 + 0.051*SL	1.14 + 0.050*SL
	t_{PHL}	1.08	0.99 + 0.041*SL	1.03 + 0.029*SL	1.07 + 0.025*SL
	t_R	0.40	0.19 + 0.105*SL	0.19 + 0.105*SL	0.16 + 0.108*SL
	t_F	0.25	0.16 + 0.046*SL	0.18 + 0.041*SL	0.17 + 0.041*SL
RN to Q	t_{PLH}	0.53	0.41 + 0.058*SL	0.43 + 0.051*SL	0.44 + 0.050*SL
	t_{PHL}	0.55	0.46 + 0.044*SL	0.50 + 0.030*SL	0.57 + 0.024*SL
	t_R	0.40	0.19 + 0.103*SL	0.18 + 0.105*SL	0.15 + 0.108*SL
	t_F	0.27	0.17 + 0.048*SL	0.20 + 0.040*SL	0.19 + 0.040*SL
SN to Q	t_{PLH}	0.86	0.74 + 0.056*SL	0.76 + 0.050*SL	0.77 + 0.050*SL
	t_R	0.39	0.19 + 0.104*SL	0.18 + 0.105*SL	0.15 + 0.108*SL
CK to QN	t_{PLH}	0.81	0.70 + 0.054*SL	0.71 + 0.051*SL	0.72 + 0.050*SL
	t_{PHL}	0.82	0.75 + 0.036*SL	0.77 + 0.027*SL	0.80 + 0.024*SL
	t_R	0.37	0.17 + 0.104*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.042*SL
RN to QN	t_{PLH}	0.94	0.83 + 0.054*SL	0.84 + 0.050*SL	0.85 + 0.050*SL
	t_R	0.38	0.17 + 0.103*SL	0.16 + 0.106*SL	0.14 + 0.108*SL
SN to QN	t_{PLH}	0.41	0.30 + 0.054*SL	0.32 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.40 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.14 + 0.043*SL	0.14 + 0.042*SL	0.14 + 0.042*SL

KGM80 FJ4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.28	1.21 + 0.032*SL	1.23 + 0.027*SL	1.25 + 0.025*SL
	t_{PHL}	1.13	1.08 + 0.027*SL	1.10 + 0.019*SL	1.14 + 0.015*SL
	t_R	0.27	0.16 + 0.057*SL	0.17 + 0.052*SL	0.17 + 0.052*SL
	t_F	0.22	0.16 + 0.028*SL	0.18 + 0.022*SL	0.20 + 0.020*SL
RN to Q	t_{PLH}	0.49	0.43 + 0.034*SL	0.44 + 0.028*SL	0.47 + 0.025*SL
	t_{PHL}	0.54	0.48 + 0.031*SL	0.50 + 0.020*SL	0.57 + 0.015*SL
	t_R	0.27	0.16 + 0.056*SL	0.17 + 0.052*SL	0.16 + 0.052*SL
	t_F	0.23	0.17 + 0.030*SL	0.19 + 0.022*SL	0.22 + 0.019*SL
SN to Q	t_{PLH}	0.90	0.84 + 0.032*SL	0.85 + 0.027*SL	0.87 + 0.025*SL
	t_R	0.27	0.16 + 0.056*SL	0.17 + 0.052*SL	0.16 + 0.052*SL
CK to QN	t_{PLH}	0.81	0.75 + 0.030*SL	0.76 + 0.026*SL	0.78 + 0.025*SL
	t_{PHL}	0.84	0.79 + 0.023*SL	0.81 + 0.016*SL	0.84 + 0.013*SL
	t_R	0.28	0.18 + 0.052*SL	0.18 + 0.052*SL	0.17 + 0.053*SL
	t_F	0.19	0.15 + 0.024*SL	0.15 + 0.021*SL	0.16 + 0.021*SL
RN to QN	t_{PLH}	0.95	0.89 + 0.031*SL	0.90 + 0.026*SL	0.91 + 0.025*SL
	t_R	0.29	0.18 + 0.052*SL	0.19 + 0.052*SL	0.17 + 0.053*SL
SN to QN	t_{PLH}	0.41	0.35 + 0.030*SL	0.36 + 0.026*SL	0.37 + 0.025*SL
	t_{PHL}	0.46	0.41 + 0.023*SL	0.43 + 0.017*SL	0.46 + 0.013*SL
	t_R	0.28	0.18 + 0.051*SL	0.18 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.20	0.15 + 0.024*SL	0.16 + 0.021*SL	0.17 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



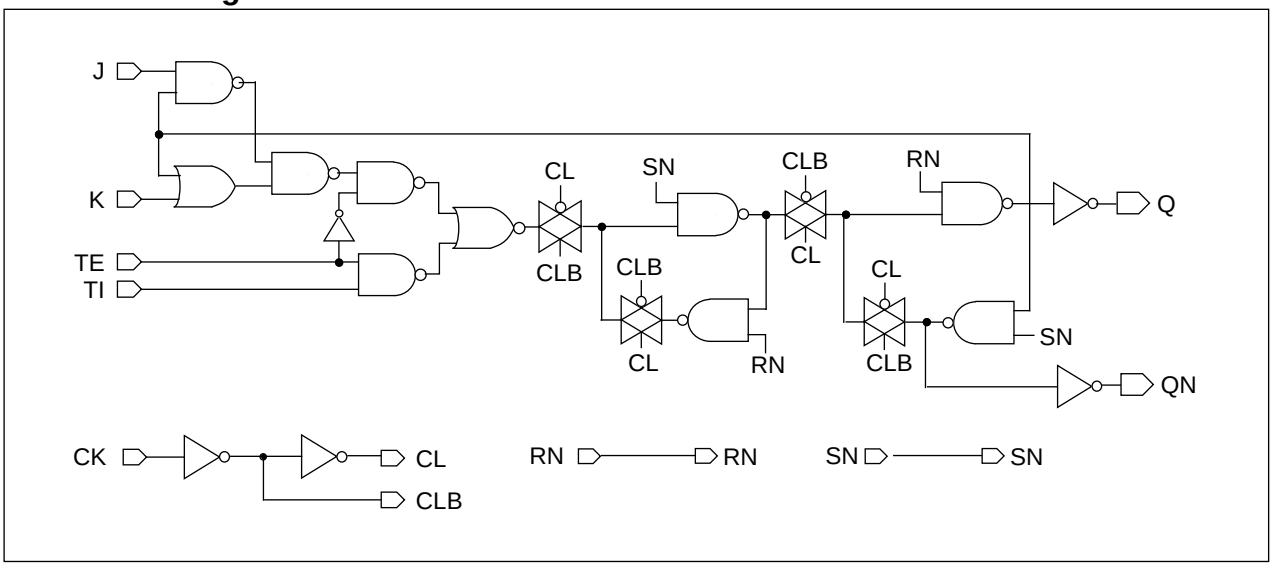
Truth Table

J	CK	K	TI	TE	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	1	0	1
1	↑	0	x	0	1	1	1	0
0	↑	0	x	0	1	1	Q (n)	QN (n)
1	↑	1	x	0	1	1	QN (n)	Q (n)
x	↓	x	x	0	1	1	Q (n)	QN (n)
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0
x	↑	x	0	1	1	1	0	1
x	↑	x	1	1	1	1	1	0

Cell Data

Input Load (SL)														Gate Count	
KG80															
FJ4S							*FJ4SD2*							*FJ4S*	*FJ4S D2*
J	CK	K	TI	TE	RN	SN	J	CK	K	TI	TE	RN	SN		
0.9	0.9	0.7	0.7	1.6	1.7	1.7	0.9	0.9	0.7	0.7	1.6	1.7	1.7	13.0	14.0
KGM80															
FJ4S							*FJ4SD2*							*FJ4S*	*FJ4S D2*
J	CK	K	TI	TE	RN	SN	J	CK	K	TI	TE	RN	SN		
1.0	1.0	1.0	0.9	1.9	2.2	2.2	1.0	1.0	1.0	0.9	1.9	2.2	2.2	13.0	14.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FJ4S	FJ4SD2	FJ4S	FJ4SD2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	1.02	1.02
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width High (RN)	t_{PWH}	0.61	0.61	1.02	1.02
Pulse Width High (SN)	t_{PWH}	0.64	0.64	1.05	1.05
Input Setup Time (J to CK)	t_{SU}	0.69	0.69	1.21	1.21
Input Hold Time (J to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.69	0.69	1.21	1.21
Input Hold Time (K to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.58	0.58	1.05	1.05
Input Hold Time (TI to CK)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.50	0.50	0.93	1.05
Input Hold Time (TE to CK)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.42	0.42	0.85	0.85
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FJ4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.59 + 0.048*SL	0.60 + 0.043*SL	0.62 + 0.042*SL
	t_{PHL}	0.67	0.59 + 0.038*SL	0.61 + 0.029*SL	0.64 + 0.025*SL
	t_R	0.32	0.15 + 0.086*SL	0.15 + 0.087*SL	0.13 + 0.088*SL
	t_F	0.22	0.14 + 0.043*SL	0.15 + 0.040*SL	0.15 + 0.040*SL
RN to Q	t_{PLH}	0.41	0.31 + 0.047*SL	0.32 + 0.042*SL	0.33 + 0.041*SL
	t_{PHL}	0.43	0.35 + 0.040*SL	0.37 + 0.030*SL	0.41 + 0.025*SL
	t_R	0.31	0.14 + 0.085*SL	0.14 + 0.086*SL	0.12 + 0.089*SL
	t_F	0.24	0.15 + 0.044*SL	0.17 + 0.038*SL	0.16 + 0.038*SL
SN to Q	t_{PLH}	0.78	0.69 + 0.046*SL	0.70 + 0.042*SL	0.70 + 0.041*SL
	t_R	0.32	0.15 + 0.085*SL	0.14 + 0.086*SL	0.12 + 0.089*SL
CK to QN	t_{PLH}	0.87	0.79 + 0.042*SL	0.79 + 0.041*SL	0.79 + 0.041*SL
	t_{PHL}	0.77	0.71 + 0.030*SL	0.72 + 0.025*SL	0.73 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.10 + 0.038*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to QN	t_{PLH}	0.63	0.55 + 0.042*SL	0.55 + 0.041*SL	0.55 + 0.041*SL
	t_R	0.28	0.11 + 0.084*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
SN to QN	t_{PLH}	0.29	0.21 + 0.043*SL	0.21 + 0.041*SL	0.21 + 0.042*SL
	t_{PHL}	0.33	0.26 + 0.032*SL	0.28 + 0.026*SL	0.29 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.039*SL	0.10 + 0.040*SL	0.09 + 0.041*SL

KG80 FJ4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.63 + 0.026*SL	0.64 + 0.023*SL	0.65 + 0.022*SL
	t_{PHL}	0.67	0.62 + 0.023*SL	0.63 + 0.018*SL	0.65 + 0.015*SL
	t_R	0.25	0.16 + 0.043*SL	0.16 + 0.043*SL	0.16 + 0.043*SL
	t_F	0.20	0.15 + 0.023*SL	0.16 + 0.021*SL	0.16 + 0.020*SL
RN to Q	t_{PLH}	0.40	0.35 + 0.026*SL	0.35 + 0.023*SL	0.36 + 0.021*SL
	t_{PHL}	0.42	0.37 + 0.025*SL	0.39 + 0.018*SL	0.41 + 0.015*SL
	t_R	0.24	0.16 + 0.042*SL	0.16 + 0.042*SL	0.15 + 0.043*SL
	t_F	0.21	0.17 + 0.024*SL	0.18 + 0.020*SL	0.18 + 0.019*SL
SN to Q	t_{PLH}	0.78	0.72 + 0.026*SL	0.73 + 0.023*SL	0.74 + 0.021*SL
	t_R	0.24	0.16 + 0.043*SL	0.16 + 0.042*SL	0.16 + 0.043*SL
CK to QN	t_{PLH}	0.91	0.87 + 0.022*SL	0.87 + 0.020*SL	0.87 + 0.020*SL
	t_{PHL}	0.81	0.77 + 0.019*SL	0.78 + 0.015*SL	0.79 + 0.013*SL
	t_R	0.19	0.11 + 0.042*SL	0.11 + 0.042*SL	0.10 + 0.043*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.019*SL
RN to QN	t_{PLH}	0.67	0.63 + 0.023*SL	0.63 + 0.020*SL	0.63 + 0.020*SL
	t_R	0.19	0.11 + 0.042*SL	0.11 + 0.042*SL	0.09 + 0.044*SL
SN to QN	t_{PLH}	0.28	0.23 + 0.024*SL	0.24 + 0.022*SL	0.24 + 0.021*SL
	t_{PHL}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_R	0.18	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FJ4S

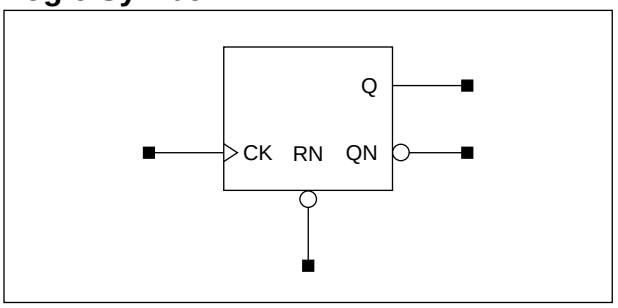
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.95	0.83 + 0.059*SL	0.85 + 0.052*SL	0.88 + 0.050*SL
	t_{PHL}	0.95	0.86 + 0.043*SL	0.90 + 0.031*SL	0.96 + 0.025*SL
	t_R	0.41	0.20 + 0.107*SL	0.20 + 0.105*SL	0.18 + 0.107*SL
	t_F	0.27	0.17 + 0.047*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
RN to Q	t_{PLH}	0.54	0.43 + 0.058*SL	0.45 + 0.051*SL	0.46 + 0.050*SL
	t_{PHL}	0.57	0.48 + 0.046*SL	0.52 + 0.031*SL	0.59 + 0.025*SL
	t_R	0.40	0.20 + 0.103*SL	0.19 + 0.105*SL	0.16 + 0.107*SL
	t_F	0.28	0.19 + 0.049*SL	0.21 + 0.040*SL	0.22 + 0.040*SL
SN to Q	t_{PLH}	1.09	0.97 + 0.059*SL	0.99 + 0.051*SL	1.01 + 0.050*SL
	t_R	0.41	0.20 + 0.104*SL	0.20 + 0.105*SL	0.17 + 0.107*SL
CK to QN	t_{PLH}	1.24	1.14 + 0.052*SL	1.14 + 0.050*SL	1.14 + 0.050*SL
	t_{PHL}	1.08	1.01 + 0.034*SL	1.04 + 0.026*SL	1.06 + 0.023*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to QN	t_{PLH}	0.87	0.77 + 0.052*SL	0.77 + 0.050*SL	0.77 + 0.050*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.106*SL	0.13 + 0.109*SL
SN to QN	t_{PLH}	0.40	0.29 + 0.054*SL	0.30 + 0.050*SL	0.31 + 0.050*SL
	t_{PHL}	0.43	0.36 + 0.035*SL	0.38 + 0.026*SL	0.41 + 0.024*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL

KGM80 FJ4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.94	0.88 + 0.033*SL	0.89 + 0.028*SL	0.91 + 0.026*SL
	t_{PHL}	0.95	0.90 + 0.027*SL	0.92 + 0.019*SL	0.97 + 0.015*SL
	t_R	0.32	0.21 + 0.055*SL	0.21 + 0.053*SL	0.22 + 0.052*SL
	t_F	0.24	0.19 + 0.027*SL	0.20 + 0.022*SL	0.22 + 0.021*SL
RN to Q	t_{PLH}	0.53	0.47 + 0.032*SL	0.48 + 0.028*SL	0.51 + 0.025*SL
	t_{PHL}	0.57	0.52 + 0.028*SL	0.54 + 0.020*SL	0.60 + 0.015*SL
	t_R	0.31	0.20 + 0.054*SL	0.21 + 0.052*SL	0.20 + 0.052*SL
	t_F	0.26	0.20 + 0.029*SL	0.22 + 0.022*SL	0.25 + 0.019*SL
SN to Q	t_{PLH}	1.08	1.02 + 0.032*SL	1.03 + 0.027*SL	1.06 + 0.025*SL
	t_R	0.32	0.21 + 0.055*SL	0.22 + 0.051*SL	0.21 + 0.052*SL
CK to QN	t_{PLH}	1.30	1.24 + 0.029*SL	1.25 + 0.025*SL	1.26 + 0.025*SL
	t_{PHL}	1.15	1.10 + 0.023*SL	1.12 + 0.016*SL	1.15 + 0.013*SL
	t_R	0.25	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
RN to QN	t_{PLH}	0.93	0.87 + 0.028*SL	0.88 + 0.025*SL	0.88 + 0.025*SL
	t_R	0.25	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
SN to QN	t_{PLH}	0.38	0.32 + 0.032*SL	0.33 + 0.026*SL	0.34 + 0.025*SL
	t_{PHL}	0.43	0.38 + 0.025*SL	0.40 + 0.017*SL	0.44 + 0.013*SL
	t_R	0.24	0.13 + 0.053*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



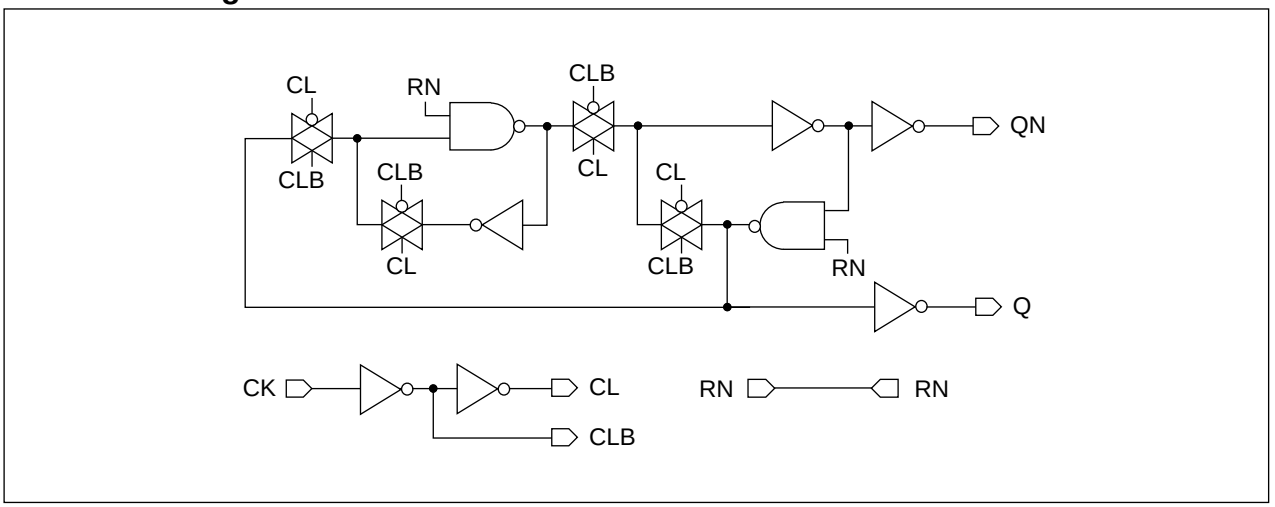
Truth Table

CK	RN	Q (n+1)	QN (n+1)
⎍	1	QN (n)	Q (n)
x	0	0	1

Cell Data

Input Load (SL)				Gate Count	
KG80					
FT2		*FT2D2*		*FT2*	*FT2D2*
CK	RN	CK	RN		
0.9	1.7	0.9	1.7	7.0	8.0
KGM80					
FT2		*FT2D2*		*FT2*	*FT2D2*
CK	RN	CK	RN		
1.0	2.2	1.0	2.1	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FT2	FT2D2	FT2	FT2D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width High (RN)	t_{PWH}	0.61	0.61	0.99	0.99
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.15	0.15	0.41	0.41

FT2/FT2D2

Toggle Flip-Flop with Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FT2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.81	0.73 + 0.043*SL	0.73 + 0.041*SL	0.73 + 0.041*SL
	t_{PHL}	0.64	0.58 + 0.033*SL	0.59 + 0.026*SL	0.61 + 0.024*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.089*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.040*SL	0.10 + 0.041*SL
RN to Q	t_{PHL}	0.37	0.30 + 0.035*SL	0.32 + 0.027*SL	0.34 + 0.024*SL
	t_F	0.20	0.12 + 0.040*SL	0.12 + 0.038*SL	0.11 + 0.040*SL
CK to QN	t_{PLH}	0.52	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.56	0.50 + 0.031*SL	0.52 + 0.026*SL	0.53 + 0.024*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
RN to QN	t_{PLH}	0.59	0.51 + 0.042*SL	0.51 + 0.041*SL	0.51 + 0.042*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL

KG80 FT2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.85	0.80 + 0.024*SL	0.81 + 0.021*SL	0.82 + 0.020*SL
	t_{PHL}	0.67	0.63 + 0.021*SL	0.64 + 0.016*SL	0.66 + 0.014*SL
	t_R	0.20	0.11 + 0.042*SL	0.11 + 0.042*SL	0.11 + 0.043*SL
	t_F	0.15	0.11 + 0.024*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
RN to Q	t_{PHL}	0.36	0.31 + 0.023*SL	0.33 + 0.017*SL	0.35 + 0.014*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.019*SL	0.14 + 0.018*SL
CK to QN	t_{PLH}	0.49	0.45 + 0.023*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.021*SL	0.53 + 0.015*SL	0.55 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.11 + 0.020*SL	0.10 + 0.020*SL
RN to QN	t_{PLH}	0.58	0.53 + 0.023*SL	0.54 + 0.021*SL	0.54 + 0.021*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.08 + 0.044*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FT2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.15	1.04 + 0.054*SL	1.05 + 0.050*SL	1.05 + 0.050*SL
	t_{PHL}	0.91	0.83 + 0.038*SL	0.86 + 0.028*SL	0.90 + 0.024*SL
	t_R	0.38	0.17 + 0.104*SL	0.16 + 0.106*SL	0.14 + 0.108*SL
	t_F	0.22	0.13 + 0.046*SL	0.14 + 0.042*SL	0.14 + 0.042*SL
RN to Q	t_{PHL}	0.49	0.42 + 0.040*SL	0.45 + 0.028*SL	0.50 + 0.024*SL
	t_F	0.24	0.14 + 0.046*SL	0.16 + 0.040*SL	0.15 + 0.041*SL
CK to QN	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.79	0.72 + 0.035*SL	0.74 + 0.026*SL	0.77 + 0.024*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.042*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
RN to QN	t_{PLH}	0.83	0.72 + 0.050*SL	0.73 + 0.050*SL	0.73 + 0.050*SL
	t_R	0.35	0.15 + 0.103*SL	0.14 + 0.108*SL	0.12 + 0.109*SL

KGM80 FT2D2

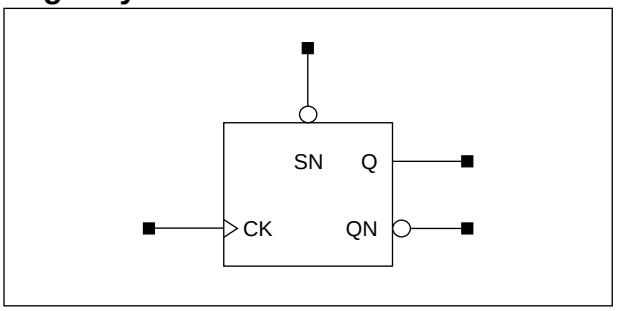
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.20	1.14 + 0.031*SL	1.16 + 0.026*SL	1.17 + 0.025*SL
	t_{PHL}	0.95	0.90 + 0.025*SL	0.92 + 0.017*SL	0.96 + 0.014*SL
	t_R	0.25	0.15 + 0.054*SL	0.15 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.13 + 0.028*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
RN to Q	t_{PHL}	0.49	0.43 + 0.028*SL	0.46 + 0.018*SL	0.51 + 0.014*SL
	t_F	0.20	0.15 + 0.027*SL	0.16 + 0.021*SL	0.18 + 0.019*SL
CK to QN	t_{PLH}	0.68	0.62 + 0.028*SL	0.63 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.80	0.75 + 0.024*SL	0.77 + 0.017*SL	0.80 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
RN to QN	t_{PLH}	0.81	0.75 + 0.029*SL	0.76 + 0.025*SL	0.76 + 0.025*SL
	t_R	0.22	0.12 + 0.050*SL	0.12 + 0.052*SL	0.10 + 0.054*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

FT3/FT3D2

Toggle Flip-Flop with Set, 1X/2X Drive

Logic Symbol



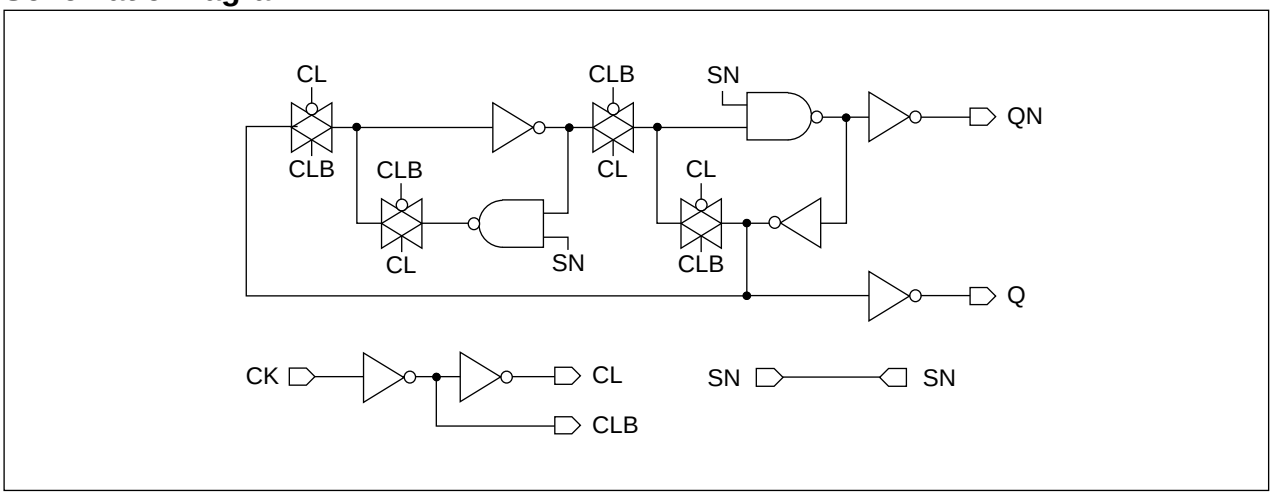
Truth Table

CK	SN	Q (n+1)	QN (n+1)
⎍	1	QN (n)	Q (n)
x	0	1	0

Cell Data

Input Load (SL)				Gate Count	
KG80					
FT3		*FT3D2*		*FT3*	*FT3D2*
CK	SN	CK	SN		
0.9	1.3	0.9	1.3	7.0	8.0
KGM80					
FT3		*FT3D2*		*FT3*	*FT3D2*
CK	SN	CK	SN		
1.0	1.9	1.0	1.9	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		FT3	FT3D2	FT3	FT3D2
Pulse Width Low (CK)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (CK)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width High (SN)	t_{PWH}	0.61	0.61	0.99	0.99
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.41	0.41	0.85	0.85

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FT3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.74	0.66 + 0.040*SL	0.66 + 0.041*SL	0.66 + 0.042*SL
	t_{PHL}	0.68	0.62 + 0.031*SL	0.63 + 0.026*SL	0.65 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.10 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.19	0.10 + 0.041*SL	0.11 + 0.040*SL	0.10 + 0.041*SL
SN to Q	t_{PLH}	0.48	0.40 + 0.040*SL	0.40 + 0.041*SL	0.39 + 0.042*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
CK to QN	t_{PLH}	0.56	0.47 + 0.044*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.57	0.50 + 0.033*SL	0.52 + 0.026*SL	0.53 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.11 + 0.039*SL	0.09 + 0.041*SL
SN to QN	t_{PHL}	0.31	0.24 + 0.032*SL	0.26 + 0.026*SL	0.27 + 0.024*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL

KG80 FT3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.77	0.73 + 0.020*SL	0.73 + 0.019*SL	0.73 + 0.020*SL
	t_{PHL}	0.72	0.69 + 0.019*SL	0.69 + 0.015*SL	0.71 + 0.013*SL
	t_R	0.18	0.09 + 0.041*SL	0.09 + 0.042*SL	0.08 + 0.044*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.019*SL	0.12 + 0.020*SL
SN to Q	t_{PLH}	0.51	0.47 + 0.020*SL	0.47 + 0.019*SL	0.46 + 0.020*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.042*SL	0.08 + 0.044*SL
CK to QN	t_{PLH}	0.55	0.50 + 0.025*SL	0.51 + 0.022*SL	0.51 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.022*SL	0.53 + 0.016*SL	0.55 + 0.014*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.15	0.11 + 0.022*SL	0.11 + 0.020*SL	0.12 + 0.020*SL
SN to QN	t_{PHL}	0.30	0.26 + 0.021*SL	0.27 + 0.016*SL	0.29 + 0.013*SL
	t_F	0.15	0.10 + 0.022*SL	0.11 + 0.020*SL	0.11 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

FT3/FT3D2

Toggle Flip-Flop with Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FT3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.05	0.95 + 0.049*SL	0.95 + 0.049*SL	0.95 + 0.050*SL
	t_{PHL}	0.97	0.89 + 0.036*SL	0.92 + 0.027*SL	0.95 + 0.024*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.22	0.14 + 0.044*SL	0.14 + 0.041*SL	0.14 + 0.042*SL
SN to Q	t_{PLH}	0.64	0.55 + 0.049*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
CK to QN	t_{PLH}	0.77	0.67 + 0.054*SL	0.68 + 0.051*SL	0.69 + 0.050*SL
	t_{PHL}	0.80	0.72 + 0.036*SL	0.75 + 0.027*SL	0.79 + 0.024*SL
	t_R	0.36	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
SN to QN	t_{PHL}	0.39	0.32 + 0.035*SL	0.35 + 0.027*SL	0.37 + 0.024*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.042*SL	0.12 + 0.042*SL

KGM80 FT3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.09	1.04 + 0.026*SL	1.04 + 0.024*SL	1.04 + 0.025*SL
	t_{PHL}	1.03	0.98 + 0.023*SL	1.00 + 0.017*SL	1.03 + 0.014*SL
	t_R	0.23	0.12 + 0.051*SL	0.12 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.19	0.13 + 0.027*SL	0.15 + 0.022*SL	0.16 + 0.021*SL
SN to Q	t_{PLH}	0.68	0.63 + 0.025*SL	0.64 + 0.024*SL	0.63 + 0.025*SL
	t_R	0.23	0.12 + 0.052*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
CK to QN	t_{PLH}	0.76	0.69 + 0.032*SL	0.71 + 0.027*SL	0.72 + 0.025*SL
	t_{PHL}	0.80	0.75 + 0.025*SL	0.77 + 0.017*SL	0.81 + 0.014*SL
	t_R	0.24	0.14 + 0.054*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
SN to QN	t_{PHL}	0.40	0.35 + 0.023*SL	0.37 + 0.017*SL	0.40 + 0.013*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

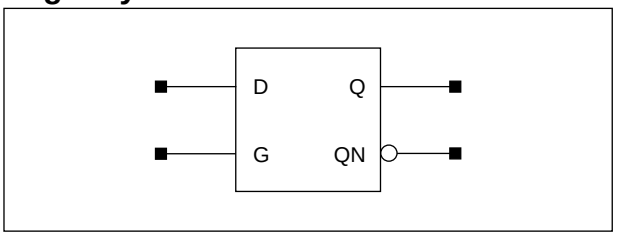
Cell List

Cell Name	Function Description
LD1	D Latch with Active High
LD1D2	D Latch with Active High, 2X Drive
LD1S	D Latch with Active High, Scan
LD1SD2	D Latch with Active High, Scan, 2X Drive
LD1Q	D Latch with Active High, Q Output Only
LD1QD2	D Latch with Active High, Q Output Only, 2X Drive
LD1X4	4-Bit D Latch with Active High
LD1X4D2	4-Bit D Latch with Active High, 2X Drive
YLD1	Fast D Latch with Active High
YLD1D2	Fast D Latch with Active High, 2X Drive
LD1A	D Latch with Active High, Tri-State Output
LD1B	D Latch with Active High, Tri-State Output, Separate WR, WRN
LD2	D Latch with Active High, Reset
LD2D2	D Latch with Active High, Reset, 2X Drive
LD2Q	D Latch with Active High, Reset, Q Output Only
LD2QD2	D Latch with Active High, Reset, Q Output Only, 2X Drive
YLD2	Fast D Latch with Active High, Reset
YLD2D2	Fast D Latch with Active High, Reset, 2X Drive
LD3	D Latch with Active High, Set
LD3D2	D Latch with Active High, Set, 2X Drive
LD4	D Latch with Active High, Reset, Set
LD4D2	D Latch with Active High, Reset, Set, 2X Drive
LD5	D Latch with Active Low
LD5D2	D Latch with Active Low, 2X Drive
LD5S	D Latch with Active Low, Scan
LD5SD2	D Latch with Active Low, Scan, 2X Drive
LD5X4	4-Bit D Latch with Active Low
LD5X4D2	4-Bit D Latch with Active Low, 2X Drive
LD6	D Latch with Active Low, Reset
LD6D2	D Latch with Active Low, Reset, 2X Drive
LD7	D Latch with Active Low, Set
LD7D2	D Latch with Active Low, Set, 2X Drive
LD8	D Latch with Active Low, Reset, Set
LD8D2	D Latch with Active Low, Reset, Set, 2X Drive

Cell List (Continued)

Cell Name	Function Description
LDS2	D Latch with Active High, Synchronous Clear
LDS6	D Latch with Active Low, Synchronous Clear
LS0	SR Latch
LS0D2	SR Latch with 2X Drive
LS1	SR Latch with Separate Inputs
LS2	SR Latch with Common Inputs

Logic Symbol



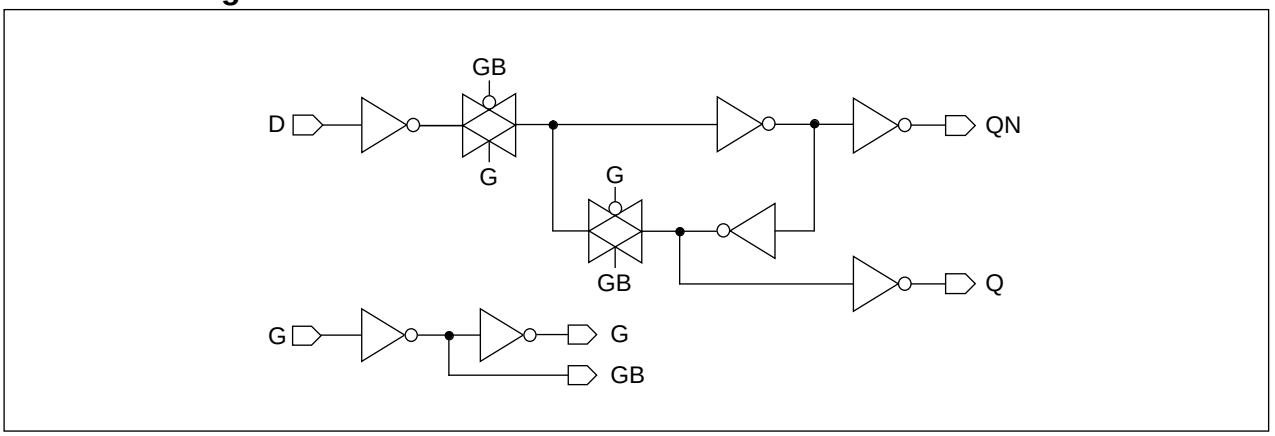
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
LD1		*LD1D2*		*LD1*	*LD1D2*
D	G	D	G		
0.9	0.9	0.9	0.9	4.0	5.0
KGM80					
LD1		*LD1D2*		*LD1*	*LD1D2*
D	G	D	G		
1.0	1.0	1.0	1.0	4.0	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD1	LD1D2	LD1	LD1D2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.34	0.37	0.61	0.64
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33

LD1/LD1D2

D Latch with Active High, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.53	0.45 + 0.040*SL	0.45 + 0.041*SL	0.45 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.030*SL	0.54 + 0.025*SL	0.55 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
G to Q	t_{PLH}	0.61	0.53 + 0.040*SL	0.52 + 0.041*SL	0.52 + 0.042*SL
	t_{PHL}	0.55	0.49 + 0.029*SL	0.50 + 0.025*SL	0.51 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.40	0.33 + 0.031*SL	0.35 + 0.025*SL	0.36 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.09 + 0.042*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
G to QN	t_{PLH}	0.47	0.39 + 0.042*SL	0.39 + 0.042*SL	0.39 + 0.042*SL
	t_{PHL}	0.47	0.41 + 0.030*SL	0.42 + 0.026*SL	0.44 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL

KG80 LD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.52 + 0.019*SL	0.52 + 0.019*SL	0.51 + 0.021*SL
	t_{PHL}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.61 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.045*SL
	t_F	0.13	0.09 + 0.021*SL	0.10 + 0.020*SL	0.09 + 0.020*SL
G to Q	t_{PLH}	0.64	0.60 + 0.019*SL	0.60 + 0.019*SL	0.59 + 0.020*SL
	t_{PHL}	0.59	0.55 + 0.018*SL	0.56 + 0.015*SL	0.57 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.09 + 0.020*SL	0.10 + 0.020*SL
D to QN	t_{PLH}	0.49	0.45 + 0.023*SL	0.45 + 0.021*SL	0.45 + 0.021*SL
	t_{PHL}	0.39	0.35 + 0.021*SL	0.36 + 0.015*SL	0.38 + 0.014*SL
	t_R	0.17	0.08 + 0.043*SL	0.09 + 0.042*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.023*SL	0.10 + 0.021*SL	0.11 + 0.019*SL
G to QN	t_{PLH}	0.45	0.41 + 0.023*SL	0.41 + 0.021*SL	0.41 + 0.021*SL
	t_{PHL}	0.47	0.43 + 0.021*SL	0.44 + 0.015*SL	0.46 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.73	0.64 + 0.049*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_{PHL}	0.82	0.76 + 0.032*SL	0.78 + 0.026*SL	0.80 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.044*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
G to Q	t_{PLH}	0.86	0.76 + 0.049*SL	0.76 + 0.050*SL	0.76 + 0.050*SL
	t_{PHL}	0.79	0.72 + 0.033*SL	0.74 + 0.025*SL	0.76 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.044*SL	0.11 + 0.041*SL	0.10 + 0.043*SL
D to QN	t_{PLH}	0.70	0.60 + 0.051*SL	0.60 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.54	0.47 + 0.034*SL	0.50 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
G to QN	t_{PLH}	0.67	0.56 + 0.051*SL	0.57 + 0.050*SL	0.57 + 0.050*SL
	t_{PHL}	0.66	0.59 + 0.034*SL	0.62 + 0.026*SL	0.65 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.11 + 0.042*SL

KGM80 LD1D2

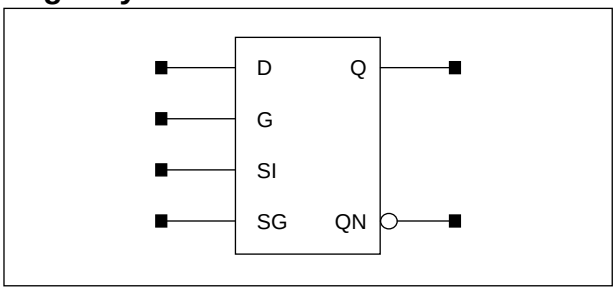
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.78	0.73 + 0.025*SL	0.73 + 0.024*SL	0.73 + 0.025*SL
	t_{PHL}	0.88	0.84 + 0.021*SL	0.85 + 0.016*SL	0.88 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
G to Q	t_{PLH}	0.90	0.85 + 0.024*SL	0.86 + 0.024*SL	0.85 + 0.025*SL
	t_{PHL}	0.84	0.80 + 0.021*SL	0.82 + 0.016*SL	0.85 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
D to QN	t_{PLH}	0.68	0.62 + 0.028*SL	0.63 + 0.025*SL	0.63 + 0.025*SL
	t_{PHL}	0.55	0.50 + 0.023*SL	0.52 + 0.016*SL	0.55 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.12 + 0.024*SL	0.12 + 0.022*SL	0.13 + 0.021*SL
G to QN	t_{PLH}	0.64	0.58 + 0.028*SL	0.59 + 0.025*SL	0.59 + 0.025*SL
	t_{PHL}	0.67	0.62 + 0.023*SL	0.64 + 0.016*SL	0.67 + 0.013*SL
	t_R	0.22	0.11 + 0.051*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

LD1S/LD1SD2

D Latch with Active High, Scan, 1X/2X Drive

Logic Symbol



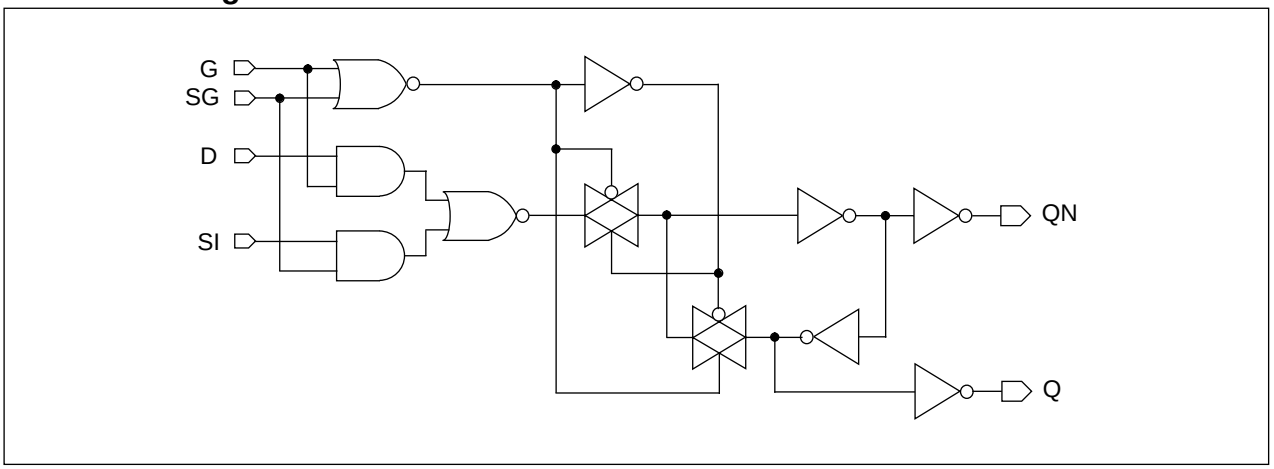
Truth Table

D	G	SI	SG	Q (n+1)	QN (n+1)
x	0	x	0	Q (n)	QN (n)
x	x	1	1	1	0
x	0	0	1	0	1
1	1	x	x	1	0
0	1	x	0	0	1
0	1	0	1	0	1

Cell Data

Input Load (SL)								Gate Count	
KG80									
LD1S				*LD1SD2*				*LD1S*	*LD1SD2*
D	G	SI	SG	D	G	SI	SG		
0.9	1.7	0.9	1.8	0.9	1.7	0.9	1.8	7.0	8.0
KGM80									
LD1S				*LD1SD2*				*LD1S*	*LD1SD2*
D	G	SI	SG	D	G	SI	SG		
1.0	1.0	2.0	2.1	1.0	1.0	2.0	2.1	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD1S	LD1SD2	LD1S	LD1SD2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width High (SG)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.37	0.42	0.74	0.80
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (SI to SG)	t_{SU}	0.37	0.39	0.68	0.74
Input Hold Time (SI to SG)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.63	0.55 + 0.040*SL	0.54 + 0.041*SL	0.54 + 0.042*SL
	t_{PHL}	0.67	0.61 + 0.029*SL	0.62 + 0.025*SL	0.63 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
SI to Q	t_{PLH}	0.70	0.62 + 0.040*SL	0.62 + 0.041*SL	0.61 + 0.042*SL
	t_{PHL}	0.71	0.65 + 0.030*SL	0.66 + 0.025*SL	0.68 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.039*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
G to Q	t_{PLH}	0.66	0.58 + 0.040*SL	0.57 + 0.041*SL	0.57 + 0.042*SL
	t_{PHL}	0.55	0.49 + 0.029*SL	0.50 + 0.025*SL	0.52 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
SG to Q	t_{PLH}	0.71	0.63 + 0.040*SL	0.63 + 0.041*SL	0.63 + 0.042*SL
	t_{PHL}	0.57	0.51 + 0.030*SL	0.52 + 0.025*SL	0.53 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.59	0.50 + 0.042*SL	0.51 + 0.041*SL	0.50 + 0.042*SL
	t_{PHL}	0.49	0.43 + 0.031*SL	0.44 + 0.026*SL	0.46 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.10 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
SI to QN	t_{PLH}	0.64	0.55 + 0.042*SL	0.55 + 0.041*SL	0.55 + 0.042*SL
	t_{PHL}	0.57	0.50 + 0.031*SL	0.52 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
G to QN	t_{PLH}	0.48	0.39 + 0.042*SL	0.39 + 0.042*SL	0.39 + 0.042*SL
	t_{PHL}	0.52	0.46 + 0.031*SL	0.47 + 0.026*SL	0.49 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SG to QN	t_{PLH}	0.49	0.41 + 0.042*SL	0.41 + 0.042*SL	0.41 + 0.042*SL
	t_{PHL}	0.58	0.52 + 0.031*SL	0.53 + 0.026*SL	0.55 + 0.023*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.10 + 0.040*SL	0.10 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.66	0.62 + 0.019*SL	0.62 + 0.019*SL	0.61 + 0.020*SL
	t_{PHL}	0.71	0.67 + 0.018*SL	0.68 + 0.015*SL	0.69 + 0.013*SL
	t_R	0.17	0.09 + 0.037*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SI to Q	t_{PLH}	0.73	0.69 + 0.019*SL	0.69 + 0.019*SL	0.69 + 0.020*SL
	t_{PHL}	0.76	0.72 + 0.018*SL	0.73 + 0.014*SL	0.74 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
G to Q	t_{PLH}	0.69	0.65 + 0.019*SL	0.65 + 0.019*SL	0.64 + 0.020*SL
	t_{PHL}	0.59	0.55 + 0.018*SL	0.56 + 0.015*SL	0.58 + 0.013*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.020*SL	0.09 + 0.020*SL
SG to Q	t_{PLH}	0.75	0.71 + 0.019*SL	0.71 + 0.019*SL	0.70 + 0.020*SL
	t_{PHL}	0.61	0.57 + 0.019*SL	0.58 + 0.015*SL	0.59 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
D to QN	t_{PLH}	0.58	0.53 + 0.023*SL	0.54 + 0.021*SL	0.53 + 0.021*SL
	t_{PHL}	0.49	0.45 + 0.020*SL	0.46 + 0.016*SL	0.48 + 0.013*SL
	t_R	0.17	0.10 + 0.038*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.11 + 0.020*SL
SI to QN	t_{PLH}	0.62	0.58 + 0.023*SL	0.58 + 0.021*SL	0.58 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.021*SL	0.53 + 0.015*SL	0.55 + 0.014*SL
	t_R	0.18	0.10 + 0.038*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.15	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
G to QN	t_{PLH}	0.46	0.41 + 0.023*SL	0.42 + 0.021*SL	0.42 + 0.021*SL
	t_{PHL}	0.52	0.48 + 0.021*SL	0.49 + 0.015*SL	0.51 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
SG to QN	t_{PLH}	0.48	0.43 + 0.023*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.58	0.54 + 0.020*SL	0.55 + 0.015*SL	0.57 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.11 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.87	0.77 + 0.049*SL	0.77 + 0.050*SL	0.77 + 0.050*SL
	t_{PHL}	0.96	0.90 + 0.033*SL	0.92 + 0.026*SL	0.94 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
SI to Q	t_{PLH}	0.96	0.87 + 0.049*SL	0.86 + 0.050*SL	0.86 + 0.050*SL
	t_{PHL}	1.06	1.00 + 0.032*SL	1.02 + 0.026*SL	1.04 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
G to Q	t_{PLH}	0.93	0.83 + 0.049*SL	0.83 + 0.050*SL	0.83 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.033*SL	0.75 + 0.026*SL	0.77 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
SG to Q	t_{PLH}	0.99	0.90 + 0.049*SL	0.89 + 0.050*SL	0.89 + 0.050*SL
	t_{PHL}	0.81	0.74 + 0.032*SL	0.76 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D to QN	t_{PLH}	0.84	0.74 + 0.051*SL	0.75 + 0.050*SL	0.75 + 0.050*SL
	t_{PHL}	0.68	0.61 + 0.034*SL	0.63 + 0.026*SL	0.66 + 0.023*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
SI to QN	t_{PLH}	0.94	0.84 + 0.051*SL	0.84 + 0.050*SL	0.85 + 0.050*SL
	t_{PHL}	0.77	0.70 + 0.035*SL	0.72 + 0.026*SL	0.76 + 0.023*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
G to QN	t_{PLH}	0.68	0.57 + 0.051*SL	0.58 + 0.050*SL	0.58 + 0.050*SL
	t_{PHL}	0.73	0.66 + 0.035*SL	0.69 + 0.026*SL	0.72 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
SG to QN	t_{PLH}	0.69	0.59 + 0.051*SL	0.59 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.75 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

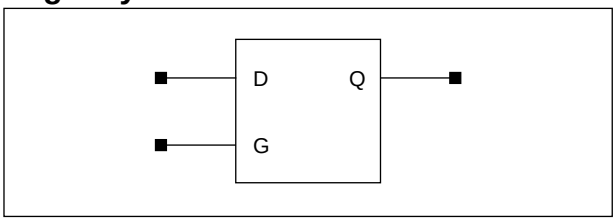
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.92	0.87 + 0.025*SL	0.87 + 0.024*SL	0.86 + 0.025*SL
	t_{PHL}	1.03	0.99 + 0.021*SL	1.00 + 0.016*SL	1.03 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
SI to Q	t_{PLH}	1.01	0.97 + 0.024*SL	0.97 + 0.024*SL	0.96 + 0.025*SL
	t_{PHL}	1.13	1.09 + 0.021*SL	1.11 + 0.016*SL	1.14 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
G to Q	t_{PLH}	0.98	0.93 + 0.024*SL	0.93 + 0.024*SL	0.92 + 0.025*SL
	t_{PHL}	0.86	0.81 + 0.021*SL	0.83 + 0.016*SL	0.86 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
SG to Q	t_{PLH}	1.05	1.00 + 0.024*SL	1.00 + 0.024*SL	0.99 + 0.025*SL
	t_{PHL}	0.87	0.83 + 0.021*SL	0.84 + 0.016*SL	0.87 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
D to QN	t_{PLH}	0.83	0.77 + 0.029*SL	0.78 + 0.025*SL	0.78 + 0.025*SL
	t_{PHL}	0.68	0.64 + 0.024*SL	0.65 + 0.017*SL	0.69 + 0.013*SL
	t_R	0.23	0.13 + 0.050*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
SI to QN	t_{PLH}	0.93	0.87 + 0.029*SL	0.88 + 0.025*SL	0.89 + 0.025*SL
	t_{PHL}	0.78	0.73 + 0.024*SL	0.75 + 0.017*SL	0.78 + 0.013*SL
	t_R	0.23	0.13 + 0.049*SL	0.12 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
G to QN	t_{PLH}	0.65	0.60 + 0.028*SL	0.60 + 0.025*SL	0.61 + 0.025*SL
	t_{PHL}	0.74	0.69 + 0.024*SL	0.71 + 0.017*SL	0.75 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
SG to QN	t_{PLH}	0.67	0.61 + 0.028*SL	0.62 + 0.025*SL	0.62 + 0.025*SL
	t_{PHL}	0.81	0.76 + 0.024*SL	0.78 + 0.017*SL	0.82 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.13 + 0.023*SL	0.13 + 0.021*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



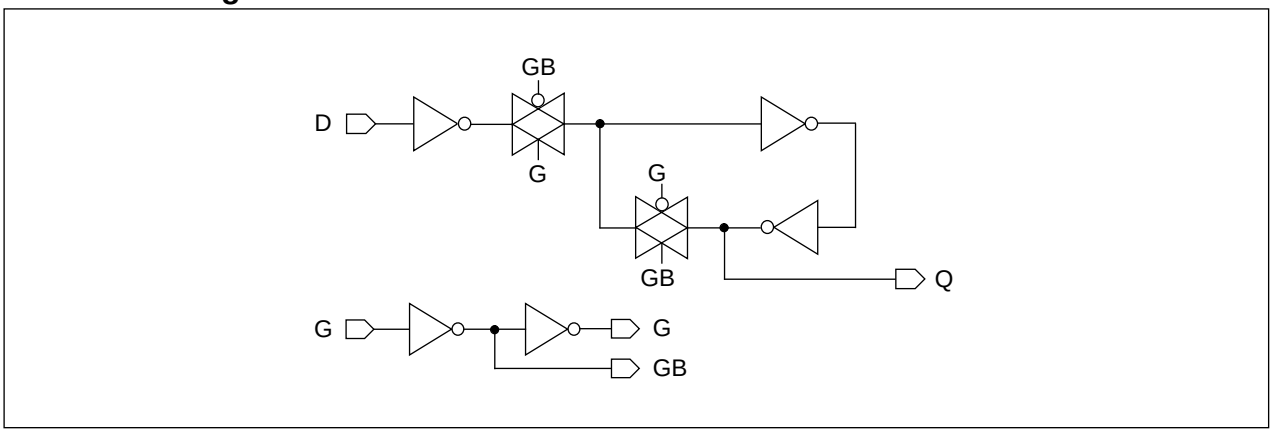
Truth Table

D	G	Q (n+1)
0	1	0
1	1	1
x	0	Q (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
LD1Q		*LD1QD2*		*LD1Q*	*LD1QD2*
D	G	D	G		
0.8	0.8	0.8	0.8	4.0	5.0
KGM80					
LD1Q		*LD1QD2*		*LD1Q*	*LD1QD2*
D	G	D	G		
0.9	0.9	0.9	0.9	4.0	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD1Q	LD1QD2	LD1Q	LD1QD2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.31	0.31	0.61	0.61
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33

LD1Q/LD1QD2

D Latch with Active High, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.49	0.40 + 0.042*SL	0.40 + 0.042*SL	0.40 + 0.042*SL
	t_{PHL}	0.54	0.48 + 0.029*SL	0.50 + 0.025*SL	0.50 + 0.023*SL
	t_R	0.26	0.08 + 0.087*SL	0.07 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.15	0.07 + 0.041*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
G to Q	t_{PLH}	0.54	0.45 + 0.042*SL	0.45 + 0.042*SL	0.45 + 0.042*SL
	t_{PHL}	0.49	0.43 + 0.029*SL	0.44 + 0.025*SL	0.45 + 0.023*SL
	t_R	0.26	0.08 + 0.087*SL	0.07 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.15	0.07 + 0.040*SL	0.07 + 0.041*SL	0.06 + 0.042*SL

KG80 LD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.47	0.42 + 0.023*SL	0.43 + 0.021*SL	0.43 + 0.021*SL
	t_{PHL}	0.54	0.51 + 0.018*SL	0.52 + 0.014*SL	0.53 + 0.012*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.046*SL
	t_F	0.13	0.09 + 0.020*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
G to Q	t_{PLH}	0.52	0.48 + 0.021*SL	0.48 + 0.021*SL	0.48 + 0.021*SL
	t_{PHL}	0.49	0.46 + 0.018*SL	0.46 + 0.014*SL	0.48 + 0.012*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.045*SL	0.08 + 0.046*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.09 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.67	0.57 + 0.051*SL	0.57 + 0.050*SL	0.57 + 0.050*SL
	t_{PHL}	0.76	0.70 + 0.032*SL	0.72 + 0.025*SL	0.74 + 0.023*SL
	t_R	0.33	0.12 + 0.106*SL	0.11 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.18	0.09 + 0.044*SL	0.10 + 0.042*SL	0.09 + 0.043*SL
G to Q	t_{PLH}	0.76	0.66 + 0.051*SL	0.66 + 0.050*SL	0.66 + 0.050*SL
	t_{PHL}	0.72	0.65 + 0.032*SL	0.67 + 0.025*SL	0.69 + 0.023*SL
	t_R	0.33	0.12 + 0.106*SL	0.11 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.18	0.10 + 0.043*SL	0.10 + 0.042*SL	0.09 + 0.043*SL

KGM80 LD1QD2

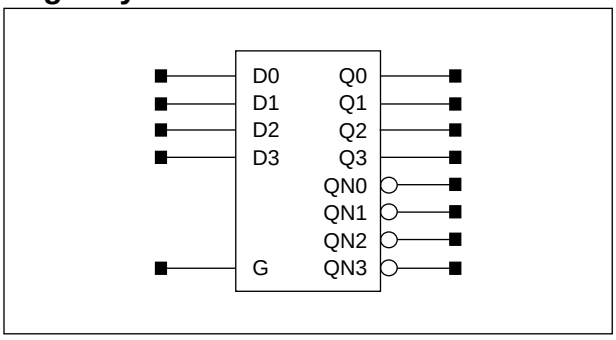
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.65	0.59 + 0.027*SL	0.60 + 0.025*SL	0.60 + 0.025*SL
	t_{PHL}	0.77	0.73 + 0.020*SL	0.75 + 0.015*SL	0.77 + 0.013*SL
	t_R	0.23	0.13 + 0.051*SL	0.12 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.021*SL	0.12 + 0.020*SL
G to Q	t_{PLH}	0.74	0.68 + 0.027*SL	0.69 + 0.025*SL	0.69 + 0.025*SL
	t_{PHL}	0.73	0.69 + 0.020*SL	0.70 + 0.015*SL	0.73 + 0.012*SL
	t_R	0.23	0.13 + 0.051*SL	0.12 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.16	0.11 + 0.023*SL	0.12 + 0.021*SL	0.12 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

LD1X4/LD1X4D2

4-Bit D Latch with Active High, 1X/2X Drive

Logic Symbol



Truth Table

Dn	G	Qn (n+1)	QNn (n+1)
0	1	0	1
1	1	1	0
x	0	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
LD1X4		*LD1X4D2*		*LD1X4*	*LD1X4D2*
Dn	G	Dn	G		
0.9	0.9	0.9	0.9	15.0	19.0
KGM80					
LD1X4		*LD1X4D2*		*LD1X4*	*LD1X4D2*
Dn	G	Dn	G		
1.0	1.1	1.0	1.1	15.0	19.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD1X4	LD1X4D2	LD1X4	LD1X4D2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D0 to G)	t_{SU}	0.26	0.28	0.52	0.55
Input Hold Time (D0 to G)	t_{HD}	0.26	0.20	0.46	0.46
Input Setup Time (D1 to G)	t_{SU}	0.26	0.28	0.52	0.55
Input Hold Time (D1 to G)	t_{HD}	0.26	0.20	0.46	0.46
Input Setup Time (D2 to G)	t_{SU}	0.26	0.28	0.52	0.55
Input Hold Time (D2 to G)	t_{HD}	0.26	0.20	0.46	0.46
Input Setup Time (D3 to G)	t_{SU}	0.26	0.28	0.52	0.55
Input Hold Time (D3 to G)	t_{HD}	0.26	0.20	0.46	0.46

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.54	0.46 + 0.040*SL	0.46 + 0.041*SL	0.45 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.56 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
G to Q0	t_{PLH}	0.78	0.70 + 0.041*SL	0.70 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.65	0.59 + 0.029*SL	0.60 + 0.025*SL	0.61 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D1 to Q1	t_{PLH}	0.55	0.46 + 0.041*SL	0.46 + 0.041*SL	0.46 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.57 + 0.023*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
G to Q1	t_{PLH}	0.79	0.71 + 0.040*SL	0.70 + 0.041*SL	0.70 + 0.042*SL
	t_{PHL}	0.66	0.60 + 0.030*SL	0.61 + 0.025*SL	0.62 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.08 + 0.040*SL	0.08 + 0.042*SL
D2 to Q2	t_{PLH}	0.54	0.46 + 0.040*SL	0.46 + 0.041*SL	0.46 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.56 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
G to Q2	t_{PLH}	0.78	0.70 + 0.040*SL	0.70 + 0.041*SL	0.70 + 0.042*SL
	t_{PHL}	0.65	0.60 + 0.030*SL	0.61 + 0.025*SL	0.62 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D3 to Q3	t_{PLH}	0.54	0.46 + 0.040*SL	0.46 + 0.041*SL	0.45 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.56 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
G to Q3	t_{PLH}	0.78	0.70 + 0.041*SL	0.70 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.65	0.59 + 0.029*SL	0.60 + 0.025*SL	0.61 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D0 to QN0	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.031*SL	0.36 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.039*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
G to QN0	t_{PLH}	0.57	0.49 + 0.041*SL	0.49 + 0.042*SL	0.49 + 0.042*SL
	t_{PHL}	0.65	0.59 + 0.030*SL	0.60 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.090*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.042*SL	0.44 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.031*SL	0.36 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.27	0.11 + 0.084*SL	0.09 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
G to QN1	t_{PLH}	0.57	0.49 + 0.042*SL	0.49 + 0.042*SL	0.49 + 0.042*SL
	t_{PHL}	0.65	0.59 + 0.030*SL	0.60 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
D2 to QN2	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.031*SL	0.36 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
G to QN2	t_{PLH}	0.58	0.49 + 0.042*SL	0.49 + 0.042*SL	0.49 + 0.042*SL
	t_{PHL}	0.65	0.59 + 0.030*SL	0.60 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.09 + 0.041*SL
D3 to QN3	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.031*SL	0.36 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.039*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
G to QN3	t_{PLH}	0.57	0.49 + 0.041*SL	0.49 + 0.042*SL	0.49 + 0.042*SL
	t_{PHL}	0.65	0.59 + 0.030*SL	0.60 + 0.026*SL	0.61 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.090*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.09 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.56	0.53 + 0.019*SL	0.53 + 0.019*SL	0.52 + 0.020*SL
	t_{PHL}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.61 + 0.013*SL
	t_R	0.16	0.09 + 0.039*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.020*SL	0.09 + 0.020*SL
G to Q0	t_{PLH}	0.81	0.77 + 0.019*SL	0.77 + 0.019*SL	0.76 + 0.020*SL
	t_{PHL}	0.68	0.65 + 0.018*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_R	0.16	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
D1 to Q1	t_{PLH}	0.57	0.53 + 0.020*SL	0.53 + 0.019*SL	0.53 + 0.020*SL
	t_{PHL}	0.64	0.60 + 0.019*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.17	0.09 + 0.039*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
G to Q1	t_{PLH}	0.82	0.78 + 0.019*SL	0.78 + 0.019*SL	0.77 + 0.020*SL
	t_{PHL}	0.69	0.65 + 0.019*SL	0.66 + 0.015*SL	0.67 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
D2 to Q2	t_{PLH}	0.58	0.54 + 0.019*SL	0.54 + 0.019*SL	0.54 + 0.020*SL
	t_{PHL}	0.65	0.61 + 0.017*SL	0.62 + 0.014*SL	0.63 + 0.013*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
G to Q2	t_{PLH}	0.83	0.79 + 0.018*SL	0.79 + 0.019*SL	0.78 + 0.020*SL
	t_{PHL}	0.70	0.66 + 0.018*SL	0.67 + 0.014*SL	0.68 + 0.013*SL
	t_R	0.19	0.11 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.10 + 0.022*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
D3 to Q3	t_{PLH}	0.56	0.53 + 0.020*SL	0.53 + 0.019*SL	0.52 + 0.020*SL
	t_{PHL}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.16	0.08 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
G to Q3	t_{PLH}	0.81	0.77 + 0.019*SL	0.77 + 0.019*SL	0.77 + 0.020*SL
	t_{PHL}	0.68	0.65 + 0.018*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
D0 to QN0	t_{PLH}	0.50	0.45 + 0.023*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.021*SL	0.37 + 0.015*SL	0.39 + 0.013*SL
	t_R	0.17	0.09 + 0.037*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
G to QN0	t_{PLH}	0.55	0.51 + 0.023*SL	0.51 + 0.021*SL	0.51 + 0.021*SL
	t_{PHL}	0.65	0.61 + 0.020*SL	0.62 + 0.015*SL	0.63 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.045*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.50	0.46 + 0.023*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.020*SL	0.37 + 0.015*SL	0.39 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
G to QN1	t_{PLH}	0.55	0.51 + 0.023*SL	0.51 + 0.021*SL	0.51 + 0.021*SL
	t_{PHL}	0.65	0.61 + 0.020*SL	0.62 + 0.015*SL	0.63 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
D2 to QN2	t_{PLH}	0.50	0.46 + 0.022*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.021*SL	0.37 + 0.015*SL	0.39 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
G to QN2	t_{PLH}	0.55	0.51 + 0.023*SL	0.51 + 0.021*SL	0.51 + 0.021*SL
	t_{PHL}	0.65	0.61 + 0.021*SL	0.62 + 0.015*SL	0.63 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
D3 to QN3	t_{PLH}	0.50	0.45 + 0.023*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.020*SL	0.37 + 0.015*SL	0.38 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
G to QN3	t_{PLH}	0.55	0.51 + 0.023*SL	0.51 + 0.021*SL	0.51 + 0.021*SL
	t_{PHL}	0.64	0.60 + 0.020*SL	0.62 + 0.015*SL	0.63 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.045*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.74	0.64 + 0.049*SL	0.64 + 0.050*SL	0.64 + 0.050*SL
	t_{PHL}	0.83	0.77 + 0.033*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
G to Q0	t_{PLH}	1.09	1.00 + 0.049*SL	0.99 + 0.050*SL	1.00 + 0.050*SL
	t_{PHL}	0.90	0.84 + 0.032*SL	0.85 + 0.026*SL	0.88 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D1 to Q1	t_{PLH}	0.75	0.66 + 0.049*SL	0.65 + 0.050*SL	0.65 + 0.050*SL
	t_{PHL}	0.84	0.78 + 0.032*SL	0.79 + 0.026*SL	0.82 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
G to Q1	t_{PLH}	1.11	1.01 + 0.049*SL	1.00 + 0.050*SL	1.01 + 0.050*SL
	t_{PHL}	0.91	0.85 + 0.032*SL	0.87 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
D2 to Q2	t_{PLH}	0.75	0.65 + 0.049*SL	0.65 + 0.050*SL	0.65 + 0.050*SL
	t_{PHL}	0.84	0.77 + 0.033*SL	0.79 + 0.026*SL	0.82 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
G to Q2	t_{PLH}	1.10	1.00 + 0.049*SL	1.00 + 0.050*SL	1.00 + 0.050*SL
	t_{PHL}	0.91	0.84 + 0.033*SL	0.86 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.042*SL	0.11 + 0.042*SL
D3 to Q3	t_{PLH}	0.74	0.64 + 0.049*SL	0.64 + 0.050*SL	0.64 + 0.050*SL
	t_{PHL}	0.83	0.76 + 0.033*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
G to Q3	t_{PLH}	1.09	1.00 + 0.049*SL	0.99 + 0.050*SL	1.00 + 0.050*SL
	t_{PHL}	0.90	0.84 + 0.033*SL	0.86 + 0.026*SL	0.88 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D0 to QN0	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.50 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
G to QN0	t_{PLH}	0.79	0.68 + 0.051*SL	0.69 + 0.050*SL	0.69 + 0.050*SL
	t_{PHL}	0.90	0.84 + 0.034*SL	0.86 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.50 + 0.026*SL	0.54 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
G to QN1	t_{PLH}	0.79	0.68 + 0.051*SL	0.69 + 0.050*SL	0.69 + 0.050*SL
	t_{PHL}	0.90	0.84 + 0.034*SL	0.86 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
D2 to QN2	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.51 + 0.026*SL	0.54 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
G to QN2	t_{PLH}	0.79	0.69 + 0.051*SL	0.69 + 0.050*SL	0.69 + 0.050*SL
	t_{PHL}	0.91	0.84 + 0.034*SL	0.86 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
D3 to QN3	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.50 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
G to QN3	t_{PLH}	0.79	0.68 + 0.051*SL	0.69 + 0.050*SL	0.69 + 0.050*SL
	t_{PHL}	0.90	0.84 + 0.034*SL	0.86 + 0.026*SL	0.89 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.78	0.74 + 0.025*SL	0.74 + 0.024*SL	0.73 + 0.025*SL
	t_{PHL}	0.89	0.84 + 0.021*SL	0.86 + 0.016*SL	0.89 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
G to Q0	t_{PLH}	1.14	1.09 + 0.025*SL	1.10 + 0.024*SL	1.09 + 0.025*SL
	t_{PHL}	0.96	0.91 + 0.021*SL	0.93 + 0.016*SL	0.96 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.026*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
D1 to Q1	t_{PLH}	0.80	0.75 + 0.025*SL	0.75 + 0.024*SL	0.74 + 0.025*SL
	t_{PHL}	0.90	0.85 + 0.021*SL	0.87 + 0.016*SL	0.90 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
G to Q1	t_{PLH}	1.15	1.10 + 0.025*SL	1.11 + 0.024*SL	1.10 + 0.025*SL
	t_{PHL}	0.97	0.92 + 0.021*SL	0.94 + 0.016*SL	0.97 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
D2 to Q2	t_{PLH}	0.81	0.76 + 0.023*SL	0.76 + 0.024*SL	0.75 + 0.025*SL
	t_{PHL}	0.91	0.87 + 0.019*SL	0.88 + 0.015*SL	0.91 + 0.013*SL
	t_R	0.25	0.15 + 0.051*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.14 + 0.021*SL
G to Q2	t_{PLH}	1.17	1.12 + 0.024*SL	1.12 + 0.024*SL	1.11 + 0.025*SL
	t_{PHL}	0.98	0.94 + 0.020*SL	0.95 + 0.015*SL	0.98 + 0.013*SL
	t_R	0.25	0.15 + 0.052*SL	0.15 + 0.052*SL	0.13 + 0.054*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
D3 to Q3	t_{PLH}	0.78	0.73 + 0.025*SL	0.74 + 0.024*SL	0.73 + 0.025*SL
	t_{PHL}	0.89	0.84 + 0.021*SL	0.86 + 0.016*SL	0.89 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
G to Q3	t_{PLH}	1.14	1.09 + 0.024*SL	1.10 + 0.024*SL	1.09 + 0.025*SL
	t_{PHL}	0.96	0.91 + 0.021*SL	0.93 + 0.016*SL	0.96 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.026*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
D0 to QN0	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.50 + 0.023*SL	0.52 + 0.017*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.12 + 0.022*SL	0.14 + 0.020*SL
G to QN0	t_{PLH}	0.76	0.70 + 0.028*SL	0.71 + 0.025*SL	0.71 + 0.025*SL
	t_{PHL}	0.91	0.86 + 0.023*SL	0.88 + 0.016*SL	0.92 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.14 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

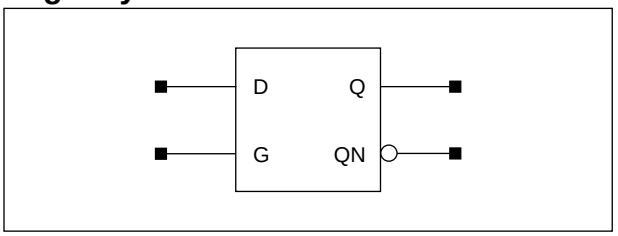
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.51 + 0.023*SL	0.53 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.049*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
G to QN1	t_{PLH}	0.76	0.70 + 0.028*SL	0.71 + 0.025*SL	0.71 + 0.025*SL
	t_{PHL}	0.91	0.87 + 0.023*SL	0.89 + 0.016*SL	0.92 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
D2 to QN2	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.51 + 0.023*SL	0.53 + 0.017*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
G to QN2	t_{PLH}	0.76	0.70 + 0.028*SL	0.71 + 0.025*SL	0.71 + 0.025*SL
	t_{PHL}	0.91	0.87 + 0.023*SL	0.89 + 0.016*SL	0.92 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
D3 to QN3	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.50 + 0.023*SL	0.52 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
G to QN3	t_{PLH}	0.76	0.70 + 0.027*SL	0.71 + 0.025*SL	0.71 + 0.025*SL
	t_{PHL}	0.91	0.86 + 0.023*SL	0.88 + 0.017*SL	0.92 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.14 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



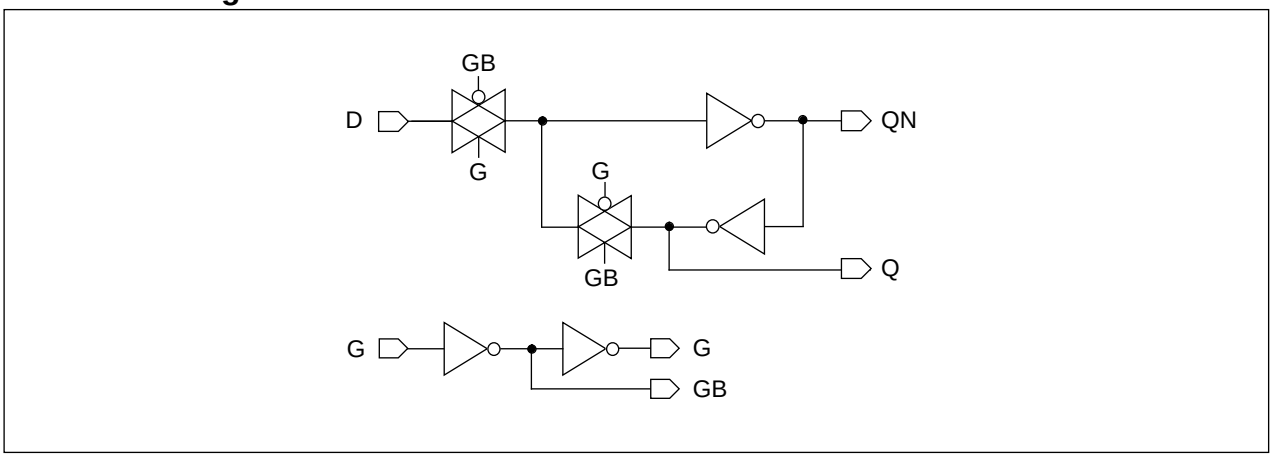
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
YLD1		*YLD1D2*		*YLD1*	*YLD1D2*
D	G	D	G		
2.9	0.8	3.7	0.8	4.0	5.0
KGM80					
YLD1		*YLD1D2*		*YLD1*	*YLD1D2*
D	G	D	G		
3.7	0.9	4.6	0.9	4.0	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		YLD1	YLD1D2	YLD1	YLD1D2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.17	0.15	0.39	0.39
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YLD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.36	0.18 + 0.086*SL	0.20 + 0.078*SL	0.22 + 0.076*SL
	t_{PHL}	0.40	0.25 + 0.076*SL	0.25 + 0.076*SL	0.25 + 0.076*SL
	t_R	0.32	0.14 + 0.090*SL	0.13 + 0.094*SL	0.13 + 0.094*SL
	t_F	0.21	0.09 + 0.061*SL	0.09 + 0.062*SL	0.08 + 0.063*SL
G to Q	t_{PLH}	0.49	0.33 + 0.080*SL	0.34 + 0.077*SL	0.34 + 0.076*SL
	t_{PHL}	0.50	0.34 + 0.077*SL	0.34 + 0.077*SL	0.34 + 0.077*SL
	t_R	0.32	0.13 + 0.094*SL	0.13 + 0.094*SL	0.13 + 0.095*SL
	t_F	0.21	0.08 + 0.064*SL	0.08 + 0.063*SL	0.08 + 0.063*SL
D to QN	t_{PLH}	0.28	0.20 + 0.041*SL	0.20 + 0.040*SL	0.19 + 0.041*SL
	t_{PHL}	0.16	0.09 + 0.036*SL	0.11 + 0.027*SL	0.14 + 0.023*SL
	t_R	0.37	0.21 + 0.080*SL	0.20 + 0.085*SL	0.18 + 0.089*SL
	t_F	0.26	0.19 + 0.037*SL	0.19 + 0.036*SL	0.17 + 0.038*SL
G to QN	t_{PLH}	0.37	0.29 + 0.042*SL	0.29 + 0.042*SL	0.29 + 0.042*SL
	t_{PHL}	0.31	0.25 + 0.028*SL	0.26 + 0.024*SL	0.27 + 0.023*SL
	t_R	0.34	0.16 + 0.087*SL	0.16 + 0.090*SL	0.15 + 0.091*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.09 + 0.042*SL

KG80 YLD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.27	0.18 + 0.047*SL	0.19 + 0.042*SL	0.20 + 0.039*SL
	t_{PHL}	0.33	0.25 + 0.040*SL	0.26 + 0.038*SL	0.25 + 0.038*SL
	t_R	0.21	0.12 + 0.044*SL	0.11 + 0.046*SL	0.11 + 0.048*SL
	t_F	0.14	0.08 + 0.030*SL	0.08 + 0.031*SL	0.07 + 0.031*SL
G to Q	t_{PLH}	0.42	0.34 + 0.042*SL	0.34 + 0.040*SL	0.35 + 0.039*SL
	t_{PHL}	0.43	0.35 + 0.039*SL	0.35 + 0.038*SL	0.35 + 0.038*SL
	t_R	0.20	0.10 + 0.047*SL	0.10 + 0.048*SL	0.10 + 0.048*SL
	t_F	0.13	0.07 + 0.031*SL	0.07 + 0.031*SL	0.06 + 0.032*SL
D to QN	t_{PLH}	0.25	0.21 + 0.022*SL	0.22 + 0.020*SL	0.21 + 0.020*SL
	t_{PHL}	0.14	0.10 + 0.020*SL	0.11 + 0.016*SL	0.13 + 0.013*SL
	t_R	0.29	0.21 + 0.040*SL	0.21 + 0.042*SL	0.20 + 0.044*SL
	t_F	0.23	0.19 + 0.018*SL	0.19 + 0.018*SL	0.19 + 0.019*SL
G to QN	t_{PLH}	0.35	0.31 + 0.021*SL	0.31 + 0.021*SL	0.31 + 0.021*SL
	t_{PHL}	0.30	0.27 + 0.016*SL	0.28 + 0.014*SL	0.28 + 0.012*SL
	t_R	0.26	0.17 + 0.043*SL	0.17 + 0.045*SL	0.16 + 0.046*SL
	t_F	0.15	0.11 + 0.020*SL	0.11 + 0.020*SL	0.11 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YLD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.49	0.29 + 0.098*SL	0.32 + 0.088*SL	0.34 + 0.086*SL
	t_{PHL}	0.52	0.34 + 0.092*SL	0.34 + 0.092*SL	0.34 + 0.092*SL
	t_R	0.43	0.21 + 0.110*SL	0.20 + 0.112*SL	0.20 + 0.113*SL
	t_F	0.25	0.12 + 0.065*SL	0.11 + 0.067*SL	0.11 + 0.067*SL
G to Q	t_{PLH}	0.67	0.48 + 0.092*SL	0.50 + 0.087*SL	0.51 + 0.086*SL
	t_{PHL}	0.69	0.50 + 0.092*SL	0.50 + 0.092*SL	0.50 + 0.092*SL
	t_R	0.42	0.20 + 0.112*SL	0.20 + 0.112*SL	0.19 + 0.113*SL
	t_F	0.25	0.11 + 0.068*SL	0.11 + 0.067*SL	0.11 + 0.068*SL
D to QN	t_{PLH}	0.36	0.26 + 0.050*SL	0.26 + 0.049*SL	0.26 + 0.050*SL
	t_{PHL}	0.23	0.16 + 0.038*SL	0.19 + 0.027*SL	0.22 + 0.023*SL
	t_R	0.47	0.27 + 0.101*SL	0.25 + 0.106*SL	0.22 + 0.109*SL
	t_F	0.29	0.20 + 0.042*SL	0.21 + 0.038*SL	0.19 + 0.040*SL
G to QN	t_{PLH}	0.52	0.42 + 0.051*SL	0.42 + 0.050*SL	0.42 + 0.050*SL
	t_{PHL}	0.42	0.36 + 0.030*SL	0.38 + 0.025*SL	0.39 + 0.023*SL
	t_R	0.44	0.23 + 0.105*SL	0.23 + 0.108*SL	0.21 + 0.109*SL
	t_F	0.21	0.13 + 0.042*SL	0.13 + 0.042*SL	0.12 + 0.043*SL

KGM80 YLD1D2

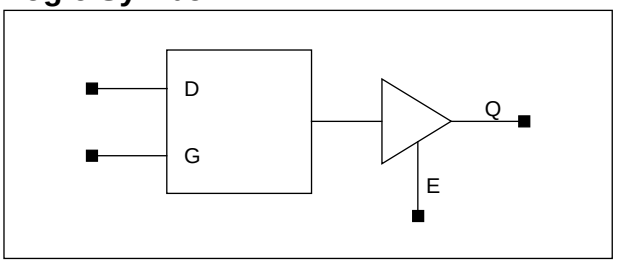
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.39	0.28 + 0.053*SL	0.30 + 0.047*SL	0.33 + 0.044*SL
	t_{PHL}	0.44	0.34 + 0.047*SL	0.35 + 0.045*SL	0.35 + 0.045*SL
	t_R	0.27	0.16 + 0.055*SL	0.16 + 0.055*SL	0.15 + 0.056*SL
	t_F	0.16	0.10 + 0.032*SL	0.09 + 0.033*SL	0.09 + 0.033*SL
G to Q	t_{PLH}	0.59	0.50 + 0.049*SL	0.51 + 0.045*SL	0.53 + 0.043*SL
	t_{PHL}	0.60	0.51 + 0.046*SL	0.51 + 0.046*SL	0.51 + 0.046*SL
	t_R	0.27	0.16 + 0.056*SL	0.15 + 0.056*SL	0.15 + 0.056*SL
	t_F	0.16	0.09 + 0.032*SL	0.09 + 0.033*SL	0.09 + 0.034*SL
D to QN	t_{PLH}	0.33	0.28 + 0.026*SL	0.28 + 0.025*SL	0.28 + 0.025*SL
	t_{PHL}	0.21	0.17 + 0.022*SL	0.18 + 0.016*SL	0.23 + 0.013*SL
	t_R	0.36	0.26 + 0.050*SL	0.26 + 0.052*SL	0.24 + 0.053*SL
	t_F	0.26	0.21 + 0.023*SL	0.22 + 0.019*SL	0.23 + 0.019*SL
G to QN	t_{PLH}	0.50	0.44 + 0.025*SL	0.45 + 0.025*SL	0.45 + 0.025*SL
	t_{PHL}	0.43	0.39 + 0.018*SL	0.40 + 0.014*SL	0.42 + 0.012*SL
	t_R	0.34	0.24 + 0.051*SL	0.23 + 0.053*SL	0.22 + 0.054*SL
	t_F	0.19	0.15 + 0.022*SL	0.15 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

LD1A

D Latch with Active High, Tri-State Output

Logic Symbol



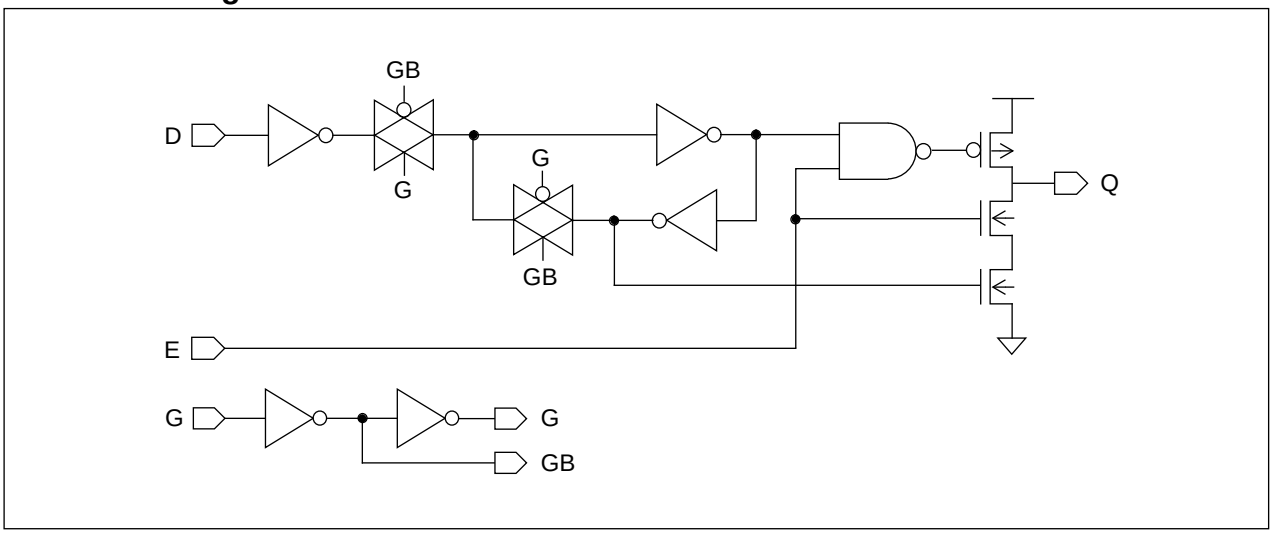
Truth Table

D	G	E	Q (n+1)
x	x	0	Hi-Z
0	1	1	0
1	1	1	1
x	0	1	Q (n)

Cell Data

Input Load (SL)			Output Load (SL)	Gate Count
KG80				
D	G	E	Q	
0.9	0.9	1.7	0.9	6.0
KGM80				
D	G	E	Q	
1.0	1.0	1.9	1.4	6.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width High (G)	t_{PWH}	0.61	0.99
Input Setup Time (D to G)	t_{SU}	0.34	0.64
Input Hold Time (D to G)	t_{HD}	0.15	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.47 + 0.043*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.64	0.56 + 0.040*SL	0.57 + 0.035*SL	0.58 + 0.034*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.066*SL	0.09 + 0.068*SL
G to Q	t_{PLH}	0.63	0.54 + 0.044*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.60	0.52 + 0.040*SL	0.53 + 0.035*SL	0.54 + 0.034*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.23	0.10 + 0.065*SL	0.10 + 0.066*SL	0.09 + 0.068*SL
E to Q	t_{PLH}	0.26	0.16 + 0.051*SL	0.18 + 0.042*SL	0.19 + 0.042*SL
	t_{PHL}	0.10	0.00 + 0.049*SL	0.03 + 0.037*SL	0.05 + 0.035*SL
	t_R	0.27	0.11 + 0.083*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.28	0.17 + 0.056*SL	0.16 + 0.062*SL	0.13 + 0.065*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.28	0.28 + 0.000*SL	0.28 + 0.000*SL	0.28 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1A

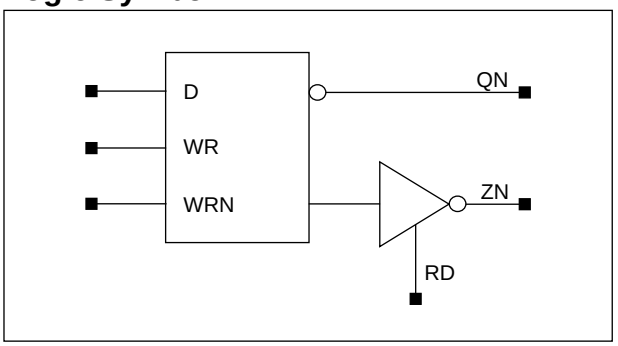
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.77	0.67 + 0.053*SL	0.68 + 0.050*SL	0.68 + 0.050*SL
	t_{PHL}	0.90	0.80 + 0.046*SL	0.82 + 0.039*SL	0.84 + 0.037*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.28	0.14 + 0.073*SL	0.14 + 0.072*SL	0.12 + 0.074*SL
G to Q	t_{PLH}	0.89	0.78 + 0.053*SL	0.79 + 0.050*SL	0.79 + 0.050*SL
	t_{PHL}	0.86	0.77 + 0.046*SL	0.79 + 0.039*SL	0.80 + 0.037*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.28	0.14 + 0.073*SL	0.14 + 0.072*SL	0.12 + 0.074*SL
E to Q	t_{PLH}	0.36	0.25 + 0.056*SL	0.26 + 0.050*SL	0.26 + 0.050*SL
	t_{PHL}	0.15	0.05 + 0.048*SL	0.08 + 0.039*SL	0.09 + 0.037*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.31	0.18 + 0.064*SL	0.16 + 0.070*SL	0.13 + 0.073*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.37	0.37 + -0.001*SL	0.36 + 0.000*SL	0.37 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

LD1B

D Latch with Active High, Tri-State Output, Separate WR, WRN

Logic Symbol



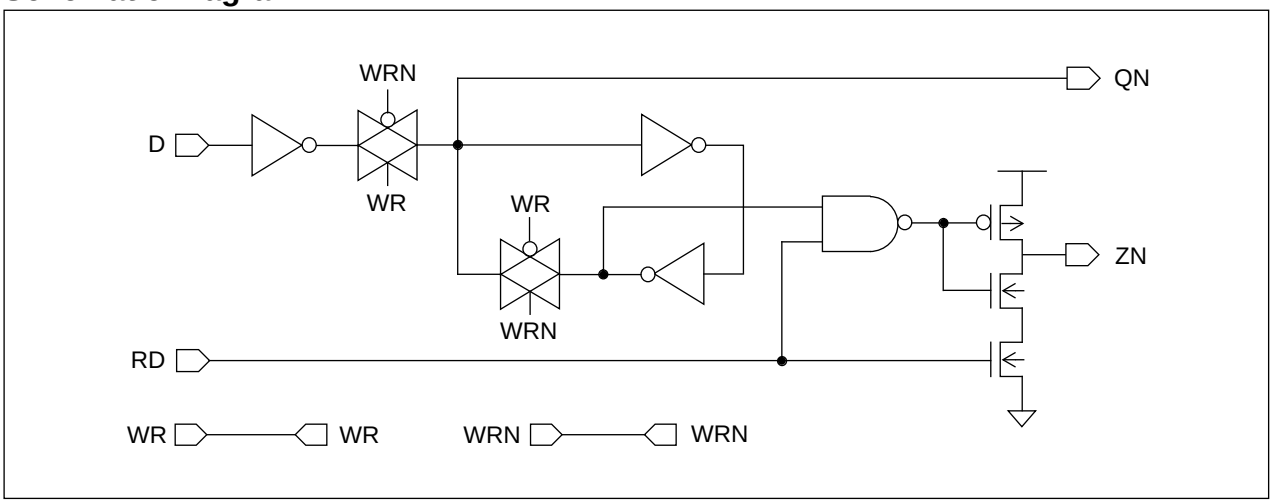
Truth Table

D	WR	WRN	RD	QN (n+1)	ZN (n+1)
0	1	0	0	1	Hi-Z
1	1	0	0	0	Hi-Z
0	1	0	1	1	1
1	1	0	1	0	0
x	0	1	0	QN (n)	Hi-Z
x	0	1	1	QN (n)	QN (n)

Cell Data

Input Load (SL)				Output Load (SL)	Gate Count
KG80					
D	WR	WRN	RD	ZN	
0.9	0.7	0.6	1.5	0.6	5.0
KGM80					
D	WR	WRN	RD	ZN	
1.0	1.1	0.7	1.8	0.8	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width High (WR)	t_{PWH}	0.61	0.99
Pulse Width Low (WRN)	t_{PWL}	0.61	0.99
Input Setup Time (D to WR)	t_{SU}	0.67	1.11
Input Hold Time (D to WR)	t_{HD}	0.15	0.33
Input Setup Time (D to WRN)	t_{SU}	0.67	1.11
Input Hold Time (D to WRN)	t_{HD}	0.15	0.33
Skew Time (WR to WRN)	t_{SK}	0.81	1.22
Skew Time (WRN to WR)	t_{SK}	0.81	1.22

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD1B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to QN	t_{PLH}	0.53	0.44 + 0.043*SL	0.45 + 0.042*SL	0.45 + 0.042*SL
	t_{PHL}	0.41	0.35 + 0.031*SL	0.36 + 0.027*SL	0.38 + 0.024*SL
	t_R	0.44	0.27 + 0.084*SL	0.26 + 0.088*SL	0.25 + 0.090*SL
	t_F	0.28	0.19 + 0.043*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
WR to QN	t_{PLH}	0.31	0.23 + 0.042*SL	0.23 + 0.042*SL	0.23 + 0.042*SL
	t_{PHL}	0.32	0.26 + 0.030*SL	0.27 + 0.026*SL	0.28 + 0.024*SL
	t_R	0.44	0.27 + 0.085*SL	0.27 + 0.088*SL	0.25 + 0.090*SL
	t_F	0.27	0.18 + 0.043*SL	0.19 + 0.042*SL	0.19 + 0.042*SL
WRN to QN	t_{PLH}	0.31	0.23 + 0.042*SL	0.23 + 0.042*SL	0.23 + 0.042*SL
	t_{PHL}	0.32	0.26 + 0.030*SL	0.27 + 0.026*SL	0.28 + 0.024*SL
	t_R	0.44	0.27 + 0.085*SL	0.27 + 0.088*SL	0.25 + 0.090*SL
	t_F	0.27	0.18 + 0.043*SL	0.19 + 0.042*SL	0.19 + 0.042*SL
D to ZN	t_{PLH}	0.82	0.64 + 0.090*SL	0.64 + 0.087*SL	0.66 + 0.085*SL
	t_{PHL}	0.67	0.52 + 0.075*SL	0.54 + 0.069*SL	0.56 + 0.065*SL
	t_R	0.31	0.14 + 0.087*SL	0.13 + 0.090*SL	0.12 + 0.091*SL
	t_F	0.21	0.08 + 0.065*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
WR to ZN	t_{PLH}	0.60	0.42 + 0.090*SL	0.43 + 0.086*SL	0.44 + 0.085*SL
	t_{PHL}	0.58	0.43 + 0.074*SL	0.45 + 0.068*SL	0.47 + 0.065*SL
	t_R	0.31	0.14 + 0.088*SL	0.13 + 0.090*SL	0.12 + 0.091*SL
	t_F	0.21	0.08 + 0.065*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
WRN to ZN	t_{PLH}	0.60	0.42 + 0.090*SL	0.43 + 0.086*SL	0.44 + 0.085*SL
	t_{PHL}	0.58	0.43 + 0.074*SL	0.45 + 0.068*SL	0.47 + 0.065*SL
	t_R	0.31	0.14 + 0.088*SL	0.13 + 0.090*SL	0.12 + 0.091*SL
	t_F	0.21	0.08 + 0.065*SL	0.08 + 0.068*SL	0.07 + 0.069*SL
RD to ZN	t_{PLH}	0.26	0.18 + 0.041*SL	0.18 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.11	0.00 + 0.055*SL	0.04 + 0.038*SL	0.07 + 0.034*SL
	t_R	0.31	0.14 + 0.084*SL	0.13 + 0.088*SL	0.12 + 0.091*SL
	t_F	0.29	0.15 + 0.067*SL	0.17 + 0.061*SL	0.14 + 0.065*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.33	0.32 + 0.002*SL	0.33 + 0.000*SL	0.33 + 0.000*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

LD1B

D Latch with Active High, Tri-State Output, Separate WR, WRN

Switching Characteristics

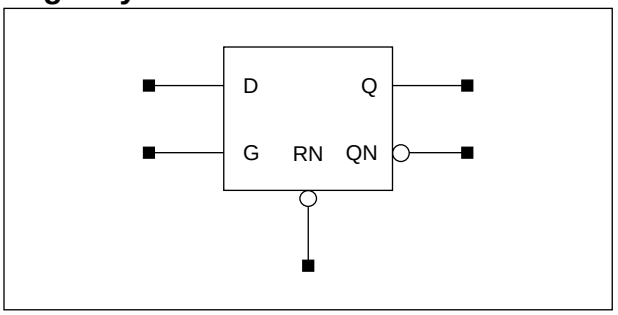
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD1B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to QN	t_{PLH}	0.70	0.60 + 0.052*SL	0.60 + 0.051*SL	0.60 + 0.050*SL
	t_{PHL}	0.59	0.52 + 0.035*SL	0.54 + 0.028*SL	0.58 + 0.024*SL
	t_R	0.59	0.38 + 0.102*SL	0.37 + 0.107*SL	0.35 + 0.109*SL
	t_F	0.35	0.26 + 0.044*SL	0.26 + 0.042*SL	0.27 + 0.042*SL
WR to QN	t_{PLH}	0.42	0.32 + 0.052*SL	0.32 + 0.051*SL	0.33 + 0.050*SL
	t_{PHL}	0.42	0.35 + 0.034*SL	0.37 + 0.027*SL	0.40 + 0.024*SL
	t_R	0.59	0.39 + 0.102*SL	0.37 + 0.107*SL	0.35 + 0.109*SL
	t_F	0.33	0.23 + 0.045*SL	0.24 + 0.043*SL	0.25 + 0.042*SL
WRN to QN	t_{PLH}	0.42	0.32 + 0.052*SL	0.32 + 0.051*SL	0.33 + 0.050*SL
	t_{PHL}	0.42	0.35 + 0.034*SL	0.37 + 0.027*SL	0.40 + 0.024*SL
	t_R	0.59	0.39 + 0.102*SL	0.37 + 0.107*SL	0.35 + 0.109*SL
	t_F	0.33	0.23 + 0.045*SL	0.24 + 0.043*SL	0.25 + 0.042*SL
D to ZN	t_{PLH}	1.10	0.88 + 0.110*SL	0.90 + 0.104*SL	0.93 + 0.101*SL
	t_{PHL}	0.94	0.78 + 0.085*SL	0.81 + 0.073*SL	0.86 + 0.069*SL
	t_R	0.40	0.19 + 0.106*SL	0.18 + 0.108*SL	0.17 + 0.109*SL
	t_F	0.25	0.11 + 0.071*SL	0.10 + 0.074*SL	0.09 + 0.075*SL
WR to ZN	t_{PLH}	0.82	0.60 + 0.111*SL	0.62 + 0.104*SL	0.66 + 0.101*SL
	t_{PHL}	0.77	0.60 + 0.084*SL	0.63 + 0.073*SL	0.68 + 0.069*SL
	t_R	0.40	0.19 + 0.106*SL	0.18 + 0.108*SL	0.17 + 0.109*SL
	t_F	0.25	0.11 + 0.072*SL	0.10 + 0.074*SL	0.09 + 0.074*SL
WRN to ZN	t_{PLH}	0.82	0.60 + 0.111*SL	0.62 + 0.104*SL	0.66 + 0.101*SL
	t_{PHL}	0.77	0.60 + 0.084*SL	0.63 + 0.073*SL	0.68 + 0.069*SL
	t_R	0.40	0.19 + 0.106*SL	0.18 + 0.108*SL	0.17 + 0.109*SL
	t_F	0.25	0.11 + 0.072*SL	0.10 + 0.074*SL	0.09 + 0.074*SL
RD to ZN	t_{PLH}	0.36	0.26 + 0.050*SL	0.27 + 0.049*SL	0.26 + 0.049*SL
	t_{PHL}	0.15	0.05 + 0.053*SL	0.09 + 0.039*SL	0.10 + 0.037*SL
	t_R	0.40	0.19 + 0.104*SL	0.18 + 0.108*SL	0.16 + 0.109*SL
	t_F	0.31	0.17 + 0.070*SL	0.17 + 0.069*SL	0.13 + 0.072*SL
	t_{PLZ}	0.20	0.20 + 0.000*SL	0.20 + 0.000*SL	0.20 + 0.000*SL
	t_{PHZ}	0.42	0.42 + 0.000*SL	0.42 + 0.000*SL	0.42 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



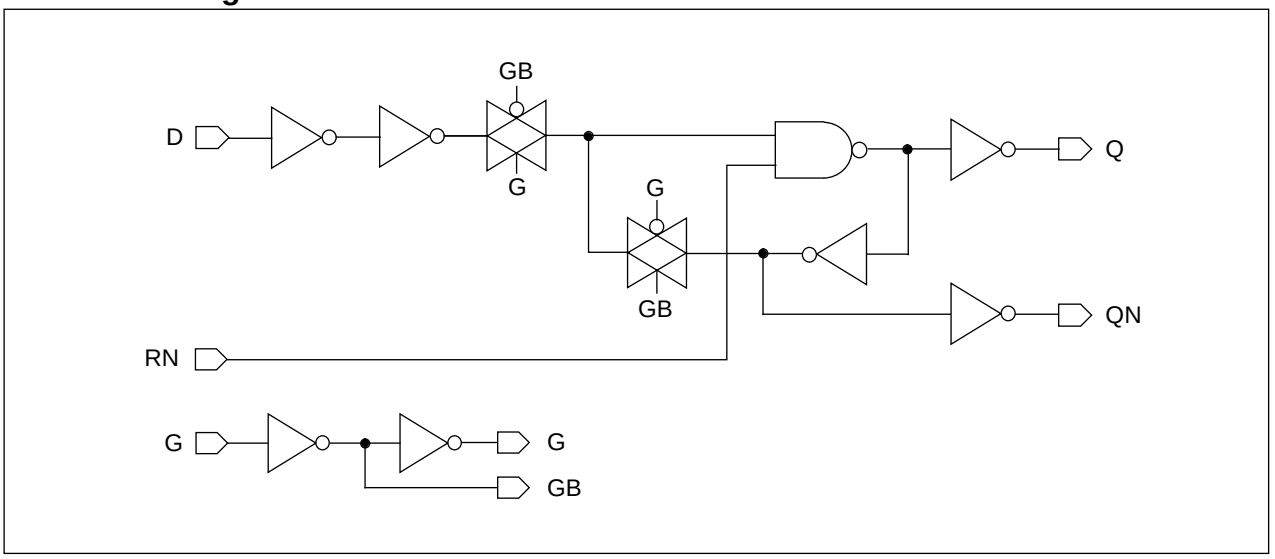
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
LD2			*LD2D2*			*LD2*	*LD2D2*
D	G	RN	D	G	RN		
0.9	0.9	0.9	0.9	0.9	0.9	6.0	7.0
KGM80							
LD2			*LD2D2*			*LD2*	*LD2D2*
D	G	RN	D	G	RN		
1.0	1.0	1.0	1.0	1.0	1.0	6.0	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD2	LD2D2	LD2	LD2D2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.37	0.39	0.64	0.68
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to G)	t_{HD}	0.26	0.20	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.47 + 0.044*SL	0.47 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.58	0.52 + 0.031*SL	0.53 + 0.026*SL	0.55 + 0.024*SL
	t_R	0.29	0.12 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.11 + 0.039*SL	0.09 + 0.041*SL
G to Q	t_{PLH}	0.52	0.44 + 0.044*SL	0.44 + 0.042*SL	0.44 + 0.042*SL
	t_{PHL}	0.50	0.44 + 0.032*SL	0.45 + 0.026*SL	0.47 + 0.023*SL
	t_R	0.29	0.11 + 0.087*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
RN to Q	t_{PLH}	0.31	0.22 + 0.044*SL	0.23 + 0.042*SL	0.23 + 0.042*SL
	t_{PHL}	0.30	0.24 + 0.030*SL	0.25 + 0.025*SL	0.27 + 0.023*SL
	t_R	0.29	0.12 + 0.085*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.039*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
D to QN	t_{PLH}	0.72	0.64 + 0.040*SL	0.64 + 0.041*SL	0.64 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.030*SL	0.59 + 0.025*SL	0.60 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
G to QN	t_{PLH}	0.64	0.56 + 0.040*SL	0.56 + 0.041*SL	0.56 + 0.042*SL
	t_{PHL}	0.60	0.55 + 0.029*SL	0.55 + 0.025*SL	0.57 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
RN to QN	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.041*SL	0.44 + 0.040*SL
	t_{PHL}	0.39	0.33 + 0.030*SL	0.34 + 0.025*SL	0.35 + 0.023*SL
	t_R	0.29	0.12 + 0.084*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.17	0.09 + 0.038*SL	0.09 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.54	0.49 + 0.025*SL	0.50 + 0.022*SL	0.51 + 0.021*SL
	t_{PHL}	0.57	0.53 + 0.021*SL	0.54 + 0.016*SL	0.56 + 0.014*SL
	t_R	0.19	0.11 + 0.041*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.15	0.11 + 0.023*SL	0.11 + 0.020*SL	0.12 + 0.019*SL
G to Q	t_{PLH}	0.51	0.46 + 0.025*SL	0.47 + 0.022*SL	0.47 + 0.021*SL
	t_{PHL}	0.49	0.45 + 0.022*SL	0.46 + 0.016*SL	0.48 + 0.014*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
RN to Q	t_{PLH}	0.29	0.25 + 0.023*SL	0.25 + 0.022*SL	0.26 + 0.021*SL
	t_{PHL}	0.30	0.26 + 0.020*SL	0.27 + 0.015*SL	0.29 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.11 + 0.019*SL	0.10 + 0.019*SL
D to QN	t_{PLH}	0.75	0.71 + 0.019*SL	0.71 + 0.019*SL	0.70 + 0.020*SL
	t_{PHL}	0.68	0.64 + 0.018*SL	0.65 + 0.015*SL	0.66 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.019*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
G to QN	t_{PLH}	0.66	0.62 + 0.019*SL	0.62 + 0.019*SL	0.62 + 0.020*SL
	t_{PHL}	0.64	0.61 + 0.018*SL	0.62 + 0.014*SL	0.63 + 0.013*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
RN to QN	t_{PLH}	0.53	0.49 + 0.023*SL	0.50 + 0.020*SL	0.49 + 0.020*SL
	t_{PHL}	0.43	0.39 + 0.018*SL	0.40 + 0.015*SL	0.42 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.042*SL	0.09 + 0.043*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.80	0.69 + 0.054*SL	0.70 + 0.051*SL	0.71 + 0.050*SL
	t_{PHL}	0.79	0.72 + 0.035*SL	0.74 + 0.027*SL	0.77 + 0.023*SL
	t_R	0.38	0.17 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.041*SL	0.12 + 0.042*SL
G to Q	t_{PLH}	0.74	0.63 + 0.054*SL	0.64 + 0.051*SL	0.65 + 0.050*SL
	t_{PHL}	0.71	0.64 + 0.036*SL	0.66 + 0.027*SL	0.70 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.12 + 0.042*SL
RN to Q	t_{PLH}	0.40	0.30 + 0.053*SL	0.30 + 0.051*SL	0.31 + 0.050*SL
	t_{PHL}	0.39	0.32 + 0.034*SL	0.34 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.11 + 0.042*SL
D to QN	t_{PLH}	0.99	0.89 + 0.049*SL	0.89 + 0.050*SL	0.89 + 0.050*SL
	t_{PHL}	0.93	0.86 + 0.032*SL	0.88 + 0.026*SL	0.90 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
G to QN	t_{PLH}	0.91	0.81 + 0.049*SL	0.81 + 0.050*SL	0.81 + 0.050*SL
	t_{PHL}	0.86	0.80 + 0.032*SL	0.82 + 0.026*SL	0.84 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.67	0.57 + 0.053*SL	0.58 + 0.050*SL	0.58 + 0.050*SL
	t_{PHL}	0.53	0.46 + 0.032*SL	0.48 + 0.026*SL	0.51 + 0.023*SL
	t_R	0.38	0.17 + 0.103*SL	0.17 + 0.106*SL	0.14 + 0.108*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD2D2

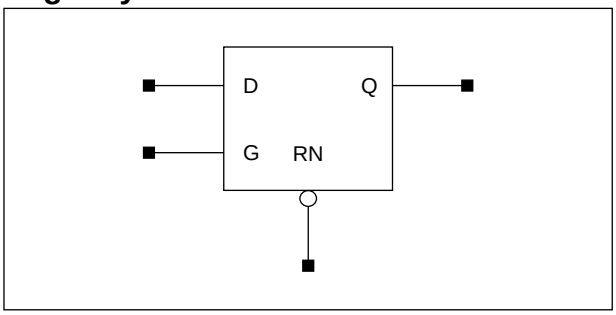
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.78	0.71 + 0.032*SL	0.73 + 0.027*SL	0.74 + 0.025*SL
	t_{PHL}	0.78	0.73 + 0.025*SL	0.76 + 0.017*SL	0.79 + 0.014*SL
	t_R	0.24	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
G to Q	t_{PLH}	0.71	0.65 + 0.031*SL	0.66 + 0.027*SL	0.68 + 0.025*SL
	t_{PHL}	0.71	0.66 + 0.025*SL	0.68 + 0.017*SL	0.72 + 0.014*SL
	t_R	0.24	0.13 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
RN to Q	t_{PLH}	0.38	0.32 + 0.031*SL	0.33 + 0.026*SL	0.34 + 0.025*SL
	t_{PHL}	0.39	0.34 + 0.024*SL	0.36 + 0.016*SL	0.40 + 0.013*SL
	t_R	0.24	0.13 + 0.052*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.17	0.12 + 0.024*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
D to QN	t_{PLH}	1.02	0.98 + 0.024*SL	0.98 + 0.024*SL	0.97 + 0.025*SL
	t_{PHL}	0.99	0.95 + 0.021*SL	0.96 + 0.016*SL	0.99 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
G to QN	t_{PLH}	0.95	0.90 + 0.024*SL	0.90 + 0.024*SL	0.89 + 0.025*SL
	t_{PHL}	0.93	0.88 + 0.020*SL	0.90 + 0.016*SL	0.93 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
RN to QN	t_{PLH}	0.71	0.65 + 0.029*SL	0.66 + 0.025*SL	0.66 + 0.025*SL
	t_{PHL}	0.59	0.55 + 0.020*SL	0.56 + 0.016*SL	0.59 + 0.013*SL
	t_R	0.24	0.14 + 0.053*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.021*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

LD2Q/LD2QD2

D Latch with Active High, Reset, Q Output Only, 1X/2X Drive

Logic Symbol



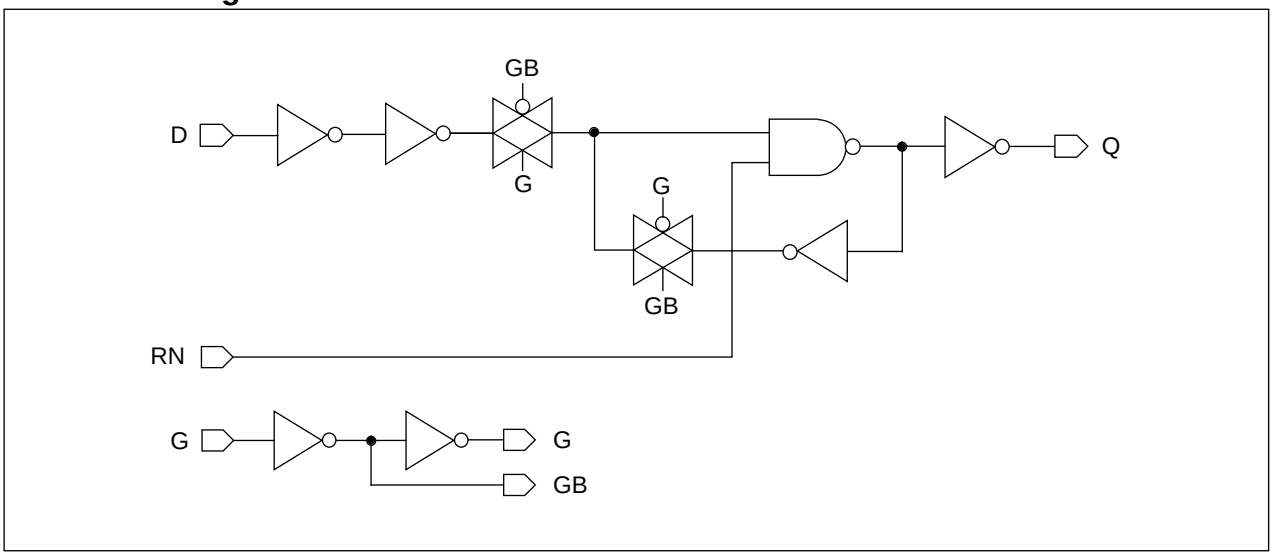
Truth Table

D	G	RN	Q (n+1)
0	1	1	0
1	1	1	1
x	0	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
KG80							
LD2Q			*LD2QD2*			*LD2Q*	*LD2QD2*
D	G	RN	D	G	RN		
0.8	0.8	0.7	0.8	0.8	0.7	6.0	7.0
KGM80							
LD2Q			*LD2QD2*			*LD2Q*	*LD2QD2*
D	G	RN	D	G	RN		
0.9	0.9	0.9	0.9	0.9	0.9	6.0	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD2Q	LD2QD2	LD2Q	LD2QD2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.37	0.39	0.68	0.71
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to G)	t_{HD}	0.26	0.20	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.47 + 0.045*SL	0.48 + 0.042*SL	0.48 + 0.042*SL
	t_{PHL}	0.55	0.49 + 0.031*SL	0.50 + 0.026*SL	0.52 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
G to Q	t_{PLH}	0.53	0.44 + 0.045*SL	0.45 + 0.042*SL	0.45 + 0.042*SL
	t_{PHL}	0.47	0.40 + 0.031*SL	0.42 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
RN to Q	t_{PLH}	0.30	0.21 + 0.045*SL	0.22 + 0.042*SL	0.22 + 0.041*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.30 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.038*SL	0.09 + 0.040*SL

KG80 LD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.51 + 0.024*SL	0.52 + 0.022*SL	0.52 + 0.021*SL
	t_{PHL}	0.55	0.51 + 0.019*SL	0.52 + 0.015*SL	0.54 + 0.013*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.044*SL	0.11 + 0.044*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
G to Q	t_{PLH}	0.52	0.48 + 0.024*SL	0.48 + 0.022*SL	0.49 + 0.021*SL
	t_{PHL}	0.47	0.43 + 0.019*SL	0.44 + 0.015*SL	0.45 + 0.013*SL
	t_R	0.21	0.12 + 0.044*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.15	0.10 + 0.024*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
RN to Q	t_{PLH}	0.29	0.25 + 0.024*SL	0.25 + 0.022*SL	0.26 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.021*SL	0.30 + 0.015*SL	0.32 + 0.013*SL
	t_R	0.21	0.12 + 0.045*SL	0.12 + 0.043*SL	0.11 + 0.045*SL
	t_F	0.16	0.12 + 0.021*SL	0.13 + 0.019*SL	0.13 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≤ SL ≤ 7, *Group3 : 7 < SL

LD2Q/LD2QD2

D Latch with Active High, Reset, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD2Q

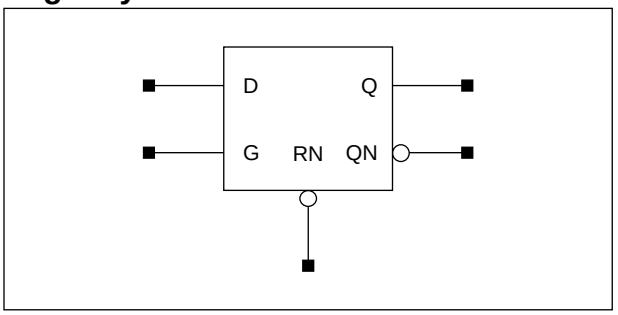
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.82	0.71 + 0.055*SL	0.72 + 0.051*SL	0.73 + 0.050*SL
	t_{PHL}	0.75	0.67 + 0.036*SL	0.70 + 0.026*SL	0.73 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.20	0.11 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
G to Q	t_{PLH}	0.76	0.65 + 0.055*SL	0.67 + 0.051*SL	0.67 + 0.050*SL
	t_{PHL}	0.66	0.59 + 0.036*SL	0.62 + 0.026*SL	0.65 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.20	0.12 + 0.045*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q	t_{PLH}	0.41	0.30 + 0.055*SL	0.31 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.036*SL	0.39 + 0.027*SL	0.43 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.040*SL	0.12 + 0.042*SL

KGM80 LD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.82	0.76 + 0.031*SL	0.77 + 0.027*SL	0.79 + 0.025*SL
	t_{PHL}	0.75	0.71 + 0.021*SL	0.72 + 0.016*SL	0.76 + 0.013*SL
	t_R	0.27	0.17 + 0.053*SL	0.17 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
G to Q	t_{PLH}	0.76	0.70 + 0.031*SL	0.71 + 0.027*SL	0.73 + 0.025*SL
	t_{PHL}	0.67	0.63 + 0.022*SL	0.64 + 0.016*SL	0.68 + 0.013*SL
	t_R	0.27	0.16 + 0.054*SL	0.17 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
RN to Q	t_{PLH}	0.40	0.34 + 0.030*SL	0.35 + 0.027*SL	0.36 + 0.025*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.42 + 0.016*SL	0.45 + 0.013*SL
	t_R	0.27	0.16 + 0.053*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.14 + 0.025*SL	0.16 + 0.020*SL	0.17 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

Logic Symbol



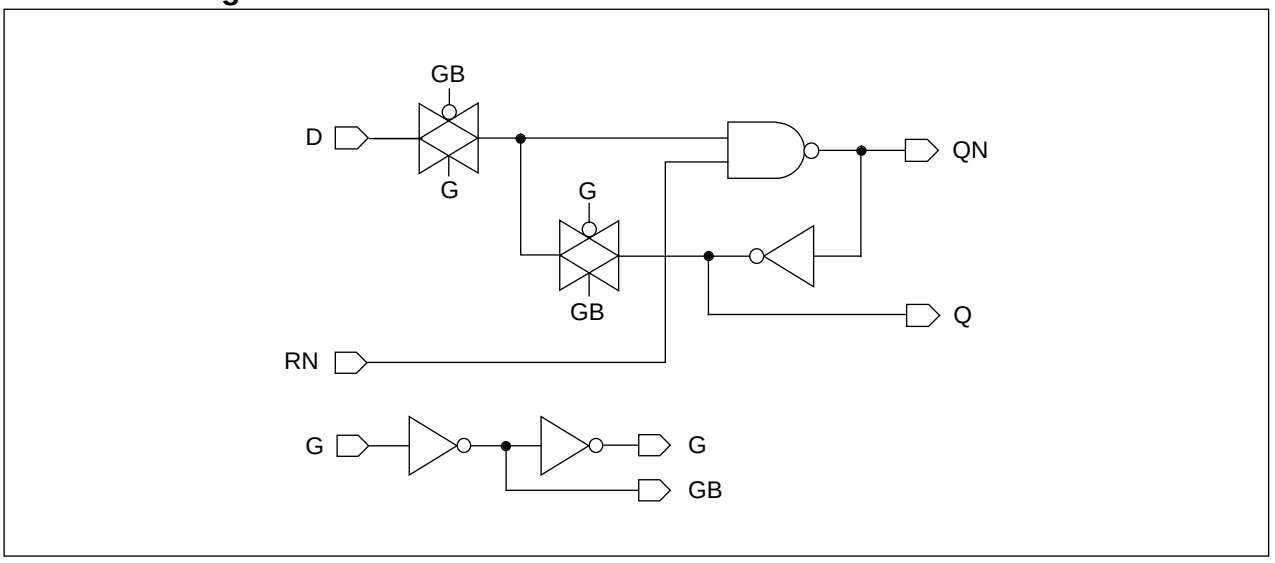
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
YLD2			*YLD2D2*			*YLD2*	*YLD2D2*
D	G	RN	D	G	RN		
2.9	0.8	0.7	3.7	0.8	1.5	6.0	7.0
KGM80							
YLD2			*YLD2D2*			*YLD2*	*YLD2D2*
D	G	RN	D	G	RN		
3.7	0.9	0.9	4.6	0.9	1.7	6.0	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		YLD2	YLD2D2	YLD2	YLD2D2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.23	0.20	0.46	0.43
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to G)	t_{HD}	0.15	0.20	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YLD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.45	0.25 + 0.100*SL	0.26 + 0.095*SL	0.26 + 0.095*SL
	t_{PHL}	0.41	0.26 + 0.078*SL	0.26 + 0.076*SL	0.26 + 0.076*SL
	t_R	0.35	0.15 + 0.099*SL	0.15 + 0.100*SL	0.14 + 0.100*SL
	t_F	0.22	0.10 + 0.060*SL	0.09 + 0.062*SL	0.09 + 0.063*SL
G to Q	t_{PLH}	0.58	0.38 + 0.097*SL	0.39 + 0.095*SL	0.39 + 0.095*SL
	t_{PHL}	0.51	0.36 + 0.077*SL	0.36 + 0.077*SL	0.36 + 0.077*SL
	t_R	0.34	0.14 + 0.099*SL	0.14 + 0.100*SL	0.14 + 0.100*SL
	t_F	0.21	0.09 + 0.062*SL	0.09 + 0.064*SL	0.09 + 0.063*SL
RN to Q	t_{PLH}	0.40	0.20 + 0.095*SL	0.21 + 0.095*SL	0.21 + 0.095*SL
	t_{PHL}	0.47	0.32 + 0.079*SL	0.32 + 0.077*SL	0.32 + 0.077*SL
	t_R	0.34	0.15 + 0.097*SL	0.14 + 0.100*SL	0.14 + 0.100*SL
	t_F	0.32	0.21 + 0.057*SL	0.20 + 0.060*SL	0.20 + 0.061*SL
D to QN	t_{PLH}	0.29	0.21 + 0.041*SL	0.21 + 0.041*SL	0.20 + 0.041*SL
	t_{PHL}	0.23	0.15 + 0.041*SL	0.16 + 0.035*SL	0.17 + 0.034*SL
	t_R	0.41	0.25 + 0.079*SL	0.23 + 0.085*SL	0.21 + 0.089*SL
	t_F	0.36	0.25 + 0.054*SL	0.23 + 0.062*SL	0.21 + 0.065*SL
G to QN	t_{PLH}	0.39	0.30 + 0.042*SL	0.30 + 0.042*SL	0.30 + 0.042*SL
	t_{PHL}	0.36	0.29 + 0.036*SL	0.29 + 0.035*SL	0.30 + 0.034*SL
	t_R	0.37	0.19 + 0.087*SL	0.19 + 0.090*SL	0.18 + 0.091*SL
	t_F	0.29	0.15 + 0.066*SL	0.15 + 0.068*SL	0.14 + 0.068*SL
RN to QN	t_{PLH}	0.29	0.21 + 0.040*SL	0.21 + 0.040*SL	0.20 + 0.041*SL
	t_{PHL}	0.18	0.10 + 0.038*SL	0.11 + 0.035*SL	0.12 + 0.034*SL
	t_R	0.44	0.30 + 0.071*SL	0.29 + 0.075*SL	0.27 + 0.079*SL
	t_F	0.32	0.21 + 0.056*SL	0.19 + 0.064*SL	0.17 + 0.067*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YLD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.34	0.24 + 0.053*SL	0.25 + 0.049*SL	0.26 + 0.048*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.26 + 0.038*SL	0.26 + 0.038*SL
	t_R	0.22	0.13 + 0.049*SL	0.12 + 0.050*SL	0.12 + 0.050*SL
	t_F	0.14	0.08 + 0.030*SL	0.08 + 0.030*SL	0.08 + 0.032*SL
G to Q	t_{PLH}	0.49	0.39 + 0.050*SL	0.39 + 0.048*SL	0.39 + 0.048*SL
	t_{PHL}	0.44	0.37 + 0.039*SL	0.37 + 0.039*SL	0.37 + 0.039*SL
	t_R	0.22	0.12 + 0.050*SL	0.12 + 0.051*SL	0.11 + 0.051*SL
	t_F	0.14	0.08 + 0.030*SL	0.08 + 0.031*SL	0.07 + 0.032*SL
RN to Q	t_{PLH}	0.28	0.18 + 0.050*SL	0.19 + 0.048*SL	0.19 + 0.048*SL
	t_{PHL}	0.36	0.28 + 0.041*SL	0.28 + 0.039*SL	0.29 + 0.039*SL
	t_R	0.22	0.13 + 0.047*SL	0.12 + 0.050*SL	0.12 + 0.051*SL
	t_F	0.22	0.16 + 0.028*SL	0.16 + 0.029*SL	0.16 + 0.030*SL
D to QN	t_{PLH}	0.26	0.22 + 0.021*SL	0.22 + 0.020*SL	0.22 + 0.021*SL
	t_{PHL}	0.20	0.15 + 0.023*SL	0.16 + 0.019*SL	0.17 + 0.017*SL
	t_R	0.32	0.24 + 0.040*SL	0.24 + 0.042*SL	0.23 + 0.044*SL
	t_F	0.30	0.25 + 0.028*SL	0.24 + 0.029*SL	0.23 + 0.031*SL
G to QN	t_{PLH}	0.37	0.32 + 0.021*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.35	0.31 + 0.019*SL	0.31 + 0.018*SL	0.32 + 0.017*SL
	t_R	0.28	0.19 + 0.045*SL	0.19 + 0.045*SL	0.19 + 0.046*SL
	t_F	0.23	0.17 + 0.031*SL	0.16 + 0.033*SL	0.16 + 0.033*SL
RN to QN	t_{PLH}	0.25	0.21 + 0.020*SL	0.21 + 0.020*SL	0.20 + 0.021*SL
	t_{PHL}	0.14	0.10 + 0.020*SL	0.10 + 0.018*SL	0.11 + 0.017*SL
	t_R	0.37	0.30 + 0.035*SL	0.30 + 0.036*SL	0.29 + 0.037*SL
	t_F	0.26	0.21 + 0.026*SL	0.20 + 0.030*SL	0.19 + 0.031*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YLD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.61	0.38 + 0.115*SL	0.39 + 0.110*SL	0.40 + 0.109*SL
	t_{PHL}	0.55	0.36 + 0.092*SL	0.36 + 0.092*SL	0.37 + 0.092*SL
	t_R	0.46	0.22 + 0.117*SL	0.22 + 0.119*SL	0.22 + 0.119*SL
	t_F	0.26	0.12 + 0.066*SL	0.12 + 0.067*SL	0.12 + 0.067*SL
G to Q	t_{PLH}	0.78	0.56 + 0.113*SL	0.56 + 0.110*SL	0.57 + 0.109*SL
	t_{PHL}	0.71	0.53 + 0.093*SL	0.53 + 0.092*SL	0.53 + 0.092*SL
	t_R	0.45	0.22 + 0.118*SL	0.22 + 0.119*SL	0.21 + 0.119*SL
	t_F	0.25	0.12 + 0.068*SL	0.12 + 0.068*SL	0.12 + 0.068*SL
RN to Q	t_{PLH}	0.52	0.30 + 0.112*SL	0.30 + 0.110*SL	0.31 + 0.109*SL
	t_{PHL}	0.60	0.41 + 0.097*SL	0.42 + 0.094*SL	0.44 + 0.092*SL
	t_R	0.46	0.22 + 0.117*SL	0.22 + 0.119*SL	0.22 + 0.119*SL
	t_F	0.40	0.28 + 0.061*SL	0.27 + 0.064*SL	0.26 + 0.066*SL
D to QN	t_{PLH}	0.38	0.28 + 0.050*SL	0.28 + 0.050*SL	0.28 + 0.050*SL
	t_{PHL}	0.32	0.23 + 0.045*SL	0.25 + 0.038*SL	0.26 + 0.037*SL
	t_R	0.52	0.31 + 0.103*SL	0.30 + 0.106*SL	0.27 + 0.109*SL
	t_F	0.42	0.28 + 0.066*SL	0.28 + 0.069*SL	0.24 + 0.072*SL
G to QN	t_{PLH}	0.54	0.44 + 0.051*SL	0.44 + 0.050*SL	0.45 + 0.050*SL
	t_{PHL}	0.50	0.41 + 0.041*SL	0.42 + 0.038*SL	0.43 + 0.037*SL
	t_R	0.49	0.28 + 0.106*SL	0.27 + 0.109*SL	0.26 + 0.109*SL
	t_F	0.35	0.21 + 0.072*SL	0.21 + 0.073*SL	0.19 + 0.074*SL
RN to QN	t_{PLH}	0.36	0.26 + 0.049*SL	0.26 + 0.050*SL	0.26 + 0.050*SL
	t_{PHL}	0.23	0.15 + 0.041*SL	0.16 + 0.038*SL	0.17 + 0.037*SL
	t_R	0.57	0.38 + 0.096*SL	0.38 + 0.097*SL	0.37 + 0.098*SL
	t_F	0.36	0.23 + 0.067*SL	0.22 + 0.072*SL	0.20 + 0.074*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YLD2D2

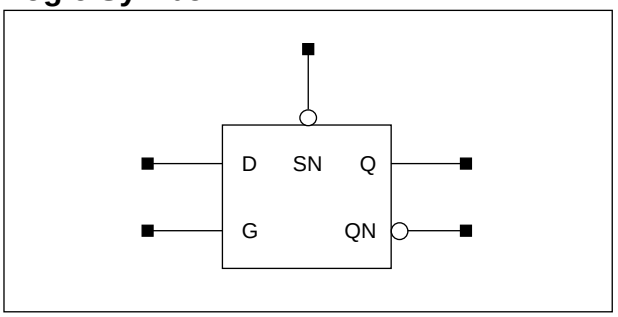
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.49	0.36 + 0.061*SL	0.38 + 0.056*SL	0.39 + 0.055*SL
	t_{PHL}	0.46	0.36 + 0.047*SL	0.37 + 0.046*SL	0.37 + 0.046*SL
	t_R	0.29	0.18 + 0.058*SL	0.18 + 0.059*SL	0.17 + 0.059*SL
	t_F	0.17	0.11 + 0.032*SL	0.10 + 0.033*SL	0.10 + 0.033*SL
G to Q	t_{PLH}	0.68	0.57 + 0.059*SL	0.57 + 0.056*SL	0.59 + 0.055*SL
	t_{PHL}	0.63	0.53 + 0.047*SL	0.53 + 0.046*SL	0.54 + 0.046*SL
	t_R	0.29	0.17 + 0.059*SL	0.17 + 0.059*SL	0.17 + 0.059*SL
	t_F	0.17	0.10 + 0.034*SL	0.10 + 0.033*SL	0.10 + 0.033*SL
RN to Q	t_{PLH}	0.38	0.27 + 0.058*SL	0.27 + 0.055*SL	0.28 + 0.055*SL
	t_{PHL}	0.46	0.36 + 0.049*SL	0.37 + 0.047*SL	0.38 + 0.046*SL
	t_R	0.29	0.17 + 0.059*SL	0.18 + 0.059*SL	0.17 + 0.059*SL
	t_F	0.27	0.21 + 0.032*SL	0.21 + 0.032*SL	0.20 + 0.032*SL
D to QN	t_{PLH}	0.35	0.30 + 0.026*SL	0.30 + 0.025*SL	0.30 + 0.025*SL
	t_{PHL}	0.29	0.24 + 0.026*SL	0.25 + 0.021*SL	0.27 + 0.019*SL
	t_R	0.41	0.30 + 0.052*SL	0.30 + 0.052*SL	0.28 + 0.053*SL
	t_F	0.36	0.29 + 0.033*SL	0.29 + 0.033*SL	0.28 + 0.034*SL
G to QN	t_{PLH}	0.52	0.46 + 0.026*SL	0.47 + 0.025*SL	0.47 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.022*SL	0.45 + 0.020*SL	0.47 + 0.018*SL
	t_R	0.38	0.28 + 0.053*SL	0.28 + 0.054*SL	0.27 + 0.054*SL
	t_F	0.29	0.22 + 0.036*SL	0.22 + 0.035*SL	0.22 + 0.036*SL
RN to QN	t_{PLH}	0.31	0.26 + 0.025*SL	0.26 + 0.025*SL	0.26 + 0.025*SL
	t_{PHL}	0.19	0.14 + 0.022*SL	0.15 + 0.020*SL	0.16 + 0.018*SL
	t_R	0.48	0.38 + 0.047*SL	0.38 + 0.047*SL	0.37 + 0.048*SL
	t_F	0.30	0.23 + 0.033*SL	0.22 + 0.035*SL	0.21 + 0.036*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

LD3/LD3D2

D Latch with Active High, Set, 1X/2X Drive

Logic Symbol



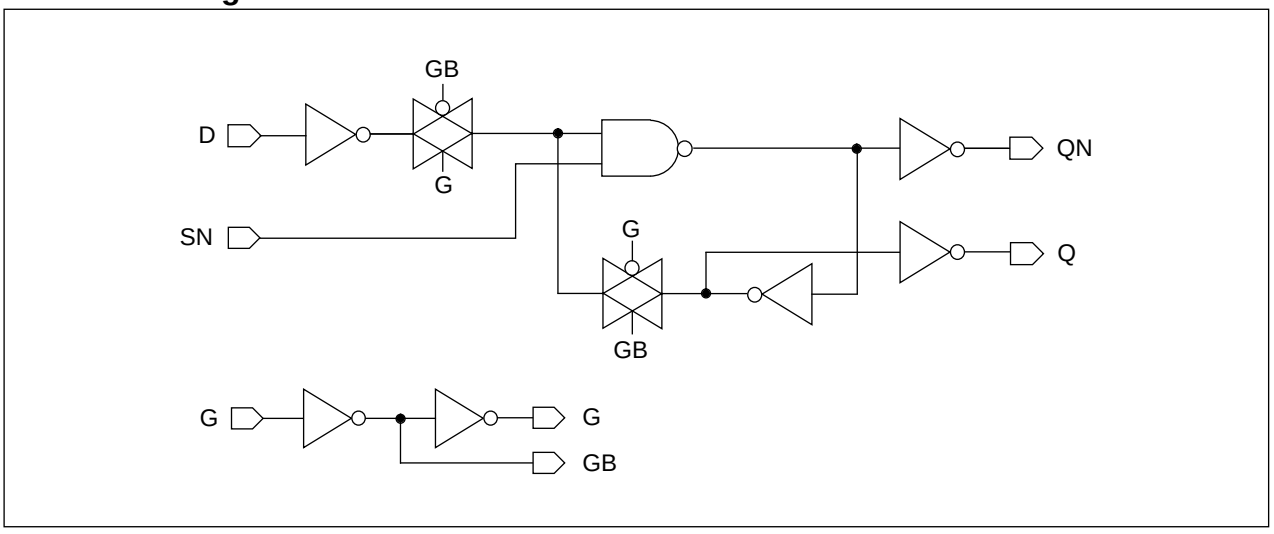
Truth Table

D	G	SN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
KG80							
LD3			*LD3D2*			*LD3*	*LD3D2*
D	G	SN	D	G	SN		
0.8	0.8	0.7	0.8	0.8	0.7	8.0	9.0
KGM80							
LD3			*LD3D2*			*LD3*	*LD3D2*
D	G	SN	D	G	SN		
0.9	0.9	0.9	0.9	0.9	0.9	8.0	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD3	LD3D2	LD3	LD3D2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.39	0.42	0.71	0.74
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to G)	t_{HD}	0.20	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.54	0.46 + 0.040*SL	0.45 + 0.041*SL	0.45 + 0.042*SL
	t_{PHL}	0.65	0.59 + 0.028*SL	0.60 + 0.025*SL	0.61 + 0.023*SL
	t_R	0.26	0.08 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
G to Q	t_{PLH}	0.59	0.51 + 0.040*SL	0.51 + 0.041*SL	0.51 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.028*SL	0.54 + 0.025*SL	0.55 + 0.023*SL
	t_R	0.26	0.08 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
SN to Q	t_{PLH}	0.55	0.47 + 0.042*SL	0.47 + 0.041*SL	0.47 + 0.041*SL
	t_{PHL}	0.37	0.31 + 0.028*SL	0.32 + 0.025*SL	0.33 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.087*SL	0.09 + 0.090*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.58	0.49 + 0.044*SL	0.50 + 0.042*SL	0.50 + 0.041*SL
	t_{PHL}	0.41	0.35 + 0.031*SL	0.36 + 0.026*SL	0.38 + 0.024*SL
	t_R	0.28	0.11 + 0.087*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
G to QN	t_{PLH}	0.53	0.44 + 0.045*SL	0.44 + 0.042*SL	0.45 + 0.042*SL
	t_{PHL}	0.47	0.40 + 0.031*SL	0.42 + 0.026*SL	0.43 + 0.024*SL
	t_R	0.28	0.10 + 0.087*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to QN	t_{PLH}	0.30	0.21 + 0.045*SL	0.22 + 0.042*SL	0.22 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.032*SL	0.29 + 0.026*SL	0.30 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.53 + 0.018*SL	0.52 + 0.020*SL	0.52 + 0.021*SL
	t_{PHL}	0.69	0.66 + 0.016*SL	0.66 + 0.014*SL	0.67 + 0.012*SL
	t_R	0.18	0.09 + 0.042*SL	0.09 + 0.044*SL	0.08 + 0.046*SL
	t_F	0.14	0.10 + 0.020*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
G to Q	t_{PLH}	0.62	0.58 + 0.019*SL	0.58 + 0.020*SL	0.57 + 0.021*SL
	t_{PHL}	0.64	0.60 + 0.016*SL	0.61 + 0.014*SL	0.62 + 0.012*SL
	t_R	0.18	0.09 + 0.042*SL	0.09 + 0.044*SL	0.08 + 0.046*SL
	t_F	0.14	0.10 + 0.019*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
SN to Q	t_{PLH}	0.58	0.53 + 0.021*SL	0.54 + 0.020*SL	0.53 + 0.020*SL
	t_{PHL}	0.40	0.37 + 0.016*SL	0.38 + 0.014*SL	0.39 + 0.012*SL
	t_R	0.20	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.14	0.10 + 0.019*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
D to QN	t_{PLH}	0.58	0.53 + 0.024*SL	0.53 + 0.022*SL	0.54 + 0.021*SL
	t_{PHL}	0.41	0.37 + 0.019*SL	0.38 + 0.015*SL	0.40 + 0.013*SL
	t_R	0.20	0.12 + 0.043*SL	0.12 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.15	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
G to QN	t_{PLH}	0.52	0.47 + 0.025*SL	0.48 + 0.022*SL	0.48 + 0.021*SL
	t_{PHL}	0.46	0.43 + 0.019*SL	0.44 + 0.015*SL	0.45 + 0.013*SL
	t_R	0.20	0.12 + 0.044*SL	0.12 + 0.044*SL	0.11 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.021*SL	0.11 + 0.020*SL
SN to QN	t_{PLH}	0.29	0.24 + 0.024*SL	0.25 + 0.022*SL	0.25 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.020*SL	0.30 + 0.015*SL	0.32 + 0.013*SL
	t_R	0.20	0.12 + 0.041*SL	0.12 + 0.043*SL	0.11 + 0.045*SL
	t_F	0.16	0.12 + 0.020*SL	0.12 + 0.019*SL	0.12 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.75	0.65 + 0.049*SL	0.65 + 0.050*SL	0.65 + 0.050*SL
	t_{PHL}	0.92	0.85 + 0.032*SL	0.87 + 0.025*SL	0.89 + 0.023*SL
	t_R	0.33	0.12 + 0.105*SL	0.11 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.041*SL	0.09 + 0.043*SL
G to Q	t_{PLH}	0.84	0.75 + 0.049*SL	0.74 + 0.050*SL	0.75 + 0.050*SL
	t_{PHL}	0.87	0.80 + 0.031*SL	0.82 + 0.025*SL	0.84 + 0.023*SL
	t_R	0.33	0.12 + 0.105*SL	0.11 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.042*SL	0.10 + 0.041*SL	0.09 + 0.043*SL
SN to Q	t_{PLH}	0.73	0.62 + 0.054*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_{PHL}	0.51	0.45 + 0.032*SL	0.47 + 0.025*SL	0.49 + 0.023*SL
	t_R	0.37	0.16 + 0.103*SL	0.16 + 0.106*SL	0.13 + 0.108*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.041*SL	0.09 + 0.043*SL
D to QN	t_{PLH}	0.81	0.70 + 0.055*SL	0.71 + 0.051*SL	0.72 + 0.050*SL
	t_{PHL}	0.57	0.50 + 0.035*SL	0.52 + 0.027*SL	0.56 + 0.024*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
G to QN	t_{PLH}	0.76	0.65 + 0.054*SL	0.66 + 0.051*SL	0.67 + 0.050*SL
	t_{PHL}	0.66	0.59 + 0.035*SL	0.62 + 0.027*SL	0.65 + 0.024*SL
	t_R	0.36	0.15 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.20	0.11 + 0.046*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
SN to QN	t_{PLH}	0.41	0.30 + 0.055*SL	0.31 + 0.051*SL	0.32 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.040*SL	0.13 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

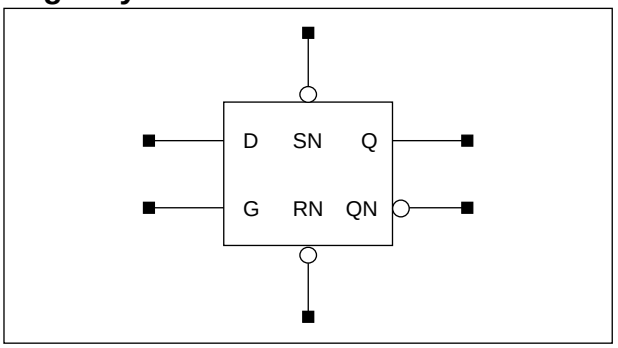
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.79	0.75 + 0.023*SL	0.75 + 0.024*SL	0.74 + 0.025*SL
	t_{PHL}	0.99	0.95 + 0.018*SL	0.96 + 0.015*SL	0.98 + 0.012*SL
	t_R	0.24	0.13 + 0.051*SL	0.13 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
G to Q	t_{PLH}	0.89	0.84 + 0.023*SL	0.84 + 0.024*SL	0.83 + 0.025*SL
	t_{PHL}	0.93	0.90 + 0.018*SL	0.91 + 0.015*SL	0.93 + 0.012*SL
	t_R	0.23	0.13 + 0.050*SL	0.13 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
SN to Q	t_{PLH}	0.77	0.71 + 0.028*SL	0.72 + 0.025*SL	0.73 + 0.024*SL
	t_{PHL}	0.57	0.54 + 0.019*SL	0.55 + 0.015*SL	0.57 + 0.012*SL
	t_R	0.27	0.16 + 0.053*SL	0.17 + 0.051*SL	0.15 + 0.053*SL
	t_F	0.17	0.13 + 0.022*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
D to QN	t_{PLH}	0.81	0.75 + 0.030*SL	0.76 + 0.026*SL	0.77 + 0.025*SL
	t_{PHL}	0.58	0.53 + 0.022*SL	0.55 + 0.016*SL	0.58 + 0.013*SL
	t_R	0.27	0.16 + 0.053*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.17	0.13 + 0.024*SL	0.13 + 0.021*SL	0.15 + 0.020*SL
G to QN	t_{PLH}	0.76	0.70 + 0.030*SL	0.71 + 0.026*SL	0.72 + 0.025*SL
	t_{PHL}	0.67	0.63 + 0.022*SL	0.64 + 0.016*SL	0.67 + 0.013*SL
	t_R	0.27	0.16 + 0.054*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.17	0.13 + 0.024*SL	0.13 + 0.021*SL	0.15 + 0.020*SL
SN to QN	t_{PLH}	0.40	0.34 + 0.030*SL	0.35 + 0.026*SL	0.36 + 0.025*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.42 + 0.016*SL	0.45 + 0.013*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.14 + 0.024*SL	0.15 + 0.020*SL	0.16 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



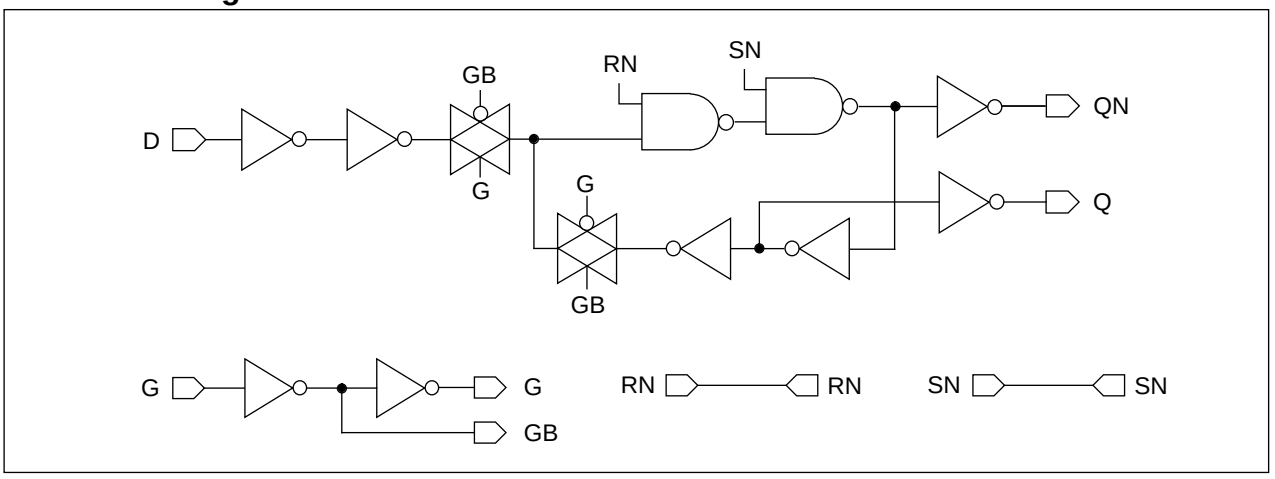
Truth Table

D	G	RN	SN	Q (n+1)	QN (n+1)
0	1	1	1	0	1
1	1	1	1	1	0
x	0	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
LD4				*LD4D2*				*LD4*	*LD4D2*
D	G	SN	RN	D	G	SN	RN		
0.8	0.8	0.7	0.8	0.8	0.8	0.7	0.8	7.0	8.0
KGM80									
LD4				*LD4D2*				*LD4*	*LD4D2*
D	G	SN	RN	D	G	SN	RN		
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD4	LD4D2	LD4	LD4D2
Pulse Width High (G)	t_{PWH}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to G)	t_{SU}	0.42	0.45	0.77	0.80
Input Hold Time (D to G)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to G)	t_{HD}	0.15	0.15	0.41	0.41
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to G)	t_{HD}	0.31	0.26	0.63	0.63

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.73	0.65 + 0.040*SL	0.65 + 0.041*SL	0.65 + 0.042*SL
	t_{PHL}	0.77	0.71 + 0.030*SL	0.73 + 0.025*SL	0.74 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.041*SL
G to Q	t_{PLH}	0.70	0.62 + 0.041*SL	0.62 + 0.041*SL	0.62 + 0.042*SL
	t_{PHL}	0.69	0.63 + 0.031*SL	0.64 + 0.025*SL	0.65 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.042*SL	0.09 + 0.040*SL	0.07 + 0.041*SL
SN to Q	t_{PLH}	0.47	0.38 + 0.040*SL	0.38 + 0.041*SL	0.38 + 0.042*SL
	t_{PHL}	0.37	0.31 + 0.030*SL	0.33 + 0.025*SL	0.34 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.07 + 0.041*SL
RN to Q	t_{PLH}	0.48	0.40 + 0.041*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_{PHL}	0.56	0.51 + 0.027*SL	0.51 + 0.025*SL	0.52 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.70	0.61 + 0.044*SL	0.62 + 0.042*SL	0.62 + 0.042*SL
	t_{PHL}	0.61	0.54 + 0.031*SL	0.56 + 0.026*SL	0.57 + 0.024*SL
	t_R	0.28	0.10 + 0.086*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.044*SL	0.09 + 0.039*SL	0.08 + 0.041*SL
G to QN	t_{PLH}	0.62	0.53 + 0.045*SL	0.53 + 0.042*SL	0.54 + 0.042*SL
	t_{PHL}	0.57	0.51 + 0.031*SL	0.52 + 0.026*SL	0.54 + 0.023*SL
	t_R	0.28	0.10 + 0.086*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.043*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
SN to QN	t_{PLH}	0.30	0.21 + 0.044*SL	0.22 + 0.042*SL	0.22 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
RN to QN	t_{PLH}	0.49	0.41 + 0.042*SL	0.40 + 0.042*SL	0.41 + 0.042*SL
	t_{PHL}	0.35	0.29 + 0.031*SL	0.30 + 0.026*SL	0.32 + 0.024*SL
	t_R	0.28	0.10 + 0.088*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.043*SL	0.09 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.76	0.72 + 0.019*SL	0.72 + 0.020*SL	0.71 + 0.021*SL
	t_{PHL}	0.81	0.78 + 0.017*SL	0.79 + 0.014*SL	0.80 + 0.012*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.019*SL
G to Q	t_{PLH}	0.73	0.69 + 0.020*SL	0.69 + 0.020*SL	0.68 + 0.021*SL
	t_{PHL}	0.73	0.69 + 0.018*SL	0.70 + 0.014*SL	0.72 + 0.012*SL
	t_R	0.18	0.10 + 0.041*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.019*SL
SN to Q	t_{PLH}	0.49	0.45 + 0.019*SL	0.45 + 0.020*SL	0.44 + 0.021*SL
	t_{PHL}	0.41	0.38 + 0.018*SL	0.39 + 0.014*SL	0.39 + 0.013*SL
	t_R	0.18	0.10 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.15	0.11 + 0.018*SL	0.11 + 0.020*SL	0.11 + 0.019*SL
RN to Q	t_{PLH}	0.50	0.46 + 0.019*SL	0.46 + 0.020*SL	0.46 + 0.021*SL
	t_{PHL}	0.60	0.57 + 0.016*SL	0.57 + 0.014*SL	0.59 + 0.012*SL
	t_R	0.18	0.10 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.020*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
D to QN	t_{PLH}	0.69	0.65 + 0.024*SL	0.65 + 0.022*SL	0.65 + 0.021*SL
	t_{PHL}	0.61	0.57 + 0.019*SL	0.58 + 0.015*SL	0.59 + 0.013*SL
	t_R	0.20	0.12 + 0.042*SL	0.11 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.021*SL	0.11 + 0.019*SL
G to QN	t_{PLH}	0.61	0.56 + 0.024*SL	0.56 + 0.022*SL	0.57 + 0.021*SL
	t_{PHL}	0.57	0.53 + 0.019*SL	0.54 + 0.015*SL	0.56 + 0.013*SL
	t_R	0.20	0.11 + 0.043*SL	0.11 + 0.044*SL	0.10 + 0.045*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.11 + 0.020*SL
SN to QN	t_{PLH}	0.29	0.24 + 0.025*SL	0.25 + 0.021*SL	0.25 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.021*SL	0.30 + 0.016*SL	0.32 + 0.014*SL
	t_R	0.20	0.12 + 0.040*SL	0.11 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.16	0.12 + 0.022*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
RN to QN	t_{PLH}	0.48	0.43 + 0.024*SL	0.44 + 0.022*SL	0.45 + 0.021*SL
	t_{PHL}	0.35	0.31 + 0.019*SL	0.32 + 0.015*SL	0.33 + 0.013*SL
	t_R	0.20	0.12 + 0.043*SL	0.11 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	1.08	0.98 + 0.050*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	1.07	1.00 + 0.033*SL	1.02 + 0.026*SL	1.05 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
G to Q	t_{PLH}	1.02	0.92 + 0.050*SL	0.92 + 0.050*SL	0.92 + 0.050*SL
	t_{PHL}	0.99	0.92 + 0.033*SL	0.94 + 0.026*SL	0.97 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.042*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
SN to Q	t_{PLH}	0.62	0.52 + 0.049*SL	0.52 + 0.050*SL	0.52 + 0.050*SL
	t_{PHL}	0.52	0.45 + 0.033*SL	0.47 + 0.026*SL	0.50 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
RN to Q	t_{PLH}	0.67	0.57 + 0.050*SL	0.57 + 0.050*SL	0.58 + 0.050*SL
	t_{PHL}	0.77	0.70 + 0.032*SL	0.72 + 0.026*SL	0.74 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D to QN	t_{PLH}	0.96	0.85 + 0.054*SL	0.86 + 0.051*SL	0.87 + 0.050*SL
	t_{PHL}	0.90	0.83 + 0.035*SL	0.85 + 0.027*SL	0.88 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
G to QN	t_{PLH}	0.88	0.77 + 0.054*SL	0.78 + 0.051*SL	0.79 + 0.050*SL
	t_{PHL}	0.84	0.77 + 0.035*SL	0.79 + 0.027*SL	0.83 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
SN to QN	t_{PLH}	0.41	0.30 + 0.054*SL	0.31 + 0.051*SL	0.32 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
RN to QN	t_{PLH}	0.66	0.55 + 0.054*SL	0.56 + 0.051*SL	0.57 + 0.050*SL
	t_{PHL}	0.49	0.43 + 0.035*SL	0.45 + 0.027*SL	0.48 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD4D2

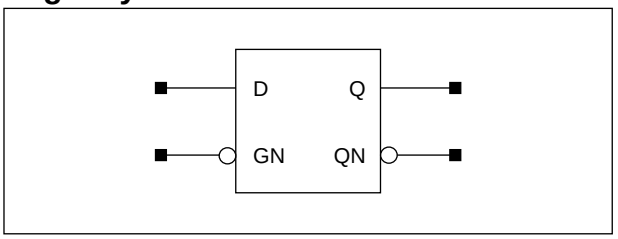
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	1.12	1.07 + 0.023*SL	1.07 + 0.024*SL	1.06 + 0.025*SL
	t_{PHL}	1.13	1.09 + 0.019*SL	1.10 + 0.015*SL	1.13 + 0.013*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.17	0.13 + 0.024*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
G to Q	t_{PLH}	1.06	1.01 + 0.024*SL	1.01 + 0.024*SL	1.01 + 0.025*SL
	t_{PHL}	1.05	1.01 + 0.019*SL	1.02 + 0.015*SL	1.05 + 0.013*SL
	t_R	0.24	0.13 + 0.052*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.17	0.13 + 0.024*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
SN to Q	t_{PLH}	0.66	0.62 + 0.023*SL	0.62 + 0.024*SL	0.61 + 0.025*SL
	t_{PHL}	0.58	0.54 + 0.019*SL	0.55 + 0.015*SL	0.58 + 0.012*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
RN to Q	t_{PLH}	0.72	0.67 + 0.023*SL	0.67 + 0.024*SL	0.66 + 0.025*SL
	t_{PHL}	0.83	0.79 + 0.019*SL	0.80 + 0.015*SL	0.83 + 0.013*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.17	0.13 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
D to QN	t_{PLH}	0.95	0.89 + 0.030*SL	0.90 + 0.026*SL	0.91 + 0.025*SL
	t_{PHL}	0.90	0.86 + 0.022*SL	0.88 + 0.016*SL	0.91 + 0.013*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.053*SL	0.15 + 0.053*SL
	t_F	0.17	0.13 + 0.025*SL	0.13 + 0.021*SL	0.15 + 0.020*SL
G to QN	t_{PLH}	0.86	0.80 + 0.030*SL	0.81 + 0.026*SL	0.83 + 0.025*SL
	t_{PHL}	0.85	0.80 + 0.021*SL	0.82 + 0.016*SL	0.85 + 0.013*SL
	t_R	0.26	0.16 + 0.053*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.17	0.13 + 0.023*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
SN to QN	t_{PLH}	0.39	0.33 + 0.030*SL	0.34 + 0.026*SL	0.36 + 0.025*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.42 + 0.017*SL	0.45 + 0.013*SL
	t_R	0.26	0.16 + 0.053*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.15 + 0.024*SL	0.15 + 0.021*SL	0.17 + 0.020*SL
RN to QN	t_{PLH}	0.65	0.59 + 0.030*SL	0.60 + 0.026*SL	0.61 + 0.025*SL
	t_{PHL}	0.50	0.46 + 0.022*SL	0.47 + 0.016*SL	0.51 + 0.013*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.053*SL	0.15 + 0.053*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

LD5/LD5D2

D Latch with Active Low, 1X/2X Drive

Logic Symbol



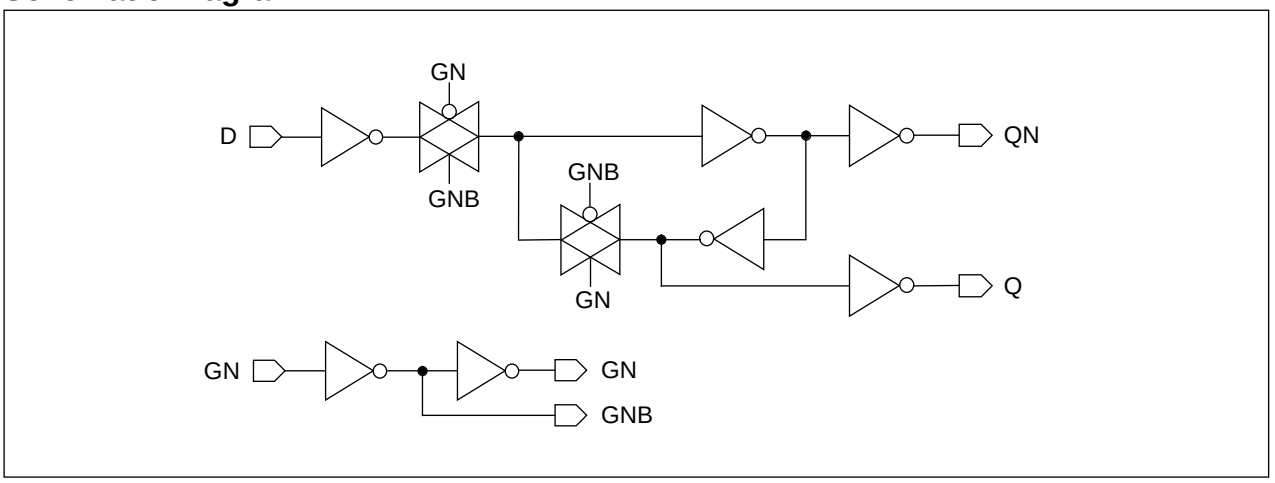
Truth Table

D	GN	Q (n+1)	QN (n+1)
0	0	0	1
1	0	1	0
x	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
LD5		*LD5D2*		*LD5*	*LD5D2*
D	GN	D	GN		
0.9	0.9	0.9	0.9	5.0	6.0
KGM80					
LD5		*LD5D2*		*LD5*	*LD5D2*
D	GN	D	GN		
1.0	1.0	1.0	1.0	5.0	6.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD5	LD5D2	LD5	LD5D2
Pulse Width Low (GN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to GN)	t_{SU}	0.37	0.39	0.68	0.71
Input Hold Time (D to GN)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.54	0.46 + 0.040*SL	0.45 + 0.041*SL	0.45 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.56 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
GN to Q	t_{PLH}	0.66	0.58 + 0.040*SL	0.58 + 0.041*SL	0.58 + 0.042*SL
	t_{PHL}	0.66	0.60 + 0.029*SL	0.61 + 0.024*SL	0.62 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.042*SL	0.44 + 0.042*SL
	t_{PHL}	0.40	0.34 + 0.030*SL	0.35 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.039*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
GN to QN	t_{PLH}	0.58	0.50 + 0.042*SL	0.50 + 0.041*SL	0.49 + 0.042*SL
	t_{PHL}	0.53	0.46 + 0.031*SL	0.48 + 0.026*SL	0.49 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.042*SL

KG80 LD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.57	0.53 + 0.019*SL	0.53 + 0.019*SL	0.52 + 0.020*SL
	t_{PHL}	0.63	0.60 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.16	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.020*SL	0.09 + 0.020*SL
GN to Q	t_{PLH}	0.69	0.65 + 0.019*SL	0.65 + 0.019*SL	0.64 + 0.020*SL
	t_{PHL}	0.69	0.66 + 0.018*SL	0.67 + 0.015*SL	0.68 + 0.013*SL
	t_R	0.16	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.020*SL	0.09 + 0.020*SL
D to QN	t_{PLH}	0.50	0.46 + 0.023*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.020*SL	0.37 + 0.015*SL	0.39 + 0.013*SL
	t_R	0.17	0.09 + 0.039*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
GN to QN	t_{PLH}	0.56	0.52 + 0.023*SL	0.52 + 0.021*SL	0.52 + 0.021*SL
	t_{PHL}	0.52	0.48 + 0.021*SL	0.50 + 0.015*SL	0.51 + 0.013*SL
	t_R	0.17	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

LD5/LD5D2

D Latch with Active Low, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD5

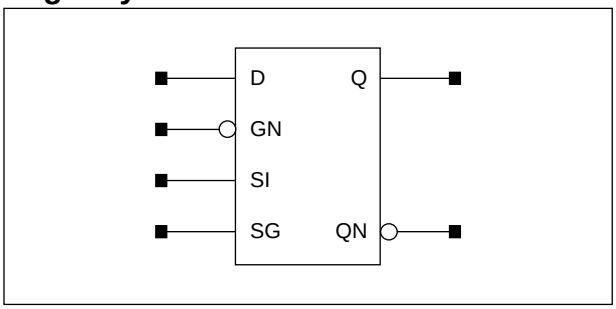
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.74	0.64 + 0.049*SL	0.64 + 0.050*SL	0.64 + 0.050*SL
	t_{PHL}	0.83	0.77 + 0.033*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
GN to Q	t_{PLH}	0.90	0.80 + 0.049*SL	0.80 + 0.050*SL	0.80 + 0.050*SL
	t_{PHL}	0.92	0.85 + 0.033*SL	0.87 + 0.026*SL	0.90 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D to QN	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.50 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
GN to QN	t_{PLH}	0.80	0.70 + 0.051*SL	0.70 + 0.050*SL	0.70 + 0.050*SL
	t_{PHL}	0.71	0.64 + 0.034*SL	0.66 + 0.026*SL	0.69 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

KGM80 LD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.79	0.74 + 0.025*SL	0.74 + 0.024*SL	0.73 + 0.025*SL
	t_{PHL}	0.89	0.85 + 0.021*SL	0.86 + 0.016*SL	0.89 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
GN to Q	t_{PLH}	0.95	0.90 + 0.025*SL	0.90 + 0.024*SL	0.89 + 0.025*SL
	t_{PHL}	0.97	0.93 + 0.021*SL	0.95 + 0.016*SL	0.98 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.026*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
D to QN	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.51 + 0.023*SL	0.53 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
GN to QN	t_{PLH}	0.77	0.72 + 0.028*SL	0.72 + 0.025*SL	0.73 + 0.025*SL
	t_{PHL}	0.71	0.67 + 0.023*SL	0.68 + 0.016*SL	0.72 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



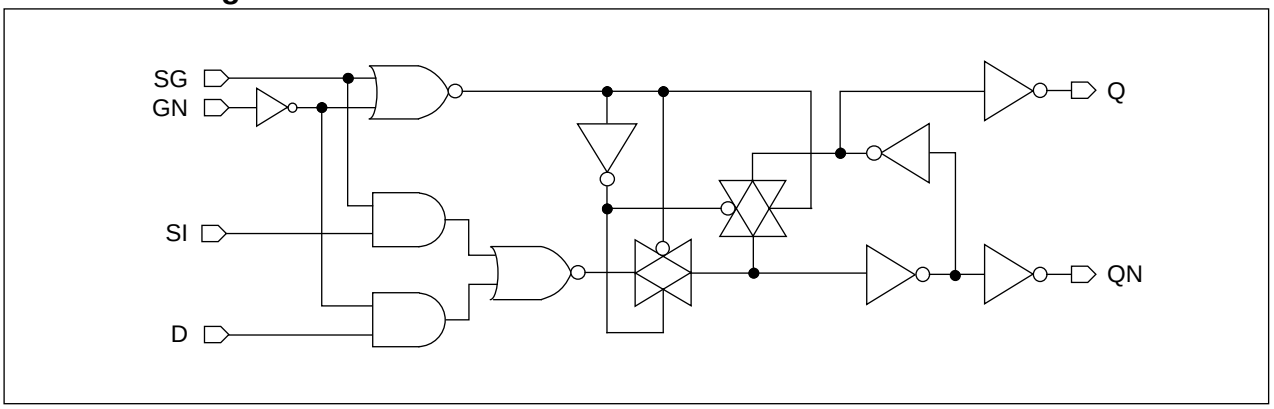
Truth Table

D	GN	SI	SG	Q (n+1)	QN (n+1)
x	1	x	0	Q (n)	QN (n)
x	x	1	1	1	0
x	1	0	1	0	1
1	0	x	x	1	0
0	0	x	0	0	1
0	0	0	1	0	1

Cell Data

Input Load (SL)								Gate Count	
KG80									
LD5S				*LD5SD2*				*LD5S*	*LD5SD2*
D	GN	SI	SG	D	GN	SI	SG		
0.6	0.9	0.8	1.8	0.6	0.9	0.8	1.8	7.0	8.0
KGM80									
LD5S				*LD5SD2*				*LD5S*	*LD5SD2*
D	GN	SI	SG	D	GN	SI	SG		
1.0	1.1	1.0	2.1	1.0	1.1	1.0	2.1	7.0	8.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD5S	LD5SD2	LD5S	LD5SD2
Pulse Width Low (GN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width High (SG)	t_{PWH}	0.61	0.61	0.99	0.99
Input Setup Time (D to GN)	t_{SU}	0.37	0.39	0.68	0.74
Input Hold Time (D to GN)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (SI to SG)	t_{SU}	0.37	0.39	0.68	0.74
Input Hold Time (SI to SG)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.63	0.55 + 0.040*SL	0.54 + 0.041*SL	0.54 + 0.042*SL
	t_{PHL}	0.67	0.61 + 0.029*SL	0.62 + 0.025*SL	0.63 + 0.023*SL
	t_R	0.26	0.09 + 0.085*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
SI to Q	t_{PLH}	0.70	0.62 + 0.040*SL	0.62 + 0.041*SL	0.62 + 0.042*SL
	t_{PHL}	0.71	0.66 + 0.030*SL	0.67 + 0.025*SL	0.68 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
GN to Q	t_{PLH}	0.86	0.78 + 0.040*SL	0.77 + 0.041*SL	0.77 + 0.042*SL
	t_{PHL}	0.76	0.70 + 0.030*SL	0.71 + 0.025*SL	0.72 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
SG to Q	t_{PLH}	0.72	0.64 + 0.040*SL	0.63 + 0.041*SL	0.63 + 0.042*SL
	t_{PHL}	0.57	0.51 + 0.029*SL	0.52 + 0.025*SL	0.53 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.59	0.51 + 0.042*SL	0.51 + 0.041*SL	0.51 + 0.042*SL
	t_{PHL}	0.49	0.43 + 0.031*SL	0.44 + 0.026*SL	0.46 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.040*SL	0.09 + 0.041*SL
SI to QN	t_{PLH}	0.64	0.55 + 0.042*SL	0.56 + 0.041*SL	0.56 + 0.041*SL
	t_{PHL}	0.57	0.50 + 0.031*SL	0.52 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
GN to QN	t_{PLH}	0.68	0.60 + 0.042*SL	0.60 + 0.042*SL	0.60 + 0.042*SL
	t_{PHL}	0.72	0.66 + 0.030*SL	0.67 + 0.026*SL	0.69 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.039*SL	0.08 + 0.041*SL
SG to QN	t_{PLH}	0.50	0.41 + 0.042*SL	0.41 + 0.042*SL	0.41 + 0.042*SL
	t_{PHL}	0.58	0.52 + 0.031*SL	0.53 + 0.026*SL	0.55 + 0.023*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.18	0.09 + 0.041*SL	0.10 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.66	0.62 + 0.020*SL	0.62 + 0.019*SL	0.61 + 0.020*SL
	t_{PHL}	0.71	0.67 + 0.018*SL	0.68 + 0.015*SL	0.69 + 0.013*SL
	t_R	0.16	0.09 + 0.038*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.023*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
SI to Q	t_{PLH}	0.73	0.69 + 0.019*SL	0.69 + 0.019*SL	0.69 + 0.020*SL
	t_{PHL}	0.76	0.72 + 0.018*SL	0.73 + 0.015*SL	0.74 + 0.013*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.10 + 0.020*SL	0.09 + 0.020*SL
GN to Q	t_{PLH}	0.89	0.85 + 0.019*SL	0.85 + 0.019*SL	0.84 + 0.020*SL
	t_{PHL}	0.79	0.76 + 0.018*SL	0.76 + 0.015*SL	0.78 + 0.013*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.023*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
SG to Q	t_{PLH}	0.75	0.71 + 0.019*SL	0.71 + 0.019*SL	0.70 + 0.020*SL
	t_{PHL}	0.61	0.57 + 0.018*SL	0.58 + 0.015*SL	0.59 + 0.013*SL
	t_R	0.17	0.09 + 0.039*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
D to QN	t_{PLH}	0.58	0.53 + 0.023*SL	0.54 + 0.021*SL	0.54 + 0.021*SL
	t_{PHL}	0.49	0.45 + 0.020*SL	0.46 + 0.015*SL	0.47 + 0.014*SL
	t_R	0.17	0.10 + 0.037*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.11 + 0.020*SL
SI to QN	t_{PLH}	0.62	0.58 + 0.023*SL	0.58 + 0.021*SL	0.58 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.021*SL	0.54 + 0.015*SL	0.55 + 0.013*SL
	t_R	0.18	0.10 + 0.039*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.15	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
GN to QN	t_{PLH}	0.66	0.62 + 0.023*SL	0.62 + 0.021*SL	0.62 + 0.021*SL
	t_{PHL}	0.72	0.68 + 0.021*SL	0.69 + 0.015*SL	0.71 + 0.013*SL
	t_R	0.17	0.09 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.11 + 0.020*SL
SG to QN	t_{PLH}	0.48	0.43 + 0.023*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.58	0.54 + 0.020*SL	0.55 + 0.016*SL	0.57 + 0.013*SL
	t_R	0.17	0.08 + 0.043*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.11 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.87	0.77 + 0.049*SL	0.77 + 0.050*SL	0.77 + 0.050*SL
	t_{PHL}	0.97	0.90 + 0.033*SL	0.92 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.044*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
SI to Q	t_{PLH}	0.97	0.87 + 0.049*SL	0.87 + 0.050*SL	0.87 + 0.050*SL
	t_{PHL}	1.07	1.00 + 0.033*SL	1.02 + 0.026*SL	1.05 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
GN to Q	t_{PLH}	1.19	1.09 + 0.049*SL	1.08 + 0.050*SL	1.08 + 0.050*SL
	t_{PHL}	1.06	0.99 + 0.032*SL	1.01 + 0.026*SL	1.04 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
SG to Q	t_{PLH}	1.00	0.90 + 0.049*SL	0.90 + 0.050*SL	0.90 + 0.050*SL
	t_{PHL}	0.81	0.75 + 0.033*SL	0.77 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D to QN	t_{PLH}	0.85	0.75 + 0.051*SL	0.75 + 0.050*SL	0.75 + 0.050*SL
	t_{PHL}	0.68	0.61 + 0.034*SL	0.63 + 0.026*SL	0.66 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
SI to QN	t_{PLH}	0.95	0.85 + 0.051*SL	0.85 + 0.050*SL	0.85 + 0.050*SL
	t_{PHL}	0.77	0.70 + 0.035*SL	0.73 + 0.026*SL	0.76 + 0.023*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
GN to QN	t_{PLH}	0.94	0.84 + 0.051*SL	0.84 + 0.050*SL	0.84 + 0.050*SL
	t_{PHL}	0.99	0.92 + 0.034*SL	0.94 + 0.026*SL	0.98 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
SG to QN	t_{PLH}	0.69	0.59 + 0.051*SL	0.59 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.76 + 0.026*SL	0.79 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD5SD2

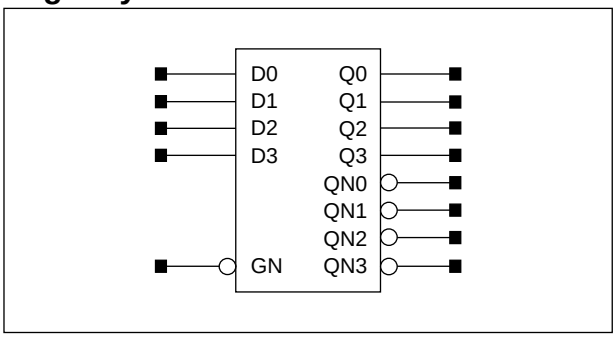
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.92	0.87 + 0.024*SL	0.87 + 0.024*SL	0.86 + 0.025*SL
	t_{PHL}	1.03	0.99 + 0.021*SL	1.01 + 0.016*SL	1.03 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
SI to Q	t_{PLH}	1.01	0.97 + 0.024*SL	0.97 + 0.024*SL	0.96 + 0.025*SL
	t_{PHL}	1.13	1.09 + 0.021*SL	1.11 + 0.016*SL	1.14 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
GN to Q	t_{PLH}	1.23	1.18 + 0.024*SL	1.19 + 0.024*SL	1.18 + 0.025*SL
	t_{PHL}	1.11	1.07 + 0.021*SL	1.09 + 0.016*SL	1.12 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
SG to Q	t_{PLH}	1.04	1.00 + 0.024*SL	1.00 + 0.024*SL	0.99 + 0.025*SL
	t_{PHL}	0.87	0.83 + 0.021*SL	0.84 + 0.016*SL	0.87 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
D to QN	t_{PLH}	0.83	0.77 + 0.029*SL	0.78 + 0.025*SL	0.79 + 0.025*SL
	t_{PHL}	0.68	0.64 + 0.023*SL	0.66 + 0.017*SL	0.69 + 0.013*SL
	t_R	0.23	0.13 + 0.050*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
SI to QN	t_{PLH}	0.93	0.88 + 0.029*SL	0.88 + 0.025*SL	0.89 + 0.025*SL
	t_{PHL}	0.78	0.73 + 0.024*SL	0.75 + 0.017*SL	0.79 + 0.013*SL
	t_R	0.23	0.13 + 0.050*SL	0.12 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
GN to QN	t_{PLH}	0.91	0.86 + 0.028*SL	0.87 + 0.025*SL	0.87 + 0.025*SL
	t_{PHL}	1.00	0.95 + 0.024*SL	0.97 + 0.017*SL	1.00 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
SG to QN	t_{PLH}	0.67	0.61 + 0.028*SL	0.62 + 0.025*SL	0.62 + 0.025*SL
	t_{PHL}	0.81	0.76 + 0.024*SL	0.78 + 0.017*SL	0.82 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

LD5X4/LD5XD2

4-Bit D Latch with Active Low, 1X/2X Drive

Logic Symbol



Truth Table

Dn	GN	Qn (n+1)	QNn (n+1)
0	0	0	1
1	0	1	0
x	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count	
KG80					
LD5X4		*LD5X4D2*		*LD5X4*	*LD5X4D2*
Dn	GN	Dn	GN		
1.0	0.9	1.0	0.9	15.0	19.0
KGM80					
LD5X4		*LD5X4D2*		*LD5X4*	*LD5X4D2*
Dn	GN	Dn	GN		
1.0	1.1	1.0	1.1	15.0	19.0

Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD5X4	LD5X4D2	LD5X4	LD5X4D2
Pulse Width Low (GN)	t_{PWL}	0.61	0.64	1.02	1.05
Input Setup Time (D0 to GN)	t_{SU}	0.26	0.28	0.52	0.55
Input Hold Time (D0 to GN)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (D1 to GN)	t_{SU}	0.26	0.28	0.52	0.55
Input Hold Time (D1 to GN)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (D2 to GN)	t_{SU}	0.26	0.28	0.52	0.55
Input Hold Time (D2 to GN)	t_{HD}	0.15	0.15	0.33	0.33
Input Setup Time (D3 to GN)	t_{SU}	0.26	0.28	0.52	0.55
Input Hold Time (D3 to GN)	t_{HD}	0.15	0.15	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.54	0.46 + 0.040*SL	0.46 + 0.041*SL	0.45 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.56 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
GN to Q0	t_{PLH}	0.77	0.69 + 0.040*SL	0.69 + 0.041*SL	0.68 + 0.042*SL
	t_{PHL}	0.85	0.79 + 0.030*SL	0.80 + 0.025*SL	0.81 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D1 to Q1	t_{PLH}	0.55	0.46 + 0.040*SL	0.46 + 0.041*SL	0.46 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.56 + 0.023*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
GN to Q1	t_{PLH}	0.78	0.70 + 0.040*SL	0.69 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.85	0.79 + 0.029*SL	0.80 + 0.025*SL	0.81 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.08 + 0.040*SL	0.08 + 0.040*SL	0.08 + 0.042*SL
D2 to Q2	t_{PLH}	0.54	0.46 + 0.040*SL	0.46 + 0.041*SL	0.46 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.56 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
GN to Q2	t_{PLH}	0.77	0.69 + 0.041*SL	0.69 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.85	0.79 + 0.029*SL	0.80 + 0.025*SL	0.81 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D3 to Q3	t_{PLH}	0.54	0.46 + 0.040*SL	0.45 + 0.041*SL	0.45 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.025*SL	0.56 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
GN to Q3	t_{PLH}	0.77	0.69 + 0.040*SL	0.69 + 0.041*SL	0.68 + 0.042*SL
	t_{PHL}	0.84	0.79 + 0.029*SL	0.80 + 0.025*SL	0.81 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
D0 to QN0	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.031*SL	0.36 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.039*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
GN to QN0	t_{PLH}	0.77	0.69 + 0.042*SL	0.69 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.031*SL	0.59 + 0.026*SL	0.60 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.042*SL	0.44 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.031*SL	0.36 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.27	0.11 + 0.084*SL	0.09 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
GN to QN1	t_{PLH}	0.77	0.69 + 0.041*SL	0.69 + 0.042*SL	0.69 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.031*SL	0.59 + 0.026*SL	0.60 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
D2 to QN2	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.031*SL	0.36 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
GN to QN2	t_{PLH}	0.77	0.69 + 0.042*SL	0.69 + 0.042*SL	0.69 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.030*SL	0.59 + 0.026*SL	0.60 + 0.023*SL
	t_R	0.27	0.11 + 0.084*SL	0.09 + 0.089*SL	0.09 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
D3 to QN3	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.031*SL	0.36 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.039*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
GN to QN3	t_{PLH}	0.77	0.69 + 0.042*SL	0.69 + 0.041*SL	0.69 + 0.042*SL
	t_{PHL}	0.64	0.58 + 0.031*SL	0.59 + 0.026*SL	0.60 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD5X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.57	0.52 + 0.020*SL	0.53 + 0.019*SL	0.52 + 0.020*SL
	t_{PHL}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.61 + 0.013*SL
	t_R	0.16	0.09 + 0.039*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
GN to Q0	t_{PLH}	0.80	0.76 + 0.019*SL	0.76 + 0.019*SL	0.75 + 0.020*SL
	t_{PHL}	0.88	0.85 + 0.018*SL	0.86 + 0.015*SL	0.87 + 0.013*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
D1 to Q1	t_{PLH}	0.57	0.52 + 0.025*SL	0.53 + 0.019*SL	0.53 + 0.020*SL
	t_{PHL}	0.64	0.60 + 0.018*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.17	0.10 + 0.036*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
GN to Q1	t_{PLH}	0.81	0.77 + 0.019*SL	0.77 + 0.019*SL	0.76 + 0.020*SL
	t_{PHL}	0.89	0.85 + 0.018*SL	0.86 + 0.015*SL	0.88 + 0.013*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
D2 to Q2	t_{PLH}	0.58	0.54 + 0.019*SL	0.54 + 0.019*SL	0.54 + 0.020*SL
	t_{PHL}	0.65	0.61 + 0.017*SL	0.62 + 0.014*SL	0.63 + 0.013*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
GN to Q2	t_{PLH}	0.82	0.78 + 0.018*SL	0.78 + 0.019*SL	0.77 + 0.020*SL
	t_{PHL}	0.90	0.87 + 0.018*SL	0.87 + 0.014*SL	0.89 + 0.013*SL
	t_R	0.19	0.11 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.10 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
D3 to Q3	t_{PLH}	0.56	0.53 + 0.020*SL	0.53 + 0.019*SL	0.52 + 0.020*SL
	t_{PHL}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.16	0.08 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.022*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
GN to Q3	t_{PLH}	0.80	0.76 + 0.019*SL	0.76 + 0.019*SL	0.75 + 0.020*SL
	t_{PHL}	0.88	0.85 + 0.018*SL	0.86 + 0.015*SL	0.87 + 0.013*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.020*SL	0.09 + 0.020*SL
D0 to QN0	t_{PLH}	0.50	0.45 + 0.023*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.020*SL	0.37 + 0.015*SL	0.38 + 0.014*SL
	t_R	0.17	0.09 + 0.039*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
GN to QN0	t_{PLH}	0.75	0.71 + 0.023*SL	0.71 + 0.021*SL	0.71 + 0.021*SL
	t_{PHL}	0.64	0.59 + 0.021*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.17	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD5X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.50	0.46 + 0.022*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.023*SL	0.37 + 0.015*SL	0.39 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.11 + 0.017*SL	0.10 + 0.020*SL	0.11 + 0.020*SL
GN to QN1	t_{PLH}	0.76	0.71 + 0.023*SL	0.71 + 0.021*SL	0.71 + 0.021*SL
	t_{PHL}	0.64	0.60 + 0.020*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.023*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
D2 to QN2	t_{PLH}	0.50	0.46 + 0.022*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.020*SL	0.37 + 0.015*SL	0.39 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.020*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
GN to QN2	t_{PLH}	0.76	0.71 + 0.023*SL	0.71 + 0.021*SL	0.71 + 0.021*SL
	t_{PHL}	0.64	0.60 + 0.020*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.023*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
D3 to QN3	t_{PLH}	0.50	0.45 + 0.023*SL	0.46 + 0.021*SL	0.46 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.021*SL	0.37 + 0.015*SL	0.38 + 0.013*SL
	t_R	0.17	0.09 + 0.039*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL
GN to QN3	t_{PLH}	0.75	0.71 + 0.023*SL	0.71 + 0.021*SL	0.71 + 0.021*SL
	t_{PHL}	0.63	0.59 + 0.020*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_R	0.17	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.14	0.09 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.74	0.64 + 0.049*SL	0.64 + 0.050*SL	0.64 + 0.050*SL
	t_{PHL}	0.83	0.77 + 0.032*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
GN to Q0	t_{PLH}	1.07	0.97 + 0.049*SL	0.97 + 0.050*SL	0.97 + 0.050*SL
	t_{PHL}	1.19	1.13 + 0.032*SL	1.15 + 0.026*SL	1.17 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D1 to Q1	t_{PLH}	0.75	0.66 + 0.049*SL	0.65 + 0.050*SL	0.65 + 0.050*SL
	t_{PHL}	0.84	0.78 + 0.032*SL	0.79 + 0.026*SL	0.82 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
GN to Q1	t_{PLH}	1.08	0.98 + 0.049*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	1.20	1.14 + 0.032*SL	1.16 + 0.026*SL	1.18 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.042*SL	0.11 + 0.042*SL
D2 to Q2	t_{PLH}	0.75	0.65 + 0.049*SL	0.65 + 0.050*SL	0.65 + 0.050*SL
	t_{PHL}	0.84	0.77 + 0.033*SL	0.79 + 0.026*SL	0.82 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
GN to Q2	t_{PLH}	1.08	0.98 + 0.049*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	1.20	1.13 + 0.033*SL	1.15 + 0.026*SL	1.18 + 0.023*SL
	t_R	0.34	0.14 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.042*SL	0.11 + 0.042*SL
D3 to Q3	t_{PLH}	0.74	0.64 + 0.049*SL	0.64 + 0.050*SL	0.64 + 0.050*SL
	t_{PHL}	0.83	0.76 + 0.033*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
GN to Q3	t_{PLH}	1.07	0.97 + 0.049*SL	0.97 + 0.050*SL	0.97 + 0.050*SL
	t_{PHL}	1.19	1.13 + 0.032*SL	1.15 + 0.026*SL	1.17 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D0 to QN0	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.50 + 0.026*SL	0.54 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
GN to QN0	t_{PLH}	1.07	0.97 + 0.051*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.88	0.81 + 0.034*SL	0.83 + 0.026*SL	0.86 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.50 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
GN to QN1	t_{PLH}	1.07	0.97 + 0.051*SL	0.97 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.88	0.81 + 0.034*SL	0.83 + 0.026*SL	0.86 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
D2 to QN2	t_{PLH}	0.72	0.61 + 0.051*SL	0.62 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.51 + 0.026*SL	0.54 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.12 + 0.043*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
GN to QN2	t_{PLH}	1.08	0.97 + 0.051*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.88	0.81 + 0.034*SL	0.83 + 0.026*SL	0.86 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
D3 to QN3	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.55	0.48 + 0.034*SL	0.50 + 0.026*SL	0.54 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.042*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
GN to QN3	t_{PLH}	1.07	0.97 + 0.051*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	0.88	0.81 + 0.034*SL	0.83 + 0.026*SL	0.86 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD5X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.78	0.74 + 0.024*SL	0.74 + 0.024*SL	0.73 + 0.025*SL
	t_{PHL}	0.89	0.84 + 0.022*SL	0.86 + 0.016*SL	0.89 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
GN to Q0	t_{PLH}	1.12	1.07 + 0.024*SL	1.07 + 0.024*SL	1.06 + 0.025*SL
	t_{PHL}	1.25	1.21 + 0.021*SL	1.23 + 0.016*SL	1.26 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
D1 to Q1	t_{PLH}	0.79	0.75 + 0.024*SL	0.75 + 0.024*SL	0.74 + 0.025*SL
	t_{PHL}	0.90	0.85 + 0.022*SL	0.87 + 0.016*SL	0.90 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.17	0.11 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
GN to Q1	t_{PLH}	1.13	1.08 + 0.025*SL	1.08 + 0.024*SL	1.07 + 0.025*SL
	t_{PHL}	1.26	1.22 + 0.021*SL	1.24 + 0.016*SL	1.27 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
D2 to Q2	t_{PLH}	0.81	0.76 + 0.023*SL	0.76 + 0.024*SL	0.75 + 0.025*SL
	t_{PHL}	0.91	0.87 + 0.020*SL	0.88 + 0.015*SL	0.91 + 0.013*SL
	t_R	0.25	0.15 + 0.051*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.14 + 0.021*SL
GN to Q2	t_{PLH}	1.14	1.09 + 0.024*SL	1.09 + 0.024*SL	1.09 + 0.025*SL
	t_{PHL}	1.28	1.24 + 0.019*SL	1.25 + 0.015*SL	1.28 + 0.013*SL
	t_R	0.25	0.15 + 0.051*SL	0.14 + 0.053*SL	0.13 + 0.054*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.15 + 0.021*SL
D3 to Q3	t_{PLH}	0.78	0.73 + 0.025*SL	0.74 + 0.024*SL	0.73 + 0.025*SL
	t_{PHL}	0.89	0.84 + 0.021*SL	0.86 + 0.016*SL	0.89 + 0.013*SL
	t_R	0.21	0.11 + 0.051*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
GN to Q3	t_{PLH}	1.11	1.07 + 0.024*SL	1.07 + 0.024*SL	1.06 + 0.025*SL
	t_{PHL}	1.25	1.21 + 0.021*SL	1.23 + 0.016*SL	1.26 + 0.013*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.052*SL	0.09 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
D0 to QN0	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.51 + 0.023*SL	0.52 + 0.017*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.11 + 0.026*SL	0.13 + 0.021*SL	0.14 + 0.020*SL
GN to QN0	t_{PLH}	1.05	1.00 + 0.028*SL	1.00 + 0.025*SL	1.01 + 0.025*SL
	t_{PHL}	0.88	0.84 + 0.023*SL	0.85 + 0.016*SL	0.89 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.13 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

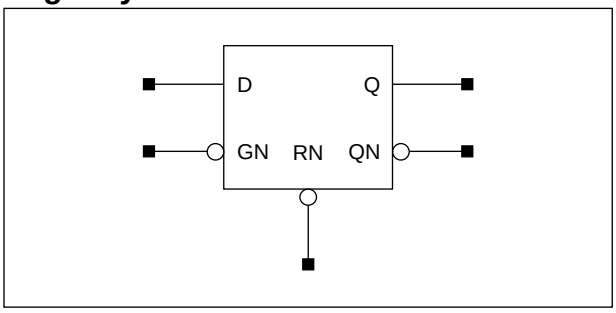
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD5X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.51 + 0.023*SL	0.53 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.049*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.024*SL	0.12 + 0.022*SL	0.14 + 0.021*SL
GN to QN1	t_{PLH}	1.06	1.00 + 0.028*SL	1.01 + 0.025*SL	1.01 + 0.025*SL
	t_{PHL}	0.89	0.84 + 0.023*SL	0.86 + 0.016*SL	0.89 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.12 + 0.022*SL	0.14 + 0.021*SL
D2 to QN2	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.51 + 0.023*SL	0.53 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
GN to QN2	t_{PLH}	1.06	1.00 + 0.028*SL	1.01 + 0.025*SL	1.01 + 0.025*SL
	t_{PHL}	0.89	0.84 + 0.023*SL	0.86 + 0.017*SL	0.89 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.12 + 0.025*SL	0.12 + 0.022*SL	0.14 + 0.021*SL
D3 to QN3	t_{PLH}	0.69	0.63 + 0.028*SL	0.64 + 0.025*SL	0.64 + 0.025*SL
	t_{PHL}	0.55	0.50 + 0.023*SL	0.52 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.22	0.12 + 0.050*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.17	0.11 + 0.026*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
GN to QN3	t_{PLH}	1.05	1.00 + 0.028*SL	1.00 + 0.025*SL	1.01 + 0.025*SL
	t_{PHL}	0.88	0.84 + 0.023*SL	0.85 + 0.017*SL	0.89 + 0.013*SL
	t_R	0.22	0.12 + 0.051*SL	0.11 + 0.053*SL	0.10 + 0.054*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Logic Symbol



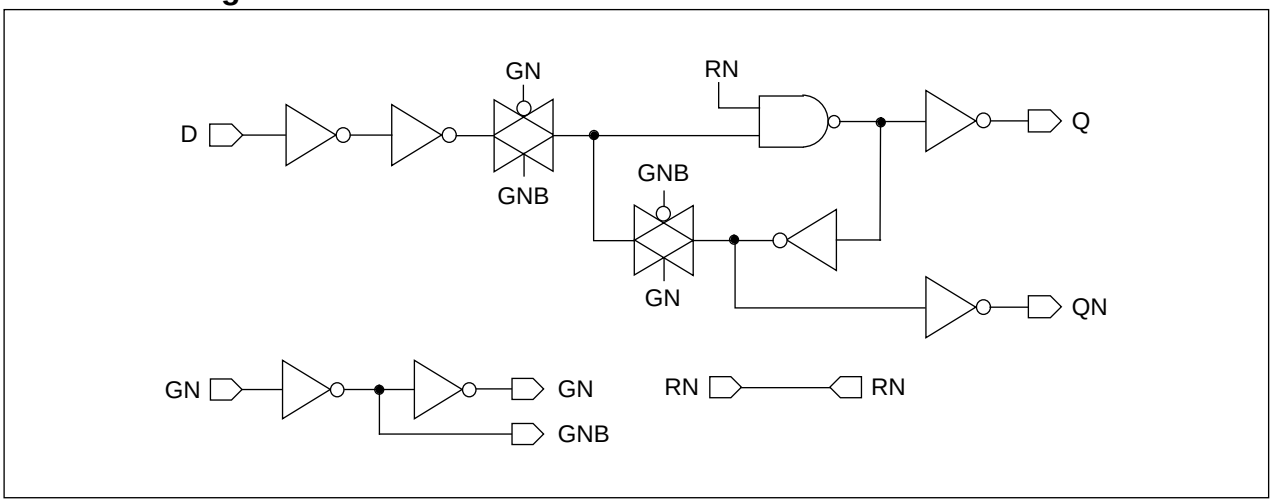
Truth Table

D	GN	RN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
LD6			*LD6D2*			*LD6*	*LD6D2*
D	GN	RN	D	GN	RN		
0.9	0.9	0.5	0.9	0.9	0.5	6.0	7.0
KGM80							
LD6			*LD6D2*			*LD6*	*LD6D2*
D	GN	RN	D	GN	RN		
1.0	1.0	1.0	1.0	1.0	1.0	6.0	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD6	LD6D2	LD6	LD6D2
Pulse Width Low (GN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to GN)	t_{SU}	0.47	0.50	0.80	0.83
Input Hold Time (D to GN)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (RN to GN)	t_{HD}	0.20	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.55	0.46 + 0.044*SL	0.47 + 0.042*SL	0.47 + 0.042*SL
	t_{PHL}	0.58	0.51 + 0.032*SL	0.53 + 0.026*SL	0.54 + 0.024*SL
	t_R	0.28	0.11 + 0.087*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
GN to Q	t_{PLH}	0.63	0.54 + 0.044*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.56	0.49 + 0.032*SL	0.51 + 0.026*SL	0.53 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
RN to Q	t_{PLH}	0.31	0.22 + 0.044*SL	0.22 + 0.042*SL	0.23 + 0.041*SL
	t_{PHL}	0.30	0.24 + 0.030*SL	0.25 + 0.025*SL	0.27 + 0.023*SL
	t_R	0.28	0.11 + 0.087*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.10 + 0.039*SL	0.10 + 0.039*SL	0.08 + 0.041*SL
D to QN	t_{PLH}	0.72	0.64 + 0.040*SL	0.63 + 0.041*SL	0.63 + 0.042*SL
	t_{PHL}	0.63	0.57 + 0.030*SL	0.59 + 0.025*SL	0.60 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.08 + 0.041*SL
GN to QN	t_{PLH}	0.70	0.62 + 0.040*SL	0.61 + 0.041*SL	0.61 + 0.042*SL
	t_{PHL}	0.71	0.65 + 0.030*SL	0.66 + 0.025*SL	0.67 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.16	0.09 + 0.040*SL	0.08 + 0.040*SL	0.08 + 0.041*SL
RN to QN	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.041*SL	0.43 + 0.041*SL
	t_{PHL}	0.39	0.33 + 0.030*SL	0.34 + 0.025*SL	0.35 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.55	0.50 + 0.024*SL	0.50 + 0.022*SL	0.51 + 0.021*SL
	t_{PHL}	0.58	0.54 + 0.020*SL	0.55 + 0.016*SL	0.56 + 0.013*SL
	t_R	0.21	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.16	0.12 + 0.021*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
GN to Q	t_{PLH}	0.62	0.58 + 0.022*SL	0.58 + 0.021*SL	0.58 + 0.021*SL
	t_{PHL}	0.56	0.52 + 0.020*SL	0.53 + 0.015*SL	0.54 + 0.014*SL
	t_R	0.21	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.16	0.11 + 0.021*SL	0.12 + 0.020*SL	0.12 + 0.019*SL
RN to Q	t_{PLH}	0.30	0.26 + 0.022*SL	0.26 + 0.022*SL	0.26 + 0.021*SL
	t_{PHL}	0.30	0.26 + 0.020*SL	0.28 + 0.015*SL	0.29 + 0.013*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.019*SL
D to QN	t_{PLH}	0.75	0.71 + 0.019*SL	0.71 + 0.019*SL	0.70 + 0.020*SL
	t_{PHL}	0.68	0.64 + 0.018*SL	0.65 + 0.014*SL	0.66 + 0.013*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.020*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
GN to QN	t_{PLH}	0.73	0.69 + 0.019*SL	0.69 + 0.019*SL	0.68 + 0.020*SL
	t_{PHL}	0.76	0.73 + 0.015*SL	0.73 + 0.014*SL	0.74 + 0.013*SL
	t_R	0.19	0.10 + 0.042*SL	0.10 + 0.042*SL	0.09 + 0.044*SL
	t_F	0.15	0.11 + 0.020*SL	0.11 + 0.019*SL	0.11 + 0.020*SL
RN to QN	t_{PLH}	0.54	0.50 + 0.022*SL	0.50 + 0.020*SL	0.50 + 0.020*SL
	t_{PHL}	0.43	0.40 + 0.016*SL	0.41 + 0.015*SL	0.42 + 0.013*SL
	t_R	0.20	0.12 + 0.041*SL	0.12 + 0.042*SL	0.11 + 0.043*SL
	t_F	0.15	0.10 + 0.022*SL	0.11 + 0.019*SL	0.11 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.79	0.68 + 0.054*SL	0.69 + 0.051*SL	0.70 + 0.050*SL
	t_{PHL}	0.78	0.71 + 0.035*SL	0.73 + 0.027*SL	0.77 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.14 + 0.108*SL
	t_F	0.21	0.13 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
GN to Q	t_{PLH}	0.87	0.76 + 0.054*SL	0.77 + 0.051*SL	0.78 + 0.050*SL
	t_{PHL}	0.76	0.69 + 0.036*SL	0.71 + 0.027*SL	0.75 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
RN to Q	t_{PLH}	0.40	0.29 + 0.053*SL	0.30 + 0.051*SL	0.31 + 0.050*SL
	t_{PHL}	0.39	0.32 + 0.034*SL	0.34 + 0.026*SL	0.37 + 0.023*SL
	t_R	0.37	0.15 + 0.106*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
D to QN	t_{PLH}	0.98	0.88 + 0.049*SL	0.88 + 0.050*SL	0.88 + 0.050*SL
	t_{PHL}	0.92	0.85 + 0.033*SL	0.87 + 0.026*SL	0.90 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.041*SL	0.11 + 0.042*SL
GN to QN	t_{PLH}	0.96	0.86 + 0.049*SL	0.86 + 0.050*SL	0.86 + 0.050*SL
	t_{PHL}	1.00	0.93 + 0.033*SL	0.95 + 0.026*SL	0.98 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.043*SL	0.11 + 0.041*SL	0.11 + 0.042*SL
RN to QN	t_{PLH}	0.67	0.56 + 0.054*SL	0.57 + 0.050*SL	0.57 + 0.050*SL
	t_{PHL}	0.53	0.46 + 0.033*SL	0.48 + 0.026*SL	0.51 + 0.023*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.106*SL	0.13 + 0.108*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD6D2

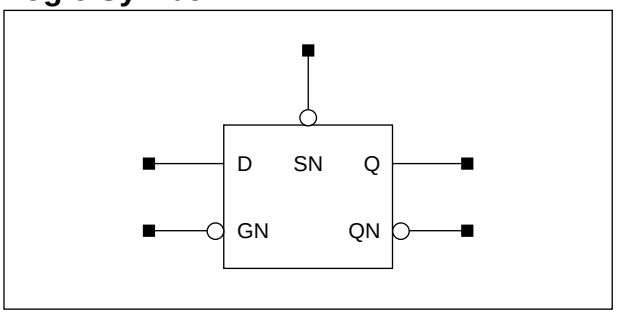
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.79	0.73 + 0.030*SL	0.74 + 0.026*SL	0.75 + 0.025*SL
	t_{PHL}	0.79	0.74 + 0.023*SL	0.76 + 0.016*SL	0.80 + 0.013*SL
	t_R	0.28	0.17 + 0.053*SL	0.17 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.19	0.14 + 0.024*SL	0.15 + 0.021*SL	0.16 + 0.020*SL
GN to Q	t_{PLH}	0.86	0.80 + 0.030*SL	0.81 + 0.026*SL	0.82 + 0.025*SL
	t_{PHL}	0.77	0.72 + 0.023*SL	0.74 + 0.016*SL	0.78 + 0.013*SL
	t_R	0.27	0.17 + 0.052*SL	0.17 + 0.053*SL	0.16 + 0.053*SL
	t_F	0.19	0.14 + 0.024*SL	0.15 + 0.021*SL	0.16 + 0.020*SL
RN to Q	t_{PLH}	0.39	0.33 + 0.029*SL	0.34 + 0.026*SL	0.35 + 0.025*SL
	t_{PHL}	0.40	0.36 + 0.021*SL	0.37 + 0.016*SL	0.40 + 0.013*SL
	t_R	0.27	0.17 + 0.052*SL	0.17 + 0.053*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
D to QN	t_{PLH}	1.03	0.98 + 0.024*SL	0.98 + 0.024*SL	0.97 + 0.025*SL
	t_{PHL}	0.99	0.95 + 0.020*SL	0.97 + 0.015*SL	0.99 + 0.013*SL
	t_R	0.24	0.14 + 0.051*SL	0.14 + 0.052*SL	0.12 + 0.054*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
GN to QN	t_{PLH}	1.01	0.96 + 0.024*SL	0.96 + 0.024*SL	0.95 + 0.025*SL
	t_{PHL}	1.07	1.03 + 0.019*SL	1.04 + 0.015*SL	1.07 + 0.013*SL
	t_R	0.24	0.14 + 0.051*SL	0.14 + 0.052*SL	0.12 + 0.054*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.021*SL	0.14 + 0.020*SL
RN to QN	t_{PLH}	0.72	0.66 + 0.028*SL	0.67 + 0.025*SL	0.67 + 0.024*SL
	t_{PHL}	0.60	0.56 + 0.019*SL	0.57 + 0.015*SL	0.60 + 0.013*SL
	t_R	0.27	0.17 + 0.052*SL	0.17 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

LD7/LD7D2

D Latch with Active Low, Set, 1X/2X Drive

Logic Symbol



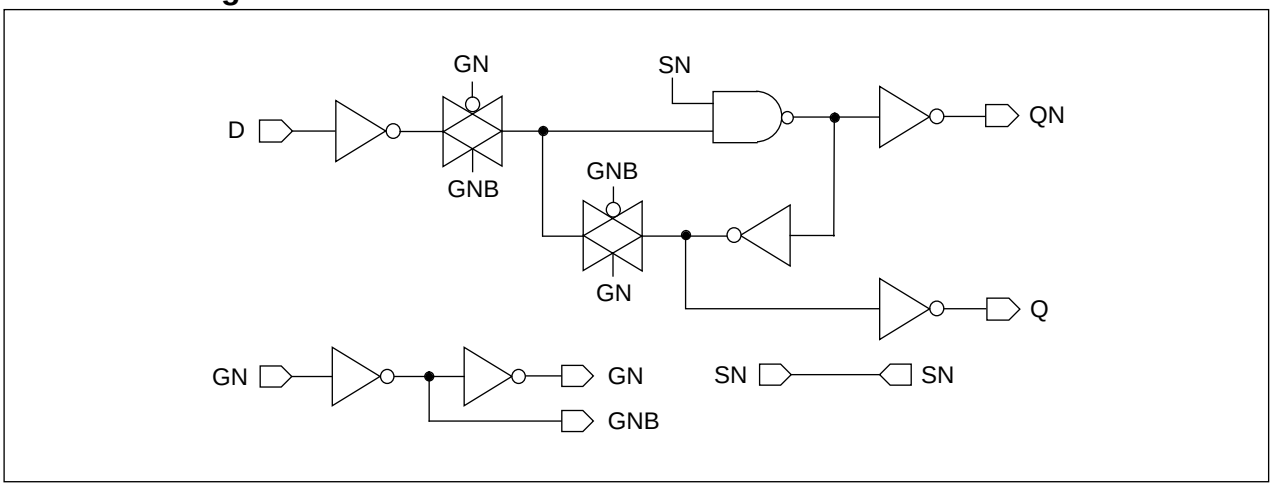
Truth Table

D	GN	SN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
KG80							
LD7			*LD7D2*			*LD7*	*LD7D2*
D	GN	SN	D	GN	SN		
0.8	0.8	0.7	0.8	0.8	0.7	6.0	7.0
KGM80							
LD7			*LD7D2*			*LD7*	*LD7D2*
D	GN	SN	D	GN	SN		
0.9	0.9	0.9	0.9	0.9	0.9	6.0	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD7	LD7D2	LD7	LD7D2
Pulse Width Low (GN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to GN)	t_{SU}	0.42	0.45	0.74	0.80
Input Hold Time (D to GN)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.15	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.54	0.46 + 0.040*SL	0.45 + 0.041*SL	0.45 + 0.042*SL
	t_{PHL}	0.65	0.59 + 0.028*SL	0.60 + 0.025*SL	0.61 + 0.023*SL
	t_R	0.26	0.08 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
GN to Q	t_{PLH}	0.66	0.58 + 0.040*SL	0.57 + 0.041*SL	0.57 + 0.042*SL
	t_{PHL}	0.70	0.64 + 0.028*SL	0.65 + 0.025*SL	0.66 + 0.023*SL
	t_R	0.26	0.08 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
SN to Q	t_{PLH}	0.55	0.46 + 0.042*SL	0.47 + 0.041*SL	0.47 + 0.041*SL
	t_{PHL}	0.37	0.31 + 0.028*SL	0.32 + 0.025*SL	0.33 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.087*SL	0.09 + 0.090*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.58	0.49 + 0.044*SL	0.50 + 0.042*SL	0.50 + 0.041*SL
	t_{PHL}	0.41	0.35 + 0.031*SL	0.36 + 0.026*SL	0.38 + 0.024*SL
	t_R	0.28	0.11 + 0.087*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
GN to QN	t_{PLH}	0.63	0.54 + 0.045*SL	0.55 + 0.042*SL	0.55 + 0.042*SL
	t_{PHL}	0.53	0.47 + 0.031*SL	0.48 + 0.026*SL	0.50 + 0.023*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to QN	t_{PLH}	0.30	0.21 + 0.045*SL	0.22 + 0.042*SL	0.22 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.032*SL	0.29 + 0.026*SL	0.30 + 0.023*SL
	t_R	0.28	0.11 + 0.087*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.039*SL	0.10 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.56	0.53 + 0.018*SL	0.52 + 0.020*SL	0.52 + 0.021*SL
	t_{PHL}	0.69	0.66 + 0.016*SL	0.66 + 0.014*SL	0.67 + 0.012*SL
	t_R	0.18	0.09 + 0.042*SL	0.09 + 0.044*SL	0.08 + 0.046*SL
	t_F	0.14	0.10 + 0.020*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
GN to Q	t_{PLH}	0.68	0.64 + 0.019*SL	0.64 + 0.020*SL	0.64 + 0.021*SL
	t_{PHL}	0.74	0.71 + 0.016*SL	0.72 + 0.014*SL	0.73 + 0.012*SL
	t_R	0.18	0.10 + 0.041*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.019*SL	0.10 + 0.019*SL	0.09 + 0.020*SL
SN to Q	t_{PLH}	0.58	0.53 + 0.021*SL	0.54 + 0.020*SL	0.54 + 0.020*SL
	t_{PHL}	0.40	0.37 + 0.016*SL	0.38 + 0.014*SL	0.39 + 0.012*SL
	t_R	0.20	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.14	0.10 + 0.019*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
D to QN	t_{PLH}	0.58	0.53 + 0.024*SL	0.54 + 0.022*SL	0.54 + 0.021*SL
	t_{PHL}	0.41	0.37 + 0.019*SL	0.38 + 0.015*SL	0.40 + 0.013*SL
	t_R	0.21	0.12 + 0.044*SL	0.12 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.15	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
GN to QN	t_{PLH}	0.63	0.58 + 0.024*SL	0.59 + 0.022*SL	0.59 + 0.021*SL
	t_{PHL}	0.53	0.49 + 0.019*SL	0.50 + 0.015*SL	0.52 + 0.013*SL
	t_R	0.20	0.12 + 0.043*SL	0.12 + 0.044*SL	0.11 + 0.044*SL
	t_F	0.14	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
SN to QN	t_{PLH}	0.29	0.24 + 0.024*SL	0.25 + 0.022*SL	0.25 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.020*SL	0.30 + 0.015*SL	0.32 + 0.013*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.045*SL
	t_F	0.16	0.12 + 0.020*SL	0.12 + 0.019*SL	0.12 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.75	0.65 + 0.049*SL	0.65 + 0.050*SL	0.65 + 0.050*SL
	t_{PHL}	0.92	0.85 + 0.032*SL	0.87 + 0.025*SL	0.89 + 0.023*SL
	t_R	0.33	0.12 + 0.105*SL	0.11 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.041*SL	0.09 + 0.043*SL
GN to Q	t_{PLH}	0.90	0.81 + 0.049*SL	0.80 + 0.050*SL	0.80 + 0.050*SL
	t_{PHL}	0.99	0.92 + 0.032*SL	0.94 + 0.025*SL	0.96 + 0.023*SL
	t_R	0.33	0.12 + 0.105*SL	0.11 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.042*SL	0.10 + 0.042*SL	0.09 + 0.043*SL
SN to Q	t_{PLH}	0.73	0.62 + 0.054*SL	0.63 + 0.050*SL	0.63 + 0.050*SL
	t_{PHL}	0.51	0.45 + 0.032*SL	0.47 + 0.025*SL	0.49 + 0.023*SL
	t_R	0.37	0.16 + 0.103*SL	0.16 + 0.106*SL	0.13 + 0.108*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
D to QN	t_{PLH}	0.81	0.70 + 0.055*SL	0.71 + 0.051*SL	0.72 + 0.050*SL
	t_{PHL}	0.57	0.50 + 0.035*SL	0.52 + 0.027*SL	0.56 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
GN to QN	t_{PLH}	0.88	0.77 + 0.054*SL	0.78 + 0.051*SL	0.80 + 0.050*SL
	t_{PHL}	0.72	0.65 + 0.035*SL	0.68 + 0.027*SL	0.71 + 0.023*SL
	t_R	0.37	0.16 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
SN to QN	t_{PLH}	0.41	0.30 + 0.055*SL	0.31 + 0.051*SL	0.32 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.040*SL	0.13 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

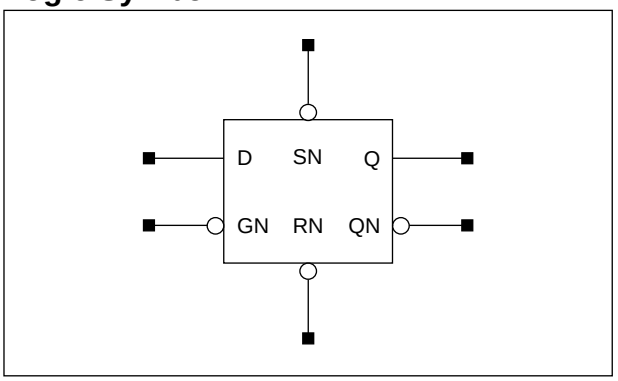
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.79	0.75 + 0.023*SL	0.74 + 0.024*SL	0.74 + 0.025*SL
	t_{PHL}	0.99	0.95 + 0.018*SL	0.96 + 0.015*SL	0.98 + 0.012*SL
	t_R	0.24	0.13 + 0.051*SL	0.13 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
GN to Q	t_{PLH}	0.95	0.90 + 0.023*SL	0.90 + 0.024*SL	0.89 + 0.025*SL
	t_{PHL}	1.06	1.02 + 0.018*SL	1.03 + 0.015*SL	1.05 + 0.012*SL
	t_R	0.24	0.13 + 0.051*SL	0.13 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
SN to Q	t_{PLH}	0.77	0.71 + 0.029*SL	0.72 + 0.025*SL	0.73 + 0.024*SL
	t_{PHL}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.57 + 0.012*SL
	t_R	0.27	0.16 + 0.052*SL	0.17 + 0.051*SL	0.15 + 0.053*SL
	t_F	0.17	0.12 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
D to QN	t_{PLH}	0.81	0.75 + 0.030*SL	0.76 + 0.026*SL	0.77 + 0.025*SL
	t_{PHL}	0.58	0.54 + 0.021*SL	0.55 + 0.016*SL	0.58 + 0.013*SL
	t_R	0.27	0.16 + 0.052*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
GN to QN	t_{PLH}	0.88	0.82 + 0.030*SL	0.83 + 0.026*SL	0.84 + 0.025*SL
	t_{PHL}	0.73	0.69 + 0.022*SL	0.71 + 0.016*SL	0.74 + 0.013*SL
	t_R	0.27	0.16 + 0.052*SL	0.16 + 0.052*SL	0.16 + 0.053*SL
	t_F	0.18	0.13 + 0.023*SL	0.13 + 0.021*SL	0.15 + 0.020*SL
SN to QN	t_{PLH}	0.40	0.34 + 0.030*SL	0.35 + 0.026*SL	0.36 + 0.025*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.41 + 0.016*SL	0.45 + 0.013*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.14 + 0.024*SL	0.15 + 0.021*SL	0.17 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



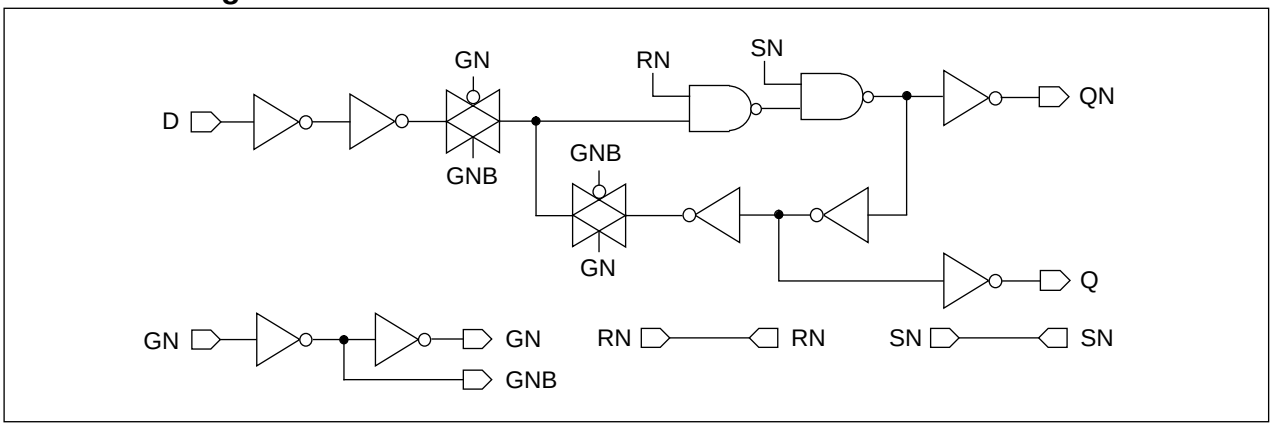
Truth Table

D	GN	RN	SN	Q (n+1)	QN (n+1)
0	0	1	1	0	1
1	0	1	1	1	0
x	1	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
LD8				*LD8D2*				*LD8*	*LD8D2*
D	GN	RN	SN	D	GN	RN	SN		
0.8	0.8	0.7	0.7	0.8	0.8	0.7	0.7	6.0	7.0
KGM80									
LD8				*LD8D2*				*LD8*	*LD8D2*
D	GN	RN	SN	D	GN	RN	SN		
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	6.0	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80		KGM80	
		LD8	LD8D2	LD8	LD8D2
Pulse Width Low (GN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (RN)	t_{PWL}	0.61	0.61	0.99	0.99
Pulse Width Low (SN)	t_{PWL}	0.61	0.61	0.99	0.99
Input Setup Time (D to GN)	t_{SU}	0.50	0.53	0.83	0.86
Input Hold Time (D to GN)	t_{HD}	0.15	0.15	0.33	0.33
Recovery Time (RN)	t_{RC}	0.17	0.20	0.36	0.43
Input Hold Time (RN to GN)	t_{HD}	0.15	0.15	0.41	0.41
Recovery Time (SN)	t_{RC}	0.15	0.15	0.33	0.33
Input Hold Time (SN to GN)	t_{HD}	0.20	0.15	0.41	0.41

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.73	0.65 + 0.040*SL	0.65 + 0.041*SL	0.65 + 0.042*SL
	t_{PHL}	0.77	0.71 + 0.030*SL	0.73 + 0.025*SL	0.74 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.041*SL
GN to Q	t_{PLH}	0.81	0.72 + 0.041*SL	0.72 + 0.041*SL	0.72 + 0.042*SL
	t_{PHL}	0.76	0.69 + 0.030*SL	0.71 + 0.025*SL	0.72 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.17	0.08 + 0.041*SL	0.09 + 0.040*SL	0.07 + 0.041*SL
SN to Q	t_{PLH}	0.47	0.38 + 0.040*SL	0.38 + 0.041*SL	0.38 + 0.042*SL
	t_{PHL}	0.37	0.31 + 0.030*SL	0.33 + 0.025*SL	0.34 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.040*SL	0.07 + 0.041*SL
RN to Q	t_{PLH}	0.48	0.40 + 0.041*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_{PHL}	0.56	0.51 + 0.027*SL	0.51 + 0.025*SL	0.52 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.70	0.61 + 0.045*SL	0.62 + 0.042*SL	0.62 + 0.042*SL
	t_{PHL}	0.61	0.54 + 0.031*SL	0.56 + 0.026*SL	0.57 + 0.024*SL
	t_R	0.28	0.10 + 0.086*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.043*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
GN to QN	t_{PLH}	0.68	0.59 + 0.045*SL	0.60 + 0.042*SL	0.60 + 0.042*SL
	t_{PHL}	0.68	0.62 + 0.031*SL	0.63 + 0.026*SL	0.65 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.043*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SN to QN	t_{PLH}	0.30	0.21 + 0.044*SL	0.22 + 0.042*SL	0.22 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.033*SL	0.29 + 0.026*SL	0.31 + 0.024*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.039*SL	0.10 + 0.041*SL
RN to QN	t_{PLH}	0.49	0.41 + 0.042*SL	0.40 + 0.042*SL	0.41 + 0.042*SL
	t_{PHL}	0.35	0.29 + 0.031*SL	0.30 + 0.026*SL	0.32 + 0.024*SL
	t_R	0.28	0.10 + 0.088*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.17	0.08 + 0.043*SL	0.09 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.76	0.72 + 0.019*SL	0.72 + 0.020*SL	0.71 + 0.021*SL
	t_{PHL}	0.81	0.78 + 0.017*SL	0.79 + 0.014*SL	0.80 + 0.012*SL
	t_R	0.18	0.10 + 0.040*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.019*SL	0.11 + 0.019*SL
GN to Q	t_{PLH}	0.83	0.79 + 0.019*SL	0.79 + 0.020*SL	0.79 + 0.021*SL
	t_{PHL}	0.79	0.76 + 0.017*SL	0.77 + 0.014*SL	0.78 + 0.013*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.019*SL	0.10 + 0.020*SL
SN to Q	t_{PLH}	0.49	0.45 + 0.019*SL	0.45 + 0.020*SL	0.44 + 0.021*SL
	t_{PHL}	0.41	0.38 + 0.017*SL	0.39 + 0.014*SL	0.39 + 0.013*SL
	t_R	0.18	0.10 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.020*SL	0.11 + 0.019*SL
RN to Q	t_{PLH}	0.50	0.46 + 0.019*SL	0.46 + 0.020*SL	0.46 + 0.021*SL
	t_{PHL}	0.60	0.57 + 0.016*SL	0.57 + 0.014*SL	0.59 + 0.012*SL
	t_R	0.18	0.10 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.14	0.10 + 0.020*SL	0.10 + 0.019*SL	0.10 + 0.020*SL
D to QN	t_{PLH}	0.69	0.65 + 0.024*SL	0.65 + 0.022*SL	0.65 + 0.021*SL
	t_{PHL}	0.61	0.57 + 0.019*SL	0.58 + 0.015*SL	0.59 + 0.013*SL
	t_R	0.20	0.12 + 0.042*SL	0.11 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.14	0.10 + 0.020*SL	0.10 + 0.021*SL	0.11 + 0.019*SL
GN to QN	t_{PLH}	0.67	0.62 + 0.025*SL	0.63 + 0.022*SL	0.64 + 0.021*SL
	t_{PHL}	0.68	0.64 + 0.019*SL	0.65 + 0.015*SL	0.66 + 0.013*SL
	t_R	0.20	0.12 + 0.041*SL	0.11 + 0.044*SL	0.10 + 0.045*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.11 + 0.020*SL
SN to QN	t_{PLH}	0.29	0.24 + 0.024*SL	0.25 + 0.021*SL	0.25 + 0.021*SL
	t_{PHL}	0.33	0.29 + 0.021*SL	0.30 + 0.016*SL	0.32 + 0.014*SL
	t_R	0.20	0.12 + 0.043*SL	0.11 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.16	0.12 + 0.022*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
RN to QN	t_{PLH}	0.48	0.43 + 0.024*SL	0.44 + 0.022*SL	0.45 + 0.021*SL
	t_{PHL}	0.35	0.31 + 0.019*SL	0.32 + 0.015*SL	0.33 + 0.013*SL
	t_R	0.20	0.12 + 0.043*SL	0.11 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	1.08	0.98 + 0.050*SL	0.98 + 0.050*SL	0.98 + 0.050*SL
	t_{PHL}	1.07	1.00 + 0.033*SL	1.02 + 0.026*SL	1.05 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
GN to Q	t_{PLH}	1.14	1.04 + 0.050*SL	1.04 + 0.050*SL	1.04 + 0.050*SL
	t_{PHL}	1.05	0.98 + 0.033*SL	1.00 + 0.026*SL	1.03 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
SN to Q	t_{PLH}	0.62	0.52 + 0.049*SL	0.52 + 0.050*SL	0.52 + 0.050*SL
	t_{PHL}	0.52	0.45 + 0.033*SL	0.47 + 0.026*SL	0.50 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.041*SL	0.10 + 0.042*SL
RN to Q	t_{PLH}	0.67	0.57 + 0.050*SL	0.57 + 0.050*SL	0.58 + 0.050*SL
	t_{PHL}	0.77	0.70 + 0.032*SL	0.72 + 0.026*SL	0.74 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D to QN	t_{PLH}	0.96	0.85 + 0.054*SL	0.86 + 0.051*SL	0.87 + 0.050*SL
	t_{PHL}	0.90	0.83 + 0.035*SL	0.85 + 0.027*SL	0.88 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
GN to QN	t_{PLH}	0.94	0.83 + 0.054*SL	0.84 + 0.051*SL	0.85 + 0.050*SL
	t_{PHL}	0.96	0.89 + 0.035*SL	0.91 + 0.027*SL	0.95 + 0.024*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.12 + 0.042*SL
SN to QN	t_{PLH}	0.41	0.30 + 0.054*SL	0.31 + 0.051*SL	0.32 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.037*SL	0.39 + 0.027*SL	0.43 + 0.024*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.22	0.13 + 0.044*SL	0.14 + 0.041*SL	0.13 + 0.042*SL
RN to QN	t_{PLH}	0.66	0.55 + 0.054*SL	0.56 + 0.051*SL	0.57 + 0.050*SL
	t_{PHL}	0.49	0.43 + 0.035*SL	0.45 + 0.027*SL	0.48 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LD8D2

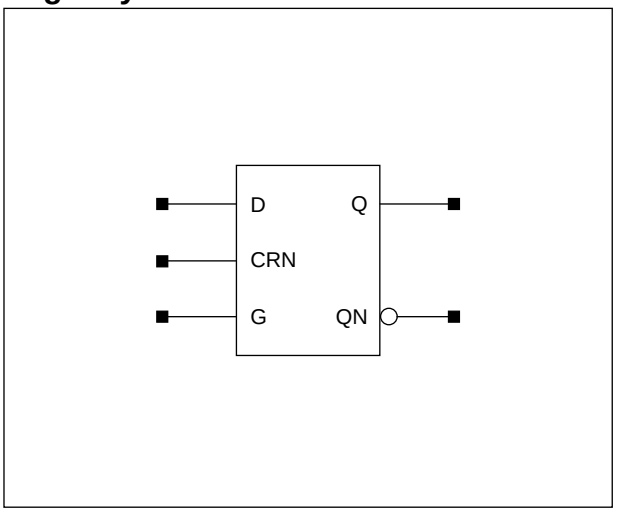
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	1.12	1.07 + 0.023*SL	1.07 + 0.024*SL	1.06 + 0.025*SL
	t_{PHL}	1.13	1.09 + 0.019*SL	1.10 + 0.015*SL	1.13 + 0.012*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.17	0.13 + 0.024*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
GN to Q	t_{PLH}	1.18	1.14 + 0.023*SL	1.13 + 0.024*SL	1.13 + 0.025*SL
	t_{PHL}	1.11	1.07 + 0.019*SL	1.08 + 0.015*SL	1.11 + 0.013*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.17	0.13 + 0.025*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
SN to Q	t_{PLH}	0.66	0.62 + 0.023*SL	0.62 + 0.024*SL	0.61 + 0.025*SL
	t_{PHL}	0.58	0.54 + 0.019*SL	0.55 + 0.015*SL	0.58 + 0.012*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.18	0.12 + 0.025*SL	0.14 + 0.020*SL	0.14 + 0.020*SL
RN to Q	t_{PLH}	0.72	0.67 + 0.023*SL	0.67 + 0.024*SL	0.66 + 0.025*SL
	t_{PHL}	0.83	0.79 + 0.019*SL	0.80 + 0.015*SL	0.83 + 0.013*SL
	t_R	0.24	0.14 + 0.051*SL	0.13 + 0.053*SL	0.12 + 0.054*SL
	t_F	0.17	0.13 + 0.023*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
D to QN	t_{PLH}	0.95	0.89 + 0.030*SL	0.90 + 0.026*SL	0.91 + 0.025*SL
	t_{PHL}	0.90	0.86 + 0.021*SL	0.87 + 0.016*SL	0.91 + 0.013*SL
	t_R	0.26	0.16 + 0.053*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.17	0.13 + 0.025*SL	0.13 + 0.021*SL	0.15 + 0.020*SL
GN to QN	t_{PLH}	0.93	0.87 + 0.030*SL	0.88 + 0.026*SL	0.89 + 0.025*SL
	t_{PHL}	0.97	0.92 + 0.022*SL	0.94 + 0.016*SL	0.97 + 0.013*SL
	t_R	0.26	0.16 + 0.053*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.15 + 0.020*SL
SN to QN	t_{PLH}	0.39	0.33 + 0.030*SL	0.35 + 0.026*SL	0.36 + 0.025*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.42 + 0.017*SL	0.45 + 0.013*SL
	t_R	0.26	0.16 + 0.053*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.19	0.15 + 0.024*SL	0.15 + 0.021*SL	0.17 + 0.020*SL
RN to QN	t_{PLH}	0.65	0.59 + 0.030*SL	0.60 + 0.026*SL	0.61 + 0.025*SL
	t_{PHL}	0.50	0.46 + 0.022*SL	0.47 + 0.016*SL	0.51 + 0.013*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.021*SL	0.14 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

LDS2

D Latch with Active High, Synchronous Clear

Logic Symbol



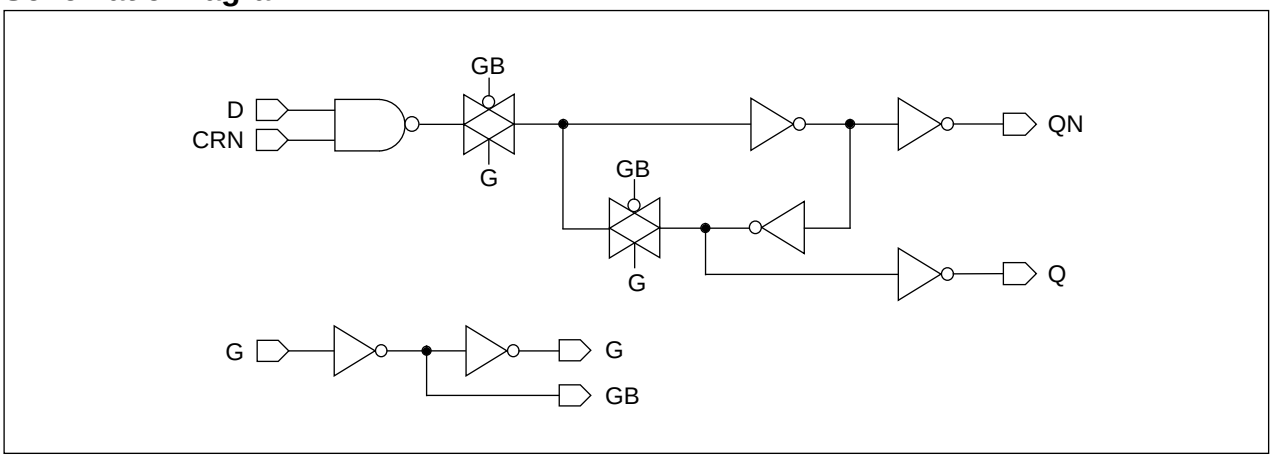
Truth Table

D	CRN	G	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	x	0	Q (n)	QN (n)
x	0	1	0	1

Cell Data

Input Load (SL)			Gate Count
KG80			
D	CRN	G	
0.9	0.8	0.9	5.0
KGM80			
D	CRN	G	
1.0	1.0	1.0	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width High (G)	t_{PWH}	0.61	0.99
Input Setup Time (D to G)	t_{SU}	0.31	0.55
Input Hold Time (D to G)	t_{HD}	0.15	0.33
Input Setup Time (CRN to G)	t_{SU}	0.31	0.55
Input Hold Time (CRN to G)	t_{HD}	0.15	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.61	0.53 + 0.040*SL	0.53 + 0.041*SL	0.53 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.029*SL	0.54 + 0.025*SL	0.55 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
CRN to Q	t_{PLH}	0.59	0.51 + 0.040*SL	0.51 + 0.041*SL	0.50 + 0.042*SL
	t_{PHL}	0.62	0.56 + 0.029*SL	0.57 + 0.025*SL	0.58 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
G to Q	t_{PLH}	0.63	0.55 + 0.040*SL	0.55 + 0.041*SL	0.54 + 0.042*SL
	t_{PHL}	0.53	0.47 + 0.030*SL	0.48 + 0.025*SL	0.49 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.48	0.41 + 0.031*SL	0.43 + 0.026*SL	0.44 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CRN to QN	t_{PLH}	0.54	0.46 + 0.042*SL	0.46 + 0.041*SL	0.46 + 0.042*SL
	t_{PHL}	0.45	0.39 + 0.031*SL	0.40 + 0.026*SL	0.42 + 0.023*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.039*SL	0.09 + 0.041*SL
G to QN	t_{PLH}	0.45	0.37 + 0.042*SL	0.37 + 0.042*SL	0.37 + 0.042*SL
	t_{PHL}	0.50	0.43 + 0.031*SL	0.45 + 0.026*SL	0.46 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

LDS2

D Latch with Active High, Synchronous Clear

Switching Characteristics

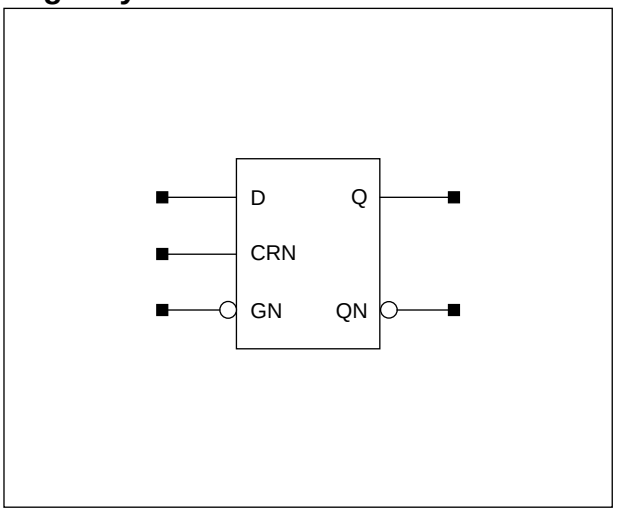
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.84	0.75 + 0.049*SL	0.74 + 0.050*SL	0.74 + 0.050*SL
	t_{PHL}	0.83	0.77 + 0.032*SL	0.78 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
CRN to Q	t_{PLH}	0.84	0.74 + 0.049*SL	0.74 + 0.050*SL	0.73 + 0.050*SL
	t_{PHL}	0.87	0.81 + 0.033*SL	0.83 + 0.025*SL	0.85 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
G to Q	t_{PLH}	0.89	0.79 + 0.049*SL	0.79 + 0.050*SL	0.79 + 0.050*SL
	t_{PHL}	0.74	0.68 + 0.032*SL	0.70 + 0.026*SL	0.72 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D to QN	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.65	0.58 + 0.035*SL	0.61 + 0.026*SL	0.64 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.11 + 0.042*SL
CRN to QN	t_{PLH}	0.75	0.65 + 0.051*SL	0.65 + 0.050*SL	0.66 + 0.050*SL
	t_{PHL}	0.64	0.57 + 0.035*SL	0.59 + 0.026*SL	0.63 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
G to QN	t_{PLH}	0.62	0.52 + 0.051*SL	0.52 + 0.050*SL	0.53 + 0.050*SL
	t_{PHL}	0.69	0.63 + 0.034*SL	0.65 + 0.026*SL	0.68 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



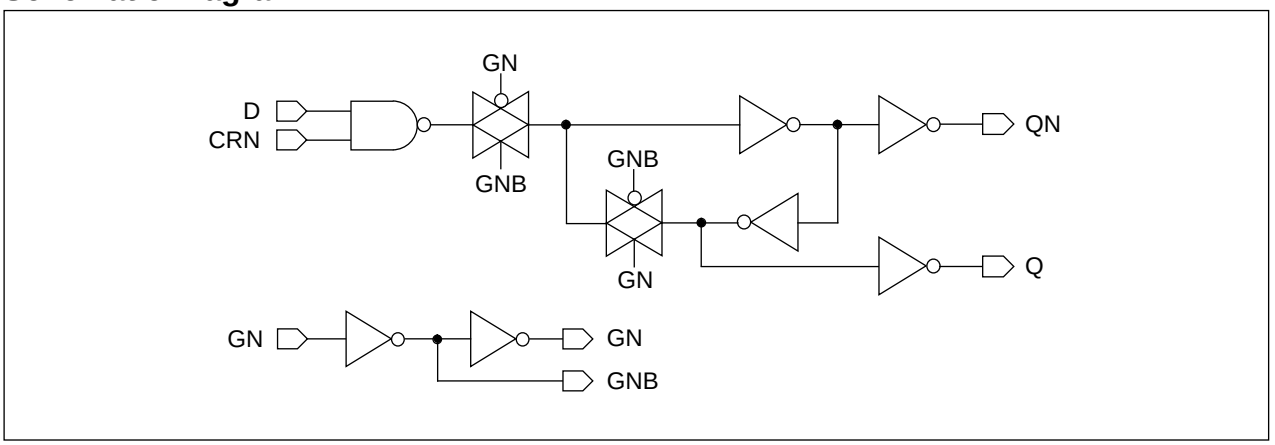
Truth Table

D	CRN	GN	Q (n+1)	QN (n+1)
0	1	0	0	1
1	1	0	1	0
x	x	1	Q (n)	QN (n)
x	0	0	0	1

Cell Data

Input Load (SL)			Gate Count
KG80			
D	CRN	GN	
0.9	0.8	0.9	5.0
KGM80			
D	CRN	GN	
1.0	1.0	1.0	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 5V, 3.3V, Unit = ns)

Parameter	Symbol	KG80	KGM80
Pulse Width Low (GN)	t_{PWL}	0.61	0.99
Input Setup Time (D to GN)	t_{SU}	0.42	0.74
Input Hold Time (D to GN)	t_{HD}	0.15	0.33
Input Setup Time (CRN to GN)	t_{SU}	0.42	0.74
Input Hold Time (CRN to GN)	t_{HD}	0.15	0.33

LDS6

D Latch with Active Low, Synchronous Clear

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LDS6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.61	0.53 + 0.040*SL	0.53 + 0.041*SL	0.53 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.029*SL	0.54 + 0.025*SL	0.55 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.041*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
CRN to Q	t_{PLH}	0.59	0.51 + 0.040*SL	0.51 + 0.041*SL	0.51 + 0.042*SL
	t_{PHL}	0.62	0.56 + 0.029*SL	0.57 + 0.025*SL	0.58 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
GN to Q	t_{PLH}	0.69	0.61 + 0.040*SL	0.60 + 0.041*SL	0.60 + 0.042*SL
	t_{PHL}	0.63	0.57 + 0.030*SL	0.58 + 0.025*SL	0.59 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
D to QN	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.48	0.41 + 0.031*SL	0.43 + 0.026*SL	0.44 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
CRN to QN	t_{PLH}	0.54	0.46 + 0.042*SL	0.46 + 0.041*SL	0.46 + 0.042*SL
	t_{PHL}	0.46	0.40 + 0.031*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
GN to QN	t_{PLH}	0.56	0.47 + 0.042*SL	0.47 + 0.042*SL	0.47 + 0.042*SL
	t_{PHL}	0.55	0.49 + 0.031*SL	0.50 + 0.025*SL	0.52 + 0.024*SL
	t_R	0.27	0.09 + 0.087*SL	0.09 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.10 + 0.040*SL	0.08 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LDS6

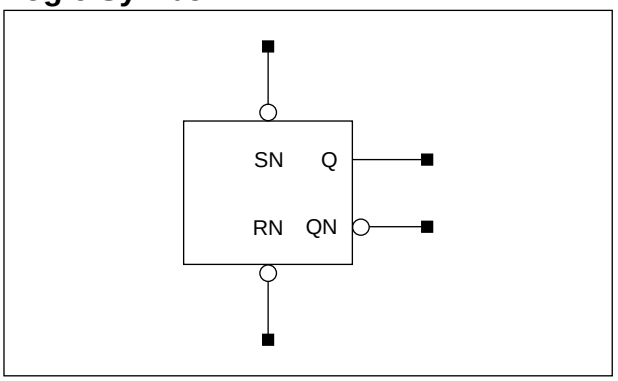
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.85	0.75 + 0.049*SL	0.75 + 0.050*SL	0.74 + 0.050*SL
	t_{PHL}	0.83	0.77 + 0.033*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.044*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
CRN to Q	t_{PLH}	0.84	0.74 + 0.049*SL	0.74 + 0.050*SL	0.74 + 0.050*SL
	t_{PHL}	0.87	0.81 + 0.032*SL	0.83 + 0.026*SL	0.85 + 0.023*SL
	t_R	0.34	0.13 + 0.104*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
GN to Q	t_{PLH}	0.94	0.84 + 0.047*SL	0.84 + 0.050*SL	0.84 + 0.050*SL
	t_{PHL}	0.88	0.81 + 0.033*SL	0.83 + 0.026*SL	0.85 + 0.023*SL
	t_R	0.34	0.13 + 0.103*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.10 + 0.042*SL
D to QN	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.65	0.58 + 0.035*SL	0.61 + 0.026*SL	0.64 + 0.023*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
CRN to QN	t_{PLH}	0.75	0.65 + 0.051*SL	0.65 + 0.050*SL	0.66 + 0.050*SL
	t_{PHL}	0.64	0.57 + 0.035*SL	0.60 + 0.026*SL	0.63 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL
GN to QN	t_{PLH}	0.76	0.65 + 0.051*SL	0.66 + 0.050*SL	0.66 + 0.050*SL
	t_{PHL}	0.74	0.68 + 0.033*SL	0.70 + 0.026*SL	0.73 + 0.023*SL
	t_R	0.34	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.11 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

LS0/LS0D2

SR Latch with 1X/2X Drive

Logic Symbol



Truth Table

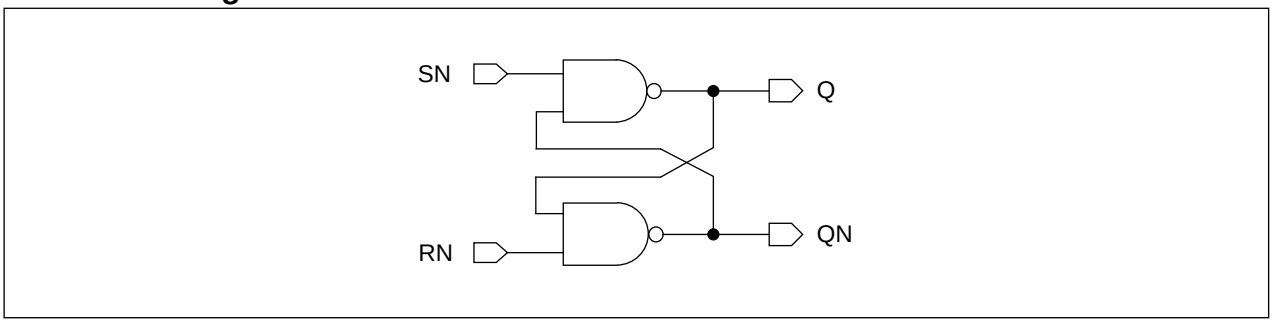
RN	SN	Q (n+1)	QN (n+1)
0	0	*	*
1	0	1	0
0	1	0	1
1	1	Q (n)	QN (n)

* Both Q and QN outputs will remain high during RN and SN are low. However, if RN and SN go high simultaneously, the output states are unpredictable.

Cell Data

Input Load (SL)				Gate Count	
KG80					
LS0		*LS0D2*		*LS0*	*LS0D2*
RN	SN	RN	SN		
0.8	0.5	1.5	1.5	5.0	6.0
KGM80					
LS0		*LS0D2*		*LS0*	*LS0D2*
RN	SN	RN	SN		
1.0	1.0	2.0	2.0	5.0	6.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LS0

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.24	0.16 + 0.042*SL	0.16 + 0.040*SL	0.16 + 0.041*SL
	t_{PHL}	0.17	0.09 + 0.041*SL	0.11 + 0.034*SL	0.11 + 0.034*SL
	t_R	0.36	0.21 + 0.077*SL	0.19 + 0.085*SL	0.17 + 0.088*SL
	t_F	0.33	0.22 + 0.055*SL	0.20 + 0.062*SL	0.18 + 0.065*SL
RN to Q	t_{PHL}	0.45	0.29 + 0.081*SL	0.29 + 0.080*SL	0.29 + 0.081*SL
	t_F	0.29	0.14 + 0.077*SL	0.13 + 0.079*SL	0.13 + 0.080*SL
SN to QN	t_{PHL}	0.43	0.25 + 0.090*SL	0.26 + 0.088*SL	0.25 + 0.089*SL
	t_F	0.32	0.15 + 0.082*SL	0.15 + 0.084*SL	0.15 + 0.084*SL
RN to QN	t_{PLH}	0.28	0.20 + 0.039*SL	0.20 + 0.040*SL	0.19 + 0.041*SL
	t_{PHL}	0.17	0.09 + 0.038*SL	0.10 + 0.034*SL	0.10 + 0.034*SL
	t_R	0.43	0.28 + 0.078*SL	0.26 + 0.084*SL	0.23 + 0.088*SL
	t_F	0.32	0.21 + 0.058*SL	0.19 + 0.064*SL	0.17 + 0.066*SL

KG80 LS0D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.23	0.19 + 0.022*SL	0.19 + 0.020*SL	0.19 + 0.020*SL
	t_{PHL}	0.12	0.08 + 0.022*SL	0.09 + 0.019*SL	0.10 + 0.017*SL
	t_R	0.33	0.26 + 0.038*SL	0.25 + 0.040*SL	0.23 + 0.042*SL
	t_F	0.25	0.19 + 0.028*SL	0.19 + 0.029*SL	0.17 + 0.032*SL
RN to Q	t_{PHL}	0.37	0.28 + 0.045*SL	0.28 + 0.044*SL	0.28 + 0.044*SL
	t_F	0.22	0.13 + 0.042*SL	0.13 + 0.041*SL	0.13 + 0.042*SL
SN to QN	t_{PHL}	0.37	0.28 + 0.044*SL	0.28 + 0.044*SL	0.28 + 0.044*SL
	t_F	0.22	0.13 + 0.042*SL	0.13 + 0.041*SL	0.13 + 0.042*SL
RN to QN	t_{PLH}	0.23	0.19 + 0.021*SL	0.19 + 0.020*SL	0.19 + 0.020*SL
	t_{PHL}	0.12	0.08 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.017*SL
	t_R	0.33	0.26 + 0.036*SL	0.25 + 0.040*SL	0.23 + 0.042*SL
	t_F	0.25	0.19 + 0.028*SL	0.19 + 0.029*SL	0.17 + 0.032*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

LS0/LS0D2

SR Latch with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LS0

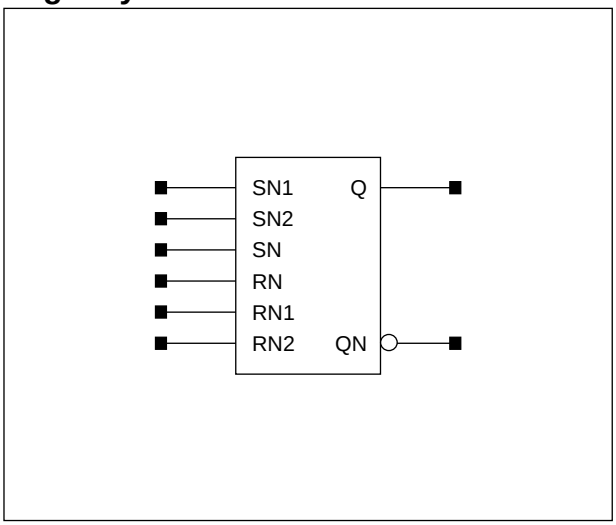
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.30	0.20 + 0.051*SL	0.20 + 0.049*SL	0.20 + 0.050*SL
	t_{PHL}	0.21	0.12 + 0.044*SL	0.14 + 0.038*SL	0.15 + 0.037*SL
	t_R	0.45	0.25 + 0.100*SL	0.24 + 0.105*SL	0.21 + 0.108*SL
	t_F	0.36	0.23 + 0.066*SL	0.22 + 0.070*SL	0.19 + 0.073*SL
RN to Q	t_{PHL}	0.58	0.38 + 0.099*SL	0.39 + 0.098*SL	0.39 + 0.097*SL
	t_F	0.34	0.18 + 0.084*SL	0.17 + 0.086*SL	0.16 + 0.087*SL
SN to QN	t_{PHL}	0.55	0.33 + 0.109*SL	0.34 + 0.107*SL	0.34 + 0.107*SL
	t_F	0.38	0.20 + 0.091*SL	0.19 + 0.093*SL	0.19 + 0.094*SL
RN to QN	t_{PLH}	0.35	0.25 + 0.050*SL	0.25 + 0.049*SL	0.25 + 0.050*SL
	t_{PHL}	0.22	0.13 + 0.042*SL	0.15 + 0.038*SL	0.15 + 0.037*SL
	t_R	0.54	0.33 + 0.100*SL	0.32 + 0.106*SL	0.29 + 0.108*SL
	t_F	0.36	0.23 + 0.067*SL	0.21 + 0.072*SL	0.19 + 0.074*SL

KGM80 LS0D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.29	0.24 + 0.026*SL	0.24 + 0.025*SL	0.24 + 0.025*SL
	t_{PHL}	0.16	0.12 + 0.023*SL	0.13 + 0.020*SL	0.14 + 0.019*SL
	t_R	0.40	0.31 + 0.048*SL	0.30 + 0.051*SL	0.28 + 0.053*SL
	t_F	0.27	0.20 + 0.035*SL	0.20 + 0.034*SL	0.19 + 0.036*SL
RN to Q	t_{PHL}	0.48	0.37 + 0.054*SL	0.37 + 0.054*SL	0.37 + 0.053*SL
	t_F	0.26	0.17 + 0.045*SL	0.17 + 0.046*SL	0.17 + 0.047*SL
SN to QN	t_{PHL}	0.48	0.37 + 0.055*SL	0.37 + 0.054*SL	0.37 + 0.053*SL
	t_F	0.26	0.17 + 0.045*SL	0.17 + 0.046*SL	0.17 + 0.047*SL
RN to QN	t_{PLH}	0.29	0.24 + 0.026*SL	0.24 + 0.025*SL	0.24 + 0.025*SL
	t_{PHL}	0.16	0.12 + 0.023*SL	0.13 + 0.020*SL	0.14 + 0.019*SL
	t_R	0.40	0.31 + 0.048*SL	0.30 + 0.051*SL	0.28 + 0.053*SL
	t_F	0.27	0.20 + 0.034*SL	0.20 + 0.034*SL	0.18 + 0.036*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

RN	SN	RN*	SN*	Q (n+1)	QN (n+1)
0	0	x	x	*	*
x	0	0	x	*	*
x	x	0	0	*	*
0	x	x	0	*	*
1	0	1	x	1	0
0	1	x	1	0	1
1	x	1	0	1	0
x	1	0	1	0	1
1	1	1	1	Q (n)	QN (n)

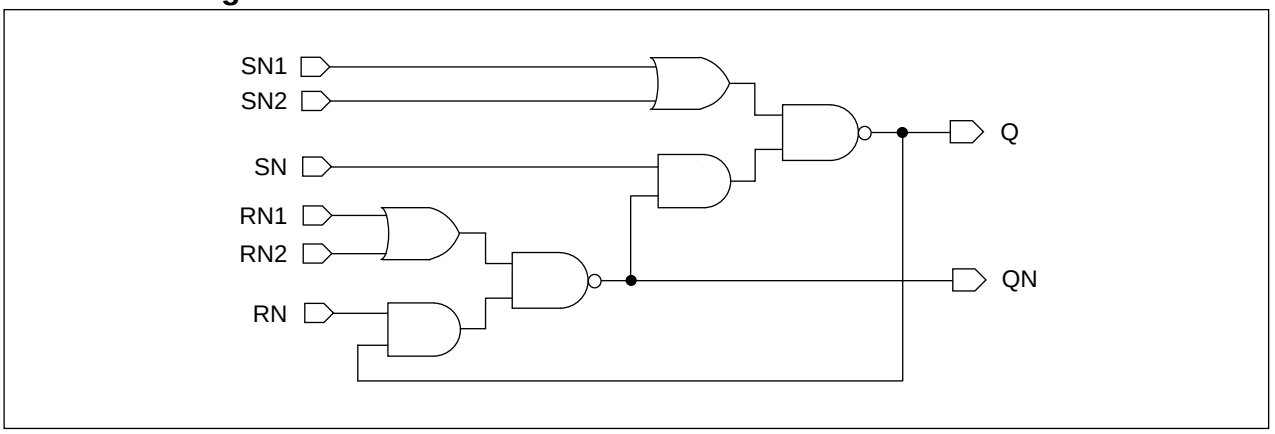
RN* = RN1 + RN2, SN* = SN1 + SN2

* Both Q and QN outputs will be unknown when RN (RN*) and SN (SN*) are low.

Cell Data

Input Load (SL)						Gate Count
KG80						
RN	RN1	RN2	SN	SN1	SN2	
0.8	0.6	0.6	0.9	0.6	0.6	4.0
KGM80						
RN	RN1	RN2	SN	SN1	SN2	
1.0	0.7	0.7	1.0	1.0	1.0	4.0

Schematic Diagram



LS1

SR Latch with Separate Inputs

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LS1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	t_{PLH}	0.39	0.25 + 0.070*SL	0.25 + 0.070*SL	0.25 + 0.071*SL
	t_{PHL}	0.24	0.15 + 0.046*SL	0.15 + 0.045*SL	0.15 + 0.045*SL
	t_R	0.72	0.41 + 0.155*SL	0.40 + 0.160*SL	0.38 + 0.163*SL
	t_F	0.47	0.30 + 0.085*SL	0.29 + 0.089*SL	0.26 + 0.093*SL
SN2 to Q	t_{PLH}	0.39	0.25 + 0.070*SL	0.25 + 0.071*SL	0.25 + 0.071*SL
	t_{PHL}	0.27	0.18 + 0.045*SL	0.18 + 0.045*SL	0.18 + 0.045*SL
	t_R	0.72	0.41 + 0.155*SL	0.40 + 0.160*SL	0.38 + 0.163*SL
	t_F	0.53	0.36 + 0.084*SL	0.35 + 0.089*SL	0.32 + 0.092*SL
SN to Q	t_{PLH}	0.31	0.23 + 0.040*SL	0.23 + 0.041*SL	0.23 + 0.041*SL
	t_{PHL}	0.26	0.17 + 0.047*SL	0.17 + 0.045*SL	0.17 + 0.045*SL
	t_R	0.50	0.34 + 0.078*SL	0.32 + 0.085*SL	0.30 + 0.089*SL
	t_F	0.46	0.29 + 0.085*SL	0.28 + 0.091*SL	0.26 + 0.093*SL
RN1 to Q	t_{PHL}	0.66	0.42 + 0.116*SL	0.42 + 0.118*SL	0.42 + 0.118*SL
	t_F	0.49	0.27 + 0.111*SL	0.27 + 0.112*SL	0.26 + 0.113*SL
RN2 to Q	t_{PHL}	0.66	0.42 + 0.118*SL	0.42 + 0.118*SL	0.42 + 0.118*SL
	t_F	0.49	0.27 + 0.110*SL	0.27 + 0.112*SL	0.26 + 0.113*SL
RN to Q	t_{PHL}	0.57	0.39 + 0.090*SL	0.40 + 0.088*SL	0.40 + 0.088*SL
	t_F	0.46	0.26 + 0.100*SL	0.26 + 0.102*SL	0.25 + 0.103*SL
SN1 to QN	t_{PHL}	0.66	0.42 + 0.117*SL	0.42 + 0.118*SL	0.42 + 0.118*SL
	t_F	0.49	0.27 + 0.111*SL	0.27 + 0.112*SL	0.26 + 0.113*SL
SN2 to QN	t_{PHL}	0.66	0.42 + 0.118*SL	0.42 + 0.118*SL	0.42 + 0.118*SL
	t_F	0.49	0.27 + 0.110*SL	0.27 + 0.112*SL	0.26 + 0.113*SL
SN to QN	t_{PHL}	0.57	0.39 + 0.089*SL	0.40 + 0.088*SL	0.40 + 0.088*SL
	t_F	0.46	0.26 + 0.100*SL	0.26 + 0.102*SL	0.25 + 0.103*SL
RN1 to QN	t_{PLH}	0.39	0.25 + 0.070*SL	0.25 + 0.070*SL	0.25 + 0.071*SL
	t_{PHL}	0.24	0.15 + 0.046*SL	0.15 + 0.045*SL	0.15 + 0.045*SL
	t_R	0.72	0.41 + 0.154*SL	0.40 + 0.160*SL	0.38 + 0.163*SL
	t_F	0.47	0.30 + 0.085*SL	0.29 + 0.089*SL	0.27 + 0.093*SL
RN2 to QN	t_{PLH}	0.39	0.26 + 0.070*SL	0.25 + 0.071*SL	0.25 + 0.071*SL
	t_{PHL}	0.27	0.18 + 0.045*SL	0.18 + 0.045*SL	0.18 + 0.045*SL
	t_R	0.72	0.41 + 0.156*SL	0.40 + 0.160*SL	0.38 + 0.163*SL
	t_F	0.53	0.36 + 0.084*SL	0.35 + 0.089*SL	0.32 + 0.092*SL
RN to QN	t_{PLH}	0.31	0.23 + 0.040*SL	0.23 + 0.041*SL	0.23 + 0.041*SL
	t_{PHL}	0.26	0.17 + 0.046*SL	0.17 + 0.045*SL	0.17 + 0.045*SL
	t_R	0.50	0.34 + 0.078*SL	0.32 + 0.085*SL	0.30 + 0.088*SL
	t_F	0.47	0.30 + 0.085*SL	0.28 + 0.091*SL	0.26 + 0.093*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LS1

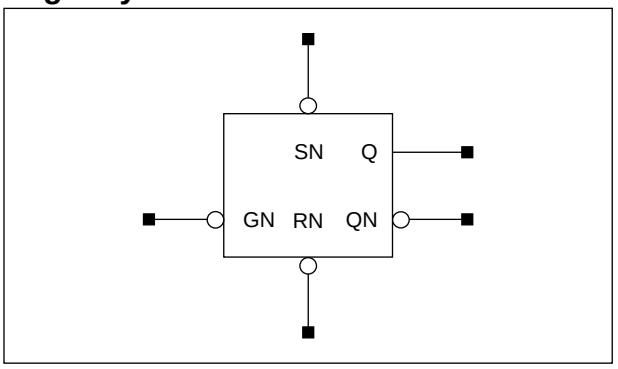
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	t_{PLH}	0.54	0.35 + 0.095*SL	0.35 + 0.094*SL	0.35 + 0.094*SL
	t_{PHL}	0.30	0.20 + 0.052*SL	0.20 + 0.051*SL	0.20 + 0.051*SL
	t_R	1.01	0.60 + 0.202*SL	0.59 + 0.207*SL	0.58 + 0.208*SL
	t_F	0.56	0.37 + 0.099*SL	0.36 + 0.103*SL	0.33 + 0.105*SL
SN2 to Q	t_{PLH}	0.57	0.37 + 0.096*SL	0.38 + 0.095*SL	0.38 + 0.094*SL
	t_{PHL}	0.34	0.24 + 0.051*SL	0.24 + 0.051*SL	0.24 + 0.051*SL
	t_R	1.01	0.60 + 0.203*SL	0.59 + 0.207*SL	0.58 + 0.208*SL
	t_F	0.63	0.43 + 0.097*SL	0.42 + 0.102*SL	0.39 + 0.105*SL
SN to Q	t_{PLH}	0.40	0.30 + 0.050*SL	0.31 + 0.050*SL	0.31 + 0.050*SL
	t_{PHL}	0.35	0.24 + 0.053*SL	0.25 + 0.051*SL	0.25 + 0.051*SL
	t_R	0.63	0.43 + 0.101*SL	0.42 + 0.106*SL	0.39 + 0.109*SL
	t_F	0.56	0.36 + 0.100*SL	0.35 + 0.103*SL	0.33 + 0.105*SL
RN1 to Q	t_{PHL}	0.91	0.61 + 0.153*SL	0.61 + 0.153*SL	0.61 + 0.153*SL
	t_F	0.61	0.36 + 0.123*SL	0.36 + 0.125*SL	0.35 + 0.126*SL
RN2 to Q	t_{PHL}	0.94	0.64 + 0.154*SL	0.64 + 0.153*SL	0.64 + 0.153*SL
	t_F	0.61	0.36 + 0.122*SL	0.36 + 0.125*SL	0.35 + 0.126*SL
RN to Q	t_{PHL}	0.77	0.56 + 0.107*SL	0.56 + 0.106*SL	0.56 + 0.106*SL
	t_F	0.57	0.34 + 0.112*SL	0.34 + 0.113*SL	0.33 + 0.114*SL
SN1 to QN	t_{PHL}	0.91	0.61 + 0.153*SL	0.61 + 0.153*SL	0.61 + 0.153*SL
	t_F	0.61	0.37 + 0.122*SL	0.36 + 0.125*SL	0.35 + 0.126*SL
SN2 to QN	t_{PHL}	0.94	0.63 + 0.154*SL	0.64 + 0.153*SL	0.64 + 0.153*SL
	t_F	0.61	0.37 + 0.122*SL	0.36 + 0.125*SL	0.35 + 0.126*SL
SN to QN	t_{PHL}	0.77	0.56 + 0.108*SL	0.56 + 0.106*SL	0.56 + 0.106*SL
	t_F	0.57	0.34 + 0.112*SL	0.34 + 0.113*SL	0.34 + 0.114*SL
RN1 to QN	t_{PLH}	0.54	0.35 + 0.095*SL	0.35 + 0.094*SL	0.36 + 0.094*SL
	t_{PHL}	0.30	0.20 + 0.052*SL	0.20 + 0.051*SL	0.20 + 0.051*SL
	t_R	1.01	0.61 + 0.202*SL	0.59 + 0.207*SL	0.58 + 0.208*SL
	t_F	0.57	0.37 + 0.098*SL	0.36 + 0.103*SL	0.33 + 0.105*SL
RN2 to QN	t_{PLH}	0.57	0.38 + 0.096*SL	0.38 + 0.095*SL	0.38 + 0.094*SL
	t_{PHL}	0.34	0.24 + 0.051*SL	0.24 + 0.051*SL	0.24 + 0.051*SL
	t_R	1.01	0.61 + 0.203*SL	0.60 + 0.207*SL	0.58 + 0.208*SL
	t_F	0.63	0.43 + 0.097*SL	0.42 + 0.102*SL	0.39 + 0.105*SL
RN to QN	t_{PLH}	0.40	0.30 + 0.050*SL	0.30 + 0.050*SL	0.31 + 0.050*SL
	t_{PHL}	0.35	0.24 + 0.053*SL	0.25 + 0.051*SL	0.25 + 0.051*SL
	t_R	0.64	0.43 + 0.102*SL	0.42 + 0.106*SL	0.39 + 0.109*SL
	t_F	0.56	0.36 + 0.101*SL	0.35 + 0.103*SL	0.33 + 0.105*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

LS2

SR Latch with Common Inputs

Logic Symbol



Truth Table

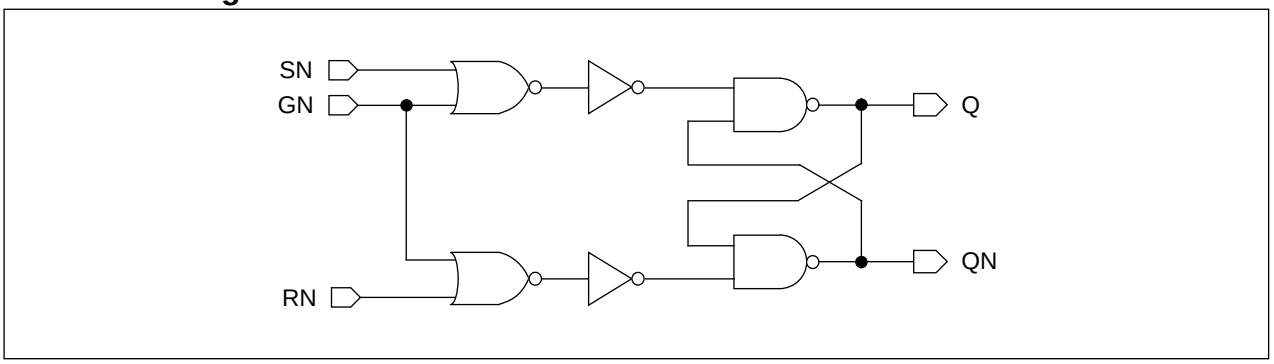
GN	RN	SN	Q (n+1)	QN (n+1)
1	x	x	Q (n)	QN (n)
0	1	1	Q (n)	QN (n)
0	0	1	0	1
0	1	0	1	0
0	0	0	*	*

* Both Q and QN outputs will be unknown when GN, RN, and SN are low.
However, if GN goes high, or RN and SN go high simultaneously, the output states are unpredictable.

Cell Data

Input Load (SL)			Gate Count
KG80			
GN	RN	SN	
1.1	0.8	0.8	5.0
KGM80			
GN	RN	SN	
2.1	1.0	1.0	5.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 LS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.50	0.41 + 0.042*SL	0.41 + 0.042*SL	0.41 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.036*SL	0.27 + 0.034*SL	0.27 + 0.034*SL
	t_R	0.36	0.18 + 0.088*SL	0.18 + 0.090*SL	0.17 + 0.091*SL
	t_F	0.26	0.13 + 0.066*SL	0.12 + 0.068*SL	0.12 + 0.069*SL
RN to Q	t_{PHL}	0.70	0.52 + 0.091*SL	0.52 + 0.089*SL	0.52 + 0.089*SL
	t_F	0.30	0.14 + 0.082*SL	0.13 + 0.084*SL	0.13 + 0.085*SL
GN to Q	t_{PLH}	0.50	0.42 + 0.042*SL	0.42 + 0.042*SL	0.42 + 0.042*SL
	t_{PHL}	0.70	0.52 + 0.091*SL	0.52 + 0.089*SL	0.52 + 0.089*SL
	t_R	0.36	0.20 + 0.080*SL	0.19 + 0.083*SL	0.19 + 0.084*SL
	t_F	0.30	0.13 + 0.085*SL	0.13 + 0.084*SL	0.13 + 0.085*SL
SN to QN	t_{PHL}	0.70	0.52 + 0.090*SL	0.52 + 0.089*SL	0.52 + 0.089*SL
	t_F	0.30	0.14 + 0.083*SL	0.13 + 0.084*SL	0.13 + 0.085*SL
RN to QN	t_{PLH}	0.50	0.42 + 0.042*SL	0.42 + 0.042*SL	0.42 + 0.042*SL
	t_{PHL}	0.35	0.27 + 0.036*SL	0.28 + 0.035*SL	0.28 + 0.034*SL
	t_R	0.36	0.19 + 0.088*SL	0.18 + 0.090*SL	0.18 + 0.091*SL
	t_F	0.26	0.13 + 0.066*SL	0.13 + 0.068*SL	0.12 + 0.069*SL
GN to QN	t_{PLH}	0.51	0.43 + 0.042*SL	0.43 + 0.042*SL	0.43 + 0.042*SL
	t_{PHL}	0.70	0.52 + 0.090*SL	0.52 + 0.089*SL	0.52 + 0.089*SL
	t_R	0.37	0.21 + 0.080*SL	0.20 + 0.083*SL	0.19 + 0.084*SL
	t_F	0.30	0.14 + 0.081*SL	0.13 + 0.085*SL	0.13 + 0.085*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

LS2

SR Latch with Common Inputs

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 LS2

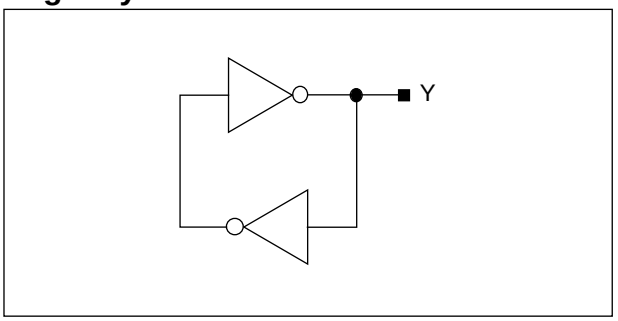
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.70	0.60 + 0.051*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.46	0.38 + 0.040*SL	0.38 + 0.038*SL	0.39 + 0.037*SL
	t_R	0.47	0.26 + 0.106*SL	0.25 + 0.109*SL	0.25 + 0.109*SL
	t_F	0.32	0.17 + 0.072*SL	0.17 + 0.074*SL	0.16 + 0.075*SL
RN to Q	t_{PHL}	0.96	0.74 + 0.109*SL	0.75 + 0.107*SL	0.75 + 0.107*SL
	t_F	0.36	0.18 + 0.092*SL	0.18 + 0.093*SL	0.17 + 0.093*SL
GN to Q	t_{PLH}	0.68	0.58 + 0.051*SL	0.58 + 0.050*SL	0.59 + 0.050*SL
	t_{PHL}	0.94	0.72 + 0.109*SL	0.73 + 0.107*SL	0.73 + 0.107*SL
	t_R	0.49	0.29 + 0.099*SL	0.28 + 0.103*SL	0.27 + 0.104*SL
	t_F	0.36	0.18 + 0.092*SL	0.18 + 0.093*SL	0.17 + 0.093*SL
SN to QN	t_{PHL}	0.96	0.74 + 0.108*SL	0.74 + 0.107*SL	0.75 + 0.107*SL
	t_F	0.37	0.18 + 0.091*SL	0.18 + 0.093*SL	0.18 + 0.093*SL
RN to QN	t_{PLH}	0.70	0.60 + 0.051*SL	0.60 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.39 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.47	0.26 + 0.106*SL	0.26 + 0.109*SL	0.25 + 0.109*SL
	t_F	0.32	0.18 + 0.071*SL	0.17 + 0.074*SL	0.16 + 0.075*SL
GN to QN	t_{PLH}	0.69	0.59 + 0.051*SL	0.59 + 0.050*SL	0.59 + 0.050*SL
	t_{PHL}	0.94	0.72 + 0.109*SL	0.72 + 0.107*SL	0.73 + 0.107*SL
	t_R	0.50	0.30 + 0.099*SL	0.29 + 0.103*SL	0.28 + 0.104*SL
	t_F	0.36	0.18 + 0.093*SL	0.18 + 0.093*SL	0.18 + 0.093*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Cell List

Cell Name	Function Description
BUSHOLDER	Bus Holder

Logic Symbol



Cell Data

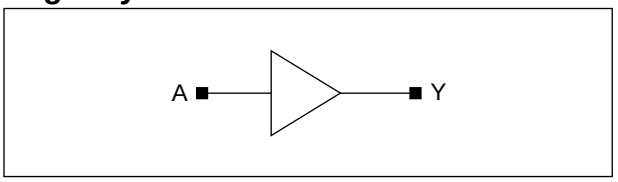
Input Load (SL)	Gate Count
KG80	
Y	
3.8	2.0
KGM80	
Y	
4.7	2.0

INTERNAL CLOCK DRIVERS

Cell List

Cell Name	Function Description
KG80	
CK2	Internal Clock Driver CMOS 2mA
CK4	Internal Clock Driver CMOS 4mA
CK8	Internal Clock Driver CMOS 8mA
CK12	Internal Clock Driver CMOS 12mA
KGM80	
CK2	Internal Clock Driver CMOS 2mA
CK4	Internal Clock Driver CMOS 4mA
CK6	Internal Clock Driver CMOS 6mA
CK8	Internal Clock Driver CMOS 8mA

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)				Gate Count			
KG80							
CK2	*CK4*	*CK8*	*CK12*	*CK2*	*CK4*	*CK8*	*CK12*
A	A	A	A				
3.1	3.1	5.5	5.5	1.0	1.0	1.0	1.0
KGM80							
CK2	*CK4*	*CK6*	*CK8*	*CK2*	*CK4*	*CK6*	*CK8*
A	A	A	A				
3.5	3.5	6.1	6.1	1.0	1.0	1.0	1.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 CK2

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.66	0.20 + 0.005*SL	0.20 + 0.005*SL	0.20 + 0.005*SL
	t_{PHL}	0.60	0.18 + 0.005*SL	0.18 + 0.005*SL	0.18 + 0.005*SL
	t_R	1.07	0.08 + 0.012*SL	0.07 + 0.012*SL	0.06 + 0.012*SL
	t_F	0.82	0.06 + 0.009*SL	0.06 + 0.009*SL	0.05 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 CK4

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.71	0.26 + 0.003*SL	0.26 + 0.003*SL	0.26 + 0.003*SL
	t_{PHL}	0.64	0.23 + 0.003*SL	0.24 + 0.002*SL	0.23 + 0.003*SL
	t_R	1.06	0.09 + 0.006*SL	0.08 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.82	0.08 + 0.004*SL	0.07 + 0.005*SL	0.06 + 0.005*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 CK8

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.70	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.67	0.26 + 0.001*SL	0.26 + 0.001*SL	0.26 + 0.001*SL
	t_R	1.05	0.09 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.003*SL
	t_F	0.82	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 CK12

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.75	0.31 + 0.001*SL	0.31 + 0.001*SL	0.31 + 0.001*SL
	t_{PHL}	0.72	0.31 + 0.001*SL	0.32 + 0.001*SL	0.32 + 0.001*SL
	t_R	1.06	0.12 + 0.002*SL	0.10 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.83	0.11 + 0.001*SL	0.10 + 0.001*SL	0.09 + 0.002*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 CK2

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.13	0.28 + 0.004*SL	0.28 + 0.004*SL	0.28 + 0.004*SL
	t_{PHL}	0.93	0.29 + 0.003*SL	0.29 + 0.003*SL	0.29 + 0.003*SL
	t_R	1.95	0.13 + 0.009*SL	0.10 + 0.010*SL	0.09 + 0.010*SL
	t_F	1.30	0.10 + 0.006*SL	0.09 + 0.006*SL	0.09 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

KGM80 CK4

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.23	0.39 + 0.002*SL	0.39 + 0.002*SL	0.39 + 0.002*SL
	t_{PHL}	1.03	0.39 + 0.002*SL	0.40 + 0.002*SL	0.40 + 0.002*SL
	t_R	1.95	0.17 + 0.005*SL	0.13 + 0.005*SL	0.13 + 0.005*SL
	t_F	1.31	0.16 + 0.003*SL	0.13 + 0.003*SL	0.10 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

KGM80 CK6

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.17	0.33 + 0.001*SL	0.33 + 0.001*SL	0.33 + 0.001*SL
	t_{PHL}	1.02	0.38 + 0.001*SL	0.38 + 0.001*SL	0.39 + 0.001*SL
	t_R	1.95	0.14 + 0.003*SL	0.12 + 0.003*SL	0.11 + 0.003*SL
	t_F	1.32	0.12 + 0.002*SL	0.13 + 0.002*SL	0.13 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

KGM80 CK8

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.22	0.38 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_{PHL}	1.08	0.43 + 0.001*SL	0.44 + 0.001*SL	0.45 + 0.001*SL
	t_R	1.95	0.17 + 0.002*SL	0.14 + 0.002*SL	0.13 + 0.002*SL
	t_F	1.33	0.15 + 0.002*SL	0.16 + 0.002*SL	0.15 + 0.002*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

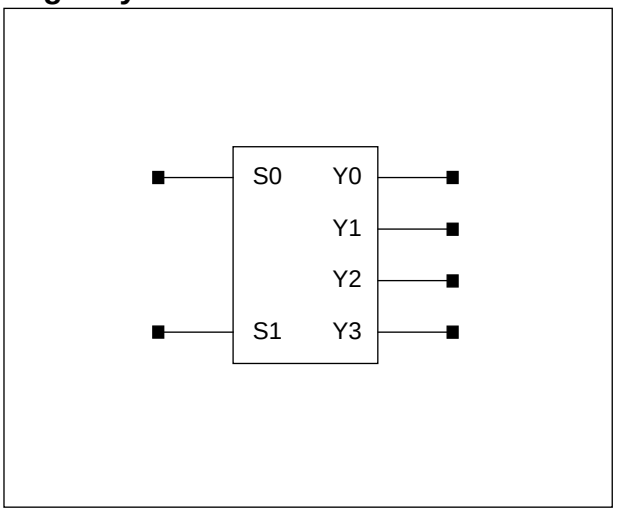
Cell List

Cell Name	Function Description
DC4	2 > 4 Non-Inverting Decoder
DC4I	2 > 4 Inverting Decoder
DC8I	3 > 8 Inverting Decoder

DC4

2 > 4 Non-Inverting Decoder

Logic Symbol



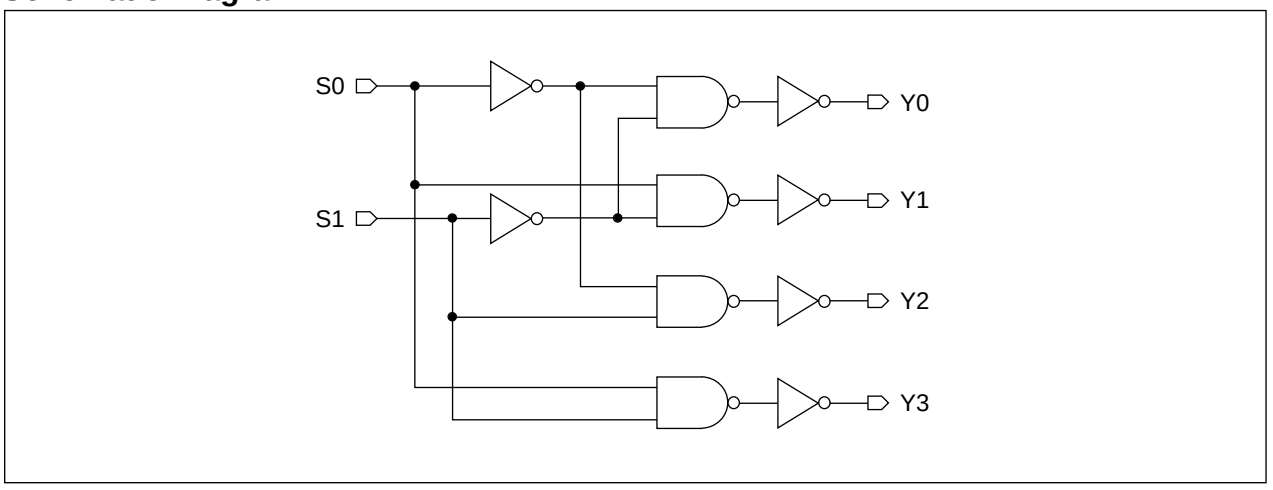
Truth Table

S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Cell Data

Input Load (SL)		Gate Count
KG80		
S0	S1	
2.3	2.6	7.0
KGM80		
S0	S1	
2.7	3.1	7.0

Schematic Diagram



Switching Characteristics

(Typical process, 25℃, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 DC4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to Y0	t_{PLH}	0.46	0.37 + 0.043*SL	0.37 + 0.042*SL	0.37 + 0.042*SL
	t_{PHL}	0.30	0.25 + 0.028*SL	0.25 + 0.024*SL	0.26 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.15	0.07 + 0.040*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
S1 to Y0	t_{PLH}	0.46	0.37 + 0.043*SL	0.38 + 0.041*SL	0.38 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.029*SL	0.28 + 0.024*SL	0.29 + 0.023*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
S0 to Y1	t_{PLH}	0.26	0.17 + 0.043*SL	0.18 + 0.041*SL	0.18 + 0.042*SL
	t_{PHL}	0.26	0.20 + 0.028*SL	0.21 + 0.024*SL	0.22 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.16	0.09 + 0.035*SL	0.08 + 0.040*SL	0.06 + 0.042*SL
S1 to Y1	t_{PLH}	0.46	0.37 + 0.042*SL	0.38 + 0.042*SL	0.37 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.029*SL	0.28 + 0.024*SL	0.29 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
S0 to Y2	t_{PLH}	0.46	0.36 + 0.046*SL	0.37 + 0.042*SL	0.38 + 0.042*SL
	t_{PHL}	0.30	0.25 + 0.028*SL	0.25 + 0.024*SL	0.26 + 0.023*SL
	t_R	0.28	0.13 + 0.074*SL	0.09 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.15	0.07 + 0.040*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
S1 to Y2	t_{PLH}	0.25	0.17 + 0.043*SL	0.17 + 0.041*SL	0.17 + 0.041*SL
	t_{PHL}	0.29	0.24 + 0.029*SL	0.25 + 0.024*SL	0.25 + 0.023*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.037*SL	0.09 + 0.039*SL	0.07 + 0.042*SL
S0 to Y3	t_{PLH}	0.26	0.18 + 0.043*SL	0.18 + 0.041*SL	0.18 + 0.042*SL
	t_{PHL}	0.26	0.21 + 0.028*SL	0.21 + 0.024*SL	0.22 + 0.023*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.16	0.09 + 0.035*SL	0.08 + 0.040*SL	0.07 + 0.042*SL
S1 to Y3	t_{PLH}	0.25	0.17 + 0.043*SL	0.17 + 0.041*SL	0.17 + 0.042*SL
	t_{PHL}	0.30	0.24 + 0.029*SL	0.25 + 0.024*SL	0.26 + 0.023*SL
	t_R	0.28	0.10 + 0.087*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.17	0.09 + 0.038*SL	0.09 + 0.039*SL	0.07 + 0.042*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

DC4

2 > 4 Non-Inverting Decoder

Switching Characteristics

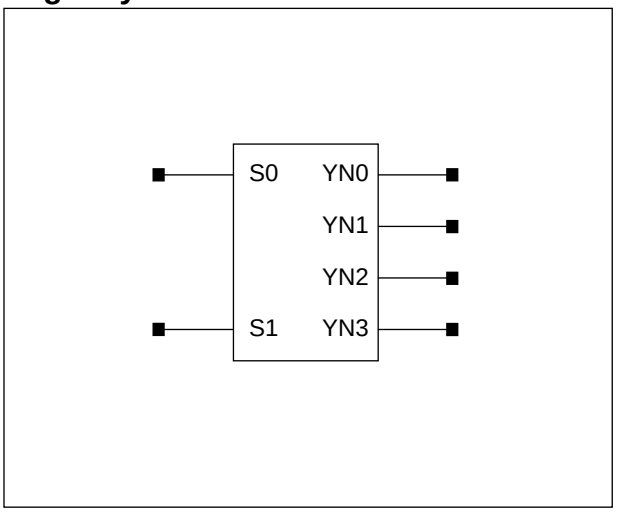
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 DC4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to Y0	t_{PLH}	0.61	0.50 + 0.052*SL	0.51 + 0.050*SL	0.51 + 0.050*SL
	t_{PHL}	0.40	0.34 + 0.030*SL	0.36 + 0.024*SL	0.37 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.18	0.09 + 0.042*SL	0.09 + 0.042*SL	0.08 + 0.043*SL
S1 to Y0	t_{PLH}	0.61	0.50 + 0.052*SL	0.51 + 0.050*SL	0.51 + 0.050*SL
	t_{PHL}	0.45	0.38 + 0.031*SL	0.40 + 0.025*SL	0.42 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.19	0.11 + 0.042*SL	0.11 + 0.041*SL	0.09 + 0.043*SL
S0 to Y1	t_{PLH}	0.34	0.24 + 0.052*SL	0.24 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.33	0.27 + 0.030*SL	0.28 + 0.024*SL	0.30 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.041*SL	0.08 + 0.043*SL
S1 to Y1	t_{PLH}	0.60	0.50 + 0.052*SL	0.51 + 0.050*SL	0.51 + 0.050*SL
	t_{PHL}	0.44	0.38 + 0.031*SL	0.40 + 0.025*SL	0.42 + 0.023*SL
	t_R	0.35	0.15 + 0.105*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.19	0.11 + 0.042*SL	0.11 + 0.041*SL	0.09 + 0.043*SL
S0 to Y2	t_{PLH}	0.60	0.50 + 0.052*SL	0.51 + 0.050*SL	0.51 + 0.050*SL
	t_{PHL}	0.40	0.34 + 0.030*SL	0.36 + 0.024*SL	0.37 + 0.023*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.18	0.09 + 0.043*SL	0.09 + 0.042*SL	0.08 + 0.043*SL
S1 to Y2	t_{PLH}	0.34	0.24 + 0.052*SL	0.25 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.37	0.31 + 0.031*SL	0.33 + 0.025*SL	0.35 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.19	0.11 + 0.039*SL	0.11 + 0.041*SL	0.09 + 0.043*SL
S0 to Y3	t_{PLH}	0.35	0.24 + 0.052*SL	0.25 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.33	0.27 + 0.030*SL	0.28 + 0.024*SL	0.30 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.041*SL	0.08 + 0.043*SL
S1 to Y3	t_{PLH}	0.34	0.24 + 0.052*SL	0.25 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.38	0.31 + 0.031*SL	0.33 + 0.025*SL	0.35 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.19	0.11 + 0.040*SL	0.11 + 0.041*SL	0.09 + 0.043*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



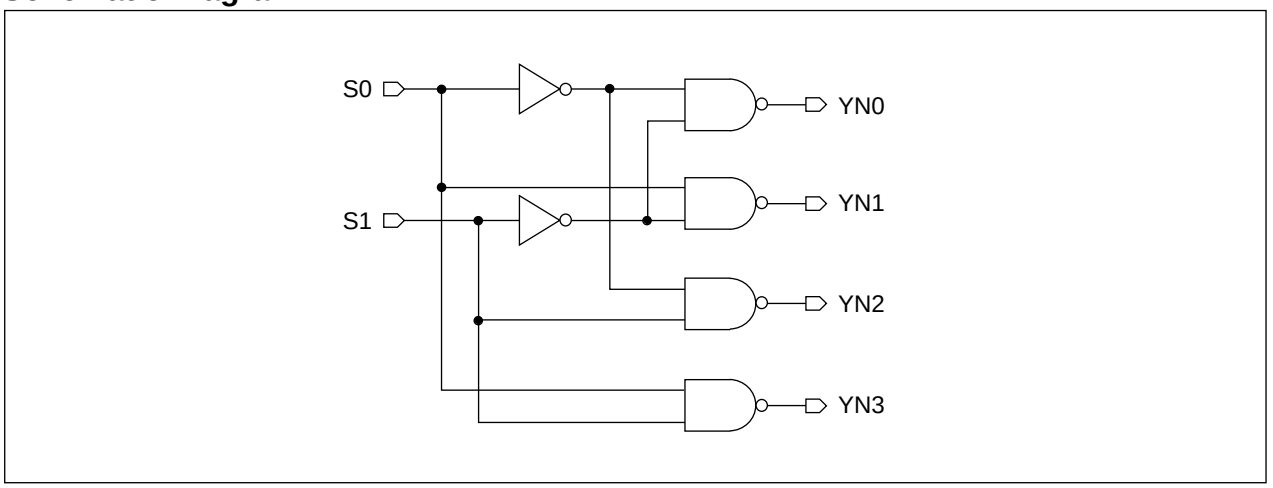
Truth Table

S1	S0	YN0	YN1	YN2	YN3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)		Gate Count
KG80		
S0	S1	
2.3	2.6	5.0
KGM80		
S0	S1	
2.7	3.0	5.0

Schematic Diagram



DC4I

2 > 4 Inverting Decoder

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 DC4I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.25	0.16 + 0.042*SL	0.17 + 0.041*SL	0.16 + 0.042*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.27 + 0.035*SL	0.28 + 0.034*SL
	t_R	0.27	0.11 + 0.082*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.24	0.11 + 0.063*SL	0.10 + 0.066*SL	0.09 + 0.068*SL
S1 to YN0	t_{PLH}	0.27	0.19 + 0.041*SL	0.19 + 0.041*SL	0.19 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.038*SL	0.27 + 0.035*SL	0.28 + 0.034*SL
	t_R	0.31	0.14 + 0.084*SL	0.13 + 0.089*SL	0.12 + 0.091*SL
	t_F	0.23	0.11 + 0.061*SL	0.10 + 0.066*SL	0.08 + 0.068*SL
S0 to YN1	t_{PLH}	0.22	0.12 + 0.046*SL	0.14 + 0.040*SL	0.13 + 0.041*SL
	t_{PHL}	0.15	0.06 + 0.045*SL	0.08 + 0.035*SL	0.09 + 0.034*SL
	t_R	0.32	0.17 + 0.076*SL	0.15 + 0.084*SL	0.12 + 0.088*SL
	t_F	0.29	0.17 + 0.059*SL	0.16 + 0.061*SL	0.13 + 0.065*SL
S1 to YN1	t_{PLH}	0.28	0.19 + 0.041*SL	0.19 + 0.041*SL	0.19 + 0.042*SL
	t_{PHL}	0.34	0.27 + 0.037*SL	0.27 + 0.035*SL	0.28 + 0.034*SL
	t_R	0.31	0.15 + 0.084*SL	0.13 + 0.089*SL	0.12 + 0.091*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.08 + 0.068*SL
S0 to YN2	t_{PLH}	0.25	0.16 + 0.042*SL	0.17 + 0.041*SL	0.16 + 0.042*SL
	t_{PHL}	0.34	0.26 + 0.039*SL	0.27 + 0.035*SL	0.27 + 0.034*SL
	t_R	0.27	0.11 + 0.082*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.066*SL	0.09 + 0.068*SL
S1 to YN2	t_{PLH}	0.24	0.16 + 0.042*SL	0.16 + 0.040*SL	0.16 + 0.041*SL
	t_{PHL}	0.14	0.05 + 0.041*SL	0.07 + 0.035*SL	0.08 + 0.034*SL
	t_R	0.36	0.21 + 0.074*SL	0.19 + 0.083*SL	0.16 + 0.088*SL
	t_F	0.27	0.15 + 0.056*SL	0.14 + 0.062*SL	0.11 + 0.066*SL
S0 to YN3	t_{PLH}	0.22	0.12 + 0.046*SL	0.14 + 0.040*SL	0.13 + 0.041*SL
	t_{PHL}	0.15	0.06 + 0.045*SL	0.08 + 0.035*SL	0.09 + 0.034*SL
	t_R	0.32	0.17 + 0.075*SL	0.15 + 0.084*SL	0.12 + 0.088*SL
	t_F	0.29	0.17 + 0.059*SL	0.16 + 0.061*SL	0.13 + 0.065*SL
S1 to YN3	t_{PLH}	0.24	0.16 + 0.041*SL	0.16 + 0.040*SL	0.16 + 0.041*SL
	t_{PHL}	0.14	0.06 + 0.041*SL	0.07 + 0.035*SL	0.08 + 0.034*SL
	t_R	0.36	0.21 + 0.075*SL	0.19 + 0.083*SL	0.16 + 0.088*SL
	t_F	0.27	0.16 + 0.055*SL	0.14 + 0.062*SL	0.11 + 0.066*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 DC4I

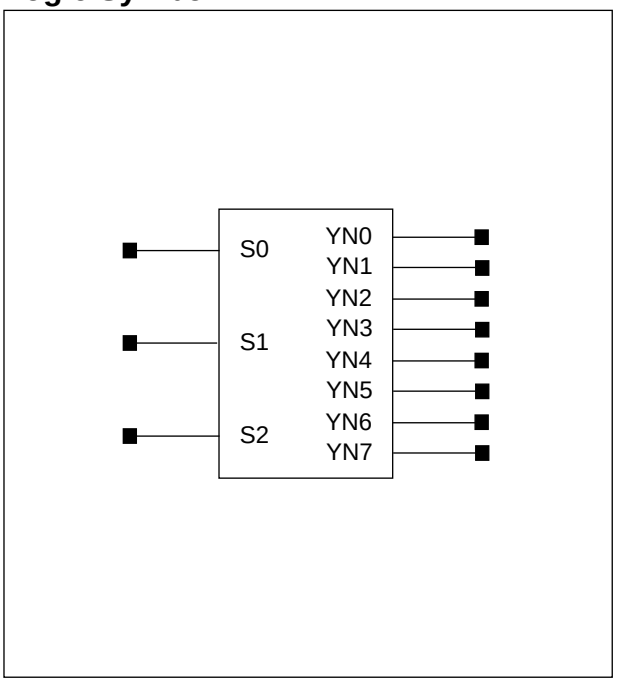
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.33	0.22 + 0.051*SL	0.23 + 0.050*SL	0.23 + 0.050*SL
	t_{PHL}	0.43	0.34 + 0.044*SL	0.36 + 0.038*SL	0.37 + 0.037*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.28	0.14 + 0.071*SL	0.14 + 0.072*SL	0.12 + 0.074*SL
S1 to YN0	t_{PLH}	0.36	0.26 + 0.051*SL	0.26 + 0.050*SL	0.27 + 0.050*SL
	t_{PHL}	0.43	0.35 + 0.042*SL	0.36 + 0.038*SL	0.37 + 0.037*SL
	t_R	0.40	0.18 + 0.105*SL	0.18 + 0.108*SL	0.17 + 0.109*SL
	t_F	0.27	0.13 + 0.070*SL	0.12 + 0.072*SL	0.10 + 0.074*SL
S0 to YN1	t_{PLH}	0.26	0.15 + 0.055*SL	0.16 + 0.049*SL	0.16 + 0.050*SL
	t_{PHL}	0.18	0.09 + 0.047*SL	0.11 + 0.038*SL	0.12 + 0.037*SL
	t_R	0.38	0.19 + 0.099*SL	0.17 + 0.105*SL	0.14 + 0.108*SL
	t_F	0.31	0.17 + 0.068*SL	0.17 + 0.070*SL	0.13 + 0.073*SL
S1 to YN1	t_{PLH}	0.37	0.26 + 0.051*SL	0.27 + 0.050*SL	0.27 + 0.050*SL
	t_{PHL}	0.43	0.35 + 0.042*SL	0.36 + 0.038*SL	0.37 + 0.037*SL
	t_R	0.40	0.19 + 0.106*SL	0.18 + 0.108*SL	0.17 + 0.109*SL
	t_F	0.27	0.13 + 0.069*SL	0.12 + 0.072*SL	0.11 + 0.074*SL
S0 to YN2	t_{PLH}	0.32	0.22 + 0.052*SL	0.23 + 0.050*SL	0.23 + 0.050*SL
	t_{PHL}	0.43	0.34 + 0.045*SL	0.36 + 0.038*SL	0.37 + 0.037*SL
	t_R	0.35	0.14 + 0.105*SL	0.13 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.28	0.14 + 0.070*SL	0.14 + 0.072*SL	0.12 + 0.074*SL
S1 to YN2	t_{PLH}	0.30	0.19 + 0.052*SL	0.20 + 0.049*SL	0.20 + 0.050*SL
	t_{PHL}	0.18	0.09 + 0.044*SL	0.11 + 0.038*SL	0.11 + 0.037*SL
	t_R	0.43	0.23 + 0.099*SL	0.22 + 0.105*SL	0.18 + 0.108*SL
	t_F	0.29	0.15 + 0.066*SL	0.14 + 0.071*SL	0.11 + 0.074*SL
S0 to YN3	t_{PLH}	0.26	0.15 + 0.055*SL	0.17 + 0.049*SL	0.16 + 0.050*SL
	t_{PHL}	0.18	0.09 + 0.047*SL	0.11 + 0.038*SL	0.12 + 0.037*SL
	t_R	0.39	0.19 + 0.098*SL	0.17 + 0.105*SL	0.14 + 0.108*SL
	t_F	0.31	0.17 + 0.068*SL	0.17 + 0.070*SL	0.13 + 0.073*SL
S1 to YN3	t_{PLH}	0.30	0.20 + 0.051*SL	0.20 + 0.049*SL	0.20 + 0.050*SL
	t_{PHL}	0.18	0.09 + 0.044*SL	0.10 + 0.038*SL	0.11 + 0.037*SL
	t_R	0.43	0.23 + 0.099*SL	0.22 + 0.105*SL	0.18 + 0.108*SL
	t_F	0.29	0.15 + 0.067*SL	0.14 + 0.071*SL	0.11 + 0.074*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

DC8I

3 > 8 Inverting Decoder

Logic Symbol



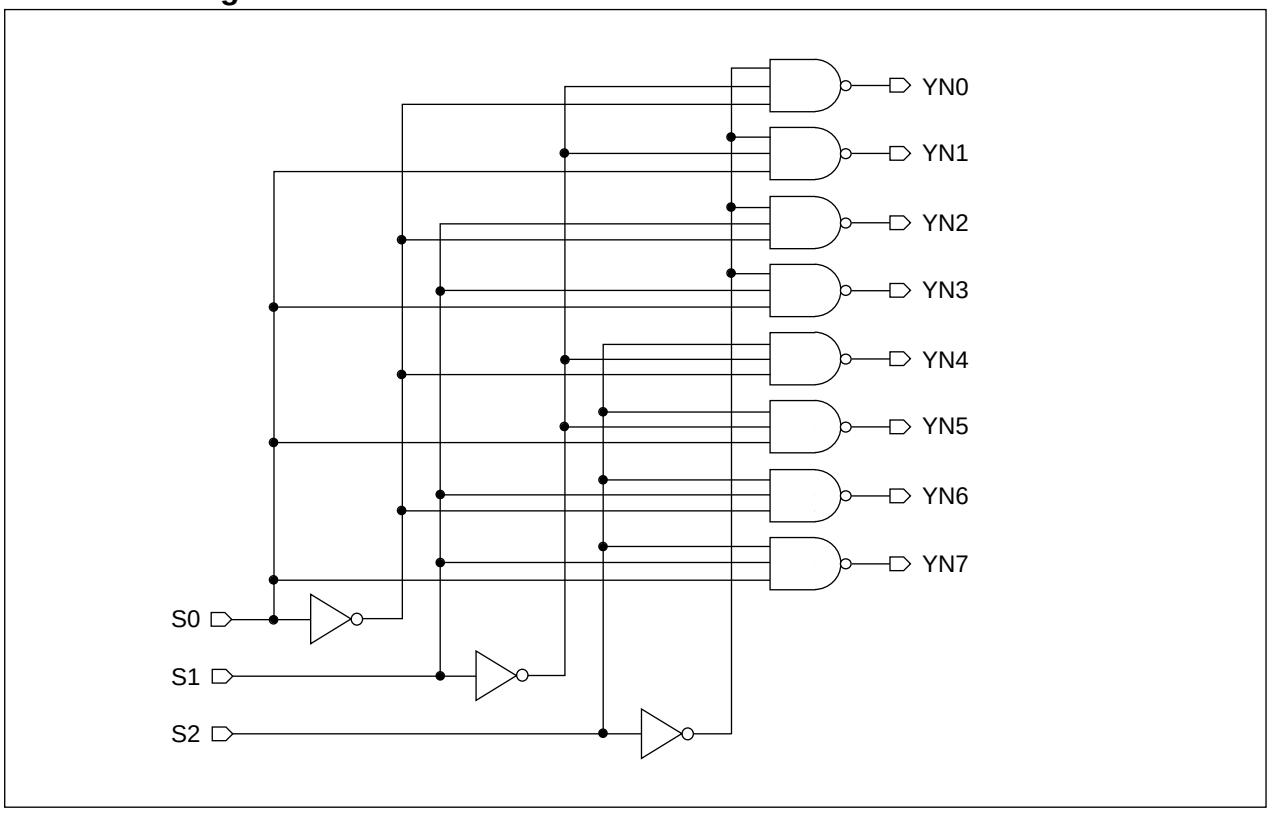
Truth Table

S0	S1	S2	YN 0	YN 1	YN 2	YN 3	YN 4	YN 5	YN 6	YN 7
0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Cell Data

Input Load (SL)			Gate Count
KG80			
S0	S1	S2	
3.5	3.2	2.9	14.0
KGM80			
S0	S1	S2	
4.1	3.8	3.4	14.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.38	0.29 + 0.043*SL	0.29 + 0.042*SL	0.29 + 0.042*SL
	t_{PHL}	0.48	0.38 + 0.047*SL	0.39 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.44	0.27 + 0.084*SL	0.26 + 0.088*SL	0.25 + 0.090*SL
	t_F	0.37	0.19 + 0.088*SL	0.18 + 0.092*SL	0.17 + 0.094*SL
S1 to YN0	t_{PLH}	0.34	0.26 + 0.042*SL	0.26 + 0.042*SL	0.26 + 0.042*SL
	t_{PHL}	0.46	0.36 + 0.047*SL	0.37 + 0.045*SL	0.37 + 0.045*SL
	t_R	0.38	0.21 + 0.085*SL	0.20 + 0.089*SL	0.19 + 0.090*SL
	t_F	0.37	0.20 + 0.087*SL	0.19 + 0.092*SL	0.18 + 0.094*SL
S2 to YN0	t_{PLH}	0.29	0.21 + 0.042*SL	0.21 + 0.041*SL	0.21 + 0.042*SL
	t_{PHL}	0.43	0.34 + 0.047*SL	0.34 + 0.045*SL	0.34 + 0.045*SL
	t_R	0.33	0.16 + 0.084*SL	0.15 + 0.089*SL	0.14 + 0.090*SL
	t_F	0.37	0.19 + 0.089*SL	0.19 + 0.092*SL	0.17 + 0.094*SL
S0 to YN1	t_{PLH}	0.30	0.21 + 0.041*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.22	0.13 + 0.047*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.48	0.32 + 0.078*SL	0.31 + 0.083*SL	0.28 + 0.088*SL
	t_F	0.38	0.21 + 0.084*SL	0.19 + 0.091*SL	0.17 + 0.094*SL
S1 to YN1	t_{PLH}	0.34	0.26 + 0.042*SL	0.26 + 0.042*SL	0.26 + 0.042*SL
	t_{PHL}	0.46	0.36 + 0.048*SL	0.37 + 0.045*SL	0.37 + 0.045*SL
	t_R	0.38	0.21 + 0.085*SL	0.20 + 0.089*SL	0.19 + 0.090*SL
	t_F	0.37	0.20 + 0.088*SL	0.19 + 0.092*SL	0.17 + 0.094*SL
S2 to YN1	t_{PLH}	0.29	0.21 + 0.042*SL	0.21 + 0.042*SL	0.21 + 0.042*SL
	t_{PHL}	0.43	0.34 + 0.047*SL	0.34 + 0.045*SL	0.34 + 0.045*SL
	t_R	0.33	0.16 + 0.084*SL	0.15 + 0.089*SL	0.14 + 0.091*SL
	t_F	0.37	0.19 + 0.089*SL	0.19 + 0.092*SL	0.17 + 0.094*SL
S0 to YN2	t_{PLH}	0.38	0.29 + 0.043*SL	0.29 + 0.042*SL	0.29 + 0.042*SL
	t_{PHL}	0.48	0.38 + 0.047*SL	0.39 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.44	0.27 + 0.084*SL	0.26 + 0.088*SL	0.25 + 0.090*SL
	t_F	0.37	0.19 + 0.088*SL	0.18 + 0.092*SL	0.17 + 0.094*SL
S1 to YN2	t_{PLH}	0.27	0.19 + 0.041*SL	0.19 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.22	0.13 + 0.048*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.42	0.27 + 0.076*SL	0.25 + 0.084*SL	0.22 + 0.088*SL
	t_F	0.39	0.23 + 0.083*SL	0.21 + 0.090*SL	0.18 + 0.093*SL
S2 to YN2	t_{PLH}	0.29	0.21 + 0.042*SL	0.21 + 0.042*SL	0.21 + 0.042*SL
	t_{PHL}	0.43	0.34 + 0.047*SL	0.34 + 0.045*SL	0.34 + 0.045*SL
	t_R	0.33	0.16 + 0.084*SL	0.15 + 0.089*SL	0.14 + 0.090*SL
	t_F	0.37	0.20 + 0.089*SL	0.19 + 0.092*SL	0.17 + 0.094*SL
S0 to YN3	t_{PLH}	0.29	0.21 + 0.041*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.22	0.13 + 0.047*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.48	0.32 + 0.078*SL	0.31 + 0.083*SL	0.28 + 0.088*SL
	t_F	0.38	0.21 + 0.085*SL	0.19 + 0.091*SL	0.17 + 0.094*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

DC8I

3 > 8 Inverting Decoder

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S1 to YN3	t_{PLH}	0.27	0.19 + 0.041*SL	0.19 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.22	0.13 + 0.048*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.42	0.27 + 0.076*SL	0.25 + 0.084*SL	0.22 + 0.088*SL
	t_F	0.39	0.23 + 0.082*SL	0.21 + 0.090*SL	0.18 + 0.093*SL
S2 to YN3	t_{PLH}	0.29	0.21 + 0.042*SL	0.21 + 0.042*SL	0.21 + 0.042*SL
	t_{PHL}	0.43	0.34 + 0.047*SL	0.34 + 0.045*SL	0.34 + 0.045*SL
	t_R	0.33	0.16 + 0.084*SL	0.15 + 0.089*SL	0.14 + 0.090*SL
	t_F	0.37	0.19 + 0.089*SL	0.19 + 0.092*SL	0.17 + 0.094*SL
S0 to YN4	t_{PLH}	0.38	0.29 + 0.043*SL	0.29 + 0.042*SL	0.29 + 0.042*SL
	t_{PHL}	0.48	0.39 + 0.047*SL	0.39 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.44	0.27 + 0.085*SL	0.26 + 0.088*SL	0.25 + 0.090*SL
	t_F	0.37	0.19 + 0.088*SL	0.18 + 0.093*SL	0.17 + 0.094*SL
S1 to YN4	t_{PLH}	0.34	0.26 + 0.041*SL	0.26 + 0.041*SL	0.25 + 0.042*SL
	t_{PHL}	0.46	0.36 + 0.048*SL	0.37 + 0.046*SL	0.37 + 0.045*SL
	t_R	0.38	0.21 + 0.084*SL	0.20 + 0.089*SL	0.19 + 0.090*SL
	t_F	0.37	0.20 + 0.087*SL	0.19 + 0.092*SL	0.17 + 0.094*SL
S2 to YN4	t_{PLH}	0.23	0.14 + 0.045*SL	0.15 + 0.041*SL	0.15 + 0.041*SL
	t_{PHL}	0.21	0.12 + 0.048*SL	0.13 + 0.044*SL	0.12 + 0.045*SL
	t_R	0.37	0.21 + 0.077*SL	0.20 + 0.084*SL	0.17 + 0.088*SL
	t_F	0.40	0.23 + 0.082*SL	0.22 + 0.089*SL	0.19 + 0.093*SL
S0 to YN5	t_{PLH}	0.30	0.21 + 0.041*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.22	0.13 + 0.047*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.48	0.32 + 0.078*SL	0.31 + 0.083*SL	0.28 + 0.088*SL
	t_F	0.38	0.21 + 0.085*SL	0.19 + 0.091*SL	0.17 + 0.094*SL
S1 to YN5	t_{PLH}	0.34	0.26 + 0.041*SL	0.26 + 0.041*SL	0.25 + 0.042*SL
	t_{PHL}	0.46	0.36 + 0.048*SL	0.37 + 0.046*SL	0.37 + 0.045*SL
	t_R	0.38	0.21 + 0.084*SL	0.20 + 0.089*SL	0.19 + 0.090*SL
	t_F	0.37	0.20 + 0.088*SL	0.19 + 0.092*SL	0.17 + 0.094*SL
S2 to YN5	t_{PLH}	0.23	0.14 + 0.045*SL	0.15 + 0.041*SL	0.15 + 0.041*SL
	t_{PHL}	0.21	0.12 + 0.048*SL	0.13 + 0.044*SL	0.12 + 0.045*SL
	t_R	0.37	0.21 + 0.077*SL	0.20 + 0.084*SL	0.17 + 0.088*SL
	t_F	0.40	0.24 + 0.081*SL	0.22 + 0.089*SL	0.19 + 0.093*SL
S0 to YN6	t_{PLH}	0.38	0.29 + 0.043*SL	0.29 + 0.042*SL	0.30 + 0.042*SL
	t_{PHL}	0.48	0.38 + 0.047*SL	0.39 + 0.046*SL	0.39 + 0.045*SL
	t_R	0.44	0.27 + 0.084*SL	0.26 + 0.088*SL	0.25 + 0.090*SL
	t_F	0.37	0.19 + 0.089*SL	0.18 + 0.093*SL	0.17 + 0.094*SL
S1 to YN6	t_{PLH}	0.27	0.19 + 0.041*SL	0.19 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.22	0.13 + 0.048*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.42	0.27 + 0.076*SL	0.25 + 0.084*SL	0.22 + 0.088*SL
	t_F	0.39	0.22 + 0.083*SL	0.21 + 0.090*SL	0.18 + 0.093*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to YN6	t_{PLH}	0.23	0.14 + 0.045*SL	0.15 + 0.041*SL	0.15 + 0.041*SL
	t_{PHL}	0.21	0.12 + 0.048*SL	0.13 + 0.044*SL	0.13 + 0.045*SL
	t_R	0.37	0.21 + 0.077*SL	0.19 + 0.084*SL	0.17 + 0.088*SL
	t_F	0.40	0.24 + 0.082*SL	0.22 + 0.089*SL	0.19 + 0.092*SL
S0 to YN7	t_{PLH}	0.29	0.21 + 0.040*SL	0.21 + 0.041*SL	0.21 + 0.041*SL
	t_{PHL}	0.22	0.13 + 0.047*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.48	0.32 + 0.079*SL	0.31 + 0.083*SL	0.28 + 0.088*SL
	t_F	0.38	0.20 + 0.086*SL	0.19 + 0.092*SL	0.18 + 0.094*SL
S1 to YN7	t_{PLH}	0.27	0.19 + 0.041*SL	0.19 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.22	0.12 + 0.048*SL	0.13 + 0.045*SL	0.13 + 0.045*SL
	t_R	0.42	0.27 + 0.076*SL	0.25 + 0.084*SL	0.22 + 0.088*SL
	t_F	0.39	0.22 + 0.083*SL	0.21 + 0.090*SL	0.18 + 0.093*SL
S2 to YN7	t_{PLH}	0.23	0.14 + 0.045*SL	0.15 + 0.041*SL	0.15 + 0.041*SL
	t_{PHL}	0.21	0.12 + 0.048*SL	0.13 + 0.044*SL	0.13 + 0.045*SL
	t_R	0.37	0.21 + 0.076*SL	0.19 + 0.084*SL	0.17 + 0.088*SL
	t_F	0.40	0.23 + 0.082*SL	0.22 + 0.089*SL	0.19 + 0.092*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

DC8I

3 > 8 Inverting Decoder

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.51	0.40 + 0.053*SL	0.41 + 0.051*SL	0.41 + 0.050*SL
	t_{PHL}	0.64	0.53 + 0.054*SL	0.54 + 0.052*SL	0.54 + 0.051*SL
	t_R	0.58	0.37 + 0.105*SL	0.36 + 0.107*SL	0.35 + 0.109*SL
	t_F	0.46	0.26 + 0.100*SL	0.25 + 0.103*SL	0.24 + 0.105*SL
S1 to YN0	t_{PLH}	0.45	0.35 + 0.051*SL	0.36 + 0.050*SL	0.36 + 0.050*SL
	t_{PHL}	0.61	0.50 + 0.055*SL	0.51 + 0.051*SL	0.51 + 0.051*SL
	t_R	0.50	0.29 + 0.105*SL	0.29 + 0.108*SL	0.28 + 0.109*SL
	t_F	0.47	0.27 + 0.100*SL	0.26 + 0.103*SL	0.24 + 0.105*SL
S2 to YN0	t_{PLH}	0.39	0.29 + 0.052*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.57	0.46 + 0.054*SL	0.47 + 0.051*SL	0.47 + 0.051*SL
	t_R	0.44	0.23 + 0.105*SL	0.22 + 0.108*SL	0.21 + 0.109*SL
	t_F	0.47	0.27 + 0.101*SL	0.26 + 0.103*SL	0.23 + 0.105*SL
S0 to YN1	t_{PLH}	0.38	0.28 + 0.052*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.31	0.20 + 0.054*SL	0.21 + 0.051*SL	0.21 + 0.051*SL
	t_R	0.60	0.41 + 0.100*SL	0.39 + 0.105*SL	0.36 + 0.108*SL
	t_F	0.46	0.26 + 0.099*SL	0.25 + 0.103*SL	0.23 + 0.105*SL
S1 to YN1	t_{PLH}	0.45	0.35 + 0.051*SL	0.36 + 0.050*SL	0.36 + 0.050*SL
	t_{PHL}	0.61	0.50 + 0.055*SL	0.51 + 0.051*SL	0.51 + 0.051*SL
	t_R	0.50	0.29 + 0.105*SL	0.29 + 0.108*SL	0.28 + 0.109*SL
	t_F	0.47	0.27 + 0.100*SL	0.26 + 0.103*SL	0.24 + 0.105*SL
S2 to YN1	t_{PLH}	0.39	0.29 + 0.051*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.57	0.46 + 0.054*SL	0.47 + 0.051*SL	0.47 + 0.051*SL
	t_R	0.44	0.23 + 0.105*SL	0.22 + 0.108*SL	0.21 + 0.109*SL
	t_F	0.47	0.27 + 0.099*SL	0.26 + 0.103*SL	0.23 + 0.105*SL
S0 to YN2	t_{PLH}	0.51	0.40 + 0.052*SL	0.41 + 0.051*SL	0.41 + 0.050*SL
	t_{PHL}	0.64	0.53 + 0.054*SL	0.54 + 0.052*SL	0.54 + 0.051*SL
	t_R	0.58	0.37 + 0.104*SL	0.36 + 0.107*SL	0.35 + 0.109*SL
	t_F	0.46	0.26 + 0.100*SL	0.25 + 0.103*SL	0.24 + 0.105*SL
S1 to YN2	t_{PLH}	0.34	0.24 + 0.050*SL	0.25 + 0.050*SL	0.24 + 0.050*SL
	t_{PHL}	0.30	0.19 + 0.054*SL	0.20 + 0.051*SL	0.20 + 0.051*SL
	t_R	0.53	0.33 + 0.100*SL	0.31 + 0.106*SL	0.28 + 0.108*SL
	t_F	0.46	0.27 + 0.097*SL	0.25 + 0.103*SL	0.23 + 0.105*SL
S2 to YN2	t_{PLH}	0.39	0.29 + 0.051*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.57	0.46 + 0.054*SL	0.47 + 0.051*SL	0.47 + 0.051*SL
	t_R	0.44	0.23 + 0.105*SL	0.22 + 0.108*SL	0.21 + 0.109*SL
	t_F	0.47	0.27 + 0.100*SL	0.26 + 0.103*SL	0.24 + 0.105*SL
S0 to YN3	t_{PLH}	0.38	0.28 + 0.051*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.31	0.20 + 0.054*SL	0.21 + 0.051*SL	0.21 + 0.051*SL
	t_R	0.60	0.40 + 0.101*SL	0.39 + 0.105*SL	0.35 + 0.108*SL
	t_F	0.45	0.25 + 0.100*SL	0.24 + 0.104*SL	0.23 + 0.105*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S1 to YN3	t_{PLH}	0.34	0.24 + 0.050*SL	0.25 + 0.050*SL	0.24 + 0.050*SL
	t_{PHL}	0.30	0.19 + 0.054*SL	0.20 + 0.051*SL	0.19 + 0.051*SL
	t_R	0.53	0.33 + 0.100*SL	0.31 + 0.106*SL	0.28 + 0.109*SL
	t_F	0.46	0.27 + 0.097*SL	0.25 + 0.103*SL	0.23 + 0.105*SL
S2 to YN3	t_{PLH}	0.39	0.29 + 0.051*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.57	0.46 + 0.054*SL	0.47 + 0.051*SL	0.47 + 0.051*SL
	t_R	0.44	0.23 + 0.105*SL	0.22 + 0.108*SL	0.21 + 0.109*SL
	t_F	0.47	0.27 + 0.100*SL	0.26 + 0.103*SL	0.24 + 0.105*SL
S0 to YN4	t_{PLH}	0.51	0.40 + 0.052*SL	0.41 + 0.051*SL	0.41 + 0.050*SL
	t_{PHL}	0.64	0.53 + 0.054*SL	0.54 + 0.052*SL	0.54 + 0.051*SL
	t_R	0.58	0.37 + 0.105*SL	0.36 + 0.108*SL	0.35 + 0.109*SL
	t_F	0.46	0.26 + 0.101*SL	0.25 + 0.104*SL	0.24 + 0.105*SL
S1 to YN4	t_{PLH}	0.46	0.35 + 0.051*SL	0.36 + 0.050*SL	0.36 + 0.050*SL
	t_{PHL}	0.61	0.50 + 0.055*SL	0.51 + 0.052*SL	0.51 + 0.051*SL
	t_R	0.50	0.30 + 0.104*SL	0.28 + 0.108*SL	0.28 + 0.109*SL
	t_F	0.47	0.27 + 0.100*SL	0.26 + 0.103*SL	0.24 + 0.105*SL
S2 to YN4	t_{PLH}	0.29	0.19 + 0.052*SL	0.20 + 0.050*SL	0.19 + 0.050*SL
	t_{PHL}	0.27	0.16 + 0.054*SL	0.17 + 0.050*SL	0.16 + 0.051*SL
	t_R	0.46	0.27 + 0.100*SL	0.25 + 0.105*SL	0.22 + 0.108*SL
	t_F	0.47	0.28 + 0.097*SL	0.26 + 0.102*SL	0.23 + 0.105*SL
S0 to YN5	t_{PLH}	0.38	0.28 + 0.052*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.31	0.20 + 0.054*SL	0.21 + 0.051*SL	0.21 + 0.051*SL
	t_R	0.61	0.40 + 0.100*SL	0.39 + 0.105*SL	0.36 + 0.108*SL
	t_F	0.45	0.25 + 0.100*SL	0.24 + 0.104*SL	0.23 + 0.105*SL
S1 to YN5	t_{PLH}	0.46	0.35 + 0.051*SL	0.36 + 0.050*SL	0.36 + 0.050*SL
	t_{PHL}	0.61	0.50 + 0.055*SL	0.51 + 0.052*SL	0.51 + 0.051*SL
	t_R	0.50	0.30 + 0.104*SL	0.29 + 0.108*SL	0.27 + 0.109*SL
	t_F	0.47	0.27 + 0.100*SL	0.26 + 0.103*SL	0.24 + 0.105*SL
S2 to YN5	t_{PLH}	0.29	0.19 + 0.052*SL	0.20 + 0.050*SL	0.19 + 0.050*SL
	t_{PHL}	0.27	0.16 + 0.054*SL	0.17 + 0.051*SL	0.17 + 0.051*SL
	t_R	0.46	0.26 + 0.100*SL	0.25 + 0.105*SL	0.22 + 0.108*SL
	t_F	0.47	0.28 + 0.098*SL	0.27 + 0.102*SL	0.23 + 0.105*SL
S0 to YN6	t_{PLH}	0.51	0.40 + 0.053*SL	0.41 + 0.051*SL	0.41 + 0.050*SL
	t_{PHL}	0.64	0.53 + 0.055*SL	0.54 + 0.052*SL	0.54 + 0.051*SL
	t_R	0.58	0.37 + 0.105*SL	0.36 + 0.107*SL	0.35 + 0.109*SL
	t_F	0.46	0.26 + 0.101*SL	0.25 + 0.104*SL	0.24 + 0.105*SL
S1 to YN6	t_{PLH}	0.34	0.24 + 0.050*SL	0.25 + 0.050*SL	0.24 + 0.050*SL
	t_{PHL}	0.29	0.19 + 0.054*SL	0.19 + 0.051*SL	0.20 + 0.051*SL
	t_R	0.53	0.33 + 0.100*SL	0.31 + 0.106*SL	0.28 + 0.109*SL
	t_F	0.46	0.27 + 0.098*SL	0.25 + 0.103*SL	0.24 + 0.105*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

(Continued)

DC8I

3 > 8 Inverting Decoder

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to YN6	t_{PLH}	0.29	0.19 + 0.052*SL	0.20 + 0.050*SL	0.19 + 0.050*SL
	t_{PHL}	0.27	0.16 + 0.055*SL	0.17 + 0.051*SL	0.17 + 0.051*SL
	t_R	0.46	0.27 + 0.100*SL	0.25 + 0.105*SL	0.22 + 0.108*SL
	t_F	0.48	0.28 + 0.097*SL	0.27 + 0.102*SL	0.24 + 0.105*SL
S0 to YN7	t_{PLH}	0.38	0.28 + 0.051*SL	0.29 + 0.050*SL	0.29 + 0.050*SL
	t_{PHL}	0.31	0.20 + 0.053*SL	0.21 + 0.051*SL	0.21 + 0.051*SL
	t_R	0.61	0.40 + 0.101*SL	0.39 + 0.105*SL	0.35 + 0.108*SL
	t_F	0.45	0.25 + 0.101*SL	0.24 + 0.104*SL	0.23 + 0.105*SL
S1 to YN7	t_{PLH}	0.34	0.24 + 0.050*SL	0.25 + 0.050*SL	0.24 + 0.050*SL
	t_{PHL}	0.29	0.19 + 0.054*SL	0.19 + 0.051*SL	0.20 + 0.051*SL
	t_R	0.53	0.33 + 0.100*SL	0.31 + 0.106*SL	0.28 + 0.109*SL
	t_F	0.46	0.27 + 0.098*SL	0.25 + 0.103*SL	0.24 + 0.105*SL
S2 to YN7	t_{PLH}	0.29	0.19 + 0.052*SL	0.20 + 0.050*SL	0.19 + 0.050*SL
	t_{PHL}	0.27	0.16 + 0.054*SL	0.17 + 0.051*SL	0.17 + 0.051*SL
	t_R	0.46	0.26 + 0.100*SL	0.25 + 0.105*SL	0.22 + 0.108*SL
	t_F	0.47	0.28 + 0.097*SL	0.27 + 0.102*SL	0.24 + 0.105*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

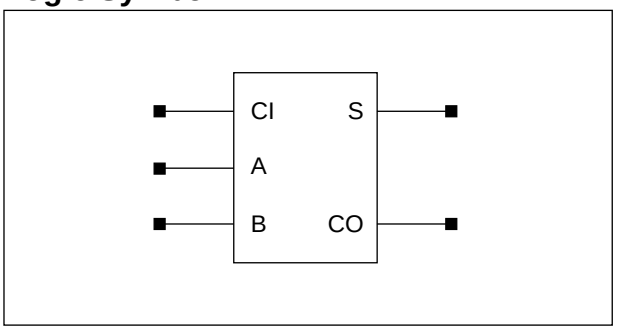
Cell List

Cell Name	Function Description
FA	Full Adder
FAD2	Full Adder with 2X Drive
HA	Half Adder
HAD2	Half Adder with 2X Drive

FA/FAD2

Full Adder with 1X/2X Drive

Logic Symbol



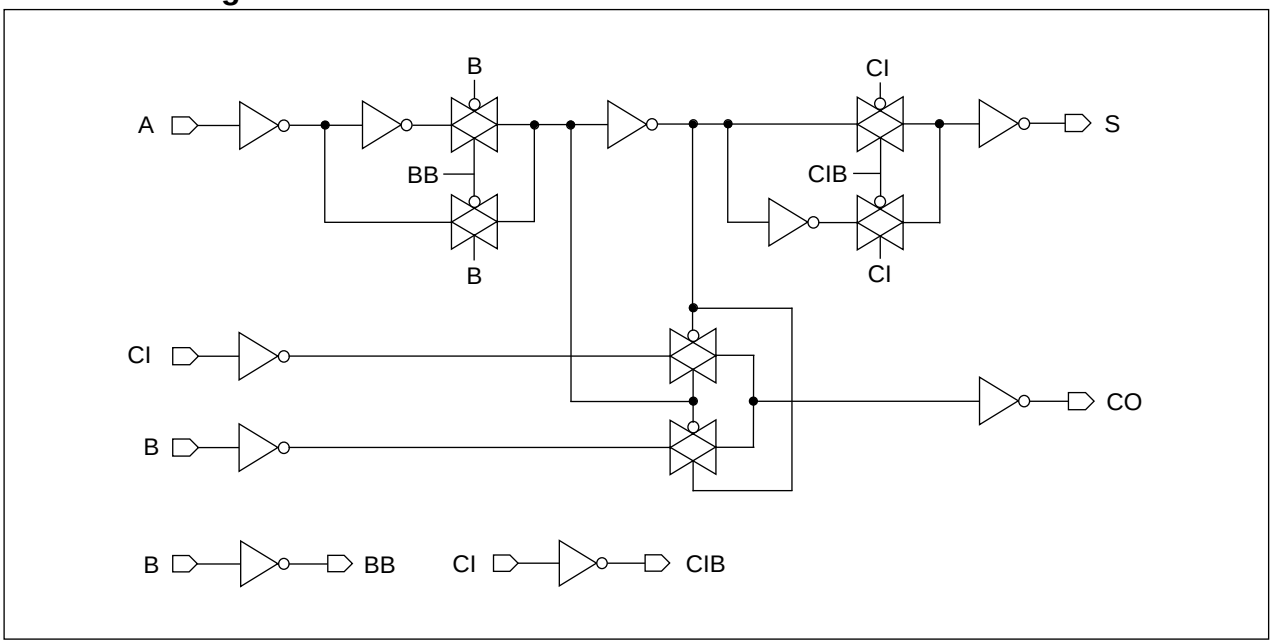
Truth Table

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	0	1	1	0
1	0	1	0	1
0	1	0	1	0
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
FA			*FAD2*			*FA*	*FAD2*
CI	A	B	CI	A	B		
1.7	0.8	1.7	1.8	0.8	1.7	7.0	8.0
KGM80							
FA			*FAD2*			*FA*	*FAD2*
CI	A	B	CI	A	B		
2.0	1.0	2.0	2.1	1.0	2.0	7.0	8.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.84	0.75 + 0.043*SL	0.75 + 0.041*SL	0.75 + 0.042*SL
	t_{PHL}	0.78	0.70 + 0.037*SL	0.72 + 0.028*SL	0.75 + 0.025*SL
	t_R	0.27	0.10 + 0.086*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.041*SL	0.12 + 0.041*SL
B to S	t_{PLH}	0.74	0.65 + 0.043*SL	0.66 + 0.041*SL	0.66 + 0.042*SL
	t_{PHL}	0.69	0.62 + 0.036*SL	0.64 + 0.028*SL	0.66 + 0.025*SL
	t_R	0.27	0.10 + 0.085*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.20	0.12 + 0.044*SL	0.12 + 0.041*SL	0.12 + 0.041*SL
CI to S	t_{PLH}	0.47	0.38 + 0.043*SL	0.39 + 0.041*SL	0.39 + 0.041*SL
	t_{PHL}	0.35	0.27 + 0.038*SL	0.29 + 0.028*SL	0.32 + 0.025*SL
	t_R	0.29	0.12 + 0.086*SL	0.11 + 0.087*SL	0.10 + 0.090*SL
	t_F	0.20	0.11 + 0.043*SL	0.12 + 0.041*SL	0.12 + 0.041*SL
A to CO	t_{PLH}	0.66	0.58 + 0.042*SL	0.58 + 0.041*SL	0.58 + 0.041*SL
	t_{PHL}	0.73	0.65 + 0.037*SL	0.67 + 0.028*SL	0.69 + 0.025*SL
	t_R	0.29	0.12 + 0.084*SL	0.12 + 0.087*SL	0.10 + 0.090*SL
	t_F	0.22	0.13 + 0.043*SL	0.14 + 0.040*SL	0.14 + 0.040*SL
B to CO	t_{PLH}	0.56	0.48 + 0.043*SL	0.48 + 0.041*SL	0.48 + 0.041*SL
	t_{PHL}	0.56	0.50 + 0.033*SL	0.51 + 0.027*SL	0.53 + 0.025*SL
	t_R	0.29	0.13 + 0.084*SL	0.12 + 0.087*SL	0.10 + 0.090*SL
	t_F	0.19	0.10 + 0.045*SL	0.11 + 0.041*SL	0.11 + 0.041*SL
CI to CO	t_{PLH}	0.35	0.26 + 0.044*SL	0.27 + 0.042*SL	0.27 + 0.041*SL
	t_{PHL}	0.41	0.34 + 0.039*SL	0.36 + 0.030*SL	0.39 + 0.025*SL
	t_R	0.29	0.13 + 0.080*SL	0.11 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.23	0.14 + 0.046*SL	0.15 + 0.041*SL	0.15 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 FAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.82	0.77 + 0.023*SL	0.78 + 0.021*SL	0.78 + 0.021*SL
	t_{PHL}	0.77	0.72 + 0.023*SL	0.73 + 0.018*SL	0.75 + 0.015*SL
	t_R	0.18	0.10 + 0.042*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.020*SL
B to S	t_{PLH}	0.72	0.67 + 0.024*SL	0.68 + 0.021*SL	0.68 + 0.021*SL
	t_{PHL}	0.69	0.64 + 0.023*SL	0.65 + 0.018*SL	0.68 + 0.015*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.042*SL	0.08 + 0.044*SL
	t_F	0.17	0.12 + 0.026*SL	0.13 + 0.022*SL	0.14 + 0.020*SL
CI to S	t_{PLH}	0.47	0.43 + 0.023*SL	0.43 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.34	0.29 + 0.024*SL	0.30 + 0.018*SL	0.33 + 0.015*SL
	t_R	0.20	0.12 + 0.040*SL	0.12 + 0.042*SL	0.11 + 0.043*SL
	t_F	0.17	0.12 + 0.023*SL	0.12 + 0.023*SL	0.14 + 0.021*SL
A to CO	t_{PLH}	0.67	0.62 + 0.024*SL	0.63 + 0.021*SL	0.63 + 0.020*SL
	t_{PHL}	0.72	0.67 + 0.025*SL	0.68 + 0.019*SL	0.71 + 0.015*SL
	t_R	0.21	0.13 + 0.040*SL	0.12 + 0.041*SL	0.11 + 0.043*SL
	t_F	0.19	0.13 + 0.027*SL	0.14 + 0.022*SL	0.16 + 0.020*SL
B to CO	t_{PLH}	0.57	0.52 + 0.024*SL	0.53 + 0.021*SL	0.54 + 0.020*SL
	t_{PHL}	0.58	0.53 + 0.023*SL	0.55 + 0.018*SL	0.57 + 0.015*SL
	t_R	0.21	0.13 + 0.040*SL	0.12 + 0.041*SL	0.11 + 0.043*SL
	t_F	0.16	0.12 + 0.024*SL	0.12 + 0.022*SL	0.13 + 0.021*SL
CI to CO	t_{PLH}	0.33	0.28 + 0.026*SL	0.29 + 0.022*SL	0.30 + 0.021*SL
	t_{PHL}	0.40	0.36 + 0.025*SL	0.37 + 0.019*SL	0.39 + 0.016*SL
	t_R	0.19	0.11 + 0.037*SL	0.10 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.19	0.14 + 0.028*SL	0.15 + 0.023*SL	0.17 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	1.16	1.05 + 0.053*SL	1.06 + 0.050*SL	1.06 + 0.050*SL
	t_{PHL}	1.12	1.03 + 0.044*SL	1.07 + 0.030*SL	1.12 + 0.025*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.048*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
B to S	t_{PLH}	1.03	0.92 + 0.053*SL	0.93 + 0.050*SL	0.93 + 0.050*SL
	t_{PHL}	0.99	0.90 + 0.044*SL	0.94 + 0.030*SL	1.00 + 0.025*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
CI to S	t_{PLH}	0.64	0.53 + 0.053*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_{PHL}	0.46	0.38 + 0.043*SL	0.41 + 0.030*SL	0.46 + 0.025*SL
	t_R	0.37	0.16 + 0.104*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.25	0.15 + 0.050*SL	0.17 + 0.042*SL	0.18 + 0.041*SL
A to CO	t_{PLH}	0.92	0.82 + 0.052*SL	0.83 + 0.050*SL	0.83 + 0.050*SL
	t_{PHL}	1.04	0.96 + 0.042*SL	0.99 + 0.030*SL	1.04 + 0.025*SL
	t_R	0.37	0.17 + 0.102*SL	0.16 + 0.107*SL	0.14 + 0.109*SL
	t_F	0.26	0.17 + 0.048*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
B to CO	t_{PLH}	0.80	0.70 + 0.052*SL	0.71 + 0.050*SL	0.71 + 0.050*SL
	t_{PHL}	0.78	0.71 + 0.038*SL	0.73 + 0.029*SL	0.78 + 0.025*SL
	t_R	0.37	0.17 + 0.103*SL	0.16 + 0.106*SL	0.14 + 0.109*SL
	t_F	0.23	0.13 + 0.048*SL	0.15 + 0.043*SL	0.16 + 0.042*SL
CI to CO	t_{PLH}	0.46	0.36 + 0.053*SL	0.36 + 0.050*SL	0.37 + 0.050*SL
	t_{PHL}	0.56	0.47 + 0.047*SL	0.51 + 0.032*SL	0.58 + 0.025*SL
	t_R	0.36	0.15 + 0.105*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.28	0.18 + 0.053*SL	0.21 + 0.042*SL	0.23 + 0.041*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

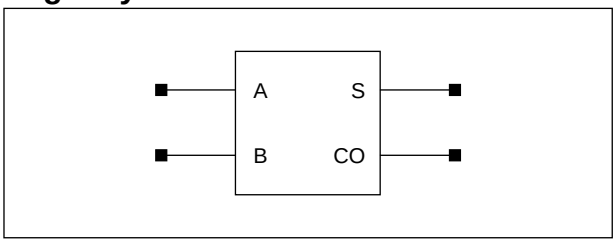
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 FAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	1.13	1.07 + 0.030*SL	1.08 + 0.026*SL	1.10 + 0.025*SL
	t_{PHL}	1.11	1.05 + 0.030*SL	1.08 + 0.020*SL	1.14 + 0.015*SL
	t_R	0.23	0.13 + 0.053*SL	0.13 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.22	0.16 + 0.031*SL	0.18 + 0.023*SL	0.21 + 0.021*SL
B to S	t_{PLH}	1.00	0.94 + 0.030*SL	0.95 + 0.026*SL	0.96 + 0.025*SL
	t_{PHL}	0.99	0.93 + 0.030*SL	0.96 + 0.020*SL	1.01 + 0.015*SL
	t_R	0.23	0.13 + 0.052*SL	0.13 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.22	0.16 + 0.030*SL	0.18 + 0.024*SL	0.21 + 0.021*SL
CI to S	t_{PLH}	0.65	0.59 + 0.029*SL	0.60 + 0.026*SL	0.61 + 0.025*SL
	t_{PHL}	0.45	0.39 + 0.030*SL	0.42 + 0.020*SL	0.47 + 0.015*SL
	t_R	0.25	0.14 + 0.053*SL	0.15 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.22	0.15 + 0.032*SL	0.18 + 0.024*SL	0.21 + 0.021*SL
A to CO	t_{PLH}	0.94	0.88 + 0.030*SL	0.89 + 0.026*SL	0.90 + 0.025*SL
	t_{PHL}	1.04	0.98 + 0.031*SL	1.01 + 0.021*SL	1.07 + 0.016*SL
	t_R	0.26	0.16 + 0.050*SL	0.15 + 0.051*SL	0.13 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.19 + 0.024*SL	0.22 + 0.021*SL
B to CO	t_{PLH}	0.82	0.76 + 0.029*SL	0.77 + 0.026*SL	0.78 + 0.025*SL
	t_{PHL}	0.82	0.77 + 0.027*SL	0.79 + 0.019*SL	0.84 + 0.015*SL
	t_R	0.26	0.16 + 0.050*SL	0.15 + 0.051*SL	0.13 + 0.053*SL
	t_F	0.21	0.15 + 0.027*SL	0.16 + 0.024*SL	0.19 + 0.021*SL
CI to CO	t_{PLH}	0.44	0.38 + 0.030*SL	0.39 + 0.026*SL	0.40 + 0.025*SL
	t_{PHL}	0.56	0.50 + 0.032*SL	0.52 + 0.022*SL	0.59 + 0.016*SL
	t_R	0.24	0.13 + 0.053*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.25	0.18 + 0.034*SL	0.20 + 0.025*SL	0.25 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



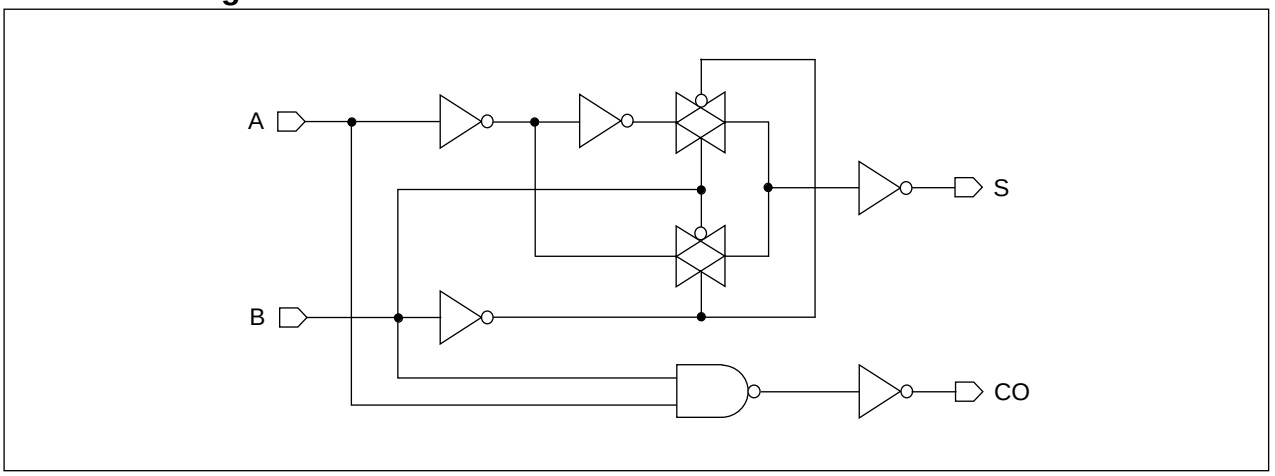
Truth Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Data

Input Load (SL)				Gate Count	
KG80					
HA		*HAD2*		*HA*	*HAD2*
A	B	A	B		
1.7	2.1	1.7	2.3	5.0	6.0
KGM80					
HA		*HAD2*		*HA*	*HAD2*
A	B	A	B		
2.0	2.7	2.0	2.7	5.0	6.0

Schematic Diagram



HA/HAD2

Half Adder with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 HA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.53	0.44 + 0.042*SL	0.44 + 0.041*SL	0.44 + 0.042*SL
	t_{PHL}	0.44	0.37 + 0.036*SL	0.38 + 0.029*SL	0.41 + 0.025*SL
	t_R	0.33	0.16 + 0.086*SL	0.15 + 0.089*SL	0.14 + 0.090*SL
	t_F	0.25	0.17 + 0.043*SL	0.17 + 0.040*SL	0.18 + 0.040*SL
B to S	t_{PLH}	0.41	0.32 + 0.043*SL	0.32 + 0.041*SL	0.32 + 0.042*SL
	t_{PHL}	0.33	0.27 + 0.031*SL	0.28 + 0.027*SL	0.30 + 0.025*SL
	t_R	0.33	0.16 + 0.083*SL	0.15 + 0.089*SL	0.14 + 0.090*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.042*SL	0.13 + 0.041*SL
A to CO	t_{PLH}	0.25	0.17 + 0.043*SL	0.17 + 0.041*SL	0.17 + 0.041*SL
	t_{PHL}	0.30	0.24 + 0.029*SL	0.25 + 0.024*SL	0.26 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.17	0.09 + 0.038*SL	0.09 + 0.039*SL	0.07 + 0.041*SL
B to CO	t_{PLH}	0.26	0.18 + 0.043*SL	0.18 + 0.041*SL	0.18 + 0.041*SL
	t_{PHL}	0.26	0.20 + 0.028*SL	0.22 + 0.024*SL	0.22 + 0.023*SL
	t_R	0.27	0.10 + 0.087*SL	0.10 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.16	0.09 + 0.036*SL	0.08 + 0.040*SL	0.06 + 0.042*SL

KG80 HAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.48	0.43 + 0.024*SL	0.44 + 0.021*SL	0.44 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.025*SL	0.37 + 0.019*SL	0.40 + 0.016*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.20	0.14 + 0.028*SL	0.15 + 0.022*SL	0.17 + 0.020*SL
B to S	t_{PLH}	0.36	0.31 + 0.025*SL	0.31 + 0.022*SL	0.32 + 0.021*SL
	t_{PHL}	0.30	0.26 + 0.022*SL	0.27 + 0.018*SL	0.29 + 0.015*SL
	t_R	0.18	0.11 + 0.036*SL	0.09 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.15	0.10 + 0.027*SL	0.11 + 0.023*SL	0.11 + 0.022*SL
A to CO	t_{PLH}	0.24	0.19 + 0.024*SL	0.20 + 0.021*SL	0.21 + 0.021*SL
	t_{PHL}	0.29	0.25 + 0.020*SL	0.27 + 0.015*SL	0.28 + 0.012*SL
	t_R	0.18	0.09 + 0.042*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.14	0.10 + 0.021*SL	0.10 + 0.019*SL	0.10 + 0.019*SL
B to CO	t_{PLH}	0.25	0.21 + 0.024*SL	0.21 + 0.021*SL	0.22 + 0.021*SL
	t_{PHL}	0.27	0.23 + 0.018*SL	0.24 + 0.014*SL	0.25 + 0.012*SL
	t_R	0.18	0.10 + 0.041*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.13	0.09 + 0.018*SL	0.09 + 0.019*SL	0.09 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 HA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.71	0.61 + 0.051*SL	0.61 + 0.050*SL	0.61 + 0.050*SL
	t_{PHL}	0.61	0.52 + 0.042*SL	0.55 + 0.030*SL	0.61 + 0.025*SL
	t_R	0.44	0.23 + 0.105*SL	0.22 + 0.108*SL	0.21 + 0.109*SL
	t_F	0.33	0.23 + 0.047*SL	0.25 + 0.041*SL	0.26 + 0.040*SL
B to S	t_{PLH}	0.54	0.44 + 0.052*SL	0.44 + 0.050*SL	0.44 + 0.050*SL
	t_{PHL}	0.44	0.37 + 0.035*SL	0.39 + 0.028*SL	0.42 + 0.025*SL
	t_R	0.44	0.23 + 0.105*SL	0.23 + 0.108*SL	0.21 + 0.109*SL
	t_F	0.26	0.17 + 0.049*SL	0.18 + 0.043*SL	0.19 + 0.042*SL
A to CO	t_{PLH}	0.34	0.24 + 0.052*SL	0.24 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.38	0.31 + 0.032*SL	0.33 + 0.025*SL	0.35 + 0.023*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.19	0.11 + 0.041*SL	0.11 + 0.041*SL	0.09 + 0.043*SL
B to CO	t_{PLH}	0.34	0.24 + 0.052*SL	0.25 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.33	0.27 + 0.031*SL	0.29 + 0.024*SL	0.30 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.18	0.10 + 0.041*SL	0.10 + 0.041*SL	0.08 + 0.043*SL

KGM80 HAD2

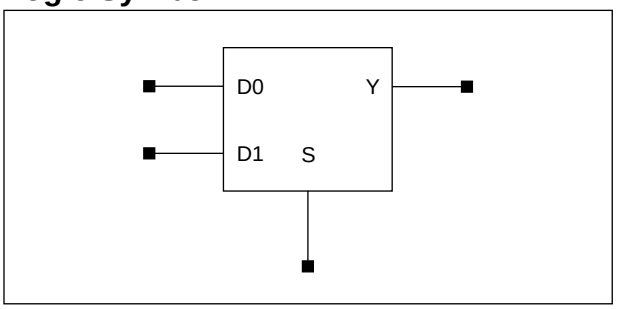
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.64	0.58 + 0.031*SL	0.59 + 0.026*SL	0.60 + 0.025*SL
	t_{PHL}	0.56	0.49 + 0.033*SL	0.52 + 0.022*SL	0.59 + 0.016*SL
	t_R	0.23	0.12 + 0.053*SL	0.13 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.25	0.18 + 0.032*SL	0.21 + 0.024*SL	0.24 + 0.021*SL
B to S	t_{PLH}	0.47	0.40 + 0.031*SL	0.42 + 0.026*SL	0.43 + 0.025*SL
	t_{PHL}	0.41	0.36 + 0.027*SL	0.38 + 0.020*SL	0.43 + 0.015*SL
	t_R	0.23	0.12 + 0.053*SL	0.13 + 0.052*SL	0.11 + 0.053*SL
	t_F	0.19	0.13 + 0.030*SL	0.14 + 0.025*SL	0.18 + 0.022*SL
A to CO	t_{PLH}	0.32	0.26 + 0.030*SL	0.28 + 0.026*SL	0.29 + 0.025*SL
	t_{PHL}	0.38	0.34 + 0.022*SL	0.36 + 0.015*SL	0.39 + 0.013*SL
	t_R	0.23	0.12 + 0.052*SL	0.12 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.16	0.11 + 0.024*SL	0.12 + 0.020*SL	0.12 + 0.020*SL
B to CO	t_{PLH}	0.33	0.27 + 0.030*SL	0.28 + 0.026*SL	0.29 + 0.025*SL
	t_{PHL}	0.34	0.30 + 0.021*SL	0.32 + 0.015*SL	0.34 + 0.012*SL
	t_R	0.23	0.12 + 0.052*SL	0.12 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Cell List

Cell Name	Function Description
MX2	2 > 1 Non-Inverting Mux
MX2D3	2 > 1 Non-Inverting Mux with 3X Drive
MX2X4	4-Bit 2 > 1 Non-Inverting Mux
YMX2	Fast 2 > 1 Non-Inverting Mux
YMX2D2	Fast 2 > 1 Non-Inverting Mux with 2X Drive
MX2I	2 > 1 Inverting Mux
MX2ID2	2 > 1 Inverting Mux with 2X Drive
MX2IA	2 > 1 Inverting Mux with Separate S and SN Inputs
MX2ID2A	2 > 1 Inverting Mux with Separate S and SN Inputs, 2X Drive
MX2IX4	4-Bit 2 > 1 Inverting Mux
MX3I	3 > 1 Inverting Mux
MX3ID2	3 > 1 Inverting Mux with 2X Drive
MX4	4 > 1 Non-Inverting Mux
MX4D2	4 > 1 Non-Inverting Mux with 2X Drive
YMX4	Fast 4 > 1 Non-Inverting Mux
YMX4D2	Fast 4 > 1 Non-Inverting Mux with 2X Drive
MX5	5 > 1 Non-Inverting Mux
MX5D2	5 > 1 Non-Inverting Mux with 2X Drive
MX8	8 > 1 Non-Inverting Mux
MX8D2	8 > 1 Non-Inverting Mux with 2X Drive
YMX8	Fast 8 > 1 Non-Inverting Mux
YMX8D2	Fast 8 > 1 Non-Inverting Mux with 2X Drive

Logic Symbol



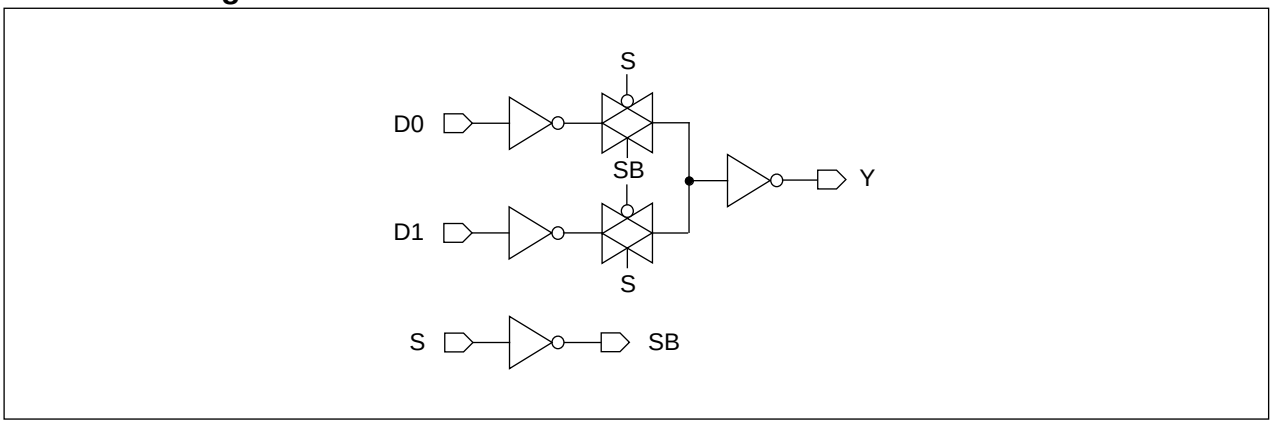
Truth Table

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
MX2			*MX2D3*			*MX2*	*MX2D3*
D0	D1	S	D0	D1	S		
0.9	0.9	1.4	0.9	0.9	1.4	3.0	4.0
KGM80							
MX2			*MX2D3*			*MX2*	*MX2D3*
D0	D1	S	D0	D1	S		
1.0	1.0	2.1	1.0	1.0	2.1	3.0	4.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.32	0.23 + 0.044*SL	0.24 + 0.041*SL	0.24 + 0.041*SL
	t_{PHL}	0.38	0.31 + 0.036*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
D1 to Y	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.23 + 0.041*SL
	t_{PHL}	0.38	0.30 + 0.037*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
S to Y	t_{PLH}	0.38	0.29 + 0.043*SL	0.29 + 0.041*SL	0.29 + 0.042*SL
	t_{PHL}	0.31	0.25 + 0.033*SL	0.26 + 0.028*SL	0.28 + 0.025*SL
	t_R	0.27	0.10 + 0.087*SL	0.10 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.18	0.10 + 0.044*SL	0.10 + 0.042*SL	0.10 + 0.041*SL

KG80 MX2D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.33	0.29 + 0.017*SL	0.30 + 0.015*SL	0.30 + 0.014*SL
	t_{PHL}	0.39	0.36 + 0.018*SL	0.37 + 0.014*SL	0.38 + 0.012*SL
	t_R	0.17	0.12 + 0.027*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_F	0.19	0.15 + 0.018*SL	0.15 + 0.016*SL	0.17 + 0.014*SL
D1 to Y	t_{PLH}	0.32	0.29 + 0.017*SL	0.29 + 0.015*SL	0.30 + 0.014*SL
	t_{PHL}	0.39	0.36 + 0.018*SL	0.37 + 0.014*SL	0.38 + 0.012*SL
	t_R	0.17	0.12 + 0.028*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_F	0.18	0.15 + 0.019*SL	0.15 + 0.016*SL	0.16 + 0.015*SL
S to Y	t_{PLH}	0.37	0.34 + 0.017*SL	0.34 + 0.015*SL	0.35 + 0.014*SL
	t_{PHL}	0.32	0.29 + 0.017*SL	0.30 + 0.014*SL	0.31 + 0.011*SL
	t_R	0.17	0.12 + 0.026*SL	0.12 + 0.028*SL	0.11 + 0.028*SL
	t_F	0.16	0.12 + 0.019*SL	0.12 + 0.017*SL	0.14 + 0.015*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.43	0.32 + 0.053*SL	0.33 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.043*SL	0.46 + 0.030*SL	0.52 + 0.025*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
D1 to Y	t_{PLH}	0.42	0.32 + 0.052*SL	0.32 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.043*SL	0.46 + 0.030*SL	0.51 + 0.025*SL
	t_R	0.35	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.048*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
S to Y	t_{PLH}	0.49	0.39 + 0.053*SL	0.39 + 0.050*SL	0.40 + 0.050*SL
	t_{PHL}	0.41	0.34 + 0.038*SL	0.36 + 0.029*SL	0.41 + 0.025*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.23	0.13 + 0.049*SL	0.15 + 0.043*SL	0.16 + 0.042*SL

KGM80 MX2D3

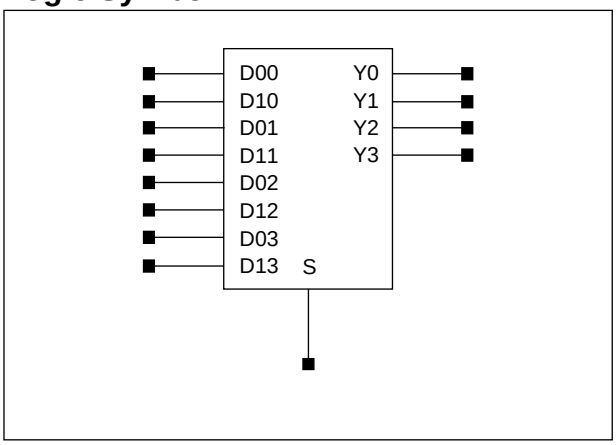
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.43	0.39 + 0.021*SL	0.39 + 0.018*SL	0.41 + 0.017*SL
	t_{PHL}	0.55	0.50 + 0.022*SL	0.52 + 0.016*SL	0.56 + 0.012*SL
	t_R	0.22	0.15 + 0.035*SL	0.15 + 0.035*SL	0.15 + 0.035*SL
	t_F	0.24	0.20 + 0.023*SL	0.21 + 0.018*SL	0.24 + 0.015*SL
D1 to Y	t_{PLH}	0.42	0.38 + 0.021*SL	0.39 + 0.018*SL	0.40 + 0.017*SL
	t_{PHL}	0.55	0.50 + 0.023*SL	0.52 + 0.016*SL	0.56 + 0.012*SL
	t_R	0.22	0.15 + 0.036*SL	0.15 + 0.035*SL	0.15 + 0.035*SL
	t_F	0.24	0.19 + 0.023*SL	0.21 + 0.018*SL	0.24 + 0.015*SL
S to Y	t_{PLH}	0.49	0.45 + 0.021*SL	0.45 + 0.018*SL	0.47 + 0.017*SL
	t_{PHL}	0.45	0.41 + 0.021*SL	0.43 + 0.016*SL	0.46 + 0.012*SL
	t_R	0.22	0.15 + 0.036*SL	0.15 + 0.035*SL	0.15 + 0.035*SL
	t_F	0.21	0.16 + 0.024*SL	0.18 + 0.019*SL	0.21 + 0.016*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

MX2X4

4-Bit 2 > 1 Non-Inverting MUX

Logic Symbol



Truth Table

S	Y0	Y1	Y2	Y3
0	D00	D01	D02	D03
1	D10	D11	D12	D13

Cell Data

Input Load (SL)									Gate Count
KG80									
MX2X4									*MX2X4*
D00	D10	D01	D11	D02	D12	D03	D13	S	
0.9	1.0	0.9	1.0	0.9	1.0	0.8	1.0	3.4	9.0
KGM80									
MX2X4									*MX2X4*
D00	D10	D01	D11	D02	D12	D03	D13	S	
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	4.4	9.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to Y0	t_{PLH}	0.32	0.23 + 0.043*SL	0.23 + 0.041*SL	0.23 + 0.041*SL
	t_{PHL}	0.37	0.30 + 0.037*SL	0.32 + 0.028*SL	0.34 + 0.025*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.041*SL	0.13 + 0.040*SL
D10 to Y0	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.23 + 0.042*SL
	t_{PHL}	0.37	0.30 + 0.037*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.27	0.11 + 0.081*SL	0.09 + 0.089*SL	0.08 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.12 + 0.041*SL	0.13 + 0.040*SL
S to Y0	t_{PLH}	0.46	0.37 + 0.043*SL	0.38 + 0.041*SL	0.38 + 0.041*SL
	t_{PHL}	0.33	0.26 + 0.036*SL	0.28 + 0.028*SL	0.30 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.10 + 0.045*SL	0.11 + 0.041*SL	0.11 + 0.041*SL
D01 to Y1	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.24 + 0.041*SL
	t_{PHL}	0.38	0.30 + 0.036*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.11 + 0.088*SL	0.11 + 0.087*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
D11 to Y1	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.23 + 0.042*SL
	t_{PHL}	0.38	0.30 + 0.037*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.040*SL	0.13 + 0.040*SL
S to Y1	t_{PLH}	0.46	0.37 + 0.043*SL	0.38 + 0.041*SL	0.38 + 0.041*SL
	t_{PHL}	0.33	0.26 + 0.036*SL	0.28 + 0.028*SL	0.30 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.10 + 0.045*SL	0.11 + 0.041*SL	0.12 + 0.041*SL
D02 to Y2	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.24 + 0.041*SL
	t_{PHL}	0.38	0.30 + 0.036*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.11 + 0.088*SL	0.11 + 0.087*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
D12 to Y2	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.24 + 0.041*SL
	t_{PHL}	0.38	0.30 + 0.037*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.11 + 0.082*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.040*SL	0.13 + 0.040*SL
S to Y2	t_{PLH}	0.46	0.37 + 0.043*SL	0.38 + 0.041*SL	0.38 + 0.041*SL
	t_{PHL}	0.33	0.26 + 0.035*SL	0.28 + 0.028*SL	0.30 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.10 + 0.045*SL	0.11 + 0.041*SL	0.12 + 0.041*SL
D03 to Y3	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.23 + 0.042*SL
	t_{PHL}	0.38	0.30 + 0.036*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.11 + 0.087*SL	0.11 + 0.087*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.040*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to Y3	t_{PLH}	0.32	0.23 + 0.043*SL	0.24 + 0.041*SL	0.24 + 0.041*SL
	t_{PHL}	0.38	0.31 + 0.036*SL	0.32 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.040*SL	0.13 + 0.040*SL
S to Y3	t_{PLH}	0.46	0.37 + 0.043*SL	0.38 + 0.041*SL	0.38 + 0.041*SL
	t_{PHL}	0.33	0.26 + 0.036*SL	0.28 + 0.028*SL	0.30 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.19	0.10 + 0.045*SL	0.11 + 0.042*SL	0.12 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to Y0	t_{PLH}	0.42	0.31 + 0.052*SL	0.32 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.50	0.42 + 0.043*SL	0.45 + 0.030*SL	0.51 + 0.025*SL
	t_R	0.35	0.14 + 0.103*SL	0.13 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
D10 to Y0	t_{PLH}	0.42	0.31 + 0.052*SL	0.32 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.043*SL	0.46 + 0.030*SL	0.51 + 0.025*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.048*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
S to Y0	t_{PLH}	0.62	0.52 + 0.052*SL	0.52 + 0.050*SL	0.53 + 0.050*SL
	t_{PHL}	0.44	0.36 + 0.042*SL	0.39 + 0.030*SL	0.45 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.24	0.14 + 0.051*SL	0.16 + 0.042*SL	0.17 + 0.041*SL
D01 to Y1	t_{PLH}	0.42	0.32 + 0.053*SL	0.33 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.043*SL	0.46 + 0.030*SL	0.51 + 0.025*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
D11 to Y1	t_{PLH}	0.42	0.32 + 0.052*SL	0.32 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.51	0.43 + 0.043*SL	0.46 + 0.030*SL	0.52 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.17 + 0.048*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
S to Y1	t_{PLH}	0.62	0.52 + 0.052*SL	0.53 + 0.050*SL	0.53 + 0.050*SL
	t_{PHL}	0.45	0.36 + 0.042*SL	0.40 + 0.029*SL	0.45 + 0.025*SL
	t_R	0.37	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.25	0.14 + 0.050*SL	0.17 + 0.042*SL	0.18 + 0.041*SL
D02 to Y2	t_{PLH}	0.42	0.32 + 0.052*SL	0.32 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.043*SL	0.46 + 0.030*SL	0.51 + 0.025*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
D12 to Y2	t_{PLH}	0.42	0.32 + 0.052*SL	0.32 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.51	0.43 + 0.043*SL	0.46 + 0.030*SL	0.52 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.17 + 0.047*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
S to Y2	t_{PLH}	0.62	0.52 + 0.052*SL	0.53 + 0.050*SL	0.53 + 0.050*SL
	t_{PHL}	0.45	0.36 + 0.042*SL	0.40 + 0.030*SL	0.45 + 0.025*SL
	t_R	0.36	0.16 + 0.102*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.24	0.14 + 0.050*SL	0.17 + 0.042*SL	0.17 + 0.042*SL
D03 to Y3	t_{PLH}	0.42	0.32 + 0.052*SL	0.32 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.043*SL	0.46 + 0.030*SL	0.51 + 0.025*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

(Continued)

MX2X4

4-Bit 2 > 1 Non-Inverting MUX

Switching Characteristics

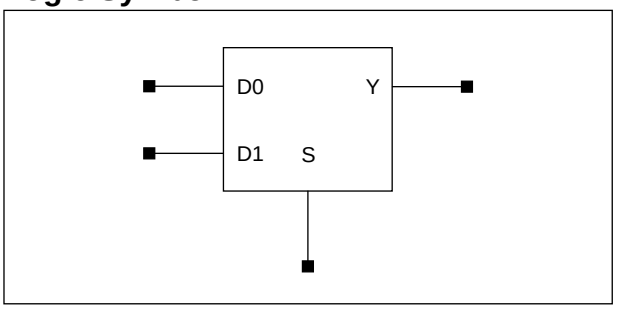
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to Y3	t_{PLH}	0.42	0.32 + 0.052*SL	0.32 + 0.050*SL	0.32 + 0.050*SL
	t_{PHL}	0.51	0.42 + 0.043*SL	0.46 + 0.030*SL	0.52 + 0.025*SL
	t_R	0.35	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.26	0.17 + 0.048*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
S to Y3	t_{PLH}	0.62	0.52 + 0.053*SL	0.53 + 0.050*SL	0.53 + 0.050*SL
	t_{PHL}	0.45	0.36 + 0.042*SL	0.40 + 0.030*SL	0.45 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.24	0.14 + 0.050*SL	0.17 + 0.042*SL	0.17 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



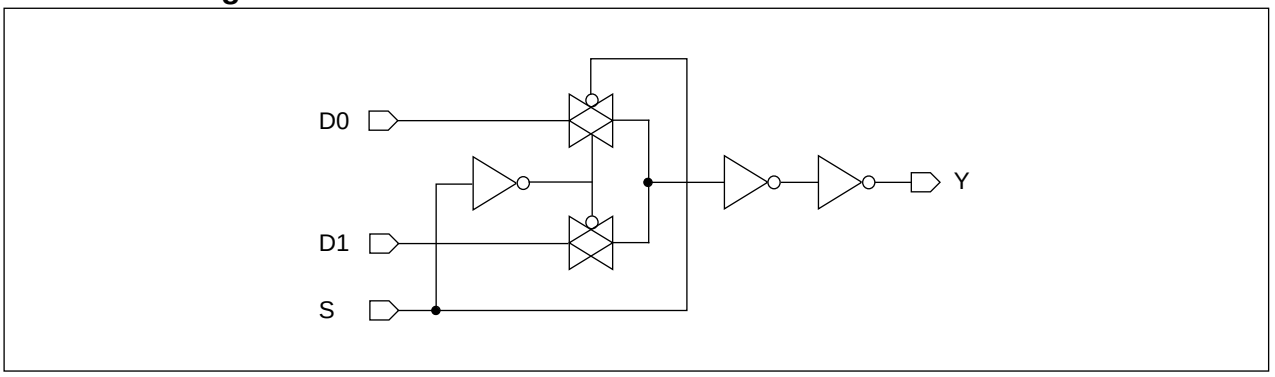
Truth Table

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)						Gate Count	
KG80							
YMX2			*YMX2D2*			*YMX2*	*YMX2D2*
D0	D1	S	D0	D1	S		
2.9	2.9	1.5	2.9	2.9	1.5	3.0	30
KGM80							
YMX2			*YMX2D2*			*YMX2*	*YMX2D2*
D0	D1	S	D0	D1	S		
3.7	3.7	1.7	3.7	3.7	1.7	3.0	3.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YMX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.23	0.15 + 0.041*SL	0.15 + 0.041*SL	0.15 + 0.042*SL
	t_{PHL}	0.29	0.23 + 0.027*SL	0.24 + 0.024*SL	0.25 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.15	0.08 + 0.037*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
D1 to Y	t_{PLH}	0.24	0.15 + 0.042*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
	t_{PHL}	0.28	0.23 + 0.028*SL	0.24 + 0.024*SL	0.24 + 0.023*SL
	t_R	0.26	0.09 + 0.086*SL	0.08 + 0.090*SL	0.07 + 0.091*SL
	t_F	0.15	0.07 + 0.039*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
S to Y	t_{PLH}	0.37	0.29 + 0.042*SL	0.29 + 0.042*SL	0.29 + 0.042*SL
	t_{PHL}	0.39	0.33 + 0.027*SL	0.34 + 0.024*SL	0.35 + 0.023*SL
	t_R	0.26	0.09 + 0.085*SL	0.08 + 0.089*SL	0.07 + 0.091*SL
	t_F	0.14	0.06 + 0.040*SL	0.06 + 0.041*SL	0.05 + 0.042*SL

KG80 YMX2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.23	0.19 + 0.021*SL	0.19 + 0.021*SL	0.19 + 0.021*SL
	t_{PHL}	0.29	0.26 + 0.016*SL	0.27 + 0.014*SL	0.28 + 0.012*SL
	t_R	0.18	0.09 + 0.044*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.13	0.08 + 0.021*SL	0.09 + 0.019*SL	0.08 + 0.020*SL
D1 to Y	t_{PLH}	0.23	0.19 + 0.021*SL	0.19 + 0.021*SL	0.19 + 0.021*SL
	t_{PHL}	0.29	0.26 + 0.017*SL	0.27 + 0.013*SL	0.27 + 0.012*SL
	t_R	0.18	0.09 + 0.043*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.12	0.09 + 0.019*SL	0.09 + 0.019*SL	0.08 + 0.020*SL
S to Y	t_{PLH}	0.36	0.32 + 0.021*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.39	0.36 + 0.016*SL	0.36 + 0.014*SL	0.37 + 0.012*SL
	t_R	0.17	0.09 + 0.042*SL	0.08 + 0.045*SL	0.08 + 0.046*SL
	t_F	0.12	0.08 + 0.019*SL	0.08 + 0.020*SL	0.08 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YMX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.34	0.24 + 0.051*SL	0.24 + 0.050*SL	0.24 + 0.050*SL
	t_{PHL}	0.37	0.31 + 0.030*SL	0.33 + 0.024*SL	0.34 + 0.023*SL
	t_R	0.33	0.13 + 0.104*SL	0.11 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.042*SL	0.07 + 0.043*SL
D1 to Y	t_{PLH}	0.35	0.25 + 0.050*SL	0.25 + 0.050*SL	0.25 + 0.050*SL
	t_{PHL}	0.37	0.31 + 0.030*SL	0.32 + 0.024*SL	0.33 + 0.023*SL
	t_R	0.33	0.12 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.042*SL	0.07 + 0.043*SL
S to Y	t_{PLH}	0.49	0.39 + 0.051*SL	0.39 + 0.050*SL	0.39 + 0.050*SL
	t_{PHL}	0.51	0.45 + 0.029*SL	0.46 + 0.024*SL	0.47 + 0.023*SL
	t_R	0.33	0.12 + 0.107*SL	0.11 + 0.109*SL	0.11 + 0.109*SL
	t_F	0.16	0.08 + 0.042*SL	0.08 + 0.042*SL	0.07 + 0.043*SL

KGM80 YMX2D2

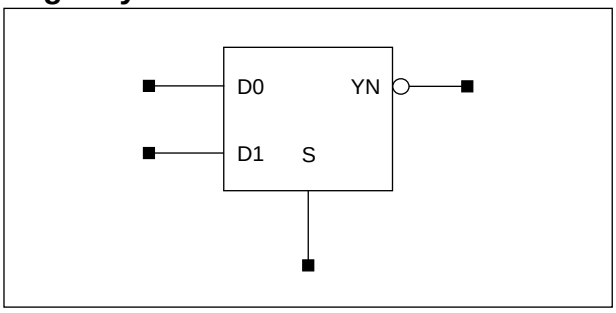
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.33	0.28 + 0.026*SL	0.29 + 0.025*SL	0.29 + 0.025*SL
	t_{PHL}	0.39	0.35 + 0.019*SL	0.37 + 0.014*SL	0.39 + 0.012*SL
	t_R	0.23	0.13 + 0.050*SL	0.12 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
D1 to Y	t_{PLH}	0.34	0.29 + 0.026*SL	0.29 + 0.025*SL	0.29 + 0.025*SL
	t_{PHL}	0.39	0.35 + 0.019*SL	0.36 + 0.014*SL	0.38 + 0.012*SL
	t_R	0.23	0.13 + 0.050*SL	0.12 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
S to Y	t_{PLH}	0.47	0.42 + 0.025*SL	0.42 + 0.025*SL	0.42 + 0.025*SL
	t_{PHL}	0.52	0.48 + 0.019*SL	0.50 + 0.014*SL	0.52 + 0.012*SL
	t_R	0.22	0.12 + 0.051*SL	0.12 + 0.053*SL	0.11 + 0.054*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.020*SL	0.10 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

MX2I/MX2ID2

2 > 1 Inverting MUX with 1X/2X Drive

Logic Symbol



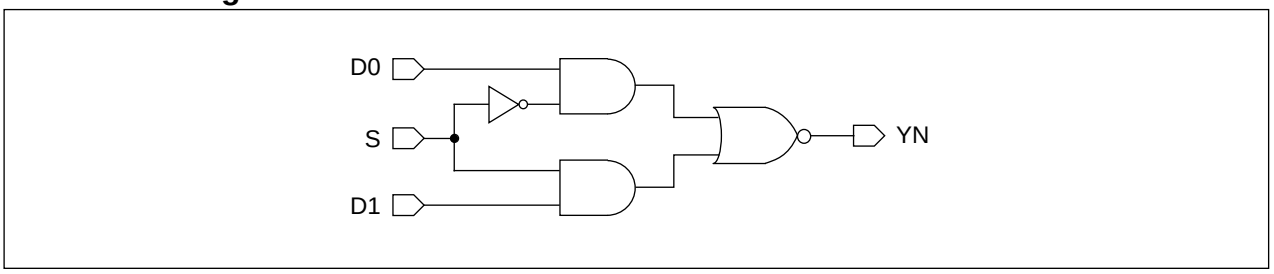
Truth Table

D0	D1	S	YN
0	x	0	1
1	x	0	0
x	0	1	1
x	1	1	0

Cell Data

Input Load (SL)						Gate Count	
KG80							
MX2I			*MX2ID2*			*MX2I*	*MX2ID2*
D0	D1	S	D0	D1	S		
0.9	0.8	1.7	0.9	0.9	1.4	3.0	4.0
KGM80							
MX2I			*MX2ID2*			*MX2I*	*MX2ID2*
D0	D1	S	D0	D1	S		
1.0	1.0	2.0	1.0	1.0	2.1	3.0	4.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX2I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.36	0.22 + 0.068*SL	0.22 + 0.070*SL	0.21 + 0.071*SL
	t_{PHL}	0.17	0.09 + 0.043*SL	0.11 + 0.034*SL	0.11 + 0.034*SL
	t_R	0.64	0.33 + 0.155*SL	0.32 + 0.160*SL	0.29 + 0.163*SL
	t_F	0.34	0.23 + 0.056*SL	0.21 + 0.062*SL	0.19 + 0.065*SL
D1 to YN	t_{PLH}	0.41	0.27 + 0.072*SL	0.27 + 0.071*SL	0.27 + 0.072*SL
	t_{PHL}	0.23	0.15 + 0.039*SL	0.16 + 0.035*SL	0.16 + 0.034*SL
	t_R	0.65	0.34 + 0.155*SL	0.33 + 0.160*SL	0.31 + 0.163*SL
	t_F	0.39	0.27 + 0.059*SL	0.26 + 0.062*SL	0.24 + 0.066*SL
S to YN	t_{PLH}	0.40	0.26 + 0.070*SL	0.26 + 0.071*SL	0.25 + 0.071*SL
	t_{PHL}	0.31	0.24 + 0.035*SL	0.24 + 0.034*SL	0.24 + 0.034*SL
	t_R	0.65	0.34 + 0.155*SL	0.32 + 0.160*SL	0.31 + 0.163*SL
	t_F	0.24	0.11 + 0.064*SL	0.10 + 0.067*SL	0.09 + 0.069*SL

KG80 MX2ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.46	0.42 + 0.023*SL	0.42 + 0.020*SL	0.42 + 0.021*SL
	t_{PHL}	0.36	0.33 + 0.018*SL	0.34 + 0.014*SL	0.35 + 0.012*SL
	t_R	0.16	0.08 + 0.040*SL	0.08 + 0.043*SL	0.06 + 0.044*SL
	t_F	0.12	0.08 + 0.020*SL	0.08 + 0.020*SL	0.08 + 0.020*SL
D1 to YN	t_{PLH}	0.46	0.42 + 0.023*SL	0.42 + 0.021*SL	0.42 + 0.021*SL
	t_{PHL}	0.36	0.32 + 0.018*SL	0.33 + 0.014*SL	0.35 + 0.012*SL
	t_R	0.16	0.08 + 0.040*SL	0.08 + 0.043*SL	0.06 + 0.044*SL
	t_F	0.12	0.08 + 0.020*SL	0.08 + 0.019*SL	0.08 + 0.020*SL
S to YN	t_{PLH}	0.40	0.35 + 0.022*SL	0.35 + 0.021*SL	0.36 + 0.021*SL
	t_{PHL}	0.42	0.38 + 0.018*SL	0.39 + 0.014*SL	0.41 + 0.012*SL
	t_R	0.16	0.08 + 0.040*SL	0.07 + 0.043*SL	0.06 + 0.045*SL
	t_F	0.12	0.08 + 0.021*SL	0.08 + 0.019*SL	0.08 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX2I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.48	0.30 + 0.093*SL	0.29 + 0.094*SL	0.30 + 0.094*SL
	t_{PHL}	0.21	0.11 + 0.046*SL	0.14 + 0.038*SL	0.14 + 0.037*SL
	t_R	0.88	0.47 + 0.204*SL	0.46 + 0.208*SL	0.45 + 0.209*SL
	t_F	0.38	0.25 + 0.064*SL	0.24 + 0.070*SL	0.20 + 0.073*SL
D1 to YN	t_{PLH}	0.61	0.42 + 0.096*SL	0.42 + 0.095*SL	0.43 + 0.094*SL
	t_{PHL}	0.28	0.20 + 0.043*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_R	0.89	0.49 + 0.202*SL	0.47 + 0.207*SL	0.46 + 0.208*SL
	t_F	0.44	0.31 + 0.067*SL	0.30 + 0.070*SL	0.27 + 0.073*SL
S to YN	t_{PLH}	0.59	0.40 + 0.095*SL	0.40 + 0.094*SL	0.40 + 0.094*SL
	t_{PHL}	0.38	0.30 + 0.039*SL	0.31 + 0.037*SL	0.31 + 0.037*SL
	t_R	0.89	0.49 + 0.202*SL	0.47 + 0.207*SL	0.46 + 0.208*SL
	t_F	0.28	0.14 + 0.071*SL	0.13 + 0.073*SL	0.12 + 0.074*SL

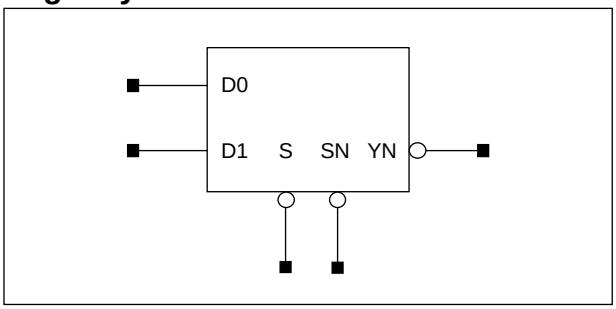
KGM80 MX2ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.64	0.58 + 0.027*SL	0.59 + 0.025*SL	0.59 + 0.025*SL
	t_{PHL}	0.50	0.46 + 0.021*SL	0.47 + 0.015*SL	0.50 + 0.012*SL
	t_R	0.21	0.11 + 0.051*SL	0.10 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.14	0.09 + 0.025*SL	0.10 + 0.021*SL	0.11 + 0.020*SL
D1 to YN	t_{PLH}	0.64	0.59 + 0.027*SL	0.59 + 0.025*SL	0.59 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.021*SL	0.47 + 0.015*SL	0.50 + 0.012*SL
	t_R	0.21	0.11 + 0.050*SL	0.10 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.021*SL	0.10 + 0.021*SL
S to YN	t_{PLH}	0.54	0.48 + 0.028*SL	0.49 + 0.025*SL	0.49 + 0.025*SL
	t_{PHL}	0.56	0.52 + 0.021*SL	0.54 + 0.015*SL	0.56 + 0.012*SL
	t_R	0.21	0.10 + 0.052*SL	0.10 + 0.053*SL	0.08 + 0.054*SL
	t_F	0.14	0.09 + 0.024*SL	0.10 + 0.021*SL	0.10 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

2 > 1 Inverting MUX with Separate S and SN Inputs, 1X/2X Drive

Logic Symbol



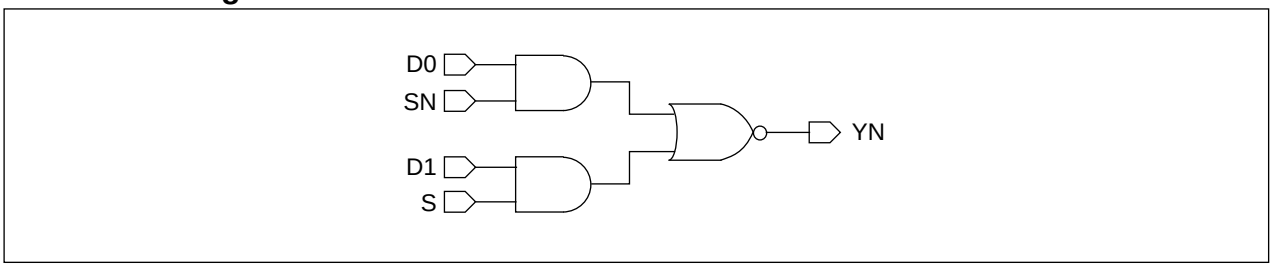
Truth Table

D0	D1	S	SN	YN
0	x	0	1	1
1	x	0	1	0
x	0	1	0	1
x	1	1	0	0

Cell Data

Input Load (SL)								Gate Count	
KG80									
MX2IA				*MX2ID2A*				*MX2IA*	*MX2ID2A*
D0	D1	S	SN	D0	D1	S	SN		
0.6	0.7	0.7	0.5	1.0	1.0	0.8	0.8	2.0	4.0
KGM80									
MX2IA				*MX2ID2A*				*MX2IA*	*MX2ID2A*
D0	D1	S	SN	D0	D1	S	SN		
1.0	1.0	1.0	1.0	1.0	1.0	0.9	0.9	2.0	4.0

Schematic Diagram



MX2IA/MX2ID2A

2 > 1 Inverting MUX with Separate S and SN Inputs, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX2IA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.36	0.22 + 0.068*SL	0.22 + 0.070*SL	0.21 + 0.071*SL
	t_{PHL}	0.17	0.09 + 0.043*SL	0.11 + 0.034*SL	0.11 + 0.034*SL
	t_R	0.64	0.33 + 0.155*SL	0.31 + 0.160*SL	0.29 + 0.163*SL
	t_F	0.34	0.23 + 0.056*SL	0.21 + 0.062*SL	0.19 + 0.065*SL
D1 to YN	t_{PLH}	0.41	0.27 + 0.072*SL	0.27 + 0.071*SL	0.27 + 0.072*SL
	t_{PHL}	0.22	0.15 + 0.037*SL	0.16 + 0.034*SL	0.16 + 0.034*SL
	t_R	0.64	0.33 + 0.155*SL	0.32 + 0.160*SL	0.31 + 0.163*SL
	t_F	0.39	0.27 + 0.062*SL	0.27 + 0.062*SL	0.24 + 0.065*SL
S to YN	t_{PLH}	0.40	0.26 + 0.070*SL	0.26 + 0.071*SL	0.26 + 0.071*SL
	t_{PHL}	0.19	0.11 + 0.039*SL	0.12 + 0.035*SL	0.13 + 0.034*SL
	t_R	0.65	0.34 + 0.155*SL	0.32 + 0.160*SL	0.31 + 0.162*SL
	t_F	0.37	0.25 + 0.059*SL	0.24 + 0.064*SL	0.22 + 0.066*SL
SN to YN	t_{PLH}	0.40	0.26 + 0.070*SL	0.26 + 0.071*SL	0.26 + 0.071*SL
	t_{PHL}	0.19	0.11 + 0.039*SL	0.12 + 0.035*SL	0.13 + 0.034*SL
	t_R	0.65	0.34 + 0.155*SL	0.32 + 0.160*SL	0.31 + 0.162*SL
	t_F	0.37	0.25 + 0.059*SL	0.24 + 0.064*SL	0.22 + 0.066*SL

KG80 MX2ID2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.46	0.42 + 0.022*SL	0.42 + 0.021*SL	0.42 + 0.021*SL
	t_{PHL}	0.36	0.32 + 0.018*SL	0.33 + 0.014*SL	0.35 + 0.012*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.06 + 0.044*SL
	t_F	0.12	0.08 + 0.020*SL	0.08 + 0.020*SL	0.08 + 0.020*SL
D1 to YN	t_{PLH}	0.46	0.42 + 0.022*SL	0.42 + 0.021*SL	0.42 + 0.021*SL
	t_{PHL}	0.35	0.32 + 0.016*SL	0.33 + 0.015*SL	0.33 + 0.013*SL
	t_R	0.16	0.08 + 0.041*SL	0.08 + 0.043*SL	0.06 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.019*SL
S to YN	t_{PLH}	0.36	0.32 + 0.022*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.29	0.25 + 0.018*SL	0.26 + 0.014*SL	0.27 + 0.012*SL
	t_R	0.16	0.08 + 0.041*SL	0.07 + 0.043*SL	0.06 + 0.045*SL
	t_F	0.12	0.08 + 0.021*SL	0.08 + 0.020*SL	0.08 + 0.020*SL
SN to YN	t_{PLH}	0.36	0.32 + 0.022*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.29	0.25 + 0.018*SL	0.26 + 0.014*SL	0.27 + 0.012*SL
	t_R	0.16	0.08 + 0.041*SL	0.07 + 0.043*SL	0.06 + 0.045*SL
	t_F	0.12	0.08 + 0.021*SL	0.08 + 0.020*SL	0.08 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX2IA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.48	0.30 + 0.093*SL	0.29 + 0.094*SL	0.29 + 0.094*SL
	t_{PHL}	0.21	0.11 + 0.046*SL	0.14 + 0.038*SL	0.14 + 0.037*SL
	t_R	0.87	0.47 + 0.204*SL	0.46 + 0.208*SL	0.44 + 0.209*SL
	t_F	0.38	0.25 + 0.064*SL	0.24 + 0.070*SL	0.20 + 0.073*SL
D1 to YN	t_{PLH}	0.61	0.41 + 0.096*SL	0.42 + 0.095*SL	0.42 + 0.094*SL
	t_{PHL}	0.28	0.20 + 0.042*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_R	0.89	0.49 + 0.202*SL	0.47 + 0.207*SL	0.46 + 0.208*SL
	t_F	0.44	0.31 + 0.067*SL	0.30 + 0.070*SL	0.27 + 0.073*SL
S to YN	t_{PLH}	0.59	0.40 + 0.095*SL	0.40 + 0.094*SL	0.40 + 0.094*SL
	t_{PHL}	0.25	0.16 + 0.043*SL	0.17 + 0.038*SL	0.18 + 0.037*SL
	t_R	0.89	0.49 + 0.202*SL	0.48 + 0.206*SL	0.46 + 0.208*SL
	t_F	0.42	0.29 + 0.067*SL	0.28 + 0.072*SL	0.25 + 0.074*SL
SN to YN	t_{PLH}	0.59	0.40 + 0.095*SL	0.40 + 0.094*SL	0.40 + 0.094*SL
	t_{PHL}	0.25	0.16 + 0.043*SL	0.17 + 0.038*SL	0.18 + 0.037*SL
	t_R	0.89	0.49 + 0.202*SL	0.48 + 0.206*SL	0.46 + 0.208*SL
	t_F	0.42	0.29 + 0.067*SL	0.28 + 0.072*SL	0.25 + 0.074*SL

KGM80 MX2ID2A

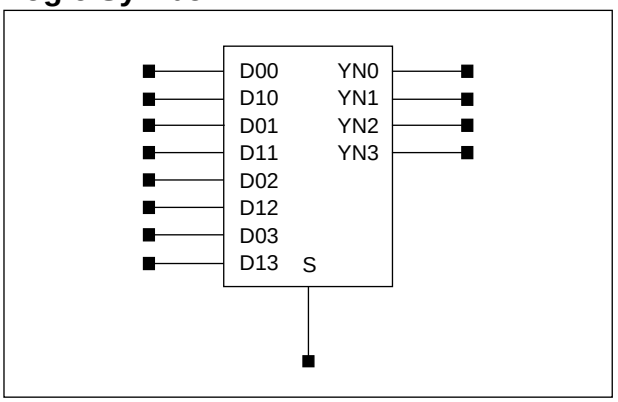
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.64	0.59 + 0.027*SL	0.59 + 0.025*SL	0.59 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.021*SL	0.47 + 0.015*SL	0.50 + 0.012*SL
	t_R	0.21	0.11 + 0.050*SL	0.10 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.14	0.10 + 0.023*SL	0.10 + 0.021*SL	0.10 + 0.021*SL
D1 to YN	t_{PLH}	0.64	0.58 + 0.027*SL	0.59 + 0.025*SL	0.59 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.021*SL	0.47 + 0.015*SL	0.49 + 0.012*SL
	t_R	0.21	0.11 + 0.051*SL	0.10 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.14	0.10 + 0.023*SL	0.10 + 0.021*SL	0.10 + 0.021*SL
S to YN	t_{PLH}	0.48	0.43 + 0.027*SL	0.43 + 0.025*SL	0.44 + 0.025*SL
	t_{PHL}	0.40	0.36 + 0.021*SL	0.38 + 0.015*SL	0.41 + 0.012*SL
	t_R	0.21	0.11 + 0.050*SL	0.10 + 0.053*SL	0.08 + 0.054*SL
	t_F	0.14	0.09 + 0.024*SL	0.10 + 0.021*SL	0.11 + 0.020*SL
SN to YN	t_{PLH}	0.48	0.43 + 0.027*SL	0.43 + 0.025*SL	0.44 + 0.025*SL
	t_{PHL}	0.40	0.36 + 0.021*SL	0.38 + 0.015*SL	0.41 + 0.012*SL
	t_R	0.21	0.11 + 0.050*SL	0.10 + 0.053*SL	0.08 + 0.054*SL
	t_F	0.14	0.09 + 0.024*SL	0.10 + 0.021*SL	0.11 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

MX2IX4

4-Bit 2 > 1 Inverting MUX

Logic Symbol



Truth Table

S	YN0	YN1	YN2	YN3
0	$\overline{D00}$	$\overline{D01}$	$\overline{D02}$	$\overline{D03}$
1	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$

Cell Data

Input Load (SL)									Gate Count
KG80									
MX2IX4									*MX2IX4*
D00	D10	D01	D11	D02	D12	D03	D13	S	
0.9	0.7	0.9	0.5	0.9	0.5	0.9	0.5	4.3	9.0
KGM80									
MX2IX4									*MX2IX4*
D00	D10	D01	D11	D02	D12	D03	D13	S	
1.0	0.9	1.0	0.9	1.0	0.7	1.0	0.7	5.0	9.0

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX2IX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to YN0	t_{PLH}	0.27	0.17 + 0.053*SL	0.17 + 0.053*SL	0.16 + 0.054*SL
	t_{PHL}	0.16	0.07 + 0.044*SL	0.09 + 0.034*SL	0.10 + 0.034*SL
	t_R	0.44	0.22 + 0.112*SL	0.20 + 0.119*SL	0.17 + 0.122*SL
	t_F	0.30	0.18 + 0.058*SL	0.18 + 0.062*SL	0.15 + 0.065*SL
D10 to YN0	t_{PLH}	0.32	0.21 + 0.056*SL	0.21 + 0.055*SL	0.21 + 0.055*SL
	t_{PHL}	0.23	0.15 + 0.039*SL	0.16 + 0.035*SL	0.16 + 0.034*SL
	t_R	0.52	0.29 + 0.114*SL	0.28 + 0.120*SL	0.26 + 0.123*SL
	t_F	0.39	0.27 + 0.058*SL	0.26 + 0.063*SL	0.24 + 0.066*SL
S to YN0	t_{PLH}	0.45	0.32 + 0.069*SL	0.31 + 0.071*SL	0.31 + 0.071*SL
	t_{PHL}	0.43	0.35 + 0.040*SL	0.36 + 0.036*SL	0.37 + 0.034*SL
	t_R	0.63	0.31 + 0.160*SL	0.30 + 0.163*SL	0.29 + 0.164*SL
	t_F	0.28	0.16 + 0.062*SL	0.15 + 0.064*SL	0.13 + 0.067*SL
D01 to YN1	t_{PLH}	0.27	0.17 + 0.053*SL	0.17 + 0.053*SL	0.16 + 0.054*SL
	t_{PHL}	0.16	0.07 + 0.044*SL	0.10 + 0.034*SL	0.10 + 0.034*SL
	t_R	0.45	0.22 + 0.112*SL	0.21 + 0.119*SL	0.18 + 0.122*SL
	t_F	0.30	0.19 + 0.058*SL	0.18 + 0.062*SL	0.15 + 0.065*SL
D11 to YN1	t_{PLH}	0.32	0.21 + 0.056*SL	0.21 + 0.055*SL	0.22 + 0.055*SL
	t_{PHL}	0.23	0.15 + 0.038*SL	0.16 + 0.035*SL	0.16 + 0.034*SL
	t_R	0.53	0.30 + 0.114*SL	0.28 + 0.120*SL	0.26 + 0.123*SL
	t_F	0.39	0.27 + 0.059*SL	0.26 + 0.063*SL	0.24 + 0.066*SL
S to YN1	t_{PLH}	0.46	0.32 + 0.069*SL	0.32 + 0.071*SL	0.31 + 0.071*SL
	t_{PHL}	0.43	0.35 + 0.039*SL	0.36 + 0.036*SL	0.37 + 0.034*SL
	t_R	0.63	0.31 + 0.160*SL	0.31 + 0.163*SL	0.30 + 0.164*SL
	t_F	0.28	0.16 + 0.061*SL	0.15 + 0.064*SL	0.13 + 0.067*SL
D02 to YN2	t_{PLH}	0.27	0.17 + 0.053*SL	0.17 + 0.053*SL	0.16 + 0.054*SL
	t_{PHL}	0.16	0.07 + 0.044*SL	0.10 + 0.034*SL	0.10 + 0.034*SL
	t_R	0.45	0.22 + 0.112*SL	0.21 + 0.119*SL	0.18 + 0.123*SL
	t_F	0.30	0.19 + 0.058*SL	0.18 + 0.062*SL	0.15 + 0.065*SL
D12 to YN2	t_{PLH}	0.32	0.21 + 0.056*SL	0.21 + 0.055*SL	0.22 + 0.055*SL
	t_{PHL}	0.23	0.15 + 0.038*SL	0.16 + 0.035*SL	0.16 + 0.034*SL
	t_R	0.53	0.30 + 0.114*SL	0.28 + 0.120*SL	0.26 + 0.123*SL
	t_F	0.39	0.27 + 0.059*SL	0.26 + 0.063*SL	0.24 + 0.066*SL
S to YN2	t_{PLH}	0.46	0.32 + 0.069*SL	0.32 + 0.071*SL	0.31 + 0.071*SL
	t_{PHL}	0.43	0.35 + 0.040*SL	0.36 + 0.036*SL	0.37 + 0.034*SL
	t_R	0.63	0.31 + 0.160*SL	0.31 + 0.163*SL	0.30 + 0.164*SL
	t_F	0.28	0.16 + 0.061*SL	0.15 + 0.064*SL	0.13 + 0.067*SL
D03 to YN3	t_{PLH}	0.27	0.17 + 0.053*SL	0.17 + 0.053*SL	0.16 + 0.054*SL
	t_{PHL}	0.16	0.07 + 0.044*SL	0.09 + 0.034*SL	0.10 + 0.034*SL
	t_R	0.44	0.22 + 0.112*SL	0.20 + 0.119*SL	0.17 + 0.122*SL
	t_F	0.30	0.18 + 0.058*SL	0.18 + 0.062*SL	0.15 + 0.065*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX2IX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to YN3	t_{PLH}	0.32	0.21 + 0.056*SL	0.21 + 0.055*SL	0.21 + 0.055*SL
	t_{PHL}	0.23	0.15 + 0.039*SL	0.16 + 0.035*SL	0.16 + 0.034*SL
	t_R	0.52	0.29 + 0.114*SL	0.28 + 0.120*SL	0.26 + 0.123*SL
	t_F	0.39	0.27 + 0.058*SL	0.26 + 0.063*SL	0.24 + 0.066*SL
S to YN3	t_{PLH}	0.45	0.32 + 0.069*SL	0.31 + 0.071*SL	0.31 + 0.071*SL
	t_{PHL}	0.43	0.35 + 0.040*SL	0.36 + 0.036*SL	0.37 + 0.034*SL
	t_R	0.63	0.31 + 0.160*SL	0.30 + 0.163*SL	0.29 + 0.164*SL
	t_F	0.28	0.16 + 0.062*SL	0.15 + 0.064*SL	0.13 + 0.067*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX2IX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to YN0	t_{PLH}	0.35	0.21 + 0.070*SL	0.21 + 0.070*SL	0.20 + 0.070*SL
	t_{PHL}	0.20	0.10 + 0.046*SL	0.13 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.59	0.29 + 0.149*SL	0.27 + 0.154*SL	0.24 + 0.157*SL
	t_F	0.33	0.20 + 0.067*SL	0.19 + 0.070*SL	0.15 + 0.073*SL
D10 to YN0	t_{PLH}	0.45	0.30 + 0.074*SL	0.31 + 0.073*SL	0.31 + 0.072*SL
	t_{PHL}	0.28	0.20 + 0.041*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_R	0.71	0.41 + 0.149*SL	0.39 + 0.155*SL	0.37 + 0.157*SL
	t_F	0.44	0.31 + 0.067*SL	0.30 + 0.071*SL	0.27 + 0.073*SL
S to YN0	t_{PLH}	0.63	0.44 + 0.094*SL	0.44 + 0.094*SL	0.44 + 0.094*SL
	t_{PHL}	0.57	0.48 + 0.045*SL	0.49 + 0.039*SL	0.51 + 0.037*SL
	t_R	0.87	0.46 + 0.207*SL	0.45 + 0.209*SL	0.45 + 0.209*SL
	t_F	0.34	0.20 + 0.069*SL	0.19 + 0.071*SL	0.17 + 0.073*SL
D01 to YN1	t_{PLH}	0.35	0.21 + 0.070*SL	0.21 + 0.070*SL	0.21 + 0.070*SL
	t_{PHL}	0.20	0.11 + 0.046*SL	0.13 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.59	0.29 + 0.149*SL	0.28 + 0.154*SL	0.25 + 0.157*SL
	t_F	0.33	0.20 + 0.066*SL	0.19 + 0.070*SL	0.16 + 0.073*SL
D11 to YN1	t_{PLH}	0.46	0.31 + 0.075*SL	0.31 + 0.073*SL	0.32 + 0.072*SL
	t_{PHL}	0.29	0.20 + 0.041*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_R	0.71	0.42 + 0.148*SL	0.40 + 0.155*SL	0.37 + 0.157*SL
	t_F	0.45	0.31 + 0.067*SL	0.30 + 0.071*SL	0.27 + 0.073*SL
S to YN1	t_{PLH}	0.63	0.44 + 0.094*SL	0.44 + 0.094*SL	0.45 + 0.094*SL
	t_{PHL}	0.57	0.48 + 0.045*SL	0.50 + 0.039*SL	0.52 + 0.037*SL
	t_R	0.88	0.47 + 0.208*SL	0.46 + 0.209*SL	0.47 + 0.209*SL
	t_F	0.34	0.20 + 0.068*SL	0.20 + 0.071*SL	0.17 + 0.073*SL
D02 to YN2	t_{PLH}	0.35	0.21 + 0.070*SL	0.21 + 0.070*SL	0.21 + 0.070*SL
	t_{PHL}	0.20	0.11 + 0.046*SL	0.13 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.59	0.29 + 0.149*SL	0.28 + 0.154*SL	0.25 + 0.157*SL
	t_F	0.33	0.20 + 0.066*SL	0.19 + 0.070*SL	0.16 + 0.073*SL
D12 to YN2	t_{PLH}	0.46	0.31 + 0.075*SL	0.31 + 0.073*SL	0.32 + 0.072*SL
	t_{PHL}	0.29	0.20 + 0.041*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_R	0.71	0.42 + 0.148*SL	0.40 + 0.155*SL	0.37 + 0.157*SL
	t_F	0.45	0.31 + 0.067*SL	0.30 + 0.071*SL	0.27 + 0.073*SL
S to YN2	t_{PLH}	0.63	0.44 + 0.094*SL	0.44 + 0.094*SL	0.45 + 0.094*SL
	t_{PHL}	0.57	0.48 + 0.045*SL	0.50 + 0.039*SL	0.52 + 0.037*SL
	t_R	0.88	0.47 + 0.207*SL	0.46 + 0.209*SL	0.46 + 0.209*SL
	t_F	0.34	0.20 + 0.068*SL	0.20 + 0.071*SL	0.17 + 0.073*SL
D03 to YN3	t_{PLH}	0.35	0.21 + 0.070*SL	0.21 + 0.070*SL	0.20 + 0.070*SL
	t_{PHL}	0.20	0.10 + 0.046*SL	0.13 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.59	0.29 + 0.149*SL	0.27 + 0.154*SL	0.24 + 0.157*SL
	t_F	0.33	0.20 + 0.067*SL	0.19 + 0.070*SL	0.15 + 0.073*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

(Continued)

Switching Characteristics

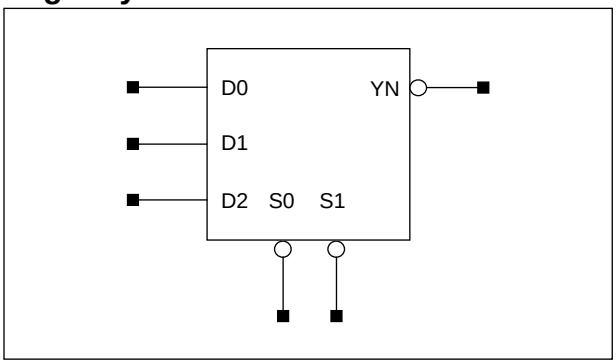
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX2IX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to YN3	t_{PLH}	0.45	0.30 + 0.074*SL	0.31 + 0.073*SL	0.31 + 0.072*SL
	t_{PHL}	0.28	0.20 + 0.041*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_R	0.71	0.41 + 0.149*SL	0.39 + 0.155*SL	0.37 + 0.157*SL
	t_F	0.44	0.31 + 0.067*SL	0.30 + 0.071*SL	0.27 + 0.073*SL
S to YN3	t_{PLH}	0.63	0.44 + 0.094*SL	0.44 + 0.094*SL	0.44 + 0.094*SL
	t_{PHL}	0.57	0.48 + 0.045*SL	0.49 + 0.039*SL	0.51 + 0.037*SL
	t_R	0.87	0.46 + 0.207*SL	0.45 + 0.209*SL	0.45 + 0.209*SL
	t_F	0.34	0.20 + 0.069*SL	0.19 + 0.071*SL	0.17 + 0.073*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



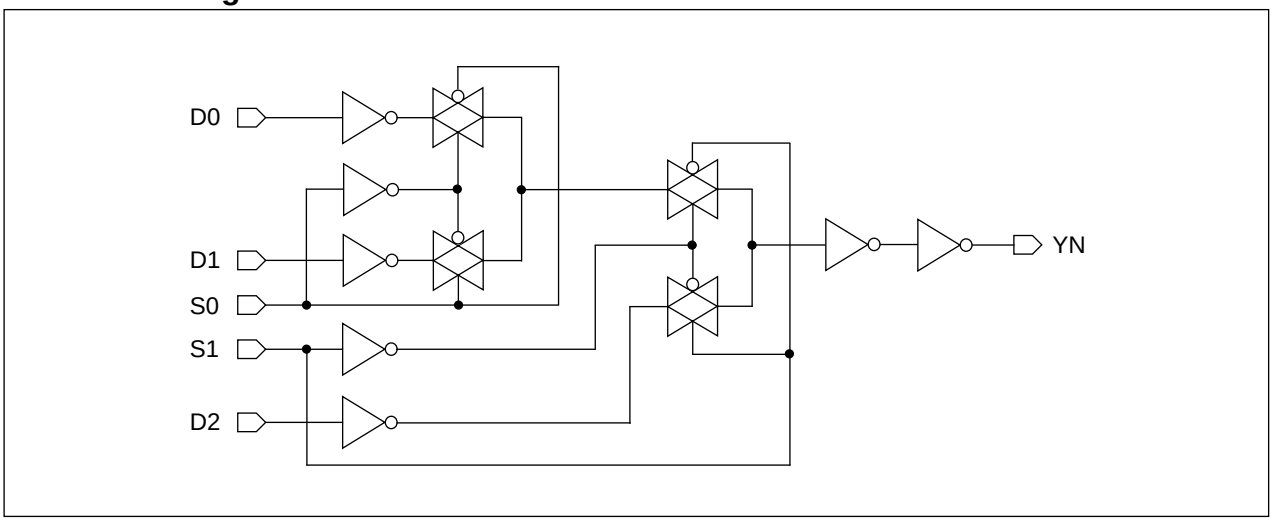
Truth Table

S0	S1	YN
0	0	$\overline{D0}$
1	0	$\overline{D1}$
x	1	$\overline{D2}$

Cell Data

Input Load (SL)										Gate Count	
KG80											
MX3I					*MX3ID2*					*MX3I*	*MX3ID2*
D0	D1	D2	S0	S1	D0	D1	D2	S0	S1		
1.0	1.0	0.9	1.1	1.4	1.0	1.0	0.9	1.1	1.4	6.0	6.0
KGM80											
MX3I					*MX3ID2*					*MX3I*	*MX3ID2*
D0	D1	D2	S0	S1	D0	D1	D2	S0	S1		
1.0	1.0	1.0	2.1	2.0	1.0	1.0	1.0	2.1	2.0	6.0	6.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX3I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.60	0.51 + 0.042*SL	0.51 + 0.041*SL	0.51 + 0.042*SL
	t_{PHL}	0.48	0.42 + 0.028*SL	0.43 + 0.024*SL	0.44 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.15	0.08 + 0.038*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
D1 to YN	t_{PLH}	0.60	0.51 + 0.042*SL	0.51 + 0.041*SL	0.51 + 0.042*SL
	t_{PHL}	0.48	0.42 + 0.028*SL	0.43 + 0.024*SL	0.44 + 0.023*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.15	0.08 + 0.038*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
D2 to YN	t_{PLH}	0.48	0.39 + 0.042*SL	0.39 + 0.042*SL	0.40 + 0.042*SL
	t_{PHL}	0.36	0.30 + 0.028*SL	0.31 + 0.024*SL	0.32 + 0.023*SL
	t_R	0.26	0.09 + 0.087*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.15	0.07 + 0.041*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
S0 to YN	t_{PLH}	0.52	0.44 + 0.042*SL	0.44 + 0.042*SL	0.44 + 0.042*SL
	t_{PHL}	0.52	0.47 + 0.028*SL	0.48 + 0.024*SL	0.48 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.15	0.07 + 0.040*SL	0.07 + 0.040*SL	0.06 + 0.042*SL
S1 to YN	t_{PLH}	0.43	0.35 + 0.042*SL	0.35 + 0.042*SL	0.35 + 0.042*SL
	t_{PHL}	0.44	0.38 + 0.028*SL	0.39 + 0.024*SL	0.40 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.08 + 0.090*SL	0.08 + 0.091*SL
	t_F	0.16	0.08 + 0.040*SL	0.08 + 0.040*SL	0.06 + 0.042*SL

KG80 MX3ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.59	0.54 + 0.023*SL	0.55 + 0.021*SL	0.55 + 0.021*SL
	t_{PHL}	0.48	0.45 + 0.018*SL	0.46 + 0.014*SL	0.47 + 0.012*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.08 + 0.020*SL
D1 to YN	t_{PLH}	0.59	0.54 + 0.023*SL	0.55 + 0.021*SL	0.55 + 0.021*SL
	t_{PHL}	0.48	0.44 + 0.019*SL	0.45 + 0.014*SL	0.46 + 0.012*SL
	t_R	0.17	0.09 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.09 + 0.020*SL	0.09 + 0.019*SL	0.08 + 0.020*SL
D2 to YN	t_{PLH}	0.46	0.42 + 0.022*SL	0.42 + 0.020*SL	0.42 + 0.021*SL
	t_{PHL}	0.36	0.32 + 0.018*SL	0.33 + 0.014*SL	0.34 + 0.012*SL
	t_R	0.16	0.08 + 0.040*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.12	0.08 + 0.020*SL	0.08 + 0.020*SL	0.08 + 0.020*SL
S0 to YN	t_{PLH}	0.52	0.47 + 0.023*SL	0.47 + 0.021*SL	0.47 + 0.021*SL
	t_{PHL}	0.53	0.49 + 0.018*SL	0.50 + 0.014*SL	0.51 + 0.012*SL
	t_R	0.17	0.09 + 0.041*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.13	0.08 + 0.022*SL	0.09 + 0.019*SL	0.08 + 0.020*SL
S1 to YN	t_{PLH}	0.42	0.37 + 0.023*SL	0.38 + 0.021*SL	0.38 + 0.021*SL
	t_{PHL}	0.44	0.41 + 0.018*SL	0.42 + 0.014*SL	0.43 + 0.012*SL
	t_R	0.16	0.08 + 0.042*SL	0.08 + 0.043*SL	0.07 + 0.044*SL
	t_F	0.12	0.08 + 0.021*SL	0.08 + 0.019*SL	0.08 + 0.020*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX3I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.86	0.75 + 0.051*SL	0.76 + 0.050*SL	0.76 + 0.050*SL
	t_{PHL}	0.66	0.60 + 0.031*SL	0.61 + 0.024*SL	0.63 + 0.023*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.08 + 0.043*SL
D1 to YN	t_{PLH}	0.86	0.76 + 0.051*SL	0.76 + 0.050*SL	0.76 + 0.050*SL
	t_{PHL}	0.65	0.59 + 0.030*SL	0.60 + 0.024*SL	0.62 + 0.023*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.042*SL	0.08 + 0.043*SL
D2 to YN	t_{PLH}	0.66	0.56 + 0.050*SL	0.56 + 0.050*SL	0.56 + 0.050*SL
	t_{PHL}	0.48	0.42 + 0.030*SL	0.44 + 0.024*SL	0.45 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.108*SL	0.11 + 0.109*SL
	t_F	0.18	0.09 + 0.043*SL	0.10 + 0.041*SL	0.08 + 0.043*SL
S0 to YN	t_{PLH}	0.76	0.66 + 0.051*SL	0.66 + 0.050*SL	0.66 + 0.050*SL
	t_{PHL}	0.71	0.65 + 0.031*SL	0.67 + 0.024*SL	0.68 + 0.023*SL
	t_R	0.35	0.14 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.08 + 0.043*SL
S1 to YN	t_{PLH}	0.58	0.48 + 0.050*SL	0.48 + 0.050*SL	0.49 + 0.050*SL
	t_{PHL}	0.58	0.52 + 0.030*SL	0.54 + 0.024*SL	0.55 + 0.023*SL
	t_R	0.34	0.13 + 0.105*SL	0.12 + 0.109*SL	0.12 + 0.109*SL
	t_F	0.18	0.10 + 0.042*SL	0.10 + 0.042*SL	0.08 + 0.043*SL

KGM80 MX3ID2

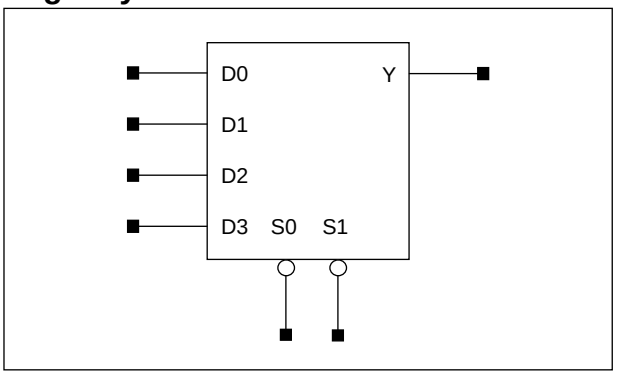
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.85	0.80 + 0.028*SL	0.80 + 0.025*SL	0.81 + 0.025*SL
	t_{PHL}	0.67	0.63 + 0.021*SL	0.65 + 0.015*SL	0.68 + 0.012*SL
	t_R	0.22	0.13 + 0.049*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
D1 to YN	t_{PLH}	0.86	0.80 + 0.028*SL	0.81 + 0.025*SL	0.81 + 0.025*SL
	t_{PHL}	0.67	0.62 + 0.021*SL	0.64 + 0.015*SL	0.67 + 0.012*SL
	t_R	0.22	0.13 + 0.049*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.15	0.10 + 0.023*SL	0.11 + 0.021*SL	0.11 + 0.020*SL
D2 to YN	t_{PLH}	0.64	0.58 + 0.027*SL	0.59 + 0.025*SL	0.59 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.021*SL	0.47 + 0.015*SL	0.49 + 0.012*SL
	t_R	0.21	0.11 + 0.050*SL	0.10 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.14	0.10 + 0.024*SL	0.11 + 0.020*SL	0.10 + 0.021*SL
S0 to YN	t_{PLH}	0.75	0.70 + 0.028*SL	0.71 + 0.025*SL	0.71 + 0.025*SL
	t_{PHL}	0.73	0.69 + 0.021*SL	0.70 + 0.015*SL	0.73 + 0.012*SL
	t_R	0.22	0.12 + 0.049*SL	0.12 + 0.052*SL	0.10 + 0.054*SL
	t_F	0.15	0.10 + 0.024*SL	0.11 + 0.020*SL	0.11 + 0.020*SL
S1 to YN	t_{PLH}	0.57	0.51 + 0.028*SL	0.52 + 0.025*SL	0.52 + 0.025*SL
	t_{PHL}	0.60	0.56 + 0.021*SL	0.57 + 0.015*SL	0.60 + 0.012*SL
	t_R	0.21	0.11 + 0.050*SL	0.11 + 0.053*SL	0.09 + 0.054*SL
	t_F	0.15	0.10 + 0.024*SL	0.11 + 0.021*SL	0.11 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 11, *Group3 : 11 < SL

MX4/MX4D2

4 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



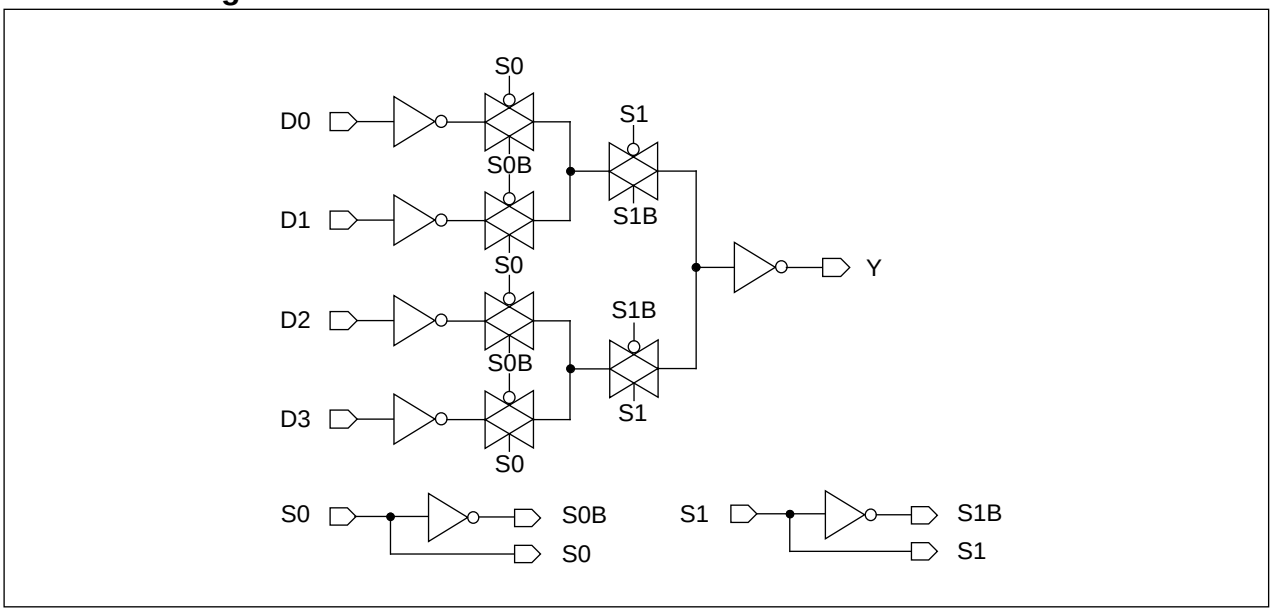
Truth Table

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)												Gate Count	
KG80													
MX4						*MX4D2*						*MX4*	*MX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
0.9	0.9	0.9	0.8	2.1	1.2	0.9	0.9	0.9	0.8	2.1	1.2	7.0	7.0
KGM80													
MX4						*MX4D2*						*MX4*	*MX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
1.0	1.0	1.0	1.0	2.8	2.1	1.0	1.0	1.0	.10	2.8	2.1	7.0	7.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.44	0.35 + 0.045*SL	0.36 + 0.042*SL	0.36 + 0.041*SL
	t_{PHL}	0.50	0.41 + 0.045*SL	0.43 + 0.034*SL	0.47 + 0.028*SL
	t_R	0.30	0.14 + 0.084*SL	0.13 + 0.087*SL	0.11 + 0.089*SL
	t_F	0.27	0.17 + 0.051*SL	0.19 + 0.043*SL	0.20 + 0.041*SL
D1 to Y	t_{PLH}	0.44	0.35 + 0.045*SL	0.35 + 0.042*SL	0.36 + 0.041*SL
	t_{PHL}	0.50	0.41 + 0.045*SL	0.43 + 0.034*SL	0.47 + 0.028*SL
	t_R	0.30	0.13 + 0.084*SL	0.13 + 0.087*SL	0.11 + 0.089*SL
	t_F	0.27	0.17 + 0.051*SL	0.19 + 0.043*SL	0.20 + 0.041*SL
D2 to Y	t_{PLH}	0.44	0.35 + 0.046*SL	0.35 + 0.042*SL	0.36 + 0.041*SL
	t_{PHL}	0.49	0.40 + 0.045*SL	0.43 + 0.034*SL	0.47 + 0.028*SL
	t_R	0.30	0.13 + 0.084*SL	0.13 + 0.087*SL	0.11 + 0.089*SL
	t_F	0.27	0.17 + 0.052*SL	0.19 + 0.043*SL	0.21 + 0.041*SL
D3 to Y	t_{PLH}	0.44	0.34 + 0.046*SL	0.35 + 0.042*SL	0.36 + 0.041*SL
	t_{PHL}	0.50	0.41 + 0.045*SL	0.43 + 0.034*SL	0.47 + 0.028*SL
	t_R	0.30	0.13 + 0.084*SL	0.13 + 0.087*SL	0.11 + 0.089*SL
	t_F	0.27	0.17 + 0.050*SL	0.19 + 0.043*SL	0.20 + 0.041*SL
S0 to Y	t_{PLH}	0.52	0.43 + 0.046*SL	0.44 + 0.042*SL	0.44 + 0.041*SL
	t_{PHL}	0.40	0.31 + 0.044*SL	0.33 + 0.034*SL	0.38 + 0.028*SL
	t_R	0.30	0.14 + 0.084*SL	0.13 + 0.087*SL	0.11 + 0.089*SL
	t_F	0.26	0.15 + 0.053*SL	0.17 + 0.044*SL	0.19 + 0.041*SL
S1 to Y	t_{PLH}	0.40	0.30 + 0.046*SL	0.31 + 0.043*SL	0.32 + 0.042*SL
	t_{PHL}	0.29	0.21 + 0.039*SL	0.23 + 0.031*SL	0.26 + 0.027*SL
	t_R	0.29	0.12 + 0.087*SL	0.12 + 0.088*SL	0.10 + 0.090*SL
	t_F	0.21	0.11 + 0.053*SL	0.13 + 0.045*SL	0.14 + 0.043*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.44	0.39 + 0.026*SL	0.40 + 0.022*SL	0.41 + 0.021*SL
	t_{PHL}	0.50	0.44 + 0.028*SL	0.46 + 0.021*SL	0.48 + 0.017*SL
	t_R	0.23	0.15 + 0.042*SL	0.15 + 0.042*SL	0.14 + 0.043*SL
	t_F	0.25	0.19 + 0.029*SL	0.20 + 0.025*SL	0.22 + 0.022*SL
D1 to Y	t_{PLH}	0.44	0.39 + 0.025*SL	0.39 + 0.022*SL	0.40 + 0.021*SL
	t_{PHL}	0.50	0.44 + 0.027*SL	0.46 + 0.021*SL	0.48 + 0.018*SL
	t_R	0.23	0.15 + 0.041*SL	0.15 + 0.042*SL	0.14 + 0.043*SL
	t_F	0.25	0.19 + 0.030*SL	0.20 + 0.025*SL	0.22 + 0.022*SL
D2 to Y	t_{PLH}	0.44	0.38 + 0.025*SL	0.39 + 0.022*SL	0.40 + 0.021*SL
	t_{PHL}	0.49	0.44 + 0.027*SL	0.45 + 0.021*SL	0.48 + 0.018*SL
	t_R	0.23	0.15 + 0.041*SL	0.15 + 0.043*SL	0.15 + 0.043*SL
	t_F	0.25	0.19 + 0.030*SL	0.20 + 0.025*SL	0.22 + 0.022*SL
D3 to Y	t_{PLH}	0.43	0.38 + 0.026*SL	0.39 + 0.022*SL	0.40 + 0.021*SL
	t_{PHL}	0.50	0.44 + 0.027*SL	0.46 + 0.021*SL	0.48 + 0.018*SL
	t_R	0.23	0.15 + 0.042*SL	0.15 + 0.043*SL	0.15 + 0.043*SL
	t_F	0.25	0.19 + 0.030*SL	0.20 + 0.025*SL	0.22 + 0.022*SL
S0 to Y	t_{PLH}	0.52	0.47 + 0.026*SL	0.47 + 0.022*SL	0.48 + 0.021*SL
	t_{PHL}	0.39	0.34 + 0.027*SL	0.35 + 0.021*SL	0.38 + 0.018*SL
	t_R	0.24	0.15 + 0.041*SL	0.15 + 0.042*SL	0.14 + 0.043*SL
	t_F	0.23	0.17 + 0.031*SL	0.19 + 0.025*SL	0.21 + 0.022*SL
S1 to Y	t_{PLH}	0.39	0.34 + 0.026*SL	0.35 + 0.023*SL	0.36 + 0.021*SL
	t_{PHL}	0.28	0.23 + 0.024*SL	0.24 + 0.020*SL	0.26 + 0.017*SL
	t_R	0.22	0.14 + 0.045*SL	0.14 + 0.043*SL	0.14 + 0.043*SL
	t_F	0.19	0.13 + 0.030*SL	0.14 + 0.026*SL	0.16 + 0.023*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.60	0.48 + 0.058*SL	0.50 + 0.051*SL	0.51 + 0.050*SL
	t_{PHL}	0.71	0.60 + 0.057*SL	0.65 + 0.038*SL	0.75 + 0.029*SL
	t_R	0.39	0.18 + 0.105*SL	0.18 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.36	0.24 + 0.061*SL	0.28 + 0.046*SL	0.33 + 0.041*SL
D1 to Y	t_{PLH}	0.59	0.48 + 0.058*SL	0.50 + 0.051*SL	0.51 + 0.050*SL
	t_{PHL}	0.71	0.60 + 0.057*SL	0.65 + 0.038*SL	0.75 + 0.029*SL
	t_R	0.39	0.18 + 0.106*SL	0.18 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.36	0.24 + 0.060*SL	0.28 + 0.046*SL	0.33 + 0.041*SL
D2 to Y	t_{PLH}	0.59	0.48 + 0.058*SL	0.49 + 0.051*SL	0.51 + 0.050*SL
	t_{PHL}	0.71	0.59 + 0.057*SL	0.64 + 0.038*SL	0.74 + 0.029*SL
	t_R	0.39	0.18 + 0.105*SL	0.18 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.36	0.24 + 0.060*SL	0.28 + 0.046*SL	0.33 + 0.041*SL
D3 to Y	t_{PLH}	0.59	0.47 + 0.057*SL	0.49 + 0.051*SL	0.50 + 0.050*SL
	t_{PHL}	0.71	0.60 + 0.057*SL	0.65 + 0.038*SL	0.75 + 0.029*SL
	t_R	0.39	0.18 + 0.105*SL	0.18 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.36	0.24 + 0.060*SL	0.28 + 0.045*SL	0.33 + 0.041*SL
S0 to Y	t_{PLH}	0.71	0.59 + 0.058*SL	0.61 + 0.051*SL	0.62 + 0.050*SL
	t_{PHL}	0.58	0.47 + 0.056*SL	0.52 + 0.037*SL	0.62 + 0.029*SL
	t_R	0.39	0.19 + 0.103*SL	0.18 + 0.105*SL	0.15 + 0.108*SL
	t_F	0.35	0.22 + 0.062*SL	0.27 + 0.046*SL	0.32 + 0.041*SL
S1 to Y	t_{PLH}	0.52	0.40 + 0.058*SL	0.42 + 0.051*SL	0.44 + 0.050*SL
	t_{PHL}	0.40	0.31 + 0.048*SL	0.35 + 0.034*SL	0.42 + 0.028*SL
	t_R	0.38	0.17 + 0.107*SL	0.17 + 0.106*SL	0.15 + 0.108*SL
	t_F	0.28	0.16 + 0.059*SL	0.19 + 0.048*SL	0.24 + 0.043*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

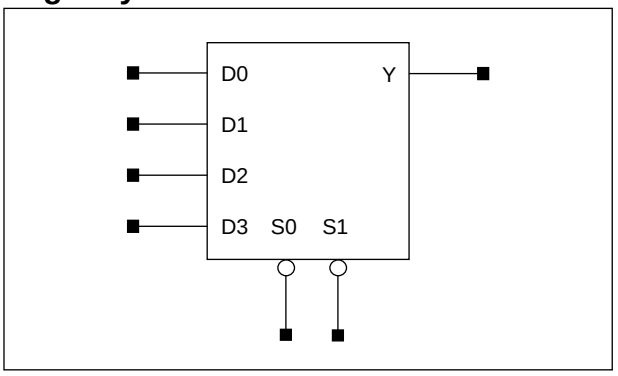
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.60	0.54 + 0.032*SL	0.55 + 0.027*SL	0.57 + 0.025*SL
	t_{PHL}	0.72	0.65 + 0.035*SL	0.68 + 0.025*SL	0.75 + 0.019*SL
	t_R	0.30	0.19 + 0.054*SL	0.20 + 0.052*SL	0.19 + 0.053*SL
	t_F	0.34	0.27 + 0.037*SL	0.29 + 0.028*SL	0.34 + 0.023*SL
D1 to Y	t_{PLH}	0.59	0.53 + 0.032*SL	0.54 + 0.028*SL	0.57 + 0.025*SL
	t_{PHL}	0.72	0.65 + 0.035*SL	0.68 + 0.026*SL	0.75 + 0.019*SL
	t_R	0.30	0.19 + 0.054*SL	0.20 + 0.052*SL	0.19 + 0.053*SL
	t_F	0.34	0.27 + 0.037*SL	0.29 + 0.027*SL	0.35 + 0.023*SL
D2 to Y	t_{PLH}	0.59	0.53 + 0.032*SL	0.54 + 0.027*SL	0.56 + 0.025*SL
	t_{PHL}	0.72	0.65 + 0.035*SL	0.67 + 0.025*SL	0.74 + 0.019*SL
	t_R	0.30	0.19 + 0.054*SL	0.20 + 0.052*SL	0.19 + 0.053*SL
	t_F	0.34	0.26 + 0.037*SL	0.29 + 0.028*SL	0.34 + 0.023*SL
D3 to Y	t_{PLH}	0.59	0.52 + 0.032*SL	0.54 + 0.027*SL	0.56 + 0.025*SL
	t_{PHL}	0.72	0.65 + 0.035*SL	0.68 + 0.025*SL	0.75 + 0.019*SL
	t_R	0.30	0.19 + 0.054*SL	0.20 + 0.052*SL	0.19 + 0.053*SL
	t_F	0.34	0.27 + 0.037*SL	0.29 + 0.028*SL	0.35 + 0.023*SL
S0 to Y	t_{PLH}	0.71	0.64 + 0.032*SL	0.65 + 0.028*SL	0.68 + 0.025*SL
	t_{PHL}	0.59	0.52 + 0.035*SL	0.54 + 0.025*SL	0.61 + 0.019*SL
	t_R	0.30	0.19 + 0.054*SL	0.20 + 0.052*SL	0.19 + 0.053*SL
	t_F	0.33	0.25 + 0.037*SL	0.28 + 0.028*SL	0.34 + 0.023*SL
S1 to Y	t_{PLH}	0.52	0.45 + 0.032*SL	0.46 + 0.028*SL	0.49 + 0.025*SL
	t_{PHL}	0.41	0.35 + 0.031*SL	0.37 + 0.024*SL	0.43 + 0.018*SL
	t_R	0.29	0.18 + 0.056*SL	0.19 + 0.053*SL	0.19 + 0.053*SL
	t_F	0.26	0.19 + 0.038*SL	0.21 + 0.029*SL	0.27 + 0.024*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



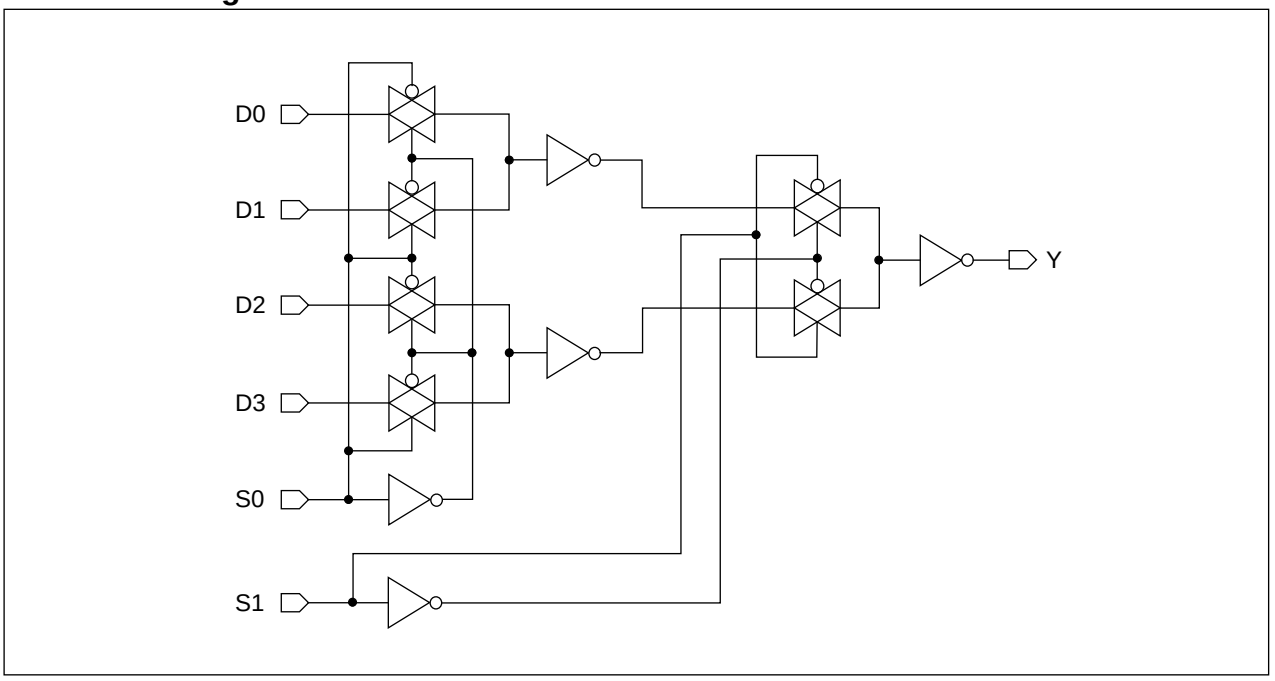
Truth Table

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)												Gate Count	
KG80													
YMX4						*YMX4D2*						*YMX4*	*YMX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
2.9	2.9	2.9	2.9	2.3	1.5	2.9	2.9	2.9	2.9	2.3	1.5	6.0	6.0
KGM80													
YMX4						*YMX4D2*						*YMX4*	*YMX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
3.7	3.7	3.7	3.7	2.7	1.7	3.7	3.7	3.7	3.7	2.7	1.7	6.0	6.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YMX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.37	0.28 + 0.045*SL	0.29 + 0.041*SL	0.28 + 0.042*SL
	t_{PHL}	0.41	0.34 + 0.037*SL	0.36 + 0.029*SL	0.39 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
D1 to Y	t_{PLH}	0.37	0.28 + 0.043*SL	0.29 + 0.041*SL	0.29 + 0.041*SL
	t_{PHL}	0.41	0.34 + 0.037*SL	0.36 + 0.029*SL	0.39 + 0.025*SL
	t_R	0.28	0.11 + 0.086*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.13 + 0.041*SL
D2 to Y	t_{PLH}	0.37	0.28 + 0.044*SL	0.29 + 0.041*SL	0.28 + 0.041*SL
	t_{PHL}	0.42	0.34 + 0.037*SL	0.36 + 0.029*SL	0.39 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
D3 to Y	t_{PLH}	0.37	0.28 + 0.045*SL	0.29 + 0.041*SL	0.29 + 0.041*SL
	t_{PHL}	0.42	0.34 + 0.038*SL	0.36 + 0.029*SL	0.39 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
S0 to Y	t_{PLH}	0.49	0.40 + 0.043*SL	0.41 + 0.041*SL	0.41 + 0.041*SL
	t_{PHL}	0.39	0.31 + 0.038*SL	0.34 + 0.029*SL	0.36 + 0.025*SL
	t_R	0.27	0.10 + 0.085*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.12 + 0.041*SL	0.13 + 0.041*SL
S1 to Y	t_{PLH}	0.38	0.29 + 0.043*SL	0.29 + 0.041*SL	0.29 + 0.042*SL
	t_{PHL}	0.27	0.20 + 0.035*SL	0.22 + 0.028*SL	0.24 + 0.025*SL
	t_R	0.27	0.10 + 0.087*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.19	0.10 + 0.046*SL	0.11 + 0.042*SL	0.11 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YMX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.36	0.31 + 0.024*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.41	0.36 + 0.023*SL	0.38 + 0.018*SL	0.40 + 0.015*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.043*SL	0.10 + 0.045*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
D1 to Y	t_{PLH}	0.36	0.32 + 0.023*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.41	0.36 + 0.023*SL	0.37 + 0.018*SL	0.39 + 0.015*SL
	t_R	0.20	0.12 + 0.043*SL	0.11 + 0.043*SL	0.10 + 0.045*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
D2 to Y	t_{PLH}	0.36	0.31 + 0.024*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.41	0.37 + 0.022*SL	0.38 + 0.018*SL	0.40 + 0.015*SL
	t_R	0.20	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.18	0.14 + 0.025*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
D3 to Y	t_{PLH}	0.36	0.31 + 0.024*SL	0.32 + 0.021*SL	0.32 + 0.021*SL
	t_{PHL}	0.41	0.36 + 0.023*SL	0.38 + 0.018*SL	0.40 + 0.015*SL
	t_R	0.20	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.18	0.14 + 0.025*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
S0 to Y	t_{PLH}	0.48	0.43 + 0.023*SL	0.43 + 0.022*SL	0.44 + 0.021*SL
	t_{PHL}	0.38	0.34 + 0.023*SL	0.35 + 0.018*SL	0.37 + 0.015*SL
	t_R	0.20	0.11 + 0.042*SL	0.11 + 0.044*SL	0.10 + 0.045*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
S1 to Y	t_{PLH}	0.36	0.32 + 0.023*SL	0.32 + 0.022*SL	0.32 + 0.021*SL
	t_{PHL}	0.26	0.22 + 0.021*SL	0.23 + 0.018*SL	0.25 + 0.015*SL
	t_R	0.20	0.12 + 0.041*SL	0.11 + 0.044*SL	0.10 + 0.045*SL
	t_F	0.17	0.12 + 0.023*SL	0.12 + 0.022*SL	0.13 + 0.021*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YMX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.53	0.42 + 0.054*SL	0.43 + 0.050*SL	0.43 + 0.050*SL
	t_{PHL}	0.59	0.50 + 0.045*SL	0.53 + 0.031*SL	0.60 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.27	0.16 + 0.050*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
D1 to Y	t_{PLH}	0.53	0.43 + 0.053*SL	0.44 + 0.050*SL	0.44 + 0.050*SL
	t_{PHL}	0.58	0.49 + 0.045*SL	0.53 + 0.031*SL	0.59 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.27	0.16 + 0.050*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
D2 to Y	t_{PLH}	0.53	0.42 + 0.054*SL	0.43 + 0.050*SL	0.43 + 0.050*SL
	t_{PHL}	0.59	0.50 + 0.045*SL	0.54 + 0.031*SL	0.60 + 0.025*SL
	t_R	0.36	0.15 + 0.102*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.050*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
D3 to Y	t_{PLH}	0.53	0.43 + 0.054*SL	0.43 + 0.050*SL	0.44 + 0.050*SL
	t_{PHL}	0.59	0.50 + 0.045*SL	0.53 + 0.031*SL	0.60 + 0.025*SL
	t_R	0.36	0.15 + 0.102*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.050*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
S0 to Y	t_{PLH}	0.65	0.54 + 0.054*SL	0.55 + 0.050*SL	0.56 + 0.050*SL
	t_{PHL}	0.57	0.48 + 0.045*SL	0.52 + 0.031*SL	0.58 + 0.025*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.050*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
S1 to Y	t_{PLH}	0.49	0.39 + 0.054*SL	0.40 + 0.050*SL	0.40 + 0.050*SL
	t_{PHL}	0.39	0.31 + 0.042*SL	0.34 + 0.030*SL	0.39 + 0.025*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.24	0.14 + 0.051*SL	0.16 + 0.043*SL	0.18 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YMX4D2

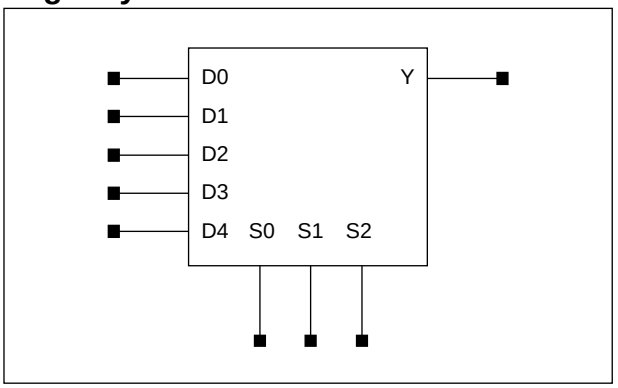
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.52	0.46 + 0.030*SL	0.47 + 0.026*SL	0.48 + 0.025*SL
	t_{PHL}	0.59	0.53 + 0.028*SL	0.55 + 0.020*SL	0.60 + 0.015*SL
	t_R	0.26	0.15 + 0.054*SL	0.16 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D1 to Y	t_{PLH}	0.52	0.46 + 0.030*SL	0.47 + 0.026*SL	0.48 + 0.025*SL
	t_{PHL}	0.58	0.53 + 0.028*SL	0.55 + 0.020*SL	0.60 + 0.015*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D2 to Y	t_{PLH}	0.51	0.45 + 0.030*SL	0.46 + 0.026*SL	0.47 + 0.025*SL
	t_{PHL}	0.59	0.53 + 0.029*SL	0.56 + 0.020*SL	0.61 + 0.015*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D3 to Y	t_{PLH}	0.52	0.46 + 0.030*SL	0.47 + 0.026*SL	0.48 + 0.025*SL
	t_{PHL}	0.59	0.53 + 0.029*SL	0.55 + 0.020*SL	0.60 + 0.015*SL
	t_R	0.26	0.16 + 0.052*SL	0.16 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
S0 to Y	t_{PLH}	0.64	0.58 + 0.030*SL	0.59 + 0.026*SL	0.60 + 0.025*SL
	t_{PHL}	0.57	0.51 + 0.029*SL	0.54 + 0.020*SL	0.59 + 0.015*SL
	t_R	0.26	0.15 + 0.052*SL	0.15 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
S1 to Y	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.026*SL	0.44 + 0.025*SL
	t_{PHL}	0.39	0.33 + 0.027*SL	0.35 + 0.020*SL	0.40 + 0.015*SL
	t_R	0.26	0.15 + 0.053*SL	0.15 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.22	0.16 + 0.029*SL	0.17 + 0.024*SL	0.21 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

MX5/MX5D2

5 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



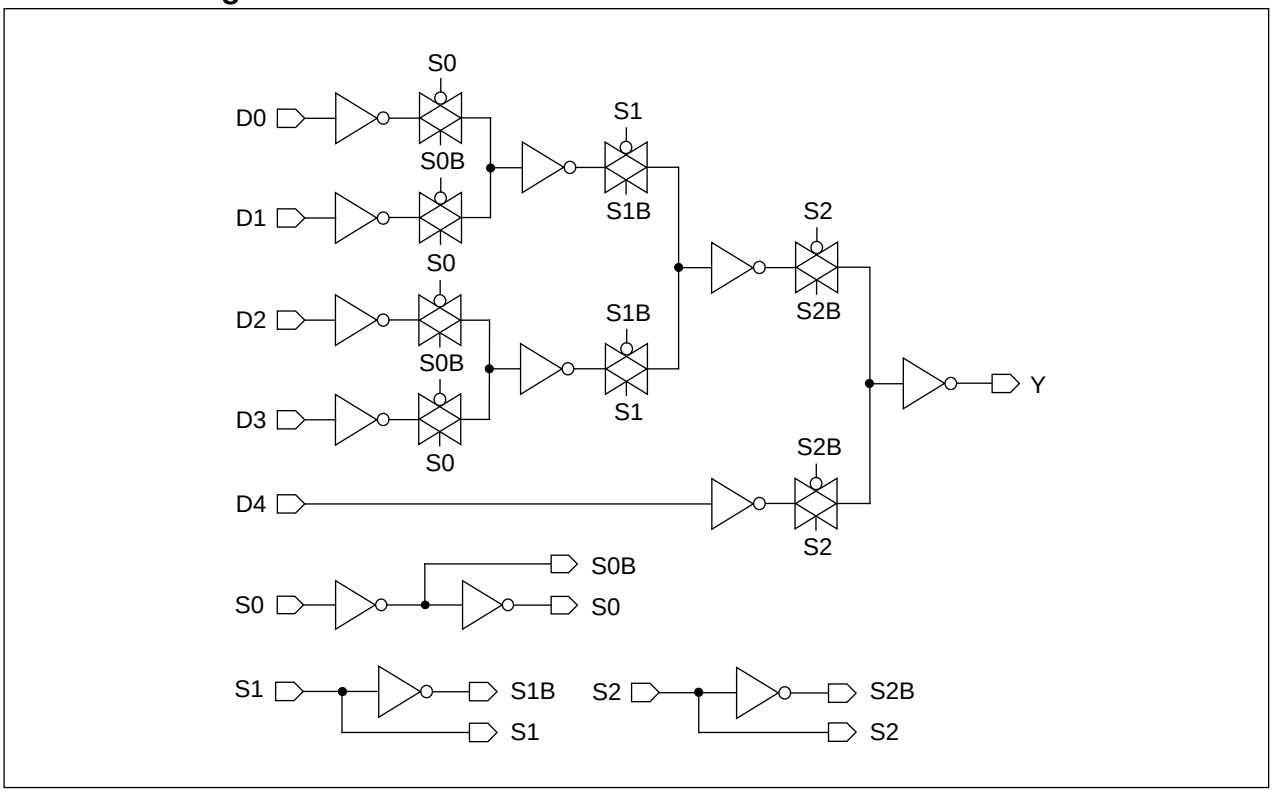
Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
x	x	1	D4

Cell Data

Input Load (SL)																Gate Count	
KG80																	
MX5								*MX5D2*								*MX5*	*MX5D2*
D0	D1	D2	D3	D4	S0	S1	S2	D0	D1	D2	D3	D4	S0	S1	S2		
0.9	0.9	0.9	0.9	1.0	0.9	1.7	1.2	0.9	0.9	0.9	0.9	1.0	0.9	1.7	1.2	11.0	11.0
KGM80																	
MX5								*MX5D2*								*MX5*	*MX5D2*
D0	D1	D2	D3	D4	S0	S1	S2	D0	D1	D2	D3	D4	S0	S1	S2		
1.0	1.0	1.0	1.0	1.0	1.0	2.0	1.8	1.0	1.0	1.0	1.0	1.0	1.0	2.0	1.8	11.0	11.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.70	0.62 + 0.043*SL	0.62 + 0.041*SL	0.62 + 0.041*SL
	t_{PHL}	0.76	0.68 + 0.036*SL	0.70 + 0.028*SL	0.73 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.12 + 0.041*SL	0.13 + 0.041*SL
D1 to Y	t_{PLH}	0.71	0.62 + 0.043*SL	0.62 + 0.041*SL	0.62 + 0.041*SL
	t_{PHL}	0.76	0.69 + 0.036*SL	0.71 + 0.028*SL	0.73 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.040*SL	0.13 + 0.041*SL
D2 to Y	t_{PLH}	0.69	0.61 + 0.043*SL	0.61 + 0.041*SL	0.61 + 0.042*SL
	t_{PHL}	0.75	0.68 + 0.036*SL	0.69 + 0.028*SL	0.72 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.040*SL	0.13 + 0.041*SL
D3 to Y	t_{PLH}	0.70	0.61 + 0.043*SL	0.61 + 0.041*SL	0.61 + 0.042*SL
	t_{PHL}	0.75	0.68 + 0.036*SL	0.70 + 0.028*SL	0.72 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.040*SL	0.12 + 0.041*SL
D4 to Y	t_{PLH}	0.32	0.24 + 0.043*SL	0.24 + 0.041*SL	0.24 + 0.042*SL
	t_{PHL}	0.38	0.31 + 0.036*SL	0.33 + 0.028*SL	0.35 + 0.025*SL
	t_R	0.28	0.13 + 0.079*SL	0.11 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
S0 to Y	t_{PLH}	0.87	0.78 + 0.043*SL	0.78 + 0.041*SL	0.78 + 0.041*SL
	t_{PHL}	0.75	0.68 + 0.036*SL	0.69 + 0.028*SL	0.72 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.040*SL	0.13 + 0.041*SL
S1 to Y	t_{PLH}	0.52	0.44 + 0.043*SL	0.44 + 0.041*SL	0.44 + 0.041*SL
	t_{PHL}	0.40	0.33 + 0.036*SL	0.35 + 0.028*SL	0.38 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.043*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
S2 to Y	t_{PLH}	0.38	0.29 + 0.043*SL	0.30 + 0.041*SL	0.29 + 0.042*SL
	t_{PHL}	0.27	0.20 + 0.035*SL	0.22 + 0.028*SL	0.24 + 0.025*SL
	t_R	0.28	0.10 + 0.087*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.11 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.68	0.64 + 0.024*SL	0.64 + 0.022*SL	0.65 + 0.021*SL
	t_{PHL}	0.75	0.70 + 0.024*SL	0.71 + 0.018*SL	0.74 + 0.015*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
D1 to Y	t_{PLH}	0.69	0.64 + 0.024*SL	0.65 + 0.021*SL	0.65 + 0.021*SL
	t_{PHL}	0.75	0.70 + 0.025*SL	0.72 + 0.018*SL	0.74 + 0.015*SL
	t_R	0.19	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
D2 to Y	t_{PLH}	0.68	0.63 + 0.024*SL	0.63 + 0.022*SL	0.64 + 0.021*SL
	t_{PHL}	0.74	0.69 + 0.025*SL	0.70 + 0.018*SL	0.73 + 0.015*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.042*SL	0.09 + 0.044*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
D3 to Y	t_{PLH}	0.68	0.63 + 0.025*SL	0.64 + 0.021*SL	0.64 + 0.021*SL
	t_{PHL}	0.74	0.69 + 0.024*SL	0.71 + 0.018*SL	0.73 + 0.015*SL
	t_R	0.18	0.10 + 0.041*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.020*SL
D4 to Y	t_{PLH}	0.30	0.26 + 0.024*SL	0.26 + 0.021*SL	0.27 + 0.021*SL
	t_{PHL}	0.37	0.32 + 0.026*SL	0.34 + 0.018*SL	0.36 + 0.015*SL
	t_R	0.18	0.10 + 0.040*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.18	0.14 + 0.022*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
S0 to Y	t_{PLH}	0.85	0.80 + 0.025*SL	0.81 + 0.021*SL	0.81 + 0.021*SL
	t_{PHL}	0.74	0.69 + 0.024*SL	0.70 + 0.018*SL	0.73 + 0.015*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.042*SL	0.09 + 0.044*SL
	t_F	0.17	0.12 + 0.026*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
S1 to Y	t_{PLH}	0.51	0.46 + 0.024*SL	0.46 + 0.022*SL	0.47 + 0.021*SL
	t_{PHL}	0.40	0.35 + 0.024*SL	0.36 + 0.018*SL	0.38 + 0.015*SL
	t_R	0.18	0.10 + 0.040*SL	0.10 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.14 + 0.021*SL
S2 to Y	t_{PLH}	0.35	0.31 + 0.023*SL	0.31 + 0.022*SL	0.32 + 0.021*SL
	t_{PHL}	0.26	0.21 + 0.023*SL	0.22 + 0.018*SL	0.25 + 0.015*SL
	t_R	0.18	0.09 + 0.042*SL	0.09 + 0.043*SL	0.08 + 0.044*SL
	t_F	0.16	0.11 + 0.025*SL	0.11 + 0.022*SL	0.12 + 0.021*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	1.01	0.90 + 0.053*SL	0.91 + 0.050*SL	0.91 + 0.050*SL
	t_{PHL}	1.09	1.00 + 0.043*SL	1.04 + 0.030*SL	1.09 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
D1 to Y	t_{PLH}	1.01	0.90 + 0.053*SL	0.91 + 0.050*SL	0.91 + 0.050*SL
	t_{PHL}	1.09	1.01 + 0.043*SL	1.04 + 0.030*SL	1.10 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
D2 to Y	t_{PLH}	1.00	0.89 + 0.053*SL	0.90 + 0.050*SL	0.90 + 0.050*SL
	t_{PHL}	1.07	0.98 + 0.043*SL	1.02 + 0.030*SL	1.08 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
D3 to Y	t_{PLH}	1.00	0.89 + 0.053*SL	0.90 + 0.050*SL	0.90 + 0.050*SL
	t_{PHL}	1.07	0.99 + 0.043*SL	1.02 + 0.030*SL	1.08 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
D4 to Y	t_{PLH}	0.43	0.32 + 0.051*SL	0.33 + 0.050*SL	0.33 + 0.050*SL
	t_{PHL}	0.52	0.43 + 0.043*SL	0.47 + 0.030*SL	0.52 + 0.025*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.049*SL	0.19 + 0.042*SL	0.19 + 0.041*SL
S0 to Y	t_{PLH}	1.23	1.12 + 0.053*SL	1.13 + 0.050*SL	1.13 + 0.050*SL
	t_{PHL}	1.08	0.99 + 0.043*SL	1.03 + 0.030*SL	1.08 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
S1 to Y	t_{PLH}	0.72	0.61 + 0.053*SL	0.62 + 0.050*SL	0.62 + 0.050*SL
	t_{PHL}	0.59	0.50 + 0.043*SL	0.54 + 0.030*SL	0.59 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.26	0.16 + 0.049*SL	0.18 + 0.042*SL	0.19 + 0.041*SL
S2 to Y	t_{PLH}	0.49	0.39 + 0.052*SL	0.39 + 0.050*SL	0.40 + 0.050*SL
	t_{PHL}	0.38	0.30 + 0.040*SL	0.33 + 0.029*SL	0.38 + 0.025*SL
	t_R	0.36	0.15 + 0.104*SL	0.14 + 0.107*SL	0.13 + 0.109*SL
	t_F	0.24	0.14 + 0.050*SL	0.16 + 0.043*SL	0.17 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

Switching Characteristics

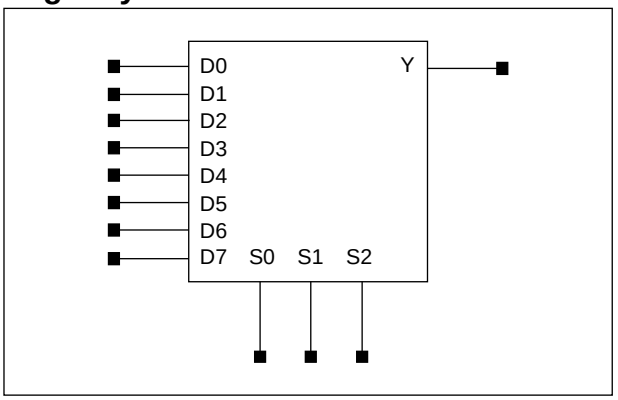
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.98	0.92 + 0.031*SL	0.93 + 0.026*SL	0.95 + 0.025*SL
	t_{PHL}	1.08	1.02 + 0.030*SL	1.05 + 0.021*SL	1.10 + 0.016*SL
	t_R	0.24	0.13 + 0.053*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.22	0.16 + 0.031*SL	0.18 + 0.024*SL	0.21 + 0.021*SL
D1 to Y	t_{PLH}	0.99	0.92 + 0.031*SL	0.94 + 0.026*SL	0.95 + 0.025*SL
	t_{PHL}	1.09	1.03 + 0.030*SL	1.05 + 0.021*SL	1.11 + 0.015*SL
	t_R	0.24	0.13 + 0.053*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.22	0.16 + 0.031*SL	0.18 + 0.024*SL	0.21 + 0.021*SL
D2 to Y	t_{PLH}	0.97	0.91 + 0.031*SL	0.92 + 0.026*SL	0.94 + 0.025*SL
	t_{PHL}	1.07	1.01 + 0.030*SL	1.03 + 0.021*SL	1.09 + 0.016*SL
	t_R	0.24	0.13 + 0.053*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.22	0.16 + 0.031*SL	0.18 + 0.024*SL	0.21 + 0.021*SL
D3 to Y	t_{PLH}	0.97	0.91 + 0.031*SL	0.92 + 0.026*SL	0.94 + 0.025*SL
	t_{PHL}	1.07	1.01 + 0.030*SL	1.03 + 0.021*SL	1.09 + 0.016*SL
	t_R	0.24	0.13 + 0.052*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.22	0.16 + 0.031*SL	0.18 + 0.024*SL	0.21 + 0.021*SL
D4 to Y	t_{PLH}	0.40	0.34 + 0.029*SL	0.35 + 0.026*SL	0.36 + 0.025*SL
	t_{PHL}	0.51	0.45 + 0.030*SL	0.48 + 0.021*SL	0.53 + 0.016*SL
	t_R	0.23	0.13 + 0.053*SL	0.13 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.23	0.17 + 0.031*SL	0.19 + 0.024*SL	0.22 + 0.021*SL
S0 to Y	t_{PLH}	1.20	1.14 + 0.030*SL	1.15 + 0.026*SL	1.16 + 0.025*SL
	t_{PHL}	1.07	1.01 + 0.030*SL	1.04 + 0.021*SL	1.09 + 0.015*SL
	t_R	0.24	0.13 + 0.052*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.22	0.16 + 0.032*SL	0.18 + 0.024*SL	0.21 + 0.021*SL
S1 to Y	t_{PLH}	0.69	0.63 + 0.031*SL	0.64 + 0.026*SL	0.65 + 0.025*SL
	t_{PHL}	0.58	0.52 + 0.030*SL	0.55 + 0.021*SL	0.60 + 0.015*SL
	t_R	0.23	0.13 + 0.053*SL	0.13 + 0.052*SL	0.12 + 0.053*SL
	t_F	0.22	0.16 + 0.032*SL	0.18 + 0.024*SL	0.22 + 0.021*SL
S2 to Y	t_{PLH}	0.46	0.40 + 0.030*SL	0.41 + 0.026*SL	0.42 + 0.025*SL
	t_{PHL}	0.37	0.31 + 0.029*SL	0.33 + 0.020*SL	0.38 + 0.015*SL
	t_R	0.23	0.13 + 0.052*SL	0.13 + 0.052*SL	0.11 + 0.054*SL
	t_F	0.20	0.14 + 0.032*SL	0.16 + 0.024*SL	0.19 + 0.022*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

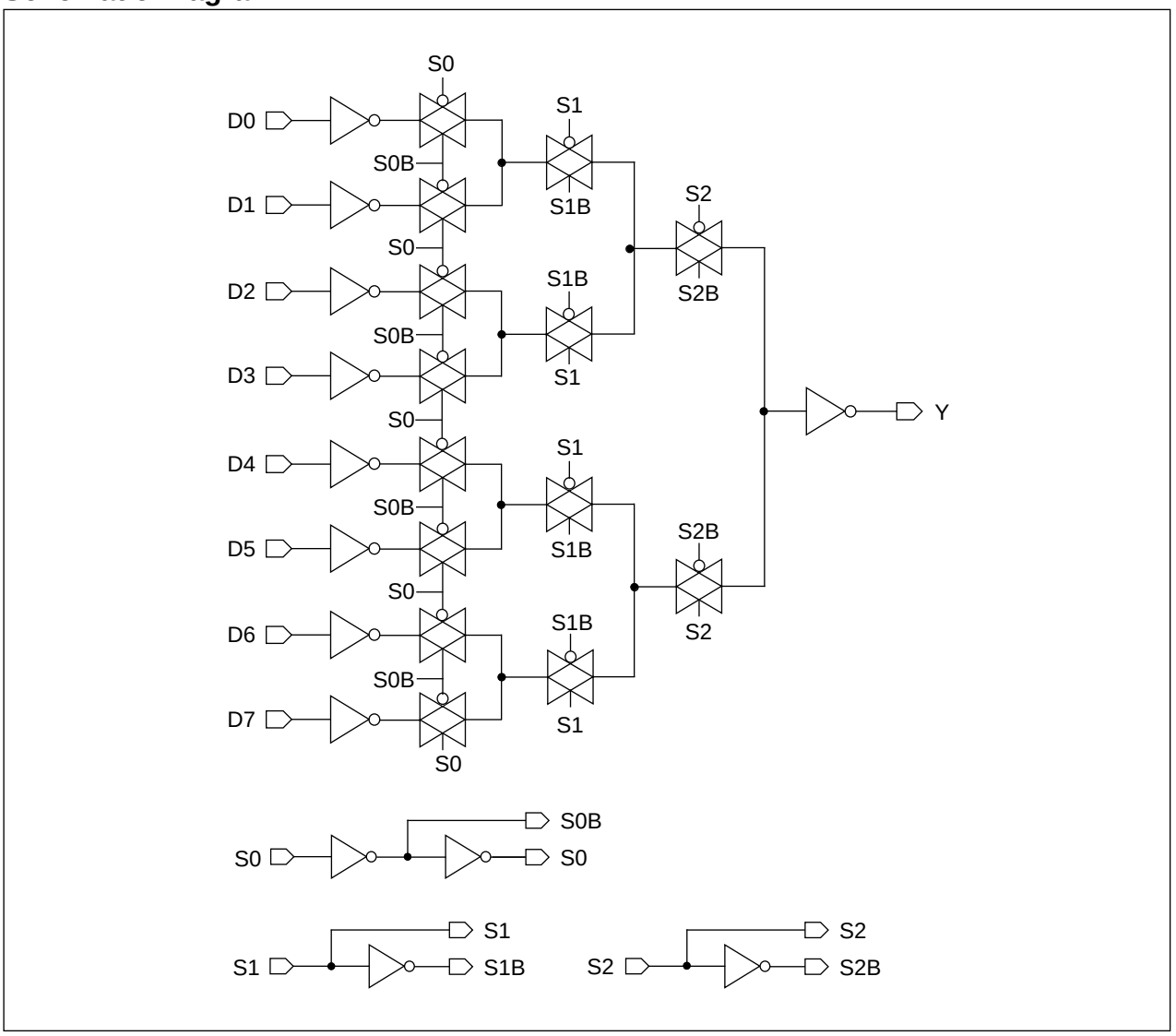
Cell Data

Input Load (SL)											Gate Count
KG80											
MX8											*MX8*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.8	0.9	1.0	0.9	0.9	0.9	1.0	0.9	0.9	1.8	1.2	14.0
MX8D2											*MX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.8	0.9	1.0	0.9	0.9	0.9	1.0	0.9	0.9	1.8	1.2	15.0
KGM80											
MX8											*MX8*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.1	2.8	1.8	14.0
MX8D2											*MX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.1	2.8	1.8	15.0

MX8/MX8D2

8 > 1 Non-Inverting MUX with 1X/2X Drive

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.59	0.49 + 0.050*SL	0.51 + 0.044*SL	0.52 + 0.042*SL
	t_{PHL}	0.63	0.53 + 0.053*SL	0.56 + 0.040*SL	0.61 + 0.032*SL
	t_R	0.34	0.17 + 0.085*SL	0.17 + 0.085*SL	0.15 + 0.087*SL
	t_F	0.34	0.23 + 0.058*SL	0.25 + 0.048*SL	0.29 + 0.043*SL
D1 to Y	t_{PLH}	0.59	0.49 + 0.050*SL	0.51 + 0.044*SL	0.52 + 0.042*SL
	t_{PHL}	0.64	0.53 + 0.052*SL	0.56 + 0.040*SL	0.61 + 0.032*SL
	t_R	0.34	0.17 + 0.085*SL	0.17 + 0.085*SL	0.15 + 0.087*SL
	t_F	0.34	0.23 + 0.058*SL	0.25 + 0.048*SL	0.29 + 0.043*SL
D2 to Y	t_{PLH}	0.59	0.49 + 0.049*SL	0.50 + 0.044*SL	0.52 + 0.042*SL
	t_{PHL}	0.63	0.53 + 0.053*SL	0.56 + 0.040*SL	0.61 + 0.032*SL
	t_R	0.34	0.17 + 0.086*SL	0.17 + 0.085*SL	0.15 + 0.087*SL
	t_F	0.34	0.23 + 0.058*SL	0.25 + 0.048*SL	0.29 + 0.042*SL
D3 to Y	t_{PLH}	0.59	0.49 + 0.049*SL	0.50 + 0.044*SL	0.52 + 0.042*SL
	t_{PHL}	0.63	0.53 + 0.053*SL	0.56 + 0.040*SL	0.61 + 0.032*SL
	t_R	0.34	0.17 + 0.085*SL	0.17 + 0.086*SL	0.15 + 0.087*SL
	t_F	0.34	0.23 + 0.058*SL	0.25 + 0.048*SL	0.29 + 0.042*SL
D4 to Y	t_{PLH}	0.59	0.49 + 0.049*SL	0.50 + 0.044*SL	0.52 + 0.042*SL
	t_{PHL}	0.63	0.53 + 0.052*SL	0.56 + 0.040*SL	0.61 + 0.032*SL
	t_R	0.34	0.17 + 0.084*SL	0.17 + 0.085*SL	0.15 + 0.088*SL
	t_F	0.34	0.22 + 0.059*SL	0.25 + 0.048*SL	0.29 + 0.043*SL
D5 to Y	t_{PLH}	0.59	0.49 + 0.049*SL	0.50 + 0.044*SL	0.52 + 0.042*SL
	t_{PHL}	0.63	0.53 + 0.053*SL	0.56 + 0.040*SL	0.61 + 0.032*SL
	t_R	0.34	0.17 + 0.083*SL	0.17 + 0.085*SL	0.15 + 0.087*SL
	t_F	0.34	0.22 + 0.059*SL	0.25 + 0.048*SL	0.29 + 0.043*SL
D6 to Y	t_{PLH}	0.58	0.48 + 0.050*SL	0.50 + 0.044*SL	0.51 + 0.042*SL
	t_{PHL}	0.63	0.52 + 0.052*SL	0.55 + 0.040*SL	0.60 + 0.032*SL
	t_R	0.34	0.17 + 0.083*SL	0.17 + 0.085*SL	0.15 + 0.087*SL
	t_F	0.34	0.22 + 0.060*SL	0.25 + 0.047*SL	0.29 + 0.042*SL
D7 to Y	t_{PLH}	0.58	0.48 + 0.050*SL	0.50 + 0.044*SL	0.51 + 0.042*SL
	t_{PHL}	0.63	0.52 + 0.052*SL	0.55 + 0.040*SL	0.61 + 0.032*SL
	t_R	0.34	0.17 + 0.085*SL	0.17 + 0.085*SL	0.15 + 0.087*SL
	t_F	0.34	0.22 + 0.059*SL	0.25 + 0.047*SL	0.28 + 0.043*SL
S0 to Y	t_{PLH}	0.85	0.75 + 0.050*SL	0.76 + 0.044*SL	0.78 + 0.042*SL
	t_{PHL}	0.72	0.62 + 0.052*SL	0.65 + 0.040*SL	0.70 + 0.032*SL
	t_R	0.34	0.17 + 0.085*SL	0.17 + 0.085*SL	0.15 + 0.087*SL
	t_F	0.33	0.22 + 0.059*SL	0.24 + 0.048*SL	0.28 + 0.043*SL
S1 to Y	t_{PLH}	0.56	0.46 + 0.050*SL	0.48 + 0.044*SL	0.49 + 0.042*SL
	t_{PHL}	0.42	0.32 + 0.051*SL	0.35 + 0.039*SL	0.40 + 0.032*SL
	t_R	0.34	0.17 + 0.085*SL	0.16 + 0.086*SL	0.15 + 0.088*SL
	t_F	0.30	0.17 + 0.063*SL	0.21 + 0.050*SL	0.25 + 0.044*SL
S2 to Y	t_{PLH}	0.42	0.32 + 0.050*SL	0.33 + 0.044*SL	0.35 + 0.042*SL
	t_{PHL}	0.29	0.21 + 0.042*SL	0.23 + 0.035*SL	0.26 + 0.030*SL
	t_R	0.31	0.13 + 0.089*SL	0.13 + 0.088*SL	0.13 + 0.089*SL
	t_F	0.23	0.11 + 0.058*SL	0.13 + 0.050*SL	0.16 + 0.045*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 MX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.60	0.54 + 0.029*SL	0.55 + 0.024*SL	0.57 + 0.022*SL
	t_{PHL}	0.63	0.57 + 0.031*SL	0.59 + 0.025*SL	0.62 + 0.021*SL
	t_R	0.28	0.20 + 0.038*SL	0.19 + 0.042*SL	0.19 + 0.043*SL
	t_F	0.32	0.25 + 0.034*SL	0.27 + 0.028*SL	0.29 + 0.024*SL
D1 to Y	t_{PLH}	0.60	0.54 + 0.029*SL	0.55 + 0.024*SL	0.57 + 0.022*SL
	t_{PHL}	0.64	0.57 + 0.031*SL	0.59 + 0.025*SL	0.62 + 0.021*SL
	t_R	0.28	0.20 + 0.039*SL	0.19 + 0.043*SL	0.19 + 0.042*SL
	t_F	0.32	0.25 + 0.034*SL	0.27 + 0.028*SL	0.29 + 0.024*SL
D2 to Y	t_{PLH}	0.59	0.54 + 0.029*SL	0.55 + 0.024*SL	0.56 + 0.022*SL
	t_{PHL}	0.63	0.57 + 0.031*SL	0.59 + 0.025*SL	0.62 + 0.020*SL
	t_R	0.28	0.20 + 0.040*SL	0.19 + 0.042*SL	0.19 + 0.042*SL
	t_F	0.32	0.25 + 0.033*SL	0.26 + 0.028*SL	0.29 + 0.024*SL
D3 to Y	t_{PLH}	0.59	0.54 + 0.028*SL	0.55 + 0.024*SL	0.56 + 0.022*SL
	t_{PHL}	0.63	0.57 + 0.031*SL	0.59 + 0.025*SL	0.62 + 0.021*SL
	t_R	0.28	0.20 + 0.040*SL	0.20 + 0.042*SL	0.19 + 0.043*SL
	t_F	0.32	0.25 + 0.033*SL	0.26 + 0.028*SL	0.29 + 0.024*SL
D4 to Y	t_{PLH}	0.60	0.54 + 0.029*SL	0.55 + 0.024*SL	0.56 + 0.022*SL
	t_{PHL}	0.63	0.57 + 0.031*SL	0.59 + 0.025*SL	0.62 + 0.021*SL
	t_R	0.28	0.20 + 0.040*SL	0.20 + 0.042*SL	0.19 + 0.043*SL
	t_F	0.32	0.25 + 0.035*SL	0.26 + 0.028*SL	0.29 + 0.024*SL
D5 to Y	t_{PLH}	0.59	0.54 + 0.029*SL	0.55 + 0.024*SL	0.56 + 0.022*SL
	t_{PHL}	0.63	0.57 + 0.031*SL	0.58 + 0.025*SL	0.62 + 0.020*SL
	t_R	0.28	0.20 + 0.041*SL	0.20 + 0.042*SL	0.19 + 0.043*SL
	t_F	0.32	0.25 + 0.034*SL	0.26 + 0.028*SL	0.29 + 0.024*SL
D6 to Y	t_{PLH}	0.59	0.53 + 0.028*SL	0.54 + 0.024*SL	0.55 + 0.022*SL
	t_{PHL}	0.63	0.56 + 0.031*SL	0.58 + 0.025*SL	0.61 + 0.020*SL
	t_R	0.28	0.20 + 0.040*SL	0.19 + 0.042*SL	0.19 + 0.043*SL
	t_F	0.32	0.25 + 0.034*SL	0.26 + 0.028*SL	0.29 + 0.024*SL
D7 to Y	t_{PLH}	0.59	0.53 + 0.028*SL	0.54 + 0.024*SL	0.55 + 0.022*SL
	t_{PHL}	0.63	0.57 + 0.031*SL	0.58 + 0.025*SL	0.61 + 0.020*SL
	t_R	0.28	0.20 + 0.041*SL	0.19 + 0.042*SL	0.19 + 0.042*SL
	t_F	0.32	0.25 + 0.034*SL	0.26 + 0.028*SL	0.29 + 0.025*SL
S0 to Y	t_{PLH}	0.85	0.80 + 0.028*SL	0.81 + 0.024*SL	0.82 + 0.022*SL
	t_{PHL}	0.72	0.66 + 0.031*SL	0.67 + 0.025*SL	0.70 + 0.020*SL
	t_R	0.28	0.20 + 0.040*SL	0.19 + 0.042*SL	0.19 + 0.042*SL
	t_F	0.31	0.24 + 0.034*SL	0.26 + 0.028*SL	0.28 + 0.025*SL
S1 to Y	t_{PLH}	0.57	0.51 + 0.029*SL	0.52 + 0.024*SL	0.53 + 0.022*SL
	t_{PHL}	0.42	0.36 + 0.031*SL	0.37 + 0.025*SL	0.40 + 0.020*SL
	t_R	0.28	0.20 + 0.040*SL	0.19 + 0.043*SL	0.19 + 0.043*SL
	t_F	0.28	0.21 + 0.036*SL	0.22 + 0.029*SL	0.25 + 0.026*SL
S2 to Y	t_{PLH}	0.42	0.36 + 0.028*SL	0.37 + 0.024*SL	0.39 + 0.022*SL
	t_{PHL}	0.29	0.24 + 0.026*SL	0.25 + 0.022*SL	0.27 + 0.019*SL
	t_R	0.25	0.17 + 0.043*SL	0.17 + 0.044*SL	0.17 + 0.043*SL
	t_F	0.21	0.14 + 0.034*SL	0.15 + 0.030*SL	0.18 + 0.026*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.82	0.69 + 0.063*SL	0.72 + 0.053*SL	0.76 + 0.050*SL
	t_{PHL}	0.94	0.80 + 0.070*SL	0.87 + 0.047*SL	1.01 + 0.034*SL
	t_R	0.43	0.21 + 0.109*SL	0.22 + 0.105*SL	0.21 + 0.106*SL
	t_F	0.48	0.33 + 0.075*SL	0.39 + 0.052*SL	0.48 + 0.044*SL
D1 to Y	t_{PLH}	0.82	0.70 + 0.063*SL	0.72 + 0.053*SL	0.76 + 0.050*SL
	t_{PHL}	0.95	0.80 + 0.070*SL	0.87 + 0.047*SL	1.01 + 0.034*SL
	t_R	0.43	0.21 + 0.109*SL	0.22 + 0.105*SL	0.21 + 0.106*SL
	t_F	0.48	0.33 + 0.073*SL	0.39 + 0.052*SL	0.48 + 0.044*SL
D2 to Y	t_{PLH}	0.81	0.69 + 0.063*SL	0.71 + 0.053*SL	0.75 + 0.050*SL
	t_{PHL}	0.94	0.80 + 0.070*SL	0.87 + 0.047*SL	1.01 + 0.034*SL
	t_R	0.43	0.21 + 0.109*SL	0.22 + 0.105*SL	0.20 + 0.106*SL
	t_F	0.48	0.33 + 0.074*SL	0.39 + 0.052*SL	0.48 + 0.044*SL
D3 to Y	t_{PLH}	0.81	0.69 + 0.063*SL	0.71 + 0.053*SL	0.75 + 0.050*SL
	t_{PHL}	0.94	0.80 + 0.070*SL	0.86 + 0.047*SL	1.01 + 0.034*SL
	t_R	0.43	0.21 + 0.109*SL	0.22 + 0.105*SL	0.20 + 0.106*SL
	t_F	0.48	0.33 + 0.074*SL	0.39 + 0.052*SL	0.48 + 0.044*SL
D4 to Y	t_{PLH}	0.82	0.69 + 0.063*SL	0.72 + 0.053*SL	0.75 + 0.050*SL
	t_{PHL}	0.94	0.80 + 0.070*SL	0.86 + 0.047*SL	1.00 + 0.034*SL
	t_R	0.43	0.21 + 0.108*SL	0.22 + 0.105*SL	0.21 + 0.106*SL
	t_F	0.48	0.33 + 0.074*SL	0.39 + 0.052*SL	0.48 + 0.044*SL
D5 to Y	t_{PLH}	0.81	0.69 + 0.063*SL	0.71 + 0.053*SL	0.75 + 0.050*SL
	t_{PHL}	0.94	0.80 + 0.070*SL	0.86 + 0.047*SL	1.00 + 0.034*SL
	t_R	0.43	0.21 + 0.108*SL	0.22 + 0.105*SL	0.21 + 0.106*SL
	t_F	0.48	0.33 + 0.074*SL	0.39 + 0.052*SL	0.48 + 0.044*SL
D6 to Y	t_{PLH}	0.80	0.68 + 0.063*SL	0.70 + 0.053*SL	0.74 + 0.050*SL
	t_{PHL}	0.93	0.79 + 0.070*SL	0.86 + 0.047*SL	1.00 + 0.034*SL
	t_R	0.43	0.21 + 0.108*SL	0.22 + 0.105*SL	0.20 + 0.106*SL
	t_F	0.47	0.33 + 0.074*SL	0.39 + 0.052*SL	0.48 + 0.043*SL
D7 to Y	t_{PLH}	0.80	0.68 + 0.063*SL	0.70 + 0.053*SL	0.74 + 0.050*SL
	t_{PHL}	0.93	0.79 + 0.070*SL	0.86 + 0.047*SL	1.00 + 0.034*SL
	t_R	0.43	0.21 + 0.108*SL	0.22 + 0.105*SL	0.20 + 0.106*SL
	t_F	0.47	0.33 + 0.074*SL	0.39 + 0.052*SL	0.48 + 0.043*SL
S0 to Y	t_{PLH}	1.18	1.06 + 0.063*SL	1.08 + 0.053*SL	1.12 + 0.050*SL
	t_{PHL}	1.10	0.96 + 0.069*SL	1.02 + 0.046*SL	1.16 + 0.034*SL
	t_R	0.43	0.22 + 0.108*SL	0.22 + 0.105*SL	0.21 + 0.106*SL
	t_F	0.46	0.32 + 0.074*SL	0.38 + 0.052*SL	0.47 + 0.044*SL
S1 to Y	t_{PLH}	0.77	0.64 + 0.063*SL	0.67 + 0.053*SL	0.70 + 0.050*SL
	t_{PHL}	0.64	0.50 + 0.068*SL	0.56 + 0.046*SL	0.70 + 0.034*SL
	t_R	0.43	0.21 + 0.109*SL	0.22 + 0.105*SL	0.20 + 0.106*SL
	t_F	0.43	0.27 + 0.076*SL	0.33 + 0.053*SL	0.44 + 0.044*SL
S2 to Y	t_{PLH}	0.55	0.42 + 0.063*SL	0.45 + 0.053*SL	0.49 + 0.050*SL
	t_{PHL}	0.42	0.31 + 0.052*SL	0.35 + 0.039*SL	0.43 + 0.031*SL
	t_R	0.40	0.18 + 0.111*SL	0.19 + 0.106*SL	0.19 + 0.107*SL
	t_F	0.30	0.16 + 0.068*SL	0.20 + 0.053*SL	0.28 + 0.046*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

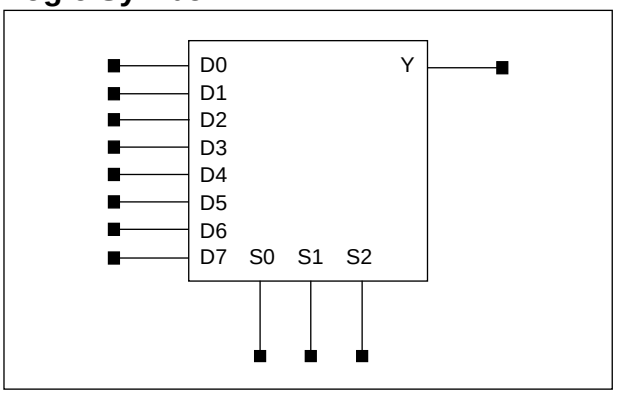
(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 MX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.83	0.76 + 0.035*SL	0.78 + 0.030*SL	0.81 + 0.026*SL
	t_{PHL}	0.96	0.88 + 0.042*SL	0.91 + 0.031*SL	0.99 + 0.023*SL
	t_R	0.35	0.23 + 0.058*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.46	0.37 + 0.043*SL	0.40 + 0.033*SL	0.48 + 0.026*SL
D1 to Y	t_{PLH}	0.83	0.76 + 0.035*SL	0.78 + 0.030*SL	0.81 + 0.026*SL
	t_{PHL}	0.96	0.88 + 0.042*SL	0.91 + 0.031*SL	0.99 + 0.023*SL
	t_R	0.35	0.23 + 0.058*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.46	0.37 + 0.044*SL	0.40 + 0.033*SL	0.48 + 0.026*SL
D2 to Y	t_{PLH}	0.82	0.76 + 0.035*SL	0.77 + 0.030*SL	0.80 + 0.026*SL
	t_{PHL}	0.96	0.87 + 0.042*SL	0.90 + 0.031*SL	0.99 + 0.023*SL
	t_R	0.34	0.23 + 0.057*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.46	0.37 + 0.043*SL	0.40 + 0.033*SL	0.47 + 0.026*SL
D3 to Y	t_{PLH}	0.82	0.76 + 0.034*SL	0.77 + 0.030*SL	0.80 + 0.026*SL
	t_{PHL}	0.96	0.87 + 0.042*SL	0.90 + 0.031*SL	0.99 + 0.023*SL
	t_R	0.34	0.23 + 0.057*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.46	0.37 + 0.044*SL	0.40 + 0.033*SL	0.48 + 0.026*SL
D4 to Y	t_{PLH}	0.83	0.76 + 0.035*SL	0.77 + 0.030*SL	0.81 + 0.026*SL
	t_{PHL}	0.96	0.87 + 0.042*SL	0.90 + 0.031*SL	0.99 + 0.023*SL
	t_R	0.35	0.23 + 0.057*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.45	0.36 + 0.045*SL	0.40 + 0.033*SL	0.48 + 0.026*SL
D5 to Y	t_{PLH}	0.83	0.76 + 0.035*SL	0.77 + 0.030*SL	0.80 + 0.026*SL
	t_{PHL}	0.96	0.87 + 0.042*SL	0.90 + 0.031*SL	0.98 + 0.023*SL
	t_R	0.35	0.23 + 0.057*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.45	0.36 + 0.044*SL	0.40 + 0.033*SL	0.47 + 0.026*SL
D6 to Y	t_{PLH}	0.81	0.74 + 0.035*SL	0.76 + 0.030*SL	0.79 + 0.026*SL
	t_{PHL}	0.95	0.86 + 0.042*SL	0.90 + 0.031*SL	0.98 + 0.023*SL
	t_R	0.35	0.23 + 0.056*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.45	0.36 + 0.044*SL	0.40 + 0.033*SL	0.47 + 0.025*SL
D7 to Y	t_{PLH}	0.81	0.74 + 0.035*SL	0.76 + 0.030*SL	0.79 + 0.026*SL
	t_{PHL}	0.95	0.87 + 0.042*SL	0.90 + 0.031*SL	0.98 + 0.023*SL
	t_R	0.34	0.23 + 0.057*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.45	0.36 + 0.044*SL	0.39 + 0.033*SL	0.47 + 0.026*SL
S0 to Y	t_{PLH}	1.19	1.12 + 0.035*SL	1.14 + 0.029*SL	1.17 + 0.026*SL
	t_{PHL}	1.11	1.03 + 0.041*SL	1.06 + 0.031*SL	1.14 + 0.023*SL
	t_R	0.35	0.23 + 0.057*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.44	0.35 + 0.045*SL	0.39 + 0.033*SL	0.46 + 0.026*SL
S1 to Y	t_{PLH}	0.78	0.71 + 0.035*SL	0.72 + 0.030*SL	0.75 + 0.026*SL
	t_{PHL}	0.65	0.57 + 0.042*SL	0.60 + 0.030*SL	0.68 + 0.023*SL
	t_R	0.34	0.23 + 0.055*SL	0.24 + 0.053*SL	0.25 + 0.052*SL
	t_F	0.41	0.32 + 0.046*SL	0.35 + 0.034*SL	0.43 + 0.026*SL
S2 to Y	t_{PLH}	0.55	0.49 + 0.035*SL	0.50 + 0.030*SL	0.53 + 0.027*SL
	t_{PHL}	0.43	0.36 + 0.034*SL	0.38 + 0.026*SL	0.44 + 0.021*SL
	t_R	0.32	0.21 + 0.058*SL	0.22 + 0.054*SL	0.23 + 0.053*SL
	t_F	0.29	0.20 + 0.043*SL	0.23 + 0.034*SL	0.30 + 0.027*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Logic Symbol



Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

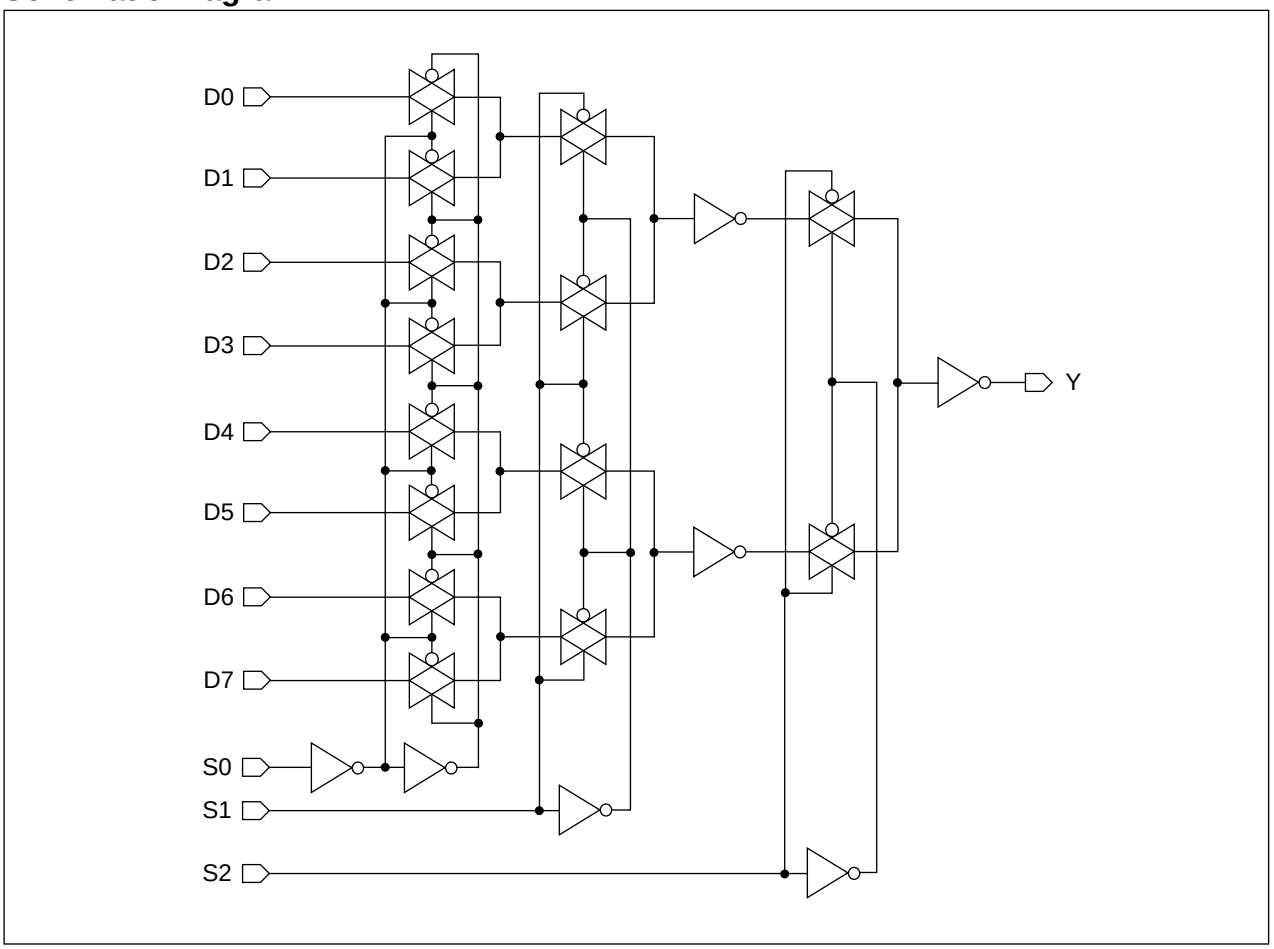
Cell Data

Input Load (SL)											Gate Count
KG80											
YMX8/YMX8D2											*YMX8*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1	0.8	2.0	1.2	11.0
KGM80											
YMX8/YMX8D2											*YMX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4	0.9	2.3	1.5	11.0

YMX8/YMX8D2

Fast 8 > 1 Non-Inverting MUX with 1X/2X Drive

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YMX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.45	0.36 + 0.043*SL	0.37 + 0.041*SL	0.37 + 0.041*SL
	t_{PHL}	0.49	0.42 + 0.038*SL	0.44 + 0.029*SL	0.47 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.13 + 0.041*SL
D1 to Y	t_{PLH}	0.45	0.36 + 0.043*SL	0.37 + 0.041*SL	0.37 + 0.042*SL
	t_{PHL}	0.49	0.42 + 0.037*SL	0.44 + 0.029*SL	0.47 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.13 + 0.041*SL
D2 to Y	t_{PLH}	0.45	0.36 + 0.044*SL	0.37 + 0.041*SL	0.37 + 0.041*SL
	t_{PHL}	0.49	0.42 + 0.037*SL	0.44 + 0.029*SL	0.47 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.11 + 0.087*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.14 + 0.040*SL
D3 to Y	t_{PLH}	0.45	0.37 + 0.043*SL	0.37 + 0.041*SL	0.37 + 0.041*SL
	t_{PHL}	0.49	0.42 + 0.037*SL	0.44 + 0.029*SL	0.46 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.14 + 0.040*SL
D4 to Y	t_{PLH}	0.45	0.36 + 0.043*SL	0.37 + 0.041*SL	0.37 + 0.041*SL
	t_{PHL}	0.50	0.42 + 0.038*SL	0.44 + 0.029*SL	0.47 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.13 + 0.040*SL
D5 to Y	t_{PLH}	0.45	0.36 + 0.044*SL	0.37 + 0.041*SL	0.37 + 0.041*SL
	t_{PHL}	0.50	0.42 + 0.038*SL	0.44 + 0.029*SL	0.47 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.14 + 0.040*SL
D6 to Y	t_{PLH}	0.45	0.36 + 0.043*SL	0.37 + 0.041*SL	0.37 + 0.041*SL
	t_{PHL}	0.49	0.42 + 0.037*SL	0.44 + 0.029*SL	0.47 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.11 + 0.087*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.14 + 0.040*SL
D7 to Y	t_{PLH}	0.45	0.36 + 0.043*SL	0.37 + 0.041*SL	0.37 + 0.041*SL
	t_{PHL}	0.49	0.42 + 0.037*SL	0.44 + 0.029*SL	0.47 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.087*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.14 + 0.040*SL
S0 to Y	t_{PLH}	0.83	0.74 + 0.043*SL	0.74 + 0.041*SL	0.74 + 0.042*SL
	t_{PHL}	0.74	0.67 + 0.038*SL	0.69 + 0.029*SL	0.72 + 0.025*SL
	t_R	0.28	0.11 + 0.084*SL	0.10 + 0.088*SL	0.09 + 0.090*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.13 + 0.041*SL
S1 to Y	t_{PLH}	0.55	0.46 + 0.043*SL	0.47 + 0.041*SL	0.47 + 0.041*SL
	t_{PHL}	0.43	0.36 + 0.037*SL	0.38 + 0.029*SL	0.40 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.21	0.12 + 0.045*SL	0.13 + 0.041*SL	0.13 + 0.041*SL
S2 to Y	t_{PLH}	0.38	0.29 + 0.043*SL	0.29 + 0.041*SL	0.29 + 0.042*SL
	t_{PHL}	0.27	0.20 + 0.035*SL	0.22 + 0.028*SL	0.24 + 0.025*SL
	t_R	0.27	0.10 + 0.087*SL	0.10 + 0.088*SL	0.08 + 0.090*SL
	t_F	0.19	0.10 + 0.045*SL	0.11 + 0.042*SL	0.11 + 0.041*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 YMX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.44	0.40 + 0.023*SL	0.40 + 0.022*SL	0.41 + 0.021*SL
	t_{PHL}	0.49	0.44 + 0.023*SL	0.46 + 0.018*SL	0.48 + 0.015*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
D1 to Y	t_{PLH}	0.44	0.40 + 0.023*SL	0.40 + 0.022*SL	0.41 + 0.021*SL
	t_{PHL}	0.49	0.44 + 0.022*SL	0.45 + 0.018*SL	0.48 + 0.015*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.19	0.14 + 0.024*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
D2 to Y	t_{PLH}	0.45	0.40 + 0.024*SL	0.40 + 0.021*SL	0.41 + 0.021*SL
	t_{PHL}	0.49	0.44 + 0.023*SL	0.45 + 0.018*SL	0.48 + 0.015*SL
	t_R	0.21	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.19	0.14 + 0.024*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
D3 to Y	t_{PLH}	0.45	0.40 + 0.024*SL	0.40 + 0.021*SL	0.41 + 0.021*SL
	t_{PHL}	0.49	0.44 + 0.023*SL	0.45 + 0.018*SL	0.48 + 0.015*SL
	t_R	0.21	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.19	0.14 + 0.024*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
D4 to Y	t_{PLH}	0.44	0.40 + 0.023*SL	0.40 + 0.022*SL	0.41 + 0.021*SL
	t_{PHL}	0.49	0.45 + 0.023*SL	0.46 + 0.018*SL	0.48 + 0.015*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.19	0.13 + 0.025*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
D5 to Y	t_{PLH}	0.44	0.40 + 0.023*SL	0.40 + 0.022*SL	0.41 + 0.021*SL
	t_{PHL}	0.49	0.45 + 0.022*SL	0.46 + 0.018*SL	0.48 + 0.015*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.19	0.14 + 0.024*SL	0.14 + 0.022*SL	0.15 + 0.021*SL
D6 to Y	t_{PLH}	0.44	0.40 + 0.024*SL	0.40 + 0.021*SL	0.41 + 0.021*SL
	t_{PHL}	0.49	0.44 + 0.023*SL	0.45 + 0.018*SL	0.48 + 0.015*SL
	t_R	0.21	0.12 + 0.041*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.19	0.14 + 0.025*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
D7 to Y	t_{PLH}	0.44	0.40 + 0.024*SL	0.40 + 0.021*SL	0.41 + 0.021*SL
	t_{PHL}	0.49	0.44 + 0.023*SL	0.45 + 0.018*SL	0.48 + 0.015*SL
	t_R	0.21	0.12 + 0.041*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.19	0.14 + 0.025*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
S0 to Y	t_{PLH}	0.82	0.77 + 0.024*SL	0.77 + 0.022*SL	0.78 + 0.021*SL
	t_{PHL}	0.74	0.69 + 0.023*SL	0.70 + 0.018*SL	0.73 + 0.015*SL
	t_R	0.20	0.12 + 0.042*SL	0.12 + 0.043*SL	0.11 + 0.044*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
S1 to Y	t_{PLH}	0.54	0.49 + 0.024*SL	0.50 + 0.022*SL	0.50 + 0.021*SL
	t_{PHL}	0.43	0.38 + 0.023*SL	0.39 + 0.018*SL	0.41 + 0.015*SL
	t_R	0.20	0.12 + 0.042*SL	0.11 + 0.044*SL	0.11 + 0.044*SL
	t_F	0.19	0.13 + 0.026*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
S2 to Y	t_{PLH}	0.36	0.31 + 0.024*SL	0.32 + 0.022*SL	0.32 + 0.021*SL
	t_{PHL}	0.26	0.22 + 0.021*SL	0.23 + 0.017*SL	0.25 + 0.015*SL
	t_R	0.20	0.11 + 0.043*SL	0.11 + 0.044*SL	0.10 + 0.045*SL
	t_F	0.17	0.12 + 0.023*SL	0.12 + 0.022*SL	0.13 + 0.021*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

YMX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.69	0.58 + 0.054*SL	0.59 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.72	0.63 + 0.045*SL	0.67 + 0.031*SL	0.73 + 0.025*SL
	t_R	0.36	0.16 + 0.102*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.27	0.16 + 0.050*SL	0.19 + 0.043*SL	0.20 + 0.041*SL
D1 to Y	t_{PLH}	0.69	0.58 + 0.054*SL	0.59 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.72	0.63 + 0.045*SL	0.67 + 0.031*SL	0.73 + 0.025*SL
	t_R	0.36	0.16 + 0.102*SL	0.15 + 0.106*SL	0.13 + 0.108*SL
	t_F	0.27	0.16 + 0.050*SL	0.19 + 0.043*SL	0.20 + 0.041*SL
D2 to Y	t_{PLH}	0.70	0.59 + 0.054*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.72	0.63 + 0.045*SL	0.67 + 0.031*SL	0.73 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.13 + 0.108*SL
	t_F	0.27	0.16 + 0.051*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
D3 to Y	t_{PLH}	0.70	0.59 + 0.054*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.72	0.63 + 0.045*SL	0.67 + 0.031*SL	0.73 + 0.025*SL
	t_R	0.36	0.16 + 0.102*SL	0.15 + 0.106*SL	0.12 + 0.109*SL
	t_F	0.27	0.16 + 0.051*SL	0.19 + 0.043*SL	0.20 + 0.041*SL
D4 to Y	t_{PLH}	0.69	0.58 + 0.054*SL	0.59 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.73	0.64 + 0.045*SL	0.67 + 0.031*SL	0.74 + 0.025*SL
	t_R	0.36	0.16 + 0.102*SL	0.15 + 0.106*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.050*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
D5 to Y	t_{PLH}	0.69	0.58 + 0.054*SL	0.59 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.73	0.64 + 0.045*SL	0.68 + 0.031*SL	0.74 + 0.025*SL
	t_R	0.36	0.16 + 0.102*SL	0.15 + 0.106*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.050*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
D6 to Y	t_{PLH}	0.69	0.59 + 0.054*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.72	0.63 + 0.045*SL	0.67 + 0.031*SL	0.73 + 0.025*SL
	t_R	0.36	0.16 + 0.102*SL	0.15 + 0.106*SL	0.12 + 0.109*SL
	t_F	0.27	0.16 + 0.052*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
D7 to Y	t_{PLH}	0.69	0.59 + 0.054*SL	0.60 + 0.050*SL	0.60 + 0.050*SL
	t_{PHL}	0.72	0.63 + 0.045*SL	0.67 + 0.031*SL	0.73 + 0.025*SL
	t_R	0.36	0.16 + 0.102*SL	0.15 + 0.106*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.050*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
S0 to Y	t_{PLH}	1.18	1.07 + 0.054*SL	1.08 + 0.050*SL	1.09 + 0.050*SL
	t_{PHL}	1.09	0.99 + 0.046*SL	1.03 + 0.031*SL	1.10 + 0.025*SL
	t_R	0.36	0.16 + 0.103*SL	0.15 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.051*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
S1 to Y	t_{PLH}	0.77	0.66 + 0.054*SL	0.67 + 0.050*SL	0.67 + 0.050*SL
	t_{PHL}	0.63	0.54 + 0.045*SL	0.58 + 0.031*SL	0.64 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.27	0.17 + 0.051*SL	0.19 + 0.042*SL	0.20 + 0.041*SL
S2 to Y	t_{PLH}	0.49	0.39 + 0.054*SL	0.40 + 0.050*SL	0.40 + 0.050*SL
	t_{PHL}	0.39	0.31 + 0.042*SL	0.34 + 0.030*SL	0.39 + 0.025*SL
	t_R	0.35	0.15 + 0.104*SL	0.14 + 0.107*SL	0.12 + 0.109*SL
	t_F	0.24	0.14 + 0.052*SL	0.16 + 0.043*SL	0.18 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 YMX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.68	0.62 + 0.030*SL	0.63 + 0.026*SL	0.65 + 0.025*SL
	t_{PHL}	0.72	0.67 + 0.029*SL	0.69 + 0.020*SL	0.74 + 0.015*SL
	t_R	0.27	0.17 + 0.051*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D1 to Y	t_{PLH}	0.68	0.62 + 0.030*SL	0.63 + 0.026*SL	0.65 + 0.025*SL
	t_{PHL}	0.72	0.67 + 0.029*SL	0.69 + 0.020*SL	0.74 + 0.015*SL
	t_R	0.27	0.16 + 0.053*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D2 to Y	t_{PLH}	0.69	0.63 + 0.030*SL	0.64 + 0.026*SL	0.65 + 0.025*SL
	t_{PHL}	0.72	0.66 + 0.028*SL	0.69 + 0.020*SL	0.74 + 0.015*SL
	t_R	0.27	0.16 + 0.053*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D3 to Y	t_{PLH}	0.69	0.63 + 0.030*SL	0.64 + 0.026*SL	0.65 + 0.025*SL
	t_{PHL}	0.72	0.66 + 0.028*SL	0.69 + 0.020*SL	0.74 + 0.015*SL
	t_R	0.27	0.16 + 0.052*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D4 to Y	t_{PLH}	0.68	0.62 + 0.030*SL	0.63 + 0.026*SL	0.64 + 0.025*SL
	t_{PHL}	0.73	0.67 + 0.029*SL	0.69 + 0.020*SL	0.74 + 0.015*SL
	t_R	0.27	0.17 + 0.051*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D5 to Y	t_{PLH}	0.68	0.62 + 0.030*SL	0.63 + 0.026*SL	0.64 + 0.025*SL
	t_{PHL}	0.73	0.67 + 0.029*SL	0.69 + 0.020*SL	0.75 + 0.015*SL
	t_R	0.27	0.17 + 0.051*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D6 to Y	t_{PLH}	0.69	0.63 + 0.030*SL	0.64 + 0.026*SL	0.65 + 0.025*SL
	t_{PHL}	0.72	0.67 + 0.029*SL	0.69 + 0.020*SL	0.74 + 0.015*SL
	t_R	0.27	0.16 + 0.052*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
D7 to Y	t_{PLH}	0.69	0.62 + 0.030*SL	0.64 + 0.026*SL	0.65 + 0.025*SL
	t_{PHL}	0.73	0.67 + 0.028*SL	0.69 + 0.020*SL	0.74 + 0.015*SL
	t_R	0.27	0.16 + 0.052*SL	0.17 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
S0 to Y	t_{PLH}	1.17	1.11 + 0.030*SL	1.12 + 0.026*SL	1.13 + 0.025*SL
	t_{PHL}	1.09	1.03 + 0.029*SL	1.05 + 0.020*SL	1.10 + 0.015*SL
	t_R	0.27	0.16 + 0.052*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
S1 to Y	t_{PLH}	0.75	0.69 + 0.030*SL	0.71 + 0.026*SL	0.72 + 0.025*SL
	t_{PHL}	0.63	0.58 + 0.028*SL	0.60 + 0.020*SL	0.65 + 0.015*SL
	t_R	0.26	0.16 + 0.053*SL	0.16 + 0.052*SL	0.15 + 0.053*SL
	t_F	0.24	0.18 + 0.030*SL	0.20 + 0.024*SL	0.23 + 0.021*SL
S2 to Y	t_{PLH}	0.48	0.42 + 0.030*SL	0.43 + 0.026*SL	0.44 + 0.025*SL
	t_{PHL}	0.39	0.33 + 0.027*SL	0.35 + 0.020*SL	0.40 + 0.015*SL
	t_R	0.26	0.15 + 0.053*SL	0.15 + 0.052*SL	0.14 + 0.053*SL
	t_F	0.22	0.16 + 0.030*SL	0.17 + 0.024*SL	0.21 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Input/Output Cells 4

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OVERVIEW

The fourth chapter describes various kinds of Input/Output cells (5V/3.3V, normal and interface operations) in KG80/KGM80 libraries.

The switching characteristics of each cell are attached to its basic cell information. The AC characteristics of bi-directional buffers are not included in this data sheet, however, they can be derived from different combinations of input and output buffers.

There are so many possible combinations of input/output cells, therefore, the naming conventions are adopted to help you memorize and use this cell library efficiently. You can refer to the naming conventions contained in “Summary Tables” section.

The “Summary Tables” section shows the list of 5V and 3.3V I/O cells separated by the category (input, output, bi-directional, etc.), and the more detailed description tables can be found on the leading part of each category.

SUMMARY TABLES

Input Buffers

Cell Type	Cell Name	KG80	KGM80	Page
CMOS Level	PIC/PICD/PICU	o	o	4-9
	PHIC/PHICD/PHICU	–	o	
	PLIC/PLICD/PLICU	o	–	
TTL Schmitt Trigger Level	PIL/PILD/PILU	o	–	4-13
	PHIL/PHILD/PHILU	–	o	
CMOS Schmitt Trigger Level	PIS/PISD/PISU	o	o	4-16
	PHIS/PHISD/PHISU	–	o	
	PLIS/PLISD/PLISU	o	–	
TTL Level	PIT/PITD/PITU	o	–	4-20
	PHIT/PHITD/PHITU	–	o	

<Naming Convention of Input Buffers>

P v l a b			
v		**a**	
None	Normal operation	C	CMOS level
H	5V interface in KGM80	L	TTL Schmitt trigger level
L	3.3V interface in KG80	S	CMOS Schmitt trigger level
b		T	TTL level
None	No resistor		
D	Pull-down resistor		
U	Pull-up resistor		

Output Buffers

Cell Type	Cell Name	Current Drive (mA)		Page
		KG80	KGM80	
Normal	POBy	1/2/4/8/12/16/20/24	1/2/4/6/8/10/12/16	4-24
	POBySH	12/16/20/24	–	
	POBySM	4/8/12/16/20/24	4/6/8/10/12/16	
	PHOBy	–	1/2/4/8/12/16/20/24	
	PHOBySH	–	12/16/20/24	
	PHOBySM	–	4/8/12/16/20/24	
	PLOBy	1/2/4/6/8/10/12/16	–	
	PLOBySM	4/6/8/10/12/16	–	

Cell Type	Cell Name	Current Drive (mA)		Page
		KG80	KGM80	
Open Drain	PODy	1/2/4/8/12/16/20/24	1/2/4/6/8/10/12/16	4-41
	PODySH	12/16/20/24	–	
	PODySM	4/8/12/16/20/24	4/6/8/10/12/16	
	PHODy	–	1/2/4/8/12/16/20/24	
	PHODySH	–	12/16/20/24	
	PHODySM	–	4/8/12/16/20/24	
	PLODy	1/2/4/6/8/10/12/16	–	
	PLODySM	4/6/8/10/12/16	–	
Tri-State	POTy	1/2/4/8/12/16/20/24	1/2/4/6/8/10/12/16	4-64
	POTySH	12/16/20/24	–	
	POTySM	4/8/12/16/20/24	4/6/8/10/12/16	
	PHOTy	–	1/2/4/8/12/16/20/24	
	PHOTySH	–	12/16/20/24	
	PHOTySM	–	4/8/12/16/20/24	
	PLOTy	1/2/4/6/8/10/12/16	–	
	PLOTySM	4/6/8/10/12/16	–	

<Naming Convention of Output Buffers>

P v O x y z			
v		**y**	
None	Normal operation	1	1mA drive
H	5V interface in KGM80	2	2mA drive
L	3.3V interface in KG80	4	4mA drive
x		6	6mA drive
B	Normal buffer	8	8mA drive
D	Open drain buffer	10	10mA drive
T	Tri-state buffer	12	12mA drive
z		16	16mA drive
None	No slew-rate control	20	20mA drive
SH	High slew-rate control	24	24mA drive
SM	Medium slew-rate control		

Bi-Directional Buffers

Cell Type	Cell Name	KG80	KGM80	Page
Open Drain	PBaDyz/PBaUDyz	o	o	4-98
	PHBaDyz/PHBaUDyz	–	o	
	PLBaDyz/PLBaUDyz	o	–	
Tri-State	PBaTyz/PBaDTyz/PBaUTyz	o	o	
	PHBaTyz/PHBaDTyz/PHBaUTyz	–	o	
	PLBaTyz/PLBaDTyz/PLBaUTyz	o	–	

<Naming Convention of Bi-Directional Buffers>

P v B a b x y z			
v		**a**	
None	Normal operation	C	CMOS level
H	5V interface in KGM80	L	TTL Schmitt trigger level
L	3.3V interface in KG80	S	CMOS Schmitt trigger level
b		T	TTL level
None	No resistor	**y**	
D	Pull-down resistor	1	1mA drive
U	Pull-up resistor	2	2mA drive
x		4	4mA drive
D	Open drain buffer	6	6mA drive
T	Tri-state buffer	8	8mA drive
z		10	10mA drive
None	No slew-rate control	12	12mA drive
SH	High slew-rate control	16	16mA drive
SM	Medium slew-rate control	20	20mA drive
		24	24mA drive

Input Clock Drivers

Cell Type	Cell Name	Current Drive (mA)		Page
		KG80	KGM80	
CMOS Level	PSCKDCy	2/4/8/12	2/4/6/8	4-100
	PSCKDCDy	2/4/8/12	2/4/6/8	
	PSCKDCUy	2/4/8/12	2/4/6/8	
TTL Schmitt Trigger Level	PSCKDLy	2/4/8/12	–	4-107
	PSCKDLDy	2/4/8/12	–	
	PSCKDLUy	2/4/8/12	–	
CMOS Schmitt Trigger Level	PSCKDSy	2/4/8/12	2/4/6/8	4-111
	PSCKDSDy	2/4/8/12	2/4/6/8	
	PSCKDSUy	2/4/8/12	2/4/6/8	
TTL Level	PSCKDTy	2/4/8/12	–	4-118
	PSCKDTDy	2/4/8/12	–	
	PSCKDTUy	2/4/8/12	–	

<Naming Convention of Input Clock Drivers>

PSCKD a b y			
a		**y**	
C	CMOS level	2	2mA drive
L	TTL Schmitt trigger level	4	4mA drive
S	CMOS Schmitt trigger level	6	6mA drive
T	TTL level	8	8mA drive
b		12	12mA drive
None	No resistor		
D	Pull-down resistor		
U	Pull-up resistor		

Oscillators

Cell Type	Cell Name		Page
	KG80	KGM80	
Oscillator with Enable	PSOSCM(1/2/3/4/5/6)	PSOSCM(1/2/3/4/5)	4-122

PCI Buffers

Cell Type	Cell Name		Page
	KG80	KGM80	
PCI Input	PSIPCIA/PLSIPCIA	PSIPCIA3/PHSIPCIA	4-132
PCI Output	PSOPCIA/PLSOPCIA	PSOPCIA3/PHSOPCIA	4-133
Universal PCI Input	PSIPCIAU	PSIPCIAU	4-134
Universal PCI Output	PSOPCIAU	PSOPCIAU	4-135

PCMCIA Buffers

Cell Type	Cell Name	Page
PCMCIA Input	PVIC(5/3)	4-139
	PVIL/PVILD/PVILU(5/3)	
	PVIT/PVITD/PITU(5/3)	
PCMCIA Output	PVOB4/PVOB8/PVOB12(5/3)	4-140
	PVOD4/PVOD8/PVOD12(5/3)	
	PVOT4/PVOT8/PVOT12(5/3)	4-141
	PVOT8SM/PVOT12SM(5/3)	
PCMCIA Bi-Directional	PVBTT4/PVBTT8/PVBTT12(5/3)	4-142
	PVBTDT8SM/PVBCT8SM(5/3)	

CardBus I/O Buffers

Cell Type	Cell Name		Page
	KG80	KGM80	
CardBus Input	PLITCBU	PITCBU	4-146
CardBus Output	PLOTCBU/ PLOTCCKCBU/ PLOTCVSCBU	POTCBU/ POTCCKCBU/ POTCVSCBU	4-147
	PLODCCKCBU	PODCCKCBU	4-148
CardBus Bi-Directional	PLBTTCBU/ PLBTCCKCBU/ PLBTCVSCBU	PBTTCBU/ PBTCCKCBU/ PBTCVSCBU	4-149
	PLBDCCKCBU	PBDCCKCBU	4-150
Level Shifter	PLSCB	PLSCB	4-151

Voltage Detector (Under development)

Cell Type	Cell Name	Page
Voltage Detector	VDET	4-152

Power Pads

Cell Type	Cell Name		Page
	KG80	KGM80	
5V VDD	VDD5(I/P/O/IP/OI/OP/T)	VDD5(P/O/OP)	4-153
3.3V VDD	VDD3(P/O/OP)	VDD3(I/P/O/IP/OI/OP/T)	
5V VSS	VSS5(I/P/O/IP/OI/OP/T)	VSS5(P/O/OP)	
3.3V VSS	VSS3(P/O/OP)	VSS3(I/P/O/IP/OI/OP/T)	

INPUT BUFFERS

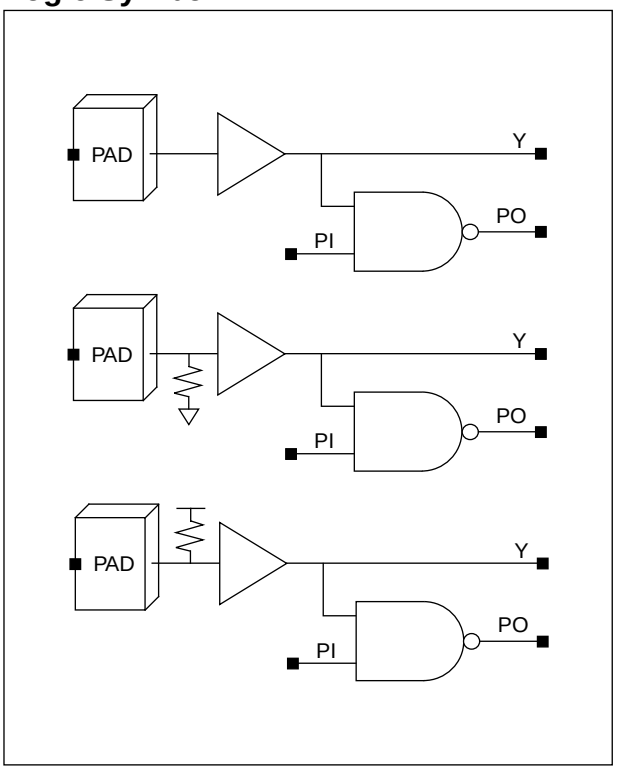
Cell List

Cell Name	Function Description
KG80	
PIC/PICD/PICU	5V CMOS Level Input Buffers
PIL/PILD/PILU	5V TTL Schmitt Trigger Level Input Buffers
PIS/PISD/PISU	5V CMOS Schmitt Trigger Level Input Buffers
PIT/PITD/PITU	5V TTL Level Input Buffers
PLIC/PLICD/PLICU	3.3V Interface CMOS Level Input Buffers
PLIS/PLISD/PLISU	3.3V Interface CMOS Schmitt Trigger Level Input Buffers
KGM80	
PIC/PICD/PICU	3.3V CMOS Level Input Buffers
PIS/PISD/PISU	3.3V CMOS Schmitt Trigger Level Input Buffers
PHIC/PHICD/PHICU	5V Interface CMOS Level Input Buffers
PHIL/PHILD/PHILU	5V Interface TTL Schmitt Trigger Level Input Buffers
PHIS/PHISD/PHISU	5V Interface CMOS Schmitt Trigger Level Input Buffers
PHIT/PHITD/PHITU	5V Interface TTL Level Input Buffers

Cell Availability

Library	5V Operation	3.3V Operation
KG80	PIC/PICD/PICU	PLIC/PLICD/PLICU
KGM80	PHIC/PHICD/PHICU	PIC/PICD/PICU

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

KG80	
	PI
PIC/PICD/PICU	1.6
PLIC/PLICD/PLICU	1.2
KGM80	
	PI
PIC/PICD/PICU	1.9
PHIC/PHICD/PHICU	1.4

I/O Slot

KG80/KGM80	
PvIC/PvICD/PvICU	1.0

NOTES:

1. KG80 3.3V interface input buffers (PLIC/PLICD/PLICU) are not available to receive input signals from 5V devices.
2. Fail-safe input buffers are available to receive signals from 5V devices without reducing reliability. However, if you want to use fail-safe input buffers, please contact to SEC ASIC first.

KG80 PIC Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.23	0.21 + 0.009*SL	0.22 + 0.008*SL	0.22 + 0.008*SL
	t_{PHL}	0.24	0.21 + 0.011*SL	0.21 + 0.010*SL	0.22 + 0.010*SL
	t_R	0.13	0.10 + 0.014*SL	0.10 + 0.014*SL	0.09 + 0.015*SL
	t_F	0.13	0.10 + 0.016*SL	0.10 + 0.018*SL	0.09 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PICD Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.24	0.23 + 0.008*SL	0.23 + 0.008*SL	0.23 + 0.008*SL
	t_{PHL}	0.24	0.22 + 0.011*SL	0.22 + 0.011*SL	0.22 + 0.010*SL
	t_R	0.13	0.10 + 0.013*SL	0.10 + 0.015*SL	0.09 + 0.016*SL
	t_F	0.13	0.10 + 0.015*SL	0.10 + 0.018*SL	0.09 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PICU Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.23	0.21 + 0.010*SL	0.22 + 0.008*SL	0.22 + 0.007*SL
	t_{PHL}	0.24	0.22 + 0.012*SL	0.22 + 0.010*SL	0.22 + 0.010*SL
	t_R	0.13	0.11 + 0.014*SL	0.11 + 0.014*SL	0.10 + 0.015*SL
	t_F	0.13	0.10 + 0.018*SL	0.10 + 0.017*SL	0.09 + 0.018*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PLIC Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.49	0.47 + 0.009*SL	0.48 + 0.007*SL	0.48 + 0.007*SL
	t_{PHL}	0.78	0.76 + 0.010*SL	0.76 + 0.012*SL	0.80 + 0.005*SL
	t_R	0.15	0.13 + 0.011*SL	0.12 + 0.012*SL	0.12 + 0.013*SL
	t_F	0.16	0.13 + 0.012*SL	0.13 + 0.014*SL	0.15 + 0.011*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PLICD Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.48	0.47 + 0.008*SL	0.47 + 0.007*SL	0.47 + 0.007*SL
	t_{PHL}	0.79	0.77 + 0.011*SL	0.76 + 0.012*SL	0.81 + 0.006*SL
	t_R	0.15	0.12 + 0.012*SL	0.12 + 0.012*SL	0.12 + 0.013*SL
	t_F	0.17	0.15 + 0.012*SL	0.15 + 0.012*SL	0.16 + 0.010*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

KG80 PLICU Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.49	0.48 + 0.008*SL	0.48 + 0.008*SL	0.49 + 0.006*SL
	t_{PHL}	0.78	0.76 + 0.011*SL	0.77 + 0.007*SL	0.74 + 0.011*SL
	t_R	0.15	0.12 + 0.013*SL	0.13 + 0.011*SL	0.11 + 0.014*SL
	t_F	0.17	0.15 + 0.012*SL	0.14 + 0.016*SL	0.19 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

KGM80 PIC Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.27	0.25 + 0.011*SL	0.25 + 0.009*SL	0.26 + 0.009*SL
	t_{PHL}	0.28	0.26 + 0.012*SL	0.26 + 0.010*SL	0.27 + 0.010*SL
	t_R	0.17	0.14 + 0.016*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
	t_F	0.16	0.12 + 0.019*SL	0.11 + 0.023*SL	0.19 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

KGM80 PICD Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.26	0.24 + 0.007*SL	0.23 + 0.011*SL	0.26 + 0.009*SL
	t_{PHL}	0.29	0.26 + 0.013*SL	0.27 + 0.011*SL	0.27 + 0.010*SL
	t_R	0.18	0.14 + 0.019*SL	0.15 + 0.016*SL	0.11 + 0.020*SL
	t_F	0.17	0.13 + 0.020*SL	0.13 + 0.018*SL	0.11 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

KGM80 PICU Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.28	0.25 + 0.011*SL	0.26 + 0.009*SL	0.26 + 0.009*SL
	t_{PHL}	0.29	0.27 + 0.009*SL	0.26 + 0.011*SL	0.27 + 0.010*SL
	t_R	0.17	0.14 + 0.016*SL	0.13 + 0.018*SL	0.11 + 0.019*SL
	t_F	0.17	0.12 + 0.022*SL	0.13 + 0.021*SL	0.19 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHIC Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.43	0.42 + 0.010*SL	0.42 + 0.009*SL	0.43 + 0.008*SL
	t_{PHL}	0.63	0.63 + 0.003*SL	0.60 + 0.012*SL	0.64 + 0.008*SL
	t_R	0.16	0.11 + 0.022*SL	0.13 + 0.017*SL	0.13 + 0.017*SL
	t_F	0.20	0.17 + 0.012*SL	0.17 + 0.014*SL	0.18 + 0.012*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHICD Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.44	0.43 + 0.005*SL	0.42 + 0.009*SL	0.44 + 0.007*SL
	t_{PHL}	0.64	0.63 + 0.004*SL	0.61 + 0.012*SL	0.64 + 0.009*SL
	t_R	0.15	0.13 + 0.013*SL	0.12 + 0.017*SL	0.12 + 0.017*SL
	t_F	0.20	0.17 + 0.014*SL	0.17 + 0.014*SL	0.17 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHICU Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

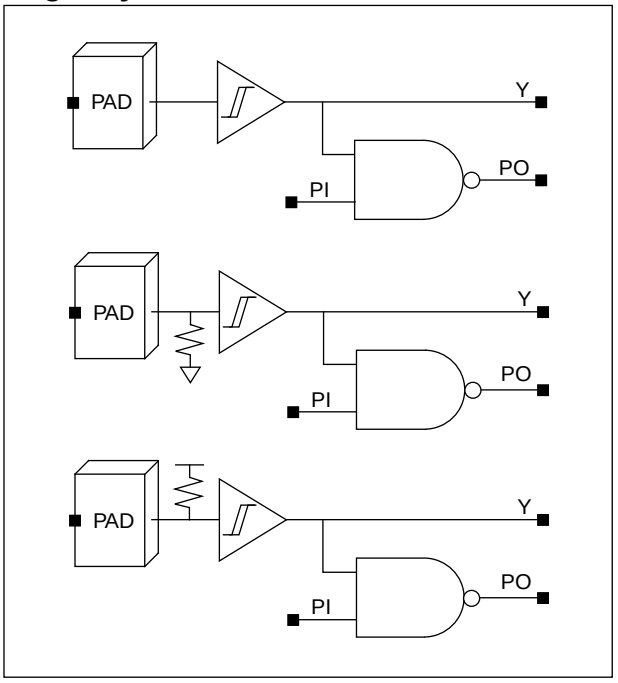
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.44	0.42 + 0.009*SL	0.42 + 0.009*SL	0.43 + 0.008*SL
	t_{PHL}	0.64	0.63 + 0.002*SL	0.61 + 0.013*SL	0.65 + 0.008*SL
	t_R	0.15	0.12 + 0.016*SL	0.11 + 0.019*SL	0.15 + 0.015*SL
	t_F	0.20	0.16 + 0.018*SL	0.18 + 0.013*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Cell Availability

Library	5V Operation	3.3V Operation
KG80	PIL/PILD/PILU	–
KGM80	PHIL/PHILD/PHILU	–

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

KG80	
	PI
PIL/PILD/PILU	1.6
KGM80	
	PI
PHIL/PHILD/PHILU	1.4

I/O Slot

KG80/KGM80	
PvIL/PvILD/PvILU	1.0

KG80 PIL Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.44	0.43 + 0.009*SL	0.43 + 0.008*SL	0.43 + 0.008*SL
	t_{PHL}	1.52	1.49 + 0.014*SL	1.49 + 0.013*SL	1.51 + 0.011*SL
	t_R	0.16	0.14 + 0.014*SL	0.13 + 0.015*SL	0.13 + 0.015*SL
	t_F	0.52	0.49 + 0.013*SL	0.50 + 0.011*SL	0.51 + 0.010*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PILD Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.46	0.44 + 0.009*SL	0.44 + 0.008*SL	0.44 + 0.008*SL
	t_{PHL}	1.53	1.50 + 0.014*SL	1.51 + 0.013*SL	1.52 + 0.011*SL
	t_R	0.17	0.14 + 0.014*SL	0.14 + 0.015*SL	0.14 + 0.015*SL
	t_F	0.52	0.50 + 0.012*SL	0.50 + 0.012*SL	0.51 + 0.010*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PILU Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.45	0.43 + 0.009*SL	0.43 + 0.008*SL	0.44 + 0.008*SL
	t_{PHL}	1.55	1.52 + 0.014*SL	1.53 + 0.013*SL	1.54 + 0.011*SL
	t_R	0.17	0.14 + 0.015*SL	0.14 + 0.014*SL	0.14 + 0.015*SL
	t_F	0.52	0.50 + 0.013*SL	0.50 + 0.012*SL	0.51 + 0.010*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KGM80 PHIL Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.53	0.51 + 0.009*SL	0.51 + 0.009*SL	0.51 + 0.008*SL
	t_{PHL}	2.21	2.19 + 0.010*SL	2.19 + 0.010*SL	2.21 + 0.008*SL
	t_R	0.15	0.12 + 0.016*SL	0.12 + 0.017*SL	0.11 + 0.017*SL
	t_F	0.20	0.15 + 0.024*SL	0.19 + 0.012*SL	0.11 + 0.019*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHILD Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.54	0.52 + 0.009*SL	0.52 + 0.008*SL	0.53 + 0.008*SL
	t_{PHL}	2.22	2.20 + 0.013*SL	2.21 + 0.010*SL	2.22 + 0.008*SL
	t_R	0.15	0.12 + 0.017*SL	0.12 + 0.016*SL	0.10 + 0.019*SL
	t_F	0.20	0.16 + 0.020*SL	0.18 + 0.012*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHILU Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.53	0.51 + 0.009*SL	0.51 + 0.008*SL	0.52 + 0.008*SL
	t_{PHL}	2.24	2.22 + 0.013*SL	2.22 + 0.010*SL	2.24 + 0.009*SL
	t_R	0.15	0.12 + 0.017*SL	0.12 + 0.017*SL	0.10 + 0.018*SL
	t_F	0.22	0.19 + 0.016*SL	0.20 + 0.010*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

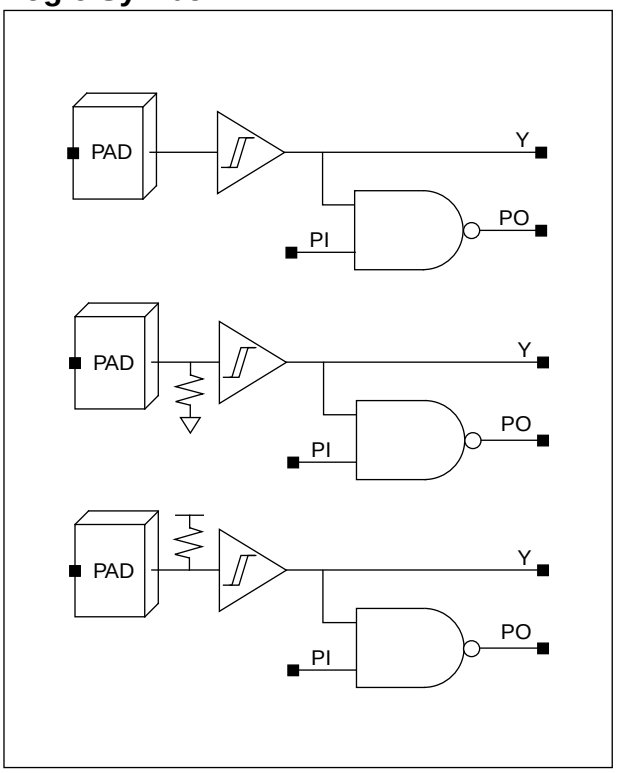
PvIS/PvISD/PvISU

CMOS Schmitt Trigger Level Input Buffers

Cell Availability

Library	5V Operation	3.3V Operation
KG80	PIS/PISD/PISU	PLIS/PLISD/PLISU
KGM80	PHIS/PHISD/PHISU	PIS/PISD/PISU

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

KG80	
	PI
PIS/PISD/PISU	1.6
PLIS/PLISD/PLISU	1.2
KGM80	
	PI
PIS/PISD/PISU	1.9
PHIS/PHISD/PHISU	1.2

I/O Slot

KG80/KGM80	
PvIS/PvISD/PvISU	1.0

NOTES:

1. KG80 3.3V interface input buffers (PLIS/PLISD/PLISU) are not available to receive input signals from 5V devices.
2. Fail-safe input buffers are available to receive signals from 5V devices without reducing reliability. However, if you want to use fail-safe input buffers, please contact to SEC ASIC first.

KG80 PIS Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.28	0.26 + 0.013*SL	0.26 + 0.011*SL	0.26 + 0.011*SL
	t_{PHL}	0.43	0.40 + 0.015*SL	0.40 + 0.013*SL	0.41 + 0.012*SL
	t_R	0.16	0.12 + 0.023*SL	0.12 + 0.022*SL	0.11 + 0.023*SL
	t_F	0.20	0.17 + 0.018*SL	0.17 + 0.017*SL	0.17 + 0.017*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PISD Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.29	0.27 + 0.012*SL	0.27 + 0.012*SL	0.27 + 0.011*SL
	t_{PHL}	0.44	0.41 + 0.015*SL	0.41 + 0.013*SL	0.42 + 0.012*SL
	t_R	0.16	0.12 + 0.020*SL	0.11 + 0.023*SL	0.12 + 0.023*SL
	t_F	0.20	0.17 + 0.018*SL	0.17 + 0.017*SL	0.16 + 0.017*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PISU Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.29	0.26 + 0.013*SL	0.27 + 0.012*SL	0.27 + 0.011*SL
	t_{PHL}	0.44	0.40 + 0.015*SL	0.41 + 0.013*SL	0.42 + 0.012*SL
	t_R	0.16	0.12 + 0.023*SL	0.12 + 0.022*SL	0.11 + 0.023*SL
	t_F	0.20	0.17 + 0.018*SL	0.17 + 0.017*SL	0.17 + 0.017*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PLIS Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.73 + 0.008*SL	0.73 + 0.008*SL	0.74 + 0.006*SL
	t_{PHL}	1.63	1.61 + 0.010*SL	1.61 + 0.011*SL	1.65 + 0.006*SL
	t_R	0.15	0.13 + 0.013*SL	0.13 + 0.011*SL	0.11 + 0.014*SL
	t_F	0.17	0.12 + 0.023*SL	0.15 + 0.013*SL	0.18 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PLISD Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.77	0.75 + 0.008*SL	0.75 + 0.007*SL	0.76 + 0.007*SL
	t_{PHL}	1.65	1.63 + 0.011*SL	1.63 + 0.011*SL	1.66 + 0.007*SL
	t_R	0.15	0.13 + 0.012*SL	0.13 + 0.011*SL	0.11 + 0.013*SL
	t_F	0.17	0.15 + 0.014*SL	0.15 + 0.010*SL	0.15 + 0.011*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

KG80 PLISU Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.76	0.75 + 0.008*SL	0.75 + 0.007*SL	0.75 + 0.007*SL
	t_{PHL}	1.64	1.62 + 0.010*SL	1.62 + 0.012*SL	1.66 + 0.006*SL
	t_R	0.15	0.13 + 0.011*SL	0.13 + 0.012*SL	0.13 + 0.012*SL
	t_F	0.16	0.14 + 0.011*SL	0.13 + 0.013*SL	0.13 + 0.013*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

KGM80 PIS Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.51	0.50 + 0.009*SL	0.50 + 0.008*SL	0.51 + 0.007*SL
	t_{PHL}	1.11	1.09 + 0.012*SL	1.09 + 0.009*SL	1.11 + 0.008*SL
	t_R	0.25	0.22 + 0.018*SL	0.24 + 0.008*SL	0.20 + 0.012*SL
	t_F	0.34	0.32 + 0.010*SL	0.32 + 0.010*SL	0.32 + 0.010*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

KGM80 PISD Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.53	0.52 + 0.008*SL	0.52 + 0.008*SL	0.53 + 0.007*SL
	t_{PHL}	1.13	1.11 + 0.010*SL	1.11 + 0.010*SL	1.13 + 0.008*SL
	t_R	0.24	0.20 + 0.017*SL	0.22 + 0.011*SL	0.22 + 0.011*SL
	t_F	0.34	0.32 + 0.012*SL	0.32 + 0.010*SL	0.33 + 0.009*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

KGM80 PISU Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.53	0.51 + 0.009*SL	0.52 + 0.008*SL	0.53 + 0.007*SL
	t_{PHL}	1.12	1.10 + 0.011*SL	1.10 + 0.009*SL	1.12 + 0.008*SL
	t_R	0.23	0.22 + 0.008*SL	0.21 + 0.011*SL	0.21 + 0.011*SL
	t_F	0.36	0.34 + 0.010*SL	0.34 + 0.008*SL	0.33 + 0.010*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHIS Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.55	0.53 + 0.009*SL	0.53 + 0.009*SL	0.54 + 0.008*SL
	t_{PHL}	1.07	1.06 + 0.005*SL	1.04 + 0.011*SL	1.07 + 0.009*SL
	t_R	0.16	0.11 + 0.022*SL	0.13 + 0.016*SL	0.13 + 0.016*SL
	t_F	0.19	0.17 + 0.014*SL	0.17 + 0.014*SL	0.17 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHISD Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.55	0.53 + 0.009*SL	0.53 + 0.009*SL	0.53 + 0.008*SL
	t_{PHL}	1.08	1.06 + 0.009*SL	1.06 + 0.011*SL	1.08 + 0.009*SL
	t_R	0.15	0.12 + 0.014*SL	0.12 + 0.017*SL	0.09 + 0.019*SL
	t_F	0.19	0.17 + 0.015*SL	0.17 + 0.013*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHISU Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.56	0.54 + 0.009*SL	0.54 + 0.009*SL	0.54 + 0.008*SL
	t_{PHL}	1.08	1.06 + 0.009*SL	1.05 + 0.011*SL	1.08 + 0.009*SL
	t_R	0.16	0.11 + 0.023*SL	0.13 + 0.015*SL	0.09 + 0.019*SL
	t_F	0.20	0.17 + 0.013*SL	0.17 + 0.013*SL	0.16 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

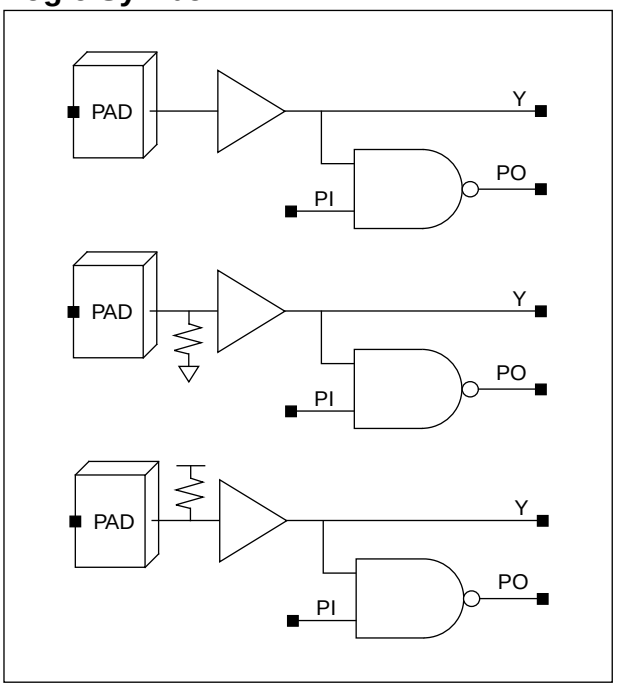
PvIT/PvITD/PvITU

TTL Level Input Buffers

Cell Availability

Library	5V Operation	3.3V Operation
KG80	PIT/PITD/PITU	–
KGM80	PHIT/PHITD/PHITU	–

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

KG80	
	PI
PIT/PITD/PITU	1.6
KGM80	
	PI
PHIT/PHITD/PHITU	1.4

I/O Slot

KG80/KGM80	
PvIT/PvITD/PvITU	1.0

KG80 PIT Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.25	0.23 + 0.011*SL	0.23 + 0.011*SL	0.23 + 0.011*SL
	t_{PHL}	0.32	0.30 + 0.011*SL	0.31 + 0.009*SL	0.32 + 0.008*SL
	t_R	0.15	0.11 + 0.023*SL	0.11 + 0.023*SL	0.10 + 0.024*SL
	t_F	0.17	0.15 + 0.010*SL	0.15 + 0.010*SL	0.15 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PITD Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.26	0.24 + 0.011*SL	0.24 + 0.011*SL	0.24 + 0.011*SL
	t_{PHL}	0.34	0.31 + 0.011*SL	0.32 + 0.009*SL	0.33 + 0.008*SL
	t_R	0.15	0.11 + 0.023*SL	0.11 + 0.023*SL	0.10 + 0.024*SL
	t_F	0.17	0.15 + 0.010*SL	0.15 + 0.010*SL	0.15 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PITU Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.25	0.23 + 0.011*SL	0.23 + 0.011*SL	0.23 + 0.011*SL
	t_{PHL}	0.33	0.31 + 0.011*SL	0.31 + 0.009*SL	0.32 + 0.007*SL
	t_R	0.15	0.11 + 0.024*SL	0.11 + 0.023*SL	0.10 + 0.024*SL
	t_F	0.17	0.15 + 0.009*SL	0.15 + 0.010*SL	0.15 + 0.009*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KGM80 PHIT Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.25	0.23 + 0.009*SL	0.23 + 0.009*SL	0.23 + 0.008*SL
	t_{PHL}	0.93	0.91 + 0.007*SL	0.90 + 0.011*SL	0.93 + 0.008*SL
	t_R	0.17	0.16 + 0.004*SL	0.12 + 0.016*SL	0.11 + 0.017*SL
	t_F	0.20	0.17 + 0.012*SL	0.17 + 0.014*SL	0.15 + 0.016*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHITD Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.27	0.26 + 0.009*SL	0.26 + 0.009*SL	0.26 + 0.008*SL
	t_{PHL}	0.93	0.92 + 0.006*SL	0.91 + 0.011*SL	0.94 + 0.009*SL
	t_R	0.16	0.13 + 0.014*SL	0.12 + 0.016*SL	0.11 + 0.017*SL
	t_F	0.20	0.17 + 0.017*SL	0.17 + 0.014*SL	0.17 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

KGM80 PHITU Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.25	0.23 + 0.009*SL	0.23 + 0.009*SL	0.23 + 0.008*SL
	t_{PHL}	0.93	0.92 + 0.008*SL	0.91 + 0.011*SL	0.94 + 0.008*SL
	t_R	0.17	0.16 + 0.004*SL	0.12 + 0.016*SL	0.11 + 0.018*SL
	t_F	0.20	0.17 + 0.013*SL	0.17 + 0.013*SL	0.15 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

Cell List

Cell Name	Function Description
KG80	
POB(1/2/4/8/12/16/20/24)	5V Normal Output Buffers
POB(12/16/20/24)SH	5V Normal Output Buffers with High Slew-Rate
POB(4/8/12/16/20/24)SM	5V Normal Output Buffers with Medium Slew-Rate
POD(1/2/4/8/12/16/20/24)	5V Open Drain Output Buffers
POD(12/16/20/24)SH	5V Open Drain Output Buffers with High Slew-Rate
POD(4/8/12/16/20/24)SM	5V Open Drain Output Buffers with Medium Slew-Rate
POT(1/2/4/8/12/16/20/24)	5V Tri-State Output Buffers
POT(12/16/20/24)SH	5V Tri-State Output Buffers with High Slew-Rate
POT(4/8/12/16/20/24)SM	5V Tri-State Output Buffers with Medium Slew-Rate
PLOB(1/2/4/6/8/10/12/16)	3.3V Interface Normal Output Buffers
PLOB(4/6/8/10/12/16)SM	3.3V Interface Normal Output Buffers with Medium Slew-Rate
PLOD(1/2/4/6/8/10/12/16)	3.3V Interface Open Drain Output Buffers
PLOD(4/6/8/10/12/16)SM	3.3V Interface Open Drain Output Buffers with Medium Slew-Rate
PLOT(1/2/4/6/8/10/12/16)	3.3V Interface Tri-State Output Buffers
PLOT(4/6/8/10/12/16)SM	3.3V Interface Tri-State Output Buffers with Medium Slew-Rate
KGM80	
POB(1/2/4/6/8/10/12/16)	3.3V Normal Output Buffers
POB(4/6/8/10/12/16)SM	3.3V Normal Output Buffers with Medium Slew-Rate Control
POD(1/2/4/6/8/10/12/16)	3.3V Open Drain Output Buffers
POD(4/6/8/10/12/16)SM	3.3V Open Drain Output Buffers with Medium Slew-Rate Control
POT(1/2/4/6/8/10/12/16)	3.3V Tri-State Output Buffers
POT(4/6/8/10/12/16)SM	3.3V Tri-State Output Buffers with Medium Slew-Rate Control
PHOB(1/2/4/8/12/16/20/24)	5V Interface Normal Output Buffers
PHOB(12/16/20/24)SH	5V Interface Normal Output Buffers with High Slew-Rate Control
PHOB(4/8/12/16/20/24)SM	5V Interface Normal Output Buffers with Medium Slew-Rate Control
PHOD(1/2/4/8/12/16/20/24)	5V Interface Open Drain Output Buffers
PHOD(12/16/20/24)SH	5V Interface Open Drain Output Buffers with High Slew-Rate Control
PHOD(4/8/12/16/20/24)SM	5V Interface Open Drain Output Buffers with Medium Slew-Rate Control
PHOT(1/2/4/8/12/16/20/24)	5V Interface Tri-State Output Buffers
PHOT(12/16/20/24)SH	5V Interface Tri-State Output Buffers with High Slew-Rate Control
PHOT(4/8/12/16/20/24)SM	5V Interface Tri-State Output Buffers with Medium Slew-Rate Control

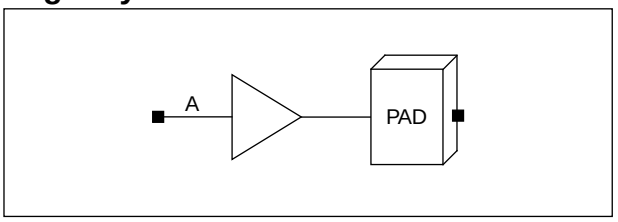
PvOByz

Normal Output Buffers

Cell Availability

Library	5V Operation	3.3V Operation
KG80	POB(1/2/4/8/12/16/20/24) POB(12/16/20/24)SH POB(4/8/12/16/20/24)SM	PLOB(1/2/4/6/8/10/12/16) PLOB(4/6/8/10/12/16)SM
KGM80	PHOB(1/2/4/8/12/16/20/24) PHOB(12/16/20/24)SH PHOB(4/8/12/16/20/24)SM	POB(1/2/4/6/8/10/12/16) POB(4/6/8/10/12/16)SM

Logic Symbol



Truth Table

A	PAD
0	0
1	1

I/O Slot

KG80/KGM80	
PvOByz	1.0

Input Load (SL)

KG80	
	A
POB(1/2/4/8/12/16)	5.5
POB20	9.5
POB24	10.2
POB12SH	20.6
POB16SH	20.0
POB(20/24)SH	10.44
POB4SM	21.3
POB(8/12)SM	20.6
POB16SM	20.0
POB(20/24)SM	11.7
PLOB(1/2/4/6/8/10/12/16)	2.3
PLOB(4/6/8/10/12/16)SM	2.3
KGM80	
	A
POB1	6.5
POB(2/12/16)	6.1
POB(4/6)	4.8
POB8	4.6
POB10	5.2
POB(4/6/8/10/12)SM	13.3
POB16SM	13.4
PHOB(1/2/4/8/12/16/20/24)	2.8
PHOB(12/16/20/24)SH	2.8
PHOB(4/8/12/16/20/24)SM	2.8

KG80 POB1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	14.98	0.36 + 0.292*CL	0.37 + 0.292*CL	0.37 + 0.292*CL
	t_{PHL}	12.03	0.39 + 0.233*CL	0.39 + 0.233*CL	0.39 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.60 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	7.60	0.30 + 0.146*CL	0.29 + 0.146*CL	0.30 + 0.146*CL
	t_{PHL}	6.13	0.31 + 0.116*CL	0.31 + 0.116*CL	0.31 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.242*CL	0.21 + 0.243*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.98	0.29 + 0.094*CL	0.29 + 0.094*CL	0.29 + 0.094*CL
	t_{PHL}	4.02	0.31 + 0.074*CL	0.30 + 0.074*CL	0.31 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.70	0.36 + 0.047*CL	0.36 + 0.047*CL	0.36 + 0.047*CL
	t_{PHL}	2.22	0.36 + 0.037*CL	0.36 + 0.037*CL	0.36 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.14	0.42 + 0.034*CL	0.42 + 0.034*CL	0.41 + 0.035*CL
	t_{PHL}	1.78	0.42 + 0.027*CL	0.42 + 0.027*CL	0.41 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.09 + 0.057*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.77	0.52 + 0.025*CL	0.52 + 0.025*CL	0.51 + 0.025*CL
	t_{PHL}	1.49	0.50 + 0.020*CL	0.50 + 0.020*CL	0.50 + 0.020*CL
	t_R	2.97	0.13 + 0.057*CL	0.12 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.14 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.36	0.37 + 0.020*CL	0.37 + 0.020*CL	0.36 + 0.020*CL
	t_{PHL}	1.24	0.45 + 0.016*CL	0.45 + 0.016*CL	0.45 + 0.016*CL
	t_R	2.33	0.10 + 0.045*CL	0.08 + 0.045*CL	0.09 + 0.045*CL
	t_F	1.74	0.13 + 0.032*CL	0.12 + 0.032*CL	0.11 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.28	0.41 + 0.017*CL	0.41 + 0.017*CL	0.40 + 0.017*CL
	t_{PHL}	1.17	0.48 + 0.014*CL	0.48 + 0.014*CL	0.48 + 0.014*CL
	t_R	2.07	0.10 + 0.039*CL	0.09 + 0.039*CL	0.09 + 0.039*CL
	t_F	1.56	0.15 + 0.028*CL	0.14 + 0.028*CL	0.13 + 0.028*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.78	1.00 + 0.036*CL	1.02 + 0.035*CL	1.03 + 0.035*CL
	t_{PHL}	3.24	1.65 + 0.032*CL	1.76 + 0.030*CL	1.81 + 0.030*CL
	t_R	4.33	0.48 + 0.077*CL	0.44 + 0.078*CL	0.41 + 0.078*CL
	t_F	3.73	0.96 + 0.055*CL	0.97 + 0.055*CL	0.97 + 0.055*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.57	1.22 + 0.027*CL	1.28 + 0.026*CL	1.31 + 0.026*CL
	t_{PHL}	2.95	1.70 + 0.025*CL	1.82 + 0.024*CL	1.87 + 0.023*CL
	t_R	3.42	0.69 + 0.055*CL	0.66 + 0.055*CL	0.65 + 0.055*CL
	t_F	2.99	0.95 + 0.041*CL	1.01 + 0.040*CL	1.02 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.03	0.98 + 0.021*CL	1.03 + 0.020*CL	1.04 + 0.020*CL
	t_{PHL}	2.09	1.22 + 0.017*CL	1.26 + 0.017*CL	1.28 + 0.017*CL
	t_R	2.70	0.56 + 0.043*CL	0.53 + 0.043*CL	0.52 + 0.043*CL
	t_F	2.22	0.69 + 0.031*CL	0.68 + 0.031*CL	0.67 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.03	1.06 + 0.019*CL	1.12 + 0.019*CL	1.15 + 0.018*CL
	t_{PHL}	2.15	1.36 + 0.016*CL	1.40 + 0.015*CL	1.42 + 0.015*CL
	t_R	2.52	0.63 + 0.038*CL	0.63 + 0.038*CL	0.61 + 0.038*CL
	t_F	2.14	0.79 + 0.027*CL	0.79 + 0.027*CL	0.78 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.22	0.53 + 0.094*CL	0.53 + 0.094*CL	0.53 + 0.094*CL
	t_{PHL}	4.76	1.03 + 0.074*CL	1.04 + 0.074*CL	1.05 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.23 + 0.212*CL	0.24 + 0.212*CL
	t_F	8.05	0.42 + 0.153*CL	0.37 + 0.153*CL	0.35 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.16	0.81 + 0.047*CL	0.82 + 0.047*CL	0.82 + 0.047*CL
	t_{PHL}	3.37	1.41 + 0.039*CL	1.48 + 0.038*CL	1.52 + 0.038*CL
	t_R	5.57	0.34 + 0.105*CL	0.29 + 0.105*CL	0.28 + 0.105*CL
	t_F	4.46	0.74 + 0.074*CL	0.72 + 0.075*CL	0.69 + 0.075*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.59	0.85 + 0.035*CL	0.87 + 0.035*CL	0.86 + 0.035*CL
	t_{PHL}	2.88	1.34 + 0.031*CL	1.44 + 0.029*CL	1.48 + 0.029*CL
	t_R	4.21	0.40 + 0.076*CL	0.36 + 0.077*CL	0.34 + 0.077*CL
	t_F	3.54	0.80 + 0.055*CL	0.82 + 0.055*CL	0.82 + 0.055*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.27	0.96 + 0.026*CL	1.00 + 0.026*CL	1.01 + 0.026*CL
	t_{PHL}	2.46	1.28 + 0.024*CL	1.36 + 0.022*CL	1.41 + 0.022*CL
	t_R	3.27	0.52 + 0.055*CL	0.49 + 0.055*CL	0.48 + 0.056*CL
	t_F	2.77	0.73 + 0.041*CL	0.77 + 0.040*CL	0.78 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.70	0.69 + 0.020*CL	0.70 + 0.020*CL	0.70 + 0.020*CL
	t_{PHL}	1.72	0.83 + 0.018*CL	0.88 + 0.017*CL	0.92 + 0.017*CL
	t_R	2.52	0.35 + 0.043*CL	0.33 + 0.044*CL	0.31 + 0.044*CL
	t_F	2.10	0.54 + 0.031*CL	0.55 + 0.031*CL	0.55 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POB24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.68	0.77 + 0.018*CL	0.79 + 0.018*CL	0.81 + 0.018*CL
	t_{PHL}	1.74	0.91 + 0.017*CL	0.98 + 0.016*CL	1.02 + 0.015*CL
	t_R	2.31	0.42 + 0.038*CL	0.40 + 0.038*CL	0.39 + 0.038*CL
	t_F	2.01	0.62 + 0.028*CL	0.63 + 0.028*CL	0.64 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	21.37	0.92 + 0.409*CL	0.93 + 0.409*CL	0.92 + 0.409*CL
	t_{PHL}	13.83	0.63 + 0.264*CL	0.63 + 0.264*CL	0.63 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	10.45	0.80 + 0.193*CL	0.80 + 0.193*CL	0.80 + 0.193*CL
	t_{PHL}	6.71	0.54 + 0.124*CL	0.54 + 0.123*CL	0.53 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.52	0.70 + 0.096*CL	0.69 + 0.097*CL	0.70 + 0.096*CL
	t_{PHL}	3.66	0.58 + 0.062*CL	0.58 + 0.062*CL	0.58 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.16 + 0.133*CL	0.15 + 0.133*CL	0.16 + 0.133*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.98	0.76 + 0.064*CL	0.76 + 0.064*CL	0.76 + 0.064*CL
	t_{PHL}	2.73	0.69 + 0.041*CL	0.67 + 0.041*CL	0.67 + 0.041*CL
	t_R	7.52	0.20 + 0.146*CL	0.19 + 0.147*CL	0.20 + 0.146*CL
	t_F	4.58	0.17 + 0.088*CL	0.14 + 0.089*CL	0.13 + 0.089*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.24	0.84 + 0.048*CL	0.83 + 0.048*CL	0.83 + 0.048*CL
	t_{PHL}	2.33	0.81 + 0.030*CL	0.81 + 0.030*CL	0.79 + 0.031*CL
	t_R	5.66	0.18 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.51	0.24 + 0.065*CL	0.22 + 0.066*CL	0.17 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.90	0.98 + 0.038*CL	0.97 + 0.039*CL	0.97 + 0.039*CL
	t_{PHL}	2.06	0.83 + 0.025*CL	0.83 + 0.025*CL	0.83 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.83	0.21 + 0.052*CL	0.21 + 0.052*CL	0.17 + 0.053*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.72	1.11 + 0.032*CL	1.11 + 0.032*CL	1.11 + 0.032*CL
	t_{PHL}	1.94	0.90 + 0.021*CL	0.92 + 0.021*CL	0.92 + 0.021*CL
	t_R	3.84	0.20 + 0.073*CL	0.18 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.27 + 0.043*CL	0.24 + 0.044*CL	0.24 + 0.044*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.49	1.28 + 0.024*CL	1.26 + 0.024*CL	1.27 + 0.024*CL
	t_{PHL}	1.86	1.04 + 0.016*CL	1.07 + 0.016*CL	1.08 + 0.016*CL
	t_R	3.00	0.25 + 0.055*CL	0.23 + 0.055*CL	0.24 + 0.055*CL
	t_F	1.98	0.36 + 0.033*CL	0.38 + 0.032*CL	0.32 + 0.033*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	6.25	1.29 + 0.099*CL	1.28 + 0.099*CL	1.29 + 0.099*CL
	t_{PHL}	4.16	0.97 + 0.064*CL	0.97 + 0.064*CL	0.98 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.26 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.76	1.48 + 0.066*CL	1.48 + 0.066*CL	1.48 + 0.066*CL
	t_{PHL}	3.43	1.31 + 0.042*CL	1.32 + 0.042*CL	1.32 + 0.042*CL
	t_R	7.71	0.27 + 0.149*CL	0.24 + 0.149*CL	0.25 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.41 + 0.089*CL	0.37 + 0.089*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.11	1.66 + 0.049*CL	1.66 + 0.049*CL	1.67 + 0.049*CL
	t_{PHL}	3.21	1.58 + 0.033*CL	1.63 + 0.032*CL	1.65 + 0.032*CL
	t_R	5.86	0.35 + 0.110*CL	0.30 + 0.111*CL	0.29 + 0.111*CL
	t_F	3.91	0.69 + 0.065*CL	0.65 + 0.065*CL	0.60 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.60	1.67 + 0.039*CL	1.67 + 0.039*CL	1.67 + 0.039*CL
	t_{PHL}	2.85	1.50 + 0.027*CL	1.57 + 0.026*CL	1.61 + 0.026*CL
	t_R	4.72	0.42 + 0.086*CL	0.36 + 0.087*CL	0.34 + 0.087*CL
	t_F	3.34	0.85 + 0.050*CL	0.78 + 0.051*CL	0.80 + 0.050*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.46	1.83 + 0.032*CL	1.85 + 0.032*CL	1.85 + 0.032*CL
	t_{PHL}	2.89	1.66 + 0.025*CL	1.77 + 0.023*CL	1.83 + 0.022*CL
	t_R	4.07	0.54 + 0.071*CL	0.46 + 0.072*CL	0.46 + 0.072*CL
	t_F	3.09	1.01 + 0.042*CL	1.04 + 0.041*CL	1.00 + 0.042*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOB16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.40	2.11 + 0.026*CL	2.17 + 0.025*CL	2.18 + 0.025*CL
	t_{PHL}	3.07	1.95 + 0.022*CL	2.09 + 0.020*CL	2.17 + 0.020*CL
	t_R	3.39	0.75 + 0.053*CL	0.68 + 0.054*CL	0.66 + 0.054*CL
	t_F	2.88	1.24 + 0.033*CL	1.35 + 0.031*CL	1.28 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	20.96	0.52 + 0.409*CL	0.52 + 0.409*CL	0.52 + 0.409*CL
	t_{PHL}	13.70	0.50 + 0.264*CL	0.50 + 0.264*CL	0.50 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	10.05	0.40 + 0.193*CL	0.40 + 0.193*CL	0.40 + 0.193*CL
	t_{PHL}	6.58	0.41 + 0.124*CL	0.41 + 0.124*CL	0.41 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.18	0.36 + 0.096*CL	0.36 + 0.096*CL	0.36 + 0.096*CL
	t_{PHL}	3.54	0.46 + 0.062*CL	0.46 + 0.062*CL	0.45 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.26 + 0.220*CL
	t_F	6.81	0.16 + 0.133*CL	0.15 + 0.133*CL	0.15 + 0.133*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.63	0.41 + 0.064*CL	0.41 + 0.064*CL	0.41 + 0.064*CL
	t_{PHL}	2.60	0.56 + 0.041*CL	0.55 + 0.041*CL	0.55 + 0.041*CL
	t_R	7.52	0.20 + 0.146*CL	0.19 + 0.147*CL	0.20 + 0.146*CL
	t_F	4.58	0.16 + 0.088*CL	0.15 + 0.089*CL	0.13 + 0.089*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.89	0.48 + 0.048*CL	0.48 + 0.048*CL	0.48 + 0.048*CL
	t_{PHL}	2.20	0.69 + 0.030*CL	0.68 + 0.030*CL	0.66 + 0.031*CL
	t_R	5.67	0.18 + 0.110*CL	0.16 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.51	0.24 + 0.065*CL	0.20 + 0.066*CL	0.19 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.50	0.58 + 0.038*CL	0.57 + 0.039*CL	0.57 + 0.039*CL
	t_{PHL}	1.94	0.71 + 0.025*CL	0.71 + 0.025*CL	0.71 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.17 + 0.088*CL	0.17 + 0.088*CL
	t_F	2.84	0.22 + 0.052*CL	0.21 + 0.052*CL	0.18 + 0.053*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.27	0.67 + 0.032*CL	0.67 + 0.032*CL	0.66 + 0.032*CL
	t_{PHL}	1.82	0.78 + 0.021*CL	0.78 + 0.021*CL	0.79 + 0.021*CL
	t_R	3.84	0.20 + 0.073*CL	0.19 + 0.073*CL	0.17 + 0.073*CL
	t_F	2.43	0.28 + 0.043*CL	0.25 + 0.043*CL	0.24 + 0.044*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.04	0.83 + 0.024*CL	0.83 + 0.024*CL	0.82 + 0.024*CL
	t_{PHL}	1.73	0.92 + 0.016*CL	0.94 + 0.016*CL	0.95 + 0.016*CL
	t_R	3.00	0.26 + 0.055*CL	0.23 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.99	0.37 + 0.032*CL	0.37 + 0.032*CL	0.34 + 0.033*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.50	0.54 + 0.099*CL	0.54 + 0.099*CL	0.54 + 0.099*CL
	t_{PHL}	3.98	0.79 + 0.064*CL	0.78 + 0.064*CL	0.79 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.26 + 0.137*CL	0.24 + 0.137*CL	0.22 + 0.137*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.98	0.72 + 0.065*CL	0.69 + 0.066*CL	0.70 + 0.066*CL
	t_{PHL}	3.24	1.12 + 0.042*CL	1.14 + 0.042*CL	1.14 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.26 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.41 + 0.089*CL	0.38 + 0.089*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.32	0.87 + 0.049*CL	0.87 + 0.049*CL	0.87 + 0.049*CL
	t_{PHL}	3.02	1.39 + 0.033*CL	1.43 + 0.032*CL	1.46 + 0.032*CL
	t_R	5.85	0.32 + 0.110*CL	0.29 + 0.111*CL	0.27 + 0.111*CL
	t_F	3.91	0.69 + 0.064*CL	0.62 + 0.065*CL	0.60 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.82	0.88 + 0.039*CL	0.89 + 0.039*CL	0.88 + 0.039*CL
	t_{PHL}	2.66	1.31 + 0.027*CL	1.38 + 0.026*CL	1.43 + 0.026*CL
	t_R	4.70	0.38 + 0.086*CL	0.33 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.34	0.85 + 0.050*CL	0.79 + 0.051*CL	0.80 + 0.050*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.66	1.04 + 0.032*CL	1.06 + 0.032*CL	1.06 + 0.032*CL
	t_{PHL}	2.70	1.47 + 0.025*CL	1.58 + 0.023*CL	1.63 + 0.022*CL
	t_R	4.05	0.50 + 0.071*CL	0.45 + 0.072*CL	0.42 + 0.072*CL
	t_F	3.09	1.03 + 0.041*CL	1.02 + 0.041*CL	1.00 + 0.042*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POB16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.59	1.31 + 0.026*CL	1.35 + 0.025*CL	1.37 + 0.025*CL
	t_{PHL}	2.87	1.76 + 0.022*CL	1.89 + 0.020*CL	1.98 + 0.020*CL
	t_R	3.36	0.70 + 0.053*CL	0.66 + 0.054*CL	0.66 + 0.054*CL
	t_F	2.88	1.25 + 0.033*CL	1.30 + 0.032*CL	1.31 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	15.36	0.75 + 0.292*CL	0.75 + 0.292*CL	0.75 + 0.292*CL
	t_{PHL}	12.37	0.73 + 0.233*CL	0.61 + 0.234*CL	0.83 + 0.232*CL
	t_R	33.59	0.59 + 0.660*CL	0.59 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	7.99	0.68 + 0.146*CL	0.68 + 0.146*CL	0.68 + 0.146*CL
	t_{PHL}	6.46	0.61 + 0.117*CL	0.65 + 0.116*CL	0.75 + 0.115*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.243*CL	0.21 + 0.243*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.37	0.68 + 0.094*CL	0.68 + 0.094*CL	0.68 + 0.094*CL
	t_{PHL}	4.35	0.64 + 0.074*CL	0.64 + 0.074*CL	0.56 + 0.075*CL
	t_R	10.81	0.21 + 0.212*CL	0.22 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.14 + 0.155*CL	0.15 + 0.155*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.09	0.75 + 0.047*CL	0.74 + 0.047*CL	0.75 + 0.047*CL
	t_{PHL}	2.56	0.70 + 0.037*CL	0.70 + 0.037*CL	0.76 + 0.036*CL
	t_R	5.43	0.13 + 0.106*CL	0.12 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.09 + 0.077*CL	0.10 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.53	0.81 + 0.034*CL	0.81 + 0.034*CL	0.81 + 0.035*CL
	t_{PHL}	2.11	0.73 + 0.028*CL	0.76 + 0.027*CL	0.81 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.12 + 0.056*CL	0.08 + 0.057*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.16	0.91 + 0.025*CL	0.91 + 0.025*CL	0.91 + 0.025*CL
	t_{PHL}	1.83	0.83 + 0.020*CL	0.77 + 0.021*CL	0.88 + 0.019*CL
	t_R	2.97	0.14 + 0.057*CL	0.12 + 0.057*CL	0.11 + 0.057*CL
	t_F	2.20	0.15 + 0.041*CL	0.14 + 0.041*CL	0.14 + 0.041*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.90	0.91 + 0.020*CL	0.90 + 0.020*CL	0.91 + 0.020*CL
	t_{PHL}	1.65	0.87 + 0.016*CL	0.87 + 0.016*CL	0.86 + 0.016*CL
	t_R	2.34	0.11 + 0.045*CL	0.08 + 0.045*CL	0.10 + 0.045*CL
	t_F	1.75	0.15 + 0.032*CL	0.10 + 0.033*CL	0.13 + 0.032*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.85	0.99 + 0.017*CL	0.98 + 0.017*CL	0.98 + 0.017*CL
	t_{PHL}	1.60	0.91 + 0.014*CL	0.92 + 0.014*CL	0.91 + 0.014*CL
	t_R	2.08	0.12 + 0.039*CL	0.11 + 0.039*CL	0.08 + 0.040*CL
	t_F	1.57	0.17 + 0.028*CL	0.13 + 0.028*CL	0.13 + 0.028*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.76	1.98 + 0.036*CL	2.00 + 0.035*CL	2.01 + 0.035*CL
	t_{PHL}	3.90	2.31 + 0.032*CL	2.42 + 0.030*CL	2.47 + 0.030*CL
	t_R	4.37	0.54 + 0.077*CL	0.48 + 0.077*CL	0.46 + 0.078*CL
	t_F	3.74	0.96 + 0.056*CL	0.99 + 0.055*CL	0.98 + 0.055*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.54	2.19 + 0.027*CL	2.25 + 0.026*CL	2.28 + 0.026*CL
	t_{PHL}	3.60	2.35 + 0.025*CL	2.46 + 0.024*CL	2.52 + 0.023*CL
	t_R	3.47	0.76 + 0.054*CL	0.73 + 0.055*CL	0.69 + 0.055*CL
	t_F	3.00	0.96 + 0.041*CL	1.00 + 0.040*CL	1.04 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.62	1.56 + 0.021*CL	1.61 + 0.020*CL	1.63 + 0.020*CL
	t_{PHL}	2.54	1.67 + 0.017*CL	1.71 + 0.017*CL	1.73 + 0.017*CL
	t_R	2.73	0.60 + 0.043*CL	0.54 + 0.043*CL	0.56 + 0.043*CL
	t_F	2.23	0.71 + 0.031*CL	0.71 + 0.030*CL	0.65 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.62	1.65 + 0.019*CL	1.71 + 0.019*CL	1.73 + 0.018*CL
	t_{PHL}	2.60	1.81 + 0.016*CL	1.85 + 0.015*CL	1.86 + 0.015*CL
	t_R	2.54	0.67 + 0.037*CL	0.63 + 0.038*CL	0.65 + 0.038*CL
	t_F	2.15	0.82 + 0.027*CL	0.78 + 0.027*CL	0.80 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	6.14	1.45 + 0.094*CL	1.44 + 0.094*CL	1.46 + 0.094*CL
	t_{PHL}	5.43	1.71 + 0.074*CL	1.72 + 0.074*CL	1.72 + 0.074*CL
	t_R	10.84	0.25 + 0.212*CL	0.25 + 0.212*CL	0.24 + 0.212*CL
	t_F	8.06	0.43 + 0.153*CL	0.39 + 0.153*CL	0.36 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.12	1.77 + 0.047*CL	1.78 + 0.047*CL	1.78 + 0.047*CL
	t_{PHL}	4.04	2.08 + 0.039*CL	2.14 + 0.038*CL	2.18 + 0.038*CL
	t_R	5.60	0.38 + 0.104*CL	0.34 + 0.105*CL	0.32 + 0.105*CL
	t_F	4.47	0.74 + 0.074*CL	0.73 + 0.075*CL	0.69 + 0.075*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.54	1.79 + 0.035*CL	1.81 + 0.035*CL	1.82 + 0.035*CL
	t_{PHL}	3.53	2.00 + 0.031*CL	2.09 + 0.030*CL	2.13 + 0.029*CL
	t_R	4.25	0.46 + 0.076*CL	0.41 + 0.077*CL	0.40 + 0.077*CL
	t_F	3.56	0.83 + 0.055*CL	0.81 + 0.055*CL	0.83 + 0.055*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.19	1.87 + 0.026*CL	1.92 + 0.026*CL	1.93 + 0.026*CL
	t_{PHL}	3.10	1.91 + 0.024*CL	2.01 + 0.022*CL	2.05 + 0.022*CL
	t_R	3.32	0.59 + 0.055*CL	0.56 + 0.055*CL	0.53 + 0.055*CL
	t_F	2.78	0.74 + 0.041*CL	0.77 + 0.040*CL	0.80 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.35	1.33 + 0.020*CL	1.36 + 0.020*CL	1.36 + 0.020*CL
	t_{PHL}	2.19	1.30 + 0.018*CL	1.35 + 0.017*CL	1.39 + 0.017*CL
	t_R	2.54	0.39 + 0.043*CL	0.35 + 0.044*CL	0.33 + 0.044*CL
	t_F	2.12	0.56 + 0.031*CL	0.57 + 0.031*CL	0.56 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOB24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

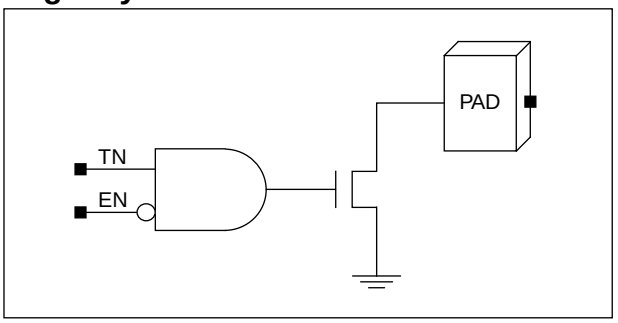
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.33	1.42 + 0.018*CL	1.44 + 0.018*CL	1.47 + 0.018*CL
	t_{PHL}	2.21	1.38 + 0.017*CL	1.45 + 0.016*CL	1.48 + 0.015*CL
	t_R	2.34	0.46 + 0.038*CL	0.44 + 0.038*CL	0.42 + 0.038*CL
	t_F	2.02	0.65 + 0.028*CL	0.65 + 0.027*CL	0.66 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Cell Availability

Library	5V Operation	3.3V Operation
KG80	POD(1/2/4/8/12/16/20/24) POD(12/16/20/24)SH POD(4/8/12/16/20/24)SM	PLOD(1/2/4/6/8/10/12/16) PLOD(4/6/8/10/12/16)SM
KGM80	PHOD(1/2/4/8/12/16/20/24) PHOD(12/16/20/24)SH PHOD(4/8/12/16/20/24)SM	POD(1/2/4/6/8/10/12/16) POD(4/6/8/10/12/16)SM

Logic Symbol



NOTES:

1. KG80 standard open-drain output buffers, POD(1/2/4/8/12/16/20/24), cannot tolerate external pull-ups to more than 5.5V. And KGM80 standard open-drain output buffers, POD(1/2/4/6/8/10/12/16), cannot tolerate external pull-ups to more than 3.6V.
2. Fail-safe open-drain output buffers with external pull-ups to more than 5.5V (in case of KG80) / 3.6V (in case of KGM80) can drive signals to that voltage range. However, if you want to use fail-safe open-drains, please contact to SEC ASIC first.

I/O Slot

KG80/KGM80	
PvODyz	1.0

Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

Input Load (SL)

KG80		
	TN	EN
POD(1/2/4/8/12/16/20/24)	1.4	1.6
POD(12/16/20/24)SH	1.4	1.6
POD(4/8/12/16/20/24)SM	1.4	1.6
PLOD(1/2/4/6/8/10/12/16)	1.2	1.2
PLOD(4/6/8/10/12/16)SM	1.2	1.2
KGM80		
	TN	EN
POD(1/2/4/6/8/10/12/16)	1.8	1.8
POD(4/6/8/10/12/16)SM	1.8	1.8
PHOD(1/2/4/8/12/16/20/24)	1.4	1.4
PHOD(12/16/20/24)SH	1.4	1.4
PHOD(4/8/12/16/20/24)SM	1.4	1.4

KG80 POD1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	12.21	0.56 + 0.233*CL	0.57 + 0.233*CL	0.56 + 0.233*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.39 + 0.485*CL
	t_{PLZ}	0.50	0.50 + 0.000*CL	0.50 + 0.000*CL	0.50 + 0.000*CL
EN to PAD	t_{PHL}	12.36	0.72 + 0.233*CL	0.71 + 0.233*CL	0.73 + 0.233*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.39 + 0.485*CL
	t_{PLZ}	0.41	0.41 + 0.000*CL	0.41 + 0.000*CL	0.41 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	6.29	0.47 + 0.116*CL	0.47 + 0.116*CL	0.47 + 0.116*CL
	t_F	12.34	0.21 + 0.243*CL	0.20 + 0.243*CL	0.21 + 0.243*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL
EN to PAD	t_{PHL}	6.45	0.63 + 0.116*CL	0.63 + 0.116*CL	0.62 + 0.116*CL
	t_F	12.34	0.21 + 0.243*CL	0.20 + 0.243*CL	0.21 + 0.243*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.19	0.48 + 0.074*CL	0.48 + 0.074*CL	0.47 + 0.074*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
	t_{PLZ}	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL
EN to PAD	t_{PHL}	4.34	0.63 + 0.074*CL	0.64 + 0.074*CL	0.63 + 0.074*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
	t_{PLZ}	0.45	0.45 + 0.000*CL	0.45 + 0.000*CL	0.45 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.38	0.53 + 0.037*CL	0.53 + 0.037*CL	0.53 + 0.037*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
EN to PAD	t_{PHL}	2.54	0.69 + 0.037*CL	0.69 + 0.037*CL	0.69 + 0.037*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
	t_{PLZ}	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.95	0.58 + 0.027*CL	0.58 + 0.027*CL	0.58 + 0.027*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.10 + 0.057*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL
EN to PAD	t_{PHL}	2.10	0.74 + 0.027*CL	0.74 + 0.027*CL	0.74 + 0.027*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.10 + 0.057*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.66	0.66 + 0.020*CL	0.66 + 0.020*CL	0.67 + 0.020*CL
	t_F	2.19	0.15 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
	t_{PLZ}	0.76	0.76 + 0.000*CL	0.76 + 0.000*CL	0.76 + 0.000*CL
EN to PAD	t_{PHL}	1.82	0.82 + 0.020*CL	0.83 + 0.020*CL	0.82 + 0.020*CL
	t_F	2.19	0.15 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.67 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.53	0.74 + 0.016*CL	0.74 + 0.016*CL	0.75 + 0.016*CL
	t_F	1.79	0.20 + 0.032*CL	0.19 + 0.032*CL	0.17 + 0.032*CL
	t_{PLZ}	0.85	0.84 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL
EN to PAD	t_{PHL}	1.69	0.89 + 0.016*CL	0.90 + 0.016*CL	0.90 + 0.016*CL
	t_F	1.79	0.20 + 0.032*CL	0.19 + 0.032*CL	0.17 + 0.032*CL
	t_{PLZ}	0.76	0.76 + 0.000*CL	0.76 + 0.000*CL	0.76 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.48	0.77 + 0.014*CL	0.79 + 0.014*CL	0.79 + 0.014*CL
	t_F	1.62	0.23 + 0.028*CL	0.22 + 0.028*CL	0.21 + 0.028*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PHL}	1.64	0.93 + 0.014*CL	0.95 + 0.014*CL	0.95 + 0.014*CL
	t_F	1.62	0.23 + 0.028*CL	0.22 + 0.028*CL	0.21 + 0.028*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.82 + 0.000*CL	0.82 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.58	1.17 + 0.028*CL	1.19 + 0.028*CL	1.20 + 0.028*CL
	t_F	3.19	0.41 + 0.056*CL	0.37 + 0.056*CL	0.35 + 0.056*CL
	t_{PLZ}	0.52	0.52 + 0.000*CL	0.52 + 0.000*CL	0.52 + 0.000*CL
EN to PAD	t_{PHL}	2.74	1.33 + 0.028*CL	1.35 + 0.028*CL	1.35 + 0.028*CL
	t_F	3.19	0.41 + 0.056*CL	0.37 + 0.056*CL	0.35 + 0.056*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.45	1.36 + 0.022*CL	1.42 + 0.021*CL	1.44 + 0.021*CL
	t_F	2.56	0.60 + 0.039*CL	0.57 + 0.040*CL	0.56 + 0.040*CL
	t_{PLZ}	0.52	0.52 + 0.000*CL	0.52 + 0.000*CL	0.52 + 0.000*CL
EN to PAD	t_{PHL}	2.61	1.52 + 0.022*CL	1.57 + 0.021*CL	1.61 + 0.021*CL
	t_F	2.56	0.60 + 0.039*CL	0.57 + 0.040*CL	0.56 + 0.040*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.27	1.34 + 0.019*CL	1.42 + 0.018*CL	1.45 + 0.017*CL
	t_F	2.26	0.73 + 0.031*CL	0.73 + 0.031*CL	0.72 + 0.031*CL
	t_{PLZ}	0.56	0.56 + 0.000*CL	0.56 + 0.000*CL	0.56 + 0.000*CL
EN to PAD	t_{PHL}	2.43	1.49 + 0.019*CL	1.57 + 0.018*CL	1.62 + 0.017*CL
	t_F	2.26	0.73 + 0.031*CL	0.73 + 0.031*CL	0.72 + 0.031*CL
	t_{PLZ}	0.47	0.47 + 0.000*CL	0.47 + 0.000*CL	0.47 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.29	1.40 + 0.018*CL	1.50 + 0.017*CL	1.54 + 0.016*CL
	t_F	2.17	0.81 + 0.027*CL	0.82 + 0.027*CL	0.82 + 0.027*CL
	t_{PLZ}	0.56	0.56 + 0.000*CL	0.56 + 0.000*CL	0.56 + 0.000*CL
EN to PAD	t_{PHL}	2.45	1.56 + 0.018*CL	1.66 + 0.016*CL	1.70 + 0.016*CL
	t_F	2.17	0.81 + 0.027*CL	0.82 + 0.027*CL	0.82 + 0.027*CL
	t_{PLZ}	0.47	0.47 + 0.000*CL	0.47 + 0.000*CL	0.47 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.43	0.71 + 0.074*CL	0.72 + 0.074*CL	0.71 + 0.074*CL
	t_F	7.89	0.16 + 0.155*CL	0.15 + 0.155*CL	0.16 + 0.155*CL
	t_{PLZ}	0.57	0.57 + 0.000*CL	0.57 + 0.000*CL	0.57 + 0.000*CL
EN to PAD	t_{PHL}	4.58	0.87 + 0.074*CL	0.87 + 0.074*CL	0.87 + 0.074*CL
	t_F	7.89	0.16 + 0.155*CL	0.15 + 0.155*CL	0.16 + 0.155*CL
	t_{PLZ}	0.49	0.49 + 0.000*CL	0.49 + 0.000*CL	0.49 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.87	1.01 + 0.037*CL	1.01 + 0.037*CL	1.02 + 0.037*CL
	t_F	4.07	0.27 + 0.076*CL	0.24 + 0.076*CL	0.22 + 0.077*CL
	t_{PLZ}	0.57	0.57 + 0.000*CL	0.57 + 0.000*CL	0.57 + 0.000*CL
EN to PAD	t_{PHL}	3.03	1.17 + 0.037*CL	1.17 + 0.037*CL	1.17 + 0.037*CL
	t_F	4.07	0.27 + 0.076*CL	0.24 + 0.076*CL	0.22 + 0.077*CL
	t_{PLZ}	0.49	0.49 + 0.000*CL	0.49 + 0.000*CL	0.49 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.38	1.00 + 0.028*CL	1.01 + 0.027*CL	1.03 + 0.027*CL
	t_F	3.10	0.36 + 0.055*CL	0.33 + 0.055*CL	0.30 + 0.056*CL
	t_{PLZ}	0.56	0.56 + 0.000*CL	0.56 + 0.000*CL	0.56 + 0.000*CL
EN to PAD	t_{PHL}	2.54	1.16 + 0.028*CL	1.17 + 0.027*CL	1.18 + 0.027*CL
	t_F	3.10	0.36 + 0.055*CL	0.33 + 0.055*CL	0.30 + 0.056*CL
	t_{PLZ}	0.48	0.48 + 0.000*CL	0.48 + 0.000*CL	0.48 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.12	1.06 + 0.021*CL	1.10 + 0.021*CL	1.12 + 0.020*CL
	t_F	2.47	0.51 + 0.039*CL	0.48 + 0.040*CL	0.46 + 0.040*CL
	t_{PLZ}	0.59	0.59 + 0.000*CL	0.59 + 0.000*CL	0.59 + 0.000*CL
EN to PAD	t_{PHL}	2.27	1.21 + 0.021*CL	1.26 + 0.021*CL	1.28 + 0.020*CL
	t_F	2.47	0.51 + 0.039*CL	0.48 + 0.040*CL	0.46 + 0.040*CL
	t_{PLZ}	0.51	0.51 + 0.000*CL	0.51 + 0.000*CL	0.51 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.98	1.08 + 0.018*CL	1.15 + 0.017*CL	1.17 + 0.017*CL
	t_F	2.15	0.62 + 0.031*CL	0.61 + 0.031*CL	0.60 + 0.031*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
EN to PAD	t_{PHL}	2.14	1.24 + 0.018*CL	1.30 + 0.017*CL	1.34 + 0.017*CL
	t_F	2.15	0.62 + 0.031*CL	0.61 + 0.031*CL	0.60 + 0.031*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POD24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.00	1.14 + 0.017*CL	1.22 + 0.016*CL	1.27 + 0.016*CL
	t_F	2.07	0.71 + 0.027*CL	0.73 + 0.027*CL	0.73 + 0.027*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
EN to PAD	t_{PHL}	2.16	1.30 + 0.017*CL	1.38 + 0.016*CL	1.42 + 0.016*CL
	t_F	2.07	0.71 + 0.027*CL	0.73 + 0.027*CL	0.73 + 0.027*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	14.09	0.89 + 0.264*CL	0.88 + 0.264*CL	0.88 + 0.264*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.80	0.80 + 0.000*CL	0.80 + 0.000*CL	0.80 + 0.000*CL
EN to PAD	t_{PHL}	14.20	1.00 + 0.264*CL	1.00 + 0.264*CL	1.00 + 0.264*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.73	0.73 + 0.000*CL	0.73 + 0.000*CL	0.73 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	6.97	0.79 + 0.124*CL	0.79 + 0.124*CL	0.80 + 0.123*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL
EN to PAD	t_{PHL}	7.08	0.91 + 0.123*CL	0.90 + 0.124*CL	0.90 + 0.124*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.78	0.78 + 0.000*CL	0.78 + 0.000*CL	0.78 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.92	0.83 + 0.062*CL	0.83 + 0.062*CL	0.82 + 0.062*CL
	t_F	6.81	0.15 + 0.133*CL	0.15 + 0.133*CL	0.16 + 0.133*CL
	t_{PLZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PHL}	4.03	0.94 + 0.062*CL	0.94 + 0.062*CL	0.94 + 0.062*CL
	t_F	6.81	0.16 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.96	0.90 + 0.041*CL	0.90 + 0.041*CL	0.91 + 0.041*CL
	t_F	4.57	0.14 + 0.089*CL	0.13 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
EN to PAD	t_{PHL}	3.07	1.01 + 0.041*CL	1.02 + 0.041*CL	1.01 + 0.041*CL
	t_F	4.57	0.14 + 0.089*CL	0.12 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.54	0.99 + 0.031*CL	0.99 + 0.031*CL	0.99 + 0.031*CL
	t_F	3.48	0.18 + 0.066*CL	0.15 + 0.066*CL	0.16 + 0.066*CL
	t_{PLZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL
EN to PAD	t_{PHL}	2.65	1.10 + 0.031*CL	1.10 + 0.031*CL	1.11 + 0.031*CL
	t_F	3.47	0.18 + 0.066*CL	0.15 + 0.066*CL	0.13 + 0.066*CL
	t_{PLZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.32	1.08 + 0.025*CL	1.08 + 0.025*CL	1.09 + 0.025*CL
	t_F	2.84	0.24 + 0.052*CL	0.17 + 0.053*CL	0.19 + 0.053*CL
	t_{PLZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
EN to PAD	t_{PHL}	2.43	1.19 + 0.025*CL	1.20 + 0.025*CL	1.19 + 0.025*CL
	t_F	2.84	0.23 + 0.052*CL	0.19 + 0.053*CL	0.19 + 0.053*CL
	t_{PLZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.20	1.16 + 0.021*CL	1.17 + 0.021*CL	1.18 + 0.021*CL
	t_F	2.43	0.28 + 0.043*CL	0.25 + 0.044*CL	0.26 + 0.043*CL
	t_{PLZ}	1.19	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
EN to PAD	t_{PHL}	2.31	1.27 + 0.021*CL	1.28 + 0.021*CL	1.28 + 0.021*CL
	t_F	2.44	0.28 + 0.043*CL	0.27 + 0.043*CL	0.26 + 0.043*CL
	t_{PLZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.11	1.29 + 0.016*CL	1.32 + 0.016*CL	1.32 + 0.016*CL
	t_F	1.99	0.37 + 0.032*CL	0.38 + 0.032*CL	0.34 + 0.033*CL
	t_{PLZ}	1.31	1.31 + 0.000*CL	1.31 + 0.000*CL	1.31 + 0.000*CL
EN to PAD	t_{PHL}	2.22	1.40 + 0.016*CL	1.42 + 0.016*CL	1.44 + 0.016*CL
	t_F	2.00	0.39 + 0.032*CL	0.37 + 0.032*CL	0.36 + 0.033*CL
	t_{PLZ}	1.25	1.24 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.51	1.32 + 0.064*CL	1.32 + 0.064*CL	1.32 + 0.064*CL
	t_F	7.11	0.28 + 0.137*CL	0.24 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	4.62	1.43 + 0.064*CL	1.43 + 0.064*CL	1.43 + 0.064*CL
	t_F	7.10	0.27 + 0.137*CL	0.24 + 0.137*CL	0.23 + 0.137*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.77	1.65 + 0.042*CL	1.66 + 0.042*CL	1.67 + 0.042*CL
	t_F	4.89	0.48 + 0.088*CL	0.44 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	3.88	1.76 + 0.042*CL	1.78 + 0.042*CL	1.79 + 0.042*CL
	t_F	4.89	0.48 + 0.088*CL	0.42 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.56	1.92 + 0.033*CL	1.98 + 0.032*CL	1.99 + 0.032*CL
	t_F	3.93	0.72 + 0.064*CL	0.65 + 0.065*CL	0.61 + 0.066*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	3.67	2.03 + 0.033*CL	2.09 + 0.032*CL	2.10 + 0.032*CL
	t_F	3.93	0.72 + 0.064*CL	0.65 + 0.065*CL	0.62 + 0.066*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.20	1.83 + 0.027*CL	1.92 + 0.026*CL	1.95 + 0.026*CL
	t_F	3.38	0.91 + 0.049*CL	0.84 + 0.050*CL	0.82 + 0.050*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
EN to PAD	t_{PHL}	3.31	1.94 + 0.027*CL	2.03 + 0.026*CL	2.07 + 0.026*CL
	t_F	3.38	0.92 + 0.049*CL	0.88 + 0.050*CL	0.82 + 0.050*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.23	1.99 + 0.025*CL	2.10 + 0.023*CL	2.16 + 0.023*CL
	t_F	3.15	1.12 + 0.041*CL	1.06 + 0.041*CL	1.08 + 0.041*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
EN to PAD	t_{PHL}	3.34	2.10 + 0.025*CL	2.21 + 0.023*CL	2.28 + 0.023*CL
	t_F	3.15	1.12 + 0.041*CL	1.11 + 0.041*CL	1.06 + 0.041*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOD16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.38	2.23 + 0.023*CL	2.41 + 0.021*CL	2.48 + 0.020*CL
	t_F	2.98	1.43 + 0.031*CL	1.44 + 0.031*CL	1.41 + 0.031*CL
	t_{PLZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PHL}	3.50	2.35 + 0.023*CL	2.51 + 0.021*CL	2.60 + 0.020*CL
	t_F	2.99	1.45 + 0.031*CL	1.42 + 0.031*CL	1.42 + 0.031*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	13.96	0.76 + 0.264*CL	0.76 + 0.264*CL	0.76 + 0.264*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.64	0.64 + 0.000*CL	0.64 + 0.000*CL	0.64 + 0.000*CL
EN to PAD	t_{PHL}	14.16	0.96 + 0.264*CL	0.96 + 0.264*CL	0.96 + 0.264*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	6.85	0.68 + 0.124*CL	0.67 + 0.124*CL	0.68 + 0.123*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL
EN to PAD	t_{PHL}	7.04	0.87 + 0.124*CL	0.87 + 0.123*CL	0.87 + 0.124*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.57	0.57 + 0.000*CL	0.57 + 0.000*CL	0.57 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.80	0.71 + 0.062*CL	0.71 + 0.062*CL	0.71 + 0.062*CL
	t_F	6.81	0.15 + 0.133*CL	0.15 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	3.99	0.90 + 0.062*CL	0.90 + 0.062*CL	0.90 + 0.062*CL
	t_F	6.81	0.15 + 0.133*CL	0.15 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	0.64	0.64 + 0.000*CL	0.64 + 0.000*CL	0.64 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.85	0.79 + 0.041*CL	0.79 + 0.041*CL	0.79 + 0.041*CL
	t_F	4.57	0.14 + 0.089*CL	0.14 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	0.82	0.82 + 0.000*CL	0.82 + 0.000*CL	0.82 + 0.000*CL
EN to PAD	t_{PHL}	3.04	0.98 + 0.041*CL	0.98 + 0.041*CL	0.98 + 0.041*CL
	t_F	4.57	0.14 + 0.089*CL	0.13 + 0.089*CL	0.14 + 0.089*CL
	t_{PLZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.40	0.86 + 0.031*CL	0.85 + 0.031*CL	0.86 + 0.031*CL
	t_F	3.49	0.21 + 0.066*CL	0.18 + 0.066*CL	0.16 + 0.066*CL
	t_{PLZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL
EN to PAD	t_{PHL}	2.61	1.07 + 0.031*CL	1.06 + 0.031*CL	1.07 + 0.031*CL
	t_F	3.47	0.18 + 0.066*CL	0.15 + 0.066*CL	0.15 + 0.066*CL
	t_{PLZ}	0.78	0.78 + 0.000*CL	0.78 + 0.000*CL	0.78 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.18	0.95 + 0.025*CL	0.95 + 0.025*CL	0.95 + 0.025*CL
	t_F	2.86	0.27 + 0.052*CL	0.22 + 0.052*CL	0.21 + 0.053*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL
EN to PAD	t_{PHL}	2.39	1.15 + 0.025*CL	1.16 + 0.025*CL	1.15 + 0.025*CL
	t_F	2.84	0.24 + 0.052*CL	0.19 + 0.053*CL	0.20 + 0.053*CL
	t_{PLZ}	0.85	0.84 + 0.000*CL	0.84 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.07	1.03 + 0.021*CL	1.03 + 0.021*CL	1.03 + 0.021*CL
	t_F	2.46	0.33 + 0.043*CL	0.30 + 0.043*CL	0.25 + 0.044*CL
	t_{PLZ}	1.02	1.02 + 0.000*CL	1.02 + 0.000*CL	1.02 + 0.000*CL
EN to PAD	t_{PHL}	2.27	1.23 + 0.021*CL	1.25 + 0.021*CL	1.25 + 0.021*CL
	t_F	2.44	0.28 + 0.043*CL	0.25 + 0.044*CL	0.26 + 0.043*CL
	t_{PLZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.98	1.16 + 0.016*CL	1.18 + 0.016*CL	1.20 + 0.016*CL
	t_F	2.01	0.39 + 0.032*CL	0.39 + 0.032*CL	0.38 + 0.032*CL
	t_{PLZ}	1.15	1.15 + 0.000*CL	1.15 + 0.000*CL	1.15 + 0.000*CL
EN to PAD	t_{PHL}	2.18	1.36 + 0.016*CL	1.40 + 0.016*CL	1.39 + 0.016*CL
	t_F	2.00	0.39 + 0.032*CL	0.36 + 0.033*CL	0.34 + 0.033*CL
	t_{PLZ}	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.39	1.20 + 0.064*CL	1.20 + 0.064*CL	1.20 + 0.064*CL
	t_F	7.11	0.28 + 0.137*CL	0.24 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	0.70	0.70 + 0.000*CL	0.70 + 0.000*CL	0.70 + 0.000*CL
EN to PAD	t_{PHL}	4.58	1.39 + 0.064*CL	1.39 + 0.064*CL	1.39 + 0.064*CL
	t_F	7.10	0.27 + 0.137*CL	0.24 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.65	1.54 + 0.042*CL	1.55 + 0.042*CL	1.55 + 0.042*CL
	t_F	4.89	0.48 + 0.088*CL	0.43 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	0.70	0.70 + 0.000*CL	0.70 + 0.000*CL	0.70 + 0.000*CL
EN to PAD	t_{PHL}	3.85	1.73 + 0.042*CL	1.74 + 0.042*CL	1.74 + 0.042*CL
	t_F	4.89	0.48 + 0.088*CL	0.43 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.44	1.80 + 0.033*CL	1.85 + 0.032*CL	1.88 + 0.032*CL
	t_F	3.93	0.73 + 0.064*CL	0.64 + 0.065*CL	0.63 + 0.065*CL
	t_{PLZ}	0.70	0.70 + 0.000*CL	0.70 + 0.000*CL	0.70 + 0.000*CL
EN to PAD	t_{PHL}	3.63	2.00 + 0.033*CL	2.04 + 0.032*CL	2.07 + 0.032*CL
	t_F	3.93	0.72 + 0.064*CL	0.66 + 0.065*CL	0.62 + 0.065*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.08	1.72 + 0.027*CL	1.80 + 0.026*CL	1.84 + 0.026*CL
	t_F	3.38	0.91 + 0.049*CL	0.86 + 0.050*CL	0.83 + 0.050*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	3.27	1.91 + 0.027*CL	1.99 + 0.026*CL	2.03 + 0.026*CL
	t_F	3.38	0.92 + 0.049*CL	0.87 + 0.050*CL	0.83 + 0.050*CL
	t_{PLZ}	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.11	1.87 + 0.025*CL	1.99 + 0.023*CL	2.04 + 0.023*CL
	t_F	3.15	1.13 + 0.040*CL	1.07 + 0.041*CL	1.07 + 0.041*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	3.30	2.06 + 0.025*CL	2.18 + 0.023*CL	2.24 + 0.023*CL
	t_F	3.15	1.12 + 0.041*CL	1.09 + 0.041*CL	1.08 + 0.041*CL
	t_{PLZ}	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POD16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.27	2.12 + 0.023*CL	2.28 + 0.021*CL	2.37 + 0.020*CL
	t_F	2.98	1.43 + 0.031*CL	1.46 + 0.031*CL	1.43 + 0.031*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	3.46	2.31 + 0.023*CL	2.48 + 0.021*CL	2.56 + 0.020*CL
	t_F	2.98	1.43 + 0.031*CL	1.45 + 0.031*CL	1.43 + 0.031*CL
	t_{PLZ}	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	12.57	0.93 + 0.233*CL	0.93 + 0.233*CL	0.93 + 0.233*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL
EN to PAD	t_{PHL}	12.75	1.10 + 0.233*CL	1.10 + 0.233*CL	1.10 + 0.233*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
	t_{PLZ}	0.77	0.77 + 0.000*CL	0.77 + 0.000*CL	0.77 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	6.66	0.84 + 0.116*CL	0.84 + 0.116*CL	0.84 + 0.116*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.243*CL	0.21 + 0.243*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	6.83	1.01 + 0.116*CL	1.01 + 0.116*CL	1.01 + 0.116*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.243*CL	0.21 + 0.243*CL
	t_{PLZ}	0.80	0.80 + 0.000*CL	0.80 + 0.000*CL	0.80 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.56	0.85 + 0.074*CL	0.85 + 0.074*CL	0.85 + 0.074*CL
	t_F	7.88	0.14 + 0.155*CL	0.14 + 0.155*CL	0.15 + 0.155*CL
	t_{PLZ}	0.88	0.88 + 0.000*CL	0.88 + 0.000*CL	0.88 + 0.000*CL
EN to PAD	t_{PHL}	4.73	1.02 + 0.074*CL	1.02 + 0.074*CL	1.02 + 0.074*CL
	t_F	7.88	0.15 + 0.155*CL	0.15 + 0.155*CL	0.15 + 0.155*CL
	t_{PLZ}	0.80	0.80 + 0.000*CL	0.80 + 0.000*CL	0.80 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.76	0.90 + 0.037*CL	0.90 + 0.037*CL	0.90 + 0.037*CL
	t_F	3.96	0.10 + 0.077*CL	0.10 + 0.077*CL	0.10 + 0.077*CL
	t_{PLZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PHL}	2.93	1.07 + 0.037*CL	1.07 + 0.037*CL	1.07 + 0.037*CL
	t_F	3.96	0.10 + 0.077*CL	0.10 + 0.077*CL	0.10 + 0.077*CL
	t_{PLZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.32	0.95 + 0.027*CL	0.96 + 0.027*CL	0.96 + 0.027*CL
	t_F	2.93	0.11 + 0.056*CL	0.12 + 0.056*CL	0.09 + 0.057*CL
	t_{PLZ}	1.03	1.03 + 0.000*CL	1.03 + 0.000*CL	1.03 + 0.000*CL
EN to PAD	t_{PHL}	2.49	1.13 + 0.027*CL	1.13 + 0.027*CL	1.13 + 0.027*CL
	t_F	2.94	0.12 + 0.056*CL	0.09 + 0.057*CL	0.10 + 0.057*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.03	1.04 + 0.020*CL	1.03 + 0.020*CL	1.04 + 0.020*CL
	t_F	2.20	0.15 + 0.041*CL	0.15 + 0.041*CL	0.15 + 0.041*CL
	t_{PLZ}	1.11	1.11 + 0.000*CL	1.10 + 0.000*CL	1.11 + 0.000*CL
EN to PAD	t_{PHL}	2.21	1.21 + 0.020*CL	1.21 + 0.020*CL	1.20 + 0.020*CL
	t_F	2.20	0.15 + 0.041*CL	0.16 + 0.041*CL	0.14 + 0.041*CL
	t_{PLZ}	1.03	1.03 + 0.000*CL	1.03 + 0.000*CL	1.03 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.90	1.11 + 0.016*CL	1.12 + 0.016*CL	1.12 + 0.016*CL
	t_F	1.80	0.23 + 0.031*CL	0.18 + 0.032*CL	0.18 + 0.032*CL
	t_{PLZ}	1.19	1.19 + 0.000*CL	1.18 + 0.000*CL	1.19 + 0.000*CL
EN to PAD	t_{PHL}	2.08	1.28 + 0.016*CL	1.29 + 0.016*CL	1.29 + 0.016*CL
	t_F	1.80	0.22 + 0.032*CL	0.19 + 0.032*CL	0.20 + 0.032*CL
	t_{PLZ}	1.12	1.11 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.86	1.15 + 0.014*CL	1.16 + 0.014*CL	1.16 + 0.014*CL
	t_F	1.63	0.24 + 0.028*CL	0.22 + 0.028*CL	0.22 + 0.028*CL
	t_{PLZ}	1.24	1.24 + 0.000*CL	1.24 + 0.000*CL	1.24 + 0.000*CL
EN to PAD	t_{PHL}	2.03	1.32 + 0.014*CL	1.33 + 0.014*CL	1.34 + 0.014*CL
	t_F	1.64	0.25 + 0.028*CL	0.23 + 0.028*CL	0.24 + 0.028*CL
	t_{PLZ}	1.17	1.17 + 0.000*CL	1.17 + 0.000*CL	1.17 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.95	1.54 + 0.028*CL	1.57 + 0.028*CL	1.57 + 0.028*CL
	t_F	3.20	0.42 + 0.056*CL	0.37 + 0.056*CL	0.35 + 0.056*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	3.13	1.71 + 0.028*CL	1.74 + 0.028*CL	1.75 + 0.028*CL
	t_F	3.20	0.42 + 0.056*CL	0.38 + 0.056*CL	0.34 + 0.057*CL
	t_{PLZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.82	1.73 + 0.022*CL	1.79 + 0.021*CL	1.81 + 0.021*CL
	t_F	2.57	0.61 + 0.039*CL	0.57 + 0.040*CL	0.57 + 0.040*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PHL}	2.99	1.90 + 0.022*CL	1.96 + 0.021*CL	1.99 + 0.021*CL
	t_F	2.57	0.62 + 0.039*CL	0.57 + 0.040*CL	0.56 + 0.040*CL
	t_{PLZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.64	1.70 + 0.019*CL	1.78 + 0.018*CL	1.83 + 0.017*CL
	t_F	2.27	0.74 + 0.031*CL	0.76 + 0.030*CL	0.72 + 0.031*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PHL}	2.82	1.88 + 0.019*CL	1.95 + 0.018*CL	2.00 + 0.017*CL
	t_F	2.27	0.75 + 0.030*CL	0.73 + 0.031*CL	0.74 + 0.031*CL
	t_{PLZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.66	1.77 + 0.018*CL	1.87 + 0.017*CL	1.91 + 0.016*CL
	t_F	2.18	0.82 + 0.027*CL	0.81 + 0.027*CL	0.84 + 0.027*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PHL}	2.83	1.94 + 0.018*CL	2.04 + 0.017*CL	2.08 + 0.016*CL
	t_F	2.18	0.84 + 0.027*CL	0.84 + 0.027*CL	0.86 + 0.027*CL
	t_{PLZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	4.80	1.08 + 0.074*CL	1.09 + 0.074*CL	1.08 + 0.074*CL
	t_F	7.89	0.16 + 0.155*CL	0.15 + 0.155*CL	0.16 + 0.155*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
EN to PAD	t_{PHL}	4.97	1.26 + 0.074*CL	1.25 + 0.074*CL	1.26 + 0.074*CL
	t_F	7.89	0.16 + 0.155*CL	0.15 + 0.155*CL	0.16 + 0.155*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.24	1.38 + 0.037*CL	1.38 + 0.037*CL	1.39 + 0.037*CL
	t_F	4.08	0.28 + 0.076*CL	0.25 + 0.076*CL	0.23 + 0.077*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
EN to PAD	t_{PHL}	3.41	1.55 + 0.037*CL	1.56 + 0.037*CL	1.56 + 0.037*CL
	t_F	4.08	0.28 + 0.076*CL	0.24 + 0.076*CL	0.23 + 0.077*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.75	1.37 + 0.028*CL	1.39 + 0.027*CL	1.40 + 0.027*CL
	t_F	3.11	0.37 + 0.055*CL	0.33 + 0.055*CL	0.30 + 0.056*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PHL}	2.92	1.54 + 0.028*CL	1.56 + 0.027*CL	1.57 + 0.027*CL
	t_F	3.11	0.36 + 0.055*CL	0.33 + 0.055*CL	0.30 + 0.056*CL
	t_{PLZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.49	1.43 + 0.021*CL	1.47 + 0.021*CL	1.50 + 0.020*CL
	t_F	2.48	0.52 + 0.039*CL	0.49 + 0.040*CL	0.46 + 0.040*CL
	t_{PLZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
EN to PAD	t_{PHL}	2.66	1.60 + 0.021*CL	1.65 + 0.021*CL	1.66 + 0.020*CL
	t_F	2.48	0.52 + 0.039*CL	0.51 + 0.039*CL	0.47 + 0.040*CL
	t_{PLZ}	0.86	0.86 + 0.000*CL	0.86 + 0.000*CL	0.86 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.35	1.45 + 0.018*CL	1.52 + 0.017*CL	1.55 + 0.017*CL
	t_F	2.16	0.62 + 0.031*CL	0.63 + 0.031*CL	0.61 + 0.031*CL
	t_{PLZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PHL}	2.52	1.62 + 0.018*CL	1.69 + 0.017*CL	1.72 + 0.017*CL
	t_F	2.16	0.64 + 0.031*CL	0.60 + 0.031*CL	0.61 + 0.031*CL
	t_{PLZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOD24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.37	1.51 + 0.017*CL	1.59 + 0.016*CL	1.63 + 0.016*CL
	t_F	2.08	0.72 + 0.027*CL	0.74 + 0.027*CL	0.74 + 0.027*CL
	t_{PLZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PHL}	2.54	1.68 + 0.017*CL	1.76 + 0.016*CL	1.81 + 0.016*CL
	t_F	2.08	0.73 + 0.027*CL	0.72 + 0.027*CL	0.74 + 0.027*CL
	t_{PLZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

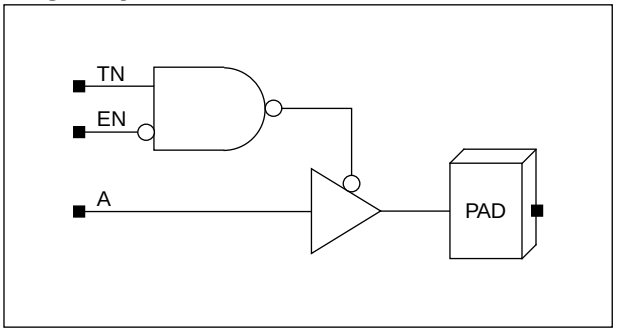
PvOTyz

Tri-State Output Buffers

Cell Availability

Library	5V Operation	3.3V Operation
KG80	POT(1/2/4/8/12/16/20/24) POT(12/16/20/24)SH POT(4/8/12/16/20/24)SM	PLOT(1/2/4/6/8/10/12/16) PLOT(4/6/8/10/12/16)SM
KGM80	PHOT(1/2/4/8/12/16/20/24) PHOT(12/16/20/24)SH PHOT(4/8/12/16/20/24)SM	POT(1/2/4/6/8/10/12/16) POT(4/6/8/10/12/16)SM

Logic Symbol



Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

I/O Slot

KG80/KGM80	
PvOTyz	1.0

Input Load (SL)

KG80			
	TN	EN	A
POT(1/2/4/8/12/16/20/24)	1.4	1.6	2.4
POT(12/16/20/24)SH	1.4	1.6	2.4
POT(4/8/12/16/20/24)SM	1.4	1.6	2.4
PLOT(1/2/4/6/8/10/12/16)	1.2	1.2	2.3
PLOT(4/6/8/10/12/16)SM	1.2	1.2	2.3
KGM80			
	TN	EN	A
POT(1/2/4/6/8/10/12/16)	1.8	1.8	2.6
POT(4/6/8/10/12/16)SM	1.8	1.8	2.6
PHOT(1/2/4/8/12/16/20/24)	1.4	1.4	2.8
PHOT(12/16/20/24)SH	1.4	1.4	2.8
PHOT(4/8/12/16/20/24)SM	1.4	1.4	2.8

KG80 POT1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	15.24	0.63 + 0.292*CL	0.63 + 0.292*CL	0.63 + 0.292*CL
	t_{PHL}	12.28	0.63 + 0.233*CL	0.63 + 0.233*CL	0.63 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.59 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
TN to PAD	t_{PLH}	15.23	0.73 + 0.290*CL	1.33 + 0.282*CL	2.49 + 0.268*CL
	t_{PHL}	12.30	0.65 + 0.233*CL	0.65 + 0.233*CL	0.65 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.60 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
	t_{PLZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
	t_{PHZ}	0.58	0.58 + 0.000*CL	0.58 + 0.000*CL	0.58 + 0.000*CL
EN to PAD	t_{PLH}	15.39	0.88 + 0.290*CL	1.49 + 0.282*CL	2.68 + 0.268*CL
	t_{PHL}	12.45	0.81 + 0.233*CL	0.81 + 0.233*CL	0.81 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.60 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
	t_{PLZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL
	t_{PHZ}	0.50	0.50 + 0.000*CL	0.50 + 0.000*CL	0.50 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	7.86	0.56 + 0.146*CL	0.55 + 0.146*CL	0.56 + 0.146*CL
	t_{PHL}	6.37	0.55 + 0.116*CL	0.55 + 0.116*CL	0.55 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.242*CL	0.21 + 0.243*CL
TN to PAD	t_{PLH}	7.86	0.55 + 0.146*CL	0.54 + 0.146*CL	0.56 + 0.146*CL
	t_{PHL}	6.39	0.57 + 0.116*CL	0.57 + 0.116*CL	0.57 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.242*CL	0.21 + 0.243*CL
	t_{PLZ}	0.69	0.69 + 0.000*CL	0.69 + 0.000*CL	0.69 + 0.000*CL
	t_{PHZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
EN to PAD	t_{PLH}	8.01	0.70 + 0.146*CL	0.71 + 0.146*CL	0.70 + 0.146*CL
	t_{PHL}	6.55	0.73 + 0.116*CL	0.72 + 0.117*CL	0.73 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.31 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.242*CL	0.21 + 0.243*CL
	t_{PLZ}	0.61	0.61 + 0.000*CL	0.61 + 0.000*CL	0.61 + 0.000*CL
	t_{PHZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.25	0.56 + 0.094*CL	0.56 + 0.094*CL	0.56 + 0.094*CL
	t_{PHL}	4.25	0.54 + 0.074*CL	0.54 + 0.074*CL	0.55 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
TN to PAD	t_{PLH}	5.24	0.55 + 0.094*CL	0.55 + 0.094*CL	0.55 + 0.094*CL
	t_{PHL}	4.27	0.56 + 0.074*CL	0.56 + 0.074*CL	0.57 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
	t_{PHZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL
EN to PAD	t_{PLH}	5.39	0.70 + 0.094*CL	0.70 + 0.094*CL	0.70 + 0.094*CL
	t_{PHL}	4.43	0.72 + 0.074*CL	0.71 + 0.074*CL	0.72 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.14 + 0.155*CL	0.15 + 0.155*CL	0.14 + 0.155*CL
	t_{PLZ}	0.67	0.67 + 0.000*CL	0.67 + 0.000*CL	0.67 + 0.000*CL
	t_{PHZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.96	0.62 + 0.047*CL	0.62 + 0.047*CL	0.62 + 0.047*CL
	t_{PHL}	2.45	0.60 + 0.037*CL	0.60 + 0.037*CL	0.60 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
TN to PAD	t_{PLH}	2.95	0.61 + 0.047*CL	0.61 + 0.047*CL	0.61 + 0.047*CL
	t_{PHL}	2.47	0.62 + 0.037*CL	0.61 + 0.037*CL	0.62 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
	t_{PLZ}	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + 0.000*CL
	t_{PHZ}	0.82	0.82 + 0.000*CL	0.82 + 0.000*CL	0.82 + 0.000*CL
EN to PAD	t_{PLH}	3.11	0.76 + 0.047*CL	0.76 + 0.047*CL	0.76 + 0.047*CL
	t_{PHL}	2.63	0.77 + 0.037*CL	0.77 + 0.037*CL	0.77 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.09 + 0.077*CL	0.09 + 0.077*CL
	t_{PLZ}	0.84	0.84 + 0.000*CL	0.83 + 0.000*CL	0.84 + 0.000*CL
	t_{PHZ}	0.74	0.74 + 0.000*CL	0.74 + 0.000*CL	0.74 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.41	0.68 + 0.035*CL	0.68 + 0.035*CL	0.68 + 0.035*CL
	t_{PHL}	2.02	0.66 + 0.027*CL	0.66 + 0.027*CL	0.66 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.09 + 0.057*CL
TN to PAD	t_{PLH}	2.39	0.66 + 0.035*CL	0.67 + 0.035*CL	0.66 + 0.035*CL
	t_{PHL}	2.03	0.67 + 0.027*CL	0.67 + 0.027*CL	0.67 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.09 + 0.057*CL
	t_{PLZ}	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL
	t_{PHZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
EN to PAD	t_{PLH}	2.54	0.82 + 0.035*CL	0.81 + 0.035*CL	0.82 + 0.035*CL
	t_{PHL}	2.19	0.82 + 0.027*CL	0.83 + 0.027*CL	0.83 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.12 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.10 + 0.057*CL	0.09 + 0.057*CL
	t_{PLZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
	t_{PHZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.84 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.03	0.78 + 0.025*CL	0.77 + 0.025*CL	0.77 + 0.025*CL
	t_{PHL}	1.74	0.75 + 0.020*CL	0.74 + 0.020*CL	0.74 + 0.020*CL
	t_R	2.97	0.13 + 0.057*CL	0.13 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.14 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
TN to PAD	t_{PLH}	2.01	0.75 + 0.025*CL	0.74 + 0.025*CL	0.75 + 0.025*CL
	t_{PHL}	1.75	0.75 + 0.020*CL	0.75 + 0.020*CL	0.75 + 0.020*CL
	t_R	2.97	0.14 + 0.057*CL	0.12 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.14 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
	t_{PLZ}	1.20	1.20 + 0.000*CL	1.20 + 0.000*CL	1.20 + 0.000*CL
	t_{PHZ}	1.07	1.07 + 0.000*CL	1.07 + 0.000*CL	1.07 + 0.000*CL
EN to PAD	t_{PLH}	2.16	0.90 + 0.025*CL	0.91 + 0.025*CL	0.90 + 0.025*CL
	t_{PHL}	1.90	0.91 + 0.020*CL	0.90 + 0.020*CL	0.91 + 0.020*CL
	t_R	2.97	0.14 + 0.057*CL	0.13 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.14 + 0.041*CL	0.13 + 0.041*CL	0.12 + 0.041*CL
	t_{PLZ}	1.12	1.12 + 0.000*CL	1.11 + 0.000*CL	1.12 + 0.000*CL
	t_{PHZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.66	0.67 + 0.020*CL	0.67 + 0.020*CL	0.66 + 0.020*CL
	t_{PHL}	1.51	0.72 + 0.016*CL	0.73 + 0.016*CL	0.72 + 0.016*CL
	t_R	2.33	0.09 + 0.045*CL	0.09 + 0.045*CL	0.08 + 0.045*CL
	t_F	1.74	0.13 + 0.032*CL	0.11 + 0.032*CL	0.11 + 0.032*CL
TN to PAD	t_{PLH}	1.65	0.65 + 0.020*CL	0.65 + 0.020*CL	0.65 + 0.020*CL
	t_{PHL}	1.52	0.73 + 0.016*CL	0.74 + 0.016*CL	0.73 + 0.016*CL
	t_R	2.33	0.10 + 0.045*CL	0.09 + 0.045*CL	0.08 + 0.045*CL
	t_F	1.74	0.13 + 0.032*CL	0.12 + 0.032*CL	0.11 + 0.032*CL
	t_{PLZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL
	t_{PHZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
EN to PAD	t_{PLH}	1.80	0.81 + 0.020*CL	0.81 + 0.020*CL	0.81 + 0.020*CL
	t_{PHL}	1.67	0.88 + 0.016*CL	0.89 + 0.016*CL	0.89 + 0.016*CL
	t_R	2.33	0.10 + 0.045*CL	0.09 + 0.045*CL	0.08 + 0.045*CL
	t_F	1.74	0.13 + 0.032*CL	0.12 + 0.032*CL	0.11 + 0.032*CL
	t_{PLZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
	t_{PHZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.59	0.72 + 0.017*CL	0.72 + 0.018*CL	0.72 + 0.018*CL
	t_{PHL}	1.45	0.75 + 0.014*CL	0.76 + 0.014*CL	0.75 + 0.014*CL
	t_R	2.07	0.11 + 0.039*CL	0.09 + 0.039*CL	0.09 + 0.039*CL
	t_F	1.56	0.15 + 0.028*CL	0.13 + 0.028*CL	0.13 + 0.028*CL
TN to PAD	t_{PLH}	1.58	0.70 + 0.018*CL	0.71 + 0.017*CL	0.70 + 0.018*CL
	t_{PHL}	1.46	0.76 + 0.014*CL	0.77 + 0.014*CL	0.77 + 0.014*CL
	t_R	2.07	0.11 + 0.039*CL	0.09 + 0.039*CL	0.09 + 0.039*CL
	t_F	1.56	0.15 + 0.028*CL	0.14 + 0.028*CL	0.13 + 0.028*CL
	t_{PLZ}	1.07	1.07 + 0.000*CL	1.06 + 0.000*CL	1.07 + 0.000*CL
	t_{PHZ}	0.97	0.97 + 0.000*CL	0.97 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PLH}	1.73	0.86 + 0.018*CL	0.86 + 0.018*CL	0.86 + 0.018*CL
	t_{PHL}	1.62	0.92 + 0.014*CL	0.92 + 0.014*CL	0.93 + 0.014*CL
	t_R	2.07	0.11 + 0.039*CL	0.09 + 0.039*CL	0.09 + 0.039*CL
	t_F	1.56	0.15 + 0.028*CL	0.14 + 0.028*CL	0.13 + 0.028*CL
	t_{PLZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
	t_{PHZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.17	1.39 + 0.036*CL	1.41 + 0.035*CL	1.42 + 0.035*CL
	t_{PHL}	3.66	2.06 + 0.032*CL	2.17 + 0.030*CL	2.23 + 0.030*CL
	t_R	4.34	0.49 + 0.077*CL	0.44 + 0.078*CL	0.43 + 0.078*CL
	t_F	3.73	0.96 + 0.055*CL	0.97 + 0.055*CL	0.98 + 0.055*CL
TN to PAD	t_{PLH}	3.12	1.34 + 0.036*CL	1.37 + 0.035*CL	1.37 + 0.035*CL
	t_{PHL}	3.67	2.07 + 0.032*CL	2.18 + 0.031*CL	2.24 + 0.030*CL
	t_R	4.34	0.49 + 0.077*CL	0.44 + 0.078*CL	0.43 + 0.078*CL
	t_F	3.74	0.98 + 0.055*CL	0.98 + 0.055*CL	0.98 + 0.055*CL
	t_{PLZ}	1.30	1.30 + 0.000*CL	1.30 + 0.000*CL	1.30 + 0.000*CL
	t_{PHZ}	1.09	1.09 + 0.000*CL	1.09 + 0.000*CL	1.09 + 0.000*CL
EN to PAD	t_{PLH}	3.28	1.50 + 0.036*CL	1.53 + 0.035*CL	1.53 + 0.035*CL
	t_{PHL}	3.82	2.22 + 0.032*CL	2.34 + 0.031*CL	2.39 + 0.030*CL
	t_R	4.34	0.49 + 0.077*CL	0.44 + 0.078*CL	0.43 + 0.078*CL
	t_F	3.74	0.98 + 0.055*CL	0.98 + 0.055*CL	0.98 + 0.055*CL
	t_{PLZ}	1.22	1.22 + 0.000*CL	1.22 + 0.000*CL	1.22 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.97	1.61 + 0.027*CL	1.68 + 0.026*CL	1.70 + 0.026*CL
	t_{PHL}	3.36	2.11 + 0.025*CL	2.21 + 0.024*CL	2.28 + 0.023*CL
	t_R	3.43	0.70 + 0.055*CL	0.68 + 0.055*CL	0.66 + 0.055*CL
	t_F	3.00	0.95 + 0.041*CL	1.01 + 0.040*CL	1.02 + 0.040*CL
TN to PAD	t_{PLH}	2.92	1.56 + 0.027*CL	1.63 + 0.026*CL	1.65 + 0.026*CL
	t_{PHL}	3.35	2.07 + 0.025*CL	2.21 + 0.024*CL	2.26 + 0.023*CL
	t_R	3.43	0.71 + 0.055*CL	0.68 + 0.055*CL	0.66 + 0.055*CL
	t_F	3.03	1.01 + 0.040*CL	1.05 + 0.040*CL	1.06 + 0.040*CL
	t_{PLZ}	1.27	1.27 + 0.000*CL	1.27 + 0.000*CL	1.27 + 0.000*CL
	t_{PHZ}	1.09	1.09 + 0.000*CL	1.09 + 0.000*CL	1.09 + 0.000*CL
EN to PAD	t_{PLH}	3.07	1.72 + 0.027*CL	1.78 + 0.026*CL	1.80 + 0.026*CL
	t_{PHL}	3.50	2.23 + 0.025*CL	2.36 + 0.024*CL	2.42 + 0.023*CL
	t_R	3.43	0.71 + 0.055*CL	0.68 + 0.055*CL	0.66 + 0.055*CL
	t_F	3.03	1.01 + 0.040*CL	1.05 + 0.040*CL	1.06 + 0.040*CL
	t_{PLZ}	1.19	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.36	1.30 + 0.021*CL	1.35 + 0.021*CL	1.36 + 0.020*CL
	t_{PHL}	2.38	1.52 + 0.017*CL	1.55 + 0.017*CL	1.57 + 0.017*CL
	t_R	2.71	0.57 + 0.043*CL	0.55 + 0.043*CL	0.53 + 0.043*CL
	t_F	2.23	0.71 + 0.030*CL	0.69 + 0.031*CL	0.68 + 0.031*CL
TN to PAD	t_{PLH}	2.31	1.25 + 0.021*CL	1.29 + 0.021*CL	1.32 + 0.020*CL
	t_{PHL}	2.29	1.35 + 0.019*CL	1.43 + 0.018*CL	1.47 + 0.017*CL
	t_R	2.72	0.59 + 0.043*CL	0.55 + 0.043*CL	0.54 + 0.043*CL
	t_F	2.22	0.67 + 0.031*CL	0.68 + 0.031*CL	0.67 + 0.031*CL
	t_{PLZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PLH}	2.47	1.41 + 0.021*CL	1.46 + 0.021*CL	1.47 + 0.020*CL
	t_{PHL}	2.44	1.51 + 0.019*CL	1.58 + 0.018*CL	1.63 + 0.017*CL
	t_R	2.72	0.59 + 0.043*CL	0.55 + 0.043*CL	0.54 + 0.043*CL
	t_F	2.22	0.67 + 0.031*CL	0.68 + 0.031*CL	0.67 + 0.031*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
	t_{PHZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.35	1.38 + 0.019*CL	1.44 + 0.019*CL	1.47 + 0.018*CL
	t_{PHL}	2.45	1.66 + 0.016*CL	1.69 + 0.015*CL	1.72 + 0.015*CL
	t_R	2.53	0.65 + 0.038*CL	0.64 + 0.038*CL	0.63 + 0.038*CL
	t_F	2.15	0.82 + 0.027*CL	0.81 + 0.027*CL	0.79 + 0.027*CL
TN to PAD	t_{PLH}	2.30	1.33 + 0.020*CL	1.39 + 0.019*CL	1.42 + 0.018*CL
	t_{PHL}	2.30	1.42 + 0.018*CL	1.52 + 0.016*CL	1.55 + 0.016*CL
	t_R	2.55	0.68 + 0.037*CL	0.66 + 0.038*CL	0.64 + 0.038*CL
	t_F	2.12	0.74 + 0.028*CL	0.77 + 0.027*CL	0.76 + 0.027*CL
	t_{PLZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.70 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PLH}	2.46	1.48 + 0.020*CL	1.54 + 0.019*CL	1.58 + 0.018*CL
	t_{PHL}	2.46	1.57 + 0.018*CL	1.67 + 0.016*CL	1.71 + 0.016*CL
	t_R	2.55	0.68 + 0.037*CL	0.66 + 0.037*CL	0.64 + 0.038*CL
	t_F	2.12	0.74 + 0.028*CL	0.77 + 0.027*CL	0.76 + 0.027*CL
	t_{PLZ}	0.62	0.62 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
	t_{PHZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.59	0.90 + 0.094*CL	0.90 + 0.094*CL	0.90 + 0.094*CL
	t_{PHL}	5.18	1.45 + 0.074*CL	1.46 + 0.074*CL	1.47 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.24 + 0.212*CL	0.23 + 0.212*CL
	t_F	8.06	0.42 + 0.153*CL	0.38 + 0.153*CL	0.35 + 0.154*CL
TN to PAD	t_{PLH}	5.55	0.85 + 0.094*CL	0.86 + 0.094*CL	0.86 + 0.094*CL
	t_{PHL}	5.19	1.47 + 0.074*CL	1.48 + 0.074*CL	1.49 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.24 + 0.212*CL	0.23 + 0.212*CL
	t_F	8.06	0.42 + 0.153*CL	0.38 + 0.153*CL	0.35 + 0.154*CL
	t_{PLZ}	1.33	1.33 + 0.000*CL	1.33 + 0.000*CL	1.33 + 0.000*CL
	t_{PHZ}	1.10	1.10 + 0.000*CL	1.10 + 0.000*CL	1.10 + 0.000*CL
EN to PAD	t_{PLH}	5.70	1.01 + 0.094*CL	1.01 + 0.094*CL	1.01 + 0.094*CL
	t_{PHL}	5.35	1.63 + 0.074*CL	1.64 + 0.074*CL	1.64 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.24 + 0.212*CL	0.23 + 0.212*CL
	t_F	8.06	0.42 + 0.153*CL	0.38 + 0.153*CL	0.35 + 0.154*CL
	t_{PLZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.55	1.20 + 0.047*CL	1.20 + 0.047*CL	1.21 + 0.047*CL
	t_{PHL}	3.79	1.83 + 0.039*CL	1.89 + 0.038*CL	1.93 + 0.038*CL
	t_R	5.57	0.34 + 0.105*CL	0.31 + 0.105*CL	0.28 + 0.105*CL
	t_F	4.46	0.74 + 0.074*CL	0.72 + 0.075*CL	0.69 + 0.075*CL
TN to PAD	t_{PLH}	3.51	1.16 + 0.047*CL	1.16 + 0.047*CL	1.16 + 0.047*CL
	t_{PHL}	3.80	1.84 + 0.039*CL	1.91 + 0.038*CL	1.94 + 0.038*CL
	t_R	5.57	0.34 + 0.105*CL	0.31 + 0.105*CL	0.28 + 0.105*CL
	t_F	4.47	0.74 + 0.074*CL	0.72 + 0.075*CL	0.70 + 0.075*CL
	t_{PLZ}	1.30	1.30 + 0.000*CL	1.30 + 0.000*CL	1.30 + 0.000*CL
	t_{PHZ}	1.09	1.09 + 0.000*CL	1.09 + 0.000*CL	1.09 + 0.000*CL
EN to PAD	t_{PLH}	3.66	1.31 + 0.047*CL	1.31 + 0.047*CL	1.32 + 0.047*CL
	t_{PHL}	3.96	1.99 + 0.039*CL	2.07 + 0.038*CL	2.10 + 0.038*CL
	t_R	5.57	0.34 + 0.105*CL	0.31 + 0.105*CL	0.28 + 0.105*CL
	t_F	4.47	0.74 + 0.074*CL	0.72 + 0.075*CL	0.70 + 0.075*CL
	t_{PLZ}	1.22	1.22 + 0.000*CL	1.22 + 0.000*CL	1.22 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.98	1.24 + 0.035*CL	1.25 + 0.035*CL	1.26 + 0.035*CL
	t_{PHL}	3.29	1.75 + 0.031*CL	1.85 + 0.029*CL	1.89 + 0.029*CL
	t_R	4.22	0.41 + 0.076*CL	0.37 + 0.077*CL	0.35 + 0.077*CL
	t_F	3.55	0.81 + 0.055*CL	0.82 + 0.055*CL	0.82 + 0.055*CL
TN to PAD	t_{PLH}	2.93	1.19 + 0.035*CL	1.20 + 0.035*CL	1.21 + 0.035*CL
	t_{PHL}	3.30	1.76 + 0.031*CL	1.86 + 0.030*CL	1.91 + 0.029*CL
	t_R	4.22	0.41 + 0.076*CL	0.37 + 0.077*CL	0.36 + 0.077*CL
	t_F	3.55	0.82 + 0.055*CL	0.83 + 0.055*CL	0.82 + 0.055*CL
	t_{PLZ}	1.54	1.54 + 0.000*CL	1.54 + 0.000*CL	1.54 + 0.000*CL
	t_{PHZ}	1.39	1.39 + 0.000*CL	1.39 + 0.000*CL	1.38 + 0.000*CL
EN to PAD	t_{PLH}	3.09	1.34 + 0.035*CL	1.36 + 0.035*CL	1.36 + 0.035*CL
	t_{PHL}	3.46	1.92 + 0.031*CL	2.02 + 0.030*CL	2.06 + 0.029*CL
	t_R	4.22	0.41 + 0.076*CL	0.37 + 0.077*CL	0.36 + 0.077*CL
	t_F	3.55	0.82 + 0.055*CL	0.83 + 0.055*CL	0.82 + 0.055*CL
	t_{PLZ}	1.46	1.45 + 0.000*CL	1.45 + 0.000*CL	1.45 + 0.000*CL
	t_{PHZ}	1.31	1.30 + 0.000*CL	1.31 + 0.000*CL	1.31 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.66	1.34 + 0.026*CL	1.38 + 0.026*CL	1.40 + 0.026*CL
	t_{PHL}	2.86	1.68 + 0.024*CL	1.76 + 0.022*CL	1.81 + 0.022*CL
	t_R	3.28	0.53 + 0.055*CL	0.51 + 0.055*CL	0.49 + 0.056*CL
	t_F	2.77	0.73 + 0.041*CL	0.77 + 0.040*CL	0.78 + 0.040*CL
TN to PAD	t_{PLH}	2.61	1.29 + 0.026*CL	1.33 + 0.026*CL	1.34 + 0.026*CL
	t_{PHL}	2.86	1.66 + 0.024*CL	1.76 + 0.023*CL	1.80 + 0.022*CL
	t_R	3.29	0.54 + 0.055*CL	0.51 + 0.055*CL	0.49 + 0.056*CL
	t_F	2.79	0.76 + 0.040*CL	0.79 + 0.040*CL	0.80 + 0.040*CL
	t_{PLZ}	1.72	1.72 + 0.000*CL	1.71 + 0.000*CL	1.72 + 0.000*CL
	t_{PHZ}	1.65	1.65 + 0.000*CL	1.64 + 0.000*CL	1.65 + 0.000*CL
EN to PAD	t_{PLH}	2.76	1.44 + 0.026*CL	1.49 + 0.026*CL	1.50 + 0.026*CL
	t_{PHL}	3.02	1.82 + 0.024*CL	1.91 + 0.023*CL	1.97 + 0.022*CL
	t_R	3.29	0.54 + 0.055*CL	0.51 + 0.055*CL	0.49 + 0.056*CL
	t_F	2.79	0.76 + 0.040*CL	0.79 + 0.040*CL	0.80 + 0.040*CL
	t_{PLZ}	1.64	1.64 + 0.000*CL	1.64 + 0.000*CL	1.63 + 0.000*CL
	t_{PHZ}	1.57	1.57 + 0.000*CL	1.57 + 0.000*CL	1.56 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.03	1.02 + 0.020*CL	1.04 + 0.020*CL	1.04 + 0.020*CL
	t_{PHL}	2.01	1.13 + 0.018*CL	1.18 + 0.017*CL	1.21 + 0.017*CL
	t_R	2.53	0.36 + 0.043*CL	0.33 + 0.044*CL	0.32 + 0.044*CL
	t_F	2.11	0.54 + 0.031*CL	0.55 + 0.031*CL	0.54 + 0.031*CL
TN to PAD	t_{PLH}	2.00	0.99 + 0.020*CL	1.01 + 0.020*CL	1.01 + 0.020*CL
	t_{PHL}	2.01	1.11 + 0.018*CL	1.17 + 0.017*CL	1.21 + 0.017*CL
	t_R	2.53	0.37 + 0.043*CL	0.34 + 0.044*CL	0.32 + 0.044*CL
	t_F	2.12	0.57 + 0.031*CL	0.57 + 0.031*CL	0.57 + 0.031*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.78 + 0.000*CL
EN to PAD	t_{PLH}	2.16	1.14 + 0.020*CL	1.16 + 0.020*CL	1.17 + 0.020*CL
	t_{PHL}	2.17	1.27 + 0.018*CL	1.33 + 0.017*CL	1.37 + 0.017*CL
	t_R	2.53	0.37 + 0.043*CL	0.34 + 0.044*CL	0.32 + 0.044*CL
	t_F	2.12	0.57 + 0.031*CL	0.57 + 0.031*CL	0.57 + 0.031*CL
	t_{PLZ}	0.79	0.79 + 0.000*CL	0.78 + 0.000*CL	0.79 + 0.000*CL
	t_{PHZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 POT24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.01	1.10 + 0.018*CL	1.12 + 0.018*CL	1.14 + 0.018*CL
	t_{PHL}	2.04	1.21 + 0.017*CL	1.27 + 0.016*CL	1.31 + 0.015*CL
	t_R	2.33	0.44 + 0.038*CL	0.42 + 0.038*CL	0.40 + 0.038*CL
	t_F	2.01	0.62 + 0.028*CL	0.64 + 0.028*CL	0.64 + 0.027*CL
TN to PAD	t_{PLH}	1.98	1.06 + 0.018*CL	1.10 + 0.018*CL	1.10 + 0.018*CL
	t_{PHL}	2.03	1.17 + 0.017*CL	1.25 + 0.016*CL	1.29 + 0.016*CL
	t_R	2.34	0.46 + 0.038*CL	0.43 + 0.038*CL	0.41 + 0.038*CL
	t_F	2.04	0.66 + 0.027*CL	0.67 + 0.027*CL	0.68 + 0.027*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL
EN to PAD	t_{PLH}	2.13	1.21 + 0.018*CL	1.25 + 0.018*CL	1.26 + 0.018*CL
	t_{PHL}	2.18	1.33 + 0.017*CL	1.41 + 0.016*CL	1.45 + 0.016*CL
	t_R	2.34	0.46 + 0.038*CL	0.43 + 0.038*CL	0.41 + 0.038*CL
	t_F	2.04	0.66 + 0.027*CL	0.67 + 0.027*CL	0.68 + 0.027*CL
	t_{PLZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL
	t_{PHZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	21.62	1.17 + 0.409*CL	1.17 + 0.409*CL	1.17 + 0.409*CL
	t_{PHL}	14.16	0.96 + 0.264*CL	0.96 + 0.264*CL	0.96 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
TN to PAD	t_{PLH}	21.41	1.49 + 0.398*CL	3.49 + 0.372*CL	6.57 + 0.335*CL
	t_{PHL}	14.16	0.96 + 0.264*CL	0.96 + 0.264*CL	0.96 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL
	t_{PHZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
EN to PAD	t_{PLH}	21.52	1.61 + 0.398*CL	3.63 + 0.371*CL	6.73 + 0.335*CL
	t_{PHL}	14.29	1.09 + 0.264*CL	1.08 + 0.264*CL	1.08 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.98	0.93 + 0.001*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
	t_{PHZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	10.70	1.05 + 0.193*CL	1.05 + 0.193*CL	1.05 + 0.193*CL
	t_{PHL}	7.04	0.87 + 0.124*CL	0.87 + 0.124*CL	0.87 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
TN to PAD	t_{PLH}	10.50	0.85 + 0.193*CL	0.85 + 0.193*CL	0.87 + 0.193*CL
	t_{PHL}	7.05	0.87 + 0.124*CL	0.87 + 0.124*CL	0.87 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + 0.000*CL
	t_{PHZ}	1.06	1.06 + 0.000*CL	1.05 + 0.000*CL	1.06 + 0.000*CL
EN to PAD	t_{PLH}	10.63	1.02 + 0.192*CL	0.84 + 0.195*CL	1.10 + 0.192*CL
	t_{PHL}	7.17	1.00 + 0.124*CL	1.00 + 0.124*CL	0.99 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + 0.000*CL
	t_{PHZ}	1.02	1.05 + -0.001*CL	0.88 + 0.002*CL	1.02 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.81	0.98 + 0.096*CL	0.98 + 0.097*CL	0.98 + 0.096*CL
	t_{PHL}	4.00	0.92 + 0.062*CL	0.91 + 0.062*CL	0.91 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.16 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
TN to PAD	t_{PLH}	5.60	0.78 + 0.096*CL	0.78 + 0.096*CL	0.78 + 0.096*CL
	t_{PHL}	4.00	0.92 + 0.062*CL	0.91 + 0.062*CL	0.92 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.15 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
	t_{PHZ}	1.70	1.70 + 0.000*CL	1.70 + 0.000*CL	1.70 + 0.000*CL
EN to PAD	t_{PLH}	5.72	0.90 + 0.096*CL	0.90 + 0.097*CL	0.90 + 0.096*CL
	t_{PHL}	4.14	1.06 + 0.062*CL	1.05 + 0.062*CL	1.06 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.15 + 0.133*CL	0.14 + 0.133*CL	0.16 + 0.133*CL
	t_{PLZ}	1.19	1.19 + 0.000*CL	1.14 + 0.001*CL	1.19 + 0.000*CL
	t_{PHZ}	1.65	1.65 + 0.000*CL	1.72 + -0.001*CL	1.64 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.26	1.04 + 0.064*CL	1.04 + 0.064*CL	1.05 + 0.064*CL
	t_{PHL}	3.07	1.02 + 0.041*CL	1.01 + 0.041*CL	1.01 + 0.041*CL
	t_R	7.52	0.20 + 0.146*CL	0.19 + 0.146*CL	0.20 + 0.146*CL
	t_F	4.58	0.17 + 0.088*CL	0.14 + 0.089*CL	0.14 + 0.089*CL
TN to PAD	t_{PLH}	4.05	0.84 + 0.064*CL	0.82 + 0.064*CL	0.85 + 0.064*CL
	t_{PHL}	3.05	0.99 + 0.041*CL	0.99 + 0.041*CL	0.99 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.19 + 0.146*CL	0.20 + 0.146*CL
	t_F	4.57	0.14 + 0.089*CL	0.12 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	1.40	1.40 + 0.000*CL	1.54 + -0.002*CL	1.38 + 0.000*CL
	t_{PHZ}	2.09	2.09 + 0.000*CL	2.09 + 0.000*CL	2.09 + 0.000*CL
EN to PAD	t_{PLH}	4.17	0.95 + 0.064*CL	0.94 + 0.064*CL	0.96 + 0.064*CL
	t_{PHL}	3.19	1.13 + 0.041*CL	1.13 + 0.041*CL	1.14 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.19 + 0.147*CL	0.20 + 0.146*CL
	t_F	4.57	0.14 + 0.089*CL	0.14 + 0.089*CL	0.12 + 0.089*CL
	t_{PLZ}	1.35	1.41 + -0.001*CL	1.32 + 0.000*CL	1.32 + 0.000*CL
	t_{PHZ}	2.02	2.02 + 0.000*CL	2.02 + 0.000*CL	2.02 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.52	1.11 + 0.048*CL	1.11 + 0.048*CL	1.11 + 0.048*CL
	t_{PHL}	2.67	1.15 + 0.030*CL	1.14 + 0.031*CL	1.13 + 0.031*CL
	t_R	5.66	0.18 + 0.110*CL	0.16 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.51	0.24 + 0.065*CL	0.20 + 0.066*CL	0.18 + 0.066*CL
TN to PAD	t_{PLH}	3.32	0.90 + 0.048*CL	0.89 + 0.048*CL	0.92 + 0.048*CL
	t_{PHL}	2.62	1.08 + 0.031*CL	1.08 + 0.031*CL	1.08 + 0.031*CL
	t_R	5.66	0.18 + 0.110*CL	0.17 + 0.110*CL	0.16 + 0.110*CL
	t_F	3.47	0.17 + 0.066*CL	0.15 + 0.066*CL	0.14 + 0.066*CL
	t_{PLZ}	1.51	1.47 + 0.001*CL	1.68 + -0.002*CL	1.40 + 0.001*CL
	t_{PHZ}	2.48	2.47 + 0.000*CL	2.48 + 0.000*CL	2.48 + 0.000*CL
EN to PAD	t_{PLH}	3.45	1.07 + 0.048*CL	0.89 + 0.050*CL	1.14 + 0.047*CL
	t_{PHL}	2.77	1.22 + 0.031*CL	1.22 + 0.031*CL	1.22 + 0.031*CL
	t_R	5.66	0.18 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.47	0.17 + 0.066*CL	0.14 + 0.066*CL	0.15 + 0.066*CL
	t_{PLZ}	1.45	1.45 + 0.000*CL	1.44 + 0.000*CL	1.31 + 0.002*CL
	t_{PHZ}	2.41	2.41 + 0.000*CL	2.41 + 0.000*CL	2.40 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.16	1.23 + 0.039*CL	1.23 + 0.039*CL	1.23 + 0.039*CL
	t_{PHL}	2.41	1.18 + 0.025*CL	1.17 + 0.025*CL	1.18 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.83	0.21 + 0.052*CL	0.17 + 0.053*CL	0.20 + 0.053*CL
TN to PAD	t_{PLH}	2.95	1.01 + 0.039*CL	1.02 + 0.039*CL	0.99 + 0.039*CL
	t_{PHL}	2.40	1.16 + 0.025*CL	1.18 + 0.025*CL	1.17 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.84	0.23 + 0.052*CL	0.18 + 0.053*CL	0.20 + 0.053*CL
	t_{PLZ}	1.65	1.68 + -0.001*CL	1.55 + 0.001*CL	1.72 + -0.001*CL
	t_{PHZ}	1.88	1.88 + 0.000*CL	1.88 + 0.000*CL	1.88 + 0.000*CL
EN to PAD	t_{PLH}	3.07	1.13 + 0.039*CL	1.14 + 0.039*CL	1.13 + 0.039*CL
	t_{PHL}	2.55	1.31 + 0.025*CL	1.30 + 0.025*CL	1.31 + 0.025*CL
	t_R	4.56	0.19 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.83	0.21 + 0.052*CL	0.21 + 0.052*CL	0.17 + 0.053*CL
	t_{PLZ}	1.57	1.53 + 0.001*CL	1.77 + -0.002*CL	1.57 + 0.000*CL
	t_{PHZ}	1.82	1.82 + 0.000*CL	1.82 + 0.000*CL	1.82 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.95	1.34 + 0.032*CL	1.34 + 0.032*CL	1.34 + 0.032*CL
	t_{PHL}	2.28	1.24 + 0.021*CL	1.25 + 0.021*CL	1.25 + 0.021*CL
	t_R	3.84	0.21 + 0.073*CL	0.20 + 0.073*CL	0.16 + 0.073*CL
	t_F	2.43	0.26 + 0.043*CL	0.26 + 0.043*CL	0.22 + 0.044*CL
TN to PAD	t_{PLH}	2.74	1.12 + 0.032*CL	1.13 + 0.032*CL	1.14 + 0.032*CL
	t_{PHL}	2.28	1.24 + 0.021*CL	1.26 + 0.021*CL	1.26 + 0.021*CL
	t_R	3.84	0.21 + 0.073*CL	0.18 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.27 + 0.043*CL	0.25 + 0.043*CL	0.24 + 0.044*CL
	t_{PLZ}	1.76	1.74 + 0.000*CL	1.77 + 0.000*CL	1.76 + 0.000*CL
	t_{PHZ}	1.69	1.69 + 0.000*CL	1.69 + 0.000*CL	1.69 + 0.000*CL
EN to PAD	t_{PLH}	2.86	1.25 + 0.032*CL	1.13 + 0.034*CL	1.36 + 0.031*CL
	t_{PHL}	2.40	1.37 + 0.021*CL	1.37 + 0.021*CL	1.37 + 0.021*CL
	t_R	3.84	0.20 + 0.073*CL	0.19 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.26 + 0.043*CL	0.26 + 0.043*CL	0.22 + 0.044*CL
	t_{PLZ}	1.73	1.72 + 0.000*CL	1.72 + 0.000*CL	1.85 + -0.002*CL
	t_{PHZ}	1.63	1.63 + 0.000*CL	1.63 + 0.000*CL	1.63 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.71	1.49 + 0.024*CL	1.49 + 0.024*CL	1.49 + 0.024*CL
	t_{PHL}	2.20	1.38 + 0.016*CL	1.40 + 0.016*CL	1.41 + 0.016*CL
	t_R	3.00	0.26 + 0.055*CL	0.24 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.98	0.36 + 0.032*CL	0.38 + 0.032*CL	0.31 + 0.033*CL
TN to PAD	t_{PLH}	2.49	1.26 + 0.025*CL	1.26 + 0.025*CL	1.26 + 0.025*CL
	t_{PHL}	2.19	1.37 + 0.016*CL	1.40 + 0.016*CL	1.40 + 0.016*CL
	t_R	3.01	0.27 + 0.055*CL	0.27 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.99	0.36 + 0.032*CL	0.38 + 0.032*CL	0.35 + 0.033*CL
	t_{PLZ}	2.01	1.99 + 0.000*CL	2.00 + 0.000*CL	2.00 + 0.000*CL
	t_{PHZ}	1.94	1.93 + 0.000*CL	1.93 + 0.000*CL	1.93 + 0.000*CL
EN to PAD	t_{PLH}	2.61	1.38 + 0.025*CL	1.38 + 0.025*CL	1.39 + 0.025*CL
	t_{PHL}	2.31	1.49 + 0.016*CL	1.52 + 0.016*CL	1.53 + 0.016*CL
	t_R	3.01	0.28 + 0.055*CL	0.23 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.99	0.37 + 0.032*CL	0.32 + 0.033*CL	0.35 + 0.033*CL
	t_{PLZ}	1.96	1.99 + -0.001*CL	1.94 + 0.000*CL	1.81 + 0.002*CL
	t_{PHZ}	1.88	1.87 + 0.000*CL	1.87 + 0.000*CL	1.87 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	6.25	1.28 + 0.099*CL	1.28 + 0.099*CL	1.28 + 0.099*CL
	t_{PHL}	4.52	1.33 + 0.064*CL	1.33 + 0.064*CL	1.33 + 0.064*CL
	t_R	11.58	0.27 + 0.226*CL	0.27 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL
TN to PAD	t_{PLH}	6.03	1.06 + 0.099*CL	1.06 + 0.099*CL	1.06 + 0.099*CL
	t_{PHL}	4.53	1.34 + 0.064*CL	1.34 + 0.064*CL	1.34 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.27 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.23 + 0.137*CL
	t_{PLZ}	1.19	1.16 + 0.001*CL	1.20 + 0.000*CL	1.20 + 0.000*CL
	t_{PHZ}	1.09	1.09 + 0.000*CL	1.09 + 0.000*CL	1.09 + 0.000*CL
EN to PAD	t_{PLH}	6.15	1.18 + 0.099*CL	1.18 + 0.099*CL	1.18 + 0.099*CL
	t_{PHL}	4.67	1.48 + 0.064*CL	1.47 + 0.064*CL	1.48 + 0.064*CL
	t_R	11.58	0.27 + 0.226*CL	0.27 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.26 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	1.15	1.20 + -0.001*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
	t_{PHZ}	1.03	1.03 + 0.000*CL	1.03 + 0.000*CL	1.03 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.76	1.48 + 0.066*CL	1.48 + 0.066*CL	1.48 + 0.066*CL
	t_{PHL}	3.76	1.65 + 0.042*CL	1.66 + 0.042*CL	1.67 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.24 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.41 + 0.089*CL	0.37 + 0.089*CL
TN to PAD	t_{PLH}	4.53	1.25 + 0.066*CL	1.25 + 0.066*CL	1.25 + 0.066*CL
	t_{PHL}	3.77	1.65 + 0.042*CL	1.66 + 0.042*CL	1.68 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.25 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.47 + 0.088*CL	0.41 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	1.14	1.14 + 0.000*CL	1.14 + 0.000*CL	1.14 + 0.000*CL
	t_{PHZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + 0.000*CL
EN to PAD	t_{PLH}	4.65	1.37 + 0.066*CL	1.37 + 0.066*CL	1.37 + 0.066*CL
	t_{PHL}	3.89	1.78 + 0.042*CL	1.78 + 0.042*CL	1.79 + 0.042*CL
	t_R	7.71	0.27 + 0.149*CL	0.24 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.40 + 0.089*CL	0.39 + 0.089*CL
	t_{PLZ}	1.09	1.09 + 0.000*CL	1.26 + -0.002*CL	1.06 + 0.000*CL
	t_{PHZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.10	1.65 + 0.049*CL	1.65 + 0.049*CL	1.66 + 0.049*CL
	t_{PHL}	3.55	1.92 + 0.033*CL	1.97 + 0.032*CL	1.99 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.29 + 0.111*CL	0.28 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.64 + 0.065*CL	0.58 + 0.066*CL
TN to PAD	t_{PLH}	3.88	1.42 + 0.049*CL	1.43 + 0.049*CL	1.43 + 0.049*CL
	t_{PHL}	3.56	1.92 + 0.033*CL	1.97 + 0.032*CL	1.99 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.30 + 0.111*CL	0.29 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.67 + 0.065*CL	0.60 + 0.066*CL
	t_{PLZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
	t_{PHZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + 0.000*CL
EN to PAD	t_{PLH}	3.99	1.54 + 0.049*CL	1.55 + 0.049*CL	1.55 + 0.049*CL
	t_{PHL}	3.68	2.04 + 0.033*CL	2.09 + 0.032*CL	2.11 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.30 + 0.111*CL	0.29 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.64 + 0.065*CL	0.61 + 0.065*CL
	t_{PLZ}	1.09	1.14 + -0.001*CL	1.07 + 0.000*CL	1.07 + 0.000*CL
	t_{PHZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.57	1.64 + 0.039*CL	1.64 + 0.039*CL	1.65 + 0.039*CL
	t_{PHL}	3.21	1.86 + 0.027*CL	1.94 + 0.026*CL	1.97 + 0.026*CL
	t_R	4.71	0.40 + 0.086*CL	0.34 + 0.087*CL	0.34 + 0.087*CL
	t_F	3.35	0.86 + 0.050*CL	0.85 + 0.050*CL	0.78 + 0.051*CL
TN to PAD	t_{PLH}	3.35	1.41 + 0.039*CL	1.43 + 0.039*CL	1.41 + 0.039*CL
	t_{PHL}	3.21	1.85 + 0.027*CL	1.93 + 0.026*CL	1.97 + 0.026*CL
	t_R	4.70	0.39 + 0.086*CL	0.35 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.35	0.87 + 0.050*CL	0.85 + 0.050*CL	0.80 + 0.051*CL
	t_{PLZ}	1.26	1.24 + 0.000*CL	1.27 + 0.000*CL	1.27 + 0.000*CL
	t_{PHZ}	1.19	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
EN to PAD	t_{PLH}	3.46	1.53 + 0.039*CL	1.53 + 0.039*CL	1.53 + 0.039*CL
	t_{PHL}	3.33	1.97 + 0.027*CL	2.06 + 0.026*CL	2.09 + 0.026*CL
	t_R	4.70	0.40 + 0.086*CL	0.35 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.35	0.88 + 0.050*CL	0.85 + 0.050*CL	0.80 + 0.050*CL
	t_{PLZ}	1.23	1.28 + -0.001*CL	1.01 + 0.003*CL	1.38 + -0.002*CL
	t_{PHZ}	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.42	1.79 + 0.033*CL	1.80 + 0.032*CL	1.82 + 0.032*CL
	t_{PHL}	3.25	2.02 + 0.025*CL	2.13 + 0.023*CL	2.19 + 0.022*CL
	t_R	4.06	0.50 + 0.071*CL	0.46 + 0.072*CL	0.43 + 0.072*CL
	t_F	3.10	1.03 + 0.041*CL	1.03 + 0.041*CL	1.02 + 0.041*CL
TN to PAD	t_{PLH}	3.19	1.56 + 0.033*CL	1.56 + 0.033*CL	1.60 + 0.032*CL
	t_{PHL}	3.24	2.00 + 0.025*CL	2.12 + 0.023*CL	2.17 + 0.023*CL
	t_R	4.06	0.52 + 0.071*CL	0.44 + 0.072*CL	0.45 + 0.072*CL
	t_F	3.12	1.08 + 0.041*CL	1.07 + 0.041*CL	1.04 + 0.041*CL
	t_{PLZ}	1.27	1.27 + 0.000*CL	1.27 + 0.000*CL	1.27 + 0.000*CL
	t_{PHZ}	1.19	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
EN to PAD	t_{PLH}	3.31	1.68 + 0.033*CL	1.69 + 0.032*CL	1.71 + 0.032*CL
	t_{PHL}	3.36	2.12 + 0.025*CL	2.24 + 0.023*CL	2.30 + 0.023*CL
	t_R	4.06	0.51 + 0.071*CL	0.47 + 0.072*CL	0.43 + 0.072*CL
	t_F	3.11	1.07 + 0.041*CL	1.04 + 0.041*CL	1.04 + 0.041*CL
	t_{PLZ}	1.23	1.28 + -0.001*CL	1.20 + 0.000*CL	1.06 + 0.002*CL
	t_{PHZ}	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PLOT16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V*, 5.0V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.35	2.06 + 0.026*CL	2.11 + 0.025*CL	2.13 + 0.025*CL
	t_{PHL}	3.43	2.31 + 0.022*CL	2.45 + 0.020*CL	2.53 + 0.020*CL
	t_R	3.38	0.74 + 0.053*CL	0.69 + 0.053*CL	0.64 + 0.054*CL
	t_F	2.88	1.25 + 0.033*CL	1.31 + 0.032*CL	1.29 + 0.032*CL
TN to PAD	t_{PLH}	3.11	1.82 + 0.026*CL	1.86 + 0.025*CL	1.90 + 0.025*CL
	t_{PHL}	3.40	2.26 + 0.023*CL	2.42 + 0.021*CL	2.50 + 0.020*CL
	t_R	3.39	0.76 + 0.053*CL	0.71 + 0.053*CL	0.68 + 0.054*CL
	t_F	2.94	1.37 + 0.031*CL	1.40 + 0.031*CL	1.38 + 0.031*CL
	t_{PLZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.17 + 0.001*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL
EN to PAD	t_{PLH}	3.23	1.93 + 0.026*CL	1.98 + 0.025*CL	2.01 + 0.025*CL
	t_{PHL}	3.52	2.38 + 0.023*CL	2.54 + 0.021*CL	2.63 + 0.020*CL
	t_R	3.38	0.76 + 0.053*CL	0.70 + 0.053*CL	0.67 + 0.054*CL
	t_F	2.94	1.36 + 0.032*CL	1.40 + 0.031*CL	1.38 + 0.031*CL
	t_{PLZ}	1.20	1.19 + 0.000*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
	t_{PHZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	21.36	0.92 + 0.409*CL	0.92 + 0.409*CL	0.92 + 0.409*CL
	t_{PHL}	14.04	0.84 + 0.264*CL	0.84 + 0.264*CL	0.84 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
TN to PAD	t_{PLH}	21.33	1.42 + 0.398*CL	3.44 + 0.371*CL	6.52 + 0.335*CL
	t_{PHL}	14.08	0.88 + 0.264*CL	0.88 + 0.264*CL	0.88 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.86	0.86 + 0.000*CL	0.86 + 0.000*CL	0.86 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL
EN to PAD	t_{PLH}	21.52	1.61 + 0.398*CL	3.67 + 0.371*CL	6.79 + 0.334*CL
	t_{PHL}	14.28	1.08 + 0.264*CL	1.08 + 0.264*CL	1.08 + 0.264*CL
	t_R	47.48	0.91 + 0.931*CL	0.91 + 0.931*CL	0.91 + 0.931*CL
	t_F	28.97	0.52 + 0.569*CL	0.51 + 0.569*CL	0.52 + 0.569*CL
	t_{PLZ}	0.77	0.77 + 0.000*CL	0.76 + 0.000*CL	0.76 + 0.000*CL
	t_{PHZ}	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	10.45	0.80 + 0.193*CL	0.80 + 0.193*CL	0.80 + 0.193*CL
	t_{PHL}	6.93	0.75 + 0.124*CL	0.75 + 0.124*CL	0.75 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
TN to PAD	t_{PLH}	10.43	0.78 + 0.193*CL	0.78 + 0.193*CL	0.79 + 0.193*CL
	t_{PHL}	6.97	0.79 + 0.124*CL	0.80 + 0.123*CL	0.79 + 0.124*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL
	t_{PHZ}	0.86	0.86 + 0.000*CL	0.86 + 0.000*CL	0.86 + 0.000*CL
EN to PAD	t_{PLH}	10.62	0.97 + 0.193*CL	0.97 + 0.193*CL	0.99 + 0.193*CL
	t_{PHL}	7.16	0.99 + 0.124*CL	0.98 + 0.124*CL	0.99 + 0.123*CL
	t_R	22.42	0.45 + 0.439*CL	0.45 + 0.439*CL	0.45 + 0.439*CL
	t_F	13.57	0.26 + 0.266*CL	0.26 + 0.266*CL	0.26 + 0.266*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.78 + 0.000*CL	0.79 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.55	0.72 + 0.097*CL	0.73 + 0.096*CL	0.73 + 0.096*CL
	t_{PHL}	3.89	0.80 + 0.062*CL	0.80 + 0.062*CL	0.80 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.16 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
TN to PAD	t_{PLH}	5.53	0.71 + 0.096*CL	0.71 + 0.097*CL	0.71 + 0.097*CL
	t_{PHL}	3.92	0.83 + 0.062*CL	0.83 + 0.062*CL	0.83 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.15 + 0.133*CL	0.15 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	1.08	1.07 + 0.000*CL	1.08 + 0.000*CL	1.06 + 0.000*CL
	t_{PHZ}	1.52	1.50 + 0.000*CL	1.51 + 0.000*CL	1.51 + 0.000*CL
EN to PAD	t_{PLH}	5.72	0.89 + 0.097*CL	0.89 + 0.097*CL	0.89 + 0.097*CL
	t_{PHL}	4.11	1.02 + 0.062*CL	1.02 + 0.062*CL	1.03 + 0.062*CL
	t_R	11.24	0.25 + 0.220*CL	0.25 + 0.220*CL	0.25 + 0.220*CL
	t_F	6.81	0.15 + 0.133*CL	0.16 + 0.133*CL	0.15 + 0.133*CL
	t_{PLZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
	t_{PHZ}	1.40	1.40 + 0.000*CL	1.40 + 0.000*CL	1.40 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.00	0.79 + 0.064*CL	0.79 + 0.064*CL	0.78 + 0.064*CL
	t_{PHL}	2.95	0.91 + 0.041*CL	0.90 + 0.041*CL	0.90 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.20 + 0.146*CL	0.20 + 0.146*CL
	t_F	4.58	0.16 + 0.088*CL	0.15 + 0.089*CL	0.13 + 0.089*CL
TN to PAD	t_{PLH}	3.98	0.77 + 0.064*CL	0.76 + 0.064*CL	0.77 + 0.064*CL
	t_{PHL}	2.97	0.91 + 0.041*CL	0.91 + 0.041*CL	0.91 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.19 + 0.147*CL	0.20 + 0.146*CL
	t_F	4.57	0.14 + 0.089*CL	0.13 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	1.21	1.21 + 0.000*CL	1.21 + 0.000*CL	1.20 + 0.000*CL
	t_{PHZ}	1.89	1.89 + 0.000*CL	1.89 + 0.000*CL	1.89 + 0.000*CL
EN to PAD	t_{PLH}	4.17	0.95 + 0.064*CL	0.95 + 0.064*CL	0.95 + 0.064*CL
	t_{PHL}	3.16	1.10 + 0.041*CL	1.10 + 0.041*CL	1.11 + 0.041*CL
	t_R	7.52	0.19 + 0.146*CL	0.20 + 0.146*CL	0.19 + 0.146*CL
	t_F	4.57	0.14 + 0.089*CL	0.14 + 0.089*CL	0.13 + 0.089*CL
	t_{PLZ}	1.13	1.18 + -0.001*CL	1.11 + 0.000*CL	1.11 + 0.000*CL
	t_{PHZ}	1.79	1.78 + 0.000*CL	1.78 + 0.000*CL	1.78 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.27	0.86 + 0.048*CL	0.85 + 0.048*CL	0.86 + 0.048*CL
	t_{PHL}	2.55	1.04 + 0.030*CL	1.02 + 0.031*CL	1.01 + 0.031*CL
	t_R	5.66	0.17 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.51	0.25 + 0.065*CL	0.20 + 0.066*CL	0.18 + 0.066*CL
TN to PAD	t_{PLH}	3.25	0.83 + 0.048*CL	0.83 + 0.048*CL	0.83 + 0.048*CL
	t_{PHL}	2.54	1.00 + 0.031*CL	0.99 + 0.031*CL	1.00 + 0.031*CL
	t_R	5.66	0.17 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.47	0.17 + 0.066*CL	0.15 + 0.066*CL	0.15 + 0.066*CL
	t_{PLZ}	1.33	1.32 + 0.000*CL	1.39 + -0.001*CL	1.33 + 0.000*CL
	t_{PHZ}	2.28	2.28 + 0.000*CL	2.28 + 0.000*CL	2.28 + 0.000*CL
EN to PAD	t_{PLH}	3.43	1.02 + 0.048*CL	1.02 + 0.048*CL	1.02 + 0.048*CL
	t_{PHL}	2.73	1.18 + 0.031*CL	1.19 + 0.031*CL	1.18 + 0.031*CL
	t_R	5.66	0.17 + 0.110*CL	0.17 + 0.110*CL	0.17 + 0.110*CL
	t_F	3.47	0.17 + 0.066*CL	0.16 + 0.066*CL	0.14 + 0.066*CL
	t_{PLZ}	1.24	1.24 + 0.000*CL	1.24 + 0.000*CL	1.24 + 0.000*CL
	t_{PHZ}	2.17	2.17 + 0.000*CL	2.17 + 0.000*CL	2.17 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT10 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.90	0.97 + 0.039*CL	0.97 + 0.039*CL	0.97 + 0.039*CL
	t_{PHL}	2.29	1.06 + 0.025*CL	1.05 + 0.025*CL	1.06 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.18 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.83	0.22 + 0.052*CL	0.17 + 0.053*CL	0.19 + 0.053*CL
TN to PAD	t_{PLH}	2.88	0.95 + 0.039*CL	0.94 + 0.039*CL	0.95 + 0.039*CL
	t_{PHL}	2.32	1.08 + 0.025*CL	1.09 + 0.025*CL	1.09 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.17 + 0.088*CL	0.16 + 0.088*CL
	t_F	2.84	0.22 + 0.052*CL	0.18 + 0.053*CL	0.19 + 0.053*CL
	t_{PLZ}	1.46	1.46 + 0.000*CL	1.44 + 0.000*CL	1.45 + 0.000*CL
	t_{PHZ}	1.69	1.69 + 0.000*CL	1.69 + 0.000*CL	1.69 + 0.000*CL
EN to PAD	t_{PLH}	3.07	1.14 + 0.039*CL	1.13 + 0.039*CL	1.14 + 0.039*CL
	t_{PHL}	2.51	1.28 + 0.025*CL	1.28 + 0.025*CL	1.28 + 0.025*CL
	t_R	4.56	0.18 + 0.088*CL	0.16 + 0.088*CL	0.17 + 0.088*CL
	t_F	2.83	0.22 + 0.052*CL	0.19 + 0.053*CL	0.18 + 0.053*CL
	t_{PLZ}	1.37	1.37 + 0.000*CL	1.36 + 0.000*CL	1.37 + 0.000*CL
	t_{PHZ}	1.58	1.58 + 0.000*CL	1.58 + 0.000*CL	1.58 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.70	1.09 + 0.032*CL	1.09 + 0.032*CL	1.08 + 0.032*CL
	t_{PHL}	2.16	1.13 + 0.021*CL	1.14 + 0.021*CL	1.13 + 0.021*CL
	t_R	3.84	0.20 + 0.073*CL	0.18 + 0.073*CL	0.17 + 0.073*CL
	t_F	2.42	0.26 + 0.043*CL	0.23 + 0.044*CL	0.24 + 0.044*CL
TN to PAD	t_{PLH}	2.67	1.06 + 0.032*CL	1.06 + 0.032*CL	1.07 + 0.032*CL
	t_{PHL}	2.20	1.16 + 0.021*CL	1.18 + 0.021*CL	1.17 + 0.021*CL
	t_R	3.84	0.21 + 0.073*CL	0.18 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.26 + 0.043*CL	0.26 + 0.043*CL	0.24 + 0.044*CL
	t_{PLZ}	1.59	1.58 + 0.000*CL	1.58 + 0.000*CL	1.59 + 0.000*CL
	t_{PHZ}	1.50	1.50 + 0.000*CL	1.50 + 0.000*CL	1.50 + 0.000*CL
EN to PAD	t_{PLH}	2.86	1.25 + 0.032*CL	1.25 + 0.032*CL	1.25 + 0.032*CL
	t_{PHL}	2.39	1.36 + 0.021*CL	1.36 + 0.021*CL	1.37 + 0.021*CL
	t_R	3.84	0.21 + 0.073*CL	0.18 + 0.073*CL	0.18 + 0.073*CL
	t_F	2.43	0.28 + 0.043*CL	0.26 + 0.043*CL	0.24 + 0.044*CL
	t_{PLZ}	1.49	1.49 + 0.000*CL	1.49 + 0.000*CL	1.49 + 0.000*CL
	t_{PHZ}	1.43	1.38 + 0.001*CL	1.45 + 0.000*CL	1.45 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.46	1.24 + 0.024*CL	1.24 + 0.024*CL	1.24 + 0.024*CL
	t_{PHL}	2.08	1.27 + 0.016*CL	1.29 + 0.016*CL	1.30 + 0.016*CL
	t_R	3.00	0.26 + 0.055*CL	0.23 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.98	0.34 + 0.033*CL	0.34 + 0.033*CL	0.34 + 0.033*CL
TN to PAD	t_{PLH}	2.42	1.19 + 0.025*CL	1.20 + 0.025*CL	1.20 + 0.025*CL
	t_{PHL}	2.11	1.29 + 0.016*CL	1.32 + 0.016*CL	1.33 + 0.016*CL
	t_R	3.01	0.27 + 0.055*CL	0.24 + 0.055*CL	0.24 + 0.055*CL
	t_F	1.98	0.35 + 0.033*CL	0.35 + 0.033*CL	0.32 + 0.033*CL
	t_{PLZ}	1.83	1.83 + 0.000*CL	1.83 + 0.000*CL	1.83 + 0.000*CL
	t_{PHZ}	1.74	1.74 + 0.000*CL	1.74 + 0.000*CL	1.74 + 0.000*CL
EN to PAD	t_{PLH}	2.61	1.38 + 0.025*CL	1.38 + 0.025*CL	1.39 + 0.025*CL
	t_{PHL}	2.30	1.48 + 0.016*CL	1.51 + 0.016*CL	1.52 + 0.016*CL
	t_R	3.01	0.28 + 0.055*CL	0.24 + 0.055*CL	0.23 + 0.055*CL
	t_F	1.98	0.36 + 0.032*CL	0.36 + 0.032*CL	0.32 + 0.033*CL
	t_{PLZ}	1.73	1.73 + 0.000*CL	1.73 + 0.000*CL	1.72 + 0.000*CL
	t_{PHZ}	1.66	1.65 + 0.000*CL	1.66 + 0.000*CL	1.65 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.99	1.03 + 0.099*CL	1.03 + 0.099*CL	1.03 + 0.099*CL
	t_{PHL}	4.41	1.22 + 0.064*CL	1.22 + 0.064*CL	1.22 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.28 + 0.226*CL	0.28 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL
TN to PAD	t_{PLH}	5.96	1.00 + 0.099*CL	1.00 + 0.099*CL	1.00 + 0.099*CL
	t_{PHL}	4.45	1.26 + 0.064*CL	1.25 + 0.064*CL	1.26 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.27 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.22 + 0.137*CL
	t_{PLZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL
	t_{PHZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
EN to PAD	t_{PLH}	6.15	1.18 + 0.099*CL	1.19 + 0.099*CL	1.15 + 0.100*CL
	t_{PHL}	4.64	1.45 + 0.064*CL	1.45 + 0.064*CL	1.45 + 0.064*CL
	t_R	11.58	0.28 + 0.226*CL	0.27 + 0.226*CL	0.27 + 0.226*CL
	t_F	7.10	0.27 + 0.137*CL	0.23 + 0.137*CL	0.23 + 0.137*CL
	t_{PLZ}	0.91	0.85 + 0.001*CL	0.94 + 0.000*CL	0.94 + 0.000*CL
	t_{PHZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT6SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.51	1.23 + 0.066*CL	1.23 + 0.066*CL	1.23 + 0.066*CL
	t_{PHL}	3.65	1.53 + 0.042*CL	1.55 + 0.042*CL	1.55 + 0.042*CL
	t_R	7.71	0.27 + 0.149*CL	0.24 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.42 + 0.089*CL	0.38 + 0.089*CL
TN to PAD	t_{PLH}	4.47	1.19 + 0.066*CL	1.20 + 0.066*CL	1.19 + 0.066*CL
	t_{PHL}	3.69	1.58 + 0.042*CL	1.59 + 0.042*CL	1.59 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.25 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.42 + 0.089*CL	0.37 + 0.089*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL
	t_{PHZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PLH}	4.66	1.38 + 0.066*CL	1.38 + 0.066*CL	1.38 + 0.066*CL
	t_{PHL}	3.89	1.77 + 0.042*CL	1.78 + 0.042*CL	1.79 + 0.042*CL
	t_R	7.71	0.26 + 0.149*CL	0.25 + 0.149*CL	0.24 + 0.149*CL
	t_F	4.88	0.46 + 0.088*CL	0.41 + 0.089*CL	0.38 + 0.089*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL
	t_{PHZ}	0.77	0.77 + 0.000*CL	0.77 + 0.000*CL	0.77 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.85	1.40 + 0.049*CL	1.40 + 0.049*CL	1.40 + 0.049*CL
	t_{PHL}	3.44	1.80 + 0.033*CL	1.85 + 0.032*CL	1.87 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.30 + 0.111*CL	0.28 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.63 + 0.065*CL	0.61 + 0.066*CL
TN to PAD	t_{PLH}	3.81	1.36 + 0.049*CL	1.22 + 0.051*CL	1.39 + 0.049*CL
	t_{PHL}	3.48	1.84 + 0.033*CL	1.89 + 0.032*CL	1.91 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.29 + 0.111*CL	0.28 + 0.111*CL
	t_F	3.91	0.68 + 0.065*CL	0.63 + 0.065*CL	0.62 + 0.065*CL
	t_{PLZ}	0.95	0.95 + 0.000*CL	0.93 + 0.000*CL	0.95 + 0.000*CL
	t_{PHZ}	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + 0.000*CL
EN to PAD	t_{PLH}	4.00	1.55 + 0.049*CL	1.55 + 0.049*CL	1.55 + 0.049*CL
	t_{PHL}	3.67	2.04 + 0.033*CL	2.08 + 0.032*CL	2.10 + 0.032*CL
	t_R	5.85	0.33 + 0.110*CL	0.29 + 0.111*CL	0.28 + 0.111*CL
	t_F	3.91	0.69 + 0.064*CL	0.61 + 0.065*CL	0.62 + 0.065*CL
	t_{PLZ}	0.88	0.93 + -0.001*CL	0.85 + 0.000*CL	0.85 + 0.000*CL
	t_{PHZ}	0.77	0.77 + 0.000*CL	0.77 + 0.000*CL	0.77 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT10SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.32	1.38 + 0.039*CL	1.39 + 0.039*CL	1.39 + 0.039*CL
	t_{PHL}	3.10	1.74 + 0.027*CL	1.82 + 0.026*CL	1.86 + 0.026*CL
	t_R	4.70	0.39 + 0.086*CL	0.35 + 0.087*CL	0.34 + 0.087*CL
	t_F	3.34	0.85 + 0.050*CL	0.83 + 0.050*CL	0.80 + 0.050*CL
TN to PAD	t_{PLH}	3.28	1.35 + 0.039*CL	1.35 + 0.039*CL	1.35 + 0.039*CL
	t_{PHL}	3.13	1.77 + 0.027*CL	1.86 + 0.026*CL	1.89 + 0.026*CL
	t_R	4.71	0.40 + 0.086*CL	0.35 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.36	0.88 + 0.049*CL	0.84 + 0.050*CL	0.79 + 0.051*CL
	t_{PLZ}	1.09	1.09 + 0.000*CL	1.08 + 0.000*CL	1.08 + 0.000*CL
	t_{PHZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
EN to PAD	t_{PLH}	3.47	1.53 + 0.039*CL	1.54 + 0.039*CL	1.54 + 0.039*CL
	t_{PHL}	3.33	1.97 + 0.027*CL	2.05 + 0.026*CL	2.08 + 0.026*CL
	t_R	4.70	0.39 + 0.086*CL	0.35 + 0.087*CL	0.32 + 0.087*CL
	t_F	3.36	0.88 + 0.049*CL	0.84 + 0.050*CL	0.80 + 0.051*CL
	t_{PLZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
	t_{PHZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.17	1.54 + 0.033*CL	1.55 + 0.032*CL	1.56 + 0.032*CL
	t_{PHL}	3.14	1.91 + 0.025*CL	2.02 + 0.023*CL	2.07 + 0.022*CL
	t_R	4.06	0.51 + 0.071*CL	0.45 + 0.072*CL	0.44 + 0.072*CL
	t_F	3.10	1.03 + 0.041*CL	1.00 + 0.042*CL	1.01 + 0.042*CL
TN to PAD	t_{PLH}	3.14	1.51 + 0.033*CL	1.64 + 0.031*CL	1.43 + 0.033*CL
	t_{PHL}	3.17	1.93 + 0.025*CL	2.04 + 0.023*CL	2.10 + 0.023*CL
	t_R	4.06	0.51 + 0.071*CL	0.46 + 0.072*CL	0.43 + 0.072*CL
	t_F	3.12	1.08 + 0.041*CL	1.06 + 0.041*CL	1.02 + 0.042*CL
	t_{PLZ}	1.09	1.09 + 0.000*CL	1.07 + 0.000*CL	1.07 + 0.000*CL
	t_{PHZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
EN to PAD	t_{PLH}	3.32	1.69 + 0.033*CL	1.70 + 0.032*CL	1.70 + 0.032*CL
	t_{PHL}	3.36	2.12 + 0.025*CL	2.24 + 0.023*CL	2.29 + 0.023*CL
	t_R	4.06	0.52 + 0.071*CL	0.46 + 0.072*CL	0.43 + 0.072*CL
	t_F	3.12	1.08 + 0.041*CL	1.06 + 0.041*CL	1.03 + 0.041*CL
	t_{PLZ}	0.99	0.98 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
	t_{PHZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 POT16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.10	1.80 + 0.026*CL	1.86 + 0.025*CL	1.87 + 0.025*CL
	t_{PHL}	3.31	2.19 + 0.022*CL	2.33 + 0.020*CL	2.41 + 0.020*CL
	t_R	3.37	0.73 + 0.053*CL	0.70 + 0.053*CL	0.66 + 0.054*CL
	t_F	2.88	1.25 + 0.033*CL	1.32 + 0.032*CL	1.30 + 0.032*CL
TN to PAD	t_{PLH}	3.05	1.72 + 0.026*CL	1.82 + 0.025*CL	1.84 + 0.025*CL
	t_{PHL}	3.32	2.18 + 0.023*CL	2.34 + 0.021*CL	2.43 + 0.020*CL
	t_R	3.38	0.76 + 0.052*CL	0.70 + 0.053*CL	0.67 + 0.054*CL
	t_F	2.95	1.38 + 0.031*CL	1.41 + 0.031*CL	1.37 + 0.031*CL
	t_{PLZ}	1.08	1.07 + 0.000*CL	1.08 + 0.000*CL	1.08 + 0.000*CL
	t_{PHZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
EN to PAD	t_{PLH}	3.23	1.94 + 0.026*CL	2.00 + 0.025*CL	2.01 + 0.025*CL
	t_{PHL}	3.52	2.37 + 0.023*CL	2.54 + 0.021*CL	2.62 + 0.020*CL
	t_R	3.39	0.77 + 0.052*CL	0.69 + 0.053*CL	0.68 + 0.054*CL
	t_F	2.94	1.37 + 0.031*CL	1.41 + 0.031*CL	1.37 + 0.031*CL
	t_{PLZ}	0.99	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
	t_{PHZ}	0.89	0.88 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	15.51	0.90 + 0.292*CL	0.90 + 0.292*CL	0.89 + 0.292*CL
	t_{PHL}	12.56	0.91 + 0.233*CL	0.92 + 0.233*CL	0.91 + 0.233*CL
	t_R	33.59	0.59 + 0.660*CL	0.60 + 0.660*CL	0.59 + 0.660*CL
	t_F	24.65	0.40 + 0.485*CL	0.40 + 0.485*CL	0.40 + 0.485*CL
TN to PAD	t_{PLH}	10.17	1.03 + 0.183*CL	1.63 + 0.175*CL	2.79 + 0.161*CL
	t_{PHL}	17.31	1.10 + 0.324*CL	1.11 + 0.324*CL	1.10 + 0.324*CL
	t_R	16.39	0.24 + 0.323*CL	0.24 + 0.323*CL	0.24 + 0.323*CL
	t_F	20.78	0.31 + 0.409*CL	0.31 + 0.409*CL	0.31 + 0.409*CL
	t_{PLZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PLH}	10.34	1.19 + 0.183*CL	1.80 + 0.175*CL	2.98 + 0.161*CL
	t_{PHL}	17.47	1.27 + 0.324*CL	1.27 + 0.324*CL	1.27 + 0.324*CL
	t_R	16.39	0.24 + 0.323*CL	0.24 + 0.323*CL	0.24 + 0.323*CL
	t_F	20.78	0.31 + 0.409*CL	0.31 + 0.409*CL	0.31 + 0.409*CL
	t_{PLZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	8.13	0.83 + 0.146*CL	0.82 + 0.146*CL	0.83 + 0.146*CL
	t_{PHL}	6.65	0.83 + 0.116*CL	0.84 + 0.116*CL	0.84 + 0.116*CL
	t_R	16.81	0.31 + 0.330*CL	0.30 + 0.330*CL	0.31 + 0.330*CL
	t_F	12.34	0.21 + 0.243*CL	0.21 + 0.243*CL	0.21 + 0.243*CL
TN to PAD	t_{PLH}	5.51	0.88 + 0.093*CL	0.88 + 0.093*CL	0.89 + 0.093*CL
	t_{PHL}	9.09	0.99 + 0.162*CL	0.99 + 0.162*CL	0.99 + 0.162*CL
	t_R	8.20	0.12 + 0.161*CL	0.13 + 0.161*CL	0.12 + 0.161*CL
	t_F	10.40	0.17 + 0.205*CL	0.17 + 0.205*CL	0.17 + 0.205*CL
	t_{PLZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.05 + 0.000*CL
	t_{PHZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
EN to PAD	t_{PLH}	5.68	1.05 + 0.093*CL	1.05 + 0.093*CL	1.05 + 0.093*CL
	t_{PHL}	9.25	1.15 + 0.162*CL	1.15 + 0.162*CL	1.15 + 0.162*CL
	t_R	8.20	0.12 + 0.161*CL	0.13 + 0.161*CL	0.12 + 0.161*CL
	t_F	10.40	0.17 + 0.205*CL	0.17 + 0.205*CL	0.17 + 0.205*CL
	t_{PLZ}	0.99	0.99 + 0.000*CL	0.99 + 0.000*CL	0.99 + 0.000*CL
	t_{PHZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.52	0.83 + 0.094*CL	0.83 + 0.094*CL	0.83 + 0.094*CL
	t_{PHL}	4.54	0.83 + 0.074*CL	0.82 + 0.074*CL	0.83 + 0.074*CL
	t_R	10.81	0.21 + 0.212*CL	0.21 + 0.212*CL	0.21 + 0.212*CL
	t_F	7.88	0.15 + 0.155*CL	0.14 + 0.155*CL	0.15 + 0.155*CL
TN to PAD	t_{PLH}	3.87	0.90 + 0.059*CL	0.90 + 0.059*CL	0.89 + 0.059*CL
	t_{PHL}	6.14	0.97 + 0.103*CL	0.97 + 0.103*CL	0.98 + 0.103*CL
	t_R	5.27	0.09 + 0.104*CL	0.09 + 0.104*CL	0.09 + 0.104*CL
	t_F	6.64	0.12 + 0.130*CL	0.12 + 0.130*CL	0.11 + 0.131*CL
	t_{PLZ}	1.13	1.12 + 0.000*CL	1.12 + 0.000*CL	1.07 + 0.001*CL
	t_{PHZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
EN to PAD	t_{PLH}	4.03	1.06 + 0.059*CL	1.03 + 0.060*CL	1.08 + 0.059*CL
	t_{PHL}	6.30	1.13 + 0.103*CL	1.14 + 0.103*CL	1.13 + 0.103*CL
	t_R	5.27	0.09 + 0.104*CL	0.09 + 0.104*CL	0.08 + 0.104*CL
	t_F	6.64	0.12 + 0.130*CL	0.13 + 0.130*CL	0.11 + 0.131*CL
	t_{PLZ}	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + 0.000*CL
	t_{PHZ}	0.88	0.88 + 0.000*CL	0.88 + 0.000*CL	0.88 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.23	0.89 + 0.047*CL	0.89 + 0.047*CL	0.89 + 0.047*CL
	t_{PHL}	2.74	0.88 + 0.037*CL	0.88 + 0.037*CL	0.89 + 0.037*CL
	t_R	5.43	0.13 + 0.106*CL	0.13 + 0.106*CL	0.13 + 0.106*CL
	t_F	3.96	0.10 + 0.077*CL	0.10 + 0.077*CL	0.10 + 0.077*CL
TN to PAD	t_{PLH}	2.45	0.97 + 0.030*CL	0.96 + 0.030*CL	0.97 + 0.030*CL
	t_{PHL}	3.61	1.03 + 0.052*CL	1.02 + 0.052*CL	1.07 + 0.051*CL
	t_R	2.64	0.06 + 0.052*CL	0.05 + 0.052*CL	0.05 + 0.052*CL
	t_F	3.34	0.08 + 0.065*CL	0.09 + 0.065*CL	0.08 + 0.065*CL
	t_{PLZ}	1.30	1.30 + 0.000*CL	1.29 + 0.000*CL	1.30 + 0.000*CL
	t_{PHZ}	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL
EN to PAD	t_{PLH}	2.62	1.13 + 0.030*CL	1.13 + 0.030*CL	1.13 + 0.030*CL
	t_{PHL}	3.77	1.18 + 0.052*CL	1.19 + 0.052*CL	1.18 + 0.052*CL
	t_R	2.64	0.06 + 0.052*CL	0.05 + 0.052*CL	0.05 + 0.052*CL
	t_F	3.34	0.08 + 0.065*CL	0.08 + 0.065*CL	0.08 + 0.065*CL
	t_{PLZ}	1.25	1.28 + -0.001*CL	1.23 + 0.000*CL	1.23 + 0.000*CL
	t_{PHZ}	0.96	0.96 + 0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.68	0.95 + 0.034*CL	0.95 + 0.035*CL	0.95 + 0.035*CL
	t_{PHL}	2.30	0.94 + 0.027*CL	0.95 + 0.027*CL	0.94 + 0.027*CL
	t_R	4.02	0.12 + 0.078*CL	0.11 + 0.078*CL	0.11 + 0.078*CL
	t_F	2.93	0.11 + 0.056*CL	0.11 + 0.056*CL	0.09 + 0.057*CL
TN to PAD	t_{PLH}	2.12	1.03 + 0.022*CL	1.03 + 0.022*CL	1.03 + 0.022*CL
	t_{PHL}	2.97	1.07 + 0.038*CL	1.07 + 0.038*CL	1.04 + 0.038*CL
	t_R	1.96	0.06 + 0.038*CL	0.05 + 0.038*CL	0.05 + 0.038*CL
	t_F	2.47	0.08 + 0.048*CL	0.08 + 0.048*CL	0.08 + 0.048*CL
	t_{PLZ}	1.43	1.42 + 0.000*CL	1.33 + 0.001*CL	1.50 + -0.001*CL
	t_{PHZ}	1.10	1.10 + 0.000*CL	1.10 + 0.000*CL	1.10 + 0.000*CL
EN to PAD	t_{PLH}	2.29	1.19 + 0.022*CL	1.19 + 0.022*CL	1.19 + 0.022*CL
	t_{PHL}	3.14	1.24 + 0.038*CL	1.24 + 0.038*CL	1.24 + 0.038*CL
	t_R	1.96	0.06 + 0.038*CL	0.06 + 0.038*CL	0.05 + 0.038*CL
	t_F	2.47	0.08 + 0.048*CL	0.09 + 0.048*CL	0.07 + 0.048*CL
	t_{PLZ}	1.37	1.35 + 0.000*CL	1.36 + 0.000*CL	1.36 + 0.000*CL
	t_{PHZ}	1.02	1.02 + 0.000*CL	1.02 + 0.000*CL	1.02 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT16 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.30	1.05 + 0.025*CL	1.05 + 0.025*CL	1.04 + 0.025*CL
	t_{PHL}	2.02	1.03 + 0.020*CL	1.04 + 0.020*CL	1.02 + 0.020*CL
	t_R	2.97	0.14 + 0.057*CL	0.12 + 0.057*CL	0.12 + 0.057*CL
	t_F	2.19	0.15 + 0.041*CL	0.14 + 0.041*CL	0.14 + 0.041*CL
TN to PAD	t_{PLH}	1.91	1.11 + 0.016*CL	1.11 + 0.016*CL	1.11 + 0.016*CL
	t_{PHL}	2.54	1.16 + 0.028*CL	1.15 + 0.028*CL	1.17 + 0.028*CL
	t_R	1.47	0.10 + 0.027*CL	0.09 + 0.027*CL	0.08 + 0.028*CL
	t_F	1.82	0.07 + 0.035*CL	0.08 + 0.035*CL	0.07 + 0.035*CL
	t_{PLZ}	1.60	1.58 + 0.000*CL	1.68 + -0.001*CL	1.60 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL
EN to PAD	t_{PLH}	2.08	1.27 + 0.016*CL	1.28 + 0.016*CL	1.27 + 0.016*CL
	t_{PHL}	2.71	1.33 + 0.028*CL	1.27 + 0.028*CL	1.32 + 0.028*CL
	t_R	1.47	0.10 + 0.027*CL	0.09 + 0.028*CL	0.08 + 0.028*CL
	t_F	1.82	0.07 + 0.035*CL	0.07 + 0.035*CL	0.08 + 0.035*CL
	t_{PLZ}	1.53	1.53 + 0.000*CL	1.53 + 0.000*CL	1.53 + 0.000*CL
	t_{PHZ}	1.10	1.10 + 0.000*CL	1.10 + 0.000*CL	1.10 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT20 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.93	0.94 + 0.020*CL	0.94 + 0.020*CL	0.94 + 0.020*CL
	t_{PHL}	1.79	1.01 + 0.016*CL	1.01 + 0.016*CL	1.00 + 0.016*CL
	t_R	2.34	0.10 + 0.045*CL	0.10 + 0.045*CL	0.08 + 0.045*CL
	t_F	1.75	0.16 + 0.032*CL	0.14 + 0.032*CL	0.12 + 0.032*CL
TN to PAD	t_{PLH}	1.65	1.02 + 0.013*CL	1.02 + 0.013*CL	1.02 + 0.013*CL
	t_{PHL}	2.23	1.14 + 0.022*CL	1.13 + 0.022*CL	1.12 + 0.022*CL
	t_R	1.15	0.07 + 0.022*CL	0.05 + 0.022*CL	0.05 + 0.022*CL
	t_F	1.44	0.06 + 0.028*CL	0.06 + 0.028*CL	0.06 + 0.028*CL
	t_{PLZ}	1.40	1.39 + 0.000*CL	1.47 + -0.001*CL	1.40 + 0.000*CL
	t_{PHZ}	1.15	1.15 + 0.000*CL	1.14 + 0.000*CL	1.15 + 0.000*CL
EN to PAD	t_{PLH}	1.82	1.18 + 0.013*CL	1.22 + 0.012*CL	1.19 + 0.013*CL
	t_{PHL}	2.39	1.29 + 0.022*CL	1.29 + 0.022*CL	1.29 + 0.022*CL
	t_R	1.15	0.07 + 0.022*CL	0.06 + 0.022*CL	0.05 + 0.022*CL
	t_F	1.44	0.07 + 0.028*CL	0.05 + 0.028*CL	0.06 + 0.028*CL
	t_{PLZ}	1.33	1.29 + 0.001*CL	1.51 + -0.002*CL	1.33 + 0.000*CL
	t_{PHZ}	1.07	1.07 + 0.000*CL	1.07 + 0.000*CL	1.07 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT24 Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.86	0.99 + 0.017*CL	0.98 + 0.018*CL	0.99 + 0.018*CL
	t_{PHL}	1.73	1.04 + 0.014*CL	1.04 + 0.014*CL	1.04 + 0.014*CL
	t_R	2.07	0.10 + 0.039*CL	0.12 + 0.039*CL	0.09 + 0.040*CL
	t_F	1.57	0.17 + 0.028*CL	0.16 + 0.028*CL	0.15 + 0.028*CL
TN to PAD	t_{PLH}	1.62	1.07 + 0.011*CL	1.07 + 0.011*CL	1.07 + 0.011*CL
	t_{PHL}	2.13	1.16 + 0.019*CL	1.17 + 0.019*CL	1.17 + 0.019*CL
	t_R	1.03	0.09 + 0.019*CL	0.06 + 0.019*CL	0.07 + 0.019*CL
	t_F	1.28	0.07 + 0.024*CL	0.09 + 0.024*CL	0.05 + 0.024*CL
	t_{PLZ}	1.46	1.45 + 0.000*CL	1.40 + 0.001*CL	1.46 + 0.000*CL
	t_{PHZ}	1.14	1.14 + 0.000*CL	1.14 + 0.000*CL	1.14 + 0.000*CL
EN to PAD	t_{PLH}	1.79	1.23 + 0.011*CL	1.23 + 0.011*CL	1.23 + 0.011*CL
	t_{PHL}	2.29	1.33 + 0.019*CL	1.31 + 0.020*CL	1.33 + 0.019*CL
	t_R	1.03	0.09 + 0.019*CL	0.07 + 0.019*CL	0.07 + 0.019*CL
	t_F	1.28	0.07 + 0.024*CL	0.06 + 0.024*CL	0.05 + 0.024*CL
	t_{PLZ}	1.39	1.39 + 0.000*CL	1.38 + 0.000*CL	1.39 + 0.000*CL
	t_{PHZ}	1.07	1.07 + 0.000*CL	1.07 + 0.000*CL	1.06 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT12SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.44	1.66 + 0.036*CL	1.69 + 0.035*CL	1.69 + 0.035*CL
	t_{PHL}	3.94	2.34 + 0.032*CL	2.45 + 0.031*CL	2.51 + 0.030*CL
	t_R	4.34	0.50 + 0.077*CL	0.44 + 0.078*CL	0.43 + 0.078*CL
	t_F	3.74	0.97 + 0.055*CL	1.00 + 0.055*CL	0.99 + 0.055*CL
TN to PAD	t_{PLH}	2.80	1.64 + 0.023*CL	1.68 + 0.023*CL	1.70 + 0.022*CL
	t_{PHL}	4.69	2.58 + 0.042*CL	2.69 + 0.041*CL	2.74 + 0.040*CL
	t_R	2.26	0.43 + 0.037*CL	0.41 + 0.037*CL	0.38 + 0.037*CL
	t_F	2.79	0.45 + 0.047*CL	0.43 + 0.047*CL	0.39 + 0.048*CL
	t_{PLZ}	1.75	1.74 + 0.000*CL	1.71 + 0.001*CL	1.81 + -0.001*CL
	t_{PHZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
EN to PAD	t_{PLH}	2.97	1.81 + 0.023*CL	1.85 + 0.023*CL	1.86 + 0.022*CL
	t_{PHL}	4.86	2.75 + 0.042*CL	2.84 + 0.041*CL	2.90 + 0.040*CL
	t_R	2.26	0.43 + 0.037*CL	0.40 + 0.037*CL	0.38 + 0.037*CL
	t_F	2.79	0.45 + 0.047*CL	0.40 + 0.047*CL	0.41 + 0.047*CL
	t_{PLZ}	1.68	1.68 + 0.000*CL	1.68 + 0.000*CL	1.68 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT16SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.24	1.89 + 0.027*CL	1.94 + 0.026*CL	1.97 + 0.026*CL
	t_{PHL}	3.64	2.39 + 0.025*CL	2.50 + 0.024*CL	2.56 + 0.023*CL
	t_R	3.43	0.71 + 0.055*CL	0.68 + 0.055*CL	0.67 + 0.055*CL
	t_F	3.00	0.96 + 0.041*CL	1.01 + 0.040*CL	1.02 + 0.040*CL
TN to PAD	t_{PLH}	2.73	1.81 + 0.019*CL	1.88 + 0.017*CL	1.91 + 0.017*CL
	t_{PHL}	4.24	2.60 + 0.033*CL	2.72 + 0.031*CL	2.78 + 0.030*CL
	t_R	1.90	0.61 + 0.026*CL	0.60 + 0.026*CL	0.59 + 0.026*CL
	t_F	2.17	0.50 + 0.033*CL	0.47 + 0.034*CL	0.47 + 0.034*CL
	t_{PLZ}	1.72	1.72 + 0.000*CL	1.72 + 0.000*CL	1.72 + 0.000*CL
	t_{PHZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
EN to PAD	t_{PLH}	2.90	1.97 + 0.018*CL	2.04 + 0.018*CL	2.08 + 0.017*CL
	t_{PHL}	4.40	2.77 + 0.033*CL	2.89 + 0.031*CL	2.94 + 0.031*CL
	t_R	1.90	0.61 + 0.026*CL	0.61 + 0.026*CL	0.59 + 0.026*CL
	t_F	2.17	0.49 + 0.033*CL	0.48 + 0.034*CL	0.47 + 0.034*CL
	t_{PLZ}	1.65	1.65 + 0.000*CL	1.65 + 0.000*CL	1.65 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT20SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.63	1.57 + 0.021*CL	1.62 + 0.021*CL	1.63 + 0.020*CL
	t_{PHL}	2.66	1.80 + 0.017*CL	1.84 + 0.017*CL	1.85 + 0.017*CL
	t_R	2.72	0.58 + 0.043*CL	0.55 + 0.043*CL	0.55 + 0.043*CL
	t_F	2.24	0.72 + 0.030*CL	0.70 + 0.031*CL	0.69 + 0.031*CL
TN to PAD	t_{PLH}	2.25	1.52 + 0.015*CL	1.58 + 0.014*CL	1.61 + 0.014*CL
	t_{PHL}	3.05	1.82 + 0.024*CL	1.91 + 0.023*CL	1.93 + 0.023*CL
	t_R	1.53	0.53 + 0.020*CL	0.50 + 0.020*CL	0.51 + 0.020*CL
	t_F	1.63	0.32 + 0.026*CL	0.29 + 0.027*CL	0.27 + 0.027*CL
	t_{PLZ}	1.08	1.06 + 0.000*CL	1.16 + -0.001*CL	1.08 + 0.000*CL
	t_{PHZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
EN to PAD	t_{PLH}	2.42	1.69 + 0.015*CL	1.75 + 0.014*CL	1.78 + 0.013*CL
	t_{PHL}	3.21	1.98 + 0.025*CL	2.07 + 0.023*CL	2.09 + 0.023*CL
	t_R	1.53	0.53 + 0.020*CL	0.50 + 0.020*CL	0.50 + 0.020*CL
	t_F	1.63	0.30 + 0.026*CL	0.32 + 0.026*CL	0.27 + 0.027*CL
	t_{PLZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
	t_{PHZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT24SH Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.62	1.65 + 0.019*CL	1.72 + 0.019*CL	1.73 + 0.018*CL
	t_{PHL}	2.73	1.94 + 0.016*CL	1.97 + 0.015*CL	1.99 + 0.015*CL
	t_R	2.54	0.66 + 0.038*CL	0.67 + 0.037*CL	0.63 + 0.038*CL
	t_F	2.15	0.81 + 0.027*CL	0.82 + 0.027*CL	0.79 + 0.027*CL
TN to PAD	t_{PLH}	2.27	1.58 + 0.014*CL	1.65 + 0.013*CL	1.68 + 0.012*CL
	t_{PHL}	3.04	1.90 + 0.023*CL	1.99 + 0.022*CL	2.04 + 0.021*CL
	t_R	1.47	0.59 + 0.018*CL	0.60 + 0.018*CL	0.57 + 0.018*CL
	t_F	1.52	0.37 + 0.023*CL	0.38 + 0.023*CL	0.34 + 0.023*CL
	t_{PLZ}	1.08	1.08 + 0.000*CL	1.08 + 0.000*CL	1.08 + 0.000*CL
	t_{PHZ}	1.12	1.12 + 0.000*CL	1.12 + 0.000*CL	1.12 + 0.000*CL
EN to PAD	t_{PLH}	2.43	1.74 + 0.014*CL	1.82 + 0.013*CL	1.84 + 0.012*CL
	t_{PHL}	3.20	2.07 + 0.023*CL	2.16 + 0.021*CL	2.19 + 0.021*CL
	t_R	1.48	0.60 + 0.018*CL	0.61 + 0.017*CL	0.57 + 0.018*CL
	t_F	1.52	0.37 + 0.023*CL	0.35 + 0.023*CL	0.35 + 0.023*CL
	t_{PLZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + 0.000*CL
	t_{PHZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT4SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	5.86	1.16 + 0.094*CL	1.17 + 0.094*CL	1.17 + 0.094*CL
	t_{PHL}	5.46	1.74 + 0.074*CL	1.75 + 0.074*CL	1.75 + 0.074*CL
	t_R	10.83	0.24 + 0.212*CL	0.23 + 0.212*CL	0.24 + 0.212*CL
	t_F	8.06	0.43 + 0.153*CL	0.38 + 0.153*CL	0.36 + 0.153*CL
TN to PAD	t_{PLH}	4.17	1.20 + 0.059*CL	1.20 + 0.059*CL	1.20 + 0.059*CL
	t_{PHL}	7.07	1.90 + 0.103*CL	1.90 + 0.103*CL	1.91 + 0.103*CL
	t_R	5.29	0.13 + 0.103*CL	0.11 + 0.103*CL	0.11 + 0.104*CL
	t_F	6.69	0.18 + 0.130*CL	0.16 + 0.130*CL	0.16 + 0.130*CL
	t_{PLZ}	1.77	1.77 + 0.000*CL	1.77 + 0.000*CL	1.77 + 0.000*CL
	t_{PHZ}	1.26	1.26 + 0.000*CL	1.26 + 0.000*CL	1.26 + 0.000*CL
EN to PAD	t_{PLH}	4.33	1.36 + 0.059*CL	1.36 + 0.060*CL	1.37 + 0.059*CL
	t_{PHL}	7.24	2.07 + 0.103*CL	2.04 + 0.104*CL	2.07 + 0.103*CL
	t_R	5.29	0.13 + 0.103*CL	0.11 + 0.103*CL	0.11 + 0.104*CL
	t_F	6.69	0.17 + 0.130*CL	0.16 + 0.130*CL	0.16 + 0.130*CL
	t_{PLZ}	1.71	1.70 + 0.000*CL	1.71 + 0.000*CL	1.71 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT8SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.82	1.47 + 0.047*CL	1.48 + 0.047*CL	1.48 + 0.047*CL
	t_{PHL}	4.07	2.11 + 0.039*CL	2.18 + 0.038*CL	2.21 + 0.038*CL
	t_R	5.58	0.35 + 0.105*CL	0.31 + 0.105*CL	0.29 + 0.105*CL
	t_F	4.47	0.75 + 0.074*CL	0.72 + 0.075*CL	0.70 + 0.075*CL
TN to PAD	t_{PLH}	2.99	1.49 + 0.030*CL	1.50 + 0.030*CL	1.50 + 0.030*CL
	t_{PHL}	4.98	2.31 + 0.053*CL	2.37 + 0.053*CL	2.38 + 0.052*CL
	t_R	2.80	0.29 + 0.050*CL	0.26 + 0.051*CL	0.23 + 0.051*CL
	t_F	3.50	0.31 + 0.064*CL	0.28 + 0.064*CL	0.25 + 0.065*CL
	t_{PLZ}	1.76	1.74 + 0.000*CL	1.66 + 0.001*CL	1.76 + 0.000*CL
	t_{PHZ}	1.25	1.25 + 0.000*CL	1.25 + 0.000*CL	1.25 + 0.000*CL
EN to PAD	t_{PLH}	3.15	1.65 + 0.030*CL	1.67 + 0.030*CL	1.67 + 0.030*CL
	t_{PHL}	5.14	2.48 + 0.053*CL	2.54 + 0.053*CL	2.56 + 0.052*CL
	t_R	2.80	0.29 + 0.050*CL	0.26 + 0.051*CL	0.23 + 0.051*CL
	t_F	3.50	0.31 + 0.064*CL	0.28 + 0.064*CL	0.25 + 0.065*CL
	t_{PLZ}	1.71	1.70 + 0.000*CL	1.69 + 0.000*CL	1.69 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT12SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.25	1.51 + 0.035*CL	1.52 + 0.035*CL	1.53 + 0.035*CL
	t_{PHL}	3.57	2.04 + 0.031*CL	2.13 + 0.029*CL	2.18 + 0.029*CL
	t_R	4.22	0.41 + 0.076*CL	0.37 + 0.077*CL	0.35 + 0.077*CL
	t_F	3.55	0.81 + 0.055*CL	0.83 + 0.055*CL	0.82 + 0.055*CL
TN to PAD	t_{PLH}	2.63	1.50 + 0.023*CL	1.53 + 0.022*CL	1.55 + 0.022*CL
	t_{PHL}	4.30	2.26 + 0.041*CL	2.35 + 0.040*CL	2.39 + 0.039*CL
	t_R	2.18	0.37 + 0.036*CL	0.32 + 0.037*CL	0.32 + 0.037*CL
	t_F	2.69	0.39 + 0.046*CL	0.37 + 0.046*CL	0.33 + 0.047*CL
	t_{PLZ}	1.99	1.99 + 0.000*CL	1.93 + 0.001*CL	2.05 + -0.001*CL
	t_{PHZ}	1.42	1.42 + 0.000*CL	1.41 + 0.000*CL	1.42 + 0.000*CL
EN to PAD	t_{PLH}	2.80	1.67 + 0.022*CL	1.67 + 0.022*CL	1.71 + 0.022*CL
	t_{PHL}	4.47	2.42 + 0.041*CL	2.51 + 0.040*CL	2.55 + 0.039*CL
	t_R	2.18	0.37 + 0.036*CL	0.33 + 0.037*CL	0.32 + 0.037*CL
	t_F	2.69	0.38 + 0.046*CL	0.36 + 0.047*CL	0.34 + 0.047*CL
	t_{PLZ}	1.92	1.92 + 0.000*CL	1.92 + 0.000*CL	1.84 + 0.001*CL
	t_{PHZ}	1.35	1.35 + 0.000*CL	1.35 + 0.000*CL	1.35 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT16SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.93	1.61 + 0.026*CL	1.65 + 0.026*CL	1.67 + 0.026*CL
	t_{PHL}	3.14	1.96 + 0.024*CL	2.05 + 0.023*CL	2.09 + 0.022*CL
	t_R	3.29	0.54 + 0.055*CL	0.50 + 0.056*CL	0.50 + 0.055*CL
	t_F	2.77	0.74 + 0.041*CL	0.77 + 0.040*CL	0.79 + 0.040*CL
TN to PAD	t_{PLH}	2.45	1.56 + 0.018*CL	1.59 + 0.017*CL	1.67 + 0.016*CL
	t_{PHL}	3.72	2.16 + 0.031*CL	2.25 + 0.030*CL	2.30 + 0.029*CL
	t_R	1.77	0.45 + 0.026*CL	0.46 + 0.026*CL	0.46 + 0.026*CL
	t_F	2.07	0.38 + 0.034*CL	0.38 + 0.034*CL	0.36 + 0.034*CL
	t_{PLZ}	2.19	2.23 + -0.001*CL	2.17 + 0.000*CL	2.11 + 0.001*CL
	t_{PHZ}	1.56	1.56 + 0.000*CL	1.56 + 0.000*CL	1.56 + 0.000*CL
EN to PAD	t_{PLH}	2.61	1.73 + 0.018*CL	1.78 + 0.017*CL	1.80 + 0.017*CL
	t_{PHL}	3.89	2.32 + 0.031*CL	2.41 + 0.030*CL	2.47 + 0.029*CL
	t_R	1.77	0.46 + 0.026*CL	0.47 + 0.026*CL	0.45 + 0.026*CL
	t_F	2.07	0.38 + 0.034*CL	0.39 + 0.034*CL	0.36 + 0.034*CL
	t_{PLZ}	2.12	2.10 + 0.000*CL	2.11 + 0.000*CL	2.11 + 0.000*CL
	t_{PHZ}	1.49	1.49 + 0.000*CL	1.49 + 0.000*CL	1.49 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT20SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.30	1.29 + 0.020*CL	1.30 + 0.020*CL	1.31 + 0.020*CL
	t_{PHL}	2.30	1.41 + 0.018*CL	1.46 + 0.017*CL	1.49 + 0.017*CL
	t_R	2.53	0.36 + 0.043*CL	0.34 + 0.044*CL	0.31 + 0.044*CL
	t_F	2.11	0.54 + 0.031*CL	0.56 + 0.031*CL	0.56 + 0.031*CL
TN to PAD	t_{PLH}	1.98	1.30 + 0.013*CL	1.34 + 0.013*CL	1.34 + 0.013*CL
	t_{PHL}	2.76	1.57 + 0.024*CL	1.61 + 0.023*CL	1.64 + 0.023*CL
	t_R	1.36	0.35 + 0.020*CL	0.32 + 0.021*CL	0.30 + 0.021*CL
	t_F	1.58	0.26 + 0.026*CL	0.24 + 0.027*CL	0.22 + 0.027*CL
	t_{PLZ}	1.25	1.24 + 0.000*CL	1.18 + 0.001*CL	1.31 + -0.001*CL
	t_{PHZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL
EN to PAD	t_{PLH}	2.14	1.47 + 0.013*CL	1.50 + 0.013*CL	1.51 + 0.013*CL
	t_{PHL}	2.92	1.74 + 0.024*CL	1.79 + 0.023*CL	1.83 + 0.023*CL
	t_R	1.35	0.33 + 0.020*CL	0.34 + 0.020*CL	0.29 + 0.021*CL
	t_F	1.59	0.28 + 0.026*CL	0.24 + 0.027*CL	0.22 + 0.027*CL
	t_{PLZ}	1.18	1.15 + 0.001*CL	1.19 + 0.000*CL	1.19 + 0.000*CL
	t_{PHZ}	0.97	0.97 + 0.000*CL	0.97 + 0.000*CL	0.97 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PHOT24SM Switching Characteristics

[Delays for typical process, 25°C, 5.0V*, 3.3V*,when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.28	1.36 + 0.018*CL	1.40 + 0.018*CL	1.41 + 0.018*CL
	t_{PHL}	2.32	1.49 + 0.017*CL	1.56 + 0.016*CL	1.59 + 0.015*CL
	t_R	2.33	0.44 + 0.038*CL	0.43 + 0.038*CL	0.41 + 0.038*CL
	t_F	2.01	0.62 + 0.028*CL	0.66 + 0.027*CL	0.65 + 0.027*CL
TN to PAD	t_{PLH}	1.98	1.35 + 0.013*CL	1.40 + 0.012*CL	1.42 + 0.012*CL
	t_{PHL}	2.75	1.65 + 0.022*CL	1.73 + 0.021*CL	1.76 + 0.021*CL
	t_R	1.30	0.42 + 0.018*CL	0.43 + 0.017*CL	0.39 + 0.018*CL
	t_F	1.47	0.32 + 0.023*CL	0.32 + 0.023*CL	0.31 + 0.023*CL
	t_{PLZ}	1.25	1.24 + 0.000*CL	1.24 + 0.000*CL	1.25 + 0.000*CL
	t_{PHZ}	1.05	1.05 + 0.000*CL	1.05 + 0.000*CL	1.05 + 0.000*CL
EN to PAD	t_{PLH}	2.14	1.52 + 0.013*CL	1.56 + 0.012*CL	1.58 + 0.012*CL
	t_{PHL}	2.92	1.80 + 0.022*CL	1.93 + 0.021*CL	1.94 + 0.020*CL
	t_R	1.29	0.40 + 0.018*CL	0.43 + 0.017*CL	0.41 + 0.018*CL
	t_F	1.47	0.33 + 0.023*CL	0.30 + 0.023*CL	0.31 + 0.023*CL
	t_{PLZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.17 + 0.000*CL
	t_{PHZ}	0.97	0.97 + 0.000*CL	0.97 + 0.000*CL	0.97 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Cell List

Cell Name	Function Description
KG80	
PBaDyz	5V Open-Drain Bi-Directional Buffers
PBaUDyz	5V Open-Drain Bi-Directional Buffers with Pull-Up
PBaTyz	5V Tri-State Bi-Directional Buffers
PBaDTyz	5V Tri-State Bi-Directional Buffers with Pull-Down
PBaUTyz	5V Tri-State Bi-Directional Buffers with Pull-Up
PLBaDyz	3.3V Interface Open-Drain Bi-Directional Buffers
PLBaUDyz	3.3V Interface Open-Drain Bi-Directional Buffers with Pull-Up
PLBaTyz	3.3V Interface Tri-State Bi-Directional Buffers
PLBaDTyz	3.3V Interface Tri-State Bi-Directional Buffers with Pull-Down
PLBaUTyz	3.3V Interface Tri-State Bi-Directional Buffers with Pull-Up
KGM80	
PBaDyz	3.3V Open-Drain Bi-Directional Buffers
PBaUDyz	3.3V Open-Drain Bi-Directional Buffers with Pull-Up
PBaTyz	3.3V Tri-State Bi-Directional Buffers
PBaDTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Down
PBaUTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Up
PHBaDyz	5V Interface Open-Drain Bi-Directional Buffers
PHBaUDyz	5V Interface Open-Drain Bi-Directional Buffers with Pull-Up
PHBaTyz	5V Interface Tri-State Bi-Directional Buffers
PHBaDTyz	5V Interface Tri-State Bi-Directional Buffers with Pull-Down
PHBaUTyz	5V Interface Tri-State Bi-Directional Buffers with Pull-Up

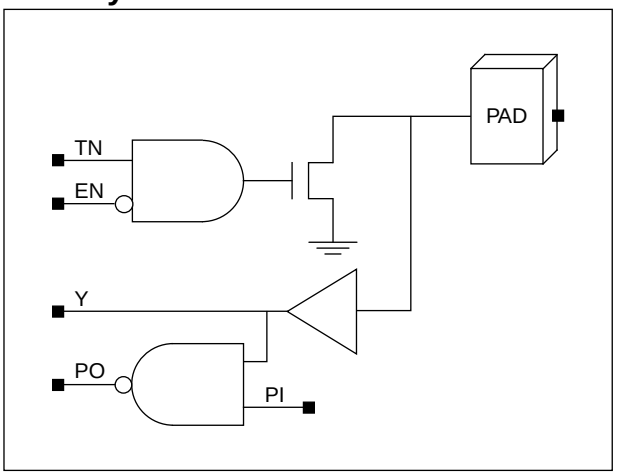
PvBaDyz/PvBaUDyz

Open Drain Bi-Directional Buffers

PvBaTyz/PvBaDTyz/PvBaUTyz

Tri-State Bi-Directional Buffers

PvBaDyz



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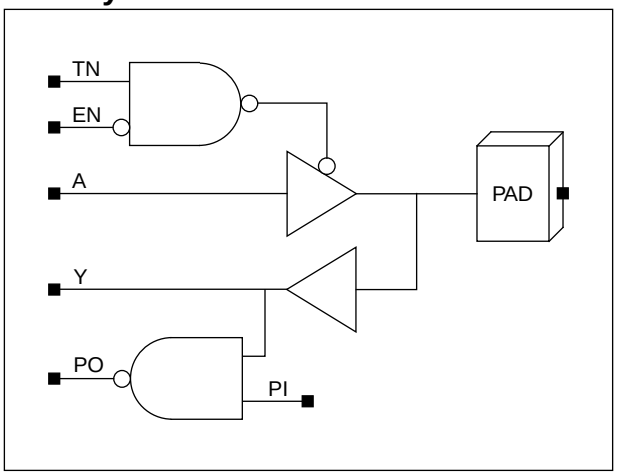

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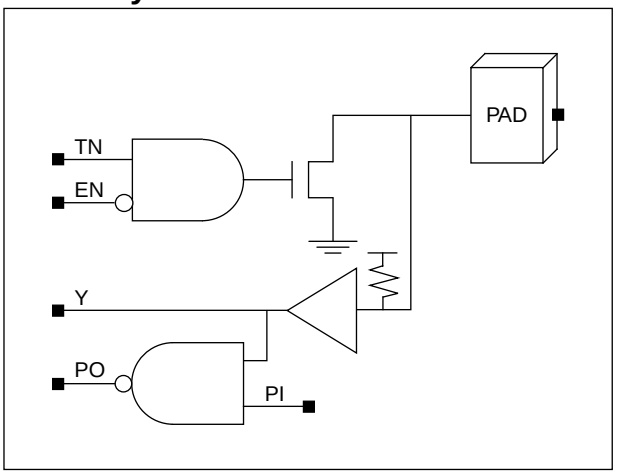

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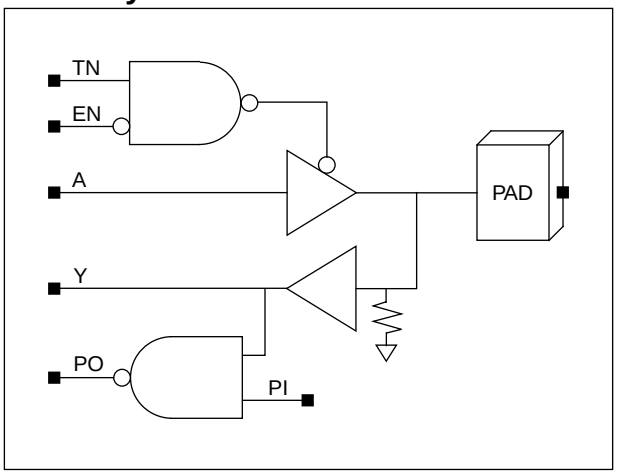

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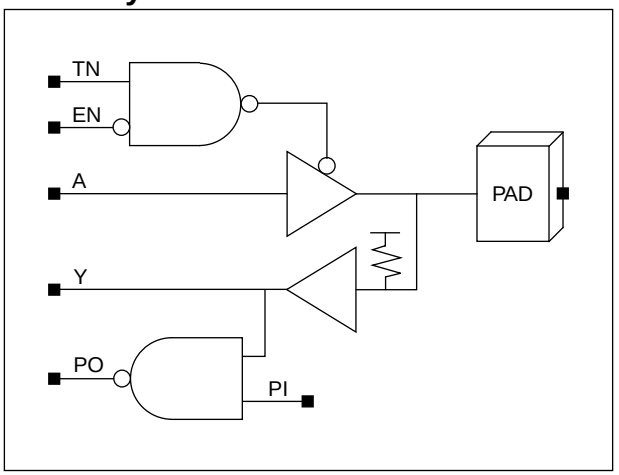


Cell List

Cell Name	Function Description
KG80	
PSCKDC(2/4/8/12)	5V CMOS Level Input Clock Drivers
PSCKDCD(2/4/8/12)	5V CMOS Level Input Clock Drivers with Pull-Down
PSCKDCU(2/4/8/12)	5V CMOS Level Input Clock Drivers with Pull-Up
PSCKDL(2/4/8/12)	5V TTL Schmitt Trigger Level Input Clock Drivers
PSCKDLD(2/4/8/12)	5V TTL Schmitt Trigger Level Input Clock Drivers with Pull-Down
PSCKDLU(2/4/8/12)	5V TTL Schmitt Trigger Level Input Clock Drivers with Pull-Up
PSCKDS(2/4/8/12)	5V CMOS Schmitt Trigger Level Input Clock Drivers
PSCKDSD(2/4/8/12)	5V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Down
PSCKDSU(2/4/8/12)	5V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Up
PSCKDT(2/4/8/12)	5V TTL Level Input Clock Drivers
PSCKDTD(2/4/8/12)	5V TTL Level Input Clock Drivers with Pull-Down
PSCKDTU(2/4/8/12)	5V TTL Level Input Clock Drivers with Pull-Up
KGM80	
PSCKDC(2/4/6/8)	3.3V CMOS Level Input Clock Drivers
PSCKDCD(2/4/6/8)	3.3V CMOS Level Input Clock Drivers with Pull-Down
PSCKDCU(2/4/6/8)	3.3V CMOS Level Input Clock Drivers with Pull-Up
PSCKDS(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers
PSCKDSD(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Down
PSCKDSU(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Up

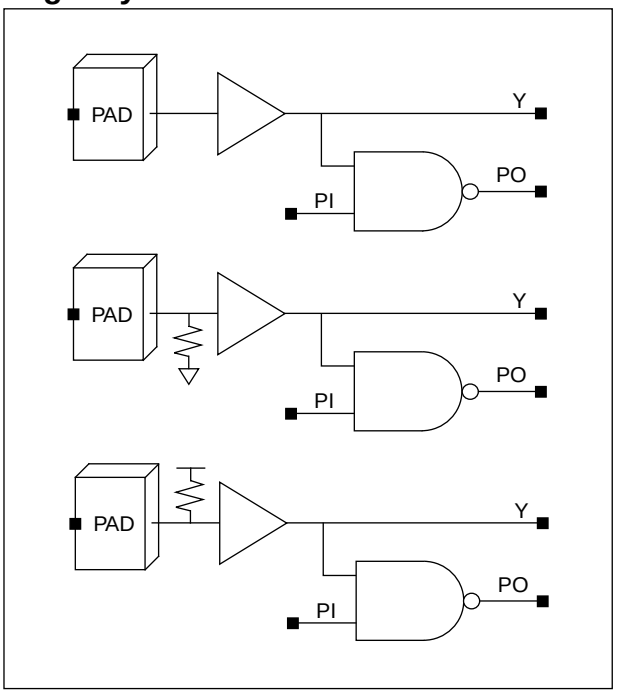
PSCKDCy/PSCKDCDy/PSCKDCUy

CMOS Level Input Clock Drivers

Cell Availability

Library	5V Operation	3.3V Operation
KG80	PSCKDC(2/4/8/12) PSCKDCD(2/4/8/12) PSCKDCU(2/4/8/12)	–
KGM80	–	PSCKDC(2/4/6/8) PSCKDCD(2/4/6/8) PSCKDCU(2/4/6/8)

Logic Symbol



Input Load (SL)

KG80	
	PI
PSCKDC(2/4/8/12)	1.6
PSCKDCD(2/4/8/12)	1.6
PSCKDCU(2/4/8/12)	1.6
KGM80	
	PI
PSCKDC(2/4/6/8)	1.9
PSCKDCD(2/4/6/8)	1.9
PSCKDCU(2/4/6/8)	1.9

I/O Slot

KG80/KGM80	
PSCKDCy/PSCKDCDy/PSCKDCUy	1.0

KG80 PSCKDC2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.70	0.24 + 0.005*SL	0.24 + 0.006*SL	0.24 + 0.005*SL
	t_{PHL}	0.64	0.22 + 0.005*SL	0.22 + 0.005*SL	0.22 + 0.005*SL
	t_R	1.08	0.09 + 0.012*SL	0.08 + 0.012*SL	0.07 + 0.012*SL
	t_F	0.84	0.08 + 0.009*SL	0.07 + 0.009*SL	0.06 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 PSCKDC4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.30 + 0.003*SL	0.30 + 0.003*SL	0.30 + 0.003*SL
	t_{PHL}	0.68	0.27 + 0.003*SL	0.27 + 0.003*SL	0.27 + 0.002*SL
	t_R	1.07	0.10 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.83	0.09 + 0.004*SL	0.08 + 0.005*SL	0.07 + 0.005*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 PSCKDC8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.76	0.32 + 0.001*SL	0.32 + 0.001*SL	0.32 + 0.001*SL
	t_{PHL}	0.73	0.32 + 0.001*SL	0.32 + 0.001*SL	0.32 + 0.001*SL
	t_R	1.06	0.10 + 0.003*SL	0.09 + 0.003*SL	0.08 + 0.003*SL
	t_F	0.82	0.10 + 0.002*SL	0.09 + 0.002*SL	0.07 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 PSCKDC12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.82	0.38 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_{PHL}	0.78	0.37 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_R	1.06	0.13 + 0.002*SL	0.11 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.84	0.12 + 0.001*SL	0.11 + 0.001*SL	0.10 + 0.002*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

KG80 PSCKDCD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.71	0.26 + 0.005*SL	0.25 + 0.006*SL	0.26 + 0.005*SL
	t_{PHL}	0.64	0.22 + 0.005*SL	0.23 + 0.005*SL	0.22 + 0.005*SL
	t_R	1.08	0.09 + 0.012*SL	0.08 + 0.012*SL	0.08 + 0.012*SL
	t_F	0.84	0.08 + 0.009*SL	0.07 + 0.009*SL	0.06 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦ SL ≦ 83, *Group3 : 83 < SL

KG80 PSCKDCD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.76	0.31 + 0.003*SL	0.31 + 0.003*SL	0.31 + 0.003*SL
	t_{PHL}	0.68	0.27 + 0.003*SL	0.27 + 0.003*SL	0.28 + 0.002*SL
	t_R	1.07	0.10 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.83	0.09 + 0.004*SL	0.08 + 0.005*SL	0.07 + 0.005*SL

*Group1 : SL < 109, *Group2 : 109 ≦ SL ≦ 164, *Group3 : 164 < SL

KG80 PSCKDCD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.33 + 0.001*SL	0.33 + 0.001*SL	0.33 + 0.001*SL
	t_{PHL}	0.73	0.32 + 0.001*SL	0.33 + 0.001*SL	0.32 + 0.001*SL
	t_R	1.06	0.10 + 0.003*SL	0.09 + 0.003*SL	0.08 + 0.003*SL
	t_F	0.83	0.10 + 0.002*SL	0.08 + 0.002*SL	0.08 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦ SL ≦ 325, *Group3 : 325 < SL

KG80 PSCKDCD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.83	0.39 + 0.001*SL	0.39 + 0.001*SL	0.39 + 0.001*SL
	t_{PHL}	0.79	0.38 + 0.001*SL	0.38 + 0.001*SL	0.39 + 0.001*SL
	t_R	1.06	0.12 + 0.002*SL	0.11 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.84	0.13 + 0.001*SL	0.11 + 0.001*SL	0.10 + 0.002*SL

*Group1 : SL < 324, *Group2 : 324 ≦ SL ≦ 486, *Group3 : 486 < SL

KG80 PSCKDCU2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.70	0.25 + 0.005*SL	0.25 + 0.005*SL	0.25 + 0.005*SL
	t_{PHL}	0.64	0.23 + 0.005*SL	0.23 + 0.005*SL	0.23 + 0.005*SL
	t_R	1.08	0.09 + 0.012*SL	0.08 + 0.012*SL	0.08 + 0.012*SL
	t_F	0.84	0.08 + 0.009*SL	0.07 + 0.009*SL	0.06 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 PSCKDCU4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.30 + 0.003*SL	0.30 + 0.003*SL	0.30 + 0.003*SL
	t_{PHL}	0.69	0.27 + 0.003*SL	0.28 + 0.002*SL	0.27 + 0.003*SL
	t_R	1.07	0.10 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.83	0.09 + 0.004*SL	0.08 + 0.005*SL	0.07 + 0.005*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 PSCKDCU8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.77	0.32 + 0.001*SL	0.32 + 0.001*SL	0.32 + 0.001*SL
	t_{PHL}	0.74	0.33 + 0.001*SL	0.33 + 0.001*SL	0.33 + 0.001*SL
	t_R	1.06	0.10 + 0.003*SL	0.09 + 0.003*SL	0.08 + 0.003*SL
	t_F	0.83	0.10 + 0.002*SL	0.08 + 0.002*SL	0.08 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 PSCKDCU12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.82	0.38 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_{PHL}	0.79	0.38 + 0.001*SL	0.39 + 0.001*SL	0.39 + 0.001*SL
	t_R	1.06	0.13 + 0.002*SL	0.11 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.83	0.12 + 0.001*SL	0.11 + 0.001*SL	0.09 + 0.002*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

KGM80 PSCKDC2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.14	0.36 + 0.004*SL	0.29 + 0.004*SL	0.30 + 0.004*SL
	t_{PHL}	0.95	0.31 + 0.003*SL	0.31 + 0.003*SL	0.32 + 0.003*SL
	t_R	1.97	0.14 + 0.009*SL	0.11 + 0.010*SL	0.14 + 0.009*SL
	t_F	1.31	0.11 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

KGM80 PSCKDC4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.26	0.42 + 0.002*SL	0.42 + 0.002*SL	0.43 + 0.002*SL
	t_{PHL}	1.05	0.41 + 0.002*SL	0.42 + 0.002*SL	0.41 + 0.002*SL
	t_R	1.96	0.16 + 0.005*SL	0.14 + 0.005*SL	0.13 + 0.005*SL
	t_F	1.32	0.13 + 0.003*SL	0.15 + 0.003*SL	0.13 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

KGM80 PSCKDC6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.23	0.39 + 0.001*SL	0.38 + 0.001*SL	0.39 + 0.001*SL
	t_{PHL}	1.05	0.41 + 0.001*SL	0.41 + 0.001*SL	0.41 + 0.001*SL
	t_R	1.96	0.14 + 0.003*SL	0.11 + 0.003*SL	0.14 + 0.003*SL
	t_F	1.33	0.23 + 0.002*SL	0.17 + 0.002*SL	0.14 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

KGM80 PSCKDC8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.28	0.44 + 0.001*SL	0.44 + 0.001*SL	0.44 + 0.001*SL
	t_{PHL}	1.13	0.49 + 0.001*SL	0.49 + 0.001*SL	0.49 + 0.001*SL
	t_R	1.95	0.15 + 0.002*SL	0.14 + 0.002*SL	0.14 + 0.002*SL
	t_F	1.33	0.17 + 0.001*SL	0.12 + 0.002*SL	0.15 + 0.002*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

KGM80 PSCKDCD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.17	0.32 + 0.004*SL	0.31 + 0.004*SL	0.33 + 0.004*SL
	t_{PHL}	0.96	0.32 + 0.003*SL	0.32 + 0.003*SL	0.32 + 0.003*SL
	t_R	1.97	0.14 + 0.009*SL	0.10 + 0.010*SL	0.15 + 0.009*SL
	t_F	1.30	0.12 + 0.006*SL	0.09 + 0.006*SL	0.08 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

KGM80 PSCKDCD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.27	0.43 + 0.002*SL	0.43 + 0.002*SL	0.44 + 0.002*SL
	t_{PHL}	1.06	0.42 + 0.002*SL	0.42 + 0.002*SL	0.42 + 0.002*SL
	t_R	1.96	0.16 + 0.005*SL	0.15 + 0.005*SL	0.14 + 0.005*SL
	t_F	1.31	0.18 + 0.003*SL	0.12 + 0.003*SL	0.11 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

KGM80 PSCKDCD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.24	0.40 + 0.001*SL	0.40 + 0.001*SL	0.41 + 0.001*SL
	t_{PHL}	1.08	0.43 + 0.001*SL	0.43 + 0.001*SL	0.44 + 0.001*SL
	t_R	1.96	0.15 + 0.003*SL	0.11 + 0.003*SL	0.13 + 0.003*SL
	t_F	1.32	0.15 + 0.002*SL	0.10 + 0.002*SL	0.12 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

KGM80 PSCKDCD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.28	0.44 + 0.001*SL	0.44 + 0.001*SL	0.44 + 0.001*SL
	t_{PHL}	1.13	0.49 + 0.001*SL	0.50 + 0.001*SL	0.50 + 0.001*SL
	t_R	1.96	0.16 + 0.002*SL	0.12 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.31	0.16 + 0.001*SL	0.16 + 0.001*SL	0.10 + 0.002*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

KGM80 PSCKDCU2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.15	0.29 + 0.004*SL	0.30 + 0.004*SL	0.31 + 0.004*SL
	t_{PHL}	0.96	0.32 + 0.003*SL	0.32 + 0.003*SL	0.32 + 0.003*SL
	t_R	1.98	0.14 + 0.009*SL	0.11 + 0.010*SL	0.16 + 0.009*SL
	t_F	1.31	0.11 + 0.006*SL	0.10 + 0.006*SL	0.09 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

KGM80 PSCKDCU4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.26	0.42 + 0.002*SL	0.43 + 0.002*SL	0.43 + 0.002*SL
	t_{PHL}	1.06	0.42 + 0.002*SL	0.42 + 0.002*SL	0.42 + 0.002*SL
	t_R	1.96	0.18 + 0.005*SL	0.13 + 0.005*SL	0.14 + 0.005*SL
	t_F	1.31	0.15 + 0.003*SL	0.13 + 0.003*SL	0.11 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

KGM80 PSCKDCU6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.23	0.39 + 0.001*SL	0.39 + 0.001*SL	0.39 + 0.001*SL
	t_{PHL}	1.07	0.43 + 0.001*SL	0.43 + 0.001*SL	0.44 + 0.001*SL
	t_R	1.96	0.16 + 0.003*SL	0.13 + 0.003*SL	0.13 + 0.003*SL
	t_F	1.32	0.16 + 0.002*SL	0.13 + 0.002*SL	0.13 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

KGM80 PSCKDCU8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

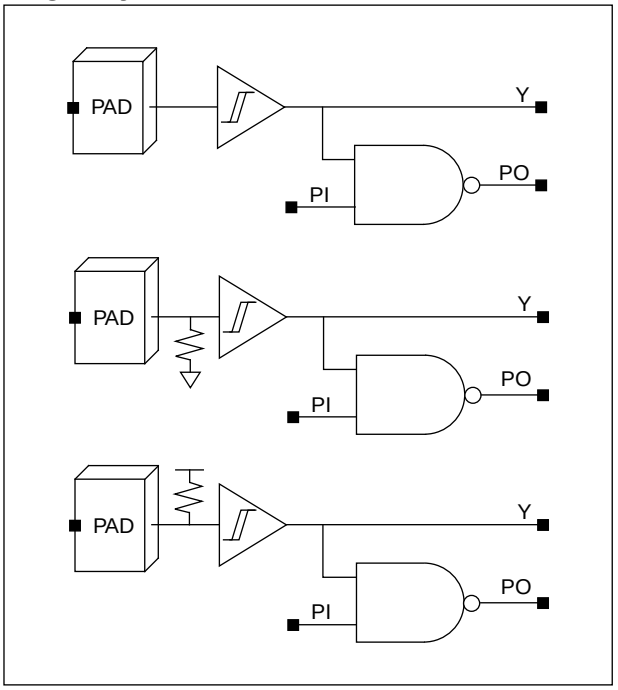
Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.28	0.45 + 0.001*SL	0.45 + 0.001*SL	0.45 + 0.001*SL
	t_{PHL}	1.13	0.49 + 0.001*SL	0.49 + 0.001*SL	0.50 + 0.001*SL
	t_R	1.95	0.15 + 0.002*SL	0.15 + 0.002*SL	0.13 + 0.002*SL
	t_F	1.32	0.17 + 0.001*SL	0.12 + 0.002*SL	0.13 + 0.002*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

Cell Availability

Library	5V Operation	3.3V Operation
KG80	PSCKDL(2/4/8/12) PSCKDLD(2/4/8/12) PSCKDLU(2/4/8/12)	–
KGM80	–	–

Logic Symbol



Input Load (SL)

KG80	
	PI
PSCKDL(2/4/8/12)	1.6
PSCKDLD(2/4/8/12)	1.6
PSCKDLU(2/4/8/12)	1.6

I/O Slot

KG80/KGM80	
PSCKDLy/PSCKDLDy/PSCKDLUy	1.0

KG80 PSCKDL2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.90	0.44 + 0.006*SL	0.45 + 0.005*SL	0.45 + 0.005*SL
	t_{PHL}	2.28	1.75 + 0.007*SL	1.79 + 0.006*SL	1.82 + 0.006*SL
	t_R	1.09	0.13 + 0.012*SL	0.11 + 0.012*SL	0.10 + 0.012*SL
	t_F	1.24	0.58 + 0.008*SL	0.58 + 0.008*SL	0.57 + 0.008*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 PSCKDL4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.99	0.53 + 0.003*SL	0.54 + 0.003*SL	0.54 + 0.003*SL
	t_{PHL}	2.94	2.36 + 0.004*SL	2.42 + 0.003*SL	2.46 + 0.003*SL
	t_R	1.10	0.16 + 0.006*SL	0.15 + 0.006*SL	0.13 + 0.006*SL
	t_F	1.48	0.83 + 0.004*SL	0.84 + 0.004*SL	0.84 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 PSCKDL8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.92	0.47 + 0.001*SL	0.47 + 0.001*SL	0.47 + 0.001*SL
	t_{PHL}	2.51	1.99 + 0.002*SL	2.03 + 0.001*SL	2.06 + 0.001*SL
	t_R	1.08	0.14 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.36	0.73 + 0.002*SL	0.73 + 0.002*SL	0.72 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 PSCKDL12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.01	0.55 + 0.001*SL	0.56 + 0.001*SL	0.57 + 0.001*SL
	t_{PHL}	3.22	2.65 + 0.001*SL	2.70 + 0.001*SL	2.74 + 0.001*SL
	t_R	1.10	0.18 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.64	1.02 + 0.001*SL	1.03 + 0.001*SL	1.03 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

KG80 PSCKDLD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.91	0.46 + 0.006*SL	0.46 + 0.005*SL	0.46 + 0.005*SL
	t_{PHL}	2.29	1.76 + 0.007*SL	1.80 + 0.006*SL	1.83 + 0.006*SL
	t_R	1.09	0.13 + 0.012*SL	0.11 + 0.012*SL	0.10 + 0.012*SL
	t_F	1.24	0.58 + 0.008*SL	0.58 + 0.008*SL	0.57 + 0.008*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 PSCKDLD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.00	0.54 + 0.003*SL	0.55 + 0.003*SL	0.55 + 0.003*SL
	t_{PHL}	2.95	2.38 + 0.004*SL	2.43 + 0.003*SL	2.47 + 0.003*SL
	t_R	1.10	0.16 + 0.006*SL	0.15 + 0.006*SL	0.13 + 0.006*SL
	t_F	1.48	0.83 + 0.004*SL	0.85 + 0.004*SL	0.83 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 PSCKDLD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.93	0.48 + 0.001*SL	0.48 + 0.001*SL	0.48 + 0.001*SL
	t_{PHL}	2.53	2.00 + 0.002*SL	2.05 + 0.001*SL	2.08 + 0.001*SL
	t_R	1.08	0.14 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.36	0.73 + 0.002*SL	0.73 + 0.002*SL	0.72 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 PSCKDLD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.02	0.57 + 0.001*SL	0.58 + 0.001*SL	0.58 + 0.001*SL
	t_{PHL}	3.24	2.67 + 0.001*SL	2.72 + 0.001*SL	2.76 + 0.001*SL
	t_R	1.10	0.19 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.64	1.01 + 0.001*SL	1.03 + 0.001*SL	1.03 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

KG80 PSCKDLU2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.90	0.45 + 0.005*SL	0.45 + 0.005*SL	0.45 + 0.005*SL
	t_{PHL}	2.32	1.78 + 0.007*SL	1.83 + 0.006*SL	1.85 + 0.006*SL
	t_R	1.09	0.13 + 0.012*SL	0.11 + 0.012*SL	0.10 + 0.012*SL
	t_F	1.24	0.59 + 0.008*SL	0.58 + 0.008*SL	0.57 + 0.008*SL

*Group1 : SL < 56, *Group2 : 56 ≤ SL ≤ 83, *Group3 : 83 < SL

KG80 PSCKDLU4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.99	0.53 + 0.003*SL	0.54 + 0.003*SL	0.54 + 0.003*SL
	t_{PHL}	2.98	2.41 + 0.004*SL	2.47 + 0.003*SL	2.50 + 0.003*SL
	t_R	1.10	0.16 + 0.006*SL	0.15 + 0.006*SL	0.13 + 0.006*SL
	t_F	1.48	0.83 + 0.004*SL	0.85 + 0.004*SL	0.84 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≤ SL ≤ 164, *Group3 : 164 < SL

KG80 PSCKDLU8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.92	0.47 + 0.001*SL	0.47 + 0.001*SL	0.47 + 0.001*SL
	t_{PHL}	2.55	2.03 + 0.002*SL	2.07 + 0.001*SL	2.10 + 0.001*SL
	t_R	1.08	0.14 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.36	0.74 + 0.002*SL	0.74 + 0.002*SL	0.72 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≤ SL ≤ 325, *Group3 : 325 < SL

KG80 PSCKDLU12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

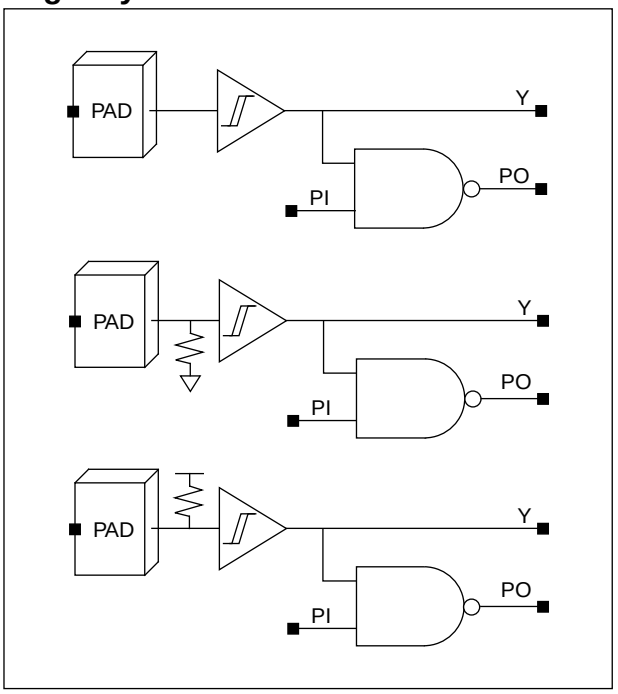
Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.01	0.56 + 0.001*SL	0.57 + 0.001*SL	0.57 + 0.001*SL
	t_{PHL}	3.27	2.70 + 0.001*SL	2.75 + 0.001*SL	2.79 + 0.001*SL
	t_R	1.10	0.18 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.65	1.02 + 0.001*SL	1.04 + 0.001*SL	1.04 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≤ SL ≤ 486, *Group3 : 486 < SL

Cell Availability

Library	5V Operation	3.3V Operation
KG80	PSCKDS(2/4/8/12) PSCKDSD(2/4/8/12) PSCKDSU(2/4/8/12)	–
KGM80	–	PSCKDS(2/4/6/8) PSCKDSD(2/4/6/8) PSCKDSU(2/4/6/8)

Logic Symbol



Input Load (SL)

KG80	
	PI
PSCKDS(2/4/8/12)	1.6
PSCKDSD(2/4/8/12)	1.6
PSCKDSU(2/4/8/12)	1.6
KGM80	
	PI
PSCKDS(2/4/6/8)	1.9
PSCKDSD(2/4/6/8)	1.9
PSCKDSU(2/4/6/8)	1.9

I/O Slot

KG80/KGM80	
PSCKDSy/PSCKDSDy/PSCKDSUy	1.0

KG80 PSCKDS2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.77	0.32 + 0.005*SL	0.31 + 0.006*SL	0.32 + 0.005*SL
	t_{PHL}	1.00	0.55 + 0.006*SL	0.57 + 0.005*SL	0.58 + 0.005*SL
	t_R	1.09	0.11 + 0.012*SL	0.10 + 0.012*SL	0.09 + 0.012*SL
	t_F	0.93	0.22 + 0.009*SL	0.21 + 0.009*SL	0.19 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 PSCKDS4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.88	0.43 + 0.003*SL	0.43 + 0.003*SL	0.43 + 0.003*SL
	t_{PHL}	1.27	0.79 + 0.003*SL	0.82 + 0.003*SL	0.84 + 0.003*SL
	t_R	1.09	0.15 + 0.006*SL	0.13 + 0.006*SL	0.12 + 0.006*SL
	t_F	1.02	0.35 + 0.004*SL	0.34 + 0.004*SL	0.32 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 PSCKDS8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.92	0.48 + 0.001*SL	0.48 + 0.001*SL	0.48 + 0.001*SL
	t_{PHL}	1.31	0.84 + 0.002*SL	0.87 + 0.001*SL	0.89 + 0.001*SL
	t_R	1.08	0.15 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.02	0.35 + 0.002*SL	0.34 + 0.002*SL	0.33 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 PSCKDS12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.04	0.59 + 0.001*SL	0.59 + 0.001*SL	0.60 + 0.001*SL
	t_{PHL}	1.58	1.08 + 0.001*SL	1.12 + 0.001*SL	1.14 + 0.001*SL
	t_R	1.11	0.19 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.14	0.49 + 0.001*SL	0.48 + 0.001*SL	0.47 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

KG80 PSCKDSD2 Switching Characteristics

[Delays for typical process, 25℃, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.33 + 0.005*SL	0.33 + 0.005*SL	0.33 + 0.005*SL
	t_{PHL}	1.01	0.56 + 0.006*SL	0.58 + 0.005*SL	0.59 + 0.005*SL
	t_R	1.09	0.11 + 0.012*SL	0.10 + 0.012*SL	0.09 + 0.012*SL
	t_F	0.93	0.22 + 0.009*SL	0.21 + 0.009*SL	0.19 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 PSCKDSD4 Switching Characteristics

[Delays for typical process, 25℃, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.89	0.44 + 0.003*SL	0.44 + 0.003*SL	0.44 + 0.003*SL
	t_{PHL}	1.28	0.81 + 0.003*SL	0.83 + 0.003*SL	0.85 + 0.003*SL
	t_R	1.09	0.15 + 0.006*SL	0.13 + 0.006*SL	0.12 + 0.006*SL
	t_F	1.02	0.35 + 0.004*SL	0.34 + 0.004*SL	0.33 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 PSCKDSD8 Switching Characteristics

[Delays for typical process, 25℃, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.94	0.49 + 0.001*SL	0.50 + 0.001*SL	0.50 + 0.001*SL
	t_{PHL}	1.33	0.85 + 0.001*SL	0.88 + 0.001*SL	0.90 + 0.001*SL
	t_R	1.08	0.15 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.02	0.35 + 0.002*SL	0.34 + 0.002*SL	0.33 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 PSCKDSD12 Switching Characteristics

[Delays for typical process, 25℃, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.06	0.60 + 0.001*SL	0.61 + 0.001*SL	0.61 + 0.001*SL
	t_{PHL}	1.59	1.10 + 0.001*SL	1.13 + 0.001*SL	1.15 + 0.001*SL
	t_R	1.11	0.19 + 0.002*SL	0.18 + 0.002*SL	0.16 + 0.002*SL
	t_F	1.14	0.48 + 0.001*SL	0.48 + 0.001*SL	0.47 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

KG80 PSCKDSU2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.32 + 0.005*SL	0.33 + 0.005*SL	0.32 + 0.005*SL
	t_{PHL}	1.01	0.56 + 0.006*SL	0.58 + 0.005*SL	0.58 + 0.005*SL
	t_R	1.09	0.11 + 0.012*SL	0.10 + 0.012*SL	0.09 + 0.012*SL
	t_F	0.93	0.22 + 0.009*SL	0.21 + 0.009*SL	0.20 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 PSCKDSU4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.89	0.44 + 0.003*SL	0.44 + 0.003*SL	0.44 + 0.003*SL
	t_{PHL}	1.28	0.80 + 0.003*SL	0.83 + 0.003*SL	0.85 + 0.003*SL
	t_R	1.09	0.15 + 0.006*SL	0.13 + 0.006*SL	0.12 + 0.006*SL
	t_F	1.03	0.35 + 0.004*SL	0.34 + 0.004*SL	0.33 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 PSCKDSU8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.93	0.48 + 0.001*SL	0.49 + 0.001*SL	0.49 + 0.001*SL
	t_{PHL}	1.33	0.85 + 0.002*SL	0.88 + 0.001*SL	0.90 + 0.001*SL
	t_R	1.08	0.15 + 0.003*SL	0.13 + 0.003*SL	0.12 + 0.003*SL
	t_F	1.02	0.35 + 0.002*SL	0.34 + 0.002*SL	0.33 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 PSCKDSU12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.05	0.59 + 0.001*SL	0.60 + 0.001*SL	0.61 + 0.001*SL
	t_{PHL}	1.60	1.10 + 0.001*SL	1.13 + 0.001*SL	1.16 + 0.001*SL
	t_R	1.11	0.19 + 0.002*SL	0.17 + 0.002*SL	0.15 + 0.002*SL
	t_F	1.14	0.49 + 0.001*SL	0.48 + 0.001*SL	0.47 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

KGM80 PSCKDS2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.48	0.62 + 0.004*SL	0.63 + 0.004*SL	0.63 + 0.004*SL
	t_{PHL}	2.03	1.28 + 0.004*SL	1.34 + 0.004*SL	1.37 + 0.003*SL
	t_R	2.01	0.23 + 0.009*SL	0.21 + 0.009*SL	0.18 + 0.009*SL
	t_F	1.52	0.39 + 0.006*SL	0.39 + 0.006*SL	0.42 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

KGM80 PSCKDS4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.73	0.84 + 0.002*SL	0.87 + 0.002*SL	0.88 + 0.002*SL
	t_{PHL}	2.70	1.86 + 0.002*SL	1.93 + 0.002*SL	1.99 + 0.002*SL
	t_R	2.07	0.32 + 0.005*SL	0.31 + 0.005*SL	0.30 + 0.005*SL
	t_F	1.74	0.62 + 0.003*SL	0.64 + 0.003*SL	0.64 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

KGM80 PSCKDS6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.62	0.75 + 0.002*SL	0.77 + 0.001*SL	0.78 + 0.001*SL
	t_{PHL}	2.37	1.57 + 0.001*SL	1.64 + 0.001*SL	1.68 + 0.001*SL
	t_R	2.03	0.28 + 0.003*SL	0.23 + 0.003*SL	0.24 + 0.003*SL
	t_F	1.61	0.51 + 0.002*SL	0.48 + 0.002*SL	0.49 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

KGM80 PSCKDS8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.74	0.86 + 0.001*SL	0.89 + 0.001*SL	0.90 + 0.001*SL
	t_{PHL}	2.70	1.87 + 0.001*SL	1.94 + 0.001*SL	2.00 + 0.001*SL
	t_R	2.06	0.30 + 0.002*SL	0.31 + 0.002*SL	0.28 + 0.002*SL
	t_F	1.72	0.61 + 0.001*SL	0.63 + 0.001*SL	0.63 + 0.001*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

KGM80 PSCKDSD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.50	0.63 + 0.004*SL	0.65 + 0.004*SL	0.65 + 0.004*SL
	t_{PHL}	2.05	1.30 + 0.004*SL	1.35 + 0.004*SL	1.39 + 0.003*SL
	t_R	2.01	0.23 + 0.009*SL	0.21 + 0.009*SL	0.18 + 0.009*SL
	t_F	1.51	0.39 + 0.006*SL	0.42 + 0.006*SL	0.37 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

KGM80 PSCKDSD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.74	0.85 + 0.002*SL	0.89 + 0.002*SL	0.91 + 0.002*SL
	t_{PHL}	2.72	1.88 + 0.002*SL	1.96 + 0.002*SL	2.01 + 0.002*SL
	t_R	2.07	0.31 + 0.005*SL	0.35 + 0.004*SL	0.28 + 0.005*SL
	t_F	1.73	0.63 + 0.003*SL	0.63 + 0.003*SL	0.62 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

KGM80 PSCKDSD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.63	0.76 + 0.002*SL	0.78 + 0.001*SL	0.79 + 0.001*SL
	t_{PHL}	2.39	1.59 + 0.001*SL	1.66 + 0.001*SL	1.70 + 0.001*SL
	t_R	2.03	0.26 + 0.003*SL	0.25 + 0.003*SL	0.22 + 0.003*SL
	t_F	1.62	0.51 + 0.002*SL	0.48 + 0.002*SL	0.50 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

KGM80 PSCKDSD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.76	0.87 + 0.001*SL	0.90 + 0.001*SL	0.91 + 0.001*SL
	t_{PHL}	2.72	1.88 + 0.001*SL	1.96 + 0.001*SL	2.02 + 0.001*SL
	t_R	2.06	0.32 + 0.002*SL	0.31 + 0.002*SL	0.26 + 0.002*SL
	t_F	1.72	0.64 + 0.001*SL	0.62 + 0.001*SL	0.60 + 0.001*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

KGM80 PSCKDSU2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 194	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.49	0.63 + 0.004*SL	0.64 + 0.004*SL	0.65 + 0.004*SL
	t_{PHL}	2.05	1.29 + 0.004*SL	1.35 + 0.004*SL	1.38 + 0.003*SL
	t_R	2.01	0.24 + 0.009*SL	0.19 + 0.009*SL	0.20 + 0.009*SL
	t_F	1.52	0.40 + 0.006*SL	0.41 + 0.006*SL	0.39 + 0.006*SL

*Group1 : SL < 130, *Group2 : 130 ≦SL≦ 194, *Group3 : 194 < SL

KGM80 PSCKDSU4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 385	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.74	0.85 + 0.002*SL	0.88 + 0.002*SL	0.89 + 0.002*SL
	t_{PHL}	2.72	1.88 + 0.002*SL	1.96 + 0.002*SL	2.02 + 0.002*SL
	t_R	2.06	0.32 + 0.005*SL	0.32 + 0.005*SL	0.28 + 0.005*SL
	t_F	1.74	0.64 + 0.003*SL	0.65 + 0.003*SL	0.63 + 0.003*SL

*Group1 : SL < 257, *Group2 : 257 ≦SL≦ 385, *Group3 : 385 < SL

KGM80 PSCKDSU6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 580	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.63	0.76 + 0.002*SL	0.78 + 0.001*SL	0.78 + 0.001*SL
	t_{PHL}	2.38	1.59 + 0.001*SL	1.66 + 0.001*SL	1.70 + 0.001*SL
	t_R	2.03	0.28 + 0.003*SL	0.23 + 0.003*SL	0.24 + 0.003*SL
	t_F	1.61	0.51 + 0.002*SL	0.49 + 0.002*SL	0.49 + 0.002*SL

*Group1 : SL < 386, *Group2 : 386 ≦SL≦ 580, *Group3 : 580 < SL

KGM80 PSCKDSU8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 770	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.75	0.87 + 0.001*SL	0.90 + 0.001*SL	0.91 + 0.001*SL
	t_{PHL}	2.72	1.88 + 0.001*SL	1.96 + 0.001*SL	2.02 + 0.001*SL
	t_R	2.06	0.30 + 0.002*SL	0.30 + 0.002*SL	0.27 + 0.002*SL
	t_F	1.72	0.62 + 0.001*SL	0.63 + 0.001*SL	0.61 + 0.001*SL

*Group1 : SL < 514, *Group2 : 514 ≦SL≦ 770, *Group3 : 770 < SL

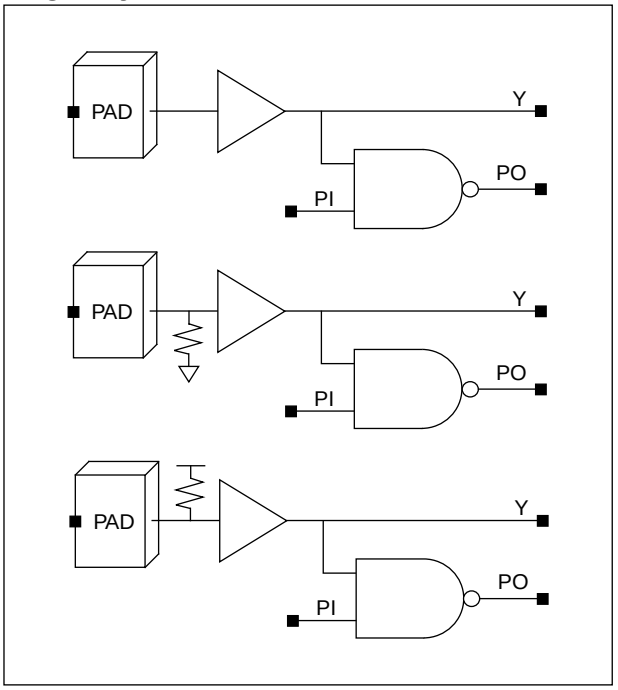
PSCKDTy/PSCKDTDy/PSCKDTUy

TTL Level Input Clock Drivers

Cell Availability

Library	5V Operation	3.3V Operation
KG80	PSCKDT(2/4/8/12) PSCKDTD(2/4/8/12) PSCKDTU(2/4/8/12)	–
KGM80	–	–

Logic Symbol



Input Load (SL)

KG80	
	PI
PSCKDT(2/4/8/12)	1.6
PSCKDTD(2/4/8/12)	1.6
PSCKDTU(2/4/8/12)	1.6

I/O Slot

KG80/KGM80	
PSCKDTy/PSCKDTDy/PSCKDTUy	1.0

KG80 PSCKDT2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.68	0.23 + 0.005*SL	0.22 + 0.006*SL	0.22 + 0.006*SL
	t_{PHL}	0.90	0.45 + 0.006*SL	0.47 + 0.005*SL	0.48 + 0.005*SL
	t_R	1.08	0.08 + 0.012*SL	0.08 + 0.012*SL	0.07 + 0.012*SL
	t_F	0.92	0.20 + 0.009*SL	0.19 + 0.009*SL	0.18 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≤ SL ≤ 83, *Group3 : 83 < SL

KG80 PSCKDT4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.72	0.27 + 0.003*SL	0.27 + 0.003*SL	0.27 + 0.003*SL
	t_{PHL}	1.13	0.65 + 0.003*SL	0.68 + 0.003*SL	0.70 + 0.003*SL
	t_R	1.06	0.08 + 0.006*SL	0.07 + 0.006*SL	0.07 + 0.006*SL
	t_F	1.01	0.33 + 0.004*SL	0.31 + 0.004*SL	0.31 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≤ SL ≤ 164, *Group3 : 164 < SL

KG80 PSCKDT8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.30 + 0.001*SL	0.30 + 0.001*SL	0.30 + 0.001*SL
	t_{PHL}	1.17	0.69 + 0.001*SL	0.72 + 0.001*SL	0.74 + 0.001*SL
	t_R	1.05	0.08 + 0.003*SL	0.07 + 0.003*SL	0.07 + 0.003*SL
	t_F	1.00	0.32 + 0.002*SL	0.32 + 0.002*SL	0.30 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≤ SL ≤ 325, *Group3 : 325 < SL

KG80 PSCKDT12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.34 + 0.001*SL	0.34 + 0.001*SL	0.34 + 0.001*SL
	t_{PHL}	1.39	0.89 + 0.001*SL	0.92 + 0.001*SL	0.95 + 0.001*SL
	t_R	1.05	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL
	t_F	1.12	0.45 + 0.001*SL	0.45 + 0.001*SL	0.44 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≤ SL ≤ 486, *Group3 : 486 < SL

KG80 PSCKDTD2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.70	0.24 + 0.005*SL	0.24 + 0.006*SL	0.24 + 0.005*SL
	t_{PHL}	0.91	0.46 + 0.006*SL	0.48 + 0.005*SL	0.49 + 0.005*SL
	t_R	1.08	0.08 + 0.012*SL	0.08 + 0.012*SL	0.07 + 0.012*SL
	t_F	0.92	0.20 + 0.009*SL	0.20 + 0.009*SL	0.18 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦SL≦ 83, *Group3 : 83 < SL

KG80 PSCKDTD4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.73	0.28 + 0.003*SL	0.28 + 0.003*SL	0.28 + 0.003*SL
	t_{PHL}	1.14	0.66 + 0.003*SL	0.69 + 0.003*SL	0.71 + 0.003*SL
	t_R	1.06	0.08 + 0.006*SL	0.07 + 0.006*SL	0.07 + 0.006*SL
	t_F	1.01	0.33 + 0.004*SL	0.32 + 0.004*SL	0.31 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦SL≦ 164, *Group3 : 164 < SL

KG80 PSCKDTD8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.76	0.32 + 0.001*SL	0.31 + 0.001*SL	0.31 + 0.001*SL
	t_{PHL}	1.18	0.70 + 0.002*SL	0.73 + 0.001*SL	0.75 + 0.001*SL
	t_R	1.05	0.09 + 0.003*SL	0.07 + 0.003*SL	0.07 + 0.003*SL
	t_F	1.00	0.32 + 0.002*SL	0.32 + 0.002*SL	0.31 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦SL≦ 325, *Group3 : 325 < SL

KG80 PSCKDTD12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.80	0.35 + 0.001*SL	0.35 + 0.001*SL	0.35 + 0.001*SL
	t_{PHL}	1.40	0.90 + 0.001*SL	0.93 + 0.001*SL	0.95 + 0.001*SL
	t_R	1.05	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL
	t_F	1.12	0.45 + 0.001*SL	0.45 + 0.001*SL	0.43 + 0.001*SL

*Group1 : SL < 324, *Group2 : 324 ≦SL≦ 486, *Group3 : 486 < SL

KG80 PSCKDTU2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 83	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.68	0.23 + 0.005*SL	0.22 + 0.006*SL	0.23 + 0.005*SL
	t_{PHL}	0.91	0.46 + 0.006*SL	0.48 + 0.005*SL	0.49 + 0.005*SL
	t_R	1.08	0.08 + 0.012*SL	0.07 + 0.012*SL	0.07 + 0.012*SL
	t_F	0.92	0.20 + 0.009*SL	0.19 + 0.009*SL	0.19 + 0.009*SL

*Group1 : SL < 56, *Group2 : 56 ≦ SL ≦ 83, *Group3 : 83 < SL

KG80 PSCKDTU4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 164	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.72	0.27 + 0.003*SL	0.27 + 0.003*SL	0.27 + 0.003*SL
	t_{PHL}	1.14	0.66 + 0.003*SL	0.69 + 0.003*SL	0.71 + 0.003*SL
	t_R	1.06	0.08 + 0.006*SL	0.07 + 0.006*SL	0.07 + 0.006*SL
	t_F	1.01	0.33 + 0.004*SL	0.32 + 0.004*SL	0.31 + 0.004*SL

*Group1 : SL < 109, *Group2 : 109 ≦ SL ≦ 164, *Group3 : 164 < SL

KG80 PSCKDTU8 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 325	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.30 + 0.001*SL	0.30 + 0.001*SL	0.30 + 0.001*SL
	t_{PHL}	1.18	0.70 + 0.002*SL	0.73 + 0.001*SL	0.75 + 0.001*SL
	t_R	1.05	0.08 + 0.003*SL	0.07 + 0.003*SL	0.07 + 0.003*SL
	t_F	1.01	0.33 + 0.002*SL	0.32 + 0.002*SL	0.31 + 0.002*SL

*Group1 : SL < 217, *Group2 : 217 ≦ SL ≦ 325, *Group3 : 325 < SL

KG80 PSCKDTU12 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 486	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.78	0.34 + 0.001*SL	0.34 + 0.001*SL	0.34 + 0.001*SL
	t_{PHL}	1.40	0.90 + 0.001*SL	0.93 + 0.001*SL	0.96 + 0.001*SL
	t_R	1.05	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL
	t_F	1.12	0.46 + 0.001*SL	0.45 + 0.001*SL	0.44 + 0.001*SL

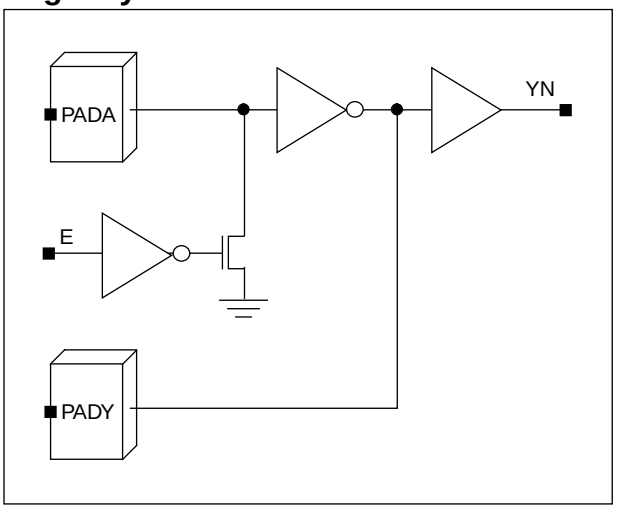
*Group1 : SL < 324, *Group2 : 324 ≦ SL ≦ 486, *Group3 : 486 < SL

OSCILLATORS

Cell List

Cell Name	Function Description
KG80	
PSOSCM1	Oscillator with Enable (1M ~ 10MHz)
PSOSCM2	Oscillator with Enable (10M ~ 30MHz)
PSOSCM3	Oscillator with Enable (30M ~ 60MHz)
PSOSCM4	Oscillator with Enable (60M ~ 80MHz)
PSOSCM5	Oscillator with Enable (80M ~ 100MHz)
PSOSCM6	Oscillator with Enable (50M ~ 100MHz)
KGM80	
PSOSCM1	Oscillator with Enable (1M ~ 10MHz)
PSOSCM2	Oscillator with Enable (10M ~ 30MHz)
PSOSCM3	Oscillator with Enable (30M ~ 60MHz)
PSOSCM4	Oscillator with Enable (60M ~ 80MHz)
PSOSCM5	Oscillator with Enable (80M ~ 100MHz)

Logic Symbol



Truth Table

SEC Tester Standard

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	x	x
1	1	0	0

Real Application

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Input Load (SL)

KG80	
	E
PSOSCM(1/2/3/4/5/6)	2.7
KGM80	
	E
PSOSCM(1/2/3/4/5)	2.7

I/O Slot

KG80	
PSOSCM(1/2/3/4/5/6)	2.0
KGM80	
PSOSCM(1/2/3/4/5)	2.0

KG80 PSOSCM1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.67	0.12 + 0.051*CL	0.11 + 0.051*CL	0.11 + 0.051*CL
	t_{PHL}	4.01	0.14 + 0.078*CL	0.13 + 0.078*CL	0.13 + 0.078*CL
	t_R	5.88	0.11 + 0.115*CL	0.10 + 0.115*CL	0.10 + 0.116*CL
	t_F	8.21	0.13 + 0.162*CL	0.13 + 0.162*CL	0.13 + 0.162*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PSOSCM1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.21	0.21 + 0.003*SL	0.21 + 0.002*SL	0.19 + 0.004*SL
	t_{PHL}	0.25	0.25 + 0.006*SL	0.26 + 0.004*SL	0.25 + 0.005*SL
	t_R	0.08	0.08 + 0.004*SL	0.09 + 0.004*SL	0.10 + 0.002*SL
	t_F	0.07	0.07 + 0.007*SL	0.08 + 0.003*SL	0.08 + 0.003*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PSOSCM2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.67	0.12 + 0.051*CL	0.11 + 0.051*CL	0.11 + 0.051*CL
	t_{PHL}	4.01	0.14 + 0.078*CL	0.13 + 0.078*CL	0.13 + 0.078*CL
	t_R	5.88	0.11 + 0.115*CL	0.10 + 0.115*CL	0.10 + 0.116*CL
	t_F	8.21	0.13 + 0.162*CL	0.13 + 0.162*CL	0.13 + 0.162*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PSOSCM2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.21	0.21 + 0.003*SL	0.21 + 0.002*SL	0.19 + 0.004*SL
	t_{PHL}	0.25	0.25 + 0.006*SL	0.26 + 0.004*SL	0.25 + 0.005*SL
	t_R	0.08	0.08 + 0.004*SL	0.09 + 0.004*SL	0.10 + 0.002*SL
	t_F	0.07	0.07 + 0.007*SL	0.08 + 0.003*SL	0.08 + 0.003*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PSOSCM3 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	1.38	0.11 + 0.026*CL	0.11 + 0.025*CL	0.10 + 0.026*CL
	t_{PHL}	2.06	0.13 + 0.039*CL	0.12 + 0.039*CL	0.12 + 0.039*CL
	t_R	2.98	0.11 + 0.057*CL	0.10 + 0.058*CL	0.10 + 0.058*CL
	t_F	4.14	0.11 + 0.081*CL	0.11 + 0.081*CL	0.10 + 0.081*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PSOSCM3 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.19	0.19 + 0.003*SL	0.19 + 0.003*SL	0.19 + 0.003*SL
	t_{PHL}	0.23	0.23 + 0.003*SL	0.23 + 0.004*SL	0.23 + 0.004*SL
	t_R	0.10	0.10 + -0.001*SL	0.09 + 0.001*SL	0.08 + 0.003*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.003*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PSOSCM4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.74	0.11 + 0.013*CL	0.10 + 0.013*CL	0.10 + 0.013*CL
	t_{PHL}	1.09	0.13 + 0.019*CL	0.12 + 0.019*CL	0.12 + 0.019*CL
	t_R	1.55	0.13 + 0.028*CL	0.11 + 0.029*CL	0.11 + 0.029*CL
	t_F	2.12	0.12 + 0.040*CL	0.11 + 0.040*CL	0.11 + 0.040*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PSOSCM4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.20	0.20 + 0.002*SL	0.21 + 0.002*SL	0.21 + 0.002*SL
	t_{PHL}	0.25	0.25 + 0.003*SL	0.25 + 0.002*SL	0.25 + 0.002*SL
	t_R	0.10	0.10 + 0.002*SL	0.10 + 0.001*SL	0.10 + 0.001*SL
	t_F	0.08	0.08 + 0.002*SL	0.08 + 0.003*SL	0.09 + 0.002*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PSOSCM5 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.53	0.10 + 0.009*CL	0.11 + 0.008*CL	0.11 + 0.008*CL
	t_{PHL}	0.77	0.13 + 0.013*CL	0.13 + 0.013*CL	0.12 + 0.013*CL
	t_R	1.08	0.15 + 0.019*CL	0.13 + 0.019*CL	0.13 + 0.019*CL
	t_F	1.45	0.13 + 0.027*CL	0.12 + 0.027*CL	0.11 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PSOSCM5 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.20	0.20 + 0.001*SL	0.20 + 0.002*SL	0.20 + 0.001*SL
	t_{PHL}	0.24	0.24 + 0.002*SL	0.24 + 0.002*SL	0.24 + 0.002*SL
	t_R	0.10	0.10 + 0.001*SL	0.10 + 0.001*SL	0.10 + 0.001*SL
	t_F	0.08	0.08 + 0.001*SL	0.08 + 0.002*SL	0.08 + 0.002*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KG80 PSOSCM6 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.42	0.09 + 0.006*CL	0.10 + 0.006*CL	0.11 + 0.006*CL
	t_{PHL}	0.61	0.12 + 0.010*CL	0.13 + 0.010*CL	0.13 + 0.010*CL
	t_R	0.85	0.16 + 0.014*CL	0.14 + 0.014*CL	0.14 + 0.014*CL
	t_F	1.12	0.14 + 0.020*CL	0.12 + 0.020*CL	0.12 + 0.020*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KG80 PSOSCM6 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.50ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_{PHL}	0.27	0.27 + 0.001*SL	0.27 + 0.001*SL	0.27 + 0.001*SL
	t_R	0.12	0.12 + 0.001*SL	0.12 + 0.001*SL	0.12 + 0.001*SL
	t_F	0.10	0.10 + 0.001*SL	0.10 + 0.001*SL	0.10 + 0.001*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

KGM80 PSOSCM1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PSOSCM1 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.23 + 0.005*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.10 + 0.001*SL	0.08 + 0.004*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.004*SL	0.09 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 6, *Group3 : 6 < SL

KGM80 PSOSCM2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PSOSCM2 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.23 + 0.005*SL	0.24 + 0.003*SL
	t_R	0.10	0.10 + 0.001*SL	0.10 + 0.001*SL	0.08 + 0.004*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.004*SL	0.09 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 6, *Group3 : 6 < SL

KGM80 PSOSCM3 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	1.41	0.12 + 0.026*CL	0.12 + 0.026*CL	0.12 + 0.026*CL
	t_{PHL}	1.87	0.12 + 0.035*CL	0.12 + 0.035*CL	0.12 + 0.035*CL
	t_R	3.00	0.10 + 0.058*CL	0.09 + 0.058*CL	0.09 + 0.058*CL
	t_F	3.96	0.11 + 0.077*CL	0.11 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PSOSCM3 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.19	0.19 + 0.003*SL	0.19 + 0.002*SL	0.19 + 0.002*SL
	t_{PHL}	0.21	0.21 + 0.002*SL	0.21 + 0.003*SL	0.22 + 0.002*SL
	t_R	0.10	0.10 + 0.002*SL	0.09 + 0.003*SL	0.11 + 0.001*SL
	t_F	0.08	0.08 + 0.004*SL	0.09 + 0.001*SL	0.10 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 6, *Group3 : 6 < SL

KGM80 PSOSCM4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.76	0.12 + 0.013*CL	0.12 + 0.013*CL	0.12 + 0.013*CL
	t_{PHL}	0.99	0.12 + 0.017*CL	0.11 + 0.017*CL	0.12 + 0.017*CL
	t_R	1.54	0.10 + 0.029*CL	0.09 + 0.029*CL	0.09 + 0.029*CL
	t_F	2.02	0.10 + 0.038*CL	0.10 + 0.038*CL	0.10 + 0.038*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PSOSCM4 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.000*SL	0.11 + 0.000*SL	0.11 + 0.001*SL
	t_F	0.09	0.09 + 0.001*SL	0.09 + 0.000*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 6, *Group3 : 6 < SL

KGM80 PSOSCM5 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.55	0.11 + 0.009*CL	0.11 + 0.009*CL	0.12 + 0.009*CL
	t_{PHL}	0.70	0.12 + 0.012*CL	0.12 + 0.012*CL	0.11 + 0.012*CL
	t_R	1.06	0.10 + 0.019*CL	0.09 + 0.019*CL	0.09 + 0.019*CL
	t_F	1.38	0.10 + 0.025*CL	0.10 + 0.026*CL	0.09 + 0.026*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

KGM80 PSOSCM5 Switching Characteristics

[Delays for typical process, 25°C, 5.0V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.000*SL	0.11 + 0.000*SL
	t_F	0.10	0.10 + 0.001*SL	0.10 + 0.000*SL	0.10 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 6, *Group3 : 6 < SL

Overview

PCI buffers are designed for PCI local bus application which is an industry-standard, high-performance 32- or 64-bit bus architecture.

SEC ASIC supports 5V and 3.3V signalling environment PCI bi-directional buffers including a Universal buffer. The Universal buffer requires a select control (EN3V) signal. EN3V pin should be tied to the Voltage Detector output directly.

Features

– High performance
– Low cost
– Easy use
– Longevity: both 5V and 3.3V signalling environments specified.

General Description

The PCI buffer's signalling environment is controlled by EN3V pin which is logically low in a 5V operation and logically high in a 3.3V operation. If you use a Voltage Detector cell with the PCI buffer, you have to connect this EN3V pin to VDET (Voltage Detector) output. Do not use a Level Shifter buffer (PLSCB).

Cell List

Cell Name	Function Description
KG80	
PSIPCIA	5V PCI Input Buffer
PSOPCIA	5V PCI Output Buffer
PLSIPCIA	Internal 5V/External 3.3V PCI Input Buffer
PLSOPCIA	Internal 5V/External 3.3V PCI Output Buffer
PSIPCIAU	Universal PCI Input Buffer
PSOPCIAU	Universal PCI Output Buffer
KGM80	
PSIPCIA3	3.3V PCI Input Buffer
PSOPCIA3	3.3V PCI Output Buffer
PHSIPCIA	Internal 3.3V/External 5V PCI Input Buffer
PHSOPCIA	Internal 3.3V/External 5V PCI Output Buffer
PSIPCIAU	Universal PCI Input Buffer
PSOPCIAU	Universal PCI Output Buffer

Electrical Characteristics

SEC ASIC guarantees PCI buffer's electrical characteristics under all conditions (V_{CC} = 3.6V, Temp. = 0°C ~ V_{CC} = 3.0V, Temp. = 125°C).

5V DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IL}	Input Low Voltage		–0.5	0.8	
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	µA
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	
V_{OL}	Output Low Voltage	I_{OUT} = 3mA, 6mA		0.55	V
V_{OH}	Output High Voltage	I_{OUT} = –2mA	2.4		
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	
C_{IDSEL}	IDSEL Pin Capacitance			8	
L_{PIN}	Pin Inductance			20	nH

5V AC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
$I_{OH\ (AC)}$	Switching Current High	$0 < V_{OUT} \leq 1.4$	–44		mA
		$1.4 < V_{OUT} < 2.4$	–44 (VOUT – 1.4) / 0.024		
		$3.1 < V_{OUT} < V_{CC}$		Eqt'n A[1]	
	(Test Point)	V_{OUT} = 3.1		–142	
$I_{OL\ (AC)}$	Switching Current Low	$V_{OUT} \geq 2.2$	95		
		$2.2 > V_{OUT} > 0.55$	V_{OUT}/0.023		
		$0.71 > V_{OUT} > 0$		Eqt'n B[2]	
	(Test Point)	V_{OUT} = 0.71		206	
I_{CL}	Low Clamp Current	$–5 < V_{IN} \leq –1$	$–25 + (V_{IN} + 1) / 0.015$		
$Slew_R$[3]	Output Rise Slew Rate	0.4V to 2.4V load	1	5	V/ns
$Slew_F$[3]	Output Fall Slew Rate	2.4V to 0.4V load	1	5	

NOTES:

1. **Equation A**: $I_{OH} = 11.9 * (V_{OUT} – 5.25) * (V_{OUT} + 2.45)$ for $V_{CC} > V_{OUT} > 3.1v$
2. **Equation B**: $I_{OL} = 78.5 * V_{OUT} * (4.4 – V_{OUT})$ for $0v < V_{OUT} < 0.71v$
3. The minimum slew rate (slowest signal edge) is guaranteed. The maximum slew rate (fastest signal edge) is a guideline, and rise and fall times faster than the maximum can occur.
   Designers should ensure that signal integrity modelling includes the potential for rise and fall times faster than the maximum shown in the table.

3.3V DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage		3.0	3.6	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.5V_{CC}$	V_{CC} + 0.5	V
V_{IPU}	Input Pull-Up Voltage		$0.7V_{CC}$		V
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CC}$		±10	µA
V_{OL}	Output Low Voltage	I_{OUT} = 1500µA		$0.1V_{CC}$	V
V_{OH}	Output High Voltage	I_{OUT} = –500µA	$0.9V_{CC}$		V
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance			8	pF
L_{PIN}	Pin Inductance			20	nH

3.3V AC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$I_{OH (AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CC}$	$-12V_{CC}$		mA
		$0.3V_{CC} < V_{OUT} < 0.9V_{CC}$	$-17.1 (V_{CC} - V_{OUT})$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}$		Eqt'n C[1]	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$		$-32V_{CC}$	mA
$I_{OL (AC)}$	Switching Current Low	$V_{CC} > V_{OUT} \geq 0.6V_{CC}$	$16V_{CC}$		mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}$	$26.7V_{OUT}$		mA
		$0.18V_{CC} > V_{OUT} > 0$		Eqt'n D[2]	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$		$38V_{CC}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High Clamp Current	$V_{CC} + 4 > V_{IN} \geq V_{CC} + 1$	$25 + (V_{IN} - V_{CC} - 1) / 0.015$		mA
$Slew_R$[3]	Output Rise Slew Rate	$0.2V_{CC}$ to $0.6V_{CC}$ load	1	4	V/ns
$Slew_F$[3]	Output Fall Slew Rate	$0.6V_{CC}$ to $0.2V_{CC}$ load	1	4	V/ns

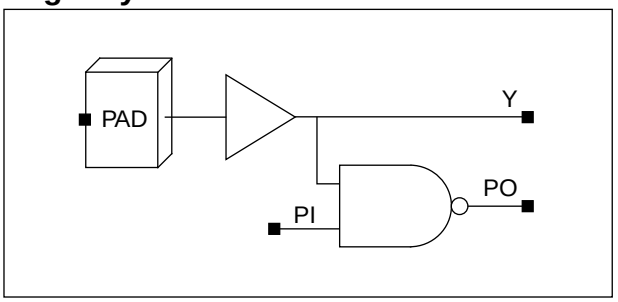
NOTES:

1. **Equation C**: $I_{OH} = (98.0 / V_{CC}) * (V_{OUT} - V_{CC}) * (V_{OUT} + 0.4V_{CC})$ for $V_{CC} > V_{OUT} > 0.7v$
2. **Equation D**: $I_{OL} = (256 / V_{CC}) * V_{OUT} * (V_{CC} - V_{OUT})$ for $0v < V_{OUT} < 0.18V_{CC}$
3. The minimum slew rate (slowest signal edge) is guaranteed. The maximum slew rate (fastest signal edge) is a guideline, and rise and fall times faster than the maximum can occur.
   Designers should ensure that signal integrity modelling includes the potential for rise and fall times faster than the maximum shown in the table.

PSIPCIA/PLSIPCIA/PSIPCIA3/PHSIPCIA

PCI Input Buffers

Logic Symbol



Input Load (SL)

KG80				
	TN	EN	A	PI
PSIPCIA/PLSIPCIA	1.0	1.6	3.6	1.0
KGM80				
	TN	EN	A	PI
PSIPCIA3/PHSIPCIA	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

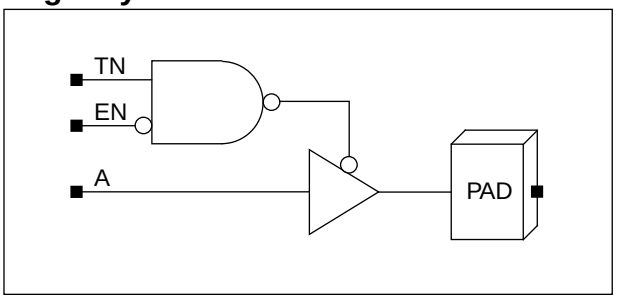
Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

I/O Slot

KG80/KGM80	
PSIPCIA/PLSIPCIA PSIPCIA3/PHSIPCIA	1.0

Logic Symbol



Input Load (SL)

KG80				
	TN	EN	A	PI
PSOPCIA/PLSOPCIA	1.0	1.6	3.6	1.0
KGM80				
	TN	EN	A	PI
PSOPCIA3/PHSOPCIA	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

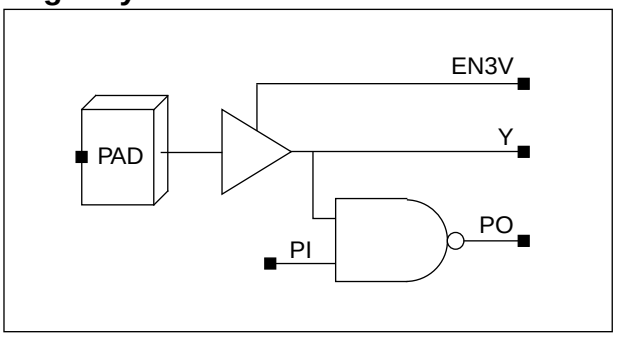
I/O Slot

KG80/KGM80	
PSOPCIA/PLSOPCIA PSOPCIA3/PHSOPCIA	1.0

PSIPCIAU

Universal PCI Input Buffer

Logic Symbol



Input Load (SL)

KG80/KGM80				
	TN	EN	A	PI
PSIPCIAU	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

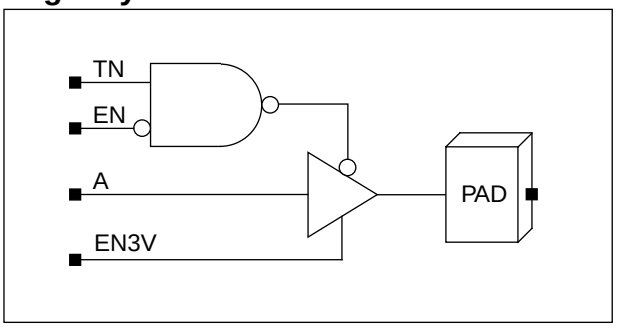
A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* EN3V (active-high) enables the 3.3V mode.

I/O Slot

KG80/KGM80	
PSIPCIAU	1.0

Logic Symbol



Input Load (SL)

KG80/KGM80				
	TN	EN	A	PI
PSOPCIAU	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* EN3V (active-high) enables the 3.3V mode.

I/O Slot

KG80/KGM80	
PSOPCIAU	1.0

PCMCIA BUFFERS

Overview

PC card technology is used in a wide variety of products including notebook computers, palmtop computers, pen computers, desktop computers, printers, telephones, medical instruments and others embedded application hosts.

For PCMCIA interface, SEC ASIC supports various kinds of PCMCIA buffers.
These PCMCIA buffers enable you to

– Maintain interface conditions and speed independent of Battery Voltage
– Allow groups of card interface input buffers to be powered down
– Use a Voltage Detector cell
– Select pull-up/pull-down option (50K/100K/200K, default = 100K).

General Description

All of PCMCIA buffers are controlled by S3V5V signal that is logically low in a 5V operation and logically high in a 3.3V operation. If you use a Voltage Detector cell with a PCMCIA buffer, you have to connect the S3V5V pin to VDET (Voltage Detector) output.

Logic Levels

Parameter	Min	Max
V_{IH}	2.0V	
V_{IL}		0.8V
V_{OH}	2.4V	
V_{OL}		0.5V

NOTES:

1. PCMCIA input buffer is TTL compatible.
2. PCMCIA output buffer has a balanced T_R & T_F.

Cell List

Cell Name	Function Description
KG80/KGM80	
PVIC(5/3)	5V/3.3V CMOS Level PCMCIA Input Buffers
PVIL(5/3)	5V/3.3V TTL Schmitt Trigger Level PCMCIA Input Buffers
PVILD(5/3)	5V/3.3V TTL Schmitt Trigger Level PCMCIA Input Buffers with Pull-Down
PVILU(5/3)	5V/3.3V TTL Schmitt Trigger Level PCMCIA Input Buffers with Pull-Up
PVIT(5/3)	5V/3.3V TTL Level PCMCIA Input Buffers
PVITD(5/3)	5V/3.3V TTL Level PCMCIA Input Buffers with Pull-Down
PVITU(5/3)	5V/3.3V TTL Level PCMCIA Input Buffers with Pull-Up
PVOB4(5/3)	5V/3.3V 4mA PCMCIA Output Buffers without SRC
PVOB8(5/3)	5V/3.3V 8mA PCMCIA Output Buffers without SRC
PVOB12(5/3)	5V/3.3V 12mA PCMCIA Output Buffers without SRC
PVOD4(5/3)	5V/3.3V 4mA Open-Drain PCMCIA Output Buffers without SRC
PVOD8(5/3)	5V/3.3V 8mA Open-Drain PCMCIA Output Buffers without SRC
PVOD12(5/3)	5V/3.3V 12mA Open-Drain PCMCIA Output Buffers without SRC
PVOT4(5/3)	5V/3.3V 4mA Tri-State PCMCIA Output Buffers without SRC
PVOT8(5/3)	5V/3.3V 8mA Tri-State PCMCIA Output Buffers without SRC
PVOT12(5/3)	5V/3.3V 12mA Tri-State PCMCIA Output Buffers without SRC
PVOT8SM(5/3)	5V/3.3V 8mA Tri-State PCMCIA Output Buffers with SRC
PVOT12SM(5/3)	5V/3.3V 12mA Tri-State PCMCIA Output Buffers with SRC
PVBTT4(5/3)	5V/3.3V 4mA PCMCIA Bi-Directional Buffers without SRC
PVBTT8(5/3)	5V/3.3V 8mA PCMCIA Bi-Directional Buffers without SRC
PVBTT12(5/3)	5V/3.3V 12mA PCMCIA Bi-Directional Buffers without SRC
PVBTDT8SM(5/3)	5V/3.3V 8mA PCMCIA Bi-Directional Buffers with SRC, Pull-Down
PVBCT8SM(5/3)	5V/3.3V 8mA PCMCIA Bi-Directional Buffers with SRC

PCMCIA BUFFERS

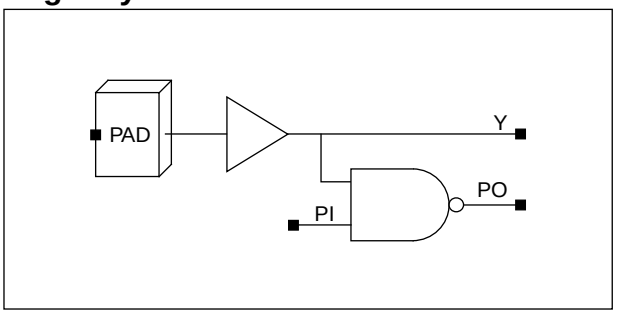
Naming Conventions

PCMCIA Input Buffers (PVI a b v)			
PCMCIA Output Buffers (PVO x y z v)			
PCMCIA Bi-Directional Buffers (PVB a b x y z v)			
a		**b**	
C	CMOS level	None	No resistor
L	TTL Schmitt trigger level	D	Pull-down resistor
S	CMOS Schmitt trigger level	U	Pull-up resistor
T	TTL level	**y**	
x		4	4mA drive
B	Normal buffer	8	8mA drive
D	Open-drain buffer	12	12mA drive
T	Tri-state buffer	**v**	
z		5	5V
None	No slew-rate control (fastest)	3	3.3V
SM	Medium slew-rate control		
SH	High slew-rate control		

PVIC(5/3)

CMOS Level PCMCIA Input Buffers

Logic Symbol



Pin Connection

Input	Output
PAD	Y
PI	PO

Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

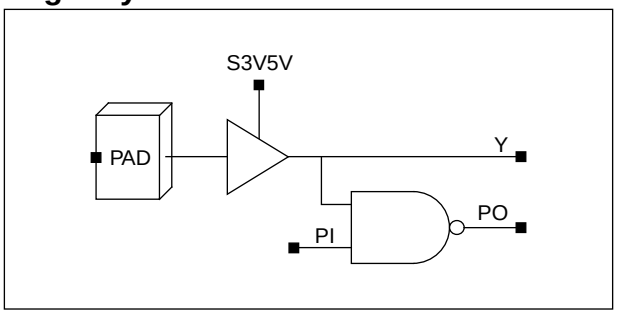
Cell Availability

5V Operation	3.3V Operation
PVIC5	PVIC3

PVIL(D/U)(5/3)/PVIT(D/U)(5/3)

TTL Level PCMCIA Input Buffers

Logic Symbol



Pin Connection

Input	Output
PAD	Y
PI	PO
S3V5V	

Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

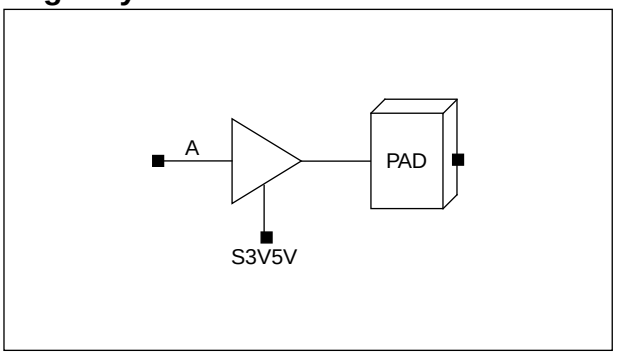
Cell Availability

5V Operation	3.3V Operation
PVIL5	PVIL3
PVILD5	PVILD3
PVILU5	PVILU3
PVIT5	PVIT3
PVITD5	PVITD3
PVITU5	PVITU3

PVOB(4/8/12)(5/3)

PCMCIA Output Buffers

Logic Symbol



Pin Connection

Input	Output
A S3V5V	PAD

Truth Table

A	PAD
0	0
1	1

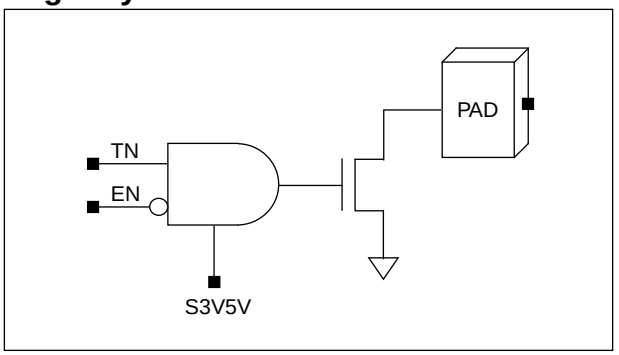
Cell Availability

5V Operation	3.3V Operation
PVOB45	PVOB43
PVOB85	PVOB83
PVOB125	PVOB123

PVOD(4/8/12)(5/3)

Open Drain PCMCIA Output Buffers

Logic Symbol



Pin Connection

Input	Output
TN EN S3V5V	PAD

Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

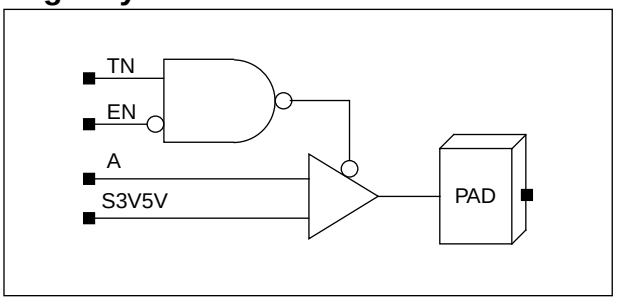
Cell Availability

5V Operation	3.3V Operation
PVOD45	PVOD43
PVOD85	PVOD83
PVOD125	PVOD123

PVOT(4/8/12)(5/3)

Tri-State PCMCIA Output Buffers

Logic Symbol



Pin Connection

Input	Output
TN	PAD
EN	
A	
S3V5V	

Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

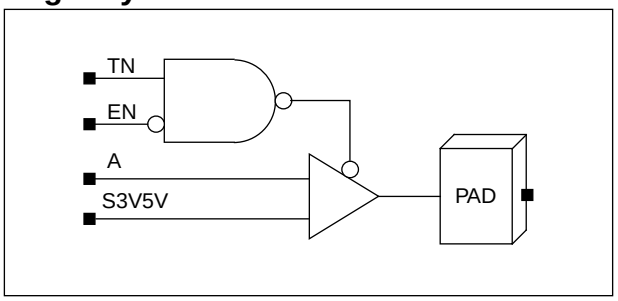
Cell Availability

5V Operation	3.3V Operation
PVOT45	PVOT43
PVOT85	PVOT83
PVOT125	PVOT123

PVOT(8/12)SM(5/3)

Tri-State PCMCIA Output Buffers

Logic Symbol



Pin Connection

Input	Output
TN	PAD
EN	
A	
S3V5V	

Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

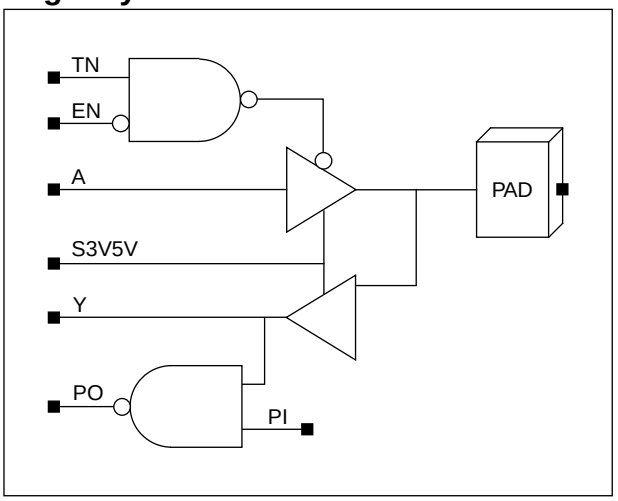
Cell Availability

5V Operation	3.3V Operation
PVOT8SM5	PVOT8SM3
PVOT12SM5	PVOT12SM3

PVBTT(4/8/12)(5/3)

PCMCIA Bi-Directional Buffers

Logic Symbol



Pin Connection

Input	Output
TN	PAD
EN	Y
A	PO
S3V5V	
PI	

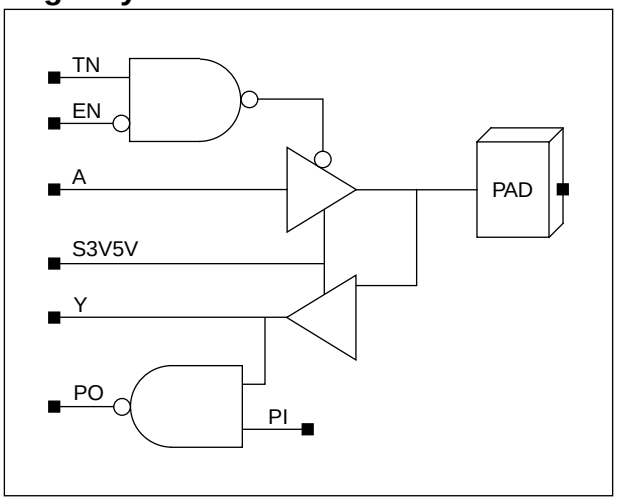
Cell Availability

5V Operation	3.3V Operation
PVBTT45	PVBTT43
PVBTT85	PVBTT83
PVBTT125	PVBTT123

PVBTDT8SM/PVBCT8SM(5/3)

PCMCIA Bi-Directional Buffers

Logic Symbol



Pin Connection

Input	Output
TN	PAD
EN	Y
A	PO
S3V5V	
PI	

Cell Availability

5V Operation	3.3V Operation
PVBTDT8SM5	PVBTDT8SM3
PVBCT8SM5	PVBCT8SM3

Overview

CardBus I/O buffers have 3.3V operation, 32-bit bus width and 33MHz of transmission speed. The latest version of the PC card standard adds information to improve compatibility with the standard by requiring a Card Information Structure (CIS) on every PC card.

The standard has also been enhanced to support the following optional features:

– Low-Voltage Only Operation (3.3V)
– Hardware Direct Memory Access (DMA)
– Multiple-Function Cards
– Industry Standard Power Management Interface (APM)
– High Throughput 32-Bit Bus Mastering Interface (CardBus)

SEC ASIC supports nine different CardBus I/O buffers. If necessary, a Voltage Detector cell can be used with them. For maximum flexibility, CardBus I/O buffers have not only a Level Shifter but also a pull-up enable control pin.

CardBus I/O buffers have only 3.3V electrical specifications, however, we can support 5V/3.3V flexible operation by using of a level shifter. Regardless of the I/O voltage, S3V5V pin controls the same input level and output driving current. S3V5V pin should be tied to the voltage detector in a mixed system, or ground in a 3.3V-only system.

We can not attribute a level shifter to PUEN (Pull-Up Enable) pin, because we have only four level shifters. In order to control the PUEN pin with an internal signal, you should use the level shifter butter (PLSCB) in a mixed system.

For minimizing power consumption, CardBus I/O buffers have a nand type input with a control pin. Therefore, the input buffers operate as active-high input buffers. However, if the control pin is in low state, the output Y is low and not tri-state.

General Description

The CardBus I/O buffer is controlled by S3V5V signal that is logically low in a 5V operation and logically high in a 3.3V operation. If you use a voltage detector cell with the CardBus I/O buffer, you have to connect this S3V5V pin to VDET (voltage detector) output. Do not use a level shifter buffer (PLSCB).

CSTSCHG Buffer Specification

The CSTSCHG pin can be used by the CardBus PC card to remotely power up the system. The design of the CardBus PC card's output buffer and the system's input buffer must ensure no electrical damage results.

– An output buffer for CSTSCHG pin never exceed 1mA.
– An input buffer for CSTSCHG pin is able to withstand sustained forward bias current of 1mA.

CCLK Specification

The electrical characteristics of CCLK follows 3.3V signalling of PCI Local bus specification Revision 2.1. Refer to the PCI buffer electrical characteristics.

CARDBUS I/O BUFFERS

Cell List

Cell Name	Function Description
KG80	
PLITCBU	3.3V Interface Universal TTL CardBus Input Buffer with Pull-Up
PLOTCBU	3.3V Interface Tri-State CardBus Output Buffer with Pull-Up
PLOTCCKCBU	3.3V Interface Tri-State CardBus Output Clock Driver with Pull-Up
PLOTCVSCBU	3.3V Interface Tri-State Output Card Voltage Sense with Pull-Up
PLODCCKCBU	3.3V Interface Open Drain CardBus Output Clock Driver with Pull-Up
PLBTTCBU	3.3V Interface Tri-State CardBus Bi-Directional Buffer with Pull-Up
PLBTCCKCBU	3.3V Interface CardBus Bi-Directional Clock Driver with Pull-Up
PLBTCVSCBU	3.3V Interface Tri-State Bi-Directional Card Voltage Sense with Pull-Up
PLBDCCKCBU	3.3V Interface Open Drain CardBus Bi-Directional Clock Driver with Pull-Up
PLSCB	3.3V Interface Level Shifter Buffer
KGM80	
PITCBU	Universal TTL CardBus Input Buffer with Pull-Up
POTCBU	Tri-State CardBus Output Buffer with Pull-Up
POTCCKCBU	Tri-State CardBus Output Clock Driver with Pull-Up
POTCVSCBU	Tri-State Output Card Voltage Sense with Pull-Up
PODCCKCBU	Open Drain CardBus Output Clock Driver with Pull-Up
PBTTCBU	Tri-State CardBus Bi-Directional Buffer with Pull-Up
PBTCCKCBU	CardBus Bi-Directional Clock Driver with Pull-Up
PBTCVSCBU	Tri-State Bi-Directional Card Voltage Sense with Pull-Up
PBDCCKCBU	Open Drain CardBus Bi-Directional Clock Driver with Pull-Up
PLSCB	Level Shifter Buffer

Electrical Characteristics
(Normal CardBus interface type buffers)

3.3V DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage		3.0	3.6	V
V_{IH}	Input High Voltage		$0.475V_{CC}$	V_{CC} + 0.5	
V_{IL}	Input Low Voltage		–0.5	$0.325V_{CC}$	
V_{OH}	Output High Voltage	I_{OUT} = –150μA	$0.9V_{CC}$		
V_{OL}	Output Low Voltage	I_{OUT} = 700μA		$0.1V_{CC}$	
I_{CC}[1]	Supply Current			1	A
I_{IL}[2]	Input Leakage Current	$0 < V_{IN} < V_{CC}$		±10	μA

NOTES:

1. This is determined solely by the maximum current capacity of the V_{CC} pins on the connector.
2. Input leakage currents include High-Z output leakage for all bi-directional buffers with High-Z outputs. CCD1#, CCD2#, CVS1 and CVS2 do not have to meet leakage requirements.

3.3V AC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
t_{RCB}[1]	Output Rise Time	$0.2V_{CC} – 0.6V_{CC}$	0.25	1.0	V/ns
t_{FCB}[1]	Output Fall Time	$0.6V_{CC} – 0.2V_{CC}$	0.25	1.0	
I_{CL}	Low Clamp Current	$–3 < V_{IN} < –1$	$–25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High Clamp Current	$V_{CC} + 4 > V_{IN} > V_{CC} + 1$	$25 + (V_{IN} – V_{CC} – 1) / 0.015$		

NOTE:

1. This does not apply to **CCLK**. Minimum and maximum rates are measured with the minimum capacitive load a driver will see (7pF). The values ensure the fastest edge rate will not switch rail-to-rail faster than 3.6ns.

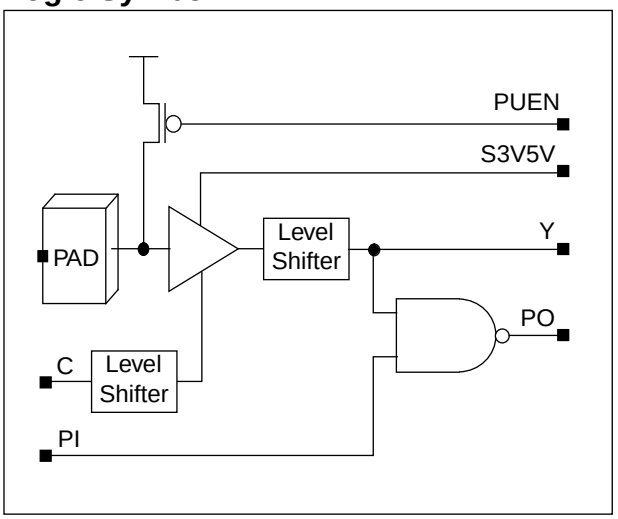
PvITCBU

Universal TTL CardBus Input Buffer with Pull-Up

Cell Availability

Library	5V Operation	3.3V Operation
KG80	–	PLITCBU
KGM80	–	PITCBU

Logic Symbol



Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

* PUEN (Pull-up control pin) is low enable.

Cell Data

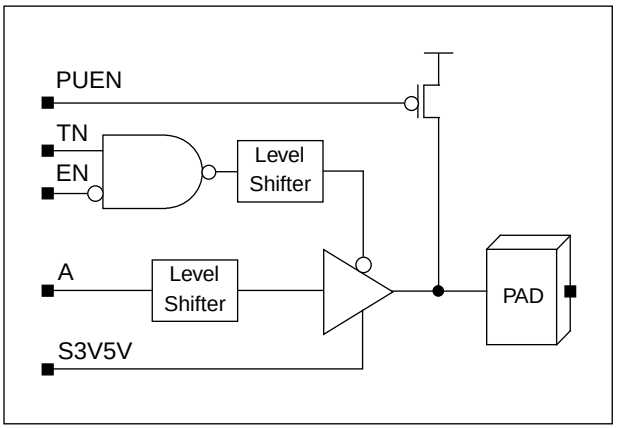
Input Load (SL)		I/O Slot
C	PI	
4.0	1.6	1.0

Cell Availability

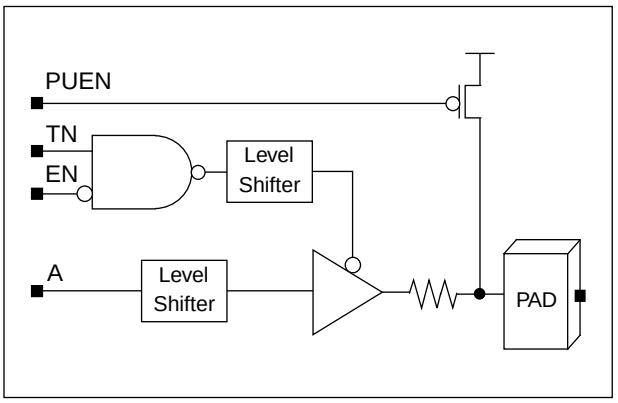
Library	5V Operation	3.3V Operation
KG80	–	PLOTCBU/PLOTCCKCBU/PLOTCVSCBU
KGM80	–	POTCBU/POTCCKCBU/POTCVSCBU

Logic Symbol

PLOTCBU/PLOTCCKCBU



PLOTCVSCBU



Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

Cell Data

Input Load (SL)				I/O Slot
A	EN	TN	PUEN	
2.3	1.2	1.2	0.5	1.0

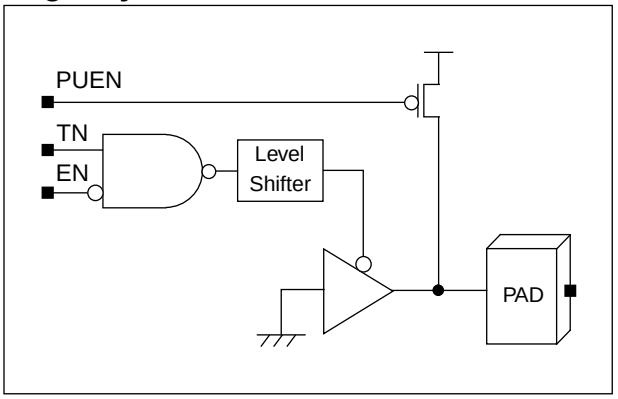
PvODCCKCBU

Open Drain CardBus Output Clock Driver with Pull-Up

Cell Availability

Library	5V Operation	3.3V Operation
KG80	–	PLODCCKCBU
KGM80	–	PODCCKCBU

Logic Symbol



Truth Table

EN	TN	PAD
0	1	0
1	x	Hi-Z
x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

Cell Data

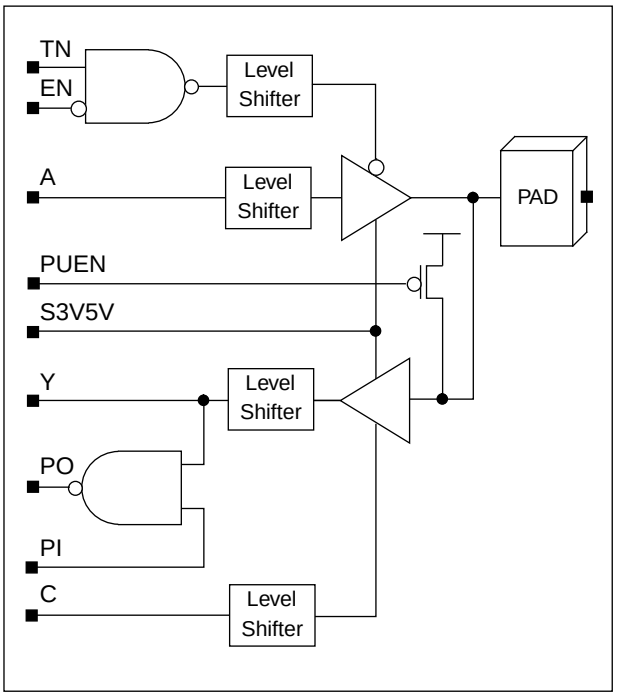
Input Load (SL)			I/O Slot
EN	TN	PUEN	
1.2	1.2	0.5	1.0

Cell Availability

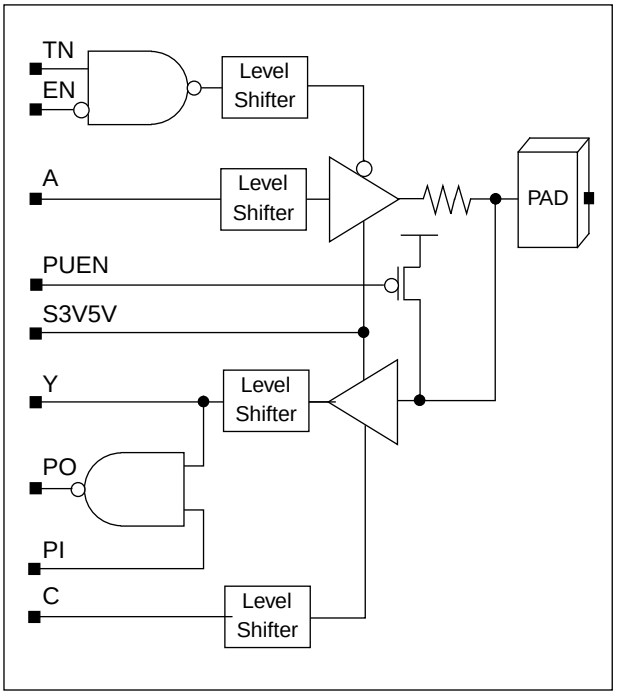
Library	5V Operation	3.3V Operation
KG80	–	PLBTTCBU/PLBTCCKCBU/PLBTCVSCBU
KGM80	–	PODCCKCBU

Logic Symbol

PLBTTCBU/PLBTCCKCBU



PLBTCVSCBU



Truth Table

Input Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

Cell Data

Input Load (SL)						I/O Slot
A	EN	TN	PUEN	C	PI	
2.3	1.2	1.2	0.5	4.0	1.6	1.0

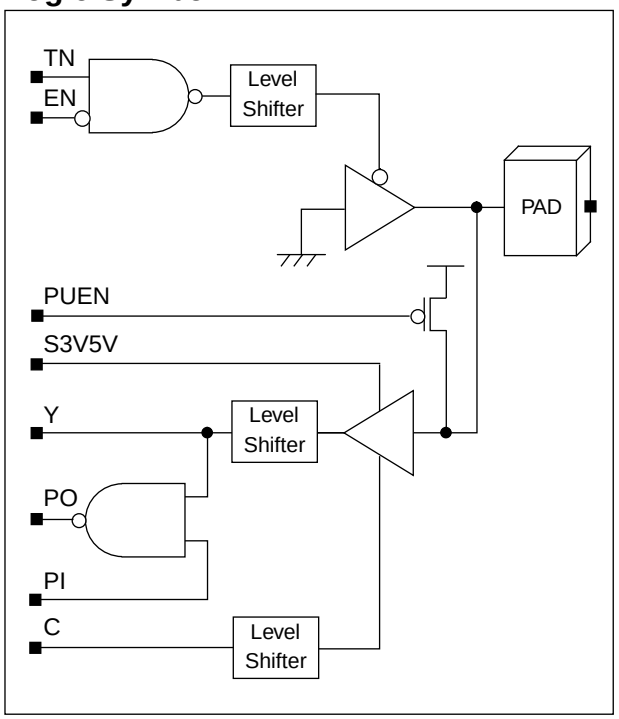
PvBDCCKCBU

Open Drain CardBus Bi-Directional Clock Driver with Pull-Up

Cell Availability

Library	5V Operation	3.3V Operation
KG80	–	PLBDCCKCBU
KGM80	–	PBDCCKCBU

Logic Symbol



Truth Table

Input Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

Output Truth Table

EN	TN	PAD
0	1	0
1	x	Hi-Z
x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

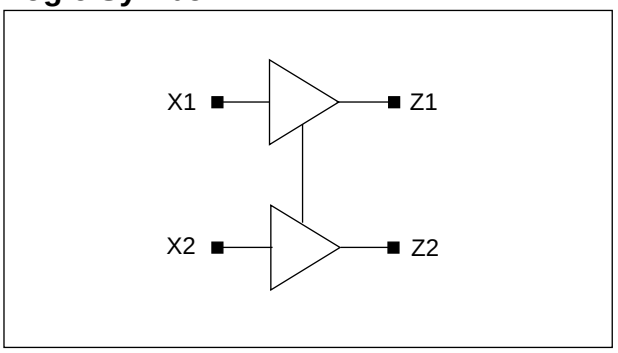
Cell Data

Input Load (SL)					I/O Slot
EN	TN	PUEN	C	PI	
1.2	1.2	0.5	4.0	1.6	1.0

Cell Availability

Library	5V Operation	3.3V Operation
KG80	–	PLSCB
KGM80	–	PLSCB

Logic Symbol



Truth Table

Xn	Zn
0	0
1 (VDDXI)	1 (VDDXO)

Cell Data

Input Load (SL)		I/O Slot
X1	X2	
2.4	2.4	1.0

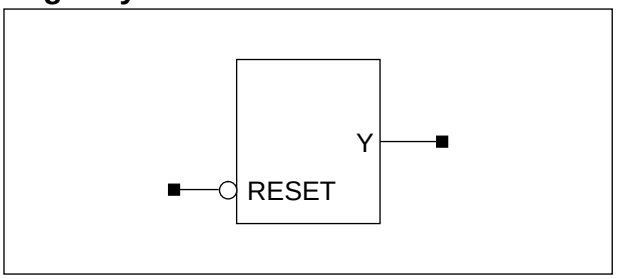
VOLTAGE DETECTOR – Under Development (Available in January 1997)

Cell List

Cell Name	Function Description
VDET	Voltage Detector

! Caution: This Voltage Detector can be used in gate array as an embedded cell only.

Logic Symbol



* Y pin should be connected to S3V5V pin directly.
Do not use a level shifter buffer (PLSCB).

Pin Connection

Input	Output
RESET	Y

Truth Table

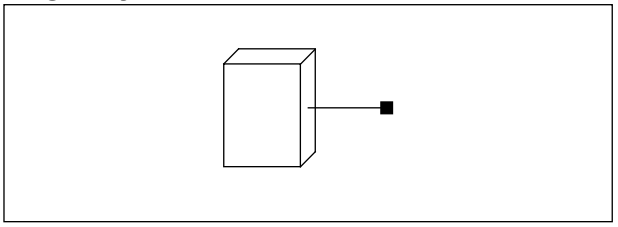
RESET	Y
0	0
1	0 (1) *

* If I/O supply voltage is 3.3V, output Y is high state.

Cell List

Cell Name		Function Description
KG80		
VDD Power Pads	**VSS Power Pads**	
VDD5I	VSS5I	5V Internal
VDD5P	VSS5P	5V Pre-Driver
VDD5O	VSS5O	5V Output-Driver
VDD5IP	VSS5IP	5V Internal and Pre-Driver
VDD5OI	VSS5OI	5V Output-Driver and Internal
VDD5OP	VSS5OP	5V Output-Driver and Pre-Driver
VDD5T	VSS5T	5V Total
VDD3P	VSS3P	3.3V Pre-Driver
VDD3O	VSS3O	3.3V Output-Driver
VDD3OP	VSS3OP	3.3V Output-Driver and Pre-Driver
KGM80		
VDD Power Pads	**VSS Power Pads**	
VDD3I	VSS3I	3.3V Internal
VDD3P	VSS3P	3.3V Pre-Driver
VDD3O	VSS3O	3.3V Output-Driver
VDD3IP	VSS3IP	3.3V Internal and Pre-Driver
VDD3OI	VSS3OI	3.3V Output-Driver and Internal
VDD3OP	VSS3OP	3.3V Output-Driver and Pre-Driver
VDD3T	VSS3T	3.3V Total
VDD5P	VSS5P	5V Pre-Driver
VDD5O	VSS5O	5V Output-Driver
VDD5OP	VSS5OP	5V Output-Driver and Pre-Driver

Logic Symbol



Memory Compilers 5

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OVERVIEW

This chapter contains information for KG80/KGM80 memory compilers such as ROM, single-port RAM, dual-port RAMs, RAM-based FIFO and multiplier generators.

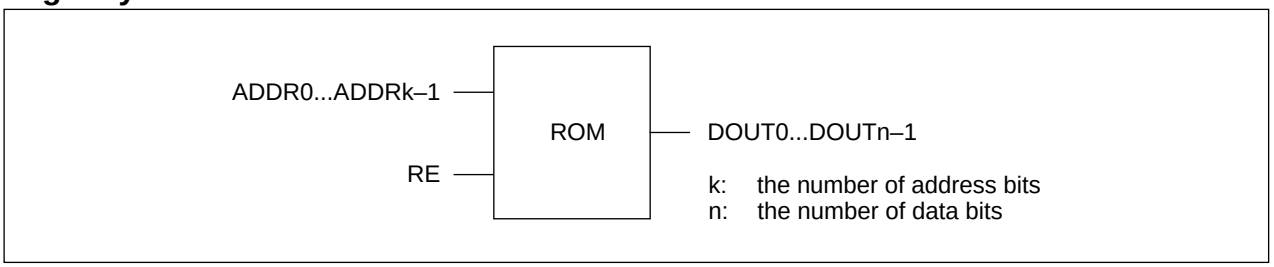
Cell Names & Function Descriptions

Cell Name	Function Description
ROM	Asynchronous/Synchronous ROM Generator
RAM	Asynchronous Single-Port RAM Generator
1R1W DPRAM	Asynchronous One Read One Write Dual-Port RAM Generator
1RW1R DPRAM	Asynchronous One Read/Write One Read Dual-Port RAM Generator
FIFO	Ram-Based First-In First-Out Memory Generator
Multiplier	Multiplier Generator

ROM

Asynchronous/Synchronous ROM Generator

Logic Symbol



NOTE: In KG80 “RE” pin should be tied to VDD.

Description

This is a high-speed, low-power ROM with fully static and asynchronous operation, and one read address port and one data output port. The number of words and word width can be configured with the MEMGEN memory compiler. ROM code is contact layer programmable.

Four ROM architectures (Type 1, 2, 3 and 4) support variable cell aspect ratios consistent with word/bit configuration limitations.

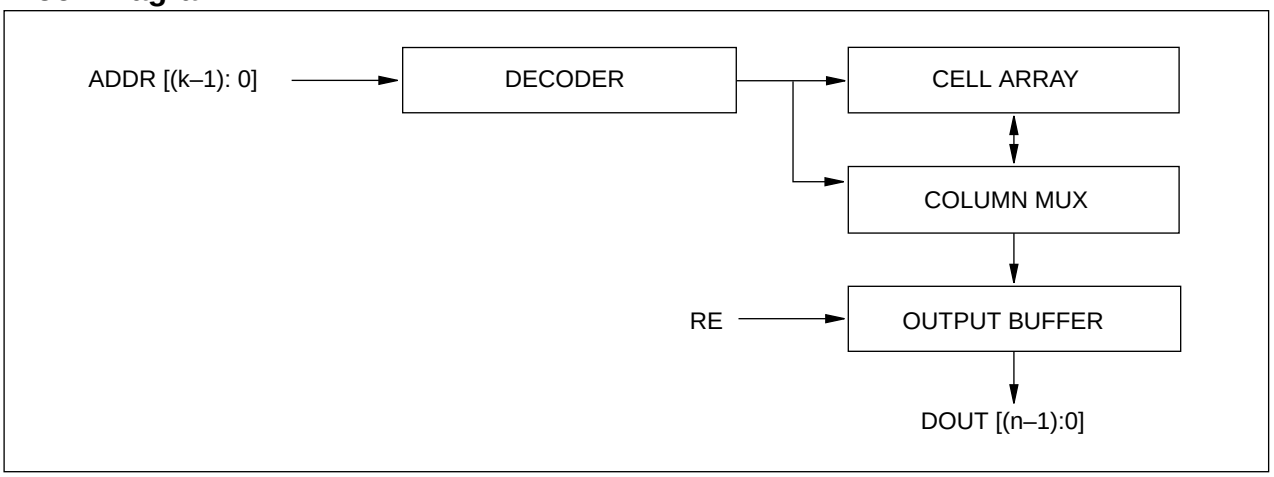
Features

- Zero standby power
- High speed
- Contact programmable ROM code
- Asynchronous and fully static operation
- Parameter-driven compiler
- Up to 36K bit block
- Variable word depth
  – 8, 16, 24, 32, 40,..., 256
- Variable word width
  – 4, 5, 6, 7, 8,..., 144
- Available architectures
  – Type1, Type 2, Type 3 and Type 4

I/O Pin Description

Name	I/O	I/O Cap. [pF]	Description
ADDR0...ADDRk–1	I	0.042	Read Address
RE	I	0.021	Read Enable
DOUT0...DOUTn–1	O	0.041	Data Output

Block Diagram



Gate Count

Gate Count = Height x Width
Size = (Height x 19.0) x (Width x 6.0)

Height Calculation

Height = (Words / (4 x Type)) + A
if (Type = 1), then A = 7
else A = 5

Width Calculation

Width = Type x Bits x 2 + 1 + Div (Type x Bits / 25) + B
A = Words / (2 x Type)

Type / A	1		2		3		4	
	Width<36	Width>=36	Width<18	Width>=18	Width<12	Width>=12	Width<9	Width>=9
4	B = 5	B = 7	B = 7	B = 7	B = 9	B = 11	B = 10	B = 11
8	B = 6	B = 8	B = 7	B = 8	B = 9	B = 11	B = 10	B = 11
12	B = 8	B = 10	B = 8	B = 10	B = 9	B = 11	B = 10	B = 11
16	B = 8	B = 10	B = 8	B = 10	B = 9	B = 11	B = 10	B = 11
20 ~ 32	B = 10	B = 12	B = 10	B = 12	B = 10	B = 12	B = 10	B = 12
36 ~ 128	B = 11	B = 13	B = 11	B = 13	B = 11	B = 13	B = 11	B = 11

< Example: ROM32 x 19 (Type = 2) >

Height = {32 / (4 x 2)} + 5 = 9
Width = 2 x 19 x 2 + 1 + 1 + 8 = 86
Gate Count = (9 x 86) arrays
Size = (9 x 19.0) x (86 x 6.0) microns

The table below shows the number of gates used for representative ROMs. Although architecture type also affects the number of gates, this table shows the number of gates for type 2.

Gate Counts for Representative ROMs

Bit / Word	32	64	128	160	192	256
8	360	533	903	1100	1276	1628
16	657	9628	1596	1925	2233	2849
24	954	1404	2310	2775	3219	4107
32	1251	1833	3003	3600	4176	5328
36	1395	2745	3339	4000	4640	5920

ROM

Asynchronous/Synchronous ROM Generator

Memgen-Supported ROM Configurations

Address Pin	Words	Type 1 (4 ~ 144)	Type 2 (4 ~ 72)	Type 3 (4 ~ 48)	Type 4 (4 ~ 36)
3	8	o			
4	16	o	o		
5	(24)	o		o	
	32	o	o		o
6	(40)	o			
	(48)	o	o	o	
	(56)	o			
	64	o	o		o
7	(72)	o			
	(80)	o	o		
	(88)	o			
	(96)	o	o	o	o
	(104)	o			
	(112)	o	o		
	(120)	o			
	128	o	o		
8	(136)	o			
	(144)	o	o		
	(152)	o			
	(160)	o	o		o
	(168)	o			
	(176)	o	o		
	(184)	o			
	(192)	o	o	o	o
	(200)	o			
	(208)	o	o		
	(216)	o			
	(224)	o	o		o
	(232)	o			
	(240)	o	o		
	(248)	o			
	256	o	o		o

NOTE: Parentheses indicate incomplete address decoding.

AC Parameters

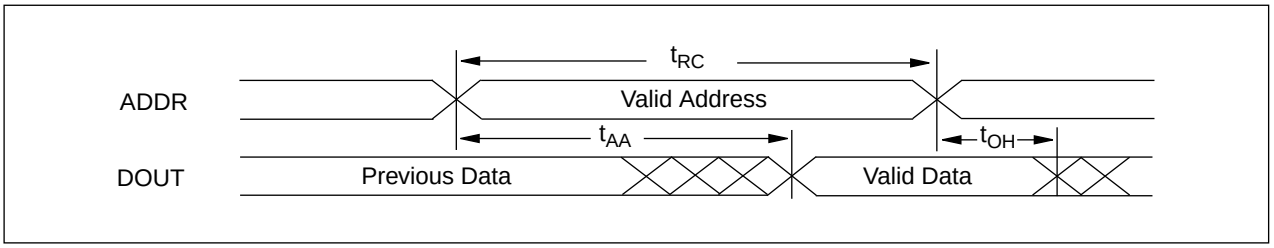
KG80		(Typical Process, 25˚C, 5V, t_R / t_F = 1.2ns, SL = 20)		
Symbol	**Parameter**	**tpd (ns)**		
		32x8 (Type=2)	**128x8 (Type=2)**	**256x8 (Type=2)**
t_{RC}	Read Cycle Time	2.401	3.012	3.468
t_{AA}	Address Access Time	3.430	4.035	4.465
t_{OH}	Output Hold Time from Address Change	1.000	1.000	1.000

KGM80		(Typical Process, 25˚C, 3.3V, t_R / t_F = 1.2ns, SL = 20)		
Symbol	**Parameter**	**tpd (ns)**		
		32x8 (Type=2)	**128x8 (Type=2)**	**256x8 (Type=2)**
t_{RP}	Read Cycle Time	1.160	1.160	1.160
t_{AS}	Address Setup Time	1.905	2.807	3.459
t_{AH}	Address Hold Time	1.000	1.000	1.000
t_{RE}	Read Enable Access Time	3.094	3.094	3.094

Timing Diagram

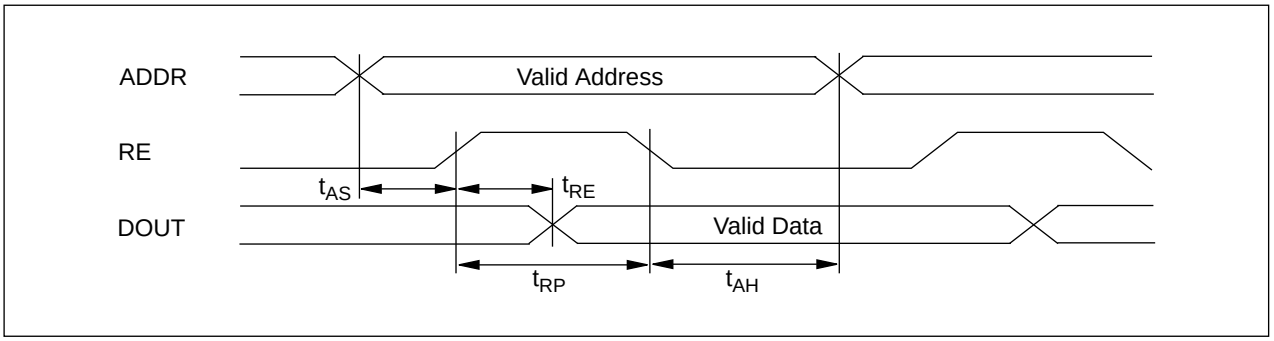
Read Cycle

<KG80>



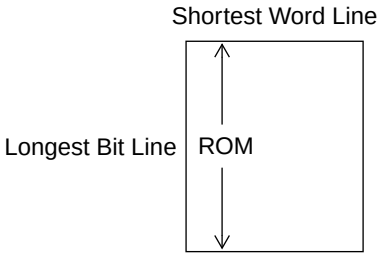
NOTE: "RE" pin is tied to VDD.

<KGM80>



Architecture

Type 1



For Type 1, the specified number of words will equal the number of rows and the specified number of bits will equal the number of columns in the ROM array.

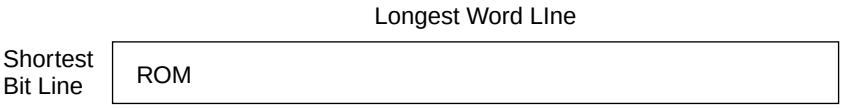
Type 2

For the same size ROM, Type 2 will have one-half the specified number of rows and twice the specified number of columns.

Type 3

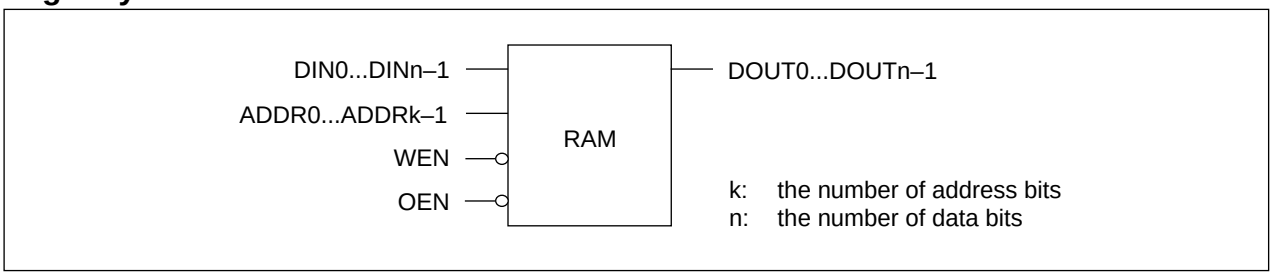
For the same size ROM, Type 3 will have one-third the specified number of rows and three times the specified number of columns.

Type 4



For the same size ROM, Type 4 will have one-fourth the specified number of rows and four times the specified number of columns.

Logic Symbol



Description

This is a high-speed, low-power, single-port RAM with fully static and asynchronous operation. The number of words and word width can be configured with the MEMGEN memory compiler. The design has one read/write address port, one data input port, and one data output port. Control pins are OEN (output enable) and WEN (write enable). During write operation, the data output port reflects data at the input port if the output tri-state buffers are enabled.

Four RAM architectures (Type 1, 2, 3 and 4) support varying aspect ratios consistent with word/bit configuration limitations.

Features

- 1 read/write address port
- 1 data input and 1 data output port
- Zero standby power
- High speed
- Asynchronous and fully static operation
- Tri-state output buffers
- Parameter-driven compiler
- Up to 9K bit block
- Variable word depth
  – 8, 16, 24, 32, 40,..., 256
- Variable word width
  – 4, 5, 6, 7, 8,..., 72
- Available architectures
  – Type1, Type 2, Type 3 and Type 4

I/O Pin Description

Name	I/O	I/O Cap. [pF]	Description
DIN0...DINn–1	I	0.021	Data Input
ADDR0...ADDRk–1	I	0.042	Read/Write Address
WEN	I	0.042	Write Enable Memory write operation is enabled when WEN is low.
OEN	I	0.021	Output Enable When OEN is high, the outputs are in high impedance state. When OEN is low, the data outputs are enabled.
DOUT0...DOUTn–1	O	0.042	Data Output

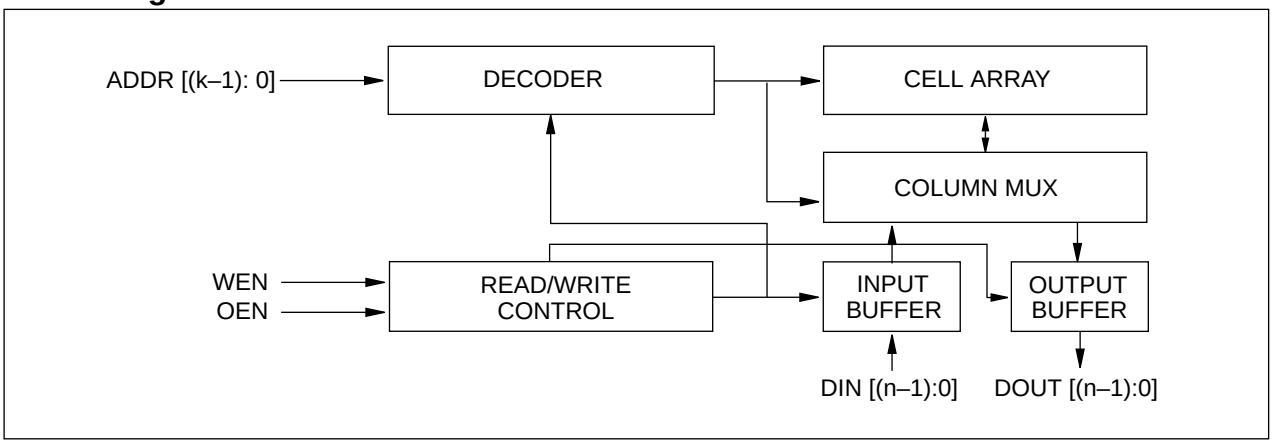
Truth Table

WEN	OEN	Mode
L	X	Write
X	L	Read
X	H	Output = High Impedance

RAM

Asynchronous Single-Port RAM Generator

Block Diagram



Gate Count

Gate Count = Height x Width
Size = (Height x 19.0) x (Width x 6.0)

Height Calculation

Height = (Bits x Type) + A
if (Words / Type = 8), then A = 5
else if {(Words / Type > 8) and (Words / Type < 72), then A = 6
else if (Words / Type >= 72), then A = 7

Width Calculation

Width = 3 x (Words / Type) + 2 + B
if (Type = 1), then B = 9
else if (Type = 2), then B = 17
else if (Type = 3), then B = 15
else if (Type = 4), then B = 14

< Example: RAM176 x 16 (Type = 2) >

Height = (16 x 2) +7 = 39
Width = 3 x (176 / 2) + 2 + 17 = 283
Gate Count = (39 x 283) arrays
Size = (39 x 19.0) x (283 x 6.0) microns

The table below shows the number of gates used for representative RAMs. Although architecture type also affects the number of gates, this table shows the number of gates for type 2.

Gate Counts for Representative RAMs

Bit \ Word	16	32	64	128	160	256
8	903	1474	2530	4642	5957	9269
16	1591	2546	4370	8018	10101	15717
24	2279	3618	6210	11394	14245	22165
32	2967	4690	8050	14770	18389	28613
36	3311	5226	8970	16458	20461	31837

Memgen-Supported RAM Configurations

Address Pin	Words	Type 1 (4 ~ 72)	Type 2 (4 ~ 36)	Type 3 (4 ~ 24)	Type 4 (4 ~ 18)
3	8	o			
4	16	o	o		
5	(24)	o		o	
	32	o	o		o
6	(40)	o			
	(48)	o	o	o	
	(56)	o			
	64	o	o		o
7	(72)	o			
	(80)	o	o		
	(88)	o			
	(96)	o	o	o	o
	(104)	o			
	(112)	o	o		
	(120)	o			
	128	o	o		o
8	(144)		o		
	(160)		o		o
	(176)		o		
	(192)		o	o	o
	(208)		o		
	(224)		o		o
	(240)		o		
	256		o		o

NOTE: Parentheses indicate incomplete address decoding.

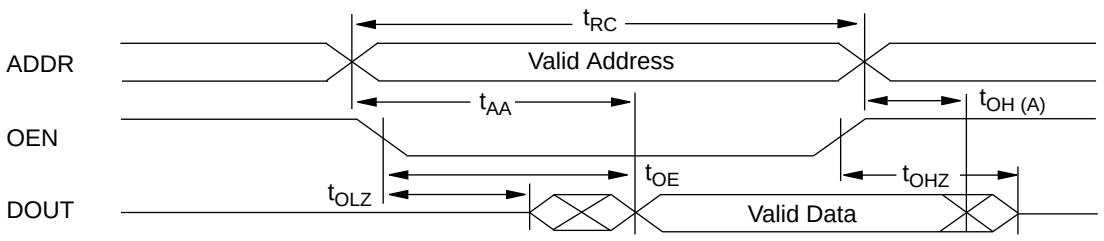
AC Parameters

KG80		(Typical Process, 25˚C, 5V, t_R / t_F = 1.2ns, SL = 20)		
Symbol	**Parameter**	**tpd (ns)**		
		32x8 (Type=2)	**128x8 (Type=2)**	**256x8 (Type=2)**
Read Cycle				
t_{RC}	Read Cycle Time	2.510	3.845	5.709
t_{AA}	Address Access Time	3.104	4.457	6.334
$t_{OH\ (A)}$	Output Hold Time from Address Change	1.000	1.000	1.000
t_{OE}	Output Enable Time	1.188	1.188	1.188
t_{OLZ}	Output Enable to Output Low-Z	0.734	0.734	0.734
t_{OHZ}	Output Disable to Output High-Z	0.364	0.364	0.364
Write Cycle				
t_{WC}	Write Cycle Time	3.358	4.989	9.199
t_{WA}	Write Enable Access Time	3.969	5.599	7.809
t_{DA}	Data-In Access Time	2.903	4.681	7.002
t_{WP}	Write Enable Pulse Width	2.314	2.777	3.428
t_{AS}	Address Setup Time	0.652	1.844	3.460
t_{AH}	Address Hold Time	0.000	0.518	1.347
t_{DW}	Data-In Setup Time	0.000	0.000	0.000
t_{DH}	Data-In Hold Time	0.726	0.817	1.055
$t_{OH\ (D)}$	Output Hold Time from DIN Change	1.000	1.000	1.000
$t_{OH\ (W)}$	Output Hold Time from WEN Change	0.588	0.578	0.565

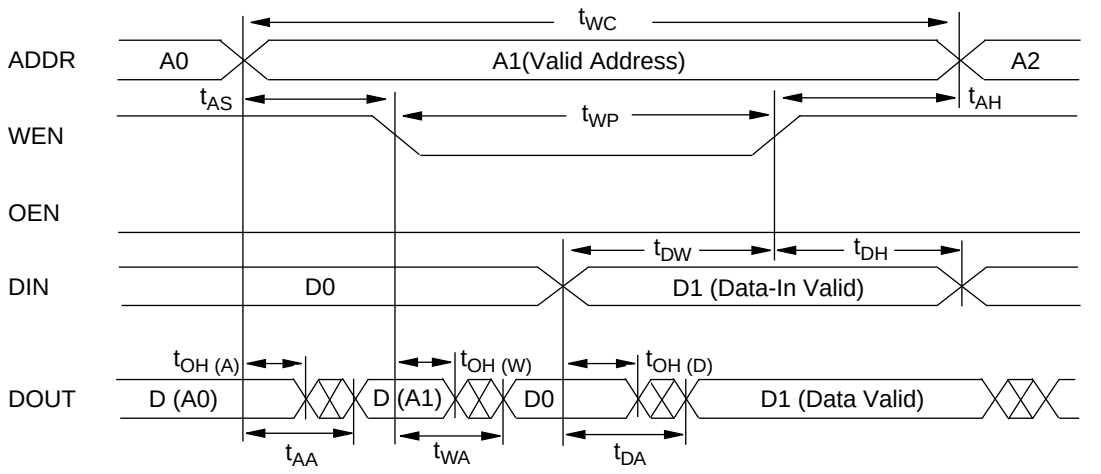
KGM80		(Typical Process, 25˚C, 3.3V, t_R / t_F = 1.2ns, SL = 20)		
Symbol	**Parameter**	**tpd (ns)**		
		32x8 (Type=2)	**128x8 (Type=2)**	**256x8 (Type=2)**
Read Cycle				
t_{RC}	Read Cycle Time	3.454	5.180	7.613
t_{AA}	Address Access Time	4.165	5.345	8.364
$t_{OH\ (A)}$	Output Hold Time from Address Change	1.000	1.000	1.000
t_{OE}	Output Enable Time	1.604	1.604	1.604
t_{OLZ}	Output Enable to Output Low-Z	0.929	0.929	0.929
t_{OHZ}	Output Disable to Output High-Z	0.561	0.561	0.561
Write Cycle				
t_{WC}	Write Cycle Time	4.703	6.754	9.501
t_{WA}	Write Enable Access Time	5.429	7.480	10.228
t_{DA}	Data-In Access Time	3.883	6.116	9.053
t_{WP}	Write Enable Pulse Width	3.141	3.603	4.369
t_{AS}	Address Setup Time	0.978	2.593	4.813
t_{AH}	Address Hold Time	0.187	0.982	2.121
t_{DW}	Data-In Setup Time	0.000	0.000	0.000
t_{DH}	Data-In Hold Time	1.224	1.498	1.960
$t_{OH\ (D)}$	Output Hold Time from DIN Change	1.000	1.000	1.000
$t_{OH\ (W)}$	Output Hold Time from WEN Change	0.857	0.840	0.817

Timing Diagram

Read Cycle



Write Cycle



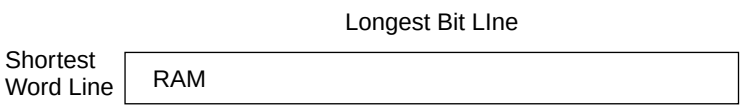
* D (An): data which are stored in An address

RAM

Asynchronous Single-Port RAM Generator

Architecture

Type 1

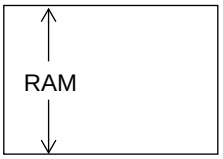


For Type 1, the specified number of words will equal the number of columns and the specified number of bits will equal the number of rows in the RAM array.

Type 2

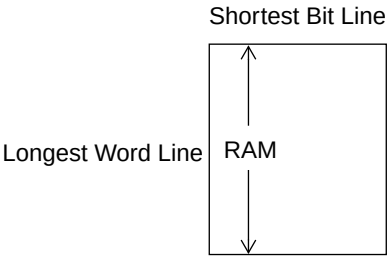
For the same size RAM, Type 2 will have twice the specified number of columns and one-half the specified number of rows.

Type 3



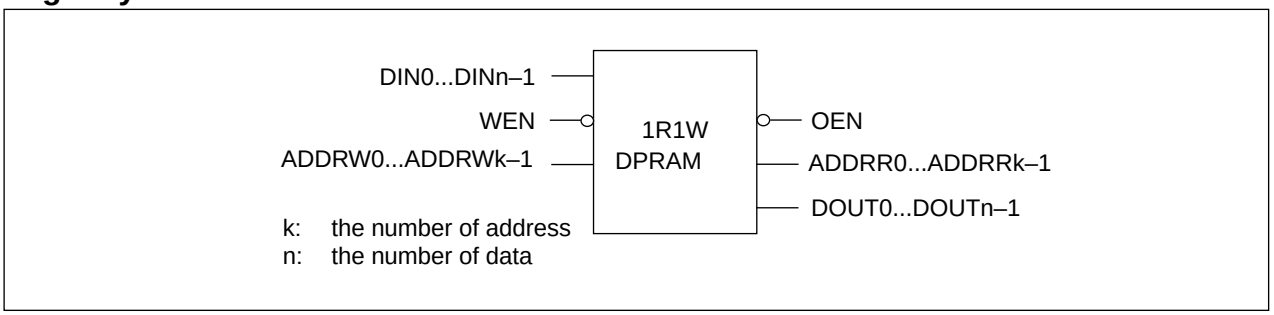
For the same size RAM, Type 3 will have three times the specified number of columns and one-third the specified number of rows.

Type 4



For the same size RAM, Type 4 will have four times the specified number of columns and one-fourth the specified number of rows.

Logic Symbol



Description

This high-speed, low-power, 1R1W dual-port RAM has fully static and asynchronous operation. The number of words and word width can be configured with the MEMGEN—embedded memory compiler. The design has one read address port and one write address port, and one data input port and one data output port. Control pins are OEN (output enable) and WEN (write enable). During a write operation, the data output ports reflect the data which are stored in the read address, if the output tri-state buffers are enabled.

Four RAM architectures (Type 1, 2, 4 and 8) support varying aspect ratios consistent with word/bit configuration limitations.

Features

- Fully asynchronous read/write operation
- Variable size dual-port RAM with
  1 read and 1 write address port,
  1 data input and 1 data output port
- Zero stand-by power
- High speed
- Tri-state output buffers
- Parameter-driven compiler
- Up to 9K bit block
- Variable word depth
  – 8, 16, 24, 32, 40,..., 1024
- Variable word width
  – 4, 5, 6, 7, 8,..., 72
- Available architectures
  – Type1, Type 2, Type 4 and Type 8

I/O Pin Description

Name	I/O	I/O Cap. [pF]	Description
DIN0...DINn–1	I	0.021	Data Input
ADDRW0...ADDRWk–1 ADDRR0...ADDRRk–1	I	0.021	Read/Write Address Input
WEN	I	0.042	Read/Write Control
OEN	I	0.021	Tri-State Control
DOUT0...DOUTn–1	O	0.098	Data Output

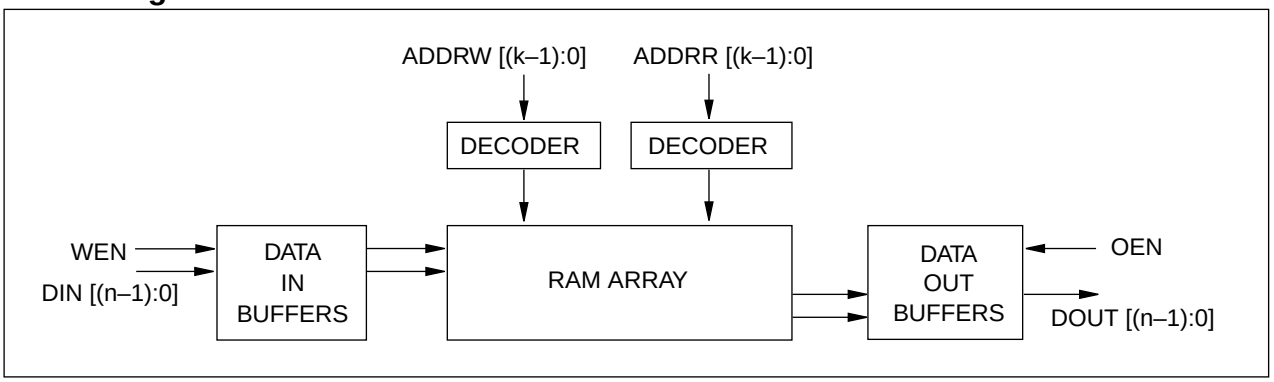
Truth Table

WEN	OEN	Mode
L	X	Write
X	L	Read
X	H	Output = High Impedance

1R1W DPRAM

Asynchronous One Read One Write Dual-Port RAM Generator

Block Diagram



Gate Count

Gate Count = Height x Width
Size = (Height x 19.0) x (Width x 6.0)

Height Calculation

Height = (Bits x Type) + 2 x A + B
A = DIV (Type / 2)
if (Words / Type = 8), then B = 8
else if {(Words / Type > 8) and (Words / Type < 40), then B = 9
else if {(Words / Type > 32) and (Words / Type < 72), then B = 10
else if (Words / Type >= 72), then B = 12

Width Calculation

Width = 3 x (Words / Type) + 15 + A
if (Type = 1), then A = 0
else if MOD (Bits / 3) = 0, then A = DIV (Bits / 3) x 2
else if MOD (Bits / 3) = 1, then A = DIV (Bits / 3) x 2 + 1
else if MOD (Bits / 3) = 2, then A = DIV (Bits / 3) x 2 + 2

< Example: 1R1W DPRAM 256 x 16 (Type = 2) >

Height = (16 x 2) + 2 x 1 + 12 = 46
Width = 3 x (256 / 2) + 14 + 12 = 410
Gate Count = (46 x 410) arrays
Size = (46 x 19.0) x (410 x 6.0) microns

The table below shows the number of gates used for representative 1r1w DPRAMs. Although architecture type also affects the number of gates, this table shows the number of gates for type 2.

Gate Counts for Representative 1r1w DPRAMs

Bit \ Word	16	32	64	128	160	256
8	1170	1863	3159	5964	7830	12150
16	2100	3182	5246	9592	12236	18860
24	3190	4661	7493	13380	16802	25730
32	4514	6375	9975	17404	21606	32838
36	5166	7221	11205	19404	23994	36378

Memgen-Supported 1R1W DPRAM Configurations

Address Pin	Words	Type 1 (4 ~ 72)	Type 2 (4 ~ 36)	Type 4 (4 ~ 18)	Type 8 (4 ~ 9)
3	8	o			
4	16	o	o		
5	(24)	o			
	32	o	o	o	
6	(40)	o			
	(48)	o	o		
	(56)	o			
	64	o	o	o	o
7	(72)	o			
	(80)	o	o		
	(88)	o			
	(96)	o	o	o	
	(104)	o			
	(112)	o	o		
	(120)	o			
	128	o	o	o	o
8	(144)		o		
	(160)		o	o	
	(176)		o		
	(192)		o	o	o
	(208)		o		
	(224)		o	o	
	(240)		o		
	256		o	o	o
9	(288)			o	
	(320)			o	o
	(352)			o	
	(384)			o	o
	(416)			o	
	(448)			o	o
	(480)			o	
	512			o	o
8	(576)				o
	(640)				o
	(704)				o
	(768)				o
	(832)				o
	(896)				o
	(960)				o
	1024				o

NOTE: Parentheses indicate incomplete address decoding.

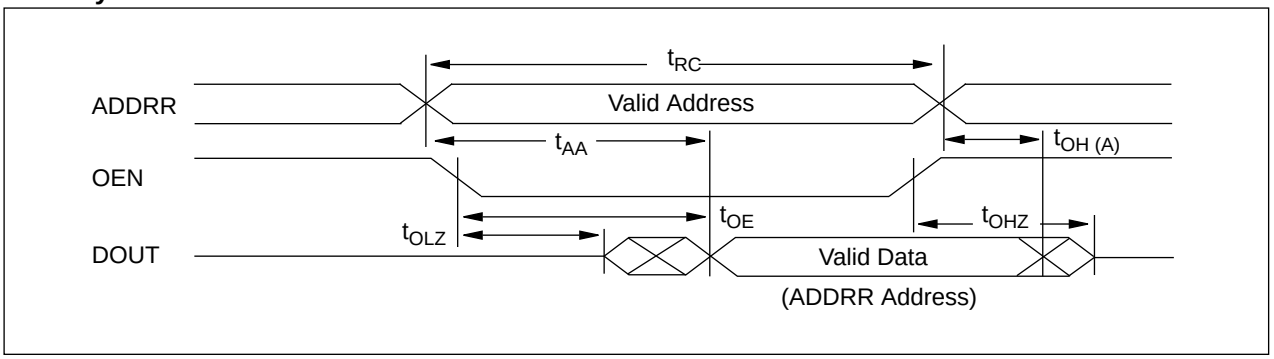
AC Parameters

KG80		(Typical Process, 25˚C, 5V, t_R / t_F = 1.2ns, SL = 20)		
Symbol	**Parameter**	**tpd (ns)**		
		32x8 (Type=2)	**128x8 (Type=2)**	**256x8 (Type=2)**
Read Cycle				
t_{RC}	Read Cycle Time	2.233	3.310	4.914
t_{AA}	Address Access Time	2.634	3.712	5.335
$t_{OH\ (A)}$	Output Hold Time from Address Change	1.000	1.000	1.000
t_{OE}	Output Enable Time	1.744	1.744	1.744
t_{OLZ}	Output Enable to Output Low-Z	1.182	1.182	1.182
t_{OHZ}	Output Disable to Output High-Z	0.768	0.768	0.768
Write Cycle				
t_{WC}	Write Cycle Time	3.682	4.091	4.851
t_{WA}	Write Enable Access Time	3.395	4.575	6.235
t_{DA}	Data-In Access Time	2.152	3.455	5.519
t_{WP}	Write Enable Pulse Width	1.954	2.230	2.667
t_{AS}	Address Setup Time	1.393	1.212	1.361
t_{AH}	Address Hold Time	0.000	0.276	0.381
t_{DW}	Data-In Setup Time	0.314	0.391	0.581
t_{DH}	Data-In Hold Time	0.971	1.026	1.285
$t_{OH\ (D)}$	Output Hold Time from DIN Change	1.000	1.000	1.000
$t_{OH\ (W)}$	Output Hold Time from WEN Change	0.000	0.000	0.000

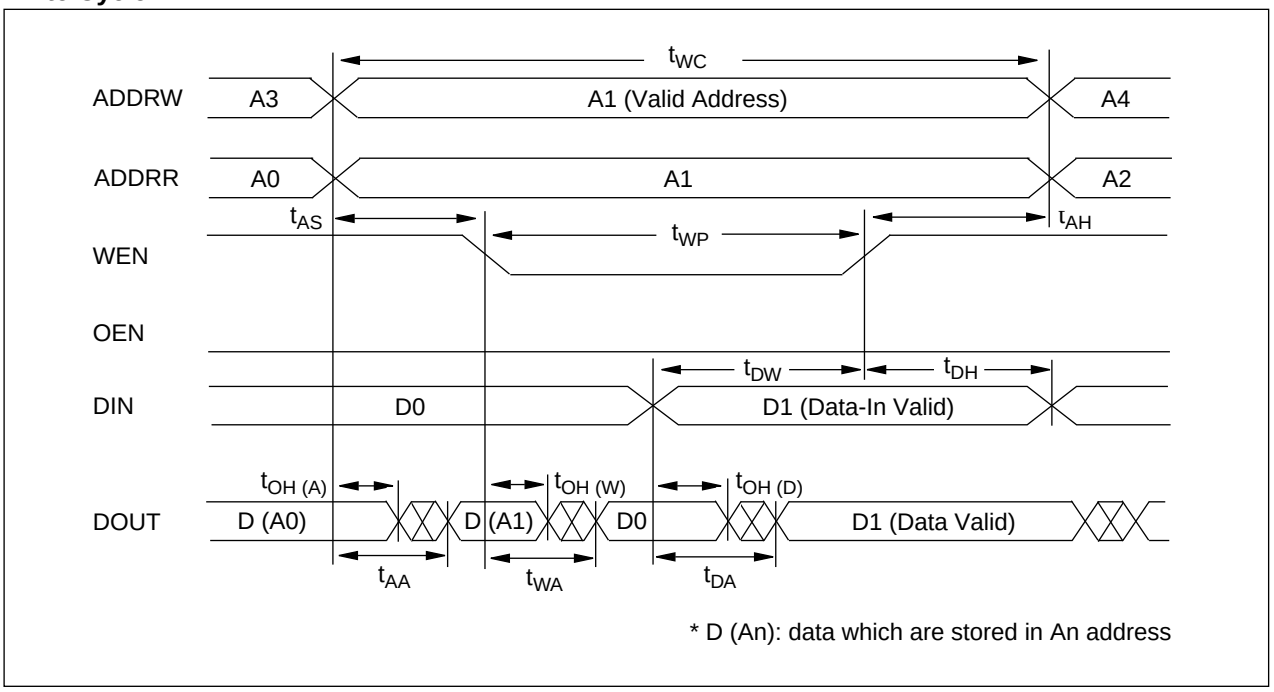
KGM80		(Typical Process, 25˚C, 3.3V, t_R / t_F = 1.2ns, SL = 20)		
Symbol	**Parameter**	**tpd (ns)**		
		32x8 (Type=2)	**128x8 (Type=2)**	**256x8 (Type=2)**
Read Cycle				
t_{RC}	Read Cycle Time	3.147	4.594	6.765
t_{AA}	Address Access Time	3.657	5.060	7.253
$t_{OH\ (A)}$	Output Hold Time from Address Change	1.000	1.000	1.000
t_{OE}	Output Enable Time	2.435	2.435	2.435
t_{OLZ}	Output Enable to Output Low-Z	1.575	1.575	1.575
t_{OHZ}	Output Disable to Output High-Z	1.136	1.136	1.136
Write Cycle				
t_{WC}	Write Cycle Time	4.746	5.405	6.301
t_{WA}	Write Enable Access Time	4.685	6.214	8.327
t_{DA}	Data-In Access Time	2.896	4.562	7.149
t_{WP}	Write Enable Pulse Width	2.499	2.838	3.347
t_{AS}	Address Setup Time	1.717	1.538	1.783
t_{AH}	Address Hold Time	0.097	0.537	0.597
t_{DW}	Data-In Setup Time	0.154	0.267	0.963
t_{DH}	Data-In Hold Time	1.535	1.655	2.003
$t_{OH\ (D)}$	Output Hold Time from DIN Change	1.000	1.000	1.000
$t_{OH\ (W)}$	Output Hold Time from WEN Change	0.000	0.000	0.000

Timing Diagram

Read Cycle



Write Cycle



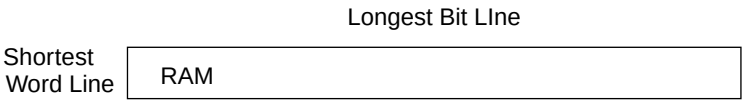
* D (An): data which are stored in An address

1R1W DPRAM

Asynchronous One Read One Write Dual-Port RAM Generator

Architecture

Type 1

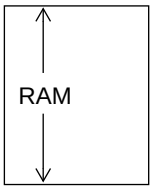


For Type 1, the specified number of words will equal the number of columns and the specified number of bits will equal the number of rows in the RAM array.

Type 2

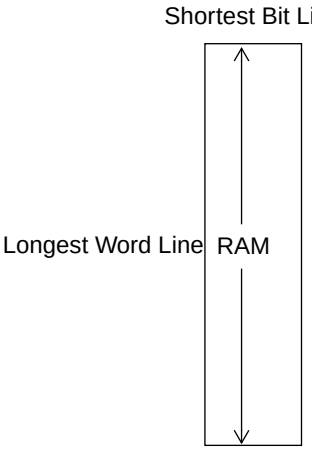
For the same size RAM, Type 2 will have twice the specified number of columns and one-half the specified number of rows.

Type 4



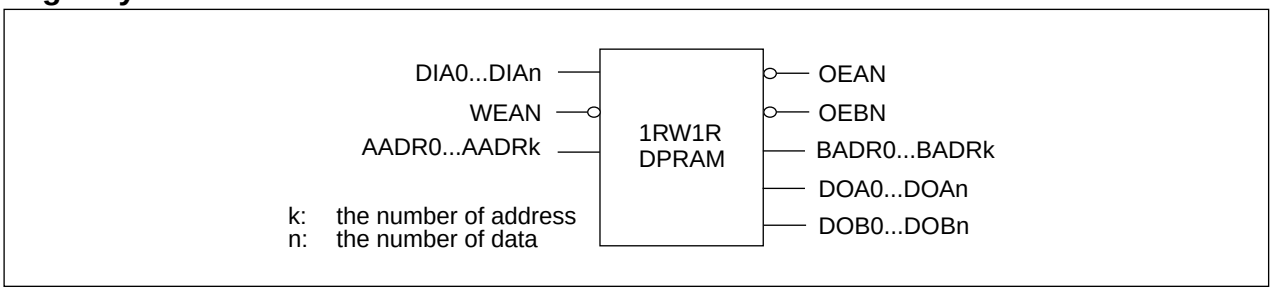
For the same size RAM, Type 4 will have four times the specified number of columns and one-fourth the specified number of rows.

Type 8



For the same size RAM, Type 8 will have eight times the specified number of columns and one-eighth the specified number of rows.

Logic Symbol



Description

This high-speed, low-power, 1RW1R dual-port RAM has fully static and asynchronous operation. The number of words and word width can be configured with the MEMGEN—embedded memory compiler.

This configuration has one read/write address port and one read address port, and one data input port and two data output ports. Control pins are OEAN / OEBN (output enable) and WEAN (write enable). During a write operation, the data output ports reflect the data which are stored in the read address, if the output tri-state buffers are enabled.

Four RAM architectures (Type 1, 2, 4 and 8) support varying aspect ratios consistent with word/bit configuration limitations.

Features

- Fully asynchronous read/write operation
- Variable size dual-port RAM with
  1 read/write and 1 read address port
- 1 data input and 2 data output ports
- Zero standby power
- High speed
- Tri-state output buffers
- Parameter-driven compiler
- Up to 9K bit block
- Variable word depth
  – 8, 16, 24, 32, 40,..., 1024
- Variable word width
  – 4, 5, 6, 7, 8,..., 72
- Available architectures
  – Type1, Type 2, Type 4 and Type 8

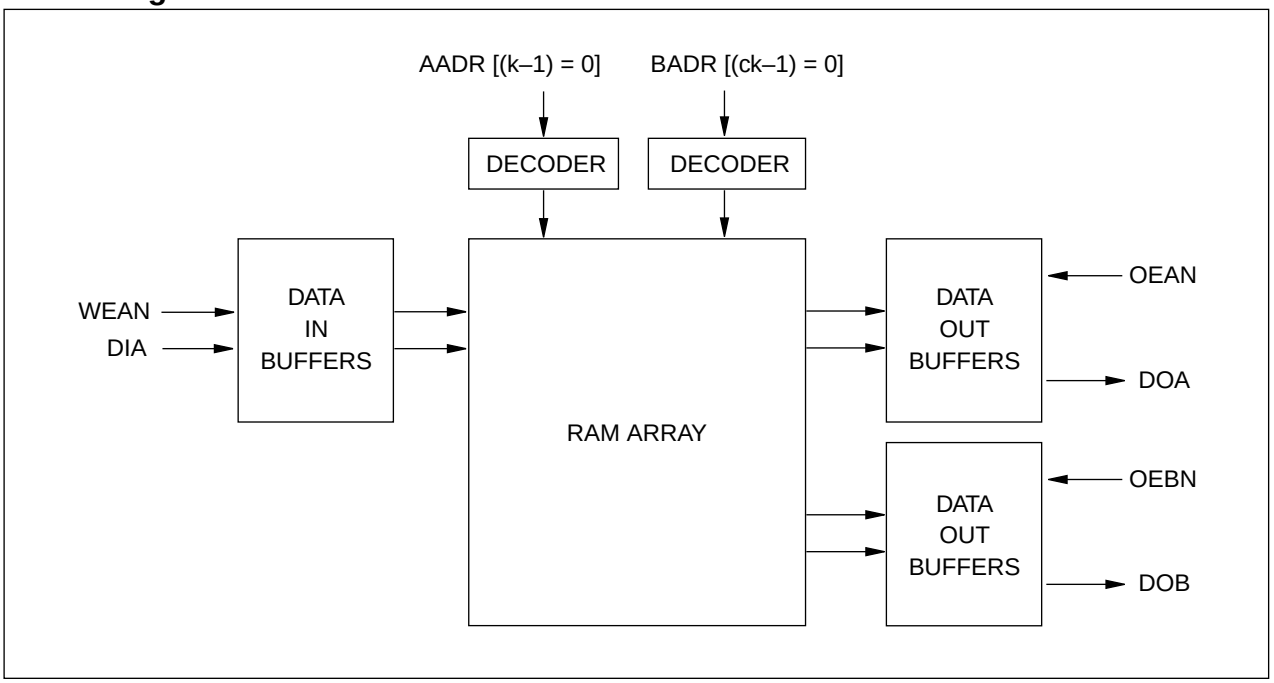
I/O Pin Description

Name	I/O	I/O Cap. [pF]	Description
DIA0...DIAn	I	0.021	Data Input
WEAN	I	0.042	Read/Write Port Read/Write Control
OEAN OEBN	I	0.021	Read/Write Port Tri-State Control Read Port Tri-State Control
AADR0...AADRk BADR0...BADRk	I	0.021	Read/Write Port Address Input Read Port Address Input
DOA DOB	O	0.098	Read/Write Port Output Read Port Output

1RW1R DPRAM

Asynchronous One Read/Write One Read Dual-Port RAM Generator

Block Diagram



Truth Table

OEBN	OEAN	WEAN	Mode
	X	L	Write
	L	X	Read
	H	X	Read/Write Port Output = High Impedance
L			Read Port Read
H			Read Port Output = High Impedance

Gate Count

Gate Count = Height x Width
Size = (Height x 19.0) x (Width x 6.0)

Height Calculation

Height = (Bits x Type) + 2 x A + B
A = DIV (Type / 2)
if {(Words / Type = 8) or (Words / Type = 16), then B = 8
else if (Words / Type > 16), then B = 10

Width Calculation

Width = 4 x (Words / Type) + A
if (Type = 1), then A = 34
else A = 34 + Bits

< Example: 1RW1R DPRAM 256 x 16 (Type = 2) >

Height = (16 x 2) +2 x 1 + 10 = 44
Width = 4 x (256 / 2) + 34 +16 = 562
Gate Count = (44 x 562) arrays
Size = (44 x 19.0) x (562 x 6.0) microns

The table below shows the number of gates used for representative 1RW1R DPRAMs. Although architecture type also affects the number of gates, this table shows the number of gates for type 2.

Gate Counts for Representative 1RW1R DPRAMs

Bit \ Word	16	32	64	128	160	256
8	1924	2756	4760	8344	10136	15512
16	3444	4788	7832	13464	16280	24728
24	5220	7076	11160	18840	22680	35200
32	7252	9620	14744	24472	29336	43928
36	8364	10988	16632	27384	32760	48888

1RW1R DPRAM

Asynchronous One Read/Write One Read Dual-Port RAM Generator

Memgen-Supported 1RW1R DPRAM Configurations

Address Pin	Words	Type 1 (4 ~ 72)	Type 2 (4 ~ 36)	Type 4 (4 ~ 18)	Type 8 (4 ~ 9)
3	8	o			
4	16	o	o		
5	(24)	o			
	32	o	o	o	
6	(40)	o			
	(48)	o	o		
	(56)	o			
	64	o	o	o	o
7	(72)	o			
	(80)	o	o		
	(88)	o			
	(96)	o	o	o	
	(104)	o			
	(112)	o	o		
	(120)	o			
	128	o	o	o	o
8	(144)		o		
	(160)		o	o	
	(176)		o		
	(192)		o	o	o
	(208)		o		
	(224)		o	o	
	(240)		o		
	256		o	o	o
9	(288)			o	
	(320)			o	o
	(352)			o	
	(384)			o	o
	(416)			o	
	(448)			o	o
	(480)			o	
	512			o	o
8	(576)				o
	(640)				o
	(704)				o
	(768)				o
	(832)				o
	(896)				o
	(960)				o
	1024				o

NOTE: Parentheses indicate incomplete address decoding.

AC Parameters

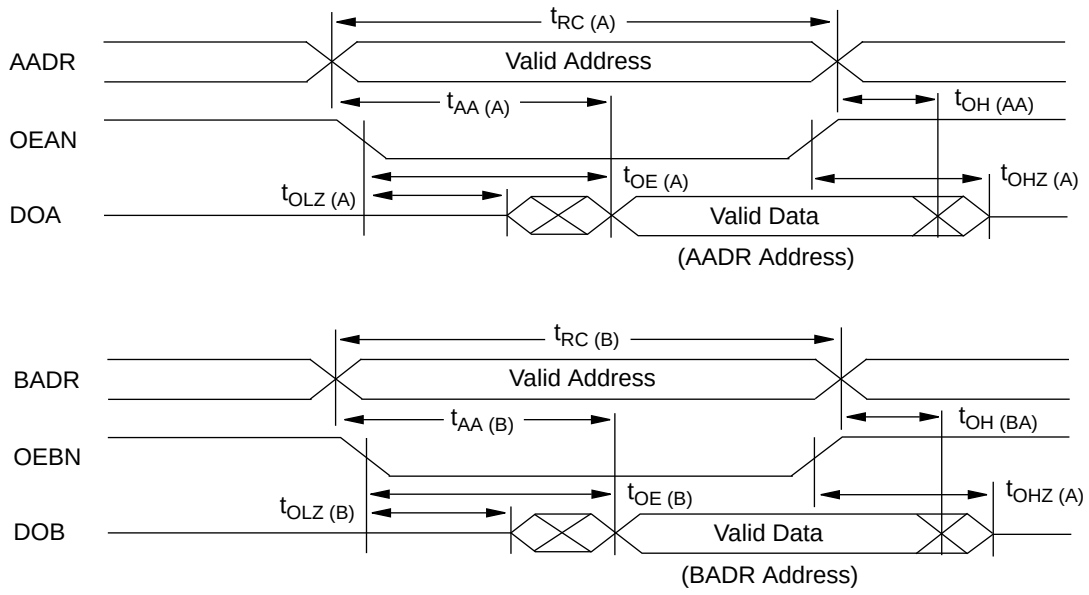
KG80		(Typical Process, 25˚C, 5V, t_R / t_F = 1.2ns, SL = 20)		
Symbol	**Parameter**	**tpd (ns)**		
		32x8 (Type=2)	**128x8 (Type=2)**	**256x8 (Type=2)**
Read Cycle				
$t_{RC\ (A)}$	Read Cycle Time	2.211	3.273	4.852
$t_{RC\ (B)}$		2.211	3.273	4.852
$t_{AA\ (A)}$	Address Access Time	2.619	3.680	5.268
$t_{AA\ (B)}$		2.217	3.672	5.260
$t_{OH\ (AA)}$	Output Hold Time from AADR Change	1.000	1.000	1.000
$t_{OH\ (BA)}$	Output Hold Time from BADR Change	1.000	1.000	1.000
$t_{OE\ (A)}$	Output Enable Time	1.675	1.675	1.675
$t_{OE\ (B)}$		1.675	1.675	1.675
$t_{OLZ\ (A)}$	Output Enable to Output Low-Z	1.175	1.175	1.175
$t_{OLZ\ (B)}$		1.175	1.175	1.175
$t_{OHZ\ (A)}$	Output Disable to Output High-Z	0.764	0.764	0.764
$t_{OHZ\ (B)}$		0.764	0.764	0.764
Write Cycle				
t_{WC}	Write Cycle Time	3.758	4.074	4.873
$t_{WA\ (A)}$	Write Enable Access Time	3.450	4.464	6.274
$t_{WA\ (B)}$		3.450	4.464	6.274
$t_{DA\ (A)}$	Data-In Access Time	2.217	3.525	5.328
$t_{DA\ (B)}$		2.217	3.525	5.328
t_{WP}	Write Enable Pulse Width	2.006	2.287	2.755
t_{AS}	Address Setup Time	1.410	1.224	1.317
t_{AH}	Address Hold Time	0.000	0.193	0.357
t_{DW}	Data-In Setup Time	0.174	0.218	0.375
t_{DH}	Data-In Hold Time	1.025	1.081	1.347
$t_{OH\ (AD)}$	DOA Hold Time from DIA Change	1.000	1.000	1.000
$t_{OH\ (BD)}$	DOB Hold Time from DIA Change	1.000	1.000	1.000
$t_{OH\ (AW)}$	DOA Hold Time from WEAN Change	0.242	0.242	0.242
$t_{OH\ (BW)}$	DOB Hold Time from WEAN Change	0.242	0.242	0.242

AC Parameters (Continued)

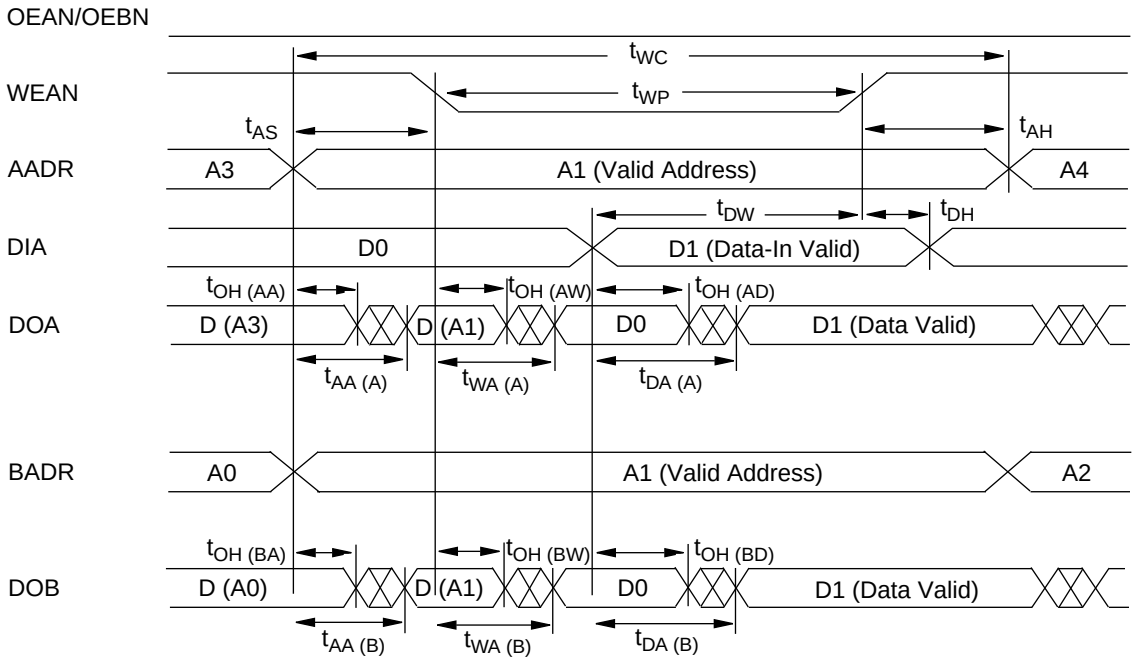
KGM80		(Typical Process, 25˚C, 3.3V, t_R / t_F = 1.2ns, SL = 20)		
Symbol	**Parameter**	**tpd (ns)**		
		32x8 (Type=2)	**128x8 (Type=2)**	**256x8 (Type=2)**
Read Cycle				
$t_{RC\ (A)}$	Read Cycle Time	3.122	4.557	6.698
$t_{RC\ (B)}$		3.122	4.557	6.698
$t_{AA\ (A)}$	Address Access Time	3.596	5.140	7.437
$t_{AA\ (B)}$		3.581	5.126	7.424
$t_{OH\ (AA)}$	Output Hold Time from AADR Change	1.000	1.000	1.000
$t_{OH\ (BA)}$	Output Hold Time from BADR Change	1.000	1.000	1.000
$t_{OE\ (A)}$	Output Enable Time	2.220	2.220	2.220
$t_{OE\ (B)}$		2.220	2.220	2.220
$t_{OLZ\ (A)}$	Output Enable to Output Low-Z	1.565	1.565	1.565
$t_{OLZ\ (B)}$		1.565	1.565	1.565
$t_{OHZ\ (A)}$	Output Disable to Output High-Z	1.135	1.135	1.135
$t_{OHZ\ (B)}$		1.135	1.135	1.135
Write Cycle				
t_{WC}	Write Cycle Time	4.729	5.379	6.375
$t_{WA\ (A)}$	Write Enable Access Time	4.867	6.281	8.786
$t_{WA\ (B)}$		4.867	6.281	8.786
$t_{DA\ (A)}$	Data-In Access Time	2.995	4.752	7.473
$t_{DA\ (B)}$		2.995	4.752	7.473
t_{WP}	Write Enable Pulse Width	2.570	2.911	3.452
t_{AS}	Address Setup Time	1.728	1.576	1.790
t_{AH}	Address Hold Time	0.000	0.402	0.552
t_{DW}	Data-In Setup Time	0.000	0.028	0.619
t_{DH}	Data-In Hold Time	1.604	1.722	2.071
$t_{OH\ (AD)}$	DOA Hold Time from DIA Change	1.000	1.000	1.000
$t_{OH\ (BD)}$	DOB Hold Time from DIA Change	1.000	1000	1.000
$t_{OH\ (AW)}$	DOA Hold Time from WEAN Change	0.399	0.399	0.399
$t_{OH\ (BW)}$	DOB Hold Time from WEAN Change	0.399	0.399	0.399

Timing Diagram

Read Cycle



Write Cycle



* D (An): data which are stored in An address

1RW1R DPRAM

Asynchronous One Read/Write One Read Dual-Port RAM Generator

Architecture

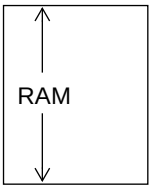
Type 1

For Type 1, the specified number of words will equal the number of columns and the specified number of bits will equal the number of rows in the RAM array.

Type 2

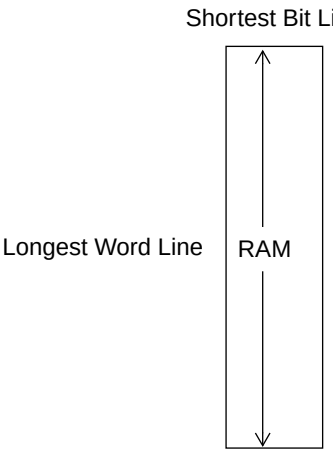
For the same size RAM, Type 2 will have twice the specified number of columns and one-half the specified number of rows.

Type 4



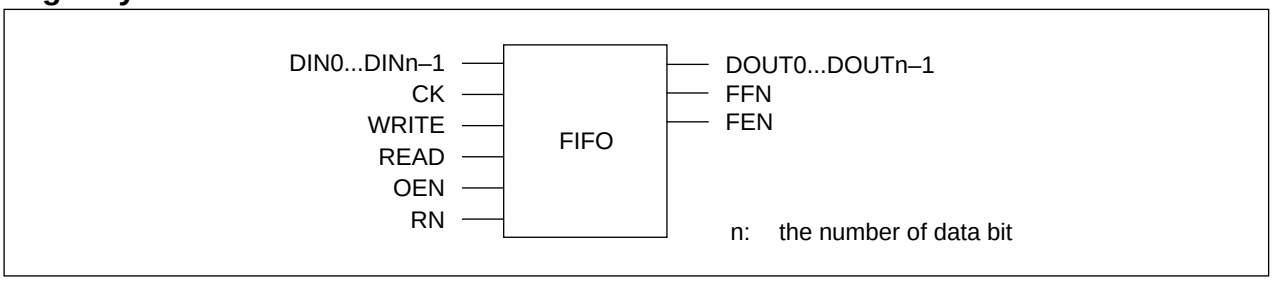
For the same size RAM, Type 4 will have four times the specified number of columns and one-fourth the specified number of rows.

Type 8



For the same size RAM, Type 8 will have eight times the specified number of columns and one-eighth the specified number of rows.

Logic Symbol



Description

FIFO builder generates a compiled first-in first-out memory block. FIFO is based on a dual-port RAM that permits completely asynchronous read/write operation. Read and write address values are stored in counters that can be cleared with the RN (reset) input. FIFO builder also has status flags for empty and full.

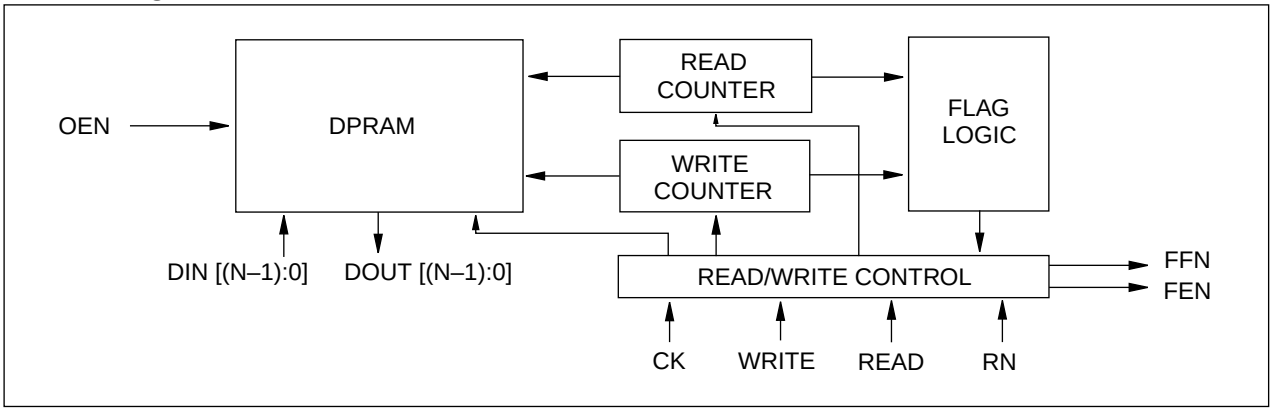
Features

- Fully asynchronous read/write operation
- 1 data input and 1 data output port
- Zero standby power
- High speed
- Parameter-driven compiler
- Variable word depth
  – 8, 10, 12, 14, 16,..., 1024
- Variable word width
  – 4, 5, 6, 7, 8,..., 72

I/O Pin Description

Name	I/O	Description
DIN0...DINn–1	I	Data Input
CK	I	Synchronous Read/Write Operation
WRITE	I	Asynchronous Write Operation
READ	I	Asynchronous Read Operation
OEN	I	Output Enable
RN	I	Reset, Status Flag Initialization
DOUT0...DOUTn–1	O	Data Output
FFN	O	Full Flag
FEN	O	Empty Flag

Block Diagram



FIFO

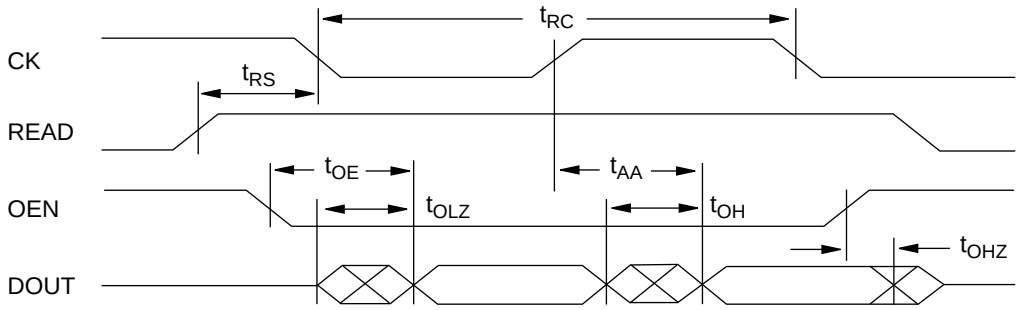
Ram-Based First-In First-Out Memory Generator

Configurations

- Word: All even numbers between 8 and 1024.
- Bit: 4, 5, 6, 7,..., 69, 70, 71, 72

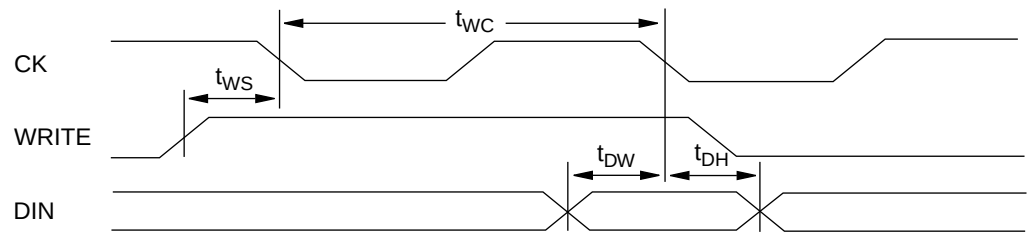
Timing Diagram

Read Cycle

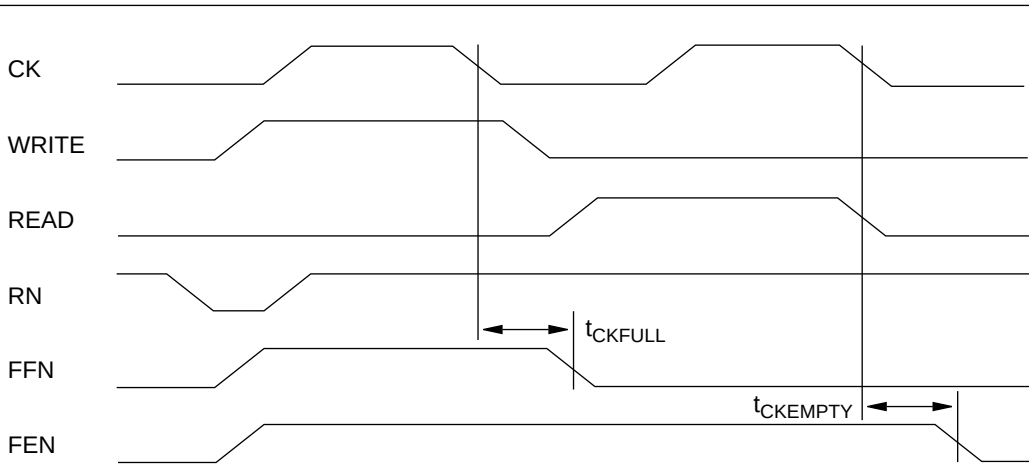


t_{RC}	Read Cycle Time	t_{OLZ}	Output Disable to Output Low-Z
t_{RS}	Read Setup Time	t_{OHZ}	Output Disable to Output High -Z
t_{OE}	Output Enable Time	t_{AA}	Address Access Time
t_{OH}	Output Data Hold Time		

Write Cycle

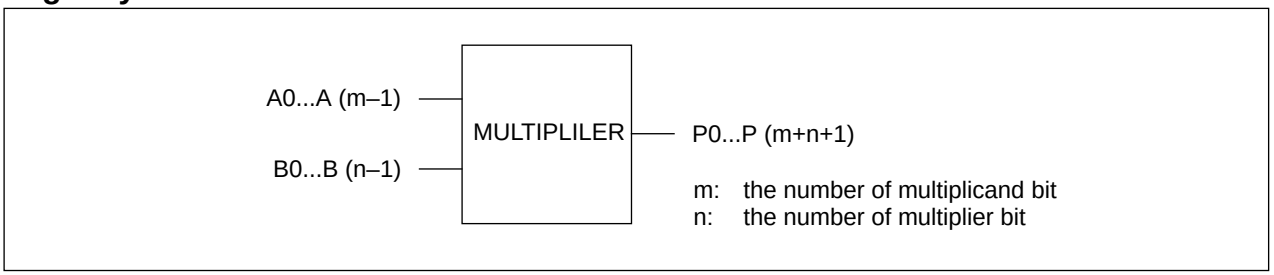


t_{WC}	Write Cycle Time	t_{DH}	Data-In Hold Time
t_{WS}	Write Setup Time	t_{DW}	Data-In Setup Time



t_{CKFULL}	CK Low to FFN Low	$t_{CKEMPTY}$	CK Low to FEN Low

Logic Symbol



Description

The function is P = A * B (A = multiplicand, B = multiplier and P = product of (A * B)). A, B and P are two's compliment formats.

The width of A input = m bit, range from [2 ** (m – 1) – 1] to [–2 ** (m – 1)] and the width of B input = n bit, range from [2 ** (n – 1) – 1] to [–2 ** (n – 1)].
The smaller bit width between A and B will be the multiplier and of even bits. That is, the multiplier might be the sum of smaller bit width and one.
The width of P output = (m + n) bit, assume that multiplicand is m bits and multiplier is n bits. m ≥ n, range from [2 ^ (m + n – 2)] to [2 ^ (n – 1) –2 ^ (m + n – 2)], 4 ≤ m and n ≤ 32.
You can choose a cell compiled with your bit request. This is the softmacro cell.

Features

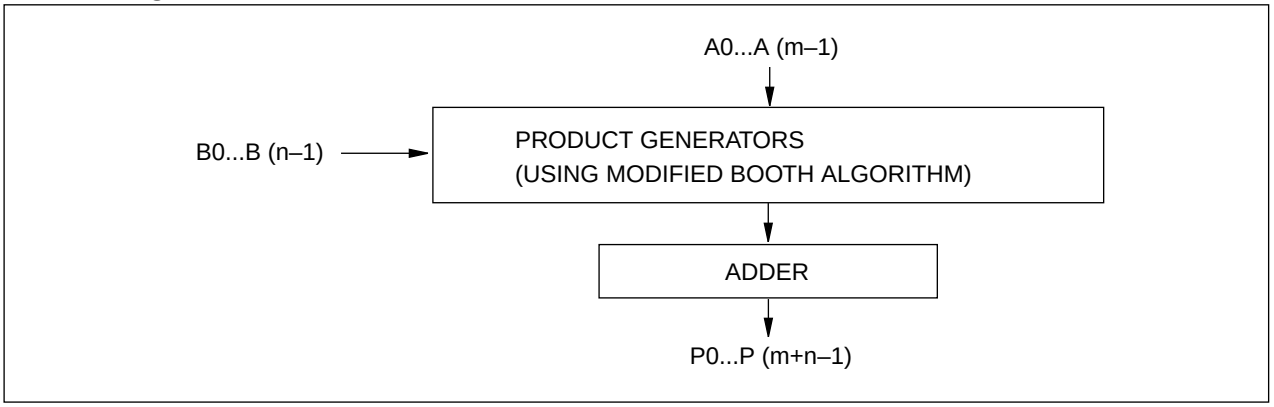
- Variable size multiplier and multiplicand bits
- Zero standby power
- High speed
- Parameter-driven compiler
- 32 bits of multiplier and multiplicand
- Variable bit size
  – Multiplicand size: 4–32 bits
  – Multiplier size: 4–32 bits

Configurations

- A: 4,..., 32
- B: 4,..., 32

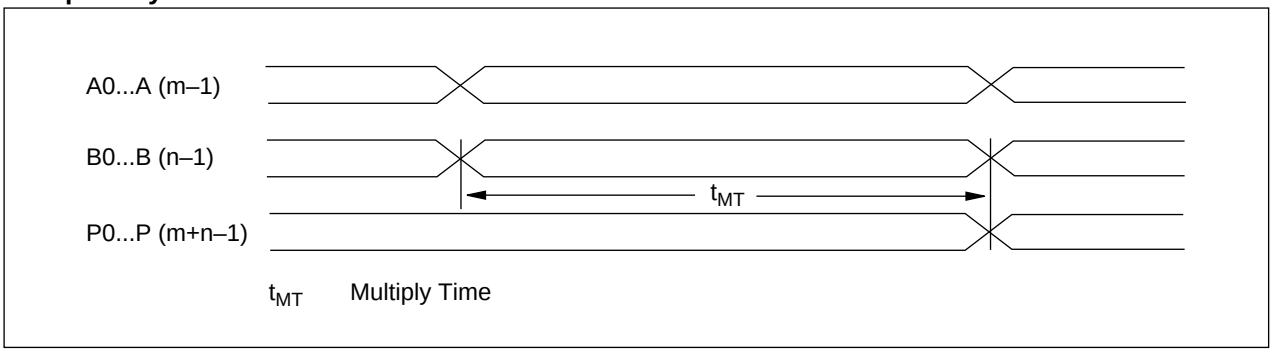
Standard design kit supports the following configurations: 8×8, 12×12, 16×16, 24×24, 32×32.
Other configurations can be provided upon request.

Block Diagram



Timing Diagram

Multiplier Cycle



JTAG Boundary Scans 6

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OVERVIEW

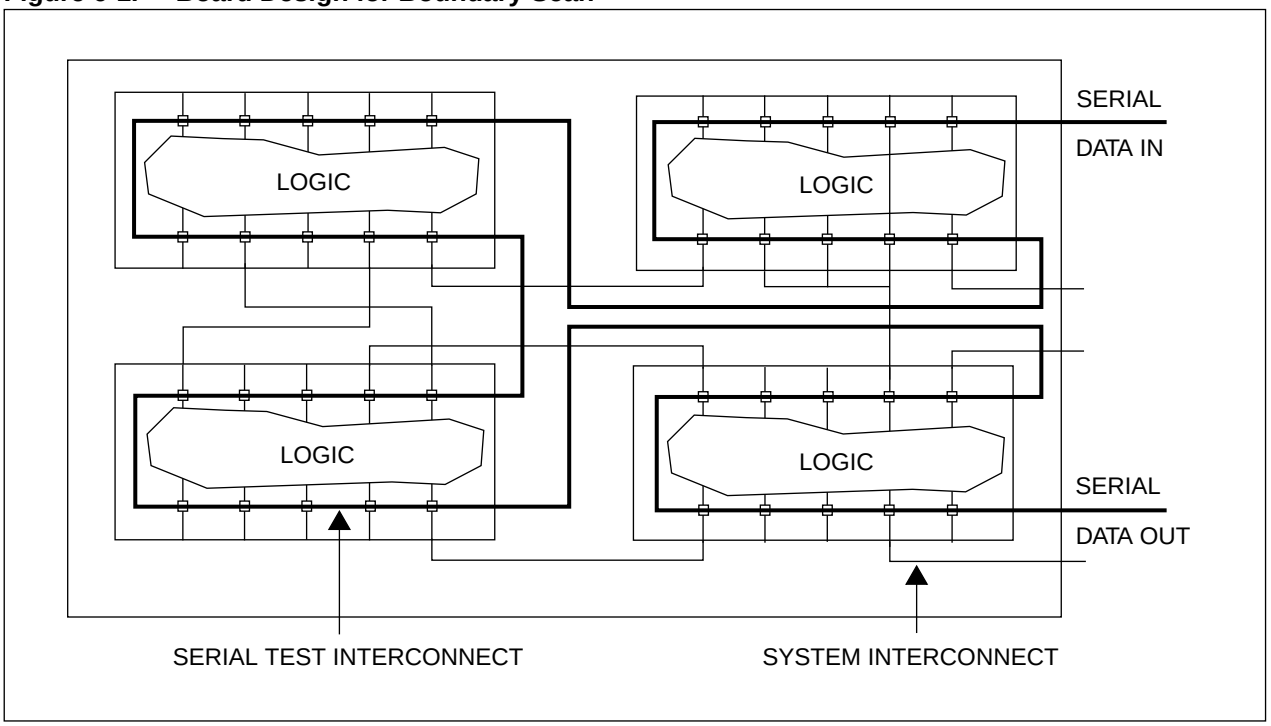
A board test is typically achieved by using in-circuit test techniques. However, in-circuit test techniques demonstrate significant limitations for Surface Mount Technology (SMT) and Fine Pitch Technology (FPT) boards. The pin and pad spacings getting tighter make it difficult to test boards with traditional methods economically and reliably.

A boundary scan design reduces the cost of a function test. A boundary scan design circuitry allows boards to be tested using the equivalent in-circuit test technique without bed-of-nails fixture. In recognition of the increasing acceptance of the boundary scan test, IEEE and JTAG (Joint Test Action Group) developed IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std 1149.1).

A boundary scan technique requires to place a boundary scan cell adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles. Each boundary scan cell for a given component is able to capture data from an input pin or from its internal logic, and to drive its internal logic or an output pin. Boundary scan cells for the pins of a given component are interconnected so as to form a shift-register chain around the border of the design, known as a boundary scan register. Boundary scan registers for individual components can be connected in series to form a single path through the complete design as shown in the figure 9-1. Alternatively, a board design can contain several independent boundary scan paths that allow individual components to be tested as well as the interconnections between components.

To test component interconnections, test data are first shifted into all boundary scan register cells associated with component output test pins. Test data are then loaded into parallel inputs of boundary scan cells associated with input pins through the component interconnections, and data captured in these cells are shifted out from the boundary cells for evaluation. For an individual component test, a boundary scan register is used to isolate on-chip system logic from stimuli received from surrounding components. An actual test can be performed through the boundary scan path or the built-in self-test hardware.

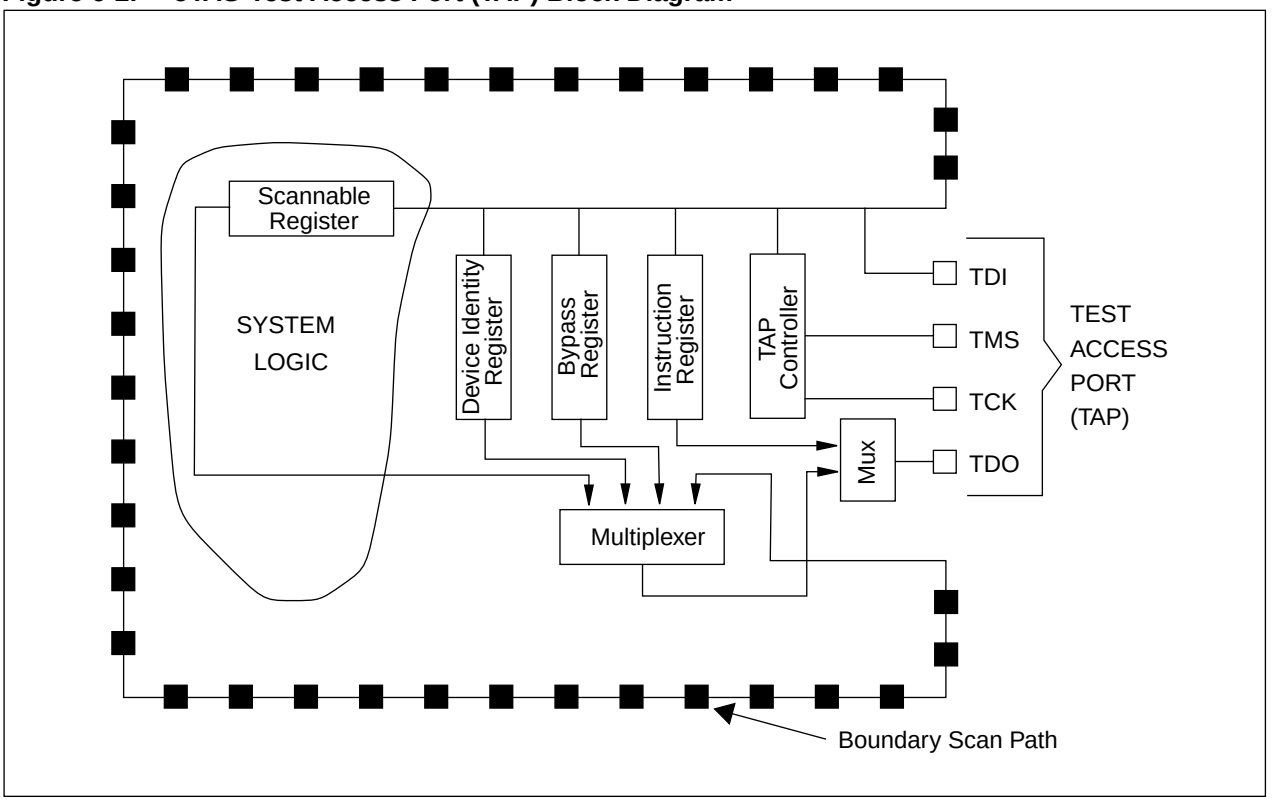
Figure 6-1. Board Design for Boundary Scan



BOUNDARY SCAN ARCHITECTURE

A boundary scan architecture contains TAP (Test Access Port), TAP controller, instruction register and a group of test data registers. The instruction and test data registers are separate shift-register-based paths connected in parallel with a common serial data input and a common serial data output which are connected to TAP, TDI and TDO signals. TAP controller selects the alternative instruction and test data register paths between TDI and TDO. The schematic view of the top level design of the test logic architecture is shown in the figure 9-2.

Figure 6-2. JTAG Test Access Port (TAP) Block Diagram



Boundary Scan Functional Block Descriptions

TAP (Test Access Port)

TAP is a general-purpose port that can provide with an access to many test support functions built into a component, including the test logic. It includes three inputs (TCK; Test Clock Signal, TMS; Test Mode Signal and TDI; Test Data Input) and one output (TDO; Test Data Output) required by the test logic. An optional fourth input (TRSTN; Test Reset) is provided for the asynchronous initialization of the test logic. The values applied at TMS and TDI pins are sampled on the rising edge of TCK, and the value placed on TDO pin changes on the falling edge of TCK.

TAP Controller

TAP controller receives TCK, interprets the signals on TMS, and generates clock and control signals for both instruction and test data registers and for other parts of the test circuitries as required.

Instruction Register/Instruction Decoder

Test instructions are shifted into and held by the instruction register. Test instructions include a selection of tests to be performed or the test data register to be accessed. A basic 3-bit instruction register and its instruction decoder are provided as macrofunctions in the library.

Test Data Registers

Data registers include a bypass register, a boundary scan register, a device identification register and other design specific registers. Only the bypass- and boundary scan registers are mandatory; the rest are optional.

Bypass register:	The bypass register provides a single-bit serial connection through the circuit when none of the other test data registers is selected. It can be used to allow test data to flow through a given device to the other components in a product without affecting a normal operation.
Boundary scan register:	The boundary scan register detects typical production defects in board interconnects, such as opens, shorts, etc. It also allows an access to component inputs and outputs when you test their logic or sample flow-through signals. Special boundary scan register macrocells are provided for this purpose. These special registers is discussed in the next section of next pages.
Design-specific test data register:	These optional registers may be provided to allow an access to design-specific test support features in the integrated circuit, such as self-test, scan test.
Device identification register:	This is an optional test data register that allows the manufacturer part number and variant of a components to be identified. The 32-bit identification register is partitioned into four fields:

Device version identifier	1st field	The first four bits beginning from MSB
Device part number	2nd field	16 bits
Manufacturer's JEDEC number	3rd field	11 bits
LSB	4th field	1 bit —tied in High

The ASIC designer is free to fill the version and part number in any manner as long as the total twenty bits are used.

SEC's JEDEC code:	78 decimal = 1001110 Continuation field (4 bits) = 0000
Contents of device identification register:	XXXX XXXXXXXXXXXXXXX 0000 1001110 1 Users can define these two fields.

BOUNDARY SCAN REGISTER MACROCELLS

The boundary scan register allows testing of circuitry external to the integrated circuit and provides for defined conditions to be established at the periphery of the on-chip system logic while it is tested itself. It also permits signals flowing through system pins to be sampled and examined without interfering with the operation of the on-chip system logic. The boundary scan register has four capabilities:

Capture: Loads data into the boundary scan register in parallel on the rising edge of TCK. It does not affect the output until Update is executed.

Shift: Shifts data from one boundary scan register to the next register towards the serial data output pin on the rising edge of TCK.

Update: Loads data in the boundary scan register into the parallel data output pin on the falling edge of TCK when EXTEST or INTEST instruction is selected.

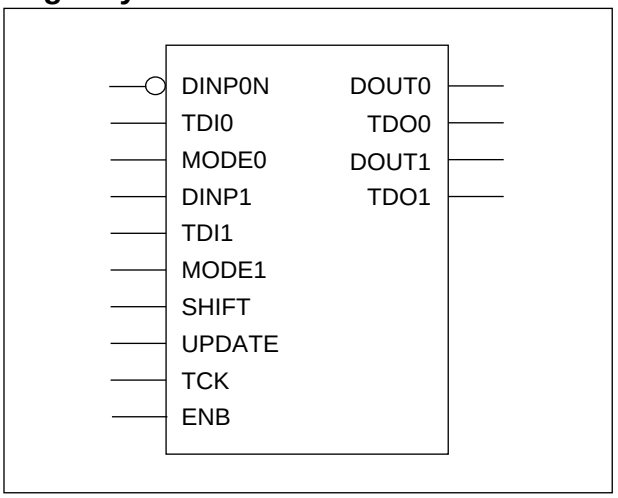
Set: Sets the parallel output pin.

SEC supports five types of boundary scan registers. Four of them, JTCK, JTBI1, JTIN1 and JTOUT1 are to be implemented around the periphery of the die next to I/O cells. For this reason, two I/O pads at each corner, that is, the total of eight I/O pads for the entire chip are not scannable. An implementation is automatically performed during a placement to achieve the most optimum placement with a minimum performance penalty. The fifth cell, JTINT1, is to be placed in the core area of the die for tri-state I/O control. Applications for each type of boundary scan register cell are summarized as follows.

Cell List

Cell Name	Function Description	Page
JTBI1	Bi-directional I/O Boundary Scan Cell	6-5
JTCK	Special Input (such as Clock Input) Boundary Scan Cell	6-12
JTIN1	Input Boundary Scan Cell	6-14
JTINT1	Tri-State I/O Control Boundary Scan Cell	6-18
JTOUT1	Output Boundary Scan Cell	6-24

Logic Symbol



Cell Data

Input Loading (SL)	
DINP0N	3
TDI0	3
MODE0	2
DINP1	4
TDI1	3
MODE1	2
SHIFT	3
UPDATE	3
TCK	1
ENB	1
Gate Count	
33	

Pin Description

Pin name	I/O	Description
DINP0N	I	Parallel Data Input Active Low for the Input Part of the Bi-Directional Pin
TDI0	I	Serial Test Data Input for Input Part of the Bi-Directional Pin
MODE0	I	Mode Select for Input Part—Low for Data Input and High for Internal Register Data Value
DINP1	I	Parallel Data Input Active Low for the Output Part of the Bi-Directional Pin
TDI1	I	Serial Test Data Input for Input Part of the Bi-Directional Pin
MODE1	I	Mode Select for Output Part—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable
DOUT0	O	Parallel Data Output for Input Part of the Bi-Directional Pin
TDO0	O	Serial Test Data Output for Input Part of the Bi-Directional Pin
DOUT1	O	Parallel Data Output for Output Part of the Bi-Directional Pin
TDO1	O	Serial Test Data Output for Output Part of the Bi-Directional Pin

JTBI1

Bi-directional I/O Scan Cell with Capture, Shift and Update

Truth Table

DINP0N	TDI0	MODE0	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT0
0	X	0	X	X	X	X	1
1	X	0	X	X	X	X	0
X	X	1	X	X	X	X	LatchQN
							TDO0
X	X	X	X	X	↗	0	TDO0o
0	X	0	0	X	↗	1	1
1	X	0	0	X	↗	1	0
X	X	1	0	X	↗	1	LatchQN
X	0	X	1	X	↗	1	0
X	1	X	1	X	↗	1	1
X	X	X	X	X	0	X	TDO0o
X	X	X	X	X	1	X	TDO0o
X	X	X	X	X	↘	X	TDO0o
							LatchQN
X	X	X	X	0	X	X	TDO0
X	X	X	X	1	X	X	LatchQNo

DINP1	TDI1	MODE1	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT1
0	X	0	X	X	X	X	0
1	X	0	X	X	X	X	1
X	X	1	X	X	X	X	LatchQ
							TDO1
X	X	X	X	X	↗	0	TDO1o
0	X	X	0	X	↗	1	0
1	X	X	0	X	↗	1	1
X	0	X	1	X	↗	1	0
X	1	X	1	X	↗	1	1
X	X	X	X	X	0	X	TDO1o
X	X	X	X	X	1	X	TDO1o
X	X	X	X	X	↘	X	TDO1o
							LatchQ
X	X	X	X	0	X	X	TDO1
X	X	X	X	1	X	X	LatchQo

NOTES:

1. Outputs are defined in separate truth tables. In addition, the internal states known as “LatchQ” and “LatchQN” are defined as the output of the latch in the logic diagram.
2. JTBI1 has a similar truth table to JTIN1 and JTOUT1 macrocells without SETN input. It has similar delays to JTIN1 and JTOUT1.

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		KG80	KGM80
Input Setup Time (TDI0 to TCK)	t_{SU}	0.34	0.64
Input Hold Time (TDI0 to TCK)	t_{HD}	0.15	0.33
Input Setup Time (TDI0 to ENB)	t_{SU}	0.34	0.64
Input Hold Time (TDI0 to ENB)	t_{HD}	0.15	0.33
Input Setup Time (TDI1 to TCK)	t_{SU}	0.34	0.64
Input Hold Time (TDI1 to TCK)	t_{HD}	0.15	0.33
Input Setup Time (TDI1 to ENB)	t_{SU}	0.34	0.64
Input Hold Time (TDI1 to ENB)	t_{HD}	0.15	0.33
Input Setup Time (DINP0N to TCK)	t_{SU}	0.56	0.99
Input Hold Time (DINP0N to TCK)	t_{HD}	0.15	0.33
Input Setup Time (DINP0N to ENB)	t_{SU}	0.56	0.99
Input Hold Time (DINP0N to ENB)	t_{HD}	0.15	0.33
Input Setup Time (DINP1 to TCK)	t_{SU}	0.37	0.68
Input Hold Time (DINP1 to TCK)	t_{HD}	0.15	0.33
Input Setup Time (DINP1 to ENB)	t_{SU}	0.34	0.64
Input Hold Time (DINP1 to ENB)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to TCK)	t_{HD}	0.15	0.30
Input Setup Time (SHIFT to ENB)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to ENB)	t_{HD}	0.15	0.33
Input Setup Time (MODE0 to TCK)	t_{SU}	0.64	1.08
Input Hold Time (MODE0 to TCK)	t_{HD}	0.15	0.33
Input Setup Time (MODE0 to ENB)	t_{SU}	0.64	1.08
Input Hold Time (MODE0 to ENB)	t_{HD}	0.15	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 JTBI1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO0	t_{PLH}	0.85	0.76 + 0.043*SL	0.76 + 0.042*SL	0.76 + 0.042*SL
	t_{PHL}	0.73	0.66 + 0.034*SL	0.68 + 0.027*SL	0.70 + 0.024*SL
	t_R	0.28	0.10 + 0.086*SL	0.10 + 0.089*SL	0.09 + 0.090*SL
	t_F	0.19	0.10 + 0.043*SL	0.11 + 0.040*SL	0.11 + 0.041*SL
ENB to TDO0	t_{PLH}	0.84	0.75 + 0.043*SL	0.76 + 0.041*SL	0.75 + 0.042*SL
	t_{PHL}	0.71	0.64 + 0.034*SL	0.66 + 0.027*SL	0.68 + 0.024*SL
	t_R	0.28	0.11 + 0.085*SL	0.10 + 0.089*SL	0.10 + 0.088*SL
	t_F	0.19	0.11 + 0.043*SL	0.11 + 0.040*SL	0.10 + 0.042*SL
TCK to TDO1	t_{PLH}	0.81	0.73 + 0.042*SL	0.73 + 0.042*SL	0.73 + 0.042*SL
	t_{PHL}	0.68	0.62 + 0.031*SL	0.63 + 0.026*SL	0.65 + 0.023*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
ENB to TDO1	t_{PLH}	0.80	0.72 + 0.042*SL	0.72 + 0.042*SL	0.72 + 0.042*SL
	t_{PHL}	0.67	0.61 + 0.031*SL	0.62 + 0.026*SL	0.64 + 0.024*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.089*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
DINP0N to DOUT0	t_{PLH}	0.21	0.17 + 0.020*SL	0.17 + 0.021*SL	0.15 + 0.024*SL
	t_{PHL}	0.10	0.02 + 0.039*SL	0.07 + 0.019*SL	0.10 + 0.015*SL
	t_R	0.22	0.13 + 0.044*SL	0.15 + 0.038*SL	0.12 + 0.041*SL
	t_F	0.19	0.11 + 0.041*SL	0.16 + 0.019*SL	0.17 + 0.019*SL
MODE0 to DOUT0	t_{PLH}	0.27	0.22 + 0.025*SL	0.23 + 0.018*SL	0.21 + 0.022*SL
	t_{PHL}	0.26	0.22 + 0.021*SL	0.23 + 0.019*SL	0.26 + 0.014*SL
	t_R	0.20	0.11 + 0.042*SL	0.11 + 0.044*SL	0.11 + 0.043*SL
	t_F	0.14	0.10 + 0.022*SL	0.10 + 0.019*SL	0.09 + 0.021*SL
UPDATE to DOUT0	t_{PLH}	0.58	0.53 + 0.024*SL	0.54 + 0.023*SL	0.55 + 0.021*SL
	t_{PHL}	0.64	0.56 + 0.037*SL	0.60 + 0.022*SL	0.66 + 0.014*SL
	t_R	0.21	0.12 + 0.044*SL	0.10 + 0.052*SL	0.17 + 0.042*SL
	t_F	0.22	0.16 + 0.030*SL	0.18 + 0.025*SL	0.21 + 0.020*SL
TCK to DOUT0	t_{PLH}	1.27	1.22 + 0.026*SL	1.23 + 0.022*SL	1.23 + 0.022*SL
	t_{PHL}	1.16	1.11 + 0.026*SL	1.12 + 0.021*SL	1.15 + 0.017*SL
	t_R	0.21	0.12 + 0.043*SL	0.12 + 0.043*SL	0.11 + 0.045*SL
	t_F	0.22	0.16 + 0.030*SL	0.18 + 0.024*SL	0.19 + 0.022*SL
ENB to DOUT0	t_{PLH}	1.27	1.22 + 0.025*SL	1.22 + 0.022*SL	1.23 + 0.021*SL
	t_{PHL}	1.15	1.10 + 0.026*SL	1.12 + 0.021*SL	1.14 + 0.017*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.044*SL	0.12 + 0.044*SL
	t_F	0.22	0.16 + 0.031*SL	0.18 + 0.023*SL	0.19 + 0.022*SL
DINP1 to DOUT1	t_{PLH}	0.31	0.23 + 0.043*SL	0.23 + 0.041*SL	0.23 + 0.041*SL
	t_{PHL}	0.36	0.30 + 0.027*SL	0.30 + 0.028*SL	0.33 + 0.025*SL
	t_R	0.28	0.10 + 0.087*SL	0.10 + 0.089*SL	0.06 + 0.096*SL
	t_F	0.21	0.12 + 0.048*SL	0.14 + 0.041*SL	0.13 + 0.041*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 JTBI1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
MODE1 to DOUT1	t_{PLH}	0.24	0.14 + 0.053*SL	0.17 + 0.038*SL	0.11 + 0.047*SL
	t_{PHL}	0.31	0.22 + 0.043*SL	0.27 + 0.024*SL	0.26 + 0.025*SL
	t_R	0.29	0.11 + 0.088*SL	0.10 + 0.092*SL	0.15 + 0.085*SL
	t_F	0.19	0.12 + 0.037*SL	0.10 + 0.042*SL	0.10 + 0.043*SL
UPDATE to DOUT1	t_{PLH}	0.70	0.63 + 0.034*SL	0.61 + 0.042*SL	0.61 + 0.043*SL
	t_{PHL}	0.62	0.55 + 0.035*SL	0.57 + 0.030*SL	0.61 + 0.023*SL
	t_R	0.28	0.11 + 0.083*SL	0.09 + 0.090*SL	0.10 + 0.090*SL
	t_F	0.20	0.12 + 0.043*SL	0.12 + 0.043*SL	0.15 + 0.039*SL
TCK to DOUT1	t_{PLH}	1.40	1.31 + 0.045*SL	1.32 + 0.041*SL	1.31 + 0.043*SL
	t_{PHL}	1.28	1.21 + 0.035*SL	1.22 + 0.028*SL	1.24 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.09 + 0.094*SL	0.14 + 0.087*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.040*SL	0.13 + 0.041*SL
ENB to DOUT1	t_{PLH}	1.39	1.31 + 0.042*SL	1.30 + 0.042*SL	1.30 + 0.042*SL
	t_{PHL}	1.27	1.20 + 0.033*SL	1.21 + 0.029*SL	1.24 + 0.025*SL
	t_R	0.28	0.11 + 0.085*SL	0.08 + 0.095*SL	0.14 + 0.088*SL
	t_F	0.21	0.12 + 0.044*SL	0.13 + 0.041*SL	0.11 + 0.043*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

JTBI1

Bi-directional I/O Scan Cell with Capture, Shift and Update

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 JTBI1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO0	t_{PLH}	1.20	1.09 + 0.053*SL	1.10 + 0.049*SL	1.10 + 0.050*SL
	t_{PHL}	1.02	0.96 + 0.030*SL	0.98 + 0.023*SL	0.90 + 0.030*SL
	t_R	0.36	0.15 + 0.104*SL	0.13 + 0.110*SL	0.18 + 0.106*SL
	t_F	0.21	0.14 + 0.034*SL	0.15 + 0.033*SL	-0.09 + 0.054*SL
ENB to TDO0	t_{PLH}	1.20	1.10 + 0.049*SL	1.09 + 0.051*SL	1.11 + 0.049*SL
	t_{PHL}	1.01	0.93 + 0.039*SL	0.96 + 0.029*SL	1.01 + 0.024*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.109*SL	0.14 + 0.109*SL
	t_F	0.23	0.14 + 0.047*SL	0.15 + 0.041*SL	0.14 + 0.042*SL
TCK to TDO1	t_{PLH}	1.15	1.06 + 0.048*SL	1.05 + 0.051*SL	1.06 + 0.050*SL
	t_{PHL}	0.96	0.89 + 0.036*SL	0.91 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.35	0.15 + 0.103*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.09 + 0.044*SL
ENB to TDO1	t_{PLH}	1.16	1.05 + 0.054*SL	1.06 + 0.050*SL	1.06 + 0.050*SL
	t_{PHL}	0.96	0.89 + 0.034*SL	0.92 + 0.026*SL	0.95 + 0.023*SL
	t_R	0.36	0.16 + 0.100*SL	0.13 + 0.108*SL	0.09 + 0.112*SL
	t_F	0.20	0.11 + 0.046*SL	0.13 + 0.041*SL	0.08 + 0.046*SL
DINP0N to DOUT0	t_{PLH}	0.28	0.24 + 0.020*SL	0.23 + 0.025*SL	0.23 + 0.024*SL
	t_{PHL}	0.16	0.08 + 0.041*SL	0.14 + 0.017*SL	0.28 + 0.004*SL
	t_R	0.25	0.16 + 0.044*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.23	0.15 + 0.043*SL	0.21 + 0.020*SL	0.36 + 0.007*SL
MODE0 to DOUT0	t_{PLH}	0.34	0.31 + 0.015*SL	0.28 + 0.028*SL	0.31 + 0.024*SL
	t_{PHL}	0.36	0.32 + 0.018*SL	0.32 + 0.018*SL	0.36 + 0.015*SL
	t_R	0.25	0.14 + 0.055*SL	0.15 + 0.053*SL	0.11 + 0.056*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.020*SL	0.12 + 0.022*SL
UPDATE to DOUT0	t_{PLH}	0.77	0.70 + 0.033*SL	0.72 + 0.028*SL	0.72 + 0.028*SL
	t_{PHL}	0.91	0.83 + 0.044*SL	0.88 + 0.025*SL	0.96 + 0.017*SL
	t_R	0.26	0.15 + 0.055*SL	0.15 + 0.055*SL	0.17 + 0.053*SL
	t_F	0.29	0.21 + 0.039*SL	0.24 + 0.028*SL	0.33 + 0.020*SL
TCK to DOUT0	t_{PLH}	1.83	1.77 + 0.031*SL	1.78 + 0.028*SL	1.81 + 0.025*SL
	t_{PHL}	1.69	1.62 + 0.034*SL	1.65 + 0.024*SL	1.72 + 0.018*SL
	t_R	0.26	0.15 + 0.055*SL	0.16 + 0.052*SL	0.12 + 0.056*SL
	t_F	0.29	0.22 + 0.035*SL	0.24 + 0.028*SL	0.32 + 0.021*SL
ENB to DOUT0	t_{PLH}	1.83	1.77 + 0.032*SL	1.78 + 0.028*SL	1.81 + 0.025*SL
	t_{PHL}	1.69	1.62 + 0.034*SL	1.65 + 0.024*SL	1.72 + 0.017*SL
	t_R	0.26	0.15 + 0.058*SL	0.16 + 0.055*SL	0.17 + 0.053*SL
	t_F	0.29	0.21 + 0.037*SL	0.24 + 0.027*SL	0.29 + 0.022*SL
DINP1 to DOUT1	t_{PLH}	0.40	0.30 + 0.048*SL	0.29 + 0.051*SL	0.30 + 0.050*SL
	t_{PHL}	0.49	0.41 + 0.040*SL	0.43 + 0.032*SL	0.54 + 0.022*SL
	t_R	0.37	0.15 + 0.114*SL	0.17 + 0.104*SL	0.11 + 0.110*SL
	t_F	0.27	0.17 + 0.052*SL	0.19 + 0.042*SL	0.21 + 0.040*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 JTBI1

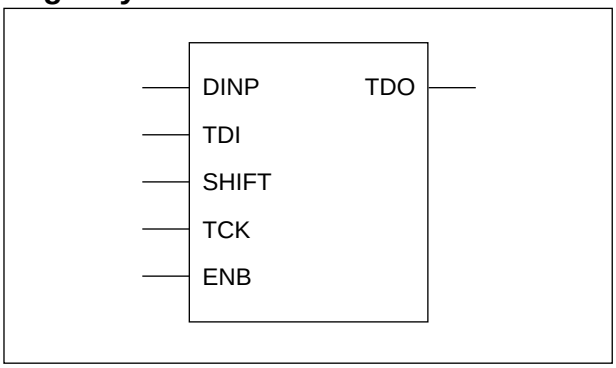
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
MODE1 to DOUT1	t_{PLH}	0.31	0.23 + 0.040*SL	0.20 + 0.050*SL	0.22 + 0.049*SL
	t_{PHL}	0.39	0.31 + 0.039*SL	0.33 + 0.032*SL	0.43 + 0.022*SL
	t_R	0.37	0.14 + 0.114*SL	0.16 + 0.108*SL	0.16 + 0.108*SL
	t_F	0.25	0.15 + 0.048*SL	0.16 + 0.043*SL	0.15 + 0.044*SL
UPDATE to DOUT1	t_{PLH}	0.97	0.85 + 0.062*SL	0.89 + 0.048*SL	0.84 + 0.052*SL
	t_{PHL}	0.86	0.77 + 0.044*SL	0.80 + 0.033*SL	0.91 + 0.023*SL
	t_R	0.37	0.18 + 0.094*SL	0.14 + 0.108*SL	0.12 + 0.110*SL
	t_F	0.27	0.17 + 0.047*SL	0.18 + 0.043*SL	0.21 + 0.040*SL
TCK to DOUT1	t_{PLH}	2.01	1.91 + 0.052*SL	1.92 + 0.050*SL	1.92 + 0.050*SL
	t_{PHL}	1.87	1.78 + 0.042*SL	1.81 + 0.031*SL	1.89 + 0.024*SL
	t_R	0.36	0.15 + 0.106*SL	0.14 + 0.110*SL	0.16 + 0.108*SL
	t_F	0.27	0.17 + 0.048*SL	0.18 + 0.044*SL	0.22 + 0.041*SL
ENB to DOUT1	t_{PLH}	2.02	1.91 + 0.053*SL	1.92 + 0.050*SL	1.92 + 0.050*SL
	t_{PHL}	1.88	1.79 + 0.042*SL	1.82 + 0.030*SL	1.88 + 0.025*SL
	t_R	0.36	0.15 + 0.103*SL	0.13 + 0.111*SL	0.17 + 0.107*SL
	t_F	0.28	0.18 + 0.048*SL	0.20 + 0.041*SL	0.18 + 0.043*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

JTCK

Special Input Scan Cell with Capture and Shift

Logic Symbol



Cell Data

Input Loading (SL)	
DINP	1
TDI	1
SHIFT	2
TCK	1
ENB	1
Gate Count	
9	

General Description

JTCK is a special input boundary scan cell for clock pad. It has capture and shift capabilities only. JTCK doesn't have update and set capabilities, but has clock enable capability.

Pin Description

Pin name	I/O	Description
DINP	I	Parallel System Data Input
TDI	I	Serial Test Data Input
SHIFT	I	Active High Shift Control Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
TDO	O	Serial Test Data Output

Truth Table

DINP	TDI	SHIFT	TCK	ENB	TDO
X	X	X	↑	0	TDOo
0	X	0	↑	1	0
1	X	0	↑	1	1
X	0	1	↑	1	0
X	1	1	↑	1	1
X	X	X	0	X	TDOo
X	X	X	1	X	TDOo
X	X	X	↓	X	TDOo

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		KG80	KGM80
Input Setup Time (TDI to TCK)	t_{SU}	0.37	0.64
Input Hold Time (TDI to TCK)	t_{HD}	0.15	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.34	0.64
Input Hold Time (TDI to ENB)	t_{HD}	0.15	0.33
Input Setup Time (DINP to TCK)	t_{SU}	0.37	0.68
Input Hold Time (DINP to TCK)	t_{HD}	0.15	0.33
Input Setup Time (DINP to ENB)	t_{SU}	0.34	0.64
Input Hold Time (DINP to ENB)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to TCK)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to ENB)	t_{HD}	0.15	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 JTCK

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.58	0.50 + 0.042*SL	0.50 + 0.041*SL	0.49 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.032*SL	0.54 + 0.026*SL	0.56 + 0.023*SL
	t_R	0.27	0.10 + 0.087*SL	0.09 + 0.091*SL	0.11 + 0.089*SL
	t_F	0.18	0.10 + 0.040*SL	0.10 + 0.039*SL	0.07 + 0.044*SL
ENB to TDO	t_{PLH}	0.57	0.48 + 0.042*SL	0.48 + 0.042*SL	0.49 + 0.041*SL
	t_{PHL}	0.59	0.52 + 0.031*SL	0.54 + 0.026*SL	0.56 + 0.023*SL
	t_R	0.28	0.09 + 0.093*SL	0.10 + 0.089*SL	0.11 + 0.088*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.041*SL	0.07 + 0.043*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 JTCK

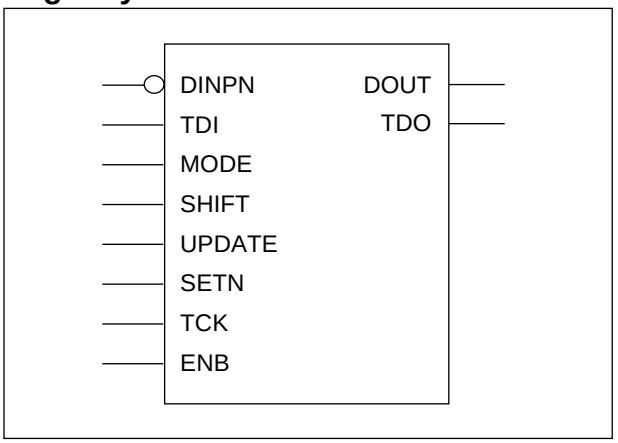
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.78	0.68 + 0.051*SL	0.68 + 0.050*SL	0.68 + 0.050*SL
	t_{PHL}	0.81	0.74 + 0.035*SL	0.77 + 0.026*SL	0.80 + 0.024*SL
	t_R	0.36	0.13 + 0.112*SL	0.15 + 0.107*SL	0.11 + 0.110*SL
	t_F	0.21	0.11 + 0.047*SL	0.13 + 0.042*SL	0.10 + 0.044*SL
ENB to TDO	t_{PLH}	0.76	0.66 + 0.052*SL	0.66 + 0.050*SL	0.67 + 0.050*SL
	t_{PHL}	0.81	0.74 + 0.035*SL	0.77 + 0.026*SL	0.79 + 0.024*SL
	t_R	0.36	0.15 + 0.105*SL	0.14 + 0.108*SL	0.13 + 0.109*SL
	t_F	0.21	0.11 + 0.050*SL	0.14 + 0.041*SL	0.12 + 0.042*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

JTIN1

Input Scan Cell with Capture, Shift, Update and Set

Logic Symbol



Cell Data

Input Loading (SL)	
DINPN	3
TDI	3
MODE	2
SHIFT	2
UPDATE	2
SETN	1
TCK	3
ENB	1
Gate Count	
16	

Pin Description

Pin name	I/O	Description
DINPN	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output

Truth Table

DINPN	TDI	MODE	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT
0	X	0	X	X	X	X	1
1	X	0	X	X	X	X	0
X	X	1	X	X	X	X	LatchQ
							TDO
X	X	X	X	X	↑	0	TDOo
0	X	0	0	X	↑	1	1
1	X	0	0	X	↑	1	0
X	X	1	0	X	↑	1	LatchQ
X	0	X	1	X	↑	1	0
X	1	X	1	X	↑	1	1
X	X	X	X	X	0	X	TDOo
X	X	X	X	X	1	X	TDOo
X	X	X	X	X	↓	X	TDOo
							LatchQ
X	X	X	X	0	X	X	0
X	X	X	X	1	0	X	TDO
X	X	X	X	1	1	X	LatchQo

NOTE: Outputs are defined in separate truth tables. In addition, an internal state known as “LatchQ” is defined as the output of the latch in the logic diagram.

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		KG80	KGM80
Input Setup Time (TDI to TCK)	t_{SU}	0.34	0.64
Input Hold Time (TDI to TCK)	t_{HD}	0.15	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.34	0.64
Input Hold Time (TDI to ENB)	t_{HD}	0.15	0.33
Input Setup Time (DINPN to TCK)	t_{SU}	0.56	0.99
Input Hold Time (DINPN to TCK)	t_{HD}	0.15	0.33
Input Setup Time (DINPN to ENB)	t_{SU}	0.56	0.99
Input Hold Time (DINPN to ENB)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to TCK)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to ENB)	t_{HD}	0.15	0.33
Input Setup Time (MODE to TCK)	t_{SU}	0.64	1.08
Input Hold Time (MODE to TCK)	t_{HD}	0.15	0.33
Input Setup Time (MODE to ENB)	t_{SU}	0.64	1.08
Input Hold Time (MODE to ENB)	t_{HD}	0.15	0.33
Recovery Time (SETN)	t_{RC}	0.15	0.33
Input Hold Time (SETN to UPDATE)	t_{HD}	0.15	0.33

JTIN1

Input Scan Cell with Capture, Shift, Update and Set

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 JTIN1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.60	0.51 + 0.041*SL	0.51 + 0.042*SL	0.51 + 0.042*SL
	t_{PHL}	0.61	0.55 + 0.033*SL	0.57 + 0.024*SL	0.57 + 0.023*SL
	t_R	0.32	0.14 + 0.089*SL	0.14 + 0.090*SL	0.13 + 0.091*SL
	t_F	0.19	0.11 + 0.041*SL	0.11 + 0.040*SL	0.10 + 0.042*SL
ENB to TDO	t_{PLH}	0.58	0.50 + 0.042*SL	0.50 + 0.042*SL	0.50 + 0.042*SL
	t_{PHL}	0.60	0.55 + 0.029*SL	0.55 + 0.025*SL	0.57 + 0.023*SL
	t_R	0.32	0.15 + 0.088*SL	0.14 + 0.090*SL	0.13 + 0.091*SL
	t_F	0.20	0.12 + 0.041*SL	0.12 + 0.039*SL	0.10 + 0.042*SL
DINPN to DOUT	t_{PLH}	0.21	0.17 + 0.023*SL	0.17 + 0.021*SL	0.56 + -0.033*SL
	t_{PHL}	0.11	0.04 + 0.033*SL	0.08 + 0.019*SL	0.45 + -0.033*SL
	t_R	0.21	0.14 + 0.035*SL	0.13 + 0.041*SL	0.83 + -0.058*SL
	t_F	0.20	0.15 + 0.026*SL	0.16 + 0.021*SL	0.56 + -0.035*SL
MODE to DOUT	t_{PLH}	0.34	0.29 + 0.023*SL	0.30 + 0.022*SL	0.68 + -0.033*SL
	t_{PHL}	0.27	0.22 + 0.020*SL	0.23 + 0.016*SL	0.53 + -0.026*SL
	t_R	0.17	0.08 + 0.043*SL	0.09 + 0.042*SL	0.83 + -0.062*SL
	t_F	0.14	0.10 + 0.025*SL	0.10 + 0.021*SL	0.49 + -0.033*SL
UPDATE to DOUT	t_{PLH}	0.69	0.63 + 0.025*SL	0.64 + 0.024*SL	1.06 + -0.035*SL
	t_{PHL}	0.69	0.65 + 0.020*SL	0.65 + 0.020*SL	1.05 + -0.036*SL
	t_R	0.20	0.11 + 0.042*SL	0.10 + 0.047*SL	0.91 + -0.066*SL
	t_F	0.21	0.16 + 0.025*SL	0.16 + 0.023*SL	0.59 + -0.037*SL
SETN to DOUT	t_{PLH}	0.56	0.51 + 0.025*SL	0.52 + 0.022*SL	0.93 + -0.036*SL
	t_{PHL}	0.50	0.44 + 0.026*SL	0.46 + 0.021*SL	0.85 + -0.035*SL
	t_R	0.20	0.12 + 0.040*SL	0.11 + 0.046*SL	0.89 + -0.065*SL
	t_F	0.21	0.14 + 0.035*SL	0.17 + 0.022*SL	0.61 + -0.039*SL
TCK to DOUT	t_{PLH}	1.19	1.14 + 0.025*SL	1.15 + 0.022*SL	1.56 + -0.036*SL
	t_{PHL}	1.30	1.23 + 0.031*SL	1.26 + 0.019*SL	1.64 + -0.035*SL
	t_R	0.20	0.11 + 0.043*SL	0.11 + 0.043*SL	0.86 + -0.063*SL
	t_F	0.21	0.15 + 0.028*SL	0.16 + 0.023*SL	0.60 + -0.038*SL
ENB to DOUT	t_{PLH}	1.17	1.13 + 0.025*SL	1.13 + 0.022*SL	1.54 + -0.036*SL
	t_{PHL}	1.29	1.23 + 0.027*SL	1.25 + 0.020*SL	1.64 + -0.035*SL
	t_R	0.20	0.11 + 0.042*SL	0.10 + 0.048*SL	0.91 + -0.067*SL
	t_F	0.21	0.14 + 0.032*SL	0.16 + 0.024*SL	0.61 + -0.039*SL

*Group1 : SL < 2, *Group2 : 2 ≦SL≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 JTIN1

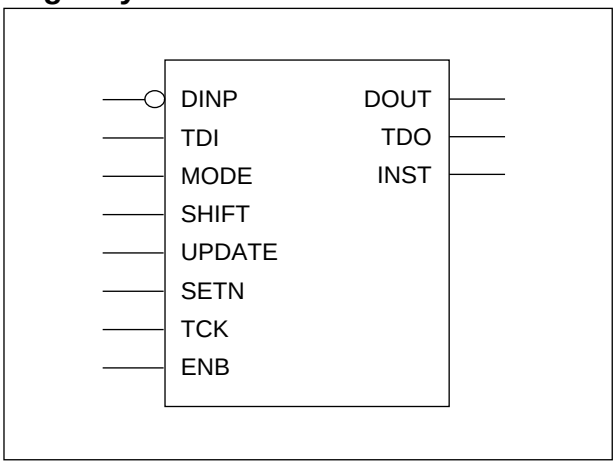
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.81	0.70 + 0.051*SL	0.71 + 0.050*SL	0.71 + 0.050*SL
	t_{PHL}	0.84	0.77 + 0.031*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.43	0.22 + 0.106*SL	0.21 + 0.109*SL	0.22 + 0.108*SL
	t_F	0.25	0.16 + 0.043*SL	0.17 + 0.040*SL	0.14 + 0.042*SL
ENB to TDO	t_{PLH}	0.83	0.73 + 0.051*SL	0.73 + 0.050*SL	0.73 + 0.050*SL
	t_{PHL}	0.86	0.80 + 0.031*SL	0.81 + 0.026*SL	0.84 + 0.023*SL
	t_R	0.43	0.22 + 0.106*SL	0.21 + 0.109*SL	0.20 + 0.110*SL
	t_F	0.24	0.15 + 0.043*SL	0.16 + 0.041*SL	0.15 + 0.042*SL
DINPN to DOUT	t_{PLH}	0.28	0.22 + 0.029*SL	0.23 + 0.025*SL	0.89 + -0.035*SL
	t_{PHL}	0.17	0.11 + 0.029*SL	0.14 + 0.019*SL	0.66 + -0.029*SL
	t_R	0.26	0.16 + 0.050*SL	0.15 + 0.051*SL	1.45 + -0.068*SL
	t_F	0.24	0.18 + 0.029*SL	0.20 + 0.023*SL	0.84 + -0.035*SL
MODE to DOUT	t_{PLH}	0.43	0.39 + 0.020*SL	0.37 + 0.028*SL	1.08 + -0.038*SL
	t_{PHL}	0.37	0.32 + 0.024*SL	0.34 + 0.017*SL	0.80 + -0.025*SL
	t_R	0.24	0.10 + 0.074*SL	0.16 + 0.051*SL	1.51 + -0.073*SL
	t_F	0.18	0.12 + 0.032*SL	0.15 + 0.022*SL	0.74 + -0.033*SL
UPDATE to DOUT	t_{PLH}	0.95	0.88 + 0.033*SL	0.90 + 0.025*SL	1.57 + -0.036*SL
	t_{PHL}	1.01	0.94 + 0.034*SL	0.98 + 0.021*SL	1.60 + -0.036*SL
	t_R	0.26	0.15 + 0.054*SL	0.15 + 0.055*SL	1.56 + -0.074*SL
	t_F	0.27	0.20 + 0.037*SL	0.23 + 0.026*SL	0.93 + -0.038*SL
SETN to DOUT	t_{PLH}	0.73	0.67 + 0.032*SL	0.68 + 0.028*SL	1.41 + -0.039*SL
	t_{PHL}	0.73	0.66 + 0.034*SL	0.68 + 0.024*SL	1.34 + -0.036*SL
	t_R	0.25	0.14 + 0.057*SL	0.15 + 0.053*SL	1.51 + -0.072*SL
	t_F	0.27	0.20 + 0.036*SL	0.22 + 0.027*SL	0.96 + -0.040*SL
TCK to DOUT	t_{PLH}	1.66	1.60 + 0.031*SL	1.61 + 0.027*SL	2.32 + -0.038*SL
	t_{PHL}	1.88	1.81 + 0.033*SL	1.84 + 0.023*SL	2.48 + -0.036*SL
	t_R	0.26	0.16 + 0.050*SL	0.16 + 0.052*SL	1.50 + -0.071*SL
	t_F	0.27	0.19 + 0.040*SL	0.23 + 0.025*SL	0.92 + -0.038*SL
ENB to DOUT	t_{PLH}	1.68	1.62 + 0.031*SL	1.63 + 0.027*SL	2.35 + -0.039*SL
	t_{PHL}	1.90	1.83 + 0.035*SL	1.86 + 0.023*SL	2.50 + -0.036*SL
	t_R	0.25	0.14 + 0.056*SL	0.15 + 0.053*SL	1.52 + -0.072*SL
	t_F	0.27	0.19 + 0.038*SL	0.23 + 0.026*SL	0.93 + -0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 11, *Group3 : 11 < SL

JTINT1

Tri-State I/O Control Scan Cell with Capture, Shift, Update and Set

Logic Symbol



Cell Data

Input Loading (SL)	
DINP	4
TDI	3
INST	3
MODE	2
SHIFT	2
UPDATE	2
SETN	1
TCK	1
ENB	1
Gate Count	
17	

Pin Description

Pin name	I/O	Description
DINP	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output
INST	O	Updated Instruction Output

Truth Table

DINP	TDI	MODE	SHIFT	UPDATE	SETN	TCK	ENB	OUTPUT
								DOUT
0	X	0	X	X	X	X	X	0
1	X	0	X	X	X	X	X	1
X	X	1	X	X	X	X	X	INST
								TDO
X	X	X	X	X	X	↑	0	TDOo
0	X	X	0	X	X	↑	1	0
1	X	X	0	X	X	↑	1	1
X	0	X	1	X	X	↑	1	0
X	1	X	1	X	X	↑	1	1
X	X	X	X	X	X	0	X	TDOo
X	X	X	X	X	X	1	X	TDOo
X	X	X	X	X	X	↓	X	TDOo
								INST
X	X	X	X	X	0	X	X	1
X	X	X	X	0	1	X	X	TDO
X	X	X	X	1	1	X	X	INSTo

NOTE: Outputs are defined in separate truth tables.

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		KG80	KGM80
Input Setup Time (TDI to TCK)	t_{SU}	0.34	0.64
Input Hold Time (TDI to TCK)	t_{HD}	0.15	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.34	0.64
Input Hold Time (TDI to ENB)	t_{HD}	0.15	0.33
Input Setup Time (DINPN to TCK)	t_{SU}	0.37	0.68
Input Hold Time (DINPN to TCK)	t_{HD}	0.15	0.33
Input Setup Time (DINPN to ENB)	t_{SU}	0.34	0.64
Input Hold Time (DINPN to ENB)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to TCK)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to ENB)	t_{HD}	0.15	0.33
Recovery Time (SETN)	t_{RC}	0.15	0.33
Input Hold Time (SETN to UPDATE)	t_{HD}	0.15	0.33

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 JTINT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.58	0.53 + 0.025*SL	0.48 + 0.045*SL	0.54 + 0.036*SL
	t_{PHL}	0.61	0.55 + 0.031*SL	0.57 + 0.025*SL	0.59 + 0.022*SL
	t_R	0.32	0.14 + 0.089*SL	0.14 + 0.089*SL	0.13 + 0.091*SL
	t_F	0.19	0.11 + 0.042*SL	0.11 + 0.040*SL	0.09 + 0.043*SL
ENB to TDO	t_{PLH}	0.58	0.50 + 0.042*SL	0.49 + 0.043*SL	0.51 + 0.040*SL
	t_{PHL}	0.60	0.55 + 0.028*SL	0.56 + 0.025*SL	0.57 + 0.024*SL
	t_R	0.32	0.15 + 0.087*SL	0.14 + 0.092*SL	0.13 + 0.093*SL
	t_F	0.19	0.11 + 0.042*SL	0.11 + 0.040*SL	0.11 + 0.042*SL
DINP to DOUT	t_{PLH}	0.29	0.25 + 0.023*SL	0.25 + 0.022*SL	0.26 + 0.020*SL
	t_{PHL}	0.35	0.31 + 0.023*SL	0.31 + 0.022*SL	0.36 + 0.015*SL
	t_R	0.19	0.12 + 0.034*SL	0.10 + 0.043*SL	0.10 + 0.043*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.021*SL	0.14 + 0.021*SL
MODE to DOUT	t_{PLH}	0.35	0.31 + 0.023*SL	0.31 + 0.021*SL	0.31 + 0.021*SL
	t_{PHL}	0.25	0.19 + 0.031*SL	0.22 + 0.018*SL	0.23 + 0.015*SL
	t_R	0.18	0.10 + 0.044*SL	0.09 + 0.045*SL	0.07 + 0.049*SL
	t_F	0.16	0.11 + 0.025*SL	0.12 + 0.022*SL	0.11 + 0.022*SL
UPDATE to DOUT	t_{PLH}	0.66	0.61 + 0.024*SL	0.62 + 0.021*SL	0.61 + 0.022*SL
	t_{PHL}	0.65	0.60 + 0.025*SL	0.62 + 0.018*SL	0.62 + 0.018*SL
	t_R	0.18	0.10 + 0.040*SL	0.09 + 0.047*SL	0.13 + 0.041*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.14 + 0.022*SL
SETN to DOUT	t_{PLH}	0.53	0.48 + 0.024*SL	0.49 + 0.022*SL	0.49 + 0.021*SL
	t_{PHL}	0.46	0.41 + 0.025*SL	0.42 + 0.018*SL	0.44 + 0.015*SL
	t_R	0.18	0.11 + 0.035*SL	0.09 + 0.043*SL	0.08 + 0.046*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.022*SL	0.13 + 0.023*SL
TCK to DOUT	t_{PLH}	1.16	1.11 + 0.025*SL	1.12 + 0.021*SL	1.12 + 0.021*SL
	t_{PHL}	1.25	1.15 + 0.049*SL	1.23 + 0.018*SL	1.25 + 0.015*SL
	t_R	0.18	0.10 + 0.042*SL	0.09 + 0.046*SL	0.11 + 0.043*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
ENB to DOUT	t_{PLH}	1.15	1.10 + 0.023*SL	1.11 + 0.022*SL	1.11 + 0.021*SL
	t_{PHL}	1.25	1.20 + 0.023*SL	1.21 + 0.018*SL	1.24 + 0.015*SL
	t_R	0.19	0.10 + 0.044*SL	0.10 + 0.045*SL	0.11 + 0.043*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.022*SL	0.14 + 0.021*SL
UPDATE to INST	t_{PLH}	0.59	0.51 + 0.041*SL	0.51 + 0.041*SL	0.49 + 0.044*SL
	t_{PHL}	0.57	0.51 + 0.030*SL	0.53 + 0.025*SL	0.52 + 0.026*SL
	t_R	0.27	0.10 + 0.084*SL	0.09 + 0.090*SL	0.07 + 0.092*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.041*SL
SETN to INST	t_{PLH}	0.47	0.39 + 0.042*SL	0.39 + 0.041*SL	0.39 + 0.042*SL
	t_{PHL}	0.38	0.31 + 0.033*SL	0.33 + 0.026*SL	0.34 + 0.023*SL
	t_R	0.27	0.09 + 0.087*SL	0.07 + 0.095*SL	0.12 + 0.089*SL
	t_F	0.17	0.10 + 0.036*SL	0.10 + 0.039*SL	0.07 + 0.043*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 JTINT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to INST	t_{PLH}	1.09	1.04 + 0.025*SL	1.00 + 0.045*SL	1.05 + 0.037*SL
	t_{PHL}	1.18	1.14 + 0.018*SL	1.11 + 0.028*SL	1.16 + 0.023*SL
	t_R	0.27	0.09 + 0.090*SL	0.10 + 0.088*SL	0.08 + 0.091*SL
	t_F	0.17	0.09 + 0.042*SL	0.09 + 0.040*SL	0.07 + 0.043*SL
ENB to INST	t_{PLH}	1.09	1.01 + 0.041*SL	1.00 + 0.044*SL	1.03 + 0.040*SL
	t_{PHL}	1.18	1.12 + 0.029*SL	1.13 + 0.025*SL	1.14 + 0.023*SL
	t_R	0.27	0.09 + 0.091*SL	0.08 + 0.096*SL	0.12 + 0.090*SL
	t_F	0.17	0.09 + 0.040*SL	0.09 + 0.041*SL	0.07 + 0.043*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

JTINT1

Tri-State I/O Control Scan Cell with Capture, Shift, Update and Set

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 JTINT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.83	0.69 + 0.066*SL	0.75 + 0.047*SL	0.71 + 0.050*SL
	t_{PHL}	0.84	0.78 + 0.031*SL	0.79 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.43	0.22 + 0.106*SL	0.22 + 0.108*SL	0.19 + 0.110*SL
	t_F	0.24	0.15 + 0.041*SL	0.15 + 0.042*SL	0.15 + 0.042*SL
ENB to TDO	t_{PLH}	0.81	0.74 + 0.034*SL	0.70 + 0.049*SL	0.65 + 0.054*SL
	t_{PHL}	0.86	0.81 + 0.023*SL	0.80 + 0.027*SL	0.84 + 0.023*SL
	t_R	0.43	0.22 + 0.106*SL	0.22 + 0.109*SL	0.20 + 0.110*SL
	t_F	0.24	0.15 + 0.044*SL	0.16 + 0.041*SL	0.15 + 0.042*SL
DINP to DOUT	t_{PLH}	0.37	0.30 + 0.034*SL	0.33 + 0.025*SL	0.33 + 0.025*SL
	t_{PHL}	0.49	0.45 + 0.019*SL	0.44 + 0.023*SL	0.55 + 0.013*SL
	t_R	0.26	0.13 + 0.063*SL	0.17 + 0.050*SL	0.14 + 0.053*SL
	t_F	0.23	0.16 + 0.034*SL	0.19 + 0.023*SL	0.21 + 0.022*SL
MODE to DOUT	t_{PLH}	0.44	0.38 + 0.031*SL	0.39 + 0.026*SL	0.41 + 0.025*SL
	t_{PHL}	0.36	0.31 + 0.027*SL	0.34 + 0.017*SL	0.33 + 0.018*SL
	t_R	0.25	0.13 + 0.060*SL	0.15 + 0.051*SL	0.12 + 0.054*SL
	t_F	0.20	0.14 + 0.032*SL	0.15 + 0.027*SL	0.21 + 0.022*SL
UPDATE to DOUT	t_{PLH}	0.90	0.84 + 0.032*SL	0.86 + 0.025*SL	0.87 + 0.024*SL
	t_{PHL}	0.93	0.87 + 0.030*SL	0.90 + 0.021*SL	0.96 + 0.015*SL
	t_R	0.29	0.14 + 0.072*SL	0.21 + 0.045*SL	0.07 + 0.059*SL
	t_F	0.23	0.17 + 0.032*SL	0.19 + 0.024*SL	0.21 + 0.023*SL
SETN to DOUT	t_{PLH}	0.70	0.66 + 0.020*SL	0.63 + 0.029*SL	0.68 + 0.025*SL
	t_{PHL}	0.66	0.60 + 0.031*SL	0.63 + 0.021*SL	0.68 + 0.016*SL
	t_R	0.27	0.10 + 0.081*SL	0.20 + 0.047*SL	0.14 + 0.053*SL
	t_F	0.23	0.17 + 0.031*SL	0.19 + 0.024*SL	0.21 + 0.022*SL
TCK to DOUT	t_{PLH}	1.61	1.55 + 0.029*SL	1.56 + 0.026*SL	1.57 + 0.025*SL
	t_{PHL}	1.82	1.77 + 0.029*SL	1.79 + 0.020*SL	1.84 + 0.016*SL
	t_R	0.27	0.11 + 0.079*SL	0.19 + 0.048*SL	0.15 + 0.052*SL
	t_F	0.24	0.17 + 0.035*SL	0.20 + 0.023*SL	0.19 + 0.024*SL
ENB to DOUT	t_{PLH}	1.64	1.58 + 0.031*SL	1.59 + 0.026*SL	1.60 + 0.025*SL
	t_{PHL}	1.84	1.78 + 0.029*SL	1.80 + 0.020*SL	1.86 + 0.015*SL
	t_R	0.27	0.11 + 0.080*SL	0.19 + 0.048*SL	0.15 + 0.051*SL
	t_F	0.23	0.17 + 0.034*SL	0.20 + 0.023*SL	0.20 + 0.023*SL
UPDATE to INST	t_{PLH}	0.81	0.70 + 0.051*SL	0.71 + 0.050*SL	0.68 + 0.052*SL
	t_{PHL}	0.80	0.73 + 0.034*SL	0.75 + 0.026*SL	0.78 + 0.024*SL
	t_R	0.36	0.13 + 0.113*SL	0.14 + 0.110*SL	0.17 + 0.107*SL
	t_F	0.20	0.11 + 0.044*SL	0.12 + 0.042*SL	0.12 + 0.042*SL
SETN to INST	t_{PLH}	0.63	0.53 + 0.051*SL	0.54 + 0.050*SL	0.54 + 0.050*SL
	t_{PHL}	0.52	0.42 + 0.050*SL	0.49 + 0.023*SL	0.48 + 0.024*SL
	t_R	0.38	0.11 + 0.132*SL	0.19 + 0.105*SL	0.16 + 0.108*SL
	t_F	0.21	0.13 + 0.039*SL	0.12 + 0.043*SL	0.12 + 0.043*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 JTINT1

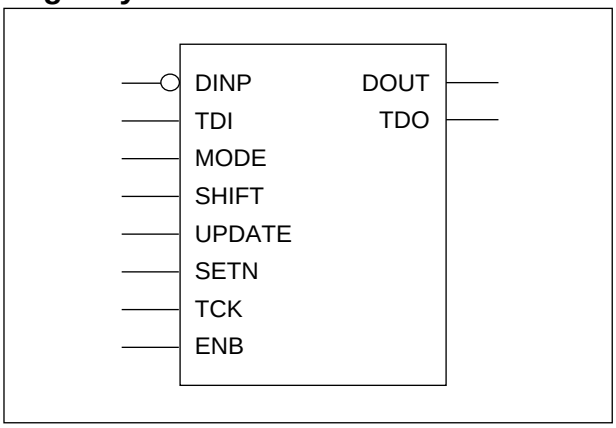
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to INST	t_{PLH}	1.57	1.44 + 0.065*SL	1.49 + 0.047*SL	1.46 + 0.050*SL
	t_{PHL}	1.69	1.63 + 0.033*SL	1.65 + 0.026*SL	1.67 + 0.024*SL
	t_R	0.37	0.12 + 0.122*SL	0.16 + 0.108*SL	0.18 + 0.107*SL
	t_F	0.21	0.11 + 0.048*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
ENB to INST	t_{PLH}	1.56	1.49 + 0.034*SL	1.45 + 0.049*SL	1.39 + 0.055*SL
	t_{PHL}	1.71	1.66 + 0.025*SL	1.65 + 0.028*SL	1.70 + 0.024*SL
	t_R	0.36	0.15 + 0.103*SL	0.14 + 0.110*SL	0.16 + 0.108*SL
	t_F	0.21	0.11 + 0.048*SL	0.13 + 0.042*SL	0.12 + 0.043*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

JTOUT1

Output Scan Cell with Capture, Shift, Update and Set

Logic Symbol



Cell Data

Input Loading (SL)	
DINP	4
TDI	3
MODE	2
SHIFT	2
UPDATE	2
SETN	1
TCK	1
ENB	1
Gate Count	
15	

Pin Description

Pin name	I/O	Description
DINP	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output

Truth Table

DINP	TDI	MODE	SHIFT	UPDATE	SETN	TCK	ENB	OUTPUT
								DOUT
0	X	0	X	X	X	X	X	0
1	X	0	X	X	X	X	X	1
X	X	1	X	X	X	X	X	LatchQ
								TDO
X	X	X	X	X	X	↑	0	TDOo
0	X	X	0	X	X	↑	1	0
1	X	X	0	X	X	↑	1	1
X	0	X	1	X	X	↑	1	0
X	1	X	1	X	X	↑	1	1
X	X	X	X	X	X	0	X	TDOo
X	X	X	X	X	X	1	X	TDOo
X	X	X	X	X	X	↓	X	TDOo
								LatchQ
X	X	X	X	X	0	X	X	1
X	X	X	X	0	1	X	X	TDO
X	X	X	X	1	1	X	X	LatchQo

NOTE: Outputs are defined in separate truth tables. In addition, an internal state known as “LatchQ” is defined as the output of the latch in the logic diagram.

Timing Requirements

(Typical process, 25°C, 5V, 3.3V)

Parameter	Symbol	Value (ns)	
		KG80	KGM80
Input Setup Time (TDI to TCK)	t_{SU}	0.34	0.64
Input Hold Time (TDI to TCK)	t_{HD}	0.15	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.34	0.64
Input Hold Time (TDI to ENB)	t_{HD}	0.15	0.33
Input Setup Time (DINP to TCK)	t_{SU}	0.37	0.68
Input Hold Time (DINP to TCK)	t_{HD}	0.15	0.33
Input Setup Time (DINP to ENB)	t_{SU}	0.34	0.64
Input Hold Time (DINP to ENB)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to TCK)	t_{HD}	0.15	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.45	0.80
Input Hold Time (SHIFT to ENB)	t_{HD}	0.15	0.33
Recovery Time (SETN)	t_{RC}	0.15	0.33
Input Hold Time (SETN to UPDATE)	t_{HD}	0.15	0.33

JTOUT1

Output Scan Cell with Capture, Shift, Update and Set

Switching Characteristics

(Typical process, 25°C, 5V, t_R/t_F = 0.40ns, SL: Standard Load)

KG80 JTOUT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.58	0.50 + 0.043*SL	0.50 + 0.041*SL	0.49 + 0.042*SL
	t_{PHL}	0.60	0.54 + 0.030*SL	0.55 + 0.026*SL	0.57 + 0.023*SL
	t_R	0.27	0.10 + 0.088*SL	0.09 + 0.089*SL	0.06 + 0.094*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
ENB to TDO	t_{PLH}	0.57	0.47 + 0.049*SL	0.49 + 0.042*SL	0.49 + 0.042*SL
	t_{PHL}	0.59	0.53 + 0.031*SL	0.54 + 0.026*SL	0.56 + 0.023*SL
	t_R	0.27	0.10 + 0.086*SL	0.09 + 0.090*SL	0.07 + 0.093*SL
	t_F	0.17	0.09 + 0.041*SL	0.09 + 0.040*SL	0.08 + 0.042*SL
DINP to DOUT	t_{PLH}	0.30	0.25 + 0.024*SL	0.25 + 0.022*SL	0.26 + 0.020*SL
	t_{PHL}	0.35	0.30 + 0.023*SL	0.31 + 0.018*SL	0.32 + 0.018*SL
	t_R	0.19	0.11 + 0.037*SL	0.10 + 0.043*SL	0.07 + 0.047*SL
	t_F	0.18	0.13 + 0.025*SL	0.14 + 0.022*SL	0.15 + 0.020*SL
MODE to DOUT	t_{PLH}	0.34	0.31 + 0.015*SL	0.29 + 0.024*SL	0.31 + 0.021*SL
	t_{PHL}	0.25	0.21 + 0.020*SL	0.22 + 0.015*SL	0.20 + 0.018*SL
	t_R	0.26	0.04 + 0.110*SL	0.25 + 0.022*SL	0.05 + 0.051*SL
	t_F	0.16	0.11 + 0.022*SL	0.11 + 0.024*SL	0.13 + 0.021*SL
UPDATE to DOUT	t_{PLH}	0.64	0.59 + 0.024*SL	0.60 + 0.022*SL	0.61 + 0.021*SL
	t_{PHL}	0.64	0.60 + 0.023*SL	0.60 + 0.021*SL	0.65 + 0.013*SL
	t_R	0.21	0.08 + 0.067*SL	0.15 + 0.035*SL	0.09 + 0.043*SL
	t_F	0.18	0.12 + 0.028*SL	0.14 + 0.022*SL	0.14 + 0.021*SL
SETN to DOUT	t_{PLH}	0.51	0.48 + 0.012*SL	0.45 + 0.026*SL	0.49 + 0.020*SL
	t_{PHL}	0.45	0.40 + 0.023*SL	0.41 + 0.018*SL	0.43 + 0.015*SL
	t_R	0.19	0.10 + 0.043*SL	0.05 + 0.064*SL	0.35 + 0.022*SL
	t_F	0.18	0.13 + 0.024*SL	0.14 + 0.023*SL	0.15 + 0.021*SL
TCK to DOUT	t_{PLH}	1.16	1.11 + 0.025*SL	1.12 + 0.021*SL	1.11 + 0.021*SL
	t_{PHL}	1.25	1.20 + 0.025*SL	1.22 + 0.018*SL	1.24 + 0.015*SL
	t_R	0.18	0.10 + 0.042*SL	0.09 + 0.046*SL	0.09 + 0.046*SL
	t_F	0.18	0.14 + 0.022*SL	0.14 + 0.023*SL	0.16 + 0.020*SL
ENB to DOUT	t_{PLH}	1.14	1.08 + 0.031*SL	1.10 + 0.022*SL	1.11 + 0.021*SL
	t_{PHL}	1.24	1.20 + 0.023*SL	1.21 + 0.018*SL	1.23 + 0.015*SL
	t_R	0.18	0.10 + 0.042*SL	0.09 + 0.044*SL	0.07 + 0.047*SL
	t_F	0.18	0.13 + 0.026*SL	0.14 + 0.023*SL	0.16 + 0.019*SL

*Group1 : SL < 2, *Group2 : 2 ≦ SL ≦ 7, *Group3 : 7 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

KGM80 JTOUT1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.78	0.68 + 0.051*SL	0.68 + 0.050*SL	0.68 + 0.050*SL
	t_{PHL}	0.81	0.74 + 0.035*SL	0.77 + 0.026*SL	0.80 + 0.023*SL
	t_R	0.36	0.15 + 0.104*SL	0.13 + 0.108*SL	0.11 + 0.110*SL
	t_F	0.21	0.13 + 0.040*SL	0.12 + 0.042*SL	0.13 + 0.042*SL
ENB to TDO	t_{PLH}	0.80	0.70 + 0.051*SL	0.70 + 0.050*SL	0.71 + 0.050*SL
	t_{PHL}	0.83	0.76 + 0.034*SL	0.78 + 0.026*SL	0.81 + 0.023*SL
	t_R	0.35	0.15 + 0.104*SL	0.13 + 0.108*SL	0.12 + 0.109*SL
	t_F	0.21	0.12 + 0.046*SL	0.13 + 0.041*SL	0.12 + 0.042*SL
DINP to DOUT	t_{PLH}	0.37	0.31 + 0.029*SL	0.32 + 0.026*SL	0.33 + 0.025*SL
	t_{PHL}	0.49	0.46 + 0.015*SL	0.43 + 0.023*SL	0.55 + 0.012*SL
	t_R	0.24	0.14 + 0.050*SL	0.14 + 0.052*SL	0.13 + 0.053*SL
	t_F	0.23	0.16 + 0.036*SL	0.19 + 0.024*SL	0.23 + 0.020*SL
MODE to DOUT	t_{PLH}	0.45	0.39 + 0.032*SL	0.40 + 0.027*SL	0.41 + 0.026*SL
	t_{PHL}	0.36	0.30 + 0.028*SL	0.32 + 0.021*SL	0.42 + 0.012*SL
	t_R	0.28	0.13 + 0.073*SL	0.16 + 0.062*SL	0.29 + 0.051*SL
	t_F	0.20	0.14 + 0.032*SL	0.15 + 0.026*SL	0.20 + 0.022*SL
UPDATE to DOUT	t_{PLH}	0.88	0.84 + 0.022*SL	0.85 + 0.016*SL	0.83 + 0.018*SL
	t_{PHL}	0.92	0.89 + 0.012*SL	0.88 + 0.015*SL	0.93 + 0.011*SL
	t_R	0.22	0.15 + 0.037*SL	0.14 + 0.039*SL	0.14 + 0.039*SL
	t_F	0.23	0.19 + 0.020*SL	0.19 + 0.019*SL	0.24 + 0.014*SL
SETN to DOUT	t_{PLH}	0.69	0.63 + 0.031*SL	0.64 + 0.027*SL	0.68 + 0.024*SL
	t_{PHL}	0.65	0.59 + 0.030*SL	0.62 + 0.021*SL	0.67 + 0.016*SL
	t_R	0.28	0.15 + 0.068*SL	0.21 + 0.047*SL	0.13 + 0.053*SL
	t_F	0.23	0.17 + 0.033*SL	0.19 + 0.024*SL	0.22 + 0.022*SL
TCK to DOUT	t_{PLH}	1.61	1.55 + 0.030*SL	1.57 + 0.026*SL	1.58 + 0.025*SL
	t_{PHL}	1.81	1.75 + 0.029*SL	1.77 + 0.021*SL	1.83 + 0.015*SL
	t_R	0.24	0.13 + 0.052*SL	0.12 + 0.056*SL	0.19 + 0.050*SL
	t_F	0.23	0.17 + 0.033*SL	0.19 + 0.025*SL	0.21 + 0.023*SL
ENB to DOUT	t_{PLH}	1.64	1.58 + 0.029*SL	1.59 + 0.026*SL	1.61 + 0.025*SL
	t_{PHL}	1.82	1.76 + 0.028*SL	1.78 + 0.021*SL	1.84 + 0.015*SL
	t_R	0.24	0.13 + 0.054*SL	0.13 + 0.056*SL	0.20 + 0.049*SL
	t_F	0.24	0.18 + 0.028*SL	0.19 + 0.025*SL	0.23 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 11, *Group3 : 11 < SL

JTAG TAP CONTROLLER MACROFUNCTION

TAP controller macrofunction consists of instruction register and data register scan paths, a bypass register, multiplexers and a 16-state finite state machine. The bypass register and instruction register are JTAG devices. TAP controller uses the largest available internal buffers (IVD8) to drive data register control signals.

Instruction register/decoder are external to TAP controller since the register length and instruction codes vary from one ASIC design to another. The instruction register consists of three JTINT1 macrocells. The instruction decoder is used to implement a minimum TAP configuration with a boundary scan register and an optional identification register.

TAP Controller Input Pin Description

Name	Mandatory	Description
BPSEL		Bypass select
DREGDI		Data register scan path data-in
IREGDI		Instruction register scan path data-in
TCK	•	Test clock
TDI	•	Test data input to the bypass register
TMS	•	Test mode select controlling state transitions of a finite state machine
TRSTN		Test reset input

TAP Controller Output Pin Description

Name	Mandatory	Description
DRE		Data register enable control output
IRE		Instruction register enable control output
RSTO		Reset output
SHFDR		Data register shift control output
SHFIR		Instruction register shift control output
TDO	•	Test data output
TDOE		TDO tri-state enable output
UPDATEDR		Data register update control output
UPDATEIR		Instruction register update control output

The bulleted pins (TCK, TDI, TMS and TDO) are mandatory pins associated with the IEEE P1149.1 standard test bus interface. TRSTN is an optional test reset input. It is possible to implement TAP without the test reset input indicated in the IEEE P1149.1 standard by setting TRSTN pin to high logic state. Alternatively, if a power-on reset capability is desired, TRSTN pin should be set to active low and connected to the power-on reset circuitry.

The 16 states of the finite state machine, diagrammed in the figure 9-3, also comply with the proposed IEEE P1149.1 standard. State transitions occur on the rising edge of TCK and are controlled by TMS. To ensure stable state transitions, TMS transitions occur on the falling edges of TCK. Capture, shift or update of test data take place on the next rising edge of TCK after the state transition or on each subsequent rising edge of TCK if no state transition occurs.

Figure 6-3. TAP Controller I/O Pin-Out Diagram

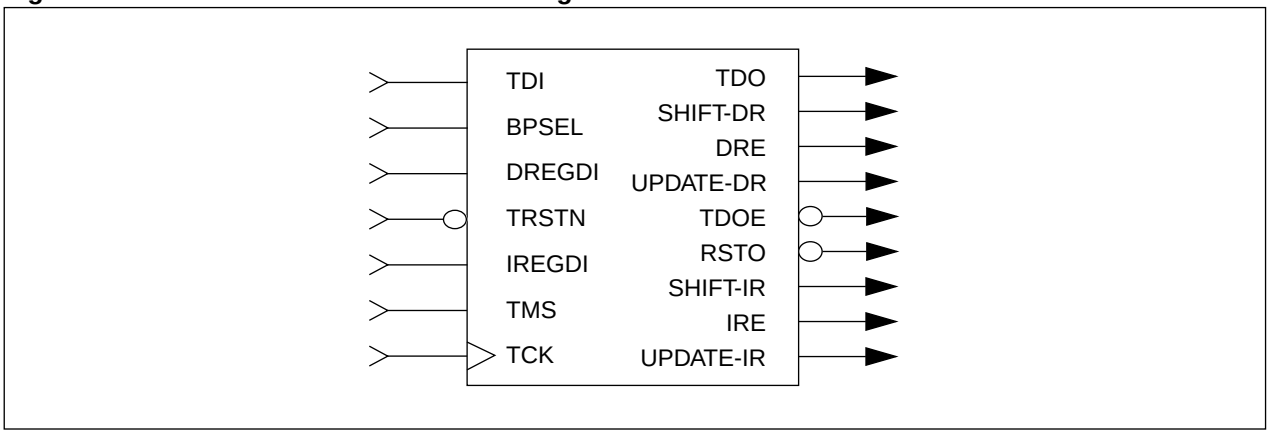
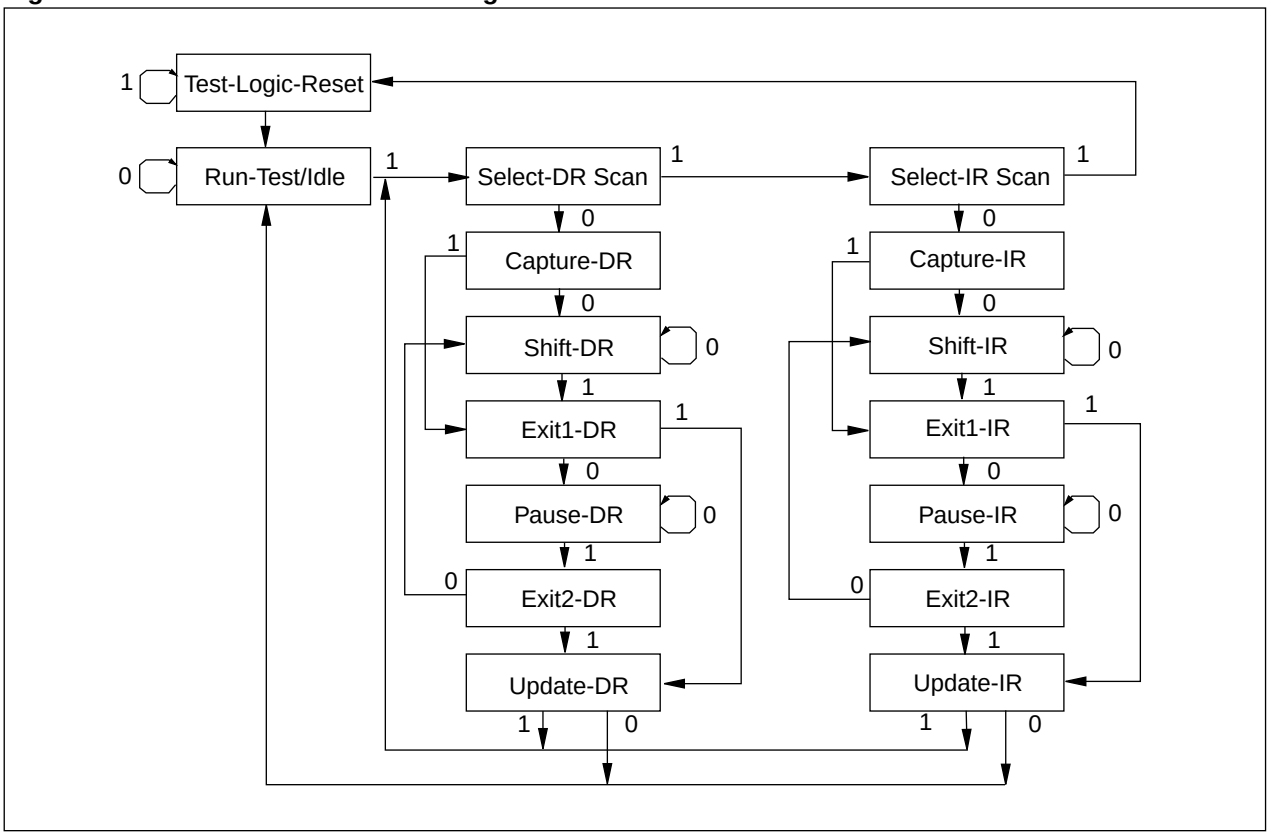


Figure 6-4. TAP Controller State Diagram



Behavior of TAP Controller States

Test-Logic-Reset

An initialization of the instruction register disables the test logic, allowing the on-chip system logic to operate normally. Irrespective of its original state, TAP controller reverts to Test-Logic-Reset when TMS is maintained high for five rising edges of TCK.

Run-Test/Idle

Idles in the state between scan operations or self-tests.

Capture-DR

Loads data parallelly into test data registers selected by the current instruction on the rising edge of TCK.

Shift-DR

Shifts data in the test data register between TDI and TDO one stage towards its serial output on each rising edge of TCK.

Pause-DR

Temporarily halts test data register shifts in the serial path between TDI and TDO.

Update-DR

Latches the data from the shift register path to the parallel output of test data registers on the falling edge of TCK.

Capture-IR

The shift-register contained in the instruction register loads a pattern of fixed logic value on the rising edge of TCK. It is possible to load design-specific data into shift-register stages that are not set to fixed values.

Shift-IR

Shifts data contained in the shift-register of the instruction register between TDI and TDO one stage towards its serial output on each rising edge of TCK.

Pause-IR

Temporarily halts shifting of the instruction register.

Update-IR

Latches the instruction shifted into the instruction register to the parallel output from the shift register path on the falling edge of TCK.

Select-DR-Scan, Select-IR-Scan, Exit1-DR, Exit2-DR, Exit1-IR, Exit2-IR

They are temporary controller states.

State Assignments for TAP Controller

Table 6-1. State Assignments

Controller State	State [3:0]	Controller State	State [3:0]
Exit2-DR	0	Exit2-IR	8
Exit1-DR	1	Exit1-IR	9
Shift-DR	2	Shift-IR	A
Pause-DR	3	Pause-IR	B
Select-IR Scan	4	Run-Test/Idle	C
Update-DR	5	Update-IR	D
Capture-DR	6	Capture-IR	E
Select-DR-Scan	7	Test-Logic-Reset	F

The bypass circuitry captures a low state during the data capture state of the finite state machine data cycle, as required by the proposed IEEE 1149.1 standard.

INSTRUCTION REGISTER/DECODER MACROFUNCTION

Instruction Register Macrofunction

The instruction register provides eight instructions in a minimum 3-bit device. These 3 bits are sufficient for operations of boundary scan cells and an instruction register, and three other operations such as the internal scan chains. Devices requiring more than eight instructions need a customer-specific design.

The instruction register allows an instruction to be shifted into the design. The instruction defines the test to be performed or the test data register to access or both. If a device identification register is present, the output register must be initialized to IDCODE instruction when TAP controller is in the Test-Logic-Reset state. Alternatively, it may be initialized to the bypass instruction. To support a fault isolation at the board-level, a constant binary ‘01’ pattern is loaded into the least significant bits of the instruction register when it is in the Capture-IR state.

Instruction Decoder Macrofunction

The instruction decoder operates with the instruction register to provide boundary scan control. Designs requiring other options need a customer-specific design.

Instruction Decoder Input Pin Description:

Name	Description
INST (2:0)	Instruction register input

Instruction Decoder Output Pin Description:

Name	Description
0_Mode	Boundary scan output mode control
I_Mode	Boundary scan input mode control

The instruction decoder has the following truth table.

INST(2)	INST(1)	INST(0)	I_Mode	0_Mode
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

IMPLEMENTATION OF IEEE P1149.1/JTAG

The following design procedures should be followed for ASIC implementation of IEEE P1149.1/JTAG using SEC boundary scan cells:

1. Allocate four (optionally five) package pins for testing.
2. Generate a bonding diagram, including provision for the corner pads that cannot be used for boundary scan I/Os.
3. Configure the top level device symbol with the same pin-out sequence as the packaged device.
4. Select appropriate boundary scan macrocells, JTBI1, JTCK, JTIN1 and JTOUT1, for the boundary-scan I/O pads. JTCK and JTIN1 must be associated with inputs; JTOUT1 with outputs and JTBI1 with bi-directional inputs and outputs.
5. ASIC clock inputs generally use JTCK macrocell, but it may be used for other critical inputs where performance considerations dominate. JTOUT1 macrocells are used for each output pin and JTBI1 macrocells are used by bi-directional pins.
6. JTAG inputs (TDI, TCK, TMS), output (TDO) and optional TRSTN are connected to TAP controller. The boundary scan register and the instruction register are connected to TDI and TCK inputs. Inputs, TDI, TMS and TRSTN should have input pull-up resistors.
7. To start the boundary scan chain sequence, connect any TDI input to JTBI1, JTCK, JTIN1, or JTOUT1 macrocells. The chain sequence proceeds to each adjacent macrocell I/O pad until terminated. TDO output of the final macrocell is connected to DREGDI input of TAP controller. Similarly, the terminal TDO output of the instruction register is connected to IREGDI of TAP controller.
8. Instruction register and data register control signals are connected to the instruction register and boundary scan registers, and INST signal lines from the instruction register are connected to the instruction decoder which supplies the control signals BPSEL, I_Mode and O_Mode for TAP controller and the boundary scan register. I_Mode is connected to JTIN1 macrocells and O_Mode is connected to JTOUT1 macrocells. I_Mode, O_Mode and MODE1 are also connected to the appropriate inputs of JTBI1 macrocells.
9. I_MODE output is connected to a IVD8 macrocell and TN inputs of the bi-directional and tri-state output buffers associated with the respective I/O pads. Other buffers may be required if there are a large number of bi-directional or tri-state pads.
10. If the design requires internal tri-state enable control signals, an additional JTINT1 macrocell is needed for each enable. Internal enable macrocells should be connected to TAP controller RSTO signal and O_MODE control line. JTIN1 macrocell is used for external tri-state enable input signals and should be connected to TAP controller RSTO signal and I_MODE control line.
11. Generate the test patterns to test JTAG portion of the design.

SYSTEM CLOCK CONSIDERATIONS

Test and system clocks must be synchronized carefully. All phases of the system clock should be gated on and off at a central point within the system. When TMS input is high, TCK can run continuously and test modes is disabled.