

256K x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 262,144 x 16 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), Access time (-5,-6 or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 256Kx16 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

• Part Identification

- KM416C254D/DL (5V, 512 Ref.)
- KM416V254D/DL (3.3V, 512 Ref.)

• Active Power Dissipation

Unit : mW

Speed	3.3V(512 Ref.)	5V(512 Ref.)
-5	-	605
-6	255	495
-7	235	440

• Refresh Cycles

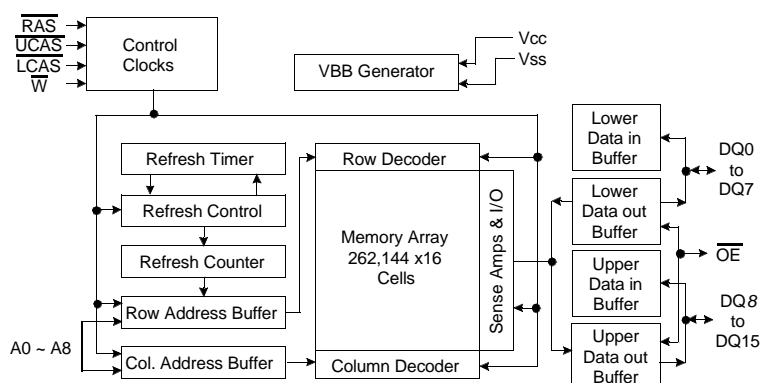
Part NO.	V _{CC}	Refresh cycle	Refresh period	
			Normal	L-ver
C254D	5V	512	8ms	128ms
V254D	3.3V			

• Performance Range

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}	Remark
-5	50ns	15ns	84ns	20ns	5V only
-6	60ns	15ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V

- Extended Data Out Mode operation
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 40-pin SOJ 400mil and 44(40)-pin TSOP(II) 400mil packages
- Triple +5V±10% power supply (5V product)
- Triple +3.3V±0.3V power supply (3.3V product)

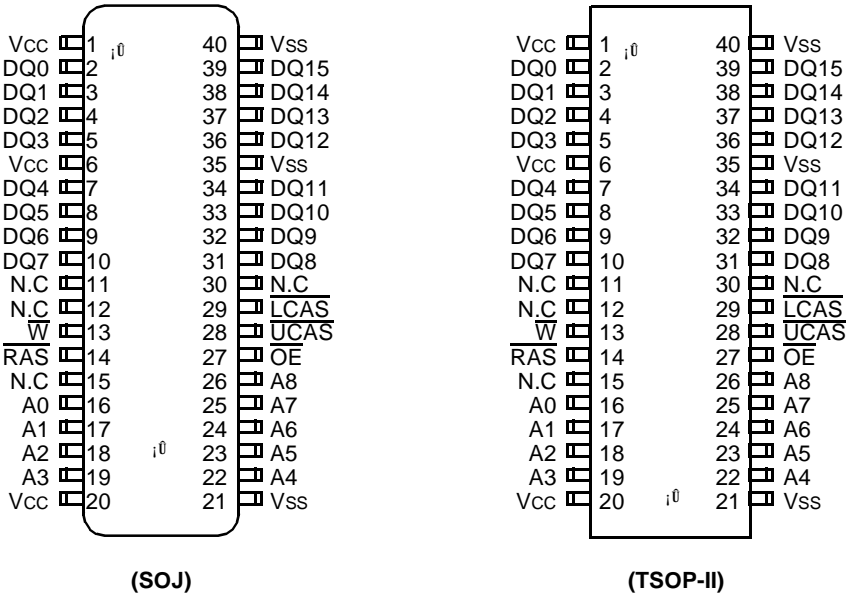
FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION (Top Views)

- KM416C/V254DJ
- KM416C/V254DT



Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 - 15	Data In/Out
Vss	Ground
\overline{RAS}	Row Address Strobe
\overline{UCAS}	Upper Column Address Strobe
\overline{LCAS}	Lower Column Address Strobe
\overline{W}	Read/Write Input
\overline{OE}	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{os}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3*1	2.4	-	V _{CC} +1.0*1	V
Input Low Voltage	V _{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Max	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.3V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			KM416V254D	KM416C254D	
I _{CC1}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
I _{CC2}	Don't care	Don't care	1	2	mA
I _{CC3}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
I _{CC4}	Don't care	-5	-	90	mA
		-6	60	80	mA
		-7	55	70	mA
I _{CC5}	Normal L	Don't care	0.5	1	mA
			100	150	uA
I _{CC6}	Don't care	-5	-	110	mA
		-6	70	90	mA
		-7	65	80	mA
I _{CC7}	L	Don't care	200	300	uA
I _{CCS}	L	Don't care	100	200	uA

I_{CC1}* : Operating Current (\overline{RAS} and \overline{UCAS} , \overline{LCAS} , Address cycling @trc=min.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$)

I_{CC3}* : \overline{RAS} -only Refresh Current ($\overline{UCAS}=\overline{LCAS}=V_{IH}$, \overline{RAS} , Address cycling @trc=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}=V_{IL}$, \overline{UCAS} or \overline{LCAS} , Address cycling @thpc=min.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : \overline{CAS} -Before- \overline{RAS} Refresh Current (\overline{RAS} and \overline{UCAS} or \overline{LCAS} cycling @trc=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})= $V_{CC}-0.2V$, Input low voltage(V_{IL})= $0.2V$, \overline{UCAS} , $\overline{LCAS}=0.2V$,

Din=Don't care, TRC=125us, TRAS=TRASmin~300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0 \sim A8=V_{CC}-0.2V$ or $0.2V$,

DQ0 ~ DQ15= $V_{CC}-0.2V$, $0.2V$ or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6} and I_{CC7}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time, thpc.

KM416C254D/DL, KM416V254D/DL

CMOS DRAM

CAPACITANCE (TA=25°C, VCC=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A8]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ15]	CDQ	-	7	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Test condition (5V device) : VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.0/0.8V

Test condition (3.3V device) : VCC=3.3V±0.3V, VIH/VIL=2.2/0.7V, VOH/VOL=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	116		138		163		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		15		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	13	3	18	ns	6,13
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		50		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	15		15		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	40		50		60		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	35	20	45	20	50	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	14
Column address hold time	tCAH	8		10		15		ns	14
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		10		10		ns	
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	8		10		15		ns	17

Note) *1 : 5V only

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 ^{*1}		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9,20
Data hold time	tDH	8		10		15		ns	9,20
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	32		32		42		ns	7,16
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	67		77		92		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	42		47		57		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	45		52		62		ns	7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		ns	18
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	19
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time (CBR counter test)	tCPT	20		20		25		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		28		35		40	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		ns	11
Hyper Page read-modify-write cycle time	tHPRWC	57		66		81		ns	11
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	tCP	8		10		10		ns	15
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	trASP	50	100K	60	100K	70	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	30		35		40		ns	
$\overline{\text{OE}}$ access time	tOEA		15		15		20	ns	3
$\overline{\text{OE}}$ to data delay	tOED	13		13		18		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	3	13	3	13	3	18	ns	6
$\overline{\text{OE}}$ command hold time	tOEH	15		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	trEZ	3	15	3	15	3	20	ns	6,13
Output buffer turn off delay from $\overline{\text{W}}$	twEZ	3	13	3	13	3	18	ns	6
$\overline{\text{W}}$ to data delay	twED	13		13		18		ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	tOCH	5		5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	tCHO	5		5		5		ns	
$\overline{\text{OE}}$ precharge time	tOEP	5		5		5		ns	
$\overline{\text{W}}$ pulse width (Hyper Page Cycle)	twPE	5		5		5		ns	
$\overline{\text{RAS}}$ pulse width (C-B-R self refresh)	trASS	100		100		100		us	12
$\overline{\text{RAS}}$ precharge time (C-B-R self refresh)	trPS	90		110		130		ns	12
$\overline{\text{CAS}}$ hold time (C-B-R self refresh)	tCHS	-50		-50		-50		ns	12

(Note) *1 : 5V only

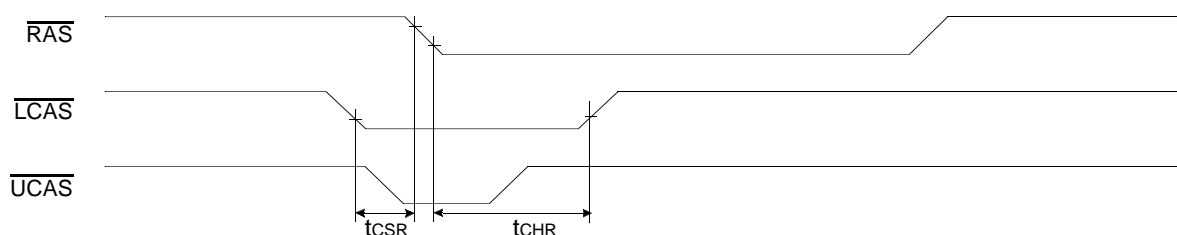
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or $\overline{\text{CBR}}$ cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il} . $V_{ih}(\text{min})$ and $V_{il}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{ih}(\text{min})$ and $V_{il}(\text{max})$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1TTL(3.3V) loads and 50pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. $t_{\text{ASC}} \geq 6\text{ns}$, Assume $t_{\text{T}} = 2.0\text{ns}$
12. 512cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).

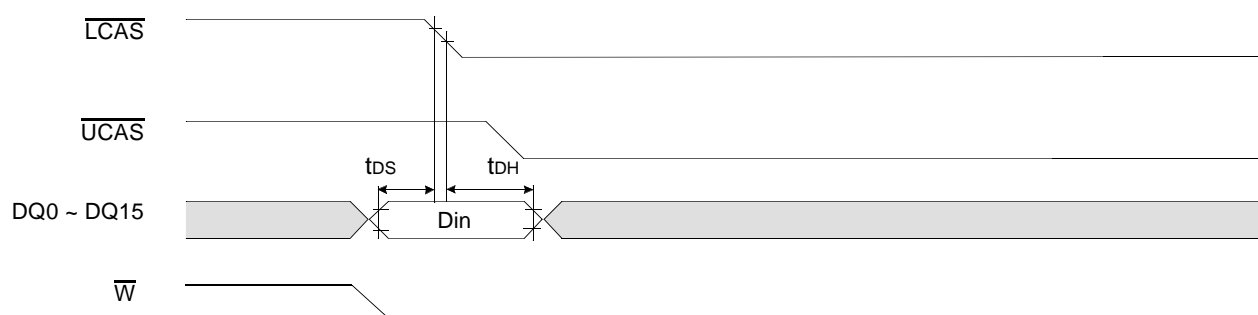
KM416C/V254D/DL Truth Table

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ0 - DQ7	DQ8-DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

13. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.
14. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ rising edge.
15. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
16. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word red-modify-write cycle.
17. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.
18. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
19. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.

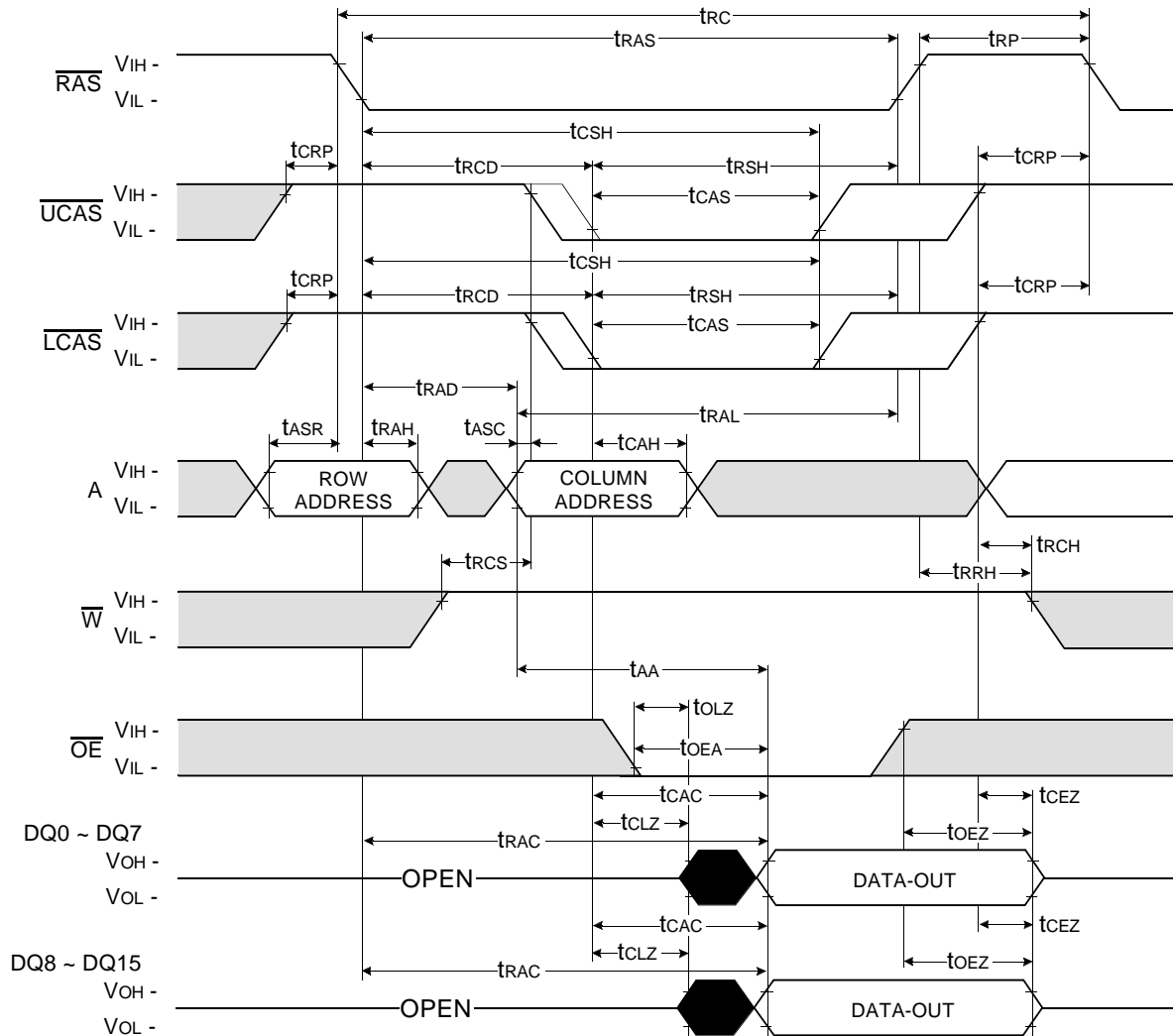


20. t_{DS} , t_{DH} are specified for the earlier $\overline{\text{CAS}}$ falling low.



WORD READ CYCLE

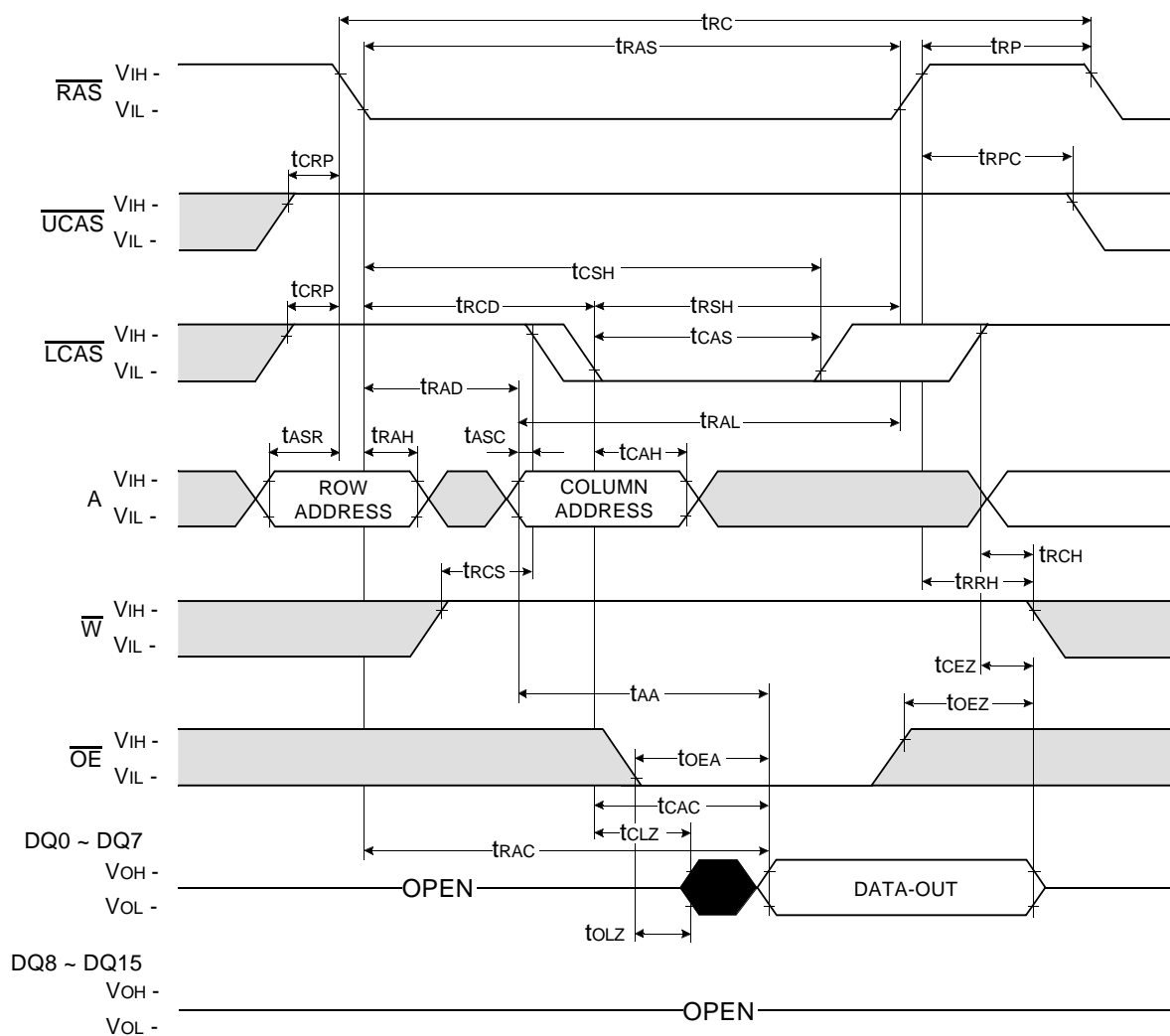
NOTE : DIN = OPEN



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LOWER BYTE READ CYCLE

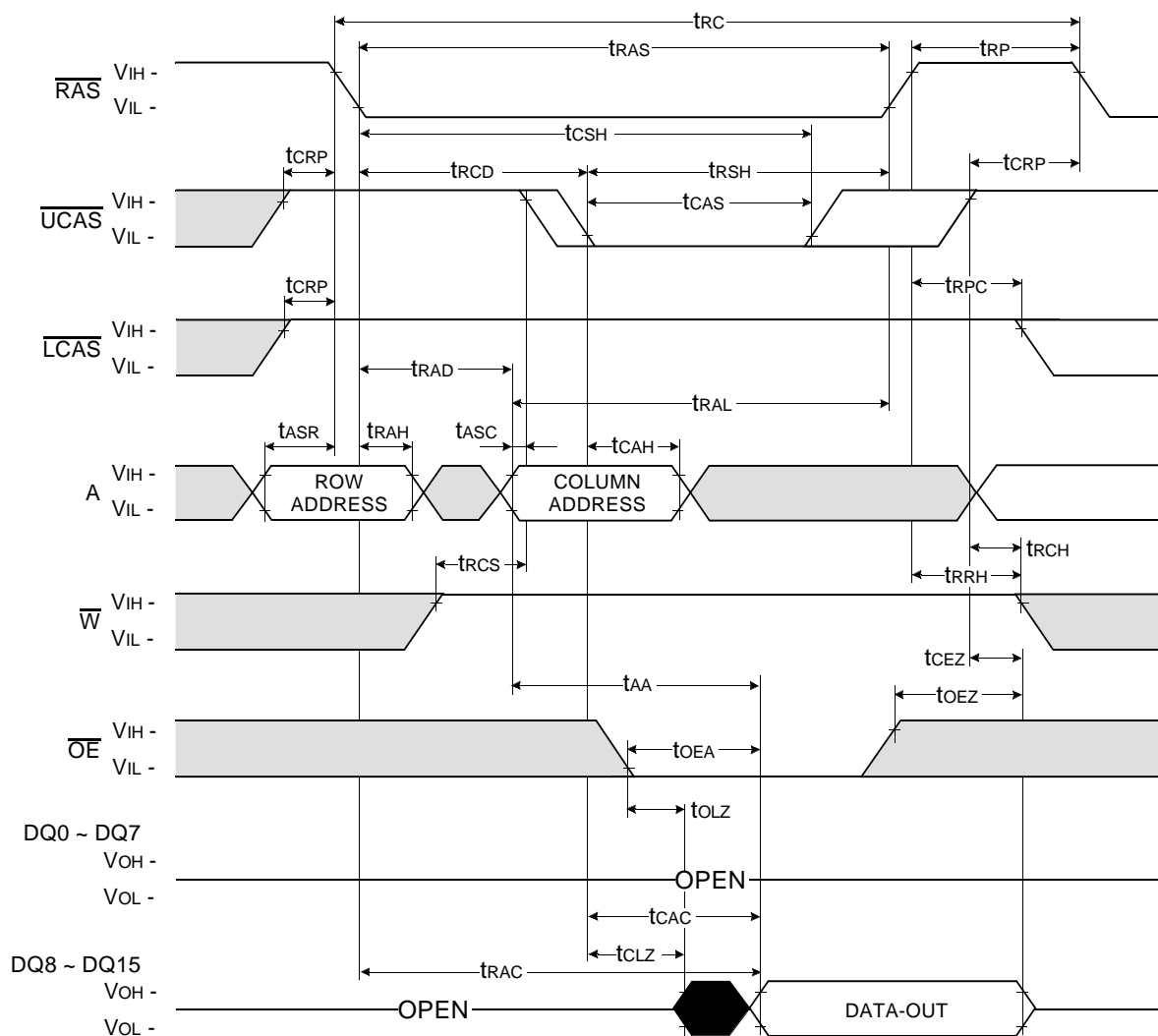
NOTE : DIN = OPEN

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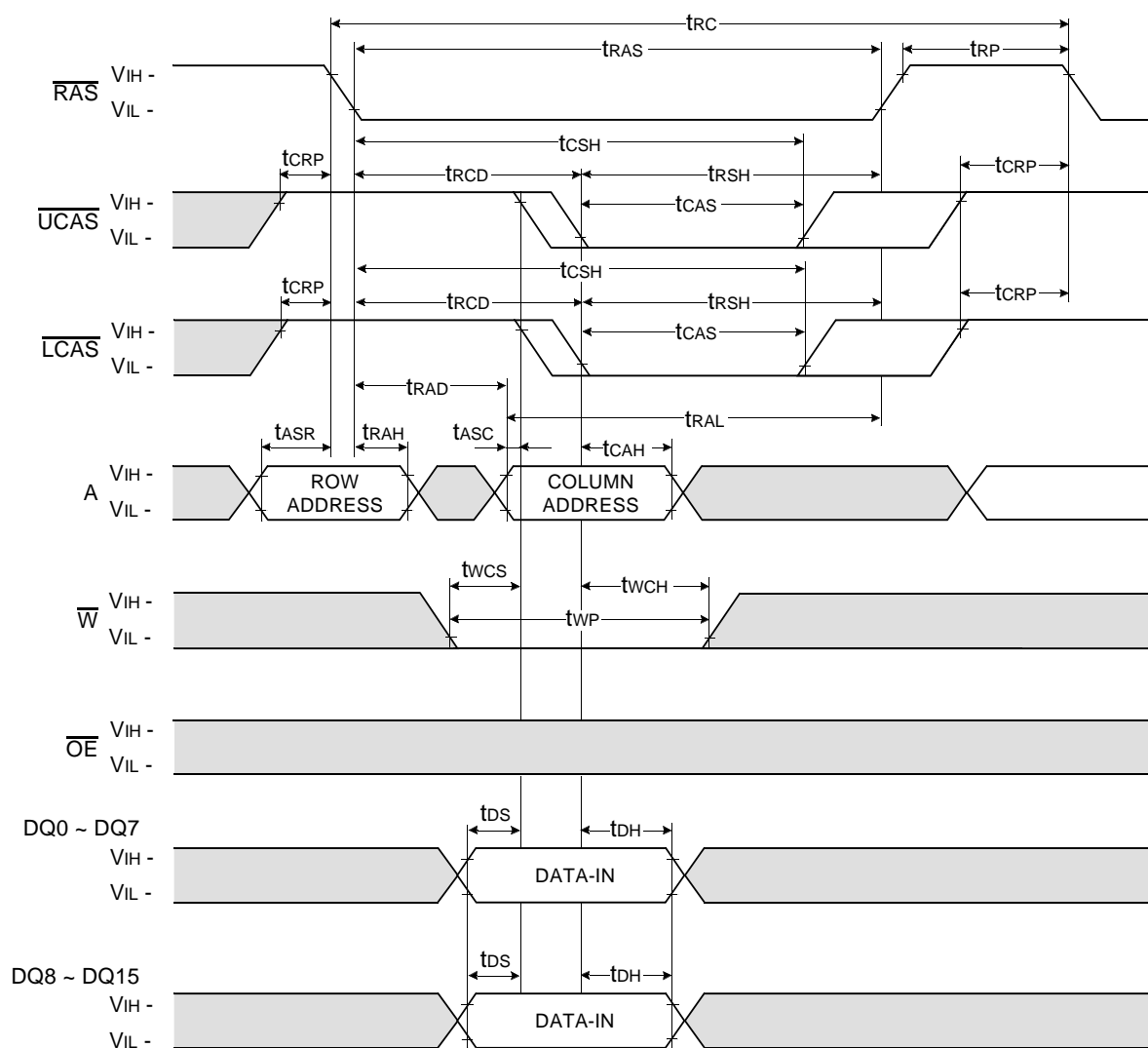
UPPER BYTE READ CYCLE

NOTE : DIN = OPEN



WORD WRITE CYCLE (EARLY WRITE)

NOTE : DoUT = OPEN

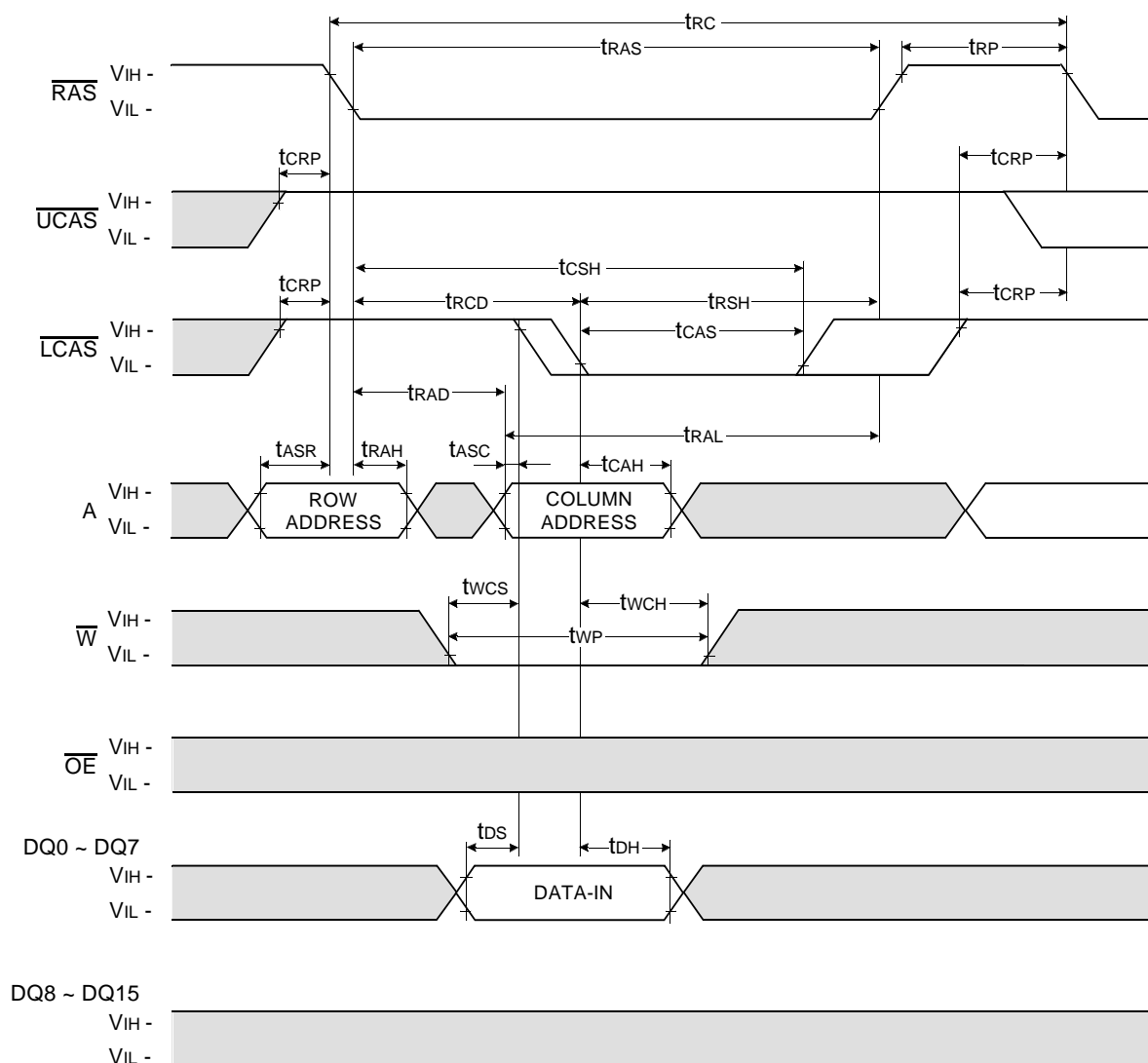




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LOWER BYTE WRITE CYCLE (EARLY WRITE)

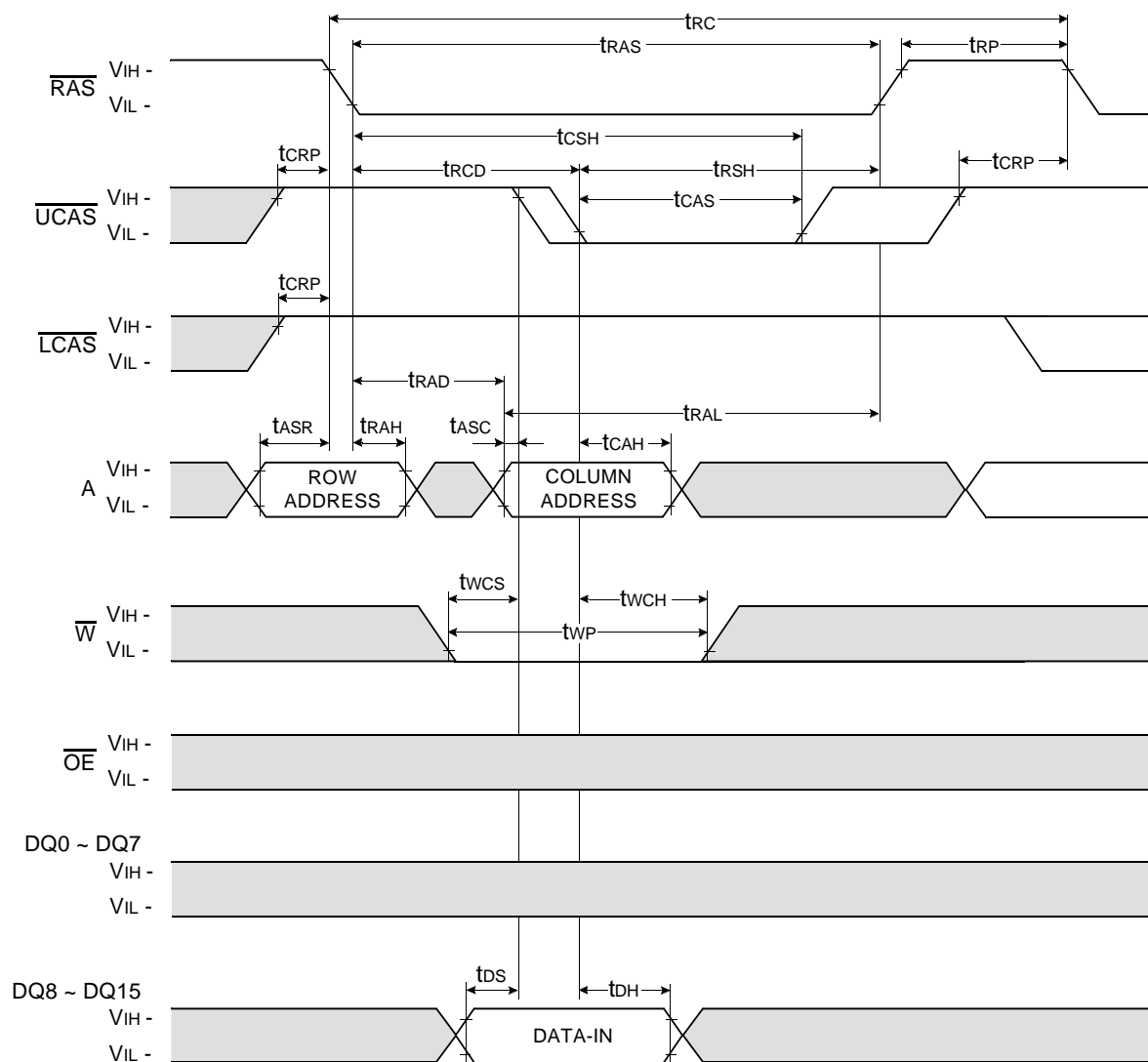
NOTE : DOUT = OPEN



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UPPER BYTE WRITE CYCLE (EARLY WRITE)

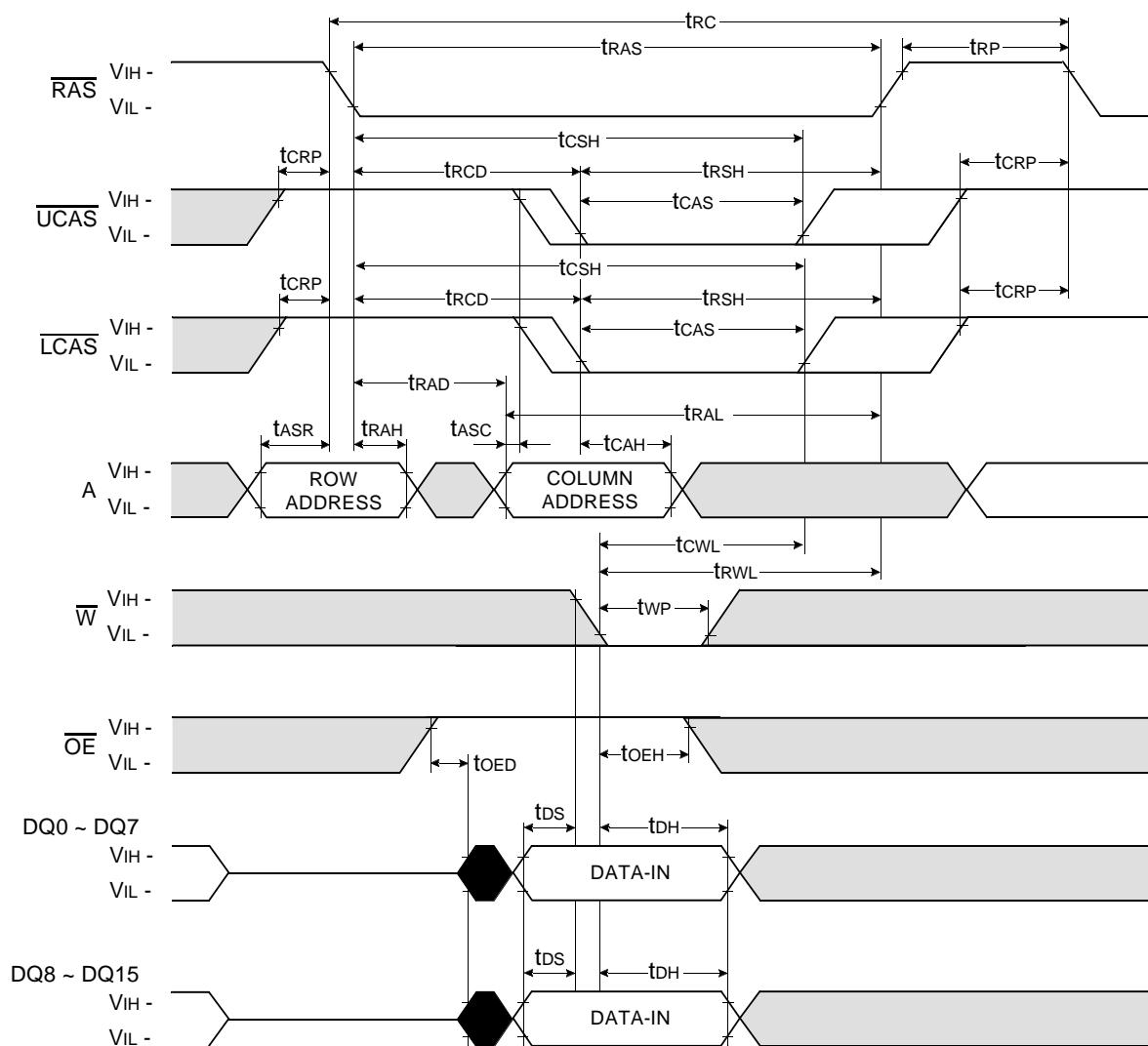
NOTE : DOUT = OPEN



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WORD WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

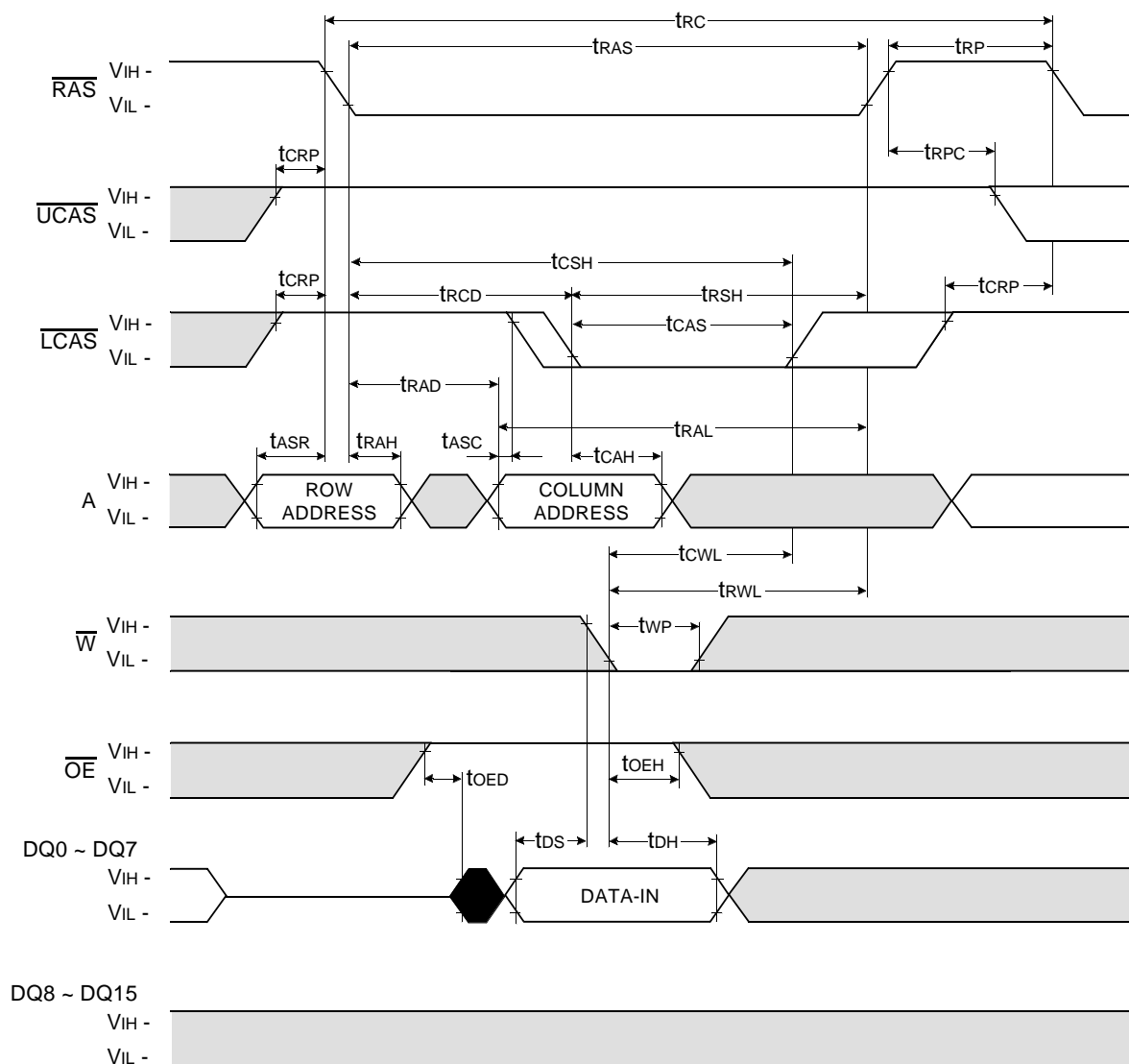
NOTE : DOUT = OPEN



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LOWER BYTE WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

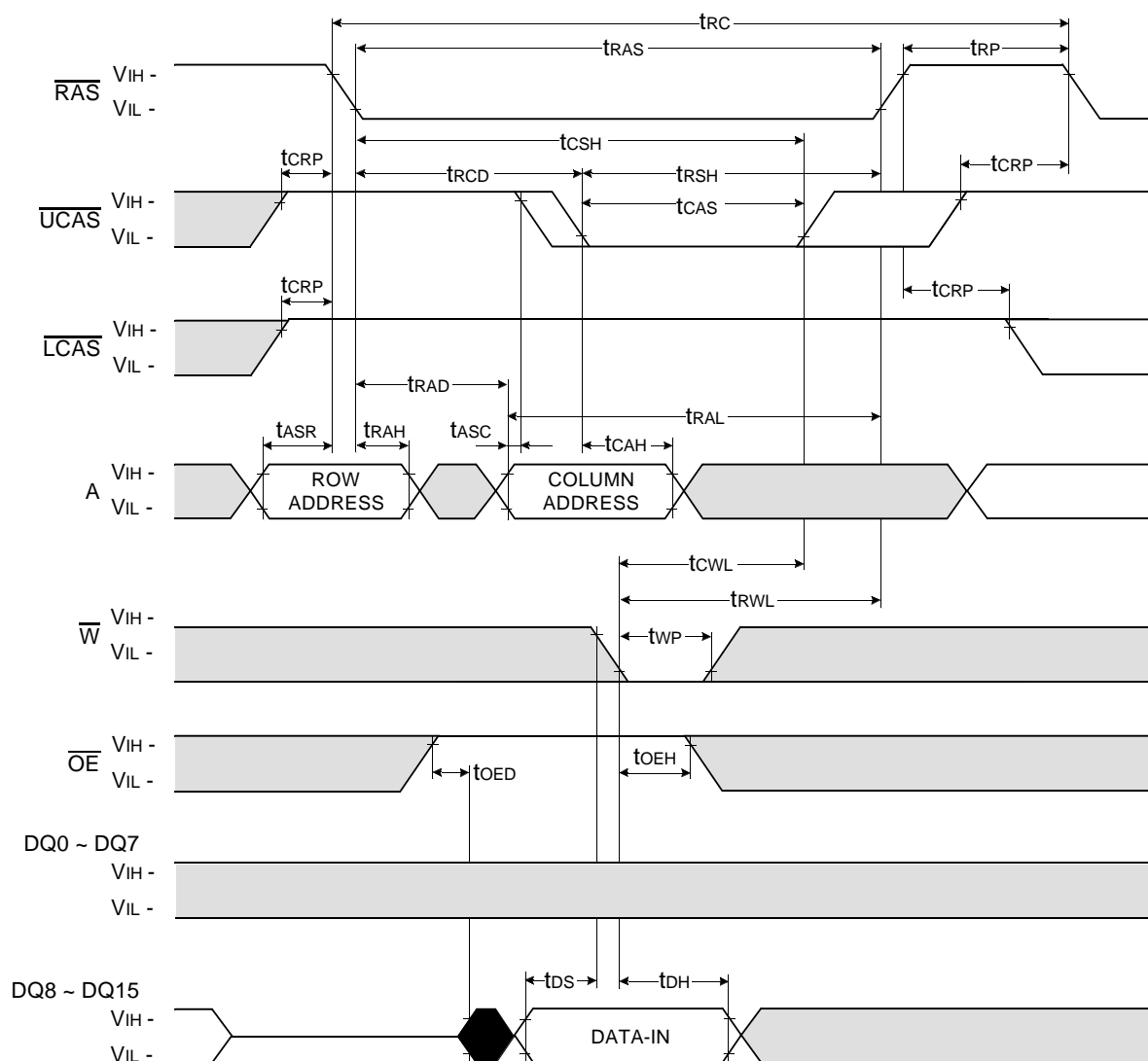
NOTE : DOUT = OPEN

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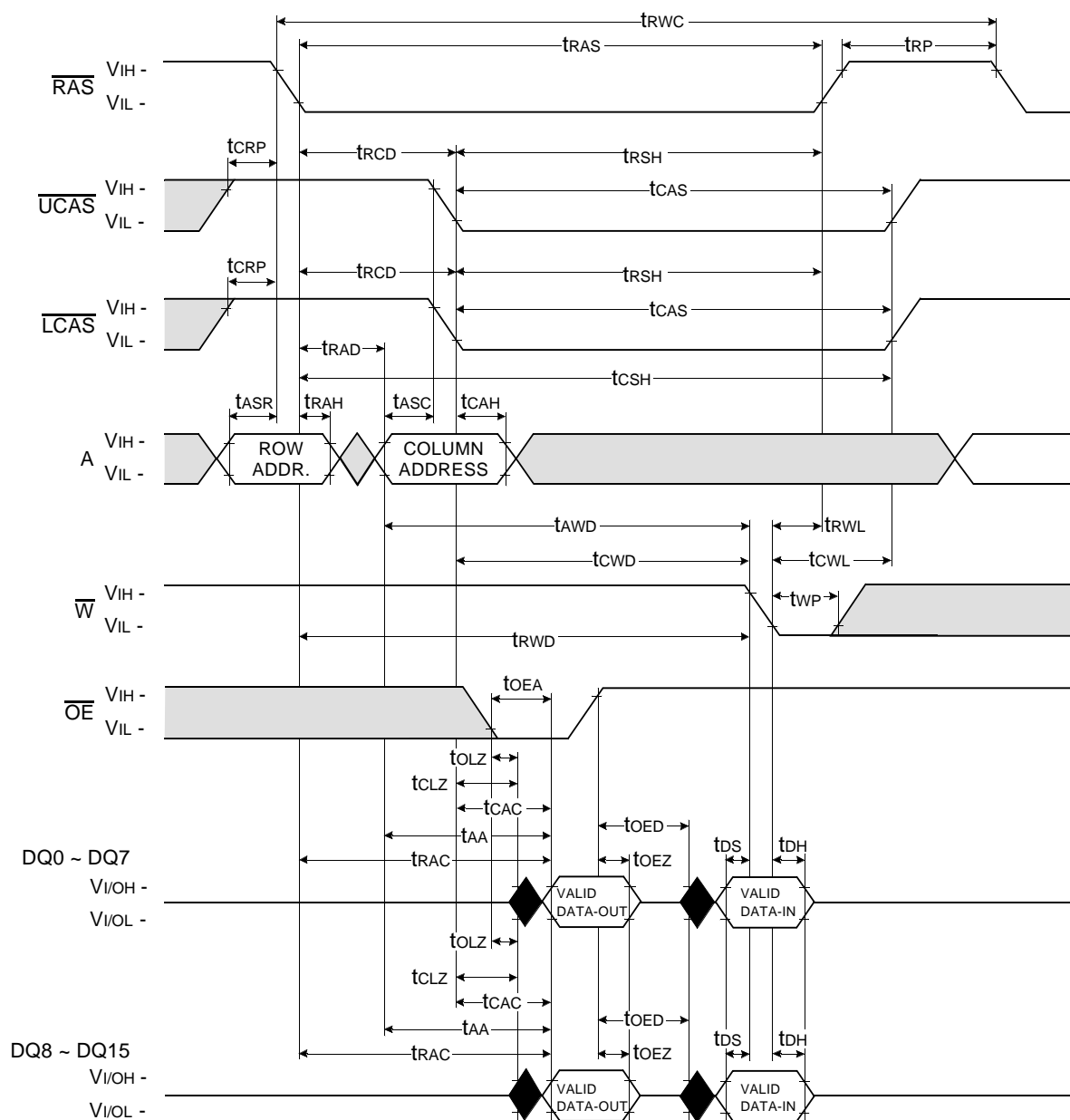
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN

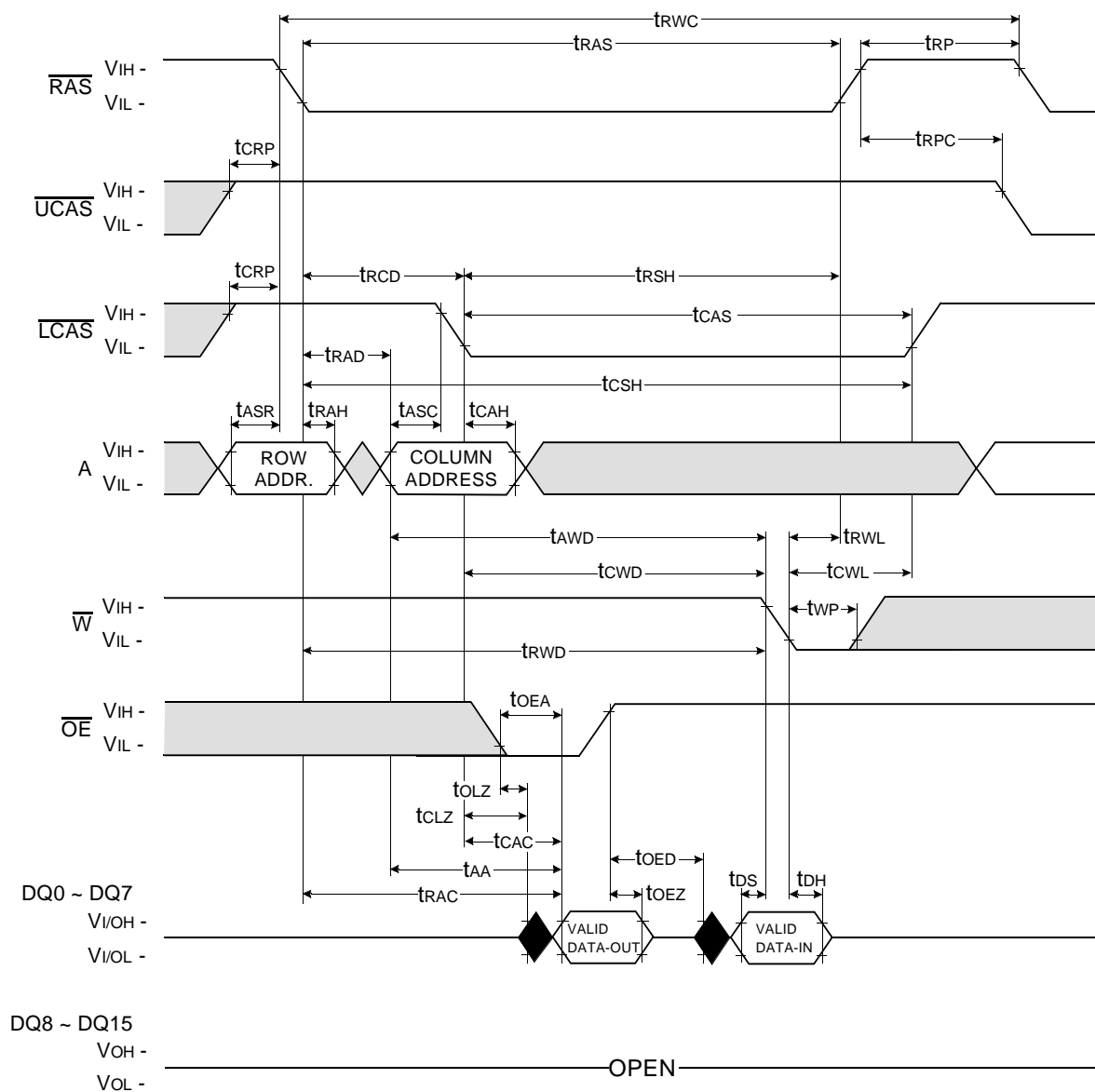


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WORD READ - MODIFY - WRITE CYCLE



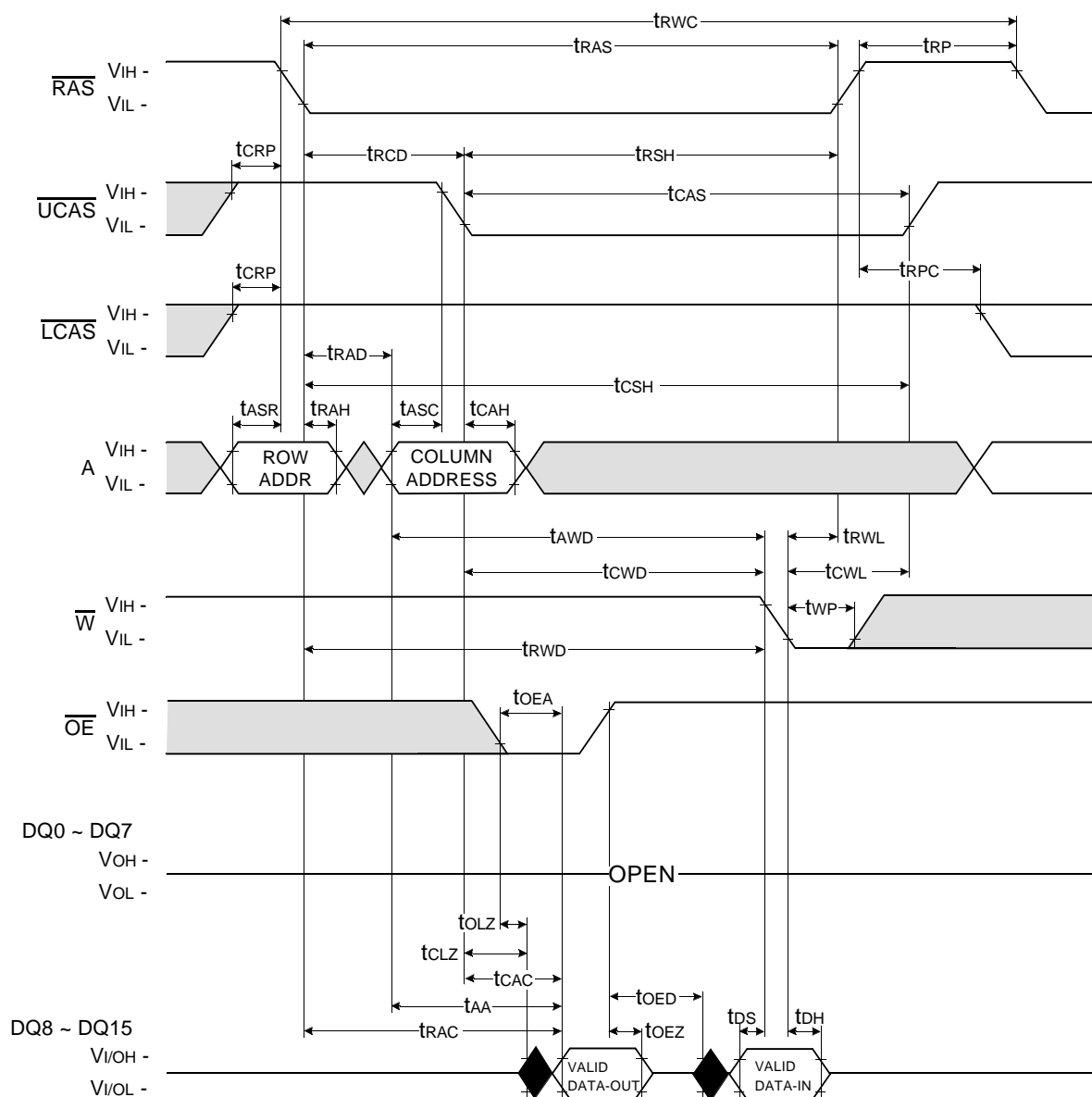
LOWER-BYTE READ - MODIFY - WRITE CYCLE



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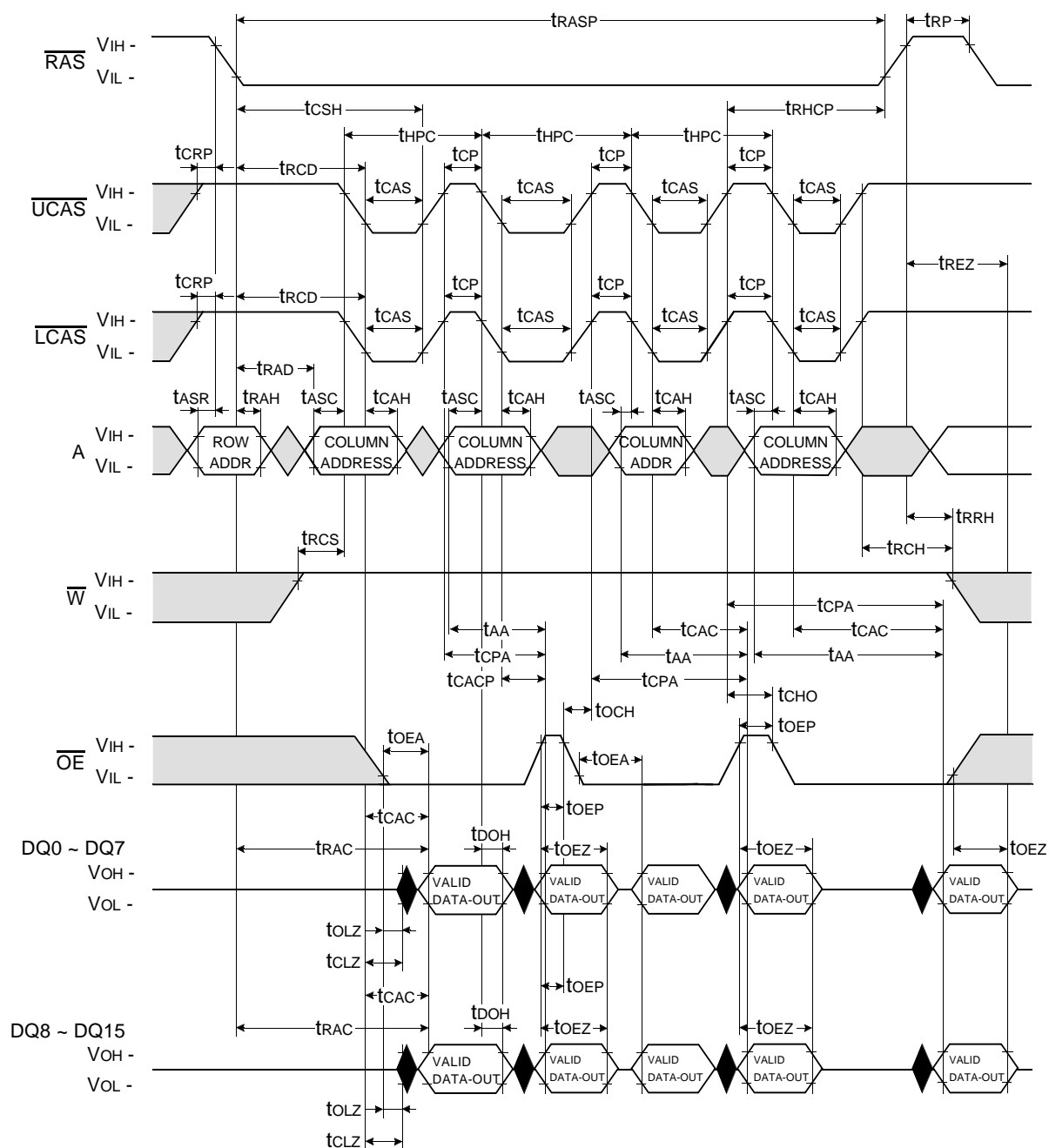
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UPPER-BYTE READ - MODIFY - WRITE CYCLE



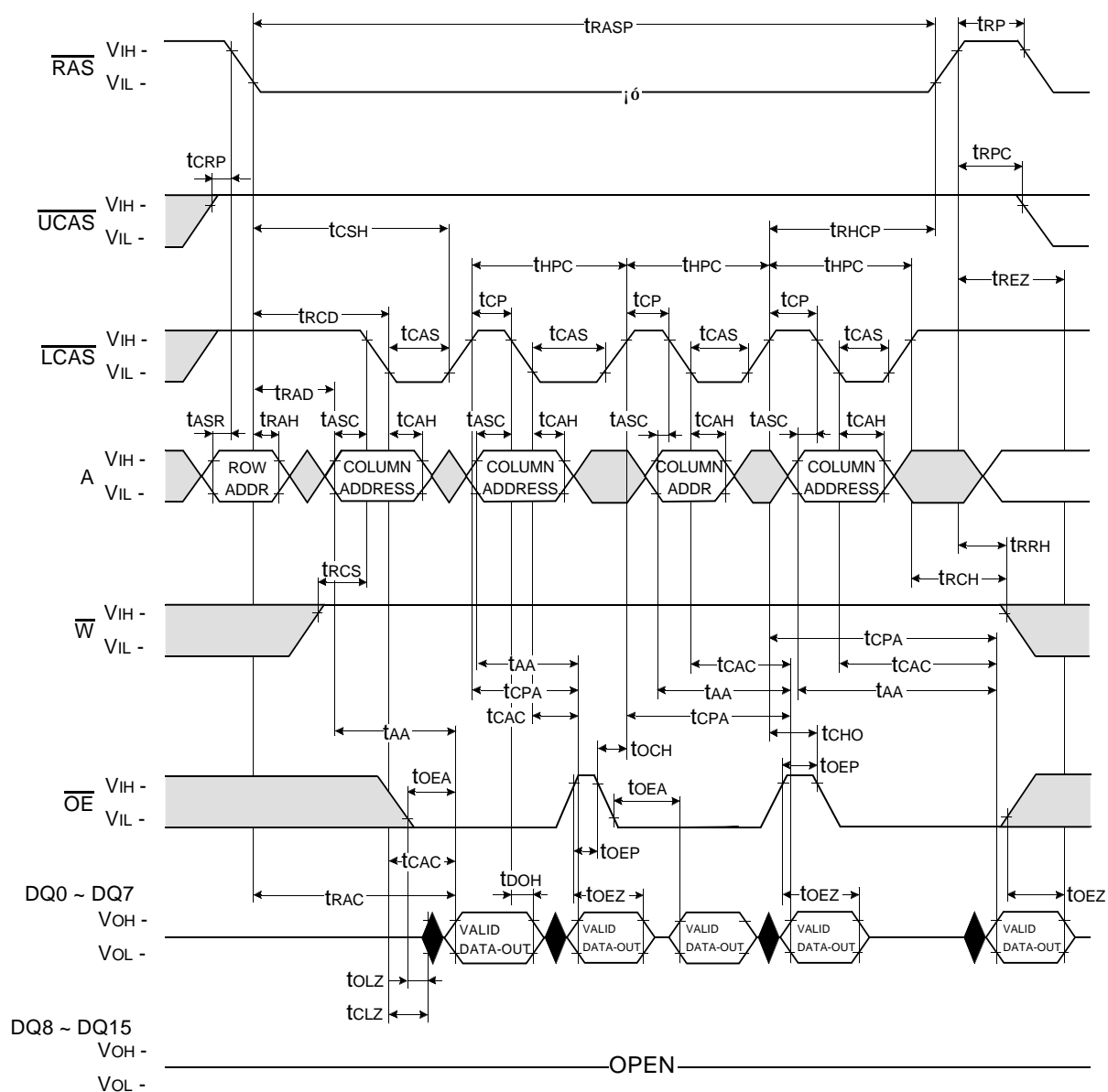
Don't care
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HYPER PAGE MODE WORD READ CYCLE


☐ Don't care

■ Undefined

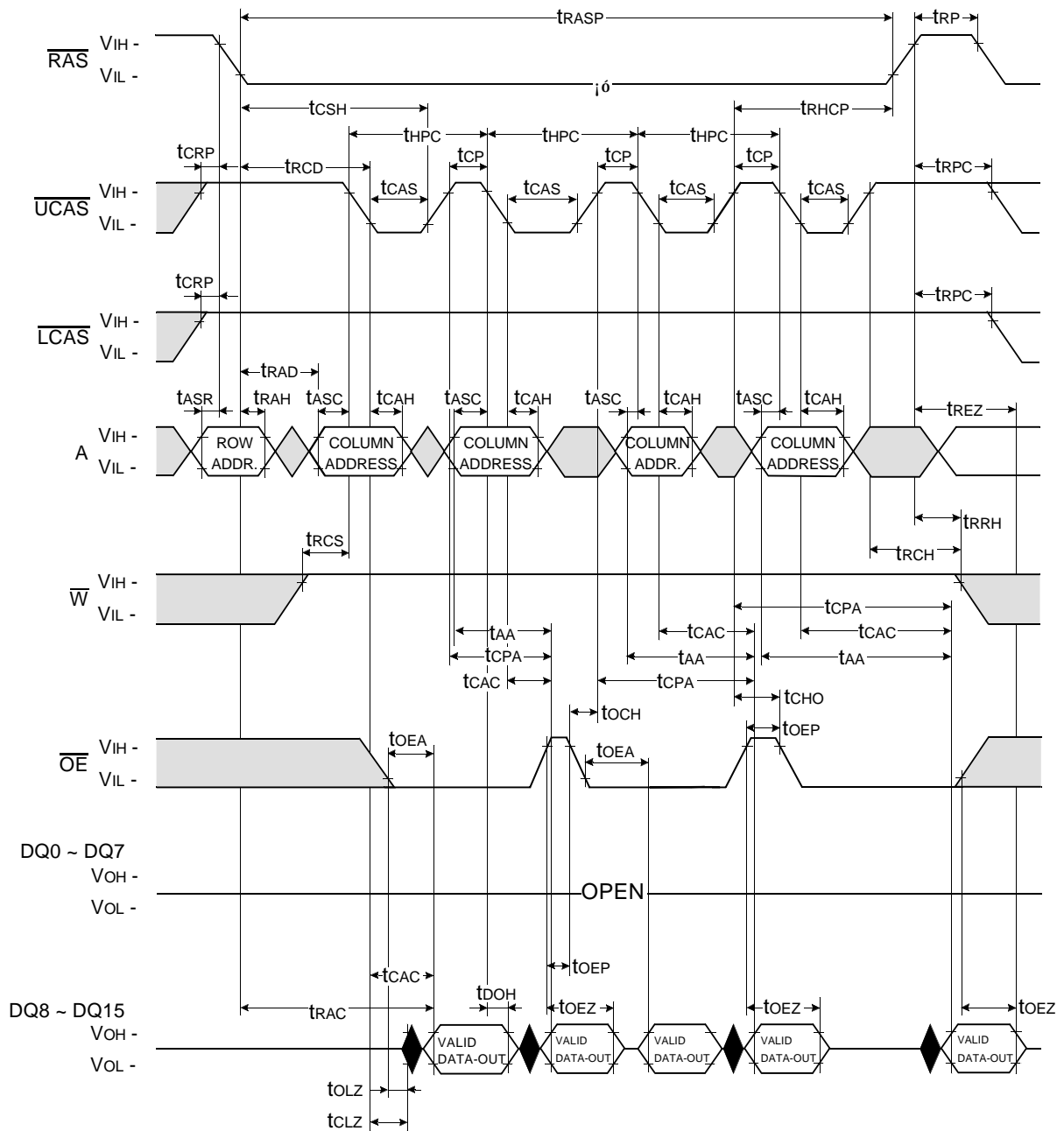
HYPER PAGE MODE LOWER BYTE READ CYCLE



 Don't care

 Undefined

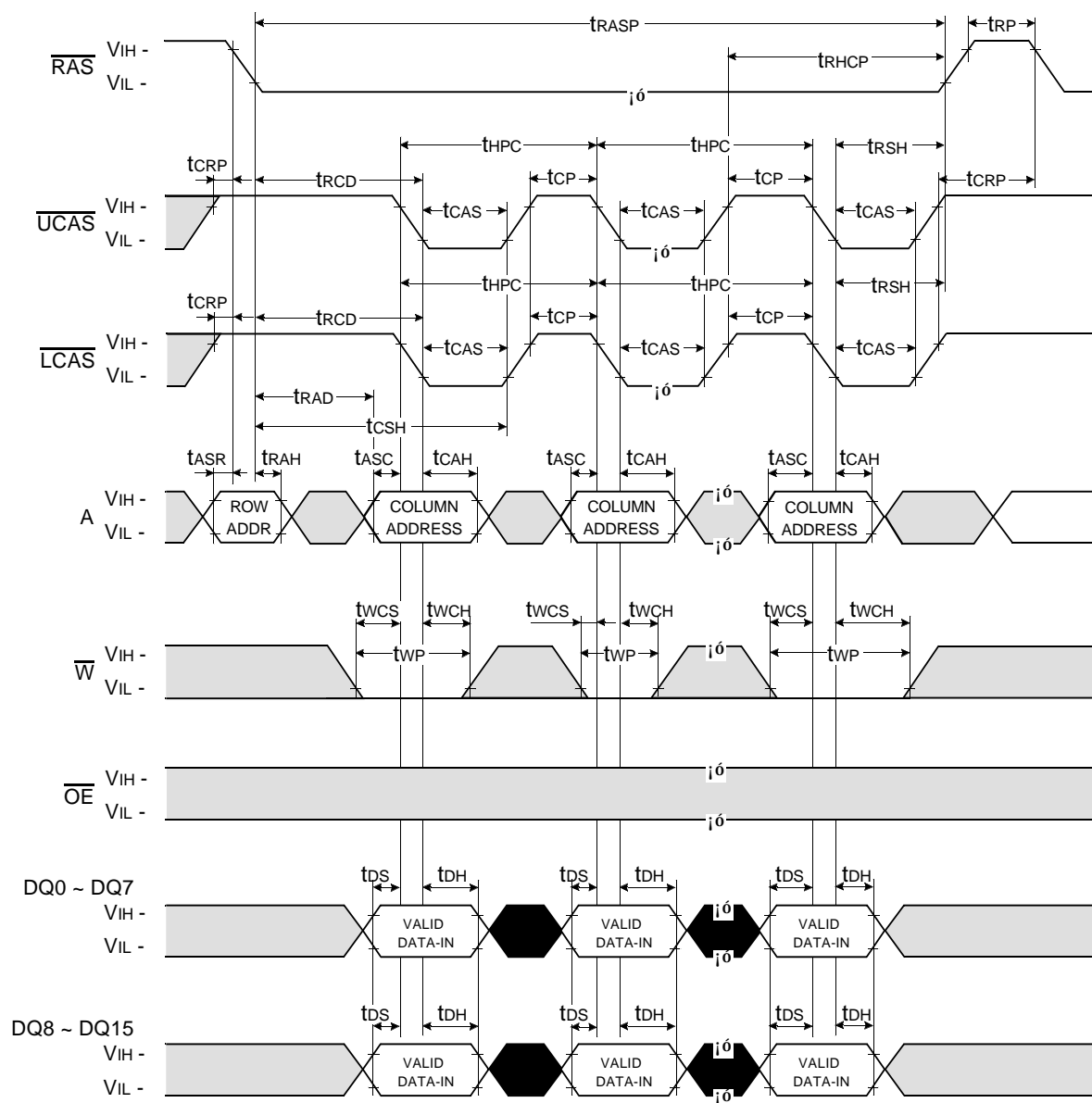
HYPER PAGE MODE UPPER BYTE READ CYCLE



Don't care
Undefined

HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

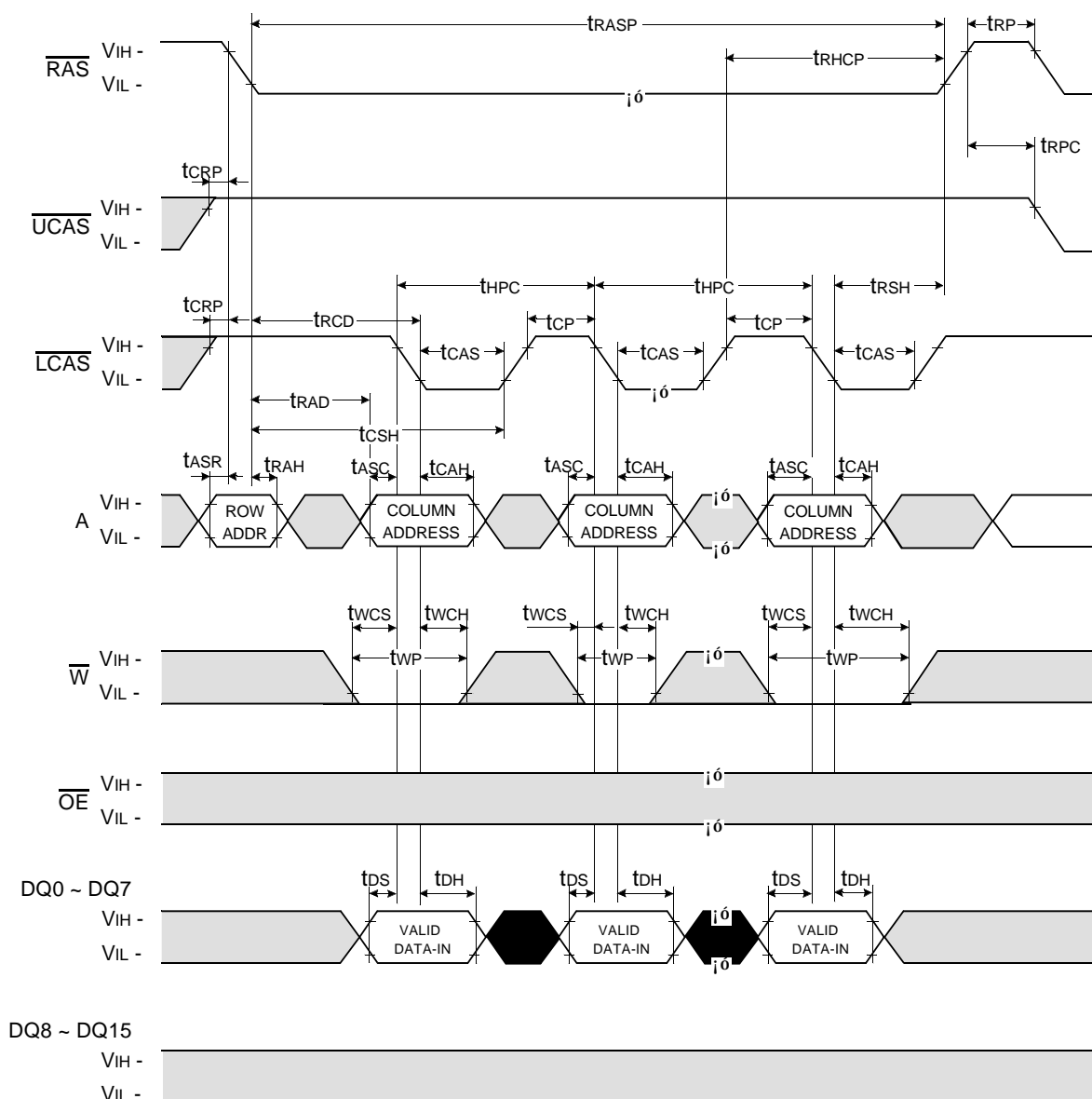
NOTE : DOUT = OPEN



Don't care
Undefined

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

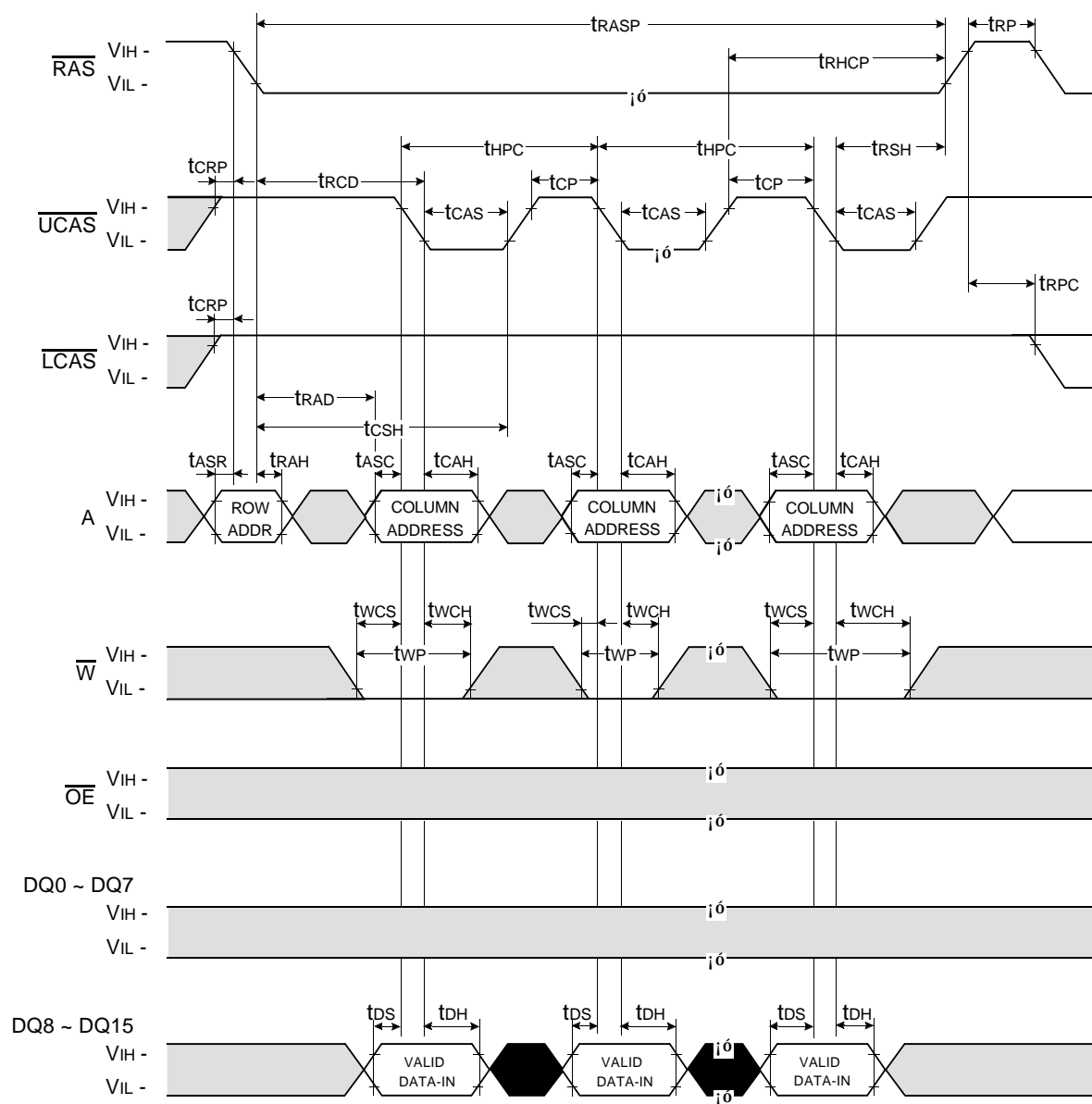
NOTE : DOUT = OPEN



Don't care
Undefined

HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

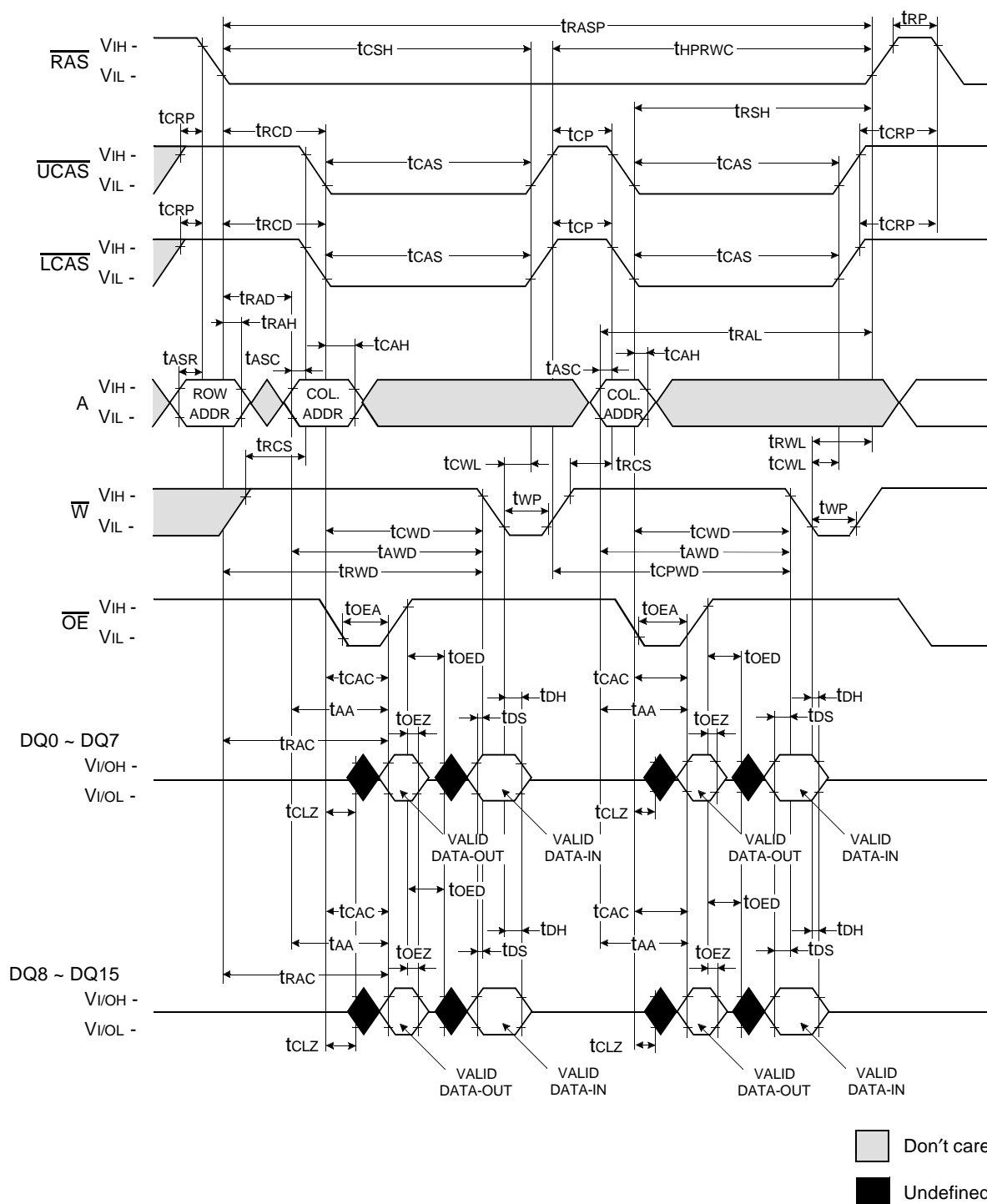
NOTE : DOUT = OPEN



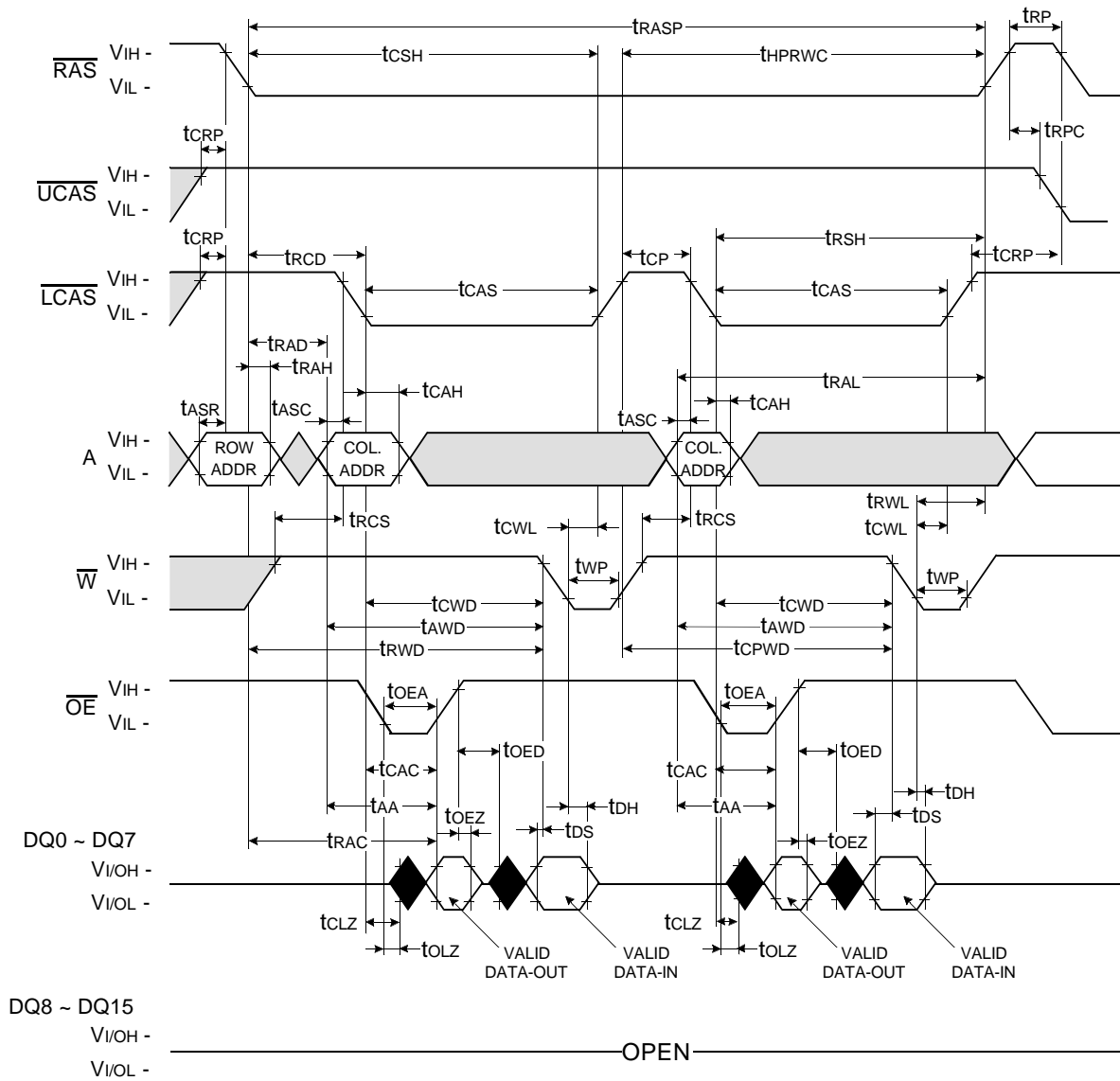
Don't care

Undefined

HYPER PAGE MODE WORD READ - MODIFY - WRITE CYCLE

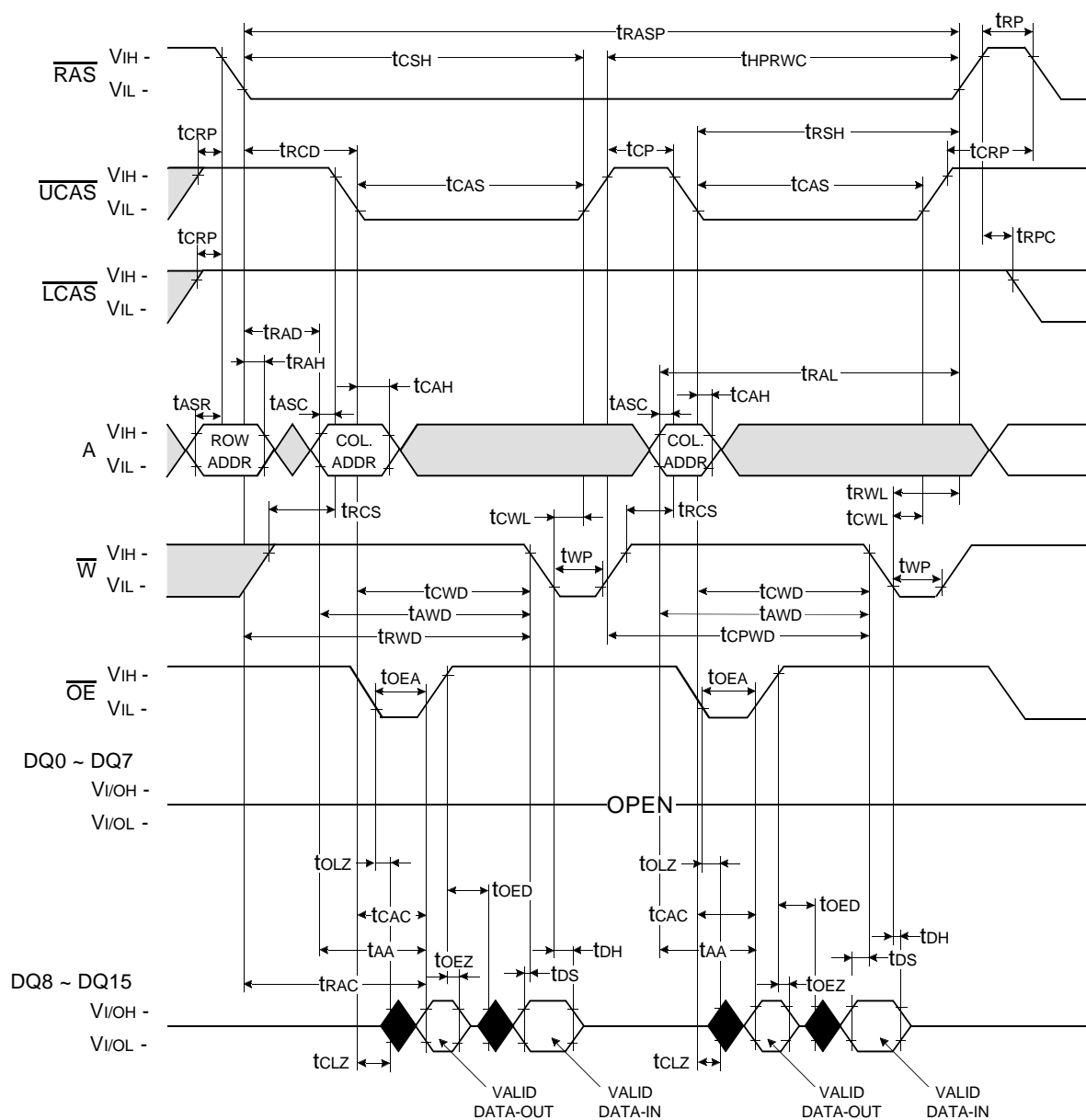



HYPER PAGE MODE LOWER BYTE READ - MODIFY - WRITE CYCLE




Don't care
Undefined

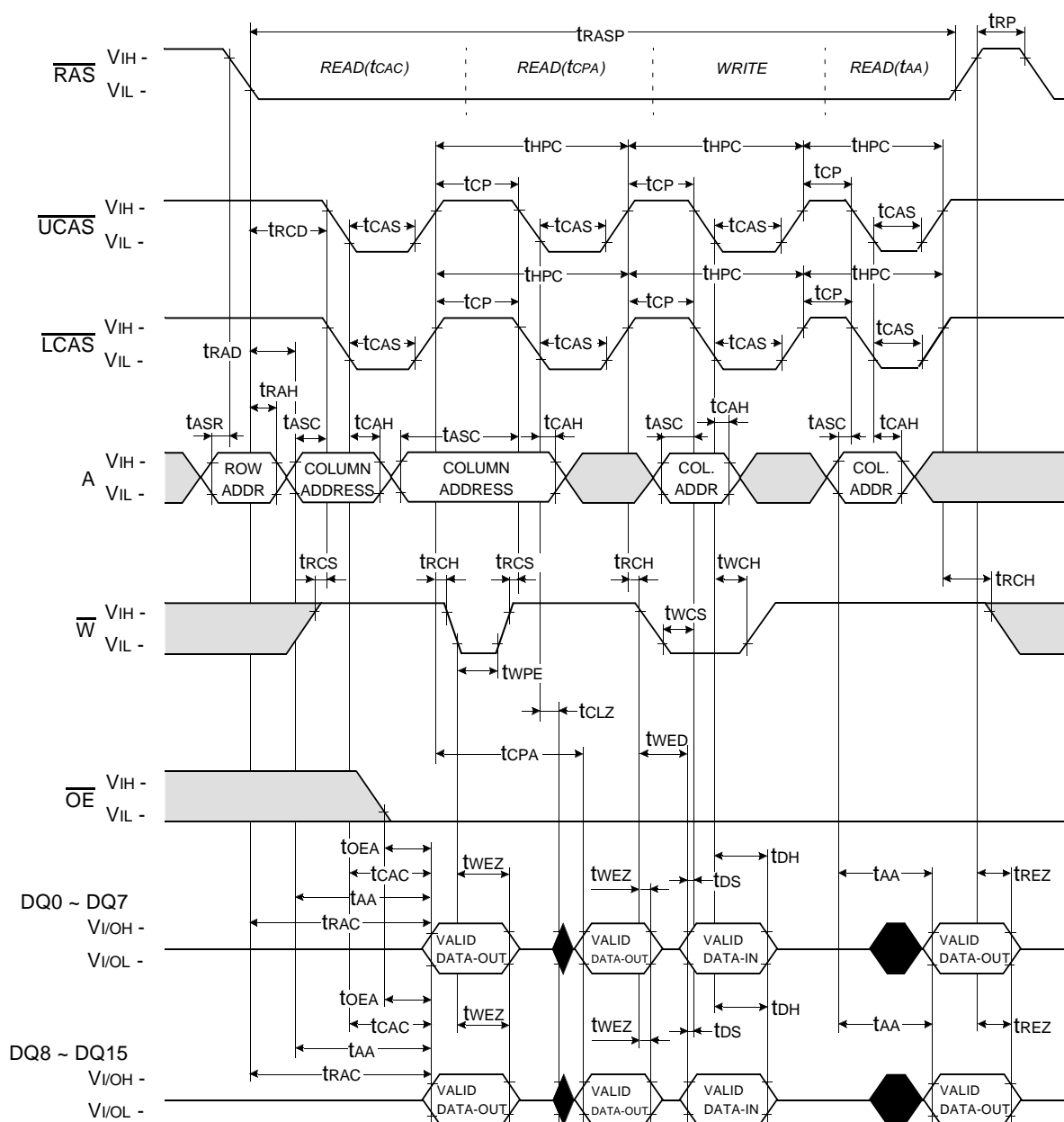
HYPER PAGE MODE UPPER BYTE READ - MODIFY - WRITE CYCLE



 Don't care

 Undefined

HYPER PAGE READ AND WRITE MIXED CYCLE

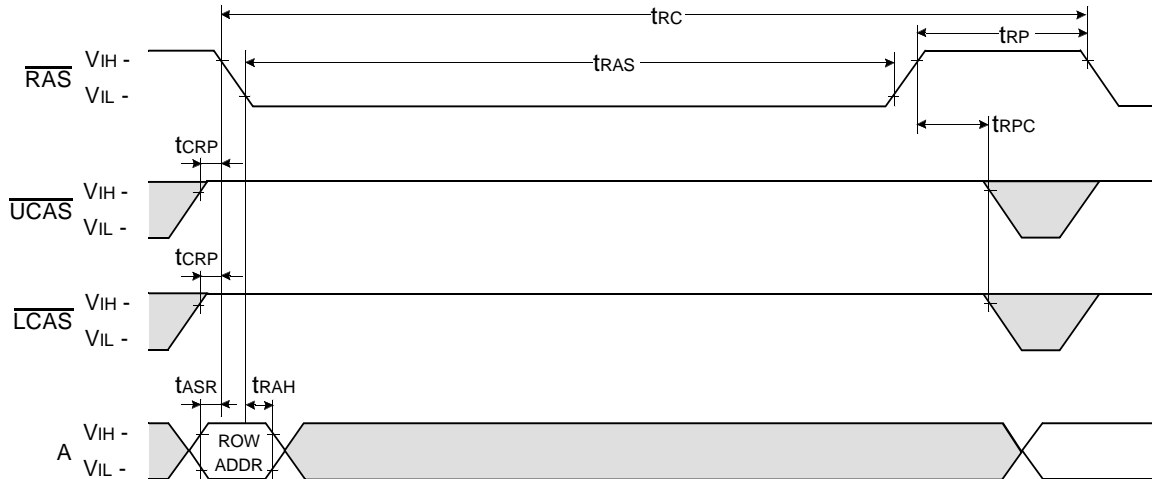
☐ Don't care

Undefined

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

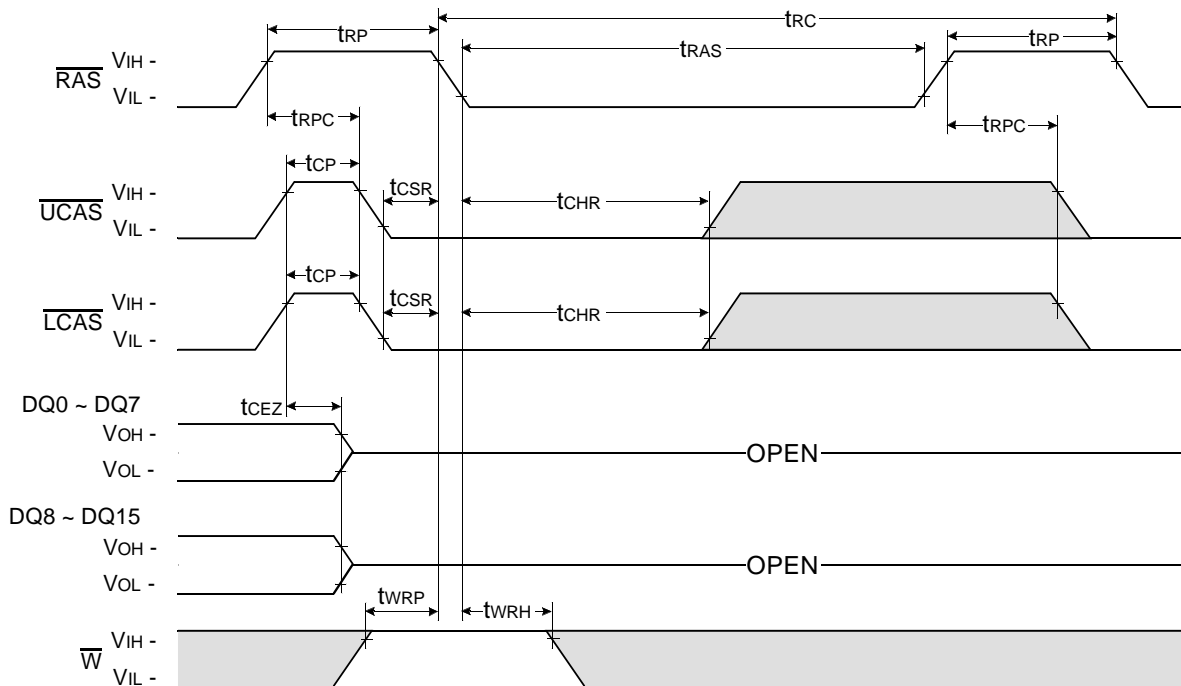
DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care

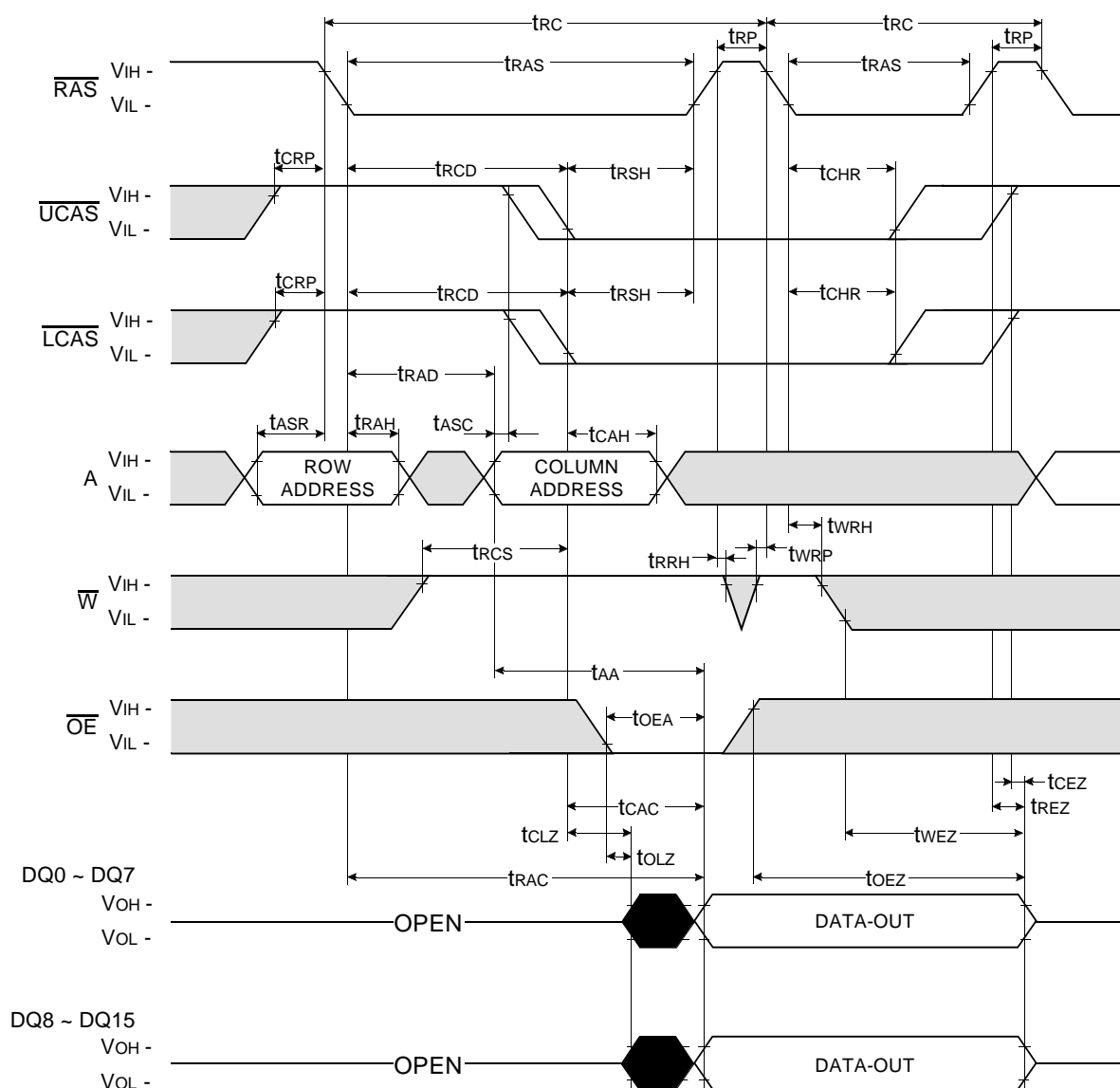
$\overline{\text{WE}}$ = Don't care (4M & 16M DRAM)



□ Don't care
■ Undefined

* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

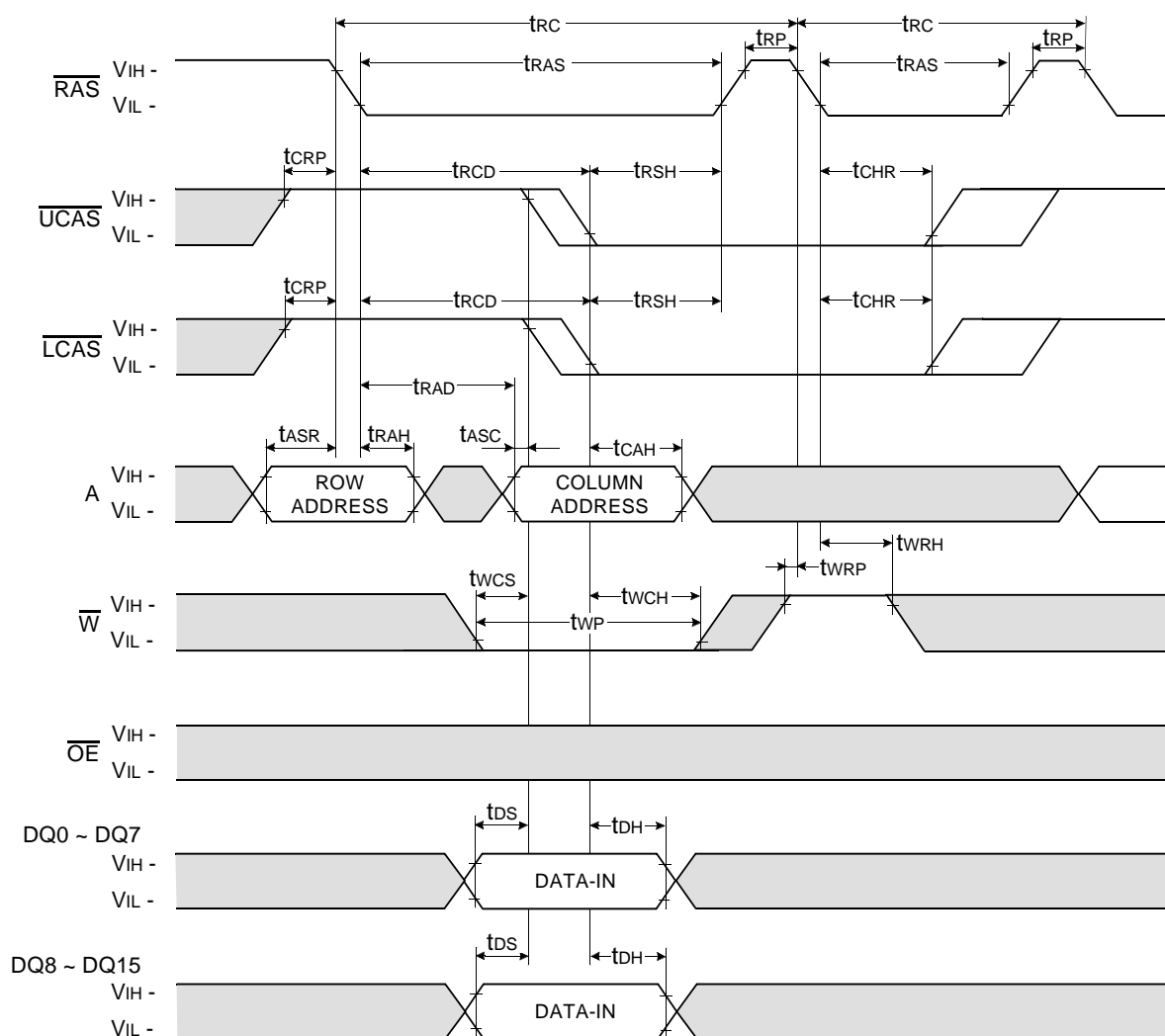
HIDDEN REFRESH CYCLE (READ)

☐ Don't care

■ Undefined

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DoUT = OPEN



Don't care
Undefined

The timing diagram illustrates three memory access cycles: READ CYCLE, WRITE CYCLE, and READ-MODIFY-WRITE.

- READ CYCLE:** Shows signals RAS, UCAS, LCAS, A (COLUMN ADDRESS), W, OE, and DQ0 ~ DQ15 (DATA-OUT). Key parameters include t_{RAS}, t_{CSR}, t_{CHR}, t_{CPT}, t_{SH}, t_{CAS}, t_{AL}, t_{ASC}, t_{CAH}, t_{WRP}, t_{WRH}, t_{RCS}, t_{AC}, t_{RRH}, t_{CH}, t_{CLZ}, t_{OEA}, t_{OEZ}, t_{REZ}.
- WRITE CYCLE:** Shows signals W, OE, and DQ0 ~ DQ15 (DATA-IN). Key parameters include t_{WRP}, t_{WRH}, t_{WCS}, t_{RWL}, t_{CWL}, t_{WCH}, t_{WP}, t_{DS}, t_{DH}.
- READ-MODIFY-WRITE:** Combines elements of both read and write cycles. It shows two consecutive accesses to the same location. Key parameters include t_{WRP}, t_{WRH}, t_{RCS}, t_{AWD}, t_{CWD}, t_{CWL}, t_{TRWL}, t_{WP}, t_{AA}, t_{OEZ}, t_{TOED}, t_{TDH}, t_{CLZ}, t_{OEZ}, t_{DS}.

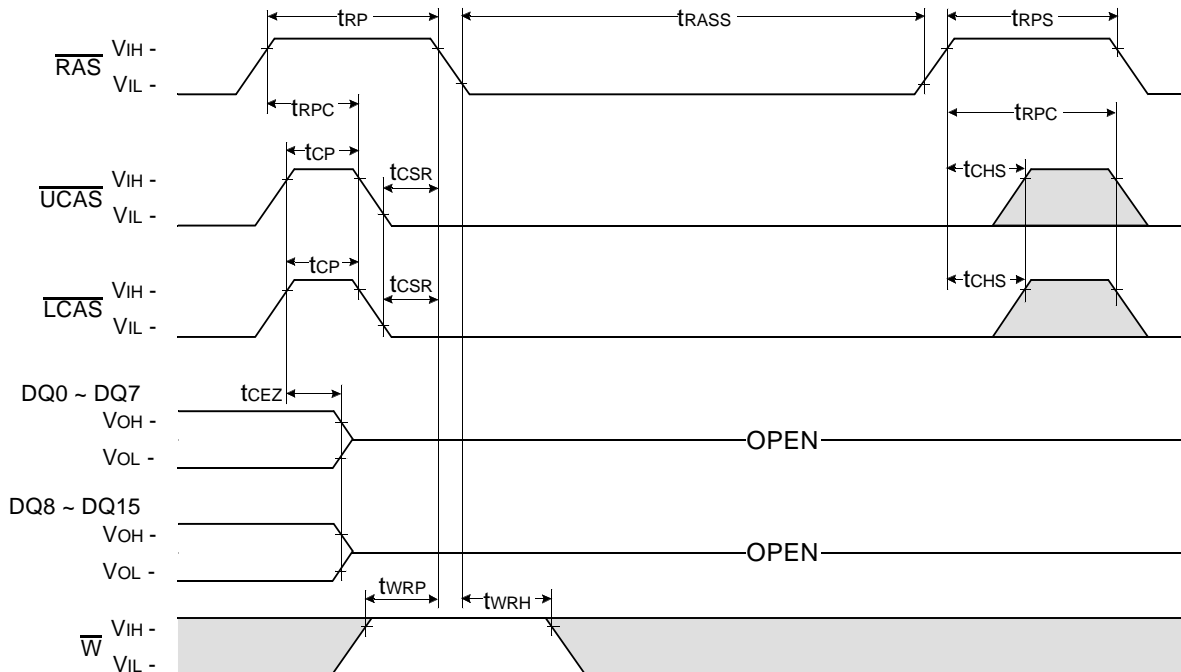
A legend at the bottom right indicates that shaded areas represent "Don't care" states.

NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care

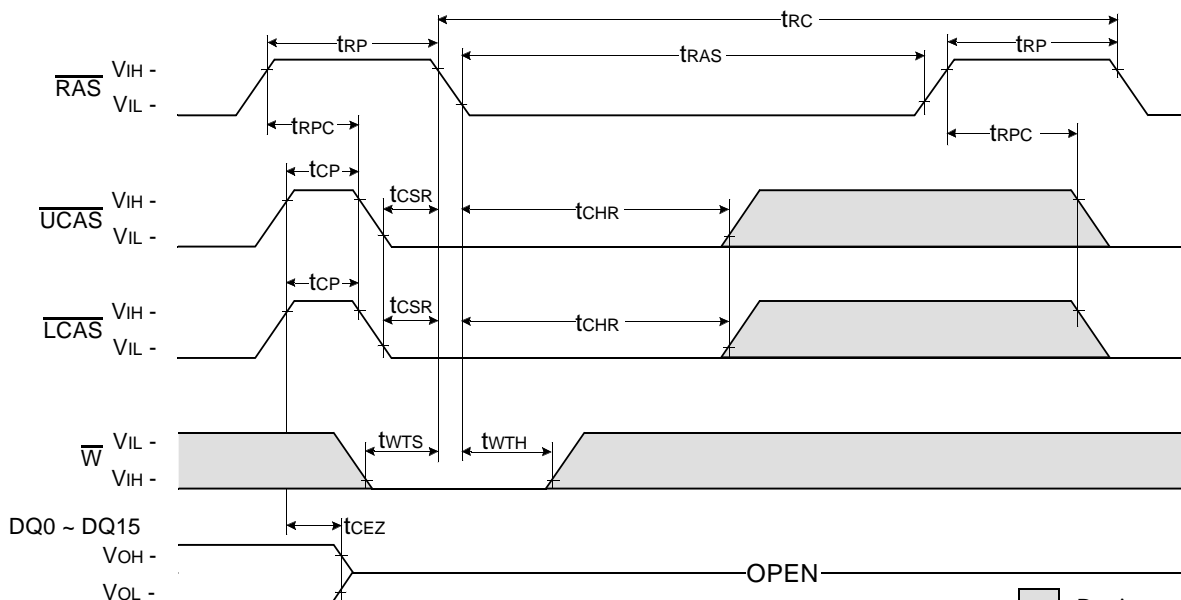
$\overline{\text{WE}}$ = Don't care (4M & 16M DRAM)



TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care

$\overline{\text{WE}}$ = Don't care (4M & 16M DRAM)



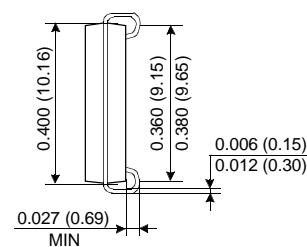
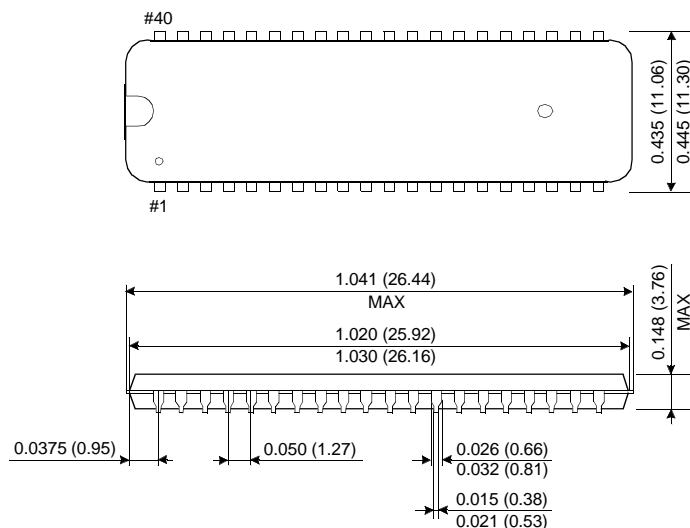
Don't care

Undefined

PACKAGE DIMENSION

40 SOJ 400mil

Units : Inches (millimeters)



44(40) TSOP(II) 400mil

Units : Inches (millimeters)

