

Revision History

Revision .1 (May 1998)

- Pin #70 MCH is changed to N.C.

Revision .2 (June 1998)

- ICC3N & ICC3NS is updated.

Revision .3 (July 1998)

-.DQ Buffer and IBIS characteristics are eliminated.

1M x 32Bit x 2 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
 - CAS latency (1, 2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)

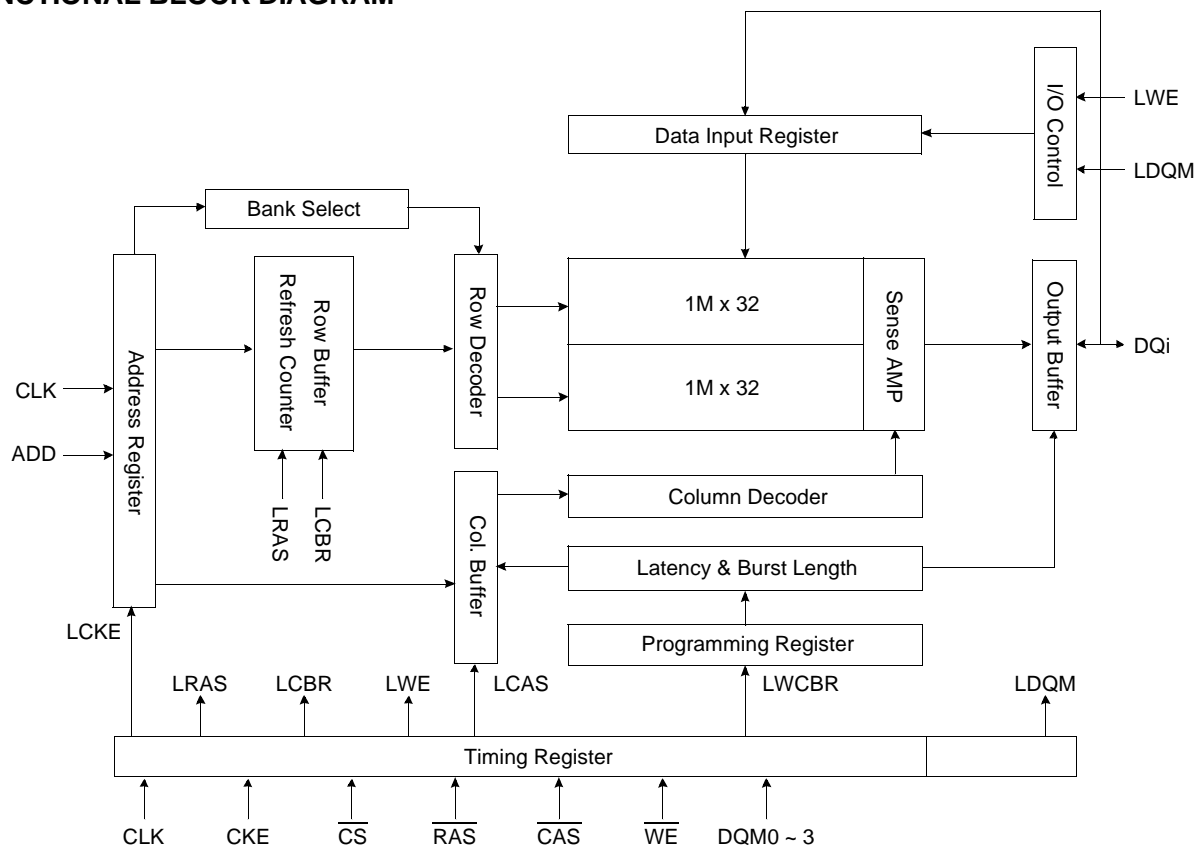
GENERAL DESCRIPTION

The KM432S2020B is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 2 x 1,048,576 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
KM432S2020BT-G/F8	125MHz	LVTTTL	86 TSOP (II)
KM432S2020BT-G/FL	100MHz		
KM432S2020BT-G/F10	100MHz		
KM432S2020BT-G/F12	83MHz		

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION (Top view)

V _{DD}	1	86	V _{SS}
DQ0	2	85	DQ15
V _{DDQ}	3	84	V _{SSQ}
DQ1	4	83	DQ14
DQ2	5	82	DQ13
V _{SSQ}	6	81	V _{DDQ}
DQ3	7	80	DQ12
DQ4	8	79	DQ11
V _{DDQ}	9	78	V _{SSQ}
DQ5	10	77	DQ10
DQ6	11	76	DQ9
V _{SSQ}	12	75	V _{DDQ}
DQ7	13	74	DQ8
N.C	14	73	N.C
V _{DD}	15	72	V _{SS}
DQM0	16	71	DQM1
$\overline{\text{WE}}$	17	70	N.C
$\overline{\text{CAS}}$	18	69	N.C
$\overline{\text{RAS}}$	19	68	CLK
$\overline{\text{CS}}$	20	67	CKE
N.C	21	66	A9
BA	22	65	A8
A11	23	64	A7
A10/AP	24	63	A6
A0	25	62	A5
A1	26	61	A4
A2	27	60	A3
DQM2	28	59	DQM3
V _{DD}	29	58	V _{SS}
N.C	30	57	N.C
DQ16	31	56	DQ31
V _{SSQ}	32	55	V _{DDQ}
DQ17	33	54	DQ30
DQ18	34	53	DQ29
V _{DDQ}	35	52	V _{SSQ}
DQ19	36	51	DQ28
DQ20	37	50	DQ27
V _{SSQ}	38	49	V _{DDQ}
DQ21	39	48	DQ26
DQ22	40	47	DQ25
V _{DDQ}	41	46	V _{SSQ}
DQ23	42	45	DQ24
V _{DD}	43	44	V _{SS}

86Pin TSOP (II)
(400mil x 875mil)
(0.5 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down mode.
A ₀ ~ A ₁₁	Address	Row/column addresses are multiplexed on the same pins. Row address : RA ₀ ~ RA ₁₁ , Column address : CA ₀ ~ CA ₇
BA	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM ₀ ~ 3	Data input/output mask	Makes data output Hi-Z, t _{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ ₀ ~ 31	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Address	C _{ADD}	2.5	5.0	pF
Clock	C _{CLK}	2.5	4.0	pF
DQ ₀ - DQ ₃₁	C _{OUT}	4.0	6.5	pF

DC OPERATING CONDITIONS

 Recommended operating conditions (Voltage referenced to $V_{SS} = 0V$, $T_A = 0$ to $70^\circ C$)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	$V_{DDQ} + 0.3$	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -2mA$
Output logic low voltage	V_{OL}	-	-	0.4	V	$I_{OL} = 2mA$
Input leakage current (Inputs)	I_{IL}	-1	-	1	μA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	μA	3,4

- Notes :**
1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is $\leq 3ns$.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is $\leq 3ns$.
 3. Any input $0V \leq V_{IN} \leq V_{DDQ}$,
Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.
 4. Dout is disabled, $0V \leq V_{OUT} \leq V_{DDQ}$.

DC CHARACTERISTICS

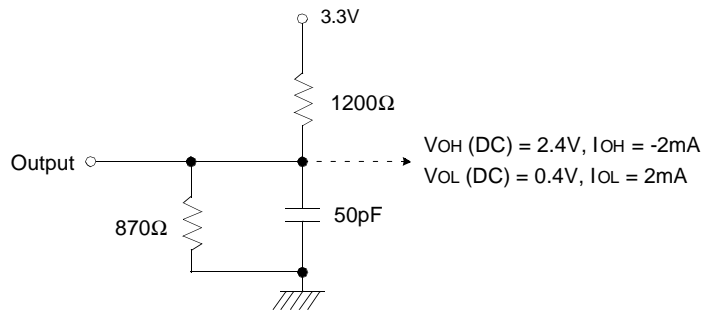
 (Recommended operating condition unless otherwise noted, $T_A = 0$ to $70^\circ C$)

Parameter	Symbol	Test Condition	CAS Latency	Version				Unit	Note
				-8	-L	-10	-12		
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IOL = 0 mA		125	120	110	100	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 15ns		1				mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞		1					
Precharge Standby Current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS} \geq V_{IH}(\min)$, tcc = 15ns Input signals are changed one time during 30ns		15				mA	
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		5				mA	
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 15ns		2				mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞		1					
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), $\overline{CS} \geq V_{IH}(\min)$, tcc = 15ns Input signals are changed one time during 30ns		30				mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		20				mA	
Operating current (Burst mode)	ICC4	IOL = 0 mA Page burst 2 Banks activated tccd = 2CLKs	3	135	120	120	110	mA	1
			2	110	110	105	100		
			1	100	100	95	85		
Refresh current	ICC5	trc ≥ trc(min)		150	150	130	115	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V		1				mA	3
				400				uA	4

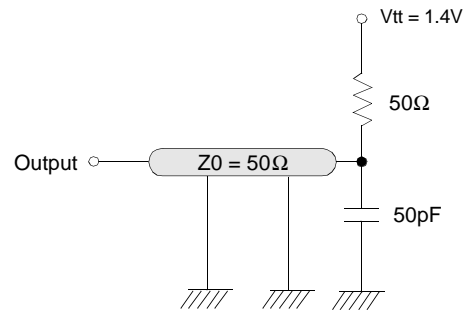
- Notes :**
1. Measured with outputs open.
 2. Refresh period is 64ms.
 3. KM432S2020BT-G**
 4. KM432S2020BT-F**

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
Input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$tr/tf = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			-8	-L	-10	-12		
Row active to row active delay		tRRD(min)	16	20	20	24	ns	1
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		tRCD(min)	20	20	26	30	ns	1
Row precharge time		tRP(min)	20	20	26	30	ns	1
Row active time		tRAS(min)	48	50	50	60	ns	1
		tRAS(max)	100				us	
Row cycle time	@ Operation	tRC(min)	68	70	80	90	ns	1
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to row precharge		tRDL(min)	8	10	13	15	ns	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	3
Number of valid output data	CAS latency=3		2				ea	4
	CAS latency=2		1					
	CAS latency=1		0					

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-8		-L		-10		-12		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	10	1000	10	1000	12	1000	ns	1
	CAS latency=2		12		12		13		15			
	CAS latency=1		24		24		26		30			
CLK to valid output delay	CAS latency=3	tSAC		6		6		7		8	ns	1,2
	CAS latency=2			6		7		8		9		
	CAS latency=1			20		20		22		24		
Output data hold time	CAS latency=3	tOH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
	CAS latency=1		5		5		5		5			
CLK high pulse width		tCH	3		3		3.5		3.5		ns	3
CLK low pulse width		tCL	3		3		3.5		3.5		ns	3
Input setup time		tSS	2		2		2.5		3		ns	3
Input hold time		tSH	1		1		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		6		7		8	ns	
	CAS latency=2			6		7		8		9		
	CAS latency=1			20		20		22		24		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.
 - This parameter is guaranteed by design not by test.

KM432S2020B

Preliminary CMOS SDRAM

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

KM432S2020BT-8

(Unit : Number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		68ns	48ns	20ns	16ns	20ns	8ns	8ns	8ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1

KM432S2020BT-L

(Unit : Number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	3	6	5	2	2	2	1	1	1
75MHz (13.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	5	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM432S2020BT-10

(Unit : Number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		80ns	50ns	26ns	20ns	26ns	10ns	10ns	13ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	2
83MHz (12.0ns)	3	7	5	3	2	3	1	1	2
75MHz (13.0ns)	2	7	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	5	3	2	2	2	1	1	1

KM432S2020BT-12

(Unit : Number of clock)

Frequency	CAS Latency	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		90ns	60ns	30ns	24ns	30ns	12ns	12ns	15ns
83MHz (12.0ns)	3	8	5	3	2	3	1	1	2
75MHz (13.0ns)	3	7	5	3	2	3	1	1	2
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1
60MHz (16.7ns)	2	6	4	2	2	2	1	1	1
50MHz (20.0ns)	2	5	3	2	2	2	1	1	1

SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DQM	BA	A10/AP	A11, A9 ~ A0	Note	
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
													3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A0 ~ A7)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	Both banks									X	H		
Clock Suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A11, BA : Program keys. (@MRS)

2. MRS can be issued only at both banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at both banks precharge state.

4. BA : Bank select address.

If "Low" at read, write, row active and precharge, bank A is selected.

If "High" at read, write, row active and precharge, bank B is selected.

If A10/AP is "High" at row precharge, BA is ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command for another bank can be issued.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)