

**Document Title****256Kx16 bit Low Power CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
0.0	Initial draft	December 17, 1998	Preliminary
1.0	Finalize	April 17, 1999	Finalize

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## 256Kx16 bit Low Power CMOS Static RAM

### FEATURES

- Process Technology: TFT
- Organization: 256Kx16
- Power Supply Voltage : 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F/R

### GENERAL DESCRIPTION

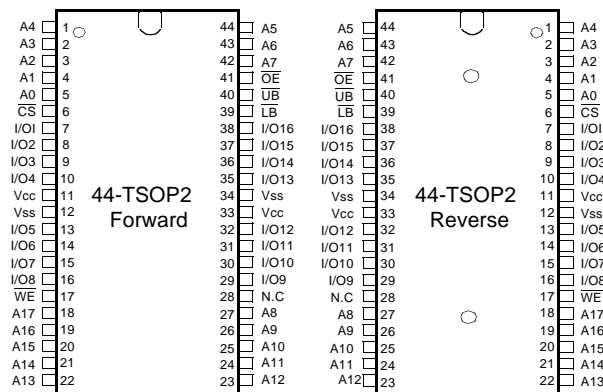
The KM6164000C families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and small package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
KM6164000CL-L	Commercial(0~70°C)	4.5~5.5V	55 <sup>1)</sup> /70	20μA	90mA	44-TSOP2-F/R
KM6164000CLI-L	Industrial(-40~85°C)			50μA		

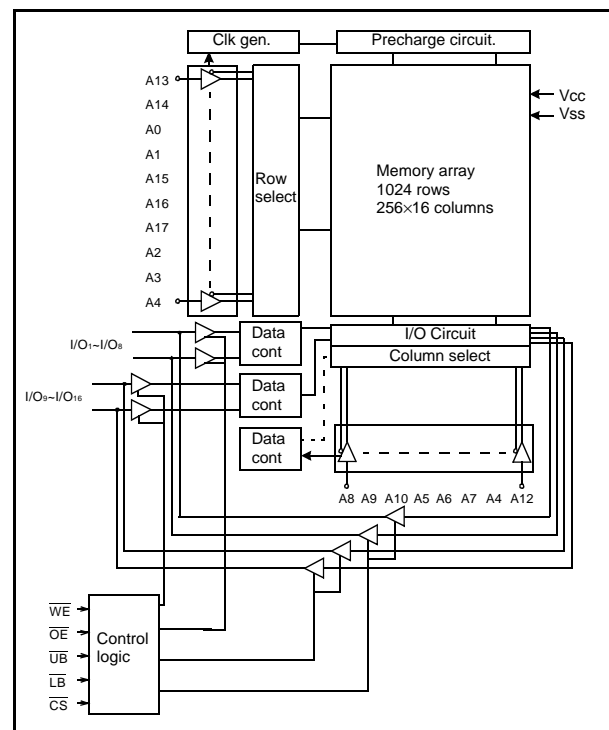
1. The parameter is measured with 50pF test load.

### PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O <sub>9-16</sub> )
A <sub>0</sub> ~A <sub>17</sub>	Address Inputs	$\overline{LB}$	Lower Byte (I/O <sub>1-8</sub> )
I/O <sub>1</sub> ~I/O <sub>16</sub>	Data Inputs/Outputs	N.C	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Temperature Product(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM6164000CLT-5L	44-TSOP2-F, 55ns, LL-pwr	KM6164000CLTI-5L	44-TSOP2-F, 55ns, LL-pwr
KM6164000CLT-7L	44-TSOP2-F, 70ns, LL-pwr	KM6164000CLTI-7L	44-TSOP2-F, 70ns, LL-pwr
KM6164000CLR-5L	44-TSOP2-R, 55ns, LL-pwr	KM6164000CLRI-5L	44-TSOP2-R, 55ns, LL-pwr
KM6164000CLR-7L	44-TSOP2-R, 70ns, LL-pwr	KM6164000CLRI-7L	44-TSOP2-R, 70ns, LL-pwr

## FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O <sub>1-8</sub>	I/O <sub>9-16</sub>	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselected	Standby
L	H	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Output Disabled	Active
L	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X <sup>1)</sup>	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X <sup>1)</sup>	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X <sup>1)</sup>	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM6164000CL-L
		-40 to 85	°C	KM6164000CLI-L

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.5 <sup>3)</sup>	-	0.8	V

Note:

- Commercial Product : T<sub>A</sub>=0 to 70°C, otherwise specified  
Industrial Product : T<sub>A</sub>=-40 to 85°C, otherwise specified
- Overshoot : V<sub>CC</sub>+3.0V in case of pulse width ≤ 30ns
- Undershoot : -3.0V in case of pulse width ≤ 30ns
- Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

- Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS}$ =V <sub>IH</sub> or $\overline{OE}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Operating power supply	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , Read	-	-	10	mA
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}$ ≤0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	15	mA
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	90	mA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V
Standby Current (TTL)	I <sub>SB</sub>	$\overline{CS}$ =V <sub>IH</sub> , Other inputs=V <sub>IL</sub> or V <sub>IH</sub>	-	-	3	mA
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS}$ ≥V <sub>CC</sub> -0.2V, Other inputs=0~V <sub>CC</sub>	-	-	20 <sup>1)</sup>	μA

- Industrial Product = 50μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Test Input/Output Reference)

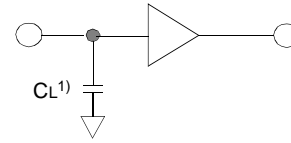
Input pulse level : 0.8 to 2.4V

Input rising and falling time : 5ns

Input and output reference voltage : 1.5V

Output load (See right) :  $C_L = 100\text{pF} + 1\text{TTL}$   
 $50\text{pF} + 1\text{TTL}^{(1)}$

1. for 55ns product



1. Including scope and jig capacitance

## AC CHARACTERISTICS (KM6164000C Family : $V_{CC} = 4.5 \sim 5.5\text{V}$ , Commercial product : $T_A = 0$ to $70^\circ\text{C}$ , Industrial product : $T_A = -40$ to $85^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	ns
	Address access time	tAA	-	55	-	70	ns
	Chip select to output	tCO	-	55	-	70	ns
	Output enable to valid output	tOE	-	25	-	35	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ enable to low-Z output	tBLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	ns
	$\overline{\text{OE}}$ disable to high-Z output	tOHZ	0	20	0	25	ns
	Output hold from address change	tOH	10	-	10	-	ns
	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ valid to data output	tBA	-	25	-	35	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ disable to high-Z output	tBHZ	0	20	0	25	ns
Write	Write cycle time	tWC	55	-	70	-	ns
	Chip select to end of write	tCW	45	-	60	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	ns
	Write pulse width	tWP	45	-	55	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	ns
	Data to write time overlap	tDW	25	-	30	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns
	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ valid to end of write	tBW	45	-	60	-	ns

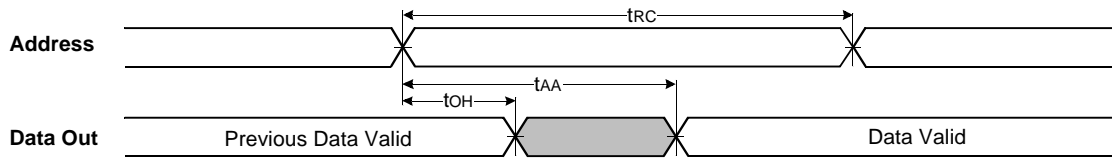
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$	2.0	-	5.5	V
Data retention current	I <sub>DR</sub>	V <sub>CC</sub> = 3.0V	-	-	15 <sup>1)</sup>	μA
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

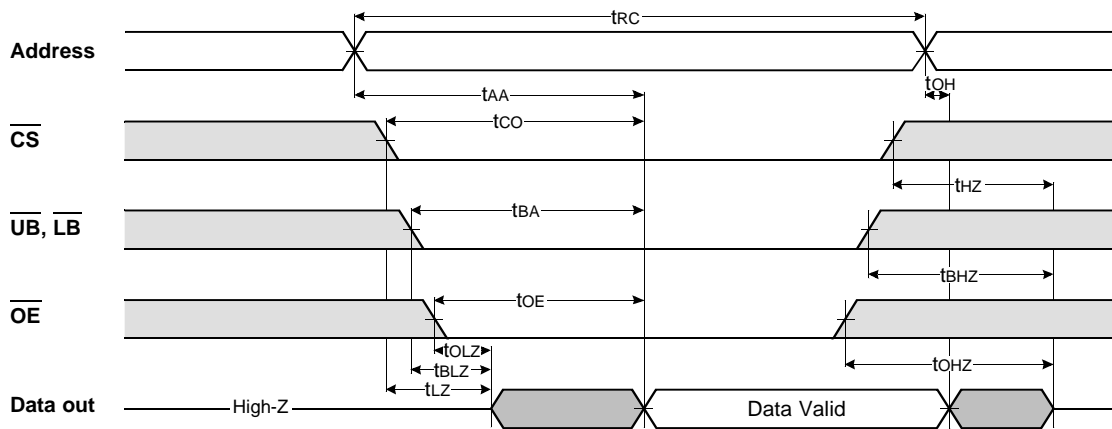
1. Industrial Product : 20μA

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or/and  $\overline{LB}=V_{IL}$ )



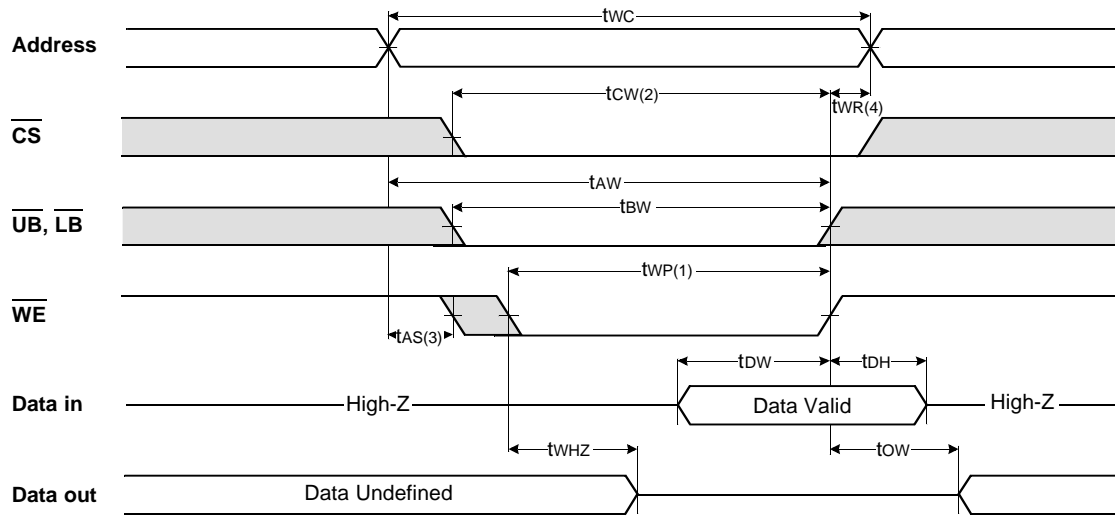
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



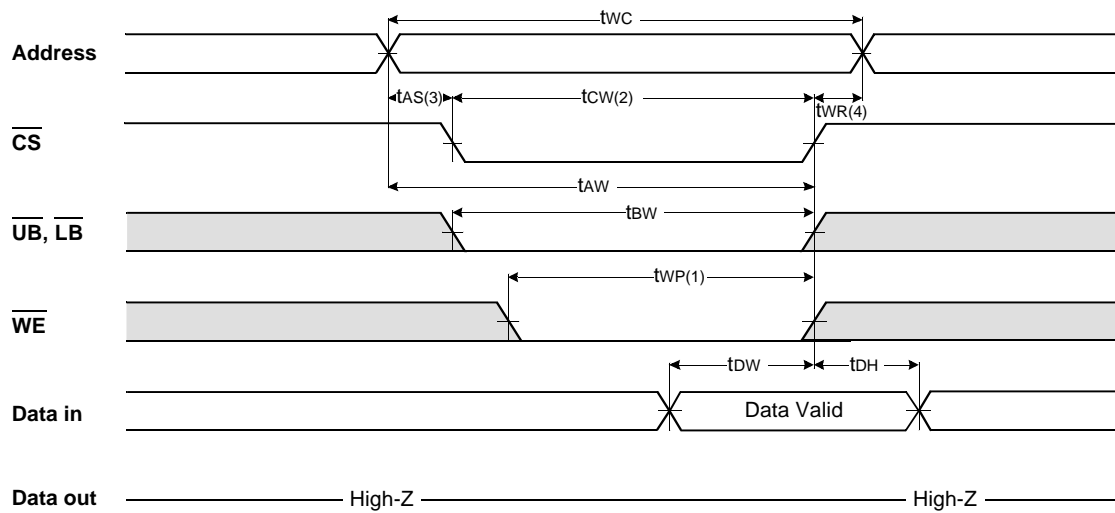
### NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

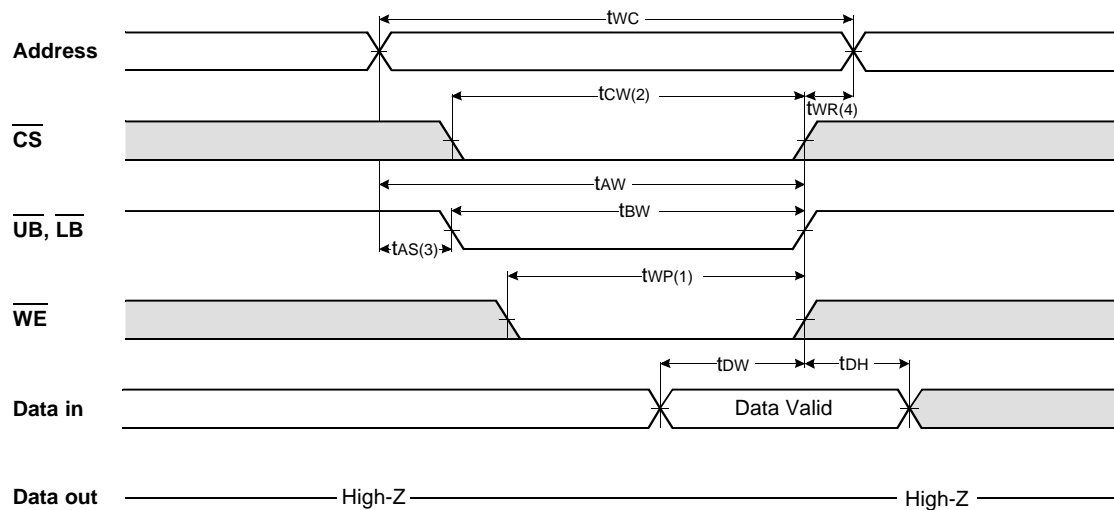
**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{\text{WE}}$  Controlled)**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{\text{CS}}$  Controlled)**



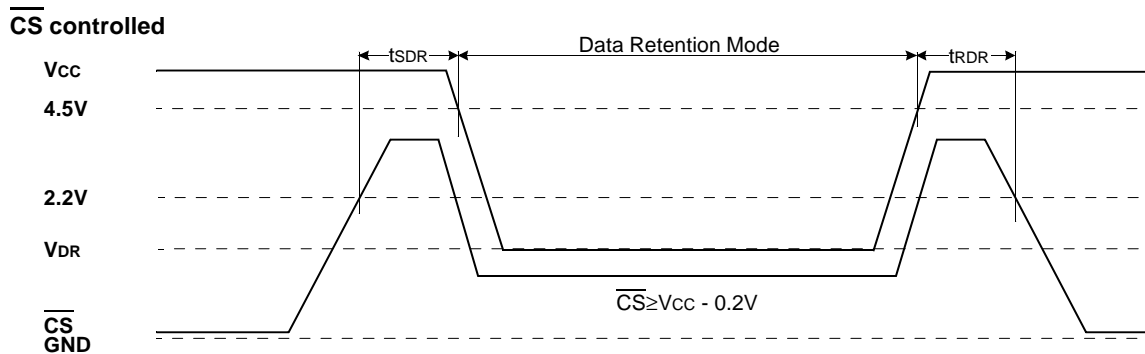
## TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{UB}$ , $\overline{LB}$ Controlled)



### NOTES (WRITE CYCLE)

1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.

## DATA RETENTION WAVE FORM

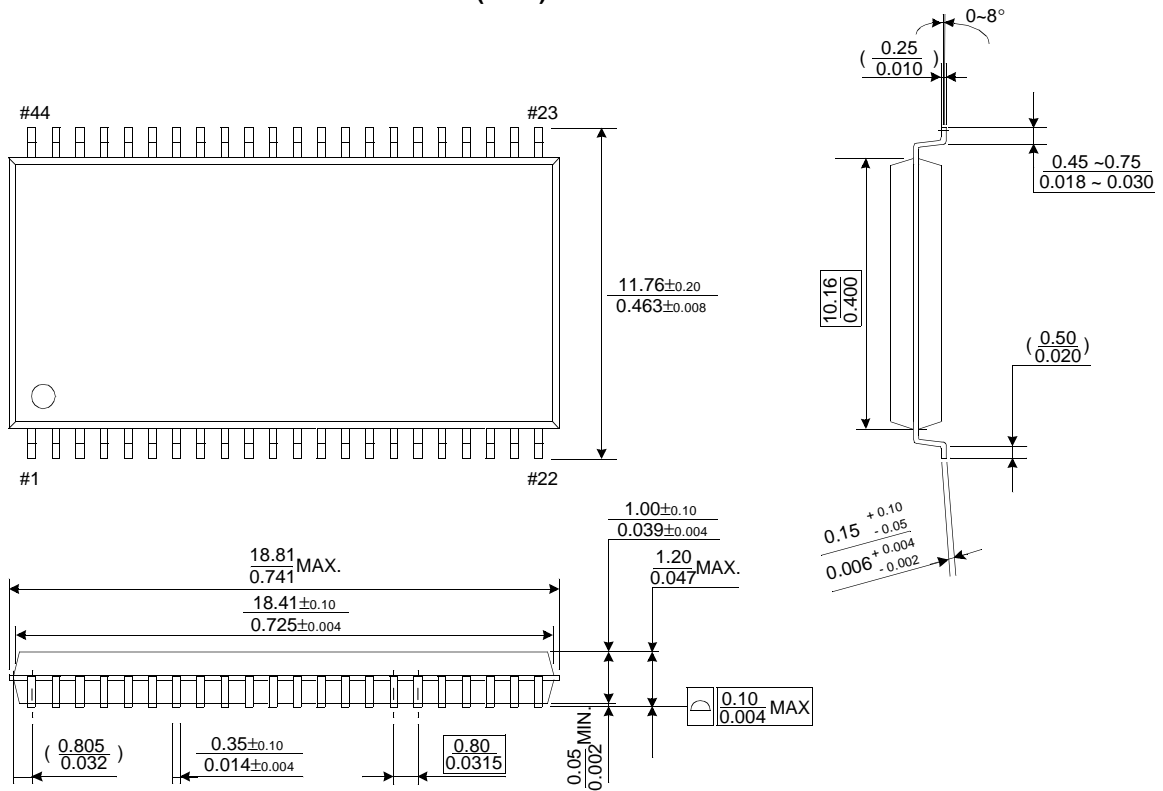




## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



### 44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

