

## Document Title

**64Kx16 Super Low Power and Low Voltage Full CMOS SRAM  
with 48-CSP Data Sheets**

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial Draft - LB, UB controls standby mode	June 3, 1997	Preliminary
0.1	Revision - Erase commercial part	December 16, 1997	Preliminary

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## 64Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM with 48-CSP

### FEATURE SUMMARY

- Process Technology : Full CMOS
- Organization : 64Kx16
- Power Supply Voltage
  - KM616FS1010 Family : 2.3V ~ 3.3V
  - KM616FR1010 Family : 1.8V ~ 2.7V
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

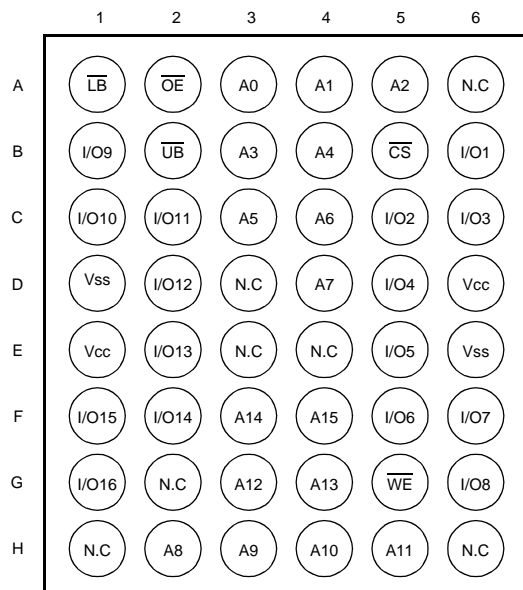
### GENERAL DESCRIPTION

The KM616FS1010Z and KM616FR1010Z families are fabricated by SAMSUNG's advanced Full CMOS process technology. The families support various operating temperature ranges and have very small size with 0.75 ball pitch and 6 x 8 ball array. The families also support low data retention voltage for battery back-up operations with low data retention current.

### PRODUCT FAMILY

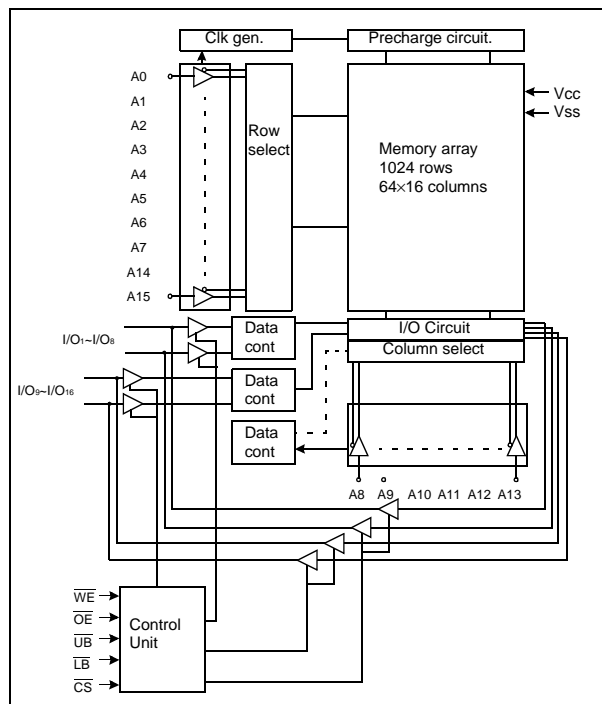
Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (IsB1, Max)	Operating (Icc2, Max)	
KM616FS1010ZI	Industrial(-40~85°C)	2.3~3.3V	100@Vcc=3.0±0.3V 150@Vcc=2.5±0.2V	5μA	80mA 50mA	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM616FR1010ZI		1.8~2.7V	300@Vcc=2.0±0.2V		25mA	

### 48-CSP PIN TOP VIEW



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	$\overline{LB}$	Lower Byte(I/O1~8)
$\overline{OE}$	Output Enable input	$\overline{UB}$	Upper Byte(I/O9~16)
$\overline{WE}$	Write Enable Input	Vcc	Power
A0~A15	Address Inputs	Vss	Ground
I/O1~I/O16	Data Inputs/Outputs	N.C.	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Industrial Temp Products(-40~85°C)	
Part Name	Function
KM616FS1010ZI-15	48-CSP, 2.5V/3.0V, 150/100ns
KM616FR1010ZI-30	48-CSP, 1.8V/2.5V, 300ns

### Note

1. The meaning of 2.5V/3.0V, 150/100ns is that the operating Vcc is ranged from 2.3V(Min) to 3.3V(Max) with speed 150ns @2.5V±0.2 and 100ns @3.0V±0.3. This type of meaning is applied to other notations like the example.
2. In case of KM616FR1010Z-30, there is only one speed bin, 300ns though it supports wide range operating Vcc.

## FUNCTIONAL DESCRIPTION

CS	OE	WE	LB	UB	I/O <sub>1~8</sub>	I/O <sub>9~16</sub>	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Delected	Standby
L	H	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Output Disabled	Active
X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	Output Disabled	Standby
L	L	H	L	H	Dout	High-Z	Read	Active
L	L	H	H	L	High-Z	Dout	Read	
L	L	H	L	L	Dout	Dout	Read	
L	X <sup>1)</sup>	L	L	H	Din	High	Write	Active
L	X <sup>1)</sup>	L	H	L	High-Z	Din	Write	
L	X <sup>1)</sup>	L	L	L	Din	Din	Write	

1. X means don't care.(Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.2 to 3.6V	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.2 to 4.0V	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-55 to 150	°C	-
Operating Temperature	T <sub>A</sub>	-40 to 85	°C	KM616FS1010ZI KM616FR1010ZI
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 5sec(Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product		Min	Typ	Max	Unit
Supply voltage	Vcc	KM616FS1010Z Family		2.3	2.5/3.0	3.3	V
		KM616FR1010Z Family		1.8	2.0/2.5	2.7	V
Ground	Vss	All Family		0	0	0	V
Input high voltage	VIH	KM616FS1010Z Family	Vcc=3.0±0.2V	2.2	-	Vcc+0.2 <sup>2)</sup>	V
			Vcc=2.5±0.2V	2.0	-	Vcc+0.2 <sup>2)</sup>	V
		KM616FR1010Z Family	Vcc=2.5±0.2V	2.0	-	Vcc+0.2 <sup>2)</sup>	V
			Vcc=2.0±0.2V	1.6	-	Vcc+0.2 <sup>2)</sup>	V
Input low voltage	VIL	KM616FS1010Z, KM616FR1010Z Family		-0.2 <sup>3)</sup>	-	0.6	V

Note:

1. T<sub>A</sub>= -40 to 85°C, unless otherwise specified

2. Overshoot : V<sub>CC</sub>+3.0V for ≤30ns pulse width

3. Undershoot: V<sub>IL</sub>(Min)=-1.5V for ≤30ns pulse width

4. Overshoot and undershoot is sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

1. Capacitance is sampled not, 100% tested

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>		-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}$ =V <sub>IH</sub> or $\overline{CS}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>		-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	$\overline{CS}$ =V <sub>IL</sub> , I <sub>IO</sub> =0mA, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	Read	-	-	10 <sup>1)</sup>	mA	
			Write	-	-	20 <sup>1)</sup>		
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100%duty $\overline{CS}$ ≤0.2V	Read	-	-	10 <sup>1)</sup>	mA	
			Write	-	-	20 <sup>1)</sup>		
	I <sub>CC2</sub>	Cycle time=Min, 100% duty I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IH</sub>	V <sub>CC</sub> =3.3V@100ns	-	-	80	mA	
			V <sub>CC</sub> =2.5V@150ns	-	-	50		
			V <sub>CC</sub> =2.0V@300ns	-	-	25		
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub>	KM616FS1010Z Family	0.5mA	-	-	0.4	V
			KM616FR1010Z Family	0.33mA	-	-	0.4	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub>	KM616FS1010ZI Family	0.5mA	2.0	-	-	V
			KM616FR1010ZI Family	-0.44mA	1.6	-	-	
Standby Current (TTL)	I <sub>SB</sub>	$\overline{CS}$ =V <sub>IH</sub>		-	-	0.3	mA	
Standby Current (CMOS)	I <sub>SB1</sub>	$\overline{CS}$ ≥V <sub>CC</sub> -0.2V or LB=UB≥V <sub>CC</sub> -0.2V, Other inpus =0~V <sub>CC</sub>		-	0.05 <sup>2)</sup>	5 <sup>3)</sup>	μA	

1. The value is measured at V<sub>CC</sub>=3.0V±0.3V, The value measured at V<sub>CC</sub>=2.5/2.0V is under the value of V<sub>CC</sub>=3.0

2. The value is not 100% tested but obtained statistically at Temp=25°C

3. The value has difference by ±1μA. The value is measured at V<sub>CC</sub>=3.3V

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V at Vcc=3.0/2.5V

0.4 to 1.8V at Vcc=2.0V

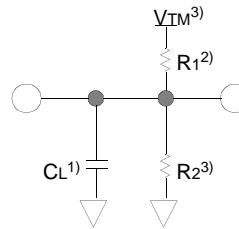
Input rising and falling time : 5ns

Input and output reference voltage : 1.5V at Vcc=3.0V,

1.1V at Vcc=2.5V,

0.9V at Vcc=2.0V

Output load(see right) : CL=30pF



1. Including scope and jig capacitance

2. R1=3070Ω, R2=3150Ω

3. VTM=2.8V/2.3V/1.8V

## AC CHARACTERISTICS (TA=-40 to 85°C, KM616FS1010ZI Family:Vcc=2.3 ~3.3V, KM616FS1010ZI Family:Vcc=1.8~2.7V)

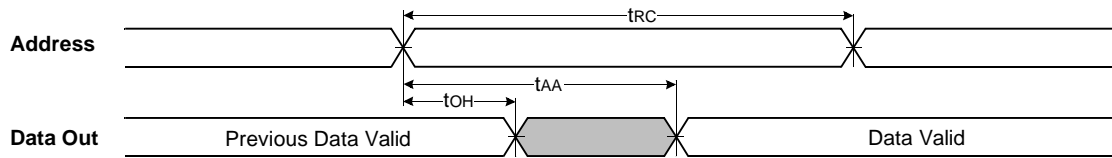
Parameter List		Symbol	Speed Bins						Units
			100ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	100	-	150	-	300	-	ns
	Address access time	tAA	-	100	-	150	-	300	ns
	Chip select to output	tCO	-	100	-	150	-	300	ns
	Output enable to valid output	tOE	-	50	-	75	-	150	ns
	$\overline{UB}$ , $\overline{LB}$ Access Time	tBA	-	100	-	150	-	300	ns
	Chip select to low-Z output	tLZ, tBLZ	10	-	20	-	50	-	ns
	$\overline{OE}$ & $\overline{LB}$ , $\overline{UB}$ to low-Z output	tOLZ	5	-	20	-	30	-	ns
	Chip disable to high-Z output	tHZ	0	30	0	40	0	60	ns
	$\overline{OE}$ & $\overline{LB}$ , $\overline{UB}$ disable to high-Z	tOHZ, tBHZ	0	30	0	40	0	60	ns
Output hold from address change	tOH	15	-	15	-	30	-	ns	
Write	Write cycle time	tWC	100	-	150	-	300	-	ns
	Chip select to end of write	tCW	80	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	80	-	120	-	300	-	ns
	Write pulse width	tWP	70	-	100	-	200	-	ns
	$\overline{UB}$ , $\overline{LB}$ Valid to End of Write	tBW	80	-	120	-	300	-	ns
	Write recovery	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	30	0	40	0	60	ns
	Data to write time overlap	tDW	40	-	60	-	120	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	20	-	ns

## DATA RETENTION CHARACTERISTICS

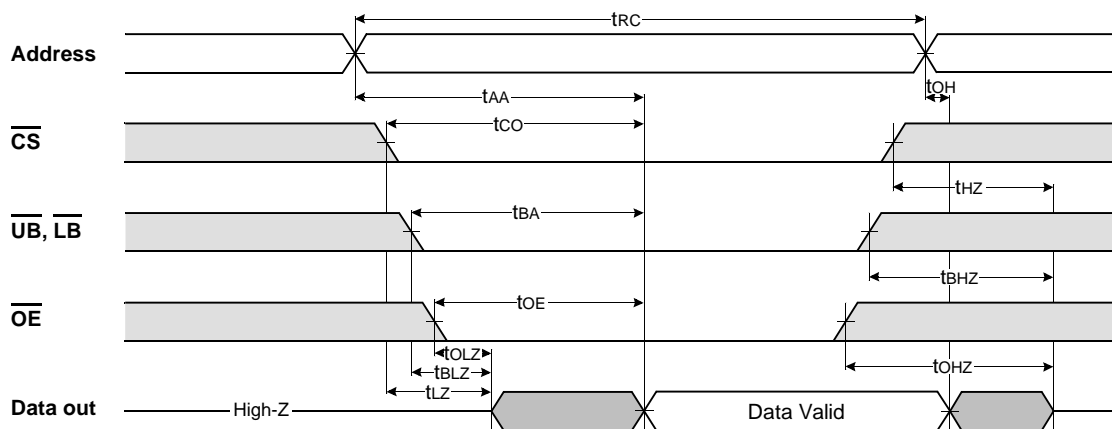
Item	Symbol	Test Condition <sup>1)</sup>	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS} \geq V_{cc} - 0.2V$	1.5	-	3.6	V
Data retention current	IDR	Vcc=3.0V, $\overline{CS} \geq V_{cc} - 0.2V$	-	-	5	μA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	trDR		tRC	-	-	

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or  $\overline{LB}=V_{IL}$ )



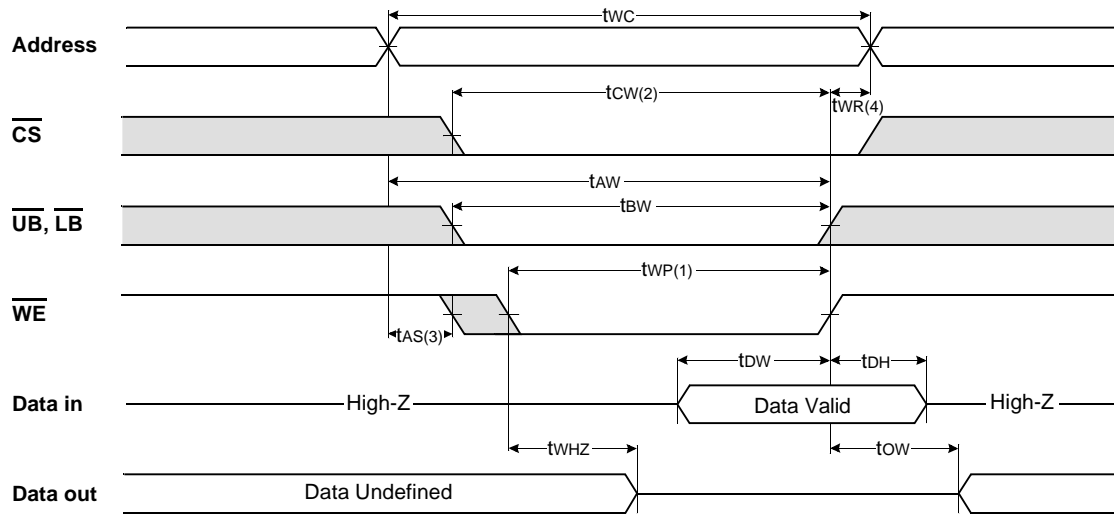
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



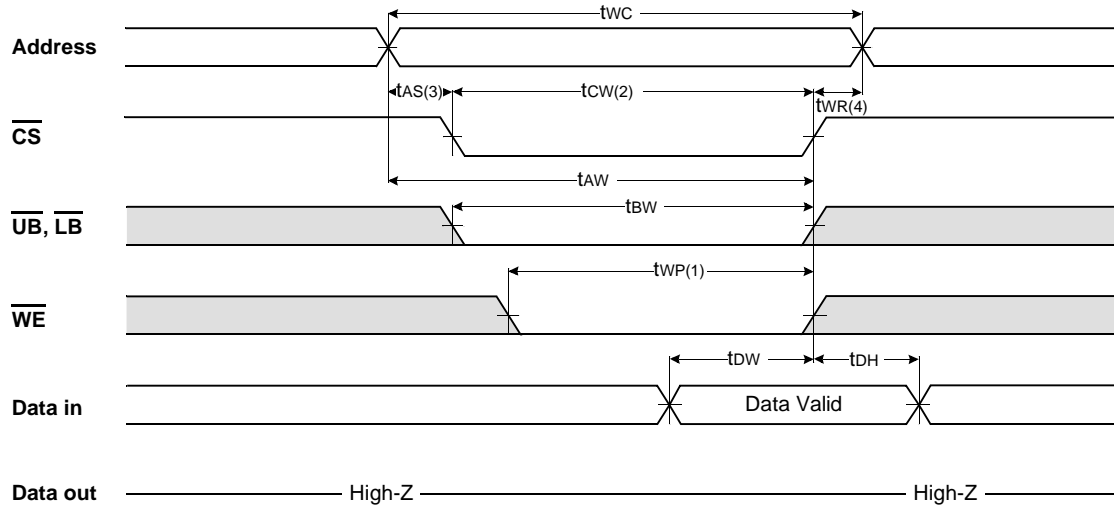
### NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

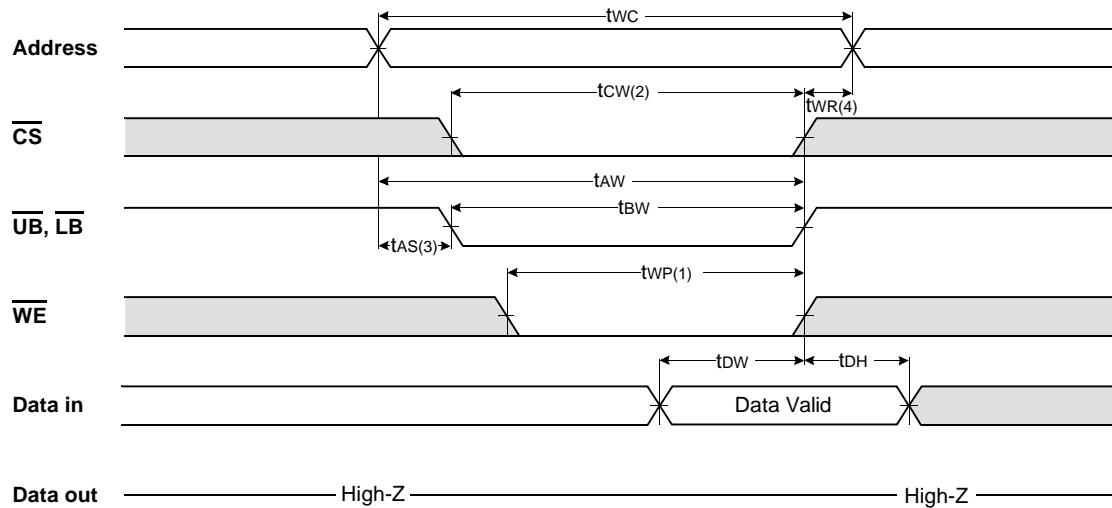
**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}$  Controlled)**



## TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{UB}$ , $\overline{LB}$ Controlled)

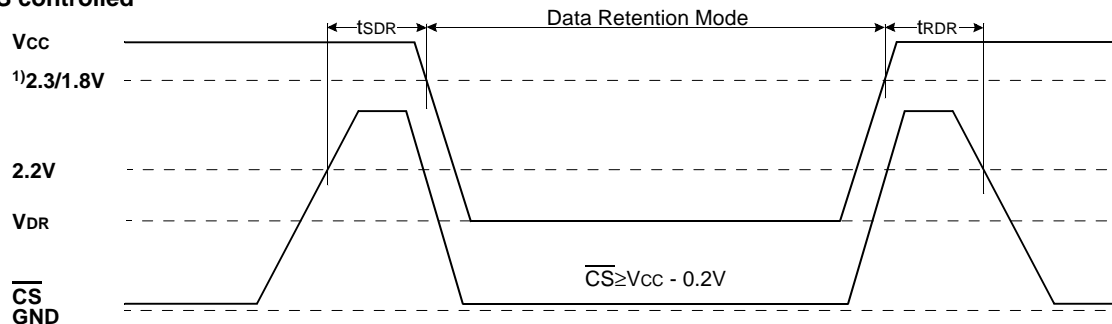


### NOTES (WRITE CYCLE)

1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.

## DATA RETENTION WAVE FORM

### $\overline{CS}$ controlled

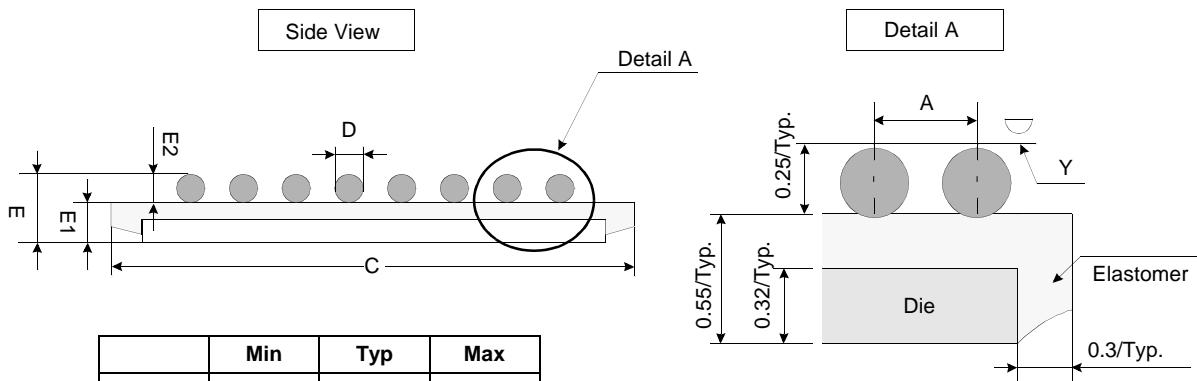
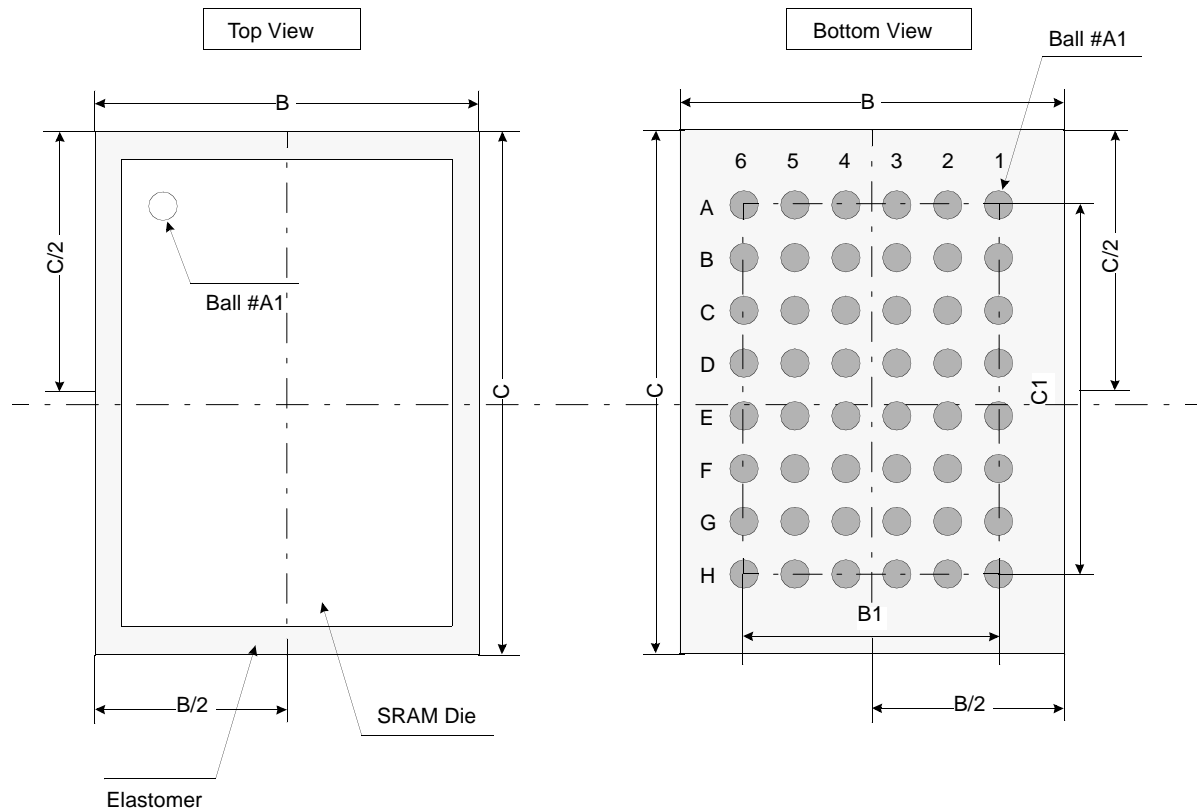


1. KM616FS1010L=2.3V, KM616FR1010L=1.8V



## PACKAGE DIMENSIONS

Unit : millimeter(inch)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08

### Notes.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)