

**Document Title**

**128Kx16 Super Low Power and Low Voltage  
Full CMOS SRAM Data Sheets for 48-CSP**

**Revision History**

| <b><u>Revision No.</u></b> | <b><u>History</u></b>   | <b><u>Draft Data</u></b> | <b><u>Remark</u></b> |
|----------------------------|---|--------------------------|----------------------|
| 0.0                        | Initialize<br>- Package dimension finalized   | February. 4, 1997        | Preliminary          |
| 0.1                        | Revised<br>- Change speed marking method<br>Marking was indicate speed at high power, that change to speed at low power | April. 17, 1997          | Preliminary          |
| 0.2                        | Revised<br>- Remove commercial products.  | August 17, 1998          | Preliminary          |

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## 128Kx16bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Scale Package)

### FEATURES SUMMARY

- Process Technology : Full CMOS
- Organization : 128Kx16
- Power Supply Voltage
  - KM616FS2000Z Family : 2.3V(Min) ~ 3.3V(Max)
  - KM616FR2000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

### GENERAL DESCRIPTION

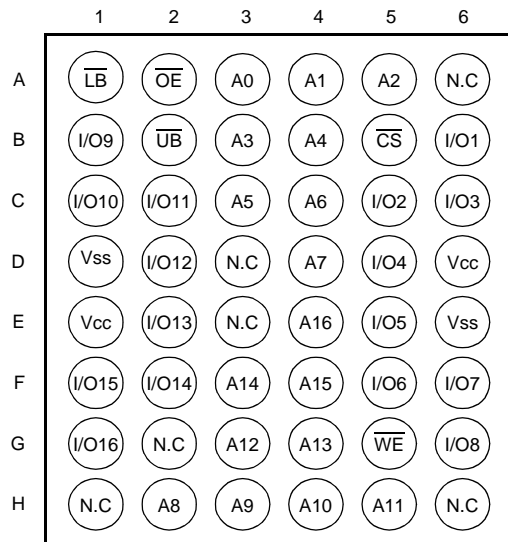
The KM616FS2000Z and KM616FR2000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family support various operating temperature ranges and has very small size with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed(ns)  | Power Dissipation   |                       | PKG Type   |
|----------------|-----------------------|-----------|--|---------------------|-----------------------|--|
|                |                       |           |  | Standby (Isb1, Max) | Operating (Icc2, Max) |  |
| KM616FS2000ZI  | Industrial(-40~85°C)  | 2.3~3.3V  | 100 <sup>1)</sup> @Vcc=3.0±0.3V<br>150 <sup>1)</sup> @Vcc=2.5±0.2V | 10µA                | 80mA<br>50mA          | 48-CSP<br>(6x8 ball area with 0.75mm ball pitch) |
| KM616FR2000ZI  |                       | 1.8~2.7V  | 300 <sup>1)</sup> @Vcc=2.0±0.2V                                    |                     | 25mA                  |  |

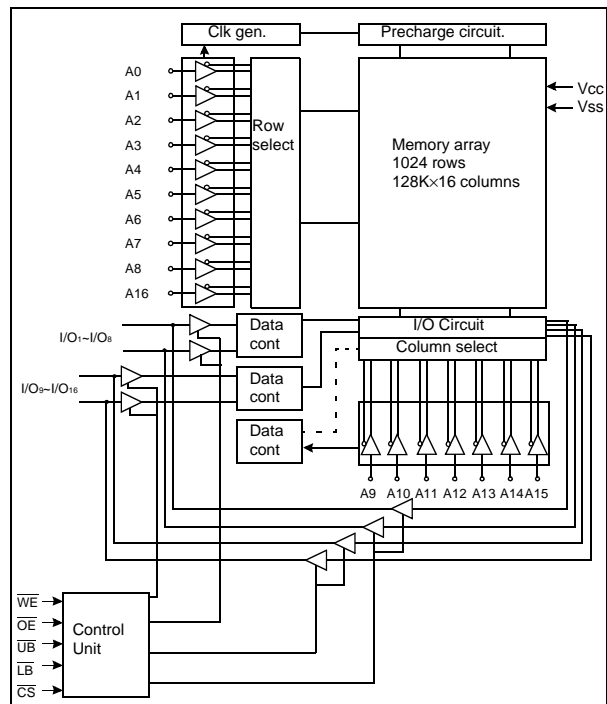
1. The parameter is measured with 30pF test load.

### 48-CSP PIN TOP VIEW



| Name            | Function                  | Name            | Function              |
|-----------------|---------------------------|-----------------|-----------------------|
| $\overline{CS}$ | Chip Select Input         | $\overline{LB}$ | Lower Byte(I/O1 ~ 8)  |
| $\overline{OE}$ | Output Enable Input Input | $\overline{UB}$ | Upper Byte(I/O9 ~ 16) |
| $\overline{WE}$ | Write Enable Input        | Vcc             | Power                 |
| A0~A16          | Address Inputs            | Vss             | Ground                |
| I/O1~I/O16      | Data Inputs/Outputs       | N.C.            | No Connection         |

### FUNCTIONAL BLOCK DIAGRAM



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# KM616FS2000Z, KM616FR2000Z Family

**Preliminary**  
**CMOS SRAM**

## PRODUCT LIST

| Industrial Temperature Products(-40~85°C) |                              |
|---|------------------------------|
| Part Name                                 | Function                     |
| KM616FS2000Z-15L                          | 48-CSP, 2.5V/3.0V, 150/100ns |
| KM616FR2000Z-30L                          | 48-CSP, 1.8V/2.5V, 300ns     |

1. The meaning of 2.5V/3.0V, 150/100ns is that the operating Vcc is ranged from 2.3V(Min) to 3.3V(Max) with speed 150ns @2.5V±0.2 and 100ns @3.0V±0.3. This type of meaning is applied to other notations like the example.
2. But in case of KM616FR2000Z-30, there is only one speed bin, 300ns though it supports wide range operating Vcc.

## FUNCTIONAL DESCRIPTION

| CS | LB              | UB              | WE              | OE              | I/O <sub>1~8</sub> | I/O <sub>9~16</sub> | Mode           | Power   |
|----|-----------------|-----------------|-----------------|-----------------|--------------------|---------------------|----------------|---------|
| H  | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | High-Z             | High-Z              | Not Select     | Standby |
| L  | X <sup>1)</sup> | X <sup>1)</sup> | H               | H               | High-Z             | High-Z              | Output Disable | Active  |
| L  | H               | H               | X <sup>1)</sup> | X <sup>1)</sup> | High-Z             | High-Z              | Output Disable |         |
| L  | L               | H               | H               | L               | Dout               | High-Z              | Read           | Active  |
| L  | H               | L               | H               | L               | High-Z             | Dout                | Read           |         |
| L  | L               | L               | H               | L               | Dout               | Dout                | Read           |         |
| L  | L               | H               | L               | X <sup>1)</sup> | Din                | High                | Write          | Active  |
| L  | H               | L               | L               | X <sup>1)</sup> | High-Z             | Din                 | Write          |         |
| L  | L               | L               | L               | X <sup>1)</sup> | Din                | Din                 | Write          |         |

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

| Item                                  | Symbol                             | Ratings                | Unit | Remark                       |
|---------------------------------------|------------------------------------|------------------------|------|------------------------------|
| Voltage on any pin relative to Vss    | V <sub>IN</sub> , V <sub>OUT</sub> | -0.2 to 3.6V           | V    | -                            |
| Voltage on Vcc supply relative to Vss | V <sub>CC</sub>                    | -0.2 to 4.0V           | V    | -                            |
| Power Dissipation                     | P <sub>D</sub>                     | 1.0                    | W    | -                            |
| Storage temperature                   | T <sub>STG</sub>                   | -55 to 150             | °C   | -                            |
| Operating Temperature                 | T <sub>A</sub>                     | -40 to 85              | °C   | KM616FS2000ZI, KM616FR2000ZI |
| Soldering temperature and time        | T <sub>SOLDER</sub>                | 260°C, 5sec(Lead Only) | -    | -                            |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# KM616FS2000Z, KM616FR2000Z Family

**Preliminary**  
**CMOS SRAM**

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

| Item               | Symbol          | Product             |                           | Min                | Typ <sup>2)</sup> | Max                                | Unit |
|--------------------|-----------------|---------------------|---------------------------|--------------------|-------------------|------------------------------------|------|
| Supply voltage     | V <sub>CC</sub> | KM616FS2000Z Family |                           | 2.3                | 2.5/3.0           | 3.3                                | V    |
|                    |                 | KM616FR2000Z Family |                           | 1.8                | 2.0/2.5           | 2.7                                | V    |
| Ground             | V <sub>SS</sub> | All Family          |                           | 0                  | 0                 | 0                                  | V    |
| Input high voltage | V <sub>IH</sub> | KM616FS2000Z Family | V <sub>CC</sub> =3.0±0.2V | 2.2                | -                 | V <sub>CC</sub> +0.2 <sup>2)</sup> | V    |
|                    |                 |                     | V <sub>CC</sub> =2.5±0.2V | 2.0                | -                 | V <sub>CC</sub> +0.2 <sup>2)</sup> | V    |
|                    |                 | KM616FR2000Z Family | V <sub>CC</sub> =2.5±0.2V | 2.0                | -                 | V <sub>CC</sub> +0.2 <sup>2)</sup> | V    |
|                    |                 |                     | V <sub>CC</sub> =2.0±0.2V | 1.6                | -                 | V <sub>CC</sub> +0.2 <sup>2)</sup> | V    |
| Input low voltage  | V <sub>IL</sub> | All Family          |                           | -0.2 <sup>3)</sup> | -                 | 0.4                                | V    |

1. T<sub>A</sub>=-40 to 85°C, unless otherwise specified

2. Overshoot : V<sub>CC</sub> + 1.0V in case of pulse width ≤20ns

3. Undershoot : -1.0V in case of pulse width ≤20ns

4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

| Item                     | Symbol          | Test Condition      | Min | Max | Unit |
|--------------------------|-----------------|---------------------|-----|-----|------|
| Input capacitance        | C <sub>IN</sub> | V <sub>IN</sub> =0V | -   | 8   | pF   |
| Input/Output capacitance | C <sub>IO</sub> | V <sub>IO</sub> =0V | -   | 10  | pF   |

1. Capacitance is sampled not, 100% tested

## DC AND OPERATING CHARACTERISTICS

| Item                           | Symbol           | Test Conditions   |                                  | Min | Typ | Max              | Unit |
|--------------------------------|------------------|---|----------------------------------|-----|-----|------------------|------|
| Input leakage current          | I <sub>LI</sub>  | V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>   |                                  | -1  | -   | 1                | μA   |
| Output leakage current         | I <sub>LO</sub>  | $\overline{CS}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>              |                                  | -1  | -   | 1                | μA   |
| Operating power supply current | I <sub>CC</sub>  | I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , Read                     |                                  | -   | -   | 10               | mA   |
|                                |                  |   |                                  | -   | -   | 25               |      |
| Average operating current      | I <sub>CC1</sub> | Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}$ ≤0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V | Read                             | -   | -   | 10               | mA   |
|                                |                  |   | Write                            | -   | -   | 25               |      |
|                                | I <sub>CC2</sub> | Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> | V <sub>CC</sub> =3.3V@100ns      | -   | -   | 80               | mA   |
|                                |                  |   | V <sub>CC</sub> =2.7V@150ns      | -   | -   | 50               |      |
|                                |                  |   | V <sub>CC</sub> =2.2V@300ns      | -   | -   | 25               |      |
| Output low voltage             | V <sub>OL</sub>  | I <sub>OL</sub>   | 2.1mA at V <sub>CC</sub> =3.0V   | -   | -   | 0.4              | V    |
|                                |                  |   | 0.5mA at V <sub>CC</sub> =2.5V   | -   | -   | 0.4              |      |
|                                |                  |   | 0.33mA at V <sub>CC</sub> =2.0V  | -   | -   | 0.4              |      |
| Output high voltage            | V <sub>OH</sub>  | I <sub>OH</sub>   | -1.0mA at V <sub>CC</sub> =3.0V  | 2.4 | -   | -                | V    |
|                                |                  |   | -0.5mA at V <sub>CC</sub> =2.5V  | 2.0 | -   | -                |      |
|                                |                  |   | -0.44mA at V <sub>CC</sub> =2.0V | 1.6 | -   | -                |      |
| Standby Current(TTL)           | I <sub>SB</sub>  | $\overline{CS}$ =V <sub>IH</sub> , Other inputs=V <sub>IL</sub> or V <sub>IH</sub>  |                                  | -   | -   | 0.3              | mA   |
| Standby Current (CMOS)         | I <sub>SB1</sub> | $\overline{CS}$ ≥V <sub>CC</sub> -0.2V, Other inputs=0~V <sub>CC</sub>  |                                  | -   | 0.1 | 10 <sup>1)</sup> | μA   |

1. Super low power product=2μA with special handling.

## AC OPERATING CONDITIONS

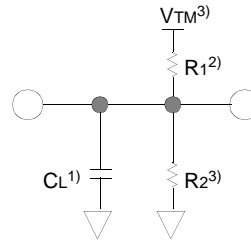
### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V to  $V_{CC}=3.0/2.5V$   
0.4 to 1.8V to  $V_{CC}=2.0V$

Input rising and falling time : 5ns

Input and output reference voltage : 1.5V to  $V_{CC}=3.0V$ ,  
1.1V to  $V_{CC}=2.5V$ ,  
0.9V to  $V_{CC}=2.0V$

Output load (see right) :  $C_L=30pF/100pF$



1. Including scope and jig capacitance
2.  $R_1=3070\Omega$ ,  $R_2=3150\Omega$
3.  $V_{TM}=2.8V$  for  $V_{CC}=3.0V$   
2.3V for  $V_{CC}=2.5V$   
1.8V for  $V_{CC}=2.0V$

## AC CHARACTERISTICS ( $T_A=-40$ to $85^\circ C$ , KM616FS2000 Family: $V_{CC}=2.3\sim 3.3V$ , KM616FR2000 Family: $V_{CC}=1.8\sim 2.7V$ )

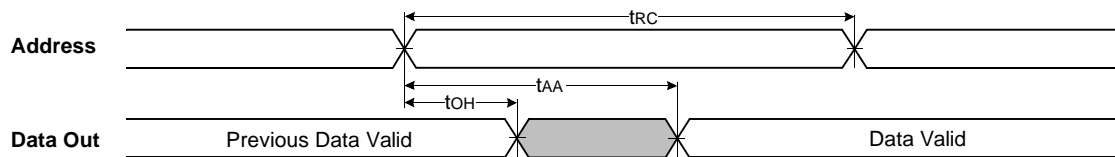
| Parameter List |   | Symbol                    | Speed Bins |     |      |     |       |     |       |     |       |     |       |     | Units |
|----------------|---|---------------------------|------------|-----|------|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|
|                |   |                           | 70ns       |     | 85ns |     | 100ns |     | 120ns |     | 150ns |     | 300ns |     |       |
|                |   |                           | Min        | Max | Min  | Max | Min   | Max | Min   | Max | Min   | Max | Min   | Max |       |
| Read           | Read cycle time   | tRC                       | 70         | -   | 85   | -   | 100   | -   | 120   | -   | 150   | -   | 300   | -   | ns    |
|                | Address access time   | tAA                       | -          | 70  | -    | 85  | -     | 100 | -     | 120 | -     | 150 | -     | 300 | ns    |
|                | Chip select to output   | tCO1                      | -          | 70  | -    | 85  | -     | 100 | -     | 120 | -     | 150 | -     | 300 | ns    |
|                | Output enable to valid output   | tOE                       | -          | 35  | -    | 45  | -     | 50  | -     | 60  | -     | 75  | -     | 150 | ns    |
|                | $\overline{UB}$ , $\overline{LB}$ Access Time                         | tBA                       | -          | 35  | -    | 45  | -     | 50  | -     | 60  | -     | 75  | -     | 150 | ns    |
|                | Chip select to low-Z output   | tLZ                       | 10         | -   | 10   | -   | 10    | -   | 20    | -   | 20    | -   | 50    | -   | ns    |
|                | $\overline{OE}$ & $\overline{LB}$ , $\overline{UB}$ to low-Z output   | tOLZ, tBLZ                | 5          | -   | 5    | -   | 5     | -   | 20    | -   | 20    | -   | 30    | -   | ns    |
|                | Chip disable to high-Z output   | tHZ                       | 0          | 25  | 0    | 25  | 0     | 30  | 0     | 35  | 0     | 40  | 0     | 60  | ns    |
|                | $\overline{OE}$ & $\overline{LB}$ , $\overline{UB}$ disable to high-Z | tOHZ, tBHZ                | 0          | 25  | 0    | 25  | 0     | 30  | 0     | 35  | 0     | 40  | 0     | 60  | ns    |
|                | Output hold from address  | tOH                       | 10         | -   | 15   | -   | 15    | -   | 15    | -   | 15    | -   | 30    | -   | ns    |
| Write          | Write cycle time  | tWC                       | 70         | -   | 85   | -   | 100   | -   | 120   | -   | 150   | -   | 300   | -   | ns    |
|                | Chip select to end of write   | tCW                       | 65         | -   | 70   | -   | 80    | -   | 100   | -   | 120   | -   | 300   | -   | ns    |
|                | Address set-up time   | tAS                       | 0          | -   | 0    | -   | 0     | -   | 0     | -   | 0     | -   | 0     | -   | ns    |
|                | Address valid to end of write   | tAW                       | 65         | -   | 70   | -   | 80    | -   | 100   | -   | 120   | -   | 300   | -   | ns    |
|                | Write pulse width   | tWP                       | 55         | -   | 60   | -   | 70    | -   | 80    | -   | 100   | -   | 200   | -   | ns    |
|                | $\overline{UB}$ , $\overline{LB}$ Valid to End of Write               | tBW                       | 65         | -   | 70   | -   | 80    | -   | 100   | -   | 120   | -   | 300   | -   | ns    |
|                | Write recovery  | tWR                       | 0          | -   | 0    | -   | 0     | -   | 0     | -   | 0     | -   | 0     | -   | ns    |
|                | Write to output high-Z  | tWHZ                      | 0          | 25  | 0    | 25  | 0     | 30  | 0     | 35  | 0     | 40  | 0     | 60  | ns    |
|                | Data to write time overlap  | tdW                       | 30         | -   | 35   | -   | 40    | -   | 50    | -   | 60    | -   | 120   | -   | ns    |
|                | Data hold from write time   | tdH                       | 0          | -   | 0    | -   | 0     | -   | 0     | -   | 0     | -   | 0     | -   | ns    |
|                |   | End write to output low-Z | tOW        | 5   | -    | 5   | -     | 5   | -     | 5   | -     | 5   | -     | 20  | -     |

## DATA RETENTION CHARACTERISTICS

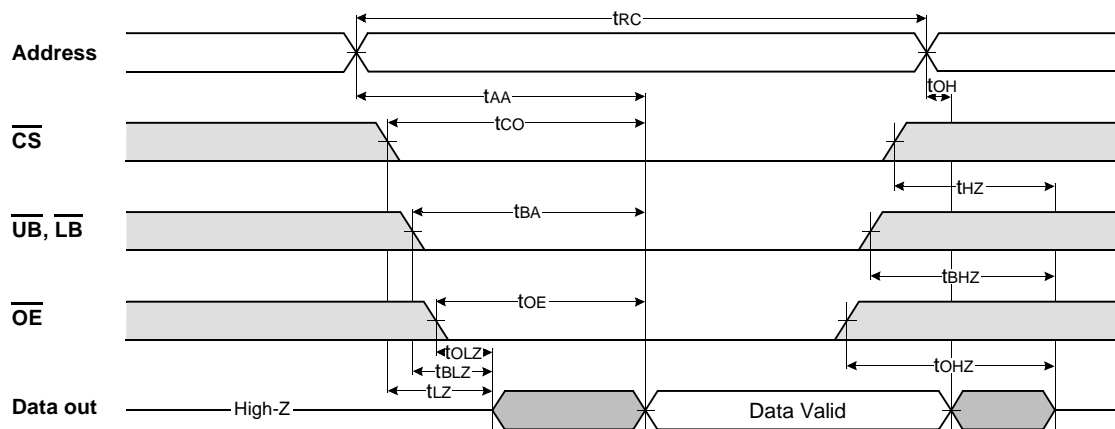
| Item                        | Symbol    | Test Condition                                 | Min      | Typ | Max | Unit    |
|-----------------------------|-----------|--|----------|-----|-----|---------|
| $V_{CC}$ for data retention | $V_{DR}$  | $\overline{CS} \geq V_{CC}-0.2V$               | 1.5      | -   | 3.6 | V       |
| Data retention current      | $I_{DR}$  | $V_{CC}=3.0V$ $\overline{CS} \geq V_{CC}-0.2V$ | -        | 0.1 | 5   | $\mu A$ |
| Data retention set-up time  | $t_{SDR}$ | See data retention waveform                    | 0        | -   | -   | ns      |
| Recovery time               | $t_{RDR}$ |  | $t_{RC}$ | -   | -   |         |

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or  $\overline{LB}=V_{IL}$ )



**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



### NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

The diagram illustrates the timing relationships for the 28C02 EPROM. The signals shown are Address, CS (Chip Select), UB and LB (Byte Enable), WE (Write Enable), Data in, and Data out. The timing parameters are defined as follows:

- Address:** The duration of the address signal is  $t_{WC}$ .
- CS:** The setup time before CS is  $t_{AS}(3)$ , the pulse width is  $t_{CW}(2)$ , and the recovery time after CS is  $t_{WR1}(4)$ .
- UB, LB:** The setup time before the data bus is  $t_{AW}$ , and the hold time after the data bus is  $t_{BW}$ .
- WE:** The pulse width of the write enable signal is  $t_{WP}(1)$ .
- Data in:** The data is valid for a duration of  $t_{DW}$  (Data Valid).
- Data out:** The data output is in a High-Z state during the  $t_{DH}$  (Data Hold) period.

The diagram illustrates the timing requirements for the 74VHC0404. The signals shown are Address, CS (Chip Select), UB and LB (Bank/Bit Selects), WE (Write Enable), Data in, and Data out. The timing parameters are defined as follows:

- $t_{WC}$ : Write Cycle time, from the start of the write command to the end of the write recovery.
- $t_{CW(2)}$ : Write Command time, from the start of the write command to the start of the write recovery.
- $t_{WR1(4)}$ : Write Recovery time, from the end of the write command to the start of the next read command.
- $t_{AW}$ : Access Write time, from the start of the write command to the start of the next read command.
- $t_{BW}$ : Burst Write time, from the start of the write command to the start of the next read command.
- $t_{AS(3)}$ : Access Setup time, from the start of the write command to the start of the next read command.
- $t_{WP(1)}$ : Write Pulse time, from the start of the write command to the start of the next read command.
- $t_{DW}$ : Data Valid time, from the start of the write command to the start of the next read command.
- $t_{DH}$ : Data Hold time, from the end of the write command to the start of the next read command.

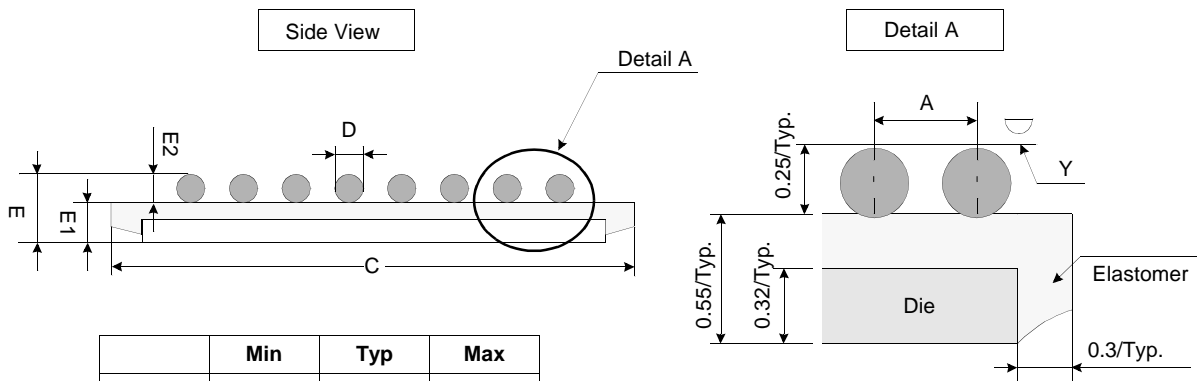
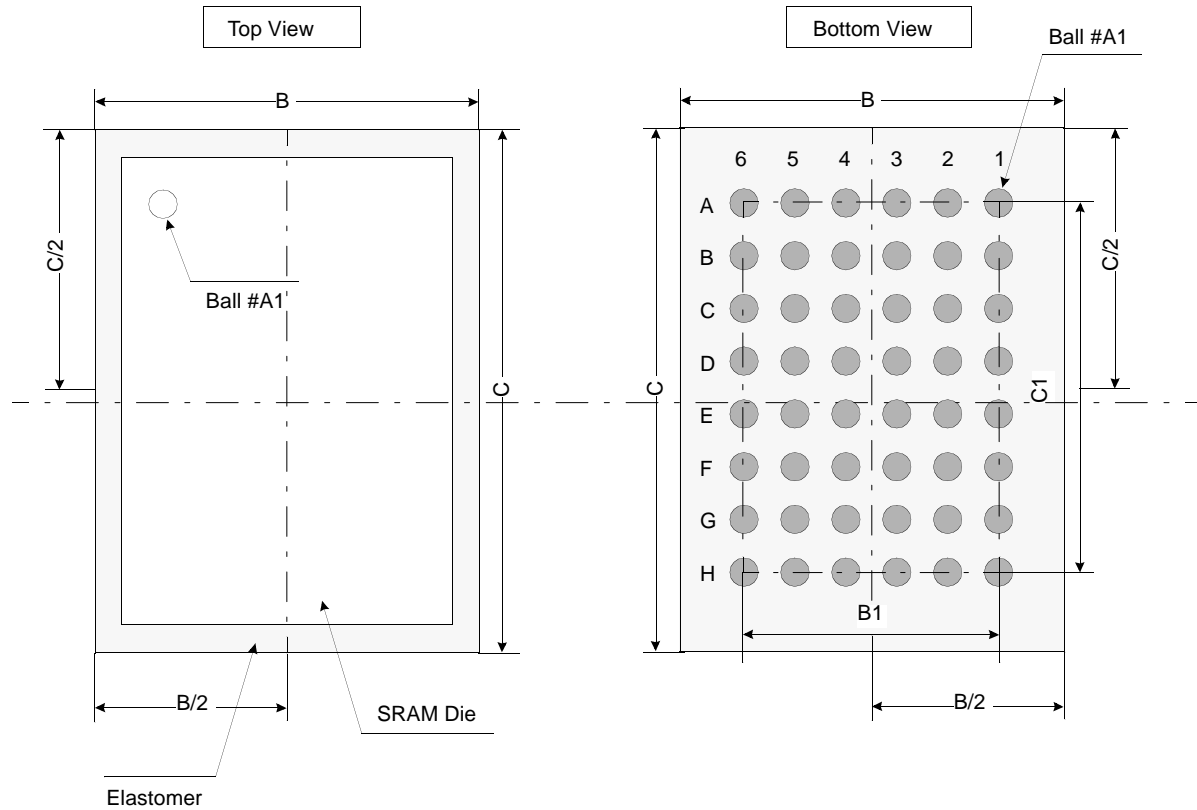
1. A **write** occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.

The diagram illustrates the timing for Data Retention Mode. It shows three signals: VCC, CS (Chip Select), and VDR (Data Retention Voltage). The VCC signal transitions between 3.3V, 3.0V, 2.7V, 2.3V, and 1.8V. The CS signal is active-low, indicated by a bar over the label. The VDR signal is shown as a trapezoidal pulse that ramps up when CS is active and ramps down when CS is inactive. The time interval for the VDR signal to ramp up is labeled t<sub>SDR</sub> (Setup Delay), and the time interval for it to ramp down is labeled t<sub>RDR</sub> (Release Delay). The VDR signal is maintained at a level greater than or equal to VCC - 0.2V during the Data Retention Mode. The diagram is labeled "Data Retention Mode" at the top.



## PACKAGE DIMENSIONS

Unit : millimeter(inch)



|    | Min   | Typ   | Max   |
|----|-------|-------|-------|
| A  | -     | 0.75  | -     |
| B  | 6.10  | 6.20  | 6.30  |
| B1 | -     | 3.75  | -     |
| C  | 13.65 | 13.75 | 13.85 |
| C1 | -     | 5.25  | -     |
| D  | 0.30  | 0.35  | 0.40  |
| E  | -     | 0.80  | 0.81  |
| E1 | -     | 0.55  | -     |
| E2 | -     | 0.25  | -     |
| Y  | -     | -     | 0.08  |

### Notes.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)