

**Document Title****128K x16 bit Super Low Power and Low Voltage Full CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Date</u></b>	<b><u>Remark</u></b>
0.0	Initial Draft	October 23, 1998	Preliminary
1.0	Finalize	December 9, 1998	Final
2.0	Revise - Change V <sub>DR</sub> =1.0 to 1.5V - Change I <sub>DR</sub> test condition ; V <sub>CC</sub> =1.2 to 1.5V	May 12, 1999	Final

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## 128K x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

### FEATURES

- Process Technology: Full CMOS
- Organization: 128K x16 bit
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 44-TSOP2-400F

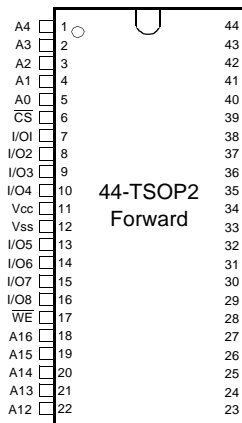
### GENERAL DESCRIPTION

The KM616FU2000A families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support various operating temperature ranges for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

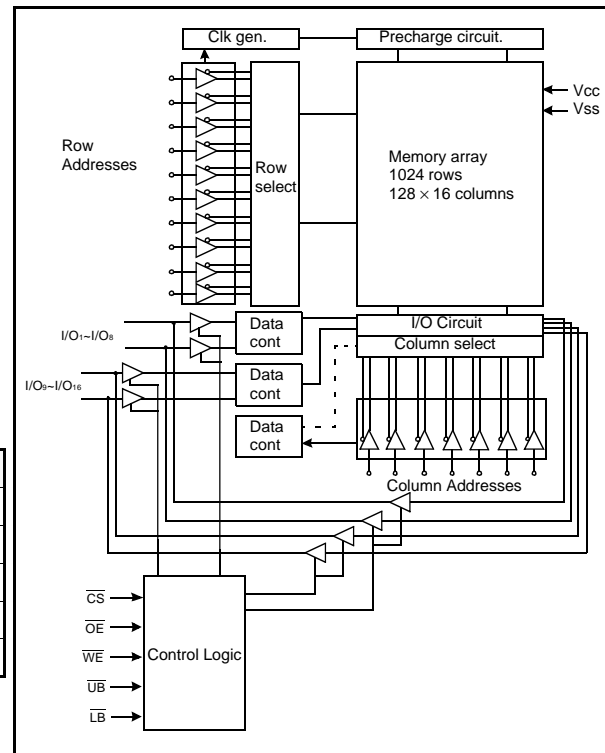
Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc1, Max)	
KM616FU2000A	Industrial(-40~85°C)	2.7 ~ 3.3V	70/100	10µA	5mA	44-TSOP2-F

### PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
A0~A16	Address Inputs	$\overline{LB}$	Lower Byte(I/O1~8)
I/O1~I/O16	Data Inputs/Outputs	N.C.	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
KM616FU2000ATI-7	44-TSOP2-F, 70ns, 3.0V, Low Low Power
KM616FU2000ATI-10	44-TSOP2-F, 100ns, 3.0V, Low Low Power

## FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O <sub>1-8</sub>	I/O <sub>9-16</sub>	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselected	Standby
L	H	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Output Disabled	Active
L	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X <sup>1)</sup>	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X <sup>1)</sup>	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X <sup>1)</sup>	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to 3.6V	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.2 to 4.0V	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage temperature	T <sub>STG</sub>	-55 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.3	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.2 <sup>3)</sup>	-	0.6	V

Note :

1. T<sub>A</sub>=-40 to 85°C, otherwise specified
2. Overshoot: V<sub>CC</sub>+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Output leakage current	I <sub>LO</sub>	$\overline{CS}$ =V <sub>IH</sub> or $\overline{OE}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	2	mA
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}$ ≤0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	5	mA
	I <sub>CC2</sub>	Cycle time=Min, I <sub>IO</sub> =0mA, 100% duty, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	35	mA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	-	-	0.4	V
Output high voltage	V <sub>OH</sub>	I <sub>OL</sub> = -1.0mA	2.2	-	-	V
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}$ =V <sub>IH</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.3	mA
Standby Current (CMOS)	I <sub>SB1</sub>	$\overline{CS}$ ≥V <sub>CC</sub> -0.2V, Other inputs=0~V <sub>CC</sub>	-	0.5	10	μA

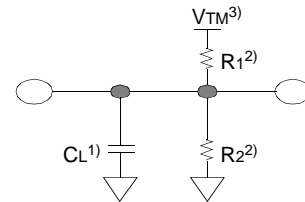
## AC OPERATING CONDITIONS

## TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load (See right):  $C_L = 100\text{pF} + 1\text{TTL}$ 

1. Including scope and jig capacitance

2.  $R_1 = 3070\Omega$ ,  $R_2 = 3150\Omega$ 3.  $V_{TM} = 2.8\text{V}$ AC CHARACTERISTICS ( $V_{CC} = 2.7 \sim 3.3\text{V}$ ,  $T_A = -40 \sim 85^\circ\text{C}$ )

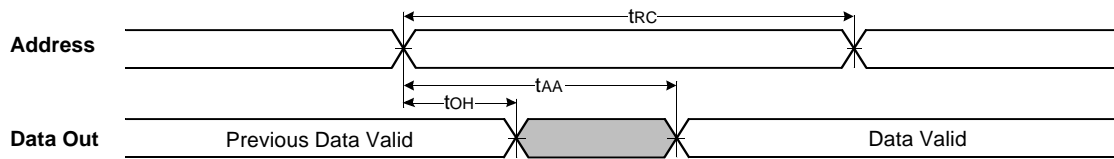
Parameter List		Symbol	Speed Bins				Units
			70ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	70	-	100	-	ns
	Address access time	t <sub>AA</sub>	-	70	-	100	ns
	Chip select to output	t <sub>CO</sub>	-	70	-	100	ns
	Output enable to valid output	t <sub>OE</sub>	-	35	-	50	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Access Time	t <sub>BA</sub>	-	35	-	50	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ enable to low-Z output	t <sub>BLZ</sub>	5	-	5	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	25	0	30	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ disable to high-Z output	t <sub>BHZ</sub>	0	25	0	30	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	25	0	30	ns
	Output hold from address change	t <sub>OH</sub>	10	-	15	-	ns
Write	Write cycle time	t <sub>WC</sub>	70	-	100	-	ns
	Chip select to end of write	t <sub>CW</sub>	60	-	80	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	60	-	80	-	ns
	$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Valid to End of Write	t <sub>BW</sub>	60	-	80	-	ns
	Write pulse width	t <sub>WP</sub>	55	-	70	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	25	0	30	ns
	Data to write time overlap	t <sub>DW</sub>	30	-	40	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	ns

## DATA RETENTION CHARACTERISTICS

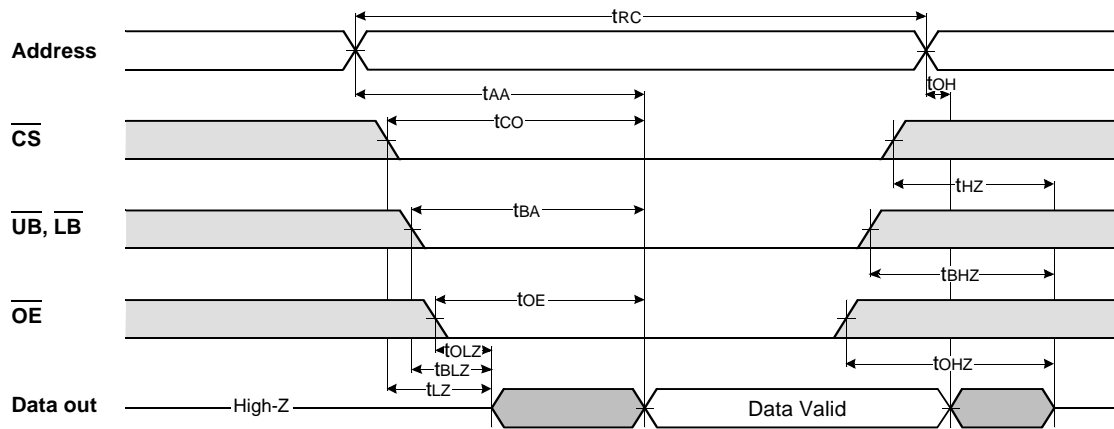
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	VDR	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$	1.5	-	3.3	V
Data retention current	IDR	$V_{CC} = 1.5\text{V}$ , $\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$	-	1	3	$\mu\text{A}$
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ns
Recovery time	t <sub>RDR</sub>		t <sub>RC</sub>	-	-	

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$  or/and  $\overline{LB}=V_{IL}$ )



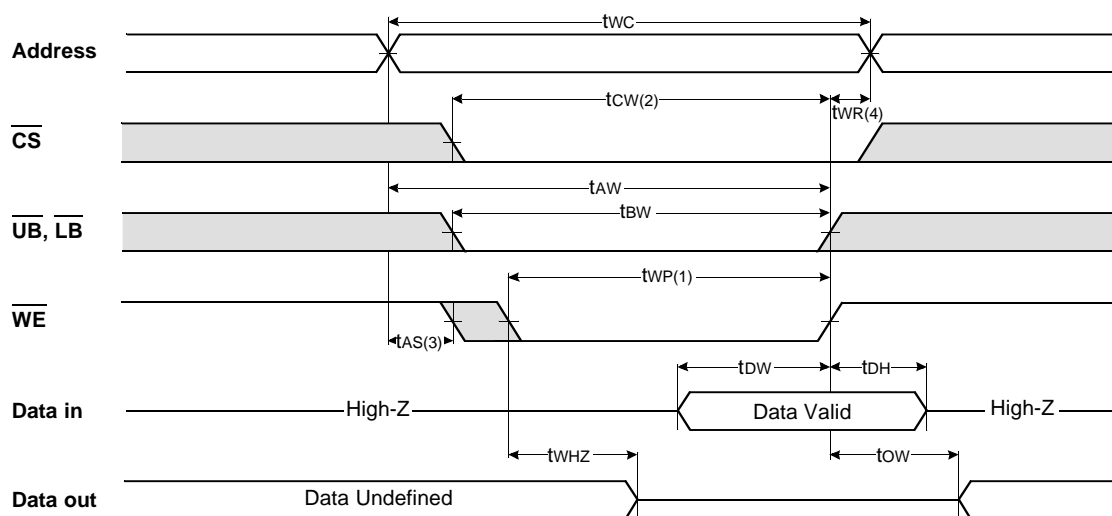
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



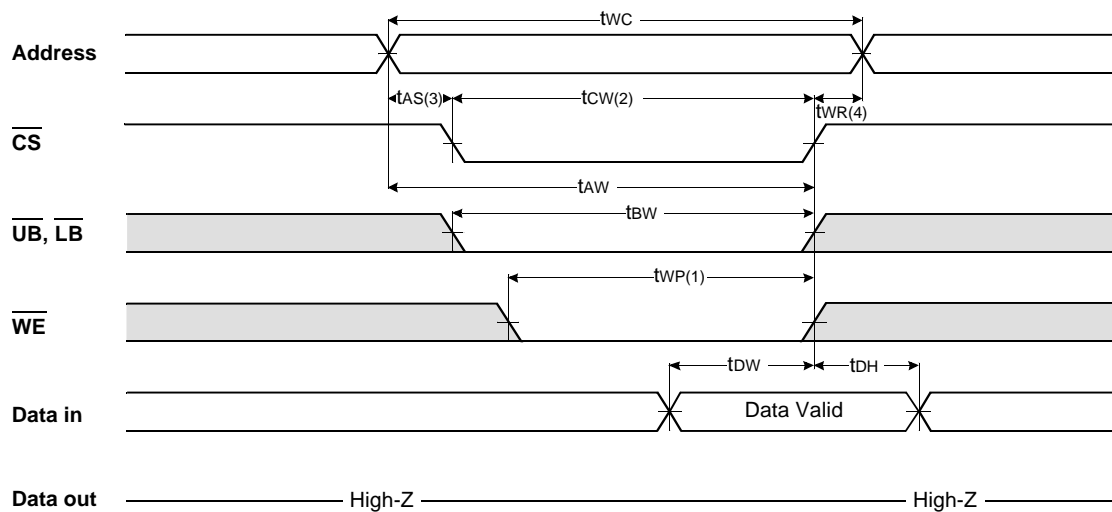
### NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

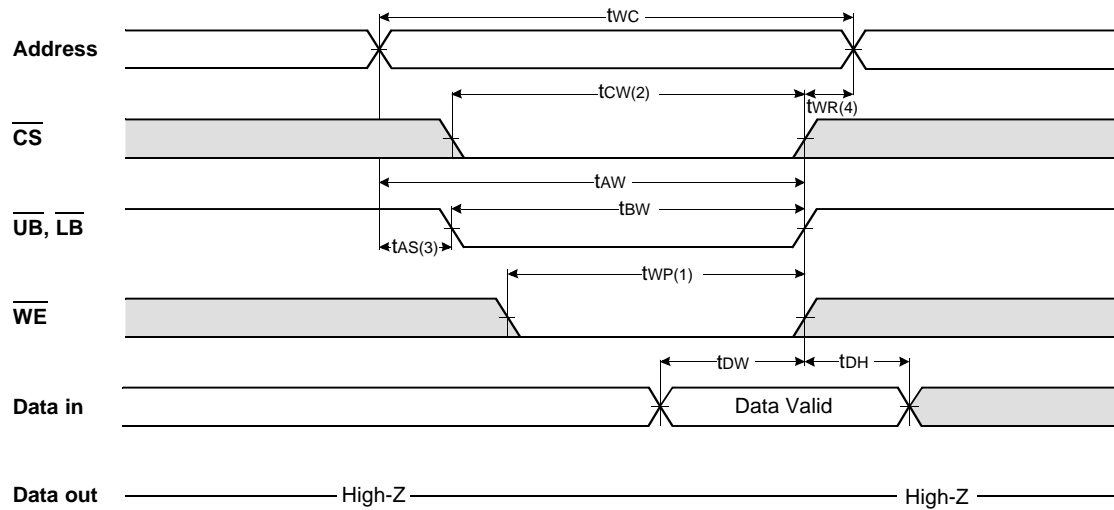
**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}$  Controlled)**



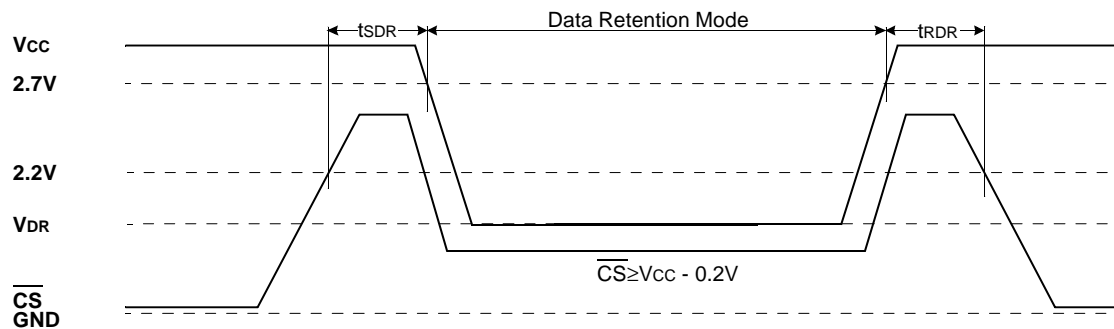
## TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{UB}$ , $\overline{LB}$ Controlled)



### NOTES (WRITE CYCLE)

1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.

## DATA RETENTION WAVE FORM





## Unit : millimeter(inch)

Top View Dimensions:

- Overall Width:  $18.81 \pm 0.741$  MAX.
- Overall Height:  $11.76 \pm 0.20$  /  $0.463 \pm 0.008$
- Pin Pitch:  $0.80 \pm 0.0315$
- Pin Diameter:  $0.805 \pm 0.032$
- Pin Spacing:  $0.35 \pm 0.10$  /  $0.014 \pm 0.004$

Side View Dimensions:

- Pin Height:  $0.50 \pm 0.020$
- Shell Thickness:  $0.10 \pm 0.004$  MAX.
- Pin Length:  $0.45 \pm 0.018$  /  $0.030$
- Pin Diameter:  $0.25 \pm 0.010$