

Document Title**64K x16 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

| <u>Revision No.</u> | <u>History</u> | <u>Draft Data</u> | <u>Remark</u> |
|----------------------------|--|--------------------------|----------------------|
| 0.0 | Design target | July 24, 1995 | Advance |
| 0.1 | Initial draft | August 12, 1995 | Preliminary |
| 1.0 | Finalize - One datasheet for commercial and industrial part and 3.0, 3.3V product. | April 13, 1996 | Final |
| 2.0 | Revised - Change datasheet format. - Remove Icc write current value. - Remove low power product from TSOP package - Remove 100ns part from KM616V1000B Family - Remove Extended product | February 25, 1998 | Final |
| 2.01 | Errata correction | August 13, 1998 | |

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64K x16 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : Poly Load
- Organization : 64K x16
- Data Byte Control : \overline{LB} =I/O_{1~8}, \overline{UB} =I/O_{9~16}
- Power Supply Voltage :
 - KM616V1000B family : 3.0~3.6V
 - KM616U1000B family : 2.7~3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type :44-TSOP2-400F/R

GENERAL DESCRIPTION

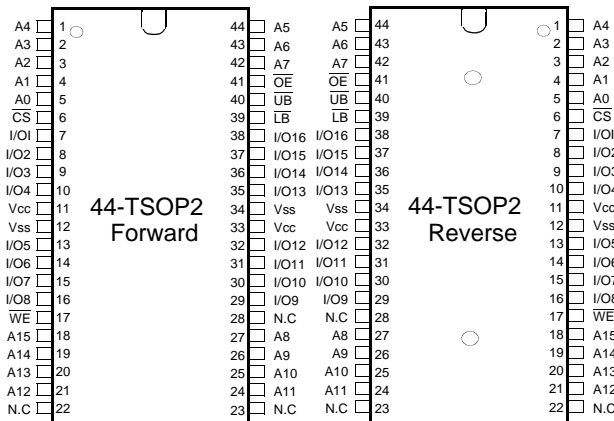
The KM616V1000B and KM616U1000B families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have small package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed(ns) | Power Dissipation | | PKG Type |
|------------------------------------|-----------------------|----------------------|-------------------------|------------------------|--------------------------|-----------------------------|
| | | | | Standby (ISB1, Max) | Operating (Icc2, Max) | |
| KM616V1000BL-L KM616U1000BL-L | Commercial(0~70°C) | 3.0~3.6V 2.7~3.3V | 70 ¹⁾ 100 | 15μA 15μA | 65mA | 44-TSOP2 Forward/Reverse |
| KM616V1000BLI-L KM616U1000BLI-L | Industrial(-40~85°C) | 3.0~3.6V 2.7~3.3V | 85 ¹⁾ 100 | 20μA 20μA | | |

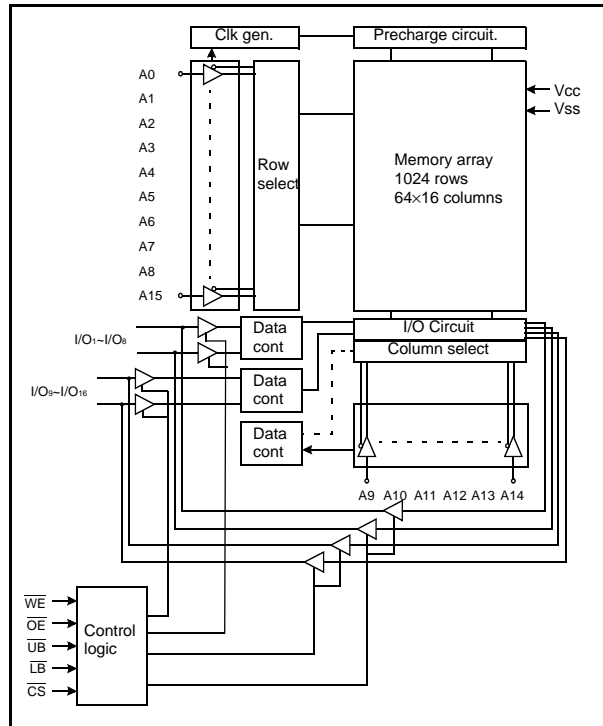
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



| Name | Function | Name | Function |
|-----------------|----------------------------------|---------------------|---------------------|
| \overline{CS} | Chip Select Input | Vcc | Power |
| \overline{OE} | Output Enable Input | Vss | Ground |
| \overline{WE} | Write Enable Input | I/O _{1~16} | Data Inputs/Outputs |
| \overline{LB} | Lower Byte (I/O _{1~8}) | A _{0~A15} | Address Inputs |
| \overline{UB} | Upper Byte(I/O _{9~16}) | N.C | No Connection |

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

| Commercial Temperature Products(0~70°C) | | Industrial Temperature Products(-40~85°C) | |
|---|-----------------------------|---|-----------------------------|
| Part Name | Function | Part Name | Function |
| KM616V1000BLT-7L | 44-TSOP-2F, 3.3V, 70ns, LL | KM616V1000BLTI-8L | 44-TSOP-2F, 3.3V, 85ns, LL |
| KM616U1000BLT-10L | 44-TSOP-2F, 3.0V, 100ns, LL | KM616U1000BLTI-10L | 44-TSOP-2F, 3.0V, 100ns, LL |
| KM616V1000BLR-7L | 44-TSOP-2R, 3.3V, 70ns, LL | KM616V1000BLRI-8L | 44-TSOP-2R, 3.3V, 85ns, LL |
| KM616U1000BLR-10L | 44-TSOP-2R, 3.0V, 100ns, LL | KM616U1000BLRI-10L | 44-TSOP-2R, 3.0V, 100ns, LL |

FUNCTIONAL DESCRIPTION

| $\overline{\text{CS}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{LB}}$ | $\overline{\text{UB}}$ | I/O ₁₋₈ | I/O ₉₋₁₆ | Mode | Power |
|------------------------|------------------------|------------------------|------------------------|------------------------|--------------------|---------------------|------------------|---------|
| H | X ¹⁾ | X ¹⁾ | X ¹⁾ | X ¹⁾ | High-Z | High-Z | Deselected | Standby |
| L | H | H | X ¹⁾ | X ¹⁾ | High-Z | High-Z | Output Disabled | Active |
| L | X ¹⁾ | X ¹⁾ | H | H | High-Z | High-Z | Output Disabled | Active |
| L | L | H | L | H | Dout | High-Z | Lower Byte Read | Active |
| L | L | H | H | L | High-Z | Dout | Upper Byte Read | Active |
| L | L | H | L | L | Dout | Dout | Word Read | Active |
| L | X ¹⁾ | L | L | H | Din | High-Z | Lower Byte Write | Active |
| L | X ¹⁾ | L | H | L | High-Z | Din | Upper Byte Write | Active |
| L | X ¹⁾ | L | L | L | Din | Din | Word Write | Active |

1. X means don't care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

| Item | Symbol | Ratings | Unit | Remark |
|---------------------------------------|------------------------------------|------------------------------|------|------------------------------------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -0.5 to V _{CC} +0.5 | V | - |
| Voltage on Vcc supply relative to Vss | V _{CC} | -0.5 to 4.6 | V | - |
| Power Dissipation | P _D | 1.0 | W | - |
| Storage temperature | T _{STG} | -65 to 150 | °C | - |
| Operating Temperature | T _A | 0 to 70 | °C | KM616V1000BL-L KM616U1000BL-L |
| | | -40 to 85 | °C | KM616V1000BLI-L KM616U1000BLI-L |
| Soldering temperature and time | T _{SOLDER} | 260°C, 10sec (Lead Only) | - | - |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

| Item | Symbol | Product | Min | Typ | Max | Unit |
|--------------------|-----------------|--|--------------------|------------|------------------------------------|------|
| Supply voltage | V _{CC} | KM616V1000B Family KM616U1000B Family | 3.0 2.7 | 3.3 3.0 | 3.6 3.3 | V |
| Ground | V _{SS} | All Family | 0 | 0 | 0 | V |
| Input high voltage | V _{IH} | KM616V1000B, KM616U1000B Family | 2.2 | - | V _{CC} +0.3 ²⁾ | V |
| Input low voltage | V _{IL} | KM616V1000B, KM616U1000B Family | -0.3 ³⁾ | - | 0.4 | V |

Note:

- Commercial Product : T_A=0 to 70°C, otherwise specified
Industrial Product : T_A=-40 to 85°C, otherwise specified
- Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
- Undershoot : -3.0V in case of pulse width ≤ 30ns
- Overshoot and undershoot are sampled, not 100% tested

CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|--------------------------|-----------------|---------------------|-----|-----|------|
| Input capacitance | C _{IN} | V _{IN} =0V | - | 6 | pF |
| Input/Output capacitance | C _{IO} | V _{IO} =0V | - | 8 | pF |

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

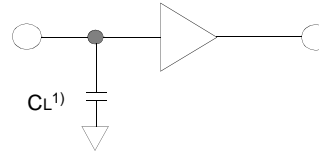
| Item | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--------------------------------|--------------------------------|--|-------|-----|------------------|------|
| Input leakage current | I _{LI} | V _{IN} =V _{SS} to V _{CC} | -1 | - | 1 | μA |
| Output leakage current | I _{LO} | \overline{CS} =V _{IH} or \overline{OE} =V _{IH} or \overline{WE} =V _{IL} , V _{IO} =V _{SS} to V _{CC} | -1 | - | 1 | μA |
| Operating power supply current | I _{CC} | I _{IO} =0mA, \overline{CS} =V _{IL} , V _{IN} =V _{IL} or V _{IH} , Read | - | - | 10 | mA |
| Average operating current | I _{CC1} ¹⁾ | Cycle time=1μs, 100% duty, I _{IO} =0mA \overline{CS} ≤0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V | Read | - | - | 15 |
| | | | Write | - | - | 40 |
| | I _{CC2} | Cycle time=Min, 100% duty, I _{IO} =0mA, \overline{CS} =V _{IL} , V _{IN} =V _{IL} or V _{IH} | - | - | 65 | mA |
| Output low voltage | V _{OL} | I _{OL} =2.1mA | - | - | 0.4 | V |
| Output high voltage | V _{OH} | I _{OH} =-1.0mA | 2.2 | - | - | V |
| Standby Current(TTL) | I _{SB} | \overline{CS} =V _{IH} , Other inputs=V _{IL} or V _{IH} | - | - | 0.5 | mA |
| Standby current(CMOS) | I _{SB1} | \overline{CS} ≥V _{CC} -0.2V, Other inputs=0-V _{CC} | - | - | 15 ²⁾ | μA |

- Industrial Product : I_{CC1}(Read/Write)=20mA/45mA
- Industrial Product=20μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V
 Input rising and falling time : 5ns
 Input and output reference voltage : 1.5V
 Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS (KM616V1000B Family : $V_{CC}=3.0\sim 3.6\text{V}$, KM616U1000B Family : $V_{CC}=2.7\sim 3.3\text{V}$ Commercial product : $T_A=0$ to 70°C , Industrial product : $T_A=-40$ to 85°C)

| Parameter List | | Symbol | Speed Bins | | | | | | Units |
|----------------|---|--------|------------|-----|------|-----|-------|-----|-------|
| | | | 70ns | | 85ns | | 100ns | | |
| | | | Min | Max | Min | Max | Min | Max | |
| Read | Read cycle time | tRC | 70 | - | 85 | - | 100 | - | ns |
| | Address access time | tAA | - | 70 | - | 85 | - | 100 | ns |
| | Chip select to output | tCO | - | 70 | - | 85 | - | 100 | ns |
| | Output enable to valid output | tOE | - | 35 | - | 40 | - | 50 | ns |
| | $\overline{UB}, \overline{LB}$ Access Time | tBA | - | 35 | - | 40 | - | 50 | ns |
| | Chip select to low-Z output | tLZ | 10 | - | 10 | - | 10 | - | ns |
| | Output enable to low-Z output | tOLZ | 5 | - | 5 | - | 5 | - | ns |
| | $\overline{UB}, \overline{LB}$ enable to low-Z output | tBLZ | 5 | - | 5 | - | 5 | - | ns |
| | Chip disable to high-Z output | tHZ | 0 | 25 | 0 | 25 | 0 | 30 | ns |
| | Output disable to high-Z output | tOHZ | 0 | 25 | 0 | 25 | 0 | 30 | ns |
| | $\overline{UB}, \overline{LB}$ disable to high-Z output | tBHZ | 0 | 25 | 0 | 25 | 0 | 30 | ns |
| | Output hold from address change | tOH | 10 | - | 10 | - | 15 | - | ns |
| Write | Write cycle time | tWC | 70 | - | 85 | - | 100 | - | ns |
| | Chip select to end of write | tCW | 60 | - | 70 | - | 80 | - | ns |
| | Address set-up time | tAS | 0 | - | 0 | - | 0 | - | ns |
| | Address valid to end of write | tAW | 60 | - | 70 | - | 80 | - | ns |
| | Write pulse width | tWP | 50 | - | 60 | - | 70 | - | ns |
| | $\overline{UB}, \overline{LB}$ valid to end of write | tBW | 60 | - | 70 | - | 80 | - | ns |
| | Write recovery time | tWR | 0 | - | 0 | - | 0 | - | ns |
| | Write to output high-Z | tWHZ | 0 | 30 | 0 | 30 | 0 | 35 | ns |
| | Data to write time overlap | tdW | 30 | - | 35 | - | 40 | - | ns |
| | Data hold from write time | tdH | 0 | - | 0 | - | 0 | - | ns |
| | End write to output low-Z | tOW | 5 | - | 5 | - | 5 | - | ns |

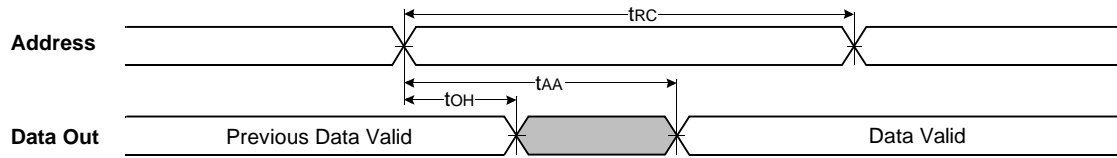
DATA RETENTION CHARACTERISTICS

| Item | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------|------------------|---|-----|-----|------------------|---------------|
| V_{CC} for data retention | V_{DR} | $\overline{CS} \geq V_{CC}-0.2\text{V}$ | 2.0 | - | 3.6 | V |
| Data retention current | I_{DR} | $V_{CC}=3.0\text{V}, \overline{CS} \geq V_{CC}-0.2\text{V}$ | - | - | 15 ¹⁾ | μA |
| Data retention set-up time | t _{SDR} | See data retention waveform | 0 | - | - | ms |
| Recovery time | t _{RDR} | | 5 | - | - | |

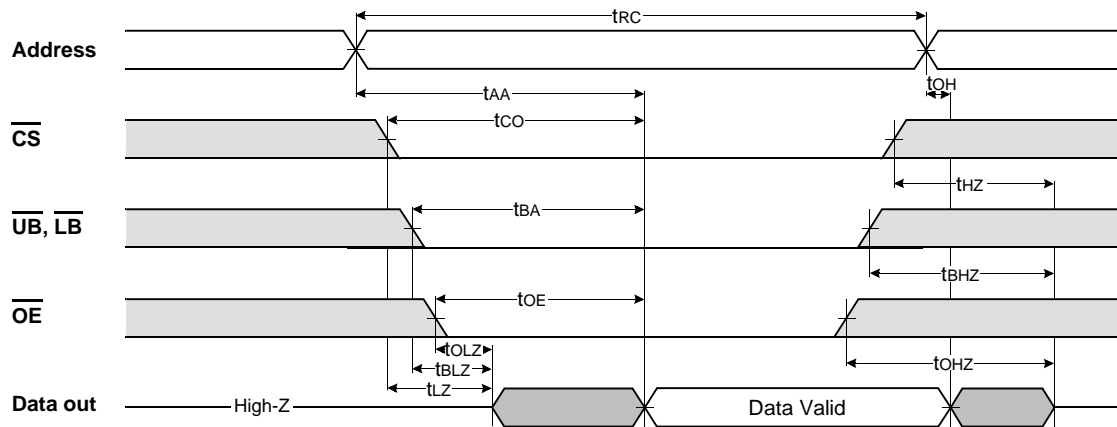
1. Industrial product=20 μA

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



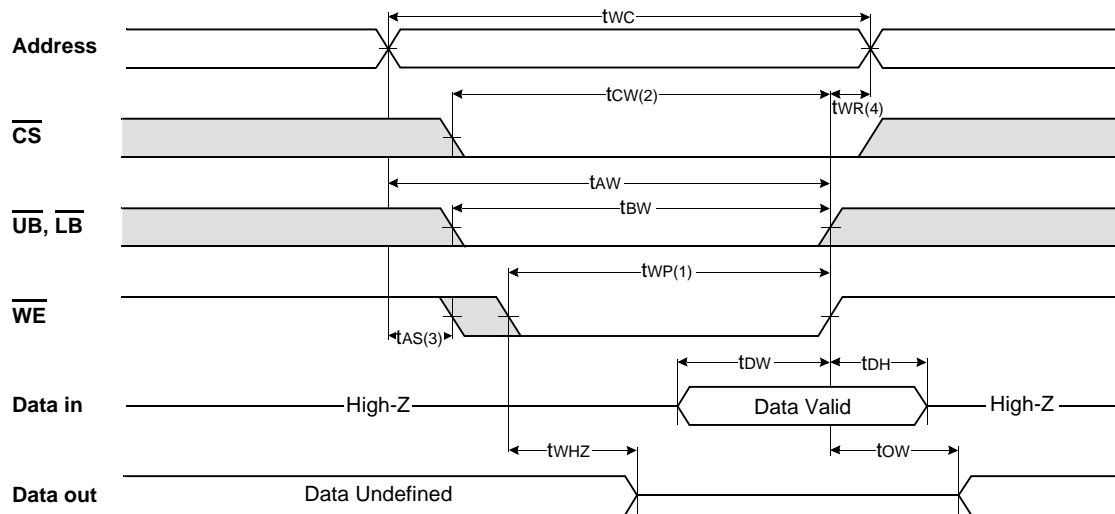
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



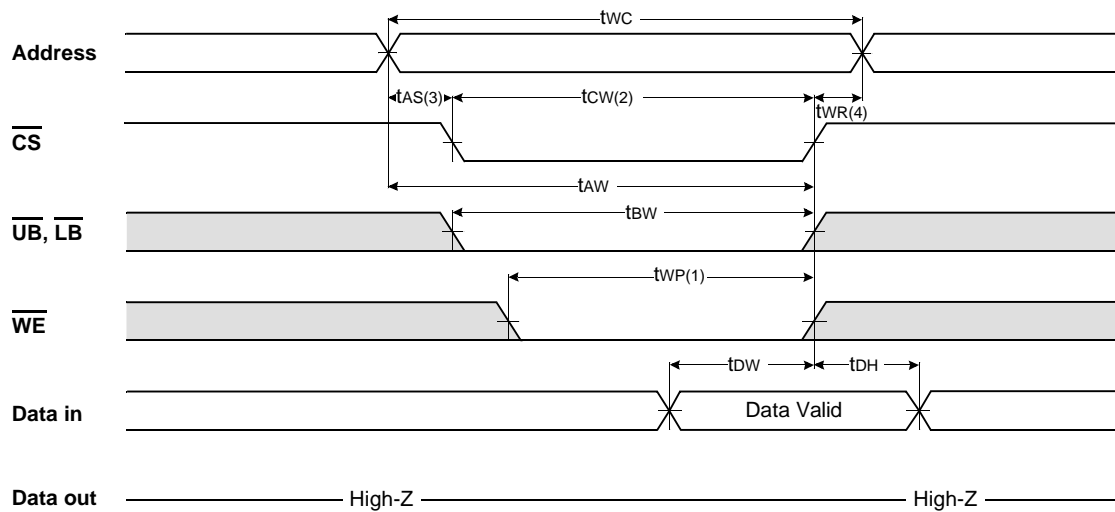
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

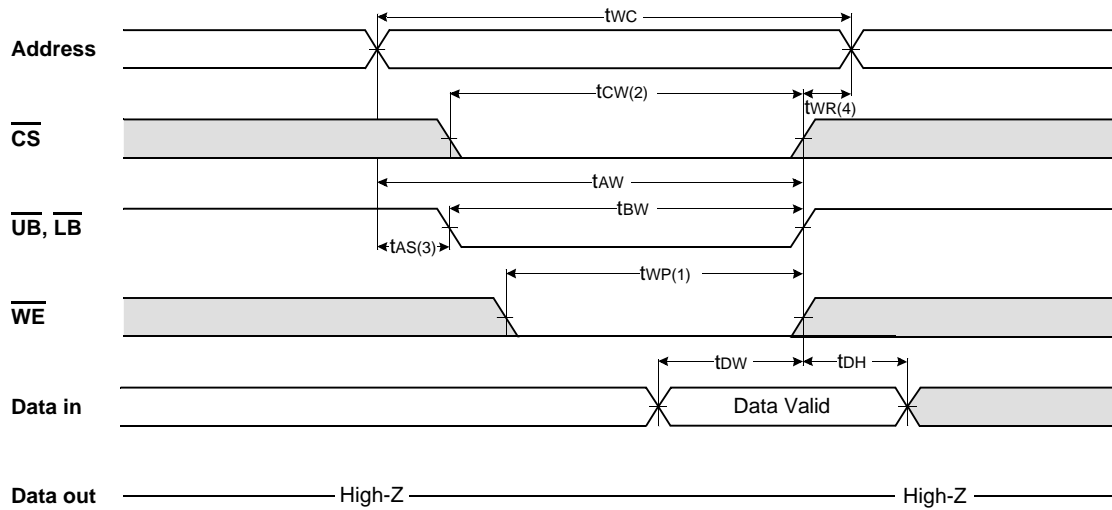
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)

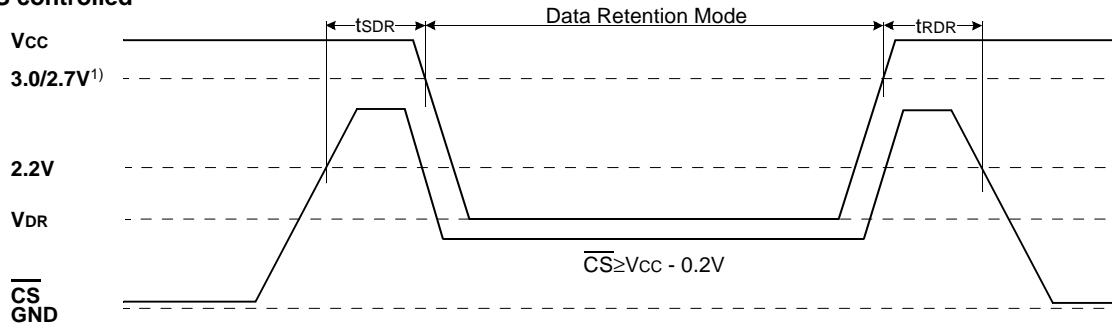


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM

\overline{CS} controlled

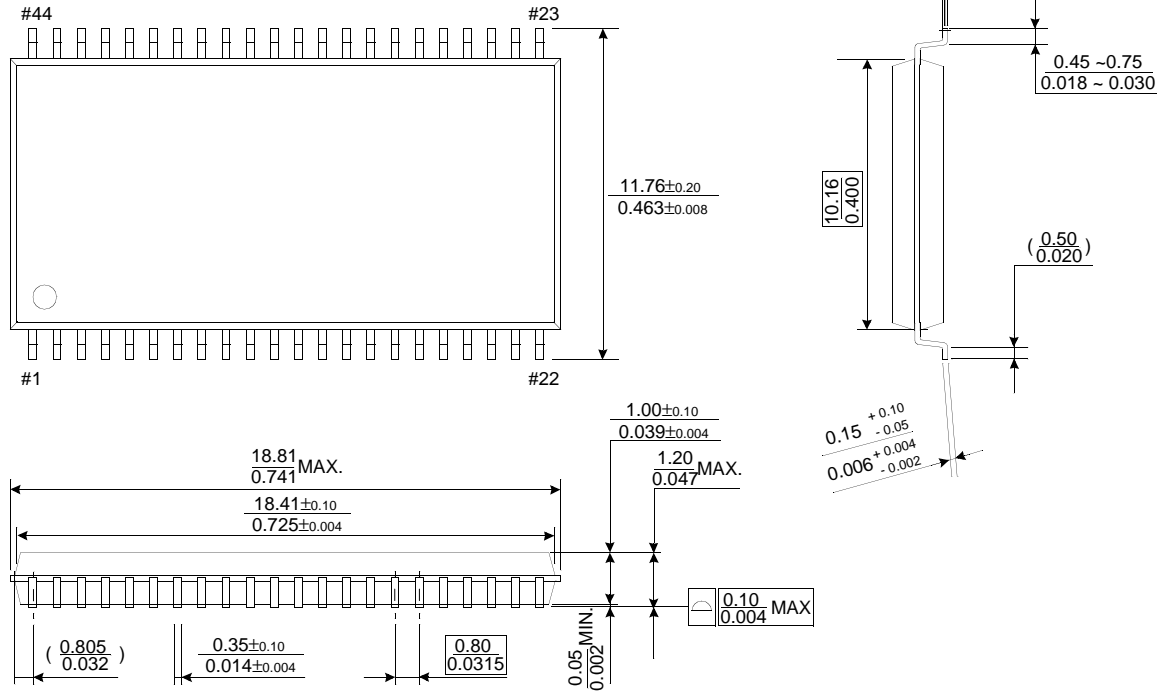


1. 3.0V for KM616V1000B family, 2.7V KM616U1000B family

PACKAGE DIMENSIONS

Unit : millimeter(inch)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

