

Document Title

256Kx4 Bit (with OE) High Speed Static RAM(5V Operating), Evolutionary Pin out.

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>												
Rev. 0.0	Initial release with Design Target.	Feb. 1st 1997	Design Target												
Rev.1.0	Release to Preliminary Data Sheet. 1.1. Replace Design Target to Preliminary.	Jun. 1st 1997	Preliminary												
Rev. 2.0	Release to Final Data Sheet. 2.1. Delete Preliminary. 2.2. Delete 17ns, L-version and Industrial Temperature Part. 2.3. Delete VOH1=3.95V. 2.4. Delete Data Retention Characteristics and Wave form. 2.5. Relex operating current.	Feb. 6th 1998	Final												
<table><tr><th>Speed</th><th>Previous</th><th>Now</th></tr><tr><td>15ns</td><td>120mA</td><td>120mA</td></tr><tr><td>17ns</td><td>110mA</td><td>-</td></tr><tr><td>20ns</td><td>100mA</td><td>118mA</td></tr></table>				Speed	Previous	Now	15ns	120mA	120mA	17ns	110mA	-	20ns	100mA	118mA
Speed	Previous	Now													
15ns	120mA	120mA													
17ns	110mA	-													
20ns	100mA	118mA													
Rev.3.0	3.1. Add Low power Version. 3.2. Add Data Retention chracteristics.	Jul. 28th 1998	Final												

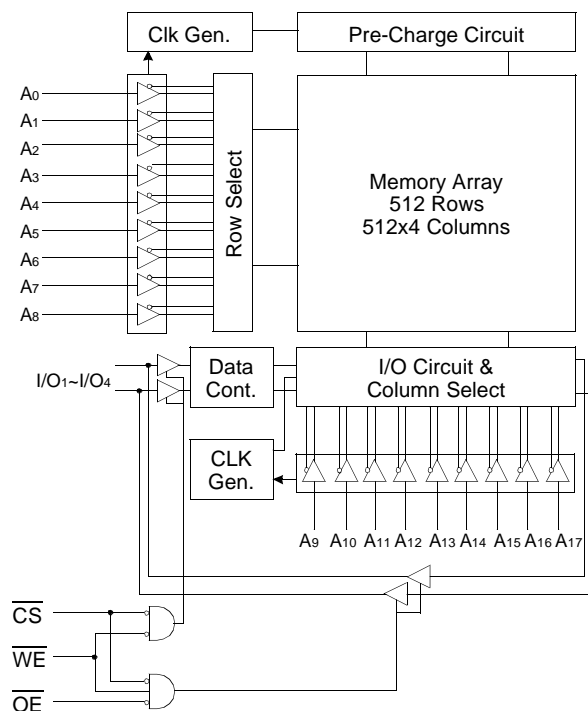
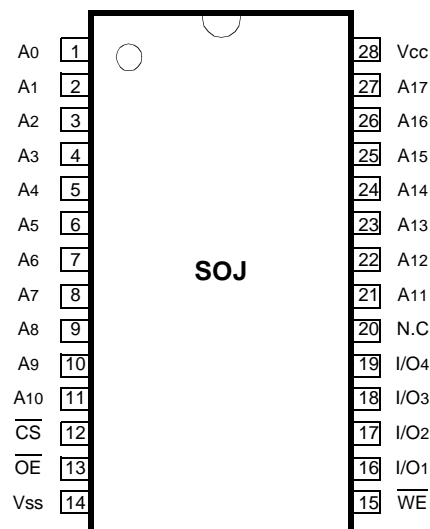
The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

**256K x 4 Bit (with OE) High-Speed CMOS Static RAM**
**FEATURES**

- Fast Access Time 15, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 20mA(Max.)
  - (CMOS) : 5mA(Max.)
  - 1mA(Max) L-Ver. Only
- Operating KM641001B/BL - 15 : 120mA(Max.)
- KM641001B/BL - 20 : 118mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Standard Pin Configuration
  - KM641001B/BLJ : 28-SOJ-400A

**GENERAL DESCRIPTION**

The KM641001B is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM641001B/BL uses 4 common input and output lines and has at output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM641001B/BL is packaged in a 400 mil 28-pin plastic SOJ.

**FUNCTIONAL BLOCK DIAGRAM**

**PIN CONFIGURATION (Top View)**

**PIN FUNCTION**

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

## ABSOLUTE MAXIMUM RATINGS\*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	0 to 70	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5**	V
Input Low Voltage	V <sub>IL</sub>	-0.5*	-	0.8	V

\* V<sub>IL</sub>(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA .

\*\* V<sub>IH</sub>(Max) = V<sub>CC</sub> + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS (T<sub>A</sub>=0 to 70°C, V<sub>CC</sub>=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>		-2	2	μA
Output Leakage Current	I <sub>LO</sub>	CS=V <sub>IH</sub> or OE=V <sub>IH</sub> or WE=V <sub>IL</sub> V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>CC</sub>		-2	2	μA
Operating Current	I <sub>CC</sub>	Min. Cycle, 100% Duty CS=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	15ns	-	120	mA
			20ns	-	118	
Standby Current	I <sub>SB</sub>	Min. Cycle, CS=V <sub>IH</sub>		-	20	mA
	I <sub>SB1</sub>	f=0MHz, CS≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V	Normal	-	5	mA
			L-ver	-	1	mA
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> =8mA		-	0.4	V
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> =-4mA		2.4	-	V

CAPACITANCE\*(T<sub>A</sub>=25°C, f=1.0MHz)

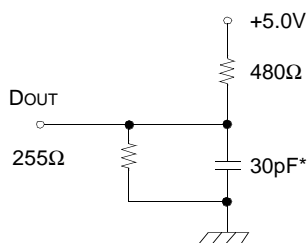
Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF

\* Capacitance is sampled and not 100% tested.

**AC CHARACTERISTICS**( $T_A=0$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 10\%$ , unless otherwise noted.)**TEST CONDITIONS**

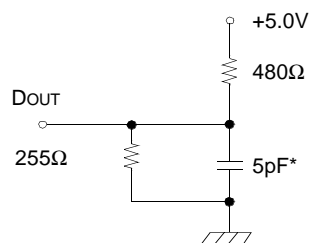
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ &amp; tOHZ



\* Including Scope and Jig Capacitance

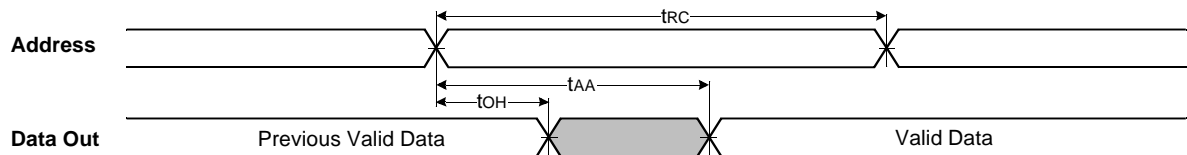
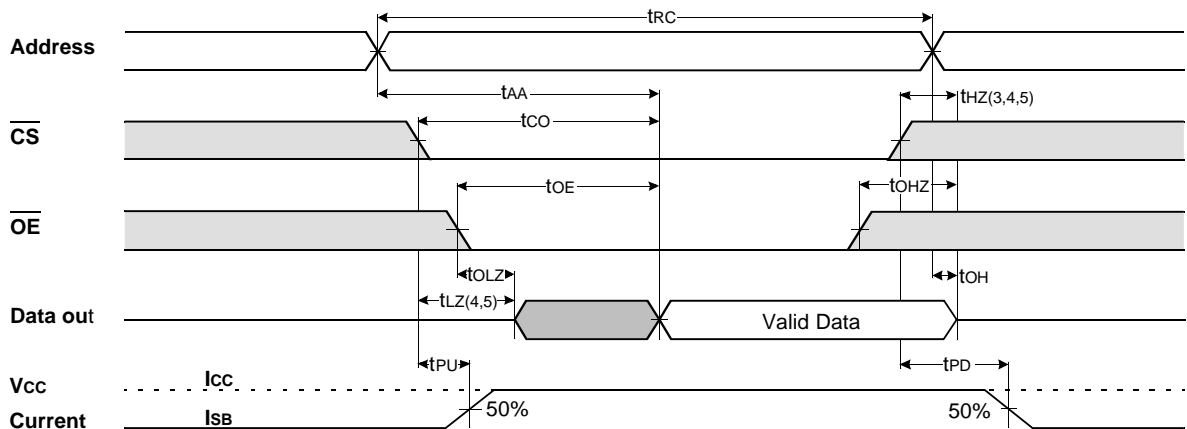
**READ CYCLE**

Parameter	Symbol	KM641001B/BL-15		KM641001B/BL-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	15	-	20	-	ns
Address Access Time	t <sub>AA</sub>	-	15	-	20	ns
Chip Select to Output	t <sub>CO</sub>	-	15	-	20	ns
Output Enable to Valid Output	t <sub>OE</sub>	-	8	-	10	ns
Chip Enable to Low-Z Output	t <sub>LZ</sub>	3	-	3	-	ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	0	-	0	-	ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	6	0	8	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	6	0	8	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	ns
Chip Selection to Power Up Time	t <sub>PU</sub>	0	-	0	-	ns
Chip Selection to Power DownTime	t <sub>PD</sub>	-	15	-	20	ns

## WRITE CYCLE

Parameter	Symbol	KM641001B/BL-15		KM641001B/BL-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	15	-	20	-	ns
Chip Select to End of Write	t <sub>CW</sub>	10	-	12	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
Address Valid to End of Write	t <sub>AW</sub>	10	-	12	-	ns
Write Pulse Width( $\overline{\text{OE}}$ High)	t <sub>WP</sub>	10	-	12	-	ns
Write Pulse Width( $\overline{\text{OE}}$ Low)	t <sub>WP1</sub>	15	-	20	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
Write to Output High-Z	t <sub>WHZ</sub>	0	8	0	10	ns
Data to Write Time Overlap	t <sub>DW</sub>	7	-	9	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	0	-	ns
End Write to Output Low-Z	t <sub>OW</sub>	3	-	3	-	ns

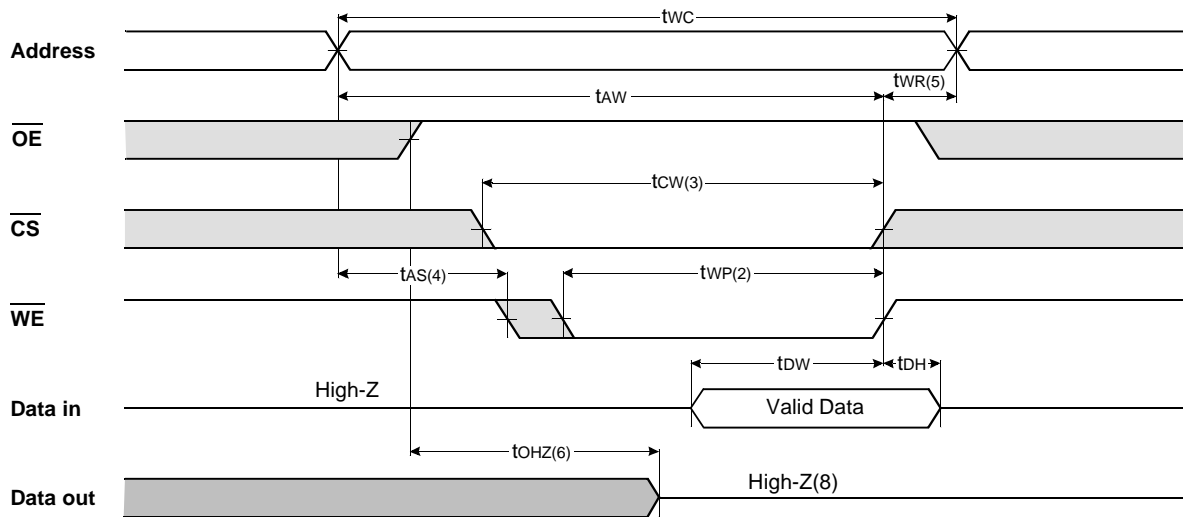
## TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$ ,  $\overline{\text{WE}}=V_{\text{IH}}$ )TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{\text{WE}}=V_{\text{IH}}$ )

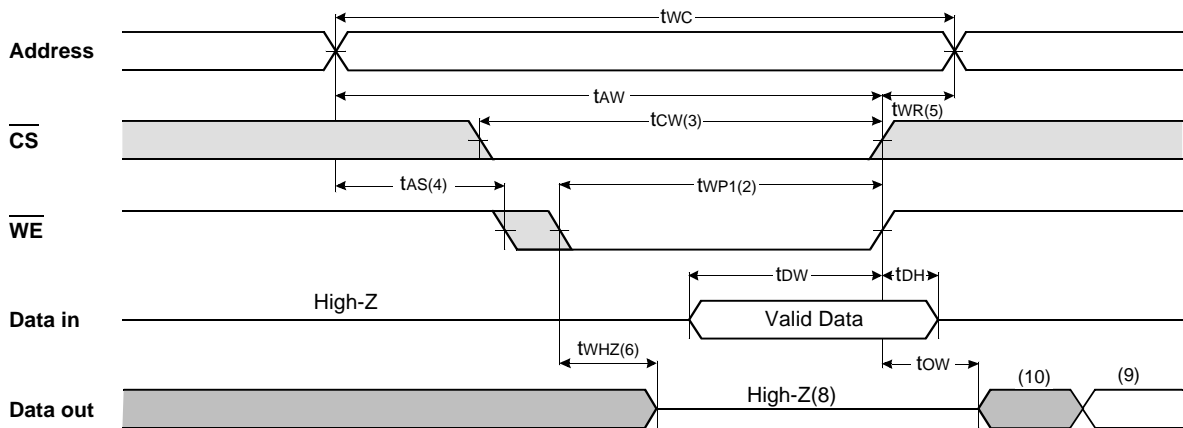
**NOTES(READ CYCLE)**

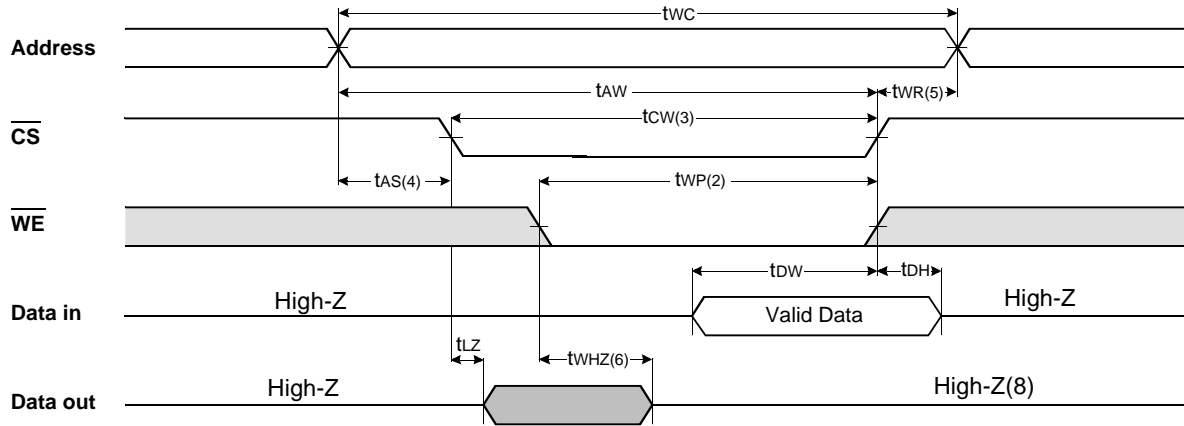
1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device.
5. Transition is measured  $\pm 200\text{mV}$  space from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS}=V_{IL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}=\text{Clock}$ )**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}=\text{Low Fixed}$ )**



TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{\text{CS}}$ =Controlled)

## NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$ . A write begins at the latest transition  $\overline{\text{CS}}$  going low and  $\overline{\text{WE}}$  going low. A write ends at the earliest transition  $\overline{\text{CS}}$  going high or  $\overline{\text{WE}}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{CW}$  is measured from the later of  $\overline{\text{CS}}$  going low to end of write.
4.  $t_{AS}$  is measured from the address valid to the beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{\text{CS}}$  or  $\overline{\text{WE}}$  going high.
6. If  $\overline{\text{OE}}$ ,  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{\text{CS}}$  goes low simultaneously with  $\overline{\text{WE}}$  going or after  $\overline{\text{WE}}$  going low, the outputs remain high impedance state.
9.  $D_{out}$  is the read data of the new address.
10. When  $\overline{\text{CS}}$  is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

# FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	ICC
L	H	L	Read	DOUT	ICC
L	L	X	Write	DIN	ICC

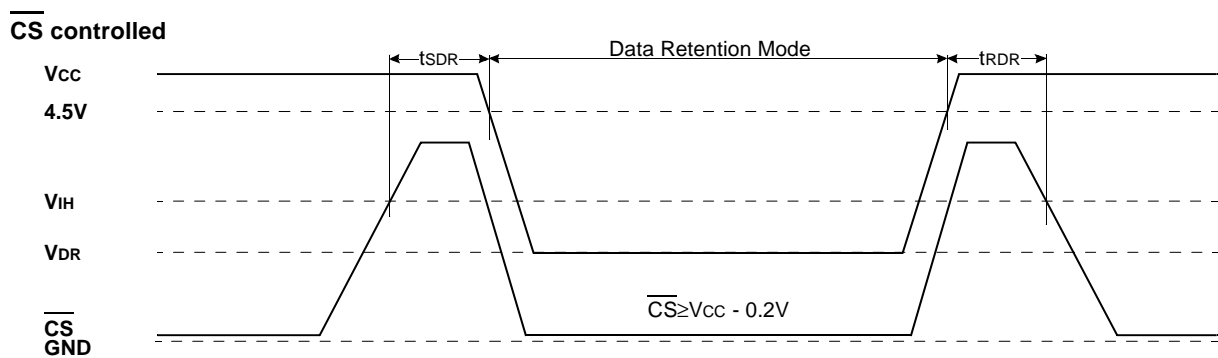
\* X means Don't Care.

# DATA RETENTION CHARACTERISTICS\*(TA=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	VDR	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	5.5	V
Data Retention Current	IDR	VCC=3.0V, $\overline{CS} \geq V_{CC} - 0.2V$ VIN ≥ VCC-0.2V or VIN ≤ 0.2V	-	-	0.4	mA
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR		5	-	-	ms

\* Data Retention Characteristic is for L-ver only.

# DATA RETENTION WAVE FORM





PACKAGE DIMENSIONS

Units: millimeters/Inches

28-SOJ-400A

