

Document Title

**1Mx4 Bit (with OE) High Speed Static RAM(5V Operating),
Operated at Commercial and Industrial Temperature Range.**

Revision History

<u>RevNo.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>																		
Rev. 0.0	Initial release with Design Target.	Jan. 1st 1997	Design Target																		
Rev.1.0	Release to Preliminary Data Sheet. 1. Replace Design Target to Preliminary.	Jun. 1st 1997	Preliminary																		
Rev. 2.0	Release to Final Data Sheet 1. Delete Preliminary 2. Add 30pF capacitive in test load 3. Relex DC characteristics	Feb. 11th 1998	Final																		
<table><tr><th colspan="2">Item</th><th>Previous</th><th>Current</th></tr><tr><td rowspan="3">Icc</td><td>10ns</td><td>190mA</td><td>195mA</td></tr><tr><td>12ns</td><td>180mA</td><td>190mA</td></tr><tr><td>15ns</td><td>170mA</td><td>185mA</td></tr><tr><td>ISB</td><td>f=max.</td><td>40mA</td><td>50mA</td></tr></table>				Item		Previous	Current	Icc	10ns	190mA	195mA	12ns	180mA	190mA	15ns	170mA	185mA	ISB	f=max.	40mA	50mA
Item		Previous	Current																		
Icc	10ns	190mA	195mA																		
	12ns	180mA	190mA																		
	15ns	170mA	185mA																		
ISB	f=max.	40mA	50mA																		
Rev.2.1	Change operating current at Industrial Temperature range. <div><div>Previous spec.</div><div>Changed spec.</div><table><tr><td>Items</td><td>(10/12/15ns part)</td><td>(10/12/15ns part)</td></tr><tr><td>Icc</td><td>195/190/185mA</td><td>220/215/210mA</td></tr></table></div>	Items	(10/12/15ns part)	(10/12/15ns part)	Icc	195/190/185mA	220/215/210mA	Jun. 27th 1998	Final												
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Icc	195/190/185mA	220/215/210mA																			

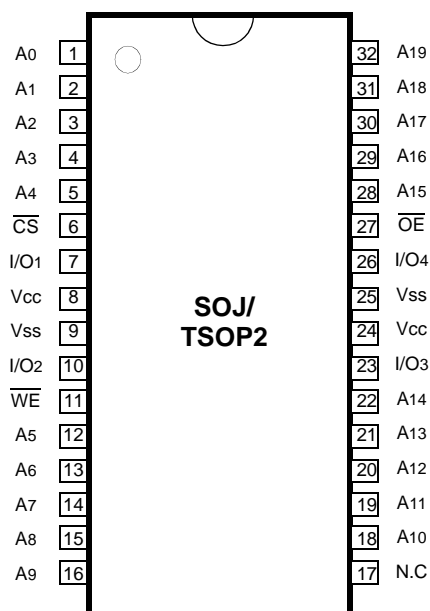
The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

1M x 4 Bit (with \overline{OE}) High-Speed CMOS Static RAM
FEATURES

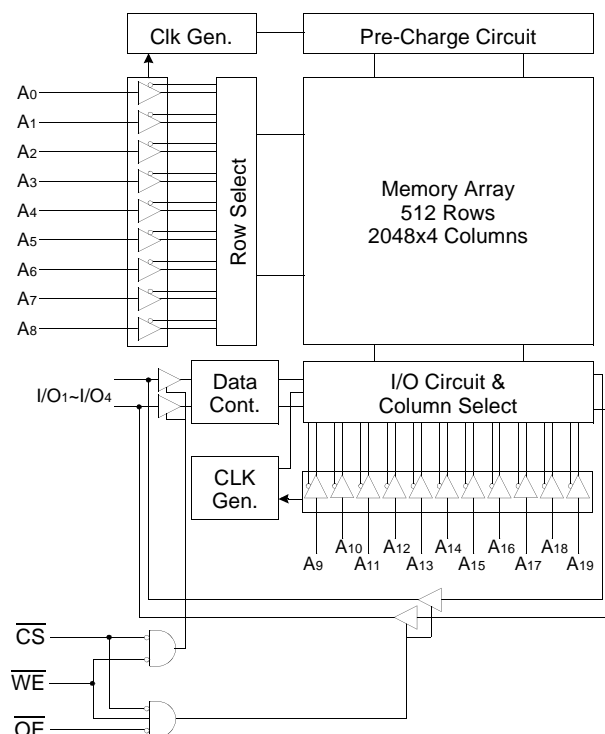
- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 50mA(Max.)
 - (CMOS) : 10mA(Max.)
 - Operating KM644002B - 10 : 195mA(Max.)
 - KM644002B - 12 : 190mA(Max.)
 - KM644002B - 15 : 185mA(Max.)
- Single 5.0V \pm 10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
 - KM644002BJ : 32-SOJ-400
 - KM644002BT : 32-TSOP2-400F

GENERAL DESCRIPTION

The KM644002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM644002B uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM644002B is packaged in a 400 mil 32-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION (Top View)

ORDERING INFORMATION

KM644002B -10/12/15	Commercial Temp.
KM644002BI -10/12/15	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM

PIN FUNCTION

Pin Name	Pin Function
A0 - A19	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
\overline{OE}	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V _{IN} , V _{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss		V _{CC}	-0.5 to 7.0	V
Power Dissipation		P _D	1.0	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} +0.5**	V
Input Low Voltage	V _{IL}	-0.5*	-	0.8	V

NOTE: The above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Input Leakage Current	ILI	VIN=VSS to VCC			-2	2	μA
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT=VSS to VCC			-2	2	μA
Operating Current	ICC	Min. Cycle, 100% Duty CS=VIL, VIN=VIH or VIL, IOUT=0mA	Com.	10ns	-	195	mA
				12ns	-	190	
				15ns	-	185	
			Ind.	10ns	-	220	
				12ns	-	215	
				15ns	-	210	
Standby Current	ISB	Min. Cycle, CS=VIH			-	50	mA
	ISB1	f=0MHz, CS≥VCC-0.2V, VIN≥VCC-0.2V or VIN≤0.2V			-	10	mA
Output Low Voltage Level	VOL	IOL=8mA			-	0.4	V
Output High Voltage Level	VOH	IOH=-4mA			2.4	-	V
	VOH1*	IOH1=-0.1mA			-	3.95	V

NOTE: The above parameters are also guaranteed at industrial temperature range.

* V_{CC}=5.0V, Temp.=25°C

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	7	pF

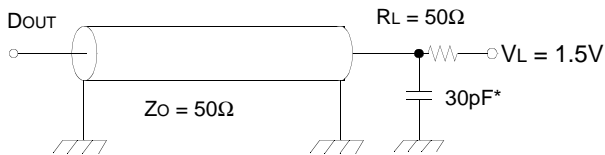
* NOTE : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS($T_A=0$ to 70°C , $V_{CC}=5.0\text{V}\pm 10\%$, unless otherwise noted.)**TEST CONDITIONS**

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

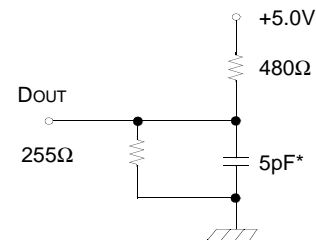
NOTE: The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM644002B-10		KM644002B-12		KM644002B-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	10	-	12	-	15	ns

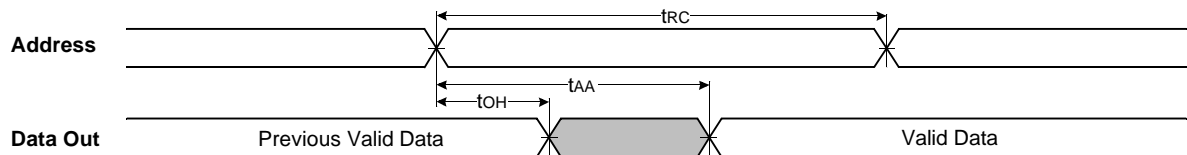
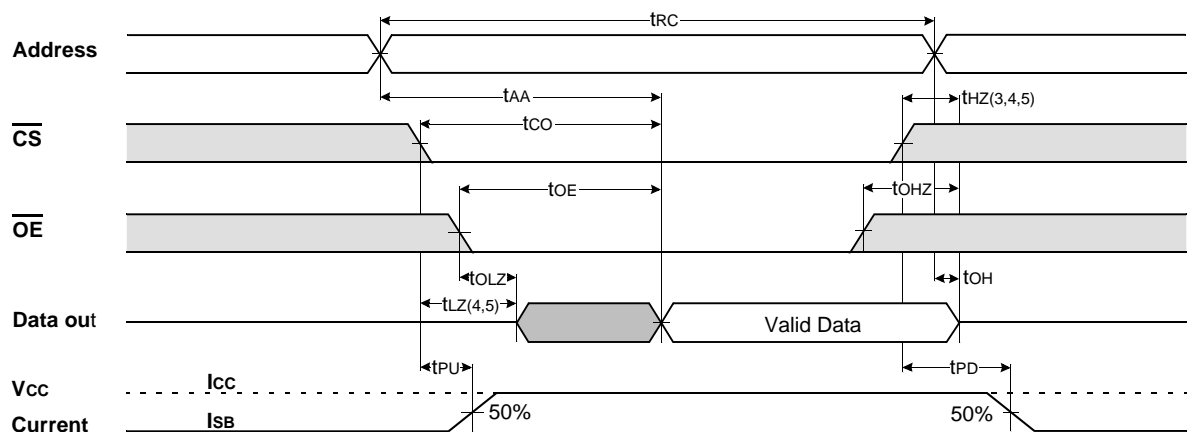
NOTE: The above parameters are also guaranteed at industrial temperature range.

WRITE CYCLE

Parameter	Symbol	KM644002B-10		KM644002B-12		KM644002B-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	7	-	8	-	10	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	7	-	8	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	tWP	7	-	8	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	tWP1	10	-	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	5	-	6	-	7	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

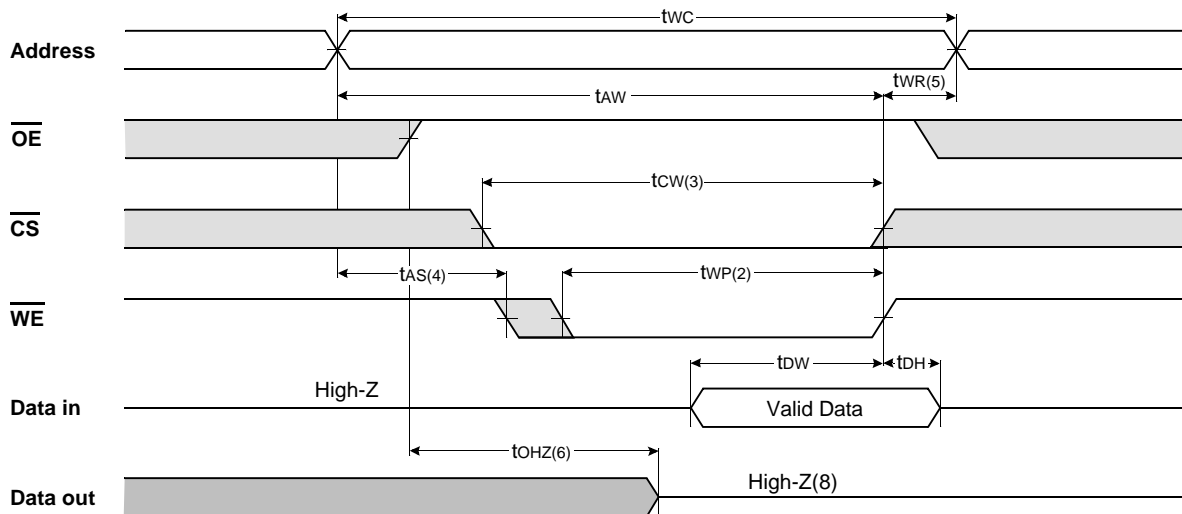
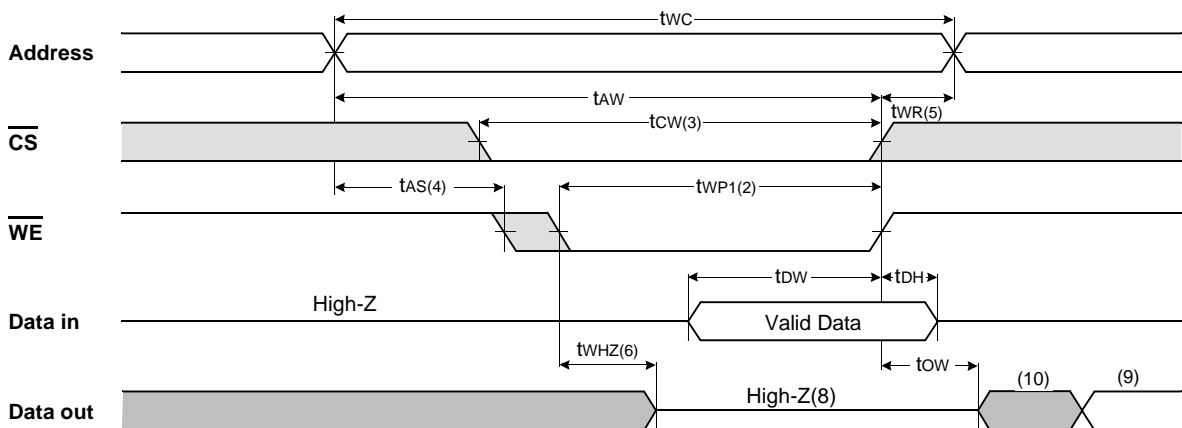
NOTE: The above parameters are also guaranteed at industrial temperature range.

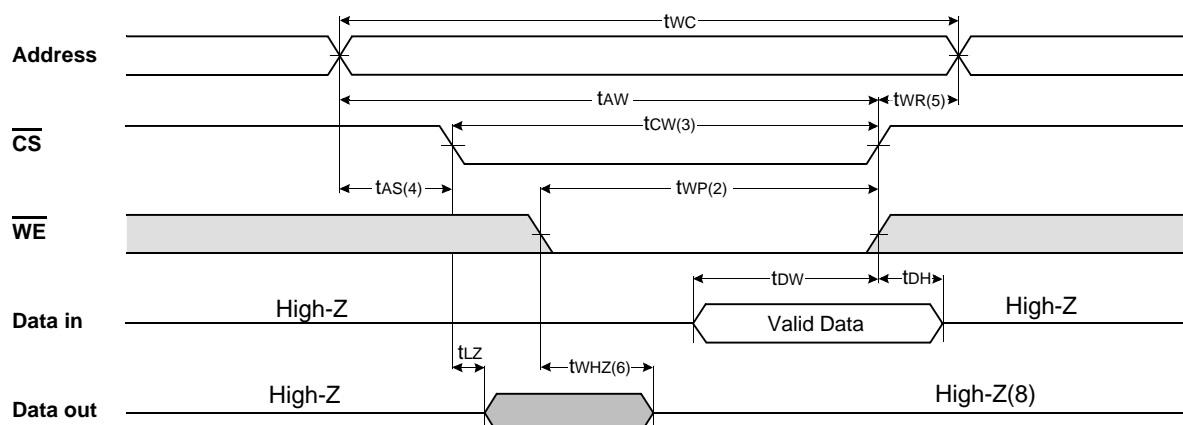
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=\text{V}_{\text{IL}}$, $\overline{\text{WE}}=\text{V}_{\text{IH}}$)TIMING WAVEFORM OF READ CYCLE(2) ($\overline{\text{WE}}=\text{V}_{\text{IH}}$)

NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{OE} = Clock)**TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{OE} =Low Fixed)**

TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{CS}}$ =Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{\text{CS}}$ and $\overline{\text{WE}}$. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low ; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{\text{CS}}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.
6. If $\overline{\text{OE}}$, $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
9. DOUT is the read data of the new address.
10. When $\overline{\text{CS}}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB} , I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	DOUT	I_{CC}
L	L	X	Write	DIN	I_{CC}

* NOTE : X means Don't Care.

32-SOJ-400

[illegible]

Units:millimeters/Inches

