

Document Title

1Mx4 Bit (with OE) High Speed Static RAM(3.3V Operating),
Operated at Commercial and Industrial Temperature Range.

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>																										
Rev. 0.0	Initial release with Design Target.	Jan. 1st, 1997	Design Target																										
Rev.1.0	Release to Preliminary Data Sheet. 1. Replace Design Target to Preliminary.	Jun. 1st, 1997	Preliminary																										
Rev. 2.0	Release to Final Data Sheet 1. Delete Preliminary 2. Add 30pF capacitive in test load 3. Relex DC characteristics	Feb.11th.1998	Final																										
<table border="1"> <thead> <tr> <th colspan="2">Item</th><th>Previous</th><th>Current</th></tr> </thead> <tbody> <tr> <td rowspan="3">Icc</td><td>10ns</td><td>160mA</td><td>185mA</td></tr> <tr> <td>12ns</td><td>150mA</td><td>180mA</td></tr> <tr> <td>15ns</td><td>140mA</td><td>175mA</td></tr> <tr> <td>ISB</td><td>f=max.</td><td>40mA</td><td>50mA</td></tr> <tr> <td>ISB1</td><td>f=0</td><td>10 / 1mA</td><td>10 / 1.2mA</td></tr> <tr> <td>IDR</td><td>VDR=3.0V</td><td>0.9mA</td><td>1.0mA</td></tr> </tbody> </table>				Item		Previous	Current	Icc	10ns	160mA	185mA	12ns	150mA	180mA	15ns	140mA	175mA	ISB	f=max.	40mA	50mA	ISB1	f=0	10 / 1mA	10 / 1.2mA	IDR	VDR=3.0V	0.9mA	1.0mA
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Rev.2.1	Change operating current at Industrial Temperature range. <div> <div>Items</div> <div>Icc</div> </div> <div> <div>Previous spec.</div> <div>(10/12/15ns part)</div> <div>185/180/175mA</div> </div> <div> <div>Changed spec.</div> <div>(10/12/15ns part)</div> <div>210/205/200mA</div> </div>	Jun. 27th 1998	Final																										

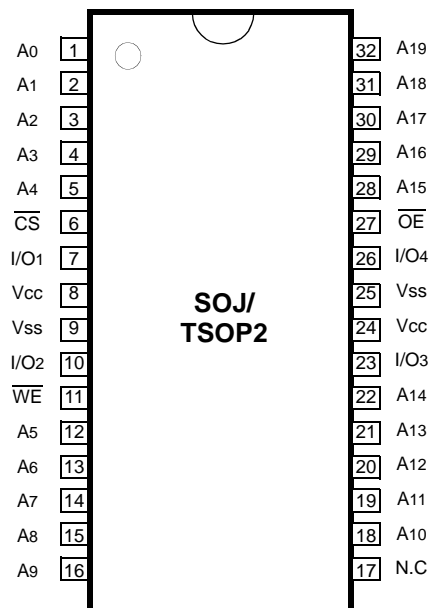
The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

1M x 4 Bit (with \overline{OE}) High-Speed CMOS Static RAM (3.3V Operating)**FEATURES**

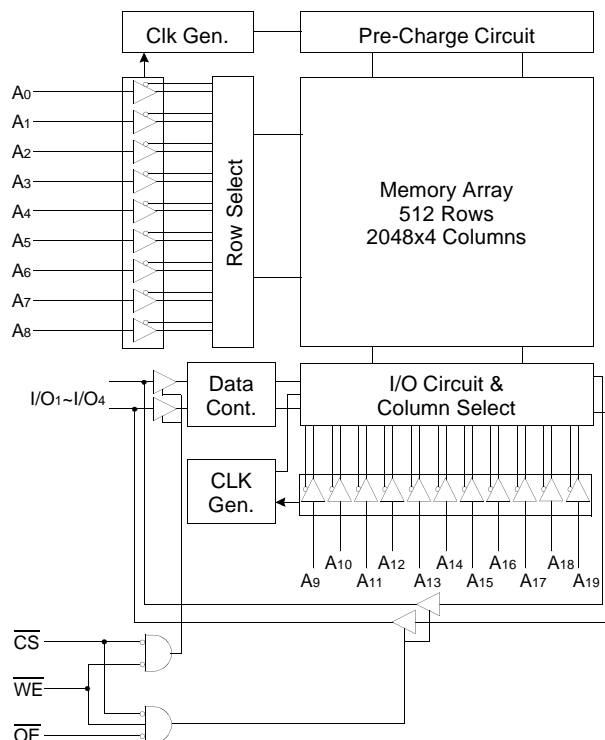
- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 50mA(Max.)
 - (CMOS) : 10mA(Max.)
 - 1.2mA(Max.)- L-Ver.
- Operating KM64V4002B/BL - 10 : 185mA(Max.)
- KM64V4002B/BL - 12 : 180mA(Max.)
- KM64V4002B/BL - 15 : 175mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V(Min.) - L-Ver. Only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
 - KM64V4002BJ : 32-SOJ-400
 - KM64V4002BT : 32-TSOP2-400F

GENERAL DESCRIPTION

The KM64V4002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 1,048,576 words by 4 bits. The KM64V4002B uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64V4002B is packaged in a 400 mil 32-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION (Top View)**ORDERING INFORMATION**

KM64V4002B/BL -10/12/15	Commercial Temp.
KM64V4002BI/BLI -10/12/15	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM**PIN FUNCTION**

Pin Name	Pin Function
A0 - A19	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
\overline{OE}	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V _{CC}	-0.5 to 4.6	V
Power Dissipation		P _D	1.0	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3**	V
Input Low Voltage	V _{IL}	-0.3*	-	0.8	V

NOTE: The above parameters are also guaranteed at industrial temperature range.

* V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}			-2	2	μA
Output Leakage Current	I _{LO}	CS=V _{IH} or OE=V _{IH} or WE=V _{IL} V _{OUT} =V _{SS} to V _{CC}			-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty CS=V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	Com.	10ns	-	185	mA
				12ns	-	180	
				15ns	-	175	
			Ind.	10ns	-	210	
				12ns	-	205	
				15ns	-	200	
Standby Current	I _{SB}	Min. Cycle, CS=V _{IH}			-	50	mA
	I _{SB1}	f=0MHz, CS ≥ V _{CC} -0.2V, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V		Normal	-	10	mA
				L-Ver.	-	1.2	
Output Low Voltage Level	V _{OL}	I _{OL} =8mA			-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA			2.4	-	V

NOTE: The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	7	pF

* NOTE : Capacitance is sampled and not 100% tested.

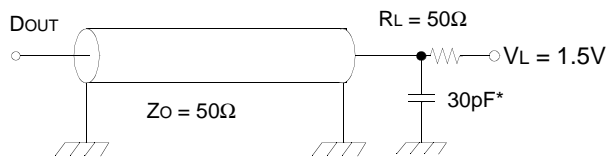
AC CHARACTERISTICS (TA=0 to 70°C, VCC=3.3±0.3V, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

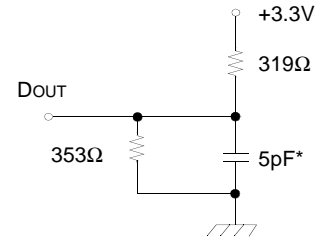
NOTE: The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM64V4002B/BL-10		KM64V4002B/BL-12		KM64V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	10	-	12	-	15	-	ns
Address Access Time	tAA	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	tPD	-	10	-	12	-	15	ns

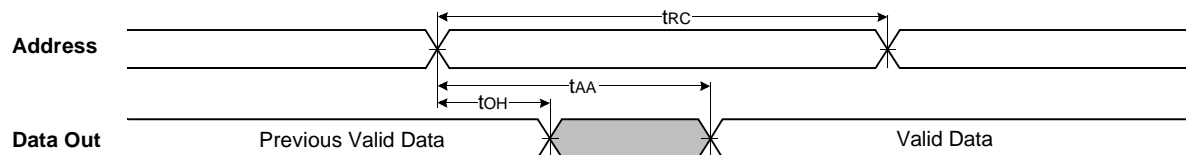
NOTE: The above parameters are also guaranteed at industrial temperature range.

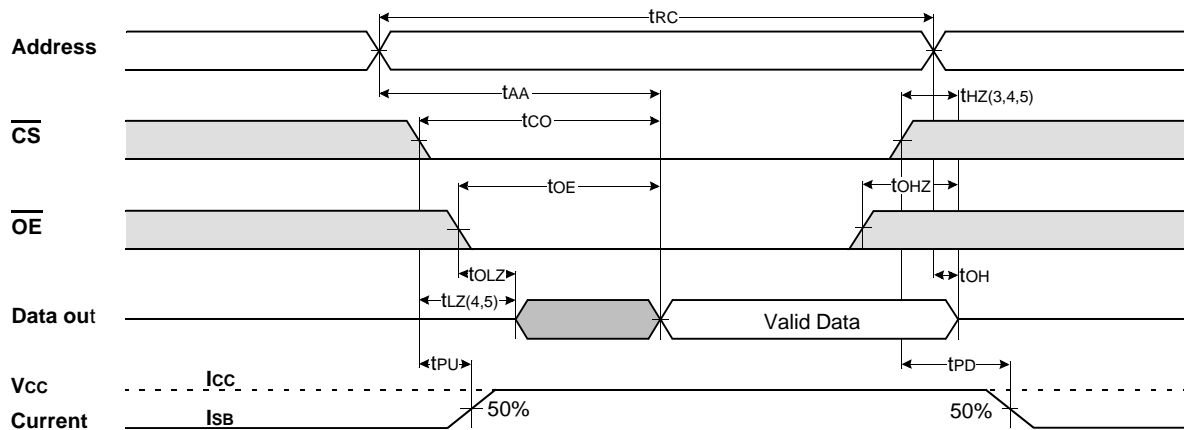
WRITE CYCLE

Parameter	Symbol	KM64V4002B/BL-10		KM64V4002B/BL-12		KM64V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t _{CW}	7	-	8	-	10	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	7	-	8	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	t _{WP}	7	-	8	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	t _{WP1}	10	-	12	-	15	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	ns

NOTE: The above parameters are also guaranteed at industrial temperature range.

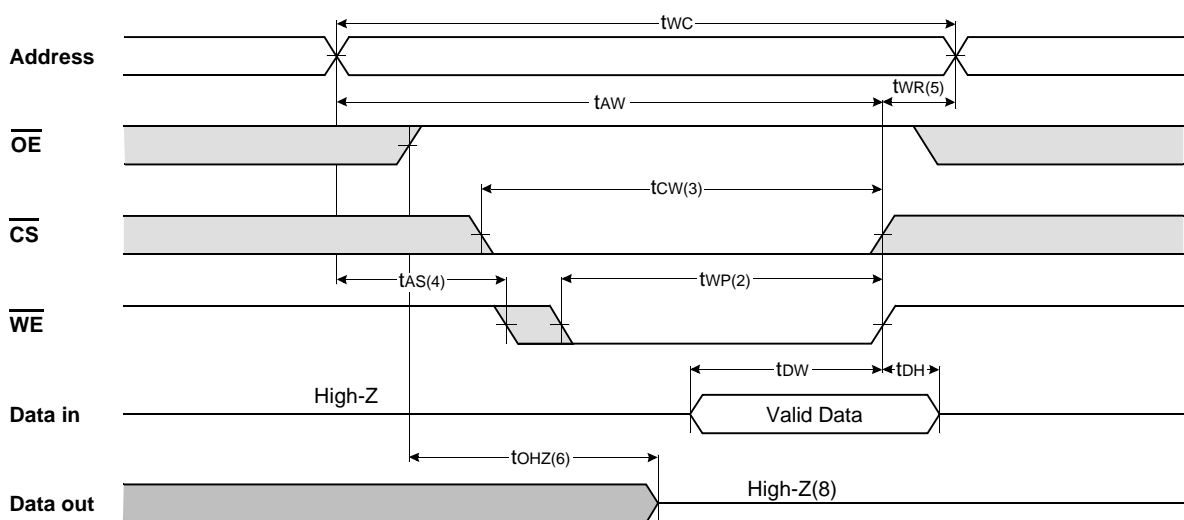
TIMMING DIAGRAMS

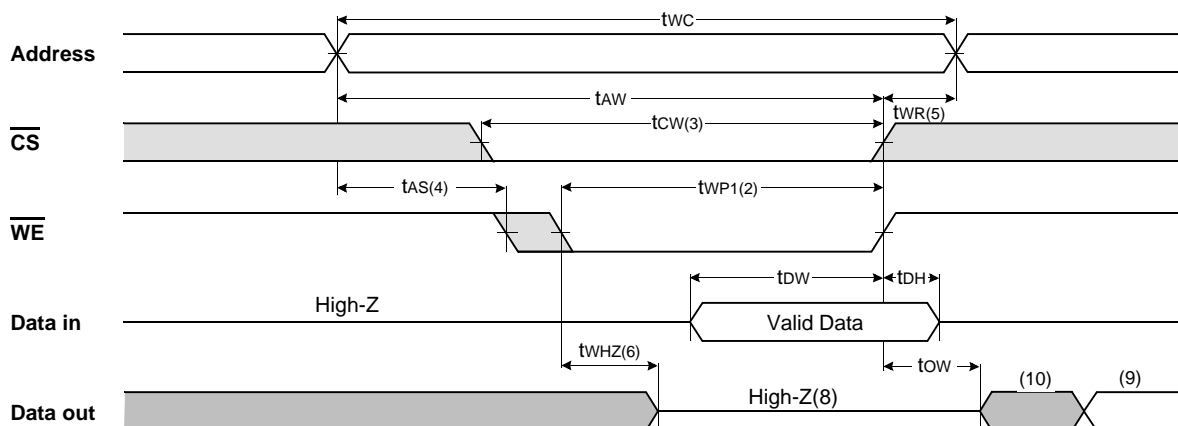
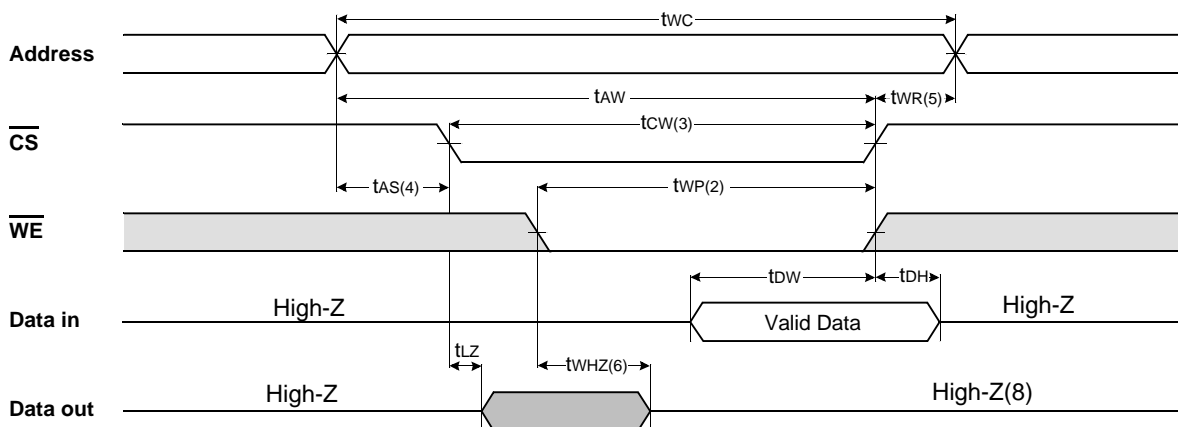
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$, $\overline{\text{WE}}=V_{\text{IH}}$)

TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

NOTES(WRITE CYCLE)

- \overline{WE} is high for read cycle.
- All read cycle timing is referenced from the last valid address to the first transition address.
- t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
- At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
- Transition is measured space $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- Device is continuously selected with $\overline{CS}=V_{IL}$.
- Address valid prior to coincident with \overline{CS} transition low.
- For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}=\text{Clock}$)

TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{\text{OE}}$ =Low Fixed)TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{\text{CS}}$ =Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low ; A write ends at the earliest transition $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of $\overline{\text{CS}}$ going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high.
6. If $\overline{\text{OE}}$, $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{WE}	\overline{OE}	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	I _{CC}
L	H	L	Read	DOUT	I _{CC}
L	L	X	Write	DIN	I _{CC}

* NOTE : X means Don't Care.

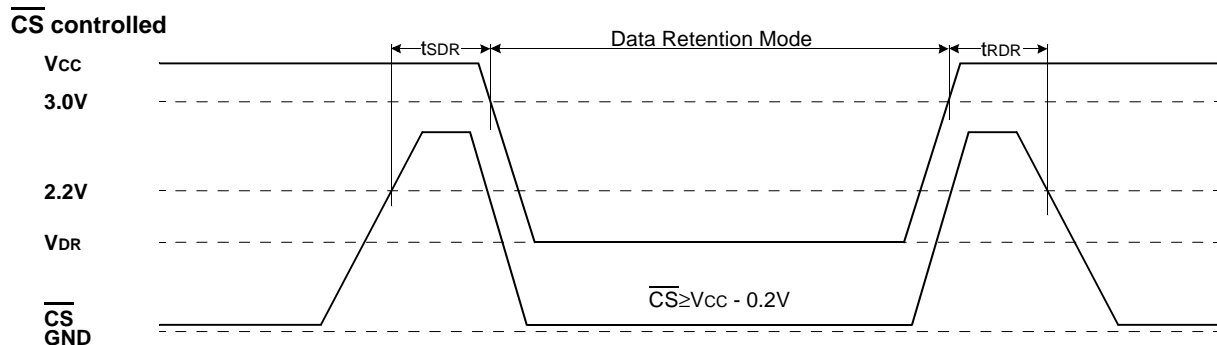
DATA RETENTION CHARACTERISTICS* (T_A=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V _{CC} for Data Retention	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} =3.0V, $\overline{CS} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	-	-	1.0	mA
		V _{CC} =2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	-	-	0.7	mA
Data Retention Set-Up Time	t _{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t _{RDR}		5	-	-	ms

NOTE: The above parameters are also guaranteed at industrial temperature range.

* L-Ver only.

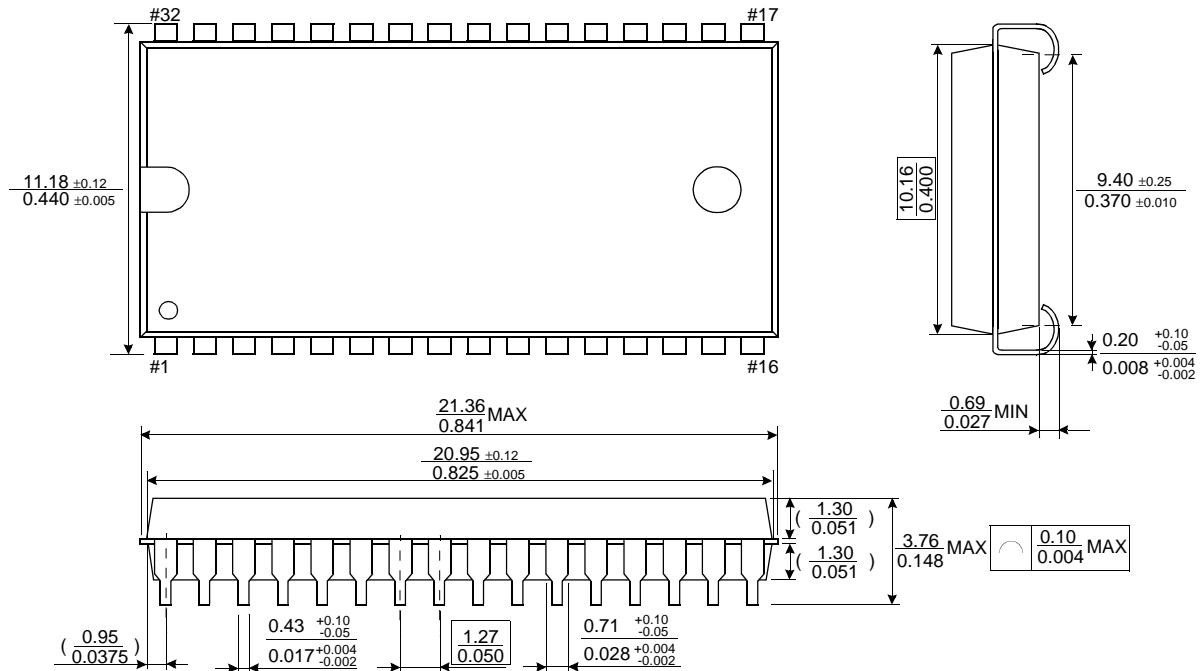
DATA RETENTION WAVE FORM



PACKAGE DIMENSIONS

32-SOJ-400

Units: millimeters/Inches



32-TSOP2-400F

Units: millimeters/Inches

