

## Document Title

128Kx8 bit Low Power and Low Voltage CMOS Static RAM

## Revision History

| <u>Revision No.</u> | <u>History</u> | <u>Draft Data</u>  | <u>Remark</u> |
|---------------------|----------------|--------------------|---------------|
| 0.0                 | Initial draft  | September 10, 1998 | Preliminary   |
| 1.0                 | Finalize       | April 12, 1999     | Final         |

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## 128Kx8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: TFT
- Organization: 128Kx8
- Power Supply Voltage: 2.3V ~ 2.7V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-TSOP1-0820F, 32-TSOP1-0813.4F

### GENERAL DESCRIPTION

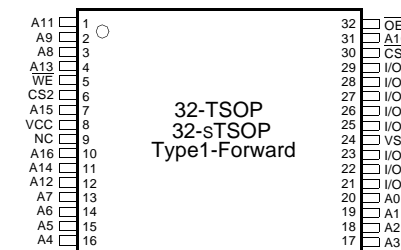
The KM68S1000E families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed(ns)             | Power Dissipation   |                       | PKG Type                           |
|----------------|-----------------------|-----------|-----------------------|---------------------|-----------------------|------------------------------------|
|                |                       |           |                       | Standby (Isb1, Max) | Operating (Icc2, Max) |                                    |
| KM68S1000ELI-L | Industrial(-40~85°C)  | 2.3~2.7V  | 85 <sup>1)</sup> /100 | 10μA                | 15mA                  | 32-TSOP1-0820F<br>32-TSOP1-0813.4F |

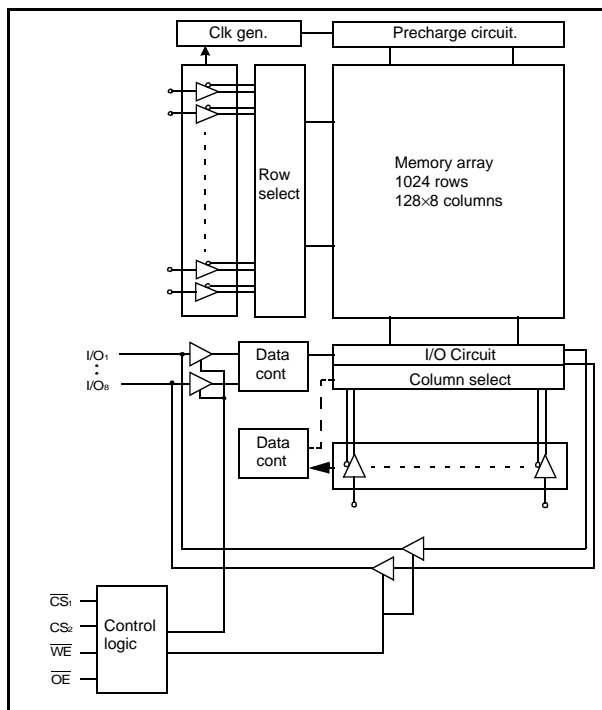
1. The parameters are tested with 30pF test load

### PIN DESCRIPTION



| Name                             | Function            |
|----------------------------------|---------------------|
| A0~A16                           | Address Inputs      |
| $\overline{WE}$                  | Write Enable Input  |
| $\overline{CS1}, \overline{CS2}$ | Chip Select Input   |
| $\overline{OE}$                  | Output Enable Input |
| I/O1~I/O8                        | Data Inputs/Outputs |
| Vcc                              | Power               |
| Vss                              | Ground              |
| N.C.                             | No Connection       |

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

| Industrial Temperature Products(-40~85°C) |                         |
|---|-------------------------|
| Part Name                                 | Function                |
| KM68S1000ELTI-8L                          | 32-TSOP F, 85ns, 2.5V   |
| KM68S1000ELTI-10L                         | 32-TSOP F, 100ns, 2.5V  |
| KM68S1000ELTGI-8L                         | 32-sTSOP F, 85ns, 2.5V  |
| KM68S1000ELTGI-10L                        | 32-sTSOP F, 100ns, 2.5V |

## FUNCTIONAL DESCRIPTION

| $\overline{CS}_1$ | $CS_2$          | $\overline{OE}$ | $\overline{WE}$ | I/O    | Mode            | Power   |
|-------------------|-----------------|-----------------|-----------------|--------|-----------------|---------|
| H                 | X <sup>1)</sup> | X <sup>1)</sup> | X <sup>1)</sup> | High-Z | Deselected      | Standby |
| X <sup>1)</sup>   | L               | X <sup>1)</sup> | X <sup>1)</sup> | High-Z | Deselected      | Standby |
| L                 | H               | H               | H               | High-Z | Output Disabled | Active  |
| L                 | H               | L               | H               | Dout   | Read            | Active  |
| L                 | H               | X <sup>1)</sup> | L               | Din    | Write           | Active  |

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

| Item                                  | Symbol                             | Ratings                      | Unit | Remark       |
|---------------------------------------|------------------------------------|------------------------------|------|--------------|
| Voltage on any pin relative to Vss    | V <sub>IN</sub> , V <sub>OUT</sub> | -0.5 to V <sub>CC</sub> +0.5 | V    | -            |
| Voltage on Vcc supply relative to Vss | V <sub>CC</sub>                    | -0.3 to 4.0                  | V    | -            |
| Power Dissipation                     | P <sub>D</sub>                     | 1.0                          | W    | -            |
| Storage temperature                   | T <sub>STG</sub>                   | -65 to 150                   | °C   | -            |
| Operating Temperature                 | T <sub>A</sub>                     | -40 to 85                    | °C   | KM68S1000ELI |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

| Item               | Symbol          | Product           | Min                | Typ | Max                  | Unit |
|--------------------|-----------------|-------------------|--------------------|-----|----------------------|------|
| Supply voltage     | V <sub>CC</sub> | KM68S1000E Family | 2.3                | 2.5 | 2.7                  | V    |
| Ground             | V <sub>SS</sub> | All Family        | 0                  | 0   | 0                    | V    |
| Input high voltage | V <sub>IH</sub> | KM68S1000E Family | 2.0                | -   | V <sub>CC</sub> +0.3 | V    |
| Input low voltage  | V <sub>IL</sub> | KM68S1000E Family | -0.3 <sup>3)</sup> | -   | 0.6                  | V    |

Note:

1. T<sub>A</sub>=-40 to 85°C, otherwise specified
2. Overshoot : V<sub>CC</sub>+1.0V in case of pulse width≤20ns
3. Undershoot : -1.0V in case of pulse width≤20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

| Item                     | Symbol          | Test Condition      | Min | Max | Unit |
|--------------------------|-----------------|---------------------|-----|-----|------|
| Input capacitance        | C <sub>IN</sub> | V <sub>IN</sub> =0V | -   | 8   | pF   |
| Input/Output capacitance | C <sub>IO</sub> | V <sub>IO</sub> =0V | -   | 10  | pF   |

1. Capacitance is sampled, not 100% tested

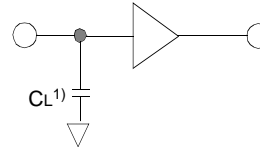
## DC AND OPERATING CHARACTERISTICS

| Item                           | Symbol           | Test Conditions  | Min | Typ | Max | Unit |
|--------------------------------|------------------|--|-----|-----|-----|------|
| Input leakage current          | I <sub>LI</sub>  | V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>  | -1  | -   | 1   | μA   |
| Output leakage current         | I <sub>LO</sub>  | $\overline{CS_1}$ =V <sub>IH</sub> or CS <sub>2</sub> =V <sub>IL</sub> or $\overline{OE}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub> | -1  | -   | 1   | μA   |
| Operating power supply current | I <sub>CC</sub>  | I <sub>IO</sub> =0mA, $\overline{CS_1}$ =V <sub>IL</sub> , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , Read   | -   | -   | 1   | mA   |
| Average operating current      | I <sub>CC1</sub> | Cycle time=1μs, 100%duty, I <sub>IO</sub> =0mA, $\overline{CS_1}$ ≤0.2V, CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V   | -   | -   | 2   | mA   |
|                                | I <sub>CC2</sub> | Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS_1}$ =V <sub>IL</sub> , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>                         | -   | -   | 15  | mA   |
| Output low voltage             | V <sub>OL</sub>  | I <sub>OL</sub> =0.5mA   | -   | -   | 0.4 | V    |
| Output high voltage            | V <sub>OH</sub>  | I <sub>OH</sub> =-0.5mA  | 2.0 | -   | -   | V    |
| Standby Current(TTL)           | I <sub>SB</sub>  | $\overline{CS_1}$ =V <sub>IH</sub> , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>  | -   | -   | 0.3 | mA   |
| Standby Current(CMOS)          | I <sub>SB1</sub> | $\overline{CS_1}$ ≥V <sub>CC</sub> -0.2V, CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V or CS <sub>2</sub> ≤0.2V, Other inputs=0~V <sub>CC</sub>  | -   | 0.2 | 10  | μA   |

## AC OPERATING CONDITIONS

### TEST CONDITIONS( Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 1.1V  
 Output load(see right) :  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS ( $V_{CC}=2.3\sim 2.7\text{V}$ , $T_A=-40$ to $85^\circ\text{C}$ )

| Parameter List |                                 | Symbol                              | Speed Bins |     |       |     | Units |
|----------------|---------------------------------|-------------------------------------|------------|-----|-------|-----|-------|
|                |                                 |                                     | 85ns       |     | 100ns |     |       |
|                |                                 |                                     | Min        | Max | Min   | Max |       |
| Read           | Read cycle time                 | t <sub>RC</sub>                     | 85         | -   | 100   | -   | ns    |
|                | Address access time             | t <sub>AA</sub>                     | -          | 85  | -     | 100 | ns    |
|                | Chip select to output           | t <sub>CO1</sub> , t <sub>CO2</sub> | -          | 85  | -     | 100 | ns    |
|                | Output enable to valid output   | t <sub>OE</sub>                     | -          | 40  | -     | 50  | ns    |
|                | Chip select to low-Z output     | t <sub>LZ</sub>                     | 10         | -   | 10    | -   | ns    |
|                | Output enable to low-Z output   | t <sub>OLZ</sub>                    | 5          | -   | 5     | -   | ns    |
|                | Chip disable to high-Z output   | t <sub>HZ</sub>                     | 0          | 25  | 0     | 30  | ns    |
|                | Output disable to high-Z output | t <sub>OHZ</sub>                    | 0          | 25  | 0     | 30  | ns    |
|                | Output hold from address change | t <sub>OH</sub>                     | 10         | -   | 15    | -   | ns    |
| Write          | Write cycle time                | t <sub>WC</sub>                     | 85         | -   | 100   | -   | ns    |
|                | Chip select to end of write     | t <sub>CW</sub>                     | 70         | -   | 80    | -   | ns    |
|                | Address set-up time             | t <sub>AS</sub>                     | 0          | -   | 0     | -   | ns    |
|                | Address valid to end of write   | t <sub>AW</sub>                     | 70         | -   | 80    | -   | ns    |
|                | Write pulse width               | t <sub>WP</sub>                     | 60         | -   | 70    | -   | ns    |
|                | Write recovery time             | t <sub>WR</sub>                     | 0          | -   | 0     | -   | ns    |
|                | Write to output high-Z          | t <sub>WHZ</sub>                    | 0          | 25  | 0     | 30  | ns    |
|                | Data to write time overlap      | t <sub>DW</sub>                     | 35         | -   | 40    | -   | ns    |
|                | Data hold from write time       | t <sub>DH</sub>                     | 0          | -   | 0     | -   | ns    |
|                | End write to output low-Z       | t <sub>OW</sub>                     | 5          | -   | 5     | -   | ns    |

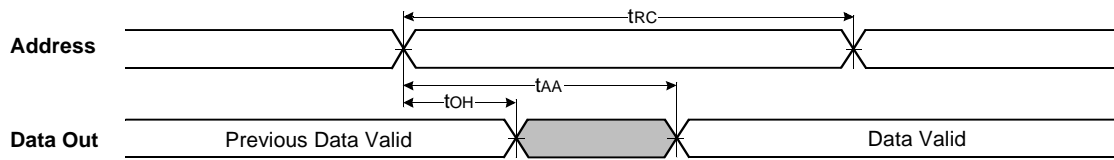
## DATA RETENTION CHARACTERISTICS

| Item                               | Symbol           | Test Condition   | Min | Typ | Max | Unit          |
|------------------------------------|------------------|--|-----|-----|-----|---------------|
| V <sub>CC</sub> for data retention | V <sub>DR</sub>  | $\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$                        | 2.0 | -   | 2.7 | V             |
| Data retention current             | I <sub>DR</sub>  | $V_{CC}=2.5\text{V}$ , $\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$ | -   | 0.2 | 10  | $\mu\text{A}$ |
| Data retention set-up time         | t <sub>SDR</sub> | See data retention waveform  | 0   | -   | -   | ms            |
| Recovery time                      | t <sub>RDR</sub> |  | 5   | -   | -   |               |

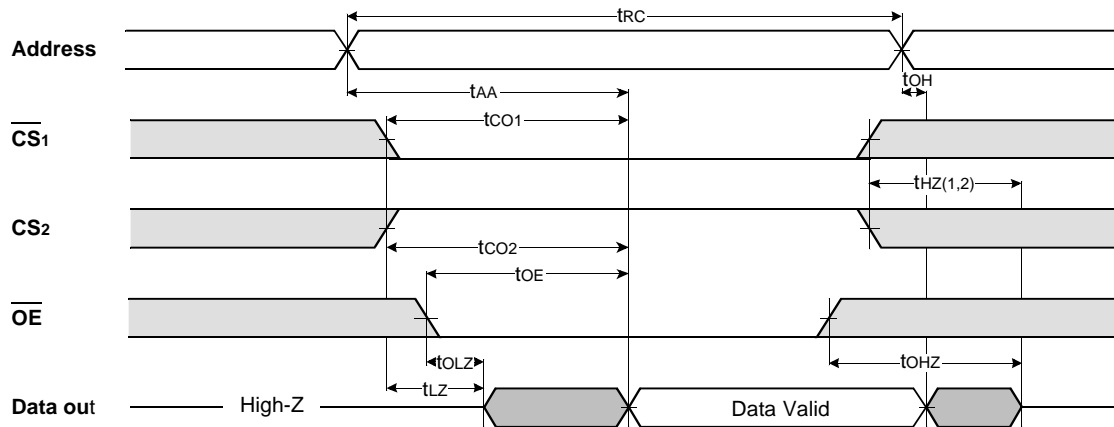
1.  $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$ ,  $\overline{CS}_2 \geq V_{CC}-0.2\text{V}$ ( $\overline{CS}_1$  controlled) or  $\overline{CS}_2 \leq 0.2\text{V}$ ( $\overline{CS}_2$  controlled)

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ )



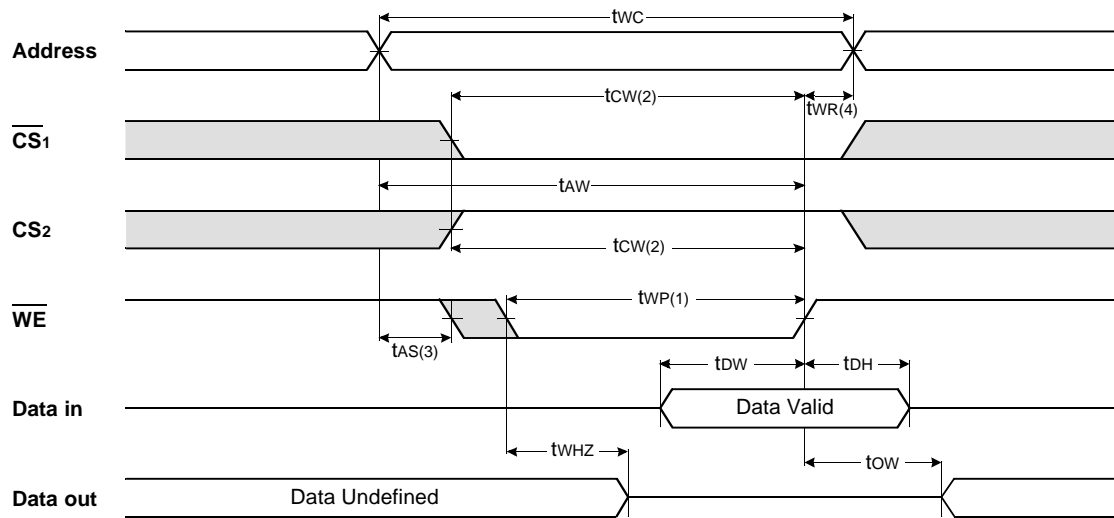
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



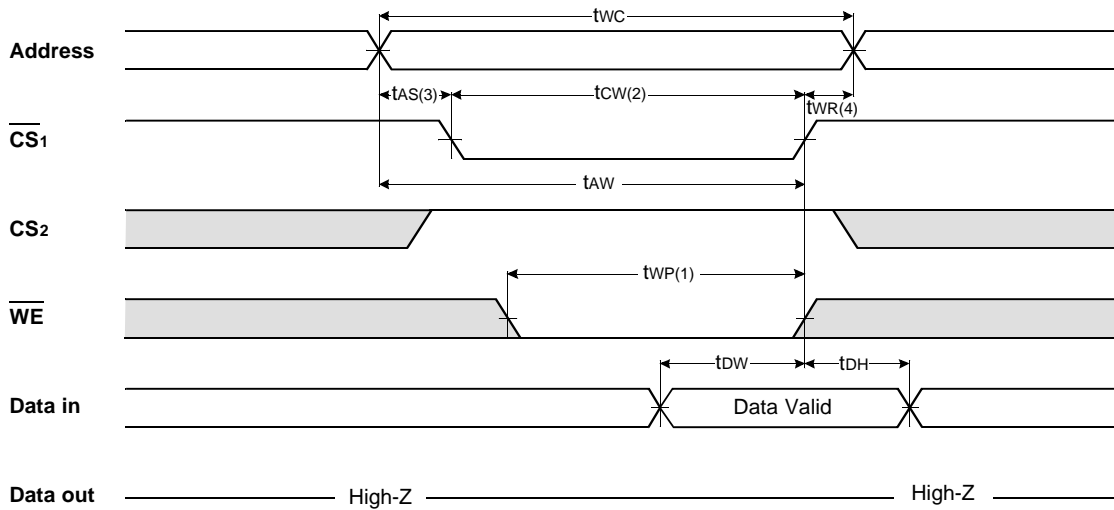
### NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

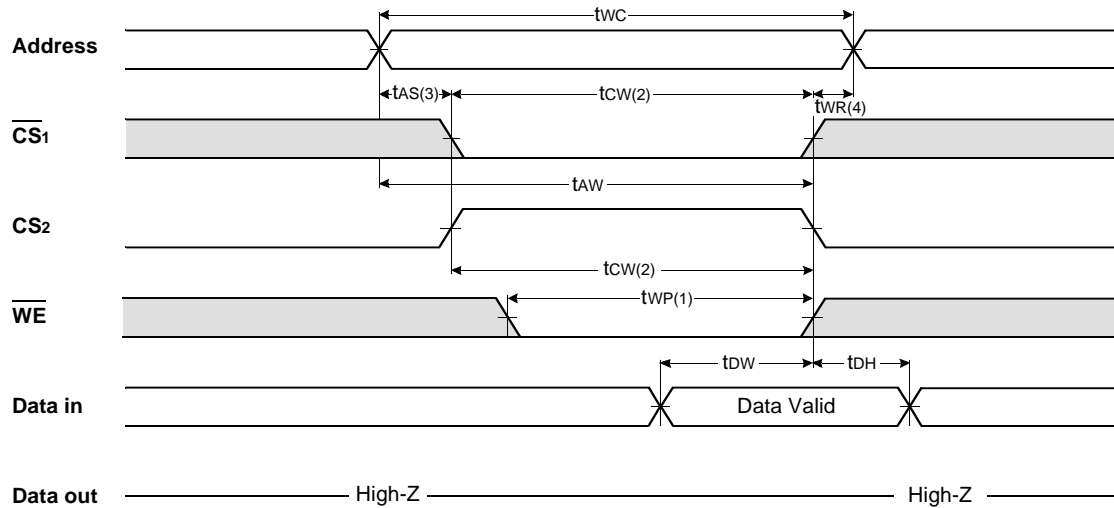
**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{\text{WE}}$  Controlled)**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{\text{CS}}_1$  Controlled)**



## TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

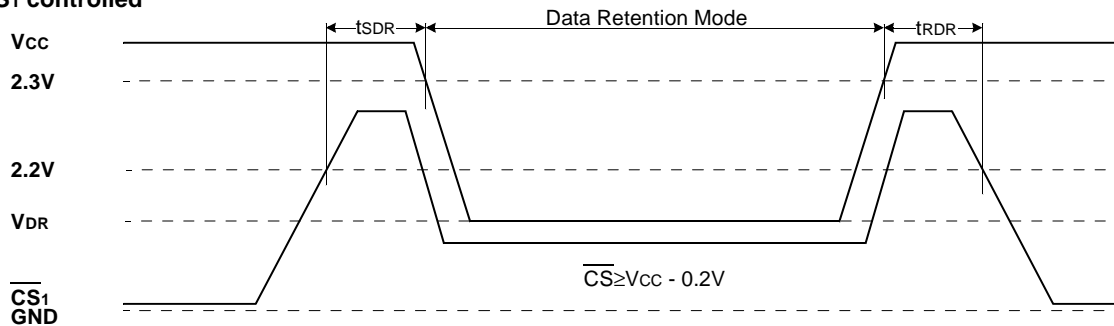


### NOTES (WRITE CYCLE)

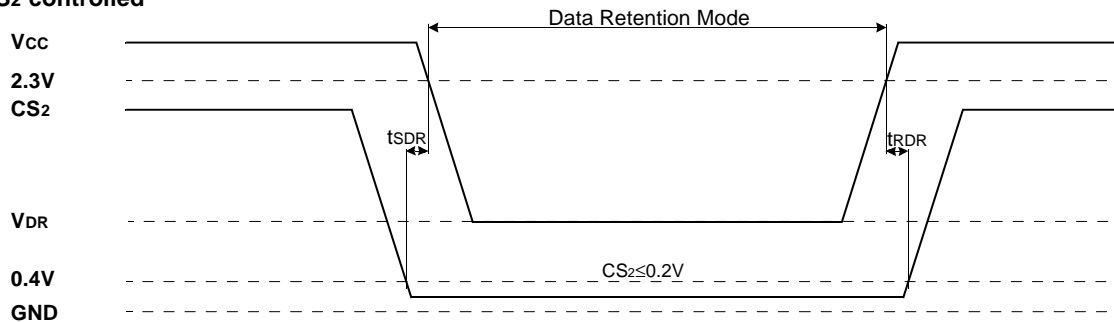
1. A write occurs during the overlap of a low  $\overline{CS_1}$ , a high CS<sub>2</sub> and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS_1}$  goes low, CS<sub>2</sub> going high and WE going low : A write ends at the earliest transition among CS<sub>1</sub> going high, CS<sub>2</sub> going low and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the CS<sub>1</sub> going low or CS<sub>2</sub> going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR<sub>1</sub> applied in case a write ends as  $\overline{CS_1}$  or  $\overline{WE}$  going high tWR<sub>2</sub> applied in case a write ends as CS<sub>2</sub> going to low.

## DATA RETENTION WAVE FORM

### CS<sub>1</sub> controlled



### CS<sub>2</sub> controlled





## Units: millimeters(inches)

The drawing shows the mechanical specifications for the 16-pin connector. The top view shows a rectangular body with two rows of pins, labeled #1 to #16 on the left and #32 to #17 on the right. The overall length is  $20.00 \pm 0.20$  (0.787 ± 0.008). The pin pitch is  $0.20 \pm 0.10$  (-0.05) (0.006 ± 0.004) (0.002). The pin diameter is  $0.50 \pm 0.0197$ . The side view shows the connector's profile with a maximum height of  $8.40 \pm 0.331$  (MAX) (8.00 ± 0.315). The pin height is  $1.00 \pm 0.10$  (0.039 ± 0.004) (1.20 ± 0.047) (MAX). The pin thickness is  $0.15 \pm 0.10$  (-0.05) (0.006 ± 0.004) (0.002). The pin width is  $0.25 \pm 0.10$  (-0.05) (0.018 ± 0.030). The pin angle is  $0-8^\circ$ . The pin length is  $0.45 \pm 0.75$  (-0.030) (0.018 ± 0.030). The pin thickness is  $0.10 \pm 0.004$  (MAX) (0.004 ± 0.004) (MAX).

Technical drawing of a rectangular component with dimensions and tolerances. The drawing includes a top view and a side view.

**Top View Dimensions:**

- Overall width:  $13.40 \pm 0.20$
- Overall height:  $0.528 \pm 0.008$
- Left side features:
  - Top left corner:  $0.20 \begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$
  - Top left corner:  $0.008 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$
  - Left side feature:  $0.50 \begin{smallmatrix} 0.0197 \end{smallmatrix}$
- Right side features:
  - Top right corner:  $0.10 \begin{smallmatrix} \text{MAX} \\ 0.004 \end{smallmatrix}$
  - Right side feature:  $0.25 \begin{smallmatrix} ( \\ 0.010 \end{smallmatrix}$

**Side View Dimensions:**

- Overall height:  $8.40 \begin{smallmatrix} 0.331 \end{smallmatrix}$
- Internal height:  $8.00 \begin{smallmatrix} 0.315 \end{smallmatrix}$
- Bottom left corner:  $0.25 \begin{smallmatrix} \text{TYP} \\ 0.010 \end{smallmatrix}$
- Bottom left corner:  $0.45-0.75 \begin{smallmatrix} 0.018-0.030 \end{smallmatrix}$
- Bottom right corner:  $0.15 \begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$
- Bottom right corner:  $0.006 \begin{smallmatrix} +0.004 \\ -0.002 \end{smallmatrix}$
- Bottom right corner:  $0.50 \begin{smallmatrix} ( \\ 0.020 \end{smallmatrix}$
- Bottom right corner:  $0.05 \begin{smallmatrix} \text{MIN} \\ 0.002 \end{smallmatrix}$
- Bottom right corner:  $1.20 \begin{smallmatrix} \text{MAX} \\ 0.047 \end{smallmatrix}$
- Bottom right corner:  $1.00 \begin{smallmatrix} \pm 0.10 \\ 0.039 \pm 0.004 \end{smallmatrix}$