

**Document Title****64Kx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
0.0	Design target	January 17, 1996	Advance
0.1	Initial draft - One datasheet for commercial, extended and industrial product. - Add 85ns part on KM68V512A Family.	April 15, 1996	Preliminary
1.0	Finalize	June 17, 1996	Final
2.0	Revise - Add 32-sTSOP type package on product.	September 10, 1996	Final
3.0	Revise - Change datasheet format - Improve power dissipation 0.7 to 1.0W	February 12, 1998	Final

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## 64Kx8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology : Poly Load
- Organization : 64Kx8
- Power Supply Voltage
  - KM68V512A family : 2.7~3.3V
  - KM68U512A family : 3.0~3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-SOP-525, 32-TSOP1-0820F, 32-TSOP1-0813.4F

### GENERAL DESCRIPTION

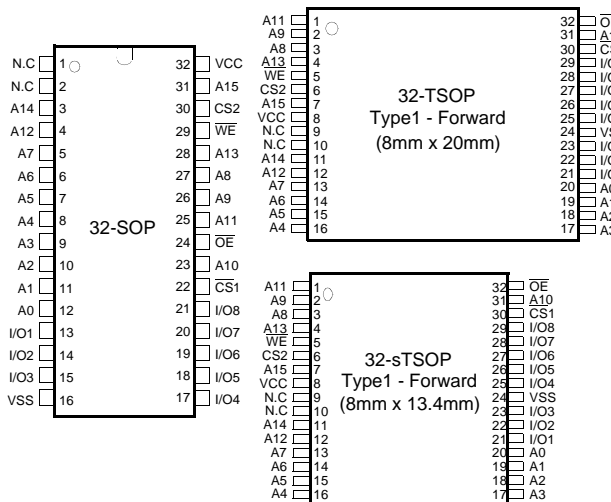
The KM68V512A and KM68U512A families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
KM68V512AL-L	Commercial(0~70°C)	3.0 ~ 3.6V	70 <sup>1)</sup> /85/100	10μA	40mA	32-SOP 32-TSOP1-F 32-sTSOP1-F
KM68U512AL-L		2.7 ~ 3.3V	85 <sup>1)</sup> /100	10μA		
KM68V512ALE-L	Extended(-25~85°C)	3.0 ~ 3.6V	70 <sup>1)</sup> /85/100	20μA		
KM68U512ALE-L		2.7 ~ 3.3V	85 <sup>1)</sup> /100	15μA		
KM68V512ALI-L	Industrial (-40~85°C)	3.0 ~ 3.6V	70 <sup>1)</sup> /85/100	20μA		
KM68U512ALI-L		2.7 ~ 3.3V	85 <sup>1)</sup> /100	15μA		

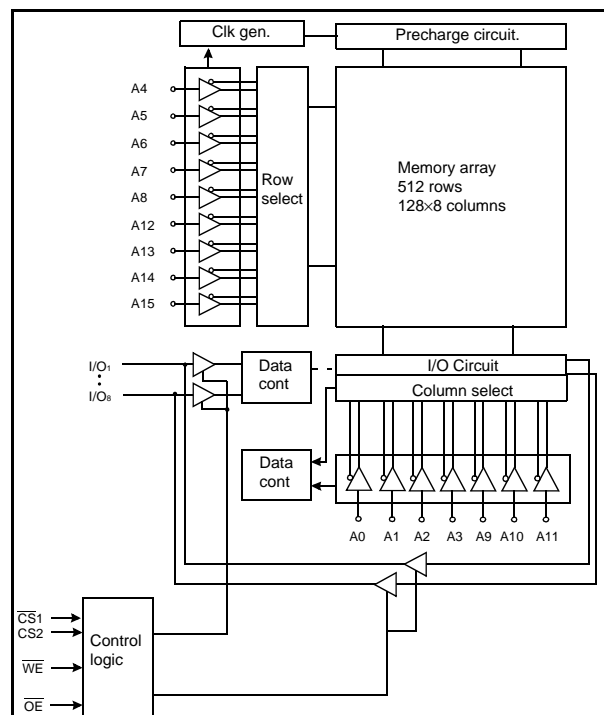
1. The parameter is measured with 30pF test load.

### PIN DESCRIPTION



Name	Function
CS1, CS2	Chip Select Inputs
OE	Output Enable Input
WE	Write Enable Input
A0~A15	Address Inputs
I/O0~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Temperature Products (0~70°C)		Extended Temperature Products (-25~85°C)		Industrial Temperature Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V512ALG-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGE-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGI-7L	32-SOP, 70ns, 3.3V, LL
KM68V512ALG-8L	32-SOP, 85ns, 3.3V, LL	KM68V512ALGE-8L	32-SOP, 85ns, 3.3V, LL	KM68V512ALGI-8L	32-SOP, 85ns, 3.3V, LL
KM68V512ALG-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGE-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGI-10L	32-SOP, 100ns, 3.3V, LL
KM68V512ALT-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTE-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTI-7L	32-TSOP F, 70ns, 3.3V, LL
KM68V512ALT-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V512ALTE-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V512ALTI-8L	32-TSOP F, 85ns, 3.3V, LL
KM68V512ALT-10L	32-TSOP F, 100ns, 3.3V, LL	KM68V512ALTE-10L	32-TSOP F, 100ns, 3.3V, LL	KM68V512ALTI-10L	32-TSOP F, 100ns, 3.3V, LL
KM68V512ALTG-7L	32-sTSOP F, 70ns, 3.3V, LL	KM68V512ALTGE-7L	32-sTSOP F, 70ns, 3.3V, LL	KM68V512ALTGI-7L	32-sTSOP F, 70ns, 3.3V, LL
KM68V512ALTG-8L	32-sTSOP F, 85ns, 3.3V, LL	KM68V512ALTGE-8L	32-sTSOP F, 85ns, 3.3V, LL	KM68V512ALTGI-8L	32-sTSOP F, 85ns, 3.3V, LL
KM68V512ALTG-10L	32-sTSOP F, 100ns, 3.3V, LL	KM68V512ALTGE-10L	32-sTSOP F, 100ns, 3.3V, LL	KM68V512ALTGI-10L	32-sTSOP F, 100ns, 3.3V, LL
KM68U512ALG-8L	32-SOP, 85ns, 3.0V, LL	KM68U512ALGE-8L	32-SOP, 85ns, 3.0V, LL	KM68U512ALGI-8L	32-SOP, 85ns, 3.0V, LL
KM68U512ALG-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGE-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGI-10L	32-SOP, 100ns, 3.0V, LL
KM68U512ALT-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U512ALTE-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U512ALTI-8L	32-TSOP F, 85ns, 3.0V, LL
KM68U512ALT-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTE-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTI-10L	32-TSOP F, 100ns, 3.0V, LL
KM68U512ALTG-8L	32-sTSOP F, 85ns, 3.0V, LL	KM68U512ALTGE-8L	32-sTSOP F, 85ns, 3.0V, LL	KM68U512ALTGI-8L	32-sTSOP F, 85ns, 3.0V, LL
KM68U512ALTG-10L	32-sTSOP F, 100ns, 3.0V, LL	KM68U512ALTGE-10L	32-sTSOP F, 100ns, 3.0V, LL	KM68U512ALTGI-10L	32-sTSOP F, 100ns, 3.0V, LL

## FUNCTIONAL DESCRIPTION

CS <sub>1</sub>	CS <sub>2</sub>	OE	WE	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care(Must be low or high state.)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V	-
Voltage on Vcc supply relative to	V <sub>CC</sub>	-0.3 to 4.6	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM68V512AL-L, KM68U512AL-L
		-25 to 85	°C	KM68V512ALE-L, KM68U512ALE-L
		-40 to 85	°C	KM68V512ALI-L, KM68U512ALI-L
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	KM68V512A Family	3.0	3.3	3.6	V
		KM68U512A Family	2.7	3.0	3.3	V
Ground	V <sub>SS</sub>	All Family	0	0	0	V
Input high voltage	V <sub>IH</sub>	KM68V512A, KM68U512A Family	2.2	-	V <sub>CC</sub> +0.3V <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	KM68V512A, KM68U512A Family	-0.3 <sup>3)</sup>	-	0.4	V

Note:

- Commercial Product : T<sub>A</sub>=0 to 70°C, otherwise specified  
Extended Product : T<sub>A</sub>=-25 to 85°C, otherwise specified  
Industrial Product : T<sub>A</sub>=-40 to 85°C, otherwise specified
- Overshoot : V<sub>CC</sub>+3.0V in case of pulse width≤30ns
- Undershoot : -3.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

- Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or CS <sub>2</sub> =V <sub>IL</sub> or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	5	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1 \leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	5	mA	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	40	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.3	mA	
Standby Current(CMOS)	I <sub>SB1</sub>		KM68V512AL-L	-	-	10	μA
			KM68V512ALE-L KM68V512ALI-L	-	-	20	μA
			KM68U512AL-L	-	-	10	μA
			KM68U512ALE-L KM68U512ALI-L	-	-	15	μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V

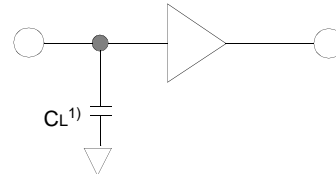
Input rising and falling time : 5ns

Input and output reference voltage : 1.5V

Output load(see right) :  $C_L=100\text{pF}+1\text{TTL}$

<sup>1)</sup> $C_L=30\text{pF}+1\text{TTL}$

1. KM68V512AL-7L Family, KM68U512AL-8L Family



1. Including scope and jig capacitance

## AC CHARACTERISTICS

(KM68V512B Family:  $V_{CC}=3.0\sim 3.6\text{V}$ , KM68U512B Family:  $V_{CC}=2.7\sim 3.3\text{V}$ ,

Commercial product:  $T_A=0$  to  $70^\circ\text{C}$ , Extended product:  $T_A=-25$  to  $85^\circ\text{C}$ , Industrial product:  $T_A=-40$  to  $85^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	45	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	20	0	20	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tdW	30	-	35	-	40	-	ns
	Data hold from write time	tdH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

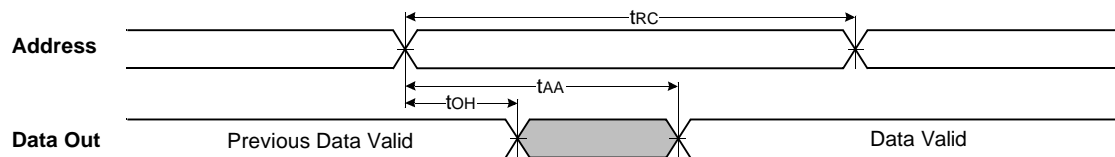
## DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR		$\overline{\text{CS}}_1^{1)} \geq V_{\text{cc}} - 0.2\text{V}$	2.0	-	3.6	V
Data retention current	IDR	KM68V512AL-L	$V_{\text{cc}} = 3.0\text{V}$ , $\overline{\text{CS}}_1 \geq V_{\text{cc}} - 0.2\text{V}$ , $\text{CS}_2 \geq V_{\text{cc}} - 0.2\text{V}$ or $\text{CS}_2 \leq 0.2\text{V}$	-	-	10	$\mu\text{A}$
		KM68V512ALE-L		-	-	15	
		KM68V512ALI-L		-	-	15	
		KM68U512AL-L		-	-	8	
		KM68U512ALE-L		-	-	10	
		KM68U512ALI-L		-	-	10	
Data retention set-up time	tSDR		See data retention waveform	0	-	-	ms
Recovery time	tRDR			5	-	-	

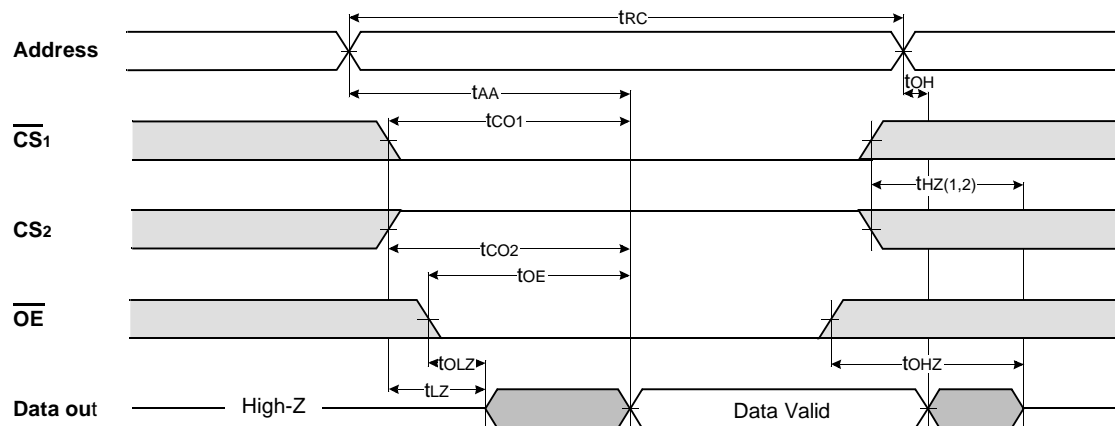
1.  $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$ ,  $CS_2 \geq V_{CC}-0.2\text{V}$  ( $\overline{CS}_1$  controlled) or  $CS_2 \leq 0.2\text{V}$  ( $CS_2$  controlled)

## TIMMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}_1 = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



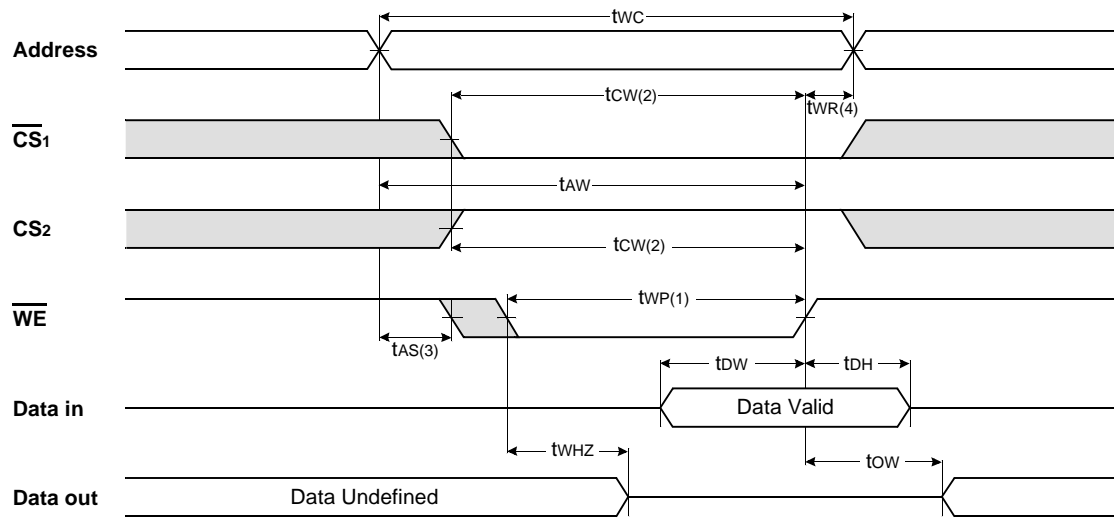
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE} = V_{IH}$ )



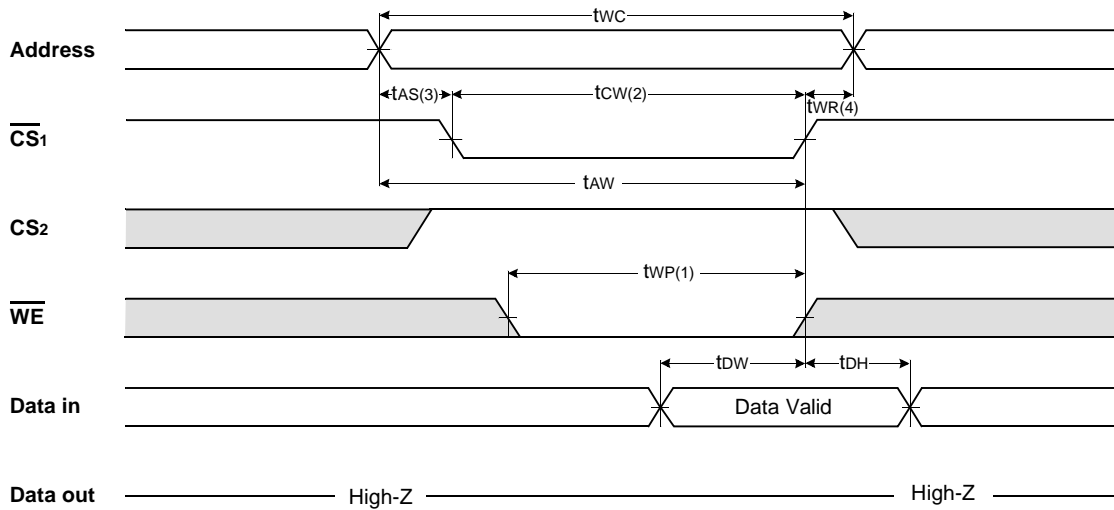
### NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

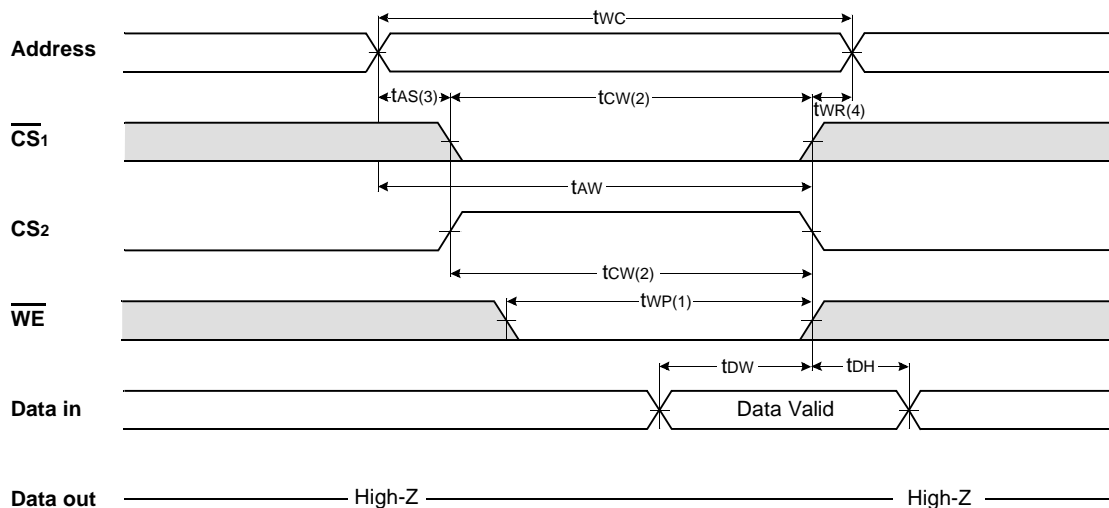
**TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)**



**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)**



## TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}_1$ Controlled)

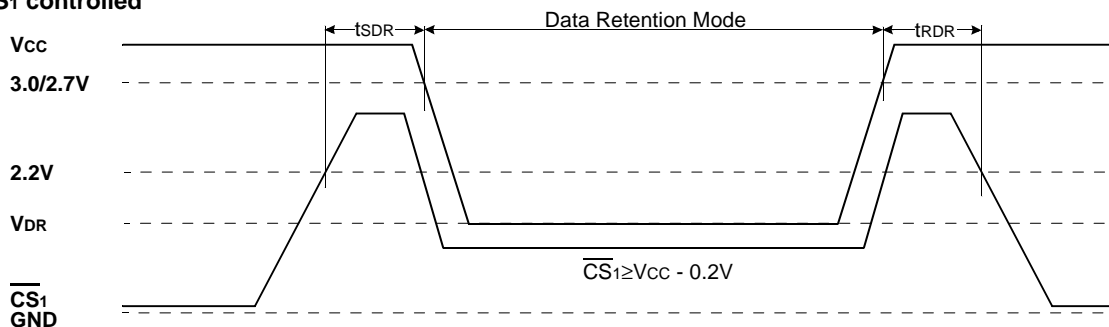


### NOTES (WRITE CYCLE)

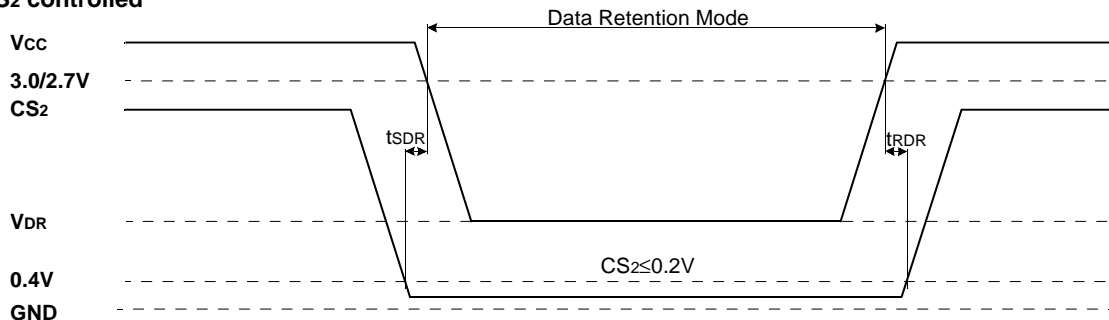
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  going low,  $CS_2$  going high and  $\overline{WE}$  going low : A write ends at the earliest transition among  $\overline{CS}_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR(1)}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR(2)}$  applied in case a write ends as  $CS_2$  going to low.

## DATA RETENTION WAVE FORM

### $\overline{CS}_1$ controlled



### $CS_2$ controlled

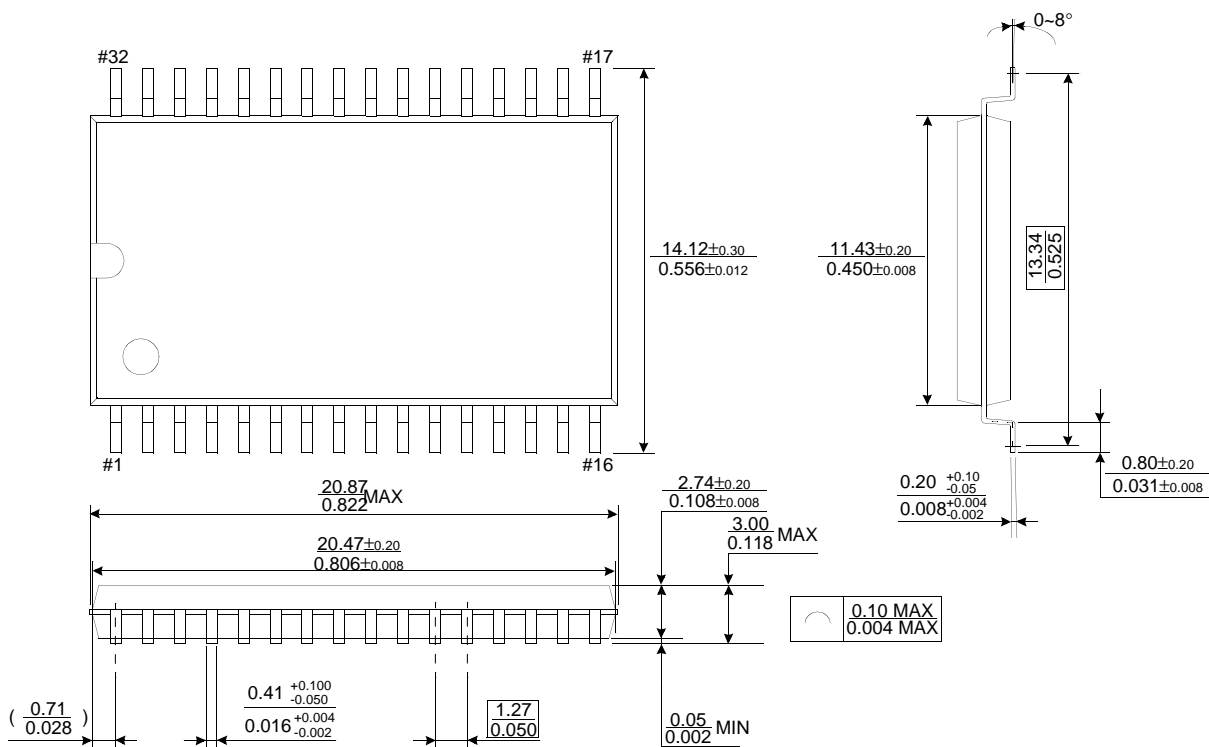




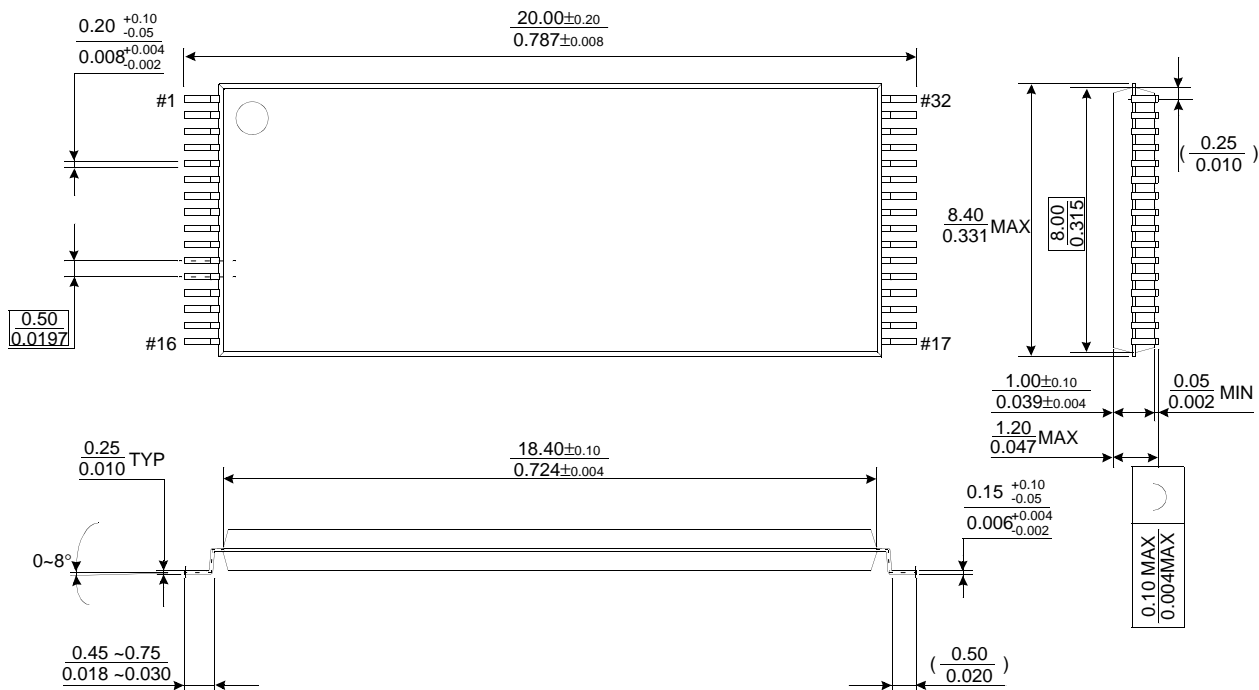
## PACKAGE DIMENSIONS

Units : millimeter(inch)

### 32 PIN SMALL OUTLINE PACKAGE (525mil)



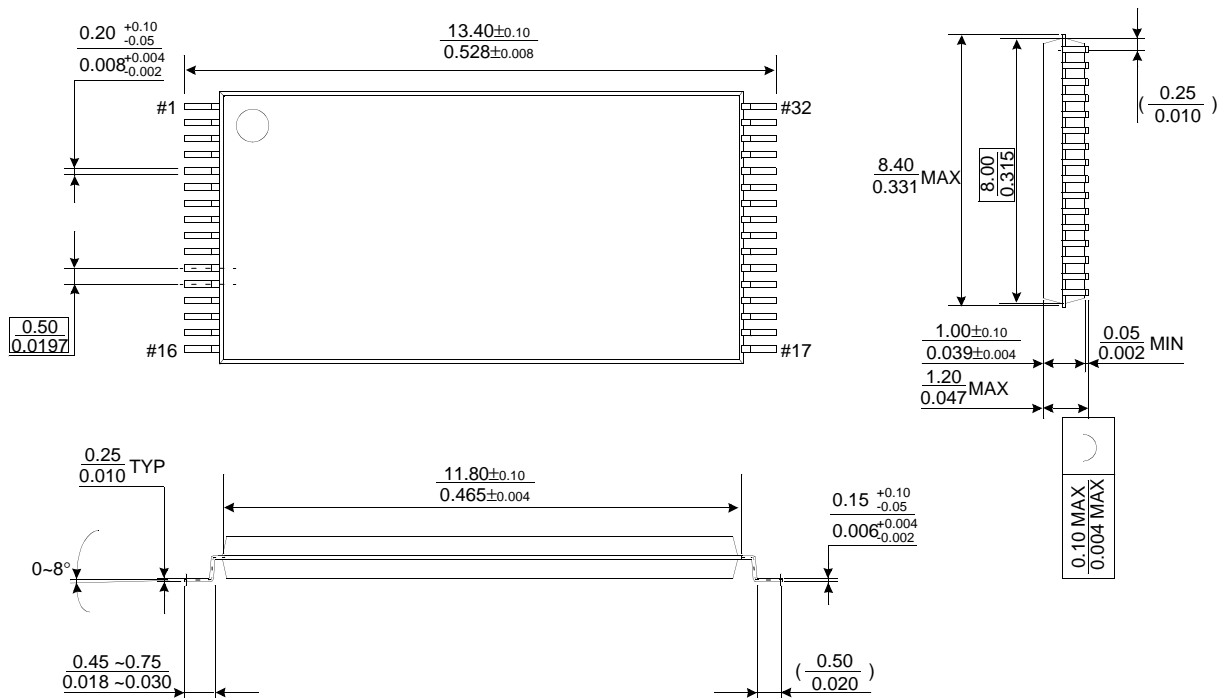
### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



## PACKAGE DIMENSIONS

Units : millimeter(inch)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)

