

Document Title

512Kx8 Bit High Speed Static RAM(3.3V Operating).
Operated at Commercial and Industrial Temperature Ranges.

Revision History

<u>RevNo.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>																										
Rev. 0.0	Initial release with Design Target.	Jan. 1st, 1997	Design Target																										
Rev. 1.0	Release to Preliminary Data Sheet. 1.1. Replace Design Target to Preliminary.	Jun. 1st, 1997	Preliminary																										
Rev. 2.0	Release to Final Data Sheet. 2.1. Delete Preliminary. 2.2. Add 30pF capacitive in test load. 2.3. Relax DC characteristics.	Feb.11th.1998	Final																										
<table><tr><th colspan="2">Item</th><th>Previous</th><th>Current</th></tr><tr><td rowspan="3">Icc</td><td>10ns</td><td>170mA</td><td>205mA</td></tr><tr><td>12ns</td><td>160mA</td><td>200mA</td></tr><tr><td>15ns</td><td>150mA</td><td>195mA</td></tr><tr><td>ISB</td><td>f=max.</td><td>40mA</td><td>50mA</td></tr><tr><td>ISB1</td><td>f=0</td><td>10 / 1mA</td><td>10 / 1.2mA</td></tr><tr><td>IDR</td><td>VDR=3.0V</td><td>0.9mA</td><td>1.0mA</td></tr></table>				Item		Previous	Current	Icc	10ns	170mA	205mA	12ns	160mA	200mA	15ns	150mA	195mA	ISB	f=max.	40mA	50mA	ISB1	f=0	10 / 1mA	10 / 1.2mA	IDR	VDR=3.0V	0.9mA	1.0mA
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Rev. 2.1	Change operating current at Industrial Temperature range.	Jun.27th 1998	Final																										
	<table><tr><td>Items</td><td>Previous spec. (10/12/15ns part)</td><td>Changed spec. (10/12/15ns part)</td></tr><tr><td>Icc</td><td>205/200/195mA</td><td>230/225/220mA</td></tr></table>	Items	Previous spec. (10/12/15ns part)	Changed spec. (10/12/15ns part)	Icc	205/200/195mA	230/225/220mA																						
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The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

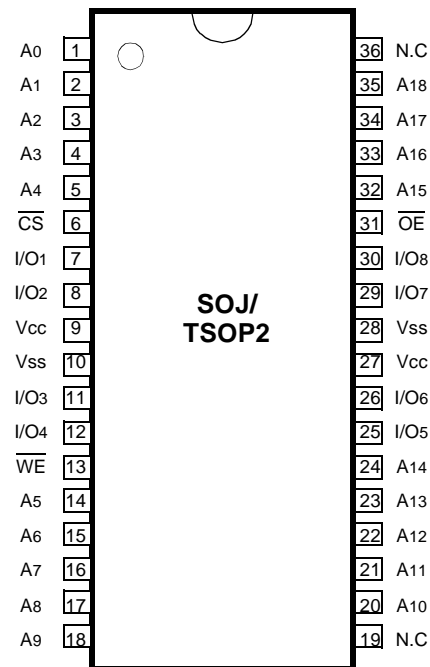


512K x 8 Bit High-Speed CMOS Static RAM(3.3V Operating)
FEATURES

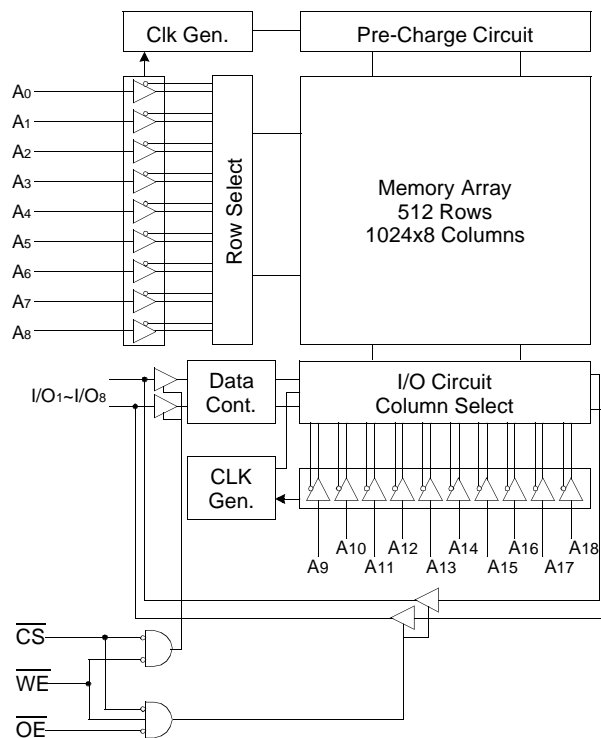
- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 50mA(Max.)
 - (CMOS) : 10mA(Max.)
 - 1.2mA(Max.)- L-Ver.
- Operating KM68V4002B/BL - 10 : 205mA(Max.)
- KM68V4002B/BL - 12 : 200mA(Max.)
- KM68V4002B/BL - 15 : 195mA(Max.)
- Single 3.3 ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention ; L-Ver. only
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
 - KM68V4002BJ : 36-SOJ-400
 - KM68V4002BT : 36-TSOP2-400F

GENERAL DESCRIPTION

The KM68V4002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68V4002B uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAM-SUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V4002B is packaged in a 400 mil 36-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION (Top View)

ORDERING INFORMATION

KM68V4002B/BL -10/12/15	Commercial Temp.
KM68V4002BI/BLI -10/12/15	Industrial Temp.

FUNCTIONAL BLOCK DIAGRAM

PIN FUNCTION

Pin Name	Pin Function
A0 - A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V _{CC}	-0.5 to 4.6	V
Power Dissipation		P _D	1.0	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3***	V
Input Low Voltage	V _{IL}	-0.3**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.

** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

*** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}		-2	2	μA
Output Leakage Current	I _{LO}	\overline{CS} =V _{IH} or \overline{OE} =V _{IH} or \overline{WE} =V _{IL} V _{OUT} =V _{SS} to V _{CC}		-2	2	μA
Operating Current	I _{CC}	Min. Cycle, 100% Duty \overline{CS} =V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	10ns	-	205	mA
			12ns	-	200	
			15ns	-	195	
Standby Current	I _{SB}	Min. Cycle, \overline{CS} =V _{IH}		-	50	mA
	I _{SB1}	f=0MHz, \overline{CS} ≥V _{CC} -0.2V, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V	Normal	-	10	mA
			L-Ver.	-	1.2	
Output Low Voltage Level	V _{OL}	I _{OL} =8mA		-	0.4	V
Output High Voltage Level	V _{OH}	I _{OH} =-4mA		2.4	-	V

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	7	pF

* Capacitance is sampled and not 100% tested.

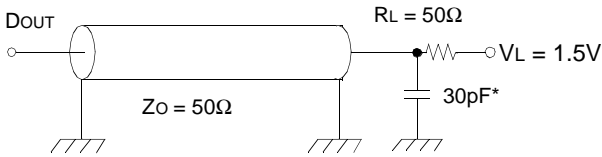
AC CHARACTERISTICS (T_A=0 to 70°C, V_{CC}=3.3±0.3V, unless otherwise noted.)

TEST CONDITIONS*

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

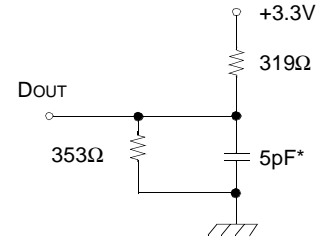
* The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	KM68V4002B/BL-10		KM68V4002B/BL-12		KM68V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t _{CO}	-	10	-	12	-	15	ns
Output Enable to Valid Output	t _{OE}	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t _{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t _{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t _{HZ}	0	5	0	6	0	7	ns
Output Disable to High-Z Output	t _{OHZ}	0	5	0	6	0	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t _{PU}	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	t _{PD}	-	15	-	12	-	15	ns

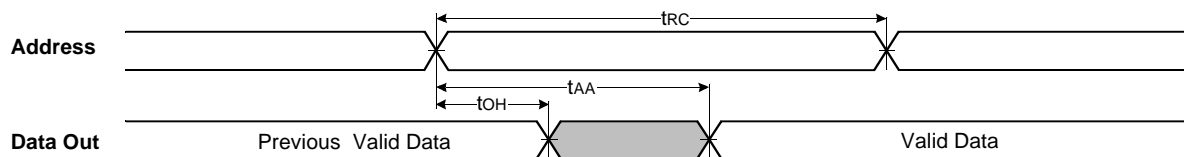
* The above parameters are also guaranteed at industrial temperature range.

WRITE CYCLE*

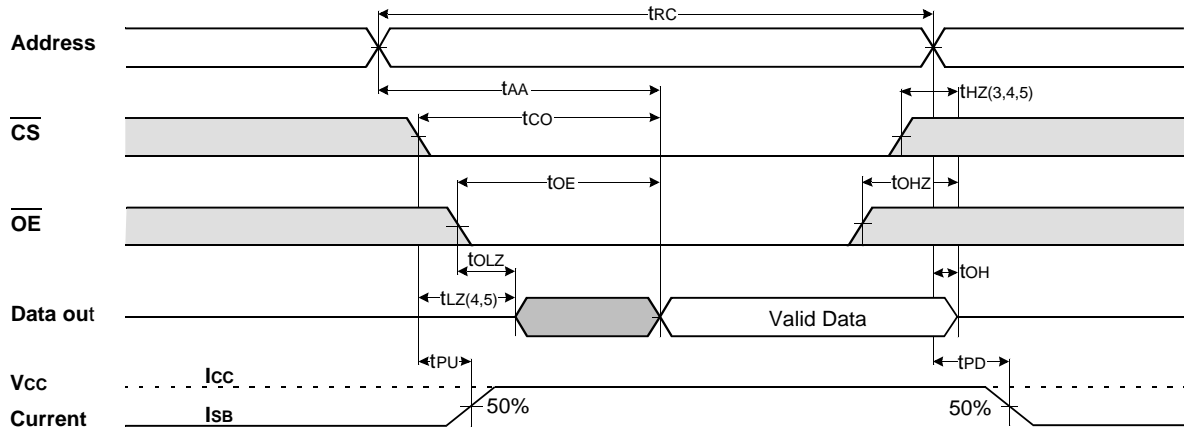
Parameter	Symbol	KM68V4002B/BL-10		KM68V4002B/BL-12		KM68V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t _{CW}	7	-	8	-	10	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	7	-	8	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ High)	t _{WP}	7	-	8	-	10	-	ns
Write Pulse Width($\overline{\text{OE}}$ Low)	t _{WP1}	10	-	12	-	15	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	ns

* The above parameters are also guaranteed at industrial temperature range.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{\text{CS}}=\overline{\text{OE}}=V_{\text{IL}}$, $\overline{\text{WE}}=V_{\text{IH}}$)

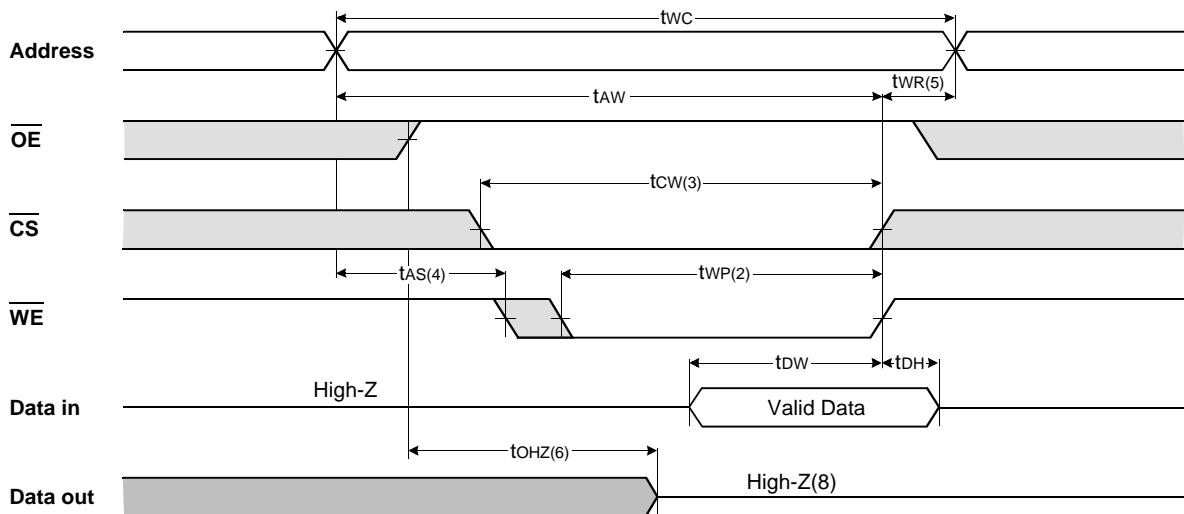
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)

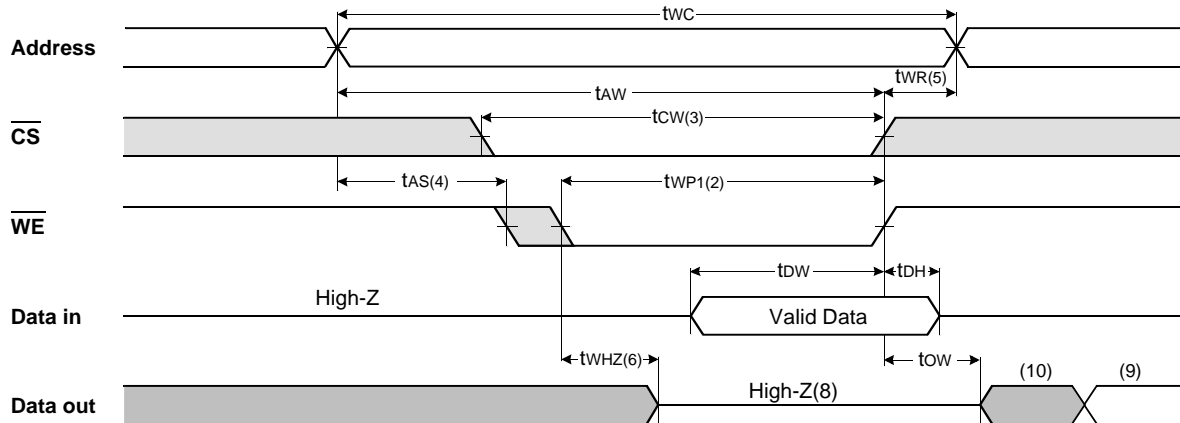
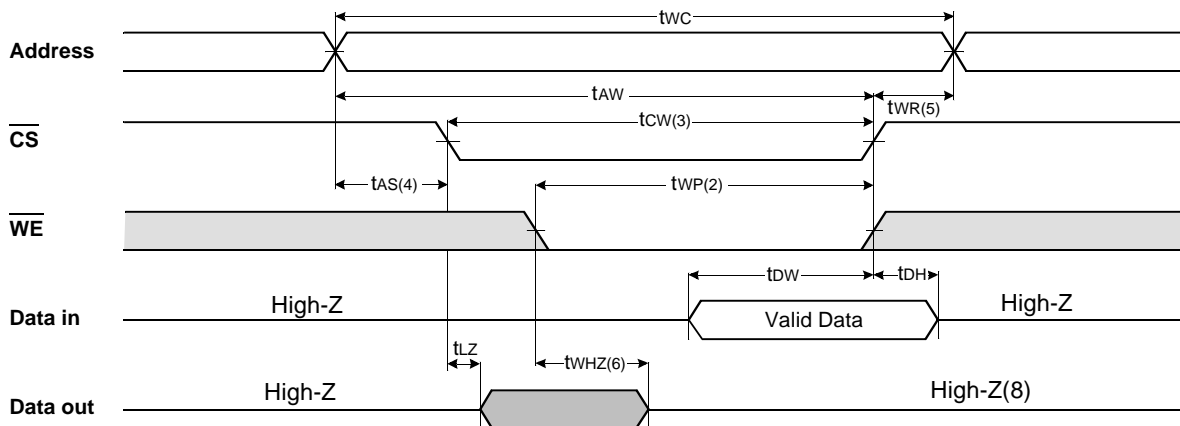


NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}=\text{Clock}$)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{OE} =Low Fixed)TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{CS} = Controlled)

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low ; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of \overline{CS} going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.
6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
9. D_{out} is the read data of the new address.
10. When \overline{CS} is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	$\text{I}_{\text{SB}}, \text{I}_{\text{SB1}}$
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	DOUT	I_{CC}
L	L	X	Write	DIN	I_{CC}

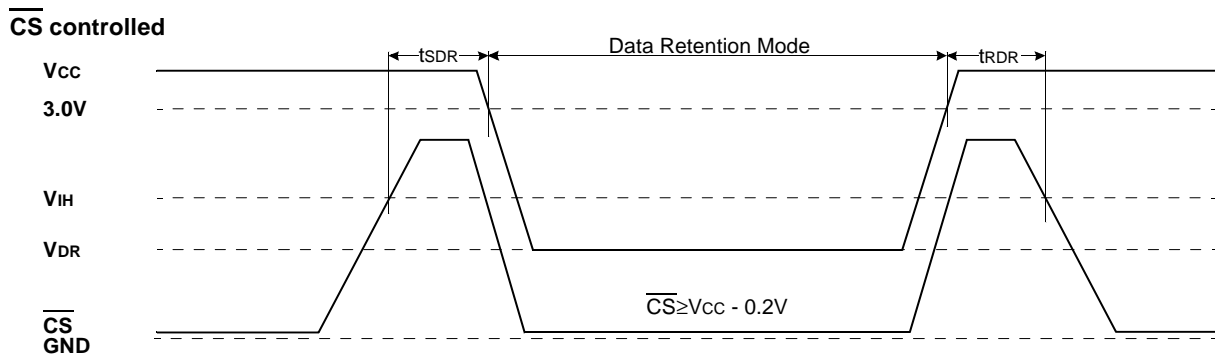
* X means Don't Care.

DATA RETENTION CHARACTERISTICS*($T_A=0$ to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V _{CC} for Data Retention	V _{DR}	$\overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$	2.0	-	3.6	V
Data Retention Current	I _{DR}	$V_{\text{CC}}=3.0\text{V}, \overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	-	-	1.0	mA
		$V_{\text{CC}} = 2.0\text{V}, \overline{\text{CS}} \geq V_{\text{CC}} - 0.2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	-	-	0.7	mA
Data Retention Set-Up Time	t _{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t _{RDR}	See Data Retention Wave form(below)	5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

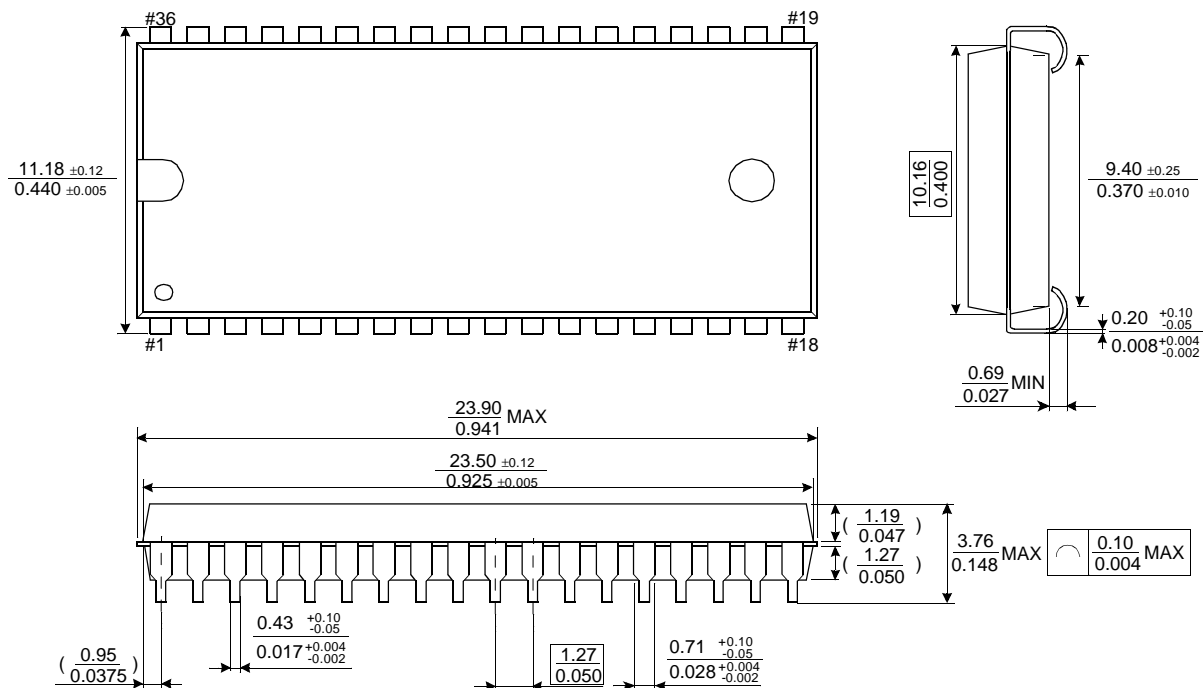
DATA RETENTION WAVE FORM



PACKAGE DIMENSIONS

Units: millimeters/Inches

36-SOJ-400



36-TSOP2-400F

