

8Mx32 SODIMM

(8Mx32 base)

Revision 0.0

Sept. 1997



ELECTRONICS

Revision History

Version 0.0 (Sept, 1997)

- Removed two AC parameters t_{CACP} (access time from $\overline{\text{CAS}}$) and t_{AAP} (access time from col. addr.) in *AC CHARACTERISTICS*.

DRAM MODULE

KMM332F803BS-L

KMM332F803BS-L EDO Mode

8M x 32 DRAM SODIMM Using 8MX8, 4K Refresh, 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM332F803B is a 8Mx32bits Dynamic RAM high density memory module. The Samsung KMM332F803B consists of four CMOS 8Mx8bits DRAMs in TSOPII packages mounted on a 72-pin zigzag glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM332F803B is a Small Out-line Dual In-line Memory Module with edge connections and is intended for mounting into 72-pin dual readout zigzag edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	13ns	90ns	25ns
-6	60ns	15ns	110ns	30ns

FEATURES

- Part Identification
 - KMM332F803BS-L5/L6
 - (4096 cycles/128ms Ref, TSOP, Low Power, 50/60ns)
- Extended Data Out Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +3.3V ± 0.3 V power supply
- JEDEC standard PDPin & pinout (72pin)
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ18
2	DQ0	38	DQ19
3	DQ1	39	$\overline{\text{Vss}}$
4	DQ2	40	$\overline{\text{CAS0}}$
5	DQ3	41	$\overline{\text{CAS2}}$
6	DQ4	42	$\overline{\text{CAS3}}$
7	DQ5	43	$\overline{\text{CAS1}}$
8	DQ6	44	$\overline{\text{RAS0}}$
9	DQ7	45	NC
10	Vcc	46	NC
11	PD1	47	$\overline{\text{W}}$
12	A0	48	NC
13	A1	49	DQ20
14	A2	50	DQ21
15	A3	51	DQ22
16	A4	52	DQ23
17	A5	53	DQ24
18	A6	54	DQ25
19	A10	55	NC
20	NC	56	DQ27
21	DQ9	57	DQ28
22	DQ10	58	DQ29
23	DQ11	59	DQ30
24	DQ12	60	DQ31
25	DQ13	61	Vcc
26	DQ14	62	DQ32
27	DQ15	63	DQ33
28	A7	64	DQ34
29	A11	65	NC
30	Vcc	66	PD2
31	A8	67	PD3
32	A9	68	PD4
33	NC	69	PD5
34	$\overline{\text{RAS2}}$	70	PD6
35	DQ16	71	PD7
36	NC	72	Vss

PIN NAMES

Pin Name	Function
A0 - 11	Address Inputs
DQ(0 -7,9-16, 18-25,27-34)	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
PD1 -PD7	Presence Detect
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection

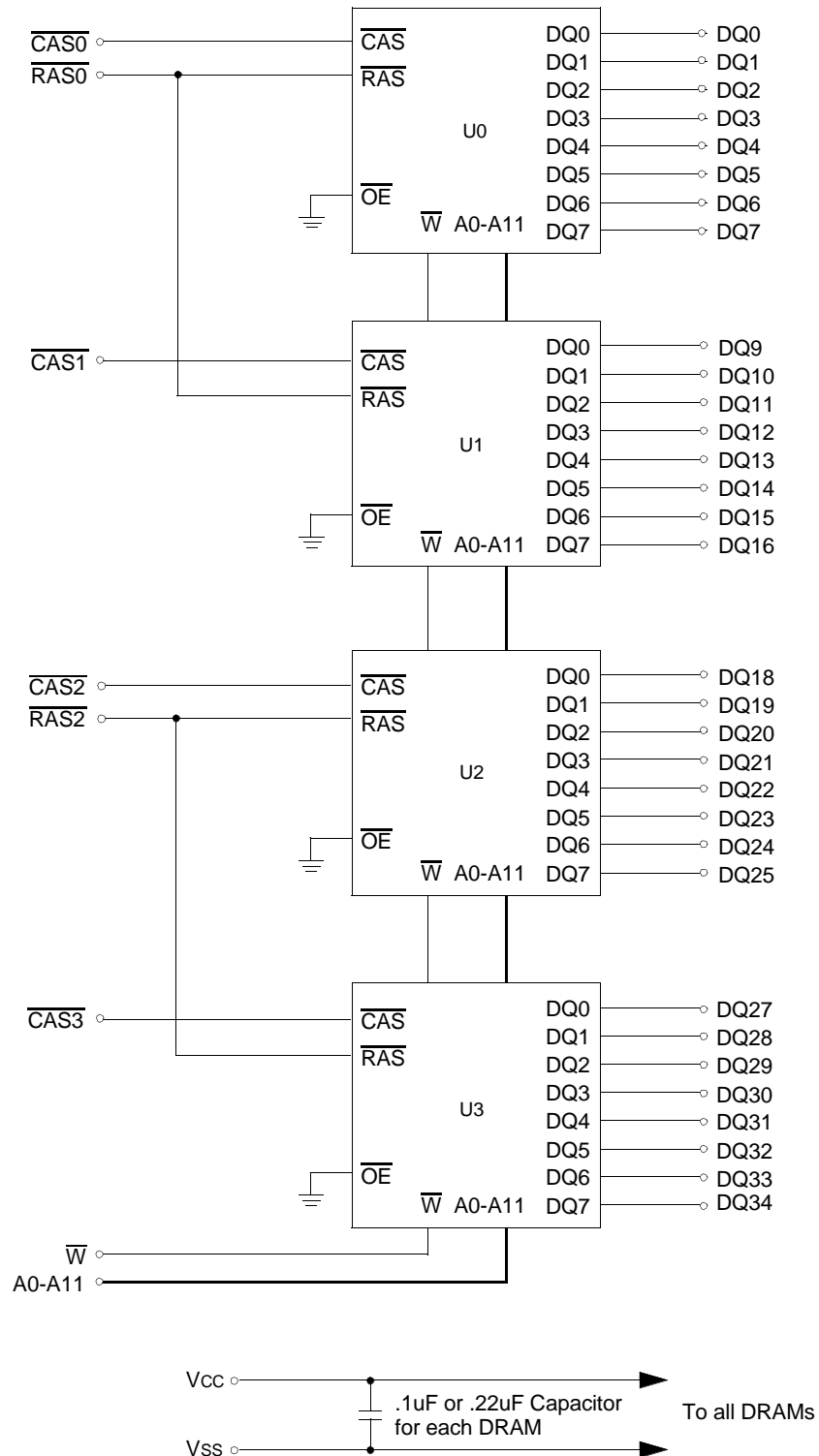
PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	Vss	Vss
PD3	NC	NC
PD4	NC	NC
PD5	Vss	NC
PD6	Vss	NC
PD7	Vss	Vss



ELECTRONICS

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V _{ss}	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on V _{cc} supply relative to V _{ss}	V _{CC}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	4	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{ss}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V at pulse width ≤15ns, which is measured at V_{CC}.

*2 : -1.3V at pulse width ≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM332F803BS		Unit
		Min	Max	
I _{CC1}	-L5	-	480	mA
	-L6	-	440	mA
I _{CC2}	Don't care	-	8	mA
I _{CC3}	-L5	-	480	mA
	-L6	-	440	mA
I _{CC4}	-L5	-	440	mA
	-L6	-	400	mA
I _{CC5}	Don't care	-	1.2	mA
I _{CC6}	-L5	-	480	mA
	-L6	-	440	mA
I _{CC7}	Don't care	-	1.6	mA
I _{CCS}	Don't care	-	1.6	mA
I _{I(L)}	Don't care	-10	10	uA
I _{O(L)}	Don't care	-5	5	uA
V _{OH}	Don't care	2.4	-	V
V _{OL}	Don't care	-	0.4	V

I_{CC1} : Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @ t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3} : \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @ t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6} : \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @ t_{RC}=min)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}=0.2V$)

DQ0-31=Don't care, t_{RC}=31.25us, t_{RAS}=t_{RASmin}~300ns

I_{CCS} : Self Refresh Current ($\overline{RAS}=\overline{CAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0-A11=V_{CC}-0.2V$ or 0.2V, DQ0-DQ34=V_{CC}-0.2V, 0.2V or OPEN

I_{I(L)} : Input Leakage Current (Any input 0 ≤ V_{IN} ≤ V_{CC}+0.3V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V ≤ V_{OUT} ≤ V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

DRAM MODULE

KMM332F803BS-L

CAPACITANCE (TA = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	CIN1	-	30	pF
Input capacitance[\overline{W}]	CIN2	-	38	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	CIN3	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	CIN4	-	17	pF
Input/Output capacitance[DQ0-7,9-16,18-25,27-34]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : VIH/VI=2.2/0.7V, VOH/VOL=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Access time from \overline{RAS}	tRAC		50		60	ns	3,4,9
Access time from \overline{CAS}	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,9
\overline{CAS} to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	tCEZ	3	13	3	13	ns	3,12
Transition time(rise and fall)	tT	1	50	1	50	ns	2
\overline{RAS} precharge time	tRP	30		40		ns	
\overline{RAS} pulse width	tRAS	50	10K	60	10K	ns	
\overline{RAS} hold time	tRSH	8		10		ns	
\overline{CAS} hold time	tCSH	38		40		ns	
\overline{CAS} pulse width	tCAS	8	10K	10	10K	ns	
\overline{RAS} to \overline{CAS} delay time	tRCD	17	37	20	45	ns	4
\overline{RAS} to column address delay time	tRAD	12	25	15	30	ns	9
\overline{CAS} to \overline{RAS} precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	7		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	7		10		ns	
Column address to \overline{RAS} lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to \overline{CAS}	tRCH	0		0		ns	7
Read command hold referenced to \overline{RAS}	tRRH	0		0		ns	7
Write command set-up time	tWCS	0		0		ns	6
Write command hold time	tWCH	7		10		ns	
Write command pulse width	tWP	7		10		ns	
Write command to \overline{RAS} lead time	tRWL	8		10		ns	
Write command to \overline{CAS} lead time	tCWL	7		10		ns	
Data set-up time	tDS	0		0		ns	8
Data hold time	tDH	7		10		ns	8
Refresh period	tREF		128		128	ms	
\overline{CAS} setup time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	5		5		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		ns	
\overline{RAS} to \overline{CAS} precharge time	tRPC	5		5		ns	
Access time from \overline{CAS} precharge	tCPA		28		35	ns	3

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

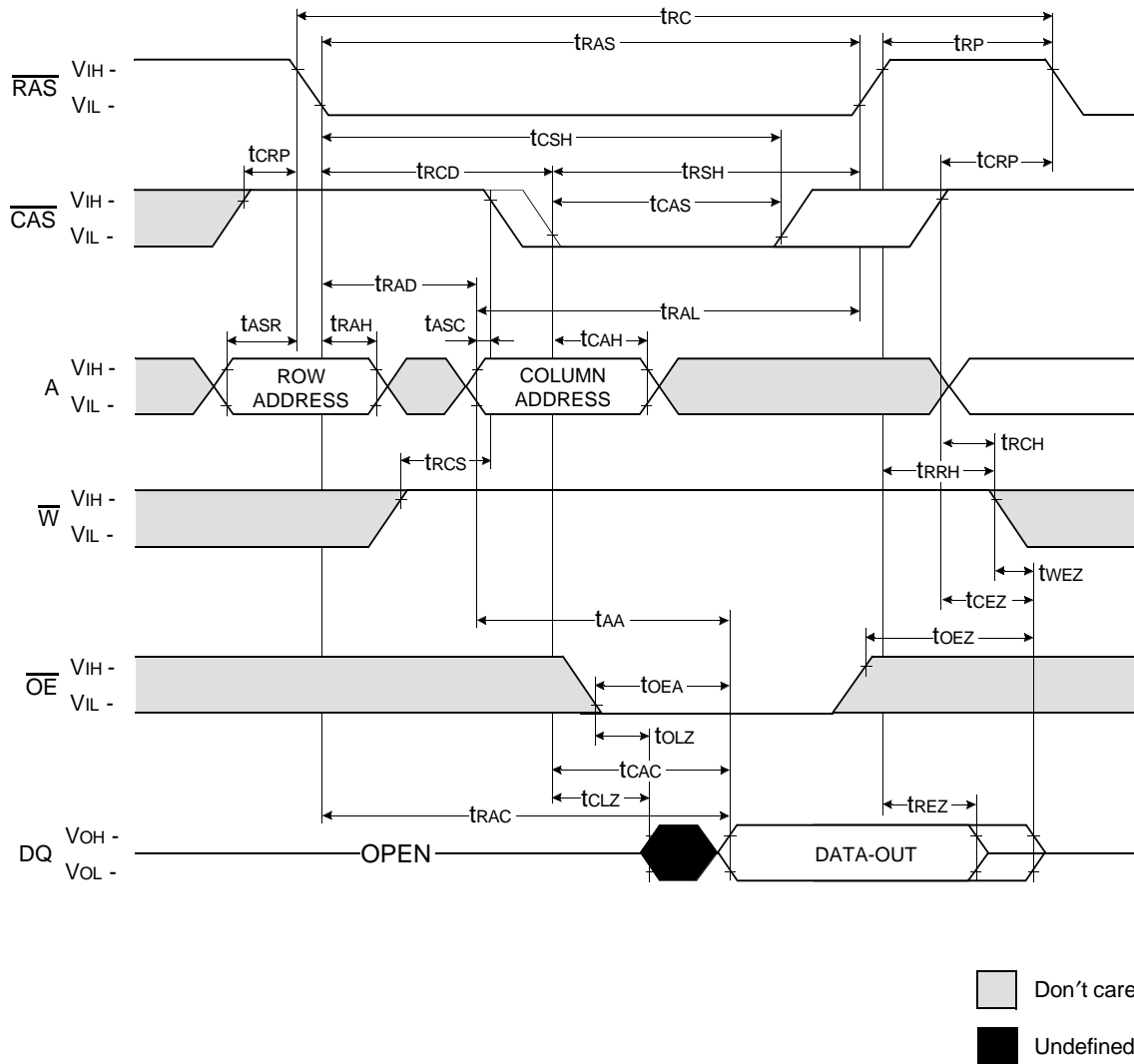
Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t _{HPC}	25		30		ns	10
$\overline{\text{CAS}}$ precharge time (Hyper page cycle)	t _{CP}	7		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	t _{RASP}	50	200K	60	200K	ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time(C-B-R refresh)	t _{WRP}	10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time(C-B-R refresh)	t _{WRH}	10		10		ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	30		35		ns	
Output data hold time	t _{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	t _{REZ}	3	13	3	15	ns	12
Output buffer turn off delay from $\overline{\text{W}}$	t _{WEZ}	3	13	3	15	ns	
$\overline{\text{W}}$ to data delay	t _{WED}	15		15		ns	
$\overline{\text{W}}$ pulse width	t _{WPE}	5		5		ns	
$\overline{\text{RAS}}$ pulse width (C-B-R self refresh)	t _{RASS}	100		100		us	11
$\overline{\text{RAS}}$ precharge time (C-B-R self refresh)	t _{RPS}	90		110		ns	11
$\overline{\text{CAS}}$ hold time (C-B-R self refresh)	t _{CHS}	-50		-50		ns	11

NOTES

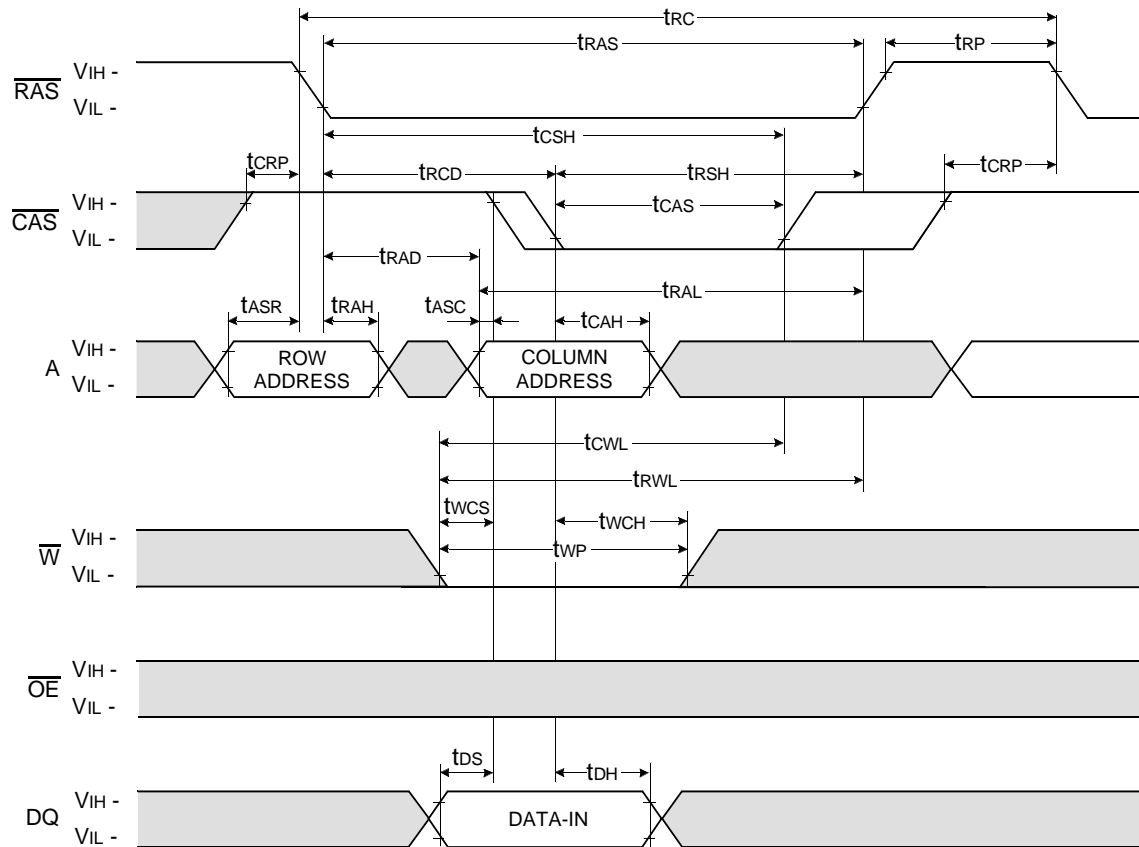
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il}. V_{ih}(min) and V_{il}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{ih}(min) and V_{il}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the t_{RCd}(max) limit insures that t_{RAC}(max) can be met. t_{RCd}(max) is specified as a reference point only. If t_{RCd} is greater than the specified t_{RCd}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that t_{RCd}≥t_{RCd}(max).
6. twcs is non-restrictive operating parameter. They is included in the data sheet as electrical characteristics only. If twcs≥twcs(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
7. Either t_{trch} or t_{trrh} must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{\text{CAS}}$ falling edge in early write cycles.
9. Operation within the t_{rad}(max) limit insures that t_{RAC}(max) can be met. t_{rad}(max) is specified as reference point only. If t_{rad} is greater than the specified t_{rad}(max) limit access time is controlled by t_{AA}.
10. t_{ASC}≥6ns, Assume t_T=2.0ns
11. For all of the refresh mode except distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, 4096 cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.
12. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.

READ CYCLE



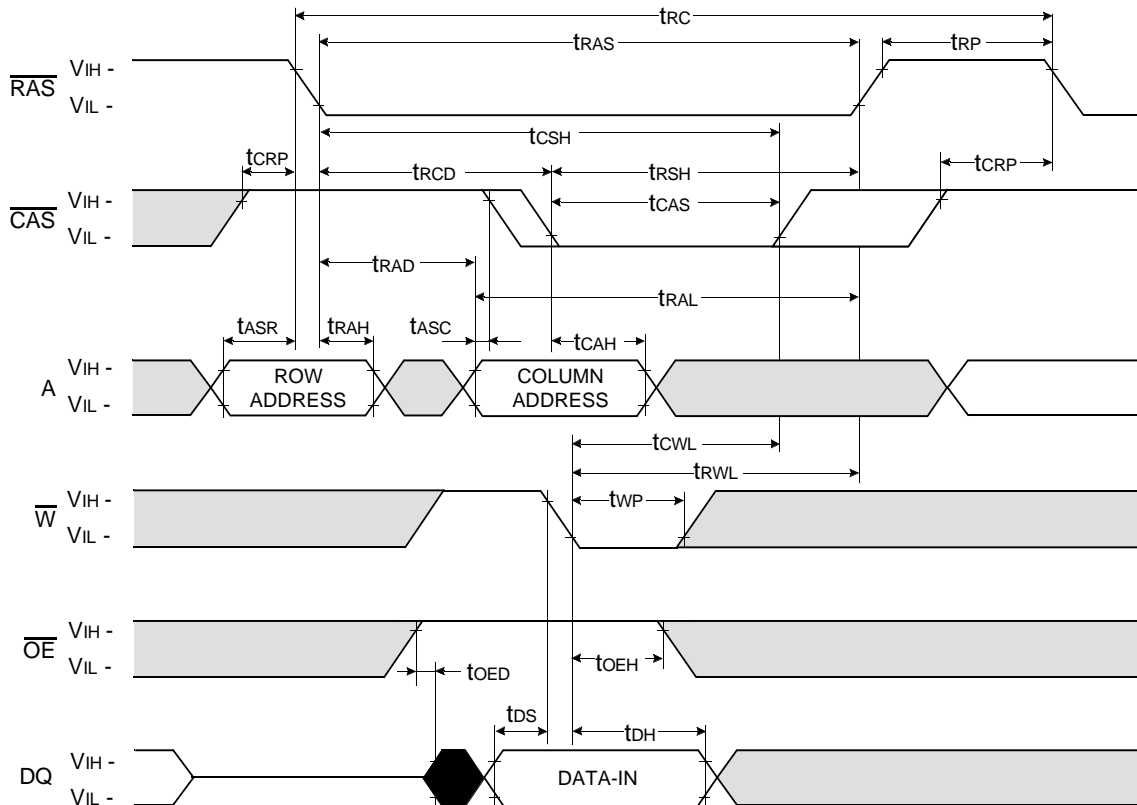
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

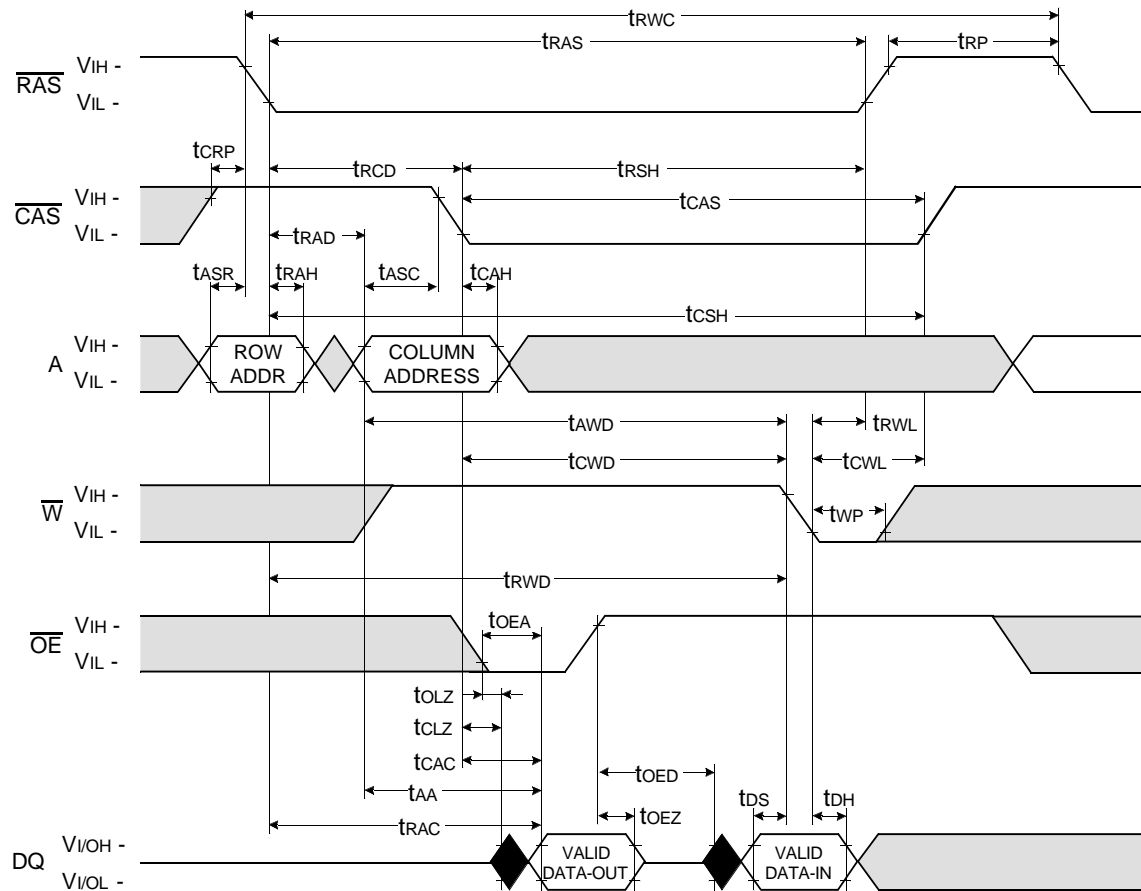
NOTE : DOUT = OPEN



Don't care

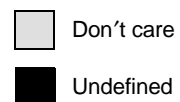
Undefined

READ - MODIFY - WRITE CYCLE

☐ Don't care

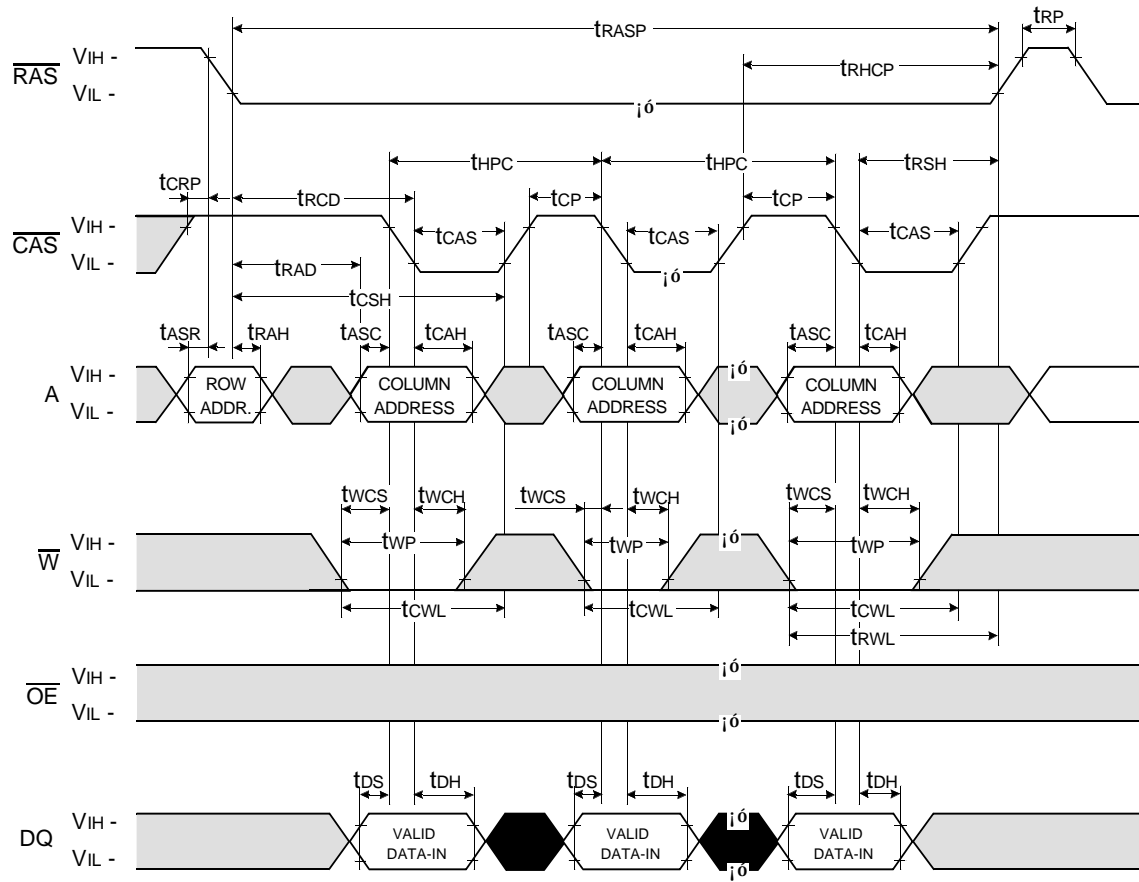
Undefined

HYPER PAGE READ CYCLE



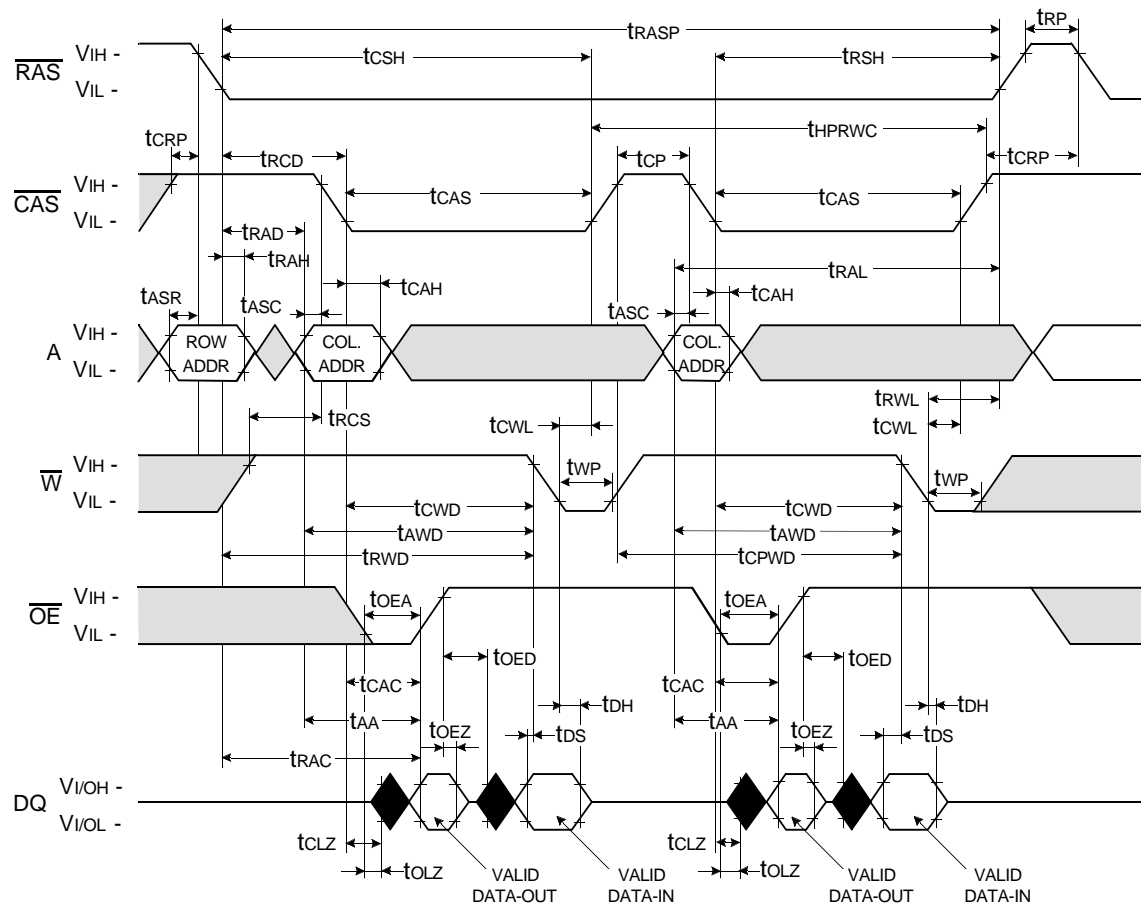
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



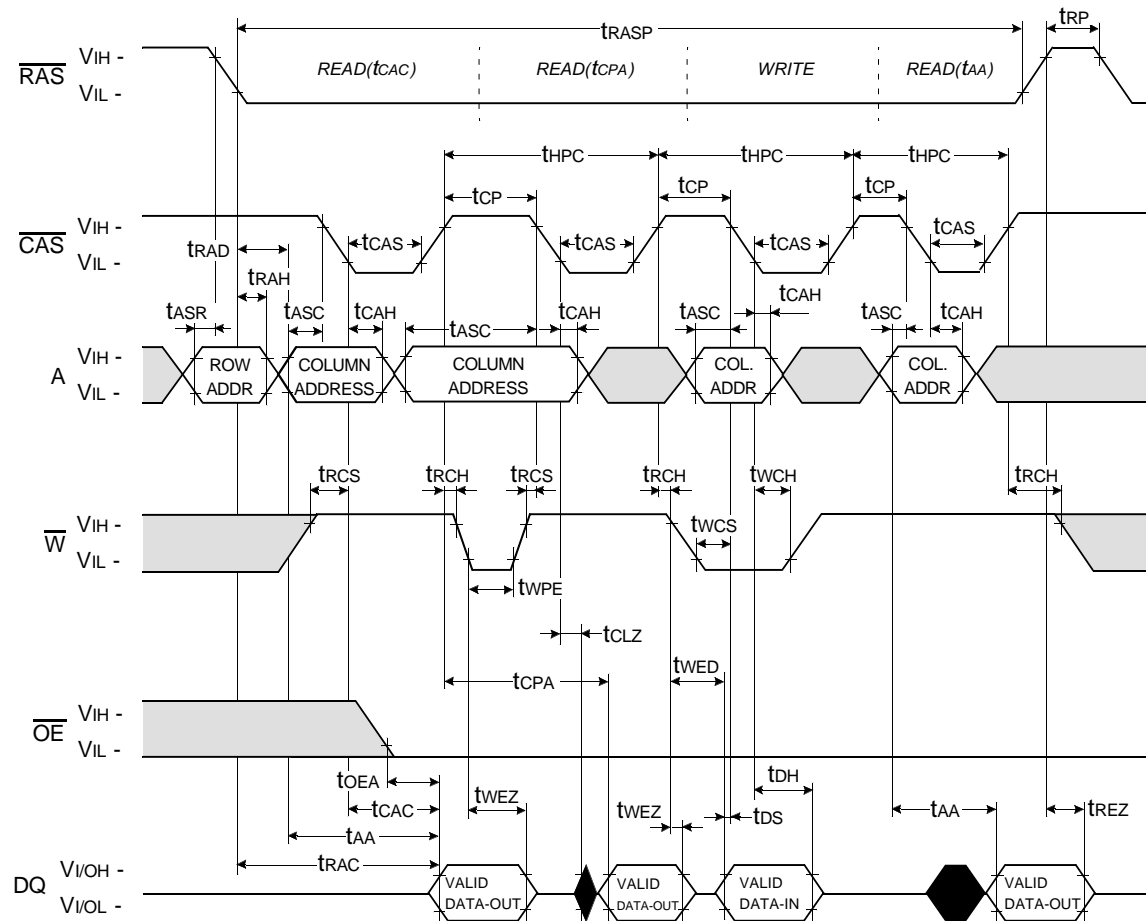
Don't care
Undefined

HYPER PAGE READ-MODIFY-WRITE CYCLE



■ Undefined

HYPER PAGE READ AND WRITE MIXED CYCLE

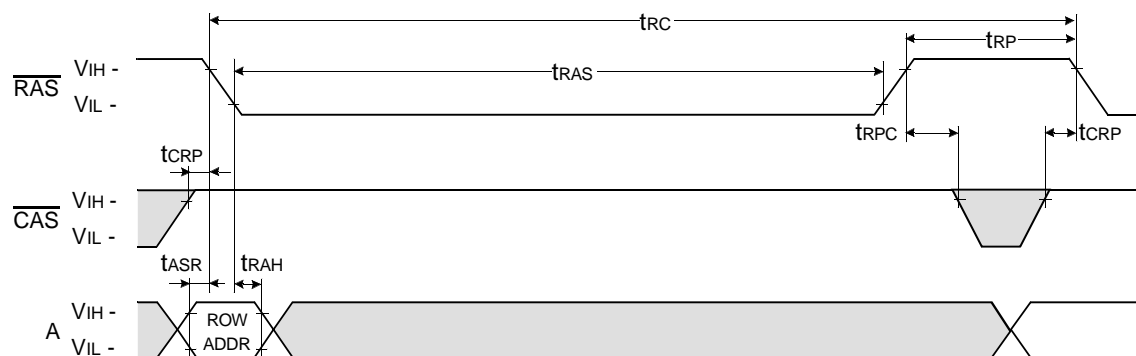


Don't care
Undefined

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

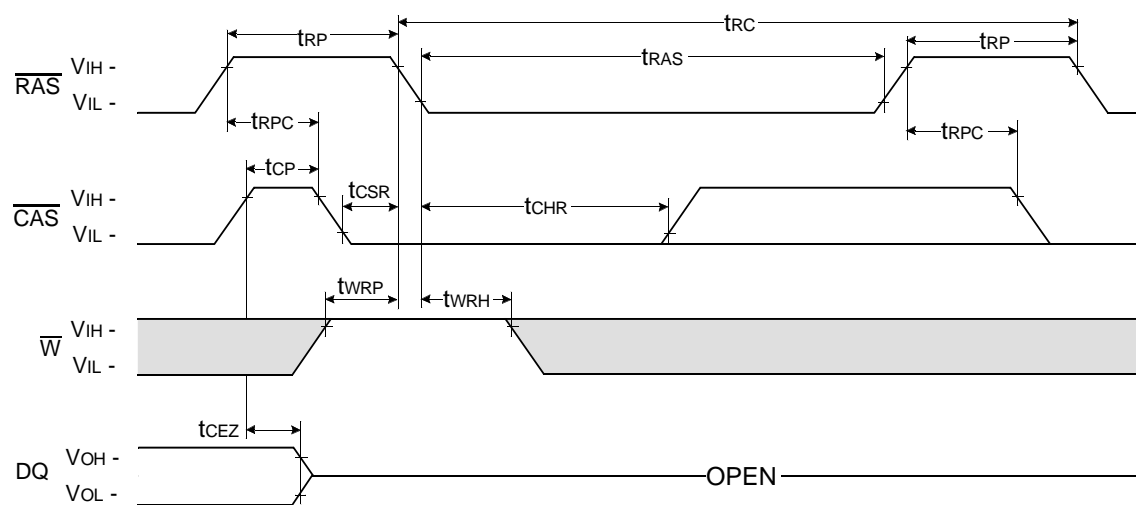
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care

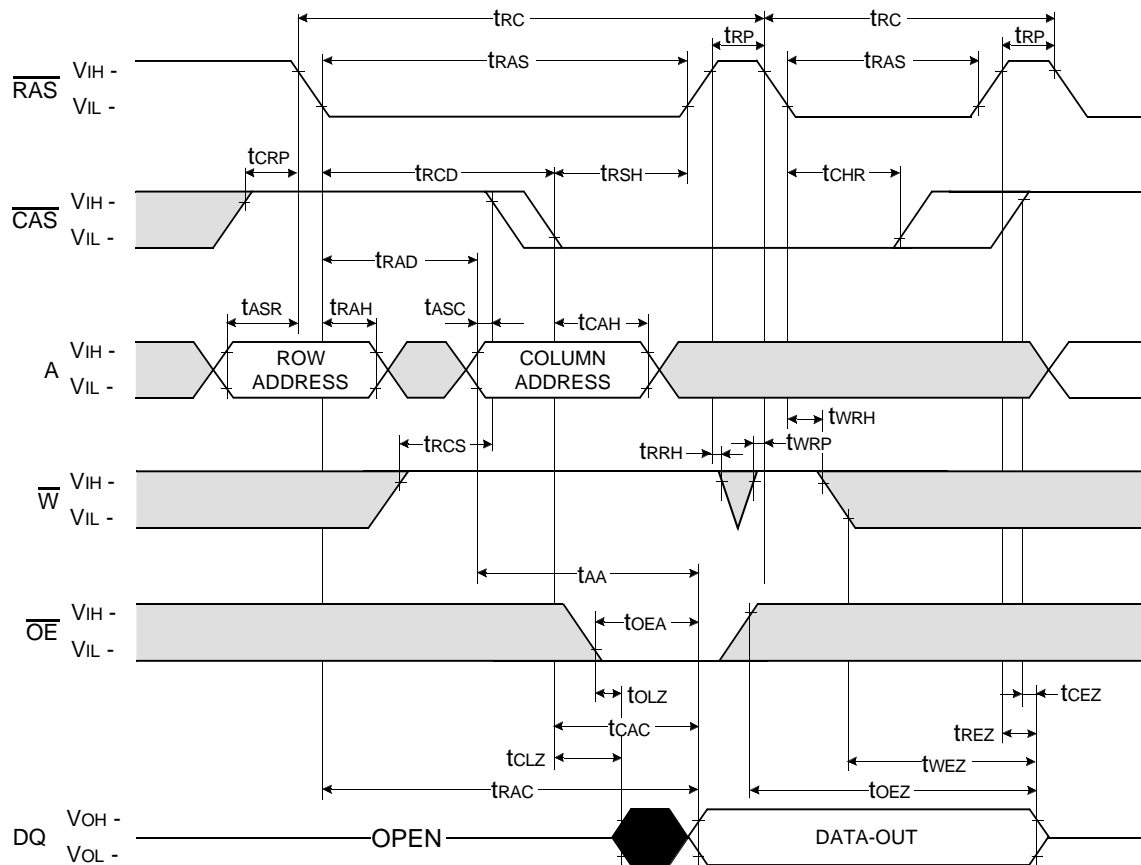


Don't care

Undefined

* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

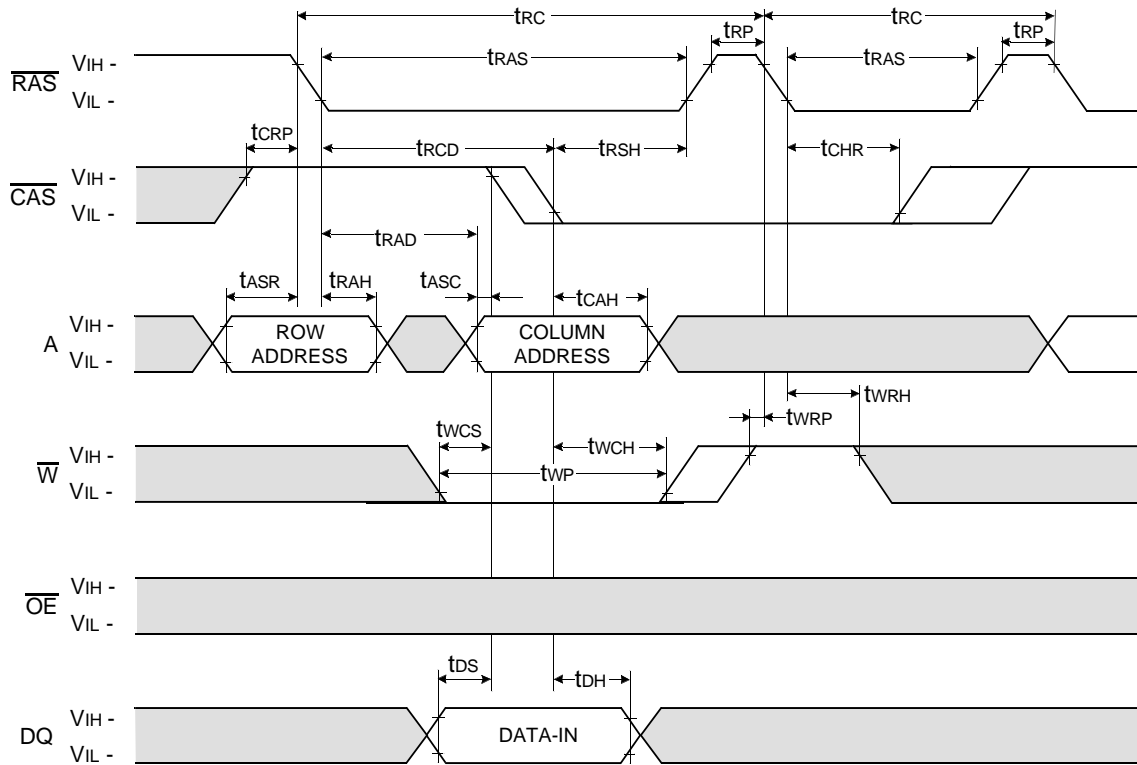
HIDDEN REFRESH CYCLE (READ)

☐ Don't care

Undefined

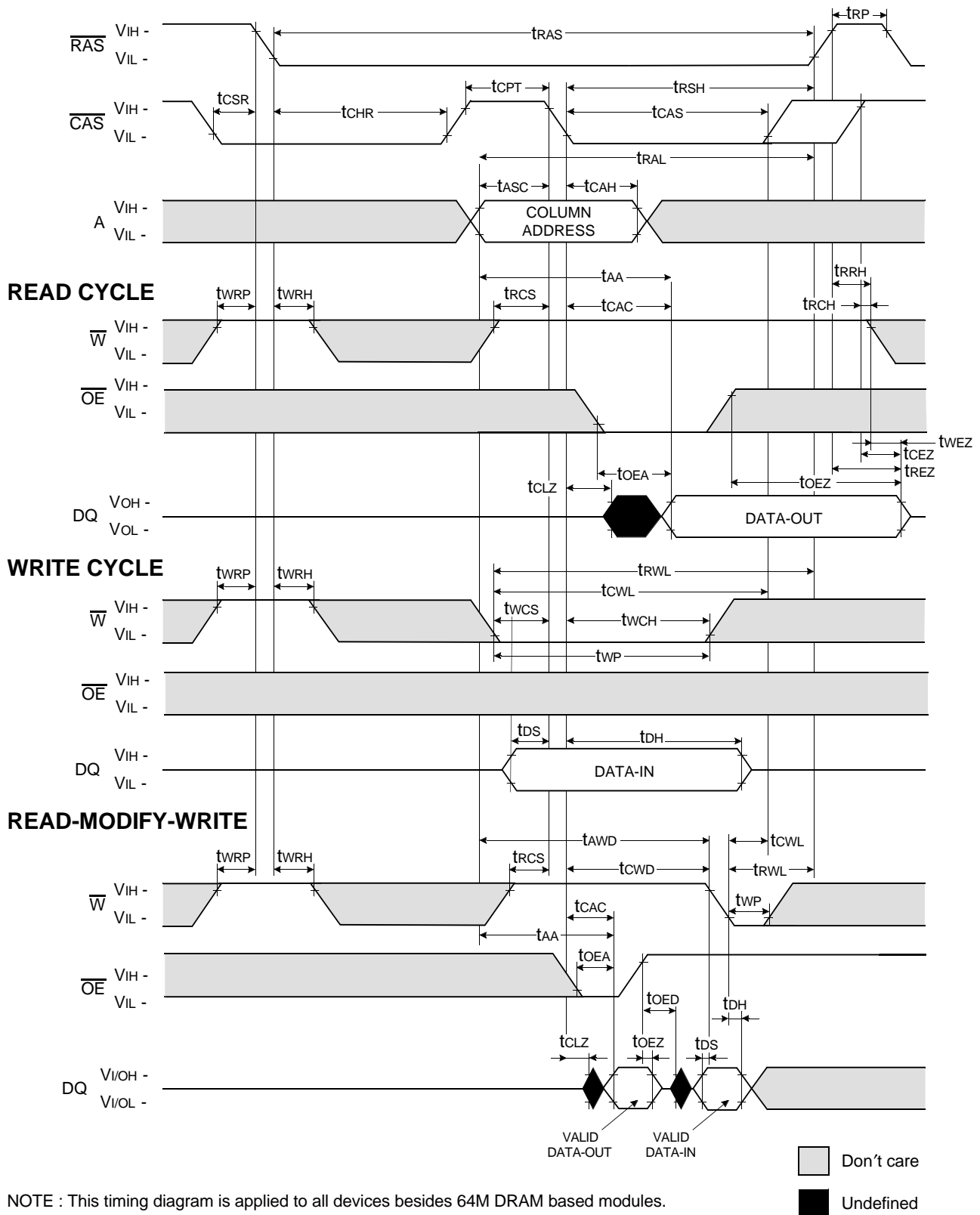
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



Don't care
Undefined

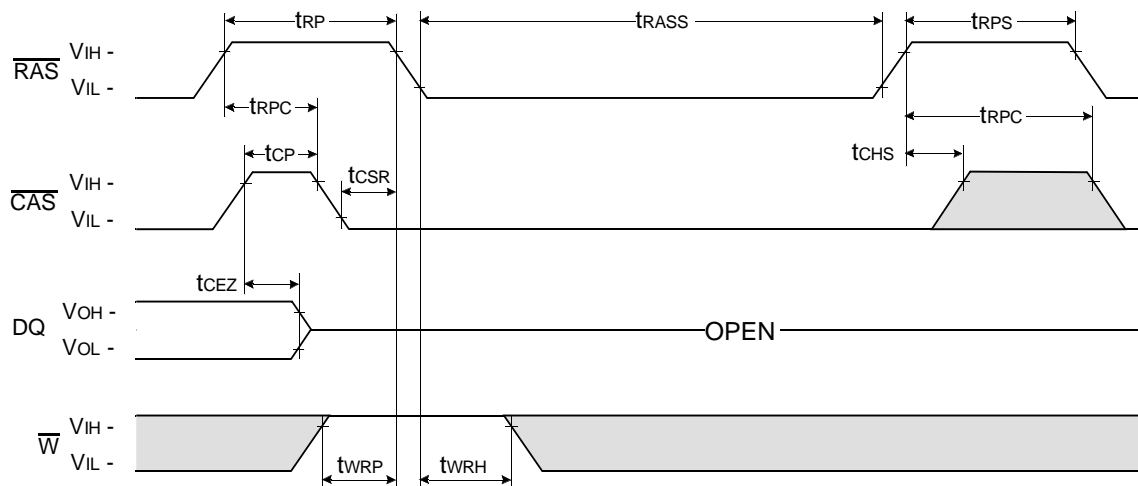
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

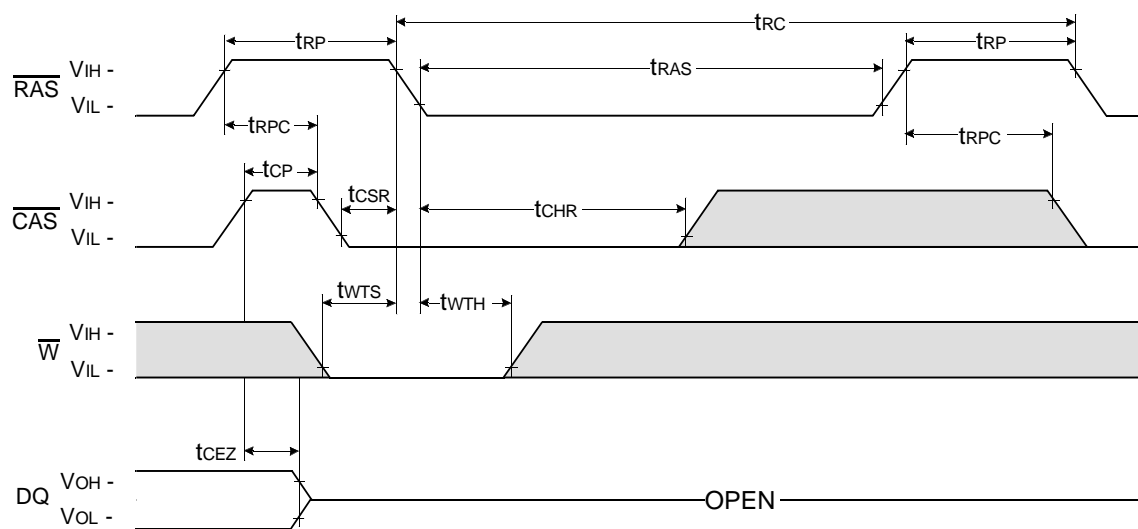
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care

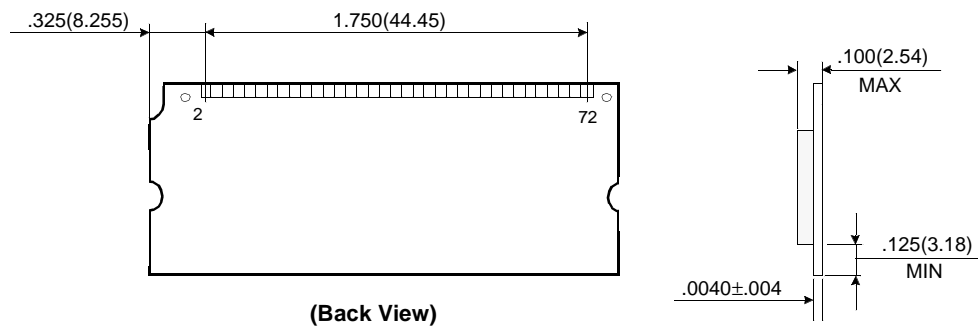
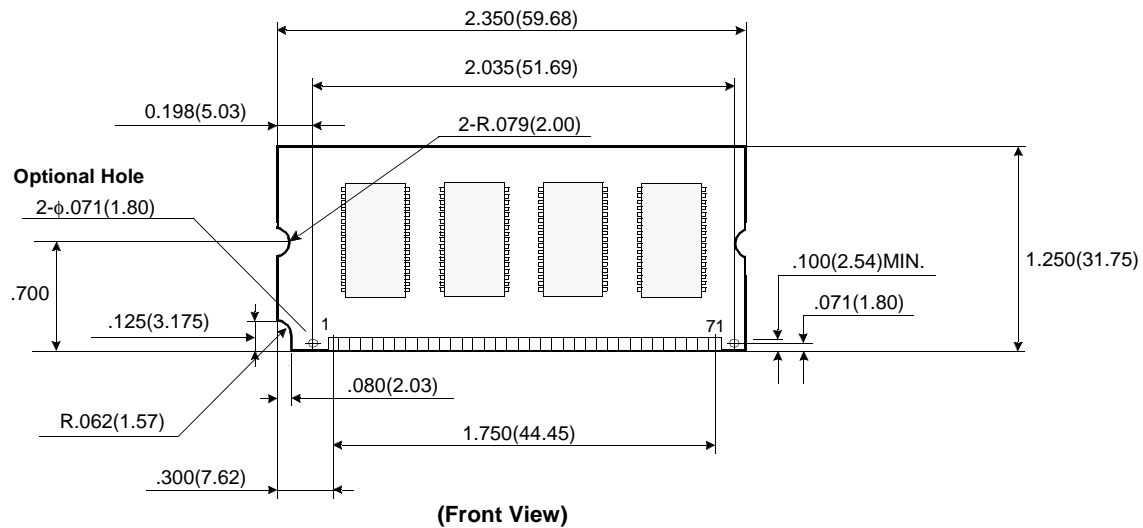
Undefined

DRAM MODULE

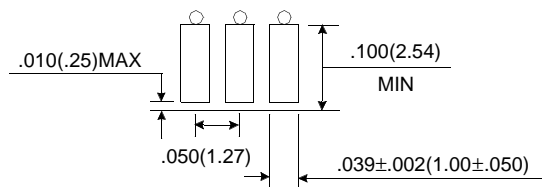
KMM332F803BS-L

PACKAGE DIMENSIONS

Units : Inches (millimeters)



Gold Plating Lead



Tolerances : \pm .005(.13) unless otherwise specified

NOTE: The used device is 8Mx8 DRAM, TSOP II
DRAM Part No : KM48V8104BS-L with Self Refresh