

8MB SGRAM MODULE

(1Mx64 SODIMM based on 512Kx32 SGRAM)

Unbuffered SGRAM
Graphics
64-bit Non-ECC/Parity
144-pin SODIMM

Revision 0.0

July 1999

Revision History

Revision 0.0 (July 1999)

First edition

SGRAM MODULE

KMM965G112AQ(P)N / KMM966G112AQ(P)N

KMM965G112AQ(P)N / KMM966G112AQ(P)N SGRAM SODIMM

1Mx64 SGRAM SODIMM based on 512Kx32, 2K Refresh, 3.3V Synchronous Graphic RAMs

GENERAL DESCRIPTION

The Samsung KMM965(6)G112AQ(P)N is a 1M bit x 64 Synchronous Graphic RAM high density memory module. The Samsung KMM965(6)G112AQ(P)N consists of four CMOS 512K x 32 bit Synchronous Graphic RAMs in 100pin QFP packages mounted on a 144pin glass-epoxy substrate. Five 0.1uF decoupling capacitors are mounted on the printed circuit board for each Synchronous GRAM. The KMM965(6)G112AQ(P)N is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Performance Range

Part NO.	Max. Freq. (tcc)
KMM965G112AQ(P)N-G5	200MHz (5ns) @CL=3
KMM965G112AQ(P)N-G6	166MHz (6ns) @CL=3
KMM965G112AQ(P)N-G7	143MHz (7ns) @CL=3
KMM965G112AQ(P)N-G8	125MHz (8ns) @CL=3

* KMM965G112AQN : based on PQFP Component

KMM965G112APN : based on TQFP Component

- Burst Mode Operation
- BLOCK-WRITE and Write-per-bit capability
- Independent byte operation via DQM0~7
- Auto & Self Refresh Capability (2048 cycles / 32ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- MRS cycle with address key programs
 - CAS Latency (2, 3)
 - Burst Length (1, 2, 4, 8 & Full page)
 - Data Scramble (Sequential & Interleave)
- Optional Serial PD with EEPROM (KMM966G112A)
- Resistor Strapping Options for speed and CAS Latency
- PCB : Height(1250mil), double sided components

PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	Voltage Key				95	DQ31	96	DQ30
3	DQ63	4	DQ62					97	DQ29	98	DQ28
5	DQ61	6	DQ60	51	RSVD	52	RSVD	99	DQ27	100	DQ26
7	DQ59	8	DQ58	53	RSVD	54	RSVD	101	DQ25	102	DQ24
9	DQ57	10	DQ56	55	Vss	56	Vss	103	Vss	104	Vss
11	VDD	12	VDD	57	DSF	58	RFU	105	DQ23	106	DQ22
13	DQ55	14	DQ54	59	RFU	60	RFU	107	DQ21	108	DQ20
15	DQ53	16	DQ52	61	RFU	62	**SBA	109	DQ19	110	DQ18
17	DQ51	18	DQ50	63	VDD	64	VDD	111	DQ17	112	DQ16
19	DQ49	20	DQ48	65	CS1	66	CS0	113	VDD	114	VDD
21	Vss	22	Vss	67	RAS	68	CAS	115	DQM3	116	DQM2
23	DQM7	24	DQM6	69	WE	70	CKE	117	DQM1	118	DQM0
25	DQM5	26	DQM4	71	Vss	72	Vss	119	Vss	120	Vss
27	VDD	28	VDD	73	CLK1	74	CLK0	121	DQ15	122	DQ14
29	DQ47	30	DQ46	75	VDD	76	VDD	123	DQ13	124	DQ12
31	DQ45	32	DQ44	77	RSVD	78	RSVD	125	DQ11	126	DQ10
33	DQ43	34	DQ42	79	RSVD	80	A8	127	DQ9	128	DQ8
35	DQ41	36	DQ40	(A11)		129	VDD	131	DQ7	132	DQ6
37	Vss	38	Vss	81	BA(A10)	82	A9/AP	133	DQ5	134	DQ4
39	DQ39	40	DQ38	83	A7	84	A6	135	DQ3	136	DQ2
41	DQ37	42	DQ36	85	Vss	86	Vss	137	DQ1	138	DQ0
43	DQ35	44	DQ34	87	A5	88	A4	139	Vss	140	Vss
45	DQ33	46	DQ32	89	A3	90	A2	141	**SDA	142	**SCL
47	VDD	48	VDD	91	A1	92	A0	143	VDD	144	VDD
49	RSVD	50	RSVD	93	VDD	94	VDD				

PIN NAMES

Pin Name	Function
A0 ~ A9	Address Input(multiplexed)
BA(A10)	Bank Select Address
DQ0 ~ 63	Data Input / Output
CLK0,CLK1	Clock Input
CKE	Clock Enable Input
CS0,CS1	Chip Select Input
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
DSF	Define Special Function
DQM0 ~ 7	DQM
VDD	Power Supply (3.3V)
Vss	Ground
**SDA	Serial Address Data I/O
**SBA	EEPROM Device Address
**SCL	Serial Clock
RSVD	Reserved
RFU	Reserved for future used
NC	No Connection

** These pins should be NC in the system which does not support SPD.

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PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System Clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + tss prior to new command. Disables input buffers for power down in standby.
A0 ~ A9	Address	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA9, column address : CA0 ~ CA7
BA(A10)	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM0 ~ 7	Data Input/Output Mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0~63	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
DSF	Define Special Function	Enables write per bit, block write and special mode register set.
VDD/VSS	Power Supply/Ground	Power and ground for the input buffers and the core logic.

RESISTOR STRAPPING OPTIONS

Three resistor straps are used to indicate the synchronous clock frequency (period) and memory timing. Timing information for each clock frequency is indicated in the section titled *AC CHARACTERISTICS*.

Clock Frequency and Memory Timing

Cycle Time	DQ30	DQ29
8ns	1	0
7ns	1	1
6ns	0	0
5ns	0	1

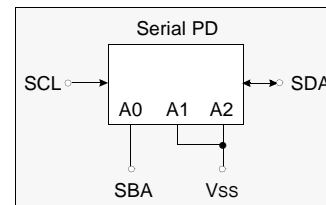
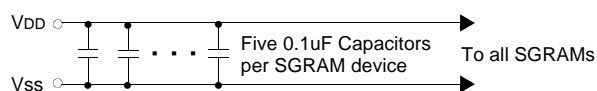
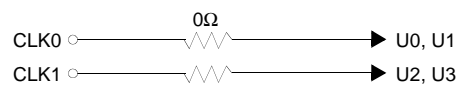
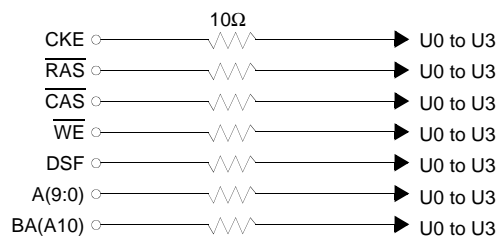
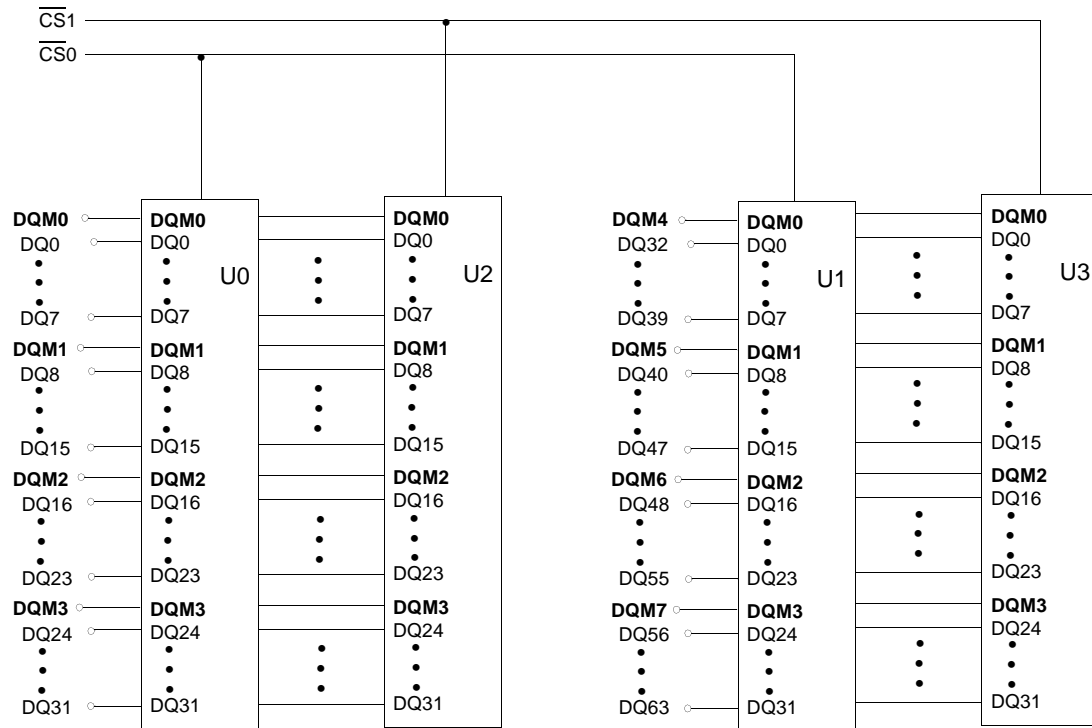
CAS Latency

CAS Latency	DQ31
3	0
2 and 3	1

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FUNCTIONAL BLOCK DIAGRAM



* Serial PD is optional

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ABSOLUTE MAXIMUM RATINGS (Voltages referenced to Vss)

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	2	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V _{DD}	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	
Input low voltage	V _{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-40	-	40	µA	Note 2
Output leakage current	I _{LO}	-20	-	20	µA	Note 3
Output Loading current	See figure 1					

Note : 1. V_{IL}(min) = -1.5V AC (pulse width ≤ 5 ns)

2. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.

3. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DD}

CAPACITANCE (V_{CC} = 3.3V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Max.	Unit
Input capacitance (A0 ~ A9, BA0)	C _{IN1}	-	26	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CKE}}$, $\overline{\text{DSF}}$)	C _{IN2}	-	26	pF
Input capacitance (CLK0, CLK1)	C _{IN3}	-	18	pF
Input capacitance ($\overline{\text{CS0}}$, $\overline{\text{CS1}}$)	C _{IN4}	-	18	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN5}	-	18	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	-	20	pF

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DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C , $V_{IH(\min)}/V_{IL(\max)}=2.0\text{V}/0.8\text{V}$)

Parameter	Symbol	Test Condition	CAS Latency	Speed				Unit	Note
				-5	-6	-7	-8		
Operating Current (One Bank Active)	I _{CC1}	Burst Length =1 trc ≥ trc(min), tcc ≥ tcc(min), lo = 0mA	3	460	420	380	360	mA	2
			2	-	-	-	360		
Precharge Standby Current in power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), tcc = 15ns		8				mA	
	I _{CC2PS}	CKE & CLK ≤ V _{IL} (max), tcc = ∞		8					
Precharge Standby Current in non power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), $\overline{\text{CS}} \geq V_{IH}(\text{min})$, tcc = 15ns Input signals are changed one time during 30ns		120				mA	
	I _{CC2NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable		60					
Active Standby Current in power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), tcc = 15ns		12				mA	
	I _{CC3PS}	CKE ≤ V _{IL} (max), tcc = ∞		12					
Active Standby Current in non power-down mode (One Bank Active)	I _{CC3N}	CKE ≥ V _{IH} (min), $\overline{\text{CS}} \geq V_{IH}(\text{min})$, tcc = 15ns Input signals are changed one time during 30ns		200				mA	
	I _{CC3NS}	CKE ≥ V _{IH} (min), CLK ≤ V _{IL} (max), tcc = ∞ Input signals are stable		120					
Operating Current (Burst Mode)	I _{CC4}	lo = 0 mA, Page Burst All bank Activated, tccd = tccd(min)	3	600	580	520	460	mA	2
			2	-	-	-	380		
Refresh Current	I _{CC5}	trc ≥ trc(min)	3	800	720	640	600	mA	3
			2	-	-	-	600		
Self Refresh Current	I _{CC6}	CKE ≤ 0.2V		8				mA	
Operating Current (One Bank Block Write)	I _{CC7}	tcc ≥ tcc(min), lo=0mA, tbwc(min)		520	460	400	360	mA	

Note : 1. Unless otherwise notes, Input level is CMOS($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$) in LVTTL.

2. Measured with outputs open. Address are changed only one time during $t_{CC(\min)}$.

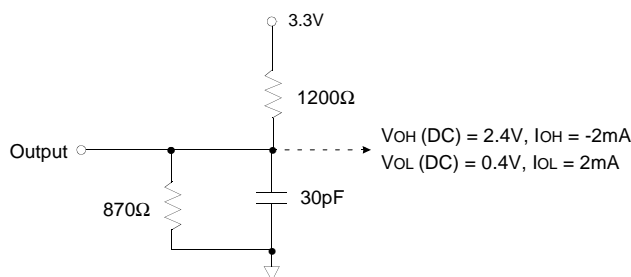
3. Refresh period is 32ms. Address are changed only one time during $t_{CC(\min)}$.

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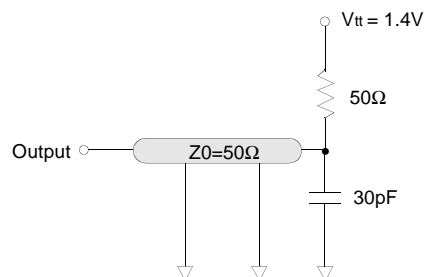
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AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value
AC input levels	$V_{ih}/V_{il} = 2.4V / 0.4V$
Input timing measurement reference level	1.4V
Input rise and fall time(See note 3)	$t_r/t_f = 1ns / 1ns$
Output timing measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-6		-7		-8		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency=3	t _{CC}	5	1000	6	1000	7	1000	8	1000	ns	1
	CAS Latency=2		-	-	-	-	-	-	10	-		
CLK to valid output delay	CAS Latency=3	t _{SAC}	-	4.5	-	5.5	-	5.5	-	6	ns	1, 2
	CAS Latency=2		-	-	-	-	-	-	-	6		
Output data hold time		t _{OH}	2	-	2.5	-	2.5	-	2.5	-	ns	2
CLK high pulse width	CAS Latency=3	t _{CH}	2	-	2.5	-	3	-	3	-	ns	3
	CAS Latency=2		-	-	-	-	-	-	-	-		
CLK low pulse width	CAS Latency=3	t _{CL}	2	-	2.5	-	3	-	3	-	ns	3
	CAS Latency=2		-	-	-	-	-	-	-	-		
Input setup time	CAS Latency=3	t _{SS}	1.5	-	1.5	-	1.75	-	2	-	ns	3
	CAS Latency=2		-	-	-	-	-	-	2.5	-		
Input hold time		t _{SH}	1	-	1	-	1	-	1	-	ns	3
CLK to output in Low-Z		t _{SLZ}	1	-	1	-	1	-	1	-	ns	2
CLK to output in Hi-Z	CAS latency=3	t _{SHZ}	-	4.5	-	5.5	-	5.5	-	6	ns	-
	CAS latency=2		-	-	-	-	-	-	-	6		

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, $(t_r/2-0.5)ns$ should be added to the parameter.

3. Assumed input rise and fall time (t_r & t_f)=1ns.

If t_r & t_f is longer than 1ns, transient time compensation should be considered,
i.e., $[(t_r + t_f)/2-1]ns$ should be added to the parameter.

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OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version								Unit	Note
			-5		-6		-7		-8			
CAS Latency		CL	3	2	3	2	3	2	3	2	CLK	
CLK cycle time		tCC(min)	5	-	6	-	7	-	8	10	ns	
Row active to row active delay		tRRD(min)	2								CLK	1
RAS to CAS delay		tRCD(min)	4	-	3	-	3	-	3	2	CLK	1
Row precharge time		tRP(min)	4	-	3	-	3	-	3	2	CLK	1
Row active time		tRAS(min)	8	-	7	-	7	-	6	5	CLK	1
		tRAS(max)	100								us	
Row cycle time		tRC(min)	12	-	10	-	10	-	9	7	CLK	1
Last data in to row precharge		tRDL(min)	2								CLK	2, 5
Last data in to new col.address delay		tCDL(min)	1								CLK	2
Last data in to burst stop		tBDL(min)	1								CLK	2
Col. address to col. address delay		tCCD(min)	1								CLK	
Block Write data-in to PRE command		tBPL(min)	2								CLK	
Block write cycle time		tBWC(min)	1								CLK	3
Mode Register Set cycle time		tMRS(min)	1								CLK	
Number of valid output data	CAS Latency=3		2								ea	4
	CAS Latency=2		1									

Parameter	Symbol	Version				Unit
		-5	-6	-7	-8	
CLK cycle time	tCC(min)	5	6	7	8	ns
Row active to row active delay	tRRD(min)	10	12	14	16	ns
RAS to CAS delay	tRCD(min)	20	18	21	20	ns
Row precharge time	tRP(min)	20	18	21	20	ns
Row active time	tRAS(min)	40	42	49	48	ns
	tRAS(max)	100				us
Row cycle time	tRC(min)	60	60	70	70	ns

- Note :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer. Refer to the following ns-unit based AC table.
 2. Minimum delay is required to complete write.
 3. This parameter means minimum CAS to CAS delay at block write cycle only.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. For -6/7/8, tRDL =1CLK product can be supported within restricted amounts and it will be distinguished by bucket code "NV". From the next generation, tRDL will be only 2CLK for every clock frequency.

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SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	CS	RAS	CAS	WE	DSF	DQM	A10	A9	A8~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	L	X	OP CODE			1, 2
	Special Mode Register Set								H					1,2,7
Refresh	Auto Refresh		H	H	L	L	L	H	L	X	X			3
	Self Refresh	Entry		L										3
		Exit	L	H	L	H	H	H	X	X	X			3
					H	X	X	X						3
Bank Active & Row Addr.	Write Per Bit Disable		H	X	L	L	H	H	L	X	V	Row Address		4, 5
	Write Per Bit Enable								H					4,5,9
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	L	X	V	L	Column Address	4
	Auto Precharge Enable											H		4, 6
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	L	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Block Write & Column Addr.	Auto Precharge Disable		H	X	L	H	L	L	H	X	V	L	Column Address	4, 5
	Auto Precharge Enable											H		4,5,6,9
Burst Stop			H	X	L	H	H	L	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	L	X	V	L	X	
	Both Banks										X	H		
Clock Suspend or Active Power Down		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
Exit		L	H	X	X	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	L	H	H	H	X	X	X			
					H	X	X	X						
		Exit	L	H	L	V	V	V	X					
					H	X	X	X						
DQM			H	X						V	X			8
No Operation Command			H	X	L	H	H	H	X	X	X			
					H	X	X	X						

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code

A0 ~ A10 : Program keys. (@MRS)

A5, A6 : LMR or LCR select. (@SMRS)

Color register exists only one per DQi which both banks share.

So dose Mask Register.

Color or mask is loaded into chip through DQ pin.

2. MRS can be issued only at both banks precharge state.

SMRS can be issued only if DQ's are idle.

A new command can be issued at the next clock of MRS/SMRS.

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SIMPLIFIED TRUTH TABLE

3. Auto refresh functions as same as CBR refresh of DRAM.
The automatical precharge without Row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at both precharge state.
4. A₁₀ : Bank select address.
If "Low" at read, (block) write, Row active and precharge, bank A is selected.
If "High" at read, (block) write, Row active and precharge, bank B is selected.
If A₉ is "High" at Row precharge, A₁₀ is ignored and both banks are selected.
5. It is determined at Row active cycle.
whether Normal/Block write operates in write per bit mode or not.
For A bank write, at A bank Row active, for B bank write, at B bank Row active.
Terminology : Write per bit =I/O mask
(Block) Write with write per bit mode=Masked(Block) Write
6. During burst read or write with auto precharge, new read/(block) write command cannot be issued.
Another bank read/(block) write command can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid only at full page burst length.
8. DQM sampled at positive going edge of a CLK.
masks the data-in at the very CLK(Write DQM latency is 0)
but makes Hi-Z state the data-out of 2 CLK cycles after.(Read DQM latency is 2)
9. Graphic features added to SDRAM's original features.
If DSF is tied to low, graphic functions are disabled and chip operates as a 16M SDRAM with 32 DQ's.

SGRAM vs SDRAM

Function	MRS		Bank Active		Write	
	L	H	L	H	L	H
SGRAM Function	MRS	SMRS	Bank Active with Write per bit Disable	Bank Active with Write per bit Enable	Normal Write	Block Write

If DSF is low, SGRAM functionality is identical to SDRAM functionality.

SGRAM can be used as an unified memory by the appropriate DSF control
--> SGRAM=Graphic Memory + Main Memory

SGRAM MODULE

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MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vendor Use Only	0	0	1	-	1	Interleave	0	0	1	2	Reserved
1	0		0	1	0	2	0		1	0	4	4	
1	1		0	1	1	3	0		1	1	8	8	
Write Burst Length			1	0	0	Reserved	1		0	0	Reserved	Reserved	
A9	Length		1	0	1	Reserved	1		0	1	Reserved	Reserved	
0	Burst		1	1	0	Reserved	1		1	0	Reserved	Reserved	
			1	1	1	Reserved	1		1	1	256(Full)	Reserved	

(Note 1)

Special Mode Register Programmed with SMRS

Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	X				LC	LM	X				

Load Color		Load Mask	
A6	Function	A5	Function
0	Disable	0	Disable
1	Enable	1	Enable

(Note 2)

POWER UP SEQUENCE

SGRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and start clock. Must maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
 2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
 3. Issue precharge commands for all banks of the devices.
 4. Issue 2 or more auto-refresh commands.
 5. Issue a mode register set command to initialize the mode register.
- cf.) Sequence of 4 & 5 may be changed.

The device is now ready for normal operation.

Note : 1. The full column burst(256bit) is available only at Sequential mode of burst type.
2. If LC and LM both high(1), data of mask and color register will be unknown.

SGRAM MODULE

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BURST SEQUENCE (BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

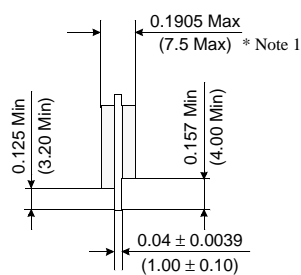
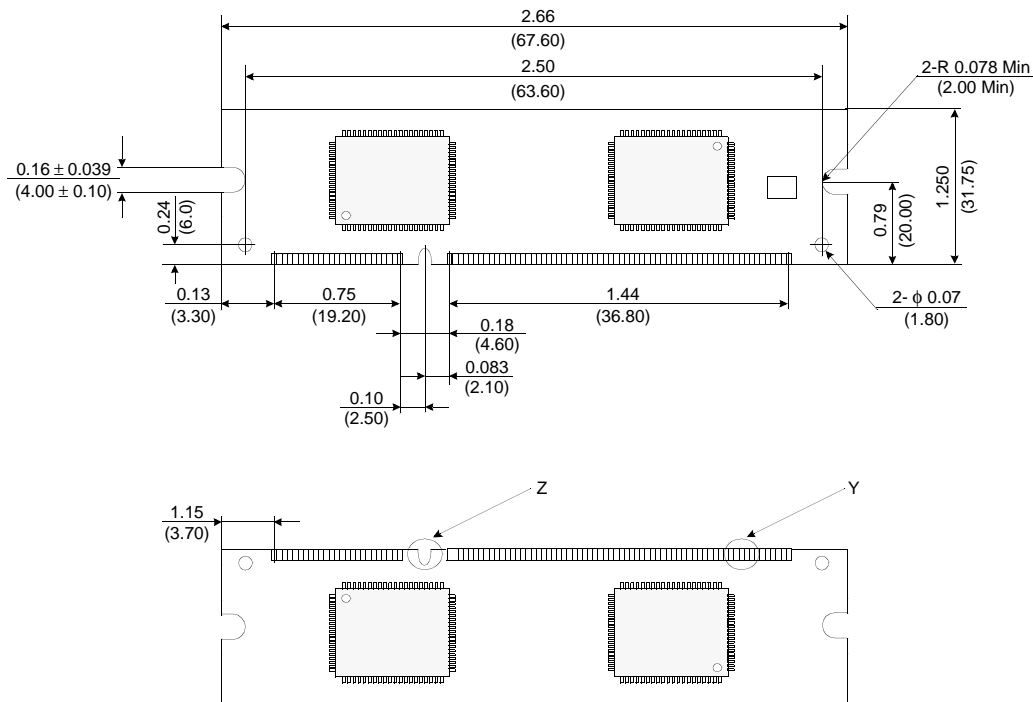
PIXEL to DQ MAPPING(at BLOCK WRITE)

Column address			7 Byte	6 Byte	5 Byte	4 Byte	3 Byte	2 Byte	1 Byte	0 Byte
A2	A1	A0	I/O63 - I/O56	I/O55 - I/O48	I/O47 - I/O40	I/O39 - I/O32	I/O31 - I/O24	I/O23 - I/O16	I/O15 - I/O8	I/O7 - I/O0
0	0	0	DQ56	DQ48	DQ40	DQ32	DQ24	DQ16	DQ8	DQ0
0	0	1	DQ57	DQ49	DQ41	DQ33	DQ25	DQ17	DQ9	DQ1
0	1	0	DQ58	DQ50	DQ42	DQ34	DQ26	DQ18	DQ10	DQ2
0	1	1	DQ59	DQ51	DQ43	DQ35	DQ27	DQ19	DQ11	DQ3
1	0	0	DQ60	DQ52	DQ44	DQ36	DQ28	DQ20	DQ12	DQ4
1	0	1	DQ61	DQ53	DQ45	DQ37	DQ29	DQ21	DQ13	DQ5
1	1	0	DQ62	DQ54	DQ46	DQ38	DQ30	DQ22	DQ14	DQ6
1	1	1	DQ63	DQ55	DQ47	DQ39	DQ31	DQ23	DQ15	DQ7

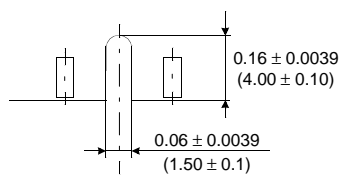
KMM965G112AQ(P)N / KMM966G112AQ(P)N

PACKAGE DIMENSIONS - *Proposal (Based on JEDEC STD.)*

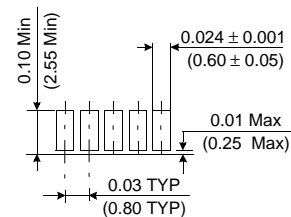
Units : Inches (millimeters)



Detail Z



Detail Y



Tolerances :±.0059(.15) unless otherwise specified

* Note 1 : This thickness is when using PQFP package. When using TQFP package, this value is 3.9mmMax.

The used device is 512Kx32, 16M SGRAM, 100pin (T)QFP

SGRAM Component Part No. : KM4132G512Q : PQFP (Height = 3.0mmMax)

KM4132G512TQ : TQFP (Height = 1.2mmMax)

SGRAM MODULE

KMM965G112AQ(P)N / KMM966G112AQ(P)N

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I²C
- Current sink capability of SDA driver ≤ 3mA
- Maximum clock frequency : 80KHz

Contents ;

Byte #	Function Described	Function Supported				Hex value				Note
		-5	-6	-7	-8	-5	-6	-7	-8	
0	# of bytes written into serial memory at module manufacturer	128bytes				80h				
1	Total # of bytes of SPD memory device	256bytes (2K bit)				08h				
2	Fundamental memory type	SGRAM				06h				TBD
3	# of row address on this assembly	10				0Ah				1
4	# of column address on this assembly	8				08h				1
5	# of module banks on this assembly	2 bank				02h				
6	Data width of this assembly	64 bits				40h				
7 Data width of this assembly	-				00h				
8	Voltage interface standard of this assembly	LVTTTL				01h				
9	SGRAM cycle time from clock @CAS latency of 3	5n	6ns	7ns	8ns	50h	60h	70h	80h	2
10	SGRAM access time from clock @CAS latency of 3	4.5n	5.5ns	6ns	6.5ns	45h	55h	60h	65h	2
11	DIMM configuraion type	Non parity				00h				
12	Refresh rate & type	15.625us, support self refresh				80h				
13	Primary SGRAM width	x32				20h				
14	Error checking SGRAM width	None				00h				
15	Minimum clock delay for back-to-back random column	tCCD = 1CLK				01h				
16	SGRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page				8Fh				
17	SGRAM device attributes : # of banks on SGRAM device	2 banks				02h				
18	SGRAM device attributes : CAS latency	2 & 3				06h				
19	SGRAM device attributes : CS latency	0 CLK				01h				
20	SGRAM device attributes : Write latency	0 CLK				01h				
21	SGRAM module attributes	Non-buffered, non-registered & redundant addressing				00h				
22	SGRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge				4Eh				
23	SGRAM cycle time @CAS latency of 2	-	-	-	10ns	00h	00h	00h	A0h	2
24	SGRAM access time @CAS latency of 2	-	-	-	6ns	00h	00h	00h	60h	2
25	SGRAM cycle time @CAS latency of 1	-	-	-	-	00h	00h	00h	00h	2
26	SGRAM access time @CAS latency of 1	-	-	-	-	00h	00h	00h	00h	2
27	Minimum row precharge time (=tRP)	20ns	18ns	21ns	20ns	14h	12h	15h	14h	2
28	Minimum row active to row active delay (tRRD)	10ns	12ns	14ns	16ns	0Ah	0Ch	0Eh	10h	2
29	Minimum RAS to CAS delay (=tRCD)	20ns	18ns	21ns	20ns	14h	12h	15h	14h	2
30	Minimum activate to precharge time (=tRAS)	40ns	42ns	49ns	48ns	28h	2Ah	31h	30h	2
31	Module bank density	1 bank of 4MB				01h				
32	Address and Command signal Input setup time (=tSS)	1.5ns	1.5ns	1.8ns	2ns	15h	15h	18h	20h	2
33	Address and Command signal Input hold time (=tSH)	1ns	1ns	1ns	1ns	10h	10h	10h	10h	2
34	Data signal Input setup time (=tSS)	1.5ns	1.5ns	1.8ns	2ns	15h	15h	18h	20h	2

SGRAM MODULE

KMM965G112AQ(P)N / KMM966G112AQ(P)N

Byte #	Function Described	Function Supported				Hex value				Note
		-5	-6	-7	-8	-5	-6	-7	-8	
35	Data signal Input hold time (=tSH)	1ns	1ns	1ns	1ns	10h	10h	10h	10h	2
36	Block Write Size	8 Columns				03h				
37~61	Superset information (maybe used in future)	-				00h				
62	SPD data revision code	Initial Release				00h				TBD
63	Checksum for bytes 0 ~ 62	-				A8h	C8h	F8h	1Ch	
64	Manufacturer JEDEC ID code	Samsung				CEh				
65~71 Manufacturer JEDEC ID code	Samsung				00h				
72	Manufacturing location	Onyang Korea				01h				
73	Manufacturer part # (Samsung memory)	K				4Bh				
74	Manufacturer part # (Samsung memory)	M				4Dh				
75	Manufacturer part # (Memory module)	M				4Dh				
76	Manufacturer part # (Memory type & edge connector)	9				39h				
77	Manufacturer part # (Data bits)	Blank				20h				
78 Manufacturer part # (Data bits)	6				36h				
79 Manufacturer part # (Data bits)	6				36h				
80	Manufacturer part # (Mode & operating voltage)	G				47h				
81	Manufacturer part #	Blank				20h				
82 Manufacturer part #	1				31h				
83	Manufacturer part #	1				31h				
84	Manufacturer part #	2				32h				
85	Manufacturer part # (Component revision)	A(1st Rev.)				41h				
86	Manufacturer part # (Package type)	Q(PQFP) / P(TQFP)				51h / 50h				
87	Manufacturer part # (PCB revision)	N				4Eh				
88	Manufacturer part # (Hyphen)	" - "				2Dh				
89	Manufacturer part # (Power)	G				47h				
90	Manufacturer part # (Minimum cycle time)	5	6	7	8	35h	36h	37h	38h	
91	Manufacturer revision code (For PCB)	N				4Eh				
92 Manufacturer revision code (For component)	A(1st Rev.)				41h				
93	Manufacturing date (Week)	-				-				3
94	Manufacturing date (Year)	-				-				3
95~98	Assembly serial #	-				-				4
99~12	Manufacturer specific data (may be used in future)	-				FFh				
126	Reserved	-				FFh				
127	Reserved	-				FFh				
128+	Unused storage locations					FFh				

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.