

# DDR SDRAM Registered Module

(60FBGA)

184pin Registered Module based on 512Mb B-die (x4, x8)  
with 1,200mil Height & 72-bit ECC

Revision 1.1  
August. 2003

## **Revision History**

**Revision 1.0 (July, 2003)**

- First release

**Revision 1.1 (August, 2003)**

- Corrected typo.

## 1GB, 2GB Registered DIMM

## DDR SDRAM

### 184Pin Registered DIMM based on 512Mb B-die FBGA (x4, x8)

#### Ordering Information

Part Number	Density	Organization	Component Composition	Height
M312L2923BG0-CB3/A2/B0	1GB	128M x 72	64Mx8( K4H510838B) * 18EA	1,125mil
M312L2920BG0-CB3/A2/B0	1GB	128M x 72	128Mx4( K4H510438B) * 18EA	1,125mil
M312L5720BG0-CB3/A2/B0	2GB	256M x 72	128Mx4( K4H510438B) * 36EA	1,200mil

#### Operating Frequencies

	B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)
Speed @CL2	133MHz	133MHz	100MHz
Speed @CL2.5	166MHz	133MHz	133MHz
CL-tRCD-tRP	2.5-3-3	2-3-3	2.5-3-3

#### Feature

- Power supply : Vdd: 2.5V  $\pm$  0.2V, Vddq: 2.5V  $\pm$  0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and  $\overline{\text{CK}}$ )
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8 $\mu$ s refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

# 1GB, 2GB Registered DIMM

# DDR SDRAM

## Pin Configuration (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0/DQS9	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3/DQS12	159	DM5/DQS14
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	/RESET	41	A2	71	*CS2	102	NC	133	DQ31	163	*CS3
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	*CK2	106	DQ13	137	CK0	167	*A13
15	VDDQ	46	VDD	76	*CK2	107	DM1/DQS10	138	/CK0	168	VDD
16	*CK1	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6/DQS15
17	*CK1	48	A0	78	DQS6	109	DQ14	140	DM8/DQS17	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7/DQS16
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2/DQS11	149	DM4/DQS13	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

### Note :

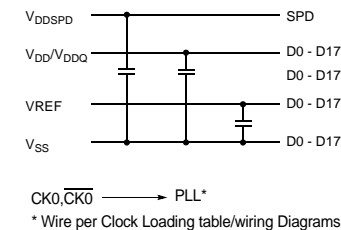
1. \* : These pins are not used in this module.
2. Pins 111, 158 are NC for 1row module [M312L2920BG0] & used for 2row module [M312L2923BG0, M312L5720BG0]
3. Pins 97, 107, 119, 129, 140, 149, 159, 169, 177 : DM (x8 base module) or DQS (x4 base module).

## Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	DM0 ~ DM8	Data - in mask
BA0 ~ BA1	Bank Select Address	VDD	Power supply (2.5V)
DQ0 ~ DQ63	Data input/output	VDDQ	Power Supply for DQS(2.5V)
DQS0 ~ DQS17	Data Strobe input/output	VSS	Ground
CK0,CK0 ~ CK2, CK2	Clock input	VREF	Power supply for reference
CKE0, CKE1(for double banks)	Clock enable input	VDDSPD	Serial EEPROM Power/Supply ( 2.3V to 3.6V )
CS0, CS1(for double banks)	Chip select input	SDA	Serial data I/O
RAS	Row address strobe	SCL	Serial clock
CAS	Column address strobe	SA0 ~ 2	Address in EEPROM
WE	Write enable	NC	No connection
CB0 ~ CB7	Check bit(Data-in/data-out)		

## DDR SDRAM

## Functional Block Diagram

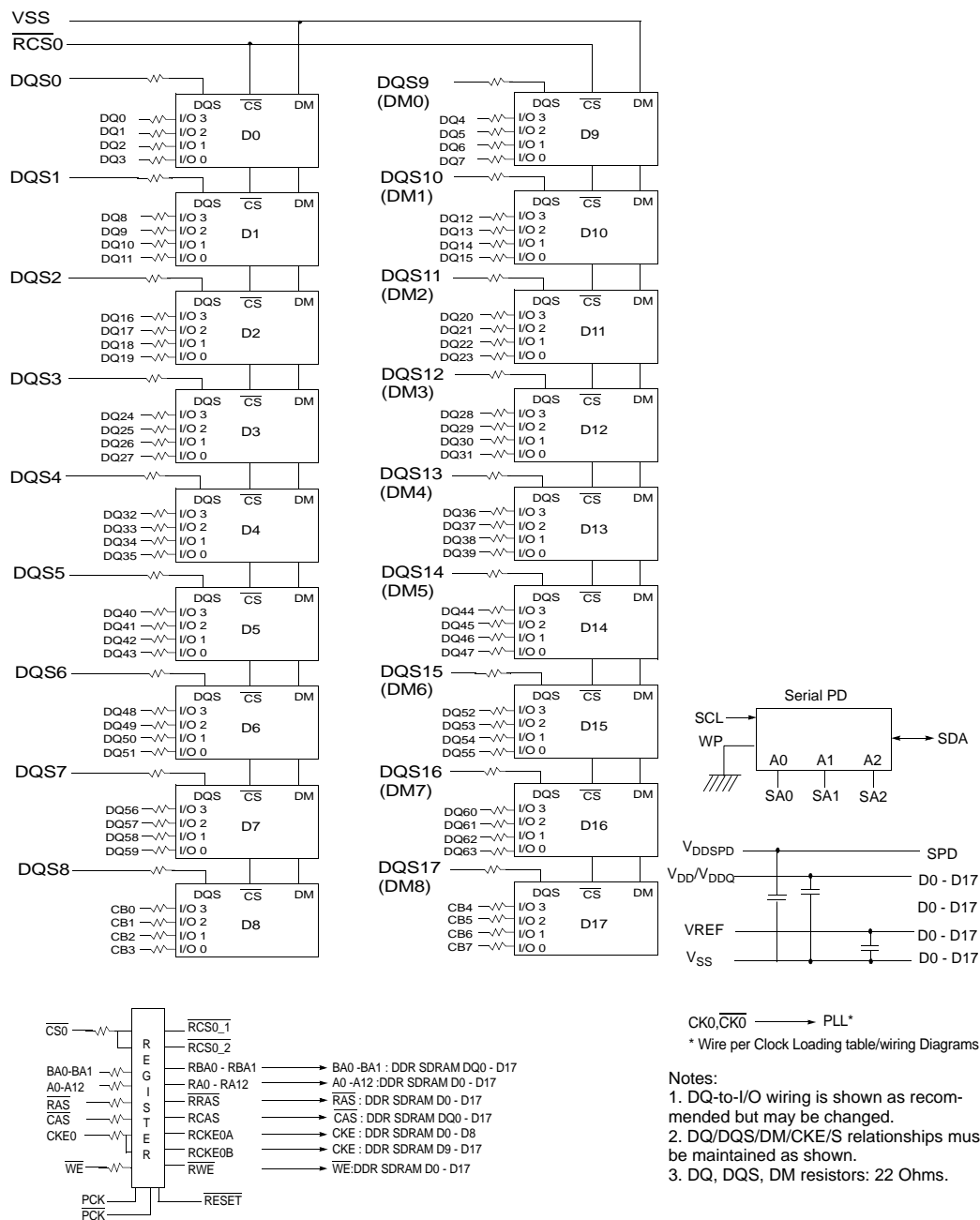


Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.

## DDR SDRAM

### Functional Block Diagram

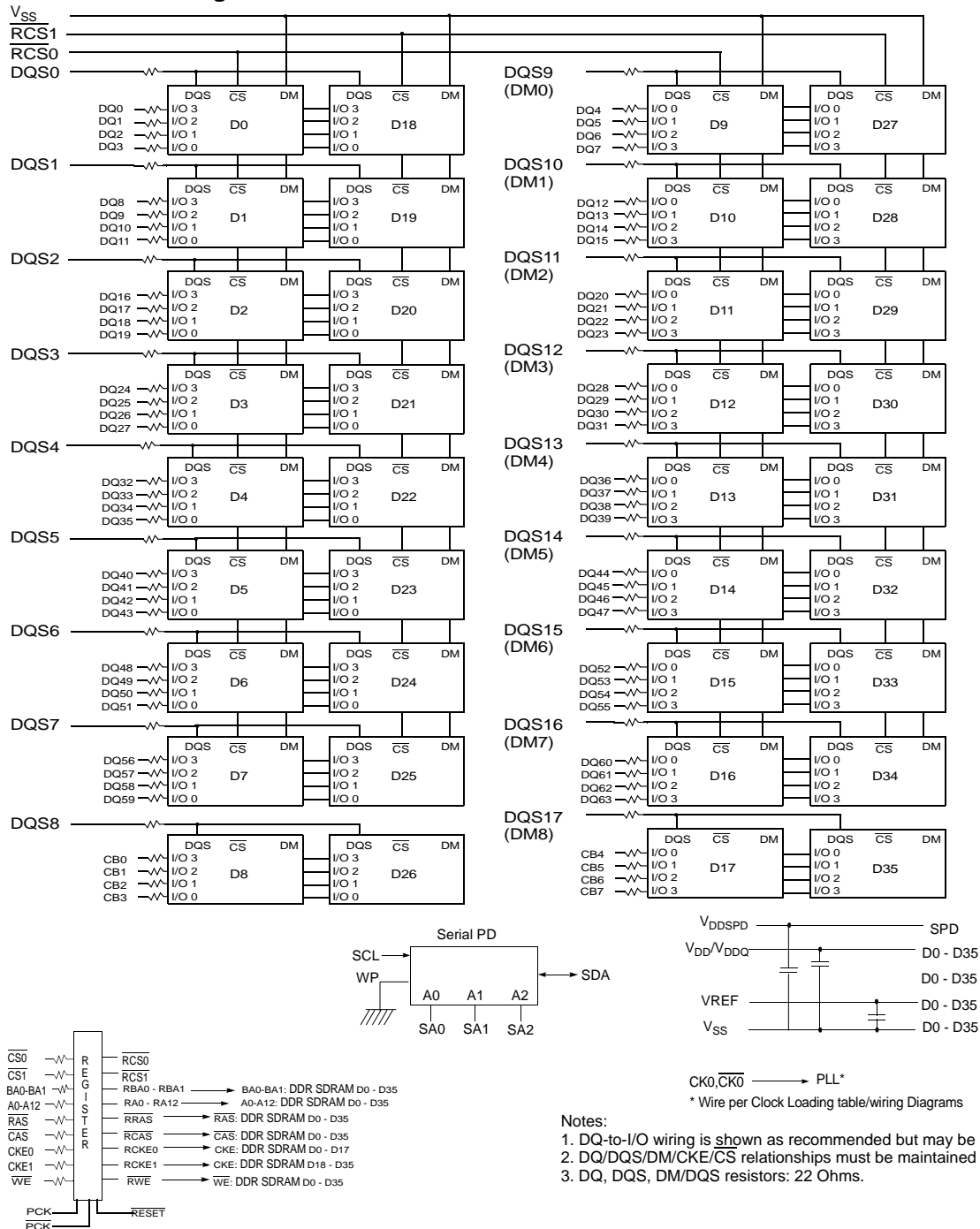


# 1GB, 2GB Registered DIMM

# DDR SDRAM

2GB, 256M x 72 ECC Module [M312L5720BG0] (Populated as 2 bank of x4 DDR SDRAM Module)

## Functional Block Diagram



## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 ~ 3.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 3.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	1.5 * # of component	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## Power &amp; DC Operating Conditions (SSTL\_2 In/Out)

Recommended operating conditions (Voltage referenced to VSS=0V, T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal VDD of 2.5V)	VDD	2.3	2.7		
I/O Supply voltage	VDDQ	2.3	2.7	V	
I/O Reference voltage	VREF	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage(system)	V <sub>TT</sub>	VREF-0.04	VREF+0.04	V	2
Input logic high voltage	V <sub>IH</sub> (DC)	VREF+0.15	VDDQ+0.3	V	4
Input logic low voltage	V <sub>IL</sub> (DC)	-0.3	VREF-0.15	V	4
Input Voltage Level, CK and $\overline{\text{CK}}$ inputs	V <sub>IN</sub> (DC)	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs	V <sub>ID</sub> (DC)	0.3	VDDQ+0.6	V	3
Input leakage current	I <sub>I</sub>	-2	2	uA	
Output leakage current	I <sub>OZ</sub>	-5	5	uA	
Output High Current(Normal strength driver) ;V <sub>OUT</sub> = V <sub>TT</sub> + 0.84V	I <sub>OH</sub>	-16.8		mA	
Output High Current(Normal strength driver) ;V <sub>OUT</sub> = V <sub>TT</sub> - 0.84V	I <sub>OL</sub>	16.8		mA	
Output High Current(Half strength driver) ;V <sub>OUT</sub> = V <sub>TT</sub> + 0.45V	I <sub>OH</sub>	-9		mA	
Output High Current(Half strength driver) ;V <sub>OUT</sub> = V <sub>TT</sub> - 0.45V	I <sub>OL</sub>	9		mA	

**Notes :** 1. Includes  $\pm 25\text{mV}$  margin for DC offset on VREF, and a combined total of  $\pm 50\text{mV}$  margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of  $\leq 3\text{nH}$ .  
2. V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF  
3. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on  $\overline{\text{CK}}$ .  
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHz.



## 1GB, 2GB Registered DIMM

## DDR SDRAM

### DDR SDRAM IDD spec table

#### M312L2923BG0 [ (64M x 8) \* 18 , 1GB Module ]

(V<sub>DD</sub>=2.7V, T = 10°C)

Symbol		B3 (DDR333@CL=2.5)	A2 (DDR266@CL=2)	B0 (DDR266@CL=2.5)	Unit	Notes
IDD0		2,450	2,190	2,190	mA	
IDD1		2,680	2,370	2,370	mA	
IDD2P		590	540	540	mA	
IDD2F		1,420	1,290	1,290	mA	
IDD2Q		950	810	810	mA	
IDD3P		1,040	990	990	mA	
IDD3N		1,780	1,650	1,650	mA	
IDD4R		2,810	2,420	2,420	mA	
IDD4W		3,040	2,550	2,550	mA	
IDD5		3,580	3,360	3,360	mA	
IDD6	Normal	590	540	540	mA	
	Low power	560	510	510	mA	Optional
IDD7A		4,930	4,170	4,170	mA	

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

#### M312L2920BG0 [ (128M x 4) \* 18 , 1GB Module ]

(V<sub>DD</sub>=2.7V, T = 10°C)

Symbol		B3 (DDR333@CL=2.5)	A2 (DDR266@CL=2)	B0 (DDR266@CL=2.5)	Unit	Notes
IDD0		3,000	2,610	2,610	mA	
IDD1		3,450	2,970	2,970	mA	
IDD2P		470	420	420	mA	
IDD2F		1,290	1,170	1,170	mA	
IDD2Q		830	690	690	mA	
IDD3P		920	870	870	mA	
IDD3N		1,650	1,530	1,530	mA	
IDD4R		3,720	3,060	3,060	mA	
IDD4W		4,170	3,330	3,330	mA	
IDD5		5,250	4,950	4,950	mA	
IDD6	Normal	670	420	420	mA	
	Low power	430	380	380	mA	Optional
IDD7A		7,950	6,570	6,570	mA	

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**DDR SDRAM IDD spec table****M312L5720BG0 [ (128M x 4) \* 36, 2GB Module ]**(V<sub>DD</sub>=2.7V, T = 10°C)

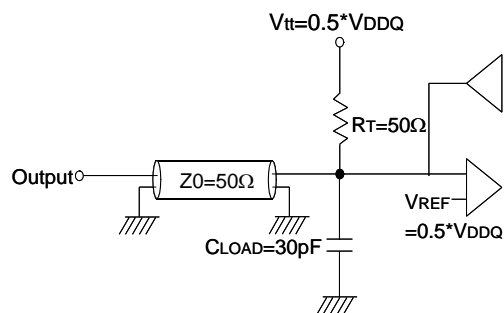
Symbol		B3 (DDR333@CL=2.5)	A2 (DDR266@CL=2)	B0 (DDR266@CL=2.5)	Unit	Notes
IDD0		4,030	3,630	3,630	mA	
IDD1		4,480	3,990	3,990	mA	
IDD2P		680	630	630	mA	
IDD2F		1,960	1,830	1,830	mA	
IDD2Q		1,400	1,170	1,170	mA	
IDD3P		1,580	1,530	1,530	mA	
IDD3N		2,680	2,550	2,550	mA	
IDD4R		4,750	4,080	4,080	mA	
IDD4W		5,200	4,350	4,350	mA	
IDD5		6,280	5,970	5,970	mA	
IDD6	Normal	680	630	630	mA	
	Low power	610	560	560	mA	Optional
IDD7A		8,980	7,590	7,590	mA	

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH}(AC)$	$V_{REF} + 0.31$		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	$V_{IL}(AC)$		$V_{REF} - 0.31$	V	3
Input Differential Voltage, CK and CK inputs	$V_{ID}(AC)$	0.7	$V_{DDQ} + 0.6$	V	1
Input Crossing Point Voltage, CK and CK inputs	$V_{IX}(AC)$	$0.5 \cdot V_{DDQ} - 0.2$	$0.5 \cdot V_{DDQ} + 0.2$	V	2

- Note :** 1. VID is the magnitude of the difference between the input level on CK and the input on  $\overline{CK}$ .  
 2. The value of  $V_{IX}$  is expected to equal  $0.5 \cdot V_{DDQ}$  of the transmitting device and must track variations in the DC level of the same.  
 3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relation to a Vref envelope that has been bandwidth limited 20MHz.



Output Load Circuit (SSTL\_2)

(VDD=2.5V, VDDQ=2.5V, TA= 25°C, f=1MHz)

## Input/Output Capacitance

Parameter	Symbol	M312L2920BG0		Unit
		Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	CIN1	9	11	pF
Input capacitance(CKE0)	CIN2	9	11	pF
Input capacitance( $\overline{CS0}$ )	CIN3	9	11	pF
Input capacitance( CLK0, $\overline{CLK0}$ )	CIN4	11	12	pF
Input capacitance(DM0~DM8)	CIN5	10	11	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	10	11	pF
Data input/output capacitance (CB0~CB7)	Cout2	10	11	pF

Parameter	Symbol	M312L2923BG0, M312L5720BG0		Unit
		Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	CIN1	9	11	pF
Input capacitance(CKE0,CKE1)	CIN2	9	11	pF
Input capacitance( $\overline{CS0}$ , $\overline{CS1}$ )	CIN3	9	11	pF
Input capacitance( CLK0, $\overline{CLK0}$ )	CIN4	11	12	pF
Input capacitance(DM0~DM8)	CIN5	13	15	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	13	15	pF
Data input/output capacitance (CB0~CB7)	Cout2	13	15	pF

## AC Timing Parameters &amp; Specifications

Parameter	Sym- bol	B3 (DDR333@CL=2.5))		A2 (DDR266@CL=2)		B0 (DDR266@CL=2.5)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Row cycle time	tRC	60		65		65		ns	
Refresh row cycle time	tRFC	72		75		75		ns	
Row active time	tRAS	42	70K	45	120K	45	120K	ns	
RAS to CAS delay	tRCD	18		20		20		ns	
Row precharge time	tRP	18		20		20		ns	
Row active to Row active	tRRD	12		15		15		ns	
Write recovery time	tWR	15		15		15		ns	
Last data in to Read com- mand	tWTR	1		1		1		tCK	
Col. address to Col. address	tCCD	1		1		1		tCK	
Clock cycle time	CL=2.0	7.5	12	7.5	12	10	12	ns	
	CL=2.5	6	12	7.5	12	7.5	12	ns	
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from	tDQSQ	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time	tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to ouput	tDQSQ	-	0.4	-	0.5	-	0.5	ns	12
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time	tWPRE	0		0		0		ns	3
DQS-in hold time	tWPRE	0.25		0.25		0.25		tCK	
DQS falling edge to CK ris-	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge from CK	tDSH	0.2		0.2		0.2		tCK	
DQS-in high level width	tDQSH	0.35		0.35		0.35		tCK	
DQS-in low level width	tDQSL	0.35		0.35		0.35		tCK	
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input	tIS	0.75		0.9		0.9		ns	i,5.7~
Address and Control Input	tIH	0.75		0.9		0.9		ns	i,5.7~
Address and Control Input	tIS	0.8		1.0		1.0		ns	i, 6~9
Address and Control Input	tIH	0.8		1.0		1.0		ns	i, 6~9
Data-out high impedance time from CK/CK	tHZ		+0.7		+0.75		+0.75	ns	1
Data-out low impedance time from CK/CK	tLZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	1
Input Slew Rate(for input	tSL(I)	0.5		0.5		0.5		V/ ns	
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		0.5		0.5		V/ ns	
Output Slew Rate(x4,x8)	tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ ns	
Output Slew Rate Matching	tSLMR	0.67	1.5	0.67	1.5	0.67	1.5		

Parameter	Symbol	B3 (DDR333@CL=2.5))		A2 (DDR266@CL=2)		B0 (DDR266@CL=2.5)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	12		15		15		ns	
DQ & DM setup time to DQS	tDS	0.45		0.5		0.5		ns	j, k
DQ & DM hold time to DQS	tDH	0.45		0.5		0.5		ns	j, k
Control & Address input	tIPW	2.2		2.2		2.2		ns	8
DQ & DM input pulse width	tDIPW	1.75		1.75		1.75		ns	8
Power down exit time	tPDEX	6		7.5		7.5		ns	
Exit self refresh to non-Read	tXSNR	75		75		75		ns	
Exit self refresh to read com-	tXSRD	200		200		200		tCK	
Refresh interval time	tREFI		7.8		7.8		7.8	us	4
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	11
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	10, 11
Data hold skew factor	tQHS		0.5		0.75		0.75	ns	11
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	2
Active to Read with Auto pre-charge command	tRAP	18		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	13

### System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR333, DDR266 & DDR200 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

**Table 1 : Input Slew Rate for DQ, DQS, and DM**

AC CHARACTERISTICS		DDR333		DDR266		DDR200		Units	Notes
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX		
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	TBD	TBD	TBD	TBD	0.5	4.0	V/ns	a, m

**Table 2 : Input Setup & Hold Time Derating for Slew Rate**

Input Slew Rate	tIS	tIH	Units	Notes
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

**Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate**

Input Slew Rate	tDS	tDH	Units	Notes
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

**Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate**

Delta Slew Rate	tDS	tDH	Units	Notes
+/- 0.0 V/ns	0	0	ps	j
+/- 0.25 V/ns	+50	+50	ps	j
+/- 0.5 V/ns	+100	+100	ps	j

**Table 5 : Output Slew Rate Characteristic (X4, X8 Devices only)**

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g,h

**Table 6 : Output Slew Rate Characteristic (X16 Devices only)**

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g,h

**Table 7 : Output Slew Rate Matching Ratio Characteristics**

AC CHARACTERISTICS	DDR333		DDR266		
PARAMETER	MIN	MAX	MIN	MAX	Notes
Output Slew Rate Matching Ratio (Pullup to Pulldown)	TBD	TBD	TBD	TBD	e,m

**System Notes :**

a. Pullup slew rate is characterized under the test conditions as shown in Figure 1.

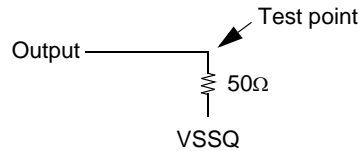


Figure 1 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

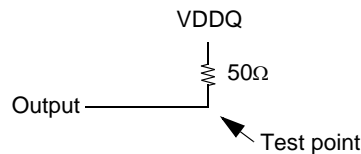


Figure 2 : Pulldown slew rate test load

- c. Pullup slew rate is measured between (VDDQ/2 - 320 mV +/- 250 mV)  
Pulldown slew rate is measured between (VDDQ/2 + 320 mV +/- 250 mV)  
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.  
Example : For typical slew rate, DQ0 is switching  
For minimum slew rate, all DQ bits are switching from either high to low, or low to high.  
The remaining DQ bits remain the same as for previous state.
- d. Evaluation conditions  
Typical : 25 °C (T Ambient), VDDQ = 2.5V, typical process  
Minimum : 70 °C (T Ambient), VDDQ = 2.3V, slow - slow process  
Maximum : 0 °C (T Ambient), VDDQ = 2.7V, fast - fast process
- e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.
- f. Verified under typical conditions for qualification purposes.
- g. TSOPII package devices only.
- h. Only intended for operation up to 266 Mbps per pin.
- i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
- j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.  
The delta rise/fall rate is calculated as:  $\{1/(\text{Slew Rate1})\} - \{1/(\text{Slew Rate2})\}$   
For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.
- k. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC - AC slew rate and the DC- DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(ac) or VIH(DC) to VIL(DC), and similarly for rising transitions.
- m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotony.

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A0 ~ A9 A11, A12	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address (A0~A9, A11,A12)		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X		8	
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

**Note** : 1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

7. Burst stop command is valid at every burst length.

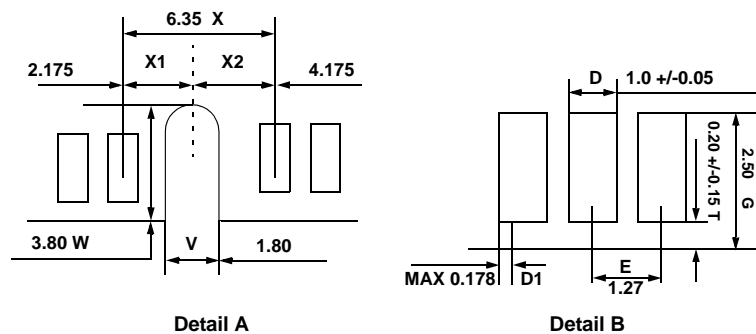
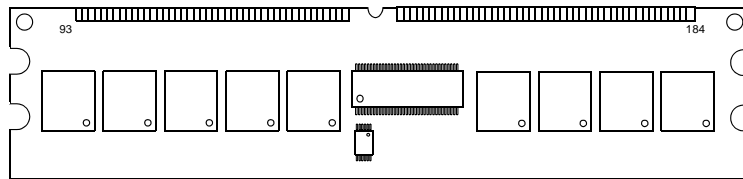
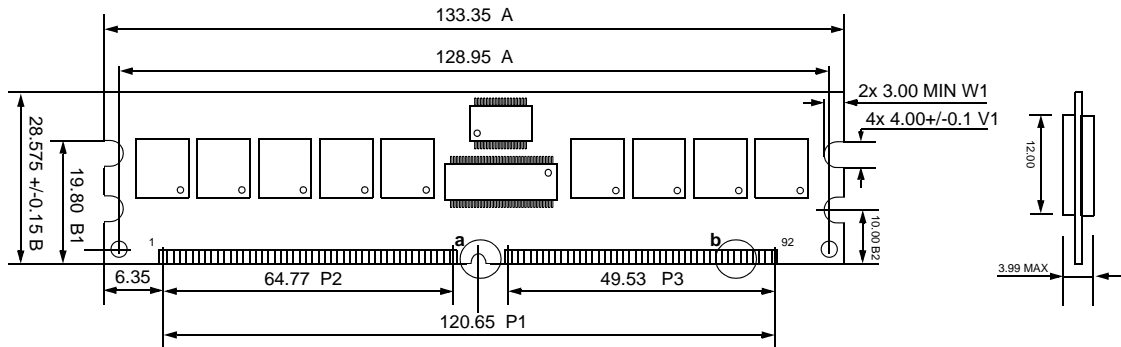
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.



## DDR SDRAM

## Units : Millimeters



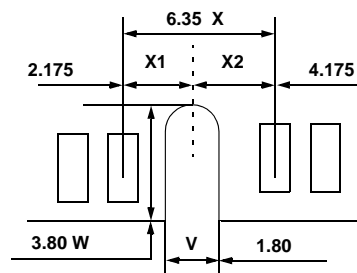
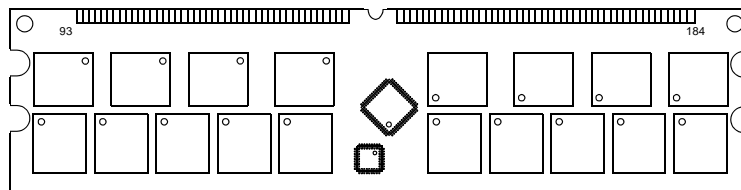
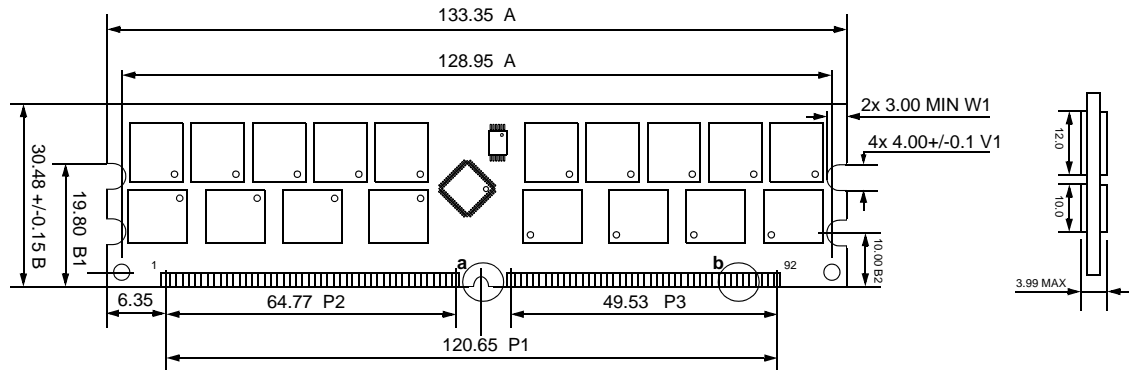
**Rev. 1.1 August. 2003**

# 1GB, 2GB Registered DIMM

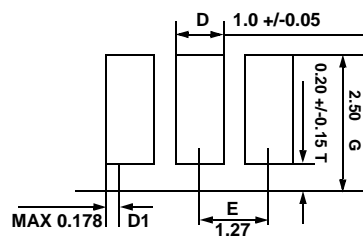
# DDR SDRAM

## Physical Dimensions: 256Mx72 (M312L5720BG0)

Units : Millimeters



Detail A



Detail B

Tolerances :  $\pm 0.005$ (.13) unless otherwise specified  
The used device is 128Mx4 DDR SDRAM, FBGA  
DDR SDRAM Part No : K4H510438B-G\*\*\*