

Unbuffered 8Mx64 DIMM

(4Mx16 base)

Revision 0.0

Jan. 1999

Revision History

Version 0.0 (Jan. 1999)

- The 4th generation of 64Mb DRAM components are applied to this module.

DRAM MODULE

M366F080(8)4CT1-C

M366F080(8)4CT1-C EDO Mode without buffer

8M x 64 DRAM DIMM Using 4Mx16, 8K & 4K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung M366F080(8)4CT1-C is a 8Mx64bits Dynamic RAM high density memory module. The Samsung M366F080(8)4CT1-C consists of eight CMOS 4Mx16bits DRAMs in TSOP 400mil packages and one 2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M366F080(8)4CT1-C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
-C50	50ns	13ns	84ns	20ns
-C60	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
M366F0804CT1-C	TSOP	4K	4K/64ms	
M366F0884CT1-C	TSOP	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{\text{CAS}}$ -before-RAS Refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{\text{CAS1}}$	57	DQ18	85	Vss	113	$\overline{\text{CAS5}}$	141	DQ50
2	DQ0	30	$\overline{\text{RAS0}}$	58	DQ19	86	DQ32	114	$\overline{\text{RAS1}}$	142	DQ51
3	DQ1	31	$\overline{\text{OE0}}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{\text{OE2}}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{\text{RAS2}}$	73	Vcc	101	DQ45	129	$\overline{\text{RAS3}}$	157	Vcc
18	Vcc	46	$\overline{\text{CAS2}}$	74	DQ28	102	Vcc	130	$\overline{\text{CAS6}}$	158	DQ60
19	DQ14	47	$\overline{\text{CAS3}}$	75	DQ29	103	DQ46	131	$\overline{\text{CAS7}}$	159	DQ61
20	DQ15	48	W2	76	DQ30	104	DQ47	132	DU	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	W0	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{\text{CAS0}}$	56	DQ17	84	Vcc	112	$\overline{\text{CAS4}}$	140	DQ49	168	Vcc

Note : A12 is used for only M366F0884CT1-C (8K ref.)

PIN NAMES

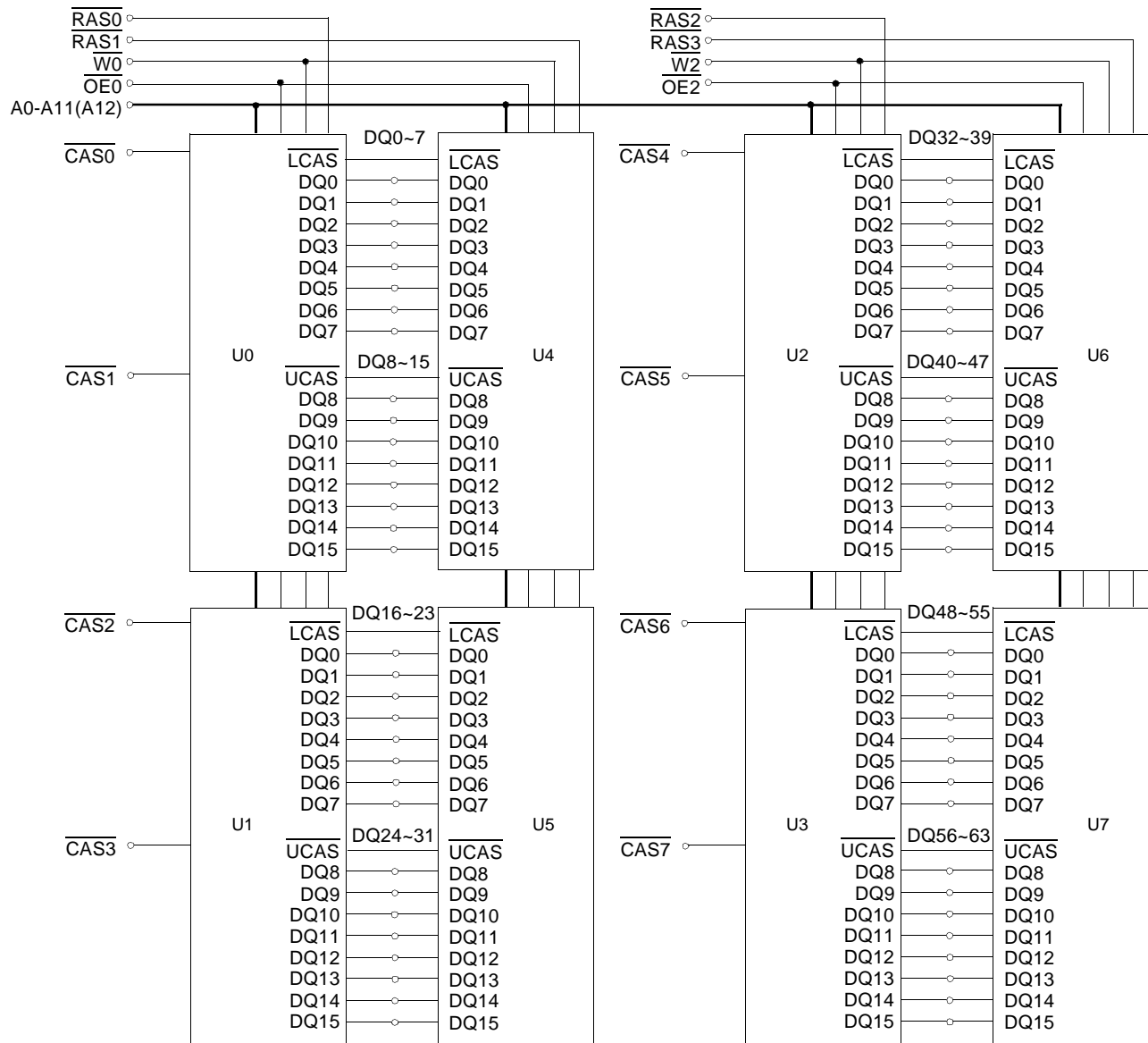
Pin Name	Function
A0 - A11	Address Input (4K ref.)
A0 - A12	Address Input (8K ref.)
DQ0 - DQ63	Data In/Out
W0, W2	Read/Write Enable
$\overline{\text{OE0}}$, $\overline{\text{OE2}}$	Output Enable
$\overline{\text{RAS0}}$ - $\overline{\text{RAS3}}$	Row Address Strobe
$\overline{\text{CAS0}}$ - $\overline{\text{CAS7}}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - CB7	Check Bit

* These pins are not used in this module.

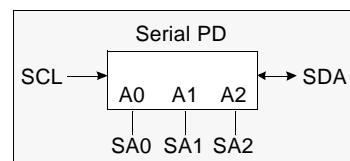
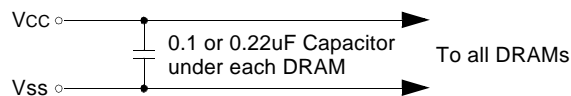
DRAM MODULE

M366F080(8)4CT1-C

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only M366F0884CT1 (8K ref.)



DRAM MODULE

M366F080(8)4CT1-C

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	8	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M366F0884CT1		M366F0804CT1		Unit
		Min	Max	Min	Max	
I _{CC1}	-50	-	324	-	484	mA
	-60	-	284	-	444	mA
I _{CC2}	Don't care	-	8	-	8	mA
I _{CC3}	-50	-	324	-	484	mA
	-60	-	284	-	444	mA
I _{CC4}	-50	-	364	-	364	mA
	-60	-	324	-	324	mA
I _{CC5}	Don't care	-	4	-	4	mA
I _{CC6}	-50	-	484	-	484	mA
	-60	-	444	-	444	mA
I _{I(L)}	Don't care	-10	10	-10	10	uA
I _{O(L)}		-10	10	-10	10	uA
V _{OH}	Don't care	2.4	-	2.4	-	V
V _{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * (R_{AS}, C_{AS}, Address cycling @trc=min)

I_{CC2} : Standby Current (R_{AS}=C_{AS}=W=V_{IH})

I_{CC3} : R_{AS} Only Refresh Current * (C_{AS}=V_{IH}, R_{AS} cycling @trc=min)

I_{CC4} : Extended Data Out Mode Current * (R_{AS}=V_{IL}, C_{AS} cycling : t_{HPC}=min)

I_{CC5} : Standby Current (R_{AS}=C_{AS}=W=V_{CC}-0.2V)

I_{CC6} : C_{AS}-Before-R_{AS} Refresh Current * (R_{AS} and C_{AS} cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while R_{AS}=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

DRAM MODULE

M366F080(8)4CT1-C

CAPACITANCE (TA = 25°C, VCC=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	CIN1	-	50	pF
Input capacitance[W0, W2, OE0, OE2]	CIN2	-	38	pF
Input capacitance[RAS0 - RAS3]	CIN3	-	24	pF
Input capacitance[CAS0 - CAS7]	CIN4	-	24	pF
Input/Output capacitance[DQ0-DQ63]	CDQ	-	24	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : VIH/VIL=2.2/0.7V, VOH/VOL=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		ns	
Read-modify-write cycle time	tRWC	128		153		ns	
Access time from RAS	tRAC		50		60	ns	3,4,9
Access time from CAS	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,9
CAS to output in Low-Z	tCLZ	3		3		ns	3
OE to output in Low-Z	tOLZ	3		3		ns	3
Output buffer turn-off delay from CAS	tCEZ	3	13	3	13	ns	6,12
Transition time(rise and fall)	tT	1	50	1	50	ns	2
RAS precharge time	tRP	30		40		ns	
RAS pulse width	tRAS	50	10K	60	10K	ns	
RAS hold time	tRSH	8		10		ns	
CAS hold time	tCSH	38		40		ns	
CAS pulse width	tCAS	8	10K	10	10K	ns	
RAS to CAS delay time	tRCD	17	37	20	45	ns	4
RAS to column address delay time	tRAD	12	25	15	30	ns	9
CAS to RAS precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	7		10		ns	
Column address set-up time	tASC	0		0		ns	13
Column address hold time	tCAH	7		10		ns	13
Column address to RAS lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to CAS	tRCH	0		0		ns	8
Read command hold referenced to RAS	tRRH	0		0		ns	8
Write command hold time	tWCH	7		10		ns	
Write command pulse width	tWP	7		10		ns	
Write command to RAS lead time	tRWL	8		10		ns	
Write command to CAS lead time	tCWL	7		10		ns	16
Data set-up time	tDS	0		0		ns	
Data hold time	tDH	7		10		ns	
Refresh period (4K & 8K Ref.)	tREF		64		64	ms	
Write command set-up time	tWCS	0		0		ns	7
CAS to W delay time	tCWD	33		38		ns	7, 15
RAS to W delay time	tRWD	70		84		ns	7

DRAM MODULE

M366F080(8)4CT1-C

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

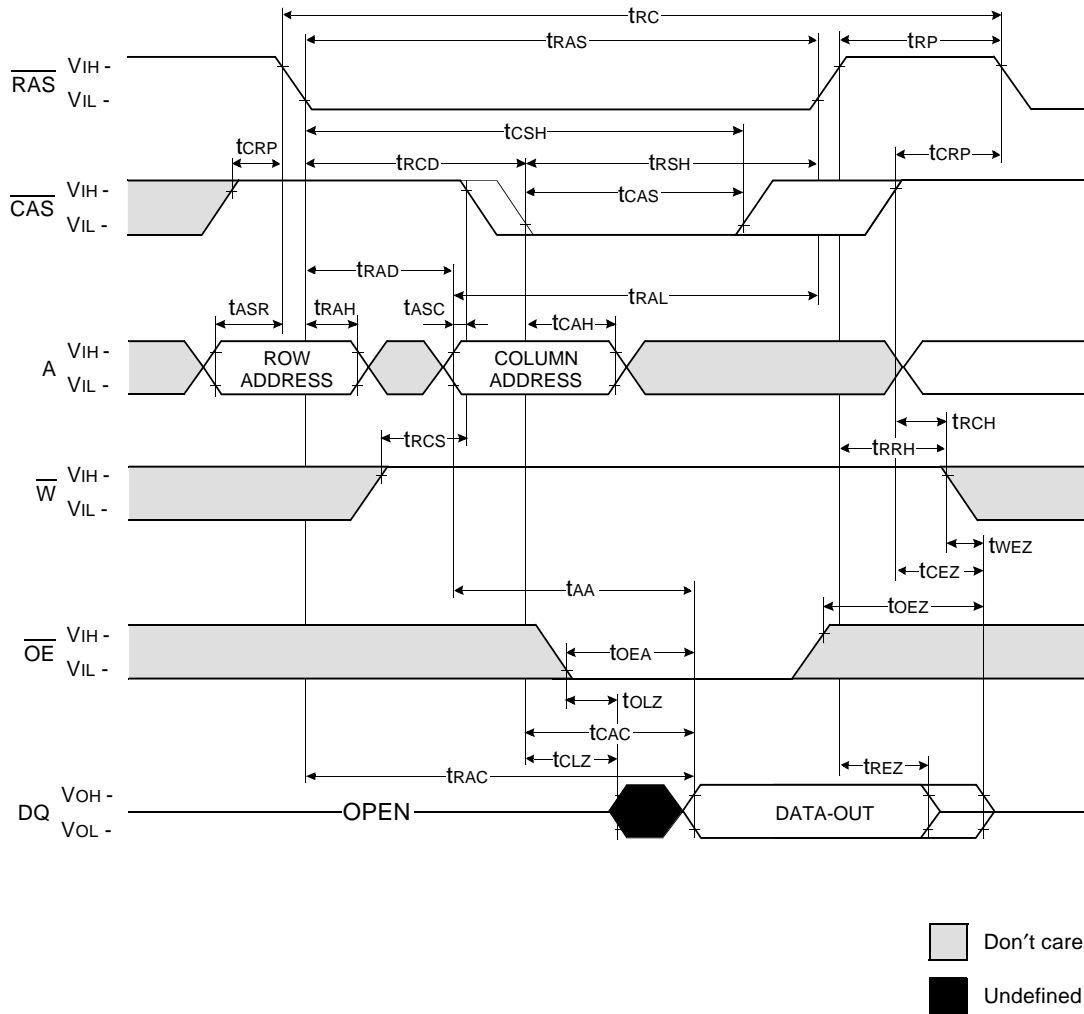
Test condition : Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Column address to \overline{W} delay time	tAWD	45		53		ns	7
\overline{CAS} precharge to \overline{W} delay time	tCPWD	47		58		ns	
\overline{CAS} setup time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	5		5		ns	17
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		ns	
\overline{RAS} to \overline{CAS} precharge time	trPC	5		5		ns	
Access time from \overline{CAS} precharge	tCPA		28		35	ns	3
Hyper page mode cycle time	tHPC	20		25		ns	10
Hyper page mode read-modify write cycle time	tHPRWC	67		73		ns	10
\overline{CAS} precharge time (Hyper page cycle)	tCP	7		10		ns	14
\overline{RAS} pulse width (Hyper page cycle)	trASP	50	200K	60	200K	ns	
\overline{RAS} hold time from \overline{CAS} precharge	trHCP	30		35		ns	
\overline{OE} access time	tOEA		13		15	ns	
\overline{OE} to data delay	tOED	10		13		ns	
Output buffer turn off delay time from \overline{OE}	tOEZ	3	13	3	13	ns	6
\overline{OE} command hold time	tOEH	5		5		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from \overline{RAS}	trEZ	3	13	3	13	ns	6,12
Output buffer turn off delay from \overline{W}	twEZ	3	13	3	13	ns	6
\overline{W} to data delay	twED	15		15		ns	
\overline{OE} to \overline{CAS} hold time	tOCH	5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		ns	
\overline{OE} precharge time	tOEP	5		5		ns	
\overline{W} pulse width (Hyper page cycle)	twPE	5		5		ns	

NOTES

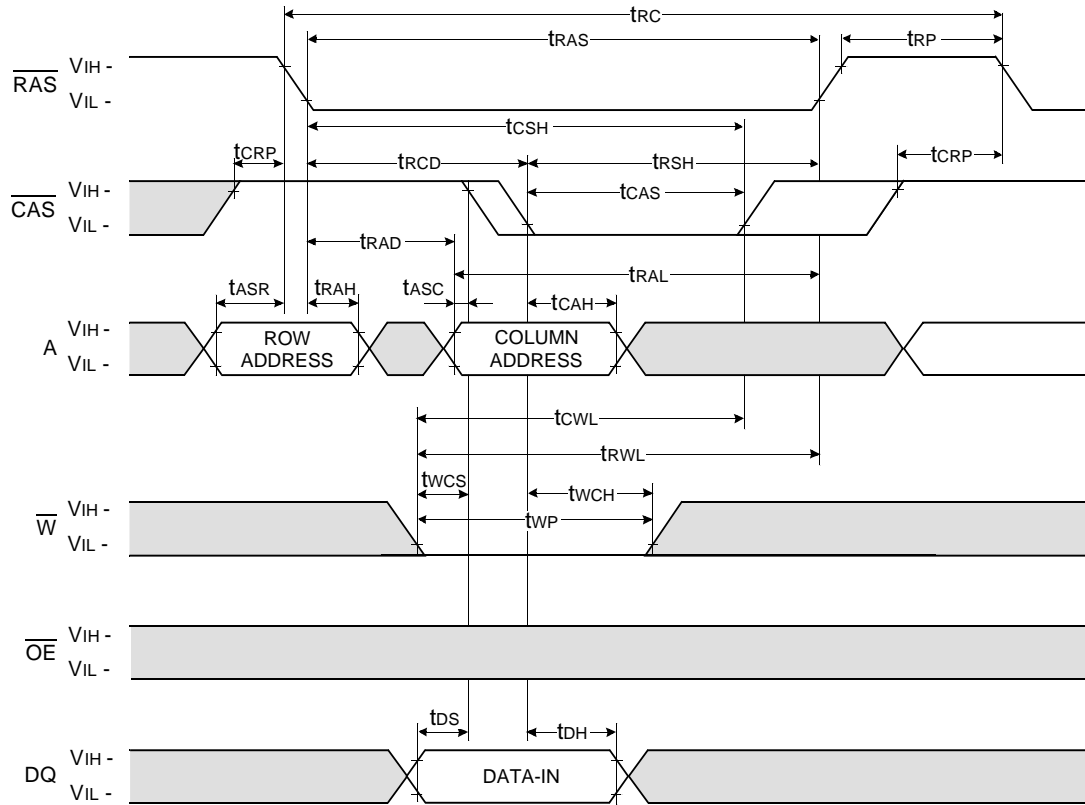
1. An initial pause of 200 μ s is required after power-up followed by any 8 RAS-only or $\overline{\text{CAS}}$ -before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL} . $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, The condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
10. $t_{\text{ASC}} \geq 6\text{ns}$, Assume $t_{\text{T}} = 2.0\text{ns}$.
11. For all of the refresh mode except distributed $\overline{\text{CAS}}$ -before-RAS refresh, 4096 cycle of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.
12. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
13. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
14. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.
17. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.

READ CYCLE



WRITE CYCLE (EARLY WRITE)

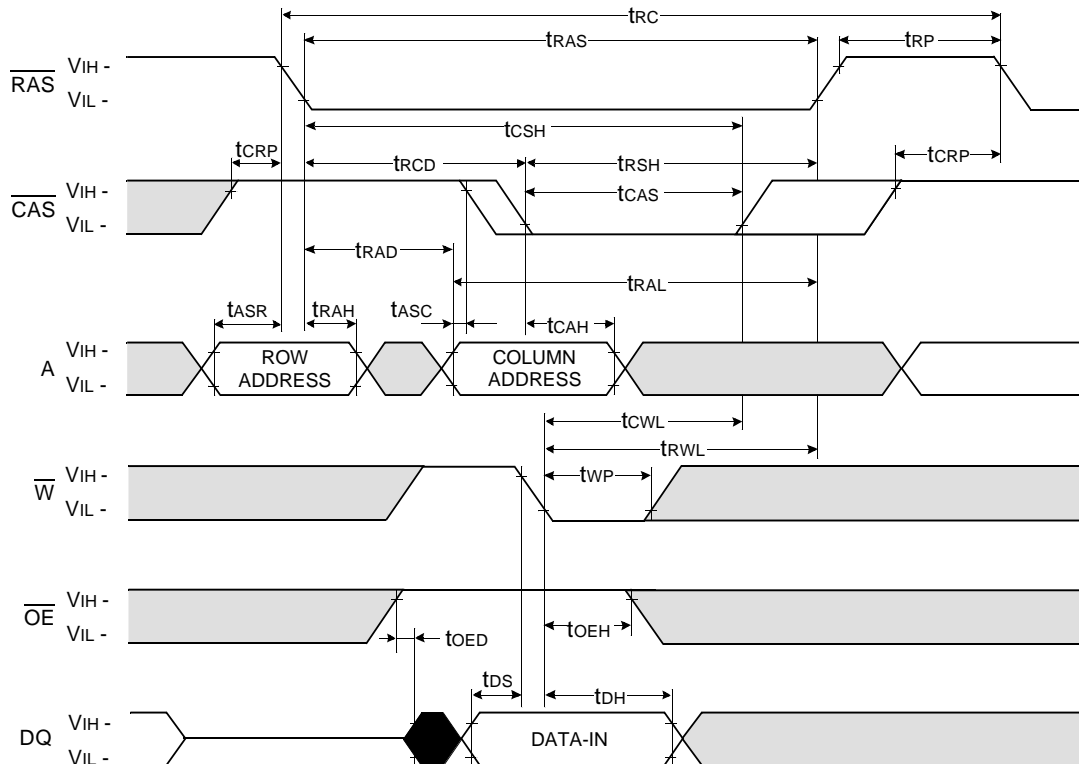
NOTE : DOUT = OPEN



Don't care
Undefined

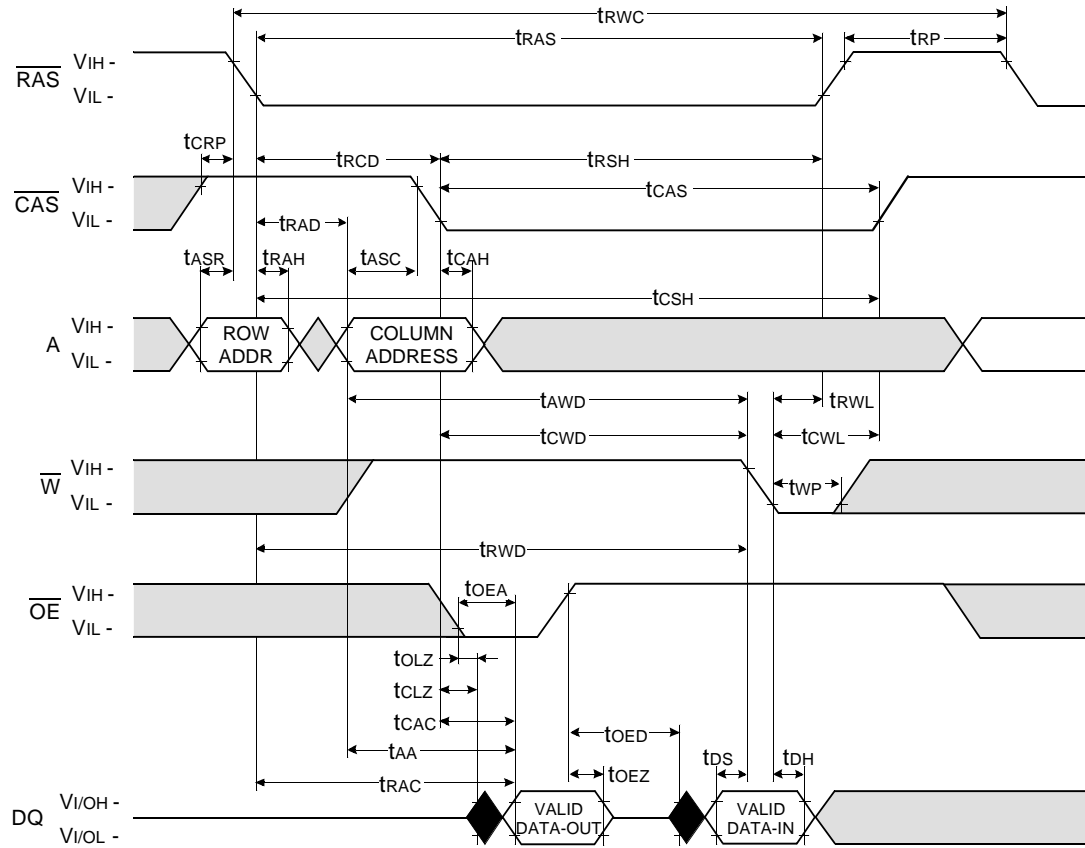
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



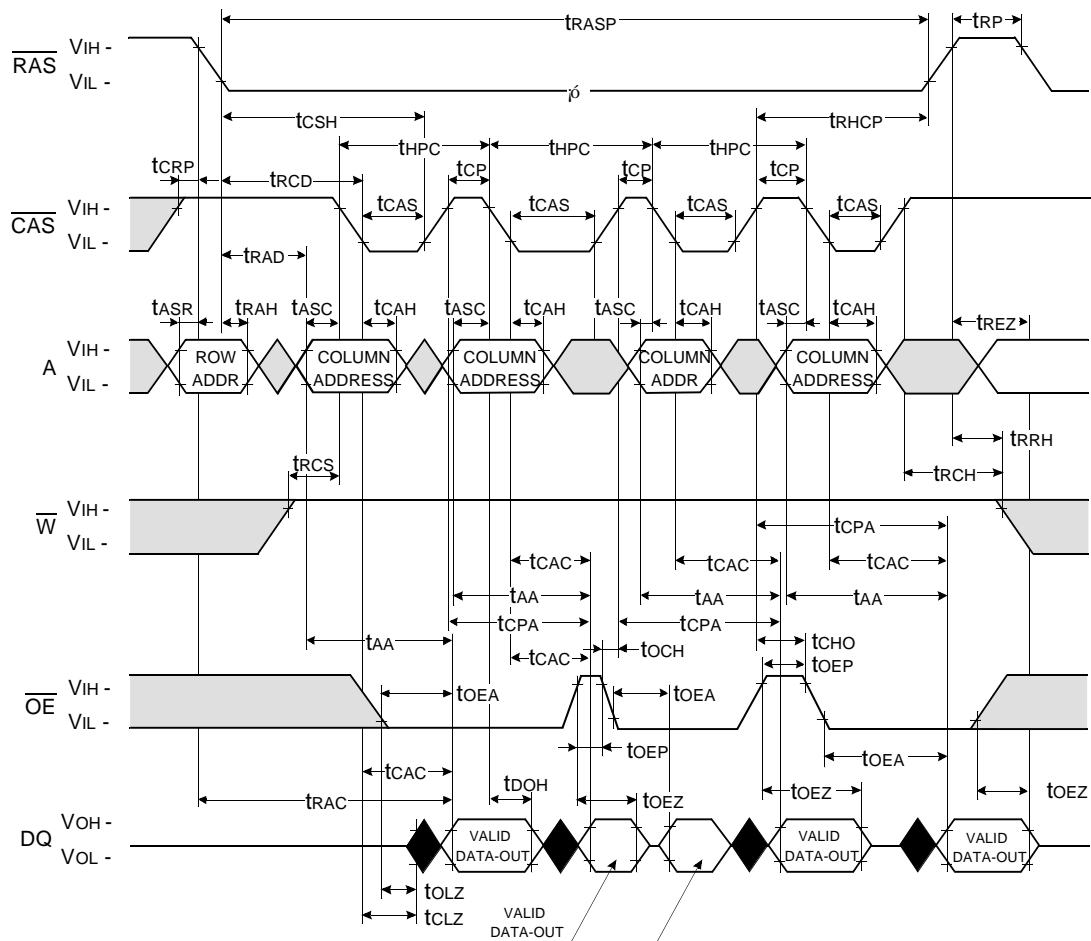
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READ - MODIFY - WRITE CYCLE



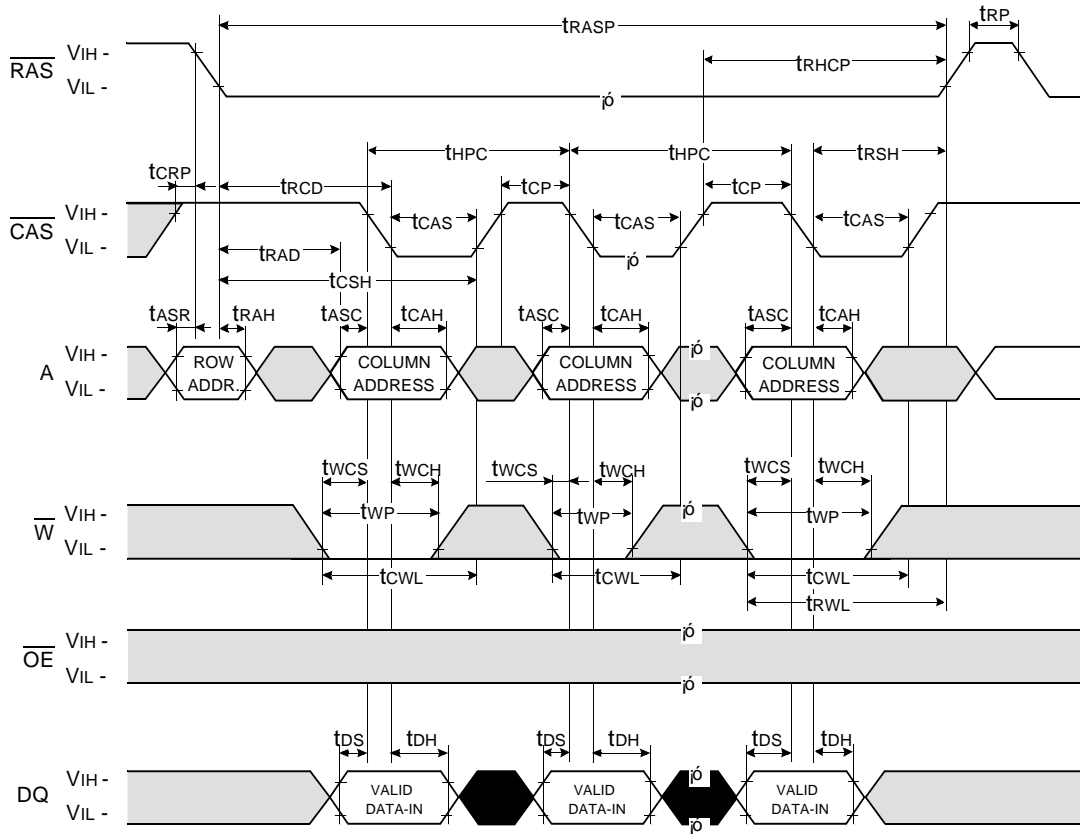
Don't care
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HYPER PAGE READ CYCLE



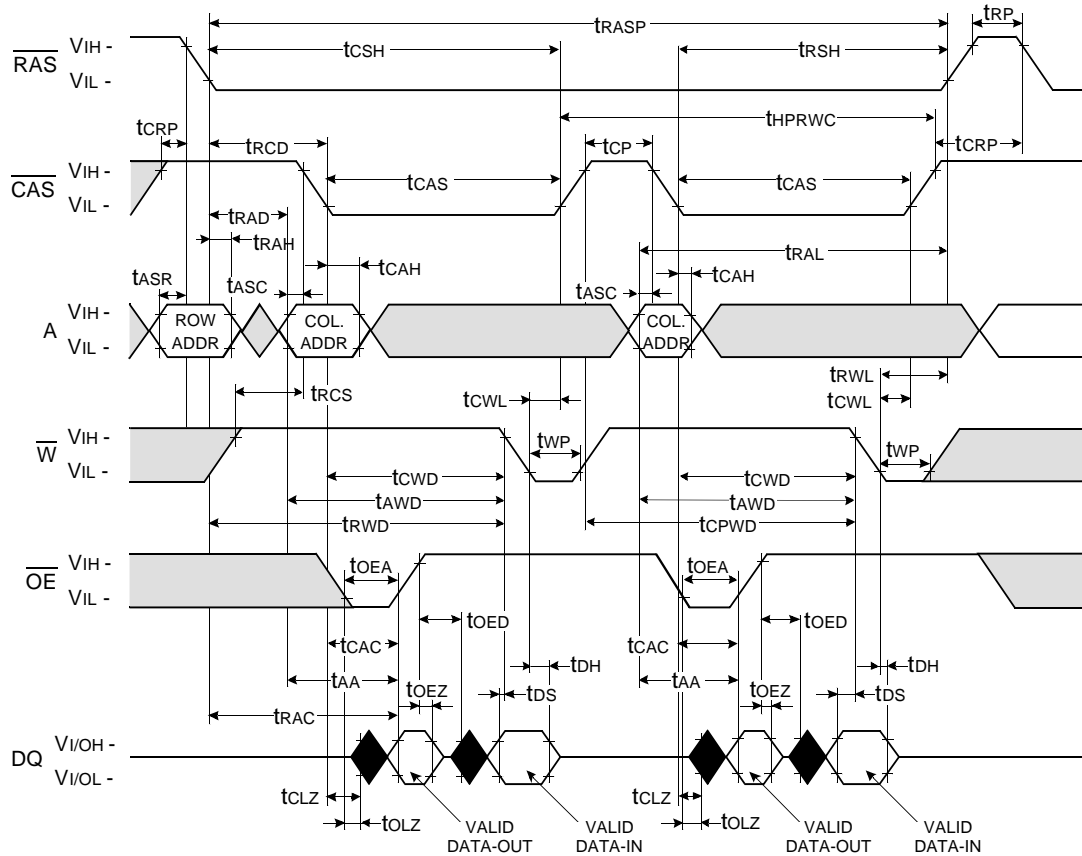
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



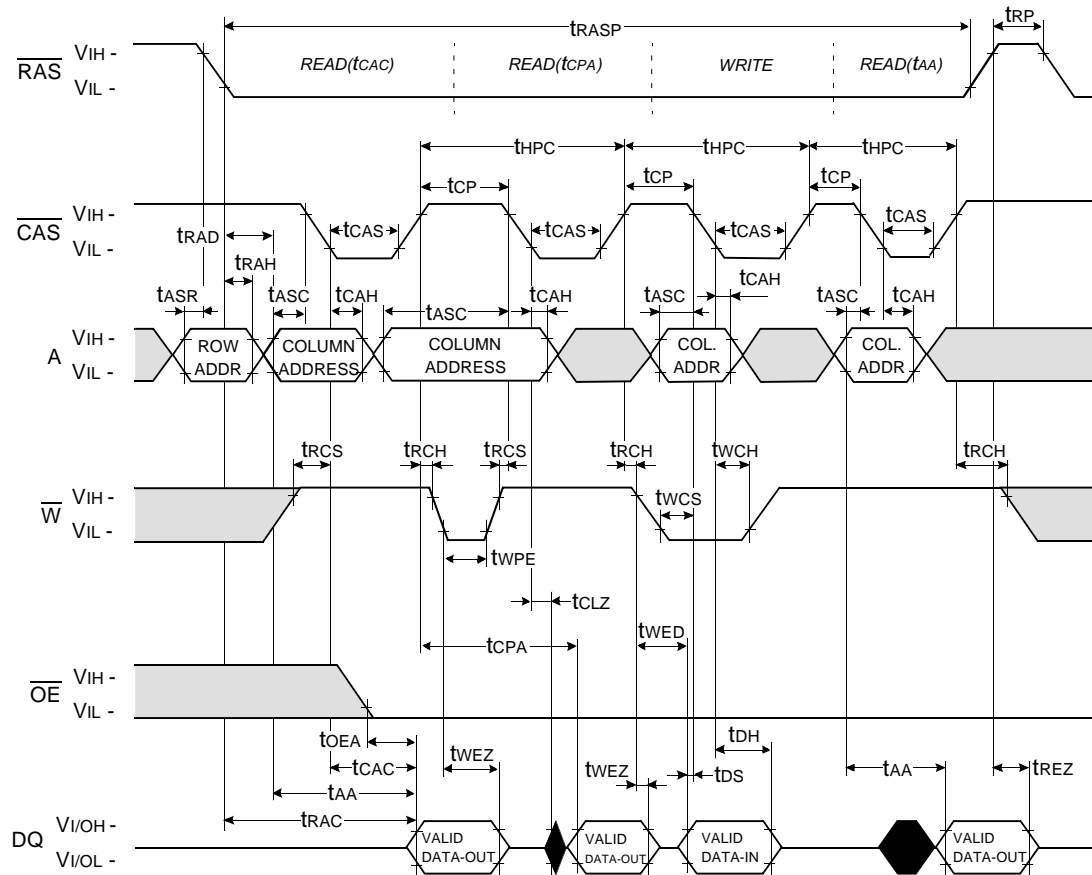
Don't care
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HYPER PAGE READ-MODIFY-WRITE CYCLE



Don't care
Undefined

HYPER PAGE READ AND WRITE MIXED CYCLE

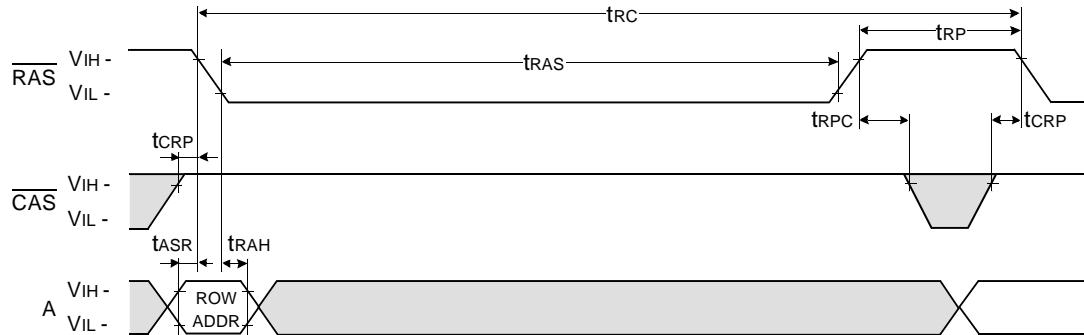


Don't care
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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

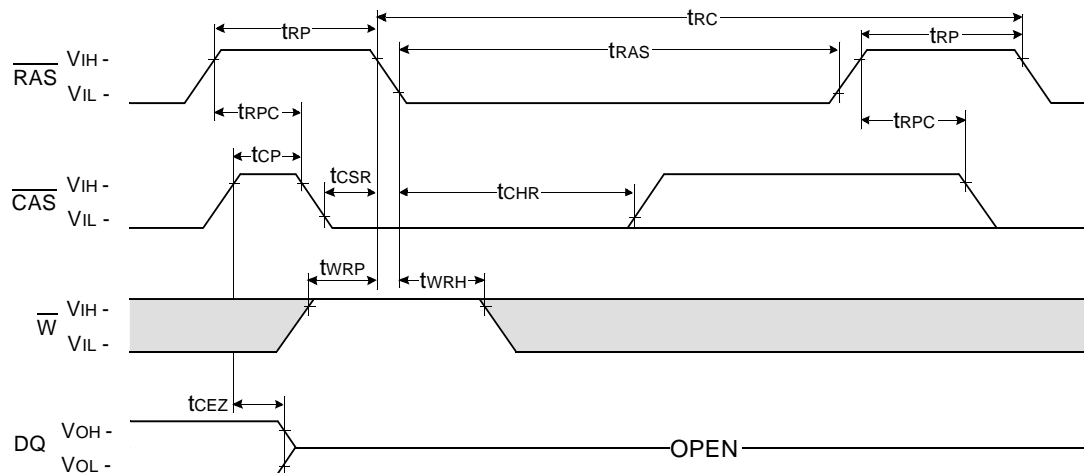
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

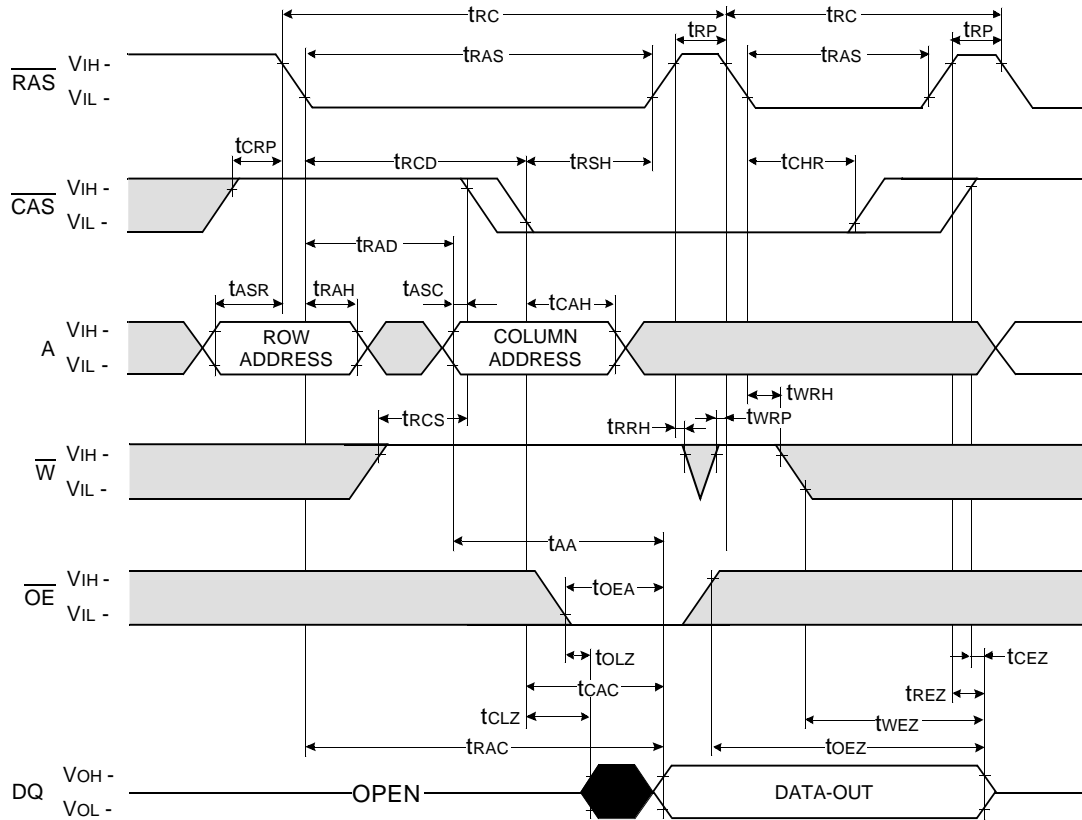
NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
Undefined

* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

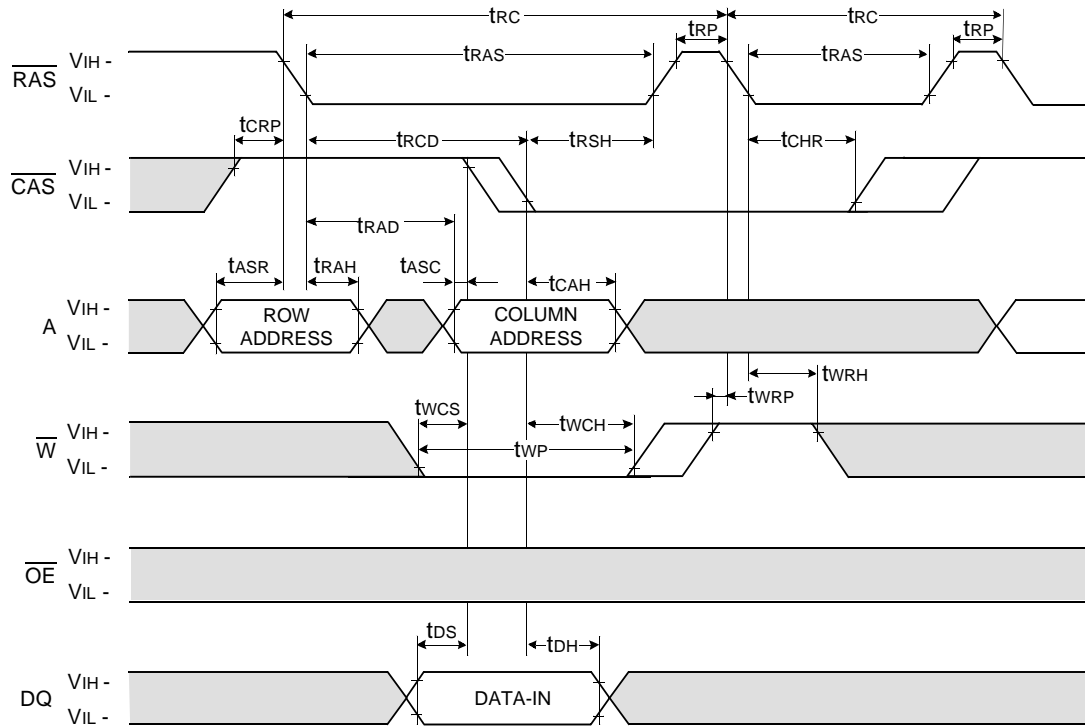
HIDDEN REFRESH CYCLE (READ)



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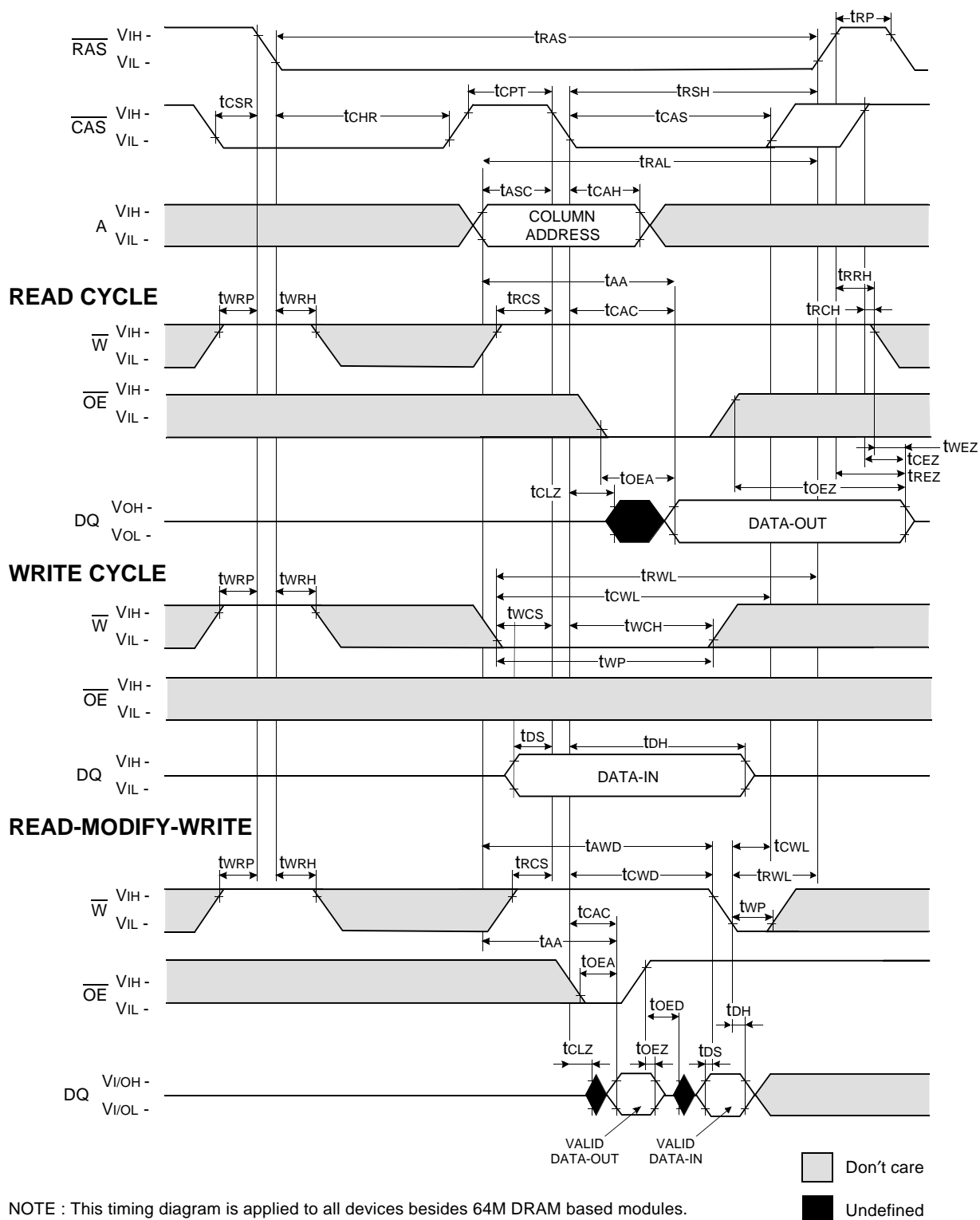
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



Don't care
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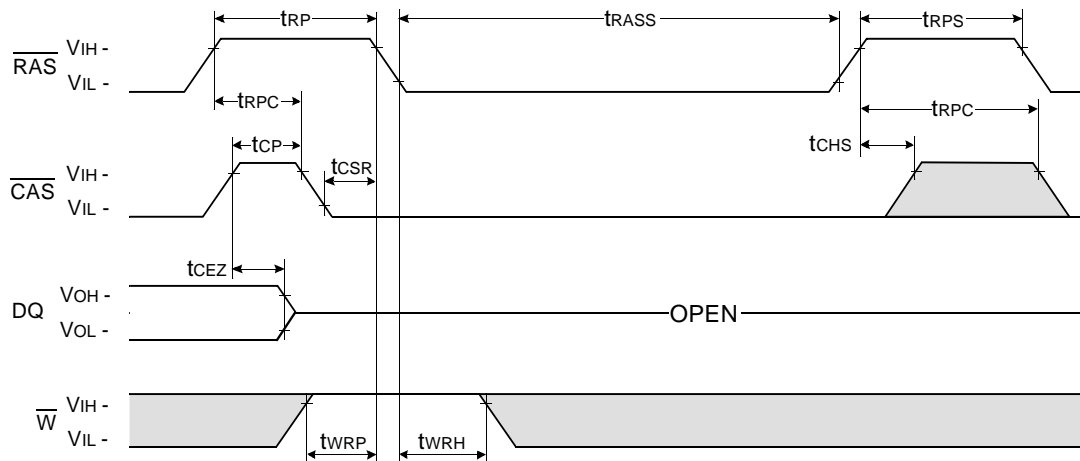
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

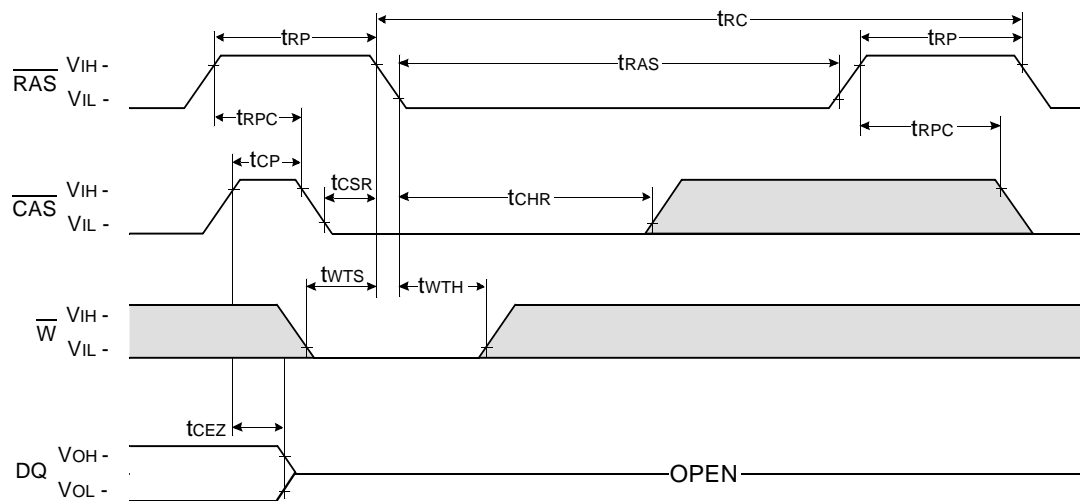
CAS - BEFORE - RAS SELF REFRESH CYCLE



NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



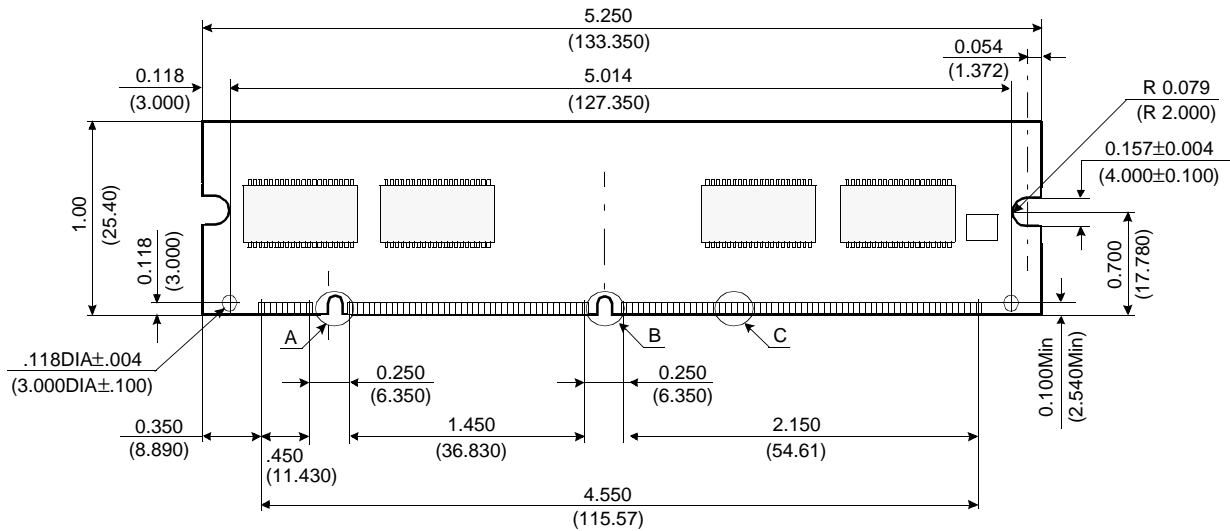
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DRAM MODULE

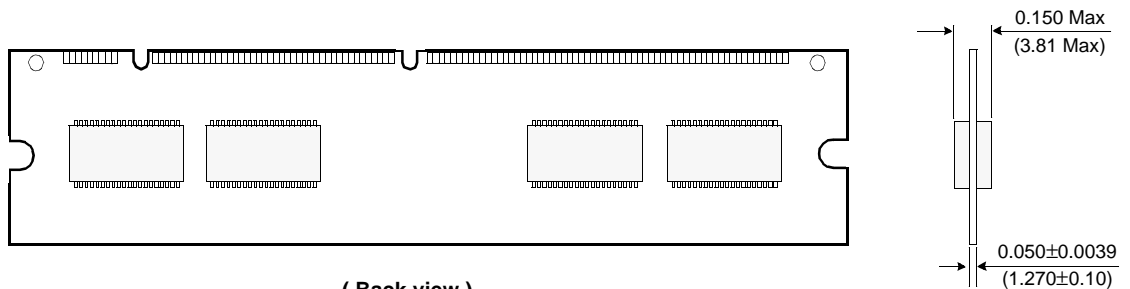
M366F080(8)4CT1-C

PACKAGE DIMENSIONS

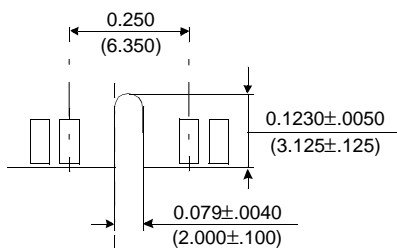
Units : Inches (millimeters)



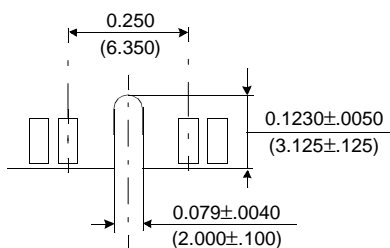
(Front view)



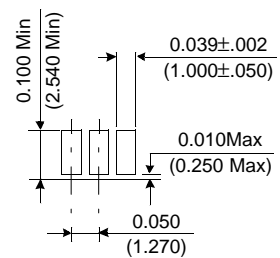
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOP II

DRAM Part No. : M366F0884CT1 - K4E661612C
M366F0804CT1 - K4E641612C