

# Buffered 32Mx72 DIMM

(16Mx4 base)

Revision 0.0

Jan. 2000

## Revision History

### Version 0.0 (Jan. 2000)

- The 4th generation of 64M DRAM components are applied to this module.

# DRAM MODULE

# M372F320(8)0CT1-C

## M372F320(8)0CT1-C EDO Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

### GENERAL DESCRIPTION

The Samsung M372F320(8)0CT1-C is a 32Mx72bits Dynamic RAM high density memory module. The Samsung M372F320(8)0CT1-C consists of thirty-six CMOS 16Mx4bits DRAMs in TSOP 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M372F320(8)0CT1-C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

### PERFORMANCE RANGE

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>HPC</sub>
-C50	50ns	18ns	84ns	20ns
-C60	60ns	20ns	104ns	25ns

### FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
M372F3200CT1-C	TSOP	4K	4K/64ms	
M372F3280CT1-C	TSOP	8K	4K/64ms	8K/64ms

- Extended Data Out Mode Operation
- CAS-before-RAS Refresh capability
- RAS-only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except  $\overline{\text{RAS}}$  and DQ
- PCB : Height(2100mil), double sided component

### PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*CAS2	57	DQ22	85	Vss	113	*CAS3	141	DQ58
2	DQ0	30	RAS0	58	DQ23	86	DQ36	114	RAS1	142	DQ59
3	DQ1	31	OE0	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	OE2	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	RAS2	73	Vcc	101	DQ49	129	RAS3	157	Vcc
18	Vcc	46	CAS4	74	DQ32	102	Vcc	130	CAS5	158	DQ68
19	DQ14	47	*CAS6	75	DQ33	103	DQ50	131	*CAS7	159	DQ69
20	DQ15	48	W2	76	DQ34	104	DQ51	132	PDE	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	W0	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	CAS0	56	DQ21	84	Vcc	112	CAS1	140	DQ57	168	Vcc

NOTE : A12 is used for only M372F3280CT1-C (8K Ref.)

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.  
ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

### PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
W0, W2	Read/Write Enable
OE0, OE2	Output Enable
RAS0 - RAS3	Row Address Strobe
CAS0, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
PDE	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked "\*" are not used in this module.

### PD & ID Table

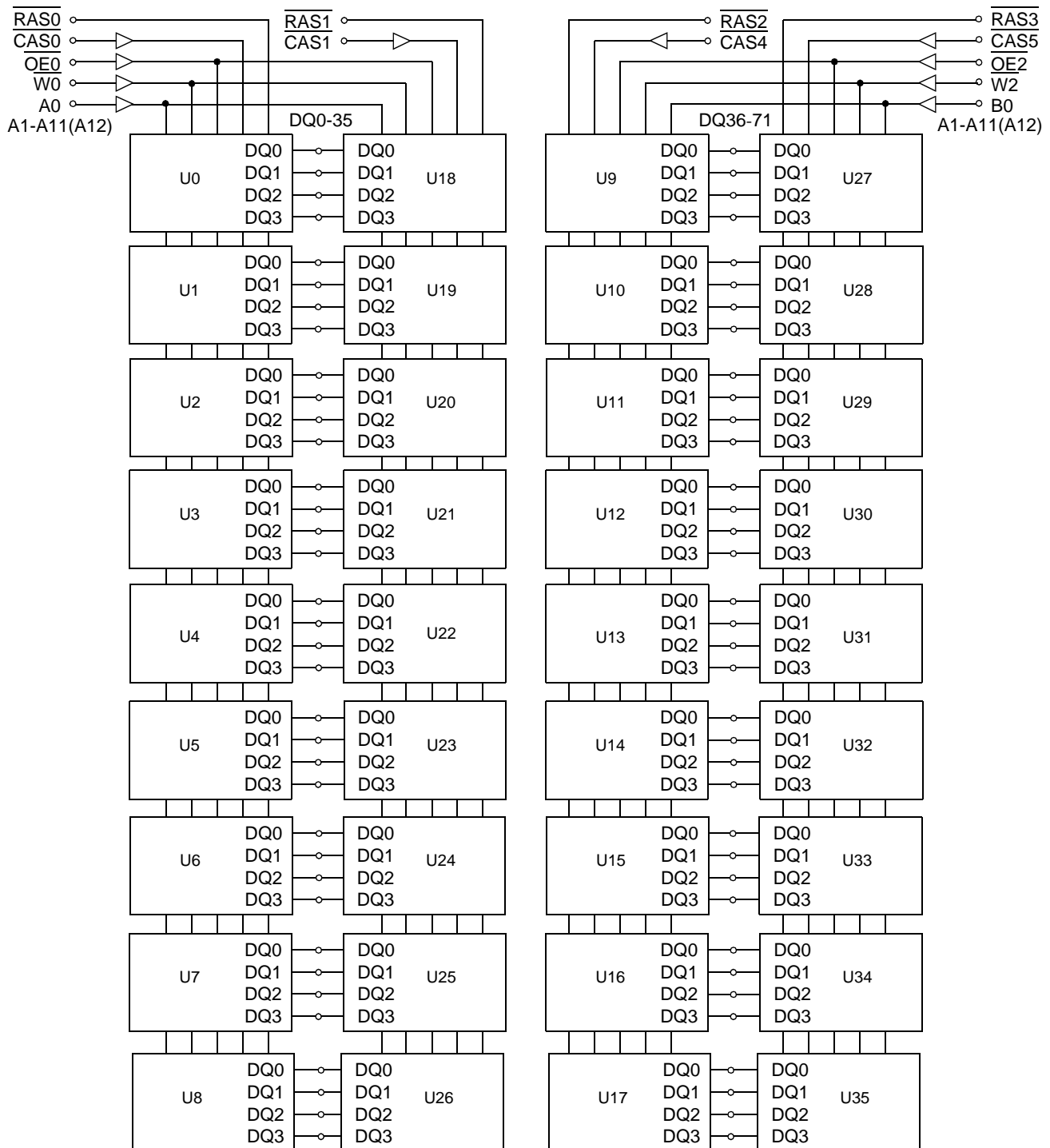
Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C  
ID : 0 for Vss & 1 for N.C

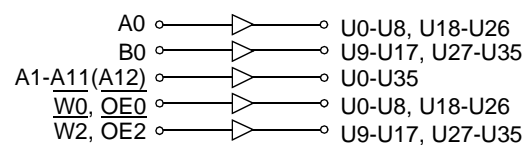
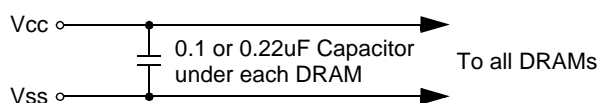
# DRAM MODULE

# M372F320(8)0CT1-C

## FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only M372F3280CT1 (8K Ref.)



## ABSOLUTE MAXIMUM RATINGS \*

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to +4.6	V
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C
Power Dissipation	P <sub>D</sub>	36	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3 <sup>*1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-0.3 <sup>*2</sup>	-	0.8	V

\*1 : V<sub>CC</sub>+1.3V at pulse width≤15ns, which is measured at V<sub>CC</sub>.

\*2 : -1.3V at pulse width≤15ns, which is measured at V<sub>SS</sub>.

## DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M372F3200CT1		M372F3280CT1		Unit
		Min	Max	Min	Max	
I <sub>CC1</sub>	-50	-	1998	-	1458	mA
	-60	-	1818	-	1278	mA
I <sub>CC2</sub>	Don't care	-	100	-	100	mA
I <sub>CC3</sub>	-50	-	1998	-	1458	mA
	-60	-	1818	-	1278	mA
I <sub>CC4</sub>	-50	-	1638	-	1638	mA
	-60	-	1458	-	1458	mA
I <sub>CC5</sub>	Don't care	-	30	-	30	mA
I <sub>CC6</sub>	-50	-	1998	-	1998	mA
	-60	-	1818	-	1818	mA
I <sub>I(L)</sub>	Don't care	-10	10	-10	10	uA
I <sub>O(L)</sub>		-10	10	-10	10	uA
V <sub>OH</sub>	Don't care	2.4	-	2.4	-	V
V <sub>OL</sub>		-	0.4	-	0.4	V

I<sub>CC1</sub>\*: Operating Current \* ( $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , Address cycling @trc=min)

I<sub>CC2</sub> : Standby Current ( $\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$ )

I<sub>CC3</sub>\*: RAS Only Refresh Current \* ( $\overline{\text{CAS}}=\text{V}_{\text{IH}}$ ,  $\overline{\text{RAS}}$  cycling @trc=min)

I<sub>CC4</sub>\*: Extended Data Out Mode Current \* ( $\overline{\text{RAS}}=\text{V}_{\text{IL}}$ ,  $\overline{\text{CAS}}$  cycling : tHPC=min)

I<sub>CC5</sub> : Standby Current ( $\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$ )

I<sub>CC6</sub>\*:  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh Current \* ( $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  cycling @trc=min)

I<sub>I(L)</sub> : Input Leakage Current (Any input  $0\leq\text{V}_{\text{IN}}\leq\text{V}_{\text{CC}}+0.3\text{V}$ , all other pins not under test=0 V)

I<sub>O(L)</sub> : Output Leakage Current(Data Out is disabled,  $0\text{V}\leq\text{V}_{\text{OUT}}\leq\text{V}_{\text{CC}}$ )

V<sub>OH</sub> : Output High Voltage Level (I<sub>OH</sub> = -2mA)

V<sub>OL</sub> : Output Low Voltage Level (I<sub>OL</sub> = 2mA)

\* **NOTE** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while  $\overline{\text{RAS}}=\text{V}_{\text{IL}}$ . In I<sub>CC4</sub>, address can be changed maximum once within one EDO mode cycle time, tHPC.

# DRAM MODULE

# M372F320(8)0CT1-C

## CAPACITANCE (T<sub>A</sub> = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C <sub>IN1</sub>	-	20	pF
Input capacitance[W0, W2, OE0, OE2]	C <sub>IN2</sub>	-	20	pF
Input capacitance[RAS0 - RAS3]	C <sub>IN3</sub>	-	73	pF
Input capacitance[CAS0, 1,4,5]	C <sub>IN4</sub>	-	20	pF
Input/Output capacitance[DQ0 - 71]	C <sub>DQ</sub>	-	24	pF

## AC CHARACTERISTICS (0°C≤T<sub>A</sub>≤70°C, V<sub>CC</sub>=3.3V±0.3V. See notes 1,2.)

Test condition : V<sub>ih</sub>/V<sub>il</sub>=2.2/0.7V, V<sub>oh</sub>/V<sub>ol</sub>=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	84		104		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	128		153		ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>		18		20	ns	3,4,5,13
Access time from column address	t <sub>AA</sub>		30		35	ns	3,10,13
$\overline{\text{CAS}}$ to output in Low-Z	t <sub>CLZ</sub>	8		8		ns	3,13
$\overline{\text{OE}}$ to output in Low-Z	t <sub>OLZ</sub>	8		8		ns	3,13
Output buffer turn-off delay from $\overline{\text{CAS}}$	t <sub>CEZ</sub>	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t <sub>T</sub>	1	50	1	50	ns	2
RAS precharge time	t <sub>RP</sub>	30		40		ns	
RAS pulse width	t <sub>RAS</sub>	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	13		15		ns	13
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	36		38		ns	13
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	8	10K	10	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RCD</sub>	15	32	18	40	ns	4,13
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	10	20	13	25	ns	10,13
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	10		10		ns	13
Row address set-up time	t <sub>ASR</sub>	5		5		ns	13
Row address hold time	t <sub>RAH</sub>	5		8		ns	13
Column address set-up time	t <sub>ASC</sub>	0		0		ns	
Column address hold time	t <sub>CAH</sub>	7		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	30		35		ns	13
Read command set-up time	t <sub>RCS</sub>	0		0		ns	
Read command hold referenced to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0		0		ns	8
Read command hold referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	-2		-2		ns	8,13
Write command set-up time	t <sub>WCS</sub>	0		0		ns	7
Write command hold time	t <sub>WCH</sub>	7		10		ns	
Write command pulse width	t <sub>WP</sub>	7		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t <sub>RWL</sub>	13		15		ns	13
Write command to $\overline{\text{CAS}}$ lead time	t <sub>CWL</sub>	7		10		ns	
Data set-up time	t <sub>DS</sub>	-2		-2		ns	9,13
Data hold time	t <sub>DH</sub>	13		15		ns	9,13
Refresh period(4K & 8K)	t <sub>REF</sub>		64		64	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t <sub>CWD</sub>	33		38		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t <sub>RWD</sub>	68		82		ns	7,13

## AC CHARACTERISTICS (0°C≤T<sub>A</sub>≤70°C, V<sub>CC</sub>=3.3V±0.3V. See notes 1,2.)

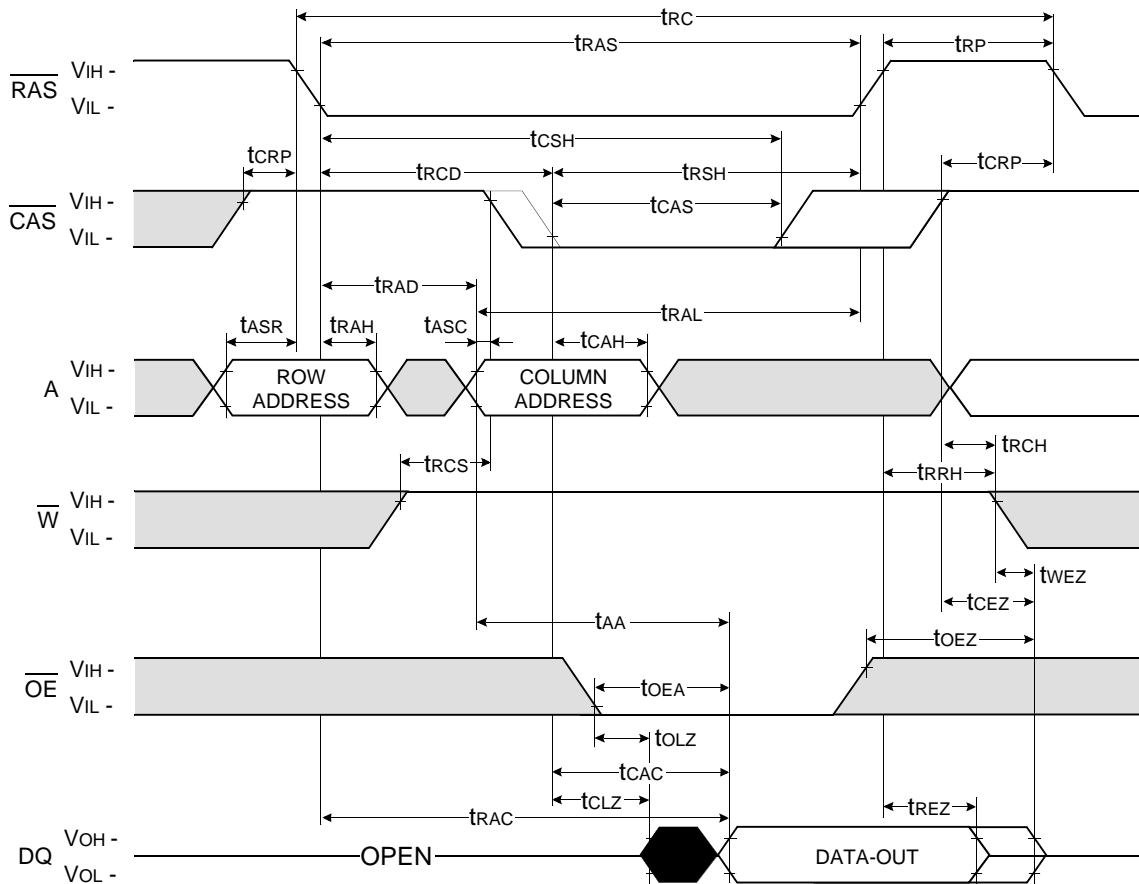
Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t <sub>AWD</sub>	45		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t <sub>CPWD</sub>	47		58		ns	
$\overline{CAS}$ setup time(CAS-before-RAS refresh)	t <sub>CSR</sub>	10		10		ns	13
$\overline{CAS}$ hold time(CAS-before-RAS refresh)	t <sub>CHR</sub>	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t <sub>RPC</sub>	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t <sub>CPA</sub>		33		40	ns	3,13
Hyper page cycle time	t <sub>HPC</sub>	20		25		ns	12
Hyper page read-modify-write cycle time	t <sub>HPRWC</sub>	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t <sub>CP</sub>	7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t <sub>RASP</sub>	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t <sub>RHCP</sub>	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t <sub>WRP</sub>	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t <sub>WRH</sub>	8		8		ns	13
$\overline{OE}$ access time	t <sub>OEa</sub>		18		20	ns	13
$\overline{OE}$ to data delay	t <sub>OED</sub>	15		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t <sub>OEZ</sub>	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t <sub>OEh</sub>	5		5		ns	
Output data hold time( $\overline{C}$ -B- $\overline{R}$ refresh)	t <sub>DOH</sub>	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t <sub>REZ</sub>	3	13	3	13	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t <sub>WEZ</sub>	8	18	8	18	ns	6,13
$\overline{W}$ to data delay	t <sub>WED</sub>	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t <sub>OCH</sub>	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t <sub>CHO</sub>	5		5		ns	
$\overline{OE}$ precharge time	t <sub>OEP</sub>	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t <sub>WPE</sub>	5		5		ns	
<b>Present Detect Read Cycle</b>							
PDE to Valid PD bit	t <sub>PD</sub>		10		10	ns	
PDE to PD bit Inactive	t <sub>PDOFF</sub>	2	7	2	7	ns	

## NOTES

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are  $V_{ih}/V_{il}$ .  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\min)$  and  $V_{IL}(\max)$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the  $t_{RCD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RCD} \geq t_{RCD}(\max)$ .
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
7.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\min)$  the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If  $t_{RWD} \geq t_{RWD}(\min)$ ,  $t_{CWD} \geq t_{CWD}(\min)$ ,  $t_{AWD} \geq t_{AWD}(\min)$  and  $t_{CPWD} \geq t_{CPWD}(\min)$ . The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
8. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
9. These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles.
10. Operation within the  $t_{RAD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then access time is controlled by  $t_{AA}$ .
11. If  $\overline{RAS}$  goes high before  $\overline{CAS}$  high going, the open circuit condition of the output is achieved by  $\overline{CAS}$  high going. If  $\overline{CAS}$  goes high before  $\overline{RAS}$  high going, the open circuit condition of the output is achieved by  $\overline{RAS}$  going.
12.  $t_{ASC} \geq 6ns$ .
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.



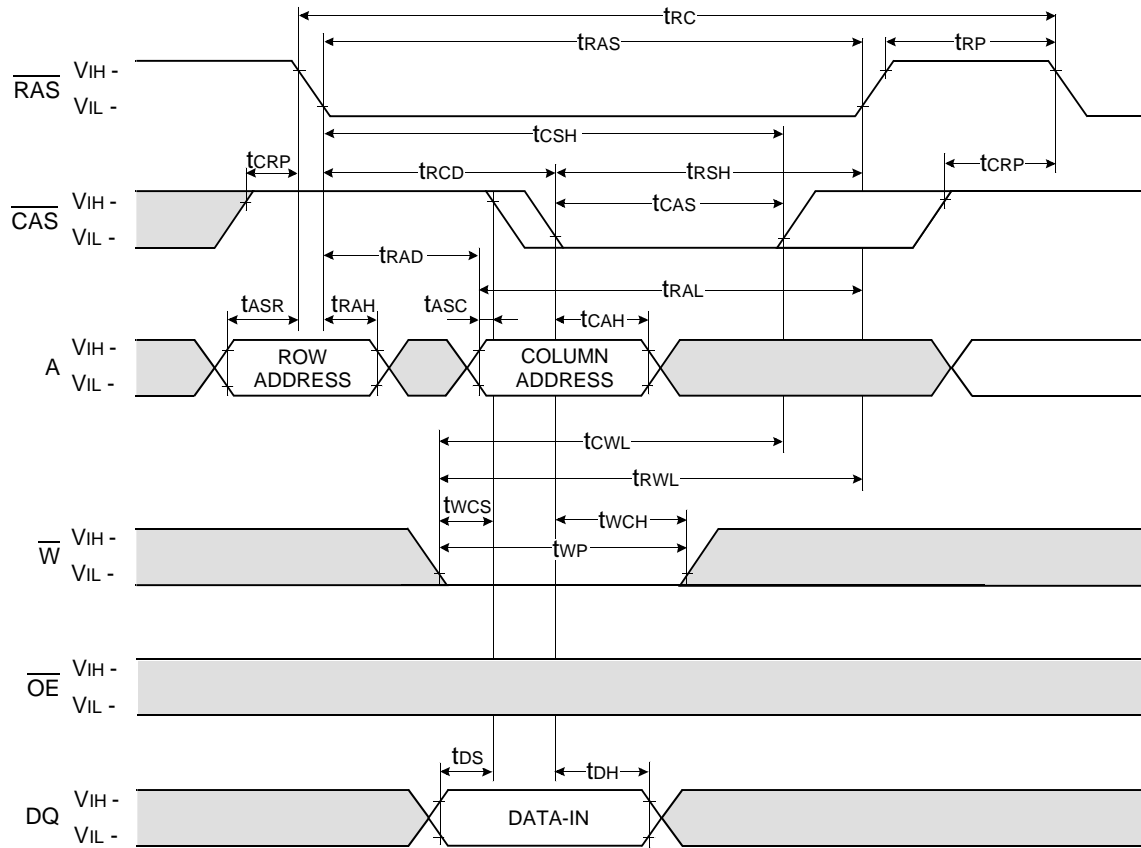
READ CYCLE



Don't care  
Undefined

WRITE CYCLE ( EARLY WRITE )

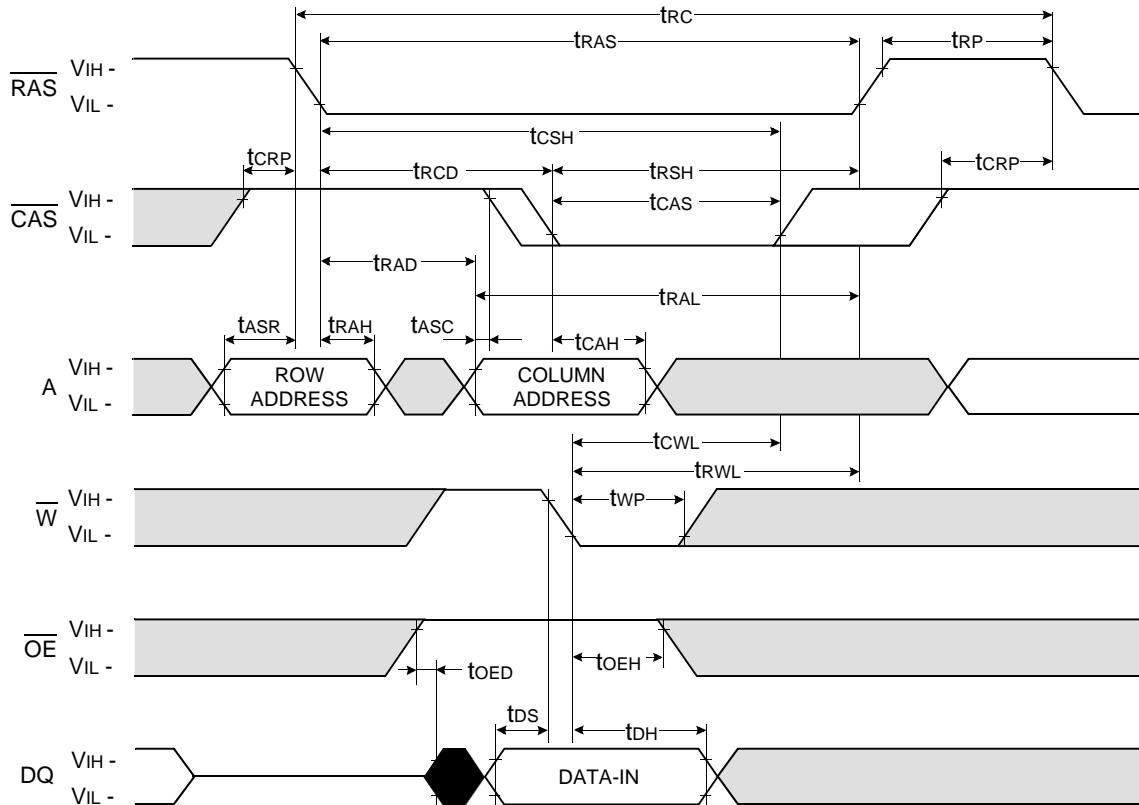
NOTE : DOUT = OPEN



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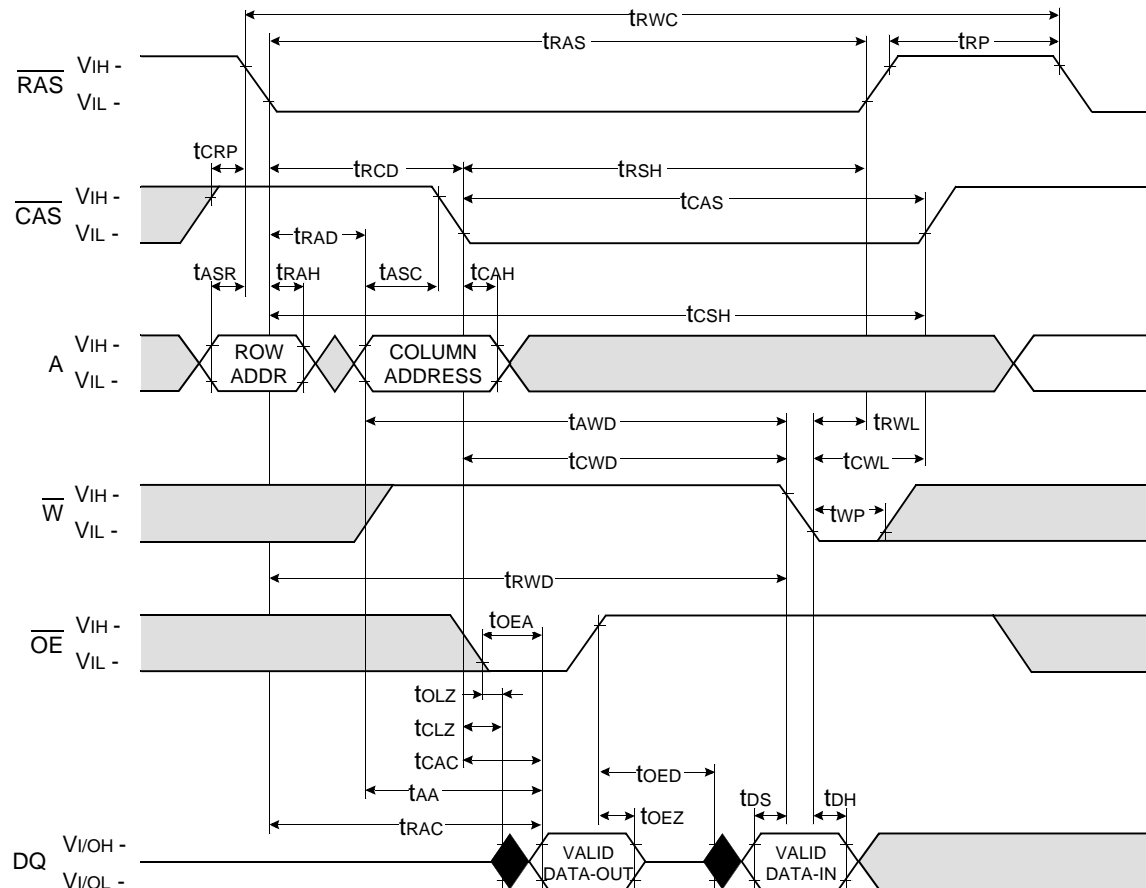
## WRITE CYCLE ( $\overline{\text{OE}}$ CONTROLLED WRITE )

NOTE : DOUT = OPEN



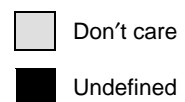
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READ - MODIFY - WRITE CYCLE



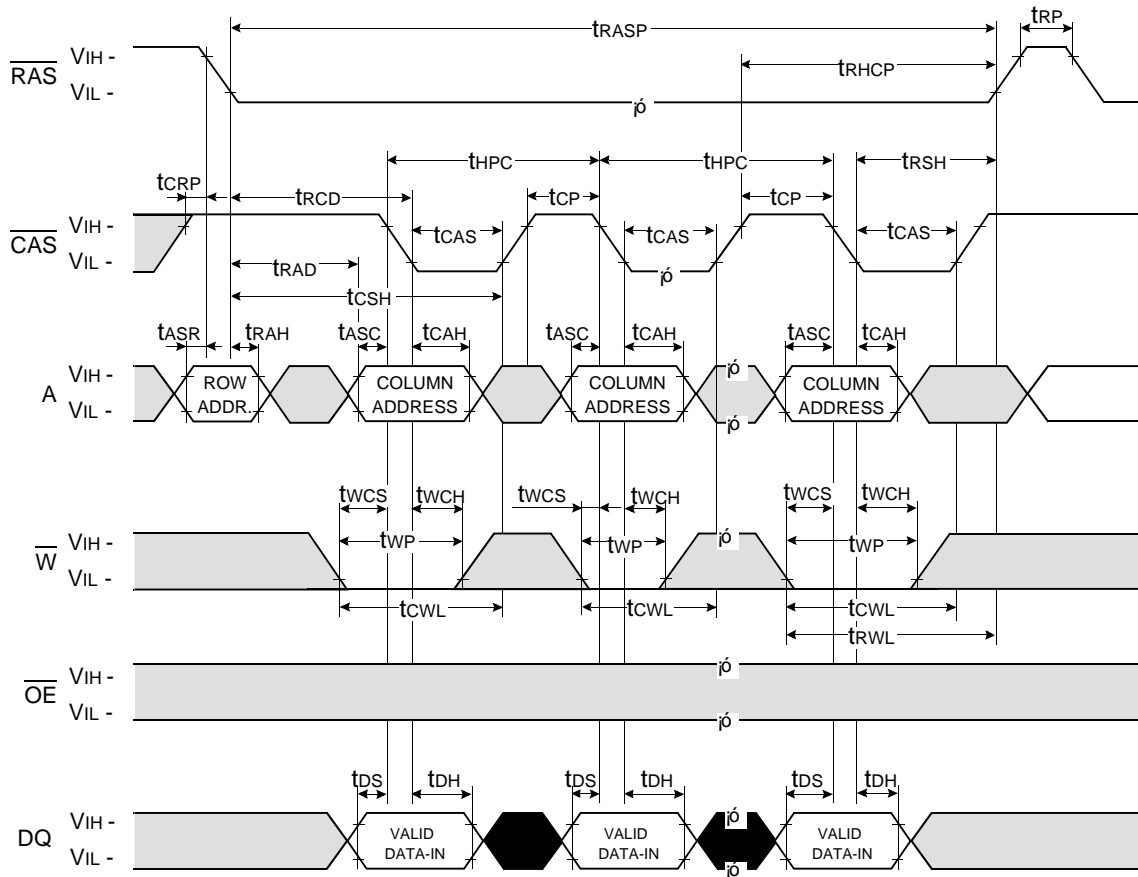
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## HYPER PAGE READ CYCLE



# HYPER PAGE WRITE CYCLE ( EARLY WRITE )

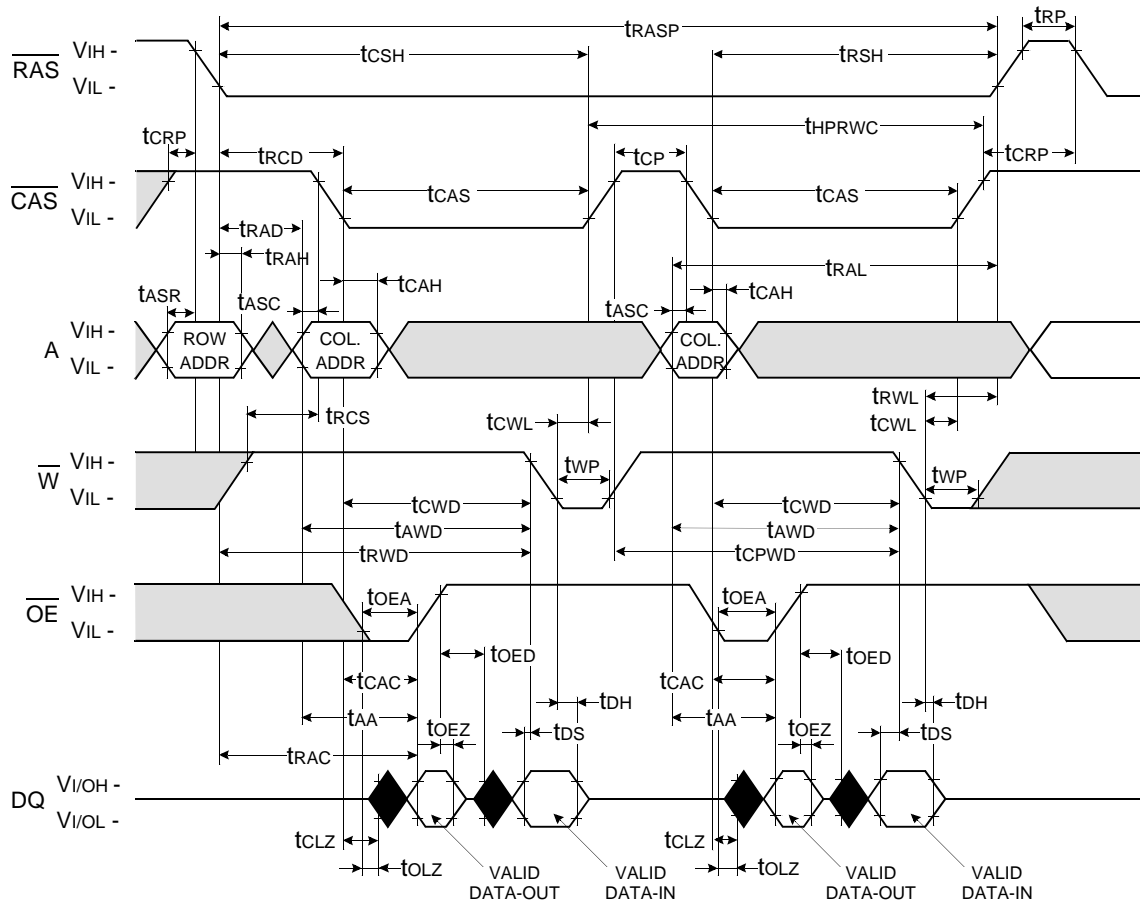
NOTE : DOUT = OPEN



Don't care

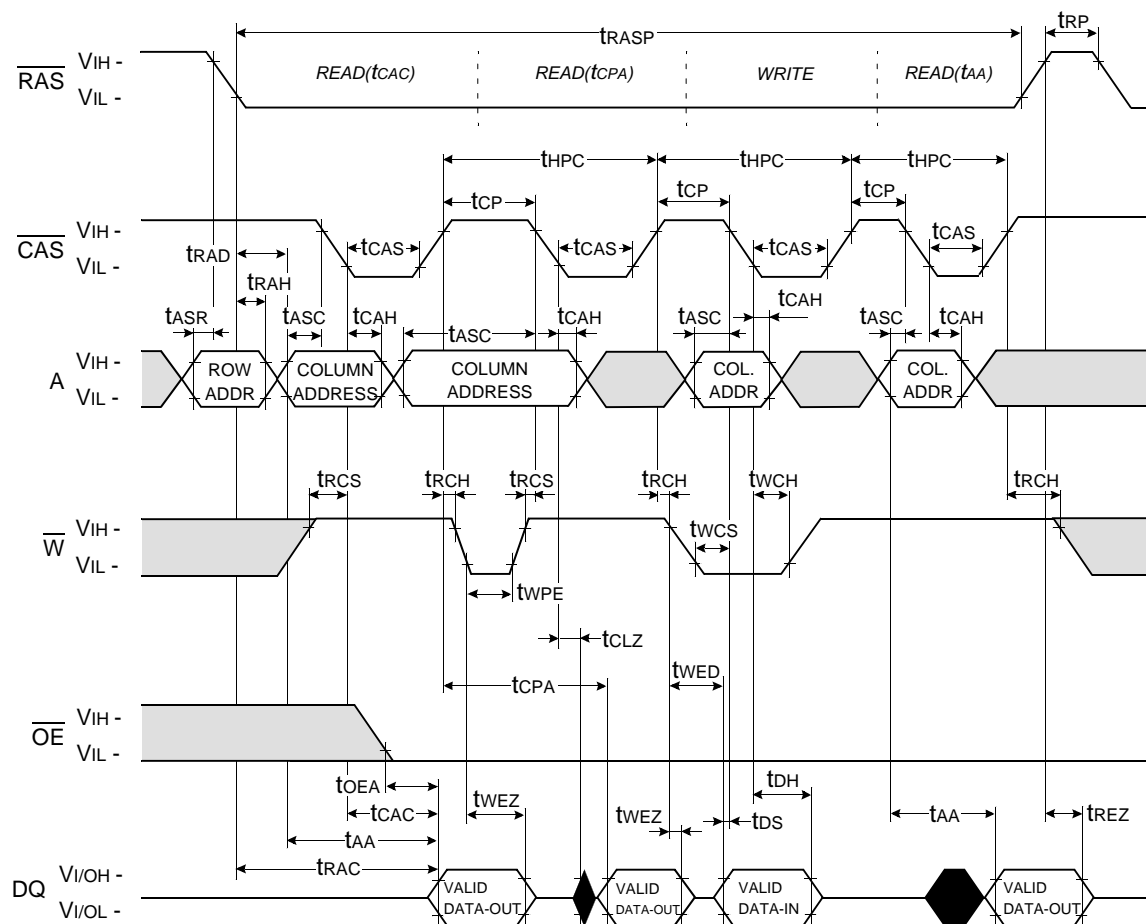
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HYPER PAGE READ-MODIFY-WRITE CYCLE




Don't care  
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## HYPER PAGE READ AND WRITE MIXED CYCLE



 Don't care

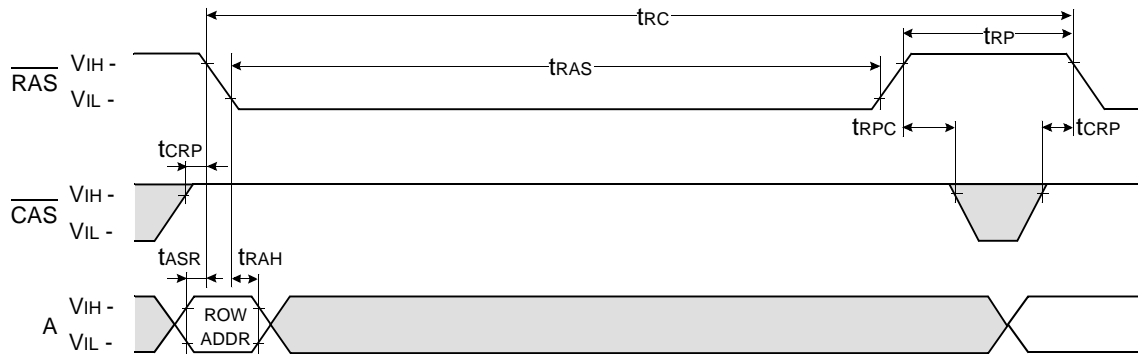
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## **RAS - ONLY REFRESH CYCLE\***

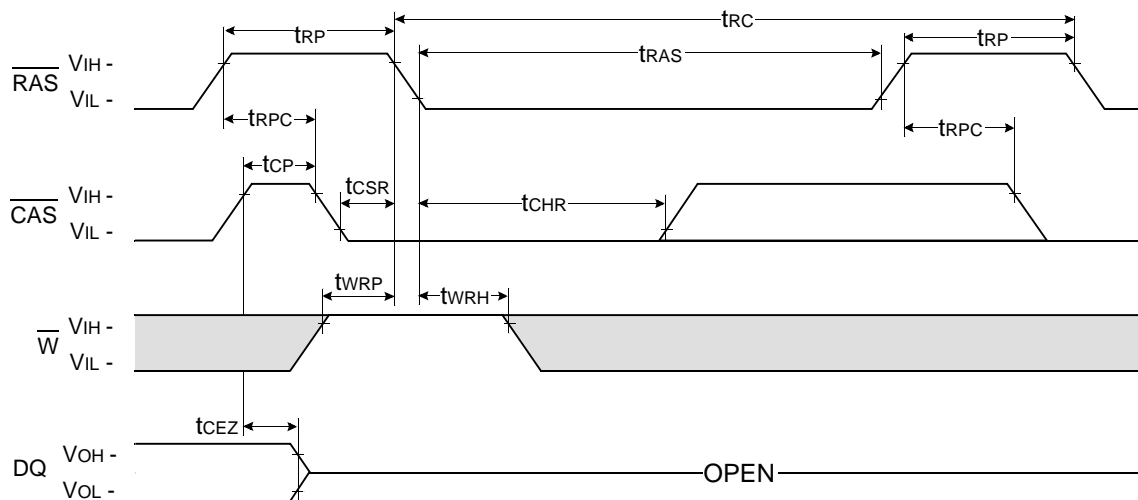
NOTE :  $\overline{W}$ ,  $\overline{OE}$ , DIN = Don't care

DOUT = OPEN



## **CAS - BEFORE - RAS REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care

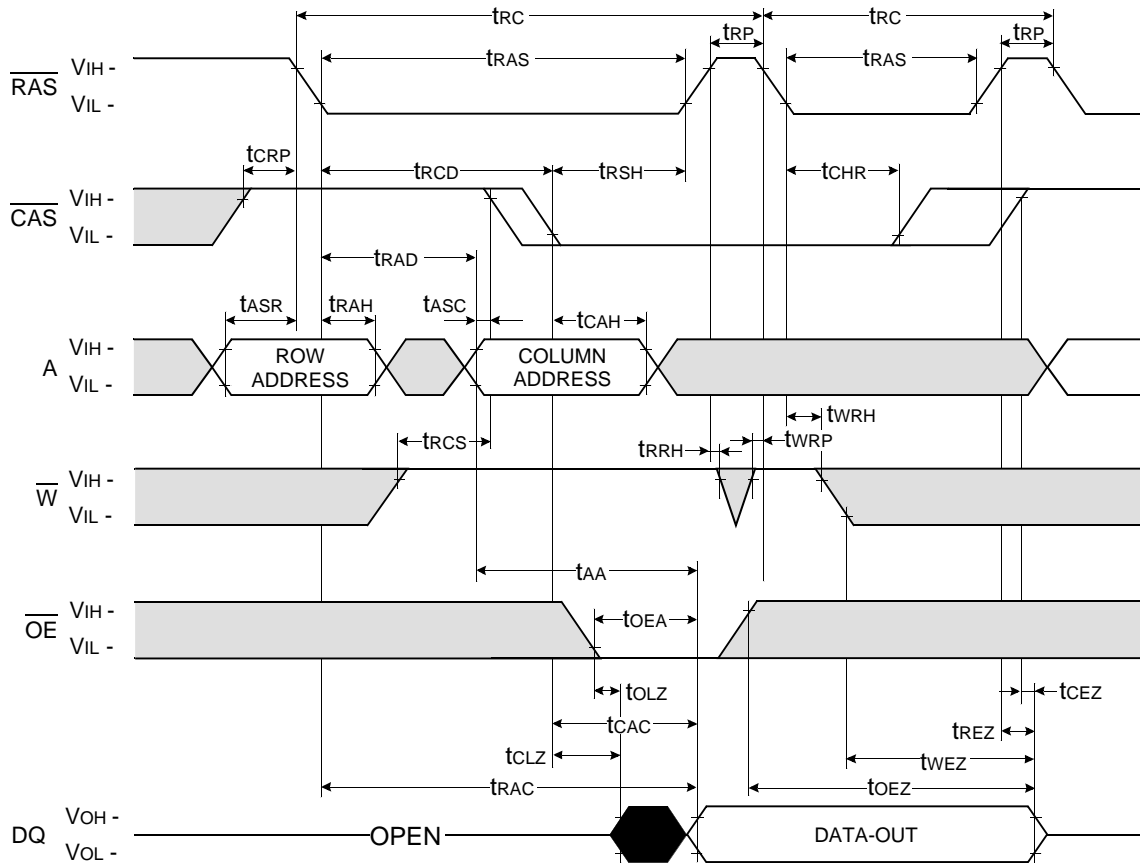


Don't care

Undefined

\* In RAS-only refresh cycle of 64Mb A-die & B-die, when  $\overline{CAS}$  signal transits from Low to High, the valid data may be cut off.

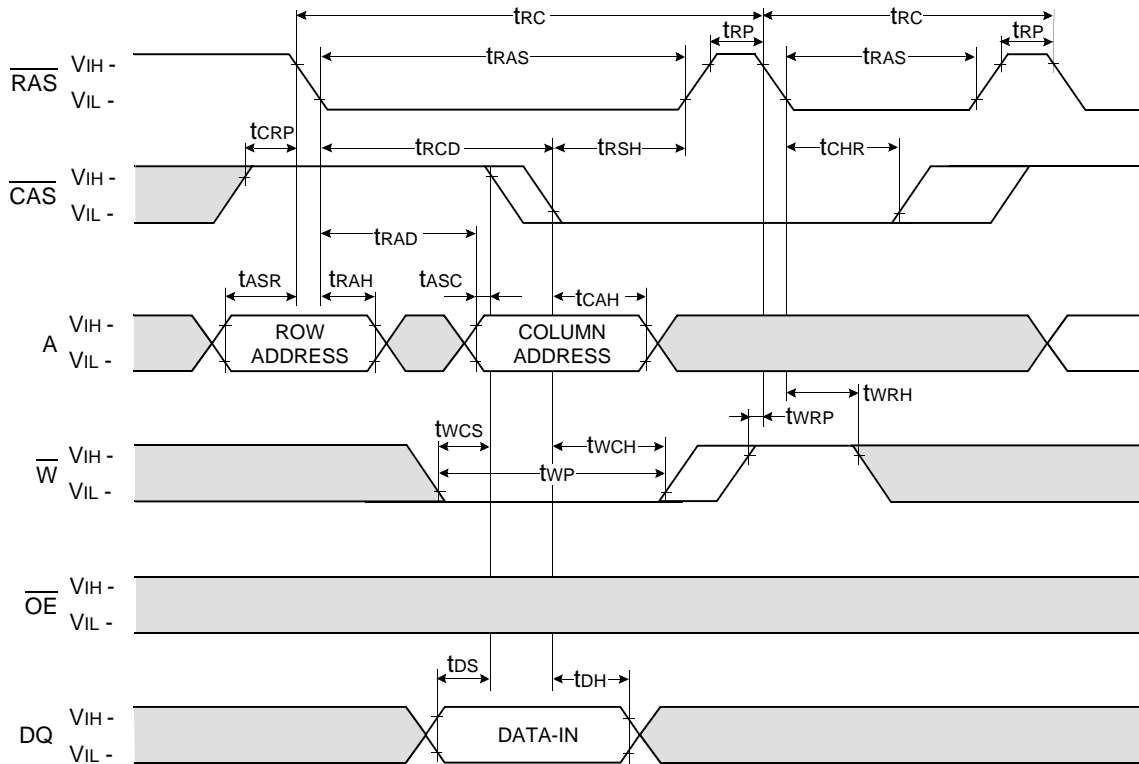
HIDDEN REFRESH CYCLE ( READ )





Don't care  
Undefined

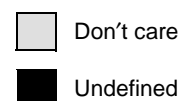
## HIDDEN REFRESH CYCLE ( WRITE )

NOTE : DOUT = OPEN



 Don't care  
 Undefined

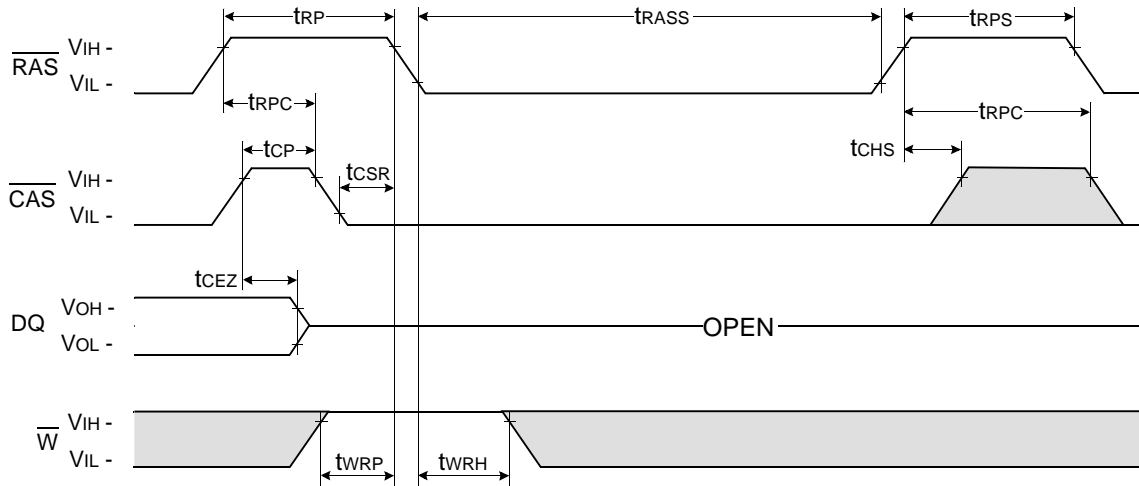
## READ CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

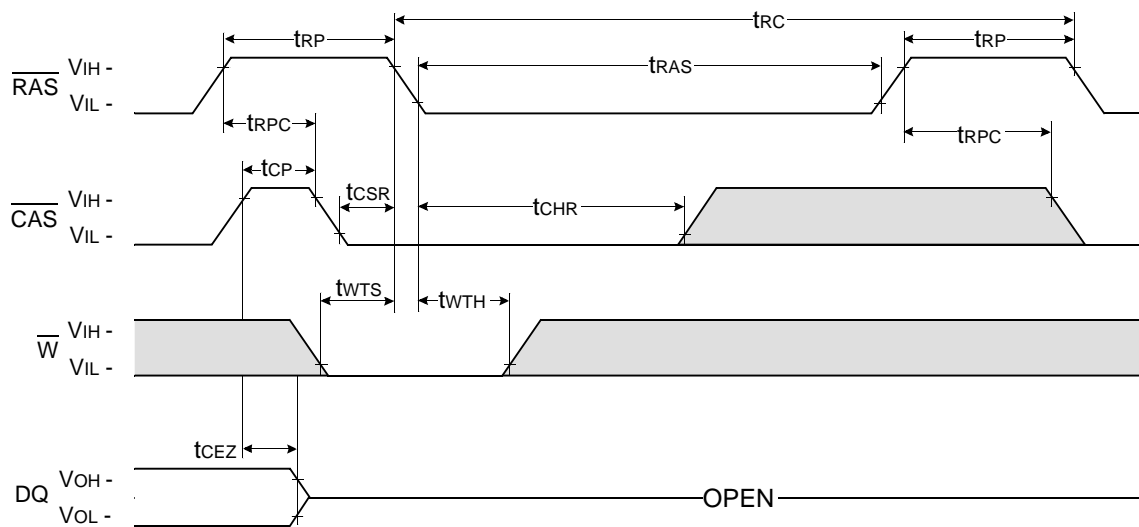
## CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE :  $\overline{OE}$ , A = Don't care



## TEST MODE IN CYCLE

NOTE :  $\overline{OE}$ , A = Don't care



Don't care

Undefined

**M372F320(8)0CT1-C**

## Units : Inches (millimeters)



The used device is 16Mx4 DRAM with EDO mode, TSOP II.  
DRAM Part No. : M372F3200CT1 - K4E640412C-T.  
M372F3280CT1 - K4E660412C-T.