

Buffered 32Mx72 DIMM

(16Mx4 base)

Revision 0.0

Jan. 1999

Revision History

Version 0.0 (Jan. 1999)

- The 4th. generation of 64M DRAM components are applied to this module.

DRAM MODULE

M372V320(8)0CT1-C

M372V320(8)0CT1-C Fast Page Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung M372V320(8)0CT1-C is a 32Mx72bits Dynamic RAM high density memory module. The Samsung M372V320(8)0CT1-C consists of thirty-six CMOS 16Mx4bits DRAMs in TSOP 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M372V320(8)0CT1-C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tPC
-C50	50ns	18ns	90ns	35ns
-C60	60ns	20ns	110ns	40ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
M372V3200CT1-C	TSOP	4K	4K/64ms	
M372V3280CT1-C	TSOP	8K	4K/64ms	8K/64ms

- Fast Page Mode Operation
- CAS-before-RAS Refresh capability
- RAS-only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except RAS and DQ
- PCB : Height(2100mil), double sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	*CAS2	57	DQ22	85	Vss	113	*CAS3	141	DQ58
2	DQ0	30	RAS0	58	DQ23	86	DQ36	114	RAS1	142	DQ59
3	DQ1	31	OE0	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	OE2	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	RAS2	73	Vcc	101	DQ49	129	RAS3	157	Vcc
18	Vcc	46	CAS4	74	DQ32	102	Vcc	130	CAS5	158	DQ68
19	DQ14	47	*CAS6	75	DQ33	103	DQ50	131	*CAS7	159	DQ69
20	DQ15	48	W2	76	DQ34	104	DQ51	132	PDE	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	W0	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	CAS0	56	DQ21	84	Vcc	112	CAS1	140	DQ57	168	Vcc

NOTE : A12 is used for only M372V3280CT1-C (8K Ref.)

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.
ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref)
A0, B0, A1 - A12	Address Input(8K ref)
DQ0 - DQ71	Data In/Out
W0, W2	Read/Write Enable
OE0, OE2	Output Enable
RAS0 - RAS3	Row Address Strobe
CAS0, 1,4,5	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
PDE	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

PD & ID Table

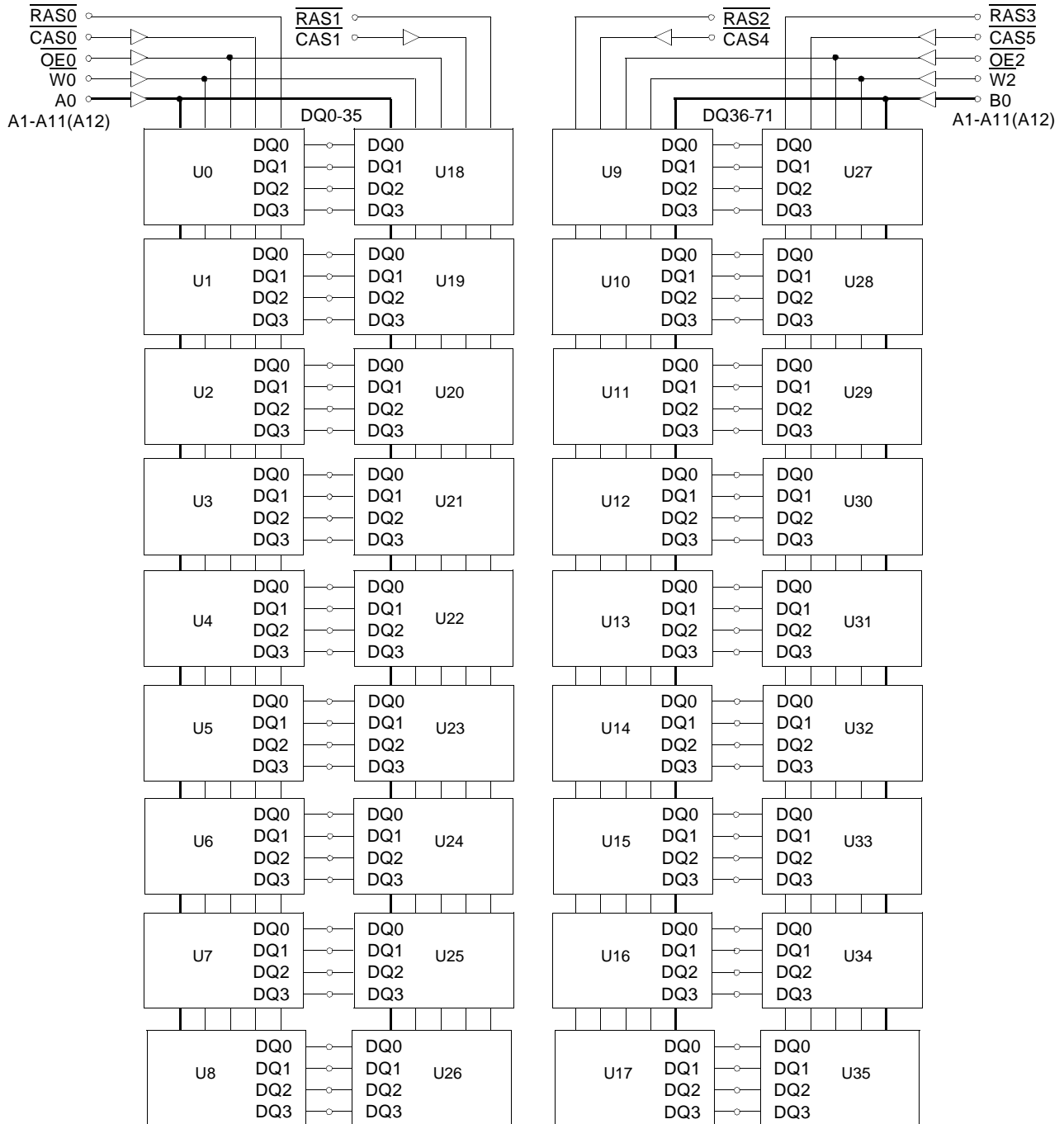
Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	0	0
PD5	0	0
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

PD : 0 for Vol of Drive IC & 1 for N.C
ID : 0 for Vss & 1 for N.C

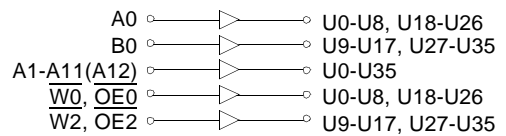
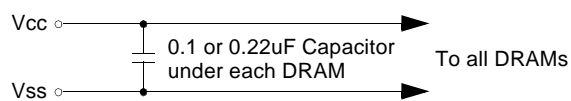
DRAM MODULE

M372V320(8)0CT1-C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only M372V3280CT1(8K Ref.)



DRAM MODULE

M372V320(8)0CT1-C

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +125	°C
Power Dissipation	Pd	36	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	Vcc+0.3 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns, which is measured at Vcc.

*2 : -1.3V at pulse width≤15ns, which is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M372V3200CT1		M372V3280CT1		Unit
		Min	Max	Min	Max	
Icc1	-50	-	1998	-	1458	mA
	-60	-	1818	-	1278	mA
Icc2	Don't care	-	100	-	100	mA
Icc3	-50	-	1998	-	1458	mA
	-60	-	1818	-	1278	mA
Icc4	-50	-	1098	-	1098	mA
	-60	-	918	-	918	mA
Icc5	Don't care	-	30	-	30	mA
Icc6	-50	-	1998	-	1998	mA
	-60	-	1818	-	1818	mA
I _{I(L)}	Don't care	-10	10	-10	10	uA
I _{O(L)}		-10	10	-10	10	uA
V _{OH}	Don't care	2.4	-	2.4	-	V
V _{OL}		-	0.4	-	0.4	V

Icc1*: Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @trc=min)

Icc2 : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

Icc3*: \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @trc=min)

Icc4*: Fast Page Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : tpc=min)

Icc5 : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{cc}-0.2V$)

Icc6*: \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{cc}+0.3V$, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, $0V \leq V_{OUT} \leq V_{cc}$)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In Icc4, address can be changed maximum once within one Fast page mode cycle time, tpc.

DRAM MODULE

M372V320(8)0CT1-C

CAPACITANCE (TA = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	CIN1	-	20	pF
Input capacitance[W0, W2, OE0, OE2]	CIN2	-	20	pF
Input capacitance[RAS0 - RAS3]	CIN3	-	73	pF
Input capacitance[CAS0, 1, 4, 5]	CIN4	-	20	pF
Input/Output capacitance[DQ0 - 71]	CDQ	-	24	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : Vin/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Read-modify-write cycle time	tRWC	133		155		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		18		20	ns	3,4,5,11
Access time from column address	tAA		30		35	ns	3,10,11
CAS to output in Low-Z	tCLZ	5		5		ns	3,11
Output buffer turn-off delay	tOFF	5	18	5	20	ns	6,11
Transition time(rise and fall)	tT	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	18		20		ns	11
$\overline{\text{CAS}}$ hold time	tCSH	48		58		ns	11
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	ns	
RAS to CAS delay time	tRCD	18	32	18	40	ns	4,11
$\overline{\text{RAS}}$ to column address delay time	tRAD	13	20	13	25	ns	10,11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	10		10		ns	11
Row address set-up time	tASR	5		5		ns	11
Row address hold time	tRAH	8		8		ns	11
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		ns	11
Read command set-up time	tRCS	0		0		ns	
Read command hold referencde to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold referenced to $\overline{\text{RAS}}$	tRRH	-2		-2		ns	8,11
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	20		20		ns	11
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		ns	
Data in set-up time	tDS	-2		-2		ns	9,11
Data in hold time	tDH	15		15		ns	9,11
Refresh period(4K & 8K)	tREF		64		64	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		ns	7
$\overline{\text{CAS}}$ prechange to $\overline{\text{W}}$ delay time	tCPWD	53		60		ns	7
$\overline{\text{RAS}}$ ro $\overline{\text{W}}$ delay time	tRWD	71		83		ns	7,11

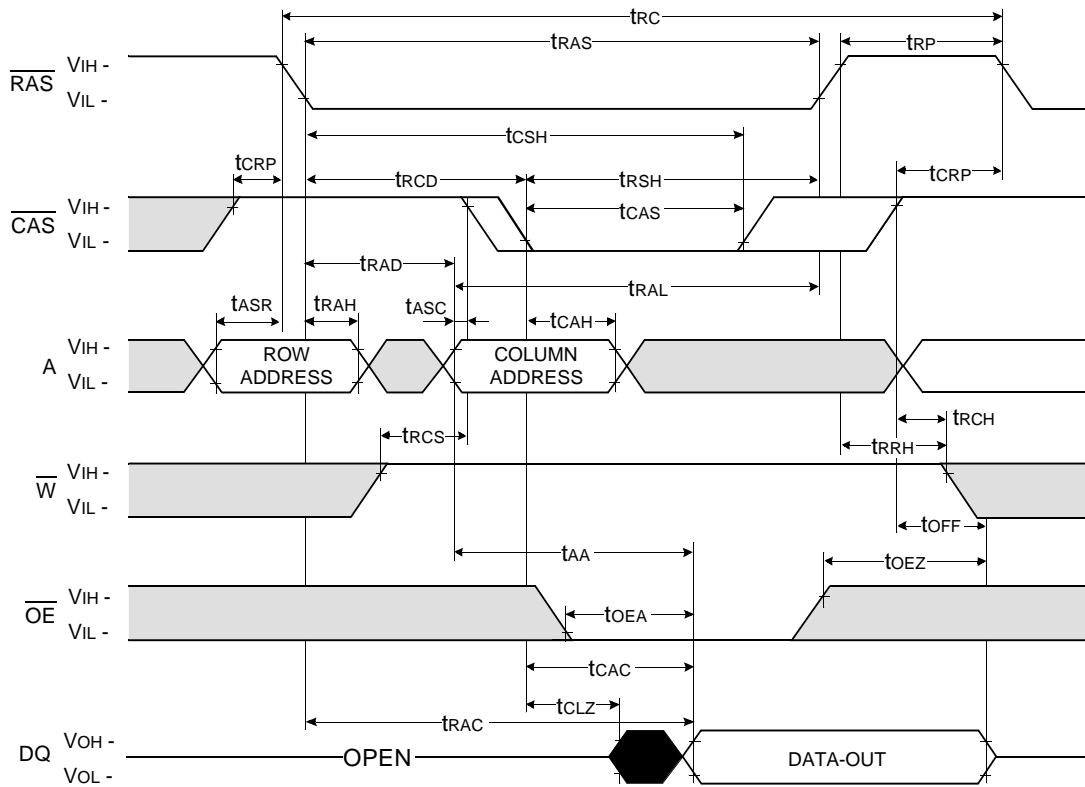
AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
CAS setup time(CAS-before-RAS refresh)	tCSR	10		10		ns	11
CAS hold time(CAS-before-RAS refresh)	tCHR	8		8		ns	11
RAS to CAS precharge time	trPC	3		3		ns	11
Access time from CAS precharge	tCPA		35		40	ns	3,11
Fast page mode cycle time	tpc	35		40		ns	
Fast page mode read-modify-write cycle time	tpRWC	76		85		ns	
CAS precharge time(Fast page cycle)	tCP	10		10		ns	
RAS pulse width(Fast page cycle)	trASP	50	200K	60	200K	ns	
RAS hold time from CAS precharge	trHCP	35		40		ns	11
W to RAS precharge time(C-B-R refresh)	tWRP	15		15		ns	11
W to RAS hold time(C-B-R refresh)	tWRH	8		8		ns	11
OE access time	toEA		18		20	ns	11
OE to data delay	toED	18		20		ns	11
Output buffer turn off delay time from OE	toEZ	5	18	5	20	ns	11
OE command hold time	toEH	13		15		ns	
Present Detect Read Cycle							
PDE to Valid PD bit	tpD		10		10	ns	
PDE to PD bit Inactive	tpDOFF	2	7	2	7	ns	

NOTES

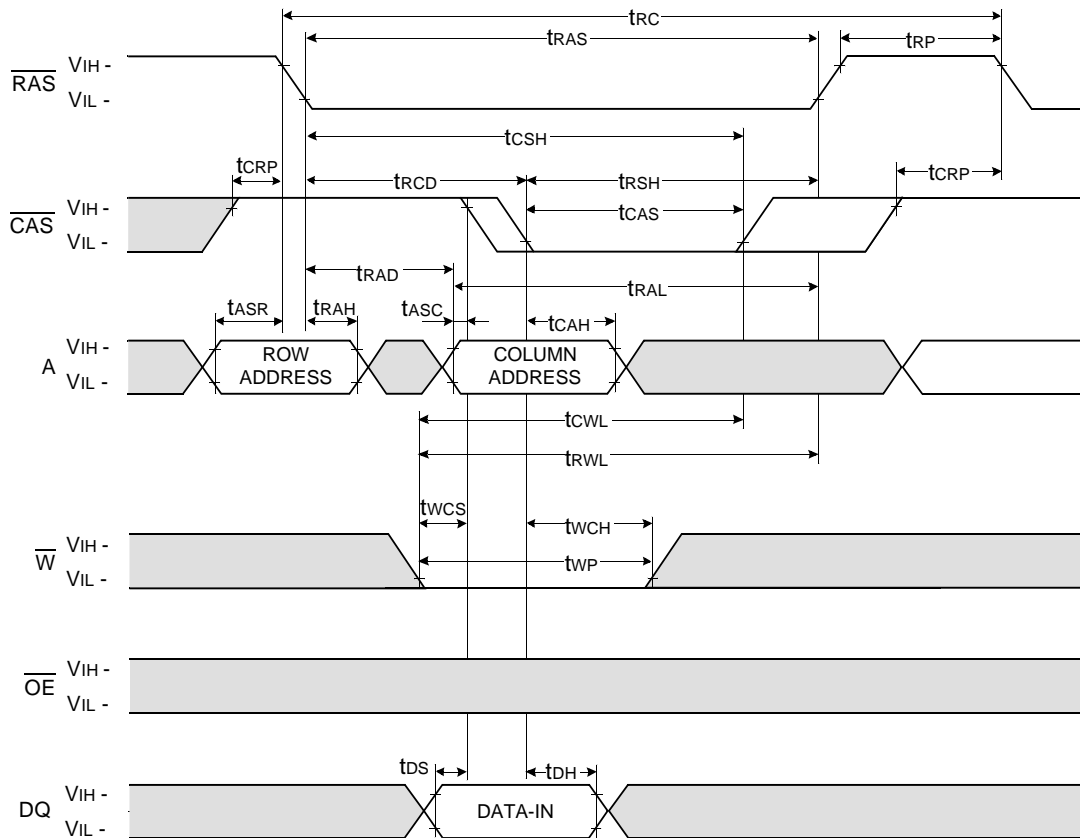
1. An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the trCD(max) limit insures that tRAC(max) can be met. trCD(max) is specified as a reference point only. If trCD is greater than the specified trCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes tha trCD≥trCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. twCS, trWD, tcWD, tAWD and tCPWD are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If twCS≥twCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If trWD≥trWD(min), tcWD≥tcWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
8. Either trCH or trRH must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

READ CYCLE



WRITE CYCLE (EARLY WRITE)

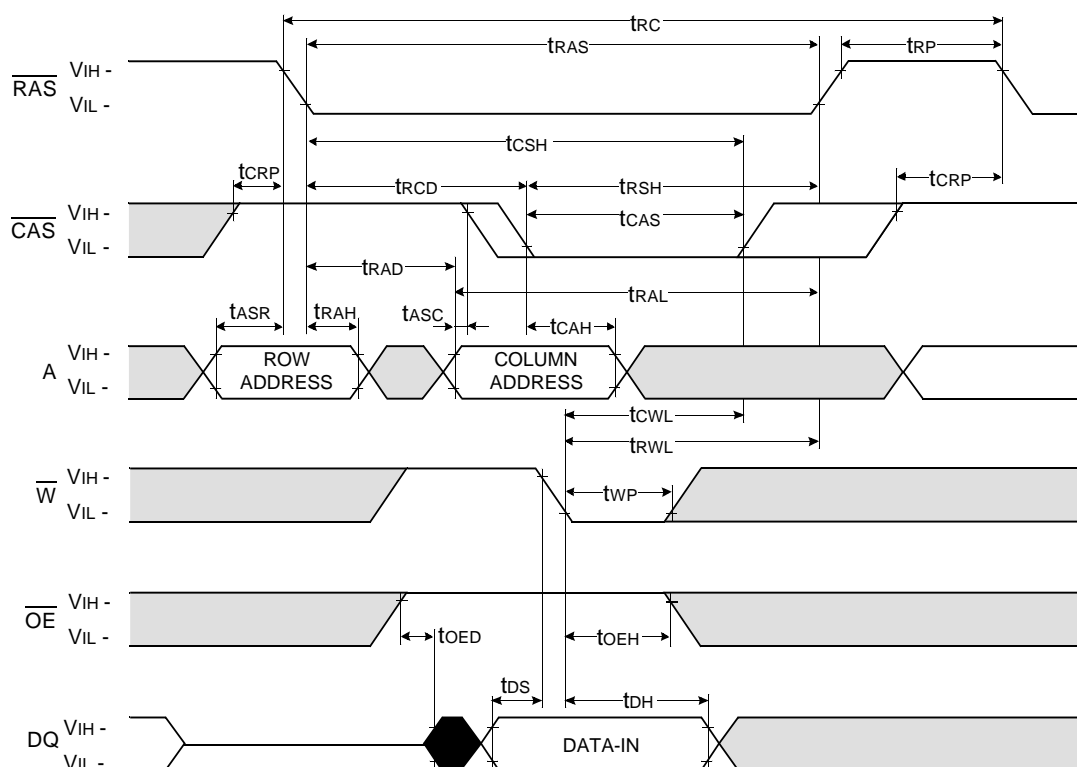
NOTE : DOUT = OPEN



Don't care
Undefined

WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

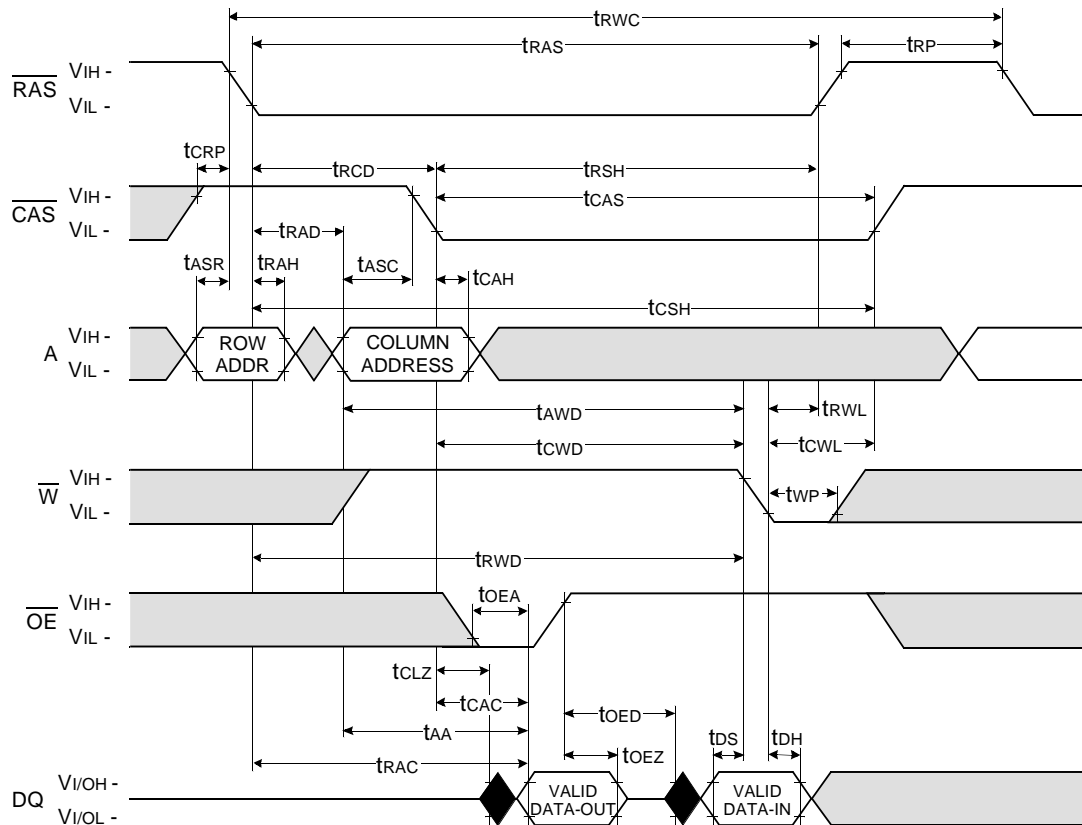
NOTE : DOUT = OPEN



Don't care

Undefined

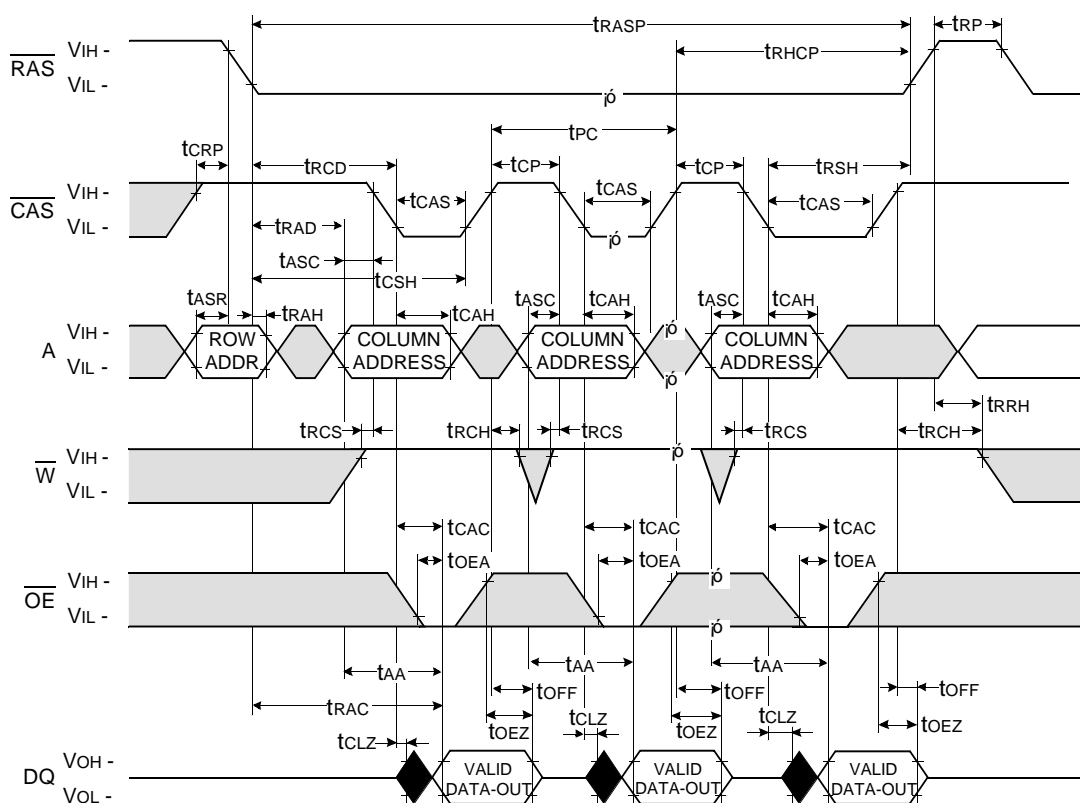
READ - MODIFY - WRITE CYCLE



Don't care
Undefined

FAST PAGE READ CYCLE

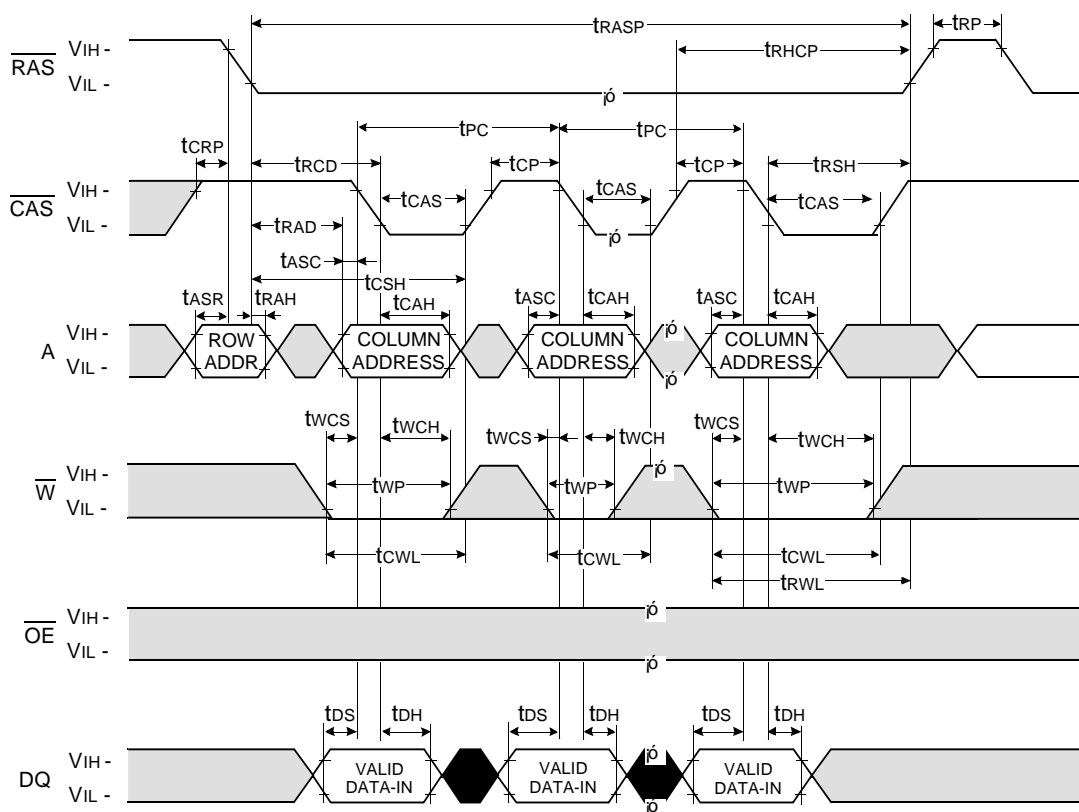
NOTE : DOUT = OPEN



Don't care
Undefined

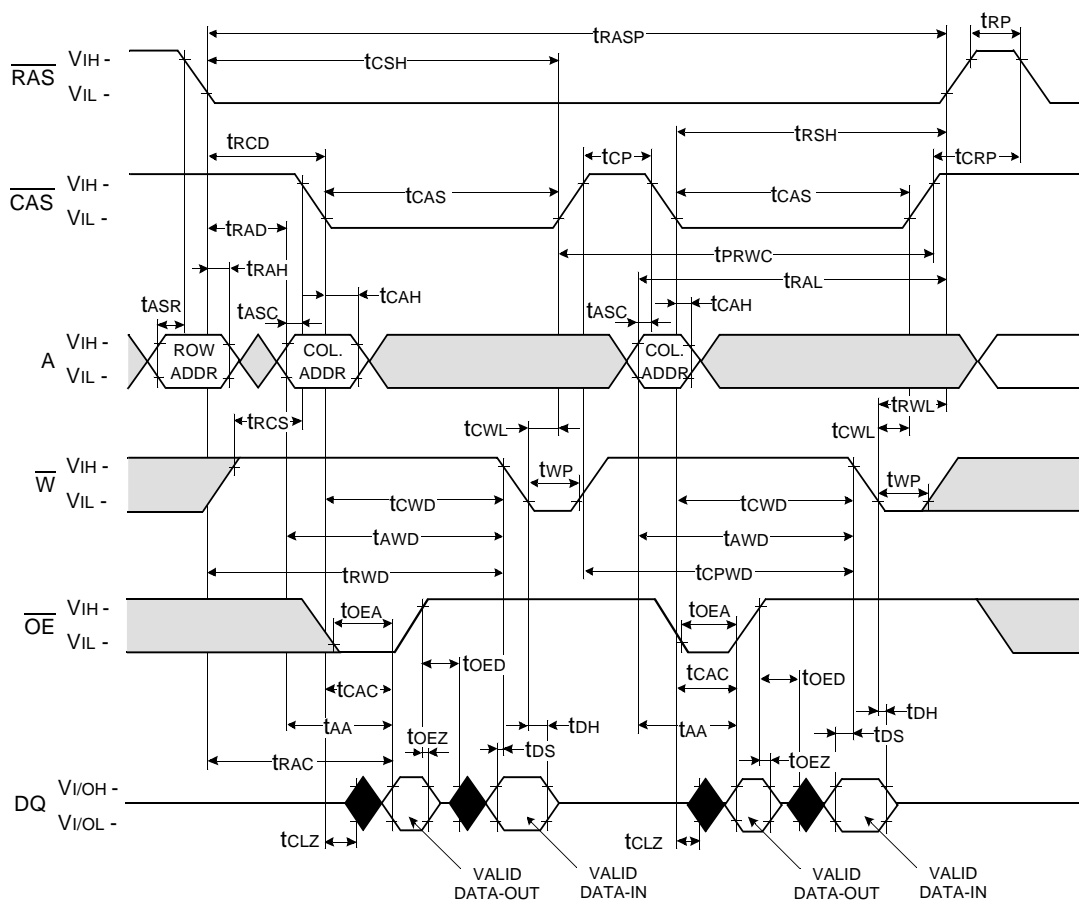
FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
Undefined

FAST PAGE READ - MODIFY - WRITE CYCLE



Don't care
Undefined

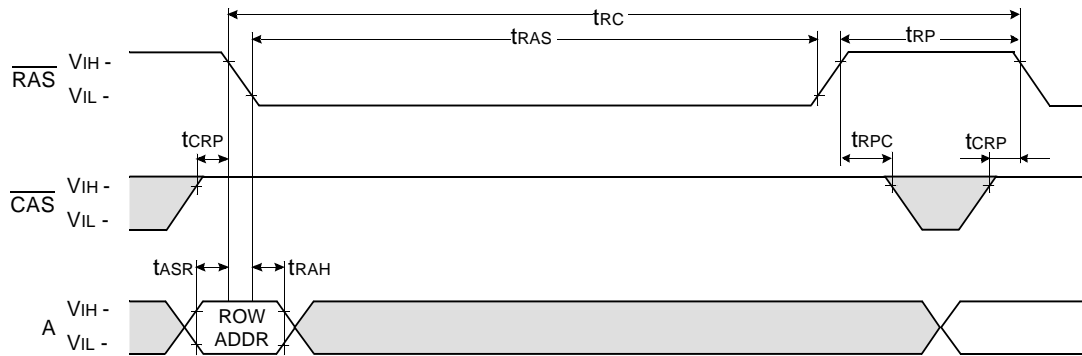
DRAM MODULE

M372V320(8)0CT1-C

RAS - ONLY REFRESH CYCLE

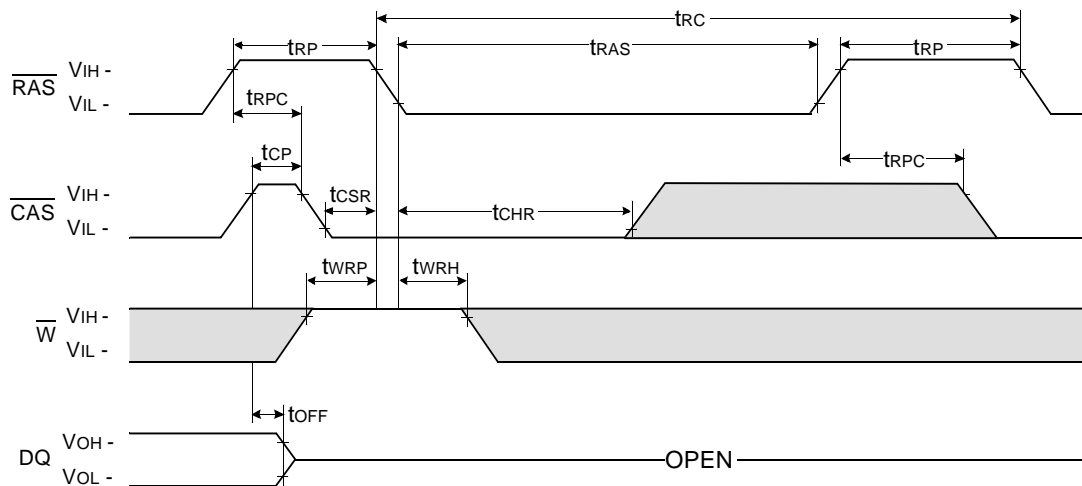
NOTE : \overline{W} , \overline{OE} , DIN = Don't care

DOUT = OPEN



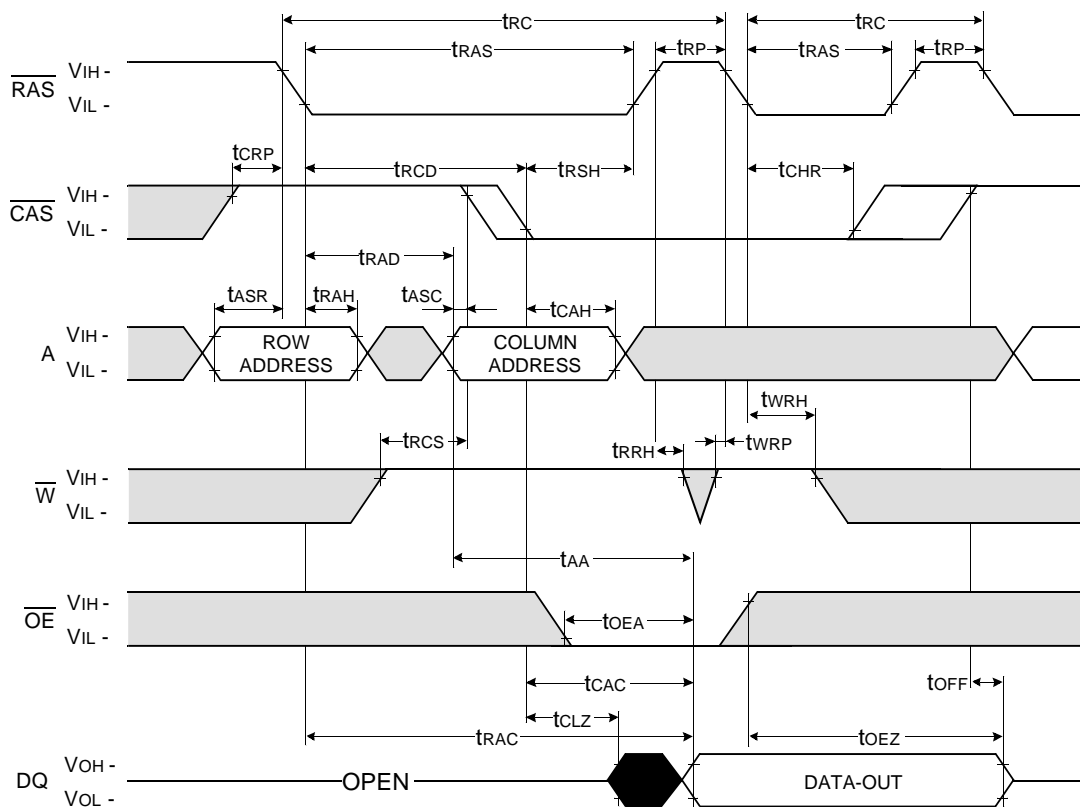
CAS - BEFORE - RAS REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care

☐ Don't care

Undefined

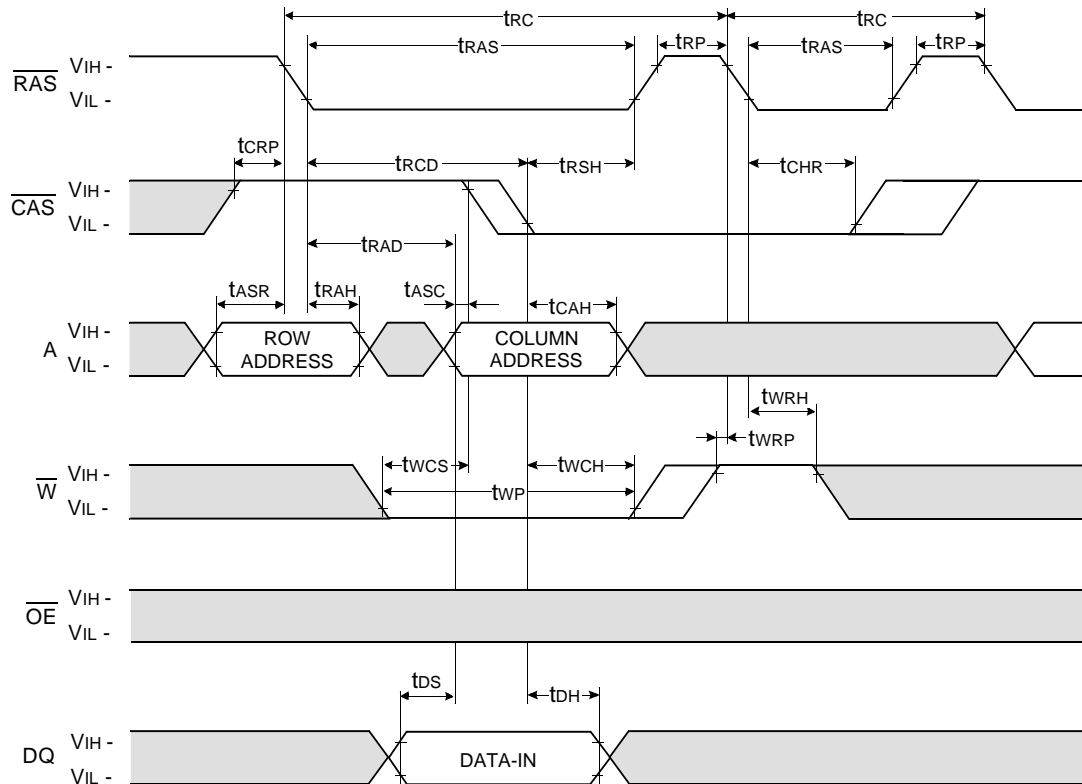
HIDDEN REFRESH CYCLE (READ)



Don't care
Undefined

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



Don't care
Undefined

The timing diagram illustrates the relationship between the Row Address Strobe (RAS), Column Address Strobe (CAS), and the Column Address (A) signals. The signals are shown as digital waveforms with high (VIH) and low (VIL) levels. The timing parameters are defined as follows:

- tr_{AS}**: RAS pulse width (high to low).
- t_{CSR}**: CAS setup time before RAS.
- t_{CHR}**: CAS hold time after RAS.
- t_{CPT}**: CAS pulse width (high to low).
- tr_{SH}**: RAS setup time before CAS.
- t_{CAS}**: CAS pulse width (low to high).
- tr_{AL}**: RAS to CAS delay.
- t_{ASC}**: CAS setup time before A.
- t_{CAH}**: CAS hold time after A.
- tr_P**: RAS pulse width (low to high).

The diagram illustrates the timing relationships for the E cycle. It shows three signals: \overline{W} , \overline{OE} , and DQ. The signal \overline{W} is active low and has a pulse width t_{WPL} . The signal \overline{OE} is active low and has a pulse width t_{OEL} . The signal DQ is active low and has a pulse width t_{DQL} . The timing parameters are defined as follows:

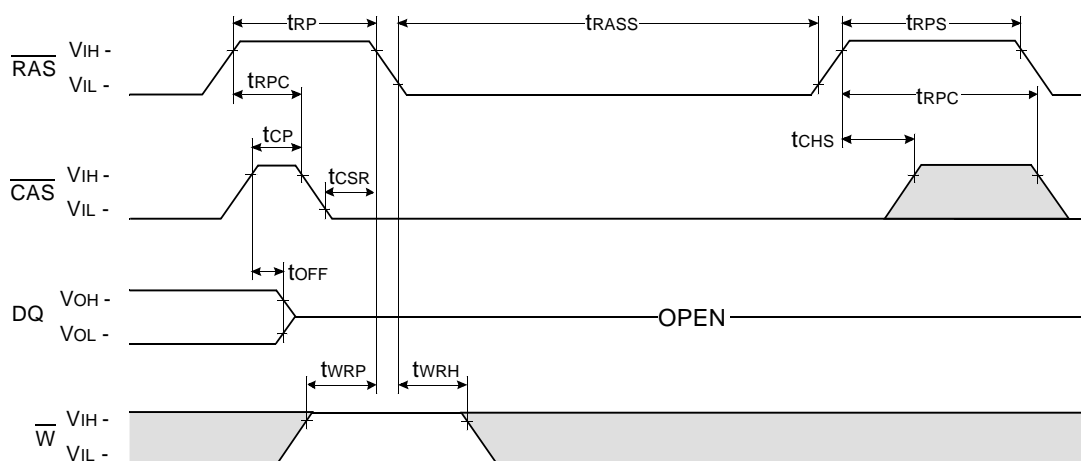
- t_{WRP} : Time from the rising edge of \overline{W} to the rising edge of \overline{OE} .
- t_{WRH} : Time from the falling edge of \overline{W} to the falling edge of \overline{OE} .
- t_{WCS} : Time from the rising edge of \overline{W} to the rising edge of DQ.
- t_{WCH} : Time from the falling edge of \overline{W} to the falling edge of DQ.
- t_{WPL} : Pulse width of \overline{W} .
- t_{OEL} : Pulse width of \overline{OE} .
- t_{DQL} : Pulse width of DQ.
- t_{DS} : Delay from the rising edge of \overline{W} to the rising edge of DQ.
- t_{DH} : Delay from the falling edge of \overline{W} to the falling edge of DQ.

Undefined

NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

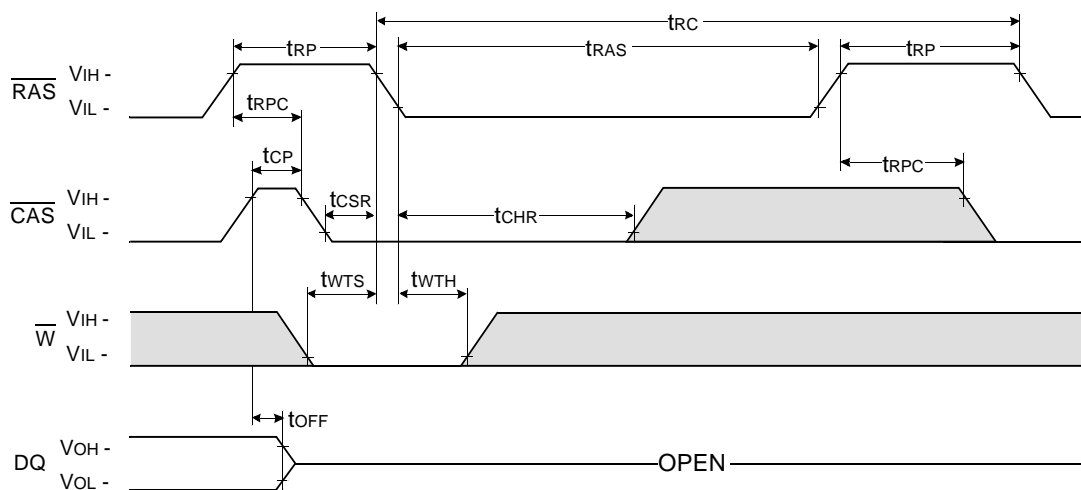
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



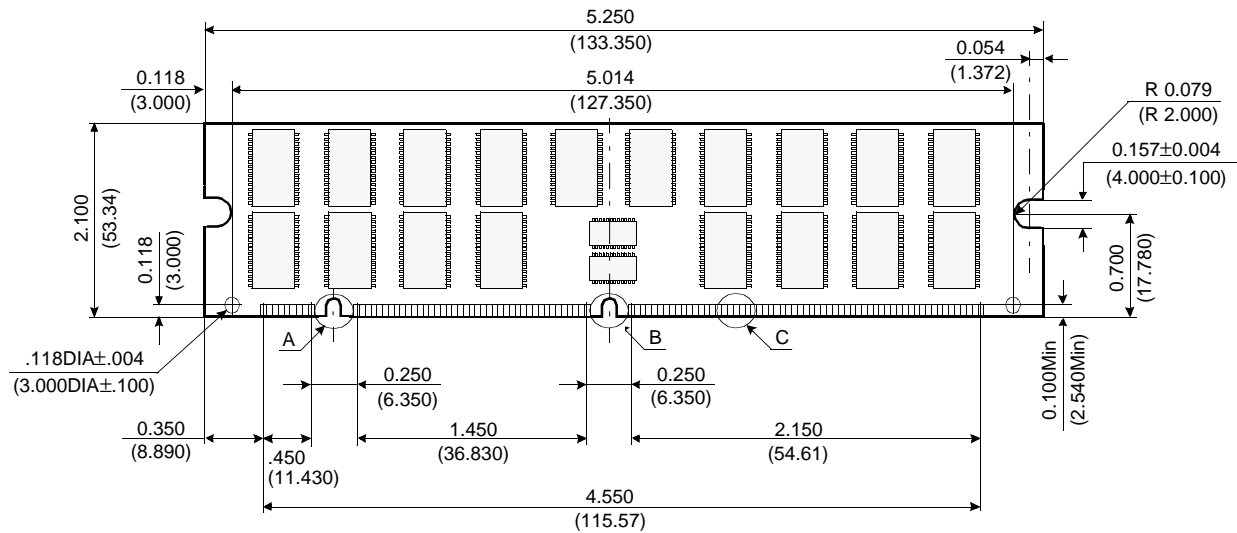
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DRAM MODULE

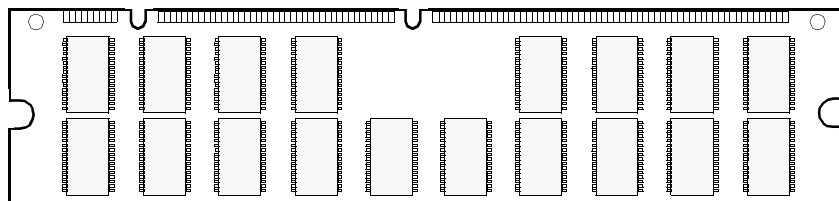
M372V320(8)0CT1-C

PACKAGE DIMENSIONS

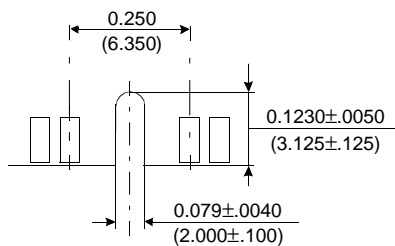
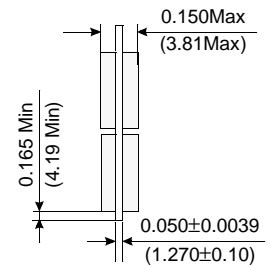
Units : Inches (millimeters)



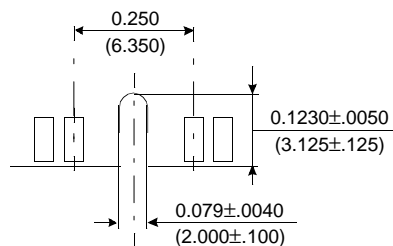
(Front view)



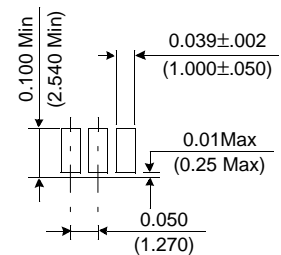
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, TSOP II
 DRAM Part No. : M372V3200CT1 - K4F640412C-T.
 M372V3280CT1 - K4F660412C-T.