

M374S3253DTS

PC133/PC100 Unbuffered DIMM

M374S3253DTS SDRAM DIMM

32Mx72 SDRAM DIMM with ECC based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M374S3253DTS is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M374S3253DTS consists of nine CMOS 32M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glas

s-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M374S3253DTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

| Part No. | Max Freq. (Speed) |
|----------------------|----------------------|
| M374S3253DTS-L7C/C7C | 133MHz (7.5ns@CL=2) |
| M374S3253DTS-L7A/C7A | 133MHz (7.5ns@CL=3) |
| M374S3253DTS-L1H/C1H | 100MHz (6.0ns@ CL=2) |
| M374S3253DTS-L1L/C1L | 100MHz (6.0ns@ CL=3) |

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V \pm 0.3V power supply
- MRS cycle with address key programs
Latency (Access from column address)
Burst length (1, 2, 4, 8 & Full page)
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, single sided component

PIN CONFIGURATIONS (Front side/back side)

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back |
|-----|-------|-----|--------|-----|-------|-----|------|-----|-------|
| 1 | Vss | 29 | DQM1 | 57 | DQ18 | 85 | Vss | 113 | DQM5 |
| 2 | DQ0 | 30 | CS0 | 58 | DQ19 | 86 | DQ32 | 114 | *CS1 |
| 3 | DQ1 | 31 | DU | 59 | VDD | 87 | DQ33 | 115 | RAS |
| 4 | DQ2 | 32 | Vss | 60 | DQ20 | 88 | DQ34 | 116 | Vss |
| 5 | DQ3 | 33 | A0 | 61 | NC | 89 | DQ35 | 117 | A1 |
| 6 | VDD | 34 | A2 | 62 | *VREF | 90 | VDD | 118 | A3 |
| 7 | DQ4 | 35 | A4 | 63 | *CKE1 | 91 | DQ36 | 119 | A5 |
| 8 | DQ5 | 36 | A6 | 64 | Vss | 92 | DQ37 | 120 | A7 |
| 9 | DQ6 | 37 | A8 | 65 | DQ21 | 93 | DQ38 | 121 | A9 |
| 10 | DQ7 | 38 | A10/AP | 66 | DQ22 | 94 | DQ39 | 122 | BA0 |
| 11 | DQ8 | 39 | BA1 | 67 | DQ23 | 95 | DQ40 | 123 | A11 |
| 12 | Vss | 40 | VDD | 68 | Vss | 96 | Vss | 124 | VDD |
| 13 | DQ9 | 41 | VDD | 69 | DQ24 | 97 | DQ41 | 125 | *CLK1 |
| 14 | DQ10 | 42 | CLK0 | 70 | DQ25 | 98 | DQ42 | 126 | A12 |
| 15 | DQ11 | 43 | Vss | 71 | DQ26 | 99 | DQ43 | 127 | Vss |
| 16 | DQ12 | 44 | DU | 72 | DQ27 | 100 | DQ44 | 128 | CKE0 |
| 17 | DQ13 | 45 | CS2 | 73 | VDD | 101 | DQ45 | 129 | *CS3 |
| 18 | VDD | 46 | DQM2 | 74 | DQ28 | 102 | VDD | 130 | DQM6 |
| 19 | DQ14 | 47 | DQM3 | 75 | DQ29 | 103 | DQ46 | 131 | DQM7 |
| 20 | DQ15 | 48 | DU | 76 | DQ30 | 104 | DQ47 | 132 | *A13 |
| 21 | CB0 | 49 | VDD | 77 | DQ31 | 105 | CB4 | 133 | VDD |
| 22 | CB1 | 50 | NC | 78 | Vss | 106 | CB5 | 134 | NC |
| 23 | Vss | 51 | NC | 79 | CLK2 | 107 | Vss | 135 | NC |
| 24 | NC | 52 | CB2 | 80 | NC | 108 | NC | 136 | CB6 |
| 25 | NC | 53 | CB3 | 81 | *WP | 109 | NC | 137 | CB7 |
| 26 | VDD | 54 | Vss | 82 | **SDA | 110 | VDD | 138 | Vss |
| 27 | WE | 55 | DQ16 | 83 | **SCL | 111 | CAS | 139 | DQ48 |
| 28 | DQM0 | 56 | DQ17 | 84 | VDD | 112 | DQM4 | 140 | DQ49 |

PIN NAMES

| Pin Name | Function |
|------------|------------------------------|
| A0 ~ A12 | Address input (Multiplexed) |
| BA0 ~ BA1 | Select bank |
| DQ0 ~ DQ63 | Data input/output |
| CB0 ~ CB7 | Check bit (Data-in/data-out) |
| CLK0, CLK2 | Clock input |
| CKE0 | Clock enable input |
| CS0, CS2 | Chip select input |
| RAS | Row address strobe |
| CAS | Column address strobe |
| WE | Write enable |
| DQM0 ~ 7 | DQM |
| VDD | Power supply (3.3V) |
| Vss | Ground |
| *VREF | Power supply for reference |
| SDA | Serial data I/O |
| SCL | Serial clock |
| SA0 ~ 2 | Address in EEPROM |
| *WP | Write protection |
| DU | Don't use |
| NC | No connection |

* These pins are not used in this module.

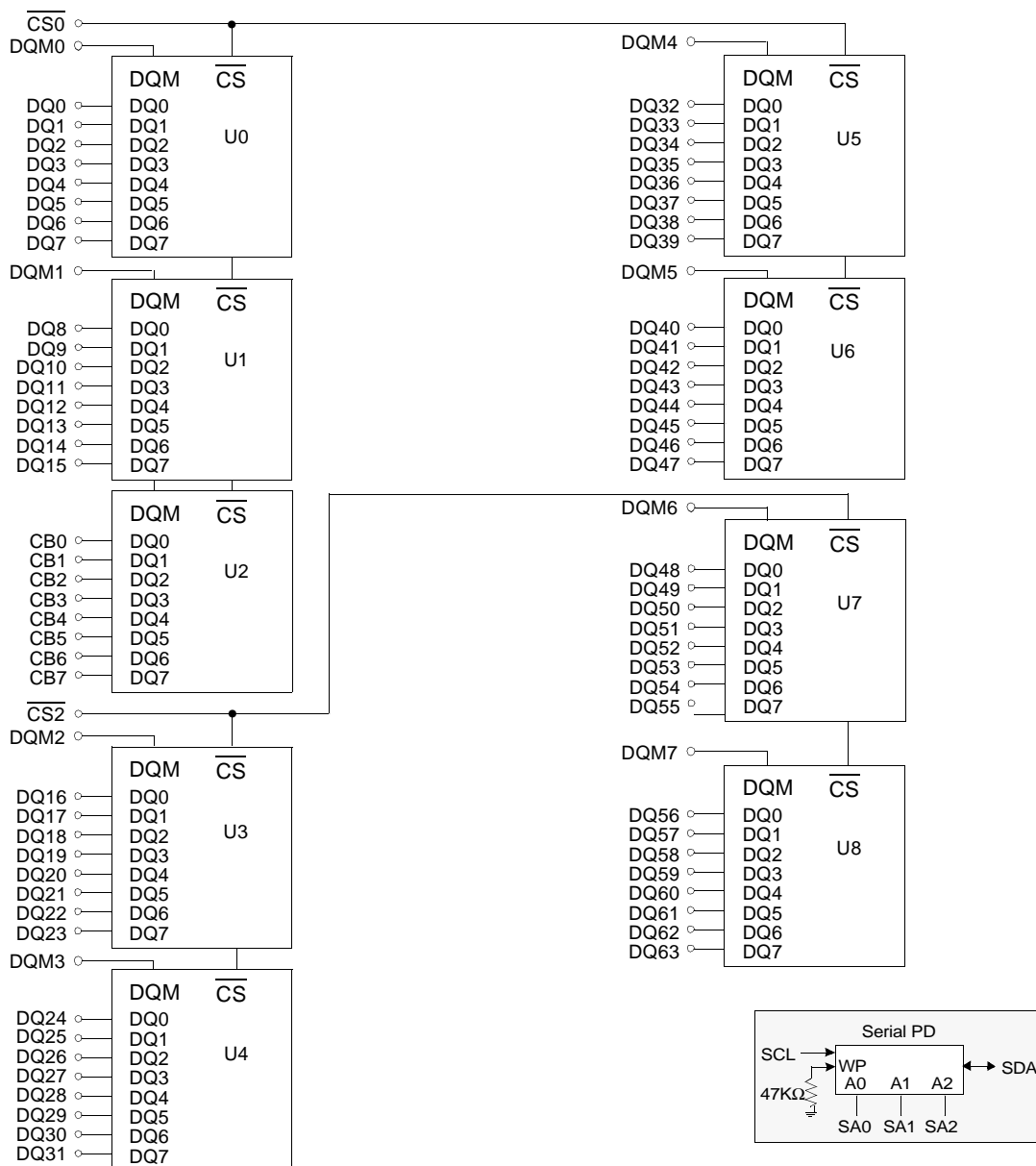
** These pins should be NC in the system which does not support SPD.

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PIN CONFIGURATION DESCRIPTION

| Pin | Name | Input Function |
|-------------------------|-------------------------------|---|
| CLK | <i>System clock</i> | Active on the positive going edge to sample all inputs. |
| $\overline{\text{CS}}$ | <i>Chip select</i> | Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM. |
| CKE | <i>Clock enable</i> | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command. |
| A0 ~ A12 | <i>Address</i> | Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9 |
| BA0 ~ BA1 | <i>Bank select address</i> | Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time. |
| $\overline{\text{RAS}}$ | <i>Row address strobe</i> | Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge. |
| $\overline{\text{CAS}}$ | <i>Column address strobe</i> | Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access. |
| $\overline{\text{WE}}$ | <i>Write enable</i> | Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active. |
| DQM0 ~ 7 | <i>Data input/output mask</i> | Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking) |
| DQ0 ~ 63 | <i>Data input/output</i> | Data inputs/outputs are multiplexed on the same pins. |
| CB0 ~ 7 | <i>Check bit</i> | Check bits for ECC. |
| VDD/VSS | <i>Power supply/ground</i> | Power and ground for the input buffers and the core logic. |

FUNCTIONAL BLOCK DIAGRAM



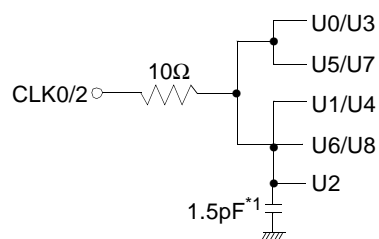
A0 ~ An, BA0 & 1 → SDRAM U0 ~ U8

 $\overline{\text{RAS}}$ → SDRAM U0 ~ U8 $\overline{\text{CAS}}$ → SDRAM U0 ~ U8 $\overline{\text{WE}}$ → SDRAM U0 ~ U8

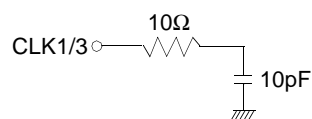
CKE0 → SDRAM U0 ~ U8

DQn $\xrightarrow{10\Omega}$ Every DQpin of SDRAM

VDD → Two 0.1μF Capacitors per each SDRAM
 VSS → To all SDRAMs



*1 : For 4 loads, CLK2 only.



ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---------------------------------------|------------------------------------|------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1.0 ~ 4.6 | V |
| Voltage on VDD supply relative to Vss | VDD, VDDQ | -1.0 ~ 4.6 | V |
| Storage temperature | T _{STG} | -55 ~ +150 | °C |
| Power dissipation | P _D | 9 | W |
| Short circuit current | I _{OS} | 50 | mA |

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------|-----------------|------|-----|----------|------|------------------------|
| Supply voltage | VDD, VDDQ | 3.0 | 3.3 | 3.6 | V | |
| Input logic high voltage | V _{IH} | 2.0 | 3.0 | VDDQ+0.3 | V | 1 |
| Input logic low voltage | V _{IL} | -0.3 | 0 | 0.8 | V | 2 |
| Output logic high voltage | V _{OH} | 2.4 | - | - | V | I _{OH} = -2mA |
| Output logic low voltage | V _{OL} | - | - | 0.4 | V | I _{OL} = 2mA |
| Input leakage current | I _{LI} | -10 | - | 10 | uA | 3 |

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ VDDQ.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

| Pin | Symbol | Min | Max | Unit |
|-------------------------------|--------|-----|-----|------|
| Address (A0 ~ A12, BA0 ~ BA1) | CADD | 35 | 45 | pF |
| RAS, CAS, WE | CIN | 35 | 45 | pF |
| CKE (CKE0) | CCKE | 35 | 45 | pF |
| Clock (CLK0, CLK2) | CCLK | 30 | 35 | pF |
| CS (CS0, CS2) | Ccs | 20 | 30 | pF |
| DQM (DQM0 ~ DQM7) | CdQM | 10 | 15 | pF |
| DQ (DQ0 ~ DQ63) | COUT1 | 6 | 8 | pF |
| CB (CB0 ~ CB7) | COUT2 | 6 | 8 | pF |

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

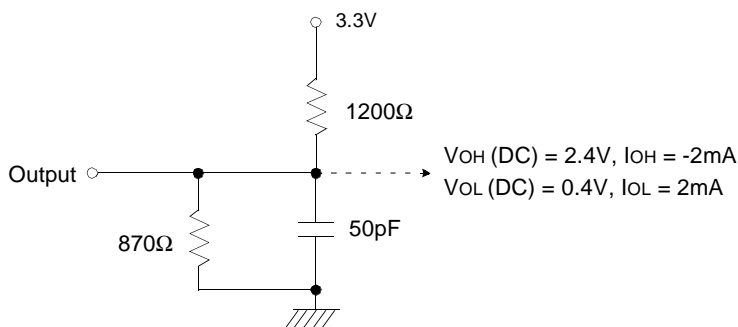
| Parameter | Symbol | Test Condition | | Version | | | | Unit | Note |
|---|--------|--|---|---------|-------|-------|-------|------|------|
| | | | | -7C | -7A | -1H | -1L | | |
| Operating current (One bank active) | ICC1 | Burst length = 1 trc ≥ trc(min) Io = 0 mA | | 900 | 810 | 810 | 810 | mA | 1 |
| Precharge standby cur- rent in power-down mode | ICC2P | CKE ≤ VIL(max), tcc = 10ns | | 18 | | | | mA | |
| | ICC2PS | CKE & CLK ≤ VIL(max), tcc = ∞ | | 18 | | | | | |
| Precharge standby cur- rent in non power-down mode | ICC2N | CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 10ns Input signals are changed one time during 20ns | | 180 | | | | mA | |
| | ICC2NS | CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable | | 90 | | | | | |
| Active standby current in power-down mode | ICC3P | CKE ≤ VIL(max), tcc = 10ns | | 54 | | | | mA | |
| | ICC3PS | CKE & CLK ≤ VIL(max), tcc = ∞ | | 54 | | | | | |
| Active standby current in non power-down mode (One bank active) | ICC3N | CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tcc = 10ns Input signals are changed one time during 20ns | | 270 | | | | mA | |
| | ICC3NS | CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable | | 225 | | | | mA | |
| Operating current (Burst mode) | ICC4 | Io = 0 mA Page burst 4banks Activated. tccd = 2CLKs | | 990 | 990 | 900 | 900 | mA | 1 |
| Refresh current | ICC5 | trc ≥ trc(min) | | 1,980 | 1,800 | 1,710 | 1,710 | mA | 2 |
| Self refresh current | ICC6 | CKE ≤ 0.2V | C | 27 | | | | mA | |
| | | | L | 13.5 | | | | mA | |

Notes :

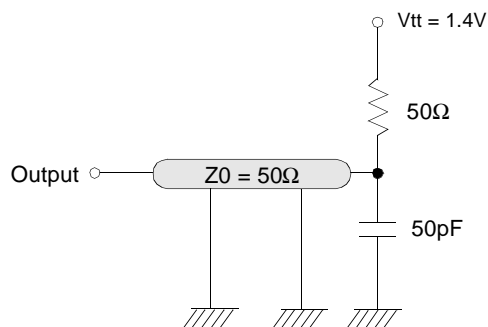
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to 70°C)

| Parameter | Value | Unit |
|---|-----------------|------|
| AC input levels (V_{ih}/V_{il}) | 2.4/0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | $t_r/t_f = 1/1$ | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Fig. 2 | |



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

| Parameter | | Symbol | Version | | | | Unit | Note |
|--|---------------|-----------|-------------|-----|-----|-----|------|------|
| | | | -7C | -7A | -1H | -1L | | |
| Row active to row active delay | | tRRD(min) | 15 | 15 | 20 | 20 | ns | 1 |
| RAS to CAS delay | | tRCD(min) | 15 | 20 | 20 | 20 | ns | 1 |
| Row precharge time | | tRP(min) | 15 | 20 | 20 | 20 | ns | 1 |
| Row active time | | tRAS(min) | 45 | 45 | 50 | 50 | ns | 1 |
| | | tRAS(max) | 100 | | | | us | |
| Row cycle time | | tRC(min) | 60 | 65 | 70 | 70 | ns | 1 |
| Last data in to row precharge | | tRDL(min) | 2 | | | | CLK | 2, 5 |
| Last data in to Active delay | | tDAL(min) | 2 CLK + tRP | | | | - | 5 |
| Last data in to new col. address delay | | tCDL(min) | 1 | | | | CLK | 2 |
| Last data in to burst stop | | tBDL(min) | 1 | | | | CLK | 2 |
| Col. address to col. address delay | | tCCD(min) | 1 | | | | CLK | 3 |
| Number of valid output data | CAS latency=3 | | 2 | | | | ea | 4 |
| | CAS latency=2 | | 1 | | | | | |

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. In 100MHz and below 100MHz operating conditions, $t_{RDL}=1\text{CLK}$ and $t_{DAL}=1\text{CLK} + 20\text{ns}$ is also supported. SAMSUNG recommends $t_{RDL}=2\text{CLK}$ and $t_{DAL}=2\text{CLK} + t_{RP}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

| Parameter | | Symbol | -7C | | -7A | | -1H | | -1L | | Unit | Note |
|---------------------------|---------------|--------|-----|------|-----|------|-----|------|-----|------|------|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| CLK cycle time | CAS latency=3 | tCC | 7.5 | 1000 | 7.5 | 1000 | 10 | 1000 | 10 | 1000 | ns | 1 |
| | CAS latency=2 | | 7.5 | | 10 | | 10 | | 12 | | | |
| CLK to valid output delay | CAS latency=3 | tSAC | | 5.4 | | 5.4 | | 6 | | 6 | ns | 1,2 |
| | CAS latency=2 | | | 5.4 | | 6 | | 6 | | 7 | | |
| Output data hold time | CAS latency=3 | tOH | 3 | | 3 | | 3 | | 3 | | ns | 2 |
| | CAS latency=2 | | 3 | | 3 | | 3 | | 3 | | | |
| CLK high pulse width | | tCH | 2.5 | | 2.5 | | 3 | | 3 | | ns | 3 |
| CLK low pulse width | | tCL | 2.5 | | 2.5 | | 3 | | 3 | | ns | 3 |
| Input setup time | | tSS | 1.5 | | 1.5 | | 2 | | 2 | | ns | 3 |
| Input hold time | | tSH | 0.8 | | 0.8 | | 1 | | 1 | | ns | 3 |
| CLK to output in Low-Z | | tSLZ | 1 | | 1 | | 1 | | 1 | | ns | 2 |
| CLK to output in Hi-Z | CAS latency=3 | tSHZ | | 5.4 | | 5.4 | | 6 | | 6 | ns | |
| | CAS latency=2 | | | 5.4 | | 6 | | 6 | | 7 | | |

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

| Command | | | CKEn-1 | CKEn | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | DQM | BA0,1 | A10/AP | A12, A11, A9 ~ A0 | Note |
|------------------------------------|------------------------|-------|--------|------|------------------------|-------------------------|-------------------------|------------------------|-----|---------|-------------|-----------------------------|------|
| Register | Mode register set | | H | X | L | L | L | L | X | OP code | | | 1,2 |
| Refresh | Auto refresh | | H | H | L | L | L | H | X | X | | | 3 |
| | Self refresh | L | | 3 | | | | | | | | | |
| | | Exit | L | H | L | H | H | H | X | X | | | 3 |
| | | | | | H | X | X | X | | | | | 3 |
| Bank active & row addr. | | | H | X | L | L | H | H | X | V | Row address | | |
| Read & column address | Auto precharge disable | | H | X | L | H | L | H | X | V | L | Column address (A0 ~ A9) | 4 |
| | Auto precharge enable | | | | | | | | | | H | | 4,5 |
| Write & column address | Auto precharge disable | | H | X | L | H | L | L | X | V | L | Column address (A0 ~ A9) | 4 |
| | Auto precharge enable | | | | | | | | | | H | | 4,5 |
| Burst stop | | | H | X | L | H | H | L | X | X | | | 6 |
| Precharge | Bank selection | | H | X | L | L | H | L | X | V | L | X | |
| | All banks | | | | | | | | | X | H | | |
| Clock suspend or active power down | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | V | V | V | | | | | |
| | | Exit | L | H | X | X | X | X | X | | | | |
| Precharge power down mode | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |
| | | Exit | L | H | H | X | X | X | X | | | | |
| | | | | | L | V | V | V | | | | | |
| DQM | | | H | X | | | | | V | X | | | 7 |
| No operation command | | | H | X | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at TRP after the end of burst.

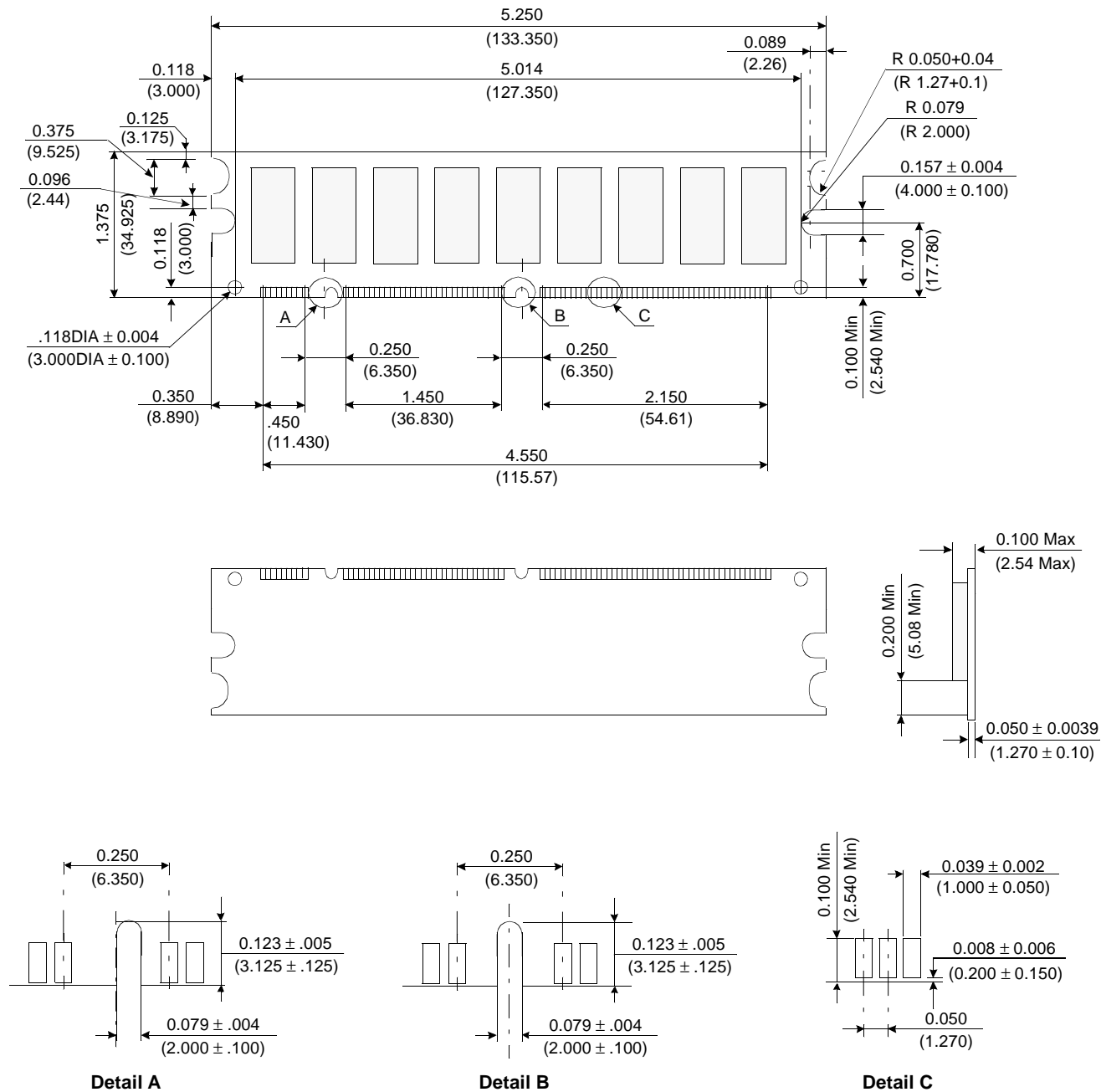
6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)

Tolerances : $\pm .005$ (.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
 SDRAM Part No. : K4S560832D

M374S3253DTS

PC133/PC100 Unbuffered DIMM

M374S3253DTS-L7C/L7A/L1H/L1L, C7C/C7A/C1H/C1L

- Organization : 32MX72
- Composition : 32MX8 *9
- Used component part # : K4S560832D-TL7C/7A/1H/1L,TC7C/7A/1H/1L
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,375 mil height & single sided component
- Refresh : 8K/64ms
- Contents :

| Byte#. | Function described | Function Supported | | | | Hex value | | | | Note |
|--------|--|--|-------|------|------|-----------|-----|-----|-----|------|
| | | -7C | -7A | -1H | -1L | -7C | -7A | -1H | -1L | |
| 0 | # of bytes written into serial memory at module manufacturer | 128bytes | | | | 80h | | | | |
| 1 | Total # of bytes of SPD memory device | 256bytes (2K-bit) | | | | 08h | | | | |
| 2 | Fundamental memory type | SDRAM | | | | 04h | | | | |
| 3 | # of row address on this assembly | 13 | | | | 0Dh | | | | 1 |
| 4 | # of column address on this assembly | 10 | | | | 0Ah | | | | 1 |
| 5 | # of module Rows on this assembly | 1 Row | | | | 01h | | | | |
| 6 | Data width of this assembly | 72 bits | | | | 48h | | | | |
| 7 | Data width of this assembly | - | | | | 00h | | | | |
| 8 | Voltage interface standard of this assembly | LVTTTL | | | | 01h | | | | |
| 9 | SDRAM cycle time from clock @CAS latency of 3 | 7.5ns | 7.5ns | 10ns | 10ns | 75h | 75h | A0h | A0h | 2 |
| 10 | SDRAM access time from clock @CAS latency of 3 | 5.4ns | 5.4ns | 6ns | 6ns | 54h | 54h | 60h | 60h | 2 |
| 11 | DIMM configuration type | ECC | | | | 02h | | | | |
| 12 | Refresh rate & type | 7.8us, support self refresh self | | | | 82h | | | | |
| 13 | Primary SDRAM width | x8 | | | | 08h | | | | |
| 14 | Error checking SDRAM width | x8 | | | | 08h | | | | |
| 15 | Minimum clock delay for back-to-back random column | tCCD = 1CLK | | | | 01h | | | | |
| 16 | SDRAM device attributes : Burst lengths supported | 1, 2, 4, 8 & full page | | | | 8Fh | | | | |
| 17 | SDRAM device attributes : # of banks on SDRAM device | 4 banks | | | | 04h | | | | |
| 18 | SDRAM device attributes : CAS latency | 2 & 3 | | | | 06h | | | | |
| 19 | SDRAM device attributes : CS latency | 0 CLK | | | | 01h | | | | |
| 20 | SDRAM device attributes : Write latency | 0 CLK | | | | 01h | | | | |
| 21 | SDRAM module attributes | Non-buffered/Non-Registered & redundant addressing | | | | 00h | | | | |
| 22 | SDRAM device attributes : General | +/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge | | | | 0Eh | | | | |
| 23 | SDRAM cycle time @CAS latency of 2 | 7.5ns | 10ns | 10ns | 12ns | 75h | A0h | A0h | C0h | 2 |
| 24 | SDRAM access time @CAS latency of 2 | 5.4ns | 6ns | 6ns | 7ns | 54h | 60h | 60h | 70h | 2 |
| 25 | SDRAM cycle time @CAS latency of 1 | - | | | | 00h | | | | 2 |
| 26 | SDRAM access time @CAS latency of 1 | - | | | | 00h | | | | 2 |
| 27 | Minimum row precharge time (=tRP) | 15ns | 20ns | 20ns | 20ns | 0Fh | 14h | 14h | 14h | |
| 28 | Minimum row active to row active delay (tRRD) | 15ns | 15ns | 20ns | 20ns | 0Fh | 0Fh | 14h | 14h | |
| 29 | Minimum RAS to CAS delay (=tRCD) | 15ns | 20ns | 20ns | 20ns | 0Fh | 14h | 14h | 14h | |
| 30 | Minimum activate precharge time (=tRAS) | 45ns | 45ns | 50ns | 50ns | 2Dh | 2Dh | 32h | 32h | |
| 31 | Module Row density | 1 Row of 128MB | | | | 40h | | | | |
| 32 | Command and Address signal input setup time | 1.5ns | 1.5ns | 2ns | 2ns | 15h | 15h | 20h | 20h | |
| 33 | Command and Address signal input hold time | 0.8ns | 0.8ns | 1ns | 1ns | 08h | 08h | 10h | 10h | |
| 34 | Data signal input setup time | 1.5ns | 1.5ns | 2ns | 2ns | 15h | 15h | 20h | 20h | |

SERIAL PRESENCE DETECT INFORMATION

| Byte # | Function described | Function Supported | | | | Hex value | | | | Note |
|--------|--|----------------------------------|-------|-----|-----|-----------|-----|-----|-----|------|
| | | -7C | -7A | -1H | -1L | -7C | -7A | -1H | -1L | |
| 35 | Data signal input hold time | 0.8ns | 0.8ns | 1ns | 1ns | 08h | 08h | 10h | 10h | |
| 36~61 | Superset information (maybe used in future) | - | | | | 00h | | | | |
| 62 | SPD data revision code | Current release Intel spd 1.2B/A | | | | 12h | | | | |
| 63 | Checksum for bytes 0 ~ 62 | - | | | | A3h | E4h | 4Bh | 7Bh | |
| 64 | Manufacturer JEDEC ID code | Samsung | | | | CEh | | | | |
| 65~71 | Manufacturer JEDEC ID code | Samsung | | | | 00h | | | | |
| 72 | Manufacturing location | Onyang Korea | | | | 01h | | | | |
| 73 | Manufacturer part # (Memory module) | M | | | | 4Dh | | | | |
| 74 | Manufacturer part # (DIMM configuration) | 3 | | | | 33h | | | | |
| 75 | Manufacturer part # (Data bits) | Blank | | | | 20h | | | | |
| 76 | Manufacturer part # (Data bits) | 7 | | | | 37h | | | | |
| 77 | Manufacturer part # (Data bits) | 4 | | | | 34h | | | | |
| 78 | Manufacturer part # (Mode & operating voltage) | S | | | | 53h | | | | |
| 79 | Manufacturer part # (Module depth) | 3 | | | | 33h | | | | |
| 80 | Manufacturer part # (Module depth) | 2 | | | | 32h | | | | |
| 81 | Manufacturer part # (Refresh, # of banks in Comp. & inter- | 5 | | | | 35h | | | | |
| 82 | Manufacturer part # (Composition component) | 3 | | | | 33h | | | | |
| 83 | Manufacturer part # (Component revision) | D | | | | 44h | | | | |
| 84 | Manufacturer part # (Package type) | T | | | | 54h | | | | |
| 85 | Manufacturer part # (PCB revision & type) | S | | | | 53h | | | | |
| 86 | Manufacturer part # (Hyphen) | " - " | | | | 2Dh | | | | |
| 87 | Manufacturer part # (Power) | L / C | | | | 4Ch / 43h | | | | |
| 88 | Manufacturer part # (Minimum cycle time) | 7 | 7 | 1 | 1 | 37h | 37h | 31h | 31h | |
| 89 | Manufacturer part # (Minimum cycle time) | C | A | H | L | 43h | 41h | 48h | 4Ch | |
| 90 | Manufacturer part # (TBD) | Blank | | | | 20h | | | | |
| 91 | Manufacturer revision code (For PCB) | S | | | | 53h | | | | |
| 92 | Manufacturer revision code (For component) | D-die (5th Gen.) | | | | 44h | | | | |
| 93 | Manufacturing date (Year) | - | | | | - | | | | 3 |
| 94 | Manufacturing date (Week) | - | | | | - | | | | 3 |
| 95~98 | Assembly serial # | - | | | | - | | | | 4 |
| 99~12 | Manufacturer specific data (may be used in future) | Undefined | | | | - | | | | 5 |
| 126 | System frequency for 100MHz | 100MHz | | | | 64h | | | | |
| 127 | Intel Specification details | Detailed 100MHz Information | | | | AFh | AFh | AFh | ADh | |
| 128+ | Unused storage locations | Undefined | | | | - | | | | 5 |

- Note :**
1. The row select address is excluded in counting the total # of addresses.
 2. This value is based on the component specification.
 3. These bytes are programmed by code of Date Week & Date Year with BCD format.
 4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.