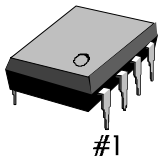
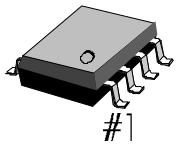
INTRODUCTION

The S1T0567 is a monolithic phase-locked loop system designed to provide a saturated transistor switch to GND when an input signal is present within the bandpass. External components are used to independently set the center frequency bandwidth and output delay.

8–DIP–300



8–SOP–225



FEATURES

- Wide frequency range (0.01Hz — 500kHz)
- Bandwidth adjustable from 0 to 14%
- Logic compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- High rejection of out-of-band signals and noise
- Frequency range adjustable over 20:1 range by an external resistor

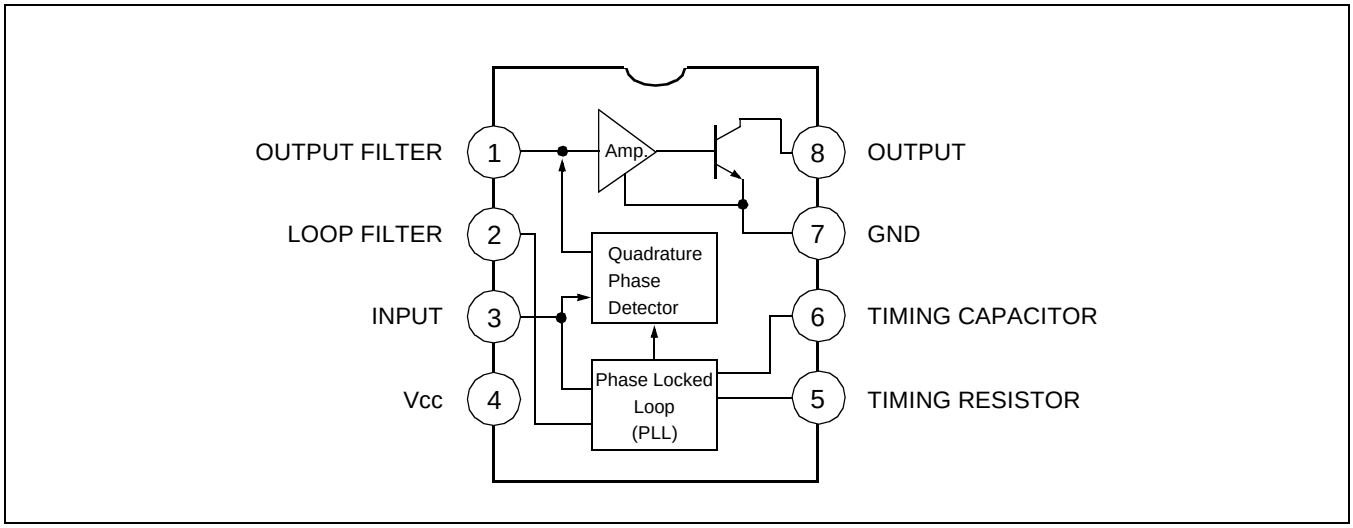
APPLICATIONS

- Touch Tone Decoder
- Wireless Intercom
- Communications paging decoders
- Frequency monitoring and control
- Ultrasonic controls (TV remote controls, etc.)
- Carrier current remote controls
- Precision oscillator

ORDERING INFORMATION

Device	Package	Operating Temperature
S1T0567X01-D0B0	8–DIP–300	0°C to + 70°C
S1T0567X01-S0B0	8–SOP–225	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

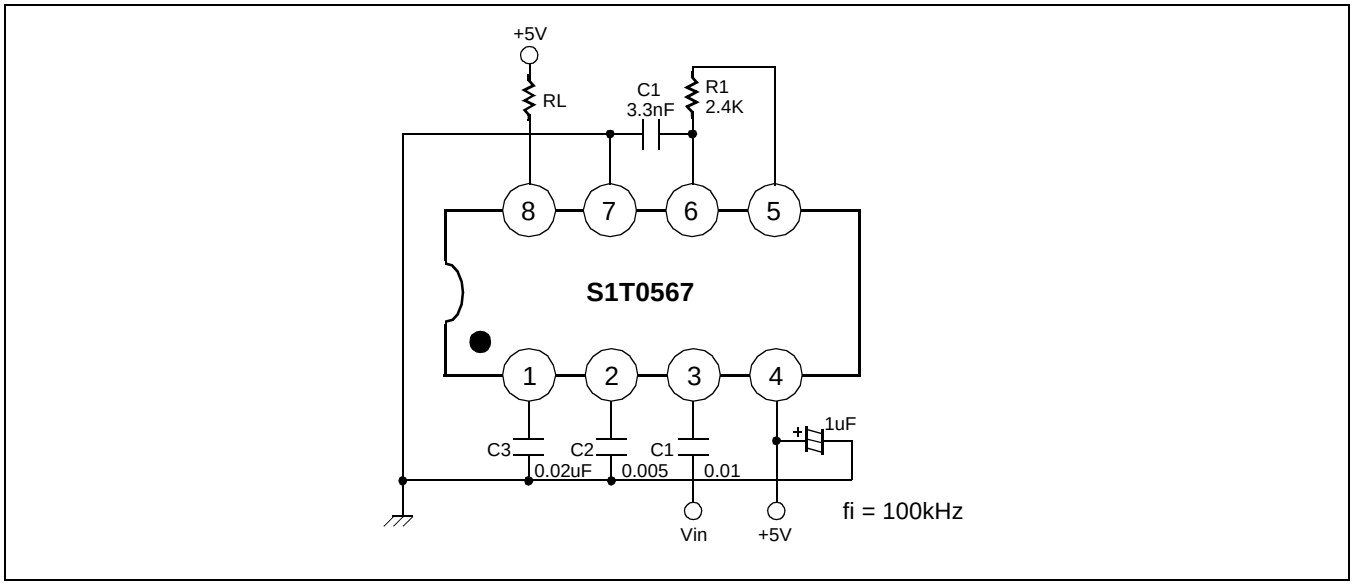
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Input Voltage	V_I	–10 — V_{CC} + 0.5	V
Output Voltage	V_O	15	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{OPR}	0 — + 70	°C
Storage Temperature	T_{STG}	– 65 — + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V, Ta = 25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating voltage range Operating current quiescent Operating current activated Quiescent power dissipation	V_{CC} $I_{CC\ (Q)}$ $I_{CC\ (A)}$ $P_{D\ (Q)}$	R_L = 20K	4.75	5.0 7 12 35	9.0 10 15	V mA mA mW
High center frequency Center frequency stability Center frequency shift with supply voltage	f_{HC} f_{ST} $\Delta f_C/\Delta V_{CC}$	R_L = 20K Ta = 0°C to 70°C	100	500 ± 60 0.7	 2	kHz ppm/°C %/V
Largest detection bandwidth Largest detection B.W skew Largest detection bandwidth variation with supply voltage Largest detection bandwidth variation with temperature	BW_{DET} BW_{DET} $\Delta BW/\Delta V_{CC}$ $\Delta BW/\Delta T$	–	10	14 2 ± 2 ± 0.1	18 3 ± 5 	% of fo % of fo %/V %/°C
Input Resistance	R_I	–	–	20	–	Kohm
Smallest detectable input voltage Largest No output input voltage	$V_{I\ (SMALL)}$ $V_{I\ (LARGE)}$	I_L = 100mA, fi = fo	 10	20 15	25 	mVrms mVrms
Greatest simultaneous outband signal to inband signal ratio Minimum input signal to wideband noise ratio	S1/SD S2/SD	R_L = 20K V_{IN} = 300mV_{rms} fi = fo = 100 kHz fi_1 = 140kHz fi_2 = 60kHz	–	+6 –6	–	dB dB
Fastest On-Off cycling rate Output leakage current	$C_{R\ (ON-OFF)}$ $I_{O\ (LKG)}$	R_L = 20 K V_{IN} = 2 5mV_{rms}	–	fo/20 0.01	 25	 µA
Output saturation voltage	V_{SAT1} V_{SAT2}	I_L = 300mA, V_{IN} = 25mVrms I_L = 100mA, V_{IN} = 25mVrms	–	0.2 0.6	0.4 1.0	V V
Output fall time Output rise time	t_F t_R	R_L = 50 R_L = 50	–	30 150	–	nS nS

TEST CIRCUIT



NOTE: Adjust for fo =100kHz

APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The S1T0567 monolithic tone decoder consists of a phase detector, low pass filter, and current-controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device normally has a high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pin 5 , Pin 6 and can typically reach 500kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependent upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is an open collector output, pull-down when an inband signal triggers the device.

Definition of S1T0567 Parameters

Center Frequency f_O

f_O is the free-running frequency of the C_L controlled oscillator with no input signal. It is determined by resistor R_1 between pins 5 and 6. Capacitor C_1 from pin 6 to ground f_O can be approximated by

$$fo \approx \frac{1}{R_1 C_1}$$

where R_1 is in ohms and C_1 is in farads.

LARGEST DETECTION BANDWIDTH

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

Detection Bandwidth (BW)

The detection bandwidth is the frequency range centered about f_O, within which an input signal larger than the threshold voltage (typically 20 mVrms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass filter. The bandwidth of the filter, as a percent of f_O, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_I}{f_o C_2}}$$

where V_i, is the input signal in volts, rms, and C_2 is the capacitance at pin 2 in μF.

Detection Band Skew

The detection band skew is a measure of how accurately the largest detection band is centered about the center frequency, f_O. It is defined as $(f_{max} + f_{min} - 2f_O)/f_O$, where f_{max} and f_{min}, are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment.

PIN DESCRIPTION

Output Filter-C_3 (Pin 1)

Capacitor C_3 connected from pin 1 to ground forms a simple low-pass post detection filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (4.7kΩ) is the internal impedance at pin 1.

The precise value of C_3 is not practical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that C_3 be ≥ 2 C_2. where C_2 is the loop filter capacitance at pin 2.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

Loop Filter - C_2 (Pin 2)

Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the S1T0567.

The filter time constant is given by $T_2 = R_2C_2$. where R_2 (10kΩ) is the impedance at pin 2.

The selection of C_2 is determined by the detection bandwidth requirements. For additional information see the section on “Definition of S1T0567 Parameters”.

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 f_O, with a slope of approximately 20 mV/% frequency deviation.

Input (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a DC level 2 volts above ground, and has an input impedance level of approximately 20kΩ.

Timing Resistor R_1 and Capacitor C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground, as shown in Figure 1.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} - 1.4V and an average DC level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average DC level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

Logic Output (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, base-collector power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor R_L, connected from pin 8 to the positive supply.

When an inband signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤ 20 volts.

OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for S1T0567 is shown in Figure 1. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_O = 1/R_1C_1$. For optimum temperature stability, R_1 should be selected *so* that 2 KΩ and the R_1C_1 product have sufficient stability over the projected operating temperature range.

2. C_2 is *a* low-pass capacitor.
If the input amplitude variation is known, the required f_OC_2 product can be found to give the desired bandwidth. Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the S1T0567 solely by the f_OC_2 product.

3. Capacitor C_3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. *A* typical minimum value of C_3 is 2 C_2.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

PRINCIPLE OF OPERATION

The S1T0567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in block diagram.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or “locks” on the input signal. The quadrature detector serves as a lock indicator : when the PLL is locked on an input signal, the DC voltage at the output of the detector is shifted. This DC level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a “bare collector” transistor stage capable of switching 100mA loads. The logic output at pin 8 is normally in a “high” state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a “low” state.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL.

This free-running frequency, f_O, is determined by the selection of R_1 and C_1 connected to pins 5 and 6, as shown in Figure 1. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2; and the output response speed is controlled by the output filter capacitor, C_3.

NOTES