

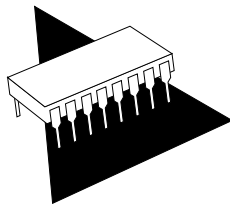
## **Revision History**

**- First Edition: March 1999**

**- Second Edition: February 2000**

- Library name change MDL110 into STD110
- All characteristic values are updated with mass product line characteristics.
- Add high density compiled memories to second edition. (chapter 5)
- The name of previous compiled memories are changed for example: spsram into spsram\_lp
- power equations are changed. (chapter 1)
- Updated PLL information
- Updated wire-load model





**STD110**

**0.25 $\mu$ m 2.5V CMOS Standard Cell Library  
for Pure Logic Products**



**STD110**  
**0.25 $\mu$ m 2.5V CMOS Standard Cell Library**  
**for Pure Logic Products**  
**Data Book**

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# Introduction

This databook contains information about STD110 0.25 $\mu$ m 2.5V standard cell library for pure Logic products developed by SEC (Samsung Electronics Corporation).

The “library” basically contains various kinds of internal and I/O cells and soft-macros which are used for developing ASIC (Application Specific Integrated Circuit). It also includes a design kit helping designers to work in a workstation platform, and all sorts of design environments needed for an automatic chip design.

There are six chapters in this databook:

Chapter 1	Introduction
Chapter 2	Electrical Characteristics
Chapter 3	Internal Macrocells
Chapter 4	Input/Output Cells
Chapter 5	Compiled Macrocells
Chapter 6	PLL

In this databook, each cell is followed by its AC electrical characteristics, and these characteristic values are almost equal when the corresponding cell is operated in a real chip.

The purpose of this databook is to prevent any misuse or misapplication of STD110 cell library by providing precise information about the cell list, electrical data, directions for use, and matters demanding special attention.

If you want to get more information about Digital cores and Analog cores that are not included in this databook, access the Samsung ASIC web site(<http://www.samsung.com/Products/Semiconductor/ASIC>) or contact head office.



# Contents

## 1 Introduction

1.1 Library Description .....	1-1
1.2 Features .....	1-2
1.3 EDA Support .....	1-4
1.4 Product Family .....	1-4
1.4.1 Analog Core Cell .....	1-4
1.4.2 Internal Macrocells .....	1-12
1.4.3 Compiled Macrocells .....	1-12
1.4.4 Input/Output Cells .....	1-13
1.5 Timings .....	1-16
1.6 Delay Model .....	1-22
1.7 Testability Design Methodology .....	1-24
1.8 Maximum Fanouts .....	1-27
1.9 Packages Capability by Lead Count .....	1-34
1.10 Power Dissipation .....	1-37
1.11 $V_{DD}/V_{SS}$ Rules and Guidelines .....	1-40
1.12 Crystal Oscillator Considerations .....	1-46

## 2 Electrical Characteristics

DC Electrical Characteristics .....	2-1
-------------------------------------	-----

## 3 Internal Macrocells

Overview .....	3-1
Summary Tables .....	3-2

### Logic Cells

AD2DH/AD2/AD2D2/AD2D4 .....	3-17
AD3DH/AD3/AD3D2/AD3D4 .....	3-19
AD4DH/AD4/AD4D2/AD4D4 .....	3-21
AD5/AD5D2/AD5D4 .....	3-24
ND2DH/ND2/ND2D2/ND2D4 .....	3-27
ND3DH/ND3/ND3D2/ND3D4 .....	3-29
ND4DH/ND4/ND4D2/ND4D2B/ND4D4 .....	3-32
ND5/ND5D2/ND5D4 .....	3-35
ND6/ND6D2/ND6D4 .....	3-38



## Contents

---

ND8/ND8D2/ND8D4 .....	3-42
NR2DH/NR2/NR2D2/NR2D2B/NR2D4/NR2A .....	3-46
NR3DH/NR3/NR3D2/NR3D2B/NR3D4/NR3A .....	3-49
NR4DH/NR4/NR4D2/NR4D2B/NR4D4 .....	3-53
NR5/NR5D2/NR5D4 .....	3-56
NR6/NR6D2/NR6D4 .....	3-60
NR8/NR8D2/NR8D4 .....	3-64
OR2DH/OR2/OR2D2/OR2D4 .....	3-68
OR3DH/OR3/OR3D3/OR3D4 .....	3-70
OR4DH/OR4/OR4D2/OR4D4 .....	3-73
OR5/OR5D2/OR5D4 .....	3-76
XN2/XN2D2/XN2D4 .....	3-80
XN3/XN3D2/XN3D4 .....	3-82
XO2/XO2D2/XO2D4 .....	3-84
XO3/XO3D2/XO3D4 .....	3-86
AO21DH/AO21/AO21D2/AO21D2B/AO21D4 .....	3-88
AO211DH/AO211/AO211D2/AO211D2B/AO211D4 .....	3-91
AO2111/AO2111D2 .....	3-94
AO22DH/AO22/AO22D2/AO22D2B/AO22D4 .....	3-97
AO22DHA/AO22A/AO22D2A/AO22D4A .....	3-100
AO221/AO221D2/AO221D4 .....	3-103
AO222/AO222D2/AO222D2B/AO222D4 .....	3-107
AO222A/AO222D2A/AO222D4A .....	3-112
AO2222/AO2222D2/AO2222D4 .....	3-114
AO31DH/AO31/AO31D2/AO31D4 .....	3-118
AO311/AO311D2/AO311D4 .....	3-121
AO3111/AO3111D2 .....	3-125
AO32/AO32D2/AO32D4 .....	3-128
AO321/AO321D2/AO321D4 .....	3-132
AO322/AO322D2/AO322D4 .....	3-136
AO33/AO33D2/AO33D4 .....	3-140
AO331/AO331D2/AO331D4 .....	3-144
AO332/AO332D2/AO332D4 .....	3-148
AO4111/AO4111D2 .....	3-152
OA21DH/OA21/OA21D2/OA21D2B/OA21D4 .....	3-155
OA211DH/OA211/OA211D2/OA211D2B/OA211D4 .....	3-158
OA2111/OA2111D2 .....	3-161
OA22DH/OA22/OA22D2/OA22D2B/OA22D4 .....	3-164
OA22DHA/OA22A/OA22D2A/OA22D4A .....	3-167
OA221/OA221D2/OA221D4 .....	3-170
OA222/OA222D2/OA222D2B/OA222D4 .....	3-174
OA2222/OA2222D2/OA2222D4 .....	3-179
OA31/OA31D2/OA31D4 .....	3-183



OA311/OA311D2/OA311D4.....	3-186
OA3111/OA3111D2 .....	3-190
OA32/OA32D2/OA32D4.....	3-193
OA321/OA321D2/OA321D.....	3-197
OA322/OA322D2/OA322D4.....	3-201
OA33/OA33D2/OA33D4.....	3-205
OA331/OA331D2/OA331D4.....	3-209
OA332/OA332D2/OA332D4.....	3-213
OA4111/OA4111D2 .....	3-217
SCG1/SCG1D2 .....	3-220
SCG2//SCG2D2 .....	3-223
SCG3/SCG3D2 .....	3-225
SCG4/SCG4D2 .....	3-228
SCG5/SCG5D2 .....	3-231
SCG6/SCG6D2 .....	3-234
SCG7/SCG7D2 .....	3-236
SCG8/SCG8D2 .....	3-239
SCG9/SCG9D2 .....	3-241
SCG10/SCG10D2 .....	3-243
SCG11/SCG11D2 .....	3-246
SCG12/SCG12D2 .....	3-248
SCG13/SCG13D2 .....	3-250
SCG14/SCG14D2 .....	3-252
SCG15/SCG15D2 .....	3-254
SCG16/SCG16D2 .....	3-256
SCG17/SCG17D2 .....	3-258
SCG18/SCG18D2 .....	3-260
SCG19/SCG19D2 .....	3-263
SCG20/SCG20D2 .....	3-265
SCG21/SCG21D2 .....	3-267
SCG22/SCG22D2 .....	3-269
DL1D2/DL1D4.....	3-271
DL2D2/DL2D4.....	3-272
DL3D2/DL3D4.....	3-273
DL4D2/DL4D4.....	3-274
DL5D2/DL5D4.....	3-275
DL10D2/DL10D4.....	3-276
IVDH/IV/IVD2/IVD3/IVD4/IVD6/IVD8/IVD16 .....	3-277
IVCD(11/13)/IVCD(22/26)/IVCD44.....	3-280
IVT/IVTD2/IVTD4/IVTD8/IVTD16 .....	3-282
IVTN/IVTND2/IVTND4/IVTND8/IVTND16 .....	3-284
NIDH/NID/NID2/NID3/NID4/NID6/NID8/NID16 .....	3-286
OAK_NID10P/OAK_NID20P .....	3-289



NIT/NITD2/NITD4/NITD8/NITD16 .....	3-290
NITN/NITND2/NITND4/NITND8/NITND16 .....	3-293
OAK_DUCLK10/OAK_DUCLK16 .....	3-296
CTSB/CTSBD2/CTSBD3/CTSBD4/CTSBD6/CTSBD8/CTSBD16.....	3-298

## Flip-Flops

FD1/FD1D2 .....	3-303
FD1CS/FD1CSD2 .....	3-305
FD1S/FD1SD2 .....	3-307
FD1SQ/FD1SQD2.....	3-309
FD1Q/FD1QD2 .....	3-311
FD2/FD2D2 .....	3-313
FD2CS/FD2CSD2 .....	3-315
FD2S/FD2SD2 .....	3-319
FD2SQ/FD2SQD2.....	3-321
FD2Q/FD2QD2 .....	3-323
FD3/FD3D2 .....	3-325
FD3CS/FD3CSD2 .....	3-327
FD3S/FD3SD2 .....	3-331
FD3SQ/FD3SQD2.....	3-333
FD3Q/FD3QD2 .....	3-335
FD4/FD4D2 .....	3-337
FD4CS/FD4CSD2 .....	3-340
FD4S/FD4SD2 .....	3-344
FD4SQ/FD4SQD2.....	3-348
FD4Q/FD4QD2 .....	3-351
FD5/FD5D2 .....	3-353
FD5S/FD5SD2 .....	3-355
FD6/FD6D2 .....	3-357
FD6S/FD6SD2 .....	3-359
FD7/FD7D2 .....	3-361
FD7S/FD7SD2 .....	3-363
FD8/FD8D2 .....	3-365
FD8S/FD8SD2 .....	3-368
FDS2/FDS2D2 .....	3-372
FDS2CS/FDS2CSD2 .....	3-374
FDS2S/FDS2SD2 .....	3-376
FDS3/FDS3D2 .....	3-378
FDS3CS/FDS3CSD2 .....	3-380
FDS3S/FDS3SD2 .....	3-382
FJ1/FJ1D2.....	3-384
FJ1S/FJ1SD2.....	3-386
FJ2/FJ2D2.....	3-388



FJ2S/FJ2SD2 .....	3-390
FJ4/FJ4D2 .....	3-392
FJ4S/FJ4SD2 .....	3-395
FT2/FT2D2 .....	3-398

## Latches

LD1/LD1D2 .....	3-402
LD1A/LD1D2A .....	3-404
LD1Q/LD1QD2 .....	3-406
LD2/LD2D2 .....	3-408
LD2Q/LD2QD2 .....	3-411
LD3/LD3D2 .....	3-413
LD4/LD4D2 .....	3-416
LD5/LD5D2 .....	3-419
LD5Q/LD5QD2 .....	3-421
LD6/LD6D2 .....	3-423
LD6Q/LD6QD2 .....	3-426
LD7/LD7D2 .....	3-428
LD8/LD8D2 .....	3-431
OAK_LDI2/OAK_LDI2D2 .....	3-434
OAK_LDI3/OAK_LDI3D2 .....	3-437
LS0/LS0D2 .....	3-442
LS1/LS1D2 .....	3-444

## Bus Holder

BUSHOLDER .....	3-448
-----------------	-------

## Internal Clock Drivers

CK(2/4/6/8) .....	3-449
-------------------	-------

## Decoders

DC4 .....	3-452
DC4I .....	3-454
DC8I .....	3-456

## Adders

FADH/FA/FAD2 .....	3-461
HADH/HA/HAD2 .....	3-464
SCG23/SCG23D2 .....	3-467

## Multiplexers

MX2DH/MX2/MX2D2/MX2D4 .....	3-471
MX2X4 .....	3-474
MX2IDH/MX2I/MX2ID2/MX2ID4 .....	3-477
MX2IDHA/MX2IA/MX2ID2A/MX2ID4A .....	3-480



MX2IX4 .....	3-483
MX3I/MX3ID2/MX3ID4 .....	3-486
MX4/MX4D2/MX4D4 .....	3-490
MX8/MX8D2/MX8D4 .....	3-494

## 4 Input/Output Cells

Overview .....	4-1
Summary Tables .....	4-2

### Input Buffers

PvIC/PvICD/PvICU .....	4-9
PvIS/PvISD/PvISU .....	4-13
PvIT/PvITD/PvITU .....	4-17

### Output Buffers

PvOByz .....	4-21
PvODyz .....	4-30
PvOTyz .....	4-40

### Bi-Directional Buffers

PvBaDyz/PvBaUDyz .....	4-60
PvBaTyz/PvBaDTyz/PvBaUTyz .....	4-60

### Input Clock Drivers

PSCKDCaby .....	4-62
PSCKDSaby .....	4-66

### Oscillators

PHSOSC(K1/K2/M1/M2/M3) .....	4-71
PHSOSC(K17/K27/M16/M26/M36) .....	4-77
PSOSC(K1/K2/M1/M2) .....	4-83

### PCI Buffers

PTIPCI .....	4-90
PTOPCI .....	4-91
PTBPCI .....	4-92

### USB I/O Buffers

PBUSB/PBUSB1 .....	4-95
PBUSB_LS .....	4-96
PBUSB_FS .....	4-97



**Power Pads**

VDD2(I/P/O/IP/OP/T/R)/VDD3(P/O/OP) .....	4-104
VSS2(I/P/O/IP/OP/T/R)/VSS3(P/O/OP) .....	4-104

**Analog Interface**

PIC_ABB .....	4-106
PICC_ABB .....	4-107
PICEN_ABB .....	4-108
POT_ABB .....	4-109

**ESD Slot Cells**

EV2I/EV2P/EV2O/EV2IP/EV2OP/EV2T/EV2P/EV2O/EV2OP .....	4-112
EV2I_ABB/EV2OP_ABB/EV2T_ABB .....	4-112

**Common Slot Cells**

EC0C0/EC0C0D/EC0CA0/EC0CA0D/EC0C0_BB/EC0C0D_BB/EC0C0_VBB/EC0C0D_VBB .....	4-113
---	-------

## 5 Compiled Macrocells

Overview to Compiled Memory .....	5-1
Compiled Memory Naming Convention .....	5-1
Characteristics for Timing and Power .....	5-2
Built-In Self Test for Compiled Memory .....	5-3
Selection Guide for Compiled Memory .....	5-4

**High-Density Compiled Memory**

SPSRAM_HD .....	5-7
SPSRAMBW_HD .....	5-17
DPSRAM_HD .....	5-27
SPARAM_HD .....	5-37
DROM_HD .....	5-48
MROM_HD .....	5-56
ARFRAM_HD .....	5-64
FIFO_HD .....	5-83

**Low-Power Compiled Memory**

SPSRAM_LP .....	5-95
DPSRAM_LP .....	5-105
SPARAM_LP .....	5-115
DROM_LP .....	5-125
MROM_LP .....	5-133



## Contents

---

### Overview to Compiled Datapath

Overview to Compiled Datapath .....5-141

Compiled Macrocell Selection Guide .....5-142

ADDER.....5-143

BS .....5-148

MPY .....5-153

## 6 PLL

PLL2013X .....6-1



## NOTE



---

# Introduction

1

---



## Table of Contents

1.1	Library Description .....	1-1
1.2	Features .....	1-2
1.3	EDA Support.....	1-4
1.4	Product Family.....	1-4
	1.4.1 Analog Core Cells .....	1-4
	1.4.2 Internal Macrocells .....	1-12
	1.4.3 Compiled Macrocells .....	1-12
	1.4.4 Input/Output Cells.....	1-14
1.5	Timings .....	1-16
1.6	Delay Model.....	1-22
1.7	Testability Design Methodology .....	1-24
1.8	Maximum Fanouts .....	1-27
1.9	Packages Capability by Lead Count .....	1-34
1.10	Power Dissipation .....	1-37
1.11	$V_{DD}/V_{SS}$ Rules and Guidelines .....	1-40
1.12	Crystal Oscillator Considerations .....	1-46



## 1.1 Library Description

SEC ASIC offers STD110 as 0.25μm CMOS standard cell library. SEC's 0.25μm cell-based logic process providing up to 5 layers of interconnect metal with various I/O pad-pitch options such as 70um pitch pad and 80um pitch pad.

STD110 which reduced power dissipation and system cost by merging the logic and IPs as a whole and connecting internally from logic to memory data bus is ideal for high-performance products such as graphics controller, projector, portable CD and so on.

STD110 can support up to eight million gate counts of logic providing 75% of usable gate. STD110 is 25% faster than 0.35um library STD90. Logic density is 2.3 times greater than that of STD90. The power consumption of compiled memory is 90% smaller than STD90.

STD110 also supports fully user-configurable compiled memory and datapath elements. Each element is provided as a compiler. Two different types of compiled memories in STD110 are available to support memories suitable to high-density and low-power applications.

To support mixed voltage environments, 2.5V, 3.3V drive and 5V-tolerant IO cells are available. LVTTTL, LVCMOS, PCI, OSC, AGP, PECL, HSTL, LVDS and USB buffers are supported. To better support a system-on-chip design style, various core cells are available including processor cores like ARM7TDMI/ARM9TDMI/ARM920T/ARM940T from ARM, Teaklite from DSPG.

The STD110 supports data transmission and communication core such as USB, IEEE1284 and UART.

The list of analog core cells includes ADC, DAC, CODEC, LVDS, RAMDAC and PLL with various bits and frequency ranges.

SEC design methodology offers an comprehensive timing driven design flow including automated time budgeting, tight floorplan synthesis intergration, powerful timing analysis and timing driven layout. Its advanced characterization flow provides accurate timing data and robust delay models for a 0.25um very deep-submicron technology. Advanced verification methods like static timing analysis and formal verification provide an effective verification methodology with a variety of simulators and cycle based simulation. SEC DFT methodology supports scan design, BIST and JTAG boundary scan. SEC provides a full set of test-ready IPs with an efficient core test integration methodology.



## 1.2 Features

- 2.5V standard cell library including processor and analog cores
- 0.25um five layer metal(from four layer metal option) CMOS technology
  - Logic, processor and analog
- High basic cell usages
  - Up to 8 million gates
  - Maximum usage: 75% for five layer metal
- High speed
  - Typical 2-input NAND gate delay (ND2D4): 70ps (F/O=2 + WL (0.02pF))
- Operation temperature ( $T_A$ )
  - Commercial range: 0°C to +70°C
  - Industrial range: -40°C to +85°C
- Digital cores usages
  - Hard-macro: ARM7TDMI, ARM9TDMI, ARM920T, ARM940T, Teaklite
  - Soft-macro: AMBA, DMA Controller, SDRAM Controller, Interrupt Controller, IIC, WDT, RTC, USB, IrDA, UART(16C450, 16C550), Fast Ethernet MAC, P1394a LINK, RS Decoder, Viterbi Decoder
- Analog cores usages
  - Ultra low voltage analog core (2.5V and 1.8V) available
  - Analog core supply voltage:
    - 2.5V analog core:  $2.5V \pm 5\%$
    - 1.8V analog core:  $1.8V \pm 5\%$
  - ADC: 8bit (30M, 2.5V), 10bit ((30M, 100M, 2.5V), (250K, 20M, 1.8V)), 12bit (200K, 20M, 2.5V)
  - DAC: 8bit (2M, 2.5V), 10bit ((300M, 2.5V), (2M, 1.8V)), 12bit ((2M, 2.5V), (80M, 1.8V))
  - CODEC: 8bit (8K~11K), 16bit (44.1K)
  - PLL: 25M ~ 300M (FSPLL, 2.5V), 1G (PLL, 1.8V), 20M ~ 170M(FSPLL, 1.8V)
  - Others: 300M (RAMDAC+PLL)
- Fully user-configurable Static RAMs and ROMs
  - High-density and low-power memory available
  - Duty-free cycle in synchronous memory available
  - 2-bank architecture available
  - Flexible aspect ratio available
  - Up to 256K-bit single-port SRAM available.
  - Up to 128K-bit dual-port SRAM available.
  - Up to 512K-bit diffusion and metal-2 ROM available.
  - Up to 16K-bit multi-port register file available.
  - Up to 32K-bit FIFO available.
- Fully configurable datapath macrocells
  - 4 ~ 64 bit adder available
  - 4 ~ 64 bit barrel shifter available
  - 6 ~ 64 bit multiplier with 1-stage pipeline available
  - Various output driver strength available
  - A tightly integrate apollo, Avant!, design environment
- I/O cells
  - 2.5V/3.3V and 5V tolerant IO
  - 3-level (high, medium, no) slew rate control
  - 1/2/4/6/8/10/12mA available for 3.3V and 2.5V output buffers
  - 1/2/3mA available for 5V-tolerant output buffers



- IO IP available
  - PCI ((33MHz, 66MHz, 3.3V), (33MHz, 3.3/5V tolerant))
  - USB (full speed/low speed)
  - SSTL2 (DDR SDRAM interface, up to 200MHz)
  - AGP (AGP2.0 Compliant, 66MHz@1X, 133MHz@2X, 266MHz@4X)
  - PECL (2.5V interface, up to 400MHz)
  - HSTL (class1, class2, 30MHz)
  - LVDS (3.3V(2.5V optional) interface, 300MHz)
- Various package options
  - QFP, thin QFP, power QFP, plastic BGA, super BGA, plastic leaded chip carrier, etc.
- Fully integrated CAD software and EDA support
  - Logic synthesis: Synopsys Design Compiler
  - Logic simulation: Cadence Verilog-XL, Cadence NC-Verilog, Viewlogic ViewSim, Mentor ModelSim-VHDL, Mentor ModelSim-Verilog, Synopsys VSS, Synopsys VCS
  - Scan insertion and ATPG: Synopsys TestGen, Synopsys Test Compiler, Mentor Fastscan
  - Static timing analysis: Synopsys PrimeTime, Synopsys MOTIVE
  - RC analysis: Avant! Star-RC
  - Power analysis: Synopsys DesignPower, CubicPower (In-House Tool)
  - Formal verification: Synopsys Formality, Chrysalis Design VERIFYer, Verplex Tuxedo-LEC
  - Fault simulation: Cadence Verifault, SuperTest (In-House Tool)
  - Delay calculator: CubicDelay (In-House Tool)
- STD110 contains 12 user selectable clock tree cells(CTC). At the pre-layout design stage, these will be used as the cells which represent actual clock tree informatin of P&R. The key features of new SEC ASIC CTS flow are as follows:
  - 12 user selectable clock tree cells(CTC) for STD110
  - Good pre-layout and post-layout correlation
  - No customer netlist modification
  - Accurate post-layout back-annotation mechanism
  - Insertion delay, skew, transition time management
  - Clock tree information file generation
  - Cover 100 to 30,000 fanouts and up to 1M gate count for CTS spanning block (GCCSB)
  - Tightly coupled with SEC in-house delay calculator, CubicDelay Gated CTS support
  - Hierarchical/Flatten verilog, edif interface for P&R

For more detail information for CTC flow, refer to "CTC flow guideline for CubicDelay" included in SEC ASIC design kit.



## 1.3 EDA Support

SEC ASIC provides an efficient solution for multi-million gate ASICs in very deep submicron (VDSM) technology. For large system-on-chip (SOC) type designs, static verification methodology (static timing analysis and formal verification) will shorten your design cycle time, which in turn will lessen today's ever-increasing time-to-market pressure. Our Design-for-Test (DFT) methodology and service take you through all phases of test insertion, test pattern generation and fault grading to get high test coverage.

STD110 supports a rich collection of industry-standard EDA tools from Cadence, Synopsys, Mentor graphics, and Avant! on multiple design platforms such as Solaris and HP. Customers are allowed to choose among the industry-leading EDA tools from design capture, synthesis, simulation, and DFT to layout. Several powerful proprietary software tools are seamlessly integrated in our design kits to improve your product quality.

For high simulation accuracy, STD110 uses a proprietary delay calculator. Cell delay is calculated based on a matrix of delay parameters for each macrocell, and signal interconnect delay is calculated based on the RC tree analysis.

## 1.4 Product Family

STD110 library include the following design elements:

- Analog core cells
- Digital core cells
- Internal macrocells
- Compiled macrocells
- Input/Output cells.

### 1.4.1 ANALOG CORE CELLS

#### Introduction to Analog Cores

SEC ASIC is one of the leading suppliers of cell based mixed analog and digital designs. As a leading supplier of mixed analog and digital designs, SEC ASIC has more analog design experience than any other vendors. Analog has been and will continue to be a part of the strategic focus at SEC ASIC. Analog design is a part of the total SEC ASIC integrated design system. Workstation symbols are supplied for analog cells and are entered as part of the design by the customer or design center. SEC ASIC uses basically the same automatic layout and verification tools for analog cells as for digital cells. Analog designs are processed on the same production line as digital designs.

SEC's analog core family comprises ADC,DAC,PLL and sigma-delta ADC/DAC, and their brief functional descriptions are introduced below.

[data sheets for all analog cores available]

#### Analog-to-Digital Converters

Analog-to-digital converters provide the link between the analog world and digital systems. Due to their extensive use of analog and mixed analog-digital operations, A/D converters often appear as the bottleneck in data processing applications, limiting the overall speed or precision.

An A/D converter produces a digital output, D, as a function of the analog input, A:

$$D = f(A)$$

While the input can assume an infinite number of values, the output can be selected from only a finite set of codes given by the converter's output word length(i.e, resolution). Thus, the ADC must approximate each input level with one of these codes, this process is so called 'quantization'.



In a digital system the amplitude is quantized into discrete steps, and at the same time the signal is sampled at discrete time intervals. This time interval is called sampling time or sampling frequency. After sampling and quantization process, the analog signal(A) becomes digital output (D).

### Digital-to-Analog Converters

The D/A converters are the digital-to-analog conversion circuits, which are also called DACs. They can be considered as decoding devices that accept digitally coded signals and provide analog output in the form of currents or voltages. In this manner, they provide an interface between the digital signal of the computer systems and continuous signals of analog world. They are employed in a variety of applications, from CRT display systems and voice sythesizers to automatic test systems, digital controlled attenuators, and process control actuators. In addition, they are key components inside most A/D converters.

Figure 1 shows the functional block diagram of a basic D/A converter system. The input to the D/A converter is a digital word, made up a stream of binary bits comprised of 1's and 0's. The output analog quantity A, which can be a voltage or current, is related to the input as

$$A = KV_{REF} \left[ \frac{b1}{2^1} + \frac{b2}{2^2} + \dots + \frac{bn}{2^n} \right]$$

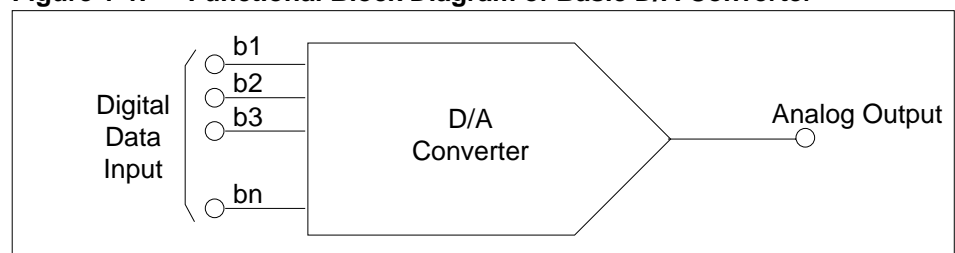
where K is a scale factor,  $V_{REF}$  is a reference voltage, n is the total number of bits, and  $b1, b2, \dots, bn$  are the bit coefficients, which are quantized to be a 1 or a 0.

As a function of the input binary word which determines the bit coefficients, the output exhibits  $2^n$  discrete voltage level ranging from zero to a maximum value of

$$Vo(max) = V_{REF} \frac{2^n - 1}{2^n}$$

with a minimum step change  $\Delta Vo$  given as  $\Delta Vo = \frac{V_{REF}}{2^n}$

**Figure 1-1. Functional Block Diagram of Basic D/A Converter**





### Sigma-Delta ADC/DAC

VLSI offers high speed and high density, but reduced accuracy for analog components and reduced signal range (reduced dynamic range). Hence, an exchange of digital complexity and of resolution in time for resolution in signal amplitude is needed. So good solution is over-sampling data converter. Oversampling sigma-delta converter is used in slow speed (audio band) application because of process limit. It's noise shaping (sigma-delta) feature make high resolution about max.  $SND=90\sim100dB$

In ADC path, analog single input is converted to differential signal with anti-aliasing filtering through anti-aliasing filter block. And sigma-delta modulator converts the signal into oversampled noise-shaping 1bit PDM (Pulse Density Modulation). Following digital decimation filter reject the out of band noise and outputs 16bits high resolution digital data with down sampled to  $F_s$  rate. In DAC path, digital input data is oversampled by interpolation filter and it is converted to noise-shaped 1bit PDM through digital sigma-delta modulator. Analog SC-post-filter rejects the out of band noise. And anti-image filter rejects sampling images and outputs single analog signal with high resolution.

### Phase Locked Loop

Samsung's PLL cores implemented as an analog function provide frequency multiplication capabilities and enable system designers to synchronize ASIC chip-level clock networks with a common reference signal.

In the past, designers wishing to incorporate a PLL into a digital design environment had only two options:

- (1) A special mixed-signal process to incorporate analog functions onto the chip
- (2) An all digital PLL that can be incorporated into a standard digital process.

However, a mixed-signal process is too expensive to be a feasible solution. On the other hand digital PLLs typically require huge silicon area and exhibits poor locking time despite their high accuracy.

Differing from the previous solutions, Samsung's PLL cores can be implemented on standard digital CMOS process while functioning as an analog PLL.

Samsung's PLL cores:

- \* Require only a few off-chip passive components for the whole function
- \* Remove the need for an expensive mixed-signal process
- \* Provide faster locking time than all digital PLLs
- \* Present low jitter characteristics

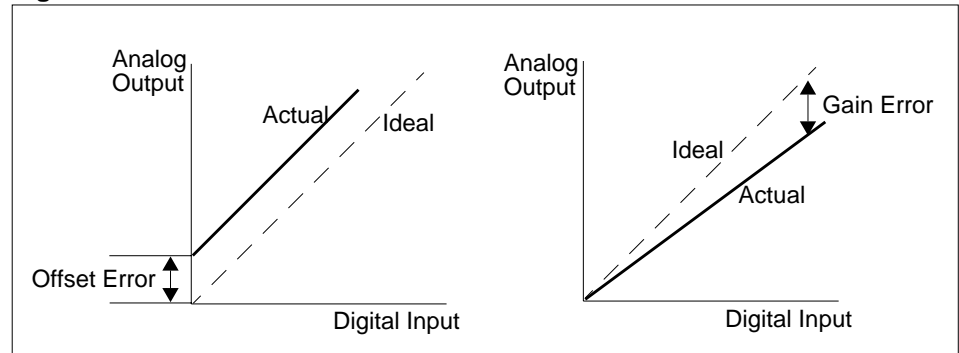
### Glossary by Core Families

#### 1. Digital-to-Analog Converter

**1. Resolution** - An n-bit binary converter should be able to provide  $2^n$  distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have resolution of n bits. The smallest output change that can be resolved by a linear DAC is  $2^{-n}$  of the full-scale span.

**2. Accuracy** - Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Source of error include gain error, offset error, linearity errors and noise. Error is usually commensurate with resolution, less than  $2^{-(n+1)}$ , or 1/2 LSB of full scale.



**Figure 1-2. Error of D/A Converter**

**3. LSB (Least-Significant Bit)** - In a system in which a numerical magnitude is represented by a series of binary digits, the LSB is that bit that carries the smallest value or weight. It represents the smallest analog change that can be resolved by an n-bit converter.

$$\text{LSB (Analog Value)} = \text{FSR}/2^n$$

FSR = Full-Scale Range, n = number of bits

**4. MSB (Most-Significant Bit)** - The binary digit with the largest numerical weighting. Normally, the MSB of a digital word has a weighting of 1/2 the full range.

**5. Compliance-Voltage Range** - For a current output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

**6. Glitch** - A glitch is a switching transient appearing in the output during a code transition. Its value is expressed as a product of voltage (V\*ns) or current (mA\*ns) and time duration or charge transferred.

**7. Harmonic Distortion (and Total Harmonic Distortion)** - The DAC is driven by the digitized representation of sine wave. The ratio of the RMS sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second through fifth.

$$\text{THD} = 20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

V1: RMS amplitude of the fundamental

**8. Signal-to-Noise Ratio (SNR)** - This signal to noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half the sampling frequency, this signal to noise ratio must be specified and should ideally follow the theoretical formula;

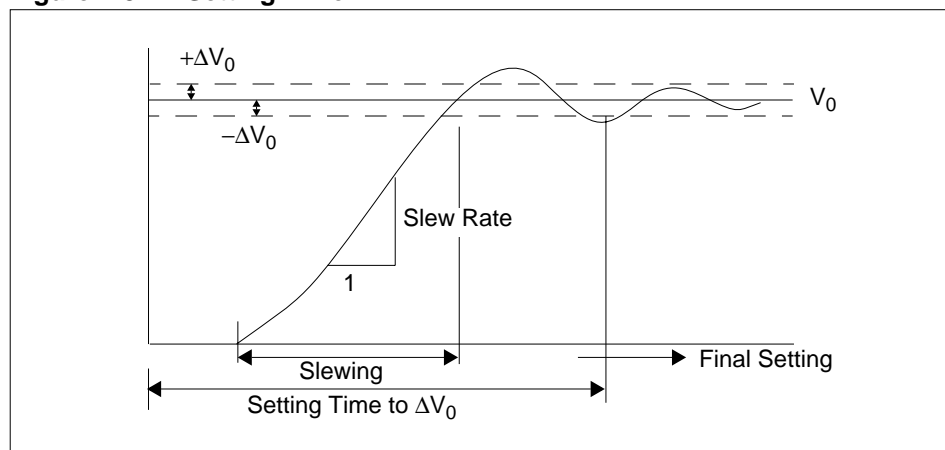
$$\text{S/N}_{\text{max}} = 6.02N + 1.76\text{dB}$$

**9. Slew Rate** - Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration such as limited current to charge of capacitor. Amplifiers with slew rate of a few V/μs are common and moderate in cost. Slew rates greater than about 75 V/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).



**10. Settling Time** - The time required, following a prescribed data change from the 50% point of the login input change, for the output of a DAC to reach and to remain within a given fraction (usually  $\pm 1/2\text{lsb}$ ) of the final value. Typical prescribed changes are full scale, 1MSB and 1LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

**Figure 1-3. Setting Time**



**11. Power-Supply Sensitivity** - The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (of fractions of 1LSB) for a 1% dc change in the power supply. Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed  $1/2\text{LSB}$  for 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

**12. ILE (integral Linearity Error)** - Linearity error of a converter, expressed in %, ppm of full-scale range or multiples of 1LSB, is a deviation of the analog values in a plot of the measured conversion relationship from a straight line. The straight line can be either a "best straight line" determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviation of the actual transfer characteristics from this straight line; or it can be a straight line passing through the endpoints of the transfer characteristic endpoints of the transfer characteristic after they have been calibrated (sometimes referred to as "endpoint" linearity). Endpoint linearity error is similar to relative accuracy error. For multiplying D/A converters, the analog linearity error, at a specified digital code, is defined in the same way as for multipliers, by deviation from a "best straight line" through the plot of the analog output-input response.

**13. DLE (Differential Linearity Error)** - Any two adjacent digital codes should result in measured output values that are exactly 1LSB apart ( $2^{-n}$  of full scale for an  $n$ -bit converter). Any deviation of the measured "step" from the ideal difference is called differential linearity error expressed in multiples of 1LSB. It is an important specification because a differential linearity error greater than 1LSB can lead to non-monotonic response in a D/A converter and missed codes in an A/D converter.

**14. Monotonic** - A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases with the result that the output will always be a single-valued function of the input. The specification "monotonic"



(over a given temperature range) is sometimes substituted for a differential non-linearity specification since differential nonlinearity less than 1LSB is a sufficient condition for monotonic behaviour.

## 2. Analog-to-Digital Converter

**1. ILE (Integral Linearity Error: INL)** - Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB before the first code transition. "Full scale" is defined as a level 1 1/2LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

**2. DLE (Differential Linearity Error: DNL)** - An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes are guaranteed.

**3. Offset Error** - The first transition should occur at a level 1/2LSB above "zero". Offset is defined as the deviation of the actual first code transition from that point.

**4. Gain Error** - The first code transition should occur for an analog value 1/2LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

**5. Pipeline Delay (Latency)** - The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

**6. Effective Number of Bits (ENOB)** - This is a measure of a device's dynamic performance and may be obtained from the SNDR or from a sine wave curve test fit according to the following expression:

$$\text{ENOB} = \text{SNDR} - 1.76/6.02$$

$$\text{ENOB} = N - \log_2[\text{RMS error (actual)} / \text{RMS error (ideal)}]$$

**7. Analog Bandwidth** - The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

**8. Aperture Delay** - The delay between the sampling clock and the instant the analog input signal is sampled.

**9. Aperture Jitter** - The sample to sample variation in aperture delay.

**10. Bit Error Rate (BER)** - The number of spurious code errors produced for any given input sine wave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sine wave.

**11. Signal to Noise Ratio** - This signal to noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half the sampling frequency, this signal to noise ratio must be specified and should ideally follow the theoretical formula;

$$\text{S/N}_{\text{max}} = 6.02N + 1.76\text{dB}$$



### 3. Phase Locked Loop

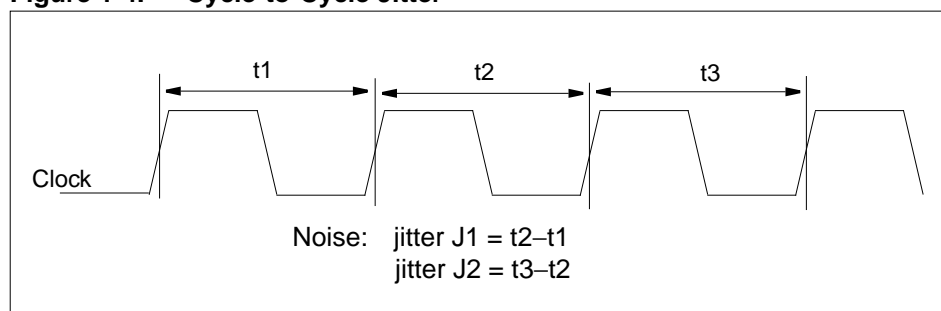
**1. Lock Time** - The time it takes the PLL to lock onto the system clock. Fast or slow lock time may be controlled by the loop filter characteristics. The loop filter characteristics are controlled by varying the R and C components. (Remember that R and C define the damping-factor as well)

**2. Phase Error** - The phase difference between the feedback clock signal and the system signal clock.

**3. Clock Jitter** - The deviations in a clock's output transitions from their ideal positions define the clock jitter. Jitter is sometimes specified as an absolute value in nanoseconds. All jitter measurement are made at a specified voltage.

1) Cycle-to-Cycle Jitter: The change in a clock's output transition from its corresponding position in the previous cycle. This kind of jitter is the most difficult to measure and usually requires a time-interval analyzer

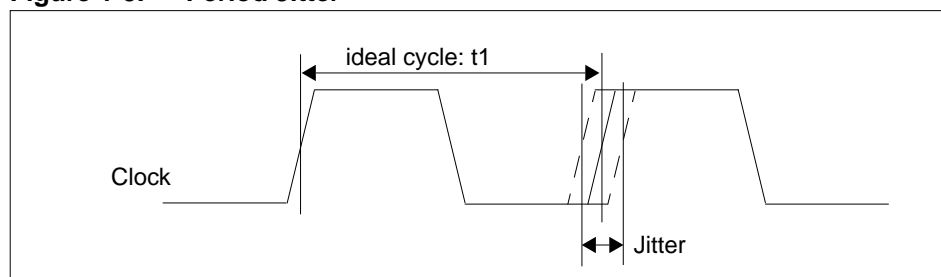
**Figure 1-4. Cycle-to-Cycle Jitter**



: The maximum of such values over multiple cycles ( $J1, J2, \dots$ ) is the max. cycle-to-cycle jitter.

2) Period Jitter: Period jitter measures the maximum change in a clock's output transition from its ideal position. You can use period-jitter measurements to calculate timing margins in systems.

**Figure 1-5. Period Jitter**



3) Long-term Jitter: Long-term jitter measures the maximum change in a clock's output transition from its ideal position over many cycles. How many cycles depends on the application and the frequency. A classic example of system affected by long-term jitter is a graphics card driving a CRT

4) Power Down Mode: PLL state in which the quiescent current is lowered to a very low level to conserve power.

5) Synthesize clock: a system clock may run at a relatively low rate compared to system components. A CPU, for example, may require an internal clock that is several times faster than the system I/O bus clock. Designers can use PLL



technology to synthesize a higher frequency on-chip clock using the system clock as a reference.

6) Deskew clock: Multiple chips on a printed circuit board or cores of different sizes within a single system on a chip experience clock skew. By using PLL or DLL technology to shift the phase of the reference clock within each chip or core, designers can minimize skew tune a system to perform up its potential.

7) Duty Ratio: the percentage of the period that the output is in a high state.

8) Output frequency range: The maximum output frequency range minus the minimum output frequency that is produced with an input signal for which the cell specifications still apply.

### **Customer Service**

SEC provides a full custom support for our customers need of analog cores. SEC's worldwide sales offices and representatives give our customers a first-hand support for analog cores. And if needed, SEC engineers are prepared to provide a fully customized total solution to satisfy our customers.

### **Technical Support**

If our customers want to develop mixed-signal products, SEC provides all technical support to meet customers needs. Mixed-signal design is quite different from pure logic design in terms of circuit design, techniques, layout and test methodology. Thus SEC provides a successful technical guide and firmly support for all development steps.

### **Definition of Analog Core Data Sheet Types**

Each product developed by SEC will be supported by technical literature where the data sheets progress through the following levels of refinement

#### **1. Core Preview**

Describes the main features and specifications for core that is under development. Some specifications such as exact pin-outs may not be finalized at time of publication. The purpose of this document is to provide customers with advance product planning information.

#### **2. Preliminary Datasheet**

This is the first document completely describing a new core. It contains an features, application, timing diagram, theory of operation, core pin information, test guide, layout guide and AC/DC electrical information. This data sheet are based on prototype silicon performance and on worst case simulation models. The purpose of this data sheet is to provide ASIC customer with technical information sufficiently detailed to guarantee that they can safely begin active development.

#### **3. Final Data sheet**

This is an updated version of preliminary data sheet reflecting actual performance of the final silicon. Updates include tighter specifications, more min. and max. values. The purpose of this data sheet is to communicate the confirmed performance of cores which have passed qualification, been fully characterized.



### 1.4.2 INTERNAL MACROCELLS

Internal Macrocells are the lowest level of logic functions such as NAND, NOR and flip-flop used for logic designs. There are about 471 different types of internal macrocells. They usually come in four levels of drive strength (0.5X, 1X, 2X and 4X).

These macrocells have many levels of representations—logic symbol, logic model, timing model, transistor schematic, HSPICE netlist, physical layout, and placement and routing model.

### 1.4.3 COMPILED MACROCELLS

Compiled macrocells of STD110 consist of compiled memory and compiled datapath macrocells.

#### 1.4.3.1 Compiled Memory Macrocells

Memories in STD110 are fully user-configurable and are provided as a compiler. Two different types of memories are available in STD110. One is suitable for high-density application with high-performance, called STD110-HD compiled memory. The other is suitable for low-power application, called STD110-LP compiled memory.

In STD110-HD compiled memory, eight types of memories are available such as single-port synchronous/asynchronous static RAM, dual-port synchronous static RAM, synchronous diffusion/metal-programmable ROM, multi-port asynchronous register file and synchronous first-in first-out memory. Synchronous memories have a fully synchronous operation at the rising-edge of clock and the duty-free cycle is available. Also, the bit-write capability is available. Asynchronous memories have a synchronous operation for a write enable signal during write mode and have an asynchronous operation for address signal during read mode. Multi-port asynchronous register file supports four kinds of configurations such as 2 port(1-read/1-write), 3 port(1-read/2-write and 2-read/1-write) and 4 port (2-read/2-write). The first-in first-out memory which is widely used in communication buffering types of applications has also fully synchronous operation at the rising- edge of clock.

On the other hand, in STD110-LP compiled memory, five types of memories are available such as single-port synchronous/asynchronous static RAM, dual-port synchronous static RAM and synchronous diffusion/metal-programmable ROM. Synchronous memories are almost same as that of STD110-HD except that the duty-free cycle is not available. Asynchronous memory is same as that of STD110-HD.

To dramatically reduce the power consumption in STD110-LP, some of low-power techniques such as a partial activation architecture in cell array and a divided word-line structure was adopted, rather than STD110-HD.

Basically in STD110-HD and STD110-LP, the power-down mode which significantly reduces the power dissipated during a read or write mode is provided. Also compiled memories have a standby mode except multi-port asynchronous register file and first-in first-out memory. While in standby mode, the data stored in the memory is retained, data outputs remain stable and the power is greatly reduced because memory operation is internally blocked while the memory contents and the data outputs are unaffected.



To improve the memory performance and to reduce the power consumption, 2-bank architecture is provided except some memories such as dual-port synchronous static RAM, multi-port asynchronous register file and first-in first-out memory. In 2-bank architecture, only one bank is activated and the other bank is in standby mode.

To support various memory shapes which are determined by the floorplan of a chip design, flexible memory aspect ratios are provided. For certain specific memory configuration, all types of timing, power and area values are provided by an automatic datasheet generator.

To easily do interface to layout, the physical abstract data for Silicon Ensemble and Apollo, called phantom cell or black box, is provided. BIST(Built-In Self-Test) circuitry is currently available for most of STD110 compiled memories. BIST circuits are designed to detect a set of fault types that impact the functionality of memory and is generated by a softmacro-based BIST generator.

The softmacro-based BIST generator generates both an individual BIST netlist for each memory and a shared BIST netlist for all memories used in a design. However, when several memories of the same or the different type area used in the design, if you generate the individual BIST netlist for each memory, there are some redundant blocks because the individual BIST netlist has same function. In this case, it would better use the shared BIST netlist to eliminate such redundancy and reduce area.

#### **1.4.3.2 Compiled Datapath Macrocells**

Compiled datapath macro cells include Adder, Barrel Shifter and Multiplier. Adder performs the adding or adding/subtracting operation on the control of a mode selection signal. Barrel Shifter makes input data shift or rotate in the left/right direction. In the shift operation, the vacant bit can be padded with zero, MSB value, or external data. Multiplier performs the 2's compliment multiplication. One pipeline stage insertion is available to get a high operating frequency.

They have two output drive strengths, which are equal to the 1X and 2X-Drive in the primitive cell library. The hard macro cells are built through the Apollo, placement and routing tool from Avant!. All the leaf cells have the same physical configuration compatible with the primitive cell library. It allows that any primitive cell can be used as a bit slice cell in the datapath module design.

We provide two kinds of engineering design services. One is to support additional compiled datapath macrocells such as ALUs, Comparators, Priority encoders, Incrementers and Decrementers, and so on. Another is to make hardwired datapath module design which provides a regular structured layout.



### 1.4.4 INPUT/OUTPUT CELLS

There are about seven hundreds different I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of a chip.

A test logic is provided to enable the efficient parametric (threshold voltage) testing on input buffers including LVCMOS and TTL level converters, Schmitt trigger input buffers, clock drivers and oscillator buffers. Pull-up and pull-down resistors are optional features.

Three basic types of output buffers (non-inverting, tri-state and open drain) are available in a range of driving capabilities from 1mA to 12mA for 2.5V, 3.3V drive and from 1mA to 3mA for 5.0V tolerant drive. One or two levels of slew rate controls are provided for each buffer type (except 1mA, 2mA and 3mA buffers) to reduce output power/ground noise and signal ringing, especially in simultaneous switching outputs.

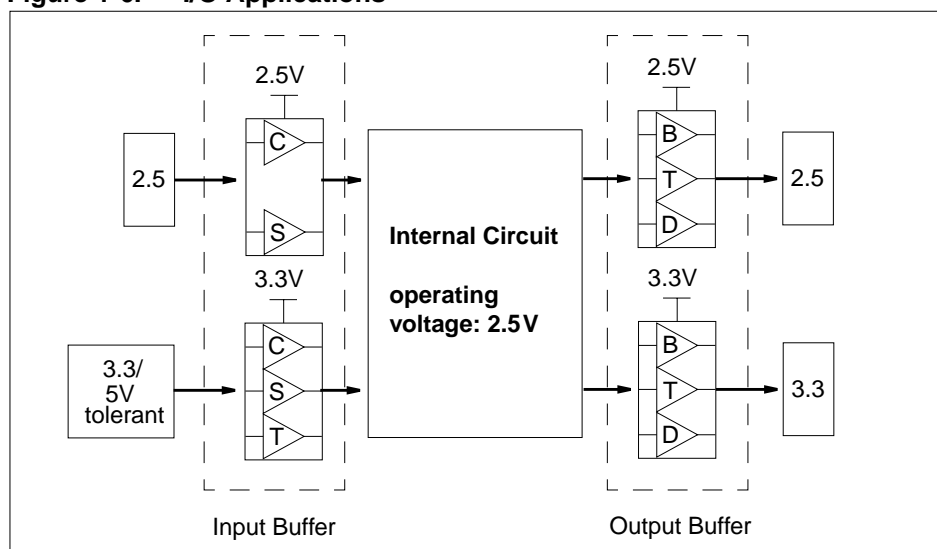
Bi-directional buffers are combinations of input buffers and output buffers (tri-state and open drain) in a single unit. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

For user's convenience, STD110 library provides 100K $\Omega$  pull-down and pull-up resistance respectively.

#### 1.4.4.1 I/O Applications

To support mixed voltage environments, LVTTTL, LVCMOS and Schmitt trigger I/O cells are available at 2.5V, 3.3V interface and 5V tolerant interface. The I/O application diagram is as follows.

**Figure 1-6. I/O Applications**



#### 1.4.4.2 I/O Cell Drives Options

To provide designers with the greater flexibility, each I/O buffer can be selected among various current levels (e.g., 1mA, 2mA,..., 12mA). The choice of current-level for I/O buffers affects their propagation delay and current noise.

The slew rate control helps decrease the system noise and output signal overshoot/undershoot caused by the switching of output buffers. The output edge rate can be slowed down by selecting the high slew rate control cells.



STD110 provides three different sets of output slew rate controls. Only one I/O slot is required for any slew rate control options.

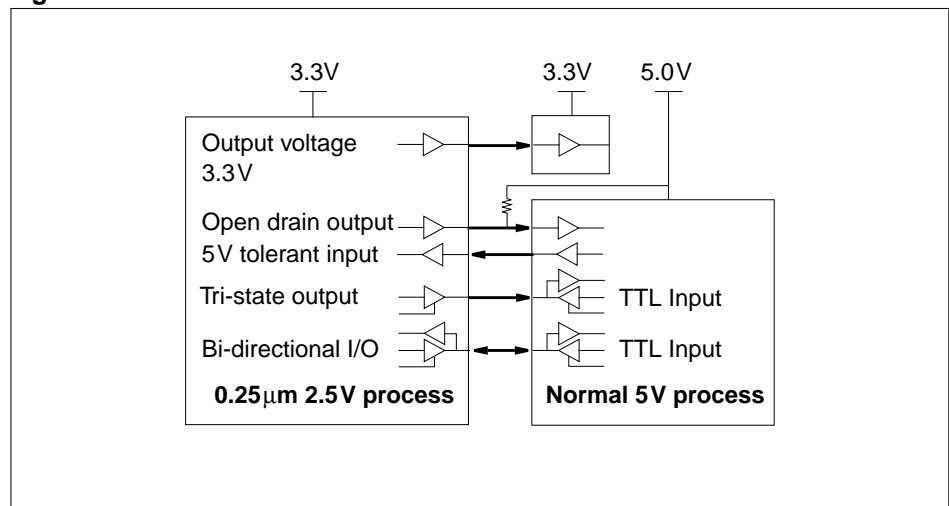
#### 1.4.4.3 5V Tolerant I/O Buffers

STD110 I/O library is based on a process which has the most optimum performance in 2.5V.

In this process, voltage more than 3.6V are not allowed at the gate oxide because of a reliability problem. And a special circuit is adopted in order to make pin voltage tolerable up to 5.25V and to offer TTL interface driving up to 3mA. Obviously, this circuit is constructed not to permit more than 3.6V at the gate oxide. The external circuit diagram is as follows.

The maximum external tolerance of this buffer is 5.25V. It can be used as a 3.3V normal buffer.

**Figure 1-7. 5V Tolerant I/O Buffers**



#### 1.4.4.4 PCI Buffers

PCI buffers are designed for PCI local bus application which is an industry-standard, high-performance 32bit or 64bit bus architecture. SEC ASIC offers input, output, bi-directional PCI buffers for 33MHz and 66MHz operation. These buffers are compliant with PCI local bus specification 2.1.

#### 1.4.4.5 USB (Universal Serial Bus) Buffers

Various kinds of peripheral equipment such as mouse, joy stick, keyboard, modem, scanner and printer improve the power of a computer. However, it is not easy to connect and use them properly in the computer.

USB specification established late in 1995 is a good solution for this problem, providing facile method of an expansion. SEC ASIC offers full speed and low speed USB buffers that complies with Universal Serial Bus specification 1.0, 1.1.

#### 1.4.4.6 Other Buffers

SEC ASIC can support various kinds of buffers such as HSTL, SSTL, AGP, PECL, LVDS, and so on. For more information please contact us.



## 1.5 Timings

### 1.5.1 WIRE LENGTH LOAD

Table 1-1. shows the equivalent standard load matrix for 4-layer and 5-layer metal interconnect. The equivalent standard load values are function of gate count and fanout. These values are based on capacitive loading and are used in wire length estimates which affect propagation delay.

**Table 1-1. Equivalent Standard loads for 4-layer and 5-layer Metal Interconnect**

Gates Count	Fanouts										
	1	2	3	4	5	6	7	8	16	32	64
<b>4LM</b>											
5000	1.159	2.242	3.822	5.113	5.965	7.020	7.859	10.94	28.672	45.642	79.821
10000	1.530	2.932	5.561	7.701	8.964	10.500	12.110	15.211	29.903	47.725	83.520
50000	4.192	8.247	12.439	16.494	16.801	17.980	21.026	22.806	35.536	48.347	84.605
100000	4.596	9.327	13.925	18.523	18.889	20.241	23.582	27.031	41.002	54.253	94.944
150000	12.843	17.125	21.406	22.684	23.600	24.296	26.001	29.730	39.828	63.672	127.344
200000	13.520	18.026	22.533	23.885	24.849	25.582	27.372	31.299	41.865	66.931	133.812
300000	14.871	19.830	24.786	26.588	27.596	28.363	30.317	34.634	46.268	73.871	147.587
400000	16.225	21.631	26.852	28.693	29.845	30.718	32.868	37.479	50.016	79.707	159.207
500000	18.099	24.132	30.166	32.177	33.435	34.390	36.777	42.032	53.235	84.861	169.459
600000	19.375	25.836	32.476	34.593	35.915	36.919	39.467	45.186	54.763	87.312	174.320
800000	22.324	29.767	37.739	40.113	41.593	42.719	45.642	52.399	59.180	94.390	188.385
1000000	25.078	33.439	42.657	45.272	46.898	48.140	51.408	59.135	63.283	100.964	201.447
1500000	32.631	43.509	56.047	59.341	61.381	62.946	67.174	77.514	75.639	120.743	240.788
2000000	39.706	52.941	68.596	72.524	74.956	76.821	81.946	94.736	87.196	139.244	277.587
2500000	46.327	61.770	80.342	84.864	87.657	89.807	95.771	110.853	97.994	156.527	311.959
3000000	52.517	70.023	91.321	96.399	99.532	101.946	108.693	125.919	108.065	172.646	344.022
4000000	60.251	80.335	104.770	110.594	114.189	116.958	124.701	144.463	123.979	198.073	394.685
5000000	67.558	90.078	117.479	124.008	128.041	131.146	139.827	161.985	139.017	222.099	442.560
6000000	75.754	101.005	131.728	139.052	143.573	147.053	156.788	181.634	155.879	249.038	496.241
<b>5LM</b>											
5000	1.101	2.131	3.631	4.856	5.667	6.669	7.466	10.397	27.238	43.360	75.830
10000	1.454	2.786	5.283	7.317	8.515	9.976	11.505	14.451	28.408	45.339	79.344
50000	3.982	7.834	11.818	15.670	15.961	17.081	19.976	21.666	33.760	45.929	80.374
100000	4.366	8.861	13.229	17.597	17.944	19.229	22.403	25.679	38.952	51.540	90.198
150000	12.201	16.268	20.336	21.549	22.420	23.081	24.701	28.244	37.837	60.488	120.977
200000	12.843	17.125	21.406	22.691	23.606	24.304	26.004	29.734	39.771	63.584	127.122
300000	14.128	18.839	23.546	25.259	26.216	26.944	28.801	32.903	43.955	70.178	140.207
400000	15.414	20.549	25.509	27.257	28.353	29.181	31.225	35.606	47.515	75.722	151.247
500000	17.195	22.925	28.658	30.567	31.763	32.670	34.938	39.931	50.573	80.618	160.986
600000	18.406	24.543	30.852	32.862	34.119	35.073	37.494	42.926	52.025	82.947	165.605
800000	21.208	28.278	35.852	38.107	39.514	40.584	43.360	49.779	56.220	89.670	178.967
1000000	23.825	31.767	40.524	43.008	44.554	45.733	48.837	56.178	60.119	95.916	191.374
1500000	31.000	41.333	53.245	56.374	58.312	59.798	63.815	73.637	71.856	114.706	228.749
2000000	37.721	50.295	65.166	68.898	71.208	72.980	77.849	90.000	82.837	132.281	263.707
2500000	44.011	58.682	76.324	80.621	83.274	85.317	90.983	105.311	93.093	148.700	296.362
3000000	49.891	66.523	86.755	91.579	94.555	96.849	103.257	119.622	102.661	164.014	326.821
4000000	57.239	76.318	99.532	105.065	108.479	111.110	118.466	137.239	117.779	188.169	374.950
5000000	64.180	85.575	111.606	117.807	121.639	124.588	132.836	153.885	132.067	210.995	420.432
6000000	71.965	95.955	125.141	132.099	136.394	139.700	148.949	172.552	148.084	236.587	471.429
7000000	78.436	104.582	136.393	143.976	148.655	152.259	162.339	188.067	161.397	257.858	513.812
8000000	87.950	117.266	152.935	161.439	166.687	170.727	182.031	210.877	180.976	289.134	576.135



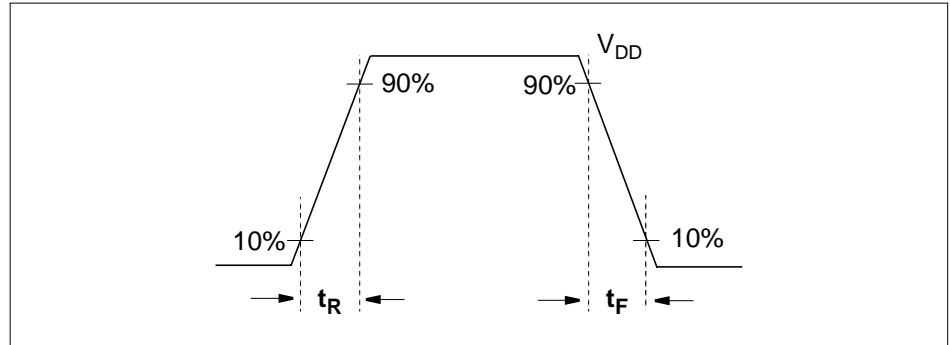
### 1.5.2 TIMING PARAMETER

This section discusses issues involving timing parameters.

#### 1.5.2.1 Transition Time

Figure 1-8. shows the definition of rise transition time ( $t_R$ ) and fall transition time ( $t_F$ ). Transition time is defined as the delay between the time when the input (output) signal voltage level is 10% of supply voltage ( $V_{DD}$ ) and the time of the input (output) signal voltage level is 90% of  $V_{DD}$ .

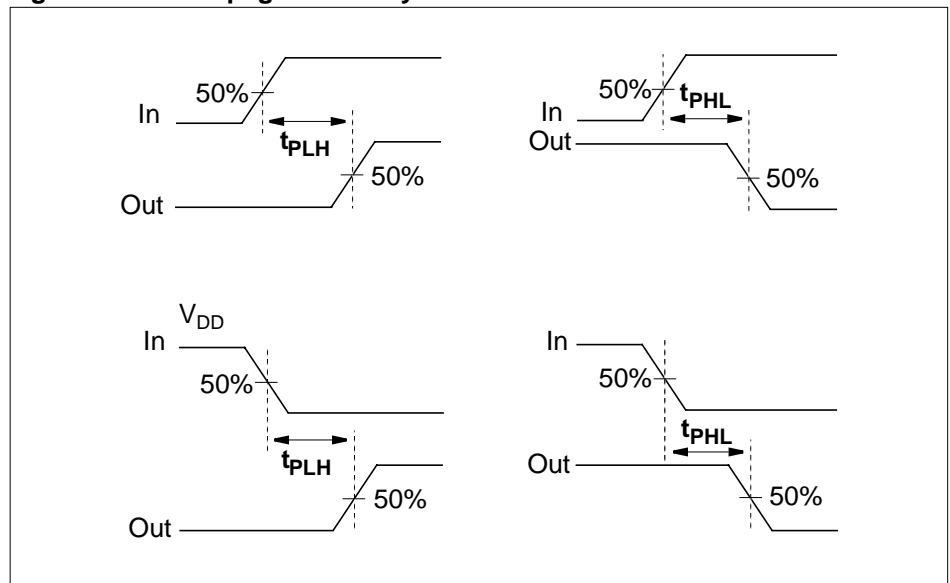
**Figure 1-8. Rise and Fall Transition Time**



#### 1.5.2.2 Propagation Delay

Figure 1-9. shows the definition of propagation delays. Propagation delay is defined as the delay between the time when the input signal voltage level is 50% of supply voltage ( $V_{DD}$ ) and the time when the output signal voltage level is 50% of  $V_{DD}$ .

**Figure 1-9. Propagation Delay**



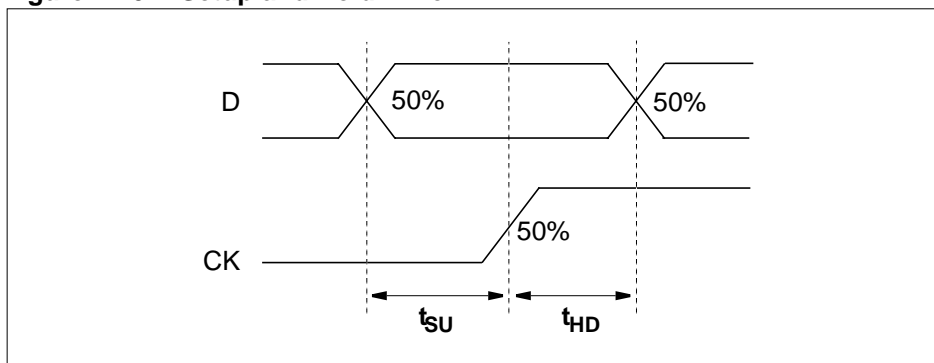


### 1.5.2.3 Setup / Hold Time

Figure 1-10. shows the definition of setup time and hold time. The setup timing check is defined as the minimum interval which a data signal must remain stable before active transition of a clock. Any change to the data signal within this interval results in a timing violation.

The hold timing check is defined as the minimum interval which a data signal must remain stable after active transition of a clock. Any change to the data signal within this interval results in a timing violation.

**Figure 1-10. Setup and Hold Time**

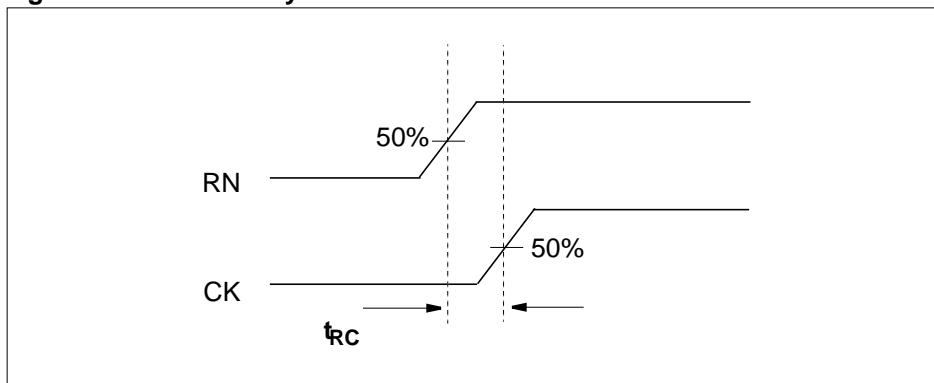


### 1.5.2.4 Recovery Time

Figure 1-11. shows the definition of recovery time. A recovery timing check measures the time between the release of an asynchronous control signal from the active state to the next active clock edge.

For example, the time between RN and the CK of FD2 cell. If the active edge of the CK occurs too soon after the release of the RN, the state of the FD2 becomes uncertain. The state can be the value set by the RN or the value clocked into the FD2 from the data input.

**Figure 1-11. Recovery Time**



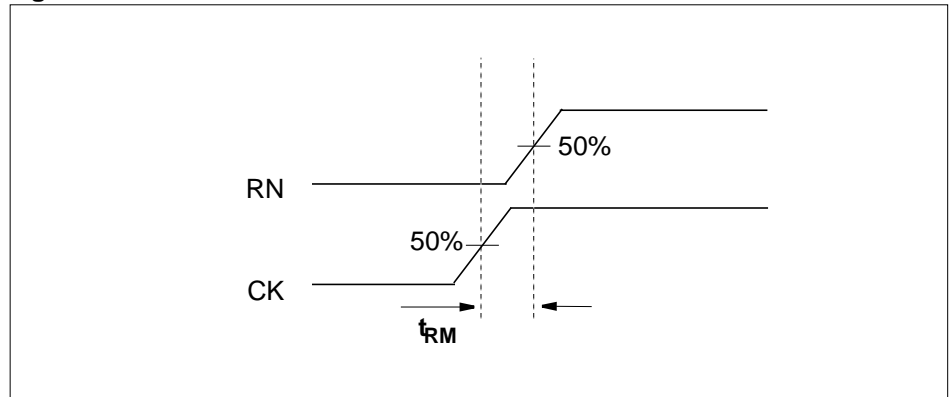


### 1.5.2.5 Removal Time

Figure 1-12. shows the definition of removal time. A removal timing check measures the time between the active clock edge and the release of an asynchronous control signal from the active state.

For example, the time between RN and the CK of FD2 cell. If the release of the RN occurs too soon after the active edge of the clock, the state of the FD2 becomes uncertain. The uncertainty can be caused by the value set by the RN or the value clocked into the FD2 from the data input.

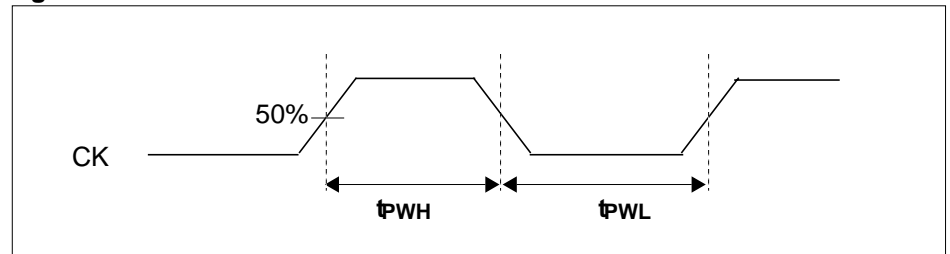
**Figure 1-12. Removal Time**



### 1.5.2.6 Minimum Pulse Width

Figure 1-13. shows the definition of minimum pulse width. The minimum pulse width timing check is the minimum allowable time for the positive (high) or negative (low) phase of each cycle.

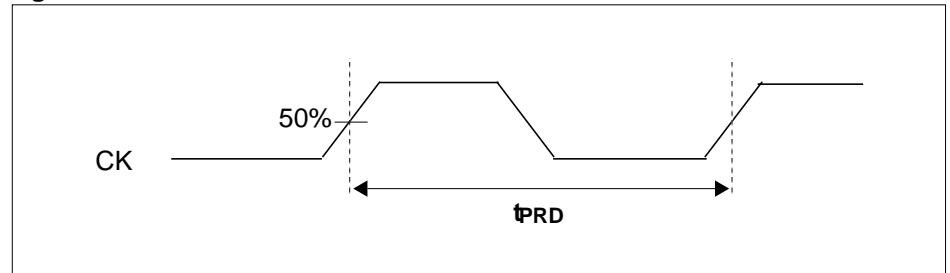
**Figure 1-13. Minimum Pulse Width**



### 1.5.2.7 Minimum Period

Figure 1-14. shows the definition of minimum period. The minimum period timing check is the minimum allowable time for one complete cycle of the signal.

**Figure 1-14. Minimum Period**



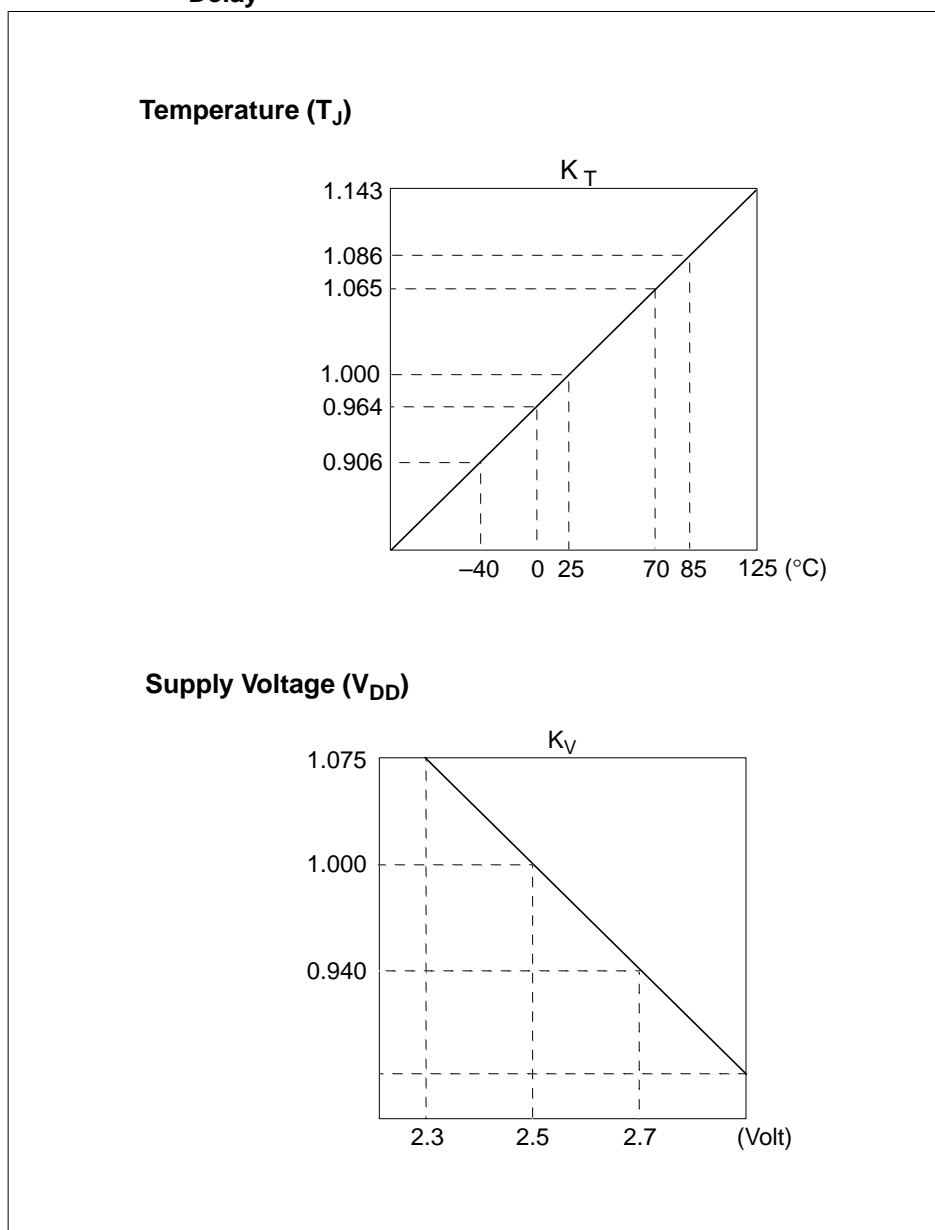


### 1.5.3 TEMPERATURE AND SUPPLY VOLTAGE

The next figure describes propagation delay derating factors ( $K_T$ ,  $K_V$ ) as a function of on-chip junction temperature ( $T_J$ ) and supply voltage ( $V_{DD}$ ). As a result of power dissipation, the junction temperature is generally higher than the ambient temperature.

The temperature of the die inside the package (junction temperature,  $T_J$ ) is calculated using chip power dissipation and the thermal resistance to the ambient temperature ( $\theta_{JA}$ ) of the package. Information on package thermal performance can be obtained from SEC application engineers.

**Figure 1-15. Effect of Temperature and Supply Voltage on Propagation Delay**





### 1.5.4 BEST AND WORST CASE CONDITIONS

A circuit should be designed to operate properly within a given specification level, either commercial or industrial. It is recommended that circuits be simulated for best case, normal case, and worst case conditions at each specification level.

The following expressions also allow for the effect of process variation on circuit performance.

Best case(Worst case):

$$T_{BC} (T_{WC}) = K_P \times K_T \times K_V \times T_{NOM}$$

where

$T_{BC}$  = Best case propagation delay

$T_{WC}$  = Worst case propagation delay

$T_{NOM}$  = Normal propagation delay

( $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 2.5\text{V}$  and typical process)

$K_P$ ,  $K_T$ ,  $K_V$  = Refer to Table 1-2., Table 1-3., and Table 1-4.

### 1.5.5 DERATING FACTORS OF STD110

The multipliers can be applied to nominal delay data in order to estimate the effects of supply voltage, temperature and process. Nominal data are provided for conditions of  $V_{DD} = 2.5\text{V}$ ,  $T_J = 25^\circ\text{C}$  and typical process.

The derating factors of STD110 is as follows.

**Table 1-2. STD110 cell process derating factor ( $K_P$ )**

Process Factor ( $K_P$ )	Slow	Typ	Fast
	1.212	1.0	0.841

**Table 1-3. STD110 cell temperature derating factor ( $K_T$ )**

Temp. ( $^\circ\text{C}$ )	125	85	70	25	0	-40
$K_T$	1.143	1.086	1.065	1.000	0.964	0.906

**Table 1-4. STD110 cell voltage derating factor ( $K_V$ )**

Voltage (V)	2.3	2.5	2.7
$K_V$	1.075	1.000	0.940



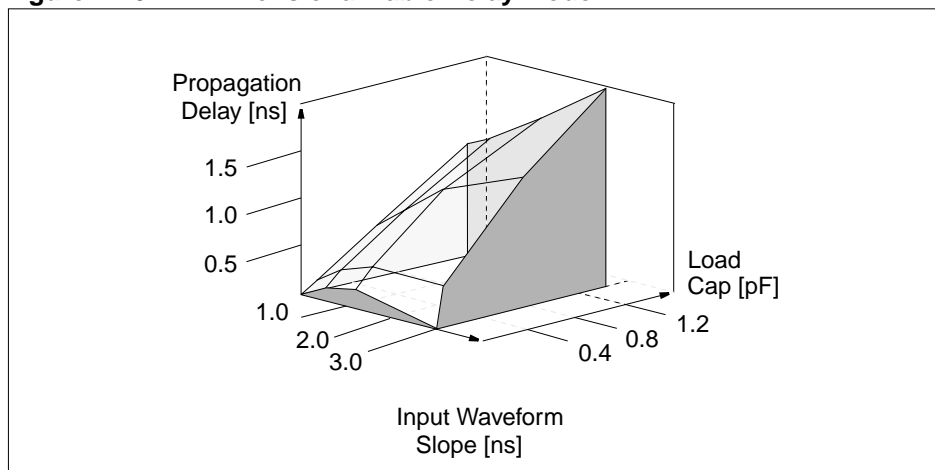
## 1.6 Delay Model

The ASIC timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout loads and distributed interconnection wire resistance and capacitance.
- Interconnection wire delay across the metal lines.
- Timing requirement parameters such as setup time, hold time, recovery time, skew time, minimum pulse width, etc.
- Derating factors for junction temperature, power supply voltage, and process variations.

Timing model for STD110 focuses on how to characterize cell propagation delay time accurately. To accomplish this goal, 2-dimensional table look-up delay model has been adopted. The index variables of this table are input waveform slope and output load capacitance. See the figure below. SEC ASIC design automation system supports an n-dimensional table model even though we adopted 2-dimensional model for our 0.25 $\mu$ m cell-based products.

**Figure 1-16. 2-Dimensional Table Delay Model**





The Table 1-5. shows an example of this model for 2-input NAND cell. The data in this table are high-to-low transition delay times from one of the two input pins to output pin. The number of points and values of the index variables can differ for each cell.

**Table 1-5. Table Delay Model Example**

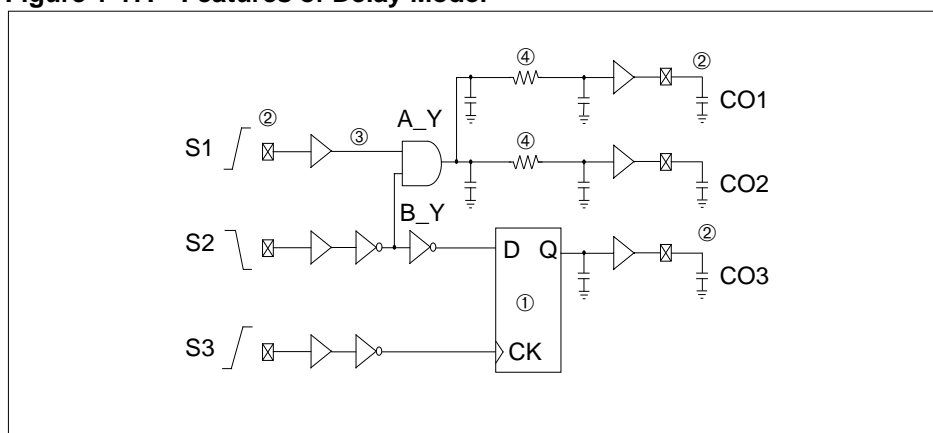
SLOP \ CAP	0.0050	0.0220	0.3030	0.5840
0.0200	0.03644	0.07275	0.66481	1.25660
0.1700	0.05508	0.09725	0.68658	1.27820
1.5850	0.07719	0.16698	0.92337	1.49790
3.0000	0.06421	0.17730	1.10970	1.74950

Notice that 4-by-4 table is used. Delay values between grid points and beyond this table are determined by linear interpolation and extrapolation methods. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a commonly-accepted way in industry.

The figure below summarizes the features of SEC ASIC's delay model.

- ① 2-dimensional table delay model for output loading and input waveform slope effects is used. The slopes ( $t_R$ ,  $t_F$ ) and delay times ( $t_{PLH}$ ,  $t_{PHL}$ ) of all cell instances are calculated recursively.
- ② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.
- ③ Pin to pin delays of cells and interconnection wires are supported.
- ④ The effect of distributed interconnection wire resistance and capacitance on cell delay is analysed using the effective capacitance concept.

**Figure 1-17. Features of Delay Model**





## 1.7 Testability Design Methodology

### 1.7.1 SCAN DESIGN

- Multiplexed scan flip-flop that minimizes the area or delay overhead needed to implement scan design.
- Automated design rules checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

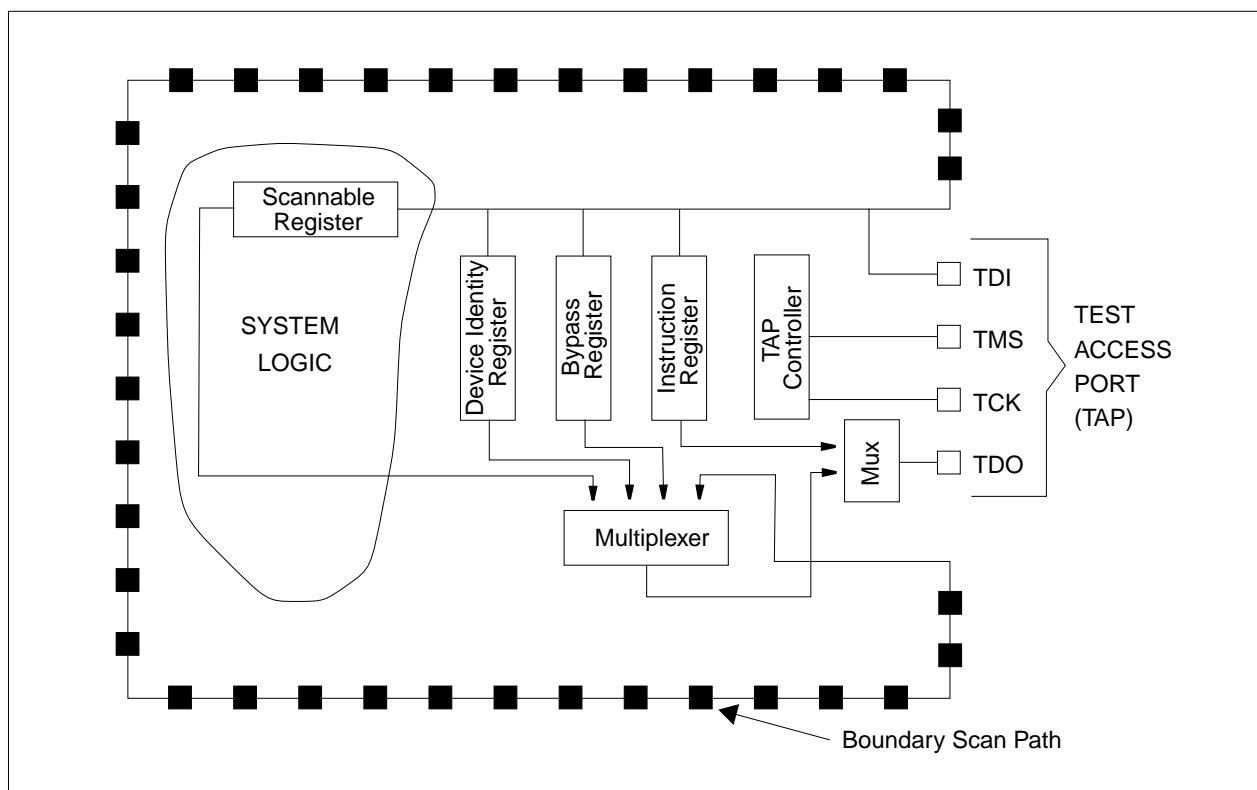
### 1.7.2 BOUNDARY-SCAN

- IEEE Std 1149.1
- JTAG boundary-scan registers with primitive cells
- Boundary-Scan Description Language (BSDL) description for board testing
- Combination with internal scan design and core testing

#### Boundary Scan Architecture

A boundary scan architecture contains TAP (Test Access Port), TAP controller, instruction register and a group of test data registers. The instruction and test data registers are separate shift-register-based paths connected in parallel with a common serial data input and a common serial data output which are connected to TAP, TDI and TDO signals. TAP controller selects the alternative instruction and test data register paths between TDI and TDO. The schematic view of the top level design of the test logic architecture is shown in the Figure 1-18.

Figure 1-18. JTAG Test Access Port (TAP) Block Diagram





## Boundary Scan Functional Block Descriptions

### TAP (Test Access Port)

TAP is a general-purpose port that can provide with an access to many test support functions built into a component, including the test logic. It includes three inputs (TCK; Test Clock Signal, TMS; Test Mode Signal and TDI; Test Data Input) and one output (TDO; Test Data Output) required by the test logic. An optional fourth input (TRSTN; Test Reset) is provided for the asynchronous initialization of the test logic. The values applied at TMS and TDI pins are sampled on the rising edge of TCK, and the value placed on TDO pin changes on the falling edge of TCK.

### TAP Controller

TAP controller receives TCK, interprets the signals on TMS, and generates clock and control signals for both instruction and test data registers and for other parts of the test circuitries as required.

### Instruction Register/Instruction Decoder

Test instructions are shifted into and held by the instruction register. Test instructions include a selection of tests to be performed or the test data register to be accessed. A basic 3-bit instruction register and its instruction decoder are provided as macrofunctions in the library.

### Test Data Registers

Data registers include a bypass register, a boundary scan register, a device identification register and other design specific registers. Only the bypass- and boundary scan registers are mandatory; the rest are optional.

**Bypass register:** The bypass register provides a single-bit serial connection through the circuit when none of the other test data registers is selected. It can be used to allow test data to flow through a given device to the other components in a product without affecting a normal operation.

**Boundary scan register:** The boundary scan register detects typical production defects in board interconnects, such as opens, shorts, etc. It also allows an access to component inputs and outputs when you test their logic or sample flow-through signals. Special boundary scan register macrocells are provided for this purpose. These special registers is discussed in the next section of next pages.

**Design-specific test data register:** These optional registers may be provided to allow an access to design-specific test support features in the integrated circuit, such as self-test, scan test.

**Device identification register:** This is an optional test data register that allows the manufacturer part number and variant of a components to be identified. The 32-bit identification register is partitioned into four fields:

Device version identifier	1st field	The first four bits beginning from MSB
Device part number	2nd field	16 bits
Manufacturer's JEDEC number	3rd field	11 bits
LSB	4th field	1 bit —tied in High



The ASIC designer is free to fill the version and part number in any manner as long as the total twenty bits are used.

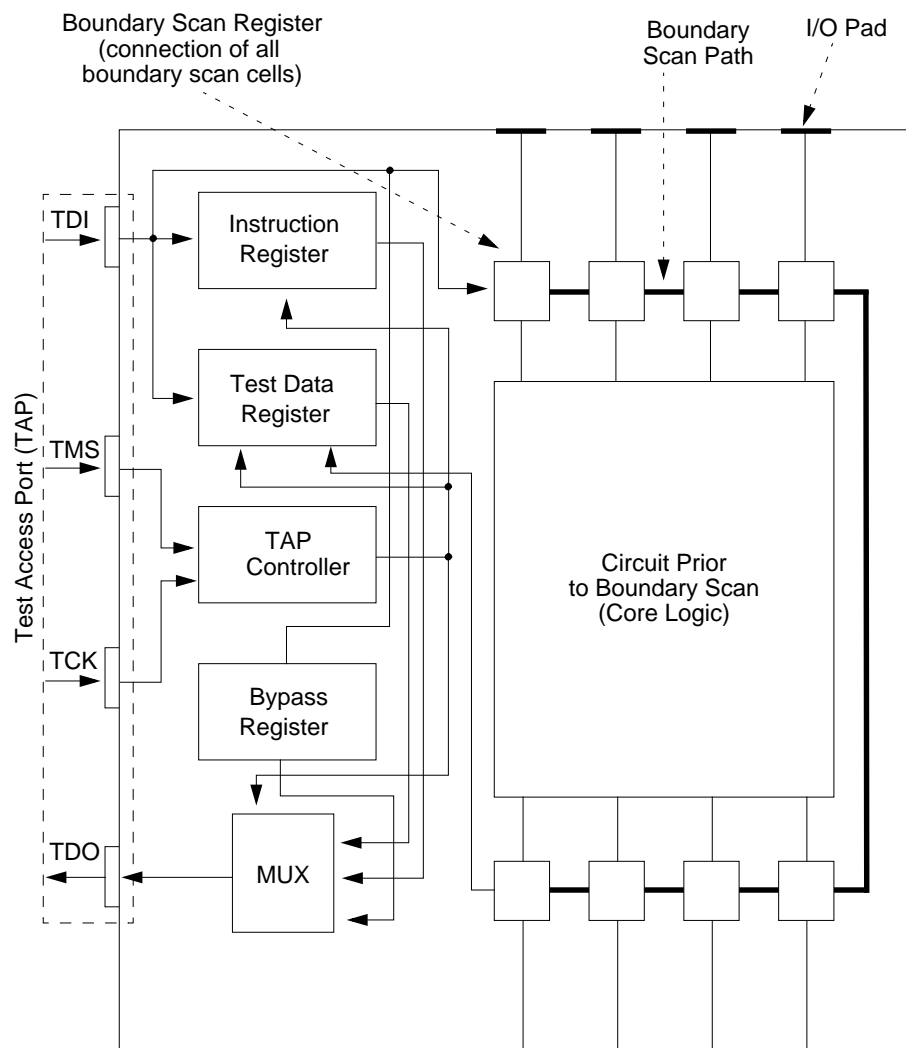
SEC's JEDEC code: 78 decimal = 1001110

Continuation field (4 bits) = 0000

Contents of device identification register:

XXXX XXXXXXXXXXXXXXXX 0000 1001110 1

Users can define these two fields.



### 1.7.3 BIST (BUILT-IN SELF-TEST)

- Efficient test solution for compiled memory macrocells
- At speed and parallel testing of multiple memories
- Less routing overhead and test pin requirements



## 1.8 Maximum Fanouts

### 1.8.1 INTERNAL MACROCELLS

The maximum fanouts for STD110 primitive cells are as follows. Note that these fanout limitation values are calculated when the rise and fall times of the input signal is 0.213ns. Depending on the rise and fall times, the maximum fanout limitations can be varied case by case.

In the following table the maximum fanout values for all pins of STD110 internal macrocells are listed.

**Table 1-6. Maximum Fanouts of Internal Macrocells**

(When input  $t_R/t_F = 0.213\text{ns}$ , one fanout (SL) = 0.006710pF)

Cell Name	Output Pin	Maximum Fanout
ad2	Y	48
ad2d2	Y	97
ad2d4	Y	190
ad2dh	Y	21
ad3	Y	48
ad3d2	Y	94
ad3d4	Y	188
ad3dh	Y	21
ad4	Y	48
ad4d2	Y	94
ad4d4	Y	185
ad4dh	Y	21
ad5	Y	23
ad5d2	Y	46
ad5d4	Y	190
ao21	Y	22
ao211	Y	14
ao2111	Y	9
ao2111d2	Y	97
ao211d2	Y	28
ao211d2b	Y	97
ao211d4	Y	195
ao211dh	Y	7
ao21d2	Y	45
ao21d2b	Y	95
ao21d4	Y	192
ao21dh	Y	10
ao22	Y	22
ao221	Y	13
ao221d2	Y	95
ao221d4	Y	192
ao222	Y	13
ao2222	Y	8
ao2222d2	Y	95
ao2222d4	Y	192
ao222a	Y	20
ao222d2	Y	25
ao222d2a	Y	95
ao222d2b	Y	95
ao222d4	Y	191
ao222d4a	Y	192
ao22a	Y	22

Cell Name	Output Pin	Maximum Fanout
ao22d2	Y	43
ao22d2a	Y	43
ao22d2b	Y	96
ao22d4	Y	191
ao22d4a	Y	191
ao22dh	Y	9
ao22dha	Y	9
ao31	Y	21
ao311	Y	13
ao3111	Y	8
ao3111d2	Y	97
ao311d2	Y	97
ao311d4	Y	191
ao31d2	Y	43
ao31d4	Y	194
ao31dh	Y	9
ao32	Y	20
ao321	Y	12
ao321d2	Y	95
ao321d4	Y	192
ao322	Y	11
ao322d2	Y	95
ao322d4	Y	192
ao32d2	Y	97
ao32d4	Y	191
ao33	Y	19
ao331	Y	11
ao331d2	Y	95
ao331d4	Y	193
ao332	Y	10
ao332d2	Y	95
ao332d4	Y	192
ao33d2	Y	95
ao33d4	Y	190
ao4111	Y	8
ao4111d2	Y	95
busholder	Y	10000
dc4	Y0	47
	Y1	47
	Y2	47
	Y3	47
dc4i	YN0	43
	YN1	43
	YN2	44
	YN3	44
dc8i	YN0	30
	YN1	30
	YN2	30
	YN3	30
	YN4	30
	YN5	30
	YN6	30
	YN7	30
dl1d2	Y	96
dl1d4	Y	195
dl2d2	Y	97
dl2d4	Y	197
dl3d2	Y	96
dl3d4	Y	194
dl4d2	Y	95
dl4d4	Y	194
dl5d2	Y	96
dl5d4	Y	194
dl10d2	Y	96
dl10d4	Y	194



Cell Name	Output Pin	Maximum Fanout
oak_ducclk 10	CK	359
	CKB	358
oak_ducclk 16	CK	359
	CKB	359
fa	S	47
	CO	46
fad2	S	96
	CO	96
fadh	S	20
	CO	20
fd1	Q	47
	QN	47
fd1d2	Q	95
	QN	95
fd1cs	Q	47
	QN	47
fd1csd2	Q	95
	QN	95
fd1q	Q	48
fd1qd2	Q	95
fd1s	Q	47
	QN	47
fd1sd2	Q	97
	QN	95
fd1sq	Q	47
fd1sqd2	Q	95
fd2	Q	47
	QN	48
fd2d2	Q	95
	QN	95
fd2cs	Q	48
	QN	47
fd2csd2	Q	97
	QN	94
fd2q	Q	48
fd2qd2	Q	95
fd2s	Q	46
	QN	48
fd2sd2	Q	95
	QN	95
fd2sq	Q	47
fd2sqd2	Q	95
fd3	Q	48
	QN	48
fd3d2	Q	103
	QN	103
fd3cs	Q	47
	QN	48
fd3csd2	Q	95
	QN	94
fd3q	Q	47
fd3qd2	Q	95
fd3s	Q	48
	QN	48
fd3sd2	Q	95
	QN	95
fd3sq	Q	47
fd3sqd2	Q	95
fd4	Q	47
	QN	48
fd4d2	Q	95
	QN	94
fd4cs	Q	46
	QN	45

Cell Name	Output Pin	Maximum Fanout
fd4csd2	Q	97
	QN	91
fd4q	Q	47
fd4qd2	Q	95
fd4s	Q	47
	QN	46
fd4sd2	Q	95
	QN	94
fd4sq	Q	47
fd4sqd2	Q	94
fd5	Q	47
	QN	47
fd5d2	Q	95
	QN	95
fd5s	Q	47
	QN	47
fd5sd2	Q	97
	QN	95
fd6	Q	47
	QN	48
fd6d2	Q	95
	QN	95
fd6s	Q	46
	QN	47
fd6sd2	Q	95
	QN	95
fd7	Q	48
	QN	48
fd7d2	Q	95
	QN	95
fd7s	Q	47
	QN	48
fd7sd2	Q	95
	QN	95
fd8	Q	47
	QN	46
fd8d2	Q	95
	QN	94
fd8s	Q	48
	QN	48
fd8sd2	Q	95
	QN	94
fds2	Q	47
	QN	46
fds2d2	Q	95
	QN	95
fds2cs	Q	47
	QN	46
fds2csd2	Q	95
	QN	95
fds2s	Q	47
	QN	48
fds2sd2	Q	95
	QN	95
fds3	Q	47
	QN	47
fds3d2	Q	95
	QN	95
fds3cs	Q	48
	QN	47
fds3csd2	Q	95
	QN	95
fds3s	Q	46
	QN	48



Cell Name	Output Pin	Maximum Fanout
fds3sd2	Q	95
	QN	95
fj1	Q	47
	QN	48
fj1d2	Q	95
	QN	95
fj1s	Q	46
	QN	48
fj1sd2	Q	95
	QN	95
fj2	Q	46
	QN	47
fj2d2	Q	95
	QN	95
fj2s	Q	46
	QN	48
fj2sd2	Q	95
	QN	95
fj4	Q	47
	QN	47
fj4d2	Q	94
	QN	96
fj4s	Q	48
	QN	47
fj4sd2	Q	95
	QN	93
ft2	Q	48
	QN	48
ft2d2	Q	94
	QN	94
ha	S	47
	CO	47
had2	S	94
	CO	95
hadh	S	21
	CO	21
iv	Y	48
ivcd11	Y	46
	YN	47
ivcd13	Y	43
	YN	144
ivcd22	Y	94
	YN	97
ivcd26	Y	87
	YN	284
ivcd44	Y	191
	YN	196
ivd2	Y	97
ivd3	Y	144
ivd4	Y	195
ivd6	Y	282
ivd8	Y	381
ivd16	Y	787
ivdh	Y	21
ivt	Y	41
ivtd2	Y	89
ivtd4	Y	187
ivtd8	Y	373
ivtd16	Y	756
ivtn	Y	41
ivtnd2	Y	89
ivtnd4	Y	187
ivtnd8	Y	373
ivtnd16	Y	757

Cell Name	Output Pin	Maximum Fanout
ld1	Q	47
	QN	46
ld1d2	Q	95
	QN	95
ld1a	Q	35
ld1d2a	Q	77
ld1q	Q	47
ld1qd2	Q	95
ld2	Q	46
	QN	47
ld2d2	Q	95
	QN	95
ld2q	Q	47
ld2qd2	Q	95
ld3	Q	47
	QN	47
ld3d2	Q	95
	QN	95
ld4	Q	48
	QN	46
ld4d2	Q	97
	QN	96
ld5	Q	47
	QN	47
ld5d2	Q	95
	QN	95
ld5q	Q	47
ld5qd2	Q	95
ld6	Q	46
	QN	47
ld6d2	Q	95
	QN	95
ld6q	Q	47
ld6qd2	Q	95
ld7	Q	47
	QN	47
ld7d2	Q	95
	QN	95
ld8	Q	48
	QN	47
ld8d2	Q	97
	QN	96
oak_ldi2	Q	47
	QN	47
oak_ldi2d2	Q	95
	QN	95
oak_ldi3	Q	47
	QN	47
oak_ldi3d2	Q	95
	QN	95
ls0	Q	44
	QN	44
ls0d2	Q	88
	QN	88
ls1	Q	22
	QN	22
ls1d2	Q	95
	QN	95
mx2	Y	47
mx2d2	Y	95
mx2d4	Y	188
mx2dh	Y	21
mx2i	YN	22
mx2ia	YN	22
mx2id2	YN	95



Cell Name	Output Pin	Maximum Fanout
mx2id2a	YN	95
mx2id4	YN	192
mx2id4a	YN	191
mx2idh	YN	9
mx2idha	YN	9
mx2ix4	YN0	22
	YN1	22
	YN2	22
	YN3	22
mx2x4	Y0	48
	Y1	48
	Y2	48
	Y3	48
mx3i	YN	46
mx3id2	YN	94
mx3id4	YN	190
mx4	Y	46
mx4d2	Y	92
mx4d4	Y	177
mx8	Y	46
mx8d2	Y	90
mx8d4	Y	170
nd2	Y	45
nd2d2	Y	91
nd2d4	Y	182
nd2dh	Y	20
nd3	Y	30
nd3d2	Y	62
nd3d4	Y	124
nd3dh	Y	14
nd4	Y	23
nd4d2	Y	46
nd4d2b	Y	94
nd4d4	Y	191
nd4dh	Y	10
nd5	Y	47
nd5d2	Y	94
nd5d4	Y	193
nd6	Y	47
nd6d2	Y	95
nd6d4	Y	191
nd8	Y	47
nd8d2	Y	95
nd8d4	Y	191
nid	Y	48
oak_nid10p	Y	2384
nid16	Y	767
nid2	Y	96
oak_nid20p	Y	4731
nid3	Y	142
nid4	Y	192
nid6	Y	283
nid8	Y	378
nidh	Y	20
nit	Y	42
nitd16	Y	758
nitd2	Y	89
nitd4	Y	186
nitd8	Y	373
nitn	Y	41
nitnd16	Y	757
nitnd2	Y	89
nitnd4	Y	186
nitnd8	Y	373
nr2	Y	23

Cell Name	Output Pin	Maximum Fanout
nr2a	Y	47
nr2d2	Y	47
nr2d2b	Y	96
nr2d4	Y	194
nr2dh	Y	10
nr3	Y	15
nr3a	Y	30
nr3d2	Y	30
nr3d2b	Y	96
nr3d4	Y	194
nr3dh	Y	9
nr4	Y	48
nr4d2	Y	97
nr4d4	Y	195
nr4dh	Y	21
nr5	Y	48
nr5d2	Y	97
nr5d4	Y	194
nr6	Y	48
nr6d2	Y	97
nr6d4	Y	195
nr8	Y	47
nr8d2	Y	95
nr8d4	Y	189
oa21	Y	23
oa211	Y	22
oa2111	Y	21
oa2111d2	Y	94
oa211d2	Y	44
oa211d2b	Y	94
oa211d4	Y	192
oa211dh	Y	10
oa21d2	Y	46
oa21d2b	Y	95
oa21d4	Y	191
oa21dh	Y	10
oa22	Y	21
oa221	Y	18
oa221d2	Y	95
oa221d4	Y	191
oa222	Y	16
oa2222	Y	11
oa2222d2	Y	95
oa2222d4	Y	192
oa222d2	Y	32
oa222d2b	Y	96
oa222d4	Y	192
oa22a	Y	23
oa22d2	Y	42
oa22d2a	Y	47
oa22d2b	Y	96
oa22d4	Y	192
oa22d4a	Y	192
oa22dh	Y	10
oa22dha	Y	10
oa31	Y	14
oa311	Y	14
oa3111	Y	12
oa3111d2	Y	95
oa311d2	Y	94
oa311d4	Y	191
oa31d2	Y	28
oa31d4	Y	191
oa31dh	Y	7
oa32	Y	13



Cell Name	Output Pin	Maximum Fanout
oa321	Y	12
oa321d2	Y	96
oa321d4	Y	192
oa322	Y	10
oa322d2	Y	95
oa322d4	Y	192
oa32d2	Y	95
oa32d4	Y	191
oa33	Y	11
oa331	Y	11
oa331d2	Y	95
oa331d4	Y	191
oa332	Y	7
oa332d2	Y	95
oa332d4	Y	192
oa33d2	Y	95
oa33d4	Y	193
oa4111	Y	8
oa4111d2	Y	95
or2	Y	47
or2d2	Y	94
or2d4	Y	190
or2dh	Y	21
or3	Y	47
or3d2	Y	97
or3d4	Y	196
or3dh	Y	21
or4	Y	43
or4d2	Y	87
or4d4	Y	191
or4dh	Y	21
or5	Y	43
or5d2	Y	86
or5d4	Y	191
scg1	Y	30
scg1d2	Y	61
scg2	Y	47
scg2d2	Y	94
scg3	Y	30
scg3d2	Y	61
scg4	Y	45
scg4d2	Y	90
scg5	Y	46
scg5d2	Y	93
scg6	Y	47
scg6d2	Y	95
scg7	Y	43
scg7d2	Y	87
scg8	Y	47
scg8d2	Y	95
scg9	Y	47
scg9d2	Y	95
scg10	Y	47
scg10d2	Y	94
scg11	Y	14
scg11d2	Y	30
scg12	Y	23
scg12d2	Y	46
scg13	Y	43
scg13d2	Y	87
scg14	Y	43
scg14d2	Y	87
scg15	Y	30
scg15d2	Y	61
scg16	Y	22

Cell Name	Output Pin	Maximum Fanout
scg16d2	Y	45
scg17	Y	44
scg17d2	Y	90
scg18	Y	30
scg18d2	Y	61
scg19	Y	22
scg19d2	Y	44
scg20	Y	23
scg20d2	Y	47
scg21	Y	14
scg21d2	Y	30
scg22	Y	22
scg22d2	Y	46
scg23	S	47
	CO	46
scg23d2	S	94
	CO	93
xn2	Y	48
xn2d2	Y	95
xn2d4	Y	191
xn3	Y	47
xn3d2	Y	93
xn3d4	Y	176
xo2	Y	47
xo2d2	Y	94
xo2d4	Y	191
xo3	Y	47
xo3d2	Y	94
xo3d4	Y	180



### 1.8.2 I/O CELLS

The maximum fanouts for I/O cells are as follows.

**Table 1-7. Maximum Fanouts of I/O Cells**

( $t_R/t_F = 0.213\text{ns}$ , one fanout (SL) =  $0.006710\text{pF}$ )

Cell Name	Output Pin	Maximum Fanout
phic	Y	270
phicd	Y	270
phicu	Y	270
phis	Y	270
phisd	Y	270
phisu	Y	270
phit	Y	270
phitd	Y	270
phitu	Y	270
phsosc1	YN	191
phsosc17	YN	191
phsosc2	YN	193
phsosc27	YN	193
phsosc1	YN	194
phsosc16	YN	194
phsosc2	YN	205
phsosc26	YN	205
phsosc3	YN	402
phsosc36	YN	402
pic	Y	131
pic_abb	Y	131
picc_abb	Y	135
picd	Y	131
picen_abb	Y	130
picu	Y	131
pipci	Y	131
pis	Y	130
pisd	Y	130
pisu	Y	130
psosc1	YN	193
psosc2	YN	193
psosc1	YN	71
psosc2	YN	251
ptic	Y	270
pticd	Y	270
pticu	Y	270
ptipci	Y	270
ptis	Y	270
ptisd	Y	270
ptisu	Y	270
ptit	Y	270
ptitd	Y	270
ptitu	Y	270



### 1.8.3 CK CELL MAX FANOUT

STD110 maximum fanout for CK cells

<Condition>

- VDD = 2.5V
- Fanout = 0.00357pF (= input cap for CK pin of FD1)
- Standard Load (SL) = 0.006710pF
- Input slope = 0.213ns
- Max output transition time (mott) = 1.5ns
- Maximum frequency  $\leq$  200MHz
- Net length ( $\mu\text{m}/\text{fanout}$ ): branch net length for each fanout except trunk

**Table 1-8. Maximum Fanout for CK Cells**

Trunk width (μm)	8				In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	5000	10000	5000	10000	
ck2	151	2	32	1	391
ck4	438	264	91	55	781
ck6	711	499	148	104	1172
ck8	966	702	202	146	1561

**Table 1-9. Maximum Fanout for NID Cells**

Trunk width (μm)	0.44		8		In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	5000	10000	5000	10000	
nid					48
nid2					96
nid3	14				142
nid4	35				192
nid6	69		14		283
nid8	93		28		378
nid16	147		83	46	767
oak_nid10p	200		283	198	2384
oak_nid20p	214		484	307	4731

For high fanout nets including clock net, SEC strongly recommends using clock tree synthesis.



## 1.9 Package Capability By Lead Count

■ In-house □ Sub-contractor

LQFP													
Package	Pitch	Lead Inductance	Lead Count										
			32	48	64	80	100	128	144	160	176	208	256
0707 mm	0.8		■										
	0.5	< 3nH		■									
1010 mm	0.5	< 5nH			■								
1212 mm	0.5	< 5nH				■							
1420 mm	0.5	< 12nH						■					
1414 mm	0.8	< 6nH			■								
	0.5	< 6nH					■						
	0.4	v						■					
2020 mm	0.4								■				
2024 mm	0.5									■	■		
2828 mm	0.5	< 17nH										■	
	0.4	< 17nH											■

TQFP													
1212 mm	0.5	< 5nH				■							
1414 mm	0.5	< 5nH					■						
1420 mm	0.065	< 10nH					■						

PQFP (PQ2 Thermally Enhanced)										
Package	Pitch	Lead Count								
		100	120	128	144	160	208	240	304	
1420 mm	0.65	□								
	0.5			□						
2828 mm	0.8		□	□						
	0.65				□	□				
	0.5						□			
3232 mm	0.5							□		
4040 mm	0.5									□

QFP (with Heat Spreader)										
1420 mm	0.65	■								
	0.5									
2828 mm	0.8		□	■						
	0.65				□	□				
	0.5						□			
3232 mm	0.5							□		
4040 mm	0.5									□



■ In-house □ Sub-contractor

PLCC									
Package	Pitch	Lead Inductance	Lead Count						
			18	28	32	44	52	68	84
7.37 x 12.35 mm	1.27		■						
11.53 x 11.53 mm				■					
11.44 x 13.98 mm					■				
16.61 x 16.61 mm		< 5nH				■			
19.10 x 19.10 mm							■		
24.23 x 24.23 mm								■	
29.31 x 29.31 mm		< 13nH							■

SOP								
Package	Pitch	Lead Count						
		32	48	64(56)	68	69	100	256
8.34 x 20.30 mm	1.27	■						
<b>TSOP1</b>								
1014 mm	0.4		■					
<b>PLCC</b>								
24.33 x 24.23mm	1.27				■			
<b>QFP</b>								
1420 mm	0.65						■	
<b>FBGA</b>								
0909 mm	0.75			■				
0911 mm	0.8					■		
1717 mm	1.00							■

SBGA									
Package	Pitch	Lead Inductance		Lead Count					
		Lp/g	Lsig	256	304	352	540	648	696
2727 mm	1.27	< 3nH	< 7nH	□					
3131 mm		< 3nH	< 8nH		□				
3535 mm		< 3nH	< 8nH			□			
42.5 x 47.5 mm		< 3nH	< 9nH				□		
4545 mm		< 3nH	< 9nH					□	
47.5 x 47.5 mm									□



## Package Parameter Guide for PBGAs and FBGAs

Lead Inductance							
Package Type	Stack-Up (layer)	PCB Size (mm x mm)	L <sub>p/g</sub> (nH)	L <sub>wire</sub> (nH)	L <sub>total</sub> (nH)	T (mm)	L <sub>sig</sub> (nH)
PBGA	2L	23 x 23	< 3.5	1.5	< 4.5	5	< 7
	2L	27 x 27	< 4	1.5	< 5.5	6	< 7.5
	2L	31 x 31	< 4.1	1.5	< 5.6	7	< 8.5
	2L	35 x 35	< 4.5	1.5	< 6	8	< 10
	4L	23 x 23	< 1.3	1.5	< 2.8	5	< 3.5
	4L	27 x 27	< 1.5	1.5	< 3	6	< 4
	4L	31 x 31	< 1.6	1.5	< 3.1	7	< 4.5
	4L	35 x 35	< 1.7	1.5	< 3.2	8	< 5.5
FBGA	2L	06 x 06	< 2	1.5	< 3.5	2	< 2.5
	2L	08 x 08	< 2	1.5	< 3.5	2	< 3.5
	2L	09 x 09	< 2	1.5	< 3.5	2	< 4.5
	2L	10 x 10	< 2	1.5	< 3.5	2	< 4.5
	2L	12 x 12	< 2	1.5	< 3.5	2	< 5
	2L	13 x 13	< 2	1.5	< 3.5	2	< 6
	2L	14 x 14	< 2	1.5	< 3.5	2	< 6
	2L	16 x 16	< 2	1.5	< 3.5	2	< 7
	2L	17 x 17	< 2	1.5	< 3.5	2	< 8
	2L	18 x 18	< 2	1.5	< 3.5	2	< 8

**NOTES: Condition to use above package parameter guide;**

1. Above data are estimated calculations with below assumptions.
2. Center balls are all ground balls for PBGA ball map design.
3. For a ball map design, the power/ground ball pair should be arranged next to each other and located on the center closed inside row and column.
4. Distance between power/ground bonding pad and ball must be less than listed above T[mm] column distance.
5. The bonding wire length between power/ground ball and PCB bonding pad should be less than 2mm.
6.  $L_{total} = L_{p/g} + L_{wire}$ ; L<sub>p/g</sub>: Total inductance of power/ground pad L<sub>sig</sub>: Signal line inductance.
7. Contact IPT development P/T for ball map design request form in special case, other than above 1) ~ 6) notes. Special guide will be provided.



## 1.10 Power Dissipation

### 1.10.1 ESTIMATION OF POWER DISSIPATION IN CMOS CIRCUIT

CMOS circuits have been traditionally considered to consume low power since they draw very small amount of current in a steady state. However, the recent revolution in a CMOS technology that allows very high gate density has changed the way the power dissipation should be understood. The power dissipation in a CMOS circuit is affected by various factors such as the number of gates, the switching frequency, the loading on the output of a gate, and so on.

Power dissipation is important when designers decide the amount of necessary power supply current for the device to operate in safety. Propagation delays and reliability of the device also depend on power dissipation that determines the temperature at which the die operates. To obtain high speed and reliability, designers must estimate power dissipation of the device accurately and determine the appropriate environments including the package and system cooling methods.

This section describes the concepts of two types of power dissipation (static and dynamic) in a CMOS circuit, the method of calculating those in the SEC STD110 library.

### 1.10.2 STATIC (DC) POWER DISSIPATION

There are two types of static or DC current contributing to the total static power dissipation in CMOS circuits.

One is the leakage current of the gates resulted by a reverse bias between a well and a substrate region. There is no DC current path from power to ground in a CMOS because one of the transistor pair is always off, therefore, no static current except the leakage current flows through the internal gates of the device. The amount of this leakage current is, however, in the range of tens of nano amperes, which is negligible.

The other is DC current that flows through the input and output buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/pull-down transistor in the input buffers is about 33μA (at 3.3V) and 25μA (at 2.5V) typically, which is also negligible. Therefore, only DC current that the output buffers source or sink has to be counted to estimate the total static power dissipation.

DC power dissipation of output and bi-directional buffers is determined by the following formula:

$$P_{DC\_OUTPUT} [mW] = \left( \sum_{k=1}^n (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^n ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) T$$

$$P_{DC\_BI} [mW] = \left( \sum_{k=1}^n (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^n ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) \times S_{out} T$$

where,

$n$  = Number of output and bidirectional buffers

$T$  = Total operation time in output mode

$t_H$  = The sum of logic high state time

$t_L$  = The sum of logic low state time

$t_L + t_H = T$  (Supposed that all output and bidirectional buffers have just logic high or low state)

$S_{out}$  is the output mode ratio of bidirectional buffers (typically 0.5)



### 1.10.3 DYNAMIC (AC) POWER DISSIPATION

When a CMOS gate changes its state, it draws switching current as a result of charging or discharging a load capacitance,  $C_L$ . The energy associated with the switching current for a node capacitance,  $C_L$ , is

$$C_L \times V_{DD}^2$$

where  $V_{DD}$  is the power supply voltage.

In addition to the power dissipated by the load capacitance, CMOS circuits consume power due to the short-circuit current flowing through a temporary  $V_{DD}$ -to-ground path during switching.

The dynamic power dissipation for an entire chip is much more complicated to estimate since it depends on the degree of switching activity of the circuit. SEC has found that the degree of switching activity is 10% on the average and recommends this number to be used in estimating the total dynamic power dissipation.

### 1.10.4 POWER DISSIPATION IN STD110

This section describes the equations on how to estimate the power dissipation in STD110. As explained in the previous section, the total power dissipation ( $P_{TOTAL}$ ) consists of static power dissipation ( $P_{DC}$ ) and dynamic power dissipation ( $P_{AC}$ ).

$$P_{TOTAL} = P_{AC} + P_{DC}$$

$P_{DC}$  is negligible in case of CMOS logic.

The dynamic power dissipation is caused by three components: input buffers ( $P_{AC\_INPUT}$ ), output buffers ( $P_{AC\_OUTPUT}$ ), bidirectional buffers ( $P_{AC\_BI}$ ), and internal cells ( $P_{AC\_INTERNAL}$ ).

$$P_{AC} = P_{AC\_INPUT} + P_{AC\_OUTPUT} + P_{AC\_BI} + P_{AC\_INTERNAL}$$

Each term mentioned above is characterized by the following equations:

$$P_{AC\_INPUT} [mW] = 2.5 \times \sum_j^{N\_2.5V\_input} \left( I_{j\_eq\_p} \times \frac{F_j}{100} \times S_j \right) + 3.3 \times \sum_k^{N\_3.3V\_input} \left( I_{k\_eq\_p} \times \frac{F_k}{100} \times S_k \right) + 6.25 \times \sum_i^{N\_total\_input} (0.001 \times S_i \times F_i \times C_{i\_inload})$$

$$P_{AC\_OUTPUT} [mW] = 2.5 \times \sum_i^{N\_2.5V\_output} \left( I_{i\_eq\_p} \times \frac{F_i}{100} \times S_i \right) + 3.3 \times \sum_j^{N\_3.3V\_output} \left( I_{j\_eq\_p} \times \frac{F_j}{100} \times S_j \right) + 6.25 \times \sum_i^{N\_2.5V\_output} (0.001 \times S_i \times F_i \times C_{i\_outload}) + 10.89 \times \sum_j^{N\_3.3V\_output} (0.001 \times S_j \times F_j \times C_{j\_outload})$$

$$P_{AC\_BI} [mW] = P_{AC\_BI\_INPUT} \times (1 - S_{out}) + P_{AC\_BI\_OUTPUT} \times S_{out}$$

$$P_{AC\_BI\_INPUT} [mW] = 2.5 \times \sum_j^{N\_2.5V\_bi} \left( I_{j\_eq\_p} \times \frac{F_j}{100} \times S_j \right) + 3.3 \times \sum_k^{N\_3.3V\_bi} \left( I_{k\_eq\_p} \times \frac{F_k}{100} \times S_k \right) + 6.25 \times \sum_i^{N\_total\_bi} (0.001 \times S_i \times F_i \times C_{i\_inload})$$

$$P_{AC\_BI\_OUTPUT} [mW] = 2.5 \times \sum_i^{N\_2.5V\_bi} \left( I_{i\_eq\_p} \times \frac{F_i}{100} \times S_i \right) + 3.3 \times \sum_j^{N\_3.3V\_bi} \left( I_{j\_eq\_p} \times \frac{F_j}{100} \times S_j \right) + 6.25 \times \sum_i^{N\_2.5V\_bi} (0.001 \times S_i \times F_i \times C_{i\_outload}) + 10.89 \times \sum_j^{N\_3.3V\_bi} (0.001 \times S_j \times F_j \times C_{j\_outload})$$

$$P_{AC\_INTERNAL} [mW] = 0.001 \times (0.2317 \times S + 0.0167) \times G \times F + \sum_j^{N\_macro} (0.001 \times P_j \times F_j)$$



where

N\_2.5V\_input is the number of 2.5V interface input buffers used

N\_3.3V\_input is the number of 3.3V interface input buffers used,

N\_total\_input = N\_2.5V\_input + N\_3.3V\_input

N\_2.5V\_output is the number of 2.5V interface output buffers used,

N\_3.3V\_output is the number of 3.3V interface output buffers used,

N\_2.5V\_bi is the number of 2.5V interface bidirectional buffers used,

N\_3.3V\_bi is the number of 3.3V interface bidirectional buffer used,

N\_macro is the number of macro cells used,

G is the size of the design in gate count,

F is the operating frequency in MHz,

S is the estimated degree of switching activity (typically 0.1 for internal and 0.5 for I/O),

Sout is the output mode ratio of bidirectional buffers (typically 0.5),

C is the load capacitance in pF.

P is the characterized power for the i-th hard macro block ( $\mu\text{W}/\text{MHz}$ )

### 1.10.5 TEMPERATURE AND POWER DISSIPATION

The total power dissipation,  $P_{\text{TOTAL}}$  can be used to find out the device temperature by the following equation:

$$\theta_{JA} = (T_J - T_A) / P_{\text{TOTAL}}$$

where

$\theta_{JA}$  is the thermal impedance,

$T_J$  is the junction temperature of the device,

$T_A$  is the ambient temperature.

Thermal impedances of the SEC packages are given in the following table. The junction temperature, obtained by multiplying  $P_{\text{TOTAL}}$  by the appropriate  $\theta_{JA}$  and adding  $T_A$ , determines the derating factor for the propagation delays and also indicates the reliability measures. Hence, designers can achieve the desired derating factor and reliability targets by choosing appropriate packages and system cooling methods.

**Table 1-10. Thermal Impedances of SEC Plastic Packages**

	SOP/TSOP								
Pin Number	20	24	28	32	44	50	54	62	66
$\theta_{JA} [^{\circ}\text{C}/\text{W}]$	63	58	41-44	46-56	44-71	39-59	34-56	27-33	34-46

	QFP									
Pin Number	44	48	80	100	120	128	160	208	240	256
$\theta_{JA} [^{\circ}\text{C}/\text{W}]$	51-62	43-56	43-74	27-61	33-47	43-51	29-51	22-43	28-47	29-42

	TQFP/LQFP							
Pin Number	32	64	100	144	160	176	208	256
$\theta_{JA} [^{\circ}\text{C}/\text{W}]$	68-70	47	37-70	38	35-62	31-34	37-56	30-42

	PBGA			
Pin Number	272	388	356 (TEPBGA)	452 (TEPBGA)
$\theta_{JA} [^{\circ}\text{C}/\text{W}]$	19-22	16-19	16	14

	SBGA				
Pin Number	256	304	352	432	600
$\theta_{JA} [^{\circ}\text{C}/\text{W}]$	14.1	13.1	11.7	10.2	8.3



## 1.11 V<sub>DD</sub>/V<sub>SS</sub> Rules And Guidelines

There are three kinds of VDD and VSS in STD110, providing power to internal and I/O area.

- Core logic
  - VDD2I, VSS2I
- Pre-driver (I/O area)
  - VDD2P, VDD3P, VSS2P, VSS3P
- Output-drive (I/O area)
  - VDD2O, VDD3O, VSS2O, VSS3O

The number of VDD and VSS pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency

### 1.11.1 BASIC PLACEMENT GUIDELINES

The purpose of these guidelines is to minimize IR drop and noise for reliable device operations.

- Core logic and pre-driver V<sub>DD</sub>/V<sub>SS</sub> pads should be evenly distributed on all sides of the chip.
- If you have core block demanding high power (compiled memory, analog), extra power pads should be placed on that side.
- Power pads for SSO group should be evenly distributed in the SSO group.
- Do not place the quiet signal (analog, reference) or analog power (VDDA/VSSA) or bi-directional buffer next to a SSO group.
- The opposite types of power pads (V<sub>DD</sub>/V<sub>SS</sub>) should be placed as close as possible.
- If it is possible, do not place power pads (V<sub>DD</sub>/V<sub>SS</sub>) at the corner of the chip.

### 1.11.2 VDD2I/VSS2I ALLOCATION GUIDELINES

The purpose of these guidelines is to ensure that the minimum number of core logic power pad pairs meeting the electromigration current limit are used. The number of VDD2I/VSS2I pads required for a specific design is determined by the function of the operating frequency of a chip.

- VDD2I bus width and the number of pads are equal to those of VSS2I
- VDD2I/VSS2I buses and pads should be distributed evenly in the core and on each side of the chip.
- The total number of core logic VDD2I pads is equal to that of VSS2I pads.



The number of VDD2I/VSS2I pad pairs required for a design can be calculated from the following expression:

The number of VDD2I/VSS2I pad pairs =

$$\left\lceil \left[ 0.001 \times (0.0927 \times S + 0.0067) \times G \times F + \sum_i^{N_{\text{macro}}} (P_i \times F_i) \right] / I_{\text{em}} \right\rceil \text{round-up}$$

where,

G = The core (excluding hard macro blocks) size in the gate counts

S = The switching ratio (typically = 0.1)

F = Operating frequency (MHz)

P<sub>i</sub> = Characterized current for the i-th hard macro block (mA/MHz)

F<sub>i</sub> = Operating frequency for the i-th hard macro block (MHz)

I<sub>em</sub> = Current limit per VDD/VSS pad pairs based on ElectroMigration rule (80mA)

For reliable device operation and minimize IR voltage drop, minimum number of VDD2I/VSS2I power pad pairs is 4.

Extra power may be needed for the demanding high power macro blocks (SRAM, analog block...).

### 1.11.3 VDD2P/VSS2P (VDD3P/VSS3P) ALLOCATION GUIDELINES.

These guidelines ensure that an adequate input threshold voltage margin is maintained during a switching.

The number of VDD2P/VSS2P (VDD3P/VSS3P) pads required for a design can be calculated from the following expression:

$$\text{Number\_of\_VDD2P/VSS2P(VDD3P/VSS3P) pairs} = \left\lceil \frac{I_{\text{eq\_p}}}{I_{\text{em}}} \right\rceil \text{round-up}$$

In above expression,

I<sub>eq\_p</sub> =  $\sum$ (Average current of input/output buffers and bi-direction pre-drivers at maximum operational I/O frequency) [mA] (Refer Table 1-11)

$$I_{\text{eq\_p}} = \sum_i^{N_{\text{input}}} \left( I_{\text{eq\_p\_in}} \times \frac{F_i}{100} \right) + \sum_j^{N_{\text{output}}} \left( I_{\text{j\_eq\_p\_out}} \times \frac{F_j}{100} \right) + \sum_k^{N_{\text{bi}}} \left[ \left( I_{\text{k\_eq\_p\_in}} \times \frac{F_k}{100} \right) (1 - S_{\text{out}}) + \left( I_{\text{k\_eq\_p\_out}} \times \frac{F_k}{100} \right) \times S_{\text{out}} \right]$$

where

N<sub>input</sub> is the number of input buffers used,

N<sub>output</sub> is the number of output buffers used,

N<sub>bi</sub> is the number of bi-directional buffers used,

F is the operating frequency in MHz,

S<sub>out</sub> is the output mode ratio of bi-directional buffers (typically 0.5),

I<sub>em</sub> = Current limit per VDD/VSS pad pairs based on electromigration rule. (80mA)

**Table 1-11. 2.5V Interface**

Input Buffer Type		CMOS			CMOS Schmitt		
I <sub>eq_p</sub> (mA)		0.35			0.36		
Output Pre-Driver Type		Driver			Tristate		
		B1-4	B6-8	B10-12	T1-4	T6-8	T10-12
I <sub>eq_p</sub> (mA)	Normal	0.14	0.27	0.41	0.24	0.36	0.53
	Slew rate	0.14	0.25	0.35	0.25	0.35	0.45



Table 1-12. 3.3V Interface

Input Buffer Type			CMOS		TTL	Schmitt Trigger		
Ieq_p (mA)	Normal		0.52		0.54	0.54		
	Tolerant		0.60		0.60	0.51		
Output Pre-driver Type			CMOS Driver			Tristate		
			B1–4	B6–8	B10–12	T1–4	T6–8	T10–12
Ieq_p (mA)	Normal	Normal	0.25	0.46	0.55	0.34	0.51	0.60
		Slew rate	0.28	0.37	0.46	0.36	0.45	0.55
	Tolerant		-	-	-	(T1,2,3) 0.50	-	-

For reliable device operation and minimum IR voltage drop, at least 4 pairs of VDD2P/VSS2P (VDD3P/VSS3P) power pads are needed.

#### 1.11.4 VDD2O/VSS2O (VDD3O/VSS3O) ALLOCATION GUIDE

SSO (Simultaneous Switching Output) current induced in power and ground inductance can cause system failure because of voltage fluctuations. For the calculation of output drive power pad numbers, we consider the SSO noise as well as the current limit based on electromigration. We may define the SSO as outputs switching simultaneously in 1ns windows, such as bus type buffers.

**NOTE:** In case of heavy load, high frequency and low package inductance, the number of power pads for SSO block could be determined by electromigration rule rather than limit of SSO noise. So the number of power pads for SSO block should be determined as the worse one of the power pad number under the limit of SSO noise and that under the limit of electromigration rule.

##### 1) Number of power pads for SSO block

##### - Number of power pads for SSO block under the limit of SSO noise

- Calculating the number of power pad for each SSO group from the following expressions:

$$NVDDO_{\text{each\_SSO}} = \frac{\text{number\_of\_SSO}}{NBvdd} \times L_{pg} \times \frac{1}{D_{SSO\_mode}}$$

$$NVSSO_{\text{each\_SSO}} = \frac{\text{number\_of\_SSO}}{NBvss} \times L_{pg} \times \frac{1}{D_{SSO\_mode}}$$

In above formula,

$NVDDO_{\text{each\_SSO}}$  = Number of VDD2O (VDD3O) pad required for each SSO group

$NVSSO_{\text{each\_SSO}}$  = Number of VSS2O (VSS3O) pad required for each SSO group

$NBvdd$  = Number of buffers per VDD2O (VDD3O) power pad with 1nH lead inductance

$NBvss$  = Number of buffers per VSS2O (VSS3O) ground pas with 1nH lead inductance

$L_{pg}$  = Package lead frame inductance

(refer to 1.9 package capability by lead count)

$D_{SSO\_mode} = D_{L\_mode} \times D_{P\_mode} \times D_{V\_mode} \times D_{T\_mode} \times D_{C\_mode}$  (Refer to Table 1-13. and Table 1-14.)

$D_{L\_mode}$  = Lead inductance derating factor

$D_{P\_mode}$  = Process derating factor

$D_{V\_mode}$  = Voltage derating factor

$D_{T\_mode}$  = Temperature derating factor

$D_{C\_mode}$  = Cload derating factor (\*mode is either vdd or vss.)



Table 1-13. Derating Equation (external 2.5V interface)

Item	Mode	Equation	Range
Package Lead	D <sub>L_vdd</sub>	0.0417 x Lpg + 0.9375 0.0417 x Lpg + 0.9375	3nH ≤ Lpg ≤ 10nH 10nH ≤ Lpg ≤ 15nH
	D <sub>L_vss</sub>	0.0417 x Lpg + 0.9375 0.0417 x Lpg + 0.9375	3nH ≤ Lpg ≤ 10nH 10nH < Lpg ≤ 15nH
Process	D <sub>P_vdd</sub>	1.0000 1.2549 1.7255	best typical worst
	D <sub>P_vss</sub>	1.0000 1.2549 1.7451	best typical worst
Voltage	D <sub>V_vdd</sub>	– 0.8824 x voltage + 3.3235 – 0.5882 x voltage + 2.5882	2.3 ≤ voltage ≤ 2.5 2.5 < voltage ≤ 2.7
	D <sub>V_vss</sub>	– 0.8824 x voltage + 3.3235 – 0.5882 x voltage + 2.5882	2.3 ≤ voltage ≤ 2.5 2.5 < voltage ≤ 2.7
Temperature	D <sub>T_vdd</sub>	0.0024 x temperature + 1.0000 0.0032 x temperature + 0.9786	–40 ≤ temperature ≤ 25 25 < temperature ≤ 125
	D <sub>T_vss</sub>	0.0031 x temperature + 1.0000 0.0029 x temperature + 1.0071	–40 ≤ temperature ≤ 25 25 < temperature ≤ 125
Cload	D <sub>C_vdd</sub>	0.0347 x Cload + 0.6525 0.0286 x Cload + 0.8369	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF
	D <sub>C_vss</sub>	0.0354 x Cload + 0.6456 0.0285 x Cload + 0.8544	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF

Table 1-14. Derating Equation (external 3.3V interface)

Item	Mode	Equation	Range
Package Lead	D <sub>L_vdd</sub>	0.0462 x Lpg + 1.1538 0.0231 x Lpg + 1.3846	3nH ≤ Lpg ≤ 10nH 10nH ≤ Lpg ≤ 15nH
	D <sub>L_vss</sub>	0.0469 x Lpg + 0.7813 0.0313 x Lpg + 0.9375	3nH ≤ Lpg ≤ 10nH 10nH < Lpg ≤ 15nH
Process	D <sub>P_vdd</sub>	1.0000 1.2537 2.2985	best typical worst
	D <sub>P_vss</sub>	1.0000 1.1563 1.4063	best typical worst
Voltage	D <sub>V_vdd</sub>	– 1.2936 x voltage + 5.4328 – 0.4478 x voltage + 2.6119	3.0 ≤ voltage ≤ 3.3 3.3 < voltage ≤ 3.6
	D <sub>V_vss</sub>	– 0.4166 x voltage + 2.5000 – 0.4166 x voltage + 2.5000	3.0 ≤ voltage ≤ 3.3 3.3 < voltage ≤ 3.6
Temperature	D <sub>T_vdd</sub>	0.0036 x temperature + 1.0000 0.0041 x temperature + 0.9878	–40 ≤ temperature ≤ 25 25 < temperature ≤ 125
	D <sub>T_vss</sub>	0.0038 x temperature + 1.0000 0.0028 x temperature + 1.0227	–40 ≤ temperature ≤ 25 25 < temperature ≤ 125
Cload	D <sub>C_vdd</sub>	0.0338 x Cload + 0.6618 0.0554 x Cload + 0.0146	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF
	D <sub>C_vss</sub>	0.0444 x Cload + 0.5556 0.0370 x Cload + 0.7778	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF



Table 1-15. NBvdd/NBvss Parameter (Process = best, Volt = 2.7V/3.6V Temp. = 0°C, Llead = 1nH)

Buffer Type	Voltage Type	Normal		Slew-Rate Medium (sm)		Slew-Rate High (sh)	
		NBvdd	NBvss	NBvdd	NBvss	NBvdd	NBvss
pob1 (pot1)	2.5V Interface	176	178	—	—	—	—
pob2 (pot2)		140	142	—	—	—	—
pob4 (pot4)		102	102	160	160	—	—
pob6 (pot6)		84	84	142	142	—	—
pob8 (pot8)		72	72	116	116	—	—
pob12 (pot12)		60	60	96	96	236	236
phob1 (phot1)	3.3V Interface	382	166	—	—	—	—
phob2 (phot2)		276	104	—	—	—	—
phob4 (phot4)		134	64	168	104	—	—
phob6 (phot6)		108	44	132	90	—	—
phob8 (phot8)		98	38	118	86	—	—
phob12 (phot12)		86	32	92	62	130	124
ptot1	5V Tolerant	434	376	—			
ptot2		272	180				
ptot3		203	116				

**NOTE:** pob1 means 1mA output driver cell, and pob12 means 12mA output driver cell.

- Calculating the number of required power pad for total SSO from the following expression:

$$NVDDO1sso = \sum NVDDOeach\_sso$$

$$NVSSO1sso = \sum NVSSOeach\_sso$$

In the above formula,

NVDDOssso = Number of VDD2O (VDD3O) pad per total SSO buffers

NVSSOssso = Number of VSS2O (VSS3O) pad per total SSO buffers



### - Number of power pads for SSO block under the limit of electromigration rule

- Calculating the following expression:

$$NVDDO2_{SSO}/NVSSO2_{SSO} = \frac{I_{eq\_o}}{I_{em}}$$

$$I_{eq\_o} = \sum_i^{N\_SSO\_output} (0.001 \times C_{i\_outload} \times V_i \times F_i \times S_i) + \sum_j^{N\_SSO\_bi} (0.001 \times C_{j\_outload} \times V_j \times F_j \times S_j \times S_{j\_out})$$

where

N\_SSO\_output is the number of simultaneous switching output buffers used,

N\_SSO\_bi is the number of simultaneous switching bi-directional buffers used,

C\_outload = Output load capacitance [pF]

V = Operating voltage [V]

F = Maximum I/O operating frequency [MHz]

S = Switching ratio (typically 0.5)

S\_out = Output mode ratio of bidirectional buffers (typically 0.5)

I\_em = Current limit per VDD/VSS pad paris based on electromigration rule. (80mA)

### 2) Number of power pads for non-SSO block

- Calculating the following expression:

$$NVDDO_{non\_SSO}/NVSSO_{non\_SSO} = \frac{I_{eq\_o}}{I_{em}}$$

$$I_{eq\_o} = \sum_i^{N\_non\_SSO\_output} (0.001 \times C_{i\_outload} \times V_i \times F_i \times S_i) + \sum_j^{N\_non\_SSO\_bi} (0.001 \times C_{j\_outload} \times V_j \times F_j \times S_j \times S_{j\_out})$$

where

N\_non\_SSO\_output is the number of non-simultaneous switching output buffers used,

N\_non\_SSO\_bi is the number of non-simultaneous switching bi-directional buffers used,

C\_outload = Output load capacitance [pF]

V = Operating voltage [V]

F = Maximum I/O operating frequency [MHz]

S = Switching ratio (typically 0.5)

S\_out = Output mode ratio of bidirectional buffers (typically 0.5)

I\_em = Current limit per VDD/VSS pad paris based on electromigration rule. (80mA)

### 3) Total number of power pads for VDD20/VSS20 (VDD30/VSS30)

- Calculating the following expressions:

$$\text{Number of VDD20 (VDD30)} = \lceil \max(NVDDO1_{SSO}, NVDDO2_{SSO}) + NVDDO_{non\_SSO} \rceil \text{ round-up}$$

$$\text{Number of VSS20 (VSS30)} = \lceil \max(NVSSO1_{SSO}, NVSSO2_{SSO}) + NVSSO_{non\_SSO} \rceil \text{ round-up}$$

When open drain type buffers are used, you can consider using VSS20 (VSS30) pads since they have current sink only.



## 1.12 Crystal Oscillator Consideration

### 1.12.1 OVERVIEW

STD110 contains a circuit commonly referred to as an “on-chip oscillator.” The on-chip circuit itself is not an oscillator but an amplifier which is suitable for being used as the amplifier part of a feedback oscillator. With proper selection of off-chip components, this oscillator circuit performs better than any other types of clock oscillators.

It is very important to select suitable off-chip components to work with the on-chip oscillator circuitry. It should be noted, however, that SEC cannot assume the responsibility of writing specifications for the off-chip components of the complete oscillator circuit, nor of guaranteeing the performance of the finished design in production, any more than a transistor manufacturer, whose data sheets show a number of suggested amplifier circuits, can assume responsibility for the operation, in production, of any of them.

We are often asked why we don’t publish a list of required crystal or ceramic resonator specifications, and recommend values for the other off-chip components. This has been done in the past, but sometimes with consequences that were not intended.

Suppose we suggest a maximum crystal resistance of 30ohms for some given frequency. Then your crystal supplier tells you the 30ohm crystals are going to cost twice as much as 50ohm crystals. Fearing that SEC will not “guarantee operation” with 50ohm crystals, you order the expensive ones.

In fact, SEC guarantees only what is embodied within an SEC product. Besides, there is no reason why 50ohm crystals couldn’t be used, if the other off-chip components are suitably adjusted.

Should we recommend values for the other off-chip components? Should we do for 50ohm crystals or 30ohm crystals? With respect to what should we optimize their selection? Should we minimize start-up time or maximize frequency stability?

In many applications, neither start-up time nor frequency stability is particularly critical, and our “recommendations” are only restricting your system to unnecessary tolerances. It all depends on the application.

### 1.12.2 OSCILLATOR DESIGN CONSIDERATIONS

ASIC designers have a number of options for clocking the system. The main decision is whether to use the “on-chip” oscillator or an external oscillator. If the choice is to use the on-chip oscillator, what kinds of external components are to use an external oscillator, what type of oscillator would it be?

The decisions have to be based on both economic and technical requirements. In this section we will discuss some of the factors that should be considered.

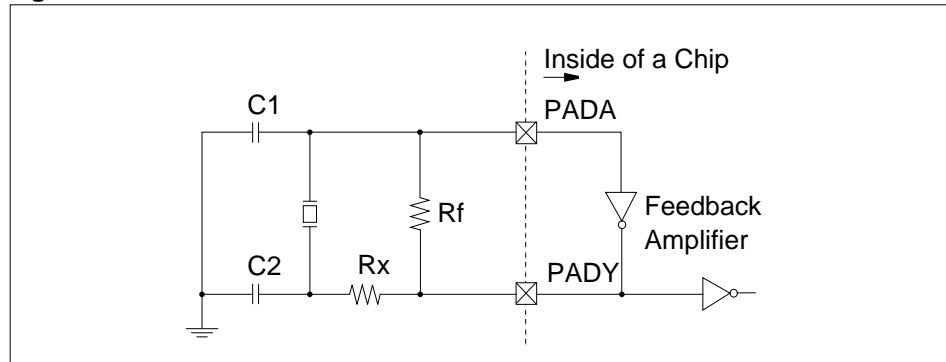


### 1.12.2.1 On-Chip Oscillator

In most cases, the on-chip amplifier with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components that commonly used for CMOS gate oscillator are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistor Rf and Rx as shown in the figure below.

**Figure 1-19. CMOS Oscillator**



### 1.12.2.2 Crystal Specifications

Specifications for an appropriate crystal are not very critical, unless the frequency is. Any fundamental-mode crystal of medium or better quality can be used.

We are often asked what maximum crystal resistance should be specified. The best answer to that question is the lower the better, but use what is available.

The crystal resistance will have some effect on start-up time and steady-state amplitude, but not so much that it can't be compensated for by appropriate selection of the capacitance, C1 and C2.

Similar questions are asked about specifications of load capacitance and shunt capacitance. The best advice we can give is to understand what these parameters mean and how they affect the operation of the circuit (that being the purpose of this application note), and then to decide for yourself if such specifications are meaningful in your frequency tolerances are tighter than about 0.1%.

Part of the problem is that crystal manufacturers are accustomed to talking "ppm" tolerances with radio engineers and simply won't take your order until you've filled out their list of frequency tolerance requirements, both for yourself and to the crystal manufacturer. Don't pay for 0.003% crystals if your actual frequency tolerance is 1%.



### 1.12.2.3 Oscillation Frequency

The oscillation frequency is determined 99.5% by the crystal and up to about 0.5% by the circuit external to the crystal.

The on-chip amplifier has little effect on the frequency, which is as it should be, since the amplifier parameterizes temperature and process dependent.

The influence of the on-chip amplifier on the frequency is by means of its input and output (pin-to-ground) capacitances, which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance, which parallels the crystal. The input and pin-to-pin capacitances are about 7pF each.

Internal phase deviations capacitance of 25 to 30pF. These deviations from the ideal have less effect in the positive reactance oscillator (with the inverting amplifier) than in a comparable series resonant oscillator (with the non-inverting amplifier) for two reasons: first, the effect of the output capacitor; second, the positive reactance oscillator is less sensitive, frequency-wise, to such phase errors.

### 1.12.2.4 C1 / C2 Selection

Optimal values for the capacitors C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and also on application-specific requirements on start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability, because of various reset and initialization requirements.

Less commonly, accuracy of the oscillator frequency is also critical, for example, when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 15pF. (But they don't have to be either.)

Increasing the value of these capacitances above some 40 or 50pF improves frequency stability. It also tends to increase the start-up time. There is a maximum value (several hundred pF, depending on the value of R1 of the quartz or ceramic resonator) above which the oscillator won't start up at all.

If the on-chip amplifier is a simple inverter, the user can select values for C1 and C2 between some 15 and 50pF, depending on whether start-up time or frequency stability is the more critical parameter in a specific application.

### 1.12.2.5 Rf / Rx Selection

A CMOS inverter might work better in this application since a large Rf (1mega-ohm) can be used to hold the inverter in its linear region.

Logic gates tend to have a fairly low output resistance, which destabilizes the oscillator. For that reason a resistor Rx (several k-ohm) is often added to the feedback network, as shown in Figure 1-19.

At higher frequencies a 20 or 30pF capacitor is sometimes used in the Rx position, to compensate for some of the internal propagation delay.



### 1.12.2.6 Pin Capacitance Rf / Rx Selection

Internal pin-to-ground and pin-to-pin capacitances, and PADA and PADY have some effect on the oscillator. These capacitances are normally taken to be in the range of 5 to 10pF, but they are extremely difficult to evaluate. Any measurement of one such capacitance necessarily include effects from the others.

One advantage of the positive reactance oscillator is that the pin-to ground cap. is paralleled by an external bulk capacitance, so a precise determination of their value is unnecessary.

We would suggest that there is little justification for more precision than to assign them a value of 7pF (PADA-to-ground and PADA-to-PADY). This value is probably not in error by more than 3 or 4pF.

The PADY-to-ground cap. is not entirely a “pin capacitance”, but more like an “equivalent output capacitance” of some 25 to 30pF, having to include the effect of internal phase delays. This value varies to some extent with temperature, process, and frequency.

### 1.12.2.7 Placement of Components

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and  $V_{SS}$  pins.

If possible, use dedicated  $V_{SS}$  and  $V_{DD}$  pin for only crystal feedback amplifier.

## 1.12.3 TROUBLESHOOTING OSCILLATOR PROBLEMS

The first thing to consider in case of difficulty is that there may be significant differences in stray caps between the test jig and the actual application, particularly if the actual application is on a multi-layer board.

Noise glitches, that are not present in the test jig but are in the application board, are another possibility. Capacitive coupling between the oscillator circuitry and other signal has already been mentioned as a source of miscounts in the internal clocking circuitry. Inductive coupling is also doubtful, if there is strong current nearby. These problems are a function of the PCB layout.

Surrounding oscillator components with “quiet” traces (for example, VCC and ground) will alleviate capacitive coupling to signals having fast transition time. To minimize inductive coupling, the PCB layout should minimize the areas of the loops formed by oscillator components.

The loops demanding to be checked are as follows:

- PADA through the resonator to PADY;
- PADA through C1 to the  $V_{SS}$  pin;
- PADY through C2 to the  $V_{SS}$  pin.

It is not unusual to find that the ground ends of C1 and C2 eventually connect up to the  $V_{SS}$  pin only after looping around the farthest ends of the board. Not good.

Finally, it should not be overlooked that software problems sometimes imitate the symptoms of a slow-starting oscillator or incorrect frequency. Never underestimate the perversity of a software problem.



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# Electrical Characteristics

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2



**Contents**

DC Electrical Characteristics ..... 2-1



## DC ELECTRICAL CHARACTERISTICS

$V_{DD} = 3.3 \pm 0.3V$ ,  $T_A = -40$  to  $85^\circ C$ ,  $V_{EXT} = 5 \pm 0.25V$  (In case of 5V tolerant)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V <sub>IH</sub>	High level input voltage					V
	LVC MOS interface		0.7V <sub>DD</sub>			
	LVTTL interface		2.0			
V <sub>IL</sub>	Low level input voltage					V
	LVC MOS interface				0.3V <sub>DD</sub>	
	LVTTL interface				0.8	
V <sub>T</sub>	Switching threshold	LVC MOS		0.5V <sub>DD</sub>		V
		LVTTL		1.4		
V <sub>T</sub> <sup>+</sup>	Schmitt trigger, positive-going threshold	LVC MOS/LVTTL			2.0	
V <sub>T</sub> <sup>−</sup>	Schmitt trigger, negative-going threshold	LVC MOS/LVTTL	0.8			
V <sub>H</sub>	V <sub>T</sub> <sup>+</sup> - V <sub>T</sub> <sup>−</sup>	Schmitt-trigger	0.5	0.575	0.65	
I <sub>IH</sub>	High level input current					μA
	Input buffer	V <sub>IN</sub> = V <sub>DD</sub>	−10		10	
	Input buffer with pull-down		10	33	60	
I <sub>IL</sub>	Low level input current					μA
	Input buffer	V <sub>IN</sub> = V <sub>SS</sub>	−10		10	
	Input buffer with pull-up		−60	−33	−10	
V <sub>OH</sub>	High level output voltage					V
	Type B1 to B12 <sup>Note1</sup>	I <sub>OH</sub> = −1μA	V <sub>DD</sub> − 0.05			
	Type B1	I <sub>OH</sub> = −1mA	2.4			
	Type B2	I <sub>OH</sub> = −2mA				
	Type B3	I <sub>OH</sub> = −3mA				
	Type B4	I <sub>OH</sub> = −4mA				
	Type B6	I <sub>OH</sub> = −6mA				
	Type B8	I <sub>OH</sub> = −8mA				
	Type B10	I <sub>OH</sub> = −10mA				
	Type B12	I <sub>OH</sub> = −12mA				
V <sub>OL</sub>	Low level output voltage					V
	Type B1 to B12 <sup>Note1</sup>	I <sub>OL</sub> = 1μA			0.05	
	Type B1	I <sub>OL</sub> = 1mA			0.4	
	Type B2	I <sub>OL</sub> = 2mA				
	Type B3	I <sub>OL</sub> = 3mA				
	Type B4	I <sub>OL</sub> = 4mA				
	Type B6	I <sub>OL</sub> = 6mA				
	Type B8	I <sub>OL</sub> = 8mA				
	Type B10	I <sub>OL</sub> = 10mA				
	Type B12	I <sub>OL</sub> = 12mA				
I <sub>OZ</sub>	Tri-state output leakage current	V <sub>OUT</sub> = V <sub>SS</sub> or V <sub>EXT</sub>	−10		10	μA
I <sub>OS</sub>	Output short circuit current	V <sub>DD</sub> = 3.6V, V <sub>O</sub> = V <sub>DD</sub>			55	mA
		V <sub>DD</sub> = 3.6V, V <sub>O</sub> = V <sub>SS</sub>	−55			
I <sub>DD</sub>	Quiescent supply current	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub>			100 <sup>Note2</sup>	μA
C <sub>IN</sub>	Input capacitance <sup>Note3</sup>	Any Input and Bidirectional Buffers			4	pF
C <sub>OUT</sub>	Output capacitance <sup>Note3</sup>	Any Output Buffer			4	pF



$V_{DD} = 2.5 \pm 0.2V$ ,  $T_A = -40$  to  $85^\circ C$  (In case of general I/O)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V <sub>IH</sub>	High level input voltage					V
	LVC MOS interface		1.7			
V <sub>IL</sub>	Low level input voltage					V
	LVC MOS interface				0.7	
V <sub>T</sub>	Switching threshold	LVC MOS		0.5V <sub>DD</sub>		V
V <sub>T</sub> <sup>+</sup>	Schmitt trigger, positive-going threshold	LVC MOS			1.9	
V <sub>T</sub> <sup>−</sup>	Schmitt trigger, negative-going threshold	LVC MOS	0.6			
V <sub>H</sub>	V <sub>T</sub> <sup>+</sup> - V <sub>T</sub> <sup>−</sup>	Schmitt-trigger	0.5	0.65	0.8	
I <sub>IH</sub>	High level input current					μA
	Input buffer	V <sub>IN</sub> = V <sub>DD</sub>	−10		10	
	Input buffer with pull-down		10	25	50	
I <sub>IL</sub>	Low level input current					μA
	Input buffer	V <sub>IN</sub> = V <sub>SS</sub>	−10		10	
	Input buffer with pull-up		−50	−25	−10	
V <sub>OH</sub>	High level output voltage					V
	Type B1 to B12 <sup>Note1</sup>	I <sub>OH</sub> = −1μA	V <sub>DD</sub> − 0.05			
	Type B1	I <sub>OH</sub> = −1mA				
	Type B2	I <sub>OH</sub> = −2mA				
	Type B4	I <sub>OH</sub> = −4mA				
	Type B6	I <sub>OH</sub> = −6mA				
	Type B8	I <sub>OH</sub> = −8mA				
	Type B10	I <sub>OH</sub> = −10mA				
	Type B12	I <sub>OH</sub> = −12mA				
V <sub>OL</sub>	Low level output voltage					V
	Type B1 to B12 <sup>Note1</sup>	I <sub>OL</sub> = 1μA			0.05	
	Type B1	I <sub>OL</sub> = 1mA			0.5	
	Type B2	I <sub>OL</sub> = 2mA				
	Type B4	I <sub>OL</sub> = 4mA				
	Type B6	I <sub>OH</sub> = 6mA				
	Type B8	I <sub>OH</sub> = 8mA				
	Type B10	I <sub>OH</sub> = 10mA				
	Type B12	I <sub>OH</sub> = 12mA				
I <sub>OZ</sub>	Tri-state output leakage current	V <sub>OUT</sub> = V <sub>SS</sub> or V <sub>EXT</sub>	−10		10	μA
I <sub>OS</sub>	Output short circuit current	V <sub>DD</sub> = 3.6V, V <sub>O</sub> = V <sub>DD</sub>			55	mA
		V <sub>DD</sub> = 3.6V, V <sub>O</sub> = V <sub>SS</sub>	−55			
I <sub>DD</sub>	Quiescent supply current	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub>			100 <sup>Note2</sup>	μA
C <sub>IN</sub>	Input capacitance <sup>Note3</sup>	Any Input and Bidirectional Buffers			4	pF
C <sub>OUT</sub>	Output capacitance <sup>Note3</sup>	Any Output Buffer			4	pF

**NOTES:**

1. Type B1 means 1mA output driver cells, and type B6/B12 means 6mA/12mA output driver cells.
2. This value depends on the customer design.
3. This value exclude package parasitics.



**Absolute Maximum Ratings**

Symbol	Parameter	Rating		Unit
$V_{DD}$	DC supply voltage	2.5V $V_{DD}$	3.6	V
		3.3V $V_{DD}$	4.6	
$V_{IN}$	DC input voltage	2.5V input buffer	3.6	
		3.3V input buffer	4.6	
		3.3V interface/5V tolerant input buffer	6.5	
$V_{OUT}$	DC output voltage	2.5V output buffer	3.6	
		3.3V output buffer	4.6	
		3.3V interface/5V tolerant output buffer	6.5	
$I_{latch}$	Latch-up current	$\pm 200$		mA
$T_{STG}$	Storage temperature	– 65 to 150		°C

**Recommended Operating Conditions**

Symbol	Parameter	Rating			Unit
			Min	Max	
V <sub>DD</sub>	DC Supply Voltage for Internal (=V <sub>DDIN</sub> )	2.5V V <sub>DD</sub>	2.3	2.7	V
	DC Supply Voltage for I/O Block (=V <sub>DDIO</sub> )	2.5V V <sub>DD</sub>	2.3	2.7	
		3.3V V <sub>DD</sub>	3.0	3.6	
	DC Supply Voltage for Analog Core (=V <sub>DDA</sub> )	2.5V V <sub>DD</sub>	2.5 – 5%	2.5 + 5%	
		3.3V V <sub>DD</sub>	3.3 – 5%	3.3 + 5%	
V <sub>IN</sub>	DC Input Voltage	2.5V input buffer	–0.2	V <sub>DDIO</sub> +0.2	
		3.3V input buffer	–0.3	V <sub>DDIO</sub> +0.3	
		3.3V interface / 5V tolerant input buffer	–0.3	5.5	
V <sub>OUT</sub>	DC Output Voltage	2.5V output buffer	–0.2	V <sub>DDIO</sub> +0.2	
		3.3V output buffer	–0.3	V <sub>DDIO</sub> +0.3	
		3.3V interface / 5V tolerant output buffer	–0.3	5.5	
T <sub>A</sub>	Commercial temperature range			0 to 70	°C
	Industrial temperature range			–40 to 85	



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## Internal Macrocells

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3



**Contents**

Overview ..... 3-1

Summary Tables..... 3-2

Logic Cells..... 3-7

Flip-Flops..... 3-300

Latches..... 3-400

Bus Holder..... 3-448

Internal Clock Drivers ..... 3-449

Decoders ..... 3-451

Adders ..... 3-460

Multiplexers ..... 3-470



## OVERVIEW

The third chapter contains data sheets of logic cells, flip-flops, latches, bus holder, internal clock drivers, decoders, adders and multiplexers.

The electrical characteristics of each cell follow its basic cell data.

Summary tables in the following pages list the whole STD110 internal macrocells by the type and show their reference page numbers for your convenience. Moreover, you can find the more detailed description tables on the leading pages of each category.



## SUMMARY TABLES

### Logic Cells

Cell Type	Cell Name	Page
AND Cells	AD2DH/AD2/AD2D2/AD2D4	3-17
	AD3DH/AD3/AD3D2/AD3D4	3-19
	AD4DH/AD4/AD4D2/AD4D4	3-21
	AD5/AD5D2/AD5D4	3-24
NAND Cells	ND2DH/ND2/ND2D2/ND2D4	3-27
	ND3DH/ND3/ND3D2/ND3D4	3-29
	ND4DH/ND4/ND4D2/ND4D2B/ND4D4	3-32
	ND5/ND5D2/ND5D4	3-35
	ND6/ND6D2/ND6D4	3-38
	ND8/ND8D2/ND8D4	3-42
NOR Cells	NR2DH/NR2/NR2D2/NR2D2B/NR2D4/NR2A	3-46
	NR3DH/NR3/NR3D2/NR3D2B/NR3D4/NR3A	3-49
	NR4DH/NR4/NR4D2/NR4D4	3-53
	NR5/NR5D2/NR5D4	3-56
	NR6/NR6D2/NR6D4	3-60
	NR8/NR8D2/NR8D4	3-64
OR Cells	OR2DH/OR2/OR2D2/OR2D4	3-68
	OR3DH/OR3/OR3D3/OR3D4	3-70
	OR4DH/OR4/OR4D2/OR4D4	3-73
	OR5/OR5D2/OR5D4	3-76
Exclusive-NOR Cells	XN2/XN2D2/XN2D4	3-80
	XN3/XN3D2/XN3D4	3-82
Exclusive-OR Cells	XO2/XO2D2/XO2D4	3-84
	XO3/XO3D2/XO3D4	3-86
Combinational Cells of AND and NOR	AO21DH/AO21/AO21D2/AO21D2B/AO21D4	3-88
	AO211DH//AO211D2/AO211D2B/AO211D4	3-91
	AO2111/AO2111D2	3-94
	AO22DH/AO22/AO22D2/AO22D2B/AO22D4	3-97
	AO22DHA/AO22A/AO22D2A/AO22D4A	3-100
	AO221/AO221D2/AO221D4	3-103
	AO222/AO222D2/AO222D2B/AO222D4	3-107
	AO222A/AO222D2A/AO222D4A	3-112
	AO2222/AO2222D2/AO2222D4	3-114
	AO31DH/AO31/AO31D2/AO31D4	3-118
	AO311/AO311D2/AO311D4	3-121
	AO3111/AO3111D2	3-125
	AO32/AO32D2/AO32D4	3-128



Cell Type	Cell Name	Page
	AO321/AO321D2/AO321D4	3-132
	AO322/AO322D2/AO322D4	3-136
	AO33/AO33D2/AO33D4	3-140
	AO331/AO331D2/AO331D4	3-144
	AO332/AO332D2/AO332D4	3-148
	AO4111/AO4111D2	3-152
Combinational Cells of OR and NAND	OA21DH/OA21/OA21D2/OA21D2B/OA21D4	3-155
	OA211DH/OA211/OA211D2/OA211D2B/OA211D4	3-158
	OA2111/OA2111D2	3-161
	OA22DH/OA22/OA22D2/OA22D2B/OA22D4	3-164
	OA22DHA/OA22A/OA22D2A/OA22D4A	3-167
	OA221/OA221D2/OA221D4	3-170
	OA222/OA222D2/OA222D2B/OA222D4	3-174
	OA2222/OA2222D2/OA2222D4	3-179
	OA31DH/OA31/OA31D2/OA31D4	3-183
	OA311/OA311D2/OA311D4	3-186
	OA3111/OA3111D2	3-190
	OA32/OA32D2/OA32D4	3-193
	OA321/OA321D2/OA321D4	3-197
	OA322/OA322D2/OA322D4	3-201
	OA33/OA33D2/OA33D4	3-205
	OA331/OA331D2/OA331D4	3-209
	OA332/OA332D2/OA332D4	3-213
	OA4111/OA4111D2	3-217
Complex Cells	SCG1/SCG1D2	3-220
	SCG2/SCG2D2	3-223
	SCG3/SCGD2	3-225
	SCG4/SCG4D2	3-228
	SCG5/SCG5D2	3-231
	SCG6/SCG6D2	3-234
	SCG7/SCG7D2	3-236
	SCG8/SCG8D2	3-239
	SCG9/SCG9D2	3-241
	SCG10/SCG10D2	3-243
	SCG11/SCG11D2	3-246
	SCG12/SCG12D2	3-248
	SCG13/SCG13D2	3-250
	SCG14/SCG14D2	3-252
	SCG15/SCG15D2	3-254
	SCG16/SCG16D2	3-256
	SCG17/SCG17D2	3-258



Cell Type	Cell Name	Page
Complex Cells	SCG18/SCG18D2	3-260
	SCG19/SCG19D2	3-263
	SCG20/SCG20D2	3-265
	SCG21/SCG21D2	3-267
	SCG22/SCG22D2	3-269
Delay Cells	DL1D2/DL1D4	3-271
	DL2D2/DL2D4	3-272
	DL3D2/DL3D4	3-273
	DL4D2/DL4D4	3-274
	DL5D2/DL5D4	3-275
	DL10D2/DL10D4	3-276
Inverters	IVDH/IV/IVD2/IVD3/IVD4/IVD6/IVD8/IVD16	3-277
	IVCD(11/13)/IVCD(22/26)/IVCD44	3-280
Inverting Tri-State Buffers	IVT/IVTD2/IVTD4/IVTD8/IVTD16	3-282
	IVTN/IVTND2/IVTND4/IVTND8/IVTND16	3-284
Non-Inverting Buffers	NIDH/NID/NID2/NID3/NID4/NID6/NID8/NID16	3-286
Clock Buffers for OAK core only	OAK_NID10P/OAK_NID 20P	3-289
Non-Inverting Tri-State Buffers	NIT/NITD2/NITD4/NITD8/NITD16	3-290
	NITN/NITND2/NITND4/NITND8/NITND16	3-293
2 Phase Clock Generator Buffers for OAK core only	OAK_DUCLK10/OAK_DUCLK16	3-296
Clock Tree Synthesis Buffers	CTSB/2/3/4/6/8/16	3-298

## Flip-Flops

Cell Type	Cell Name	Page
D Flip-Flop	FD1/FD1D2	3-303
	FD1CS/FD1CSD2	3-305
	FD1S/FD1SD2	3-307
	FD1SQ/FD1SQD2	3-309
	FD1Q/FD1QD2	3-311
D Flip-Flop with Reset	FD2/FD2D2	3-313
	FD2CS/FD2CSD2	3-315
	FD2S/FD2SD2	3-319
	FD2SQ/FD2SQD2	3-321
	FD2Q/FD2QD2	3-323
D Flip-Flop with Set	FD3/FD3D2	3-325
	FD3CS/FD3CSD2	3-327
	FD3S/FD3SD2	3-331
	FD3SQ/FD3SQD2	3-333
	FD3Q/FD3QD2	3-335



Cell Type	Cell Name	Page
D Flip-Flop with Reset, Set	FD4/FD4D2	3-337
	FD4CS/FD4CSD2	3-340
	FD4S/FD4SD2	3-344
	FD4SQ/FD4SQD2	3-348
	FD4Q/FD4QD2	3-351
D Flip-Flop with Negative Edge Trigger	FD5/FD5D2	3-353
	FD5S/FD5SD2	3-355
	FD6/FD6D2	3-357
	FD6S/FD6SD2	3-359
	FD7/FD7D2	3-361
	FD7S/FD7SD2	3-363
	FD8/FD8D2	3-365
	FD8S/FD8SD2	3-368
D Flip-Flop with Synchronous Clear	FDS2/FDS2D2	3-372
	FDS2CS/FDS2CSD2	3-374
	FDS2S/FDS2SD2	3-376
	FDS3/FDS3D2	3-378
	FDS3CS/FDS3CSD2	3-380
	FDS3S/FDS3SD2	3-382
JK Flip-Flop	FJ1/FJ1D2	3-384
	FJ1S/FJ1SD2	3-386
	FJ2/FJ2D2	3-388
	FJ2S/FJ2SD2	3-390
	FJ4/FJ4D2	3-392
	FJ4S/FJ4SD2	3-395
Toggle Flip-Flop	FT2/FT2D2	3-398

## Latches

Cell Type	Cell Name	Page
D Latch with Active High	LD1/LD1D2	3-402
	LD1A/LD1D2A	3-404
	LD1Q/LD1QD2	3-406
	LD2/LD2D2	3-408
	LD2Q/LD2QD2	3-411
	LD3/LD3D2	3-413
	LD4/LD4D2	3-416
D Latch with Active Low	LD5/LD5D2	3-419
	LD5Q/LD5QD2	3-421
	LD6/LD6D2	3-423
	LD6Q/LD6QD2	3-426



Cell Type	Cell Name	Page
	LD7/LD7D2	3-428
	LD8/LD8D2	3-431
D Latch with Active Low for OAK core only	OAK_LDI2/OAK_LDI2D2	3-434
	OAK_LDI3/OAK_LDI3D2	3-437
SR Latch	LS0/LS0D2	3-442
	LS1/LS1D2	3-444

## Bus Holder

Cell Type	Cell Name	Page
Bus Holder	BUSHOLDER	3-448

## Internal Clock Drivers

Cell Type	Cell Name	Page
Internal Clock Drivers	CK(2/4/6/8)	3-449

## Decoders

Cell Type	Cell Name	Page
Non-Inverting Decoder	DC4	3-452
Inverting Decoders	DC4I	3-454
	DC8I	3-456

## Adders

Cell Type	Cell Name	Page
Full Adders	FADH/FA/FAD2	3-461
Half Adders	HADH/HA/HAD2	3-464
Complex Cells	SCG23/SCG23D2	3-467

## Multiplexers

Cell Type	Cell Name	Page
2 > 1 Non-Inverting Mux	MX2DH/MX2/MX2D2/MX2D4	3-471
	MX2X4	3-474
2 > 1 Inverting Mux	MX2IDH/MX2I/MX2ID2/MX2ID4	3-477
	MX2IDHA/MX2IA/MX2ID2A/MX2ID4A	3-480
	MX2IX4	3-483
3 > 1 Inverting Mux	MX3I/MX3ID2/MX3ID4	3-486
4 > 1 Non-Inverting Mux	MX4/MX4D2/MX4D4	3-490
8 > 1 Non-Inverting Mux	MX8/MX8D2/MX8D4	3-494



## Cell Names & Function Descriptions

Cell Name	Function Description
AD2DH	2-Input AND with 0.5X Drive
AD2	2-Input AND with 1X Drive
AD2D2	2-Input AND with 2X Drive
AD2D4	2-Input AND with 4X Drive
AD3DH	3-Input AND with 0.5X Drive
AD3	3-Input AND with 1X Drive
AD3D2	3-Input AND with 2X Drive
AD3D4	3-Input AND with 4X Drive
AD4DH	4-Input AND with 0.5X Drive
AD4	4-Input AND with 1X Drive
AD4D2	4-Input AND with 2X Drive
AD4D4	4-Input AND with 4X Drive
AD5	5-Input AND with 1X Drive
AD5D2	5-Input AND with 2X Drive
AD5D4	5-Input AND with 4X Drive
ND2DH	2-Input NAND with 0.5X Drive
ND2	2-Input NAND with 1X Drive
ND2D2	2-Input NAND with 2X Drive
ND2D4	2-Input NAND with 4X Drive
ND3DH	3-Input NAND with 0.5X Drive
ND3	3-Input NAND with 1X Drive
ND3D2	3-Input NAND with 2X Drive
ND3D4	3-Input NAND with 4X Drive
ND4DH	4-Input NAND with 0.5X Drive
ND4	4-Input NAND with 1X Drive
ND4D2	4-Input NAND with 2X Drive
ND4D2B	4-Input NAND with 2X (Buffered) Drive
ND4D4	4-Input NAND with 4X Drive
ND5	5-Input NAND with 1X Drive
ND5D2	5-Input NAND with 2X Drive
ND5D4	5-Input NAND with 4X Drive
ND6	6-Input NAND with 1X Drive
ND6D2	6-Input NAND with 2X Drive
ND6D4	6-Input NAND with 4X Drive
ND8	8-Input NAND with 1X Drive
ND8D2	8-Input NAND with 2X Drive
ND8D4	8-Input NAND with 4X Drive



## LOGIC CELLS

### Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
NR2DH	2-Input NOR with 0.5X Drive
NR2	2-Input NOR with 1X Drive
NR2D2	2-Input NOR with 2X Drive
NR2D2B	2-Input NOR with 2X (Buffered) Drive
NR2D4	2-Input NOR with 4X Drive
NR2A	NR2 with 2X P-Transistor, 1X N-Transistor
NR3DH	3-Input NOR with 0.5X Drive
NR3	3-Input NOR with 1X Drive
NR3D2	3-Input NOR with 2X Drive
NR3D2B	3-Input NOR with 2X (Buffered) Drive
NR3D4	3-Input NOR with 4X Drive
NR3A	NR3 with 2X P-Transistor, 1X N-Transistor
NR4DH	4-Input NOR with 0.5X Drive
NR4	4-Input NOR with 1X Drive
NR4D2	4-Input NOR with 2X Drive
NR4D4	4-Input NOR with 4X Drive
NR5	5-Input NOR with 1X Drive
NR5D2	5-Input NOR with 2X Drive
NR5D4	5-Input NOR with 4X Drive
NR6	6-Input NOR with 1X Drive
NR6D2	6-Input NOR with 2X Drive
NR6D4	6-Input NOR with 4X Drive
NR8	8-Input NOR with 1X Drive
NR8D2	8-Input NOR with 2X Drive
NR8D4	8-Input NOR with 4X Drive
OR2DH	2-Input OR with 0.5X Drive
OR2	2-Input OR with 1X Drive
OR2D2	2-Input OR with 2X Drive
OR2D4	2-Input OR with 4X Drive
OR3DH	3-Input OR with 0.5X Drive
OR3	3-Input OR with 1X Drive
OR3D2	3-Input OR with 2X Drive
OR3D4	3-Input OR with 4X Drive
OR4DH	4-Input OR with 0.5X Drive
OR4	4-Input OR with 1X Drive
OR4D2	4-Input OR with 2X Drive
OR4D4	4-Input OR with 4X Drive



**Cell Names & Function Descriptions (Continued)**

Cell Name	Function Description
OR5	5-Input OR with 1X Drive
OR5D2	5-Input OR with 2X Drive
OR5D4	5-Input OR with 4X Drive
XN2	2-Input Exclusive-NOR with 1X Drive
XN2D2	2-Input Exclusive-NOR with 2X Drive
XN2D4	2-Input Exclusive-NOR with 4X Drive
XN3	3-Input Exclusive-NOR with 1X Drive
XN3D2	3-Input Exclusive-NOR with 2X Drive
XN3D4	3-Input Exclusive-NOR with 4X Drive
XO2	2-Input Exclusive-OR with 1X Drive
XO2D2	2-Input Exclusive-OR with 2X Drive
XO2D4	2-Input Exclusive-OR with 4X Drive
XO3	3-Input Exclusive-OR with 1X Drive
XO3D2	3-Input Exclusive-OR with 2X Drive
XO3D4	3-Input Exclusive-OR with 4X Drive
AO21DH	2-AND into 2-NOR with 0.5X Drive
AO21	2-AND into 2-NOR with 1X Drive
AO21D2	2-AND into 2-NOR with 2X Drive
AO21D2B	2-AND into 2-NOR with 2X(Buffered) Drive
AO21D4	2-AND into 2-NOR with 4X Drive
AO211DH	2-AND into 3-NOR with 0.5X Drive
AO211	2-AND into 3-NOR with 1X Drive
AO211D2	2-AND into 3-NOR with 2X Drive
AO211D2B	2-AND into 3-NOR with 2X(Buffered) Drive
AO211D4	2-AND into 3-NOR with 4X Drive
AO2111	2-AND into 4-NOR with 1X Drive
AO2111D2	2-AND into 4-NOR with 2X Drive
AO22DH	Two 2-ANDs into 2-NOR with 0.5X Drive
AO22	Two 2-ANDs into 2-NOR with 1X Drive
AO22D2	Two 2-ANDs into 2-NOR with 2X Drive
AO22D2B	Two 2-ANDs into 2-NOR with 2X(Buffered) Drive
AO22D4	Two 2-ANDs into 2-NOR with 4X Drive
AO22DHA	2-AND and 2-NOR into 2-NOR with 0.5X Drive
AO22A	2-AND and 2-NOR into 2-NOR with 1X Drive
AO22D2A	2-AND and 2-NOR into 2-NOR with 2X Drive
AO22D4A	2-AND and 2-NOR into 2-NOR with 4X Drive



## LOGIC CELLS

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### Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
AO221	Two 2-ANDs into 3-NOR with 1X Drive
AO221D2	Two 2-ANDs into 3-NOR with 2X Drive
AO221D4	Two 2-ANDs into 3-NOR with 4X Drive
AO222	Three 2-ANDs into 3-NOR with 1X Drive
AO222D2	Three 2-ANDs into 3-NOR with 2X Drive
AO222D2B	Three 2-ANDs into 3-NOR with 2X(Buffered) Drive
AO222D4	Three 2-ANDs into 3-NOR with 4X Drive
AO222A	Inverting 2-of-3 Majority with 1X Drive
AO222D2A	Inverting 2-of-3 Majority with 2X Drive
AO222D4A	Inverting 2-of-3 Majority with 4X Drive
AO2222	Four 2-ANDs into 4-NOR with 1X Drive
AO2222D2	Four 2-ANDs into 4-NOR with 2X Drive
AO2222D4	Four 2-ANDs into 4-NOR with 4X Drive
AO31DH	3-AND into 2-NOR with 0.5X Drive
AO31	3-AND into 2-NOR with 1X Drive
AO31D2	3-AND into 2-NOR with 2X Drive
AO31D4	3-AND into 2-NOR with 4X Drive
AO311	3-AND into 3-NOR with 1X Drive
AO311D2	3-AND into 3-NOR with 2X Drive
AO311D4	3-AND into 3-NOR with 4X Drive
AO3111	3-AND into 4-NOR with 1X Drive
AO3111D2	3-AND into 4-NOR with 2X Drive
AO32	3-AND and 2-AND into 2-NOR with 1X Drive
AO32D2	3-AND and 2-AND into 2-NOR with 2X Drive
AO32D4	3-AND and 2-AND into 2-NOR with 4X Drive
AO321	3-AND and 2-AND into 3-NOR with 1X Drive
AO321D2	3-AND and 2-AND into 3-NOR with 2X Drive
AO321D4	3-AND and 2-AND into 3-NOR with 4X Drive
AO322	3-AND and Two 2-ANDs into 3-NOR with 1X Drive
AO322D2	3-AND and Two 2-ANDs into 3-NOR with 2X Drive
AO322D4	3-AND and Two 2-ANDs into 3-NOR with 4X Drive
AO33	Two 3-ANDs into 2-NOR with 1X Drive
AO33D2	Two 3-ANDs into 2-NOR with 2X Drive
AO33D4	Two 3-ANDs into 2-NOR with 4X Drive
AO331	Two 3-ANDs into 3-NOR with 1X Drive
AO331D2	Two 3-ANDs into 3-NOR with 2X Drive
AO331D4	Two 3-ANDs into 3-NOR with 4X Drive



## Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
AO332	Two 3-ANDs and 2-AND into 3-NOR
AO332D2	Two 3-ANDs and 2-AND into 3-NOR with 2X Drive
AO332D4	Two 3-ANDs and 2-AND into 3-NOR with 4X Drive
AO4111	4-AND into 4-NOR with 1X Drive
AO4111D2	4-AND into 4-NOR with 2X Drive
OA21DH	2-OR into 2-NAND with 0.5X Drive
OA21	2-OR into 2-NAND with 1X Drive
OA21D2	2-OR into 2-NAND with 2X Drive
OA21D2B	2-OR into 2-NAND with 2X(Buffered) Drive
OA21D4	2-OR into 2-NAND with 4X Drive
OA211DH	2-OR into 3-NAND with 0.5X Drive
OA211	2-OR into 3-NAND with 1X Drive
OA211D2	2-OR into 3-NAND with 2X Drive
OA211D2B	2-OR into 3-NAND with 2X(Buffered) Drive
OA211D4	2-OR into 3-NAND with 4X Drive
OA2111	2-OR into 4-NAND with 1X Drive
OA2111D2	2-OR into 4-NAND with 2X Drive
OA22DH	Two 2-ORs into 2-NAND with 0.5X Drive
OA22	Two 2-ORs into 2-NAND with 1X Drive
OA22D2	Two 2-ORs into 2-NAND with 2X Drive
OA22D2B	Two 2-ORs into 2-NAND with 2X(Buffered) Drive
OA22D4	Two 2-ORs into 2-NAND with 4X Drive
OA22DHA	2-OR and 2-NAND into 2-NAND with 0.5X Drive
OA22A	2-OR and 2-NAND into 2-NAND with 1X Drive
OA22D2A	2-OR and 2-NAND into 2-NAND with 2X Drive
OA22D4A	2-OR and 2-NAND into 2-NAND with 4X Drive
OA221	Two 2-ORs into 3-NAND with 1X Drive
OA221D2	Two 2-ORs into 3-NAND with 2X Drive
OA221D4	Two 2-ORs into 3-NAND with 4X Drive
OA222	Three 2-ORs into 3-NAND with 1X Drive
OA222D2	Three 2-ORs into 3-NAND with 2X Drive
OA222D2B	Three 2-ORs into 3-NAND with 2X(Buffered) Drive
OA222D4	Three 2-ORs into 3-NAND with 4X Drive
OA2222	Four 2-ORs into 4-NAND with 1X Drive
OA2222D2	Four 2-ORs into 4-NAND with 2X Drive
OA2222D4	Four 2-ORs into 4-NAND with 4X Drive



## LOGIC CELLS

### Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
OA31DH	3-OR into 2-NAND with 0.5X Drive
OA31	3-OR into 2-NAND with 1X Drive
OA31D2	3-OR into 2-NAND with 2X Drive
OA31D4	3-OR into 2-NAND with 4X Drive
OA311	3-OR into 3-NAND with 1X Drive
OA311D2	3-OR into 3-NAND with 2X Drive
OA311D4	3-OR into 3-NAND with 4X Drive
OA3111	3-OR into 4-NAND with 1X Drive
OA3111D2	3-OR into 4-NAND with 2X Drive
OA32	3-OR and 2-OR into 2-NAND with 1X Drive
OA32D2	3-OR and 2-OR into 2-NAND with 2X Drive
OA32D4	3-OR and 2-OR into 2-NAND with 4X Drive
OA321	3-OR and 2-OR into 3-NAND with 1X Drive
OA321D2	3-OR and 2-OR into 3-NAND with 2X Drive
OA321D4	3-OR and 2-OR into 3-NAND with 4X Drive
OA322	3-OR and Two 2-ORs into 3-NAND with 1X Drive
OA322D2	3-OR and Two 2-ORs into 3-NAND with 2X Drive
OA322D4	3-OR and Two 2-ORs into 3-NAND with 4X Drive
OA33	Two 3-ORs into 2-NAND with 1X Drive
OA33D2	Two 3-ORs into 2-NAND with 2X Drive
OA33D4	Two 3-ORs into 2-NAND with 4X Drive
OA331	Two 3-ORs into 3-NAND with 1X Drive
OA331D2	Two 3-ORs into 3-NAND with 2X Drive
OA331D4	Two 3-ORs into 3-NAND with 4X Drive
OA332	Two 3-ORs and 2-OR into 3-NAND with 1X Drive
OA332D2	Two 3-ORs and 2-OR into 3-NAND with 2X Drive
OA332D4	Two 3-ORs and 2-OR into 3-NAND with 4X Drive
OA4111	4-OR into 4-NAND with 1X Drive
OA4111D2	4-OR into 4-NAND with 2X Drive
SCG1	2-NAND and two (2-AND into 2-NOR)s into 3-NAND
SCG1D2	2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 2X Drive
SCG2	Two 2-ANDs into 2-OR
SCG2D2	Two 2-ANDs into 2-OR with 2X Drive
SCG3	Two 2-NANDs into 3-NAND
SCG3D2	Two 2-NANDs into 3-NAND with 2X Drive
SCG4	Two (two 2-ANDs into 2-NOR)s into 2-NAND
SCG4D2	Two (two 2-ANDs into 2-NOR)s into 2-NAND with 2X Drive



## Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
SCG5	Three 2-ANDs into 3-OR
SCG5D2	Three 2-ANDs into 3-OR with 2X Drive
SCG6	2-AND into 2-OR
SCG6D2	2-AND into 2-OR with 2X Drive
SCG7	2-NAND and (2-AND into 2-NOR) into 2-NAND
SCG7D2	2-NAND and (2-AND into 2-NOR) into 2-NAND with 2X Drive
SCG8	2-AND into 3-OR
SCG8D2	2-AND into 3-OR with 2X Drive
SCG9	2-OR into 2-AND
SCG9D2	2-OR into 2-AND with 2X Drive
SCG10	Two 2-ORs into 2-AND
SCG10D2	Two 2-ORs into 2-AND with 2X Drive
SCG11	Two 2-NORs into 3-NOR
SCG11D2	Two 2-NORs into 3-NOR with 2X Drive
SCG12	2-NAND into 2-NOR
SCG12D2	2-NAND into 2-NOR with 2X Drive
SCG13	2-NOR into 2-NAND
SCG13D2	2-NOR into 2-NAND with 2X Drive
SCG14	2-NAND into 2-NAND
SCG14D2	2-NAND into 2-NAND with 2X Drive
SCG15	2-NAND into 3-NAND
SCG15D2	2-NAND into 3-NAND with 2X Drive
SCG16	2-OR with one inverted input into 2-NAND
SCG16D2	2-OR with one inverted input into 2-NAND with 2X Drive
SCG17	2-AND into 2-NOR into 2-NAND
SCG17D2	2-AND into 2-NOR into 2-NAND with 2X Drive
SCG18	2-AND into 2-NOR into 3-NAND
SCG18D2	2-AND into 2-NOR into 3-NAND with 2X Drive
SCG19	2-AND into 2-AND into 2-NOR
SCG19D2	2-AND into 2-AND into 2-NOR with 2X Drive
SCG20	2-NOR into 2-NOR
SCG20D2	2-NOR into 2-NOR with 2X Drive
SCG21	2-NOR into 3-NOR
SCG21D2	2-NOR into 3-NOR with 2X Drive
SCG22	2-NAND into 2-OR into 2-NAND
SCG22D2	2-NAND into 2-OR into 2-NAND with 2X Drive
SCG23	Full Adder with one inverted input with 1X Drive
SCG23D2	Full Adder with one inverted input with 2X Drive



## LOGIC CELLS

### Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
DL1D2	1ns Delay Cell with 2X Drive
DL1D4	1ns Delay Cell with 4X Drive
DL2D2	2ns Delay Cell with 2X Drive
DL2D4	2ns Delay Cell with 4X Drive
DL3D2	3ns Delay Cell with 2X Drive
DL3D4	3ns Delay Cell with 4X Drive
DL4D2	4ns Delay Cell with 2X Drive
DL4D4	4ns Delay Cell with 4X Drive
DL5D2	5ns Delay Cell with 2X Drive
DL5D4	5ns Delay Cell with 4X Drive
DL10D2	10ns Delay Cell with 2X Drive
DL10D4	10ns Delay Cell with 4X Drive
IVDH	Inverter with 0.5X Drive
IV	Inverter with 1X Drive
IVD2	Inverter with 2X Drive
IVD3	Inverter with 3X Drive
IVD4	Inverter with 4X Drive
IVD6	Inverter with 6X Drive
IVD8	Inverter with 8X Drive
IVD16	Inverter with 16X Drive
IVCD11	1X Inverter into 1X Inverter
IVCD13	1X Inverter into 3X Inverter
IVCD22	2X Inverter into 2X Inverter
IVCD26	2X Inverter into 6X Inverter
IVCD44	4X Inverter into 4X Inverter
IVT	Inverting Tri-State Buffer with Enable High, 1X Drive
IVTD2	Inverting Tri-State Buffer with Enable High, 2X Drive
IVTD4	Inverting Tri-State Buffer with Enable High, 4X Drive
IVTD8	Inverting Tri-State Buffer with Enable High, 8X Drive
IVTD16	Inverting Tri-State Buffer with Enable High, 16X Drive
IVTN	Inverting Tri-State Buffer with Enable Low, 1X Drive
IVTND2	Inverting Tri-State Buffer with Enable Low, 2X Drive
IVTND4	Inverting Tri-State Buffer with Enable Low, 4X Drive
IVTND8	Inverting Tri-State Buffer with Enable Low, 8X Drive
IVTND16	Inverting Tri-State Buffer with Enable Low, 16X Drive
NIDH	Non-Inverting Buffer with 0.5X Drive
NID	Non-Inverting Buffer with 1X Drive
NID2	Non-Inverting Buffer with 2X Drive



## Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
NID3	Non-Inverting Buffer with 3X Drive
NID4	Non-Inverting Buffer with 4X Drive
NID6	Non-Inverting Buffer with 6X Drive
NID8	Non-Inverting Buffer with 8X Drive
NID16	Non-Inverting Buffer with 16X Drive
OAK_NID10P	Clock Buffer for 10pF Drive (for OAK core only)
OAK_NID20P	Clock Buffer for 20pF Drive (for OAK core only)
NIT	Non-Inverting Tri-State Buffer with Enable High, 1X Drive
NITD2	Non-Inverting Tri-State Buffer with Enable High, 2X Drive
NITD4	Non-Inverting Tri-State Buffer with Enable High, 4X Drive
NITD8	Non-Inverting Tri-State Buffer with Enable High, 8X Drive
NITD16	Non-Inverting Tri-State Buffer with Enable High, 16X Drive
NITN	Non-Inverting Tri-State Buffer with Enable Low, 1X Drive
NITND2	Non-Inverting Tri-State Buffer with Enable Low, 2X Drive
NITND4	Non-Inverting Tri-State Buffer with Enable Low, 4X Drive
NITND8	Non-Inverting Tri-State Buffer with Enable Low, 8X Drive
NITND16	Non-Inverting Tri-State Buffer with Enable Low, 16X Drive
OAK_DUCLK10	2 Phase Clock Generator (1ns Non-overlapped, for OAK core only)
OAK_DUCLK16	2 Phase Clock Generator (1.6ns Non-overlapped, for OAK core only)
CTSB	Clock Tree Synthesis Buffer with 1X Drive
CTSBD2	Clock Tree Synthesis Buffer with 2X Drive
CTSBD3	Clock Tree Synthesis Buffer with 3X Drive
CTSBD4	Clock Tree Synthesis Buffer with 4X Drive
CTSBD6	Clock Tree Synthesis Buffer with 6X Drive
CTSBD8	Clock Tree Synthesis Buffer with 8X Drive
CTSBD16	Clock Tree Synthesis Buffer with 16X Drive



## NOTE

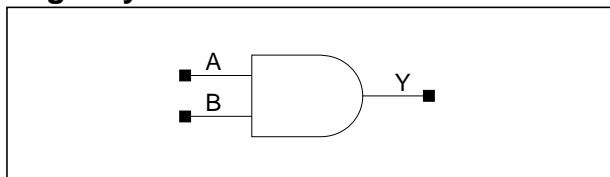
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## AD2DH/AD2/AD2D2/AD2D4

### 2-Input AND with 0.5X/1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

#### Cell Data

Input Load (SL)								Gate Count			
AD2DH		AD2		AD2D2		AD2D4		AD2DH	AD2	AD2D2	AD2D4
A	B	A	B	A	B	A	B				
0.6	0.6	0.8	0.9	0.8	0.8	1.1	1.2	1.33	1.33	1.67	2.33

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### AD2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.195	$0.068 + 0.063 \cdot \text{SL}$	$0.060 + 0.065 \cdot \text{SL}$	$0.052 + 0.066 \cdot \text{SL}$
	$t_F$	0.156	$0.056 + 0.050 \cdot \text{SL}$	$0.049 + 0.052 \cdot \text{SL}$	$0.043 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.128 + 0.030 \cdot \text{SL}$	$0.132 + 0.029 \cdot \text{SL}$	$0.133 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.188	$0.131 + 0.029 \cdot \text{SL}$	$0.136 + 0.027 \cdot \text{SL}$	$0.137 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.194	$0.067 + 0.064 \cdot \text{SL}$	$0.060 + 0.065 \cdot \text{SL}$	$0.053 + 0.066 \cdot \text{SL}$
	$t_F$	0.159	$0.060 + 0.049 \cdot \text{SL}$	$0.052 + 0.051 \cdot \text{SL}$	$0.044 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.183	$0.123 + 0.030 \cdot \text{SL}$	$0.128 + 0.029 \cdot \text{SL}$	$0.129 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.203	$0.145 + 0.029 \cdot \text{SL}$	$0.151 + 0.027 \cdot \text{SL}$	$0.152 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

##### AD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.118	$0.061 + 0.028 \cdot \text{SL}$	$0.059 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$
	$t_F$	0.103	$0.055 + 0.024 \cdot \text{SL}$	$0.051 + 0.025 \cdot \text{SL}$	$0.044 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.150	$0.120 + 0.015 \cdot \text{SL}$	$0.126 + 0.014 \cdot \text{SL}$	$0.129 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.155	$0.124 + 0.016 \cdot \text{SL}$	$0.131 + 0.014 \cdot \text{SL}$	$0.133 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.118	$0.061 + 0.029 \cdot \text{SL}$	$0.058 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$
	$t_F$	0.104	$0.055 + 0.025 \cdot \text{SL}$	$0.052 + 0.025 \cdot \text{SL}$	$0.047 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.144	$0.114 + 0.015 \cdot \text{SL}$	$0.120 + 0.014 \cdot \text{SL}$	$0.124 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.169	$0.138 + 0.016 \cdot \text{SL}$	$0.145 + 0.014 \cdot \text{SL}$	$0.148 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AD2DH/AD2/AD2D2/AD2D4

### 2-Input AND with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### AD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.090	$0.062 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.079	$0.052 + 0.014 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.154	$0.136 + 0.009 \cdot \text{SL}$	$0.142 + 0.007 \cdot \text{SL}$	$0.152 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.162	$0.142 + 0.010 \cdot \text{SL}$	$0.150 + 0.008 \cdot \text{SL}$	$0.159 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.091	$0.061 + 0.015 \cdot \text{SL}$	$0.063 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.014 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.147	$0.129 + 0.009 \cdot \text{SL}$	$0.135 + 0.007 \cdot \text{SL}$	$0.145 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.175	$0.155 + 0.010 \cdot \text{SL}$	$0.163 + 0.008 \cdot \text{SL}$	$0.173 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### AD2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.083	$0.068 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$	$0.064 + 0.008 \cdot \text{SL}$
	$t_F$	0.071	$0.057 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.162	$0.151 + 0.005 \cdot \text{SL}$	$0.157 + 0.004 \cdot \text{SL}$	$0.171 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.164	$0.153 + 0.006 \cdot \text{SL}$	$0.159 + 0.004 \cdot \text{SL}$	$0.173 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.082	$0.066 + 0.008 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.064 + 0.008 \cdot \text{SL}$
	$t_F$	0.074	$0.059 + 0.008 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.155	$0.144 + 0.005 \cdot \text{SL}$	$0.149 + 0.004 \cdot \text{SL}$	$0.164 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.164 + 0.006 \cdot \text{SL}$	$0.170 + 0.004 \cdot \text{SL}$	$0.185 + 0.004 \cdot \text{SL}$

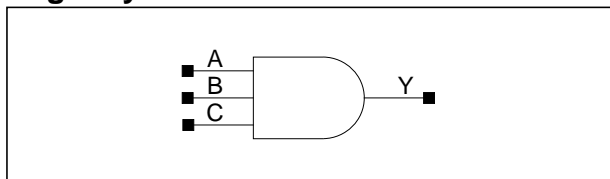
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# AD3DH/AD3/AD3D2/AD3D4

## 3-Input AND with 0.5X/1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

### Cell Data

Input Load (SL)												Gate Count			
AD3DH			AD3			AD3D2			AD3D4			AD3DH	AD3	AD3D2	AD3D4
A	B	C	A	B	C	A	B	C	A	B	C				
0.5	0.6	0.6	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.0	1.1	1.67	1.67	2.00	2.67

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AD3DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.209	$0.082 + 0.064 \cdot \text{SL}$	$0.079 + 0.064 \cdot \text{SL}$	$0.069 + 0.066 \cdot \text{SL}$
	$t_F$	0.163	$0.063 + 0.050 \cdot \text{SL}$	$0.060 + 0.051 \cdot \text{SL}$	$0.051 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.231	$0.167 + 0.032 \cdot \text{SL}$	$0.178 + 0.029 \cdot \text{SL}$	$0.182 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.218	$0.159 + 0.030 \cdot \text{SL}$	$0.168 + 0.027 \cdot \text{SL}$	$0.171 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.210	$0.084 + 0.063 \cdot \text{SL}$	$0.079 + 0.064 \cdot \text{SL}$	$0.069 + 0.066 \cdot \text{SL}$
	$t_F$	0.168	$0.068 + 0.050 \cdot \text{SL}$	$0.063 + 0.051 \cdot \text{SL}$	$0.054 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.233	$0.169 + 0.032 \cdot \text{SL}$	$0.180 + 0.029 \cdot \text{SL}$	$0.184 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.234	$0.174 + 0.030 \cdot \text{SL}$	$0.184 + 0.028 \cdot \text{SL}$	$0.188 + 0.027 \cdot \text{SL}$
C to Y	$t_R$	0.210	$0.084 + 0.063 \cdot \text{SL}$	$0.078 + 0.064 \cdot \text{SL}$	$0.068 + 0.066 \cdot \text{SL}$
	$t_F$	0.171	$0.072 + 0.050 \cdot \text{SL}$	$0.068 + 0.051 \cdot \text{SL}$	$0.058 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.232	$0.167 + 0.032 \cdot \text{SL}$	$0.179 + 0.029 \cdot \text{SL}$	$0.183 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.248	$0.187 + 0.031 \cdot \text{SL}$	$0.199 + 0.028 \cdot \text{SL}$	$0.203 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### AD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.130	$0.072 + 0.029 \cdot \text{SL}$	$0.072 + 0.029 \cdot \text{SL}$	$0.067 + 0.030 \cdot \text{SL}$
	$t_F$	0.108	$0.059 + 0.025 \cdot \text{SL}$	$0.056 + 0.025 \cdot \text{SL}$	$0.053 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.146 + 0.017 \cdot \text{SL}$	$0.155 + 0.014 \cdot \text{SL}$	$0.163 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.178	$0.145 + 0.017 \cdot \text{SL}$	$0.153 + 0.014 \cdot \text{SL}$	$0.158 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.133	$0.078 + 0.028 \cdot \text{SL}$	$0.071 + 0.029 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.111	$0.060 + 0.025 \cdot \text{SL}$	$0.062 + 0.025 \cdot \text{SL}$	$0.056 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.180	$0.147 + 0.017 \cdot \text{SL}$	$0.157 + 0.014 \cdot \text{SL}$	$0.164 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.193	$0.160 + 0.017 \cdot \text{SL}$	$0.169 + 0.015 \cdot \text{SL}$	$0.174 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.131	$0.073 + 0.029 \cdot \text{SL}$	$0.071 + 0.029 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$
	$t_F$	0.114	$0.064 + 0.025 \cdot \text{SL}$	$0.065 + 0.025 \cdot \text{SL}$	$0.059 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.146 + 0.017 \cdot \text{SL}$	$0.155 + 0.014 \cdot \text{SL}$	$0.162 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.206	$0.173 + 0.017 \cdot \text{SL}$	$0.182 + 0.015 \cdot \text{SL}$	$0.188 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AD3DH/AD3/AD3D2/AD3D4

### 3-Input AND with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### AD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.104	$0.073 + 0.015 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$	$0.074 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.057 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.166 + 0.010 \cdot \text{SL}$	$0.175 + 0.008 \cdot \text{SL}$	$0.190 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.183	$0.162 + 0.010 \cdot \text{SL}$	$0.170 + 0.008 \cdot \text{SL}$	$0.183 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.105	$0.074 + 0.016 \cdot \text{SL}$	$0.077 + 0.015 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.063 + 0.014 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.189	$0.168 + 0.010 \cdot \text{SL}$	$0.176 + 0.008 \cdot \text{SL}$	$0.192 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.197	$0.176 + 0.011 \cdot \text{SL}$	$0.185 + 0.008 \cdot \text{SL}$	$0.199 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.105	$0.075 + 0.015 \cdot \text{SL}$	$0.076 + 0.015 \cdot \text{SL}$	$0.074 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.069 + 0.014 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.186	$0.165 + 0.011 \cdot \text{SL}$	$0.174 + 0.008 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.209	$0.187 + 0.011 \cdot \text{SL}$	$0.197 + 0.009 \cdot \text{SL}$	$0.212 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### AD3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.104	$0.090 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$
	$t_F$	0.083	$0.068 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.203	$0.190 + 0.006 \cdot \text{SL}$	$0.198 + 0.005 \cdot \text{SL}$	$0.217 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.193	$0.181 + 0.006 \cdot \text{SL}$	$0.187 + 0.005 \cdot \text{SL}$	$0.206 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.104	$0.090 + 0.007 \cdot \text{SL}$	$0.087 + 0.008 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$
	$t_F$	0.088	$0.073 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.204	$0.192 + 0.006 \cdot \text{SL}$	$0.199 + 0.005 \cdot \text{SL}$	$0.219 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.206	$0.193 + 0.006 \cdot \text{SL}$	$0.201 + 0.005 \cdot \text{SL}$	$0.220 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.105	$0.090 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$
	$t_F$	0.093	$0.077 + 0.008 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.202	$0.189 + 0.006 \cdot \text{SL}$	$0.196 + 0.005 \cdot \text{SL}$	$0.216 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.218	$0.205 + 0.007 \cdot \text{SL}$	$0.213 + 0.005 \cdot \text{SL}$	$0.233 + 0.004 \cdot \text{SL}$

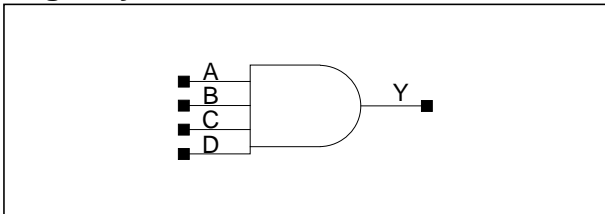
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## AD4DH/AD4/AD4D2/AD4D4

### 4-Input AND with 0.5X/1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

#### Cell Data

Input Load (SL)															
AD4DH				AD4				AD4D2				AD4D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.5	0.5	0.5	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.9	0.9	0.9	1.0
Gate Counts															
AD4DH				AD4				AD4D2				AD4D4			
2.00				2.00				2.33				3.00			



## AD4DH/AD4/AD4D2/AD4D4

### 4-Input AND with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### AD4DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.224	$0.097 + 0.064 \cdot \text{SL}$	$0.095 + 0.064 \cdot \text{SL}$	$0.086 + 0.065 \cdot \text{SL}$
	$t_F$	0.172	$0.072 + 0.050 \cdot \text{SL}$	$0.069 + 0.051 \cdot \text{SL}$	$0.059 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.255	$0.187 + 0.034 \cdot \text{SL}$	$0.203 + 0.030 \cdot \text{SL}$	$0.212 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.178 + 0.031 \cdot \text{SL}$	$0.191 + 0.028 \cdot \text{SL}$	$0.196 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.225	$0.098 + 0.064 \cdot \text{SL}$	$0.097 + 0.064 \cdot \text{SL}$	$0.086 + 0.065 \cdot \text{SL}$
	$t_F$	0.177	$0.079 + 0.049 \cdot \text{SL}$	$0.073 + 0.051 \cdot \text{SL}$	$0.063 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.265	$0.197 + 0.034 \cdot \text{SL}$	$0.213 + 0.030 \cdot \text{SL}$	$0.222 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.260	$0.197 + 0.031 \cdot \text{SL}$	$0.211 + 0.028 \cdot \text{SL}$	$0.216 + 0.027 \cdot \text{SL}$
C to Y	$t_R$	0.226	$0.099 + 0.063 \cdot \text{SL}$	$0.096 + 0.064 \cdot \text{SL}$	$0.086 + 0.065 \cdot \text{SL}$
	$t_F$	0.182	$0.084 + 0.049 \cdot \text{SL}$	$0.081 + 0.050 \cdot \text{SL}$	$0.068 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.271	$0.203 + 0.034 \cdot \text{SL}$	$0.219 + 0.030 \cdot \text{SL}$	$0.229 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.276	$0.213 + 0.032 \cdot \text{SL}$	$0.228 + 0.028 \cdot \text{SL}$	$0.234 + 0.027 \cdot \text{SL}$
D to Y	$t_R$	0.225	$0.099 + 0.063 \cdot \text{SL}$	$0.096 + 0.064 \cdot \text{SL}$	$0.086 + 0.065 \cdot \text{SL}$
	$t_F$	0.188	$0.090 + 0.049 \cdot \text{SL}$	$0.087 + 0.050 \cdot \text{SL}$	$0.075 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.274	$0.206 + 0.034 \cdot \text{SL}$	$0.223 + 0.030 \cdot \text{SL}$	$0.232 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.291	$0.226 + 0.032 \cdot \text{SL}$	$0.242 + 0.028 \cdot \text{SL}$	$0.251 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

##### AD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.140	$0.080 + 0.030 \cdot \text{SL}$	$0.083 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$
	$t_F$	0.111	$0.059 + 0.026 \cdot \text{SL}$	$0.061 + 0.025 \cdot \text{SL}$	$0.057 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.193	$0.158 + 0.018 \cdot \text{SL}$	$0.168 + 0.015 \cdot \text{SL}$	$0.179 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.192	$0.158 + 0.017 \cdot \text{SL}$	$0.167 + 0.015 \cdot \text{SL}$	$0.174 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.141	$0.081 + 0.030 \cdot \text{SL}$	$0.085 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$
	$t_F$	0.116	$0.066 + 0.025 \cdot \text{SL}$	$0.068 + 0.025 \cdot \text{SL}$	$0.062 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.202	$0.167 + 0.018 \cdot \text{SL}$	$0.177 + 0.015 \cdot \text{SL}$	$0.188 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.176 + 0.017 \cdot \text{SL}$	$0.186 + 0.015 \cdot \text{SL}$	$0.193 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.141	$0.082 + 0.030 \cdot \text{SL}$	$0.084 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$
	$t_F$	0.123	$0.073 + 0.025 \cdot \text{SL}$	$0.073 + 0.025 \cdot \text{SL}$	$0.067 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.207	$0.172 + 0.018 \cdot \text{SL}$	$0.182 + 0.015 \cdot \text{SL}$	$0.193 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.226	$0.191 + 0.018 \cdot \text{SL}$	$0.202 + 0.015 \cdot \text{SL}$	$0.210 + 0.014 \cdot \text{SL}$
D to Y	$t_R$	0.141	$0.082 + 0.030 \cdot \text{SL}$	$0.085 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$
	$t_F$	0.127	$0.077 + 0.025 \cdot \text{SL}$	$0.079 + 0.025 \cdot \text{SL}$	$0.075 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.209	$0.174 + 0.018 \cdot \text{SL}$	$0.185 + 0.015 \cdot \text{SL}$	$0.196 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.203 + 0.018 \cdot \text{SL}$	$0.214 + 0.015 \cdot \text{SL}$	$0.224 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AD4DH/AD4/AD4D2/AD4D4

## 4-Input AND with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.117	$0.086 + 0.016 \cdot \text{SL}$	$0.088 + 0.015 \cdot \text{SL}$	$0.090 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.065 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.204	$0.181 + 0.011 \cdot \text{SL}$	$0.191 + 0.009 \cdot \text{SL}$	$0.209 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.199	$0.178 + 0.011 \cdot \text{SL}$	$0.186 + 0.009 \cdot \text{SL}$	$0.201 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.119	$0.089 + 0.015 \cdot \text{SL}$	$0.088 + 0.015 \cdot \text{SL}$	$0.091 + 0.015 \cdot \text{SL}$
	$t_F$	0.099	$0.071 + 0.014 \cdot \text{SL}$	$0.076 + 0.013 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.213	$0.190 + 0.011 \cdot \text{SL}$	$0.201 + 0.009 \cdot \text{SL}$	$0.218 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.217	$0.194 + 0.011 \cdot \text{SL}$	$0.205 + 0.009 \cdot \text{SL}$	$0.220 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.119	$0.088 + 0.015 \cdot \text{SL}$	$0.089 + 0.015 \cdot \text{SL}$	$0.091 + 0.015 \cdot \text{SL}$
	$t_F$	0.105	$0.077 + 0.014 \cdot \text{SL}$	$0.080 + 0.013 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.218	$0.195 + 0.011 \cdot \text{SL}$	$0.206 + 0.009 \cdot \text{SL}$	$0.224 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.232	$0.209 + 0.012 \cdot \text{SL}$	$0.220 + 0.009 \cdot \text{SL}$	$0.237 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.119	$0.089 + 0.015 \cdot \text{SL}$	$0.088 + 0.015 \cdot \text{SL}$	$0.090 + 0.015 \cdot \text{SL}$
	$t_F$	0.111	$0.084 + 0.014 \cdot \text{SL}$	$0.087 + 0.013 \cdot \text{SL}$	$0.084 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.220	$0.197 + 0.011 \cdot \text{SL}$	$0.208 + 0.009 \cdot \text{SL}$	$0.226 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.245	$0.221 + 0.012 \cdot \text{SL}$	$0.232 + 0.009 \cdot \text{SL}$	$0.251 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### AD4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.125	$0.110 + 0.008 \cdot \text{SL}$	$0.109 + 0.008 \cdot \text{SL}$	$0.113 + 0.007 \cdot \text{SL}$
	$t_F$	0.095	$0.080 + 0.008 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.233	$0.219 + 0.007 \cdot \text{SL}$	$0.228 + 0.005 \cdot \text{SL}$	$0.251 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.221	$0.208 + 0.007 \cdot \text{SL}$	$0.215 + 0.005 \cdot \text{SL}$	$0.236 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.125	$0.109 + 0.008 \cdot \text{SL}$	$0.111 + 0.008 \cdot \text{SL}$	$0.112 + 0.007 \cdot \text{SL}$
	$t_F$	0.102	$0.088 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.243	$0.228 + 0.007 \cdot \text{SL}$	$0.237 + 0.005 \cdot \text{SL}$	$0.261 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.238	$0.224 + 0.007 \cdot \text{SL}$	$0.232 + 0.005 \cdot \text{SL}$	$0.254 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.125	$0.110 + 0.008 \cdot \text{SL}$	$0.110 + 0.008 \cdot \text{SL}$	$0.113 + 0.007 \cdot \text{SL}$
	$t_F$	0.108	$0.093 + 0.008 \cdot \text{SL}$	$0.096 + 0.007 \cdot \text{SL}$	$0.100 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.247	$0.233 + 0.007 \cdot \text{SL}$	$0.242 + 0.005 \cdot \text{SL}$	$0.265 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.252	$0.238 + 0.007 \cdot \text{SL}$	$0.247 + 0.005 \cdot \text{SL}$	$0.270 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.124	$0.108 + 0.008 \cdot \text{SL}$	$0.110 + 0.008 \cdot \text{SL}$	$0.112 + 0.007 \cdot \text{SL}$
	$t_F$	0.116	$0.101 + 0.007 \cdot \text{SL}$	$0.104 + 0.007 \cdot \text{SL}$	$0.106 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.250	$0.235 + 0.007 \cdot \text{SL}$	$0.244 + 0.005 \cdot \text{SL}$	$0.268 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.265	$0.250 + 0.007 \cdot \text{SL}$	$0.259 + 0.005 \cdot \text{SL}$	$0.284 + 0.004 \cdot \text{SL}$

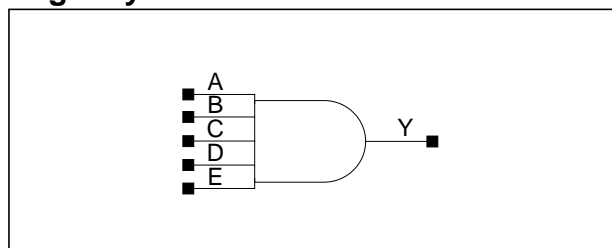
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# AD5/AD5D2/AD5D4

## 5-Input AND with 1X/2X/4XDrive

### Logic Symbol



### Truth Table

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	1

### Cell Data

Input Load (SL)														
AD5					AD5D2					AD5D4				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.8	0.9	0.9	0.9	0.9	0.8	0.9	0.9	0.8	0.9	0.8	0.9	0.9	0.9	0.9
Gate Count														
AD5					AD5D2					AD5D4				
2.67					3.00					4.33				

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.223	$0.107 + 0.058 \cdot \text{SL}$	$0.104 + 0.059 \cdot \text{SL}$	$0.098 + 0.059 \cdot \text{SL}$
	$t_F$	0.117	$0.063 + 0.027 \cdot \text{SL}$	$0.064 + 0.027 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.190	$0.136 + 0.027 \cdot \text{SL}$	$0.141 + 0.026 \cdot \text{SL}$	$0.143 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.201	$0.166 + 0.018 \cdot \text{SL}$	$0.175 + 0.015 \cdot \text{SL}$	$0.182 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.223	$0.108 + 0.058 \cdot \text{SL}$	$0.104 + 0.059 \cdot \text{SL}$	$0.098 + 0.059 \cdot \text{SL}$
	$t_F$	0.123	$0.070 + 0.026 \cdot \text{SL}$	$0.071 + 0.026 \cdot \text{SL}$	$0.064 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.140 + 0.027 \cdot \text{SL}$	$0.145 + 0.026 \cdot \text{SL}$	$0.147 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.224	$0.188 + 0.018 \cdot \text{SL}$	$0.198 + 0.016 \cdot \text{SL}$	$0.206 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.223	$0.108 + 0.058 \cdot \text{SL}$	$0.103 + 0.059 \cdot \text{SL}$	$0.098 + 0.059 \cdot \text{SL}$
	$t_F$	0.128	$0.076 + 0.026 \cdot \text{SL}$	$0.076 + 0.026 \cdot \text{SL}$	$0.069 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.193	$0.139 + 0.027 \cdot \text{SL}$	$0.144 + 0.026 \cdot \text{SL}$	$0.146 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.202 + 0.018 \cdot \text{SL}$	$0.213 + 0.016 \cdot \text{SL}$	$0.221 + 0.015 \cdot \text{SL}$
D to Y	$t_R$	0.215	$0.098 + 0.058 \cdot \text{SL}$	$0.095 + 0.059 \cdot \text{SL}$	$0.092 + 0.060 \cdot \text{SL}$
	$t_F$	0.135	$0.083 + 0.026 \cdot \text{SL}$	$0.081 + 0.026 \cdot \text{SL}$	$0.073 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.171	$0.118 + 0.027 \cdot \text{SL}$	$0.121 + 0.026 \cdot \text{SL}$	$0.123 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.199	$0.166 + 0.017 \cdot \text{SL}$	$0.172 + 0.015 \cdot \text{SL}$	$0.176 + 0.015 \cdot \text{SL}$
E to Y	$t_R$	0.215	$0.098 + 0.058 \cdot \text{SL}$	$0.094 + 0.059 \cdot \text{SL}$	$0.091 + 0.060 \cdot \text{SL}$
	$t_F$	0.140	$0.089 + 0.025 \cdot \text{SL}$	$0.085 + 0.026 \cdot \text{SL}$	$0.078 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.169	$0.116 + 0.027 \cdot \text{SL}$	$0.119 + 0.026 \cdot \text{SL}$	$0.121 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.223	$0.190 + 0.017 \cdot \text{SL}$	$0.196 + 0.015 \cdot \text{SL}$	$0.200 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AD5D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.159	$0.100 + 0.030 \cdot \text{SL}$	$0.099 + 0.030 \cdot \text{SL}$	$0.092 + 0.030 \cdot \text{SL}$
	$t_F$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.185	$0.155 + 0.015 \cdot \text{SL}$	$0.161 + 0.014 \cdot \text{SL}$	$0.167 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.210	$0.187 + 0.011 \cdot \text{SL}$	$0.197 + 0.009 \cdot \text{SL}$	$0.212 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.159	$0.100 + 0.029 \cdot \text{SL}$	$0.099 + 0.030 \cdot \text{SL}$	$0.092 + 0.030 \cdot \text{SL}$
	$t_F$	0.103	$0.076 + 0.014 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$	$0.076 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.188	$0.158 + 0.015 \cdot \text{SL}$	$0.164 + 0.014 \cdot \text{SL}$	$0.169 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.226	$0.203 + 0.011 \cdot \text{SL}$	$0.213 + 0.009 \cdot \text{SL}$	$0.230 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.159	$0.100 + 0.030 \cdot \text{SL}$	$0.099 + 0.030 \cdot \text{SL}$	$0.092 + 0.030 \cdot \text{SL}$
	$t_F$	0.114	$0.086 + 0.014 \cdot \text{SL}$	$0.090 + 0.013 \cdot \text{SL}$	$0.087 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.185	$0.155 + 0.015 \cdot \text{SL}$	$0.161 + 0.014 \cdot \text{SL}$	$0.166 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.248	$0.224 + 0.012 \cdot \text{SL}$	$0.236 + 0.009 \cdot \text{SL}$	$0.255 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.149	$0.089 + 0.030 \cdot \text{SL}$	$0.088 + 0.030 \cdot \text{SL}$	$0.084 + 0.030 \cdot \text{SL}$
	$t_F$	0.119	$0.093 + 0.013 \cdot \text{SL}$	$0.094 + 0.013 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.167	$0.137 + 0.015 \cdot \text{SL}$	$0.143 + 0.014 \cdot \text{SL}$	$0.147 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.191 + 0.010 \cdot \text{SL}$	$0.198 + 0.008 \cdot \text{SL}$	$0.209 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.149	$0.089 + 0.030 \cdot \text{SL}$	$0.087 + 0.030 \cdot \text{SL}$	$0.084 + 0.030 \cdot \text{SL}$
	$t_F$	0.127	$0.101 + 0.013 \cdot \text{SL}$	$0.103 + 0.013 \cdot \text{SL}$	$0.095 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.162	$0.133 + 0.015 \cdot \text{SL}$	$0.138 + 0.014 \cdot \text{SL}$	$0.143 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.233	$0.212 + 0.010 \cdot \text{SL}$	$0.220 + 0.008 \cdot \text{SL}$	$0.232 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## AD5/AD5D2/AD5D4

### 5-Input AND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AD5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.055 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.325	$0.314 + 0.005 \cdot \text{SL}$	$0.319 + 0.004 \cdot \text{SL}$	$0.330 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.321	$0.309 + 0.006 \cdot \text{SL}$	$0.315 + 0.004 \cdot \text{SL}$	$0.329 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.068	$0.052 + 0.008 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.328	$0.318 + 0.005 \cdot \text{SL}$	$0.323 + 0.004 \cdot \text{SL}$	$0.334 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.344	$0.332 + 0.006 \cdot \text{SL}$	$0.338 + 0.004 \cdot \text{SL}$	$0.352 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.056 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.327	$0.317 + 0.005 \cdot \text{SL}$	$0.322 + 0.004 \cdot \text{SL}$	$0.333 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.358	$0.347 + 0.006 \cdot \text{SL}$	$0.352 + 0.004 \cdot \text{SL}$	$0.367 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.078	$0.063 + 0.008 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.068	$0.053 + 0.008 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.305	$0.295 + 0.005 \cdot \text{SL}$	$0.300 + 0.004 \cdot \text{SL}$	$0.311 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.323	$0.311 + 0.006 \cdot \text{SL}$	$0.317 + 0.004 \cdot \text{SL}$	$0.331 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.078	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.068	$0.052 + 0.008 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.304	$0.293 + 0.005 \cdot \text{SL}$	$0.298 + 0.004 \cdot \text{SL}$	$0.309 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.347	$0.336 + 0.006 \cdot \text{SL}$	$0.341 + 0.004 \cdot \text{SL}$	$0.355 + 0.004 \cdot \text{SL}$

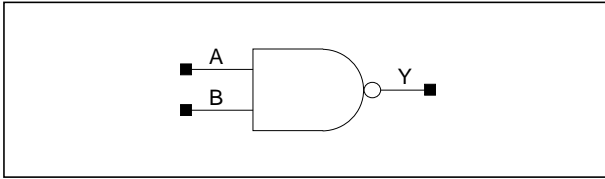
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## ND2DH/ND2/ND2D2/ND2D4

### 2-Input NAND with 0.5X/1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

#### Cell Data

Input Load (SL)								Gate Count			
ND2DH		ND2		ND2D2		ND2D4		ND2DH	ND2	ND2D2	ND2D4
A	B	A	B	A	B	A	B				
0.6	0.6	1.1	1.1	2.3	2.3	4.7	4.6	1.00	1.00	1.67	2.67

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### ND2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.220	$0.094 + 0.063 \cdot \text{SL}$	$0.077 + 0.067 \cdot \text{SL}$	$0.058 + 0.069 \cdot \text{SL}$
	$t_F$	0.218	$0.097 + 0.060 \cdot \text{SL}$	$0.078 + 0.065 \cdot \text{SL}$	$0.060 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.133	$0.071 + 0.031 \cdot \text{SL}$	$0.075 + 0.030 \cdot \text{SL}$	$0.074 + 0.030 \cdot \text{SL}$
	$t_{PHL}$	0.128	$0.062 + 0.033 \cdot \text{SL}$	$0.066 + 0.032 \cdot \text{SL}$	$0.065 + 0.032 \cdot \text{SL}$
B to Y	$t_R$	0.236	$0.110 + 0.063 \cdot \text{SL}$	$0.094 + 0.067 \cdot \text{SL}$	$0.075 + 0.069 \cdot \text{SL}$
	$t_F$	0.209	$0.085 + 0.062 \cdot \text{SL}$	$0.070 + 0.066 \cdot \text{SL}$	$0.059 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.143	$0.084 + 0.030 \cdot \text{SL}$	$0.084 + 0.030 \cdot \text{SL}$	$0.083 + 0.030 \cdot \text{SL}$
	$t_{PHL}$	0.121	$0.055 + 0.033 \cdot \text{SL}$	$0.059 + 0.032 \cdot \text{SL}$	$0.058 + 0.032 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

##### ND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.144	$0.092 + 0.026 \cdot \text{SL}$	$0.082 + 0.028 \cdot \text{SL}$	$0.070 + 0.030 \cdot \text{SL}$
	$t_F$	0.149	$0.095 + 0.027 \cdot \text{SL}$	$0.087 + 0.029 \cdot \text{SL}$	$0.072 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.089	$0.056 + 0.016 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.088	$0.052 + 0.018 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.160	$0.108 + 0.026 \cdot \text{SL}$	$0.098 + 0.028 \cdot \text{SL}$	$0.086 + 0.030 \cdot \text{SL}$
	$t_F$	0.140	$0.086 + 0.027 \cdot \text{SL}$	$0.076 + 0.030 \cdot \text{SL}$	$0.064 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.101	$0.071 + 0.015 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.081	$0.047 + 0.017 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## ND2DH/ND2/ND2D2/ND2D4

### 2-Input NAND with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### ND2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.119	$0.094 + 0.012 \cdot \text{SL}$	$0.089 + 0.014 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$
	$t_F$	0.122	$0.095 + 0.014 \cdot \text{SL}$	$0.093 + 0.014 \cdot \text{SL}$	$0.077 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.073	$0.054 + 0.009 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.070	$0.049 + 0.010 \cdot \text{SL}$	$0.058 + 0.008 \cdot \text{SL}$	$0.064 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.135	$0.110 + 0.013 \cdot \text{SL}$	$0.105 + 0.014 \cdot \text{SL}$	$0.091 + 0.015 \cdot \text{SL}$
	$t_F$	0.114	$0.087 + 0.013 \cdot \text{SL}$	$0.084 + 0.014 \cdot \text{SL}$	$0.066 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.086	$0.069 + 0.008 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.064	$0.045 + 0.009 \cdot \text{SL}$	$0.051 + 0.008 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### ND2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.104	$0.091 + 0.007 \cdot \text{SL}$	$0.091 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_F$	0.107	$0.091 + 0.008 \cdot \text{SL}$	$0.094 + 0.007 \cdot \text{SL}$	$0.078 + 0.008 \cdot \text{SL}$
	$t_{PLH}$	0.061	$0.051 + 0.005 \cdot \text{SL}$	$0.056 + 0.004 \cdot \text{SL}$	$0.069 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.059	$0.047 + 0.006 \cdot \text{SL}$	$0.053 + 0.004 \cdot \text{SL}$	$0.064 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.122	$0.110 + 0.006 \cdot \text{SL}$	$0.108 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$
	$t_F$	0.099	$0.084 + 0.007 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.068 + 0.008 \cdot \text{SL}$
	$t_{PLH}$	0.076	$0.067 + 0.005 \cdot \text{SL}$	$0.070 + 0.004 \cdot \text{SL}$	$0.078 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.054	$0.043 + 0.005 \cdot \text{SL}$	$0.047 + 0.004 \cdot \text{SL}$	$0.055 + 0.004 \cdot \text{SL}$

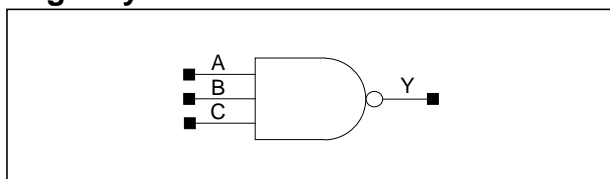
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# ND3DH/ND3/ND3D2/ND3D4

## 3-Input NAND with 0.5X/1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

### Cell Data

Input Load (SL)											
ND3DH			ND3			ND3D2			ND3D4		
A	B	C	A	B	C	A	B	C	A	B	C
0.5	0.5	0.5	1.0	1.0	1.0	2.2	2.1	2.0	4.4	4.3	4.3
Gate Count											
ND3DH			ND3			ND3D2			ND3D4		
1.33			1.33			2.33			4.00		



## ND3DH/ND3/ND3D2/ND3D4

### 3-Input NAND with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### ND3DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.275	$0.120 + 0.077 \cdot \text{SL}$	$0.107 + 0.081 \cdot \text{SL}$	$0.091 + 0.083 \cdot \text{SL}$
	$t_F$	0.325	$0.144 + 0.091 \cdot \text{SL}$	$0.127 + 0.095 \cdot \text{SL}$	$0.114 + 0.096 \cdot \text{SL}$
	$t_{PLH}$	0.162	$0.091 + 0.036 \cdot \text{SL}$	$0.091 + 0.036 \cdot \text{SL}$	$0.090 + 0.036 \cdot \text{SL}$
	$t_{PHL}$	0.175	$0.087 + 0.044 \cdot \text{SL}$	$0.085 + 0.044 \cdot \text{SL}$	$0.084 + 0.044 \cdot \text{SL}$
B to Y	$t_R$	0.295	$0.141 + 0.077 \cdot \text{SL}$	$0.126 + 0.081 \cdot \text{SL}$	$0.110 + 0.083 \cdot \text{SL}$
	$t_F$	0.321	$0.136 + 0.092 \cdot \text{SL}$	$0.126 + 0.095 \cdot \text{SL}$	$0.115 + 0.096 \cdot \text{SL}$
	$t_{PLH}$	0.174	$0.104 + 0.035 \cdot \text{SL}$	$0.103 + 0.036 \cdot \text{SL}$	$0.102 + 0.036 \cdot \text{SL}$
	$t_{PHL}$	0.178	$0.089 + 0.044 \cdot \text{SL}$	$0.089 + 0.044 \cdot \text{SL}$	$0.089 + 0.044 \cdot \text{SL}$
C to Y	$t_R$	0.317	$0.163 + 0.077 \cdot \text{SL}$	$0.147 + 0.081 \cdot \text{SL}$	$0.131 + 0.083 \cdot \text{SL}$
	$t_F$	0.317	$0.130 + 0.093 \cdot \text{SL}$	$0.122 + 0.095 \cdot \text{SL}$	$0.115 + 0.096 \cdot \text{SL}$
	$t_{PLH}$	0.185	$0.114 + 0.036 \cdot \text{SL}$	$0.114 + 0.036 \cdot \text{SL}$	$0.114 + 0.036 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.087 + 0.045 \cdot \text{SL}$	$0.087 + 0.044 \cdot \text{SL}$	$0.087 + 0.044 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

##### ND3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.177	$0.109 + 0.034 \cdot \text{SL}$	$0.099 + 0.036 \cdot \text{SL}$	$0.087 + 0.038 \cdot \text{SL}$
	$t_F$	0.210	$0.128 + 0.041 \cdot \text{SL}$	$0.118 + 0.043 \cdot \text{SL}$	$0.105 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.111	$0.074 + 0.018 \cdot \text{SL}$	$0.081 + 0.017 \cdot \text{SL}$	$0.080 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.115	$0.072 + 0.022 \cdot \text{SL}$	$0.076 + 0.021 \cdot \text{SL}$	$0.074 + 0.021 \cdot \text{SL}$
B to Y	$t_R$	0.196	$0.128 + 0.034 \cdot \text{SL}$	$0.118 + 0.036 \cdot \text{SL}$	$0.105 + 0.038 \cdot \text{SL}$
	$t_F$	0.204	$0.122 + 0.041 \cdot \text{SL}$	$0.110 + 0.044 \cdot \text{SL}$	$0.102 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.124	$0.090 + 0.017 \cdot \text{SL}$	$0.093 + 0.017 \cdot \text{SL}$	$0.092 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.117	$0.073 + 0.022 \cdot \text{SL}$	$0.077 + 0.021 \cdot \text{SL}$	$0.076 + 0.021 \cdot \text{SL}$
C to Y	$t_R$	0.216	$0.149 + 0.034 \cdot \text{SL}$	$0.139 + 0.036 \cdot \text{SL}$	$0.125 + 0.038 \cdot \text{SL}$
	$t_F$	0.198	$0.113 + 0.043 \cdot \text{SL}$	$0.105 + 0.045 \cdot \text{SL}$	$0.098 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.134	$0.100 + 0.017 \cdot \text{SL}$	$0.102 + 0.017 \cdot \text{SL}$	$0.101 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.114	$0.070 + 0.022 \cdot \text{SL}$	$0.073 + 0.021 \cdot \text{SL}$	$0.073 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# ND3DH/ND3/ND3D2/ND3D4

## 3-Input NAND with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### ND3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.140	$0.109 + 0.015 \cdot \text{SL}$	$0.099 + 0.018 \cdot \text{SL}$	$0.086 + 0.019 \cdot \text{SL}$
	$t_F$	0.166	$0.127 + 0.019 \cdot \text{SL}$	$0.120 + 0.021 \cdot \text{SL}$	$0.104 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.090	$0.069 + 0.011 \cdot \text{SL}$	$0.077 + 0.009 \cdot \text{SL}$	$0.080 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.090	$0.066 + 0.012 \cdot \text{SL}$	$0.073 + 0.010 \cdot \text{SL}$	$0.073 + 0.010 \cdot \text{SL}$
B to Y	$t_R$	0.157	$0.125 + 0.016 \cdot \text{SL}$	$0.118 + 0.018 \cdot \text{SL}$	$0.105 + 0.019 \cdot \text{SL}$
	$t_F$	0.160	$0.121 + 0.019 \cdot \text{SL}$	$0.113 + 0.021 \cdot \text{SL}$	$0.099 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.104	$0.085 + 0.010 \cdot \text{SL}$	$0.090 + 0.008 \cdot \text{SL}$	$0.090 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.090	$0.066 + 0.012 \cdot \text{SL}$	$0.072 + 0.011 \cdot \text{SL}$	$0.073 + 0.011 \cdot \text{SL}$
C to Y	$t_R$	0.178	$0.146 + 0.016 \cdot \text{SL}$	$0.140 + 0.018 \cdot \text{SL}$	$0.125 + 0.019 \cdot \text{SL}$
	$t_F$	0.152	$0.112 + 0.020 \cdot \text{SL}$	$0.104 + 0.022 \cdot \text{SL}$	$0.095 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.115	$0.096 + 0.009 \cdot \text{SL}$	$0.100 + 0.008 \cdot \text{SL}$	$0.100 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.088	$0.065 + 0.012 \cdot \text{SL}$	$0.069 + 0.011 \cdot \text{SL}$	$0.070 + 0.011 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### ND3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.122	$0.105 + 0.008 \cdot \text{SL}$	$0.104 + 0.009 \cdot \text{SL}$	$0.087 + 0.009 \cdot \text{SL}$
	$t_F$	0.144	$0.126 + 0.009 \cdot \text{SL}$	$0.121 + 0.010 \cdot \text{SL}$	$0.104 + 0.011 \cdot \text{SL}$
	$t_{PLH}$	0.078	$0.066 + 0.006 \cdot \text{SL}$	$0.072 + 0.005 \cdot \text{SL}$	$0.079 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.077	$0.064 + 0.007 \cdot \text{SL}$	$0.068 + 0.005 \cdot \text{SL}$	$0.072 + 0.005 \cdot \text{SL}$
B to Y	$t_R$	0.141	$0.126 + 0.008 \cdot \text{SL}$	$0.122 + 0.009 \cdot \text{SL}$	$0.106 + 0.009 \cdot \text{SL}$
	$t_F$	0.139	$0.122 + 0.009 \cdot \text{SL}$	$0.114 + 0.011 \cdot \text{SL}$	$0.100 + 0.011 \cdot \text{SL}$
	$t_{PLH}$	0.094	$0.083 + 0.005 \cdot \text{SL}$	$0.087 + 0.004 \cdot \text{SL}$	$0.090 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.078	$0.065 + 0.006 \cdot \text{SL}$	$0.068 + 0.005 \cdot \text{SL}$	$0.073 + 0.005 \cdot \text{SL}$
C to Y	$t_R$	0.162	$0.147 + 0.008 \cdot \text{SL}$	$0.143 + 0.009 \cdot \text{SL}$	$0.127 + 0.009 \cdot \text{SL}$
	$t_F$	0.129	$0.109 + 0.010 \cdot \text{SL}$	$0.106 + 0.011 \cdot \text{SL}$	$0.094 + 0.011 \cdot \text{SL}$
	$t_{PLH}$	0.105	$0.095 + 0.005 \cdot \text{SL}$	$0.098 + 0.004 \cdot \text{SL}$	$0.100 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.076	$0.064 + 0.006 \cdot \text{SL}$	$0.067 + 0.005 \cdot \text{SL}$	$0.070 + 0.005 \cdot \text{SL}$

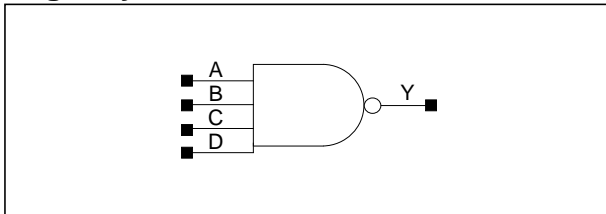
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# ND4DH/ND4/ND4D2/ND4D2B/ND4D4

## 4-Input NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

### Cell Data

Input Load (SL)																			
ND4DH				ND4				ND4D2				ND4D2B				ND4D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.5	0.5	0.5	0.9	0.9	0.9	0.9	1.7	1.9	1.9	2.1	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9
Gate Count																			
ND4DH				ND4				ND4D2				ND4D2B				ND4D4			
1.67				1.67				2.67				2.67				3.33			

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### ND4DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.324	$0.127 + 0.098 \cdot \text{SL}$	$0.111 + 0.102 \cdot \text{SL}$	$0.100 + 0.104 \cdot \text{SL}$
	$t_F$	0.412	$0.171 + 0.120 \cdot \text{SL}$	$0.155 + 0.124 \cdot \text{SL}$	$0.147 + 0.125 \cdot \text{SL}$
	$t_{PLH}$	0.188	$0.099 + 0.044 \cdot \text{SL}$	$0.099 + 0.045 \cdot \text{SL}$	$0.098 + 0.045 \cdot \text{SL}$
	$t_{PHL}$	0.201	$0.088 + 0.056 \cdot \text{SL}$	$0.087 + 0.057 \cdot \text{SL}$	$0.086 + 0.057 \cdot \text{SL}$
B to Y	$t_R$	0.348	$0.151 + 0.098 \cdot \text{SL}$	$0.135 + 0.102 \cdot \text{SL}$	$0.126 + 0.104 \cdot \text{SL}$
	$t_F$	0.412	$0.169 + 0.121 \cdot \text{SL}$	$0.158 + 0.124 \cdot \text{SL}$	$0.149 + 0.125 \cdot \text{SL}$
	$t_{PLH}$	0.204	$0.115 + 0.044 \cdot \text{SL}$	$0.115 + 0.045 \cdot \text{SL}$	$0.114 + 0.045 \cdot \text{SL}$
	$t_{PHL}$	0.212	$0.099 + 0.057 \cdot \text{SL}$	$0.099 + 0.057 \cdot \text{SL}$	$0.099 + 0.057 \cdot \text{SL}$
C to Y	$t_R$	0.375	$0.179 + 0.098 \cdot \text{SL}$	$0.162 + 0.102 \cdot \text{SL}$	$0.152 + 0.104 \cdot \text{SL}$
	$t_F$	0.409	$0.164 + 0.122 \cdot \text{SL}$	$0.156 + 0.124 \cdot \text{SL}$	$0.149 + 0.125 \cdot \text{SL}$
	$t_{PLH}$	0.218	$0.128 + 0.045 \cdot \text{SL}$	$0.129 + 0.045 \cdot \text{SL}$	$0.129 + 0.045 \cdot \text{SL}$
	$t_{PHL}$	0.219	$0.106 + 0.057 \cdot \text{SL}$	$0.106 + 0.057 \cdot \text{SL}$	$0.106 + 0.057 \cdot \text{SL}$
D to Y	$t_R$	0.402	$0.206 + 0.098 \cdot \text{SL}$	$0.189 + 0.102 \cdot \text{SL}$	$0.179 + 0.104 \cdot \text{SL}$
	$t_F$	0.406	$0.160 + 0.123 \cdot \text{SL}$	$0.153 + 0.125 \cdot \text{SL}$	$0.149 + 0.125 \cdot \text{SL}$
	$t_{PLH}$	0.228	$0.137 + 0.045 \cdot \text{SL}$	$0.139 + 0.045 \cdot \text{SL}$	$0.141 + 0.045 \cdot \text{SL}$
	$t_{PHL}$	0.220	$0.106 + 0.057 \cdot \text{SL}$	$0.107 + 0.057 \cdot \text{SL}$	$0.107 + 0.057 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# ND4DH/ND4/ND4D2/ND4D2B/ND4D4

## 4-Input NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### ND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.199	$0.111 + 0.044 \cdot \text{SL}$	$0.102 + 0.046 \cdot \text{SL}$	$0.089 + 0.048 \cdot \text{SL}$
	$t_F$	0.262	$0.152 + 0.055 \cdot \text{SL}$	$0.142 + 0.057 \cdot \text{SL}$	$0.128 + 0.059 \cdot \text{SL}$
	$t_{PLH}$	0.127	$0.084 + 0.022 \cdot \text{SL}$	$0.087 + 0.021 \cdot \text{SL}$	$0.087 + 0.021 \cdot \text{SL}$
	$t_{PHL}$	0.128	$0.075 + 0.027 \cdot \text{SL}$	$0.074 + 0.027 \cdot \text{SL}$	$0.073 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.223	$0.135 + 0.044 \cdot \text{SL}$	$0.126 + 0.046 \cdot \text{SL}$	$0.113 + 0.048 \cdot \text{SL}$
	$t_F$	0.260	$0.149 + 0.055 \cdot \text{SL}$	$0.139 + 0.058 \cdot \text{SL}$	$0.130 + 0.059 \cdot \text{SL}$
	$t_{PLH}$	0.144	$0.102 + 0.021 \cdot \text{SL}$	$0.103 + 0.021 \cdot \text{SL}$	$0.102 + 0.021 \cdot \text{SL}$
	$t_{PHL}$	0.137	$0.082 + 0.028 \cdot \text{SL}$	$0.085 + 0.027 \cdot \text{SL}$	$0.084 + 0.027 \cdot \text{SL}$
C to Y	$t_R$	0.248	$0.161 + 0.044 \cdot \text{SL}$	$0.151 + 0.046 \cdot \text{SL}$	$0.138 + 0.048 \cdot \text{SL}$
	$t_F$	0.255	$0.142 + 0.056 \cdot \text{SL}$	$0.134 + 0.058 \cdot \text{SL}$	$0.128 + 0.059 \cdot \text{SL}$
	$t_{PLH}$	0.156	$0.114 + 0.021 \cdot \text{SL}$	$0.115 + 0.021 \cdot \text{SL}$	$0.115 + 0.021 \cdot \text{SL}$
	$t_{PHL}$	0.143	$0.088 + 0.028 \cdot \text{SL}$	$0.090 + 0.027 \cdot \text{SL}$	$0.090 + 0.027 \cdot \text{SL}$
D to Y	$t_R$	0.274	$0.187 + 0.044 \cdot \text{SL}$	$0.177 + 0.046 \cdot \text{SL}$	$0.164 + 0.048 \cdot \text{SL}$
	$t_F$	0.250	$0.136 + 0.057 \cdot \text{SL}$	$0.130 + 0.059 \cdot \text{SL}$	$0.125 + 0.059 \cdot \text{SL}$
	$t_{PLH}$	0.165	$0.122 + 0.022 \cdot \text{SL}$	$0.124 + 0.021 \cdot \text{SL}$	$0.125 + 0.021 \cdot \text{SL}$
	$t_{PHL}$	0.144	$0.089 + 0.027 \cdot \text{SL}$	$0.091 + 0.027 \cdot \text{SL}$	$0.091 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### ND4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.153	$0.112 + 0.020 \cdot \text{SL}$	$0.103 + 0.023 \cdot \text{SL}$	$0.088 + 0.024 \cdot \text{SL}$
	$t_F$	0.202	$0.149 + 0.027 \cdot \text{SL}$	$0.142 + 0.028 \cdot \text{SL}$	$0.126 + 0.029 \cdot \text{SL}$
	$t_{PLH}$	0.101	$0.077 + 0.012 \cdot \text{SL}$	$0.084 + 0.010 \cdot \text{SL}$	$0.084 + 0.010 \cdot \text{SL}$
	$t_{PHL}$	0.098	$0.069 + 0.014 \cdot \text{SL}$	$0.074 + 0.013 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
B to Y	$t_R$	0.175	$0.134 + 0.021 \cdot \text{SL}$	$0.127 + 0.023 \cdot \text{SL}$	$0.111 + 0.024 \cdot \text{SL}$
	$t_F$	0.199	$0.145 + 0.027 \cdot \text{SL}$	$0.138 + 0.029 \cdot \text{SL}$	$0.126 + 0.029 \cdot \text{SL}$
	$t_{PLH}$	0.119	$0.097 + 0.011 \cdot \text{SL}$	$0.099 + 0.010 \cdot \text{SL}$	$0.099 + 0.010 \cdot \text{SL}$
	$t_{PHL}$	0.106	$0.077 + 0.015 \cdot \text{SL}$	$0.081 + 0.013 \cdot \text{SL}$	$0.081 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.201	$0.159 + 0.021 \cdot \text{SL}$	$0.153 + 0.022 \cdot \text{SL}$	$0.136 + 0.024 \cdot \text{SL}$
	$t_F$	0.193	$0.139 + 0.027 \cdot \text{SL}$	$0.132 + 0.029 \cdot \text{SL}$	$0.124 + 0.030 \cdot \text{SL}$
	$t_{PLH}$	0.132	$0.110 + 0.011 \cdot \text{SL}$	$0.112 + 0.010 \cdot \text{SL}$	$0.112 + 0.010 \cdot \text{SL}$
	$t_{PHL}$	0.112	$0.082 + 0.015 \cdot \text{SL}$	$0.087 + 0.014 \cdot \text{SL}$	$0.087 + 0.014 \cdot \text{SL}$
D to Y	$t_R$	0.227	$0.184 + 0.021 \cdot \text{SL}$	$0.180 + 0.022 \cdot \text{SL}$	$0.162 + 0.024 \cdot \text{SL}$
	$t_F$	0.188	$0.133 + 0.028 \cdot \text{SL}$	$0.126 + 0.029 \cdot \text{SL}$	$0.120 + 0.030 \cdot \text{SL}$
	$t_{PLH}$	0.141	$0.119 + 0.011 \cdot \text{SL}$	$0.120 + 0.011 \cdot \text{SL}$	$0.122 + 0.011 \cdot \text{SL}$
	$t_{PHL}$	0.113	$0.085 + 0.014 \cdot \text{SL}$	$0.088 + 0.014 \cdot \text{SL}$	$0.088 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## ND4DH/ND4/ND4D2/ND4D2B/ND4D4

### 4-Input NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### ND4D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.076	$0.047 + 0.015 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$	$0.037 + 0.015 \cdot \text{SL}$
	$t_F$	0.071	$0.043 + 0.014 \cdot \text{SL}$	$0.049 + 0.013 \cdot \text{SL}$	$0.041 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.224	$0.208 + 0.008 \cdot \text{SL}$	$0.213 + 0.007 \cdot \text{SL}$	$0.216 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.231	$0.213 + 0.009 \cdot \text{SL}$	$0.220 + 0.008 \cdot \text{SL}$	$0.226 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.077	$0.048 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$	$0.038 + 0.015 \cdot \text{SL}$
	$t_F$	0.072	$0.046 + 0.013 \cdot \text{SL}$	$0.047 + 0.013 \cdot \text{SL}$	$0.041 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.243	$0.227 + 0.008 \cdot \text{SL}$	$0.232 + 0.007 \cdot \text{SL}$	$0.235 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.221 + 0.009 \cdot \text{SL}$	$0.228 + 0.008 \cdot \text{SL}$	$0.235 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.077	$0.049 + 0.014 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$	$0.039 + 0.015 \cdot \text{SL}$
	$t_F$	0.072	$0.045 + 0.013 \cdot \text{SL}$	$0.049 + 0.013 \cdot \text{SL}$	$0.041 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.259	$0.243 + 0.008 \cdot \text{SL}$	$0.248 + 0.007 \cdot \text{SL}$	$0.251 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.245	$0.226 + 0.009 \cdot \text{SL}$	$0.233 + 0.008 \cdot \text{SL}$	$0.240 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.079	$0.051 + 0.014 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$	$0.040 + 0.015 \cdot \text{SL}$
	$t_F$	0.072	$0.046 + 0.013 \cdot \text{SL}$	$0.049 + 0.013 \cdot \text{SL}$	$0.040 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.271	$0.255 + 0.008 \cdot \text{SL}$	$0.260 + 0.007 \cdot \text{SL}$	$0.263 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.246	$0.227 + 0.009 \cdot \text{SL}$	$0.234 + 0.008 \cdot \text{SL}$	$0.241 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### ND4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.076	$0.061 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$	$0.054 + 0.008 \cdot \text{SL}$
	$t_F$	0.075	$0.061 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.260	$0.250 + 0.005 \cdot \text{SL}$	$0.254 + 0.004 \cdot \text{SL}$	$0.265 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.270	$0.258 + 0.006 \cdot \text{SL}$	$0.264 + 0.004 \cdot \text{SL}$	$0.279 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.077	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.054 + 0.008 \cdot \text{SL}$
	$t_F$	0.076	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.278	$0.268 + 0.005 \cdot \text{SL}$	$0.273 + 0.004 \cdot \text{SL}$	$0.283 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.279	$0.268 + 0.006 \cdot \text{SL}$	$0.273 + 0.004 \cdot \text{SL}$	$0.288 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.076	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.296	$0.285 + 0.005 \cdot \text{SL}$	$0.290 + 0.004 \cdot \text{SL}$	$0.301 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.284	$0.273 + 0.006 \cdot \text{SL}$	$0.278 + 0.004 \cdot \text{SL}$	$0.293 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.076	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.308	$0.298 + 0.005 \cdot \text{SL}$	$0.303 + 0.004 \cdot \text{SL}$	$0.313 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.287	$0.276 + 0.006 \cdot \text{SL}$	$0.281 + 0.004 \cdot \text{SL}$	$0.296 + 0.004 \cdot \text{SL}$

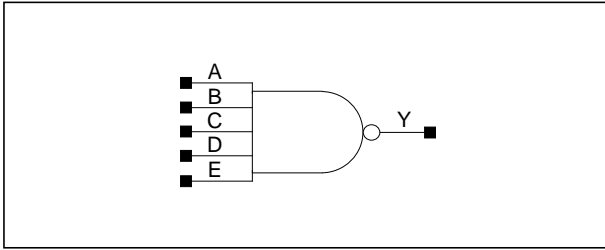
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# ND5/ND5D2/ND5D4

## 5-Input NAND with 1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

### Cell Data

Input Load (SL)															Gate Count		
ND5					ND5D2					ND5D4					ND5	ND5D2	ND5D4
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E			
0.8	0.9	0.9	0.9	0.9	0.8	0.9	0.9	0.9	0.9	0.8	0.9	0.9	0.9	0.9	3.33	3.67	4.00

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### ND5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.110	$0.051 + 0.029 \cdot \text{SL}$	$0.047 + 0.031 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.114	$0.063 + 0.026 \cdot \text{SL}$	$0.065 + 0.025 \cdot \text{SL}$	$0.061 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.247	$0.218 + 0.014 \cdot \text{SL}$	$0.221 + 0.014 \cdot \text{SL}$	$0.222 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.247	$0.212 + 0.017 \cdot \text{SL}$	$0.222 + 0.015 \cdot \text{SL}$	$0.230 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.110	$0.052 + 0.029 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.114	$0.062 + 0.026 \cdot \text{SL}$	$0.065 + 0.025 \cdot \text{SL}$	$0.061 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.241 + 0.014 \cdot \text{SL}$	$0.244 + 0.014 \cdot \text{SL}$	$0.245 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.250	$0.215 + 0.017 \cdot \text{SL}$	$0.225 + 0.015 \cdot \text{SL}$	$0.233 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.112	$0.053 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.114	$0.061 + 0.026 \cdot \text{SL}$	$0.065 + 0.025 \cdot \text{SL}$	$0.062 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.289	$0.260 + 0.014 \cdot \text{SL}$	$0.264 + 0.014 \cdot \text{SL}$	$0.264 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.248	$0.214 + 0.017 \cdot \text{SL}$	$0.223 + 0.015 \cdot \text{SL}$	$0.231 + 0.014 \cdot \text{SL}$
D to Y	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.112	$0.060 + 0.026 \cdot \text{SL}$	$0.063 + 0.025 \cdot \text{SL}$	$0.060 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.247	$0.218 + 0.014 \cdot \text{SL}$	$0.221 + 0.014 \cdot \text{SL}$	$0.222 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.231	$0.197 + 0.017 \cdot \text{SL}$	$0.206 + 0.015 \cdot \text{SL}$	$0.214 + 0.014 \cdot \text{SL}$
E to Y	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.112	$0.060 + 0.026 \cdot \text{SL}$	$0.063 + 0.025 \cdot \text{SL}$	$0.060 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.268	$0.239 + 0.014 \cdot \text{SL}$	$0.243 + 0.014 \cdot \text{SL}$	$0.244 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.228	$0.193 + 0.017 \cdot \text{SL}$	$0.203 + 0.015 \cdot \text{SL}$	$0.211 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## ND5/ND5D2/ND5D4

### 5-Input NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### ND5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.078	$0.050 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$	$0.040 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.067 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.248	$0.231 + 0.008 \cdot \text{SL}$	$0.236 + 0.007 \cdot \text{SL}$	$0.240 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.254	$0.233 + 0.011 \cdot \text{SL}$	$0.242 + 0.008 \cdot \text{SL}$	$0.258 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.079	$0.051 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$	$0.040 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.066 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.271	$0.254 + 0.008 \cdot \text{SL}$	$0.259 + 0.007 \cdot \text{SL}$	$0.263 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.257	$0.236 + 0.011 \cdot \text{SL}$	$0.245 + 0.008 \cdot \text{SL}$	$0.261 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.080	$0.052 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$	$0.041 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.068 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.291	$0.274 + 0.008 \cdot \text{SL}$	$0.279 + 0.007 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.255	$0.234 + 0.011 \cdot \text{SL}$	$0.243 + 0.008 \cdot \text{SL}$	$0.259 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.081	$0.052 + 0.015 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.066 + 0.013 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.246	$0.229 + 0.008 \cdot \text{SL}$	$0.234 + 0.007 \cdot \text{SL}$	$0.239 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.238	$0.216 + 0.011 \cdot \text{SL}$	$0.225 + 0.008 \cdot \text{SL}$	$0.242 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.082	$0.053 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.066 + 0.013 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.268	$0.251 + 0.008 \cdot \text{SL}$	$0.256 + 0.007 \cdot \text{SL}$	$0.261 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.234	$0.213 + 0.011 \cdot \text{SL}$	$0.222 + 0.008 \cdot \text{SL}$	$0.238 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## ND5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.077	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.053 + 0.007 \cdot \text{SL}$
	$t_F$	0.110	$0.095 + 0.007 \cdot \text{SL}$	$0.098 + 0.007 \cdot \text{SL}$	$0.101 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.274	$0.264 + 0.005 \cdot \text{SL}$	$0.269 + 0.004 \cdot \text{SL}$	$0.279 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.303	$0.289 + 0.007 \cdot \text{SL}$	$0.297 + 0.005 \cdot \text{SL}$	$0.320 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_F$	0.109	$0.094 + 0.007 \cdot \text{SL}$	$0.096 + 0.007 \cdot \text{SL}$	$0.102 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.298	$0.287 + 0.005 \cdot \text{SL}$	$0.292 + 0.004 \cdot \text{SL}$	$0.303 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.306	$0.292 + 0.007 \cdot \text{SL}$	$0.300 + 0.005 \cdot \text{SL}$	$0.323 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.079	$0.064 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.056 + 0.007 \cdot \text{SL}$
	$t_F$	0.108	$0.092 + 0.008 \cdot \text{SL}$	$0.098 + 0.007 \cdot \text{SL}$	$0.102 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.318	$0.308 + 0.005 \cdot \text{SL}$	$0.313 + 0.004 \cdot \text{SL}$	$0.324 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.304	$0.290 + 0.007 \cdot \text{SL}$	$0.298 + 0.005 \cdot \text{SL}$	$0.321 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_F$	0.109	$0.093 + 0.008 \cdot \text{SL}$	$0.098 + 0.007 \cdot \text{SL}$	$0.101 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.259 + 0.005 \cdot \text{SL}$	$0.265 + 0.004 \cdot \text{SL}$	$0.276 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.286	$0.272 + 0.007 \cdot \text{SL}$	$0.280 + 0.005 \cdot \text{SL}$	$0.303 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.081	$0.066 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.109	$0.094 + 0.007 \cdot \text{SL}$	$0.097 + 0.007 \cdot \text{SL}$	$0.101 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.292	$0.281 + 0.005 \cdot \text{SL}$	$0.287 + 0.004 \cdot \text{SL}$	$0.298 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.283	$0.269 + 0.007 \cdot \text{SL}$	$0.277 + 0.005 \cdot \text{SL}$	$0.300 + 0.004 \cdot \text{SL}$

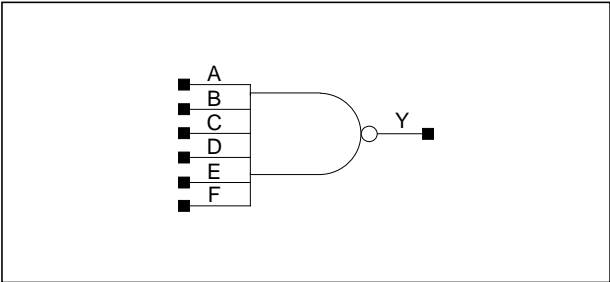
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# ND6/ND6D2/ND6D4

## 6-Input NAND with 1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	E	F	Y
1	1	1	1	1	1	0
Other States						1

### Cell Data

Input Load (SL)																	
ND6						ND6D2						ND6D4					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.8	0.9	0.9	0.9	0.9	0.9	0.8	0.9	0.9	0.9	0.9	0.9	0.8	0.9	0.9	0.9	0.9	0.9
Gate Count																	
ND6						ND6D2						ND6D4					
3.33						3.67						4.33					



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## ND6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.109	$0.052 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.117	$0.062 + 0.027 \cdot \text{SL}$	$0.065 + 0.026 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.250	$0.222 + 0.014 \cdot \text{SL}$	$0.225 + 0.013 \cdot \text{SL}$	$0.226 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.252	$0.216 + 0.018 \cdot \text{SL}$	$0.226 + 0.016 \cdot \text{SL}$	$0.234 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.110	$0.052 + 0.029 \cdot \text{SL}$	$0.048 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.116	$0.062 + 0.027 \cdot \text{SL}$	$0.066 + 0.026 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.273	$0.244 + 0.014 \cdot \text{SL}$	$0.248 + 0.013 \cdot \text{SL}$	$0.248 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.255	$0.219 + 0.018 \cdot \text{SL}$	$0.228 + 0.016 \cdot \text{SL}$	$0.237 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.111	$0.054 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.044 + 0.030 \cdot \text{SL}$
	$t_F$	0.117	$0.063 + 0.027 \cdot \text{SL}$	$0.066 + 0.026 \cdot \text{SL}$	$0.062 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.292	$0.263 + 0.014 \cdot \text{SL}$	$0.267 + 0.013 \cdot \text{SL}$	$0.268 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.253	$0.217 + 0.018 \cdot \text{SL}$	$0.227 + 0.016 \cdot \text{SL}$	$0.235 + 0.015 \cdot \text{SL}$
D to Y	$t_R$	0.113	$0.056 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.030 \cdot \text{SL}$
	$t_F$	0.117	$0.063 + 0.027 \cdot \text{SL}$	$0.066 + 0.026 \cdot \text{SL}$	$0.062 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.234 + 0.014 \cdot \text{SL}$	$0.238 + 0.013 \cdot \text{SL}$	$0.239 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.225 + 0.018 \cdot \text{SL}$	$0.235 + 0.016 \cdot \text{SL}$	$0.243 + 0.015 \cdot \text{SL}$
E to Y	$t_R$	0.113	$0.056 + 0.028 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$	$0.046 + 0.030 \cdot \text{SL}$
	$t_F$	0.118	$0.064 + 0.027 \cdot \text{SL}$	$0.066 + 0.026 \cdot \text{SL}$	$0.062 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.286	$0.257 + 0.014 \cdot \text{SL}$	$0.261 + 0.013 \cdot \text{SL}$	$0.262 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.264	$0.228 + 0.018 \cdot \text{SL}$	$0.238 + 0.016 \cdot \text{SL}$	$0.246 + 0.015 \cdot \text{SL}$
F to Y	$t_R$	0.114	$0.057 + 0.028 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$	$0.045 + 0.030 \cdot \text{SL}$
	$t_F$	0.118	$0.064 + 0.027 \cdot \text{SL}$	$0.067 + 0.026 \cdot \text{SL}$	$0.062 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.305	$0.276 + 0.014 \cdot \text{SL}$	$0.281 + 0.013 \cdot \text{SL}$	$0.282 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.264	$0.228 + 0.018 \cdot \text{SL}$	$0.238 + 0.016 \cdot \text{SL}$	$0.246 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## ND6/ND6D2/ND6D4

### 6-Input NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### ND6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.079	$0.051 + 0.014 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$	$0.041 + 0.015 \cdot \text{SL}$
	$t_F$	0.094	$0.068 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.252	$0.236 + 0.008 \cdot \text{SL}$	$0.241 + 0.007 \cdot \text{SL}$	$0.245 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.257	$0.236 + 0.011 \cdot \text{SL}$	$0.245 + 0.009 \cdot \text{SL}$	$0.261 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.080	$0.051 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$	$0.041 + 0.015 \cdot \text{SL}$
	$t_F$	0.094	$0.067 + 0.014 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.276	$0.259 + 0.008 \cdot \text{SL}$	$0.264 + 0.007 \cdot \text{SL}$	$0.269 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.260	$0.239 + 0.011 \cdot \text{SL}$	$0.248 + 0.009 \cdot \text{SL}$	$0.264 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.081	$0.053 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.094	$0.068 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.295	$0.278 + 0.008 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$	$0.289 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.258	$0.237 + 0.011 \cdot \text{SL}$	$0.246 + 0.009 \cdot \text{SL}$	$0.262 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.083	$0.054 + 0.014 \cdot \text{SL}$	$0.053 + 0.014 \cdot \text{SL}$	$0.043 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.069 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.246 + 0.008 \cdot \text{SL}$	$0.252 + 0.007 \cdot \text{SL}$	$0.257 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.266	$0.244 + 0.011 \cdot \text{SL}$	$0.254 + 0.009 \cdot \text{SL}$	$0.270 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.083	$0.054 + 0.014 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$	$0.043 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.068 + 0.014 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.286	$0.269 + 0.008 \cdot \text{SL}$	$0.275 + 0.007 \cdot \text{SL}$	$0.280 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.269	$0.247 + 0.011 \cdot \text{SL}$	$0.257 + 0.009 \cdot \text{SL}$	$0.273 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.068 + 0.014 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.306	$0.289 + 0.008 \cdot \text{SL}$	$0.295 + 0.007 \cdot \text{SL}$	$0.300 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.269	$0.247 + 0.011 \cdot \text{SL}$	$0.256 + 0.009 \cdot \text{SL}$	$0.273 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## ND6D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.110	$0.094 + 0.008 \cdot \text{SL}$	$0.099 + 0.007 \cdot \text{SL}$	$0.103 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.279	$0.269 + 0.005 \cdot \text{SL}$	$0.274 + 0.004 \cdot \text{SL}$	$0.285 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.305	$0.291 + 0.007 \cdot \text{SL}$	$0.299 + 0.005 \cdot \text{SL}$	$0.322 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.078	$0.063 + 0.008 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.110	$0.096 + 0.007 \cdot \text{SL}$	$0.096 + 0.007 \cdot \text{SL}$	$0.102 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.303	$0.293 + 0.005 \cdot \text{SL}$	$0.298 + 0.004 \cdot \text{SL}$	$0.309 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.308	$0.294 + 0.007 \cdot \text{SL}$	$0.302 + 0.005 \cdot \text{SL}$	$0.326 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.057 + 0.008 \cdot \text{SL}$
	$t_F$	0.108	$0.093 + 0.008 \cdot \text{SL}$	$0.098 + 0.007 \cdot \text{SL}$	$0.103 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.324	$0.313 + 0.005 \cdot \text{SL}$	$0.318 + 0.004 \cdot \text{SL}$	$0.329 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.306	$0.292 + 0.007 \cdot \text{SL}$	$0.300 + 0.005 \cdot \text{SL}$	$0.323 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$	$0.058 + 0.008 \cdot \text{SL}$
	$t_F$	0.110	$0.095 + 0.008 \cdot \text{SL}$	$0.099 + 0.007 \cdot \text{SL}$	$0.103 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.288	$0.277 + 0.005 \cdot \text{SL}$	$0.283 + 0.004 \cdot \text{SL}$	$0.294 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.314	$0.300 + 0.007 \cdot \text{SL}$	$0.308 + 0.005 \cdot \text{SL}$	$0.332 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.059 + 0.008 \cdot \text{SL}$
	$t_F$	0.110	$0.097 + 0.007 \cdot \text{SL}$	$0.097 + 0.007 \cdot \text{SL}$	$0.102 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.312	$0.301 + 0.005 \cdot \text{SL}$	$0.306 + 0.004 \cdot \text{SL}$	$0.318 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.317	$0.303 + 0.007 \cdot \text{SL}$	$0.311 + 0.005 \cdot \text{SL}$	$0.335 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.084	$0.070 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.110	$0.097 + 0.007 \cdot \text{SL}$	$0.097 + 0.007 \cdot \text{SL}$	$0.102 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.332	$0.322 + 0.005 \cdot \text{SL}$	$0.327 + 0.004 \cdot \text{SL}$	$0.339 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.317	$0.303 + 0.007 \cdot \text{SL}$	$0.311 + 0.005 \cdot \text{SL}$	$0.334 + 0.004 \cdot \text{SL}$

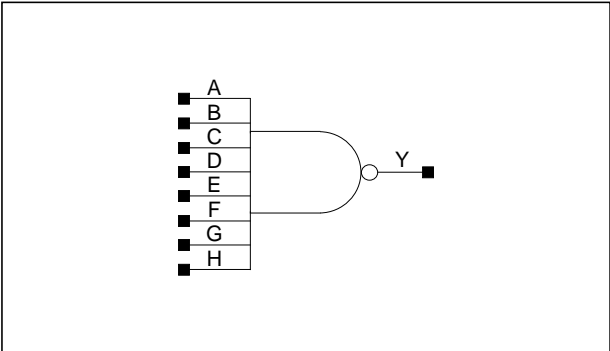
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



ND8/ND8D2/ND8D4

8-Input NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	1	1	1	1	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
ND8								ND8
A	B	C	D	E	F	G	H	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	4.00
ND8D2								ND8D2
A	B	C	D	E	F	G	H	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	4.33
ND8D4								ND8D4
A	B	C	D	E	F	G	H	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	5.00



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## ND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.111	$0.052 + 0.029 \cdot \text{SL}$	$0.048 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.119	$0.065 + 0.027 \cdot \text{SL}$	$0.067 + 0.026 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.269	$0.240 + 0.014 \cdot \text{SL}$	$0.243 + 0.014 \cdot \text{SL}$	$0.244 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.273	$0.237 + 0.018 \cdot \text{SL}$	$0.247 + 0.016 \cdot \text{SL}$	$0.255 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.112	$0.054 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.118	$0.064 + 0.027 \cdot \text{SL}$	$0.067 + 0.026 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.295	$0.266 + 0.014 \cdot \text{SL}$	$0.270 + 0.014 \cdot \text{SL}$	$0.271 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.283	$0.247 + 0.018 \cdot \text{SL}$	$0.257 + 0.016 \cdot \text{SL}$	$0.265 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.119	$0.065 + 0.027 \cdot \text{SL}$	$0.067 + 0.026 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.318	$0.289 + 0.015 \cdot \text{SL}$	$0.293 + 0.014 \cdot \text{SL}$	$0.294 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.253 + 0.018 \cdot \text{SL}$	$0.263 + 0.016 \cdot \text{SL}$	$0.271 + 0.015 \cdot \text{SL}$
D to Y	$t_R$	0.115	$0.058 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.119	$0.065 + 0.027 \cdot \text{SL}$	$0.067 + 0.026 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.338	$0.309 + 0.015 \cdot \text{SL}$	$0.312 + 0.014 \cdot \text{SL}$	$0.313 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.292	$0.256 + 0.018 \cdot \text{SL}$	$0.266 + 0.016 \cdot \text{SL}$	$0.274 + 0.015 \cdot \text{SL}$
E to Y	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.119	$0.065 + 0.027 \cdot \text{SL}$	$0.066 + 0.026 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.282	$0.253 + 0.015 \cdot \text{SL}$	$0.257 + 0.014 \cdot \text{SL}$	$0.258 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.279	$0.243 + 0.018 \cdot \text{SL}$	$0.253 + 0.016 \cdot \text{SL}$	$0.261 + 0.015 \cdot \text{SL}$
F to Y	$t_R$	0.115	$0.058 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.120	$0.066 + 0.027 \cdot \text{SL}$	$0.068 + 0.026 \cdot \text{SL}$	$0.064 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.280 + 0.015 \cdot \text{SL}$	$0.284 + 0.014 \cdot \text{SL}$	$0.285 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.288	$0.251 + 0.018 \cdot \text{SL}$	$0.261 + 0.016 \cdot \text{SL}$	$0.270 + 0.015 \cdot \text{SL}$
G to Y	$t_R$	0.116	$0.059 + 0.028 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$	$0.047 + 0.031 \cdot \text{SL}$
	$t_F$	0.119	$0.065 + 0.027 \cdot \text{SL}$	$0.066 + 0.026 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.333	$0.304 + 0.015 \cdot \text{SL}$	$0.308 + 0.014 \cdot \text{SL}$	$0.309 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.294	$0.257 + 0.018 \cdot \text{SL}$	$0.268 + 0.016 \cdot \text{SL}$	$0.276 + 0.015 \cdot \text{SL}$
H to Y	$t_R$	0.118	$0.061 + 0.028 \cdot \text{SL}$	$0.054 + 0.030 \cdot \text{SL}$	$0.048 + 0.031 \cdot \text{SL}$
	$t_F$	0.119	$0.065 + 0.027 \cdot \text{SL}$	$0.066 + 0.026 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.353	$0.323 + 0.015 \cdot \text{SL}$	$0.328 + 0.014 \cdot \text{SL}$	$0.329 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.297	$0.261 + 0.018 \cdot \text{SL}$	$0.271 + 0.016 \cdot \text{SL}$	$0.279 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# ND8/ND8D2/ND8D4

## 8-Input NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### ND8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.080	$0.051 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$	$0.040 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.068 + 0.014 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.253 + 0.008 \cdot \text{SL}$	$0.259 + 0.007 \cdot \text{SL}$	$0.264 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.280	$0.258 + 0.011 \cdot \text{SL}$	$0.268 + 0.009 \cdot \text{SL}$	$0.284 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.081	$0.053 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$	$0.041 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.068 + 0.014 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.298	$0.281 + 0.008 \cdot \text{SL}$	$0.286 + 0.007 \cdot \text{SL}$	$0.291 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.291	$0.269 + 0.011 \cdot \text{SL}$	$0.278 + 0.009 \cdot \text{SL}$	$0.294 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.082	$0.054 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$	$0.043 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.067 + 0.014 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.321	$0.304 + 0.009 \cdot \text{SL}$	$0.310 + 0.007 \cdot \text{SL}$	$0.315 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.297	$0.274 + 0.011 \cdot \text{SL}$	$0.284 + 0.009 \cdot \text{SL}$	$0.300 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$	$0.044 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.069 + 0.014 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.342	$0.325 + 0.009 \cdot \text{SL}$	$0.330 + 0.007 \cdot \text{SL}$	$0.335 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.278 + 0.011 \cdot \text{SL}$	$0.287 + 0.009 \cdot \text{SL}$	$0.303 + 0.008 \cdot \text{SL}$
E to Y	$t_R$	0.083	$0.056 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$	$0.043 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.069 + 0.014 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.282	$0.265 + 0.009 \cdot \text{SL}$	$0.271 + 0.007 \cdot \text{SL}$	$0.275 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.285	$0.263 + 0.011 \cdot \text{SL}$	$0.273 + 0.009 \cdot \text{SL}$	$0.289 + 0.008 \cdot \text{SL}$
F to Y	$t_R$	0.084	$0.057 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$	$0.044 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.070 + 0.014 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.292 + 0.009 \cdot \text{SL}$	$0.298 + 0.007 \cdot \text{SL}$	$0.303 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.294	$0.272 + 0.011 \cdot \text{SL}$	$0.281 + 0.009 \cdot \text{SL}$	$0.298 + 0.008 \cdot \text{SL}$
G to Y	$t_R$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.069 + 0.014 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.334	$0.316 + 0.009 \cdot \text{SL}$	$0.322 + 0.007 \cdot \text{SL}$	$0.328 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.278 + 0.011 \cdot \text{SL}$	$0.287 + 0.009 \cdot \text{SL}$	$0.304 + 0.008 \cdot \text{SL}$
H to Y	$t_R$	0.087	$0.060 + 0.013 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.068 + 0.015 \cdot \text{SL}$	$0.074 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.354	$0.337 + 0.009 \cdot \text{SL}$	$0.343 + 0.007 \cdot \text{SL}$	$0.348 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.304	$0.281 + 0.011 \cdot \text{SL}$	$0.291 + 0.009 \cdot \text{SL}$	$0.307 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## ND8D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.079	$0.064 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.112	$0.098 + 0.007 \cdot \text{SL}$	$0.099 + 0.007 \cdot \text{SL}$	$0.104 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.299	$0.288 + 0.005 \cdot \text{SL}$	$0.293 + 0.004 \cdot \text{SL}$	$0.305 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.330	$0.316 + 0.007 \cdot \text{SL}$	$0.324 + 0.005 \cdot \text{SL}$	$0.347 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.057 + 0.008 \cdot \text{SL}$
	$t_F$	0.112	$0.098 + 0.007 \cdot \text{SL}$	$0.100 + 0.007 \cdot \text{SL}$	$0.104 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.327	$0.316 + 0.005 \cdot \text{SL}$	$0.321 + 0.004 \cdot \text{SL}$	$0.332 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.340	$0.326 + 0.007 \cdot \text{SL}$	$0.334 + 0.005 \cdot \text{SL}$	$0.357 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.110	$0.094 + 0.008 \cdot \text{SL}$	$0.100 + 0.007 \cdot \text{SL}$	$0.105 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.351	$0.341 + 0.005 \cdot \text{SL}$	$0.346 + 0.004 \cdot \text{SL}$	$0.357 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.346	$0.332 + 0.007 \cdot \text{SL}$	$0.340 + 0.005 \cdot \text{SL}$	$0.363 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.084	$0.070 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_F$	0.111	$0.094 + 0.008 \cdot \text{SL}$	$0.100 + 0.007 \cdot \text{SL}$	$0.105 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.373	$0.362 + 0.005 \cdot \text{SL}$	$0.367 + 0.004 \cdot \text{SL}$	$0.379 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.349	$0.335 + 0.007 \cdot \text{SL}$	$0.343 + 0.005 \cdot \text{SL}$	$0.366 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.083	$0.069 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.113	$0.098 + 0.007 \cdot \text{SL}$	$0.100 + 0.007 \cdot \text{SL}$	$0.104 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.298 + 0.005 \cdot \text{SL}$	$0.304 + 0.004 \cdot \text{SL}$	$0.315 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.334	$0.320 + 0.007 \cdot \text{SL}$	$0.328 + 0.005 \cdot \text{SL}$	$0.352 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_F$	0.112	$0.098 + 0.007 \cdot \text{SL}$	$0.101 + 0.007 \cdot \text{SL}$	$0.104 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.337	$0.326 + 0.005 \cdot \text{SL}$	$0.331 + 0.004 \cdot \text{SL}$	$0.343 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.343	$0.328 + 0.007 \cdot \text{SL}$	$0.337 + 0.005 \cdot \text{SL}$	$0.360 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_F$	0.112	$0.099 + 0.007 \cdot \text{SL}$	$0.100 + 0.007 \cdot \text{SL}$	$0.104 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.362	$0.351 + 0.005 \cdot \text{SL}$	$0.357 + 0.004 \cdot \text{SL}$	$0.369 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.349	$0.335 + 0.007 \cdot \text{SL}$	$0.343 + 0.005 \cdot \text{SL}$	$0.366 + 0.004 \cdot \text{SL}$
H to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.111	$0.095 + 0.008 \cdot \text{SL}$	$0.100 + 0.007 \cdot \text{SL}$	$0.105 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.383	$0.372 + 0.005 \cdot \text{SL}$	$0.378 + 0.004 \cdot \text{SL}$	$0.390 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.352	$0.338 + 0.007 \cdot \text{SL}$	$0.346 + 0.005 \cdot \text{SL}$	$0.370 + 0.004 \cdot \text{SL}$

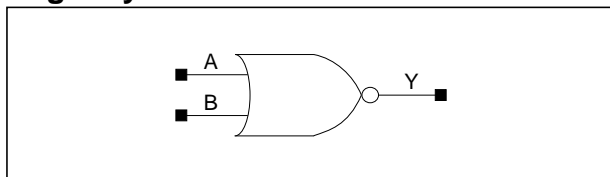
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# NR2DH/NR2/NR2D2/NR2D2B/NR2D4/NR2A

## 2-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X/(2X/1X) Drive

### Logic Symbol



### Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

### Cell Data

Input Load (SL)											
NR2DH		NR2		NR2D2		NR2D2B		NR2D4		NR2A	
A	B	A	B	A	B	A	B	A	B	A	B
0.5	0.5	1.0	1.0	1.9	2.1	1.0	1.1	1.0	1.1	1.5	1.7
Gate Count											
NR2DH		NR2		NR2D2		NR2D2B		NR2D4		NR2A	
1.00		1.00		1.67		2.33		3.00		1.67	

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.380	$0.130 + 0.125 \cdot \text{SL}$	$0.111 + 0.130 \cdot \text{SL}$	$0.101 + 0.131 \cdot \text{SL}$
	$t_F$	0.173	$0.083 + 0.045 \cdot \text{SL}$	$0.064 + 0.050 \cdot \text{SL}$	$0.046 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.197	$0.087 + 0.055 \cdot \text{SL}$	$0.084 + 0.056 \cdot \text{SL}$	$0.082 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.066 + 0.027 \cdot \text{SL}$	$0.066 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.375	$0.121 + 0.127 \cdot \text{SL}$	$0.110 + 0.130 \cdot \text{SL}$	$0.102 + 0.131 \cdot \text{SL}$
	$t_F$	0.194	$0.105 + 0.045 \cdot \text{SL}$	$0.085 + 0.050 \cdot \text{SL}$	$0.065 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.197	$0.085 + 0.056 \cdot \text{SL}$	$0.084 + 0.056 \cdot \text{SL}$	$0.083 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.129	$0.072 + 0.028 \cdot \text{SL}$	$0.076 + 0.027 \cdot \text{SL}$	$0.076 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### NR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.227	$0.119 + 0.054 \cdot \text{SL}$	$0.106 + 0.057 \cdot \text{SL}$	$0.093 + 0.059 \cdot \text{SL}$
	$t_F$	0.127	$0.081 + 0.023 \cdot \text{SL}$	$0.072 + 0.025 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.124	$0.072 + 0.026 \cdot \text{SL}$	$0.075 + 0.025 \cdot \text{SL}$	$0.073 + 0.025 \cdot \text{SL}$
	$t_{PHL}$	0.085	$0.049 + 0.018 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.221	$0.110 + 0.056 \cdot \text{SL}$	$0.099 + 0.058 \cdot \text{SL}$	$0.090 + 0.059 \cdot \text{SL}$
	$t_F$	0.149	$0.105 + 0.022 \cdot \text{SL}$	$0.096 + 0.025 \cdot \text{SL}$	$0.080 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.122	$0.069 + 0.026 \cdot \text{SL}$	$0.073 + 0.025 \cdot \text{SL}$	$0.071 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.100	$0.067 + 0.017 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# NR2DH/NR2/NR2D2/NR2D2B/NR2D4/NR2A

## 2-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X/(2X/1X) Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.164	$0.113 + 0.026 \cdot \text{SL}$	$0.103 + 0.028 \cdot \text{SL}$	$0.086 + 0.029 \cdot \text{SL}$
	$t_F$	0.098	$0.073 + 0.012 \cdot \text{SL}$	$0.076 + 0.012 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.092	$0.063 + 0.015 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.061	$0.039 + 0.011 \cdot \text{SL}$	$0.052 + 0.008 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.157	$0.104 + 0.026 \cdot \text{SL}$	$0.094 + 0.029 \cdot \text{SL}$	$0.082 + 0.030 \cdot \text{SL}$
	$t_F$	0.124	$0.102 + 0.011 \cdot \text{SL}$	$0.098 + 0.012 \cdot \text{SL}$	$0.081 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.091	$0.062 + 0.014 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.079	$0.059 + 0.010 \cdot \text{SL}$	$0.068 + 0.008 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### NR2D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.071	$0.043 + 0.014 \cdot \text{SL}$	$0.039 + 0.015 \cdot \text{SL}$	$0.033 + 0.015 \cdot \text{SL}$
	$t_F$	0.072	$0.045 + 0.013 \cdot \text{SL}$	$0.046 + 0.013 \cdot \text{SL}$	$0.042 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.196	$0.181 + 0.008 \cdot \text{SL}$	$0.185 + 0.007 \cdot \text{SL}$	$0.187 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.171 + 0.010 \cdot \text{SL}$	$0.179 + 0.008 \cdot \text{SL}$	$0.187 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.071	$0.043 + 0.014 \cdot \text{SL}$	$0.040 + 0.015 \cdot \text{SL}$	$0.033 + 0.015 \cdot \text{SL}$
	$t_F$	0.072	$0.045 + 0.014 \cdot \text{SL}$	$0.048 + 0.013 \cdot \text{SL}$	$0.042 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.196	$0.180 + 0.008 \cdot \text{SL}$	$0.184 + 0.007 \cdot \text{SL}$	$0.187 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.192 + 0.010 \cdot \text{SL}$	$0.199 + 0.008 \cdot \text{SL}$	$0.207 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### NR2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.067	$0.053 + 0.007 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$	$0.044 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.062 + 0.008 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.210 + 0.005 \cdot \text{SL}$	$0.214 + 0.004 \cdot \text{SL}$	$0.221 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.223	$0.211 + 0.006 \cdot \text{SL}$	$0.217 + 0.004 \cdot \text{SL}$	$0.233 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.068	$0.053 + 0.007 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$	$0.044 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.210 + 0.005 \cdot \text{SL}$	$0.213 + 0.004 \cdot \text{SL}$	$0.221 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.243	$0.231 + 0.006 \cdot \text{SL}$	$0.237 + 0.004 \cdot \text{SL}$	$0.253 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## NR2DH/NR2/NR2D2/NR2D2B/NR2D4/NR2A

### 2-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X/(2X/1X) Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.166	$0.116 + 0.025 \cdot \text{SL}$	$0.105 + 0.028 \cdot \text{SL}$	$0.093 + 0.029 \cdot \text{SL}$
	$t_F$	0.125	$0.078 + 0.024 \cdot \text{SL}$	$0.070 + 0.025 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.079	$0.046 + 0.016 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.099	$0.065 + 0.017 \cdot \text{SL}$	$0.075 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.153	$0.101 + 0.026 \cdot \text{SL}$	$0.090 + 0.029 \cdot \text{SL}$	$0.080 + 0.030 \cdot \text{SL}$
	$t_F$	0.164	$0.117 + 0.024 \cdot \text{SL}$	$0.108 + 0.026 \cdot \text{SL}$	$0.098 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.082	$0.052 + 0.015 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.128	$0.098 + 0.015 \cdot \text{SL}$	$0.100 + 0.014 \cdot \text{SL}$	$0.100 + 0.014 \cdot \text{SL}$

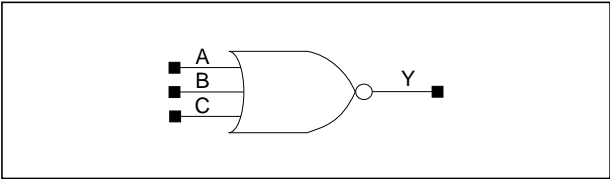
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# NR3DH/NR3/NR3D2/NR3D2B/NR3D4/NR3A

## 3-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X/(2X/1X) Drive

### Logic Symbol



### Truth Table

A	B	C	Y
0	0	0	1
Other States			0

### Cell Data

Input Load (SL)																	
NR3DH			NR3			NR3D2			NR3D2B			NR3D4			NR3A		
A	B	C	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
0.6	0.6	0.6	0.9	0.9	0.9	1.8	2.0	2.0	0.9	0.9	1.0	0.9	0.9	1.0	1.4	1.6	1.7
Gate Count																	
NR3DH			NR3			NR3D2			NR3D2B			NR3D4			NR3A		
1.33			1.33			2.33			2.67			3.33			2.00		



# NR3DH/NR3/NR3D2/NR3D2B/NR3D4/NR3A

## 3-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X/(2X/1X) Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR3DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.476	$0.200 + 0.138 \cdot \text{SL}$	$0.184 + 0.142 \cdot \text{SL}$	$0.180 + 0.143 \cdot \text{SL}$
	$t_F$	0.183	$0.091 + 0.046 \cdot \text{SL}$	$0.075 + 0.050 \cdot \text{SL}$	$0.058 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.099 + 0.060 \cdot \text{SL}$	$0.096 + 0.061 \cdot \text{SL}$	$0.094 + 0.061 \cdot \text{SL}$
	$t_{PHL}$	0.129	$0.073 + 0.028 \cdot \text{SL}$	$0.077 + 0.027 \cdot \text{SL}$	$0.077 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.478	$0.200 + 0.139 \cdot \text{SL}$	$0.190 + 0.142 \cdot \text{SL}$	$0.182 + 0.142 \cdot \text{SL}$
	$t_F$	0.207	$0.114 + 0.047 \cdot \text{SL}$	$0.100 + 0.050 \cdot \text{SL}$	$0.082 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.240	$0.117 + 0.061 \cdot \text{SL}$	$0.117 + 0.061 \cdot \text{SL}$	$0.118 + 0.061 \cdot \text{SL}$
	$t_{PHL}$	0.146	$0.091 + 0.028 \cdot \text{SL}$	$0.092 + 0.027 \cdot \text{SL}$	$0.092 + 0.027 \cdot \text{SL}$
C to Y	$t_R$	0.475	$0.195 + 0.140 \cdot \text{SL}$	$0.187 + 0.142 \cdot \text{SL}$	$0.182 + 0.142 \cdot \text{SL}$
	$t_F$	0.234	$0.140 + 0.047 \cdot \text{SL}$	$0.128 + 0.050 \cdot \text{SL}$	$0.110 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.248	$0.124 + 0.062 \cdot \text{SL}$	$0.125 + 0.061 \cdot \text{SL}$	$0.126 + 0.061 \cdot \text{SL}$
	$t_{PHL}$	0.154	$0.097 + 0.028 \cdot \text{SL}$	$0.100 + 0.028 \cdot \text{SL}$	$0.103 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### NR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.352	$0.183 + 0.085 \cdot \text{SL}$	$0.172 + 0.087 \cdot \text{SL}$	$0.158 + 0.089 \cdot \text{SL}$
	$t_F$	0.148	$0.088 + 0.030 \cdot \text{SL}$	$0.077 + 0.032 \cdot \text{SL}$	$0.062 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.164	$0.090 + 0.037 \cdot \text{SL}$	$0.087 + 0.038 \cdot \text{SL}$	$0.085 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.107	$0.066 + 0.020 \cdot \text{SL}$	$0.075 + 0.018 \cdot \text{SL}$	$0.074 + 0.018 \cdot \text{SL}$
B to Y	$t_R$	0.353	$0.182 + 0.085 \cdot \text{SL}$	$0.173 + 0.088 \cdot \text{SL}$	$0.164 + 0.089 \cdot \text{SL}$
	$t_F$	0.174	$0.115 + 0.029 \cdot \text{SL}$	$0.103 + 0.032 \cdot \text{SL}$	$0.088 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.182	$0.105 + 0.038 \cdot \text{SL}$	$0.106 + 0.038 \cdot \text{SL}$	$0.106 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.125	$0.086 + 0.019 \cdot \text{SL}$	$0.090 + 0.018 \cdot \text{SL}$	$0.090 + 0.018 \cdot \text{SL}$
C to Y	$t_R$	0.349	$0.176 + 0.086 \cdot \text{SL}$	$0.169 + 0.088 \cdot \text{SL}$	$0.162 + 0.089 \cdot \text{SL}$
	$t_F$	0.199	$0.138 + 0.031 \cdot \text{SL}$	$0.131 + 0.032 \cdot \text{SL}$	$0.118 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.189	$0.112 + 0.038 \cdot \text{SL}$	$0.112 + 0.038 \cdot \text{SL}$	$0.113 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.133	$0.095 + 0.019 \cdot \text{SL}$	$0.097 + 0.019 \cdot \text{SL}$	$0.100 + 0.018 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# NR3DH/NR3/NR3D2/NR3D2B/NR3D4/NR3A

## 3-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X/(2X/1X) Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t <sub>R</sub>	0.247	$0.165 + 0.041 \cdot \text{SL}$	$0.157 + 0.043 \cdot \text{SL}$	$0.139 + 0.044 \cdot \text{SL}$
	t <sub>F</sub>	0.110	$0.079 + 0.015 \cdot \text{SL}$	$0.079 + 0.015 \cdot \text{SL}$	$0.059 + 0.017 \cdot \text{SL}$
	t <sub>PLH</sub>	0.116	$0.078 + 0.019 \cdot \text{SL}$	$0.079 + 0.019 \cdot \text{SL}$	$0.075 + 0.019 \cdot \text{SL}$
	t <sub>PHL</sub>	0.078	$0.053 + 0.012 \cdot \text{SL}$	$0.066 + 0.009 \cdot \text{SL}$	$0.069 + 0.009 \cdot \text{SL}$
B to Y	t <sub>R</sub>	0.247	$0.164 + 0.041 \cdot \text{SL}$	$0.156 + 0.043 \cdot \text{SL}$	$0.144 + 0.044 \cdot \text{SL}$
	t <sub>F</sub>	0.137	$0.109 + 0.014 \cdot \text{SL}$	$0.102 + 0.016 \cdot \text{SL}$	$0.085 + 0.017 \cdot \text{SL}$
	t <sub>PLH</sub>	0.133	$0.093 + 0.020 \cdot \text{SL}$	$0.097 + 0.019 \cdot \text{SL}$	$0.097 + 0.019 \cdot \text{SL}$
	t <sub>PHL</sub>	0.099	$0.077 + 0.011 \cdot \text{SL}$	$0.084 + 0.009 \cdot \text{SL}$	$0.086 + 0.009 \cdot \text{SL}$
C to Y	t <sub>R</sub>	0.241	$0.157 + 0.042 \cdot \text{SL}$	$0.150 + 0.044 \cdot \text{SL}$	$0.141 + 0.044 \cdot \text{SL}$
	t <sub>F</sub>	0.163	$0.133 + 0.015 \cdot \text{SL}$	$0.129 + 0.016 \cdot \text{SL}$	$0.114 + 0.017 \cdot \text{SL}$
	t <sub>PLH</sub>	0.139	$0.099 + 0.020 \cdot \text{SL}$	$0.102 + 0.019 \cdot \text{SL}$	$0.103 + 0.019 \cdot \text{SL}$
	t <sub>PHL</sub>	0.107	$0.085 + 0.011 \cdot \text{SL}$	$0.091 + 0.009 \cdot \text{SL}$	$0.094 + 0.009 \cdot \text{SL}$

\*Group1 : SL < 4, \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 : 13 < SL

#### NR3D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t <sub>R</sub>	0.075	$0.046 + 0.014 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$	$0.036 + 0.015 \cdot \text{SL}$
	t <sub>F</sub>	0.071	$0.043 + 0.014 \cdot \text{SL}$	$0.048 + 0.013 \cdot \text{SL}$	$0.041 + 0.014 \cdot \text{SL}$
	t <sub>PLH</sub>	0.239	$0.223 + 0.008 \cdot \text{SL}$	$0.228 + 0.007 \cdot \text{SL}$	$0.231 + 0.007 \cdot \text{SL}$
	t <sub>PHL</sub>	0.213	$0.194 + 0.010 \cdot \text{SL}$	$0.201 + 0.008 \cdot \text{SL}$	$0.209 + 0.007 \cdot \text{SL}$
B to Y	t <sub>R</sub>	0.076	$0.049 + 0.014 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$	$0.036 + 0.015 \cdot \text{SL}$
	t <sub>F</sub>	0.073	$0.046 + 0.013 \cdot \text{SL}$	$0.047 + 0.013 \cdot \text{SL}$	$0.041 + 0.014 \cdot \text{SL}$
	t <sub>PLH</sub>	0.256	$0.240 + 0.008 \cdot \text{SL}$	$0.245 + 0.007 \cdot \text{SL}$	$0.248 + 0.007 \cdot \text{SL}$
	t <sub>PHL</sub>	0.235	$0.215 + 0.010 \cdot \text{SL}$	$0.223 + 0.008 \cdot \text{SL}$	$0.230 + 0.007 \cdot \text{SL}$
C to Y	t <sub>R</sub>	0.076	$0.048 + 0.014 \cdot \text{SL}$	$0.046 + 0.014 \cdot \text{SL}$	$0.036 + 0.015 \cdot \text{SL}$
	t <sub>F</sub>	0.072	$0.043 + 0.015 \cdot \text{SL}$	$0.048 + 0.013 \cdot \text{SL}$	$0.042 + 0.014 \cdot \text{SL}$
	t <sub>PLH</sub>	0.265	$0.249 + 0.008 \cdot \text{SL}$	$0.254 + 0.007 \cdot \text{SL}$	$0.257 + 0.007 \cdot \text{SL}$
	t <sub>PHL</sub>	0.249	$0.230 + 0.010 \cdot \text{SL}$	$0.237 + 0.008 \cdot \text{SL}$	$0.245 + 0.007 \cdot \text{SL}$

\*Group1 : SL < 4, \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 : 13 < SL



# NR3DH/NR3/NR3D2/NR3D2B/NR3D4/NR3A

## 3-Input NOR with 0.5X/1X/2X/2X(Buffered)/4X/(2X/1X) Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.073	$0.059 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$	$0.048 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.059 + 0.008 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.261	$0.252 + 0.005 \cdot \text{SL}$	$0.256 + 0.004 \cdot \text{SL}$	$0.264 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.228 + 0.006 \cdot \text{SL}$	$0.234 + 0.004 \cdot \text{SL}$	$0.250 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.074	$0.060 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$	$0.049 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.061 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.279	$0.269 + 0.005 \cdot \text{SL}$	$0.273 + 0.004 \cdot \text{SL}$	$0.281 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.262	$0.250 + 0.006 \cdot \text{SL}$	$0.256 + 0.004 \cdot \text{SL}$	$0.272 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.073	$0.058 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$	$0.048 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.061 + 0.008 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.287	$0.277 + 0.005 \cdot \text{SL}$	$0.282 + 0.004 \cdot \text{SL}$	$0.290 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.276	$0.264 + 0.006 \cdot \text{SL}$	$0.270 + 0.004 \cdot \text{SL}$	$0.286 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$

#### NR3A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.241	$0.159 + 0.041 \cdot \text{SL}$	$0.150 + 0.043 \cdot \text{SL}$	$0.137 + 0.045 \cdot \text{SL}$
	$t_F$	0.147	$0.085 + 0.031 \cdot \text{SL}$	$0.077 + 0.033 \cdot \text{SL}$	$0.065 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.101	$0.060 + 0.021 \cdot \text{SL}$	$0.066 + 0.019 \cdot \text{SL}$	$0.064 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.122	$0.083 + 0.019 \cdot \text{SL}$	$0.088 + 0.018 \cdot \text{SL}$	$0.087 + 0.018 \cdot \text{SL}$
B to Y	$t_R$	0.238	$0.155 + 0.042 \cdot \text{SL}$	$0.146 + 0.044 \cdot \text{SL}$	$0.138 + 0.045 \cdot \text{SL}$
	$t_F$	0.195	$0.132 + 0.031 \cdot \text{SL}$	$0.124 + 0.033 \cdot \text{SL}$	$0.114 + 0.035 \cdot \text{SL}$
	$t_{PLH}$	0.123	$0.080 + 0.021 \cdot \text{SL}$	$0.087 + 0.020 \cdot \text{SL}$	$0.087 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.157	$0.120 + 0.019 \cdot \text{SL}$	$0.121 + 0.018 \cdot \text{SL}$	$0.122 + 0.018 \cdot \text{SL}$
C to Y	$t_R$	0.231	$0.145 + 0.043 \cdot \text{SL}$	$0.138 + 0.044 \cdot \text{SL}$	$0.132 + 0.045 \cdot \text{SL}$
	$t_F$	0.246	$0.181 + 0.032 \cdot \text{SL}$	$0.178 + 0.033 \cdot \text{SL}$	$0.167 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.133	$0.091 + 0.021 \cdot \text{SL}$	$0.095 + 0.020 \cdot \text{SL}$	$0.096 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.177	$0.138 + 0.020 \cdot \text{SL}$	$0.141 + 0.019 \cdot \text{SL}$	$0.145 + 0.018 \cdot \text{SL}$

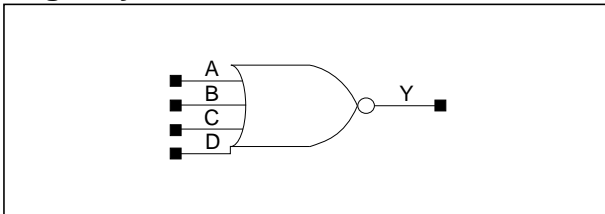
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# NR4DH/NR4/NR4D2/NR4D4

## 4-Input NOR with 0.5X/1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	Y
0	0	0	0	1
Other States				0

### Cell Data

Input Load (SL)															
NR4DH				NR4				NR4D2				NR4D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.6	0.6	0.6	1.0	1.0	1.0	1.1	1.0	1.0	1.0	1.1	1.0	1.0	1.0	1.1
Gate Count															
NR4DH				NR4				NR4D2				NR4D4			
3.00				3.00				3.33				4.00			

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR4DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.197	$0.069 + 0.064 \cdot \text{SL}$	$0.063 + 0.065 \cdot \text{SL}$	$0.057 + 0.066 \cdot \text{SL}$
	$t_F$	0.168	$0.068 + 0.050 \cdot \text{SL}$	$0.063 + 0.051 \cdot \text{SL}$	$0.054 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.294	$0.235 + 0.030 \cdot \text{SL}$	$0.239 + 0.029 \cdot \text{SL}$	$0.240 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.270	$0.211 + 0.030 \cdot \text{SL}$	$0.220 + 0.027 \cdot \text{SL}$	$0.222 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.197	$0.069 + 0.064 \cdot \text{SL}$	$0.063 + 0.065 \cdot \text{SL}$	$0.057 + 0.066 \cdot \text{SL}$
	$t_F$	0.167	$0.067 + 0.050 \cdot \text{SL}$	$0.063 + 0.051 \cdot \text{SL}$	$0.054 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.295	$0.235 + 0.030 \cdot \text{SL}$	$0.239 + 0.029 \cdot \text{SL}$	$0.240 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.288	$0.229 + 0.030 \cdot \text{SL}$	$0.238 + 0.027 \cdot \text{SL}$	$0.240 + 0.027 \cdot \text{SL}$
C to Y	$t_R$	0.197	$0.068 + 0.064 \cdot \text{SL}$	$0.063 + 0.065 \cdot \text{SL}$	$0.056 + 0.066 \cdot \text{SL}$
	$t_F$	0.172	$0.073 + 0.049 \cdot \text{SL}$	$0.067 + 0.051 \cdot \text{SL}$	$0.057 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.288	$0.228 + 0.030 \cdot \text{SL}$	$0.233 + 0.029 \cdot \text{SL}$	$0.234 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.285	$0.224 + 0.030 \cdot \text{SL}$	$0.235 + 0.028 \cdot \text{SL}$	$0.238 + 0.027 \cdot \text{SL}$
D to Y	$t_R$	0.197	$0.069 + 0.064 \cdot \text{SL}$	$0.063 + 0.065 \cdot \text{SL}$	$0.056 + 0.066 \cdot \text{SL}$
	$t_F$	0.172	$0.073 + 0.049 \cdot \text{SL}$	$0.068 + 0.051 \cdot \text{SL}$	$0.057 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.288	$0.229 + 0.030 \cdot \text{SL}$	$0.233 + 0.029 \cdot \text{SL}$	$0.234 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.303	$0.243 + 0.030 \cdot \text{SL}$	$0.254 + 0.028 \cdot \text{SL}$	$0.257 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# NR4DH/NR4/NR4D2/NR4D4

## 4-Input NOR with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$	$0.048 + 0.030 \cdot \text{SL}$
	$t_F$	0.109	$0.056 + 0.026 \cdot \text{SL}$	$0.054 + 0.027 \cdot \text{SL}$	$0.048 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.225	$0.195 + 0.015 \cdot \text{SL}$	$0.200 + 0.013 \cdot \text{SL}$	$0.203 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.219	$0.186 + 0.017 \cdot \text{SL}$	$0.193 + 0.015 \cdot \text{SL}$	$0.196 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$
	$t_F$	0.107	$0.053 + 0.027 \cdot \text{SL}$	$0.054 + 0.027 \cdot \text{SL}$	$0.049 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.223	$0.194 + 0.015 \cdot \text{SL}$	$0.199 + 0.013 \cdot \text{SL}$	$0.201 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.238	$0.205 + 0.017 \cdot \text{SL}$	$0.212 + 0.015 \cdot \text{SL}$	$0.215 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$
	$t_F$	0.111	$0.058 + 0.026 \cdot \text{SL}$	$0.057 + 0.027 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.220	$0.190 + 0.015 \cdot \text{SL}$	$0.195 + 0.014 \cdot \text{SL}$	$0.198 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.228	$0.194 + 0.017 \cdot \text{SL}$	$0.202 + 0.015 \cdot \text{SL}$	$0.206 + 0.015 \cdot \text{SL}$
D to Y	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$	$0.048 + 0.030 \cdot \text{SL}$
	$t_F$	0.113	$0.061 + 0.026 \cdot \text{SL}$	$0.059 + 0.026 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.189 + 0.015 \cdot \text{SL}$	$0.195 + 0.013 \cdot \text{SL}$	$0.197 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.247	$0.213 + 0.017 \cdot \text{SL}$	$0.221 + 0.015 \cdot \text{SL}$	$0.226 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### NR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.083	$0.053 + 0.015 \cdot \text{SL}$	$0.055 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.053 + 0.014 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.224	$0.207 + 0.009 \cdot \text{SL}$	$0.213 + 0.007 \cdot \text{SL}$	$0.220 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.191 + 0.010 \cdot \text{SL}$	$0.199 + 0.008 \cdot \text{SL}$	$0.209 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.083	$0.054 + 0.015 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.079	$0.051 + 0.014 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.223	$0.206 + 0.009 \cdot \text{SL}$	$0.212 + 0.007 \cdot \text{SL}$	$0.219 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.230	$0.210 + 0.010 \cdot \text{SL}$	$0.217 + 0.008 \cdot \text{SL}$	$0.228 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.083	$0.054 + 0.015 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.201 + 0.009 \cdot \text{SL}$	$0.208 + 0.007 \cdot \text{SL}$	$0.215 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.221	$0.201 + 0.010 \cdot \text{SL}$	$0.209 + 0.008 \cdot \text{SL}$	$0.221 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.082	$0.052 + 0.015 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.218	$0.200 + 0.009 \cdot \text{SL}$	$0.207 + 0.007 \cdot \text{SL}$	$0.215 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.241	$0.221 + 0.010 \cdot \text{SL}$	$0.229 + 0.008 \cdot \text{SL}$	$0.241 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# NR4DH/NR4/NR4D2/NR4D4

## 4-Input NOR with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.086	$0.072 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$
	$t_F$	0.084	$0.069 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.262	$0.251 + 0.005 \cdot \text{SL}$	$0.256 + 0.004 \cdot \text{SL}$	$0.271 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.228 + 0.006 \cdot \text{SL}$	$0.234 + 0.005 \cdot \text{SL}$	$0.252 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$
	$t_F$	0.084	$0.069 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.261	$0.250 + 0.005 \cdot \text{SL}$	$0.255 + 0.004 \cdot \text{SL}$	$0.270 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.258	$0.246 + 0.006 \cdot \text{SL}$	$0.252 + 0.005 \cdot \text{SL}$	$0.270 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.086	$0.071 + 0.008 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.253	$0.242 + 0.005 \cdot \text{SL}$	$0.248 + 0.004 \cdot \text{SL}$	$0.263 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.247	$0.234 + 0.006 \cdot \text{SL}$	$0.241 + 0.005 \cdot \text{SL}$	$0.260 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.086	$0.072 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$
	$t_F$	0.090	$0.077 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.253	$0.242 + 0.005 \cdot \text{SL}$	$0.247 + 0.004 \cdot \text{SL}$	$0.262 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.267	$0.254 + 0.006 \cdot \text{SL}$	$0.261 + 0.005 \cdot \text{SL}$	$0.280 + 0.004 \cdot \text{SL}$

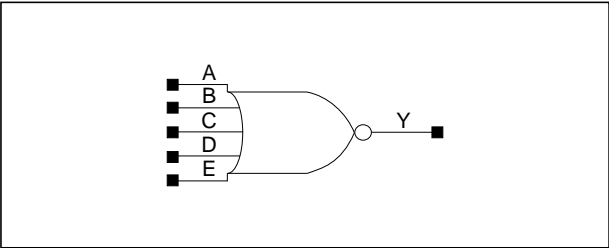
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



NR5/NR5D2/NR5D4

5-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	1
Other States					0

Cell Data

Input Load (SL)															Gate Count		
NR5					NR5D2					NR5D4					NR5	NR5D2	NR5D4
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E			
0.9	0.9	1.0	1.0	1.1	0.9	0.9	1.0	1.0	1.1	0.9	0.9	1.0	1.0	1.1	3.33	3.67	4.33



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**NR5**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$
	$t_F$	0.108	$0.056 + 0.026 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.048 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.264	$0.234 + 0.015 \cdot \text{SL}$	$0.240 + 0.013 \cdot \text{SL}$	$0.242 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.243	$0.209 + 0.017 \cdot \text{SL}$	$0.216 + 0.015 \cdot \text{SL}$	$0.220 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.117	$0.060 + 0.028 \cdot \text{SL}$	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$
	$t_F$	0.109	$0.057 + 0.026 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.048 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.281	$0.251 + 0.015 \cdot \text{SL}$	$0.256 + 0.014 \cdot \text{SL}$	$0.258 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.264	$0.231 + 0.017 \cdot \text{SL}$	$0.238 + 0.015 \cdot \text{SL}$	$0.241 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$
	$t_F$	0.109	$0.056 + 0.026 \cdot \text{SL}$	$0.055 + 0.027 \cdot \text{SL}$	$0.050 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.289	$0.259 + 0.015 \cdot \text{SL}$	$0.264 + 0.013 \cdot \text{SL}$	$0.267 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.244 + 0.017 \cdot \text{SL}$	$0.251 + 0.015 \cdot \text{SL}$	$0.254 + 0.014 \cdot \text{SL}$
D to Y	$t_R$	0.113	$0.056 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$	$0.048 + 0.030 \cdot \text{SL}$
	$t_F$	0.112	$0.058 + 0.027 \cdot \text{SL}$	$0.059 + 0.026 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.217	$0.188 + 0.015 \cdot \text{SL}$	$0.193 + 0.014 \cdot \text{SL}$	$0.195 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.228	$0.194 + 0.017 \cdot \text{SL}$	$0.202 + 0.015 \cdot \text{SL}$	$0.206 + 0.015 \cdot \text{SL}$
E to Y	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$
	$t_F$	0.113	$0.061 + 0.026 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.216	$0.187 + 0.015 \cdot \text{SL}$	$0.192 + 0.013 \cdot \text{SL}$	$0.194 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.248	$0.214 + 0.017 \cdot \text{SL}$	$0.222 + 0.015 \cdot \text{SL}$	$0.226 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## NR5/NR5D2/NR5D4

### 5-Input NOR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.053 + 0.014 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$	$0.053 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.252 + 0.009 \cdot \text{SL}$	$0.258 + 0.007 \cdot \text{SL}$	$0.267 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.244	$0.224 + 0.010 \cdot \text{SL}$	$0.232 + 0.008 \cdot \text{SL}$	$0.243 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.088	$0.059 + 0.014 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$	$0.053 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.287	$0.269 + 0.009 \cdot \text{SL}$	$0.275 + 0.007 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.265	$0.245 + 0.010 \cdot \text{SL}$	$0.253 + 0.008 \cdot \text{SL}$	$0.264 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.087	$0.058 + 0.015 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.054 + 0.014 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.295	$0.277 + 0.009 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$	$0.291 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.279	$0.259 + 0.010 \cdot \text{SL}$	$0.267 + 0.008 \cdot \text{SL}$	$0.278 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.083	$0.054 + 0.015 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.218	$0.200 + 0.009 \cdot \text{SL}$	$0.207 + 0.007 \cdot \text{SL}$	$0.215 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.227	$0.206 + 0.011 \cdot \text{SL}$	$0.215 + 0.008 \cdot \text{SL}$	$0.227 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.082	$0.052 + 0.015 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.217	$0.199 + 0.009 \cdot \text{SL}$	$0.206 + 0.007 \cdot \text{SL}$	$0.214 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.247	$0.226 + 0.011 \cdot \text{SL}$	$0.235 + 0.008 \cdot \text{SL}$	$0.247 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**NR5D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.091	$0.077 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.093	$0.080 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.298 + 0.005 \cdot \text{SL}$	$0.303 + 0.004 \cdot \text{SL}$	$0.318 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.287	$0.274 + 0.006 \cdot \text{SL}$	$0.281 + 0.005 \cdot \text{SL}$	$0.300 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.092	$0.078 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.093	$0.079 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.326	$0.315 + 0.005 \cdot \text{SL}$	$0.320 + 0.004 \cdot \text{SL}$	$0.335 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.308	$0.295 + 0.006 \cdot \text{SL}$	$0.302 + 0.005 \cdot \text{SL}$	$0.322 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.092	$0.078 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.095	$0.082 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.334	$0.323 + 0.005 \cdot \text{SL}$	$0.328 + 0.004 \cdot \text{SL}$	$0.343 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.323	$0.310 + 0.006 \cdot \text{SL}$	$0.317 + 0.005 \cdot \text{SL}$	$0.336 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.100	$0.088 + 0.006 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.248	$0.237 + 0.005 \cdot \text{SL}$	$0.243 + 0.004 \cdot \text{SL}$	$0.257 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.266	$0.253 + 0.007 \cdot \text{SL}$	$0.261 + 0.005 \cdot \text{SL}$	$0.282 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.085	$0.070 + 0.008 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.100	$0.086 + 0.007 \cdot \text{SL}$	$0.088 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.247	$0.236 + 0.005 \cdot \text{SL}$	$0.242 + 0.004 \cdot \text{SL}$	$0.257 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.286	$0.273 + 0.007 \cdot \text{SL}$	$0.281 + 0.005 \cdot \text{SL}$	$0.302 + 0.004 \cdot \text{SL}$

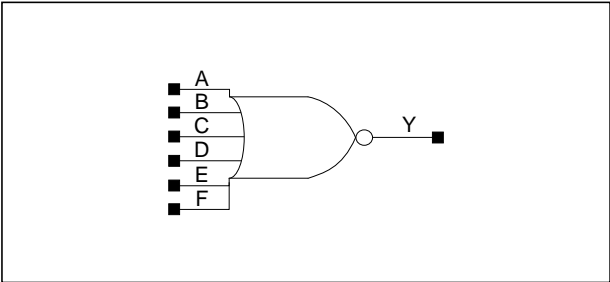
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



NR6/NR6D2/NR6D4

6-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
Other States						0

Cell Data

Input Load (SL)																	
NR6						NR6D2						NR6D4					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.9	0.9	1.0	0.9	1.0	1.0	0.9	0.9	1.0	0.9	1.0	1.0	0.9	0.9	1.0	0.9	1.0	1.0
Gate Count																	
NR6						NR6D2						NR6D4					
3.67						4.00						4.67					



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## NR6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$
	$t_F$	0.108	$0.056 + 0.026 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$	$0.048 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.266	$0.236 + 0.015 \cdot \text{SL}$	$0.242 + 0.013 \cdot \text{SL}$	$0.244 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.241	$0.208 + 0.017 \cdot \text{SL}$	$0.215 + 0.015 \cdot \text{SL}$	$0.218 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.117	$0.060 + 0.029 \cdot \text{SL}$	$0.056 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$
	$t_F$	0.108	$0.056 + 0.026 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.048 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.283	$0.253 + 0.015 \cdot \text{SL}$	$0.258 + 0.013 \cdot \text{SL}$	$0.260 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.263	$0.229 + 0.017 \cdot \text{SL}$	$0.236 + 0.015 \cdot \text{SL}$	$0.240 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.056 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$
	$t_F$	0.109	$0.056 + 0.026 \cdot \text{SL}$	$0.055 + 0.027 \cdot \text{SL}$	$0.049 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.291	$0.261 + 0.015 \cdot \text{SL}$	$0.266 + 0.013 \cdot \text{SL}$	$0.269 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.276	$0.242 + 0.017 \cdot \text{SL}$	$0.249 + 0.015 \cdot \text{SL}$	$0.253 + 0.014 \cdot \text{SL}$
D to Y	$t_R$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.055 + 0.030 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$
	$t_F$	0.113	$0.061 + 0.026 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.253	$0.223 + 0.015 \cdot \text{SL}$	$0.228 + 0.014 \cdot \text{SL}$	$0.231 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.250	$0.216 + 0.017 \cdot \text{SL}$	$0.224 + 0.015 \cdot \text{SL}$	$0.228 + 0.015 \cdot \text{SL}$
E to Y	$t_R$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$
	$t_F$	0.112	$0.059 + 0.026 \cdot \text{SL}$	$0.059 + 0.026 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.240 + 0.015 \cdot \text{SL}$	$0.245 + 0.014 \cdot \text{SL}$	$0.248 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.272	$0.238 + 0.017 \cdot \text{SL}$	$0.246 + 0.015 \cdot \text{SL}$	$0.250 + 0.015 \cdot \text{SL}$
F to Y	$t_R$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$
	$t_F$	0.114	$0.062 + 0.026 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.278	$0.248 + 0.015 \cdot \text{SL}$	$0.254 + 0.014 \cdot \text{SL}$	$0.257 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.286	$0.252 + 0.017 \cdot \text{SL}$	$0.260 + 0.015 \cdot \text{SL}$	$0.265 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## NR6/NR6D2/NR6D4

### 6-Input NOR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.054 + 0.014 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.053 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.253 + 0.009 \cdot \text{SL}$	$0.259 + 0.007 \cdot \text{SL}$	$0.267 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.244	$0.224 + 0.010 \cdot \text{SL}$	$0.232 + 0.008 \cdot \text{SL}$	$0.243 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.088	$0.059 + 0.014 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.054 + 0.014 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.287	$0.270 + 0.009 \cdot \text{SL}$	$0.276 + 0.007 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.266	$0.245 + 0.010 \cdot \text{SL}$	$0.253 + 0.008 \cdot \text{SL}$	$0.264 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.087	$0.058 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.054 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.295	$0.278 + 0.009 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$	$0.292 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.279	$0.259 + 0.010 \cdot \text{SL}$	$0.267 + 0.008 \cdot \text{SL}$	$0.278 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.086	$0.056 + 0.015 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.059 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.254	$0.237 + 0.009 \cdot \text{SL}$	$0.243 + 0.007 \cdot \text{SL}$	$0.251 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.251	$0.230 + 0.011 \cdot \text{SL}$	$0.239 + 0.008 \cdot \text{SL}$	$0.251 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.086	$0.056 + 0.015 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.060 + 0.014 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.271	$0.253 + 0.009 \cdot \text{SL}$	$0.260 + 0.007 \cdot \text{SL}$	$0.268 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.273	$0.252 + 0.011 \cdot \text{SL}$	$0.261 + 0.008 \cdot \text{SL}$	$0.273 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.085	$0.056 + 0.015 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.063 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.280	$0.262 + 0.009 \cdot \text{SL}$	$0.268 + 0.007 \cdot \text{SL}$	$0.277 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.288	$0.267 + 0.010 \cdot \text{SL}$	$0.276 + 0.008 \cdot \text{SL}$	$0.288 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## NR6D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.091	$0.077 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.093	$0.080 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.298 + 0.005 \cdot \text{SL}$	$0.304 + 0.004 \cdot \text{SL}$	$0.318 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.287	$0.274 + 0.006 \cdot \text{SL}$	$0.281 + 0.005 \cdot \text{SL}$	$0.301 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.091	$0.078 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.093	$0.080 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.326	$0.315 + 0.005 \cdot \text{SL}$	$0.321 + 0.004 \cdot \text{SL}$	$0.336 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.309	$0.296 + 0.006 \cdot \text{SL}$	$0.303 + 0.005 \cdot \text{SL}$	$0.322 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.092	$0.078 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.095	$0.081 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.334	$0.323 + 0.005 \cdot \text{SL}$	$0.329 + 0.004 \cdot \text{SL}$	$0.344 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.323	$0.310 + 0.006 \cdot \text{SL}$	$0.317 + 0.005 \cdot \text{SL}$	$0.337 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.088	$0.074 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.100	$0.085 + 0.008 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.287	$0.276 + 0.006 \cdot \text{SL}$	$0.281 + 0.004 \cdot \text{SL}$	$0.296 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.291	$0.278 + 0.007 \cdot \text{SL}$	$0.285 + 0.005 \cdot \text{SL}$	$0.306 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.088	$0.074 + 0.007 \cdot \text{SL}$	$0.074 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.101	$0.086 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.303	$0.292 + 0.006 \cdot \text{SL}$	$0.298 + 0.004 \cdot \text{SL}$	$0.313 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.313	$0.300 + 0.007 \cdot \text{SL}$	$0.308 + 0.005 \cdot \text{SL}$	$0.329 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.088	$0.074 + 0.007 \cdot \text{SL}$	$0.074 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.101	$0.087 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$	$0.091 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.312	$0.301 + 0.006 \cdot \text{SL}$	$0.306 + 0.004 \cdot \text{SL}$	$0.322 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.329	$0.315 + 0.007 \cdot \text{SL}$	$0.323 + 0.005 \cdot \text{SL}$	$0.344 + 0.004 \cdot \text{SL}$

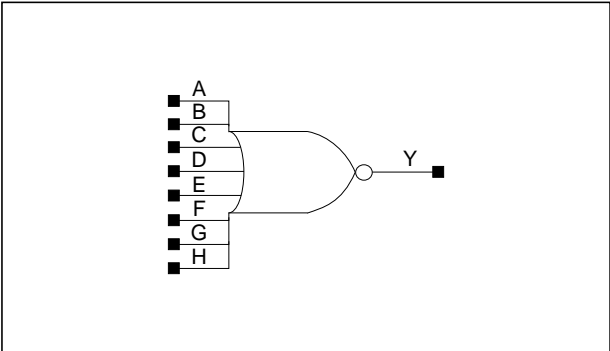
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



NR8/NR8D2/NR8D4

8-Input NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
NR8								NR8
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	4.67
NR8D2								NR8D2
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	1.0	5.00
NR8D4								NR8D4
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	0.9	1.0	5.67



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## NR8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.126	$0.068 + 0.029 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.113	$0.060 + 0.026 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$	$0.054 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.281	$0.248 + 0.016 \cdot \text{SL}$	$0.256 + 0.014 \cdot \text{SL}$	$0.262 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.273	$0.238 + 0.017 \cdot \text{SL}$	$0.247 + 0.015 \cdot \text{SL}$	$0.252 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.126	$0.067 + 0.029 \cdot \text{SL}$	$0.067 + 0.030 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.112	$0.058 + 0.027 \cdot \text{SL}$	$0.060 + 0.027 \cdot \text{SL}$	$0.054 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.299	$0.267 + 0.016 \cdot \text{SL}$	$0.275 + 0.014 \cdot \text{SL}$	$0.281 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.265 + 0.017 \cdot \text{SL}$	$0.273 + 0.015 \cdot \text{SL}$	$0.279 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.127	$0.068 + 0.029 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$	$0.062 + 0.030 \cdot \text{SL}$
	$t_F$	0.115	$0.062 + 0.026 \cdot \text{SL}$	$0.062 + 0.026 \cdot \text{SL}$	$0.056 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.308	$0.275 + 0.016 \cdot \text{SL}$	$0.283 + 0.014 \cdot \text{SL}$	$0.289 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.318	$0.283 + 0.017 \cdot \text{SL}$	$0.291 + 0.015 \cdot \text{SL}$	$0.297 + 0.015 \cdot \text{SL}$
D to Y	$t_R$	0.128	$0.069 + 0.029 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$	$0.064 + 0.030 \cdot \text{SL}$
	$t_F$	0.119	$0.067 + 0.026 \cdot \text{SL}$	$0.067 + 0.026 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.281	$0.248 + 0.016 \cdot \text{SL}$	$0.256 + 0.014 \cdot \text{SL}$	$0.263 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.254 + 0.018 \cdot \text{SL}$	$0.263 + 0.015 \cdot \text{SL}$	$0.270 + 0.015 \cdot \text{SL}$
E to Y	$t_R$	0.128	$0.071 + 0.029 \cdot \text{SL}$	$0.068 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.120	$0.068 + 0.026 \cdot \text{SL}$	$0.067 + 0.026 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.299	$0.266 + 0.016 \cdot \text{SL}$	$0.275 + 0.014 \cdot \text{SL}$	$0.281 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.316	$0.281 + 0.018 \cdot \text{SL}$	$0.290 + 0.015 \cdot \text{SL}$	$0.297 + 0.015 \cdot \text{SL}$
F to Y	$t_R$	0.128	$0.070 + 0.029 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$	$0.064 + 0.030 \cdot \text{SL}$
	$t_F$	0.120	$0.068 + 0.026 \cdot \text{SL}$	$0.068 + 0.026 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.307	$0.275 + 0.016 \cdot \text{SL}$	$0.283 + 0.014 \cdot \text{SL}$	$0.289 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.335	$0.299 + 0.018 \cdot \text{SL}$	$0.309 + 0.015 \cdot \text{SL}$	$0.315 + 0.015 \cdot \text{SL}$
G to Y	$t_R$	0.126	$0.067 + 0.029 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$	$0.062 + 0.030 \cdot \text{SL}$
	$t_F$	0.126	$0.073 + 0.026 \cdot \text{SL}$	$0.074 + 0.026 \cdot \text{SL}$	$0.068 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.226 + 0.016 \cdot \text{SL}$	$0.234 + 0.014 \cdot \text{SL}$	$0.240 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.295	$0.259 + 0.018 \cdot \text{SL}$	$0.270 + 0.016 \cdot \text{SL}$	$0.277 + 0.015 \cdot \text{SL}$
H to Y	$t_R$	0.125	$0.066 + 0.030 \cdot \text{SL}$	$0.067 + 0.029 \cdot \text{SL}$	$0.062 + 0.030 \cdot \text{SL}$
	$t_F$	0.126	$0.073 + 0.026 \cdot \text{SL}$	$0.073 + 0.026 \cdot \text{SL}$	$0.067 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.225 + 0.016 \cdot \text{SL}$	$0.234 + 0.014 \cdot \text{SL}$	$0.240 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.282 + 0.018 \cdot \text{SL}$	$0.293 + 0.016 \cdot \text{SL}$	$0.301 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# NR8/NR8D2/NR8D4

## 8-Input NOR with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NR8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.096	$0.066 + 0.015 \cdot \text{SL}$	$0.066 + 0.015 \cdot \text{SL}$	$0.065 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.057 + 0.015 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.286	$0.266 + 0.010 \cdot \text{SL}$	$0.274 + 0.008 \cdot \text{SL}$	$0.287 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.275	$0.253 + 0.011 \cdot \text{SL}$	$0.262 + 0.009 \cdot \text{SL}$	$0.276 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.098	$0.069 + 0.014 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.059 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.304	$0.284 + 0.010 \cdot \text{SL}$	$0.292 + 0.008 \cdot \text{SL}$	$0.305 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.301	$0.280 + 0.011 \cdot \text{SL}$	$0.288 + 0.009 \cdot \text{SL}$	$0.302 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.097	$0.066 + 0.016 \cdot \text{SL}$	$0.069 + 0.015 \cdot \text{SL}$	$0.066 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.062 + 0.014 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.312	$0.292 + 0.010 \cdot \text{SL}$	$0.300 + 0.008 \cdot \text{SL}$	$0.313 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.298 + 0.011 \cdot \text{SL}$	$0.307 + 0.009 \cdot \text{SL}$	$0.321 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.097	$0.066 + 0.016 \cdot \text{SL}$	$0.069 + 0.015 \cdot \text{SL}$	$0.066 + 0.015 \cdot \text{SL}$
	$t_F$	0.094	$0.068 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.282	$0.262 + 0.010 \cdot \text{SL}$	$0.270 + 0.008 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.288	$0.266 + 0.011 \cdot \text{SL}$	$0.276 + 0.009 \cdot \text{SL}$	$0.292 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.098	$0.067 + 0.015 \cdot \text{SL}$	$0.069 + 0.015 \cdot \text{SL}$	$0.065 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.067 + 0.014 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.301	$0.280 + 0.010 \cdot \text{SL}$	$0.289 + 0.008 \cdot \text{SL}$	$0.302 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.316	$0.293 + 0.011 \cdot \text{SL}$	$0.303 + 0.009 \cdot \text{SL}$	$0.319 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.097	$0.067 + 0.015 \cdot \text{SL}$	$0.068 + 0.015 \cdot \text{SL}$	$0.066 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.068 + 0.014 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.289 + 0.010 \cdot \text{SL}$	$0.297 + 0.008 \cdot \text{SL}$	$0.311 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.334	$0.312 + 0.011 \cdot \text{SL}$	$0.322 + 0.009 \cdot \text{SL}$	$0.338 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.095	$0.063 + 0.016 \cdot \text{SL}$	$0.066 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.075 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.257	$0.237 + 0.010 \cdot \text{SL}$	$0.245 + 0.008 \cdot \text{SL}$	$0.258 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.291	$0.268 + 0.012 \cdot \text{SL}$	$0.279 + 0.009 \cdot \text{SL}$	$0.296 + 0.008 \cdot \text{SL}$
H to Y	$t_R$	0.094	$0.064 + 0.015 \cdot \text{SL}$	$0.065 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.103	$0.074 + 0.014 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.075 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.238 + 0.010 \cdot \text{SL}$	$0.246 + 0.008 \cdot \text{SL}$	$0.259 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.316	$0.293 + 0.012 \cdot \text{SL}$	$0.304 + 0.009 \cdot \text{SL}$	$0.321 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## NR8D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.107	$0.093 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$	$0.091 + 0.007 \cdot \text{SL}$
	$t_F$	0.097	$0.082 + 0.008 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.087 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.322 + 0.006 \cdot \text{SL}$	$0.329 + 0.005 \cdot \text{SL}$	$0.348 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.313	$0.300 + 0.007 \cdot \text{SL}$	$0.307 + 0.005 \cdot \text{SL}$	$0.328 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.107	$0.093 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.091 + 0.007 \cdot \text{SL}$
	$t_F$	0.098	$0.084 + 0.007 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.088 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.353	$0.340 + 0.006 \cdot \text{SL}$	$0.347 + 0.005 \cdot \text{SL}$	$0.367 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.340	$0.326 + 0.007 \cdot \text{SL}$	$0.334 + 0.005 \cdot \text{SL}$	$0.355 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.107	$0.092 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$	$0.091 + 0.007 \cdot \text{SL}$
	$t_F$	0.098	$0.083 + 0.008 \cdot \text{SL}$	$0.087 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.361	$0.348 + 0.006 \cdot \text{SL}$	$0.355 + 0.005 \cdot \text{SL}$	$0.375 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.358	$0.345 + 0.007 \cdot \text{SL}$	$0.352 + 0.005 \cdot \text{SL}$	$0.374 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.107	$0.093 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$	$0.091 + 0.007 \cdot \text{SL}$
	$t_F$	0.104	$0.088 + 0.008 \cdot \text{SL}$	$0.093 + 0.007 \cdot \text{SL}$	$0.096 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.325	$0.313 + 0.006 \cdot \text{SL}$	$0.320 + 0.005 \cdot \text{SL}$	$0.340 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.322	$0.308 + 0.007 \cdot \text{SL}$	$0.317 + 0.005 \cdot \text{SL}$	$0.340 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.106	$0.092 + 0.007 \cdot \text{SL}$	$0.091 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$
	$t_F$	0.104	$0.088 + 0.008 \cdot \text{SL}$	$0.094 + 0.007 \cdot \text{SL}$	$0.096 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.344	$0.331 + 0.006 \cdot \text{SL}$	$0.338 + 0.005 \cdot \text{SL}$	$0.358 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.349	$0.335 + 0.007 \cdot \text{SL}$	$0.344 + 0.005 \cdot \text{SL}$	$0.367 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.106	$0.093 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$
	$t_F$	0.106	$0.092 + 0.007 \cdot \text{SL}$	$0.095 + 0.007 \cdot \text{SL}$	$0.095 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.352	$0.339 + 0.006 \cdot \text{SL}$	$0.347 + 0.005 \cdot \text{SL}$	$0.367 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.369	$0.355 + 0.007 \cdot \text{SL}$	$0.363 + 0.005 \cdot \text{SL}$	$0.386 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.105	$0.090 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$
	$t_F$	0.112	$0.098 + 0.007 \cdot \text{SL}$	$0.100 + 0.007 \cdot \text{SL}$	$0.102 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.301	$0.288 + 0.006 \cdot \text{SL}$	$0.295 + 0.005 \cdot \text{SL}$	$0.315 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.327	$0.313 + 0.007 \cdot \text{SL}$	$0.321 + 0.005 \cdot \text{SL}$	$0.346 + 0.004 \cdot \text{SL}$
H to Y	$t_R$	0.105	$0.090 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$
	$t_F$	0.112	$0.096 + 0.008 \cdot \text{SL}$	$0.101 + 0.007 \cdot \text{SL}$	$0.103 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.302	$0.289 + 0.006 \cdot \text{SL}$	$0.296 + 0.005 \cdot \text{SL}$	$0.316 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.352	$0.337 + 0.007 \cdot \text{SL}$	$0.346 + 0.005 \cdot \text{SL}$	$0.370 + 0.004 \cdot \text{SL}$

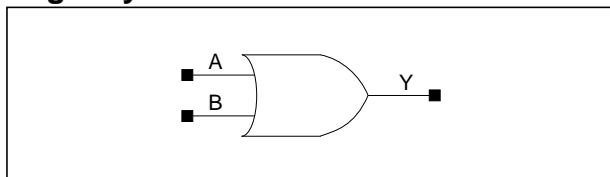
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# OR2DH/OR2/OR2D2/OR2D4

## 2-Input OR with 0.5X/1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

### Cell Data

Input Load (SL)								Gate Count			
OR2DH		OR2		OR2D2		OR2D4		OR2DH	OR2	OR2D2	OR2D4
A	B	A	B	A	B	A	B				
0.5	0.6	0.8	0.8	0.8	0.8	1.0	1.0	1.33	1.33	1.67	2.33

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OR2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.188	$0.059 + 0.064 \cdot \text{SL}$	$0.053 + 0.066 \cdot \text{SL}$	$0.047 + 0.067 \cdot \text{SL}$
	$t_F$	0.175	$0.075 + 0.050 \cdot \text{SL}$	$0.074 + 0.050 \cdot \text{SL}$	$0.064 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.170	$0.112 + 0.029 \cdot \text{SL}$	$0.113 + 0.029 \cdot \text{SL}$	$0.114 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.234	$0.171 + 0.031 \cdot \text{SL}$	$0.185 + 0.028 \cdot \text{SL}$	$0.192 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.191	$0.066 + 0.063 \cdot \text{SL}$	$0.054 + 0.066 \cdot \text{SL}$	$0.048 + 0.066 \cdot \text{SL}$
	$t_F$	0.176	$0.075 + 0.050 \cdot \text{SL}$	$0.075 + 0.050 \cdot \text{SL}$	$0.064 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.189	$0.131 + 0.029 \cdot \text{SL}$	$0.132 + 0.029 \cdot \text{SL}$	$0.132 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.236	$0.173 + 0.031 \cdot \text{SL}$	$0.187 + 0.028 \cdot \text{SL}$	$0.194 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### OR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.120	$0.066 + 0.027 \cdot \text{SL}$	$0.069 + 0.026 \cdot \text{SL}$	$0.065 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.136	$0.107 + 0.014 \cdot \text{SL}$	$0.111 + 0.014 \cdot \text{SL}$	$0.111 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.194	$0.158 + 0.018 \cdot \text{SL}$	$0.167 + 0.016 \cdot \text{SL}$	$0.176 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.121	$0.068 + 0.027 \cdot \text{SL}$	$0.069 + 0.026 \cdot \text{SL}$	$0.065 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.155	$0.126 + 0.014 \cdot \text{SL}$	$0.129 + 0.014 \cdot \text{SL}$	$0.130 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.194	$0.157 + 0.018 \cdot \text{SL}$	$0.167 + 0.016 \cdot \text{SL}$	$0.176 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## OR2DH/OR2/OR2D2/OR2D4

### 2-Input OR with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### OR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.053 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.102	$0.073 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.141	$0.124 + 0.008 \cdot \text{SL}$	$0.130 + 0.007 \cdot \text{SL}$	$0.134 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.206	$0.184 + 0.011 \cdot \text{SL}$	$0.193 + 0.009 \cdot \text{SL}$	$0.211 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.088	$0.064 + 0.012 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$	$0.044 + 0.015 \cdot \text{SL}$
	$t_F$	0.103	$0.075 + 0.014 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.080 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.157	$0.140 + 0.009 \cdot \text{SL}$	$0.146 + 0.007 \cdot \text{SL}$	$0.152 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.207	$0.184 + 0.011 \cdot \text{SL}$	$0.194 + 0.009 \cdot \text{SL}$	$0.211 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### OR2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.078	$0.063 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.053 + 0.008 \cdot \text{SL}$
	$t_F$	0.107	$0.091 + 0.008 \cdot \text{SL}$	$0.095 + 0.007 \cdot \text{SL}$	$0.101 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.155	$0.145 + 0.005 \cdot \text{SL}$	$0.149 + 0.004 \cdot \text{SL}$	$0.160 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.231	$0.217 + 0.007 \cdot \text{SL}$	$0.225 + 0.005 \cdot \text{SL}$	$0.248 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.081	$0.070 + 0.006 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.107	$0.091 + 0.008 \cdot \text{SL}$	$0.096 + 0.007 \cdot \text{SL}$	$0.101 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.170	$0.159 + 0.006 \cdot \text{SL}$	$0.165 + 0.004 \cdot \text{SL}$	$0.176 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.231	$0.217 + 0.007 \cdot \text{SL}$	$0.225 + 0.005 \cdot \text{SL}$	$0.248 + 0.004 \cdot \text{SL}$

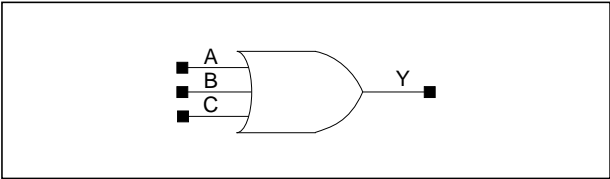
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OR3DH/OR3/OR3D2/OR3D4

3-Input OR with 0.5X/1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
1	x	x	1
x	1	x	1
x	x	1	1

Cell Data

Input Load (SL)											
OR3DH			OR3			OR3D2			OR3D4		
A	B	C	A	B	C	A	B	C	A	B	C
0.6	0.6	0.7	0.7	0.7	0.8	0.7	0.7	0.8	0.9	0.9	1.0
Gate Count											
OR3DH			OR3			OR3D2			OR3D4		
1.67			1.67			2.00			2.67		



# OR3DH/OR3/OR3D2/OR3D4

## 3-Input OR with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OR3DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.190	$0.062 + 0.064 \cdot \text{SL}$	$0.055 + 0.066 \cdot \text{SL}$	$0.049 + 0.066 \cdot \text{SL}$
	$t_F$	0.195	$0.091 + 0.052 \cdot \text{SL}$	$0.098 + 0.050 \cdot \text{SL}$	$0.091 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.189	$0.131 + 0.029 \cdot \text{SL}$	$0.133 + 0.029 \cdot \text{SL}$	$0.133 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.265	$0.196 + 0.034 \cdot \text{SL}$	$0.216 + 0.029 \cdot \text{SL}$	$0.232 + 0.028 \cdot \text{SL}$
B to Y	$t_R$	0.193	$0.065 + 0.064 \cdot \text{SL}$	$0.057 + 0.066 \cdot \text{SL}$	$0.052 + 0.066 \cdot \text{SL}$
	$t_F$	0.197	$0.094 + 0.051 \cdot \text{SL}$	$0.100 + 0.050 \cdot \text{SL}$	$0.092 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.211	$0.152 + 0.030 \cdot \text{SL}$	$0.155 + 0.029 \cdot \text{SL}$	$0.155 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.284	$0.215 + 0.034 \cdot \text{SL}$	$0.235 + 0.029 \cdot \text{SL}$	$0.251 + 0.028 \cdot \text{SL}$
C to Y	$t_R$	0.197	$0.070 + 0.064 \cdot \text{SL}$	$0.064 + 0.065 \cdot \text{SL}$	$0.056 + 0.066 \cdot \text{SL}$
	$t_F$	0.196	$0.093 + 0.052 \cdot \text{SL}$	$0.098 + 0.050 \cdot \text{SL}$	$0.092 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.224	$0.164 + 0.030 \cdot \text{SL}$	$0.169 + 0.029 \cdot \text{SL}$	$0.171 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.295	$0.226 + 0.034 \cdot \text{SL}$	$0.246 + 0.029 \cdot \text{SL}$	$0.261 + 0.028 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### OR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.117	$0.059 + 0.029 \cdot \text{SL}$	$0.054 + 0.030 \cdot \text{SL}$	$0.049 + 0.031 \cdot \text{SL}$
	$t_F$	0.148	$0.091 + 0.028 \cdot \text{SL}$	$0.097 + 0.027 \cdot \text{SL}$	$0.099 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.161	$0.131 + 0.015 \cdot \text{SL}$	$0.137 + 0.014 \cdot \text{SL}$	$0.138 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.242	$0.201 + 0.021 \cdot \text{SL}$	$0.214 + 0.017 \cdot \text{SL}$	$0.230 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.121	$0.064 + 0.029 \cdot \text{SL}$	$0.058 + 0.030 \cdot \text{SL}$	$0.052 + 0.031 \cdot \text{SL}$
	$t_F$	0.150	$0.094 + 0.028 \cdot \text{SL}$	$0.098 + 0.027 \cdot \text{SL}$	$0.100 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.182	$0.151 + 0.015 \cdot \text{SL}$	$0.157 + 0.014 \cdot \text{SL}$	$0.159 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.220 + 0.021 \cdot \text{SL}$	$0.233 + 0.017 \cdot \text{SL}$	$0.249 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.125	$0.066 + 0.029 \cdot \text{SL}$	$0.064 + 0.030 \cdot \text{SL}$	$0.058 + 0.031 \cdot \text{SL}$
	$t_F$	0.148	$0.091 + 0.029 \cdot \text{SL}$	$0.098 + 0.027 \cdot \text{SL}$	$0.101 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.162 + 0.016 \cdot \text{SL}$	$0.169 + 0.014 \cdot \text{SL}$	$0.173 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.271	$0.230 + 0.021 \cdot \text{SL}$	$0.242 + 0.018 \cdot \text{SL}$	$0.258 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## OR3DH/OR3/OR3D2/OR3D4

### 3-Input OR with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### OR3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.091	$0.066 + 0.013 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.142	$0.112 + 0.015 \cdot \text{SL}$	$0.116 + 0.014 \cdot \text{SL}$	$0.123 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.168	$0.150 + 0.009 \cdot \text{SL}$	$0.157 + 0.007 \cdot \text{SL}$	$0.165 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.271	$0.244 + 0.013 \cdot \text{SL}$	$0.257 + 0.010 \cdot \text{SL}$	$0.280 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.094	$0.065 + 0.015 \cdot \text{SL}$	$0.068 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.142	$0.112 + 0.015 \cdot \text{SL}$	$0.116 + 0.014 \cdot \text{SL}$	$0.124 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.169 + 0.009 \cdot \text{SL}$	$0.176 + 0.007 \cdot \text{SL}$	$0.185 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.291	$0.264 + 0.013 \cdot \text{SL}$	$0.277 + 0.010 \cdot \text{SL}$	$0.300 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.100	$0.073 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.141	$0.111 + 0.015 \cdot \text{SL}$	$0.116 + 0.014 \cdot \text{SL}$	$0.123 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.200	$0.182 + 0.009 \cdot \text{SL}$	$0.189 + 0.008 \cdot \text{SL}$	$0.200 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.301	$0.274 + 0.013 \cdot \text{SL}$	$0.287 + 0.010 \cdot \text{SL}$	$0.310 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### OR3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$
	$t_F$	0.155	$0.139 + 0.008 \cdot \text{SL}$	$0.142 + 0.007 \cdot \text{SL}$	$0.150 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.186	$0.176 + 0.005 \cdot \text{SL}$	$0.181 + 0.004 \cdot \text{SL}$	$0.195 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.307	$0.292 + 0.008 \cdot \text{SL}$	$0.301 + 0.006 \cdot \text{SL}$	$0.329 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.092	$0.079 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.154	$0.137 + 0.008 \cdot \text{SL}$	$0.143 + 0.007 \cdot \text{SL}$	$0.150 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.205	$0.194 + 0.006 \cdot \text{SL}$	$0.200 + 0.004 \cdot \text{SL}$	$0.215 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.328	$0.312 + 0.008 \cdot \text{SL}$	$0.321 + 0.006 \cdot \text{SL}$	$0.350 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.099	$0.086 + 0.007 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$
	$t_F$	0.154	$0.136 + 0.009 \cdot \text{SL}$	$0.143 + 0.007 \cdot \text{SL}$	$0.150 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.218	$0.207 + 0.006 \cdot \text{SL}$	$0.214 + 0.004 \cdot \text{SL}$	$0.229 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.337	$0.321 + 0.008 \cdot \text{SL}$	$0.330 + 0.006 \cdot \text{SL}$	$0.359 + 0.004 \cdot \text{SL}$

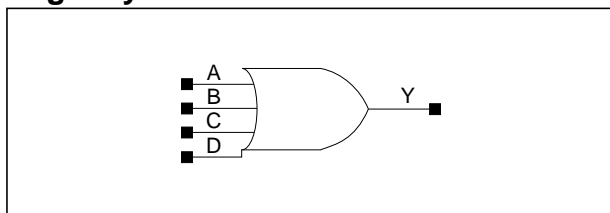
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## OR4DH/OR4/OR4D2/OR4D4

### 4-Input OR with 0.5X/1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

#### Cell Data

Input Load (SL)															
OR4DH				OR4				OR4D2				OR4D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.6	0.6	0.6	0.9	1.0	1.0	1.0	0.9	1.0	0.9	1.0	0.9	1.0	1.0	1.0
Gate Count															
OR4DH				OR4				OR4D2				OR4D4			
2.67				2.67				3.00				4.33			



# OR4DH/OR4/OR4D2/OR4D4

## 4-Input OR with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OR4DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.196	$0.066 + 0.065 \cdot \text{SL}$	$0.062 + 0.066 \cdot \text{SL}$	$0.057 + 0.067 \cdot \text{SL}$
	$t_F$	0.224	$0.094 + 0.065 \cdot \text{SL}$	$0.091 + 0.066 \cdot \text{SL}$	$0.083 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.121 + 0.029 \cdot \text{SL}$	$0.123 + 0.029 \cdot \text{SL}$	$0.123 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.253	$0.182 + 0.035 \cdot \text{SL}$	$0.193 + 0.033 \cdot \text{SL}$	$0.197 + 0.032 \cdot \text{SL}$
B to Y	$t_R$	0.198	$0.069 + 0.064 \cdot \text{SL}$	$0.063 + 0.066 \cdot \text{SL}$	$0.058 + 0.066 \cdot \text{SL}$
	$t_F$	0.225	$0.095 + 0.065 \cdot \text{SL}$	$0.092 + 0.066 \cdot \text{SL}$	$0.083 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.197	$0.138 + 0.029 \cdot \text{SL}$	$0.140 + 0.029 \cdot \text{SL}$	$0.141 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.254	$0.183 + 0.036 \cdot \text{SL}$	$0.194 + 0.033 \cdot \text{SL}$	$0.198 + 0.032 \cdot \text{SL}$
C to Y	$t_R$	0.213	$0.084 + 0.064 \cdot \text{SL}$	$0.078 + 0.066 \cdot \text{SL}$	$0.073 + 0.067 \cdot \text{SL}$
	$t_F$	0.217	$0.087 + 0.065 \cdot \text{SL}$	$0.081 + 0.066 \cdot \text{SL}$	$0.075 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.129 + 0.029 \cdot \text{SL}$	$0.130 + 0.029 \cdot \text{SL}$	$0.130 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.248	$0.179 + 0.035 \cdot \text{SL}$	$0.187 + 0.033 \cdot \text{SL}$	$0.190 + 0.032 \cdot \text{SL}$
D to Y	$t_R$	0.215	$0.087 + 0.064 \cdot \text{SL}$	$0.079 + 0.066 \cdot \text{SL}$	$0.074 + 0.066 \cdot \text{SL}$
	$t_F$	0.217	$0.086 + 0.065 \cdot \text{SL}$	$0.082 + 0.066 \cdot \text{SL}$	$0.076 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.205	$0.147 + 0.029 \cdot \text{SL}$	$0.148 + 0.029 \cdot \text{SL}$	$0.149 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.249	$0.180 + 0.035 \cdot \text{SL}$	$0.188 + 0.033 \cdot \text{SL}$	$0.191 + 0.032 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### OR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.119	$0.062 + 0.029 \cdot \text{SL}$	$0.058 + 0.030 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$
	$t_F$	0.143	$0.078 + 0.033 \cdot \text{SL}$	$0.079 + 0.032 \cdot \text{SL}$	$0.076 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.153	$0.125 + 0.014 \cdot \text{SL}$	$0.128 + 0.013 \cdot \text{SL}$	$0.129 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.186	$0.149 + 0.019 \cdot \text{SL}$	$0.156 + 0.017 \cdot \text{SL}$	$0.162 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.125	$0.071 + 0.027 \cdot \text{SL}$	$0.060 + 0.030 \cdot \text{SL}$	$0.056 + 0.030 \cdot \text{SL}$
	$t_F$	0.144	$0.079 + 0.032 \cdot \text{SL}$	$0.079 + 0.032 \cdot \text{SL}$	$0.076 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.175	$0.146 + 0.014 \cdot \text{SL}$	$0.150 + 0.013 \cdot \text{SL}$	$0.151 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.186	$0.149 + 0.019 \cdot \text{SL}$	$0.157 + 0.017 \cdot \text{SL}$	$0.162 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.135	$0.079 + 0.028 \cdot \text{SL}$	$0.073 + 0.030 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$
	$t_F$	0.138	$0.074 + 0.032 \cdot \text{SL}$	$0.072 + 0.033 \cdot \text{SL}$	$0.069 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.160	$0.133 + 0.014 \cdot \text{SL}$	$0.135 + 0.013 \cdot \text{SL}$	$0.135 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.184	$0.148 + 0.018 \cdot \text{SL}$	$0.153 + 0.017 \cdot \text{SL}$	$0.158 + 0.016 \cdot \text{SL}$
D to Y	$t_R$	0.139	$0.084 + 0.028 \cdot \text{SL}$	$0.076 + 0.030 \cdot \text{SL}$	$0.072 + 0.030 \cdot \text{SL}$
	$t_F$	0.139	$0.076 + 0.032 \cdot \text{SL}$	$0.073 + 0.033 \cdot \text{SL}$	$0.069 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.182	$0.154 + 0.014 \cdot \text{SL}$	$0.157 + 0.013 \cdot \text{SL}$	$0.158 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.185	$0.149 + 0.018 \cdot \text{SL}$	$0.154 + 0.017 \cdot \text{SL}$	$0.158 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**OR4DH/OR4/OR4D2/OR4D4****4-Input OR with 0.5X/1X/2X/4X Drive****Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**OR4D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.094	$0.066 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.117	$0.084 + 0.017 \cdot \text{SL}$	$0.086 + 0.016 \cdot \text{SL}$	$0.086 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.164	$0.148 + 0.008 \cdot \text{SL}$	$0.152 + 0.007 \cdot \text{SL}$	$0.157 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.199	$0.178 + 0.011 \cdot \text{SL}$	$0.184 + 0.009 \cdot \text{SL}$	$0.196 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.099	$0.071 + 0.014 \cdot \text{SL}$	$0.069 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.119	$0.085 + 0.017 \cdot \text{SL}$	$0.088 + 0.016 \cdot \text{SL}$	$0.086 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.183	$0.166 + 0.008 \cdot \text{SL}$	$0.171 + 0.007 \cdot \text{SL}$	$0.177 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.198	$0.177 + 0.011 \cdot \text{SL}$	$0.183 + 0.009 \cdot \text{SL}$	$0.196 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.114	$0.087 + 0.013 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$	$0.074 + 0.015 \cdot \text{SL}$
	$t_F$	0.115	$0.084 + 0.015 \cdot \text{SL}$	$0.082 + 0.016 \cdot \text{SL}$	$0.079 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.176	$0.161 + 0.008 \cdot \text{SL}$	$0.164 + 0.007 \cdot \text{SL}$	$0.168 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.203	$0.182 + 0.010 \cdot \text{SL}$	$0.188 + 0.009 \cdot \text{SL}$	$0.196 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.119	$0.091 + 0.014 \cdot \text{SL}$	$0.089 + 0.014 \cdot \text{SL}$	$0.077 + 0.015 \cdot \text{SL}$
	$t_F$	0.116	$0.083 + 0.016 \cdot \text{SL}$	$0.084 + 0.016 \cdot \text{SL}$	$0.079 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.196	$0.180 + 0.008 \cdot \text{SL}$	$0.184 + 0.007 \cdot \text{SL}$	$0.188 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.203	$0.182 + 0.010 \cdot \text{SL}$	$0.187 + 0.009 \cdot \text{SL}$	$0.196 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$ **OR4D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.074	$0.059 + 0.008 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$	$0.052 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.054 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.294	$0.284 + 0.005 \cdot \text{SL}$	$0.288 + 0.004 \cdot \text{SL}$	$0.298 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.289 + 0.006 \cdot \text{SL}$	$0.294 + 0.004 \cdot \text{SL}$	$0.309 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.074	$0.060 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$	$0.052 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.054 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.315	$0.305 + 0.005 \cdot \text{SL}$	$0.309 + 0.004 \cdot \text{SL}$	$0.320 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.289 + 0.006 \cdot \text{SL}$	$0.294 + 0.004 \cdot \text{SL}$	$0.309 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.074	$0.059 + 0.008 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$	$0.052 + 0.008 \cdot \text{SL}$
	$t_F$	0.070	$0.055 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.300	$0.290 + 0.005 \cdot \text{SL}$	$0.295 + 0.004 \cdot \text{SL}$	$0.305 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.290	$0.278 + 0.006 \cdot \text{SL}$	$0.284 + 0.004 \cdot \text{SL}$	$0.298 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.075	$0.060 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$	$0.053 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.056 + 0.007 \cdot \text{SL}$	$0.056 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.323	$0.313 + 0.005 \cdot \text{SL}$	$0.318 + 0.004 \cdot \text{SL}$	$0.328 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.290	$0.279 + 0.006 \cdot \text{SL}$	$0.284 + 0.004 \cdot \text{SL}$	$0.299 + 0.004 \cdot \text{SL}$

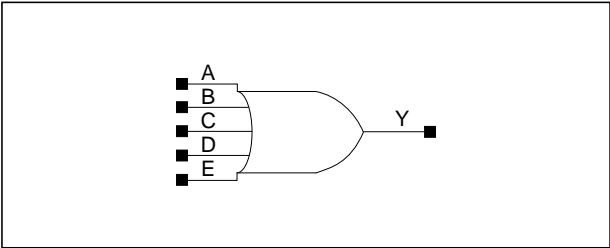
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OR5/OR5D2/OR5D4

5-Input OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Cell Data

Input Load (SL)															Gate Count		
OR5					OR5D2					OR5D4					OR5	OR5D2	OR5D4
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E			
0.9	0.9	0.9	1.0	1.0	0.8	0.9	0.9	0.9	1.0	0.9	0.9	1.0	1.0	1.1	3.00	3.33	4.67



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## OR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.124	$0.066 + 0.029 \cdot \text{SL}$	$0.064 + 0.029 \cdot \text{SL}$	$0.058 + 0.030 \cdot \text{SL}$
	$t_F$	0.163	$0.096 + 0.034 \cdot \text{SL}$	$0.101 + 0.032 \cdot \text{SL}$	$0.101 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.149 + 0.015 \cdot \text{SL}$	$0.154 + 0.013 \cdot \text{SL}$	$0.156 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.227	$0.186 + 0.020 \cdot \text{SL}$	$0.196 + 0.018 \cdot \text{SL}$	$0.208 + 0.017 \cdot \text{SL}$
B to Y	$t_R$	0.129	$0.072 + 0.028 \cdot \text{SL}$	$0.069 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.166	$0.100 + 0.033 \cdot \text{SL}$	$0.104 + 0.032 \cdot \text{SL}$	$0.103 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.204	$0.174 + 0.015 \cdot \text{SL}$	$0.180 + 0.014 \cdot \text{SL}$	$0.183 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.246	$0.205 + 0.020 \cdot \text{SL}$	$0.215 + 0.018 \cdot \text{SL}$	$0.227 + 0.017 \cdot \text{SL}$
C to Y	$t_R$	0.137	$0.082 + 0.028 \cdot \text{SL}$	$0.076 + 0.029 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.166	$0.101 + 0.033 \cdot \text{SL}$	$0.102 + 0.032 \cdot \text{SL}$	$0.103 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.221	$0.190 + 0.015 \cdot \text{SL}$	$0.197 + 0.014 \cdot \text{SL}$	$0.201 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.255	$0.214 + 0.020 \cdot \text{SL}$	$0.224 + 0.018 \cdot \text{SL}$	$0.235 + 0.017 \cdot \text{SL}$
D to Y	$t_R$	0.135	$0.079 + 0.028 \cdot \text{SL}$	$0.073 + 0.030 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$
	$t_F$	0.139	$0.074 + 0.032 \cdot \text{SL}$	$0.072 + 0.033 \cdot \text{SL}$	$0.070 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.160	$0.133 + 0.014 \cdot \text{SL}$	$0.135 + 0.013 \cdot \text{SL}$	$0.136 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.185	$0.149 + 0.018 \cdot \text{SL}$	$0.154 + 0.017 \cdot \text{SL}$	$0.159 + 0.016 \cdot \text{SL}$
E to Y	$t_R$	0.138	$0.080 + 0.029 \cdot \text{SL}$	$0.077 + 0.030 \cdot \text{SL}$	$0.072 + 0.030 \cdot \text{SL}$
	$t_F$	0.140	$0.076 + 0.032 \cdot \text{SL}$	$0.073 + 0.033 \cdot \text{SL}$	$0.071 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.183	$0.155 + 0.014 \cdot \text{SL}$	$0.157 + 0.013 \cdot \text{SL}$	$0.158 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.185	$0.149 + 0.018 \cdot \text{SL}$	$0.155 + 0.017 \cdot \text{SL}$	$0.159 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## OR5/OR5D2/OR5D4

### 5-Input OR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.104	$0.076 + 0.014 \cdot \text{SL}$	$0.075 + 0.014 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$
	$t_F$	0.149	$0.117 + 0.016 \cdot \text{SL}$	$0.116 + 0.016 \cdot \text{SL}$	$0.118 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.177 + 0.009 \cdot \text{SL}$	$0.182 + 0.007 \cdot \text{SL}$	$0.190 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.248	$0.224 + 0.012 \cdot \text{SL}$	$0.233 + 0.010 \cdot \text{SL}$	$0.250 + 0.009 \cdot \text{SL}$
B to Y	$t_R$	0.111	$0.083 + 0.014 \cdot \text{SL}$	$0.083 + 0.014 \cdot \text{SL}$	$0.072 + 0.015 \cdot \text{SL}$
	$t_F$	0.149	$0.117 + 0.016 \cdot \text{SL}$	$0.117 + 0.016 \cdot \text{SL}$	$0.119 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.201 + 0.009 \cdot \text{SL}$	$0.207 + 0.007 \cdot \text{SL}$	$0.216 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.268	$0.244 + 0.012 \cdot \text{SL}$	$0.252 + 0.010 \cdot \text{SL}$	$0.270 + 0.009 \cdot \text{SL}$
C to Y	$t_R$	0.119	$0.092 + 0.014 \cdot \text{SL}$	$0.089 + 0.014 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$
	$t_F$	0.149	$0.117 + 0.016 \cdot \text{SL}$	$0.116 + 0.016 \cdot \text{SL}$	$0.119 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.236	$0.218 + 0.009 \cdot \text{SL}$	$0.224 + 0.008 \cdot \text{SL}$	$0.234 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.252 + 0.012 \cdot \text{SL}$	$0.261 + 0.010 \cdot \text{SL}$	$0.279 + 0.009 \cdot \text{SL}$
D to Y	$t_R$	0.113	$0.087 + 0.013 \cdot \text{SL}$	$0.082 + 0.014 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$
	$t_F$	0.115	$0.084 + 0.016 \cdot \text{SL}$	$0.082 + 0.016 \cdot \text{SL}$	$0.079 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.177	$0.161 + 0.008 \cdot \text{SL}$	$0.165 + 0.007 \cdot \text{SL}$	$0.168 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.202	$0.182 + 0.010 \cdot \text{SL}$	$0.187 + 0.009 \cdot \text{SL}$	$0.195 + 0.008 \cdot \text{SL}$
E to Y	$t_R$	0.119	$0.091 + 0.014 \cdot \text{SL}$	$0.090 + 0.014 \cdot \text{SL}$	$0.079 + 0.015 \cdot \text{SL}$
	$t_F$	0.116	$0.084 + 0.016 \cdot \text{SL}$	$0.083 + 0.016 \cdot \text{SL}$	$0.080 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.197	$0.181 + 0.008 \cdot \text{SL}$	$0.184 + 0.007 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.202	$0.181 + 0.010 \cdot \text{SL}$	$0.186 + 0.009 \cdot \text{SL}$	$0.195 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**OR5D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.076	$0.061 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$	$0.053 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.057 + 0.006 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.313	$0.303 + 0.005 \cdot \text{SL}$	$0.308 + 0.004 \cdot \text{SL}$	$0.318 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.339	$0.327 + 0.006 \cdot \text{SL}$	$0.333 + 0.004 \cdot \text{SL}$	$0.347 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.075	$0.059 + 0.008 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$	$0.053 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.054 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.325 + 0.005 \cdot \text{SL}$	$0.330 + 0.004 \cdot \text{SL}$	$0.341 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.356	$0.344 + 0.006 \cdot \text{SL}$	$0.350 + 0.004 \cdot \text{SL}$	$0.364 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.075	$0.060 + 0.008 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$	$0.053 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.054 + 0.007 \cdot \text{SL}$	$0.056 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.349	$0.339 + 0.005 \cdot \text{SL}$	$0.343 + 0.004 \cdot \text{SL}$	$0.354 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.364	$0.352 + 0.006 \cdot \text{SL}$	$0.358 + 0.004 \cdot \text{SL}$	$0.372 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.075	$0.060 + 0.008 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.053 + 0.008 \cdot \text{SL}$
	$t_F$	0.068	$0.053 + 0.008 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$	$0.053 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.301	$0.291 + 0.005 \cdot \text{SL}$	$0.295 + 0.004 \cdot \text{SL}$	$0.306 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.277 + 0.006 \cdot \text{SL}$	$0.283 + 0.004 \cdot \text{SL}$	$0.297 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.076	$0.061 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$	$0.054 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.056 + 0.006 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.321	$0.311 + 0.005 \cdot \text{SL}$	$0.316 + 0.004 \cdot \text{SL}$	$0.326 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.288	$0.276 + 0.006 \cdot \text{SL}$	$0.282 + 0.004 \cdot \text{SL}$	$0.296 + 0.004 \cdot \text{SL}$

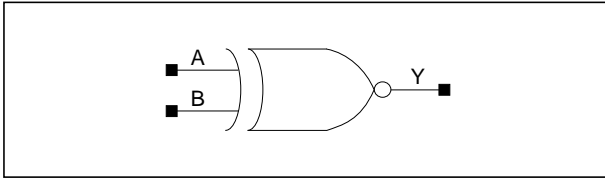
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## XN2/XN2D2/XN2D4

### 2-Input Exclusive-NOR with 1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

#### Cell Data

Input Load (SL)						Gate Count		
XN2		XN2D2		XN2D4		XN2	XN2D2	XN2D4
A	B	A	B	A	B			
0.8	1.5	0.8	1.5	0.8	1.5	2.33	2.67	3.00

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### XN2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.131	$0.074 + 0.029 \cdot \text{SL}$	$0.074 + 0.029 \cdot \text{SL}$	$0.067 + 0.030 \cdot \text{SL}$
	$t_F$	0.136	$0.083 + 0.026 \cdot \text{SL}$	$0.087 + 0.025 \cdot \text{SL}$	$0.087 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.257	$0.225 + 0.016 \cdot \text{SL}$	$0.233 + 0.014 \cdot \text{SL}$	$0.239 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.241 + 0.018 \cdot \text{SL}$	$0.252 + 0.015 \cdot \text{SL}$	$0.263 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.128	$0.070 + 0.029 \cdot \text{SL}$	$0.068 + 0.029 \cdot \text{SL}$	$0.064 + 0.030 \cdot \text{SL}$
	$t_F$	0.128	$0.074 + 0.027 \cdot \text{SL}$	$0.081 + 0.025 \cdot \text{SL}$	$0.082 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.233	$0.201 + 0.016 \cdot \text{SL}$	$0.210 + 0.014 \cdot \text{SL}$	$0.215 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.219	$0.180 + 0.019 \cdot \text{SL}$	$0.193 + 0.016 \cdot \text{SL}$	$0.206 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**XN2/XN2D2/XN2D4****2-Input Exclusive-NOR with 1X/2X/4X Drive****Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**XN2D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.110	$0.081 + 0.015 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$	$0.079 + 0.015 \cdot \text{SL}$
	$t_F$	0.122	$0.091 + 0.015 \cdot \text{SL}$	$0.099 + 0.014 \cdot \text{SL}$	$0.106 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.268	$0.247 + 0.010 \cdot \text{SL}$	$0.256 + 0.008 \cdot \text{SL}$	$0.270 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.295	$0.270 + 0.012 \cdot \text{SL}$	$0.282 + 0.009 \cdot \text{SL}$	$0.303 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.107	$0.077 + 0.015 \cdot \text{SL}$	$0.079 + 0.015 \cdot \text{SL}$	$0.077 + 0.015 \cdot \text{SL}$
	$t_F$	0.118	$0.088 + 0.015 \cdot \text{SL}$	$0.094 + 0.014 \cdot \text{SL}$	$0.100 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.243	$0.223 + 0.010 \cdot \text{SL}$	$0.232 + 0.008 \cdot \text{SL}$	$0.246 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.227	$0.201 + 0.013 \cdot \text{SL}$	$0.214 + 0.010 \cdot \text{SL}$	$0.237 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$ **XN2D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.134	$0.120 + 0.007 \cdot \text{SL}$	$0.119 + 0.007 \cdot \text{SL}$	$0.120 + 0.007 \cdot \text{SL}$
	$t_F$	0.155	$0.139 + 0.008 \cdot \text{SL}$	$0.144 + 0.007 \cdot \text{SL}$	$0.157 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.327	$0.313 + 0.007 \cdot \text{SL}$	$0.322 + 0.005 \cdot \text{SL}$	$0.343 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.368	$0.353 + 0.008 \cdot \text{SL}$	$0.362 + 0.005 \cdot \text{SL}$	$0.390 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.133	$0.119 + 0.007 \cdot \text{SL}$	$0.118 + 0.007 \cdot \text{SL}$	$0.119 + 0.007 \cdot \text{SL}$
	$t_F$	0.154	$0.138 + 0.008 \cdot \text{SL}$	$0.142 + 0.007 \cdot \text{SL}$	$0.155 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.298	$0.285 + 0.007 \cdot \text{SL}$	$0.293 + 0.005 \cdot \text{SL}$	$0.315 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.288	$0.271 + 0.008 \cdot \text{SL}$	$0.281 + 0.006 \cdot \text{SL}$	$0.313 + 0.004 \cdot \text{SL}$

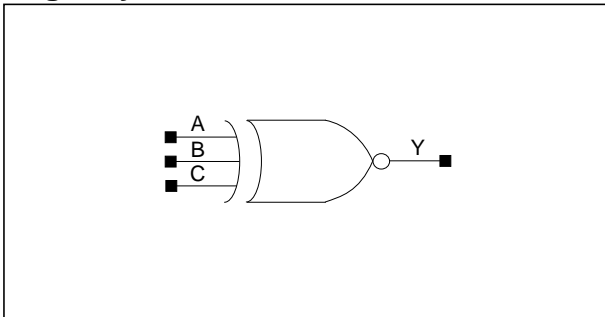
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## XN3/XN3D2/XN3D4

### 3-Input Exclusive-NOR with 1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

#### Cell Data

Input Load (SL)									Gate Count		
XN3			XN3D2			XN3D4			XN3	XN3D2	XN3D4
A	B	C	A	B	C	A	B	C			
1.4	0.8	1.5	1.4	0.8	1.5	1.3	0.8	1.5	4.00	4.33	4.67

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### XN3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.154	$0.091 + 0.031 \cdot \text{SL}$	$0.097 + 0.030 \cdot \text{SL}$	$0.101 + 0.029 \cdot \text{SL}$
	$t_F$	0.145	$0.086 + 0.029 \cdot \text{SL}$	$0.095 + 0.027 \cdot \text{SL}$	$0.105 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.236	$0.197 + 0.019 \cdot \text{SL}$	$0.209 + 0.016 \cdot \text{SL}$	$0.224 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.243	$0.207 + 0.018 \cdot \text{SL}$	$0.218 + 0.016 \cdot \text{SL}$	$0.229 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.175	$0.115 + 0.030 \cdot \text{SL}$	$0.120 + 0.029 \cdot \text{SL}$	$0.118 + 0.029 \cdot \text{SL}$
	$t_F$	0.202	$0.143 + 0.029 \cdot \text{SL}$	$0.155 + 0.026 \cdot \text{SL}$	$0.164 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.412	$0.380 + 0.016 \cdot \text{SL}$	$0.389 + 0.014 \cdot \text{SL}$	$0.395 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.428	$0.381 + 0.023 \cdot \text{SL}$	$0.400 + 0.019 \cdot \text{SL}$	$0.422 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.173	$0.114 + 0.030 \cdot \text{SL}$	$0.117 + 0.029 \cdot \text{SL}$	$0.118 + 0.029 \cdot \text{SL}$
	$t_F$	0.129	$0.079 + 0.025 \cdot \text{SL}$	$0.081 + 0.025 \cdot \text{SL}$	$0.078 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.361	$0.323 + 0.019 \cdot \text{SL}$	$0.336 + 0.016 \cdot \text{SL}$	$0.350 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.398	$0.361 + 0.018 \cdot \text{SL}$	$0.373 + 0.016 \cdot \text{SL}$	$0.384 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**XN3D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.146	$0.116 + 0.015 \cdot \text{SL}$	$0.116 + 0.015 \cdot \text{SL}$	$0.124 + 0.015 \cdot \text{SL}$
	$t_F$	0.142	$0.108 + 0.017 \cdot \text{SL}$	$0.119 + 0.014 \cdot \text{SL}$	$0.136 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.252	$0.226 + 0.013 \cdot \text{SL}$	$0.240 + 0.010 \cdot \text{SL}$	$0.263 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.237 + 0.012 \cdot \text{SL}$	$0.249 + 0.009 \cdot \text{SL}$	$0.269 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.163	$0.133 + 0.015 \cdot \text{SL}$	$0.134 + 0.015 \cdot \text{SL}$	$0.138 + 0.014 \cdot \text{SL}$
	$t_F$	0.198	$0.164 + 0.017 \cdot \text{SL}$	$0.178 + 0.014 \cdot \text{SL}$	$0.191 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.427	$0.407 + 0.010 \cdot \text{SL}$	$0.416 + 0.008 \cdot \text{SL}$	$0.430 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.451	$0.421 + 0.015 \cdot \text{SL}$	$0.437 + 0.011 \cdot \text{SL}$	$0.470 + 0.009 \cdot \text{SL}$
C to Y	$t_R$	0.162	$0.132 + 0.015 \cdot \text{SL}$	$0.133 + 0.015 \cdot \text{SL}$	$0.137 + 0.014 \cdot \text{SL}$
	$t_F$	0.119	$0.093 + 0.013 \cdot \text{SL}$	$0.094 + 0.013 \cdot \text{SL}$	$0.096 + 0.012 \cdot \text{SL}$
	$t_{PLH}$	0.380	$0.355 + 0.013 \cdot \text{SL}$	$0.369 + 0.009 \cdot \text{SL}$	$0.390 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.418	$0.394 + 0.012 \cdot \text{SL}$	$0.406 + 0.009 \cdot \text{SL}$	$0.426 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

**XN3D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.194	$0.180 + 0.007 \cdot \text{SL}$	$0.178 + 0.007 \cdot \text{SL}$	$0.178 + 0.007 \cdot \text{SL}$
	$t_F$	0.226	$0.208 + 0.009 \cdot \text{SL}$	$0.211 + 0.008 \cdot \text{SL}$	$0.238 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.322	$0.304 + 0.009 \cdot \text{SL}$	$0.315 + 0.006 \cdot \text{SL}$	$0.351 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.332	$0.312 + 0.010 \cdot \text{SL}$	$0.323 + 0.007 \cdot \text{SL}$	$0.368 + 0.005 \cdot \text{SL}$
B to Y	$t_R$	0.128	$0.114 + 0.007 \cdot \text{SL}$	$0.112 + 0.007 \cdot \text{SL}$	$0.111 + 0.007 \cdot \text{SL}$
	$t_F$	0.229	$0.212 + 0.008 \cdot \text{SL}$	$0.216 + 0.007 \cdot \text{SL}$	$0.235 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.480	$0.467 + 0.007 \cdot \text{SL}$	$0.475 + 0.005 \cdot \text{SL}$	$0.497 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.536	$0.517 + 0.010 \cdot \text{SL}$	$0.528 + 0.007 \cdot \text{SL}$	$0.569 + 0.005 \cdot \text{SL}$
C to Y	$t_R$	0.179	$0.165 + 0.007 \cdot \text{SL}$	$0.164 + 0.007 \cdot \text{SL}$	$0.165 + 0.007 \cdot \text{SL}$
	$t_F$	0.146	$0.131 + 0.008 \cdot \text{SL}$	$0.134 + 0.007 \cdot \text{SL}$	$0.142 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.446	$0.429 + 0.008 \cdot \text{SL}$	$0.440 + 0.006 \cdot \text{SL}$	$0.471 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.486	$0.471 + 0.008 \cdot \text{SL}$	$0.480 + 0.005 \cdot \text{SL}$	$0.508 + 0.004 \cdot \text{SL}$

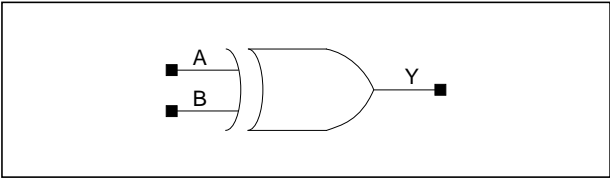
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



**XO2/XO2D2/XO2D4**

**2-Input Exclusive-OR with 1X/2X/4X Drive**

**Logic Symbol**



**Truth Table**

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

**Cell Data**

Input Load (SL)						Gate Count		
XO2		XO2D2		XO2D4		XO2	XO2D2	XO2D4
A	B	A	B	A	B	2.33	2.67	3.00
0.8	1.3	0.8	1.3	0.8	1.3			



**XO2/XO2D2/XO2D4****2-Input Exclusive-OR with 1X/2X/4X Drive****Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**XO2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.137	$0.079 + 0.029 \cdot \text{SL}$	$0.077 + 0.029 \cdot \text{SL}$	$0.072 + 0.030 \cdot \text{SL}$
	$t_F$	0.142	$0.085 + 0.028 \cdot \text{SL}$	$0.093 + 0.026 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.264	$0.231 + 0.017 \cdot \text{SL}$	$0.239 + 0.014 \cdot \text{SL}$	$0.246 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.292	$0.254 + 0.019 \cdot \text{SL}$	$0.266 + 0.016 \cdot \text{SL}$	$0.277 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.134	$0.076 + 0.029 \cdot \text{SL}$	$0.075 + 0.030 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.134	$0.078 + 0.028 \cdot \text{SL}$	$0.085 + 0.027 \cdot \text{SL}$	$0.084 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.216	$0.182 + 0.017 \cdot \text{SL}$	$0.192 + 0.015 \cdot \text{SL}$	$0.199 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.255	$0.216 + 0.019 \cdot \text{SL}$	$0.228 + 0.016 \cdot \text{SL}$	$0.240 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ **XO2D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.114	$0.084 + 0.015 \cdot \text{SL}$	$0.086 + 0.015 \cdot \text{SL}$	$0.082 + 0.015 \cdot \text{SL}$
	$t_F$	0.127	$0.098 + 0.015 \cdot \text{SL}$	$0.102 + 0.014 \cdot \text{SL}$	$0.108 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.273	$0.253 + 0.010 \cdot \text{SL}$	$0.262 + 0.008 \cdot \text{SL}$	$0.276 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.304	$0.280 + 0.012 \cdot \text{SL}$	$0.291 + 0.009 \cdot \text{SL}$	$0.312 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.113	$0.084 + 0.015 \cdot \text{SL}$	$0.083 + 0.015 \cdot \text{SL}$	$0.083 + 0.015 \cdot \text{SL}$
	$t_F$	0.120	$0.090 + 0.015 \cdot \text{SL}$	$0.094 + 0.014 \cdot \text{SL}$	$0.104 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.222	$0.200 + 0.011 \cdot \text{SL}$	$0.210 + 0.008 \cdot \text{SL}$	$0.226 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.267	$0.243 + 0.012 \cdot \text{SL}$	$0.254 + 0.009 \cdot \text{SL}$	$0.275 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$ **XO2D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.135	$0.122 + 0.007 \cdot \text{SL}$	$0.120 + 0.007 \cdot \text{SL}$	$0.121 + 0.007 \cdot \text{SL}$
	$t_F$	0.155	$0.139 + 0.008 \cdot \text{SL}$	$0.143 + 0.007 \cdot \text{SL}$	$0.156 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.326	$0.313 + 0.007 \cdot \text{SL}$	$0.321 + 0.005 \cdot \text{SL}$	$0.343 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.371	$0.356 + 0.008 \cdot \text{SL}$	$0.365 + 0.005 \cdot \text{SL}$	$0.394 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.134	$0.120 + 0.007 \cdot \text{SL}$	$0.119 + 0.007 \cdot \text{SL}$	$0.120 + 0.007 \cdot \text{SL}$
	$t_F$	0.152	$0.134 + 0.009 \cdot \text{SL}$	$0.141 + 0.007 \cdot \text{SL}$	$0.152 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.266	$0.252 + 0.007 \cdot \text{SL}$	$0.261 + 0.005 \cdot \text{SL}$	$0.286 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.333	$0.318 + 0.008 \cdot \text{SL}$	$0.327 + 0.005 \cdot \text{SL}$	$0.355 + 0.004 \cdot \text{SL}$

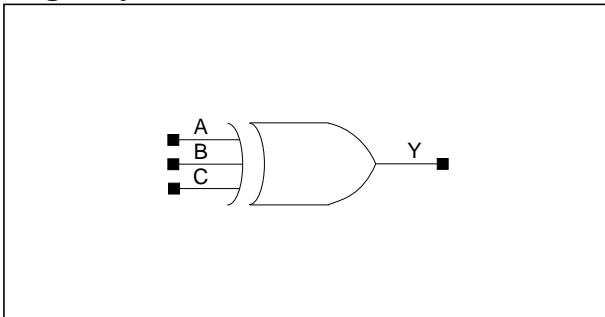
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## XO3/XO3D2/XO3D4

### 3-Input Exclusive-OR with 1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

#### Cell Data

Input Load (SL)									Gate Count		
XO3			XO3D2			XO3D4			XO3	XO3D2	XO3D4
A	B	C	A	B	C	A	B	C			
1.4	0.8	1.5	1.4	0.8	1.5	1.4	0.8	1.5	4.00	4.33	4.67

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### XO3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.140	$0.079 + 0.031 \cdot \text{SL}$	$0.084 + 0.030 \cdot \text{SL}$	$0.084 + 0.030 \cdot \text{SL}$
	$t_F$	0.164	$0.102 + 0.031 \cdot \text{SL}$	$0.114 + 0.028 \cdot \text{SL}$	$0.129 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.228	$0.196 + 0.016 \cdot \text{SL}$	$0.205 + 0.014 \cdot \text{SL}$	$0.210 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.245	$0.198 + 0.024 \cdot \text{SL}$	$0.216 + 0.019 \cdot \text{SL}$	$0.238 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.175	$0.115 + 0.030 \cdot \text{SL}$	$0.120 + 0.029 \cdot \text{SL}$	$0.118 + 0.029 \cdot \text{SL}$
	$t_F$	0.201	$0.143 + 0.029 \cdot \text{SL}$	$0.155 + 0.026 \cdot \text{SL}$	$0.164 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.412	$0.380 + 0.016 \cdot \text{SL}$	$0.388 + 0.014 \cdot \text{SL}$	$0.395 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.428	$0.381 + 0.023 \cdot \text{SL}$	$0.400 + 0.019 \cdot \text{SL}$	$0.422 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.173	$0.114 + 0.030 \cdot \text{SL}$	$0.117 + 0.029 \cdot \text{SL}$	$0.118 + 0.029 \cdot \text{SL}$
	$t_F$	0.129	$0.078 + 0.025 \cdot \text{SL}$	$0.081 + 0.025 \cdot \text{SL}$	$0.078 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.359	$0.321 + 0.019 \cdot \text{SL}$	$0.334 + 0.016 \cdot \text{SL}$	$0.348 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.396	$0.360 + 0.018 \cdot \text{SL}$	$0.371 + 0.016 \cdot \text{SL}$	$0.382 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# XO3/XO3D2/XO3D4

## 3-Input Exclusive-OR with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### XO3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.129	$0.097 + 0.016 \cdot \text{SL}$	$0.100 + 0.015 \cdot \text{SL}$	$0.104 + 0.015 \cdot \text{SL}$
	$t_F$	0.167	$0.131 + 0.018 \cdot \text{SL}$	$0.146 + 0.015 \cdot \text{SL}$	$0.163 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.241	$0.221 + 0.010 \cdot \text{SL}$	$0.230 + 0.008 \cdot \text{SL}$	$0.243 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.264	$0.233 + 0.016 \cdot \text{SL}$	$0.249 + 0.012 \cdot \text{SL}$	$0.284 + 0.009 \cdot \text{SL}$
B to Y	$t_R$	0.163	$0.133 + 0.015 \cdot \text{SL}$	$0.134 + 0.015 \cdot \text{SL}$	$0.138 + 0.014 \cdot \text{SL}$
	$t_F$	0.198	$0.164 + 0.017 \cdot \text{SL}$	$0.178 + 0.014 \cdot \text{SL}$	$0.191 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.428	$0.407 + 0.010 \cdot \text{SL}$	$0.416 + 0.008 \cdot \text{SL}$	$0.430 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.452	$0.422 + 0.015 \cdot \text{SL}$	$0.438 + 0.011 \cdot \text{SL}$	$0.470 + 0.009 \cdot \text{SL}$
C to Y	$t_R$	0.162	$0.132 + 0.015 \cdot \text{SL}$	$0.133 + 0.015 \cdot \text{SL}$	$0.137 + 0.014 \cdot \text{SL}$
	$t_F$	0.119	$0.093 + 0.013 \cdot \text{SL}$	$0.094 + 0.013 \cdot \text{SL}$	$0.097 + 0.012 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.353 + 0.013 \cdot \text{SL}$	$0.367 + 0.009 \cdot \text{SL}$	$0.388 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.417	$0.393 + 0.012 \cdot \text{SL}$	$0.405 + 0.009 \cdot \text{SL}$	$0.425 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### XO3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.167	$0.152 + 0.007 \cdot \text{SL}$	$0.151 + 0.008 \cdot \text{SL}$	$0.154 + 0.007 \cdot \text{SL}$
	$t_F$	0.233	$0.215 + 0.009 \cdot \text{SL}$	$0.220 + 0.008 \cdot \text{SL}$	$0.244 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.292	$0.279 + 0.007 \cdot \text{SL}$	$0.287 + 0.005 \cdot \text{SL}$	$0.308 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.346	$0.326 + 0.010 \cdot \text{SL}$	$0.337 + 0.007 \cdot \text{SL}$	$0.382 + 0.005 \cdot \text{SL}$
B to Y	$t_R$	0.127	$0.114 + 0.007 \cdot \text{SL}$	$0.112 + 0.007 \cdot \text{SL}$	$0.110 + 0.007 \cdot \text{SL}$
	$t_F$	0.229	$0.212 + 0.008 \cdot \text{SL}$	$0.216 + 0.007 \cdot \text{SL}$	$0.235 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.479	$0.466 + 0.007 \cdot \text{SL}$	$0.474 + 0.005 \cdot \text{SL}$	$0.496 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.536	$0.517 + 0.010 \cdot \text{SL}$	$0.528 + 0.007 \cdot \text{SL}$	$0.569 + 0.005 \cdot \text{SL}$
C to Y	$t_R$	0.179	$0.165 + 0.007 \cdot \text{SL}$	$0.164 + 0.007 \cdot \text{SL}$	$0.164 + 0.007 \cdot \text{SL}$
	$t_F$	0.147	$0.132 + 0.008 \cdot \text{SL}$	$0.136 + 0.007 \cdot \text{SL}$	$0.143 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.443	$0.426 + 0.008 \cdot \text{SL}$	$0.437 + 0.006 \cdot \text{SL}$	$0.468 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.488	$0.472 + 0.008 \cdot \text{SL}$	$0.481 + 0.005 \cdot \text{SL}$	$0.510 + 0.004 \cdot \text{SL}$

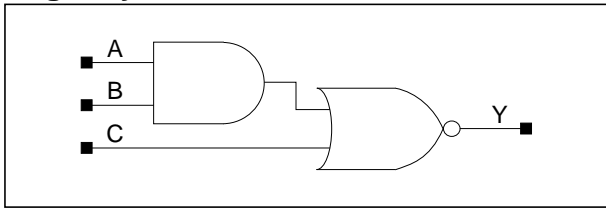
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# AO21DH/AO21/AO21D2/AO21D2B/AO21D4

## 2-AND into 2-NOR with 0.5X/1X/2X/2X(Bufferd)/4X Drive

### Logic Symbol



### Truth Table

A	B	C	Y
0	x	0	1
x	0	0	1
Other States			0

### Cell Data

Input Load (SL)														
AO21DH			AO21			AO21D2			AO21D2B			AO21D4		
A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
0.5	0.5	0.5	0.9	0.9	0.9	1.9	1.8	2.0	0.9	0.9	1.0	0.9	1.0	1.0
Gate Count														
AO21DH			AO21			AO21D2			AO21D2B			AO21D4		
1.33			1.33			2.33			2.33			3.00		

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO21DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.379	$0.143 + 0.118 \cdot \text{SL}$	$0.125 + 0.122 \cdot \text{SL}$	$0.115 + 0.124 \cdot \text{SL}$
	$t_F$	0.254	$0.101 + 0.077 \cdot \text{SL}$	$0.083 + 0.081 \cdot \text{SL}$	$0.067 + 0.083 \cdot \text{SL}$
	$t_{PLH}$	0.190	$0.085 + 0.052 \cdot \text{SL}$	$0.083 + 0.053 \cdot \text{SL}$	$0.082 + 0.053 \cdot \text{SL}$
	$t_{PHL}$	0.155	$0.076 + 0.040 \cdot \text{SL}$	$0.076 + 0.040 \cdot \text{SL}$	$0.076 + 0.040 \cdot \text{SL}$
B to Y	$t_R$	0.404	$0.167 + 0.118 \cdot \text{SL}$	$0.149 + 0.123 \cdot \text{SL}$	$0.140 + 0.124 \cdot \text{SL}$
	$t_F$	0.249	$0.092 + 0.078 \cdot \text{SL}$	$0.077 + 0.082 \cdot \text{SL}$	$0.068 + 0.083 \cdot \text{SL}$
	$t_{PLH}$	0.205	$0.100 + 0.052 \cdot \text{SL}$	$0.098 + 0.053 \cdot \text{SL}$	$0.096 + 0.053 \cdot \text{SL}$
	$t_{PHL}$	0.148	$0.068 + 0.040 \cdot \text{SL}$	$0.070 + 0.040 \cdot \text{SL}$	$0.070 + 0.040 \cdot \text{SL}$
C to Y	$t_R$	0.399	$0.157 + 0.121 \cdot \text{SL}$	$0.148 + 0.123 \cdot \text{SL}$	$0.142 + 0.124 \cdot \text{SL}$
	$t_F$	0.215	$0.122 + 0.047 \cdot \text{SL}$	$0.108 + 0.050 \cdot \text{SL}$	$0.090 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.225	$0.119 + 0.053 \cdot \text{SL}$	$0.119 + 0.053 \cdot \text{SL}$	$0.119 + 0.053 \cdot \text{SL}$
	$t_{PHL}$	0.151	$0.095 + 0.028 \cdot \text{SL}$	$0.097 + 0.027 \cdot \text{SL}$	$0.097 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO21DH/AO21/AO21D2/AO21D2B/AO21D4

## 2-AND into 2-NOR with 0.5X/1X/2X/2X(Bufferd)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.246	$0.136 + 0.055 \cdot \text{SL}$	$0.122 + 0.059 \cdot \text{SL}$	$0.108 + 0.060 \cdot \text{SL}$
	$t_F$	0.196	$0.102 + 0.047 \cdot \text{SL}$	$0.089 + 0.050 \cdot \text{SL}$	$0.076 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.124	$0.071 + 0.027 \cdot \text{SL}$	$0.074 + 0.026 \cdot \text{SL}$	$0.073 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.128	$0.076 + 0.026 \cdot \text{SL}$	$0.079 + 0.025 \cdot \text{SL}$	$0.079 + 0.025 \cdot \text{SL}$
B to Y	$t_R$	0.266	$0.155 + 0.056 \cdot \text{SL}$	$0.142 + 0.059 \cdot \text{SL}$	$0.127 + 0.061 \cdot \text{SL}$
	$t_F$	0.190	$0.094 + 0.048 \cdot \text{SL}$	$0.083 + 0.051 \cdot \text{SL}$	$0.073 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.137	$0.085 + 0.026 \cdot \text{SL}$	$0.085 + 0.026 \cdot \text{SL}$	$0.084 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.120	$0.069 + 0.026 \cdot \text{SL}$	$0.072 + 0.025 \cdot \text{SL}$	$0.072 + 0.025 \cdot \text{SL}$
C to Y	$t_R$	0.256	$0.139 + 0.058 \cdot \text{SL}$	$0.132 + 0.060 \cdot \text{SL}$	$0.124 + 0.061 \cdot \text{SL}$
	$t_F$	0.183	$0.126 + 0.029 \cdot \text{SL}$	$0.119 + 0.031 \cdot \text{SL}$	$0.106 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.153	$0.100 + 0.027 \cdot \text{SL}$	$0.102 + 0.026 \cdot \text{SL}$	$0.102 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.137	$0.102 + 0.017 \cdot \text{SL}$	$0.103 + 0.017 \cdot \text{SL}$	$0.104 + 0.017 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### AO21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.190	$0.137 + 0.026 \cdot \text{SL}$	$0.129 + 0.028 \cdot \text{SL}$	$0.112 + 0.030 \cdot \text{SL}$
	$t_F$	0.152	$0.108 + 0.022 \cdot \text{SL}$	$0.098 + 0.025 \cdot \text{SL}$	$0.082 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.076 + 0.013 \cdot \text{SL}$	$0.075 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.081 + 0.012 \cdot \text{SL}$	$0.080 + 0.012 \cdot \text{SL}$
B to Y	$t_R$	0.210	$0.157 + 0.027 \cdot \text{SL}$	$0.148 + 0.029 \cdot \text{SL}$	$0.131 + 0.030 \cdot \text{SL}$
	$t_F$	0.145	$0.100 + 0.022 \cdot \text{SL}$	$0.090 + 0.025 \cdot \text{SL}$	$0.078 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.112	$0.085 + 0.014 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$	$0.086 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.095	$0.067 + 0.014 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$
C to Y	$t_R$	0.197	$0.142 + 0.028 \cdot \text{SL}$	$0.135 + 0.030 \cdot \text{SL}$	$0.126 + 0.030 \cdot \text{SL}$
	$t_F$	0.153	$0.127 + 0.013 \cdot \text{SL}$	$0.121 + 0.015 \cdot \text{SL}$	$0.107 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.124	$0.096 + 0.014 \cdot \text{SL}$	$0.099 + 0.013 \cdot \text{SL}$	$0.100 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.118	$0.099 + 0.009 \cdot \text{SL}$	$0.102 + 0.009 \cdot \text{SL}$	$0.103 + 0.009 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## AO21DH/AO21/AO21D2/AO21D2B/AO21D4

### 2-AND into 2-NOR with 0.5X/1X/2X/2X(Bufferd)/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### AO21D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.054 + 0.013 \cdot \text{SL}$	$0.056 + 0.012 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.234	$0.216 + 0.009 \cdot \text{SL}$	$0.222 + 0.007 \cdot \text{SL}$	$0.228 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.221 + 0.010 \cdot \text{SL}$	$0.228 + 0.008 \cdot \text{SL}$	$0.238 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.085	$0.058 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.078	$0.050 + 0.014 \cdot \text{SL}$	$0.056 + 0.012 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.249	$0.232 + 0.009 \cdot \text{SL}$	$0.238 + 0.007 \cdot \text{SL}$	$0.244 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.232	$0.213 + 0.010 \cdot \text{SL}$	$0.221 + 0.008 \cdot \text{SL}$	$0.231 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.079	$0.053 + 0.013 \cdot \text{SL}$	$0.055 + 0.012 \cdot \text{SL}$	$0.049 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.267	$0.250 + 0.009 \cdot \text{SL}$	$0.256 + 0.007 \cdot \text{SL}$	$0.261 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.256	$0.237 + 0.010 \cdot \text{SL}$	$0.244 + 0.008 \cdot \text{SL}$	$0.254 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### AO21D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.077	$0.062 + 0.008 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.054 + 0.008 \cdot \text{SL}$
	$t_F$	0.070	$0.057 + 0.006 \cdot \text{SL}$	$0.057 + 0.006 \cdot \text{SL}$	$0.056 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.255	$0.245 + 0.005 \cdot \text{SL}$	$0.250 + 0.004 \cdot \text{SL}$	$0.260 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.251	$0.240 + 0.006 \cdot \text{SL}$	$0.245 + 0.004 \cdot \text{SL}$	$0.259 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_F$	0.070	$0.056 + 0.007 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.271	$0.261 + 0.005 \cdot \text{SL}$	$0.265 + 0.004 \cdot \text{SL}$	$0.276 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.243	$0.232 + 0.006 \cdot \text{SL}$	$0.238 + 0.004 \cdot \text{SL}$	$0.252 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_F$	0.068	$0.053 + 0.008 \cdot \text{SL}$	$0.058 + 0.006 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.287	$0.277 + 0.005 \cdot \text{SL}$	$0.282 + 0.004 \cdot \text{SL}$	$0.292 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.250 + 0.005 \cdot \text{SL}$	$0.255 + 0.004 \cdot \text{SL}$	$0.269 + 0.004 \cdot \text{SL}$

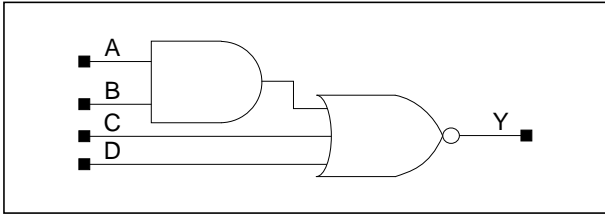
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# AO211DH/AO211/AO211D2/AO211D2B/AO211D4

## 2-AND into 3-NOR with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	Y
0	x	0	0	1
x	0	0	0	1
Other States				0

### Cell Data

Input Load (SL)																			
AO211DH				AO211				AO211D2				AO211D2B				AO211D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.6	0.6	0.6	0.9	0.9	0.8	0.9	1.7	1.8	1.8	2.0	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9
Gate Count																			
AO211DH				AO211				AO211D2				AO211D2B				AO211D4			
1.67				1.67				2.67				2.67				3.33			

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO211DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.582	$0.252 + 0.165 \cdot \text{SL}$	$0.237 + 0.169 \cdot \text{SL}$	$0.242 + 0.168 \cdot \text{SL}$
	$t_F$	0.294	$0.123 + 0.086 \cdot \text{SL}$	$0.109 + 0.089 \cdot \text{SL}$	$0.096 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.245	$0.101 + 0.072 \cdot \text{SL}$	$0.100 + 0.072 \cdot \text{SL}$	$0.100 + 0.072 \cdot \text{SL}$
	$t_{PHL}$	0.181	$0.095 + 0.043 \cdot \text{SL}$	$0.095 + 0.043 \cdot \text{SL}$	$0.094 + 0.043 \cdot \text{SL}$
B to Y	$t_R$	0.611	$0.282 + 0.164 \cdot \text{SL}$	$0.266 + 0.168 \cdot \text{SL}$	$0.271 + 0.168 \cdot \text{SL}$
	$t_F$	0.290	$0.115 + 0.087 \cdot \text{SL}$	$0.106 + 0.090 \cdot \text{SL}$	$0.097 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.261	$0.119 + 0.071 \cdot \text{SL}$	$0.117 + 0.072 \cdot \text{SL}$	$0.116 + 0.072 \cdot \text{SL}$
	$t_{PHL}$	0.175	$0.088 + 0.043 \cdot \text{SL}$	$0.088 + 0.043 \cdot \text{SL}$	$0.088 + 0.043 \cdot \text{SL}$
C to Y	$t_R$	0.620	$0.291 + 0.165 \cdot \text{SL}$	$0.282 + 0.167 \cdot \text{SL}$	$0.278 + 0.167 \cdot \text{SL}$
	$t_F$	0.230	$0.134 + 0.048 \cdot \text{SL}$	$0.124 + 0.051 \cdot \text{SL}$	$0.108 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.325	$0.180 + 0.073 \cdot \text{SL}$	$0.182 + 0.072 \cdot \text{SL}$	$0.184 + 0.072 \cdot \text{SL}$
	$t_{PHL}$	0.165	$0.109 + 0.028 \cdot \text{SL}$	$0.111 + 0.027 \cdot \text{SL}$	$0.112 + 0.027 \cdot \text{SL}$
D to Y	$t_R$	0.619	$0.289 + 0.165 \cdot \text{SL}$	$0.281 + 0.167 \cdot \text{SL}$	$0.278 + 0.167 \cdot \text{SL}$
	$t_F$	0.253	$0.157 + 0.048 \cdot \text{SL}$	$0.148 + 0.050 \cdot \text{SL}$	$0.131 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.332	$0.187 + 0.073 \cdot \text{SL}$	$0.189 + 0.072 \cdot \text{SL}$	$0.191 + 0.072 \cdot \text{SL}$
	$t_{PHL}$	0.172	$0.115 + 0.028 \cdot \text{SL}$	$0.118 + 0.028 \cdot \text{SL}$	$0.121 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO211DH/AO211/AO211D2/AO211D2B/AO211D4

## 2-AND into 3-NOR with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.389	$0.218 + 0.086 \cdot \text{SL}$	$0.207 + 0.088 \cdot \text{SL}$	$0.194 + 0.090 \cdot \text{SL}$
	$t_F$	0.224	$0.118 + 0.053 \cdot \text{SL}$	$0.106 + 0.056 \cdot \text{SL}$	$0.094 + 0.058 \cdot \text{SL}$
	$t_{PLH}$	0.162	$0.088 + 0.037 \cdot \text{SL}$	$0.083 + 0.038 \cdot \text{SL}$	$0.083 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.148	$0.093 + 0.028 \cdot \text{SL}$	$0.093 + 0.028 \cdot \text{SL}$	$0.093 + 0.028 \cdot \text{SL}$
B to Y	$t_R$	0.412	$0.242 + 0.085 \cdot \text{SL}$	$0.231 + 0.088 \cdot \text{SL}$	$0.217 + 0.090 \cdot \text{SL}$
	$t_F$	0.219	$0.110 + 0.054 \cdot \text{SL}$	$0.101 + 0.057 \cdot \text{SL}$	$0.094 + 0.058 \cdot \text{SL}$
	$t_{PLH}$	0.176	$0.102 + 0.037 \cdot \text{SL}$	$0.097 + 0.038 \cdot \text{SL}$	$0.096 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.141	$0.085 + 0.028 \cdot \text{SL}$	$0.086 + 0.028 \cdot \text{SL}$	$0.086 + 0.028 \cdot \text{SL}$
C to Y	$t_R$	0.418	$0.246 + 0.086 \cdot \text{SL}$	$0.238 + 0.088 \cdot \text{SL}$	$0.231 + 0.089 \cdot \text{SL}$
	$t_F$	0.229	$0.152 + 0.039 \cdot \text{SL}$	$0.144 + 0.041 \cdot \text{SL}$	$0.133 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.227	$0.149 + 0.039 \cdot \text{SL}$	$0.150 + 0.038 \cdot \text{SL}$	$0.152 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.175	$0.131 + 0.022 \cdot \text{SL}$	$0.132 + 0.022 \cdot \text{SL}$	$0.133 + 0.022 \cdot \text{SL}$
D to Y	$t_R$	0.416	$0.243 + 0.086 \cdot \text{SL}$	$0.236 + 0.088 \cdot \text{SL}$	$0.230 + 0.089 \cdot \text{SL}$
	$t_F$	0.262	$0.184 + 0.039 \cdot \text{SL}$	$0.179 + 0.040 \cdot \text{SL}$	$0.167 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.233	$0.156 + 0.039 \cdot \text{SL}$	$0.157 + 0.038 \cdot \text{SL}$	$0.158 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.188	$0.142 + 0.023 \cdot \text{SL}$	$0.145 + 0.022 \cdot \text{SL}$	$0.148 + 0.022 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### AO211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.291	$0.206 + 0.042 \cdot \text{SL}$	$0.198 + 0.044 \cdot \text{SL}$	$0.181 + 0.045 \cdot \text{SL}$
	$t_F$	0.165	$0.114 + 0.026 \cdot \text{SL}$	$0.106 + 0.028 \cdot \text{SL}$	$0.091 + 0.029 \cdot \text{SL}$
	$t_{PLH}$	0.123	$0.086 + 0.019 \cdot \text{SL}$	$0.083 + 0.019 \cdot \text{SL}$	$0.082 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.114	$0.085 + 0.015 \cdot \text{SL}$	$0.089 + 0.014 \cdot \text{SL}$	$0.088 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.315	$0.232 + 0.042 \cdot \text{SL}$	$0.223 + 0.044 \cdot \text{SL}$	$0.205 + 0.045 \cdot \text{SL}$
	$t_F$	0.160	$0.109 + 0.026 \cdot \text{SL}$	$0.099 + 0.028 \cdot \text{SL}$	$0.088 + 0.029 \cdot \text{SL}$
	$t_{PLH}$	0.138	$0.102 + 0.018 \cdot \text{SL}$	$0.098 + 0.019 \cdot \text{SL}$	$0.096 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.108	$0.078 + 0.015 \cdot \text{SL}$	$0.082 + 0.014 \cdot \text{SL}$	$0.082 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.316	$0.230 + 0.043 \cdot \text{SL}$	$0.225 + 0.044 \cdot \text{SL}$	$0.214 + 0.045 \cdot \text{SL}$
	$t_F$	0.179	$0.142 + 0.019 \cdot \text{SL}$	$0.137 + 0.020 \cdot \text{SL}$	$0.125 + 0.021 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.140 + 0.020 \cdot \text{SL}$	$0.141 + 0.020 \cdot \text{SL}$	$0.142 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.146	$0.123 + 0.011 \cdot \text{SL}$	$0.124 + 0.011 \cdot \text{SL}$	$0.125 + 0.011 \cdot \text{SL}$
D to Y	$t_R$	0.313	$0.226 + 0.043 \cdot \text{SL}$	$0.222 + 0.044 \cdot \text{SL}$	$0.213 + 0.045 \cdot \text{SL}$
	$t_F$	0.210	$0.172 + 0.019 \cdot \text{SL}$	$0.169 + 0.020 \cdot \text{SL}$	$0.158 + 0.021 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.148 + 0.020 \cdot \text{SL}$	$0.149 + 0.020 \cdot \text{SL}$	$0.151 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.159	$0.135 + 0.012 \cdot \text{SL}$	$0.137 + 0.011 \cdot \text{SL}$	$0.140 + 0.011 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# AO211DH/AO211/AO211D2/AO211D2B/AO211D4

## 2-AND into 3-NOR with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO211D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.091	$0.064 + 0.013 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.013 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.280	$0.263 + 0.009 \cdot \text{SL}$	$0.269 + 0.007 \cdot \text{SL}$	$0.276 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.266	$0.246 + 0.010 \cdot \text{SL}$	$0.254 + 0.008 \cdot \text{SL}$	$0.264 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.092	$0.065 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.055 + 0.013 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.298	$0.281 + 0.009 \cdot \text{SL}$	$0.287 + 0.007 \cdot \text{SL}$	$0.294 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.259	$0.240 + 0.010 \cdot \text{SL}$	$0.247 + 0.008 \cdot \text{SL}$	$0.257 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.093	$0.065 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.052 + 0.014 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.349	$0.331 + 0.009 \cdot \text{SL}$	$0.338 + 0.007 \cdot \text{SL}$	$0.345 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.281 + 0.010 \cdot \text{SL}$	$0.288 + 0.008 \cdot \text{SL}$	$0.299 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.092	$0.066 + 0.013 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.013 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.357	$0.339 + 0.009 \cdot \text{SL}$	$0.345 + 0.007 \cdot \text{SL}$	$0.352 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.300 + 0.010 \cdot \text{SL}$	$0.307 + 0.008 \cdot \text{SL}$	$0.317 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### AO211D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_F$	0.072	$0.060 + 0.006 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$	$0.058 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.307	$0.296 + 0.005 \cdot \text{SL}$	$0.301 + 0.004 \cdot \text{SL}$	$0.313 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.276	$0.265 + 0.006 \cdot \text{SL}$	$0.270 + 0.004 \cdot \text{SL}$	$0.284 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.086	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.072	$0.058 + 0.007 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.324	$0.314 + 0.005 \cdot \text{SL}$	$0.319 + 0.004 \cdot \text{SL}$	$0.331 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.269	$0.258 + 0.006 \cdot \text{SL}$	$0.263 + 0.004 \cdot \text{SL}$	$0.277 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_F$	0.070	$0.055 + 0.008 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.375	$0.365 + 0.005 \cdot \text{SL}$	$0.370 + 0.004 \cdot \text{SL}$	$0.382 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.306	$0.295 + 0.006 \cdot \text{SL}$	$0.301 + 0.004 \cdot \text{SL}$	$0.314 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.086	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_F$	0.072	$0.057 + 0.007 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.058 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.381	$0.371 + 0.005 \cdot \text{SL}$	$0.376 + 0.004 \cdot \text{SL}$	$0.388 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.324	$0.313 + 0.006 \cdot \text{SL}$	$0.318 + 0.004 \cdot \text{SL}$	$0.332 + 0.004 \cdot \text{SL}$

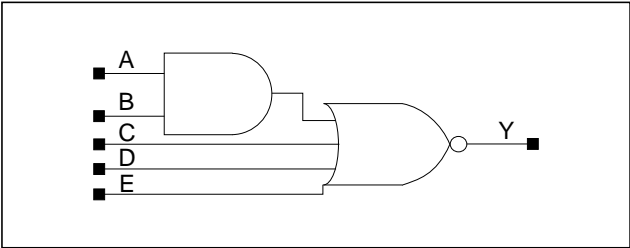
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO2111/AO2111D2

2-AND into 4-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0
Other states					1

Cell Data

Input Load (SL)										Gate Count	
AO2111					AO2111D2					AO2111	AO2111D2
A	B	C	D	E	A	B	C	D	E		
0.9	0.9	0.8	0.8	0.8	0.9	0.9	0.8	0.8	0.9	2.00	3.00



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AO2111**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.550	$0.316 + 0.117 \cdot \text{SL}$	$0.307 + 0.119 \cdot \text{SL}$	$0.298 + 0.120 \cdot \text{SL}$
	$t_F$	0.241	$0.129 + 0.056 \cdot \text{SL}$	$0.118 + 0.059 \cdot \text{SL}$	$0.107 + 0.060 \cdot \text{SL}$
	$t_{PLH}$	0.193	$0.096 + 0.049 \cdot \text{SL}$	$0.086 + 0.051 \cdot \text{SL}$	$0.087 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.159	$0.101 + 0.029 \cdot \text{SL}$	$0.101 + 0.029 \cdot \text{SL}$	$0.100 + 0.029 \cdot \text{SL}$
B to Y	$t_R$	0.581	$0.349 + 0.116 \cdot \text{SL}$	$0.338 + 0.119 \cdot \text{SL}$	$0.329 + 0.120 \cdot \text{SL}$
	$t_F$	0.237	$0.122 + 0.057 \cdot \text{SL}$	$0.115 + 0.059 \cdot \text{SL}$	$0.107 + 0.060 \cdot \text{SL}$
	$t_{PLH}$	0.210	$0.111 + 0.049 \cdot \text{SL}$	$0.105 + 0.051 \cdot \text{SL}$	$0.105 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.152	$0.094 + 0.029 \cdot \text{SL}$	$0.094 + 0.029 \cdot \text{SL}$	$0.094 + 0.029 \cdot \text{SL}$
C to Y	$t_R$	0.608	$0.377 + 0.116 \cdot \text{SL}$	$0.369 + 0.118 \cdot \text{SL}$	$0.364 + 0.118 \cdot \text{SL}$
	$t_F$	0.275	$0.179 + 0.048 \cdot \text{SL}$	$0.171 + 0.050 \cdot \text{SL}$	$0.163 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.295	$0.191 + 0.052 \cdot \text{SL}$	$0.193 + 0.051 \cdot \text{SL}$	$0.196 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.210	$0.156 + 0.027 \cdot \text{SL}$	$0.158 + 0.027 \cdot \text{SL}$	$0.159 + 0.026 \cdot \text{SL}$
D to Y	$t_R$	0.610	$0.379 + 0.116 \cdot \text{SL}$	$0.371 + 0.117 \cdot \text{SL}$	$0.365 + 0.118 \cdot \text{SL}$
	$t_F$	0.315	$0.218 + 0.049 \cdot \text{SL}$	$0.212 + 0.050 \cdot \text{SL}$	$0.203 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.326	$0.222 + 0.052 \cdot \text{SL}$	$0.224 + 0.051 \cdot \text{SL}$	$0.227 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.230	$0.174 + 0.028 \cdot \text{SL}$	$0.177 + 0.027 \cdot \text{SL}$	$0.180 + 0.027 \cdot \text{SL}$
E to Y	$t_R$	0.608	$0.376 + 0.116 \cdot \text{SL}$	$0.369 + 0.118 \cdot \text{SL}$	$0.364 + 0.118 \cdot \text{SL}$
	$t_F$	0.352	$0.253 + 0.050 \cdot \text{SL}$	$0.251 + 0.050 \cdot \text{SL}$	$0.243 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.339	$0.235 + 0.052 \cdot \text{SL}$	$0.238 + 0.051 \cdot \text{SL}$	$0.240 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.243	$0.185 + 0.029 \cdot \text{SL}$	$0.190 + 0.028 \cdot \text{SL}$	$0.196 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AO2111/AO2111D2

### 2-AND into 4-NOR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO2111D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.096	$0.069 + 0.013 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.013 \cdot \text{SL}$	$0.059 + 0.012 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.300	$0.282 + 0.009 \cdot \text{SL}$	$0.289 + 0.007 \cdot \text{SL}$	$0.296 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.269	$0.249 + 0.010 \cdot \text{SL}$	$0.257 + 0.008 \cdot \text{SL}$	$0.267 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.098	$0.072 + 0.013 \cdot \text{SL}$	$0.068 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.053 + 0.014 \cdot \text{SL}$	$0.057 + 0.012 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.322	$0.305 + 0.009 \cdot \text{SL}$	$0.311 + 0.007 \cdot \text{SL}$	$0.319 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.242 + 0.010 \cdot \text{SL}$	$0.250 + 0.008 \cdot \text{SL}$	$0.260 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.098	$0.071 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.055 + 0.013 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.405	$0.387 + 0.009 \cdot \text{SL}$	$0.394 + 0.007 \cdot \text{SL}$	$0.402 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.330	$0.310 + 0.010 \cdot \text{SL}$	$0.318 + 0.008 \cdot \text{SL}$	$0.328 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.099	$0.072 + 0.014 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.014 \cdot \text{SL}$	$0.059 + 0.012 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.436	$0.419 + 0.009 \cdot \text{SL}$	$0.426 + 0.007 \cdot \text{SL}$	$0.433 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.355	$0.336 + 0.010 \cdot \text{SL}$	$0.343 + 0.008 \cdot \text{SL}$	$0.354 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.099	$0.072 + 0.014 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.057 + 0.013 \cdot \text{SL}$	$0.062 + 0.012 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.450	$0.432 + 0.009 \cdot \text{SL}$	$0.439 + 0.007 \cdot \text{SL}$	$0.446 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.373	$0.354 + 0.010 \cdot \text{SL}$	$0.361 + 0.008 \cdot \text{SL}$	$0.372 + 0.007 \cdot \text{SL}$

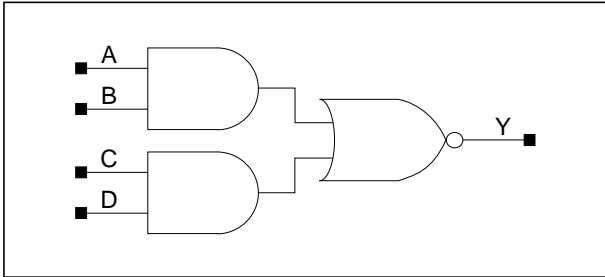
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# AO22DH/AO22/AO22D2/AO22D2B/AO22D4

Two 2-ANDs into 2-NOR with 0.5X/1X/2X/2X(Buffered)/4X Drive

## Logic Symbol



## Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

## Cell Data

Input Load (SL)																			
AO22DH				AO22				AO22D2				AO22D2B				AO22D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.5	0.5	0.5	1.0	1.0	1.0	1.0	2.0	1.9	2.1	2.0	1.0	1.1	1.1	1.0	1.0	1.1	1.0	1.0
Gate Count																			
AO22DH				AO22				AO22D2				AO22D2B				AO22D4			
1.67				1.67				2.67				2.67				3.33			

## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

### AO22DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.444	$0.184 + 0.130 \cdot \text{SL}$	$0.168 + 0.134 \cdot \text{SL}$	$0.164 + 0.135 \cdot \text{SL}$
	$t_F$	0.292	$0.128 + 0.082 \cdot \text{SL}$	$0.112 + 0.086 \cdot \text{SL}$	$0.097 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.217	$0.102 + 0.057 \cdot \text{SL}$	$0.101 + 0.058 \cdot \text{SL}$	$0.101 + 0.058 \cdot \text{SL}$
	$t_{PHL}$	0.171	$0.087 + 0.042 \cdot \text{SL}$	$0.087 + 0.042 \cdot \text{SL}$	$0.087 + 0.042 \cdot \text{SL}$
B to Y	$t_R$	0.469	$0.209 + 0.130 \cdot \text{SL}$	$0.193 + 0.134 \cdot \text{SL}$	$0.189 + 0.135 \cdot \text{SL}$
	$t_F$	0.287	$0.120 + 0.084 \cdot \text{SL}$	$0.108 + 0.087 \cdot \text{SL}$	$0.098 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.231	$0.117 + 0.057 \cdot \text{SL}$	$0.115 + 0.058 \cdot \text{SL}$	$0.114 + 0.058 \cdot \text{SL}$
	$t_{PHL}$	0.163	$0.078 + 0.042 \cdot \text{SL}$	$0.080 + 0.042 \cdot \text{SL}$	$0.080 + 0.042 \cdot \text{SL}$
C to Y	$t_R$	0.445	$0.182 + 0.131 \cdot \text{SL}$	$0.172 + 0.134 \cdot \text{SL}$	$0.168 + 0.134 \cdot \text{SL}$
	$t_F$	0.351	$0.184 + 0.083 \cdot \text{SL}$	$0.171 + 0.087 \cdot \text{SL}$	$0.159 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.260	$0.143 + 0.058 \cdot \text{SL}$	$0.145 + 0.058 \cdot \text{SL}$	$0.147 + 0.058 \cdot \text{SL}$
	$t_{PHL}$	0.220	$0.133 + 0.043 \cdot \text{SL}$	$0.137 + 0.042 \cdot \text{SL}$	$0.139 + 0.042 \cdot \text{SL}$
D to Y	$t_R$	0.469	$0.206 + 0.132 \cdot \text{SL}$	$0.197 + 0.134 \cdot \text{SL}$	$0.193 + 0.134 \cdot \text{SL}$
	$t_F$	0.347	$0.177 + 0.085 \cdot \text{SL}$	$0.168 + 0.087 \cdot \text{SL}$	$0.160 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.275	$0.159 + 0.058 \cdot \text{SL}$	$0.160 + 0.058 \cdot \text{SL}$	$0.161 + 0.058 \cdot \text{SL}$
	$t_{PHL}$	0.213	$0.126 + 0.043 \cdot \text{SL}$	$0.130 + 0.042 \cdot \text{SL}$	$0.132 + 0.042 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AO22DH/AO22/AO22D2/AO22D2B/AO22D4

### Two 2-ANDs into 2-NOR with 0.5X/1X/2X/2X(Buffered)/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.277	$0.163 + 0.057 \cdot \text{SL}$	$0.155 + 0.059 \cdot \text{SL}$	$0.143 + 0.060 \cdot \text{SL}$
	$t_F$	0.200	$0.125 + 0.038 \cdot \text{SL}$	$0.114 + 0.040 \cdot \text{SL}$	$0.101 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.144	$0.093 + 0.026 \cdot \text{SL}$	$0.092 + 0.026 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.120	$0.077 + 0.021 \cdot \text{SL}$	$0.081 + 0.020 \cdot \text{SL}$	$0.081 + 0.020 \cdot \text{SL}$
B to Y	$t_R$	0.299	$0.186 + 0.057 \cdot \text{SL}$	$0.177 + 0.059 \cdot \text{SL}$	$0.165 + 0.060 \cdot \text{SL}$
	$t_F$	0.192	$0.115 + 0.038 \cdot \text{SL}$	$0.104 + 0.041 \cdot \text{SL}$	$0.096 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.157	$0.107 + 0.025 \cdot \text{SL}$	$0.105 + 0.026 \cdot \text{SL}$	$0.104 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.112	$0.069 + 0.022 \cdot \text{SL}$	$0.074 + 0.020 \cdot \text{SL}$	$0.074 + 0.020 \cdot \text{SL}$
C to Y	$t_R$	0.274	$0.158 + 0.058 \cdot \text{SL}$	$0.151 + 0.060 \cdot \text{SL}$	$0.144 + 0.060 \cdot \text{SL}$
	$t_F$	0.250	$0.172 + 0.039 \cdot \text{SL}$	$0.165 + 0.041 \cdot \text{SL}$	$0.155 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.174	$0.121 + 0.027 \cdot \text{SL}$	$0.122 + 0.026 \cdot \text{SL}$	$0.123 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.167	$0.125 + 0.021 \cdot \text{SL}$	$0.126 + 0.021 \cdot \text{SL}$	$0.128 + 0.020 \cdot \text{SL}$
D to Y	$t_R$	0.295	$0.178 + 0.058 \cdot \text{SL}$	$0.172 + 0.060 \cdot \text{SL}$	$0.166 + 0.060 \cdot \text{SL}$
	$t_F$	0.245	$0.165 + 0.040 \cdot \text{SL}$	$0.160 + 0.041 \cdot \text{SL}$	$0.152 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.188	$0.135 + 0.026 \cdot \text{SL}$	$0.136 + 0.026 \cdot \text{SL}$	$0.137 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.159	$0.117 + 0.021 \cdot \text{SL}$	$0.119 + 0.021 \cdot \text{SL}$	$0.121 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### AO22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.223	$0.166 + 0.028 \cdot \text{SL}$	$0.162 + 0.029 \cdot \text{SL}$	$0.147 + 0.031 \cdot \text{SL}$
	$t_F$	0.170	$0.132 + 0.019 \cdot \text{SL}$	$0.124 + 0.021 \cdot \text{SL}$	$0.110 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.122	$0.095 + 0.013 \cdot \text{SL}$	$0.097 + 0.013 \cdot \text{SL}$	$0.095 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.101	$0.076 + 0.012 \cdot \text{SL}$	$0.083 + 0.011 \cdot \text{SL}$	$0.083 + 0.011 \cdot \text{SL}$
B to Y	$t_R$	0.248	$0.191 + 0.028 \cdot \text{SL}$	$0.187 + 0.029 \cdot \text{SL}$	$0.171 + 0.031 \cdot \text{SL}$
	$t_F$	0.161	$0.122 + 0.019 \cdot \text{SL}$	$0.116 + 0.021 \cdot \text{SL}$	$0.103 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.137	$0.111 + 0.013 \cdot \text{SL}$	$0.110 + 0.013 \cdot \text{SL}$	$0.109 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.094	$0.070 + 0.012 \cdot \text{SL}$	$0.075 + 0.011 \cdot \text{SL}$	$0.077 + 0.011 \cdot \text{SL}$
C to Y	$t_R$	0.216	$0.159 + 0.028 \cdot \text{SL}$	$0.154 + 0.030 \cdot \text{SL}$	$0.145 + 0.030 \cdot \text{SL}$
	$t_F$	0.209	$0.170 + 0.019 \cdot \text{SL}$	$0.167 + 0.020 \cdot \text{SL}$	$0.153 + 0.021 \cdot \text{SL}$
	$t_{PLH}$	0.146	$0.118 + 0.014 \cdot \text{SL}$	$0.121 + 0.013 \cdot \text{SL}$	$0.122 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.143	$0.122 + 0.011 \cdot \text{SL}$	$0.122 + 0.010 \cdot \text{SL}$	$0.124 + 0.010 \cdot \text{SL}$
D to Y	$t_R$	0.240	$0.182 + 0.029 \cdot \text{SL}$	$0.178 + 0.030 \cdot \text{SL}$	$0.170 + 0.031 \cdot \text{SL}$
	$t_F$	0.202	$0.163 + 0.020 \cdot \text{SL}$	$0.158 + 0.021 \cdot \text{SL}$	$0.150 + 0.021 \cdot \text{SL}$
	$t_{PLH}$	0.163	$0.136 + 0.013 \cdot \text{SL}$	$0.136 + 0.013 \cdot \text{SL}$	$0.137 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.136	$0.114 + 0.011 \cdot \text{SL}$	$0.115 + 0.011 \cdot \text{SL}$	$0.118 + 0.010 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# AO22DH/AO22/AO22D2/AO22D2B/AO22D4

## Two 2-ANDs into 2-NOR with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO22D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.052 + 0.014 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.261	$0.244 + 0.009 \cdot \text{SL}$	$0.249 + 0.007 \cdot \text{SL}$	$0.256 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.220 + 0.010 \cdot \text{SL}$	$0.228 + 0.008 \cdot \text{SL}$	$0.238 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.053 + 0.013 \cdot \text{SL}$	$0.057 + 0.012 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.280	$0.263 + 0.008 \cdot \text{SL}$	$0.269 + 0.007 \cdot \text{SL}$	$0.274 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.233	$0.214 + 0.010 \cdot \text{SL}$	$0.221 + 0.008 \cdot \text{SL}$	$0.231 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.086	$0.059 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.013 \cdot \text{SL}$	$0.059 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.280	$0.264 + 0.008 \cdot \text{SL}$	$0.269 + 0.007 \cdot \text{SL}$	$0.275 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.285	$0.266 + 0.010 \cdot \text{SL}$	$0.274 + 0.008 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.013 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.298	$0.281 + 0.008 \cdot \text{SL}$	$0.286 + 0.007 \cdot \text{SL}$	$0.292 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.258 + 0.010 \cdot \text{SL}$	$0.266 + 0.008 \cdot \text{SL}$	$0.276 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### AO22D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.071	$0.056 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$	$0.056 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.276	$0.265 + 0.005 \cdot \text{SL}$	$0.270 + 0.004 \cdot \text{SL}$	$0.281 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.245	$0.234 + 0.006 \cdot \text{SL}$	$0.239 + 0.004 \cdot \text{SL}$	$0.254 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.079	$0.064 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.059 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.294	$0.284 + 0.005 \cdot \text{SL}$	$0.289 + 0.004 \cdot \text{SL}$	$0.299 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.228 + 0.006 \cdot \text{SL}$	$0.233 + 0.004 \cdot \text{SL}$	$0.247 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.058 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.303	$0.293 + 0.005 \cdot \text{SL}$	$0.297 + 0.004 \cdot \text{SL}$	$0.308 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.288 + 0.006 \cdot \text{SL}$	$0.294 + 0.004 \cdot \text{SL}$	$0.308 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.079	$0.064 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.058 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.322	$0.312 + 0.005 \cdot \text{SL}$	$0.317 + 0.004 \cdot \text{SL}$	$0.328 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.294	$0.283 + 0.006 \cdot \text{SL}$	$0.288 + 0.004 \cdot \text{SL}$	$0.302 + 0.004 \cdot \text{SL}$

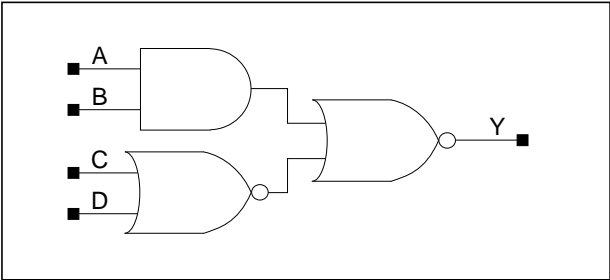
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO22DHA/AO22A/AO22D2A/AO22D4A

2-AND and 2-NOR into 2-NOR with 0.5X/1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)															
AO22DHA				AO22A				AO22D2A				AO22D4A			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.5	0.5	0.6	1.0	1.0	0.9	0.9	2.0	2.0	0.9	0.9	1.0	1.1	0.9	0.9
Gate Count															
AO22DHA				AO22A				AO22D2A				AO22D4A			
2.67				2.67				3.67				4.33			



# AO22DHA/AO22A/AO22D2A/AO22D4A

## 2-AND and 2-NOR into 2-NOR with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO22DHA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.436	$0.182 + 0.127 \cdot \text{SL}$	$0.166 + 0.131 \cdot \text{SL}$	$0.161 + 0.131 \cdot \text{SL}$
	$t_F$	0.293	$0.128 + 0.082 \cdot \text{SL}$	$0.112 + 0.086 \cdot \text{SL}$	$0.097 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.213	$0.101 + 0.056 \cdot \text{SL}$	$0.099 + 0.056 \cdot \text{SL}$	$0.099 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.170	$0.086 + 0.042 \cdot \text{SL}$	$0.086 + 0.042 \cdot \text{SL}$	$0.087 + 0.042 \cdot \text{SL}$
B to Y	$t_R$	0.460	$0.206 + 0.127 \cdot \text{SL}$	$0.190 + 0.131 \cdot \text{SL}$	$0.185 + 0.132 \cdot \text{SL}$
	$t_F$	0.288	$0.120 + 0.084 \cdot \text{SL}$	$0.108 + 0.087 \cdot \text{SL}$	$0.098 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.226	$0.115 + 0.056 \cdot \text{SL}$	$0.113 + 0.056 \cdot \text{SL}$	$0.112 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.163	$0.078 + 0.043 \cdot \text{SL}$	$0.079 + 0.042 \cdot \text{SL}$	$0.080 + 0.042 \cdot \text{SL}$
C to Y	$t_R$	0.436	$0.175 + 0.131 \cdot \text{SL}$	$0.169 + 0.132 \cdot \text{SL}$	$0.167 + 0.132 \cdot \text{SL}$
	$t_F$	0.349	$0.176 + 0.086 \cdot \text{SL}$	$0.171 + 0.088 \cdot \text{SL}$	$0.167 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.316	$0.200 + 0.058 \cdot \text{SL}$	$0.203 + 0.057 \cdot \text{SL}$	$0.205 + 0.057 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.202 + 0.044 \cdot \text{SL}$	$0.207 + 0.043 \cdot \text{SL}$	$0.210 + 0.042 \cdot \text{SL}$
D to Y	$t_R$	0.457	$0.197 + 0.130 \cdot \text{SL}$	$0.192 + 0.131 \cdot \text{SL}$	$0.189 + 0.131 \cdot \text{SL}$
	$t_F$	0.347	$0.173 + 0.087 \cdot \text{SL}$	$0.170 + 0.088 \cdot \text{SL}$	$0.167 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.325	$0.212 + 0.057 \cdot \text{SL}$	$0.213 + 0.057 \cdot \text{SL}$	$0.214 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.201 + 0.044 \cdot \text{SL}$	$0.206 + 0.043 \cdot \text{SL}$	$0.209 + 0.042 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### AO22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.278	$0.164 + 0.057 \cdot \text{SL}$	$0.156 + 0.059 \cdot \text{SL}$	$0.144 + 0.060 \cdot \text{SL}$
	$t_F$	0.200	$0.125 + 0.037 \cdot \text{SL}$	$0.114 + 0.040 \cdot \text{SL}$	$0.101 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.144	$0.093 + 0.026 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.119	$0.077 + 0.021 \cdot \text{SL}$	$0.081 + 0.020 \cdot \text{SL}$	$0.081 + 0.020 \cdot \text{SL}$
B to Y	$t_R$	0.300	$0.186 + 0.057 \cdot \text{SL}$	$0.178 + 0.059 \cdot \text{SL}$	$0.166 + 0.060 \cdot \text{SL}$
	$t_F$	0.192	$0.115 + 0.039 \cdot \text{SL}$	$0.105 + 0.041 \cdot \text{SL}$	$0.097 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.157	$0.107 + 0.025 \cdot \text{SL}$	$0.105 + 0.026 \cdot \text{SL}$	$0.103 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.112	$0.069 + 0.022 \cdot \text{SL}$	$0.073 + 0.020 \cdot \text{SL}$	$0.074 + 0.020 \cdot \text{SL}$
C to Y	$t_R$	0.268	$0.150 + 0.059 \cdot \text{SL}$	$0.146 + 0.060 \cdot \text{SL}$	$0.142 + 0.061 \cdot \text{SL}$
	$t_F$	0.237	$0.154 + 0.041 \cdot \text{SL}$	$0.152 + 0.042 \cdot \text{SL}$	$0.148 + 0.043 \cdot \text{SL}$
	$t_{PLH}$	0.271	$0.217 + 0.027 \cdot \text{SL}$	$0.219 + 0.026 \cdot \text{SL}$	$0.221 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.207	$0.163 + 0.022 \cdot \text{SL}$	$0.166 + 0.021 \cdot \text{SL}$	$0.169 + 0.021 \cdot \text{SL}$
D to Y	$t_R$	0.290	$0.172 + 0.059 \cdot \text{SL}$	$0.167 + 0.060 \cdot \text{SL}$	$0.164 + 0.061 \cdot \text{SL}$
	$t_F$	0.235	$0.151 + 0.042 \cdot \text{SL}$	$0.149 + 0.042 \cdot \text{SL}$	$0.147 + 0.043 \cdot \text{SL}$
	$t_{PLH}$	0.283	$0.230 + 0.027 \cdot \text{SL}$	$0.231 + 0.026 \cdot \text{SL}$	$0.232 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.208	$0.164 + 0.022 \cdot \text{SL}$	$0.167 + 0.021 \cdot \text{SL}$	$0.170 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO22DHA/AO22A/AO22D2A/AO22D4A

## 2-AND and 2-NOR into 2-NOR with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.224	$0.168 + 0.028 \cdot \text{SL}$	$0.163 + 0.029 \cdot \text{SL}$	$0.148 + 0.031 \cdot \text{SL}$
	$t_F$	0.170	$0.133 + 0.018 \cdot \text{SL}$	$0.125 + 0.021 \cdot \text{SL}$	$0.110 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.121	$0.095 + 0.013 \cdot \text{SL}$	$0.096 + 0.013 \cdot \text{SL}$	$0.094 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.100	$0.075 + 0.012 \cdot \text{SL}$	$0.082 + 0.011 \cdot \text{SL}$	$0.083 + 0.011 \cdot \text{SL}$
B to Y	$t_R$	0.249	$0.193 + 0.028 \cdot \text{SL}$	$0.188 + 0.029 \cdot \text{SL}$	$0.173 + 0.031 \cdot \text{SL}$
	$t_F$	0.161	$0.122 + 0.020 \cdot \text{SL}$	$0.117 + 0.021 \cdot \text{SL}$	$0.104 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.137	$0.111 + 0.013 \cdot \text{SL}$	$0.110 + 0.013 \cdot \text{SL}$	$0.109 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.093	$0.069 + 0.012 \cdot \text{SL}$	$0.074 + 0.011 \cdot \text{SL}$	$0.076 + 0.011 \cdot \text{SL}$
C to Y	$t_R$	0.215	$0.156 + 0.030 \cdot \text{SL}$	$0.153 + 0.030 \cdot \text{SL}$	$0.146 + 0.031 \cdot \text{SL}$
	$t_F$	0.197	$0.155 + 0.021 \cdot \text{SL}$	$0.154 + 0.021 \cdot \text{SL}$	$0.149 + 0.021 \cdot \text{SL}$
	$t_{PLH}$	0.264	$0.235 + 0.014 \cdot \text{SL}$	$0.238 + 0.013 \cdot \text{SL}$	$0.241 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.213	$0.190 + 0.011 \cdot \text{SL}$	$0.192 + 0.011 \cdot \text{SL}$	$0.196 + 0.010 \cdot \text{SL}$
D to Y	$t_R$	0.238	$0.178 + 0.030 \cdot \text{SL}$	$0.176 + 0.030 \cdot \text{SL}$	$0.170 + 0.031 \cdot \text{SL}$
	$t_F$	0.193	$0.151 + 0.021 \cdot \text{SL}$	$0.150 + 0.021 \cdot \text{SL}$	$0.148 + 0.021 \cdot \text{SL}$
	$t_{PLH}$	0.274	$0.246 + 0.014 \cdot \text{SL}$	$0.248 + 0.013 \cdot \text{SL}$	$0.249 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.188 + 0.011 \cdot \text{SL}$	$0.190 + 0.011 \cdot \text{SL}$	$0.194 + 0.010 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### AO22D4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.058 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.277	$0.267 + 0.005 \cdot \text{SL}$	$0.272 + 0.004 \cdot \text{SL}$	$0.283 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.247	$0.235 + 0.006 \cdot \text{SL}$	$0.241 + 0.004 \cdot \text{SL}$	$0.255 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.059 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.296	$0.286 + 0.005 \cdot \text{SL}$	$0.290 + 0.004 \cdot \text{SL}$	$0.301 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.229 + 0.006 \cdot \text{SL}$	$0.234 + 0.004 \cdot \text{SL}$	$0.248 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.056 + 0.008 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.402	$0.392 + 0.005 \cdot \text{SL}$	$0.397 + 0.004 \cdot \text{SL}$	$0.407 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.341	$0.329 + 0.006 \cdot \text{SL}$	$0.335 + 0.004 \cdot \text{SL}$	$0.349 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.080	$0.065 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.058 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.421	$0.411 + 0.005 \cdot \text{SL}$	$0.416 + 0.004 \cdot \text{SL}$	$0.426 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.343	$0.331 + 0.006 \cdot \text{SL}$	$0.337 + 0.004 \cdot \text{SL}$	$0.351 + 0.004 \cdot \text{SL}$

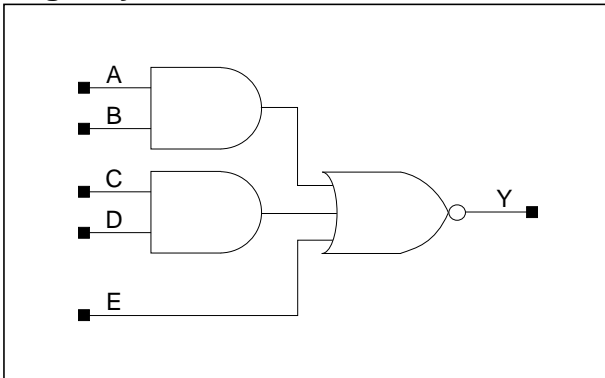
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## AO221/AO221D2/AO221D4

### Two 2-ANDs into 3-NOR with 1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	C	D	E	Y
1	1	x	x	x	0
x	x	1	1	x	0
x	x	x	x	1	0
Other States					1

#### Cell Data

Input Load (SL)														
AO221					AO221D2					AO221D4				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	1.0	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9
Gate Count														
AO221					AO221D2					AO221D4				
2.00					3.00					3.67				



## AO221/AO221D2/AO221D4

### Two 2-ANDs into 3-NOR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO221

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.427	$0.250 + 0.089 \cdot \text{SL}$	$0.241 + 0.091 \cdot \text{SL}$	$0.230 + 0.092 \cdot \text{SL}$
	$t_F$	0.237	$0.139 + 0.049 \cdot \text{SL}$	$0.129 + 0.051 \cdot \text{SL}$	$0.116 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.183	$0.107 + 0.038 \cdot \text{SL}$	$0.102 + 0.039 \cdot \text{SL}$	$0.102 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.145	$0.094 + 0.026 \cdot \text{SL}$	$0.095 + 0.025 \cdot \text{SL}$	$0.095 + 0.025 \cdot \text{SL}$
B to Y	$t_R$	0.456	$0.279 + 0.089 \cdot \text{SL}$	$0.269 + 0.091 \cdot \text{SL}$	$0.258 + 0.092 \cdot \text{SL}$
	$t_F$	0.231	$0.132 + 0.050 \cdot \text{SL}$	$0.122 + 0.052 \cdot \text{SL}$	$0.115 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.199	$0.122 + 0.038 \cdot \text{SL}$	$0.119 + 0.039 \cdot \text{SL}$	$0.118 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.138	$0.086 + 0.026 \cdot \text{SL}$	$0.088 + 0.026 \cdot \text{SL}$	$0.088 + 0.026 \cdot \text{SL}$
C to Y	$t_R$	0.436	$0.260 + 0.088 \cdot \text{SL}$	$0.252 + 0.090 \cdot \text{SL}$	$0.246 + 0.091 \cdot \text{SL}$
	$t_F$	0.289	$0.189 + 0.050 \cdot \text{SL}$	$0.182 + 0.052 \cdot \text{SL}$	$0.172 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.237	$0.157 + 0.040 \cdot \text{SL}$	$0.159 + 0.039 \cdot \text{SL}$	$0.161 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.195	$0.143 + 0.026 \cdot \text{SL}$	$0.145 + 0.026 \cdot \text{SL}$	$0.146 + 0.026 \cdot \text{SL}$
D to Y	$t_R$	0.466	$0.287 + 0.089 \cdot \text{SL}$	$0.281 + 0.091 \cdot \text{SL}$	$0.274 + 0.092 \cdot \text{SL}$
	$t_F$	0.286	$0.184 + 0.051 \cdot \text{SL}$	$0.179 + 0.052 \cdot \text{SL}$	$0.172 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.256	$0.176 + 0.040 \cdot \text{SL}$	$0.178 + 0.040 \cdot \text{SL}$	$0.179 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.190	$0.137 + 0.026 \cdot \text{SL}$	$0.139 + 0.026 \cdot \text{SL}$	$0.141 + 0.026 \cdot \text{SL}$
E to Y	$t_R$	0.464	$0.285 + 0.090 \cdot \text{SL}$	$0.279 + 0.091 \cdot \text{SL}$	$0.274 + 0.092 \cdot \text{SL}$
	$t_F$	0.251	$0.186 + 0.033 \cdot \text{SL}$	$0.183 + 0.033 \cdot \text{SL}$	$0.175 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.282	$0.202 + 0.040 \cdot \text{SL}$	$0.203 + 0.040 \cdot \text{SL}$	$0.205 + 0.040 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.136 + 0.020 \cdot \text{SL}$	$0.139 + 0.019 \cdot \text{SL}$	$0.144 + 0.019 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**AO221D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.091	$0.064 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.055 + 0.013 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.297	$0.280 + 0.009 \cdot \text{SL}$	$0.286 + 0.007 \cdot \text{SL}$	$0.293 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.271	$0.251 + 0.010 \cdot \text{SL}$	$0.259 + 0.008 \cdot \text{SL}$	$0.270 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.093	$0.066 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.013 \cdot \text{SL}$	$0.059 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.318	$0.300 + 0.009 \cdot \text{SL}$	$0.307 + 0.007 \cdot \text{SL}$	$0.314 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.263	$0.244 + 0.010 \cdot \text{SL}$	$0.252 + 0.008 \cdot \text{SL}$	$0.262 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.093	$0.064 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.370	$0.352 + 0.009 \cdot \text{SL}$	$0.359 + 0.007 \cdot \text{SL}$	$0.366 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.340	$0.320 + 0.010 \cdot \text{SL}$	$0.328 + 0.008 \cdot \text{SL}$	$0.339 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.094	$0.066 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.393	$0.375 + 0.009 \cdot \text{SL}$	$0.381 + 0.007 \cdot \text{SL}$	$0.388 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.333	$0.313 + 0.010 \cdot \text{SL}$	$0.321 + 0.008 \cdot \text{SL}$	$0.332 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.094	$0.066 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.013 \cdot \text{SL}$	$0.060 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.417	$0.399 + 0.009 \cdot \text{SL}$	$0.405 + 0.007 \cdot \text{SL}$	$0.412 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.315	$0.295 + 0.010 \cdot \text{SL}$	$0.303 + 0.008 \cdot \text{SL}$	$0.314 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## AO221/AO221D2/AO221D4

### Two 2-ANDs into 3-NOR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO221D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.089	$0.075 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.060 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.332	$0.321 + 0.005 \cdot \text{SL}$	$0.327 + 0.004 \cdot \text{SL}$	$0.339 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.280	$0.268 + 0.006 \cdot \text{SL}$	$0.274 + 0.004 \cdot \text{SL}$	$0.288 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.058 + 0.008 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.352	$0.342 + 0.005 \cdot \text{SL}$	$0.347 + 0.004 \cdot \text{SL}$	$0.360 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.272	$0.261 + 0.006 \cdot \text{SL}$	$0.267 + 0.004 \cdot \text{SL}$	$0.281 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.089	$0.075 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.405	$0.394 + 0.005 \cdot \text{SL}$	$0.400 + 0.004 \cdot \text{SL}$	$0.412 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.349	$0.338 + 0.006 \cdot \text{SL}$	$0.343 + 0.004 \cdot \text{SL}$	$0.358 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.090	$0.077 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.428	$0.417 + 0.005 \cdot \text{SL}$	$0.422 + 0.004 \cdot \text{SL}$	$0.435 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.342	$0.331 + 0.006 \cdot \text{SL}$	$0.336 + 0.004 \cdot \text{SL}$	$0.351 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.090	$0.077 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.058 + 0.007 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.453	$0.442 + 0.005 \cdot \text{SL}$	$0.448 + 0.004 \cdot \text{SL}$	$0.460 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.321	$0.310 + 0.006 \cdot \text{SL}$	$0.315 + 0.004 \cdot \text{SL}$	$0.330 + 0.004 \cdot \text{SL}$

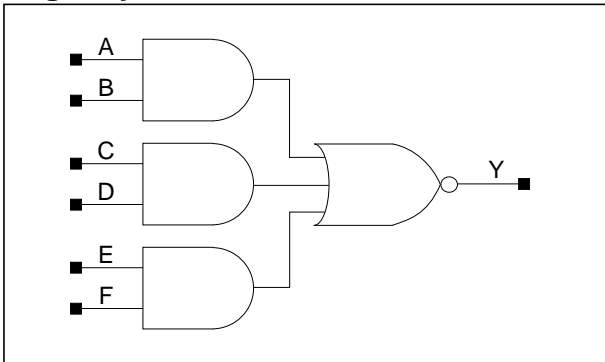
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# AO222/AO222D2/AO222D2B/AO222D4

## Three 2-ANDs into 3-NOR with 1X/2X/2X(Buffered)/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
Other States						1

### Cell Data

Input Load (SL)												Gate Count	
AO222						AO222D2						AO222	AO222D2
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	0.9	1.0	0.9	1.0	1.0	1.8	1.9	1.8	1.9	1.8	2.0	2.33	4.33
AO222D2B						AO222D4						AO222D2B	AO222D4
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	1.0	0.9	1.0	0.9	1.0	0.9	0.9	0.9	1.0	1.0	1.0	3.33	4.00



## AO222/AO222D2/AO222D2B/AO222D4

### Three 2-ANDs into 3-NOR with 1X/2X/2X(Buffered)/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.461	$0.283 + 0.089 \cdot \text{SL}$	$0.275 + 0.091 \cdot \text{SL}$	$0.265 + 0.092 \cdot \text{SL}$
	$t_F$	0.252	$0.158 + 0.047 \cdot \text{SL}$	$0.149 + 0.049 \cdot \text{SL}$	$0.136 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.118 + 0.038 \cdot \text{SL}$	$0.114 + 0.039 \cdot \text{SL}$	$0.114 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.146	$0.097 + 0.025 \cdot \text{SL}$	$0.098 + 0.025 \cdot \text{SL}$	$0.098 + 0.025 \cdot \text{SL}$
B to Y	$t_R$	0.489	$0.311 + 0.089 \cdot \text{SL}$	$0.303 + 0.091 \cdot \text{SL}$	$0.293 + 0.092 \cdot \text{SL}$
	$t_F$	0.247	$0.152 + 0.048 \cdot \text{SL}$	$0.142 + 0.050 \cdot \text{SL}$	$0.134 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.210	$0.133 + 0.038 \cdot \text{SL}$	$0.130 + 0.039 \cdot \text{SL}$	$0.130 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.139	$0.089 + 0.025 \cdot \text{SL}$	$0.091 + 0.025 \cdot \text{SL}$	$0.092 + 0.025 \cdot \text{SL}$
C to Y	$t_R$	0.476	$0.300 + 0.088 \cdot \text{SL}$	$0.293 + 0.090 \cdot \text{SL}$	$0.288 + 0.090 \cdot \text{SL}$
	$t_F$	0.318	$0.222 + 0.048 \cdot \text{SL}$	$0.215 + 0.050 \cdot \text{SL}$	$0.206 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.269	$0.190 + 0.040 \cdot \text{SL}$	$0.192 + 0.039 \cdot \text{SL}$	$0.195 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.207	$0.156 + 0.025 \cdot \text{SL}$	$0.158 + 0.025 \cdot \text{SL}$	$0.160 + 0.025 \cdot \text{SL}$
D to Y	$t_R$	0.506	$0.329 + 0.089 \cdot \text{SL}$	$0.322 + 0.090 \cdot \text{SL}$	$0.318 + 0.091 \cdot \text{SL}$
	$t_F$	0.315	$0.217 + 0.049 \cdot \text{SL}$	$0.213 + 0.050 \cdot \text{SL}$	$0.206 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.287	$0.208 + 0.040 \cdot \text{SL}$	$0.209 + 0.039 \cdot \text{SL}$	$0.211 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.199	$0.148 + 0.026 \cdot \text{SL}$	$0.150 + 0.025 \cdot \text{SL}$	$0.152 + 0.025 \cdot \text{SL}$
E to Y	$t_R$	0.476	$0.300 + 0.088 \cdot \text{SL}$	$0.294 + 0.090 \cdot \text{SL}$	$0.288 + 0.091 \cdot \text{SL}$
	$t_F$	0.379	$0.281 + 0.049 \cdot \text{SL}$	$0.276 + 0.050 \cdot \text{SL}$	$0.267 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.300	$0.220 + 0.040 \cdot \text{SL}$	$0.222 + 0.039 \cdot \text{SL}$	$0.225 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.185 + 0.027 \cdot \text{SL}$	$0.190 + 0.026 \cdot \text{SL}$	$0.196 + 0.025 \cdot \text{SL}$
F to Y	$t_R$	0.505	$0.327 + 0.089 \cdot \text{SL}$	$0.322 + 0.090 \cdot \text{SL}$	$0.317 + 0.091 \cdot \text{SL}$
	$t_F$	0.377	$0.277 + 0.050 \cdot \text{SL}$	$0.275 + 0.050 \cdot \text{SL}$	$0.269 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.319	$0.239 + 0.040 \cdot \text{SL}$	$0.241 + 0.039 \cdot \text{SL}$	$0.242 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.233	$0.179 + 0.027 \cdot \text{SL}$	$0.184 + 0.026 \cdot \text{SL}$	$0.190 + 0.025 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO222/AO222D2/AO222D2B/AO222D4

## Three 2-ANDs into 3-NOR with 1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.379	$0.291 + 0.044 \cdot \text{SL}$	$0.286 + 0.045 \cdot \text{SL}$	$0.274 + 0.046 \cdot \text{SL}$
	$t_F$	0.212	$0.166 + 0.023 \cdot \text{SL}$	$0.161 + 0.024 \cdot \text{SL}$	$0.146 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.166	$0.129 + 0.019 \cdot \text{SL}$	$0.125 + 0.020 \cdot \text{SL}$	$0.124 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.125	$0.100 + 0.013 \cdot \text{SL}$	$0.102 + 0.012 \cdot \text{SL}$	$0.102 + 0.012 \cdot \text{SL}$
B to Y	$t_R$	0.407	$0.319 + 0.044 \cdot \text{SL}$	$0.314 + 0.045 \cdot \text{SL}$	$0.302 + 0.046 \cdot \text{SL}$
	$t_F$	0.206	$0.160 + 0.023 \cdot \text{SL}$	$0.152 + 0.025 \cdot \text{SL}$	$0.143 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.183	$0.145 + 0.019 \cdot \text{SL}$	$0.142 + 0.020 \cdot \text{SL}$	$0.141 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.118	$0.092 + 0.013 \cdot \text{SL}$	$0.095 + 0.012 \cdot \text{SL}$	$0.096 + 0.012 \cdot \text{SL}$
C to Y	$t_R$	0.394	$0.305 + 0.044 \cdot \text{SL}$	$0.301 + 0.045 \cdot \text{SL}$	$0.294 + 0.046 \cdot \text{SL}$
	$t_F$	0.261	$0.214 + 0.024 \cdot \text{SL}$	$0.210 + 0.025 \cdot \text{SL}$	$0.198 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.222	$0.181 + 0.020 \cdot \text{SL}$	$0.182 + 0.020 \cdot \text{SL}$	$0.185 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.175	$0.149 + 0.013 \cdot \text{SL}$	$0.150 + 0.012 \cdot \text{SL}$	$0.152 + 0.012 \cdot \text{SL}$
D to Y	$t_R$	0.419	$0.330 + 0.044 \cdot \text{SL}$	$0.327 + 0.045 \cdot \text{SL}$	$0.319 + 0.046 \cdot \text{SL}$
	$t_F$	0.256	$0.207 + 0.024 \cdot \text{SL}$	$0.205 + 0.025 \cdot \text{SL}$	$0.197 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.240	$0.200 + 0.020 \cdot \text{SL}$	$0.201 + 0.020 \cdot \text{SL}$	$0.202 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.169	$0.143 + 0.013 \cdot \text{SL}$	$0.144 + 0.013 \cdot \text{SL}$	$0.146 + 0.012 \cdot \text{SL}$
E to Y	$t_R$	0.393	$0.304 + 0.044 \cdot \text{SL}$	$0.300 + 0.045 \cdot \text{SL}$	$0.294 + 0.046 \cdot \text{SL}$
	$t_F$	0.325	$0.276 + 0.024 \cdot \text{SL}$	$0.274 + 0.025 \cdot \text{SL}$	$0.264 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.217 + 0.020 \cdot \text{SL}$	$0.218 + 0.020 \cdot \text{SL}$	$0.221 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.209	$0.181 + 0.014 \cdot \text{SL}$	$0.184 + 0.013 \cdot \text{SL}$	$0.191 + 0.013 \cdot \text{SL}$
F to Y	$t_R$	0.417	$0.328 + 0.044 \cdot \text{SL}$	$0.325 + 0.045 \cdot \text{SL}$	$0.319 + 0.046 \cdot \text{SL}$
	$t_F$	0.321	$0.272 + 0.025 \cdot \text{SL}$	$0.270 + 0.025 \cdot \text{SL}$	$0.265 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.276	$0.235 + 0.020 \cdot \text{SL}$	$0.236 + 0.020 \cdot \text{SL}$	$0.238 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.202	$0.175 + 0.014 \cdot \text{SL}$	$0.178 + 0.013 \cdot \text{SL}$	$0.185 + 0.013 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## AO222/AO222D2/AO222D2B/AO222D4

### Three 2-ANDs into 3-NOR with 1X/2X/2X(Buffered)/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO222D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.093	$0.066 + 0.013 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.057 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.318	$0.301 + 0.009 \cdot \text{SL}$	$0.307 + 0.007 \cdot \text{SL}$	$0.314 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.256 + 0.010 \cdot \text{SL}$	$0.264 + 0.008 \cdot \text{SL}$	$0.275 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.094	$0.068 + 0.013 \cdot \text{SL}$	$0.063 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.054 + 0.014 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.339	$0.322 + 0.009 \cdot \text{SL}$	$0.328 + 0.007 \cdot \text{SL}$	$0.335 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.270	$0.250 + 0.010 \cdot \text{SL}$	$0.258 + 0.008 \cdot \text{SL}$	$0.268 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.094	$0.066 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.392	$0.374 + 0.009 \cdot \text{SL}$	$0.381 + 0.007 \cdot \text{SL}$	$0.388 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.344	$0.324 + 0.010 \cdot \text{SL}$	$0.332 + 0.008 \cdot \text{SL}$	$0.342 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.095	$0.067 + 0.014 \cdot \text{SL}$	$0.067 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.414	$0.396 + 0.009 \cdot \text{SL}$	$0.402 + 0.007 \cdot \text{SL}$	$0.410 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.338	$0.317 + 0.010 \cdot \text{SL}$	$0.326 + 0.008 \cdot \text{SL}$	$0.336 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.094	$0.067 + 0.014 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.420	$0.403 + 0.009 \cdot \text{SL}$	$0.409 + 0.007 \cdot \text{SL}$	$0.416 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.382	$0.362 + 0.010 \cdot \text{SL}$	$0.370 + 0.008 \cdot \text{SL}$	$0.381 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.095	$0.068 + 0.013 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.060 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.442	$0.424 + 0.009 \cdot \text{SL}$	$0.430 + 0.007 \cdot \text{SL}$	$0.437 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.375	$0.355 + 0.010 \cdot \text{SL}$	$0.363 + 0.008 \cdot \text{SL}$	$0.374 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# AO222/AO222D2/AO222D2B/AO222D4

## Three 2-ANDs into 3-NOR with 1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO222D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.059 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.356	$0.346 + 0.005 \cdot \text{SL}$	$0.351 + 0.004 \cdot \text{SL}$	$0.363 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.290	$0.279 + 0.006 \cdot \text{SL}$	$0.284 + 0.004 \cdot \text{SL}$	$0.299 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.090	$0.077 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.375	$0.365 + 0.005 \cdot \text{SL}$	$0.370 + 0.004 \cdot \text{SL}$	$0.382 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.282	$0.271 + 0.006 \cdot \text{SL}$	$0.276 + 0.004 \cdot \text{SL}$	$0.291 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.089	$0.075 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.430	$0.420 + 0.005 \cdot \text{SL}$	$0.425 + 0.004 \cdot \text{SL}$	$0.437 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.356	$0.345 + 0.006 \cdot \text{SL}$	$0.351 + 0.004 \cdot \text{SL}$	$0.365 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.452	$0.441 + 0.005 \cdot \text{SL}$	$0.446 + 0.004 \cdot \text{SL}$	$0.459 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.350	$0.338 + 0.006 \cdot \text{SL}$	$0.344 + 0.004 \cdot \text{SL}$	$0.359 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.088	$0.074 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.457	$0.447 + 0.005 \cdot \text{SL}$	$0.452 + 0.004 \cdot \text{SL}$	$0.464 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.394	$0.383 + 0.006 \cdot \text{SL}$	$0.388 + 0.004 \cdot \text{SL}$	$0.403 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.091	$0.077 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.065 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.479	$0.468 + 0.005 \cdot \text{SL}$	$0.474 + 0.004 \cdot \text{SL}$	$0.486 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.387	$0.376 + 0.006 \cdot \text{SL}$	$0.381 + 0.004 \cdot \text{SL}$	$0.396 + 0.004 \cdot \text{SL}$

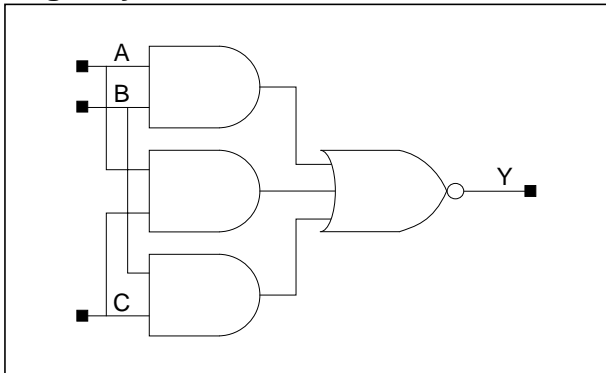
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# AO222A/AO222D2A/AO222D4A

## Inverting 2-of-3 Majority with 1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

### Cell Data

Input Load (SL)									Gate Count		
AO222A			AO222D2A			AO222D4A			AO222A	AO222D2A	AO222D4A
A	B	C	A	B	C	A	B	C			
1.7	1.9	1.9	1.7	2.0	1.9	1.7	1.9	1.9	2.33	3.33	3.67

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO222A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.399	$0.286 + 0.056 \cdot \text{SL}$	$0.278 + 0.058 \cdot \text{SL}$	$0.268 + 0.060 \cdot \text{SL}$
	$t_F$	0.277	$0.182 + 0.048 \cdot \text{SL}$	$0.178 + 0.049 \cdot \text{SL}$	$0.170 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.175	$0.123 + 0.026 \cdot \text{SL}$	$0.123 + 0.026 \cdot \text{SL}$	$0.124 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.142 + 0.024 \cdot \text{SL}$	$0.144 + 0.024 \cdot \text{SL}$	$0.145 + 0.024 \cdot \text{SL}$
B to Y	$t_R$	0.397	$0.282 + 0.057 \cdot \text{SL}$	$0.276 + 0.059 \cdot \text{SL}$	$0.270 + 0.059 \cdot \text{SL}$
	$t_F$	0.291	$0.196 + 0.048 \cdot \text{SL}$	$0.192 + 0.049 \cdot \text{SL}$	$0.184 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.136 + 0.026 \cdot \text{SL}$	$0.136 + 0.026 \cdot \text{SL}$	$0.136 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.213	$0.165 + 0.024 \cdot \text{SL}$	$0.166 + 0.024 \cdot \text{SL}$	$0.167 + 0.024 \cdot \text{SL}$
C to Y	$t_R$	0.368	$0.254 + 0.057 \cdot \text{SL}$	$0.248 + 0.058 \cdot \text{SL}$	$0.241 + 0.059 \cdot \text{SL}$
	$t_F$	0.294	$0.200 + 0.047 \cdot \text{SL}$	$0.195 + 0.049 \cdot \text{SL}$	$0.189 + 0.049 \cdot \text{SL}$
	$t_{PLH}$	0.178	$0.127 + 0.025 \cdot \text{SL}$	$0.127 + 0.026 \cdot \text{SL}$	$0.127 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.189	$0.141 + 0.024 \cdot \text{SL}$	$0.142 + 0.024 \cdot \text{SL}$	$0.143 + 0.024 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO222A/AO222D2A/AO222D4A

## Inverting 2-of-3 Majority with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO222D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.093	$0.065 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.054 + 0.014 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.310	$0.292 + 0.009 \cdot \text{SL}$	$0.299 + 0.007 \cdot \text{SL}$	$0.306 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.326	$0.306 + 0.010 \cdot \text{SL}$	$0.314 + 0.008 \cdot \text{SL}$	$0.324 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.093	$0.066 + 0.014 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.055 + 0.014 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.313	$0.296 + 0.009 \cdot \text{SL}$	$0.302 + 0.007 \cdot \text{SL}$	$0.308 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.350	$0.330 + 0.010 \cdot \text{SL}$	$0.338 + 0.008 \cdot \text{SL}$	$0.348 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.055 + 0.014 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.307	$0.289 + 0.009 \cdot \text{SL}$	$0.296 + 0.007 \cdot \text{SL}$	$0.302 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.325	$0.305 + 0.010 \cdot \text{SL}$	$0.312 + 0.008 \cdot \text{SL}$	$0.323 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### AO222D4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.074 + 0.006 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.059 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.332	$0.322 + 0.005 \cdot \text{SL}$	$0.327 + 0.004 \cdot \text{SL}$	$0.339 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.333	$0.321 + 0.006 \cdot \text{SL}$	$0.327 + 0.004 \cdot \text{SL}$	$0.341 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.086	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.059 + 0.007 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.333	$0.322 + 0.005 \cdot \text{SL}$	$0.328 + 0.004 \cdot \text{SL}$	$0.339 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.356	$0.344 + 0.006 \cdot \text{SL}$	$0.350 + 0.004 \cdot \text{SL}$	$0.364 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.084	$0.070 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.058 + 0.008 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.329	$0.318 + 0.005 \cdot \text{SL}$	$0.324 + 0.004 \cdot \text{SL}$	$0.335 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.332	$0.320 + 0.006 \cdot \text{SL}$	$0.326 + 0.004 \cdot \text{SL}$	$0.340 + 0.004 \cdot \text{SL}$

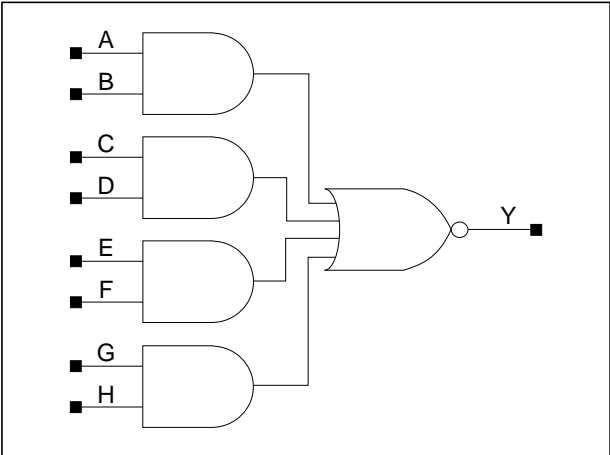
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# AO2222/AO2222D2/AO2222D4

## Four 2-ANDs into 4-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	0
x	x	1	1	x	x	x	x	0
x	x	x	x	1	1	x	x	0
x	x	x	x	x	x	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
AO2222								AO2222
A	B	C	D	E	F	G	H	3.00
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	
AO2222D2								AO2222D2
A	B	C	D	E	F	G	H	4.33
0.9	1.0	0.9	0.9	0.9	0.9	0.9	0.9	
AO2222D4								AO2222D4
A	B	C	D	E	F	G	H	5.00
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	



# AO2222/AO2222D2/AO2222D4

## Four 2-ANDs into 4-NOR with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.644	$0.401 + 0.122 \cdot \text{SL}$	$0.396 + 0.123 \cdot \text{SL}$	$0.389 + 0.124 \cdot \text{SL}$
	$t_F$	0.295	$0.191 + 0.052 \cdot \text{SL}$	$0.180 + 0.055 \cdot \text{SL}$	$0.167 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.215	$0.117 + 0.049 \cdot \text{SL}$	$0.104 + 0.052 \cdot \text{SL}$	$0.104 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.166	$0.112 + 0.027 \cdot \text{SL}$	$0.113 + 0.027 \cdot \text{SL}$	$0.113 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.678	$0.435 + 0.121 \cdot \text{SL}$	$0.429 + 0.123 \cdot \text{SL}$	$0.421 + 0.124 \cdot \text{SL}$
	$t_F$	0.290	$0.183 + 0.054 \cdot \text{SL}$	$0.175 + 0.055 \cdot \text{SL}$	$0.167 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.232	$0.133 + 0.049 \cdot \text{SL}$	$0.123 + 0.052 \cdot \text{SL}$	$0.122 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.159	$0.104 + 0.027 \cdot \text{SL}$	$0.105 + 0.027 \cdot \text{SL}$	$0.105 + 0.027 \cdot \text{SL}$
C to Y	$t_R$	0.699	$0.460 + 0.119 \cdot \text{SL}$	$0.455 + 0.120 \cdot \text{SL}$	$0.452 + 0.121 \cdot \text{SL}$
	$t_F$	0.371	$0.263 + 0.054 \cdot \text{SL}$	$0.257 + 0.055 \cdot \text{SL}$	$0.248 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.227 + 0.054 \cdot \text{SL}$	$0.231 + 0.053 \cdot \text{SL}$	$0.235 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.236	$0.180 + 0.028 \cdot \text{SL}$	$0.182 + 0.027 \cdot \text{SL}$	$0.184 + 0.027 \cdot \text{SL}$
D to Y	$t_R$	0.732	$0.493 + 0.119 \cdot \text{SL}$	$0.488 + 0.121 \cdot \text{SL}$	$0.485 + 0.121 \cdot \text{SL}$
	$t_F$	0.369	$0.259 + 0.055 \cdot \text{SL}$	$0.255 + 0.056 \cdot \text{SL}$	$0.250 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.355	$0.248 + 0.053 \cdot \text{SL}$	$0.251 + 0.053 \cdot \text{SL}$	$0.254 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.228	$0.172 + 0.028 \cdot \text{SL}$	$0.174 + 0.027 \cdot \text{SL}$	$0.177 + 0.027 \cdot \text{SL}$
E to Y	$t_R$	0.738	$0.502 + 0.118 \cdot \text{SL}$	$0.495 + 0.120 \cdot \text{SL}$	$0.489 + 0.121 \cdot \text{SL}$
	$t_F$	0.445	$0.337 + 0.054 \cdot \text{SL}$	$0.331 + 0.055 \cdot \text{SL}$	$0.321 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.426	$0.318 + 0.054 \cdot \text{SL}$	$0.322 + 0.053 \cdot \text{SL}$	$0.326 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.270	$0.212 + 0.029 \cdot \text{SL}$	$0.217 + 0.028 \cdot \text{SL}$	$0.220 + 0.028 \cdot \text{SL}$
F to Y	$t_R$	0.769	$0.532 + 0.119 \cdot \text{SL}$	$0.527 + 0.120 \cdot \text{SL}$	$0.521 + 0.121 \cdot \text{SL}$
	$t_F$	0.443	$0.334 + 0.055 \cdot \text{SL}$	$0.331 + 0.056 \cdot \text{SL}$	$0.324 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.446	$0.340 + 0.053 \cdot \text{SL}$	$0.343 + 0.052 \cdot \text{SL}$	$0.345 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.264	$0.206 + 0.029 \cdot \text{SL}$	$0.211 + 0.028 \cdot \text{SL}$	$0.214 + 0.028 \cdot \text{SL}$
G to Y	$t_R$	0.740	$0.503 + 0.118 \cdot \text{SL}$	$0.496 + 0.120 \cdot \text{SL}$	$0.490 + 0.121 \cdot \text{SL}$
	$t_F$	0.533	$0.423 + 0.055 \cdot \text{SL}$	$0.420 + 0.056 \cdot \text{SL}$	$0.415 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.471	$0.364 + 0.054 \cdot \text{SL}$	$0.367 + 0.053 \cdot \text{SL}$	$0.371 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.298	$0.235 + 0.031 \cdot \text{SL}$	$0.242 + 0.030 \cdot \text{SL}$	$0.252 + 0.028 \cdot \text{SL}$
H to Y	$t_R$	0.770	$0.533 + 0.118 \cdot \text{SL}$	$0.527 + 0.120 \cdot \text{SL}$	$0.521 + 0.121 \cdot \text{SL}$
	$t_F$	0.532	$0.419 + 0.056 \cdot \text{SL}$	$0.419 + 0.056 \cdot \text{SL}$	$0.417 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.491	$0.385 + 0.053 \cdot \text{SL}$	$0.387 + 0.053 \cdot \text{SL}$	$0.390 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.291	$0.228 + 0.032 \cdot \text{SL}$	$0.236 + 0.030 \cdot \text{SL}$	$0.246 + 0.028 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO2222/AO2222D2/AO2222D4

## Four 2-ANDs into 4-NOR with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO2222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.099	$0.071 + 0.014 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.057 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.316 + 0.009 \cdot \text{SL}$	$0.324 + 0.007 \cdot \text{SL}$	$0.332 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.297	$0.277 + 0.010 \cdot \text{SL}$	$0.285 + 0.008 \cdot \text{SL}$	$0.296 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.101	$0.074 + 0.014 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.059 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.358	$0.340 + 0.009 \cdot \text{SL}$	$0.347 + 0.007 \cdot \text{SL}$	$0.356 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.290	$0.270 + 0.010 \cdot \text{SL}$	$0.278 + 0.008 \cdot \text{SL}$	$0.289 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.102	$0.075 + 0.014 \cdot \text{SL}$	$0.075 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.061 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.452	$0.434 + 0.009 \cdot \text{SL}$	$0.442 + 0.007 \cdot \text{SL}$	$0.450 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.378	$0.358 + 0.010 \cdot \text{SL}$	$0.366 + 0.008 \cdot \text{SL}$	$0.377 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.104	$0.077 + 0.014 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.061 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.477	$0.458 + 0.009 \cdot \text{SL}$	$0.466 + 0.007 \cdot \text{SL}$	$0.475 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.370	$0.350 + 0.010 \cdot \text{SL}$	$0.358 + 0.008 \cdot \text{SL}$	$0.369 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.105	$0.080 + 0.013 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.547	$0.528 + 0.009 \cdot \text{SL}$	$0.536 + 0.007 \cdot \text{SL}$	$0.544 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.421	$0.401 + 0.010 \cdot \text{SL}$	$0.409 + 0.008 \cdot \text{SL}$	$0.420 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.106	$0.079 + 0.014 \cdot \text{SL}$	$0.078 + 0.014 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.572	$0.553 + 0.009 \cdot \text{SL}$	$0.561 + 0.007 \cdot \text{SL}$	$0.570 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.415	$0.395 + 0.010 \cdot \text{SL}$	$0.403 + 0.008 \cdot \text{SL}$	$0.414 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.104	$0.076 + 0.014 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.065 + 0.014 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.592	$0.574 + 0.009 \cdot \text{SL}$	$0.582 + 0.007 \cdot \text{SL}$	$0.590 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.459	$0.439 + 0.010 \cdot \text{SL}$	$0.447 + 0.008 \cdot \text{SL}$	$0.458 + 0.007 \cdot \text{SL}$
H to Y	$t_R$	0.106	$0.079 + 0.014 \cdot \text{SL}$	$0.079 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.065 + 0.014 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.616	$0.598 + 0.009 \cdot \text{SL}$	$0.606 + 0.007 \cdot \text{SL}$	$0.615 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.453	$0.432 + 0.010 \cdot \text{SL}$	$0.441 + 0.008 \cdot \text{SL}$	$0.452 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



**AO2222/AO2222D2/AO2222D4****Four 2-ANDs into 4-NOR with 1X/2X/4X Drive****Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AO2222D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.096	$0.083 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.061 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.375	$0.364 + 0.006 \cdot \text{SL}$	$0.371 + 0.004 \cdot \text{SL}$	$0.384 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.303	$0.291 + 0.006 \cdot \text{SL}$	$0.297 + 0.004 \cdot \text{SL}$	$0.312 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.099	$0.087 + 0.006 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.400	$0.389 + 0.006 \cdot \text{SL}$	$0.395 + 0.004 \cdot \text{SL}$	$0.410 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.296	$0.284 + 0.006 \cdot \text{SL}$	$0.290 + 0.004 \cdot \text{SL}$	$0.305 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.099	$0.086 + 0.007 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.497	$0.485 + 0.006 \cdot \text{SL}$	$0.492 + 0.004 \cdot \text{SL}$	$0.506 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.383	$0.371 + 0.006 \cdot \text{SL}$	$0.377 + 0.004 \cdot \text{SL}$	$0.392 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.102	$0.089 + 0.006 \cdot \text{SL}$	$0.087 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.064 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.522	$0.510 + 0.006 \cdot \text{SL}$	$0.517 + 0.004 \cdot \text{SL}$	$0.532 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.375	$0.364 + 0.006 \cdot \text{SL}$	$0.370 + 0.004 \cdot \text{SL}$	$0.384 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.101	$0.088 + 0.006 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_F$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.592	$0.580 + 0.006 \cdot \text{SL}$	$0.587 + 0.004 \cdot \text{SL}$	$0.601 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.427	$0.415 + 0.006 \cdot \text{SL}$	$0.421 + 0.004 \cdot \text{SL}$	$0.436 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.102	$0.090 + 0.006 \cdot \text{SL}$	$0.088 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_F$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.618	$0.606 + 0.006 \cdot \text{SL}$	$0.613 + 0.004 \cdot \text{SL}$	$0.627 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.420	$0.409 + 0.006 \cdot \text{SL}$	$0.415 + 0.004 \cdot \text{SL}$	$0.430 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.101	$0.088 + 0.006 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_F$	0.084	$0.070 + 0.007 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.638	$0.626 + 0.006 \cdot \text{SL}$	$0.633 + 0.004 \cdot \text{SL}$	$0.647 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.464	$0.452 + 0.006 \cdot \text{SL}$	$0.459 + 0.004 \cdot \text{SL}$	$0.474 + 0.004 \cdot \text{SL}$
H to Y	$t_R$	0.103	$0.090 + 0.006 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$
	$t_F$	0.084	$0.071 + 0.007 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.662	$0.651 + 0.006 \cdot \text{SL}$	$0.658 + 0.004 \cdot \text{SL}$	$0.672 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.458	$0.446 + 0.006 \cdot \text{SL}$	$0.452 + 0.004 \cdot \text{SL}$	$0.468 + 0.004 \cdot \text{SL}$

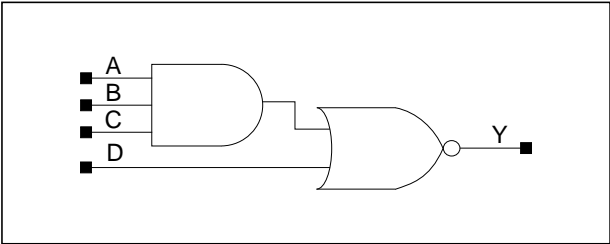
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO31DH/AO31/AO31D2/AO31D4

3-AND into 2-NOR with 0.5X/1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	1	x	0
x	x	x	1	0
Other States				1

Cell Data

Input Load (SL)															
AO31DH				AO31				AO31D2				AO31D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.5	0.5	0.5	1.0	1.0	1.0	1.0	1.9	2.1	2.2	1.9	1.0	1.0	1.0	1.0
Gate Count															
AO31DH				AO31				AO31D2				AO31D4			
1.67				1.67				2.67				3.33			



# AO31DH/AO31/AO31D2/AO31D4

## 3-AND into 2-NOR with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO31DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.450	$0.197 + 0.127 \cdot \text{SL}$	$0.181 + 0.130 \cdot \text{SL}$	$0.177 + 0.131 \cdot \text{SL}$
	$t_F$	0.385	$0.163 + 0.111 \cdot \text{SL}$	$0.148 + 0.115 \cdot \text{SL}$	$0.142 + 0.115 \cdot \text{SL}$
	$t_{PLH}$	0.218	$0.106 + 0.056 \cdot \text{SL}$	$0.105 + 0.056 \cdot \text{SL}$	$0.105 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.214	$0.108 + 0.053 \cdot \text{SL}$	$0.107 + 0.053 \cdot \text{SL}$	$0.107 + 0.053 \cdot \text{SL}$
B to Y	$t_R$	0.483	$0.224 + 0.129 \cdot \text{SL}$	$0.209 + 0.133 \cdot \text{SL}$	$0.205 + 0.134 \cdot \text{SL}$
	$t_F$	0.383	$0.159 + 0.112 \cdot \text{SL}$	$0.150 + 0.114 \cdot \text{SL}$	$0.142 + 0.115 \cdot \text{SL}$
	$t_{PLH}$	0.237	$0.123 + 0.057 \cdot \text{SL}$	$0.122 + 0.057 \cdot \text{SL}$	$0.121 + 0.057 \cdot \text{SL}$
	$t_{PHL}$	0.215	$0.109 + 0.053 \cdot \text{SL}$	$0.109 + 0.053 \cdot \text{SL}$	$0.109 + 0.053 \cdot \text{SL}$
C to Y	$t_R$	0.508	$0.253 + 0.128 \cdot \text{SL}$	$0.236 + 0.132 \cdot \text{SL}$	$0.231 + 0.133 \cdot \text{SL}$
	$t_F$	0.380	$0.154 + 0.113 \cdot \text{SL}$	$0.148 + 0.115 \cdot \text{SL}$	$0.142 + 0.115 \cdot \text{SL}$
	$t_{PLH}$	0.249	$0.136 + 0.057 \cdot \text{SL}$	$0.135 + 0.057 \cdot \text{SL}$	$0.135 + 0.057 \cdot \text{SL}$
	$t_{PHL}$	0.213	$0.106 + 0.053 \cdot \text{SL}$	$0.107 + 0.053 \cdot \text{SL}$	$0.107 + 0.053 \cdot \text{SL}$
D to Y	$t_R$	0.505	$0.246 + 0.130 \cdot \text{SL}$	$0.237 + 0.132 \cdot \text{SL}$	$0.234 + 0.132 \cdot \text{SL}$
	$t_F$	0.237	$0.140 + 0.048 \cdot \text{SL}$	$0.130 + 0.051 \cdot \text{SL}$	$0.117 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.281	$0.166 + 0.057 \cdot \text{SL}$	$0.168 + 0.057 \cdot \text{SL}$	$0.169 + 0.057 \cdot \text{SL}$
	$t_{PHL}$	0.171	$0.116 + 0.027 \cdot \text{SL}$	$0.117 + 0.027 \cdot \text{SL}$	$0.117 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### AO31

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.283	$0.169 + 0.057 \cdot \text{SL}$	$0.160 + 0.059 \cdot \text{SL}$	$0.148 + 0.061 \cdot \text{SL}$
	$t_F$	0.252	$0.145 + 0.053 \cdot \text{SL}$	$0.137 + 0.055 \cdot \text{SL}$	$0.125 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.144	$0.092 + 0.026 \cdot \text{SL}$	$0.092 + 0.026 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.149	$0.097 + 0.026 \cdot \text{SL}$	$0.096 + 0.026 \cdot \text{SL}$	$0.096 + 0.026 \cdot \text{SL}$
B to Y	$t_R$	0.308	$0.194 + 0.057 \cdot \text{SL}$	$0.184 + 0.060 \cdot \text{SL}$	$0.172 + 0.061 \cdot \text{SL}$
	$t_F$	0.249	$0.140 + 0.054 \cdot \text{SL}$	$0.134 + 0.056 \cdot \text{SL}$	$0.126 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.159	$0.107 + 0.026 \cdot \text{SL}$	$0.106 + 0.026 \cdot \text{SL}$	$0.105 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.150	$0.096 + 0.027 \cdot \text{SL}$	$0.097 + 0.026 \cdot \text{SL}$	$0.097 + 0.026 \cdot \text{SL}$
C to Y	$t_R$	0.334	$0.221 + 0.057 \cdot \text{SL}$	$0.210 + 0.059 \cdot \text{SL}$	$0.197 + 0.061 \cdot \text{SL}$
	$t_F$	0.245	$0.135 + 0.055 \cdot \text{SL}$	$0.129 + 0.056 \cdot \text{SL}$	$0.125 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.171	$0.119 + 0.026 \cdot \text{SL}$	$0.118 + 0.026 \cdot \text{SL}$	$0.118 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.146	$0.093 + 0.027 \cdot \text{SL}$	$0.094 + 0.027 \cdot \text{SL}$	$0.094 + 0.026 \cdot \text{SL}$
D to Y	$t_R$	0.325	$0.207 + 0.059 \cdot \text{SL}$	$0.201 + 0.060 \cdot \text{SL}$	$0.195 + 0.061 \cdot \text{SL}$
	$t_F$	0.190	$0.138 + 0.026 \cdot \text{SL}$	$0.135 + 0.027 \cdot \text{SL}$	$0.126 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.193	$0.139 + 0.027 \cdot \text{SL}$	$0.140 + 0.027 \cdot \text{SL}$	$0.141 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.146	$0.115 + 0.015 \cdot \text{SL}$	$0.116 + 0.015 \cdot \text{SL}$	$0.116 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AO31DH/AO31/AO31D2/AO31D4

### 3-AND into 2-NOR with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### AO31D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.216	$0.161 + 0.027 \cdot \text{SL}$	$0.154 + 0.029 \cdot \text{SL}$	$0.139 + 0.030 \cdot \text{SL}$
	$t_F$	0.190	$0.139 + 0.026 \cdot \text{SL}$	$0.132 + 0.027 \cdot \text{SL}$	$0.118 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.110	$0.083 + 0.014 \cdot \text{SL}$	$0.086 + 0.013 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.115	$0.087 + 0.014 \cdot \text{SL}$	$0.090 + 0.013 \cdot \text{SL}$	$0.089 + 0.013 \cdot \text{SL}$
B to Y	$t_R$	0.239	$0.185 + 0.027 \cdot \text{SL}$	$0.179 + 0.029 \cdot \text{SL}$	$0.162 + 0.030 \cdot \text{SL}$
	$t_F$	0.186	$0.135 + 0.026 \cdot \text{SL}$	$0.127 + 0.028 \cdot \text{SL}$	$0.117 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.126	$0.100 + 0.013 \cdot \text{SL}$	$0.101 + 0.013 \cdot \text{SL}$	$0.099 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.116	$0.087 + 0.014 \cdot \text{SL}$	$0.091 + 0.013 \cdot \text{SL}$	$0.091 + 0.013 \cdot \text{SL}$
C to Y	$t_R$	0.265	$0.211 + 0.027 \cdot \text{SL}$	$0.204 + 0.029 \cdot \text{SL}$	$0.187 + 0.030 \cdot \text{SL}$
	$t_F$	0.180	$0.126 + 0.027 \cdot \text{SL}$	$0.122 + 0.028 \cdot \text{SL}$	$0.114 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.139	$0.113 + 0.013 \cdot \text{SL}$	$0.112 + 0.013 \cdot \text{SL}$	$0.112 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.113	$0.084 + 0.014 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$
D to Y	$t_R$	0.253	$0.196 + 0.029 \cdot \text{SL}$	$0.192 + 0.030 \cdot \text{SL}$	$0.184 + 0.030 \cdot \text{SL}$
	$t_F$	0.165	$0.141 + 0.012 \cdot \text{SL}$	$0.136 + 0.013 \cdot \text{SL}$	$0.128 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.163	$0.136 + 0.013 \cdot \text{SL}$	$0.137 + 0.013 \cdot \text{SL}$	$0.139 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.129	$0.114 + 0.008 \cdot \text{SL}$	$0.115 + 0.008 \cdot \text{SL}$	$0.116 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### AO31D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.061 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.280	$0.270 + 0.005 \cdot \text{SL}$	$0.275 + 0.004 \cdot \text{SL}$	$0.286 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.283	$0.272 + 0.005 \cdot \text{SL}$	$0.277 + 0.004 \cdot \text{SL}$	$0.291 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.072	$0.058 + 0.007 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.299	$0.289 + 0.005 \cdot \text{SL}$	$0.294 + 0.004 \cdot \text{SL}$	$0.305 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.283	$0.272 + 0.006 \cdot \text{SL}$	$0.278 + 0.004 \cdot \text{SL}$	$0.292 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.061 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.315	$0.305 + 0.005 \cdot \text{SL}$	$0.310 + 0.004 \cdot \text{SL}$	$0.321 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.280	$0.268 + 0.006 \cdot \text{SL}$	$0.274 + 0.004 \cdot \text{SL}$	$0.288 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.081	$0.067 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.069	$0.054 + 0.007 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$	$0.054 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.336	$0.326 + 0.005 \cdot \text{SL}$	$0.331 + 0.004 \cdot \text{SL}$	$0.341 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.274	$0.263 + 0.006 \cdot \text{SL}$	$0.268 + 0.004 \cdot \text{SL}$	$0.282 + 0.004 \cdot \text{SL}$

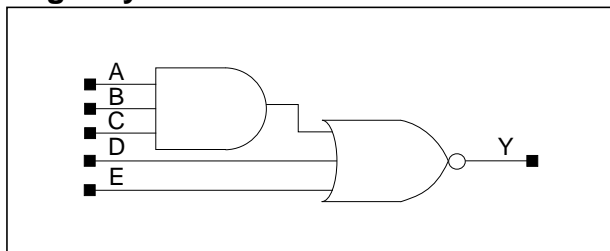
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# AO311/AO311D2/AO311D4

## 3-AND into 3-NOR with 1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	E	Y
1	1	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0
Other States					1

### Cell Data

Input Load (SL)														
AO311					AO311D2					AO311D4				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9
Gate Count														
AO311					AO311D2					AO311D4				
2.00					3.00					3.33				



# AO311/AO311D2/AO311D4

## 3-AND into 3-NOR with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO311

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.437	$0.264 + 0.087 \cdot \text{SL}$	$0.255 + 0.089 \cdot \text{SL}$	$0.244 + 0.090 \cdot \text{SL}$
	$t_F$	0.308	$0.173 + 0.067 \cdot \text{SL}$	$0.165 + 0.069 \cdot \text{SL}$	$0.155 + 0.071 \cdot \text{SL}$
	$t_{PLH}$	0.181	$0.106 + 0.038 \cdot \text{SL}$	$0.103 + 0.038 \cdot \text{SL}$	$0.102 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.182	$0.117 + 0.032 \cdot \text{SL}$	$0.117 + 0.033 \cdot \text{SL}$	$0.116 + 0.033 \cdot \text{SL}$
B to Y	$t_R$	0.468	$0.294 + 0.087 \cdot \text{SL}$	$0.284 + 0.089 \cdot \text{SL}$	$0.273 + 0.091 \cdot \text{SL}$
	$t_F$	0.306	$0.170 + 0.068 \cdot \text{SL}$	$0.164 + 0.070 \cdot \text{SL}$	$0.157 + 0.071 \cdot \text{SL}$
	$t_{PLH}$	0.198	$0.122 + 0.038 \cdot \text{SL}$	$0.120 + 0.039 \cdot \text{SL}$	$0.120 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.184	$0.118 + 0.033 \cdot \text{SL}$	$0.118 + 0.033 \cdot \text{SL}$	$0.119 + 0.033 \cdot \text{SL}$
C to Y	$t_R$	0.498	$0.326 + 0.086 \cdot \text{SL}$	$0.314 + 0.089 \cdot \text{SL}$	$0.302 + 0.091 \cdot \text{SL}$
	$t_F$	0.304	$0.166 + 0.069 \cdot \text{SL}$	$0.161 + 0.070 \cdot \text{SL}$	$0.156 + 0.071 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.137 + 0.038 \cdot \text{SL}$	$0.136 + 0.039 \cdot \text{SL}$	$0.136 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.181	$0.115 + 0.033 \cdot \text{SL}$	$0.115 + 0.033 \cdot \text{SL}$	$0.116 + 0.033 \cdot \text{SL}$
D to Y	$t_R$	0.504	$0.329 + 0.088 \cdot \text{SL}$	$0.322 + 0.089 \cdot \text{SL}$	$0.316 + 0.090 \cdot \text{SL}$
	$t_F$	0.261	$0.181 + 0.040 \cdot \text{SL}$	$0.176 + 0.041 \cdot \text{SL}$	$0.168 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.273	$0.195 + 0.039 \cdot \text{SL}$	$0.196 + 0.039 \cdot \text{SL}$	$0.198 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.202	$0.158 + 0.022 \cdot \text{SL}$	$0.159 + 0.022 \cdot \text{SL}$	$0.159 + 0.022 \cdot \text{SL}$
E to Y	$t_R$	0.502	$0.326 + 0.088 \cdot \text{SL}$	$0.321 + 0.089 \cdot \text{SL}$	$0.316 + 0.090 \cdot \text{SL}$
	$t_F$	0.292	$0.212 + 0.040 \cdot \text{SL}$	$0.208 + 0.041 \cdot \text{SL}$	$0.200 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.280	$0.201 + 0.039 \cdot \text{SL}$	$0.203 + 0.039 \cdot \text{SL}$	$0.205 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.217	$0.171 + 0.023 \cdot \text{SL}$	$0.173 + 0.022 \cdot \text{SL}$	$0.175 + 0.022 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**AO311D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.093	$0.066 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.059 + 0.013 \cdot \text{SL}$	$0.060 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.303	$0.285 + 0.009 \cdot \text{SL}$	$0.292 + 0.007 \cdot \text{SL}$	$0.298 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.306	$0.287 + 0.010 \cdot \text{SL}$	$0.295 + 0.008 \cdot \text{SL}$	$0.305 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.095	$0.068 + 0.013 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.013 \cdot \text{SL}$	$0.060 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.324	$0.307 + 0.009 \cdot \text{SL}$	$0.313 + 0.007 \cdot \text{SL}$	$0.320 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.308	$0.288 + 0.010 \cdot \text{SL}$	$0.296 + 0.008 \cdot \text{SL}$	$0.307 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.096	$0.069 + 0.013 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.059 + 0.013 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.342	$0.325 + 0.009 \cdot \text{SL}$	$0.331 + 0.007 \cdot \text{SL}$	$0.338 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.305	$0.285 + 0.010 \cdot \text{SL}$	$0.293 + 0.008 \cdot \text{SL}$	$0.303 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.096	$0.070 + 0.013 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.014 \cdot \text{SL}$	$0.059 + 0.012 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.400	$0.382 + 0.009 \cdot \text{SL}$	$0.389 + 0.007 \cdot \text{SL}$	$0.396 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.331	$0.312 + 0.010 \cdot \text{SL}$	$0.319 + 0.008 \cdot \text{SL}$	$0.329 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.096	$0.068 + 0.014 \cdot \text{SL}$	$0.068 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.406	$0.389 + 0.009 \cdot \text{SL}$	$0.395 + 0.007 \cdot \text{SL}$	$0.402 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.350	$0.331 + 0.010 \cdot \text{SL}$	$0.339 + 0.008 \cdot \text{SL}$	$0.349 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## AO311/AO311D2/AO311D4

### 3-AND into 3-NOR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

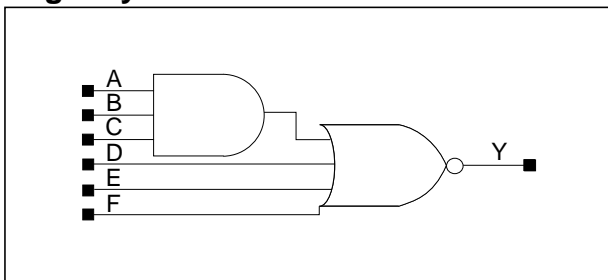
#### AO311D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.074 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$	$0.062 + 0.008 \cdot \text{SL}$
	$t_F$	0.075	$0.060 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.331	$0.321 + 0.005 \cdot \text{SL}$	$0.326 + 0.004 \cdot \text{SL}$	$0.338 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.320	$0.309 + 0.006 \cdot \text{SL}$	$0.315 + 0.004 \cdot \text{SL}$	$0.329 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.088	$0.074 + 0.007 \cdot \text{SL}$	$0.074 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.063 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.353	$0.342 + 0.005 \cdot \text{SL}$	$0.348 + 0.004 \cdot \text{SL}$	$0.360 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.322	$0.311 + 0.006 \cdot \text{SL}$	$0.316 + 0.004 \cdot \text{SL}$	$0.331 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.089	$0.075 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.061 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.371	$0.361 + 0.005 \cdot \text{SL}$	$0.366 + 0.004 \cdot \text{SL}$	$0.378 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.307 + 0.006 \cdot \text{SL}$	$0.313 + 0.004 \cdot \text{SL}$	$0.328 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.089	$0.075 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.071	$0.055 + 0.008 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$	$0.056 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.430	$0.419 + 0.005 \cdot \text{SL}$	$0.425 + 0.004 \cdot \text{SL}$	$0.437 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.340	$0.328 + 0.006 \cdot \text{SL}$	$0.334 + 0.004 \cdot \text{SL}$	$0.348 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.072	$0.057 + 0.008 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.437	$0.426 + 0.005 \cdot \text{SL}$	$0.432 + 0.004 \cdot \text{SL}$	$0.444 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.359	$0.348 + 0.006 \cdot \text{SL}$	$0.354 + 0.004 \cdot \text{SL}$	$0.368 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



### Logic Symbol



### Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0
Other States						1

### Cell Data

Input Load (SL)												Gate Count	
AO3111						AO3111D2						AO3111	AO3111D2
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	0.9	0.9	0.8	0.8	0.9	0.9	0.9	0.9	0.8	0.8	0.9	2.33	3.33



## AO3111/AO3111D2

### 3-AND into 4-NOR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO3111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.597	$0.361 + 0.118 \cdot \text{SL}$	$0.353 + 0.120 \cdot \text{SL}$	$0.346 + 0.121 \cdot \text{SL}$
	$t_F$	0.328	$0.181 + 0.073 \cdot \text{SL}$	$0.174 + 0.075 \cdot \text{SL}$	$0.165 + 0.076 \cdot \text{SL}$
	$t_{PLH}$	0.208	$0.108 + 0.050 \cdot \text{SL}$	$0.102 + 0.051 \cdot \text{SL}$	$0.103 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.194	$0.124 + 0.035 \cdot \text{SL}$	$0.124 + 0.035 \cdot \text{SL}$	$0.124 + 0.035 \cdot \text{SL}$
B to Y	$t_R$	0.634	$0.399 + 0.118 \cdot \text{SL}$	$0.388 + 0.120 \cdot \text{SL}$	$0.382 + 0.121 \cdot \text{SL}$
	$t_F$	0.326	$0.178 + 0.074 \cdot \text{SL}$	$0.174 + 0.075 \cdot \text{SL}$	$0.166 + 0.076 \cdot \text{SL}$
	$t_{PLH}$	0.229	$0.128 + 0.050 \cdot \text{SL}$	$0.125 + 0.051 \cdot \text{SL}$	$0.125 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.196	$0.126 + 0.035 \cdot \text{SL}$	$0.126 + 0.035 \cdot \text{SL}$	$0.126 + 0.035 \cdot \text{SL}$
C to Y	$t_R$	0.671	$0.437 + 0.117 \cdot \text{SL}$	$0.425 + 0.120 \cdot \text{SL}$	$0.418 + 0.121 \cdot \text{SL}$
	$t_F$	0.324	$0.175 + 0.074 \cdot \text{SL}$	$0.171 + 0.075 \cdot \text{SL}$	$0.166 + 0.076 \cdot \text{SL}$
	$t_{PLH}$	0.248	$0.146 + 0.051 \cdot \text{SL}$	$0.144 + 0.051 \cdot \text{SL}$	$0.144 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.193	$0.122 + 0.035 \cdot \text{SL}$	$0.123 + 0.035 \cdot \text{SL}$	$0.123 + 0.035 \cdot \text{SL}$
D to Y	$t_R$	0.698	$0.464 + 0.117 \cdot \text{SL}$	$0.457 + 0.119 \cdot \text{SL}$	$0.452 + 0.119 \cdot \text{SL}$
	$t_F$	0.314	$0.212 + 0.051 \cdot \text{SL}$	$0.208 + 0.052 \cdot \text{SL}$	$0.203 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.344	$0.239 + 0.052 \cdot \text{SL}$	$0.242 + 0.052 \cdot \text{SL}$	$0.244 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.243	$0.188 + 0.028 \cdot \text{SL}$	$0.189 + 0.027 \cdot \text{SL}$	$0.190 + 0.027 \cdot \text{SL}$
E to Y	$t_R$	0.698	$0.465 + 0.117 \cdot \text{SL}$	$0.458 + 0.119 \cdot \text{SL}$	$0.453 + 0.119 \cdot \text{SL}$
	$t_F$	0.352	$0.249 + 0.051 \cdot \text{SL}$	$0.246 + 0.052 \cdot \text{SL}$	$0.241 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.373	$0.268 + 0.052 \cdot \text{SL}$	$0.271 + 0.052 \cdot \text{SL}$	$0.273 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.265	$0.208 + 0.028 \cdot \text{SL}$	$0.211 + 0.028 \cdot \text{SL}$	$0.213 + 0.027 \cdot \text{SL}$
F to Y	$t_R$	0.698	$0.463 + 0.117 \cdot \text{SL}$	$0.457 + 0.119 \cdot \text{SL}$	$0.452 + 0.119 \cdot \text{SL}$
	$t_F$	0.389	$0.286 + 0.051 \cdot \text{SL}$	$0.283 + 0.052 \cdot \text{SL}$	$0.279 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.384	$0.279 + 0.052 \cdot \text{SL}$	$0.281 + 0.052 \cdot \text{SL}$	$0.284 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.280	$0.222 + 0.029 \cdot \text{SL}$	$0.225 + 0.028 \cdot \text{SL}$	$0.230 + 0.028 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## AO3111D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.099	$0.072 + 0.014 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.059 + 0.013 \cdot \text{SL}$	$0.062 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.331	$0.314 + 0.009 \cdot \text{SL}$	$0.320 + 0.007 \cdot \text{SL}$	$0.328 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.300 + 0.010 \cdot \text{SL}$	$0.307 + 0.008 \cdot \text{SL}$	$0.318 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.101	$0.074 + 0.014 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.059 + 0.013 \cdot \text{SL}$	$0.062 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.357	$0.339 + 0.009 \cdot \text{SL}$	$0.346 + 0.007 \cdot \text{SL}$	$0.355 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.321	$0.301 + 0.010 \cdot \text{SL}$	$0.309 + 0.008 \cdot \text{SL}$	$0.320 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.103	$0.075 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.058 + 0.013 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.380	$0.362 + 0.009 \cdot \text{SL}$	$0.369 + 0.007 \cdot \text{SL}$	$0.377 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.317	$0.298 + 0.010 \cdot \text{SL}$	$0.305 + 0.008 \cdot \text{SL}$	$0.316 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.104	$0.076 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.013 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.474	$0.456 + 0.009 \cdot \text{SL}$	$0.463 + 0.007 \cdot \text{SL}$	$0.471 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.376	$0.356 + 0.010 \cdot \text{SL}$	$0.364 + 0.008 \cdot \text{SL}$	$0.374 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.104	$0.076 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.014 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.502	$0.484 + 0.009 \cdot \text{SL}$	$0.491 + 0.007 \cdot \text{SL}$	$0.500 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.402	$0.383 + 0.010 \cdot \text{SL}$	$0.391 + 0.008 \cdot \text{SL}$	$0.401 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.104	$0.076 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.061 + 0.013 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.514	$0.496 + 0.009 \cdot \text{SL}$	$0.503 + 0.007 \cdot \text{SL}$	$0.511 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.423	$0.403 + 0.010 \cdot \text{SL}$	$0.411 + 0.008 \cdot \text{SL}$	$0.421 + 0.007 \cdot \text{SL}$

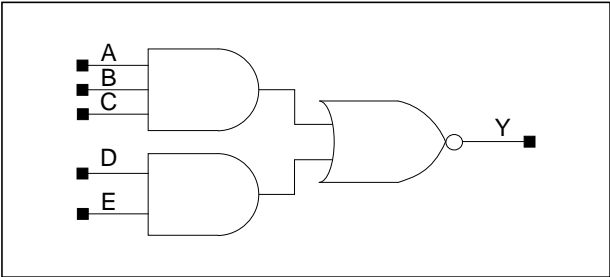
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



AO32/AO32D2/AO32D4

3-AND and 2-AND into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	1	x	x	0
x	x	x	1	1	0
Other States					1

Cell Data

Input Load (SL)														
AO32					AO32D2					AO32D4				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.0	1.0	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
Gate Count														
AO32					AO32D2					AO32D4				
2.00					3.00					3.67				



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**AO32**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.317	$0.200 + 0.058 \cdot \text{SL}$	$0.194 + 0.060 \cdot \text{SL}$	$0.183 + 0.061 \cdot \text{SL}$
	$t_F$	0.268	$0.175 + 0.046 \cdot \text{SL}$	$0.166 + 0.049 \cdot \text{SL}$	$0.155 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.165	$0.113 + 0.026 \cdot \text{SL}$	$0.111 + 0.026 \cdot \text{SL}$	$0.111 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.145	$0.098 + 0.023 \cdot \text{SL}$	$0.099 + 0.023 \cdot \text{SL}$	$0.099 + 0.023 \cdot \text{SL}$
B to Y	$t_R$	0.344	$0.227 + 0.058 \cdot \text{SL}$	$0.220 + 0.060 \cdot \text{SL}$	$0.209 + 0.061 \cdot \text{SL}$
	$t_F$	0.264	$0.170 + 0.047 \cdot \text{SL}$	$0.162 + 0.049 \cdot \text{SL}$	$0.154 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.181	$0.129 + 0.026 \cdot \text{SL}$	$0.128 + 0.026 \cdot \text{SL}$	$0.127 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.146	$0.098 + 0.024 \cdot \text{SL}$	$0.100 + 0.023 \cdot \text{SL}$	$0.100 + 0.023 \cdot \text{SL}$
C to Y	$t_R$	0.372	$0.256 + 0.058 \cdot \text{SL}$	$0.248 + 0.060 \cdot \text{SL}$	$0.236 + 0.061 \cdot \text{SL}$
	$t_F$	0.259	$0.162 + 0.048 \cdot \text{SL}$	$0.156 + 0.050 \cdot \text{SL}$	$0.152 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.195	$0.142 + 0.026 \cdot \text{SL}$	$0.142 + 0.026 \cdot \text{SL}$	$0.142 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.143	$0.095 + 0.024 \cdot \text{SL}$	$0.097 + 0.023 \cdot \text{SL}$	$0.098 + 0.023 \cdot \text{SL}$
D to Y	$t_R$	0.342	$0.223 + 0.059 \cdot \text{SL}$	$0.218 + 0.060 \cdot \text{SL}$	$0.211 + 0.061 \cdot \text{SL}$
	$t_F$	0.243	$0.179 + 0.032 \cdot \text{SL}$	$0.173 + 0.034 \cdot \text{SL}$	$0.165 + 0.035 \cdot \text{SL}$
	$t_{PLH}$	0.213	$0.159 + 0.027 \cdot \text{SL}$	$0.161 + 0.027 \cdot \text{SL}$	$0.162 + 0.027 \cdot \text{SL}$
	$t_{PHL}$	0.166	$0.131 + 0.017 \cdot \text{SL}$	$0.132 + 0.017 \cdot \text{SL}$	$0.133 + 0.017 \cdot \text{SL}$
E to Y	$t_R$	0.367	$0.248 + 0.060 \cdot \text{SL}$	$0.245 + 0.060 \cdot \text{SL}$	$0.238 + 0.061 \cdot \text{SL}$
	$t_F$	0.238	$0.172 + 0.033 \cdot \text{SL}$	$0.167 + 0.034 \cdot \text{SL}$	$0.162 + 0.035 \cdot \text{SL}$
	$t_{PLH}$	0.230	$0.176 + 0.027 \cdot \text{SL}$	$0.177 + 0.027 \cdot \text{SL}$	$0.178 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.158	$0.123 + 0.017 \cdot \text{SL}$	$0.125 + 0.017 \cdot \text{SL}$	$0.126 + 0.017 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AO32/AO32D2/AO32D4

### 3-AND and 2-AND into 2-NOR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO32D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.088	$0.060 + 0.014 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.282	$0.265 + 0.009 \cdot \text{SL}$	$0.271 + 0.007 \cdot \text{SL}$	$0.278 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.276	$0.256 + 0.010 \cdot \text{SL}$	$0.264 + 0.008 \cdot \text{SL}$	$0.274 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.302	$0.285 + 0.009 \cdot \text{SL}$	$0.291 + 0.007 \cdot \text{SL}$	$0.298 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.257 + 0.010 \cdot \text{SL}$	$0.265 + 0.008 \cdot \text{SL}$	$0.275 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.320	$0.303 + 0.009 \cdot \text{SL}$	$0.309 + 0.007 \cdot \text{SL}$	$0.316 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.275	$0.255 + 0.010 \cdot \text{SL}$	$0.263 + 0.008 \cdot \text{SL}$	$0.273 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.088	$0.061 + 0.014 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.053 + 0.014 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.317 + 0.009 \cdot \text{SL}$	$0.323 + 0.007 \cdot \text{SL}$	$0.330 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.303	$0.283 + 0.010 \cdot \text{SL}$	$0.291 + 0.008 \cdot \text{SL}$	$0.301 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.089	$0.062 + 0.013 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.057 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.356	$0.338 + 0.009 \cdot \text{SL}$	$0.344 + 0.007 \cdot \text{SL}$	$0.351 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.296	$0.277 + 0.010 \cdot \text{SL}$	$0.285 + 0.008 \cdot \text{SL}$	$0.295 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

AO32D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.081	$0.067 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$	$0.057 + 0.008 \cdot \text{SL}$
	$t_F$	0.075	$0.061 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.304	$0.293 + 0.005 \cdot \text{SL}$	$0.299 + 0.004 \cdot \text{SL}$	$0.309 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.285	$0.273 + 0.006 \cdot \text{SL}$	$0.279 + 0.004 \cdot \text{SL}$	$0.294 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.058 + 0.008 \cdot \text{SL}$
	$t_F$	0.076	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.324	$0.314 + 0.005 \cdot \text{SL}$	$0.319 + 0.004 \cdot \text{SL}$	$0.330 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.286	$0.275 + 0.006 \cdot \text{SL}$	$0.280 + 0.004 \cdot \text{SL}$	$0.295 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.083	$0.070 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.062 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.342	$0.332 + 0.005 \cdot \text{SL}$	$0.337 + 0.004 \cdot \text{SL}$	$0.348 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.284	$0.272 + 0.006 \cdot \text{SL}$	$0.278 + 0.004 \cdot \text{SL}$	$0.293 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.083	$0.069 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.058 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.357	$0.347 + 0.005 \cdot \text{SL}$	$0.352 + 0.004 \cdot \text{SL}$	$0.363 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.310	$0.298 + 0.006 \cdot \text{SL}$	$0.304 + 0.004 \cdot \text{SL}$	$0.319 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.084	$0.072 + 0.006 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.059 + 0.007 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.368 + 0.005 \cdot \text{SL}$	$0.373 + 0.004 \cdot \text{SL}$	$0.384 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.303	$0.291 + 0.006 \cdot \text{SL}$	$0.297 + 0.004 \cdot \text{SL}$	$0.312 + 0.004 \cdot \text{SL}$

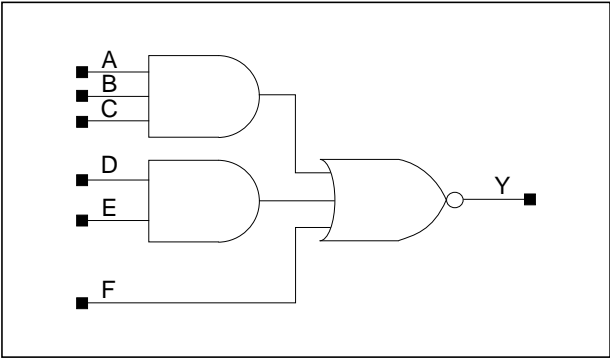
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO321/AO321D2/AO321D4

3-AND and 2-AND into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	x	0
x	x	x	x	x	1	0
Other States						1

Cell Data

Input Load (SL)																	
AO321						AO321D2						AO321D4					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
1.0	1.0	1.0	0.9	0.9	0.9	1.0	1.0	1.0	0.9	0.9	0.9	1.0	1.0	1.0	0.9	0.9	0.9
Gate Count																	
AO321						AO321D2						AO321D4					
2.67						3.33						4.00					



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AO321**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.497	$0.317 + 0.090 \cdot \text{SL}$	$0.310 + 0.092 \cdot \text{SL}$	$0.302 + 0.093 \cdot \text{SL}$
	$t_F$	0.316	$0.198 + 0.059 \cdot \text{SL}$	$0.189 + 0.061 \cdot \text{SL}$	$0.178 + 0.063 \cdot \text{SL}$
	$t_{PLH}$	0.200	$0.123 + 0.038 \cdot \text{SL}$	$0.119 + 0.039 \cdot \text{SL}$	$0.119 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.118 + 0.029 \cdot \text{SL}$	$0.118 + 0.029 \cdot \text{SL}$	$0.118 + 0.029 \cdot \text{SL}$
B to Y	$t_R$	0.530	$0.350 + 0.090 \cdot \text{SL}$	$0.342 + 0.092 \cdot \text{SL}$	$0.334 + 0.093 \cdot \text{SL}$
	$t_F$	0.313	$0.193 + 0.060 \cdot \text{SL}$	$0.187 + 0.062 \cdot \text{SL}$	$0.180 + 0.062 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.142 + 0.039 \cdot \text{SL}$	$0.139 + 0.039 \cdot \text{SL}$	$0.139 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.178	$0.119 + 0.029 \cdot \text{SL}$	$0.119 + 0.029 \cdot \text{SL}$	$0.121 + 0.029 \cdot \text{SL}$
C to Y	$t_R$	0.564	$0.385 + 0.089 \cdot \text{SL}$	$0.376 + 0.092 \cdot \text{SL}$	$0.367 + 0.093 \cdot \text{SL}$
	$t_F$	0.310	$0.189 + 0.061 \cdot \text{SL}$	$0.184 + 0.062 \cdot \text{SL}$	$0.178 + 0.063 \cdot \text{SL}$
	$t_{PLH}$	0.236	$0.158 + 0.039 \cdot \text{SL}$	$0.157 + 0.039 \cdot \text{SL}$	$0.157 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.174	$0.115 + 0.029 \cdot \text{SL}$	$0.116 + 0.029 \cdot \text{SL}$	$0.117 + 0.029 \cdot \text{SL}$
D to Y	$t_R$	0.551	$0.372 + 0.089 \cdot \text{SL}$	$0.367 + 0.090 \cdot \text{SL}$	$0.361 + 0.091 \cdot \text{SL}$
	$t_F$	0.328	$0.233 + 0.047 \cdot \text{SL}$	$0.229 + 0.048 \cdot \text{SL}$	$0.221 + 0.049 \cdot \text{SL}$
	$t_{PLH}$	0.303	$0.222 + 0.040 \cdot \text{SL}$	$0.224 + 0.040 \cdot \text{SL}$	$0.227 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.226	$0.177 + 0.024 \cdot \text{SL}$	$0.178 + 0.024 \cdot \text{SL}$	$0.180 + 0.024 \cdot \text{SL}$
E to Y	$t_R$	0.581	$0.402 + 0.090 \cdot \text{SL}$	$0.397 + 0.091 \cdot \text{SL}$	$0.392 + 0.092 \cdot \text{SL}$
	$t_F$	0.325	$0.229 + 0.048 \cdot \text{SL}$	$0.227 + 0.049 \cdot \text{SL}$	$0.221 + 0.049 \cdot \text{SL}$
	$t_{PLH}$	0.322	$0.242 + 0.040 \cdot \text{SL}$	$0.243 + 0.040 \cdot \text{SL}$	$0.245 + 0.040 \cdot \text{SL}$
	$t_{PHL}$	0.219	$0.170 + 0.024 \cdot \text{SL}$	$0.172 + 0.024 \cdot \text{SL}$	$0.173 + 0.024 \cdot \text{SL}$
F to Y	$t_R$	0.580	$0.401 + 0.090 \cdot \text{SL}$	$0.396 + 0.091 \cdot \text{SL}$	$0.392 + 0.092 \cdot \text{SL}$
	$t_F$	0.300	$0.238 + 0.031 \cdot \text{SL}$	$0.233 + 0.032 \cdot \text{SL}$	$0.225 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.347	$0.266 + 0.040 \cdot \text{SL}$	$0.268 + 0.040 \cdot \text{SL}$	$0.270 + 0.040 \cdot \text{SL}$
	$t_{PHL}$	0.194	$0.157 + 0.019 \cdot \text{SL}$	$0.159 + 0.018 \cdot \text{SL}$	$0.163 + 0.018 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AO321/AO321D2/AO321D4

### 3-AND and 2-AND into 3-NOR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO321D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.094	$0.066 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.054 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.325	$0.307 + 0.009 \cdot \text{SL}$	$0.313 + 0.007 \cdot \text{SL}$	$0.321 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.311	$0.290 + 0.010 \cdot \text{SL}$	$0.299 + 0.008 \cdot \text{SL}$	$0.310 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.096	$0.070 + 0.013 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.349	$0.331 + 0.009 \cdot \text{SL}$	$0.338 + 0.007 \cdot \text{SL}$	$0.345 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.312	$0.292 + 0.010 \cdot \text{SL}$	$0.300 + 0.008 \cdot \text{SL}$	$0.311 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.070 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.370	$0.352 + 0.009 \cdot \text{SL}$	$0.359 + 0.007 \cdot \text{SL}$	$0.367 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.309	$0.289 + 0.010 \cdot \text{SL}$	$0.297 + 0.008 \cdot \text{SL}$	$0.308 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.097	$0.069 + 0.014 \cdot \text{SL}$	$0.069 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.057 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.431	$0.413 + 0.009 \cdot \text{SL}$	$0.419 + 0.007 \cdot \text{SL}$	$0.427 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.368	$0.347 + 0.010 \cdot \text{SL}$	$0.356 + 0.008 \cdot \text{SL}$	$0.366 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.454	$0.436 + 0.009 \cdot \text{SL}$	$0.443 + 0.007 \cdot \text{SL}$	$0.450 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.361	$0.341 + 0.010 \cdot \text{SL}$	$0.349 + 0.008 \cdot \text{SL}$	$0.360 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.054 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.478	$0.460 + 0.009 \cdot \text{SL}$	$0.467 + 0.007 \cdot \text{SL}$	$0.474 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.338	$0.318 + 0.010 \cdot \text{SL}$	$0.326 + 0.008 \cdot \text{SL}$	$0.337 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AO321D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.062 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.358	$0.347 + 0.005 \cdot \text{SL}$	$0.353 + 0.004 \cdot \text{SL}$	$0.365 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.320	$0.308 + 0.006 \cdot \text{SL}$	$0.314 + 0.004 \cdot \text{SL}$	$0.329 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.091	$0.078 + 0.006 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.062 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.383	$0.372 + 0.005 \cdot \text{SL}$	$0.378 + 0.004 \cdot \text{SL}$	$0.390 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.321	$0.310 + 0.006 \cdot \text{SL}$	$0.315 + 0.004 \cdot \text{SL}$	$0.330 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.092	$0.079 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.405	$0.395 + 0.005 \cdot \text{SL}$	$0.400 + 0.004 \cdot \text{SL}$	$0.413 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.318	$0.307 + 0.006 \cdot \text{SL}$	$0.312 + 0.004 \cdot \text{SL}$	$0.327 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.091	$0.078 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.059 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.466	$0.455 + 0.005 \cdot \text{SL}$	$0.461 + 0.004 \cdot \text{SL}$	$0.473 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.374	$0.363 + 0.006 \cdot \text{SL}$	$0.368 + 0.004 \cdot \text{SL}$	$0.383 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.093	$0.080 + 0.007 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.490	$0.479 + 0.005 \cdot \text{SL}$	$0.485 + 0.004 \cdot \text{SL}$	$0.497 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.368	$0.356 + 0.006 \cdot \text{SL}$	$0.362 + 0.004 \cdot \text{SL}$	$0.376 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.093	$0.079 + 0.007 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.059 + 0.007 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.514	$0.503 + 0.005 \cdot \text{SL}$	$0.509 + 0.004 \cdot \text{SL}$	$0.521 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.342	$0.330 + 0.006 \cdot \text{SL}$	$0.336 + 0.004 \cdot \text{SL}$	$0.350 + 0.004 \cdot \text{SL}$

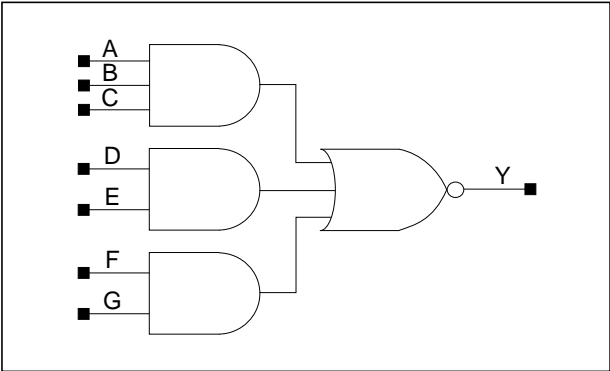
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO322/AO322D2/AO322D4

3-AND and Two 2-ANDs into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	x	x	x	x	0
x	x	x	1	1	x	x	0
x	x	x	x	x	1	1	0
Other States							1

Cell Data

Input Load (SL)							Gate Count
AO322							AO322
A	B	C	D	E	F	G	2.67
1.0	1.0	1.0	1.0	1.1	1.0	1.0	
AO322D2							AO322D2
A	B	C	D	E	F	G	3.67
1.0	1.0	1.0	1.0	1.2	1.0	1.0	
AO322D4							AO322D4
A	B	C	D	E	F	G	4.33
1.0	1.0	1.0	1.0	1.2	1.0	1.0	



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## AO322

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.544	$0.363 + 0.090 \cdot \text{SL}$	$0.358 + 0.092 \cdot \text{SL}$	$0.351 + 0.092 \cdot \text{SL}$
	$t_F$	0.328	$0.224 + 0.052 \cdot \text{SL}$	$0.216 + 0.054 \cdot \text{SL}$	$0.204 + 0.055 \cdot \text{SL}$
	$t_{PLH}$	0.233	$0.155 + 0.039 \cdot \text{SL}$	$0.154 + 0.039 \cdot \text{SL}$	$0.154 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.172	$0.120 + 0.026 \cdot \text{SL}$	$0.121 + 0.026 \cdot \text{SL}$	$0.121 + 0.026 \cdot \text{SL}$
B to Y	$t_R$	0.579	$0.398 + 0.090 \cdot \text{SL}$	$0.393 + 0.092 \cdot \text{SL}$	$0.386 + 0.092 \cdot \text{SL}$
	$t_F$	0.324	$0.218 + 0.053 \cdot \text{SL}$	$0.212 + 0.055 \cdot \text{SL}$	$0.206 + 0.055 \cdot \text{SL}$
	$t_{PLH}$	0.254	$0.176 + 0.039 \cdot \text{SL}$	$0.175 + 0.039 \cdot \text{SL}$	$0.175 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.173	$0.121 + 0.026 \cdot \text{SL}$	$0.121 + 0.026 \cdot \text{SL}$	$0.122 + 0.026 \cdot \text{SL}$
C to Y	$t_R$	0.614	$0.435 + 0.090 \cdot \text{SL}$	$0.429 + 0.091 \cdot \text{SL}$	$0.422 + 0.092 \cdot \text{SL}$
	$t_F$	0.321	$0.214 + 0.054 \cdot \text{SL}$	$0.209 + 0.055 \cdot \text{SL}$	$0.204 + 0.055 \cdot \text{SL}$
	$t_{PLH}$	0.273	$0.195 + 0.039 \cdot \text{SL}$	$0.195 + 0.039 \cdot \text{SL}$	$0.195 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.169	$0.117 + 0.026 \cdot \text{SL}$	$0.118 + 0.026 \cdot \text{SL}$	$0.119 + 0.026 \cdot \text{SL}$
D to Y	$t_R$	0.601	$0.422 + 0.089 \cdot \text{SL}$	$0.418 + 0.090 \cdot \text{SL}$	$0.413 + 0.091 \cdot \text{SL}$
	$t_F$	0.330	$0.252 + 0.039 \cdot \text{SL}$	$0.246 + 0.040 \cdot \text{SL}$	$0.237 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.337	$0.257 + 0.040 \cdot \text{SL}$	$0.259 + 0.040 \cdot \text{SL}$	$0.262 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.201	$0.159 + 0.021 \cdot \text{SL}$	$0.161 + 0.020 \cdot \text{SL}$	$0.162 + 0.020 \cdot \text{SL}$
E to Y	$t_R$	0.632	$0.453 + 0.090 \cdot \text{SL}$	$0.449 + 0.090 \cdot \text{SL}$	$0.446 + 0.091 \cdot \text{SL}$
	$t_F$	0.325	$0.245 + 0.040 \cdot \text{SL}$	$0.241 + 0.041 \cdot \text{SL}$	$0.236 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.360	$0.280 + 0.040 \cdot \text{SL}$	$0.282 + 0.039 \cdot \text{SL}$	$0.284 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.195	$0.153 + 0.021 \cdot \text{SL}$	$0.155 + 0.020 \cdot \text{SL}$	$0.156 + 0.020 \cdot \text{SL}$
F to Y	$t_R$	0.602	$0.423 + 0.090 \cdot \text{SL}$	$0.419 + 0.091 \cdot \text{SL}$	$0.415 + 0.091 \cdot \text{SL}$
	$t_F$	0.387	$0.308 + 0.039 \cdot \text{SL}$	$0.304 + 0.040 \cdot \text{SL}$	$0.294 + 0.041 \cdot \text{SL}$
	$t_{PLH}$	0.369	$0.288 + 0.040 \cdot \text{SL}$	$0.290 + 0.040 \cdot \text{SL}$	$0.293 + 0.040 \cdot \text{SL}$
	$t_{PHL}$	0.224	$0.181 + 0.022 \cdot \text{SL}$	$0.183 + 0.021 \cdot \text{SL}$	$0.187 + 0.021 \cdot \text{SL}$
G to Y	$t_R$	0.632	$0.453 + 0.090 \cdot \text{SL}$	$0.449 + 0.090 \cdot \text{SL}$	$0.446 + 0.091 \cdot \text{SL}$
	$t_F$	0.382	$0.302 + 0.040 \cdot \text{SL}$	$0.299 + 0.041 \cdot \text{SL}$	$0.293 + 0.042 \cdot \text{SL}$
	$t_{PLH}$	0.389	$0.309 + 0.040 \cdot \text{SL}$	$0.311 + 0.039 \cdot \text{SL}$	$0.313 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.217	$0.174 + 0.022 \cdot \text{SL}$	$0.177 + 0.021 \cdot \text{SL}$	$0.180 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO322/AO322D2/AO322D4

## 3-AND and Two 2-ANDs into 3-NOR with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO322D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.061 + 0.013 \cdot \text{SL}$	$0.062 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.367	$0.349 + 0.009 \cdot \text{SL}$	$0.356 + 0.007 \cdot \text{SL}$	$0.363 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.313	$0.293 + 0.010 \cdot \text{SL}$	$0.301 + 0.008 \cdot \text{SL}$	$0.312 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.100	$0.072 + 0.014 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.060 + 0.013 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.392	$0.374 + 0.009 \cdot \text{SL}$	$0.381 + 0.007 \cdot \text{SL}$	$0.389 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.313	$0.293 + 0.010 \cdot \text{SL}$	$0.301 + 0.008 \cdot \text{SL}$	$0.312 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.060 + 0.013 \cdot \text{SL}$	$0.064 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.415	$0.397 + 0.009 \cdot \text{SL}$	$0.404 + 0.007 \cdot \text{SL}$	$0.412 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.309	$0.290 + 0.010 \cdot \text{SL}$	$0.298 + 0.008 \cdot \text{SL}$	$0.309 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.100	$0.073 + 0.014 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.058 + 0.013 \cdot \text{SL}$	$0.063 + 0.012 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.478	$0.460 + 0.009 \cdot \text{SL}$	$0.467 + 0.007 \cdot \text{SL}$	$0.474 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.348	$0.329 + 0.010 \cdot \text{SL}$	$0.337 + 0.008 \cdot \text{SL}$	$0.348 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.102	$0.076 + 0.013 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.058 + 0.013 \cdot \text{SL}$	$0.063 + 0.012 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.503	$0.484 + 0.009 \cdot \text{SL}$	$0.491 + 0.007 \cdot \text{SL}$	$0.499 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.343	$0.323 + 0.010 \cdot \text{SL}$	$0.331 + 0.008 \cdot \text{SL}$	$0.342 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.100	$0.072 + 0.014 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.062 + 0.013 \cdot \text{SL}$	$0.063 + 0.012 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.505	$0.487 + 0.009 \cdot \text{SL}$	$0.494 + 0.007 \cdot \text{SL}$	$0.501 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.378	$0.358 + 0.010 \cdot \text{SL}$	$0.366 + 0.008 \cdot \text{SL}$	$0.377 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.102	$0.075 + 0.013 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.062 + 0.013 \cdot \text{SL}$	$0.064 + 0.012 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.529	$0.511 + 0.009 \cdot \text{SL}$	$0.518 + 0.007 \cdot \text{SL}$	$0.526 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.371	$0.351 + 0.010 \cdot \text{SL}$	$0.359 + 0.008 \cdot \text{SL}$	$0.370 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## 3-AND and Two 2-ANDs into 3-NOR with 1X/2X/4X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## AO322D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.092	$0.078 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.400	$0.390 + 0.005 \cdot \text{SL}$	$0.395 + 0.004 \cdot \text{SL}$	$0.408 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.322	$0.310 + 0.006 \cdot \text{SL}$	$0.316 + 0.004 \cdot \text{SL}$	$0.331 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.093	$0.080 + 0.007 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.426	$0.416 + 0.005 \cdot \text{SL}$	$0.421 + 0.004 \cdot \text{SL}$	$0.434 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.322	$0.311 + 0.006 \cdot \text{SL}$	$0.317 + 0.004 \cdot \text{SL}$	$0.332 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.096	$0.083 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.064 + 0.006 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.450	$0.439 + 0.005 \cdot \text{SL}$	$0.445 + 0.004 \cdot \text{SL}$	$0.458 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.307 + 0.006 \cdot \text{SL}$	$0.313 + 0.004 \cdot \text{SL}$	$0.328 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.094	$0.081 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.509	$0.498 + 0.005 \cdot \text{SL}$	$0.504 + 0.004 \cdot \text{SL}$	$0.517 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.355	$0.344 + 0.006 \cdot \text{SL}$	$0.349 + 0.004 \cdot \text{SL}$	$0.364 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.096	$0.083 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.538	$0.527 + 0.005 \cdot \text{SL}$	$0.534 + 0.004 \cdot \text{SL}$	$0.546 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.350	$0.339 + 0.006 \cdot \text{SL}$	$0.344 + 0.004 \cdot \text{SL}$	$0.359 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.094	$0.081 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.541	$0.530 + 0.005 \cdot \text{SL}$	$0.536 + 0.004 \cdot \text{SL}$	$0.548 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.385	$0.374 + 0.006 \cdot \text{SL}$	$0.380 + 0.004 \cdot \text{SL}$	$0.394 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.096	$0.083 + 0.006 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.565	$0.554 + 0.006 \cdot \text{SL}$	$0.561 + 0.004 \cdot \text{SL}$	$0.573 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.378	$0.367 + 0.006 \cdot \text{SL}$	$0.373 + 0.004 \cdot \text{SL}$	$0.388 + 0.004 \cdot \text{SL}$

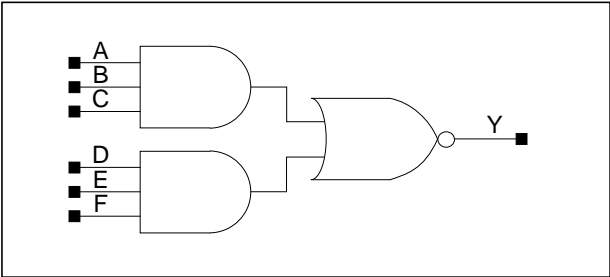
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO33/AO33D2/AO33D4

Two 3-ANDs into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
Other States						1

Cell Data

Input Load (SL)																	
AO33						AO33D2						AO33D4					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.2
Gate Count																	
AO33						AO33D2						AO33D4					
2.33						3.00						3.67					



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AO33**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.350	$0.233 + 0.059 \cdot \text{SL}$	$0.226 + 0.060 \cdot \text{SL}$	$0.217 + 0.061 \cdot \text{SL}$
	$t_F$	0.287	$0.204 + 0.041 \cdot \text{SL}$	$0.195 + 0.044 \cdot \text{SL}$	$0.183 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.185	$0.132 + 0.027 \cdot \text{SL}$	$0.133 + 0.026 \cdot \text{SL}$	$0.133 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.136	$0.093 + 0.022 \cdot \text{SL}$	$0.094 + 0.022 \cdot \text{SL}$	$0.095 + 0.021 \cdot \text{SL}$
B to Y	$t_R$	0.378	$0.260 + 0.059 \cdot \text{SL}$	$0.254 + 0.060 \cdot \text{SL}$	$0.246 + 0.061 \cdot \text{SL}$
	$t_F$	0.282	$0.198 + 0.042 \cdot \text{SL}$	$0.190 + 0.044 \cdot \text{SL}$	$0.181 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.204	$0.152 + 0.026 \cdot \text{SL}$	$0.152 + 0.026 \cdot \text{SL}$	$0.152 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.138	$0.094 + 0.022 \cdot \text{SL}$	$0.096 + 0.022 \cdot \text{SL}$	$0.098 + 0.021 \cdot \text{SL}$
C to Y	$t_R$	0.408	$0.291 + 0.059 \cdot \text{SL}$	$0.284 + 0.060 \cdot \text{SL}$	$0.276 + 0.061 \cdot \text{SL}$
	$t_F$	0.276	$0.190 + 0.043 \cdot \text{SL}$	$0.184 + 0.045 \cdot \text{SL}$	$0.178 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.221	$0.168 + 0.026 \cdot \text{SL}$	$0.168 + 0.026 \cdot \text{SL}$	$0.168 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.135	$0.090 + 0.022 \cdot \text{SL}$	$0.092 + 0.022 \cdot \text{SL}$	$0.095 + 0.021 \cdot \text{SL}$
D to Y	$t_R$	0.349	$0.230 + 0.059 \cdot \text{SL}$	$0.225 + 0.061 \cdot \text{SL}$	$0.219 + 0.061 \cdot \text{SL}$
	$t_F$	0.314	$0.228 + 0.043 \cdot \text{SL}$	$0.223 + 0.044 \cdot \text{SL}$	$0.214 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.222	$0.167 + 0.027 \cdot \text{SL}$	$0.169 + 0.027 \cdot \text{SL}$	$0.171 + 0.027 \cdot \text{SL}$
	$t_{PHL}$	0.196	$0.153 + 0.022 \cdot \text{SL}$	$0.154 + 0.021 \cdot \text{SL}$	$0.155 + 0.021 \cdot \text{SL}$
E to Y	$t_R$	0.378	$0.259 + 0.060 \cdot \text{SL}$	$0.255 + 0.061 \cdot \text{SL}$	$0.250 + 0.061 \cdot \text{SL}$
	$t_F$	0.312	$0.224 + 0.044 \cdot \text{SL}$	$0.220 + 0.045 \cdot \text{SL}$	$0.215 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.242	$0.188 + 0.027 \cdot \text{SL}$	$0.189 + 0.027 \cdot \text{SL}$	$0.191 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.199	$0.156 + 0.022 \cdot \text{SL}$	$0.157 + 0.021 \cdot \text{SL}$	$0.158 + 0.021 \cdot \text{SL}$
F to Y	$t_R$	0.407	$0.288 + 0.060 \cdot \text{SL}$	$0.284 + 0.061 \cdot \text{SL}$	$0.279 + 0.061 \cdot \text{SL}$
	$t_F$	0.309	$0.220 + 0.044 \cdot \text{SL}$	$0.217 + 0.045 \cdot \text{SL}$	$0.213 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.205 + 0.027 \cdot \text{SL}$	$0.206 + 0.027 \cdot \text{SL}$	$0.207 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.196	$0.152 + 0.022 \cdot \text{SL}$	$0.154 + 0.021 \cdot \text{SL}$	$0.155 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AO33/AO33D2/AO33D4

### Two 3-ANDs into 2-NOR with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO33D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.090	$0.061 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.058 + 0.014 \cdot \text{SL}$	$0.064 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.316	$0.299 + 0.009 \cdot \text{SL}$	$0.305 + 0.007 \cdot \text{SL}$	$0.311 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.286	$0.266 + 0.010 \cdot \text{SL}$	$0.274 + 0.008 \cdot \text{SL}$	$0.285 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.060 + 0.013 \cdot \text{SL}$	$0.062 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.340	$0.322 + 0.009 \cdot \text{SL}$	$0.328 + 0.007 \cdot \text{SL}$	$0.335 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.287	$0.267 + 0.010 \cdot \text{SL}$	$0.275 + 0.008 \cdot \text{SL}$	$0.286 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.092	$0.065 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.059 + 0.013 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.359	$0.341 + 0.009 \cdot \text{SL}$	$0.347 + 0.007 \cdot \text{SL}$	$0.354 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.285	$0.265 + 0.010 \cdot \text{SL}$	$0.273 + 0.008 \cdot \text{SL}$	$0.284 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.090	$0.063 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.013 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.354	$0.336 + 0.009 \cdot \text{SL}$	$0.342 + 0.007 \cdot \text{SL}$	$0.349 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.350	$0.330 + 0.010 \cdot \text{SL}$	$0.338 + 0.008 \cdot \text{SL}$	$0.349 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.091	$0.064 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.063 + 0.012 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.375	$0.358 + 0.009 \cdot \text{SL}$	$0.364 + 0.007 \cdot \text{SL}$	$0.370 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.353	$0.333 + 0.010 \cdot \text{SL}$	$0.341 + 0.008 \cdot \text{SL}$	$0.352 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.092	$0.065 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.014 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.397	$0.380 + 0.009 \cdot \text{SL}$	$0.386 + 0.007 \cdot \text{SL}$	$0.392 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.349	$0.330 + 0.010 \cdot \text{SL}$	$0.338 + 0.008 \cdot \text{SL}$	$0.349 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## AO33D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.061 + 0.008 \cdot \text{SL}$
	$t_F$	0.077	$0.064 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.340	$0.330 + 0.005 \cdot \text{SL}$	$0.335 + 0.004 \cdot \text{SL}$	$0.346 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.277 + 0.006 \cdot \text{SL}$	$0.283 + 0.004 \cdot \text{SL}$	$0.298 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.086	$0.072 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.062 + 0.008 \cdot \text{SL}$
	$t_F$	0.077	$0.064 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.364	$0.354 + 0.005 \cdot \text{SL}$	$0.359 + 0.004 \cdot \text{SL}$	$0.370 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.278 + 0.006 \cdot \text{SL}$	$0.284 + 0.004 \cdot \text{SL}$	$0.298 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.063 + 0.008 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.383	$0.373 + 0.005 \cdot \text{SL}$	$0.378 + 0.004 \cdot \text{SL}$	$0.390 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.287	$0.276 + 0.006 \cdot \text{SL}$	$0.281 + 0.004 \cdot \text{SL}$	$0.296 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.085	$0.072 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.061 + 0.008 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.377	$0.367 + 0.005 \cdot \text{SL}$	$0.372 + 0.004 \cdot \text{SL}$	$0.384 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.348	$0.337 + 0.006 \cdot \text{SL}$	$0.342 + 0.004 \cdot \text{SL}$	$0.357 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.087	$0.074 + 0.006 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.061 + 0.008 \cdot \text{SL}$
	$t_F$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.399	$0.389 + 0.005 \cdot \text{SL}$	$0.394 + 0.004 \cdot \text{SL}$	$0.406 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.350	$0.339 + 0.006 \cdot \text{SL}$	$0.344 + 0.004 \cdot \text{SL}$	$0.359 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.063 + 0.008 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.423	$0.412 + 0.005 \cdot \text{SL}$	$0.418 + 0.004 \cdot \text{SL}$	$0.429 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.347	$0.336 + 0.006 \cdot \text{SL}$	$0.341 + 0.004 \cdot \text{SL}$	$0.356 + 0.004 \cdot \text{SL}$

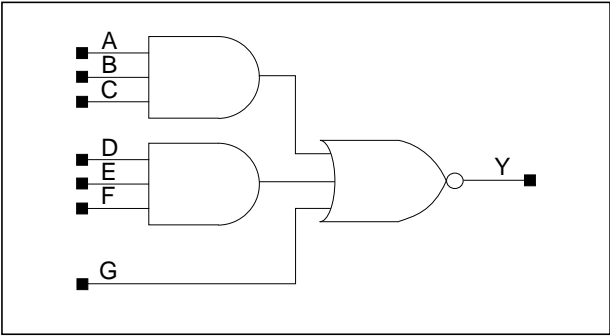
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO331/AO331D2/AO331D4

Two 3-ANDs into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	x	x	x	x	0
x	x	x	1	1	1	x	0
x	x	x	x	x	x	1	0
Other States							1

Cell Data

Input Load (SL)							Gate Count
AO331							AO331
A	B	C	D	E	F	G	2.67
1.0	1.0	1.0	1.0	1.0	1.0	0.9	
AO331D2							AO331D2
A	B	C	D	E	F	G	3.33
1.0	1.0	1.0	1.0	1.0	1.0	1.0	
AO331D4							AO331D4
A	B	C	D	E	F	G	4.00
1.0	1.0	1.0	1.0	1.0	1.0	1.0	



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## AO331

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.544	$0.363 + 0.090 \cdot \text{SL}$	$0.357 + 0.092 \cdot \text{SL}$	$0.350 + 0.093 \cdot \text{SL}$
	$t_F$	0.338	$0.230 + 0.054 \cdot \text{SL}$	$0.221 + 0.056 \cdot \text{SL}$	$0.209 + 0.058 \cdot \text{SL}$
	$t_{PLH}$	0.227	$0.148 + 0.039 \cdot \text{SL}$	$0.147 + 0.040 \cdot \text{SL}$	$0.148 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.170	$0.115 + 0.027 \cdot \text{SL}$	$0.115 + 0.027 \cdot \text{SL}$	$0.118 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.578	$0.397 + 0.091 \cdot \text{SL}$	$0.391 + 0.092 \cdot \text{SL}$	$0.384 + 0.093 \cdot \text{SL}$
	$t_F$	0.335	$0.225 + 0.055 \cdot \text{SL}$	$0.218 + 0.057 \cdot \text{SL}$	$0.210 + 0.058 \cdot \text{SL}$
	$t_{PLH}$	0.248	$0.169 + 0.039 \cdot \text{SL}$	$0.169 + 0.039 \cdot \text{SL}$	$0.169 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.172	$0.116 + 0.028 \cdot \text{SL}$	$0.117 + 0.027 \cdot \text{SL}$	$0.120 + 0.027 \cdot \text{SL}$
C to Y	$t_R$	0.612	$0.432 + 0.090 \cdot \text{SL}$	$0.425 + 0.092 \cdot \text{SL}$	$0.417 + 0.092 \cdot \text{SL}$
	$t_F$	0.331	$0.220 + 0.056 \cdot \text{SL}$	$0.215 + 0.057 \cdot \text{SL}$	$0.209 + 0.058 \cdot \text{SL}$
	$t_{PLH}$	0.266	$0.188 + 0.039 \cdot \text{SL}$	$0.187 + 0.039 \cdot \text{SL}$	$0.188 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.168	$0.112 + 0.028 \cdot \text{SL}$	$0.113 + 0.028 \cdot \text{SL}$	$0.117 + 0.027 \cdot \text{SL}$
D to Y	$t_R$	0.563	$0.385 + 0.089 \cdot \text{SL}$	$0.380 + 0.090 \cdot \text{SL}$	$0.374 + 0.091 \cdot \text{SL}$
	$t_F$	0.394	$0.281 + 0.056 \cdot \text{SL}$	$0.277 + 0.057 \cdot \text{SL}$	$0.270 + 0.058 \cdot \text{SL}$
	$t_{PLH}$	0.314	$0.232 + 0.041 \cdot \text{SL}$	$0.235 + 0.040 \cdot \text{SL}$	$0.238 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.251	$0.196 + 0.027 \cdot \text{SL}$	$0.197 + 0.027 \cdot \text{SL}$	$0.198 + 0.027 \cdot \text{SL}$
E to Y	$t_R$	0.599	$0.419 + 0.090 \cdot \text{SL}$	$0.415 + 0.091 \cdot \text{SL}$	$0.410 + 0.092 \cdot \text{SL}$
	$t_F$	0.393	$0.280 + 0.057 \cdot \text{SL}$	$0.277 + 0.057 \cdot \text{SL}$	$0.272 + 0.058 \cdot \text{SL}$
	$t_{PLH}$	0.338	$0.257 + 0.040 \cdot \text{SL}$	$0.259 + 0.040 \cdot \text{SL}$	$0.261 + 0.040 \cdot \text{SL}$
	$t_{PHL}$	0.253	$0.198 + 0.028 \cdot \text{SL}$	$0.200 + 0.027 \cdot \text{SL}$	$0.201 + 0.027 \cdot \text{SL}$
F to Y	$t_R$	0.632	$0.453 + 0.090 \cdot \text{SL}$	$0.449 + 0.091 \cdot \text{SL}$	$0.444 + 0.091 \cdot \text{SL}$
	$t_F$	0.392	$0.278 + 0.057 \cdot \text{SL}$	$0.276 + 0.058 \cdot \text{SL}$	$0.272 + 0.058 \cdot \text{SL}$
	$t_{PLH}$	0.358	$0.277 + 0.040 \cdot \text{SL}$	$0.279 + 0.040 \cdot \text{SL}$	$0.281 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.250	$0.195 + 0.028 \cdot \text{SL}$	$0.197 + 0.027 \cdot \text{SL}$	$0.199 + 0.027 \cdot \text{SL}$
G to Y	$t_R$	0.631	$0.452 + 0.090 \cdot \text{SL}$	$0.448 + 0.091 \cdot \text{SL}$	$0.444 + 0.091 \cdot \text{SL}$
	$t_F$	0.296	$0.238 + 0.029 \cdot \text{SL}$	$0.234 + 0.030 \cdot \text{SL}$	$0.226 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.386	$0.305 + 0.040 \cdot \text{SL}$	$0.307 + 0.040 \cdot \text{SL}$	$0.310 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.185	$0.148 + 0.018 \cdot \text{SL}$	$0.151 + 0.018 \cdot \text{SL}$	$0.156 + 0.017 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO331/AO331D2/AO331D4

## Two 3-ANDs into 3-NOR with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO331D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.363	$0.345 + 0.009 \cdot \text{SL}$	$0.352 + 0.007 \cdot \text{SL}$	$0.359 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.321	$0.301 + 0.010 \cdot \text{SL}$	$0.309 + 0.008 \cdot \text{SL}$	$0.320 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.100	$0.073 + 0.014 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.389	$0.371 + 0.009 \cdot \text{SL}$	$0.378 + 0.007 \cdot \text{SL}$	$0.385 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.322	$0.302 + 0.010 \cdot \text{SL}$	$0.310 + 0.008 \cdot \text{SL}$	$0.321 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.410	$0.392 + 0.009 \cdot \text{SL}$	$0.399 + 0.007 \cdot \text{SL}$	$0.407 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.298 + 0.010 \cdot \text{SL}$	$0.307 + 0.008 \cdot \text{SL}$	$0.318 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.099	$0.071 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.448	$0.430 + 0.009 \cdot \text{SL}$	$0.437 + 0.007 \cdot \text{SL}$	$0.444 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.406	$0.385 + 0.010 \cdot \text{SL}$	$0.393 + 0.008 \cdot \text{SL}$	$0.404 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.101	$0.073 + 0.014 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.060 + 0.014 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.476	$0.458 + 0.009 \cdot \text{SL}$	$0.465 + 0.007 \cdot \text{SL}$	$0.473 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.407	$0.387 + 0.010 \cdot \text{SL}$	$0.396 + 0.008 \cdot \text{SL}$	$0.406 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.103	$0.076 + 0.013 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.062 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.500	$0.482 + 0.009 \cdot \text{SL}$	$0.489 + 0.007 \cdot \text{SL}$	$0.497 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.405	$0.385 + 0.010 \cdot \text{SL}$	$0.393 + 0.008 \cdot \text{SL}$	$0.404 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.103	$0.075 + 0.014 \cdot \text{SL}$	$0.075 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.529	$0.510 + 0.009 \cdot \text{SL}$	$0.518 + 0.007 \cdot \text{SL}$	$0.526 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.336	$0.316 + 0.010 \cdot \text{SL}$	$0.324 + 0.008 \cdot \text{SL}$	$0.334 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AO331D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.094	$0.081 + 0.006 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.398	$0.388 + 0.005 \cdot \text{SL}$	$0.393 + 0.004 \cdot \text{SL}$	$0.406 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.329	$0.318 + 0.006 \cdot \text{SL}$	$0.323 + 0.004 \cdot \text{SL}$	$0.338 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.096	$0.083 + 0.006 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.425	$0.414 + 0.005 \cdot \text{SL}$	$0.420 + 0.004 \cdot \text{SL}$	$0.433 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.330	$0.319 + 0.006 \cdot \text{SL}$	$0.324 + 0.004 \cdot \text{SL}$	$0.339 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.096	$0.083 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.064 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.447	$0.436 + 0.005 \cdot \text{SL}$	$0.443 + 0.004 \cdot \text{SL}$	$0.456 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.327	$0.315 + 0.006 \cdot \text{SL}$	$0.321 + 0.004 \cdot \text{SL}$	$0.336 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.094	$0.081 + 0.006 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.484	$0.473 + 0.005 \cdot \text{SL}$	$0.479 + 0.004 \cdot \text{SL}$	$0.492 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.414	$0.402 + 0.006 \cdot \text{SL}$	$0.408 + 0.004 \cdot \text{SL}$	$0.423 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.095	$0.082 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.513	$0.502 + 0.005 \cdot \text{SL}$	$0.508 + 0.004 \cdot \text{SL}$	$0.521 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.416	$0.404 + 0.006 \cdot \text{SL}$	$0.410 + 0.004 \cdot \text{SL}$	$0.425 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.097	$0.084 + 0.006 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.537	$0.526 + 0.006 \cdot \text{SL}$	$0.533 + 0.004 \cdot \text{SL}$	$0.546 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.413	$0.402 + 0.006 \cdot \text{SL}$	$0.407 + 0.004 \cdot \text{SL}$	$0.422 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.097	$0.084 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.059 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.566	$0.555 + 0.006 \cdot \text{SL}$	$0.561 + 0.004 \cdot \text{SL}$	$0.574 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.339	$0.327 + 0.006 \cdot \text{SL}$	$0.333 + 0.004 \cdot \text{SL}$	$0.347 + 0.004 \cdot \text{SL}$

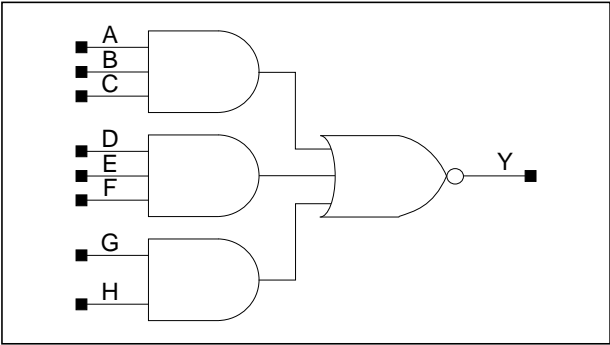
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO332/AO332D2/AO332D4

Two 3-ANDs and 2-AND into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	1	x	x	x	x	x	0
x	x	x	1	1	1	x	x	0
x	x	x	x	x	x	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
AO332								AO332
A	B	C	D	E	F	G	H	3.00
1.0	1.0	1.0	1.0	1.0	1.1	1.1	1.1	
AO332D2								AO332D2
A	B	C	D	E	F	G	H	4.00
1.0	1.1	1.1	1.0	1.1	1.1	1.1	1.1	
AO332D4								AO332D4
A	B	C	D	E	F	G	H	4.67
1.0	1.1	1.1	1.0	1.0	1.1	1.1	1.1	



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AO332**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.564	$0.382 + 0.091 \cdot \text{SL}$	$0.378 + 0.092 \cdot \text{SL}$	$0.371 + 0.093 \cdot \text{SL}$
	$t_F$	0.354	$0.257 + 0.048 \cdot \text{SL}$	$0.250 + 0.050 \cdot \text{SL}$	$0.239 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.239	$0.161 + 0.039 \cdot \text{SL}$	$0.159 + 0.040 \cdot \text{SL}$	$0.160 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.168	$0.118 + 0.025 \cdot \text{SL}$	$0.119 + 0.024 \cdot \text{SL}$	$0.121 + 0.024 \cdot \text{SL}$
B to Y	$t_R$	0.603	$0.420 + 0.091 \cdot \text{SL}$	$0.416 + 0.092 \cdot \text{SL}$	$0.409 + 0.093 \cdot \text{SL}$
	$t_F$	0.350	$0.252 + 0.049 \cdot \text{SL}$	$0.245 + 0.051 \cdot \text{SL}$	$0.238 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.262	$0.184 + 0.039 \cdot \text{SL}$	$0.183 + 0.039 \cdot \text{SL}$	$0.183 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.169	$0.120 + 0.025 \cdot \text{SL}$	$0.120 + 0.025 \cdot \text{SL}$	$0.123 + 0.024 \cdot \text{SL}$
C to Y	$t_R$	0.642	$0.461 + 0.091 \cdot \text{SL}$	$0.455 + 0.092 \cdot \text{SL}$	$0.449 + 0.093 \cdot \text{SL}$
	$t_F$	0.346	$0.247 + 0.050 \cdot \text{SL}$	$0.242 + 0.051 \cdot \text{SL}$	$0.237 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.284	$0.205 + 0.039 \cdot \text{SL}$	$0.205 + 0.039 \cdot \text{SL}$	$0.205 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.165	$0.116 + 0.025 \cdot \text{SL}$	$0.117 + 0.025 \cdot \text{SL}$	$0.120 + 0.024 \cdot \text{SL}$
D to Y	$t_R$	0.627	$0.446 + 0.090 \cdot \text{SL}$	$0.443 + 0.091 \cdot \text{SL}$	$0.439 + 0.092 \cdot \text{SL}$
	$t_F$	0.419	$0.321 + 0.049 \cdot \text{SL}$	$0.315 + 0.051 \cdot \text{SL}$	$0.306 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.354	$0.273 + 0.041 \cdot \text{SL}$	$0.275 + 0.040 \cdot \text{SL}$	$0.278 + 0.040 \cdot \text{SL}$
	$t_{PHL}$	0.235	$0.186 + 0.025 \cdot \text{SL}$	$0.187 + 0.024 \cdot \text{SL}$	$0.188 + 0.024 \cdot \text{SL}$
E to Y	$t_R$	0.664	$0.483 + 0.091 \cdot \text{SL}$	$0.480 + 0.091 \cdot \text{SL}$	$0.477 + 0.092 \cdot \text{SL}$
	$t_F$	0.418	$0.318 + 0.050 \cdot \text{SL}$	$0.314 + 0.051 \cdot \text{SL}$	$0.308 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.379	$0.299 + 0.040 \cdot \text{SL}$	$0.300 + 0.040 \cdot \text{SL}$	$0.303 + 0.040 \cdot \text{SL}$
	$t_{PHL}$	0.237	$0.188 + 0.025 \cdot \text{SL}$	$0.189 + 0.024 \cdot \text{SL}$	$0.191 + 0.024 \cdot \text{SL}$
F to Y	$t_R$	0.700	$0.520 + 0.090 \cdot \text{SL}$	$0.517 + 0.091 \cdot \text{SL}$	$0.514 + 0.091 \cdot \text{SL}$
	$t_F$	0.415	$0.315 + 0.050 \cdot \text{SL}$	$0.312 + 0.051 \cdot \text{SL}$	$0.307 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.402	$0.322 + 0.040 \cdot \text{SL}$	$0.323 + 0.040 \cdot \text{SL}$	$0.325 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.235	$0.185 + 0.025 \cdot \text{SL}$	$0.187 + 0.024 \cdot \text{SL}$	$0.188 + 0.024 \cdot \text{SL}$
G to Y	$t_R$	0.662	$0.483 + 0.090 \cdot \text{SL}$	$0.479 + 0.091 \cdot \text{SL}$	$0.475 + 0.091 \cdot \text{SL}$
	$t_F$	0.354	$0.290 + 0.032 \cdot \text{SL}$	$0.286 + 0.033 \cdot \text{SL}$	$0.276 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.421	$0.340 + 0.041 \cdot \text{SL}$	$0.342 + 0.040 \cdot \text{SL}$	$0.346 + 0.040 \cdot \text{SL}$
	$t_{PHL}$	0.193	$0.155 + 0.019 \cdot \text{SL}$	$0.158 + 0.018 \cdot \text{SL}$	$0.164 + 0.017 \cdot \text{SL}$
H to Y	$t_R$	0.701	$0.521 + 0.090 \cdot \text{SL}$	$0.518 + 0.091 \cdot \text{SL}$	$0.514 + 0.091 \cdot \text{SL}$
	$t_F$	0.348	$0.282 + 0.033 \cdot \text{SL}$	$0.279 + 0.034 \cdot \text{SL}$	$0.274 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.447	$0.366 + 0.040 \cdot \text{SL}$	$0.368 + 0.040 \cdot \text{SL}$	$0.370 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.186	$0.148 + 0.019 \cdot \text{SL}$	$0.151 + 0.018 \cdot \text{SL}$	$0.157 + 0.017 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# AO332/AO332D2/AO332D4

## Two 3-ANDs and 2-AND into 3-NOR with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO332D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.099	$0.072 + 0.013 \cdot \text{SL}$	$0.069 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.062 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.373	$0.354 + 0.009 \cdot \text{SL}$	$0.362 + 0.007 \cdot \text{SL}$	$0.369 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.317	$0.297 + 0.010 \cdot \text{SL}$	$0.305 + 0.008 \cdot \text{SL}$	$0.316 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.101	$0.075 + 0.013 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.062 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.400	$0.382 + 0.009 \cdot \text{SL}$	$0.389 + 0.007 \cdot \text{SL}$	$0.397 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.318	$0.297 + 0.010 \cdot \text{SL}$	$0.305 + 0.008 \cdot \text{SL}$	$0.316 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.104	$0.078 + 0.013 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.426	$0.407 + 0.009 \cdot \text{SL}$	$0.415 + 0.007 \cdot \text{SL}$	$0.423 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.314	$0.294 + 0.010 \cdot \text{SL}$	$0.302 + 0.008 \cdot \text{SL}$	$0.313 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.101	$0.073 + 0.014 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.489	$0.471 + 0.009 \cdot \text{SL}$	$0.478 + 0.007 \cdot \text{SL}$	$0.486 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.390	$0.370 + 0.010 \cdot \text{SL}$	$0.378 + 0.008 \cdot \text{SL}$	$0.389 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.103	$0.076 + 0.013 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.062 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.520	$0.501 + 0.009 \cdot \text{SL}$	$0.509 + 0.007 \cdot \text{SL}$	$0.517 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.392	$0.372 + 0.010 \cdot \text{SL}$	$0.380 + 0.008 \cdot \text{SL}$	$0.391 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.106	$0.080 + 0.013 \cdot \text{SL}$	$0.075 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.546	$0.527 + 0.009 \cdot \text{SL}$	$0.535 + 0.007 \cdot \text{SL}$	$0.544 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.389	$0.369 + 0.010 \cdot \text{SL}$	$0.377 + 0.008 \cdot \text{SL}$	$0.388 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.103	$0.076 + 0.013 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.560	$0.542 + 0.009 \cdot \text{SL}$	$0.549 + 0.007 \cdot \text{SL}$	$0.558 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.347	$0.327 + 0.010 \cdot \text{SL}$	$0.335 + 0.008 \cdot \text{SL}$	$0.346 + 0.007 \cdot \text{SL}$
H to Y	$t_R$	0.105	$0.078 + 0.014 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.591	$0.572 + 0.009 \cdot \text{SL}$	$0.580 + 0.007 \cdot \text{SL}$	$0.589 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.340	$0.320 + 0.010 \cdot \text{SL}$	$0.328 + 0.008 \cdot \text{SL}$	$0.339 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## AO332D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.094	$0.081 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.065 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.405	$0.394 + 0.005 \cdot \text{SL}$	$0.400 + 0.004 \cdot \text{SL}$	$0.413 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.321	$0.309 + 0.006 \cdot \text{SL}$	$0.316 + 0.004 \cdot \text{SL}$	$0.330 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.096	$0.082 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.434	$0.423 + 0.006 \cdot \text{SL}$	$0.429 + 0.004 \cdot \text{SL}$	$0.443 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.322	$0.311 + 0.006 \cdot \text{SL}$	$0.317 + 0.004 \cdot \text{SL}$	$0.332 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.099	$0.086 + 0.006 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.461	$0.449 + 0.006 \cdot \text{SL}$	$0.456 + 0.004 \cdot \text{SL}$	$0.470 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.307 + 0.006 \cdot \text{SL}$	$0.313 + 0.004 \cdot \text{SL}$	$0.328 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.097	$0.085 + 0.006 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.080	$0.067 + 0.007 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.524	$0.513 + 0.006 \cdot \text{SL}$	$0.519 + 0.004 \cdot \text{SL}$	$0.532 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.394	$0.383 + 0.006 \cdot \text{SL}$	$0.389 + 0.004 \cdot \text{SL}$	$0.404 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.098	$0.085 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.080	$0.067 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.555	$0.544 + 0.006 \cdot \text{SL}$	$0.550 + 0.004 \cdot \text{SL}$	$0.564 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.397	$0.385 + 0.006 \cdot \text{SL}$	$0.391 + 0.004 \cdot \text{SL}$	$0.406 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.101	$0.088 + 0.006 \cdot \text{SL}$	$0.087 + 0.007 \cdot \text{SL}$	$0.074 + 0.007 \cdot \text{SL}$
	$t_F$	0.080	$0.067 + 0.007 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.582	$0.571 + 0.006 \cdot \text{SL}$	$0.578 + 0.004 \cdot \text{SL}$	$0.592 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.394	$0.382 + 0.006 \cdot \text{SL}$	$0.388 + 0.004 \cdot \text{SL}$	$0.403 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.098	$0.085 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.064 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.595	$0.584 + 0.006 \cdot \text{SL}$	$0.591 + 0.004 \cdot \text{SL}$	$0.604 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.350	$0.338 + 0.006 \cdot \text{SL}$	$0.344 + 0.004 \cdot \text{SL}$	$0.359 + 0.004 \cdot \text{SL}$
H to Y	$t_R$	0.101	$0.088 + 0.006 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.627	$0.616 + 0.006 \cdot \text{SL}$	$0.622 + 0.004 \cdot \text{SL}$	$0.636 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.343	$0.331 + 0.006 \cdot \text{SL}$	$0.337 + 0.004 \cdot \text{SL}$	$0.352 + 0.004 \cdot \text{SL}$

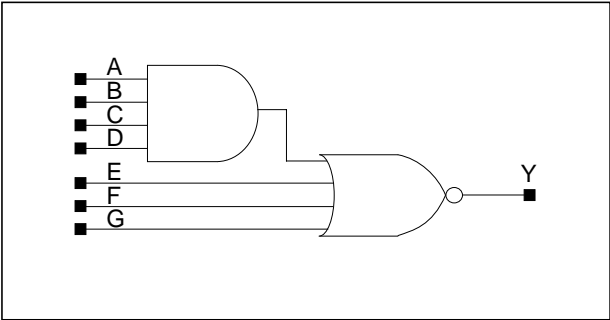
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



AO4111/AO4111D2

4-AND into 4-NOR with 1X/2X Drive

Logic SymbolCell Data



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	1	x	x	x	0
x	x	x	x	1	x	x	0
x	x	x	x	x	1	x	0
x	x	x	x	x	x	1	0
Other States							1

Cell Data

Input Load (SL)							Gate Count
AO4111							AO4111
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.8	0.8	0.9	2.67
AO4111D2							AO4111D2
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	0.8	0.8	0.9	3.33



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**AO4111**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.630	$0.391 + 0.119 \cdot \text{SL}$	$0.386 + 0.120 \cdot \text{SL}$	$0.378 + 0.121 \cdot \text{SL}$
	$t_F$	0.420	$0.238 + 0.091 \cdot \text{SL}$	$0.230 + 0.093 \cdot \text{SL}$	$0.225 + 0.094 \cdot \text{SL}$
	$t_{PLH}$	0.202	$0.105 + 0.049 \cdot \text{SL}$	$0.094 + 0.051 \cdot \text{SL}$	$0.095 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.227	$0.143 + 0.042 \cdot \text{SL}$	$0.142 + 0.042 \cdot \text{SL}$	$0.142 + 0.042 \cdot \text{SL}$
B to Y	$t_R$	0.669	$0.431 + 0.119 \cdot \text{SL}$	$0.423 + 0.121 \cdot \text{SL}$	$0.416 + 0.122 \cdot \text{SL}$
	$t_F$	0.422	$0.239 + 0.091 \cdot \text{SL}$	$0.233 + 0.093 \cdot \text{SL}$	$0.227 + 0.094 \cdot \text{SL}$
	$t_{PLH}$	0.224	$0.124 + 0.050 \cdot \text{SL}$	$0.117 + 0.051 \cdot \text{SL}$	$0.118 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.237	$0.151 + 0.043 \cdot \text{SL}$	$0.152 + 0.043 \cdot \text{SL}$	$0.153 + 0.043 \cdot \text{SL}$
C to Y	$t_R$	0.709	$0.473 + 0.118 \cdot \text{SL}$	$0.462 + 0.121 \cdot \text{SL}$	$0.454 + 0.122 \cdot \text{SL}$
	$t_F$	0.420	$0.237 + 0.092 \cdot \text{SL}$	$0.232 + 0.093 \cdot \text{SL}$	$0.227 + 0.094 \cdot \text{SL}$
	$t_{PLH}$	0.244	$0.143 + 0.051 \cdot \text{SL}$	$0.139 + 0.051 \cdot \text{SL}$	$0.140 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.241	$0.155 + 0.043 \cdot \text{SL}$	$0.156 + 0.043 \cdot \text{SL}$	$0.158 + 0.043 \cdot \text{SL}$
D to Y	$t_R$	0.750	$0.515 + 0.118 \cdot \text{SL}$	$0.503 + 0.120 \cdot \text{SL}$	$0.493 + 0.122 \cdot \text{SL}$
	$t_F$	0.419	$0.234 + 0.092 \cdot \text{SL}$	$0.230 + 0.093 \cdot \text{SL}$	$0.227 + 0.094 \cdot \text{SL}$
	$t_{PLH}$	0.261	$0.158 + 0.051 \cdot \text{SL}$	$0.158 + 0.052 \cdot \text{SL}$	$0.159 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.242	$0.156 + 0.043 \cdot \text{SL}$	$0.157 + 0.043 \cdot \text{SL}$	$0.159 + 0.043 \cdot \text{SL}$
E to Y	$t_R$	0.790	$0.556 + 0.117 \cdot \text{SL}$	$0.550 + 0.118 \cdot \text{SL}$	$0.544 + 0.119 \cdot \text{SL}$
	$t_F$	0.343	$0.240 + 0.051 \cdot \text{SL}$	$0.237 + 0.052 \cdot \text{SL}$	$0.231 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.399	$0.293 + 0.053 \cdot \text{SL}$	$0.297 + 0.052 \cdot \text{SL}$	$0.300 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.263	$0.207 + 0.028 \cdot \text{SL}$	$0.209 + 0.027 \cdot \text{SL}$	$0.210 + 0.027 \cdot \text{SL}$
F to Y	$t_R$	0.791	$0.558 + 0.117 \cdot \text{SL}$	$0.551 + 0.118 \cdot \text{SL}$	$0.544 + 0.119 \cdot \text{SL}$
	$t_F$	0.380	$0.277 + 0.051 \cdot \text{SL}$	$0.274 + 0.052 \cdot \text{SL}$	$0.270 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.427	$0.321 + 0.053 \cdot \text{SL}$	$0.325 + 0.052 \cdot \text{SL}$	$0.329 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.284	$0.228 + 0.028 \cdot \text{SL}$	$0.230 + 0.028 \cdot \text{SL}$	$0.233 + 0.027 \cdot \text{SL}$
G to Y	$t_R$	0.791	$0.557 + 0.117 \cdot \text{SL}$	$0.551 + 0.118 \cdot \text{SL}$	$0.544 + 0.119 \cdot \text{SL}$
	$t_F$	0.417	$0.313 + 0.052 \cdot \text{SL}$	$0.311 + 0.052 \cdot \text{SL}$	$0.308 + 0.053 \cdot \text{SL}$
	$t_{PLH}$	0.438	$0.332 + 0.053 \cdot \text{SL}$	$0.335 + 0.052 \cdot \text{SL}$	$0.339 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.242 + 0.029 \cdot \text{SL}$	$0.245 + 0.028 \cdot \text{SL}$	$0.250 + 0.028 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## AO4111/AO4111D2

### 4-AND into 4-NOR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### AO4111D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.099	$0.071 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.062 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.330	$0.311 + 0.009 \cdot \text{SL}$	$0.319 + 0.007 \cdot \text{SL}$	$0.327 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.358	$0.338 + 0.010 \cdot \text{SL}$	$0.346 + 0.008 \cdot \text{SL}$	$0.357 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.102	$0.075 + 0.013 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.060 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.356	$0.338 + 0.009 \cdot \text{SL}$	$0.345 + 0.007 \cdot \text{SL}$	$0.354 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.367	$0.346 + 0.010 \cdot \text{SL}$	$0.355 + 0.008 \cdot \text{SL}$	$0.366 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.103	$0.076 + 0.014 \cdot \text{SL}$	$0.075 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.062 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.380	$0.362 + 0.009 \cdot \text{SL}$	$0.369 + 0.007 \cdot \text{SL}$	$0.378 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.371	$0.351 + 0.010 \cdot \text{SL}$	$0.359 + 0.008 \cdot \text{SL}$	$0.370 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.105	$0.078 + 0.014 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.059 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.401	$0.382 + 0.009 \cdot \text{SL}$	$0.390 + 0.007 \cdot \text{SL}$	$0.400 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.371	$0.351 + 0.010 \cdot \text{SL}$	$0.359 + 0.008 \cdot \text{SL}$	$0.370 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.107	$0.079 + 0.014 \cdot \text{SL}$	$0.079 + 0.014 \cdot \text{SL}$	$0.065 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.535	$0.516 + 0.009 \cdot \text{SL}$	$0.525 + 0.007 \cdot \text{SL}$	$0.534 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.406	$0.385 + 0.010 \cdot \text{SL}$	$0.393 + 0.008 \cdot \text{SL}$	$0.404 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.107	$0.079 + 0.014 \cdot \text{SL}$	$0.079 + 0.014 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.058 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.563	$0.544 + 0.009 \cdot \text{SL}$	$0.553 + 0.007 \cdot \text{SL}$	$0.562 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.431	$0.411 + 0.010 \cdot \text{SL}$	$0.419 + 0.008 \cdot \text{SL}$	$0.430 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.106	$0.079 + 0.014 \cdot \text{SL}$	$0.079 + 0.014 \cdot \text{SL}$	$0.065 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.575	$0.556 + 0.009 \cdot \text{SL}$	$0.564 + 0.007 \cdot \text{SL}$	$0.573 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.451	$0.431 + 0.010 \cdot \text{SL}$	$0.439 + 0.008 \cdot \text{SL}$	$0.450 + 0.007 \cdot \text{SL}$

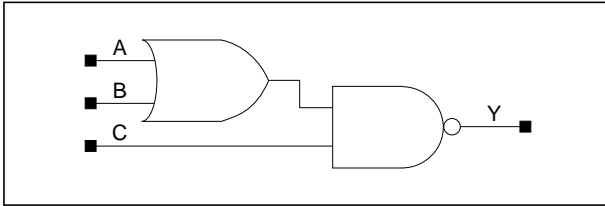
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA21DH/OA21/OA21D2/OA21D2B/OA21D4

## 2-OR into 2-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Logic Symbol



### Truth Table

A	B	C	Y
0	0	x	1
x	x	0	1
Others States			0

### Cell Data

Input Load (SL)														
OA21DH			OA21			OA21D2			OA21D2B			OA21D4		
A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
0.5	0.6	0.6	0.9	1.0	0.9	1.8	2.0	1.9	1.0	1.0	1.0	1.0	1.0	1.0
Gate Count														
OA21DH			OA21			OA21D2			OA21D2B			OA21D4		
1.33			1.33			2.33			2.33			3.00		

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA21DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.428	$0.176 + 0.126 \cdot \text{SL}$	$0.159 + 0.130 \cdot \text{SL}$	$0.152 + 0.131 \cdot \text{SL}$
	$t_F$	0.253	$0.112 + 0.070 \cdot \text{SL}$	$0.098 + 0.074 \cdot \text{SL}$	$0.082 + 0.076 \cdot \text{SL}$
	$t_{PLH}$	0.216	$0.105 + 0.056 \cdot \text{SL}$	$0.104 + 0.056 \cdot \text{SL}$	$0.103 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.159	$0.086 + 0.036 \cdot \text{SL}$	$0.086 + 0.037 \cdot \text{SL}$	$0.085 + 0.037 \cdot \text{SL}$
B to Y	$t_R$	0.425	$0.169 + 0.128 \cdot \text{SL}$	$0.160 + 0.130 \cdot \text{SL}$	$0.153 + 0.131 \cdot \text{SL}$
	$t_F$	0.280	$0.141 + 0.069 \cdot \text{SL}$	$0.125 + 0.073 \cdot \text{SL}$	$0.108 + 0.075 \cdot \text{SL}$
	$t_{PLH}$	0.218	$0.106 + 0.056 \cdot \text{SL}$	$0.105 + 0.056 \cdot \text{SL}$	$0.106 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.174	$0.101 + 0.036 \cdot \text{SL}$	$0.101 + 0.036 \cdot \text{SL}$	$0.101 + 0.036 \cdot \text{SL}$
C to Y	$t_R$	0.261	$0.139 + 0.061 \cdot \text{SL}$	$0.126 + 0.064 \cdot \text{SL}$	$0.110 + 0.066 \cdot \text{SL}$
	$t_F$	0.267	$0.122 + 0.073 \cdot \text{SL}$	$0.115 + 0.075 \cdot \text{SL}$	$0.108 + 0.075 \cdot \text{SL}$
	$t_{PLH}$	0.160	$0.103 + 0.028 \cdot \text{SL}$	$0.102 + 0.028 \cdot \text{SL}$	$0.101 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.166	$0.093 + 0.037 \cdot \text{SL}$	$0.094 + 0.037 \cdot \text{SL}$	$0.094 + 0.037 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OA21DH/OA21/OA21D2/OA21D2B/OA21D4

## 2-OR into 2-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.263	$0.153 + 0.055 \cdot \text{SL}$	$0.142 + 0.058 \cdot \text{SL}$	$0.129 + 0.059 \cdot \text{SL}$
	$t_F$	0.229	$0.127 + 0.051 \cdot \text{SL}$	$0.118 + 0.053 \cdot \text{SL}$	$0.105 + 0.055 \cdot \text{SL}$
	$t_{PLH}$	0.138	$0.087 + 0.026 \cdot \text{SL}$	$0.088 + 0.025 \cdot \text{SL}$	$0.087 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.144	$0.092 + 0.026 \cdot \text{SL}$	$0.092 + 0.026 \cdot \text{SL}$	$0.092 + 0.026 \cdot \text{SL}$
B to Y	$t_R$	0.256	$0.143 + 0.056 \cdot \text{SL}$	$0.135 + 0.058 \cdot \text{SL}$	$0.127 + 0.059 \cdot \text{SL}$
	$t_F$	0.267	$0.167 + 0.050 \cdot \text{SL}$	$0.157 + 0.053 \cdot \text{SL}$	$0.143 + 0.054 \cdot \text{SL}$
	$t_{PLH}$	0.137	$0.085 + 0.026 \cdot \text{SL}$	$0.087 + 0.026 \cdot \text{SL}$	$0.087 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.166	$0.114 + 0.026 \cdot \text{SL}$	$0.114 + 0.026 \cdot \text{SL}$	$0.114 + 0.026 \cdot \text{SL}$
C to Y	$t_R$	0.177	$0.126 + 0.026 \cdot \text{SL}$	$0.117 + 0.028 \cdot \text{SL}$	$0.106 + 0.029 \cdot \text{SL}$
	$t_F$	0.257	$0.153 + 0.052 \cdot \text{SL}$	$0.147 + 0.054 \cdot \text{SL}$	$0.140 + 0.054 \cdot \text{SL}$
	$t_{PLH}$	0.107	$0.077 + 0.015 \cdot \text{SL}$	$0.084 + 0.013 \cdot \text{SL}$	$0.084 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.177	$0.125 + 0.026 \cdot \text{SL}$	$0.125 + 0.026 \cdot \text{SL}$	$0.126 + 0.026 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### OA21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.187	$0.134 + 0.027 \cdot \text{SL}$	$0.125 + 0.029 \cdot \text{SL}$	$0.108 + 0.030 \cdot \text{SL}$
	$t_F$	0.150	$0.107 + 0.022 \cdot \text{SL}$	$0.099 + 0.024 \cdot \text{SL}$	$0.082 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.101	$0.071 + 0.015 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.078 + 0.012 \cdot \text{SL}$	$0.077 + 0.012 \cdot \text{SL}$
B to Y	$t_R$	0.178	$0.123 + 0.027 \cdot \text{SL}$	$0.115 + 0.029 \cdot \text{SL}$	$0.105 + 0.030 \cdot \text{SL}$
	$t_F$	0.187	$0.144 + 0.021 \cdot \text{SL}$	$0.136 + 0.023 \cdot \text{SL}$	$0.117 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.101	$0.072 + 0.015 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.121	$0.096 + 0.013 \cdot \text{SL}$	$0.099 + 0.012 \cdot \text{SL}$	$0.098 + 0.012 \cdot \text{SL}$
C to Y	$t_R$	0.142	$0.116 + 0.013 \cdot \text{SL}$	$0.113 + 0.014 \cdot \text{SL}$	$0.098 + 0.015 \cdot \text{SL}$
	$t_F$	0.171	$0.125 + 0.023 \cdot \text{SL}$	$0.120 + 0.024 \cdot \text{SL}$	$0.110 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.088	$0.071 + 0.009 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.123	$0.098 + 0.013 \cdot \text{SL}$	$0.100 + 0.012 \cdot \text{SL}$	$0.101 + 0.012 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA21DH/OA21/OA21D2/OA21D2B/OA21D4

## 2-OR into 2-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA21D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.083	$0.054 + 0.015 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$	$0.044 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.053 + 0.014 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$	$0.049 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.233	$0.216 + 0.009 \cdot \text{SL}$	$0.221 + 0.007 \cdot \text{SL}$	$0.227 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.235	$0.215 + 0.010 \cdot \text{SL}$	$0.223 + 0.008 \cdot \text{SL}$	$0.233 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.083	$0.054 + 0.015 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$	$0.044 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.051 + 0.014 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.049 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.233	$0.215 + 0.009 \cdot \text{SL}$	$0.221 + 0.007 \cdot \text{SL}$	$0.227 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.263	$0.243 + 0.010 \cdot \text{SL}$	$0.251 + 0.008 \cdot \text{SL}$	$0.261 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.082	$0.052 + 0.015 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$	$0.043 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.052 + 0.014 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.049 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.202 + 0.009 \cdot \text{SL}$	$0.208 + 0.007 \cdot \text{SL}$	$0.213 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.266	$0.245 + 0.010 \cdot \text{SL}$	$0.253 + 0.008 \cdot \text{SL}$	$0.263 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### OA21D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.079	$0.064 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.069	$0.054 + 0.007 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.253 + 0.005 \cdot \text{SL}$	$0.258 + 0.004 \cdot \text{SL}$	$0.269 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.243	$0.232 + 0.006 \cdot \text{SL}$	$0.238 + 0.004 \cdot \text{SL}$	$0.252 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.071	$0.056 + 0.007 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.253 + 0.005 \cdot \text{SL}$	$0.258 + 0.004 \cdot \text{SL}$	$0.268 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.271	$0.260 + 0.006 \cdot \text{SL}$	$0.266 + 0.004 \cdot \text{SL}$	$0.280 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.076	$0.061 + 0.008 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.054 + 0.008 \cdot \text{SL}$
	$t_F$	0.070	$0.056 + 0.007 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.241	$0.231 + 0.005 \cdot \text{SL}$	$0.236 + 0.004 \cdot \text{SL}$	$0.247 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.275	$0.263 + 0.006 \cdot \text{SL}$	$0.269 + 0.004 \cdot \text{SL}$	$0.283 + 0.004 \cdot \text{SL}$

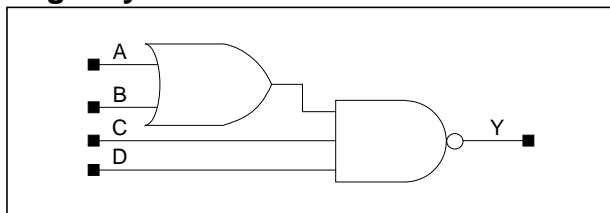
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# OA211DH/OA211/OA211D2/OA211D2B/OA211D4

## 2-OR into 3-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
Other States				0

### Cell Data

Input Load (SL)																			
OA211DH				OA211				OA211D2				OA211D2B				OA211D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.6	0.6	0.6	0.6	1.0	1.0	1.0	1.0	2.1	2.0	2.2	2.0	1.0	1.1	1.1	1.1	1.0	1.1	1.1	1.1
Gate Count																			
OA211DH				OA211				OA211D2				OA211D2B				OA211D4			
1.67				1.67				3.00				2.67				3.33			

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA211DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.438	$0.185 + 0.126 \cdot \text{SL}$	$0.170 + 0.130 \cdot \text{SL}$	$0.164 + 0.131 \cdot \text{SL}$
	$t_F$	0.308	$0.139 + 0.084 \cdot \text{SL}$	$0.125 + 0.088 \cdot \text{SL}$	$0.112 + 0.089 \cdot \text{SL}$
	$t_{PLH}$	0.223	$0.111 + 0.056 \cdot \text{SL}$	$0.110 + 0.056 \cdot \text{SL}$	$0.109 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.173	$0.091 + 0.041 \cdot \text{SL}$	$0.089 + 0.042 \cdot \text{SL}$	$0.089 + 0.042 \cdot \text{SL}$
B to Y	$t_R$	0.436	$0.180 + 0.128 \cdot \text{SL}$	$0.171 + 0.130 \cdot \text{SL}$	$0.165 + 0.131 \cdot \text{SL}$
	$t_F$	0.340	$0.173 + 0.084 \cdot \text{SL}$	$0.156 + 0.088 \cdot \text{SL}$	$0.143 + 0.090 \cdot \text{SL}$
	$t_{PLH}$	0.224	$0.112 + 0.056 \cdot \text{SL}$	$0.112 + 0.056 \cdot \text{SL}$	$0.112 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.108 + 0.042 \cdot \text{SL}$	$0.107 + 0.042 \cdot \text{SL}$	$0.107 + 0.042 \cdot \text{SL}$
C to Y	$t_R$	0.280	$0.150 + 0.065 \cdot \text{SL}$	$0.137 + 0.068 \cdot \text{SL}$	$0.123 + 0.070 \cdot \text{SL}$
	$t_F$	0.333	$0.160 + 0.087 \cdot \text{SL}$	$0.152 + 0.088 \cdot \text{SL}$	$0.145 + 0.089 \cdot \text{SL}$
	$t_{PLH}$	0.172	$0.112 + 0.030 \cdot \text{SL}$	$0.112 + 0.030 \cdot \text{SL}$	$0.112 + 0.030 \cdot \text{SL}$
	$t_{PHL}$	0.199	$0.114 + 0.042 \cdot \text{SL}$	$0.115 + 0.042 \cdot \text{SL}$	$0.116 + 0.042 \cdot \text{SL}$
D to Y	$t_R$	0.302	$0.172 + 0.065 \cdot \text{SL}$	$0.159 + 0.068 \cdot \text{SL}$	$0.145 + 0.070 \cdot \text{SL}$
	$t_F$	0.330	$0.155 + 0.088 \cdot \text{SL}$	$0.150 + 0.089 \cdot \text{SL}$	$0.144 + 0.089 \cdot \text{SL}$
	$t_{PLH}$	0.183	$0.122 + 0.030 \cdot \text{SL}$	$0.122 + 0.030 \cdot \text{SL}$	$0.122 + 0.030 \cdot \text{SL}$
	$t_{PHL}$	0.198	$0.114 + 0.042 \cdot \text{SL}$	$0.115 + 0.042 \cdot \text{SL}$	$0.116 + 0.042 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OA211DH/OA211/OA211D2/OA211D2B/OA211D4

## 2-OR into 3-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.275	$0.161 + 0.057 \cdot \text{SL}$	$0.153 + 0.059 \cdot \text{SL}$	$0.139 + 0.061 \cdot \text{SL}$
	$t_F$	0.255	$0.148 + 0.053 \cdot \text{SL}$	$0.140 + 0.055 \cdot \text{SL}$	$0.129 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.148	$0.095 + 0.026 \cdot \text{SL}$	$0.095 + 0.026 \cdot \text{SL}$	$0.095 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.146	$0.094 + 0.026 \cdot \text{SL}$	$0.093 + 0.026 \cdot \text{SL}$	$0.092 + 0.026 \cdot \text{SL}$
B to Y	$t_R$	0.269	$0.152 + 0.058 \cdot \text{SL}$	$0.145 + 0.060 \cdot \text{SL}$	$0.139 + 0.061 \cdot \text{SL}$
	$t_F$	0.297	$0.191 + 0.053 \cdot \text{SL}$	$0.181 + 0.056 \cdot \text{SL}$	$0.168 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.146	$0.093 + 0.027 \cdot \text{SL}$	$0.095 + 0.026 \cdot \text{SL}$	$0.095 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.168	$0.116 + 0.026 \cdot \text{SL}$	$0.115 + 0.026 \cdot \text{SL}$	$0.115 + 0.026 \cdot \text{SL}$
C to Y	$t_R$	0.185	$0.131 + 0.027 \cdot \text{SL}$	$0.123 + 0.029 \cdot \text{SL}$	$0.114 + 0.030 \cdot \text{SL}$
	$t_F$	0.290	$0.180 + 0.055 \cdot \text{SL}$	$0.174 + 0.056 \cdot \text{SL}$	$0.168 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.117	$0.088 + 0.014 \cdot \text{SL}$	$0.093 + 0.013 \cdot \text{SL}$	$0.092 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.182	$0.128 + 0.027 \cdot \text{SL}$	$0.129 + 0.027 \cdot \text{SL}$	$0.130 + 0.027 \cdot \text{SL}$
D to Y	$t_R$	0.200	$0.146 + 0.027 \cdot \text{SL}$	$0.139 + 0.029 \cdot \text{SL}$	$0.127 + 0.030 \cdot \text{SL}$
	$t_F$	0.287	$0.176 + 0.056 \cdot \text{SL}$	$0.171 + 0.057 \cdot \text{SL}$	$0.167 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.124	$0.095 + 0.014 \cdot \text{SL}$	$0.098 + 0.013 \cdot \text{SL}$	$0.098 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.180	$0.127 + 0.027 \cdot \text{SL}$	$0.127 + 0.027 \cdot \text{SL}$	$0.129 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### OA211D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.224	$0.169 + 0.028 \cdot \text{SL}$	$0.163 + 0.029 \cdot \text{SL}$	$0.148 + 0.030 \cdot \text{SL}$
	$t_F$	0.205	$0.154 + 0.026 \cdot \text{SL}$	$0.149 + 0.027 \cdot \text{SL}$	$0.135 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.122	$0.095 + 0.014 \cdot \text{SL}$	$0.098 + 0.013 \cdot \text{SL}$	$0.097 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.121	$0.095 + 0.013 \cdot \text{SL}$	$0.096 + 0.013 \cdot \text{SL}$	$0.095 + 0.013 \cdot \text{SL}$
B to Y	$t_R$	0.217	$0.161 + 0.028 \cdot \text{SL}$	$0.154 + 0.030 \cdot \text{SL}$	$0.146 + 0.030 \cdot \text{SL}$
	$t_F$	0.248	$0.197 + 0.026 \cdot \text{SL}$	$0.191 + 0.027 \cdot \text{SL}$	$0.175 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.121	$0.093 + 0.014 \cdot \text{SL}$	$0.097 + 0.013 \cdot \text{SL}$	$0.096 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.144	$0.117 + 0.013 \cdot \text{SL}$	$0.117 + 0.013 \cdot \text{SL}$	$0.117 + 0.013 \cdot \text{SL}$
C to Y	$t_R$	0.160	$0.135 + 0.013 \cdot \text{SL}$	$0.129 + 0.014 \cdot \text{SL}$	$0.118 + 0.015 \cdot \text{SL}$
	$t_F$	0.238	$0.185 + 0.027 \cdot \text{SL}$	$0.180 + 0.028 \cdot \text{SL}$	$0.173 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.103	$0.088 + 0.008 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$	$0.093 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.157	$0.130 + 0.013 \cdot \text{SL}$	$0.131 + 0.013 \cdot \text{SL}$	$0.132 + 0.013 \cdot \text{SL}$
D to Y	$t_R$	0.175	$0.149 + 0.013 \cdot \text{SL}$	$0.145 + 0.014 \cdot \text{SL}$	$0.132 + 0.015 \cdot \text{SL}$
	$t_F$	0.234	$0.179 + 0.027 \cdot \text{SL}$	$0.177 + 0.028 \cdot \text{SL}$	$0.171 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.110	$0.095 + 0.008 \cdot \text{SL}$	$0.098 + 0.007 \cdot \text{SL}$	$0.099 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.154	$0.127 + 0.014 \cdot \text{SL}$	$0.128 + 0.013 \cdot \text{SL}$	$0.129 + 0.013 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA211DH/OA211/OA211D2/OA211D2B/OA211D4

## 2-OR into 3-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA211D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.246 + 0.009 \cdot \text{SL}$	$0.252 + 0.007 \cdot \text{SL}$	$0.258 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.269	$0.250 + 0.010 \cdot \text{SL}$	$0.258 + 0.008 \cdot \text{SL}$	$0.268 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.014 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.246 + 0.009 \cdot \text{SL}$	$0.251 + 0.007 \cdot \text{SL}$	$0.258 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.299	$0.280 + 0.010 \cdot \text{SL}$	$0.288 + 0.008 \cdot \text{SL}$	$0.298 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.084	$0.055 + 0.015 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.239	$0.222 + 0.009 \cdot \text{SL}$	$0.227 + 0.007 \cdot \text{SL}$	$0.233 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.313	$0.293 + 0.010 \cdot \text{SL}$	$0.301 + 0.008 \cdot \text{SL}$	$0.312 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.084	$0.055 + 0.015 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.247	$0.230 + 0.009 \cdot \text{SL}$	$0.235 + 0.007 \cdot \text{SL}$	$0.241 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.308	$0.289 + 0.010 \cdot \text{SL}$	$0.297 + 0.008 \cdot \text{SL}$	$0.307 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### OA211D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.061 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.286	$0.275 + 0.005 \cdot \text{SL}$	$0.280 + 0.004 \cdot \text{SL}$	$0.290 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.281	$0.270 + 0.006 \cdot \text{SL}$	$0.276 + 0.004 \cdot \text{SL}$	$0.290 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.062 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.285	$0.275 + 0.005 \cdot \text{SL}$	$0.280 + 0.004 \cdot \text{SL}$	$0.290 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.311	$0.300 + 0.006 \cdot \text{SL}$	$0.305 + 0.004 \cdot \text{SL}$	$0.319 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.076	$0.060 + 0.008 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$	$0.054 + 0.008 \cdot \text{SL}$
	$t_F$	0.075	$0.062 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.253	$0.244 + 0.005 \cdot \text{SL}$	$0.248 + 0.004 \cdot \text{SL}$	$0.258 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.324	$0.313 + 0.006 \cdot \text{SL}$	$0.318 + 0.004 \cdot \text{SL}$	$0.333 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.076	$0.061 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$	$0.054 + 0.008 \cdot \text{SL}$
	$t_F$	0.074	$0.059 + 0.007 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.253 + 0.005 \cdot \text{SL}$	$0.257 + 0.004 \cdot \text{SL}$	$0.267 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.321	$0.309 + 0.006 \cdot \text{SL}$	$0.315 + 0.004 \cdot \text{SL}$	$0.330 + 0.004 \cdot \text{SL}$

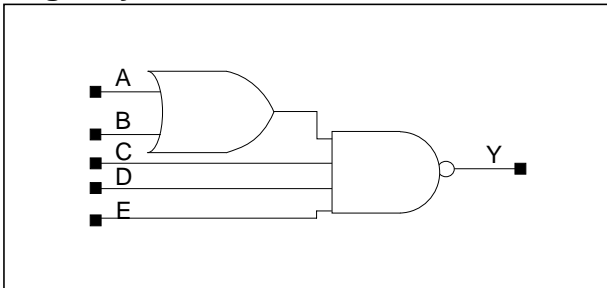
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# OA2111/OA2111D2

## 2-OR into 4-NAND with 1X/2X Drive

### Logic Symbol



### Truth Table

A	B	C	D	E	Y
0	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
Other States					0

### Cell Data

Input Load (SL)										Gate Count	
OA2111					OA2111D2					OA2111	OA2111D2
A	B	C	D	E	A	B	C	D	E		
1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	2.00	3.00



## OA2111/OA2111D2

### 2-OR into 4-NAND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA2111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.310	$0.197 + 0.056 \cdot \text{SL}$	$0.189 + 0.058 \cdot \text{SL}$	$0.179 + 0.059 \cdot \text{SL}$
	$t_F$	0.323	$0.208 + 0.057 \cdot \text{SL}$	$0.202 + 0.059 \cdot \text{SL}$	$0.191 + 0.060 \cdot \text{SL}$
	$t_{PLH}$	0.165	$0.114 + 0.025 \cdot \text{SL}$	$0.114 + 0.026 \cdot \text{SL}$	$0.114 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.163	$0.109 + 0.027 \cdot \text{SL}$	$0.108 + 0.027 \cdot \text{SL}$	$0.107 + 0.027 \cdot \text{SL}$
B to Y	$t_R$	0.305	$0.190 + 0.058 \cdot \text{SL}$	$0.185 + 0.059 \cdot \text{SL}$	$0.179 + 0.059 \cdot \text{SL}$
	$t_F$	0.364	$0.251 + 0.057 \cdot \text{SL}$	$0.243 + 0.059 \cdot \text{SL}$	$0.232 + 0.060 \cdot \text{SL}$
	$t_{PLH}$	0.164	$0.113 + 0.026 \cdot \text{SL}$	$0.113 + 0.026 \cdot \text{SL}$	$0.113 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.184	$0.130 + 0.027 \cdot \text{SL}$	$0.130 + 0.027 \cdot \text{SL}$	$0.129 + 0.027 \cdot \text{SL}$
C to Y	$t_R$	0.208	$0.153 + 0.028 \cdot \text{SL}$	$0.147 + 0.029 \cdot \text{SL}$	$0.138 + 0.030 \cdot \text{SL}$
	$t_F$	0.362	$0.245 + 0.058 \cdot \text{SL}$	$0.242 + 0.059 \cdot \text{SL}$	$0.236 + 0.060 \cdot \text{SL}$
	$t_{PLH}$	0.133	$0.106 + 0.014 \cdot \text{SL}$	$0.107 + 0.013 \cdot \text{SL}$	$0.107 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.156 + 0.028 \cdot \text{SL}$	$0.156 + 0.027 \cdot \text{SL}$	$0.157 + 0.027 \cdot \text{SL}$
D to Y	$t_R$	0.224	$0.168 + 0.028 \cdot \text{SL}$	$0.163 + 0.029 \cdot \text{SL}$	$0.154 + 0.030 \cdot \text{SL}$
	$t_F$	0.360	$0.243 + 0.058 \cdot \text{SL}$	$0.241 + 0.059 \cdot \text{SL}$	$0.235 + 0.060 \cdot \text{SL}$
	$t_{PLH}$	0.141	$0.114 + 0.014 \cdot \text{SL}$	$0.114 + 0.013 \cdot \text{SL}$	$0.115 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.215	$0.160 + 0.028 \cdot \text{SL}$	$0.161 + 0.027 \cdot \text{SL}$	$0.162 + 0.027 \cdot \text{SL}$
E to Y	$t_R$	0.241	$0.186 + 0.028 \cdot \text{SL}$	$0.181 + 0.029 \cdot \text{SL}$	$0.171 + 0.030 \cdot \text{SL}$
	$t_F$	0.358	$0.240 + 0.059 \cdot \text{SL}$	$0.238 + 0.059 \cdot \text{SL}$	$0.234 + 0.060 \cdot \text{SL}$
	$t_{PLH}$	0.147	$0.119 + 0.014 \cdot \text{SL}$	$0.120 + 0.014 \cdot \text{SL}$	$0.121 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.218	$0.162 + 0.028 \cdot \text{SL}$	$0.163 + 0.028 \cdot \text{SL}$	$0.165 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

OA2111D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.090	$0.061 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.013 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.291	$0.273 + 0.009 \cdot \text{SL}$	$0.279 + 0.007 \cdot \text{SL}$	$0.285 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.302	$0.282 + 0.010 \cdot \text{SL}$	$0.290 + 0.008 \cdot \text{SL}$	$0.301 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.090	$0.062 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.062 + 0.013 \cdot \text{SL}$	$0.066 + 0.012 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.291	$0.273 + 0.009 \cdot \text{SL}$	$0.279 + 0.007 \cdot \text{SL}$	$0.285 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.331	$0.311 + 0.010 \cdot \text{SL}$	$0.319 + 0.008 \cdot \text{SL}$	$0.330 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.260	$0.243 + 0.009 \cdot \text{SL}$	$0.248 + 0.007 \cdot \text{SL}$	$0.254 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.355	$0.336 + 0.010 \cdot \text{SL}$	$0.343 + 0.008 \cdot \text{SL}$	$0.354 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.088	$0.060 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.013 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.252 + 0.009 \cdot \text{SL}$	$0.258 + 0.007 \cdot \text{SL}$	$0.264 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.360	$0.341 + 0.010 \cdot \text{SL}$	$0.348 + 0.008 \cdot \text{SL}$	$0.359 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.062 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.278	$0.260 + 0.009 \cdot \text{SL}$	$0.266 + 0.007 \cdot \text{SL}$	$0.272 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.364	$0.344 + 0.010 \cdot \text{SL}$	$0.352 + 0.008 \cdot \text{SL}$	$0.362 + 0.007 \cdot \text{SL}$

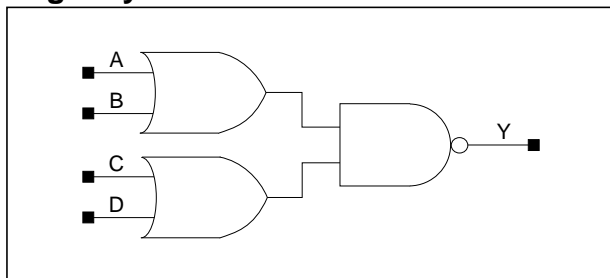
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA22DH/OA22/OA22D2/OA22D2B/OA22D4

Two 2-ORs into 2-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

## Logic Symbol



## Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
Other States				0

## Cell Data

Input Load (SL)																			
OA22DH				OA22				OA22D2				OA22D2B				OA22D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.6	0.5	0.6	0.9	0.9	0.9	0.9	1.9	1.8	1.9	1.8	0.9	1.0	1.1	0.9	0.9	1.0	1.1	0.9
Gate Count																			
OA22DH				OA22				OA22D2				OA22D2B				OA22D4			
2.00				2.00				3.00				2.67				3.33			

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

### OA22DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.439	$0.210 + 0.115 \cdot \text{SL}$	$0.190 + 0.119 \cdot \text{SL}$	$0.178 + 0.121 \cdot \text{SL}$
	$t_F$	0.312	$0.139 + 0.086 \cdot \text{SL}$	$0.125 + 0.090 \cdot \text{SL}$	$0.113 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.202	$0.097 + 0.053 \cdot \text{SL}$	$0.099 + 0.052 \cdot \text{SL}$	$0.101 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.104 + 0.044 \cdot \text{SL}$	$0.105 + 0.043 \cdot \text{SL}$	$0.105 + 0.043 \cdot \text{SL}$
B to Y	$t_R$	0.434	$0.200 + 0.117 \cdot \text{SL}$	$0.188 + 0.120 \cdot \text{SL}$	$0.179 + 0.121 \cdot \text{SL}$
	$t_F$	0.346	$0.173 + 0.086 \cdot \text{SL}$	$0.158 + 0.090 \cdot \text{SL}$	$0.147 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.203	$0.097 + 0.053 \cdot \text{SL}$	$0.100 + 0.052 \cdot \text{SL}$	$0.103 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.123 + 0.044 \cdot \text{SL}$	$0.124 + 0.043 \cdot \text{SL}$	$0.125 + 0.043 \cdot \text{SL}$
C to Y	$t_R$	0.497	$0.267 + 0.115 \cdot \text{SL}$	$0.248 + 0.120 \cdot \text{SL}$	$0.239 + 0.121 \cdot \text{SL}$
	$t_F$	0.306	$0.129 + 0.088 \cdot \text{SL}$	$0.121 + 0.090 \cdot \text{SL}$	$0.114 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.239	$0.134 + 0.053 \cdot \text{SL}$	$0.136 + 0.052 \cdot \text{SL}$	$0.139 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.207	$0.118 + 0.044 \cdot \text{SL}$	$0.120 + 0.044 \cdot \text{SL}$	$0.122 + 0.043 \cdot \text{SL}$
D to Y	$t_R$	0.493	$0.259 + 0.117 \cdot \text{SL}$	$0.248 + 0.120 \cdot \text{SL}$	$0.239 + 0.121 \cdot \text{SL}$
	$t_F$	0.339	$0.162 + 0.088 \cdot \text{SL}$	$0.154 + 0.090 \cdot \text{SL}$	$0.148 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.240	$0.134 + 0.053 \cdot \text{SL}$	$0.138 + 0.052 \cdot \text{SL}$	$0.141 + 0.052 \cdot \text{SL}$
	$t_{PHL}$	0.226	$0.138 + 0.044 \cdot \text{SL}$	$0.140 + 0.044 \cdot \text{SL}$	$0.141 + 0.043 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OA22DH/OA22/OA22D2/OA22D2B/OA22D4

## Two 2-ORs into 2-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.302	$0.193 + 0.055 \cdot \text{SL}$	$0.178 + 0.058 \cdot \text{SL}$	$0.163 + 0.060 \cdot \text{SL}$
	$t_F$	0.256	$0.143 + 0.057 \cdot \text{SL}$	$0.132 + 0.059 \cdot \text{SL}$	$0.122 + 0.061 \cdot \text{SL}$
	$t_{PLH}$	0.135	$0.080 + 0.027 \cdot \text{SL}$	$0.083 + 0.027 \cdot \text{SL}$	$0.085 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.170	$0.112 + 0.029 \cdot \text{SL}$	$0.112 + 0.029 \cdot \text{SL}$	$0.113 + 0.029 \cdot \text{SL}$
B to Y	$t_R$	0.293	$0.179 + 0.057 \cdot \text{SL}$	$0.170 + 0.059 \cdot \text{SL}$	$0.160 + 0.060 \cdot \text{SL}$
	$t_F$	0.298	$0.185 + 0.057 \cdot \text{SL}$	$0.174 + 0.059 \cdot \text{SL}$	$0.164 + 0.061 \cdot \text{SL}$
	$t_{PLH}$	0.135	$0.079 + 0.028 \cdot \text{SL}$	$0.083 + 0.027 \cdot \text{SL}$	$0.086 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.195	$0.137 + 0.029 \cdot \text{SL}$	$0.137 + 0.029 \cdot \text{SL}$	$0.138 + 0.029 \cdot \text{SL}$
C to Y	$t_R$	0.341	$0.232 + 0.055 \cdot \text{SL}$	$0.217 + 0.058 \cdot \text{SL}$	$0.201 + 0.060 \cdot \text{SL}$
	$t_F$	0.250	$0.133 + 0.058 \cdot \text{SL}$	$0.128 + 0.060 \cdot \text{SL}$	$0.121 + 0.061 \cdot \text{SL}$
	$t_{PLH}$	0.160	$0.106 + 0.027 \cdot \text{SL}$	$0.108 + 0.027 \cdot \text{SL}$	$0.110 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.179	$0.120 + 0.030 \cdot \text{SL}$	$0.121 + 0.029 \cdot \text{SL}$	$0.123 + 0.029 \cdot \text{SL}$
D to Y	$t_R$	0.332	$0.218 + 0.057 \cdot \text{SL}$	$0.209 + 0.059 \cdot \text{SL}$	$0.199 + 0.060 \cdot \text{SL}$
	$t_F$	0.291	$0.174 + 0.059 \cdot \text{SL}$	$0.169 + 0.060 \cdot \text{SL}$	$0.163 + 0.061 \cdot \text{SL}$
	$t_{PLH}$	0.160	$0.106 + 0.027 \cdot \text{SL}$	$0.108 + 0.027 \cdot \text{SL}$	$0.110 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.205	$0.146 + 0.030 \cdot \text{SL}$	$0.147 + 0.029 \cdot \text{SL}$	$0.149 + 0.029 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### OA22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.264	$0.212 + 0.026 \cdot \text{SL}$	$0.204 + 0.028 \cdot \text{SL}$	$0.185 + 0.029 \cdot \text{SL}$
	$t_F$	0.217	$0.160 + 0.028 \cdot \text{SL}$	$0.156 + 0.029 \cdot \text{SL}$	$0.143 + 0.030 \cdot \text{SL}$
	$t_{PLH}$	0.115	$0.087 + 0.014 \cdot \text{SL}$	$0.091 + 0.013 \cdot \text{SL}$	$0.093 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.153	$0.124 + 0.015 \cdot \text{SL}$	$0.124 + 0.015 \cdot \text{SL}$	$0.125 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.253	$0.199 + 0.027 \cdot \text{SL}$	$0.193 + 0.029 \cdot \text{SL}$	$0.181 + 0.030 \cdot \text{SL}$
	$t_F$	0.262	$0.204 + 0.029 \cdot \text{SL}$	$0.200 + 0.030 \cdot \text{SL}$	$0.188 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.114	$0.085 + 0.014 \cdot \text{SL}$	$0.090 + 0.013 \cdot \text{SL}$	$0.092 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.180	$0.150 + 0.015 \cdot \text{SL}$	$0.151 + 0.015 \cdot \text{SL}$	$0.152 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.300	$0.248 + 0.026 \cdot \text{SL}$	$0.240 + 0.028 \cdot \text{SL}$	$0.221 + 0.029 \cdot \text{SL}$
	$t_F$	0.215	$0.155 + 0.030 \cdot \text{SL}$	$0.153 + 0.031 \cdot \text{SL}$	$0.146 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.139	$0.112 + 0.013 \cdot \text{SL}$	$0.113 + 0.013 \cdot \text{SL}$	$0.115 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.165	$0.134 + 0.015 \cdot \text{SL}$	$0.135 + 0.015 \cdot \text{SL}$	$0.138 + 0.015 \cdot \text{SL}$
D to Y	$t_R$	0.289	$0.235 + 0.027 \cdot \text{SL}$	$0.228 + 0.029 \cdot \text{SL}$	$0.218 + 0.030 \cdot \text{SL}$
	$t_F$	0.255	$0.197 + 0.029 \cdot \text{SL}$	$0.193 + 0.030 \cdot \text{SL}$	$0.186 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.138	$0.111 + 0.014 \cdot \text{SL}$	$0.112 + 0.013 \cdot \text{SL}$	$0.115 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.188	$0.158 + 0.015 \cdot \text{SL}$	$0.159 + 0.015 \cdot \text{SL}$	$0.161 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA22DH/OA22/OA22D2/OA22D2B/OA22D4

## Two 2-ORs into 2-NAND with 0.5X/1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA22D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.089	$0.060 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.057 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.260	$0.243 + 0.009 \cdot \text{SL}$	$0.249 + 0.007 \cdot \text{SL}$	$0.255 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.295	$0.275 + 0.010 \cdot \text{SL}$	$0.283 + 0.008 \cdot \text{SL}$	$0.293 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.057 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.260	$0.243 + 0.009 \cdot \text{SL}$	$0.249 + 0.007 \cdot \text{SL}$	$0.256 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.329	$0.309 + 0.010 \cdot \text{SL}$	$0.317 + 0.008 \cdot \text{SL}$	$0.327 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.089	$0.062 + 0.013 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.286	$0.269 + 0.009 \cdot \text{SL}$	$0.275 + 0.007 \cdot \text{SL}$	$0.281 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.280 + 0.010 \cdot \text{SL}$	$0.288 + 0.008 \cdot \text{SL}$	$0.298 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.054 + 0.014 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.285	$0.267 + 0.009 \cdot \text{SL}$	$0.273 + 0.007 \cdot \text{SL}$	$0.280 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.333	$0.313 + 0.010 \cdot \text{SL}$	$0.321 + 0.008 \cdot \text{SL}$	$0.331 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### OA22D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.058 + 0.007 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.282	$0.272 + 0.005 \cdot \text{SL}$	$0.277 + 0.004 \cdot \text{SL}$	$0.288 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.305	$0.294 + 0.006 \cdot \text{SL}$	$0.299 + 0.004 \cdot \text{SL}$	$0.314 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.059 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.282	$0.272 + 0.005 \cdot \text{SL}$	$0.277 + 0.004 \cdot \text{SL}$	$0.288 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.339	$0.327 + 0.006 \cdot \text{SL}$	$0.333 + 0.004 \cdot \text{SL}$	$0.348 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.083	$0.069 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_F$	0.073	$0.059 + 0.007 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.299 + 0.005 \cdot \text{SL}$	$0.304 + 0.004 \cdot \text{SL}$	$0.315 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.311	$0.299 + 0.006 \cdot \text{SL}$	$0.305 + 0.004 \cdot \text{SL}$	$0.319 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.083	$0.068 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.061 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.307	$0.297 + 0.005 \cdot \text{SL}$	$0.302 + 0.004 \cdot \text{SL}$	$0.313 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.344	$0.332 + 0.006 \cdot \text{SL}$	$0.338 + 0.004 \cdot \text{SL}$	$0.353 + 0.004 \cdot \text{SL}$

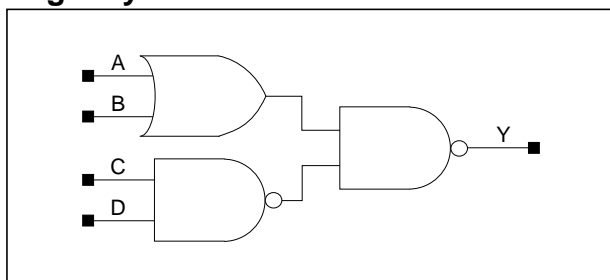
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# OA22DHA/OA22A/OA22D2A/OA22D4A

## 2-OR and 2-NAND into 2-NAND with 0.5X/1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
Other States				0

### Cell Data

Input Load (SL)															
OA22DHA				OA22A				OA22D2A				OA22D4A			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.5	0.5	0.5	0.5	1.0	1.0	0.6	0.6	2.0	1.9	0.6	0.6	1.0	1.0	0.6	0.6
Gate Count															
OA22DHA				OA22A				OA22D2A				OA22D4A			
2.00				2.00				3.00				4.00			



# OA22DHA/OA22A/OA22D2A/OA22D4A

## 2-OR and 2-NAND into 2-NAND with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA22DHA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.398	$0.147 + 0.125 \cdot \text{SL}$	$0.128 + 0.130 \cdot \text{SL}$	$0.121 + 0.131 \cdot \text{SL}$
	$t_F$	0.231	$0.098 + 0.066 \cdot \text{SL}$	$0.082 + 0.071 \cdot \text{SL}$	$0.064 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.206	$0.094 + 0.056 \cdot \text{SL}$	$0.093 + 0.056 \cdot \text{SL}$	$0.092 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.146	$0.075 + 0.036 \cdot \text{SL}$	$0.076 + 0.035 \cdot \text{SL}$	$0.075 + 0.035 \cdot \text{SL}$
B to Y	$t_R$	0.394	$0.139 + 0.127 \cdot \text{SL}$	$0.129 + 0.130 \cdot \text{SL}$	$0.121 + 0.131 \cdot \text{SL}$
	$t_F$	0.259	$0.126 + 0.066 \cdot \text{SL}$	$0.108 + 0.071 \cdot \text{SL}$	$0.090 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.206	$0.093 + 0.056 \cdot \text{SL}$	$0.093 + 0.056 \cdot \text{SL}$	$0.093 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.161	$0.090 + 0.036 \cdot \text{SL}$	$0.090 + 0.035 \cdot \text{SL}$	$0.090 + 0.036 \cdot \text{SL}$
C to Y	$t_R$	0.241	$0.113 + 0.064 \cdot \text{SL}$	$0.107 + 0.065 \cdot \text{SL}$	$0.100 + 0.066 \cdot \text{SL}$
	$t_F$	0.239	$0.095 + 0.072 \cdot \text{SL}$	$0.091 + 0.073 \cdot \text{SL}$	$0.088 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.242	$0.183 + 0.030 \cdot \text{SL}$	$0.186 + 0.029 \cdot \text{SL}$	$0.187 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.243	$0.170 + 0.036 \cdot \text{SL}$	$0.172 + 0.036 \cdot \text{SL}$	$0.174 + 0.036 \cdot \text{SL}$
D to Y	$t_R$	0.241	$0.113 + 0.064 \cdot \text{SL}$	$0.107 + 0.065 \cdot \text{SL}$	$0.100 + 0.066 \cdot \text{SL}$
	$t_F$	0.240	$0.097 + 0.072 \cdot \text{SL}$	$0.092 + 0.073 \cdot \text{SL}$	$0.088 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.237	$0.177 + 0.030 \cdot \text{SL}$	$0.181 + 0.029 \cdot \text{SL}$	$0.182 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.254	$0.181 + 0.036 \cdot \text{SL}$	$0.184 + 0.036 \cdot \text{SL}$	$0.186 + 0.036 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### OA22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.244	$0.136 + 0.054 \cdot \text{SL}$	$0.122 + 0.057 \cdot \text{SL}$	$0.109 + 0.059 \cdot \text{SL}$
	$t_F$	0.200	$0.109 + 0.046 \cdot \text{SL}$	$0.097 + 0.049 \cdot \text{SL}$	$0.084 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.129	$0.077 + 0.026 \cdot \text{SL}$	$0.080 + 0.025 \cdot \text{SL}$	$0.079 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.128	$0.078 + 0.025 \cdot \text{SL}$	$0.081 + 0.024 \cdot \text{SL}$	$0.080 + 0.024 \cdot \text{SL}$
B to Y	$t_R$	0.236	$0.125 + 0.056 \cdot \text{SL}$	$0.115 + 0.058 \cdot \text{SL}$	$0.106 + 0.059 \cdot \text{SL}$
	$t_F$	0.238	$0.146 + 0.046 \cdot \text{SL}$	$0.134 + 0.049 \cdot \text{SL}$	$0.121 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.128	$0.075 + 0.026 \cdot \text{SL}$	$0.079 + 0.026 \cdot \text{SL}$	$0.078 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.150	$0.101 + 0.024 \cdot \text{SL}$	$0.101 + 0.024 \cdot \text{SL}$	$0.101 + 0.024 \cdot \text{SL}$
C to Y	$t_R$	0.153	$0.097 + 0.028 \cdot \text{SL}$	$0.092 + 0.029 \cdot \text{SL}$	$0.088 + 0.030 \cdot \text{SL}$
	$t_F$	0.221	$0.121 + 0.050 \cdot \text{SL}$	$0.117 + 0.051 \cdot \text{SL}$	$0.114 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.189	$0.159 + 0.015 \cdot \text{SL}$	$0.164 + 0.014 \cdot \text{SL}$	$0.167 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.249	$0.198 + 0.026 \cdot \text{SL}$	$0.201 + 0.025 \cdot \text{SL}$	$0.203 + 0.025 \cdot \text{SL}$
D to Y	$t_R$	0.184	$0.129 + 0.028 \cdot \text{SL}$	$0.124 + 0.029 \cdot \text{SL}$	$0.116 + 0.030 \cdot \text{SL}$
	$t_F$	0.222	$0.122 + 0.050 \cdot \text{SL}$	$0.118 + 0.051 \cdot \text{SL}$	$0.115 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.182	$0.152 + 0.015 \cdot \text{SL}$	$0.157 + 0.014 \cdot \text{SL}$	$0.161 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.262	$0.211 + 0.026 \cdot \text{SL}$	$0.214 + 0.025 \cdot \text{SL}$	$0.216 + 0.025 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OA22DHA/OA22A/OA22D2A/OA22D4A

## 2-OR and 2-NAND into 2-NAND with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA22D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.191	$0.140 + 0.026 \cdot \text{SL}$	$0.131 + 0.028 \cdot \text{SL}$	$0.114 + 0.029 \cdot \text{SL}$
	$t_F$	0.155	$0.111 + 0.022 \cdot \text{SL}$	$0.103 + 0.024 \cdot \text{SL}$	$0.088 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.080 + 0.013 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.103	$0.075 + 0.014 \cdot \text{SL}$	$0.082 + 0.012 \cdot \text{SL}$	$0.081 + 0.012 \cdot \text{SL}$
B to Y	$t_R$	0.182	$0.129 + 0.027 \cdot \text{SL}$	$0.120 + 0.029 \cdot \text{SL}$	$0.110 + 0.030 \cdot \text{SL}$
	$t_F$	0.195	$0.151 + 0.022 \cdot \text{SL}$	$0.143 + 0.024 \cdot \text{SL}$	$0.126 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.126	$0.101 + 0.013 \cdot \text{SL}$	$0.103 + 0.012 \cdot \text{SL}$	$0.102 + 0.012 \cdot \text{SL}$
C to Y	$t_R$	0.142	$0.113 + 0.014 \cdot \text{SL}$	$0.113 + 0.014 \cdot \text{SL}$	$0.108 + 0.015 \cdot \text{SL}$
	$t_F$	0.182	$0.134 + 0.024 \cdot \text{SL}$	$0.131 + 0.025 \cdot \text{SL}$	$0.124 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.202 + 0.009 \cdot \text{SL}$	$0.207 + 0.007 \cdot \text{SL}$	$0.216 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.265	$0.238 + 0.013 \cdot \text{SL}$	$0.241 + 0.013 \cdot \text{SL}$	$0.245 + 0.012 \cdot \text{SL}$
D to Y	$t_R$	0.142	$0.113 + 0.014 \cdot \text{SL}$	$0.114 + 0.014 \cdot \text{SL}$	$0.108 + 0.015 \cdot \text{SL}$
	$t_F$	0.184	$0.136 + 0.024 \cdot \text{SL}$	$0.133 + 0.025 \cdot \text{SL}$	$0.126 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.197 + 0.009 \cdot \text{SL}$	$0.201 + 0.007 \cdot \text{SL}$	$0.211 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.278	$0.251 + 0.013 \cdot \text{SL}$	$0.254 + 0.013 \cdot \text{SL}$	$0.258 + 0.012 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### OA22D4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.078	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.007 \cdot \text{SL}$
	$t_F$	0.071	$0.057 + 0.007 \cdot \text{SL}$	$0.059 + 0.006 \cdot \text{SL}$	$0.057 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.253 + 0.005 \cdot \text{SL}$	$0.258 + 0.004 \cdot \text{SL}$	$0.268 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.254	$0.243 + 0.006 \cdot \text{SL}$	$0.248 + 0.004 \cdot \text{SL}$	$0.263 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.078	$0.063 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.057 + 0.007 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.262	$0.252 + 0.005 \cdot \text{SL}$	$0.257 + 0.004 \cdot \text{SL}$	$0.268 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.282	$0.271 + 0.006 \cdot \text{SL}$	$0.277 + 0.004 \cdot \text{SL}$	$0.291 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.075	$0.061 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$	$0.053 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.058 + 0.007 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.326	$0.316 + 0.005 \cdot \text{SL}$	$0.321 + 0.004 \cdot \text{SL}$	$0.331 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.382	$0.371 + 0.006 \cdot \text{SL}$	$0.377 + 0.004 \cdot \text{SL}$	$0.391 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.076	$0.061 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$	$0.053 + 0.008 \cdot \text{SL}$
	$t_F$	0.073	$0.060 + 0.006 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.320	$0.310 + 0.005 \cdot \text{SL}$	$0.315 + 0.004 \cdot \text{SL}$	$0.325 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.396	$0.384 + 0.006 \cdot \text{SL}$	$0.390 + 0.004 \cdot \text{SL}$	$0.404 + 0.004 \cdot \text{SL}$

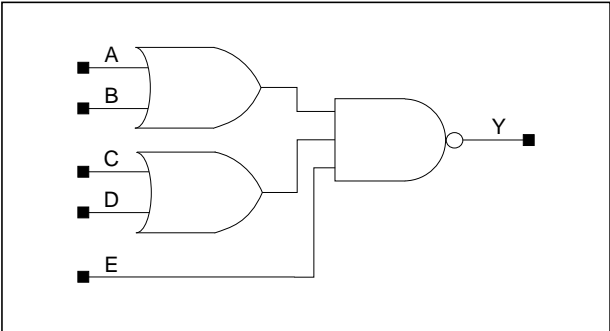
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OA221/OA221D2/OA221D4

Two 2-ORs into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)															
OA221					OA221D2					OA221D4					
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E	
1.0	1.0	1.0	1.2	1.0	1.0	1.0	1.0	1.2	1.0	1.0	1.0	1.0	1.2	1.0	
Gate Count															
OA221					OA221D2					OA221D4					
2.00					3.00					3.67					



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA221**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.342	$0.232 + 0.055 \cdot \text{SL}$	$0.222 + 0.058 \cdot \text{SL}$	$0.209 + 0.059 \cdot \text{SL}$
	$t_F$	0.340	$0.211 + 0.065 \cdot \text{SL}$	$0.205 + 0.066 \cdot \text{SL}$	$0.196 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.155	$0.103 + 0.026 \cdot \text{SL}$	$0.104 + 0.026 \cdot \text{SL}$	$0.106 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.200	$0.137 + 0.031 \cdot \text{SL}$	$0.138 + 0.031 \cdot \text{SL}$	$0.138 + 0.031 \cdot \text{SL}$
B to Y	$t_R$	0.335	$0.222 + 0.056 \cdot \text{SL}$	$0.214 + 0.058 \cdot \text{SL}$	$0.207 + 0.059 \cdot \text{SL}$
	$t_F$	0.389	$0.259 + 0.065 \cdot \text{SL}$	$0.253 + 0.066 \cdot \text{SL}$	$0.244 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.156	$0.103 + 0.027 \cdot \text{SL}$	$0.104 + 0.026 \cdot \text{SL}$	$0.107 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.229	$0.166 + 0.031 \cdot \text{SL}$	$0.167 + 0.031 \cdot \text{SL}$	$0.167 + 0.031 \cdot \text{SL}$
C to Y	$t_R$	0.377	$0.267 + 0.055 \cdot \text{SL}$	$0.257 + 0.058 \cdot \text{SL}$	$0.243 + 0.059 \cdot \text{SL}$
	$t_F$	0.339	$0.209 + 0.065 \cdot \text{SL}$	$0.205 + 0.066 \cdot \text{SL}$	$0.198 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.178	$0.126 + 0.026 \cdot \text{SL}$	$0.127 + 0.026 \cdot \text{SL}$	$0.129 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.215	$0.152 + 0.031 \cdot \text{SL}$	$0.154 + 0.031 \cdot \text{SL}$	$0.156 + 0.031 \cdot \text{SL}$
D to Y	$t_R$	0.370	$0.256 + 0.057 \cdot \text{SL}$	$0.250 + 0.058 \cdot \text{SL}$	$0.243 + 0.059 \cdot \text{SL}$
	$t_F$	0.388	$0.256 + 0.066 \cdot \text{SL}$	$0.253 + 0.067 \cdot \text{SL}$	$0.246 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.180	$0.128 + 0.026 \cdot \text{SL}$	$0.129 + 0.026 \cdot \text{SL}$	$0.131 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.248	$0.184 + 0.032 \cdot \text{SL}$	$0.186 + 0.031 \cdot \text{SL}$	$0.187 + 0.031 \cdot \text{SL}$
E to Y	$t_R$	0.237	$0.185 + 0.026 \cdot \text{SL}$	$0.178 + 0.028 \cdot \text{SL}$	$0.166 + 0.029 \cdot \text{SL}$
	$t_F$	0.385	$0.252 + 0.066 \cdot \text{SL}$	$0.249 + 0.067 \cdot \text{SL}$	$0.245 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.128	$0.101 + 0.014 \cdot \text{SL}$	$0.103 + 0.013 \cdot \text{SL}$	$0.104 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.255	$0.191 + 0.032 \cdot \text{SL}$	$0.193 + 0.031 \cdot \text{SL}$	$0.195 + 0.031 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## OA221/OA221D2/OA221D4

### Two 2-ORs into 3-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA221D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.090	$0.062 + 0.014 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.060 + 0.013 \cdot \text{SL}$	$0.061 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.286	$0.268 + 0.009 \cdot \text{SL}$	$0.274 + 0.007 \cdot \text{SL}$	$0.281 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.333	$0.314 + 0.010 \cdot \text{SL}$	$0.322 + 0.008 \cdot \text{SL}$	$0.333 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.014 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.285	$0.268 + 0.009 \cdot \text{SL}$	$0.274 + 0.007 \cdot \text{SL}$	$0.281 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.369	$0.349 + 0.010 \cdot \text{SL}$	$0.358 + 0.008 \cdot \text{SL}$	$0.369 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.091	$0.064 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.059 + 0.013 \cdot \text{SL}$	$0.063 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.313	$0.295 + 0.009 \cdot \text{SL}$	$0.301 + 0.007 \cdot \text{SL}$	$0.308 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.347	$0.328 + 0.010 \cdot \text{SL}$	$0.336 + 0.008 \cdot \text{SL}$	$0.346 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.092	$0.064 + 0.014 \cdot \text{SL}$	$0.063 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.013 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.314	$0.297 + 0.009 \cdot \text{SL}$	$0.303 + 0.007 \cdot \text{SL}$	$0.309 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.387	$0.367 + 0.010 \cdot \text{SL}$	$0.376 + 0.008 \cdot \text{SL}$	$0.387 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.088	$0.060 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.061 + 0.013 \cdot \text{SL}$	$0.063 + 0.012 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.265	$0.247 + 0.009 \cdot \text{SL}$	$0.253 + 0.007 \cdot \text{SL}$	$0.259 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.395	$0.375 + 0.010 \cdot \text{SL}$	$0.383 + 0.008 \cdot \text{SL}$	$0.394 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA221D4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.084	$0.069 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.308	$0.298 + 0.005 \cdot \text{SL}$	$0.303 + 0.004 \cdot \text{SL}$	$0.314 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.345	$0.334 + 0.006 \cdot \text{SL}$	$0.340 + 0.004 \cdot \text{SL}$	$0.355 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.084	$0.071 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.308	$0.297 + 0.005 \cdot \text{SL}$	$0.303 + 0.004 \cdot \text{SL}$	$0.314 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.381	$0.369 + 0.006 \cdot \text{SL}$	$0.376 + 0.004 \cdot \text{SL}$	$0.391 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.086	$0.073 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.336	$0.325 + 0.005 \cdot \text{SL}$	$0.331 + 0.004 \cdot \text{SL}$	$0.342 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.362	$0.351 + 0.006 \cdot \text{SL}$	$0.357 + 0.004 \cdot \text{SL}$	$0.372 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.338	$0.327 + 0.005 \cdot \text{SL}$	$0.333 + 0.004 \cdot \text{SL}$	$0.344 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.398	$0.386 + 0.006 \cdot \text{SL}$	$0.392 + 0.004 \cdot \text{SL}$	$0.407 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.057 + 0.008 \cdot \text{SL}$
	$t_F$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.280	$0.270 + 0.005 \cdot \text{SL}$	$0.275 + 0.004 \cdot \text{SL}$	$0.286 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.407	$0.395 + 0.006 \cdot \text{SL}$	$0.401 + 0.004 \cdot \text{SL}$	$0.416 + 0.004 \cdot \text{SL}$

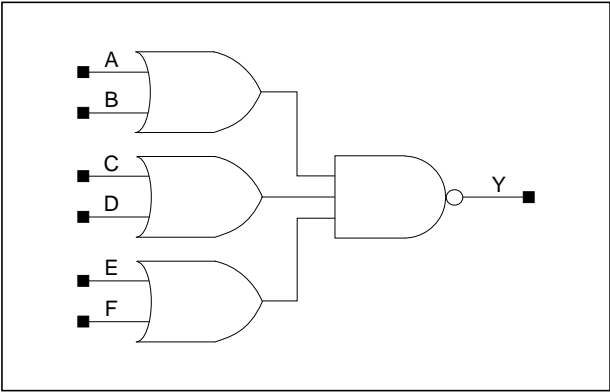
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OA222/OA222D2/OA222D2B/OA222D4

Three 2-ORs into 3-NAND with 1X/2X/2X(Buffered)/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
Other States						0

Cell Data

Input Load (SL)												Gate Count	
OA222						OA222D2						OA222	OA222D2
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	1.0	1.0	1.0	0.9	1.0	1.8	2.1	1.8	2.0	1.8	2.0	2.67	4.67
OA222D2B						OA222D4						OA222D2B	OA222D4
A	B	C	D	E	F	A	B	C	D	E	F		
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	0.9	1.0	3.67	4.33



# OA222/OA222D2/OA222D2B/OA222D4

## Three 2-ORs into 3-NAND with 1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.408	$0.298 + 0.055 \cdot \text{SL}$	$0.288 + 0.057 \cdot \text{SL}$	$0.274 + 0.059 \cdot \text{SL}$
	$t_F$	0.423	$0.280 + 0.072 \cdot \text{SL}$	$0.274 + 0.073 \cdot \text{SL}$	$0.270 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.167	$0.114 + 0.027 \cdot \text{SL}$	$0.116 + 0.026 \cdot \text{SL}$	$0.119 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.254	$0.185 + 0.034 \cdot \text{SL}$	$0.186 + 0.034 \cdot \text{SL}$	$0.187 + 0.034 \cdot \text{SL}$
B to Y	$t_R$	0.401	$0.288 + 0.056 \cdot \text{SL}$	$0.281 + 0.058 \cdot \text{SL}$	$0.273 + 0.059 \cdot \text{SL}$
	$t_F$	0.471	$0.328 + 0.071 \cdot \text{SL}$	$0.323 + 0.073 \cdot \text{SL}$	$0.318 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.167	$0.113 + 0.027 \cdot \text{SL}$	$0.115 + 0.026 \cdot \text{SL}$	$0.119 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.282	$0.214 + 0.034 \cdot \text{SL}$	$0.215 + 0.034 \cdot \text{SL}$	$0.216 + 0.034 \cdot \text{SL}$
C to Y	$t_R$	0.447	$0.337 + 0.055 \cdot \text{SL}$	$0.327 + 0.057 \cdot \text{SL}$	$0.313 + 0.059 \cdot \text{SL}$
	$t_F$	0.422	$0.278 + 0.072 \cdot \text{SL}$	$0.274 + 0.073 \cdot \text{SL}$	$0.271 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.196	$0.143 + 0.027 \cdot \text{SL}$	$0.144 + 0.026 \cdot \text{SL}$	$0.147 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.278	$0.209 + 0.035 \cdot \text{SL}$	$0.211 + 0.034 \cdot \text{SL}$	$0.213 + 0.034 \cdot \text{SL}$
D to Y	$t_R$	0.440	$0.327 + 0.057 \cdot \text{SL}$	$0.320 + 0.058 \cdot \text{SL}$	$0.313 + 0.059 \cdot \text{SL}$
	$t_F$	0.472	$0.328 + 0.072 \cdot \text{SL}$	$0.325 + 0.073 \cdot \text{SL}$	$0.322 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.198	$0.144 + 0.027 \cdot \text{SL}$	$0.146 + 0.026 \cdot \text{SL}$	$0.150 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.310	$0.241 + 0.034 \cdot \text{SL}$	$0.243 + 0.034 \cdot \text{SL}$	$0.245 + 0.034 \cdot \text{SL}$
E to Y	$t_R$	0.488	$0.379 + 0.055 \cdot \text{SL}$	$0.368 + 0.057 \cdot \text{SL}$	$0.353 + 0.059 \cdot \text{SL}$
	$t_F$	0.421	$0.277 + 0.072 \cdot \text{SL}$	$0.274 + 0.073 \cdot \text{SL}$	$0.271 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.215	$0.161 + 0.027 \cdot \text{SL}$	$0.164 + 0.026 \cdot \text{SL}$	$0.167 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.288	$0.218 + 0.035 \cdot \text{SL}$	$0.220 + 0.034 \cdot \text{SL}$	$0.223 + 0.034 \cdot \text{SL}$
F to Y	$t_R$	0.481	$0.369 + 0.056 \cdot \text{SL}$	$0.361 + 0.058 \cdot \text{SL}$	$0.353 + 0.059 \cdot \text{SL}$
	$t_F$	0.470	$0.326 + 0.072 \cdot \text{SL}$	$0.324 + 0.073 \cdot \text{SL}$	$0.322 + 0.073 \cdot \text{SL}$
	$t_{PLH}$	0.216	$0.162 + 0.027 \cdot \text{SL}$	$0.164 + 0.026 \cdot \text{SL}$	$0.168 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.320	$0.251 + 0.034 \cdot \text{SL}$	$0.252 + 0.034 \cdot \text{SL}$	$0.254 + 0.034 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OA222/OA222D2/OA222D2B/OA222D4

## Three 2-ORs into 3-NAND with 1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.353	$0.300 + 0.027 \cdot \text{SL}$	$0.293 + 0.028 \cdot \text{SL}$	$0.276 + 0.029 \cdot \text{SL}$
	$t_F$	0.348	$0.277 + 0.035 \cdot \text{SL}$	$0.274 + 0.036 \cdot \text{SL}$	$0.266 + 0.037 \cdot \text{SL}$
	$t_{PLH}$	0.140	$0.113 + 0.014 \cdot \text{SL}$	$0.114 + 0.013 \cdot \text{SL}$	$0.118 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.218	$0.183 + 0.017 \cdot \text{SL}$	$0.184 + 0.017 \cdot \text{SL}$	$0.186 + 0.017 \cdot \text{SL}$
B to Y	$t_R$	0.344	$0.289 + 0.027 \cdot \text{SL}$	$0.283 + 0.029 \cdot \text{SL}$	$0.274 + 0.030 \cdot \text{SL}$
	$t_F$	0.397	$0.326 + 0.035 \cdot \text{SL}$	$0.323 + 0.036 \cdot \text{SL}$	$0.316 + 0.037 \cdot \text{SL}$
	$t_{PLH}$	0.141	$0.113 + 0.014 \cdot \text{SL}$	$0.115 + 0.013 \cdot \text{SL}$	$0.120 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.250	$0.216 + 0.017 \cdot \text{SL}$	$0.216 + 0.017 \cdot \text{SL}$	$0.217 + 0.017 \cdot \text{SL}$
C to Y	$t_R$	0.387	$0.333 + 0.027 \cdot \text{SL}$	$0.327 + 0.028 \cdot \text{SL}$	$0.311 + 0.030 \cdot \text{SL}$
	$t_F$	0.349	$0.278 + 0.036 \cdot \text{SL}$	$0.276 + 0.036 \cdot \text{SL}$	$0.270 + 0.037 \cdot \text{SL}$
	$t_{PLH}$	0.164	$0.137 + 0.013 \cdot \text{SL}$	$0.138 + 0.013 \cdot \text{SL}$	$0.141 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.237	$0.202 + 0.018 \cdot \text{SL}$	$0.203 + 0.017 \cdot \text{SL}$	$0.206 + 0.017 \cdot \text{SL}$
D to Y	$t_R$	0.378	$0.322 + 0.028 \cdot \text{SL}$	$0.318 + 0.029 \cdot \text{SL}$	$0.308 + 0.030 \cdot \text{SL}$
	$t_F$	0.397	$0.326 + 0.036 \cdot \text{SL}$	$0.324 + 0.036 \cdot \text{SL}$	$0.319 + 0.037 \cdot \text{SL}$
	$t_{PLH}$	0.165	$0.139 + 0.013 \cdot \text{SL}$	$0.139 + 0.013 \cdot \text{SL}$	$0.143 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.268	$0.234 + 0.017 \cdot \text{SL}$	$0.234 + 0.017 \cdot \text{SL}$	$0.237 + 0.017 \cdot \text{SL}$
E to Y	$t_R$	0.429	$0.376 + 0.027 \cdot \text{SL}$	$0.370 + 0.028 \cdot \text{SL}$	$0.352 + 0.029 \cdot \text{SL}$
	$t_F$	0.346	$0.274 + 0.036 \cdot \text{SL}$	$0.273 + 0.036 \cdot \text{SL}$	$0.269 + 0.037 \cdot \text{SL}$
	$t_{PLH}$	0.186	$0.158 + 0.014 \cdot \text{SL}$	$0.160 + 0.013 \cdot \text{SL}$	$0.163 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.249	$0.214 + 0.018 \cdot \text{SL}$	$0.216 + 0.017 \cdot \text{SL}$	$0.219 + 0.017 \cdot \text{SL}$
F to Y	$t_R$	0.420	$0.365 + 0.028 \cdot \text{SL}$	$0.360 + 0.029 \cdot \text{SL}$	$0.350 + 0.030 \cdot \text{SL}$
	$t_F$	0.394	$0.322 + 0.036 \cdot \text{SL}$	$0.321 + 0.036 \cdot \text{SL}$	$0.318 + 0.037 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.160 + 0.014 \cdot \text{SL}$	$0.161 + 0.013 \cdot \text{SL}$	$0.166 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.282	$0.247 + 0.017 \cdot \text{SL}$	$0.249 + 0.017 \cdot \text{SL}$	$0.251 + 0.017 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA222/OA222D2/OA222D2B/OA222D4

## Three 2-ORs into 3-NAND with 1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA222D2B

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.095	$0.067 + 0.014 \cdot \text{SL}$	$0.067 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.064 + 0.012 \cdot \text{SL}$	$0.064 + 0.012 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.310	$0.292 + 0.009 \cdot \text{SL}$	$0.298 + 0.007 \cdot \text{SL}$	$0.305 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.400	$0.380 + 0.010 \cdot \text{SL}$	$0.388 + 0.008 \cdot \text{SL}$	$0.399 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.095	$0.067 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.064 + 0.013 \cdot \text{SL}$	$0.069 + 0.012 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.291 + 0.009 \cdot \text{SL}$	$0.297 + 0.007 \cdot \text{SL}$	$0.304 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.437	$0.417 + 0.010 \cdot \text{SL}$	$0.425 + 0.008 \cdot \text{SL}$	$0.436 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.096	$0.068 + 0.014 \cdot \text{SL}$	$0.068 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.064 + 0.013 \cdot \text{SL}$	$0.064 + 0.012 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.341	$0.324 + 0.009 \cdot \text{SL}$	$0.330 + 0.007 \cdot \text{SL}$	$0.337 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.423	$0.404 + 0.010 \cdot \text{SL}$	$0.411 + 0.008 \cdot \text{SL}$	$0.422 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.096	$0.069 + 0.014 \cdot \text{SL}$	$0.068 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.066 + 0.012 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.343	$0.326 + 0.009 \cdot \text{SL}$	$0.332 + 0.007 \cdot \text{SL}$	$0.339 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.464	$0.445 + 0.010 \cdot \text{SL}$	$0.453 + 0.008 \cdot \text{SL}$	$0.464 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.070 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.066 + 0.012 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.365	$0.347 + 0.009 \cdot \text{SL}$	$0.354 + 0.007 \cdot \text{SL}$	$0.361 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.434	$0.415 + 0.010 \cdot \text{SL}$	$0.423 + 0.008 \cdot \text{SL}$	$0.434 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.070 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.064 + 0.013 \cdot \text{SL}$	$0.069 + 0.012 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.365	$0.348 + 0.009 \cdot \text{SL}$	$0.354 + 0.007 \cdot \text{SL}$	$0.361 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.475	$0.455 + 0.010 \cdot \text{SL}$	$0.463 + 0.008 \cdot \text{SL}$	$0.474 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA222/OA222D2/OA222D2B/OA222D4

## Three 2-ORs into 3-NAND with 1X/2X/2X(Buffered)/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA222D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.088	$0.075 + 0.007 \cdot \text{SL}$	$0.074 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.081	$0.068 + 0.007 \cdot \text{SL}$	$0.069 + 0.006 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.334	$0.323 + 0.005 \cdot \text{SL}$	$0.329 + 0.004 \cdot \text{SL}$	$0.340 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.414	$0.402 + 0.006 \cdot \text{SL}$	$0.408 + 0.004 \cdot \text{SL}$	$0.423 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.088	$0.075 + 0.007 \cdot \text{SL}$	$0.074 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.083	$0.069 + 0.007 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.333	$0.322 + 0.005 \cdot \text{SL}$	$0.328 + 0.004 \cdot \text{SL}$	$0.340 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.450	$0.438 + 0.006 \cdot \text{SL}$	$0.444 + 0.004 \cdot \text{SL}$	$0.459 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.081	$0.068 + 0.007 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.366	$0.355 + 0.005 \cdot \text{SL}$	$0.361 + 0.004 \cdot \text{SL}$	$0.373 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.437	$0.426 + 0.006 \cdot \text{SL}$	$0.431 + 0.004 \cdot \text{SL}$	$0.447 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.090	$0.078 + 0.006 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$
	$t_F$	0.083	$0.070 + 0.007 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.368	$0.357 + 0.005 \cdot \text{SL}$	$0.363 + 0.004 \cdot \text{SL}$	$0.375 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.478	$0.467 + 0.006 \cdot \text{SL}$	$0.472 + 0.004 \cdot \text{SL}$	$0.488 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.091	$0.078 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.081	$0.067 + 0.007 \cdot \text{SL}$	$0.069 + 0.006 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.390	$0.379 + 0.005 \cdot \text{SL}$	$0.385 + 0.004 \cdot \text{SL}$	$0.397 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.447	$0.436 + 0.006 \cdot \text{SL}$	$0.442 + 0.004 \cdot \text{SL}$	$0.457 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.091	$0.077 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.083	$0.070 + 0.007 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.390	$0.380 + 0.005 \cdot \text{SL}$	$0.385 + 0.004 \cdot \text{SL}$	$0.398 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.488	$0.476 + 0.006 \cdot \text{SL}$	$0.482 + 0.004 \cdot \text{SL}$	$0.497 + 0.004 \cdot \text{SL}$

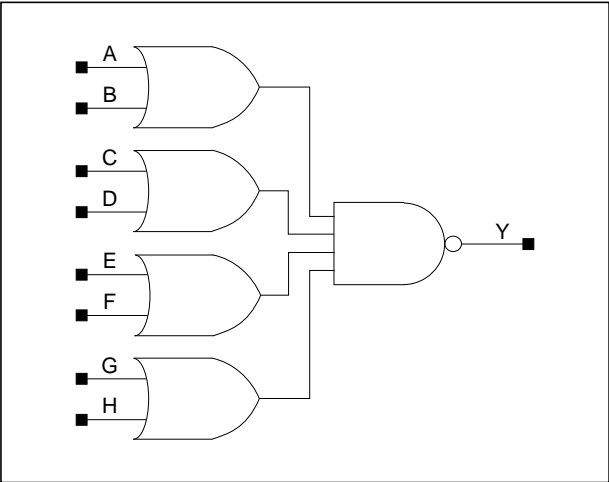
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OA2222/OA2222D2/OA2222D4

Four 2-ORs into 4-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
OA2222								OA2222
A	B	C	D	E	F	G	H	
0.9	1.0	0.9	1.0	1.0	1.0	1.1	1.0	3.33
OA2222D2								OA2222D2
A	B	C	D	E	F	G	H	
1.0	1.0	0.9	1.0	0.9	1.0	1.1	1.0	4.33
OA2222D4								OA2222D4
A	B	C	D	E	F	G	H	
1.0	1.0	0.9	1.0	1.0	1.0	1.1	1.0	5.00



# OA2222/OA2222D2/OA2222D4

## Four 2-ORs into 4-NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.484	$0.374 + 0.055 \cdot \text{SL}$	$0.365 + 0.058 \cdot \text{SL}$	$0.351 + 0.059 \cdot \text{SL}$
	$t_F$	0.477	$0.324 + 0.076 \cdot \text{SL}$	$0.319 + 0.078 \cdot \text{SL}$	$0.316 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.188	$0.134 + 0.027 \cdot \text{SL}$	$0.136 + 0.026 \cdot \text{SL}$	$0.140 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.268	$0.196 + 0.036 \cdot \text{SL}$	$0.197 + 0.036 \cdot \text{SL}$	$0.198 + 0.036 \cdot \text{SL}$
B to Y	$t_R$	0.477	$0.364 + 0.057 \cdot \text{SL}$	$0.357 + 0.058 \cdot \text{SL}$	$0.351 + 0.059 \cdot \text{SL}$
	$t_F$	0.531	$0.377 + 0.077 \cdot \text{SL}$	$0.372 + 0.078 \cdot \text{SL}$	$0.369 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.189	$0.135 + 0.027 \cdot \text{SL}$	$0.137 + 0.026 \cdot \text{SL}$	$0.142 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.302	$0.230 + 0.036 \cdot \text{SL}$	$0.231 + 0.036 \cdot \text{SL}$	$0.232 + 0.036 \cdot \text{SL}$
C to Y	$t_R$	0.536	$0.424 + 0.056 \cdot \text{SL}$	$0.414 + 0.058 \cdot \text{SL}$	$0.401 + 0.060 \cdot \text{SL}$
	$t_F$	0.480	$0.327 + 0.076 \cdot \text{SL}$	$0.323 + 0.078 \cdot \text{SL}$	$0.320 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.223	$0.169 + 0.027 \cdot \text{SL}$	$0.171 + 0.026 \cdot \text{SL}$	$0.174 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.303	$0.230 + 0.036 \cdot \text{SL}$	$0.232 + 0.036 \cdot \text{SL}$	$0.234 + 0.036 \cdot \text{SL}$
D to Y	$t_R$	0.530	$0.415 + 0.058 \cdot \text{SL}$	$0.409 + 0.059 \cdot \text{SL}$	$0.401 + 0.060 \cdot \text{SL}$
	$t_F$	0.535	$0.381 + 0.077 \cdot \text{SL}$	$0.378 + 0.078 \cdot \text{SL}$	$0.375 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.225	$0.171 + 0.027 \cdot \text{SL}$	$0.173 + 0.027 \cdot \text{SL}$	$0.177 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.338	$0.265 + 0.036 \cdot \text{SL}$	$0.267 + 0.036 \cdot \text{SL}$	$0.269 + 0.036 \cdot \text{SL}$
E to Y	$t_R$	0.577	$0.466 + 0.056 \cdot \text{SL}$	$0.456 + 0.058 \cdot \text{SL}$	$0.442 + 0.060 \cdot \text{SL}$
	$t_F$	0.481	$0.327 + 0.077 \cdot \text{SL}$	$0.324 + 0.078 \cdot \text{SL}$	$0.322 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.246	$0.192 + 0.027 \cdot \text{SL}$	$0.194 + 0.027 \cdot \text{SL}$	$0.197 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.319	$0.246 + 0.037 \cdot \text{SL}$	$0.248 + 0.036 \cdot \text{SL}$	$0.251 + 0.036 \cdot \text{SL}$
F to Y	$t_R$	0.572	$0.457 + 0.057 \cdot \text{SL}$	$0.451 + 0.059 \cdot \text{SL}$	$0.443 + 0.060 \cdot \text{SL}$
	$t_F$	0.534	$0.379 + 0.077 \cdot \text{SL}$	$0.377 + 0.078 \cdot \text{SL}$	$0.375 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.247	$0.193 + 0.027 \cdot \text{SL}$	$0.195 + 0.027 \cdot \text{SL}$	$0.198 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.353	$0.281 + 0.036 \cdot \text{SL}$	$0.282 + 0.036 \cdot \text{SL}$	$0.284 + 0.036 \cdot \text{SL}$
G to Y	$t_R$	0.616	$0.505 + 0.056 \cdot \text{SL}$	$0.496 + 0.058 \cdot \text{SL}$	$0.481 + 0.060 \cdot \text{SL}$
	$t_F$	0.614	$0.438 + 0.088 \cdot \text{SL}$	$0.437 + 0.088 \cdot \text{SL}$	$0.435 + 0.088 \cdot \text{SL}$
	$t_{PLH}$	0.264	$0.209 + 0.027 \cdot \text{SL}$	$0.211 + 0.027 \cdot \text{SL}$	$0.215 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.422	$0.339 + 0.041 \cdot \text{SL}$	$0.341 + 0.041 \cdot \text{SL}$	$0.344 + 0.040 \cdot \text{SL}$
H to Y	$t_R$	0.611	$0.496 + 0.057 \cdot \text{SL}$	$0.490 + 0.059 \cdot \text{SL}$	$0.482 + 0.060 \cdot \text{SL}$
	$t_F$	0.678	$0.501 + 0.089 \cdot \text{SL}$	$0.500 + 0.089 \cdot \text{SL}$	$0.499 + 0.089 \cdot \text{SL}$
	$t_{PLH}$	0.264	$0.209 + 0.028 \cdot \text{SL}$	$0.212 + 0.027 \cdot \text{SL}$	$0.216 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.460	$0.378 + 0.041 \cdot \text{SL}$	$0.380 + 0.041 \cdot \text{SL}$	$0.382 + 0.040 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OA2222/OA2222D2/OA2222D4

## Four 2-ORs into 4-NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA2222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.098	$0.071 + 0.013 \cdot \text{SL}$	$0.067 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.065 + 0.013 \cdot \text{SL}$	$0.066 + 0.012 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.339	$0.321 + 0.009 \cdot \text{SL}$	$0.328 + 0.007 \cdot \text{SL}$	$0.335 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.422	$0.402 + 0.010 \cdot \text{SL}$	$0.410 + 0.008 \cdot \text{SL}$	$0.421 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.098	$0.072 + 0.013 \cdot \text{SL}$	$0.067 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.063 + 0.013 \cdot \text{SL}$	$0.069 + 0.012 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.340	$0.322 + 0.009 \cdot \text{SL}$	$0.329 + 0.007 \cdot \text{SL}$	$0.336 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.464	$0.444 + 0.010 \cdot \text{SL}$	$0.452 + 0.008 \cdot \text{SL}$	$0.464 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.100	$0.074 + 0.013 \cdot \text{SL}$	$0.070 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.063 + 0.013 \cdot \text{SL}$	$0.069 + 0.012 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.360 + 0.009 \cdot \text{SL}$	$0.367 + 0.007 \cdot \text{SL}$	$0.375 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.456	$0.437 + 0.010 \cdot \text{SL}$	$0.445 + 0.008 \cdot \text{SL}$	$0.456 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.100	$0.072 + 0.014 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.066 + 0.013 \cdot \text{SL}$	$0.070 + 0.012 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.381	$0.363 + 0.009 \cdot \text{SL}$	$0.369 + 0.007 \cdot \text{SL}$	$0.377 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.499	$0.479 + 0.010 \cdot \text{SL}$	$0.488 + 0.008 \cdot \text{SL}$	$0.499 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.102	$0.076 + 0.013 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.064 + 0.013 \cdot \text{SL}$	$0.066 + 0.012 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.403	$0.385 + 0.009 \cdot \text{SL}$	$0.392 + 0.007 \cdot \text{SL}$	$0.400 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.468	$0.448 + 0.010 \cdot \text{SL}$	$0.456 + 0.008 \cdot \text{SL}$	$0.468 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.102	$0.076 + 0.013 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.066 + 0.013 \cdot \text{SL}$	$0.070 + 0.012 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.406	$0.387 + 0.009 \cdot \text{SL}$	$0.395 + 0.007 \cdot \text{SL}$	$0.402 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.515	$0.495 + 0.010 \cdot \text{SL}$	$0.503 + 0.008 \cdot \text{SL}$	$0.515 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.104	$0.079 + 0.013 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.070 + 0.012 \cdot \text{SL}$	$0.071 + 0.012 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.426	$0.407 + 0.009 \cdot \text{SL}$	$0.415 + 0.007 \cdot \text{SL}$	$0.423 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.589	$0.569 + 0.010 \cdot \text{SL}$	$0.578 + 0.008 \cdot \text{SL}$	$0.590 + 0.007 \cdot \text{SL}$
H to Y	$t_R$	0.104	$0.078 + 0.013 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.099	$0.073 + 0.013 \cdot \text{SL}$	$0.077 + 0.012 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.428	$0.409 + 0.009 \cdot \text{SL}$	$0.416 + 0.007 \cdot \text{SL}$	$0.425 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.639	$0.619 + 0.010 \cdot \text{SL}$	$0.628 + 0.008 \cdot \text{SL}$	$0.640 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA2222/OA2222D2/OA2222D4

## Four 2-ORs into 4-NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA2222D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.092	$0.079 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.083	$0.070 + 0.007 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.366	$0.355 + 0.005 \cdot \text{SL}$	$0.361 + 0.004 \cdot \text{SL}$	$0.373 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.429	$0.418 + 0.006 \cdot \text{SL}$	$0.424 + 0.004 \cdot \text{SL}$	$0.439 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.092	$0.078 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.072 + 0.006 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$	$0.069 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.367	$0.356 + 0.005 \cdot \text{SL}$	$0.361 + 0.004 \cdot \text{SL}$	$0.374 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.470	$0.459 + 0.006 \cdot \text{SL}$	$0.465 + 0.004 \cdot \text{SL}$	$0.480 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.094	$0.081 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.082	$0.069 + 0.007 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.407	$0.396 + 0.005 \cdot \text{SL}$	$0.402 + 0.004 \cdot \text{SL}$	$0.415 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.465	$0.453 + 0.006 \cdot \text{SL}$	$0.459 + 0.004 \cdot \text{SL}$	$0.474 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.094	$0.081 + 0.006 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.072 + 0.006 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$	$0.069 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.409	$0.398 + 0.005 \cdot \text{SL}$	$0.404 + 0.004 \cdot \text{SL}$	$0.417 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.506	$0.494 + 0.006 \cdot \text{SL}$	$0.501 + 0.004 \cdot \text{SL}$	$0.516 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.096	$0.083 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.083	$0.070 + 0.007 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.430	$0.419 + 0.005 \cdot \text{SL}$	$0.425 + 0.004 \cdot \text{SL}$	$0.438 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.480	$0.468 + 0.006 \cdot \text{SL}$	$0.475 + 0.004 \cdot \text{SL}$	$0.490 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.096	$0.083 + 0.006 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.072 + 0.007 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.430	$0.419 + 0.005 \cdot \text{SL}$	$0.425 + 0.004 \cdot \text{SL}$	$0.439 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.522	$0.510 + 0.006 \cdot \text{SL}$	$0.516 + 0.004 \cdot \text{SL}$	$0.531 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.097	$0.084 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.088	$0.075 + 0.007 \cdot \text{SL}$	$0.078 + 0.006 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.453	$0.442 + 0.006 \cdot \text{SL}$	$0.449 + 0.004 \cdot \text{SL}$	$0.462 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.597	$0.586 + 0.006 \cdot \text{SL}$	$0.592 + 0.004 \cdot \text{SL}$	$0.608 + 0.004 \cdot \text{SL}$
H to Y	$t_R$	0.099	$0.086 + 0.006 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_F$	0.092	$0.078 + 0.007 \cdot \text{SL}$	$0.081 + 0.006 \cdot \text{SL}$	$0.075 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.454	$0.443 + 0.006 \cdot \text{SL}$	$0.449 + 0.004 \cdot \text{SL}$	$0.463 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.644	$0.632 + 0.006 \cdot \text{SL}$	$0.639 + 0.004 \cdot \text{SL}$	$0.654 + 0.004 \cdot \text{SL}$

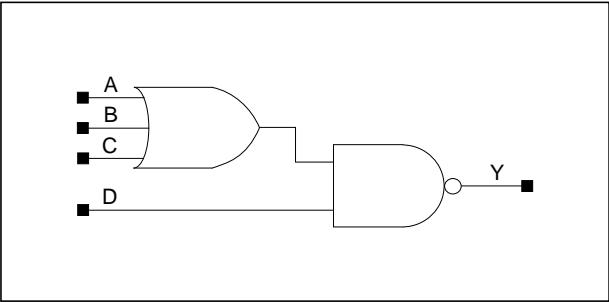
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OA31DH/OA31/OA31D2/OA31D4

3-OR into 2-NAND with 0.5X/1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)															
OA31DH				OA31				OA31D2				OA31D4			
A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0.6	0.6	0.6	0.6	0.8	0.9	0.9	0.9	1.8	1.8	1.7	1.7	0.9	0.9	0.9	0.9
Gate Count															
OA31DH				OA31				OA31D2				OA31D4			
2.00				2.00				2.67				3.33			



# OA31DH/OA31/OA31D2/OA31D4

## 3-OR into 2-NAND with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA31DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.611	$0.283 + 0.164 \cdot \text{SL}$	$0.270 + 0.168 \cdot \text{SL}$	$0.272 + 0.167 \cdot \text{SL}$
	$t_F$	0.268	$0.129 + 0.070 \cdot \text{SL}$	$0.116 + 0.073 \cdot \text{SL}$	$0.101 + 0.075 \cdot \text{SL}$
	$t_{PLH}$	0.275	$0.132 + 0.072 \cdot \text{SL}$	$0.131 + 0.072 \cdot \text{SL}$	$0.130 + 0.072 \cdot \text{SL}$
	$t_{PHL}$	0.171	$0.099 + 0.036 \cdot \text{SL}$	$0.098 + 0.036 \cdot \text{SL}$	$0.098 + 0.036 \cdot \text{SL}$
B to Y	$t_R$	0.615	$0.286 + 0.164 \cdot \text{SL}$	$0.275 + 0.167 \cdot \text{SL}$	$0.273 + 0.167 \cdot \text{SL}$
	$t_F$	0.299	$0.160 + 0.070 \cdot \text{SL}$	$0.146 + 0.073 \cdot \text{SL}$	$0.132 + 0.075 \cdot \text{SL}$
	$t_{PLH}$	0.302	$0.157 + 0.073 \cdot \text{SL}$	$0.158 + 0.072 \cdot \text{SL}$	$0.159 + 0.072 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.118 + 0.036 \cdot \text{SL}$	$0.119 + 0.036 \cdot \text{SL}$	$0.119 + 0.036 \cdot \text{SL}$
C to Y	$t_R$	0.612	$0.282 + 0.165 \cdot \text{SL}$	$0.275 + 0.167 \cdot \text{SL}$	$0.273 + 0.167 \cdot \text{SL}$
	$t_F$	0.333	$0.194 + 0.069 \cdot \text{SL}$	$0.181 + 0.072 \cdot \text{SL}$	$0.166 + 0.074 \cdot \text{SL}$
	$t_{PLH}$	0.313	$0.168 + 0.073 \cdot \text{SL}$	$0.170 + 0.072 \cdot \text{SL}$	$0.172 + 0.072 \cdot \text{SL}$
	$t_{PHL}$	0.203	$0.128 + 0.038 \cdot \text{SL}$	$0.131 + 0.037 \cdot \text{SL}$	$0.134 + 0.036 \cdot \text{SL}$
D to Y	$t_R$	0.320	$0.198 + 0.061 \cdot \text{SL}$	$0.184 + 0.065 \cdot \text{SL}$	$0.170 + 0.066 \cdot \text{SL}$
	$t_F$	0.320	$0.175 + 0.073 \cdot \text{SL}$	$0.171 + 0.074 \cdot \text{SL}$	$0.166 + 0.074 \cdot \text{SL}$
	$t_{PLH}$	0.175	$0.118 + 0.029 \cdot \text{SL}$	$0.117 + 0.029 \cdot \text{SL}$	$0.118 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.192	$0.117 + 0.038 \cdot \text{SL}$	$0.121 + 0.037 \cdot \text{SL}$	$0.124 + 0.036 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### OA31

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.409	$0.239 + 0.085 \cdot \text{SL}$	$0.228 + 0.088 \cdot \text{SL}$	$0.216 + 0.089 \cdot \text{SL}$
	$t_F$	0.280	$0.151 + 0.065 \cdot \text{SL}$	$0.143 + 0.067 \cdot \text{SL}$	$0.132 + 0.068 \cdot \text{SL}$
	$t_{PLH}$	0.183	$0.107 + 0.038 \cdot \text{SL}$	$0.106 + 0.038 \cdot \text{SL}$	$0.106 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.180	$0.116 + 0.032 \cdot \text{SL}$	$0.115 + 0.032 \cdot \text{SL}$	$0.115 + 0.032 \cdot \text{SL}$
B to Y	$t_R$	0.409	$0.237 + 0.086 \cdot \text{SL}$	$0.231 + 0.088 \cdot \text{SL}$	$0.222 + 0.089 \cdot \text{SL}$
	$t_F$	0.327	$0.198 + 0.065 \cdot \text{SL}$	$0.190 + 0.067 \cdot \text{SL}$	$0.180 + 0.068 \cdot \text{SL}$
	$t_{PLH}$	0.205	$0.128 + 0.039 \cdot \text{SL}$	$0.129 + 0.038 \cdot \text{SL}$	$0.129 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.146 + 0.033 \cdot \text{SL}$	$0.146 + 0.032 \cdot \text{SL}$	$0.147 + 0.032 \cdot \text{SL}$
C to Y	$t_R$	0.405	$0.231 + 0.087 \cdot \text{SL}$	$0.226 + 0.088 \cdot \text{SL}$	$0.220 + 0.089 \cdot \text{SL}$
	$t_F$	0.382	$0.255 + 0.064 \cdot \text{SL}$	$0.246 + 0.066 \cdot \text{SL}$	$0.234 + 0.067 \cdot \text{SL}$
	$t_{PLH}$	0.216	$0.139 + 0.039 \cdot \text{SL}$	$0.140 + 0.038 \cdot \text{SL}$	$0.141 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.233	$0.166 + 0.034 \cdot \text{SL}$	$0.169 + 0.033 \cdot \text{SL}$	$0.173 + 0.032 \cdot \text{SL}$
D to Y	$t_R$	0.213	$0.162 + 0.026 \cdot \text{SL}$	$0.154 + 0.028 \cdot \text{SL}$	$0.142 + 0.029 \cdot \text{SL}$
	$t_F$	0.373	$0.241 + 0.066 \cdot \text{SL}$	$0.238 + 0.067 \cdot \text{SL}$	$0.232 + 0.068 \cdot \text{SL}$
	$t_{PLH}$	0.111	$0.082 + 0.015 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.242	$0.174 + 0.034 \cdot \text{SL}$	$0.178 + 0.033 \cdot \text{SL}$	$0.182 + 0.033 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OA31DH/OA31/OA31D2/OA31D4

## 3-OR into 2-NAND with 0.5X/1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA31D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.302	$0.217 + 0.042 \cdot \text{SL}$	$0.210 + 0.044 \cdot \text{SL}$	$0.193 + 0.045 \cdot \text{SL}$
	$t_F$	0.191	$0.132 + 0.029 \cdot \text{SL}$	$0.125 + 0.031 \cdot \text{SL}$	$0.111 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.138	$0.100 + 0.019 \cdot \text{SL}$	$0.099 + 0.019 \cdot \text{SL}$	$0.098 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.132	$0.101 + 0.016 \cdot \text{SL}$	$0.102 + 0.015 \cdot \text{SL}$	$0.102 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.301	$0.214 + 0.043 \cdot \text{SL}$	$0.209 + 0.045 \cdot \text{SL}$	$0.199 + 0.045 \cdot \text{SL}$
	$t_F$	0.237	$0.178 + 0.029 \cdot \text{SL}$	$0.171 + 0.031 \cdot \text{SL}$	$0.156 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.157	$0.117 + 0.020 \cdot \text{SL}$	$0.119 + 0.020 \cdot \text{SL}$	$0.119 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.160	$0.129 + 0.016 \cdot \text{SL}$	$0.130 + 0.016 \cdot \text{SL}$	$0.130 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.296	$0.209 + 0.044 \cdot \text{SL}$	$0.204 + 0.045 \cdot \text{SL}$	$0.196 + 0.045 \cdot \text{SL}$
	$t_F$	0.287	$0.228 + 0.029 \cdot \text{SL}$	$0.222 + 0.031 \cdot \text{SL}$	$0.205 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.165	$0.125 + 0.020 \cdot \text{SL}$	$0.126 + 0.020 \cdot \text{SL}$	$0.128 + 0.020 \cdot \text{SL}$
	$t_{PHL}$	0.177	$0.144 + 0.017 \cdot \text{SL}$	$0.147 + 0.016 \cdot \text{SL}$	$0.151 + 0.016 \cdot \text{SL}$
D to Y	$t_R$	0.181	$0.156 + 0.012 \cdot \text{SL}$	$0.151 + 0.014 \cdot \text{SL}$	$0.137 + 0.015 \cdot \text{SL}$
	$t_F$	0.273	$0.210 + 0.032 \cdot \text{SL}$	$0.209 + 0.032 \cdot \text{SL}$	$0.202 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.092	$0.076 + 0.008 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.184	$0.151 + 0.017 \cdot \text{SL}$	$0.153 + 0.016 \cdot \text{SL}$	$0.158 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### OA31D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.059 + 0.007 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.333	$0.322 + 0.005 \cdot \text{SL}$	$0.328 + 0.004 \cdot \text{SL}$	$0.340 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.311	$0.299 + 0.006 \cdot \text{SL}$	$0.305 + 0.004 \cdot \text{SL}$	$0.320 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.076	$0.063 + 0.006 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.354	$0.344 + 0.005 \cdot \text{SL}$	$0.349 + 0.004 \cdot \text{SL}$	$0.361 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.349	$0.338 + 0.006 \cdot \text{SL}$	$0.344 + 0.004 \cdot \text{SL}$	$0.359 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.086	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.065 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.363	$0.352 + 0.005 \cdot \text{SL}$	$0.358 + 0.004 \cdot \text{SL}$	$0.370 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.377	$0.365 + 0.006 \cdot \text{SL}$	$0.371 + 0.004 \cdot \text{SL}$	$0.386 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.081	$0.067 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.057 + 0.008 \cdot \text{SL}$
	$t_F$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.248 + 0.005 \cdot \text{SL}$	$0.253 + 0.004 \cdot \text{SL}$	$0.263 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.386	$0.375 + 0.006 \cdot \text{SL}$	$0.381 + 0.004 \cdot \text{SL}$	$0.396 + 0.004 \cdot \text{SL}$

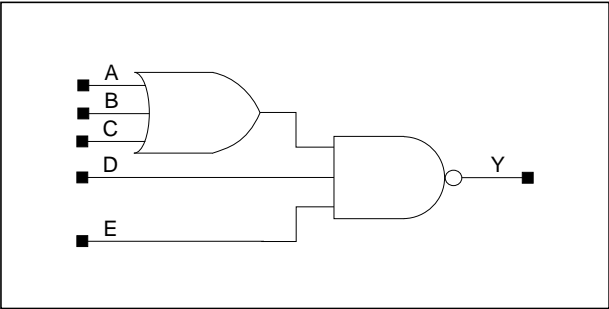
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OA311/OA311D2/OA311D4

3-OR into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)														
OA311					OA311D2					OA311D4				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	1.0	1.0	0.9	0.9	0.9	1.0	1.0	0.9	0.9	1.0	1.0	1.0
Gate Count														
OA311					OA311D2					OA311D4				
2.00					3.00					3.67				



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA311**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.427	$0.257 + 0.085 \cdot \text{SL}$	$0.246 + 0.088 \cdot \text{SL}$	$0.236 + 0.089 \cdot \text{SL}$
	$t_F$	0.347	$0.197 + 0.075 \cdot \text{SL}$	$0.189 + 0.077 \cdot \text{SL}$	$0.181 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.193	$0.117 + 0.038 \cdot \text{SL}$	$0.116 + 0.038 \cdot \text{SL}$	$0.116 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.196	$0.125 + 0.036 \cdot \text{SL}$	$0.124 + 0.036 \cdot \text{SL}$	$0.124 + 0.036 \cdot \text{SL}$
B to Y	$t_R$	0.429	$0.255 + 0.087 \cdot \text{SL}$	$0.250 + 0.088 \cdot \text{SL}$	$0.242 + 0.089 \cdot \text{SL}$
	$t_F$	0.404	$0.254 + 0.075 \cdot \text{SL}$	$0.245 + 0.077 \cdot \text{SL}$	$0.237 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.217	$0.139 + 0.039 \cdot \text{SL}$	$0.140 + 0.038 \cdot \text{SL}$	$0.141 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.232	$0.160 + 0.036 \cdot \text{SL}$	$0.160 + 0.036 \cdot \text{SL}$	$0.161 + 0.036 \cdot \text{SL}$
C to Y	$t_R$	0.425	$0.251 + 0.087 \cdot \text{SL}$	$0.246 + 0.088 \cdot \text{SL}$	$0.241 + 0.089 \cdot \text{SL}$
	$t_F$	0.463	$0.315 + 0.074 \cdot \text{SL}$	$0.306 + 0.076 \cdot \text{SL}$	$0.297 + 0.078 \cdot \text{SL}$
	$t_{PLH}$	0.226	$0.148 + 0.039 \cdot \text{SL}$	$0.149 + 0.039 \cdot \text{SL}$	$0.151 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.257	$0.183 + 0.037 \cdot \text{SL}$	$0.186 + 0.036 \cdot \text{SL}$	$0.189 + 0.036 \cdot \text{SL}$
D to Y	$t_R$	0.223	$0.171 + 0.026 \cdot \text{SL}$	$0.163 + 0.028 \cdot \text{SL}$	$0.151 + 0.029 \cdot \text{SL}$
	$t_F$	0.458	$0.307 + 0.076 \cdot \text{SL}$	$0.302 + 0.077 \cdot \text{SL}$	$0.297 + 0.077 \cdot \text{SL}$
	$t_{PLH}$	0.118	$0.090 + 0.014 \cdot \text{SL}$	$0.094 + 0.013 \cdot \text{SL}$	$0.094 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.280	$0.205 + 0.038 \cdot \text{SL}$	$0.209 + 0.037 \cdot \text{SL}$	$0.213 + 0.036 \cdot \text{SL}$
E to Y	$t_R$	0.236	$0.183 + 0.027 \cdot \text{SL}$	$0.175 + 0.028 \cdot \text{SL}$	$0.164 + 0.030 \cdot \text{SL}$
	$t_F$	0.457	$0.305 + 0.076 \cdot \text{SL}$	$0.302 + 0.077 \cdot \text{SL}$	$0.297 + 0.077 \cdot \text{SL}$
	$t_{PLH}$	0.125	$0.096 + 0.014 \cdot \text{SL}$	$0.099 + 0.014 \cdot \text{SL}$	$0.099 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.276	$0.201 + 0.038 \cdot \text{SL}$	$0.205 + 0.037 \cdot \text{SL}$	$0.209 + 0.036 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## OA311/OA311D2/OA311D4

### 3-OR into 3-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA311D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.091	$0.064 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.057 + 0.014 \cdot \text{SL}$	$0.062 + 0.012 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.312	$0.294 + 0.009 \cdot \text{SL}$	$0.301 + 0.007 \cdot \text{SL}$	$0.307 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.322	$0.302 + 0.010 \cdot \text{SL}$	$0.310 + 0.008 \cdot \text{SL}$	$0.321 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.091	$0.064 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.014 \cdot \text{SL}$	$0.064 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.317 + 0.009 \cdot \text{SL}$	$0.323 + 0.007 \cdot \text{SL}$	$0.330 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.367	$0.347 + 0.010 \cdot \text{SL}$	$0.355 + 0.008 \cdot \text{SL}$	$0.366 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.092	$0.064 + 0.014 \cdot \text{SL}$	$0.063 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.344	$0.326 + 0.009 \cdot \text{SL}$	$0.332 + 0.007 \cdot \text{SL}$	$0.339 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.399	$0.380 + 0.010 \cdot \text{SL}$	$0.388 + 0.008 \cdot \text{SL}$	$0.399 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.086	$0.057 + 0.015 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.064 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.243	$0.225 + 0.009 \cdot \text{SL}$	$0.231 + 0.007 \cdot \text{SL}$	$0.237 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.422	$0.402 + 0.010 \cdot \text{SL}$	$0.410 + 0.008 \cdot \text{SL}$	$0.422 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.251	$0.233 + 0.009 \cdot \text{SL}$	$0.239 + 0.007 \cdot \text{SL}$	$0.245 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.418	$0.398 + 0.010 \cdot \text{SL}$	$0.406 + 0.008 \cdot \text{SL}$	$0.418 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA311/OA311D2/OA311D4

## 3-OR into 3-NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA311D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.085	$0.072 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.064 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.343	$0.332 + 0.005 \cdot \text{SL}$	$0.337 + 0.004 \cdot \text{SL}$	$0.349 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.337	$0.325 + 0.006 \cdot \text{SL}$	$0.331 + 0.004 \cdot \text{SL}$	$0.346 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.086	$0.073 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.065 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.367	$0.357 + 0.005 \cdot \text{SL}$	$0.362 + 0.004 \cdot \text{SL}$	$0.374 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.383	$0.371 + 0.006 \cdot \text{SL}$	$0.377 + 0.004 \cdot \text{SL}$	$0.392 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_F$	0.081	$0.068 + 0.007 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.375	$0.364 + 0.005 \cdot \text{SL}$	$0.370 + 0.004 \cdot \text{SL}$	$0.381 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.414	$0.403 + 0.006 \cdot \text{SL}$	$0.408 + 0.004 \cdot \text{SL}$	$0.424 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.081	$0.068 + 0.007 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.248 + 0.005 \cdot \text{SL}$	$0.253 + 0.004 \cdot \text{SL}$	$0.263 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.437	$0.425 + 0.006 \cdot \text{SL}$	$0.431 + 0.004 \cdot \text{SL}$	$0.446 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.080	$0.065 + 0.007 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.056 + 0.008 \cdot \text{SL}$
	$t_F$	0.081	$0.068 + 0.007 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.267	$0.256 + 0.005 \cdot \text{SL}$	$0.261 + 0.004 \cdot \text{SL}$	$0.272 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.433	$0.421 + 0.006 \cdot \text{SL}$	$0.427 + 0.004 \cdot \text{SL}$	$0.442 + 0.004 \cdot \text{SL}$

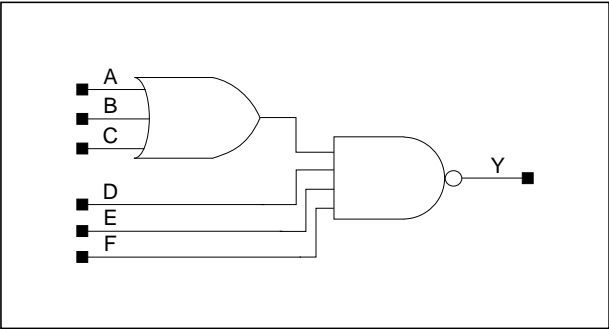
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OA3111/OA3111D2

3-OR into 4-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
Other States						0

Cell Data

Input Load (SL)												Gate Count	
OA3111						OA3111D2						OA3111	OA3111D2
A	B	C	D	E	F	A	B	C	D	E	F		
0.9	1.0	1.0	1.0	1.0	1.0	0.9	1.0	1.0	1.0	1.0	1.0	2.33	3.33



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA3111**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.487	$0.313 + 0.087 \cdot \text{SL}$	$0.307 + 0.088 \cdot \text{SL}$	$0.299 + 0.089 \cdot \text{SL}$
	$t_F$	0.451	$0.284 + 0.084 \cdot \text{SL}$	$0.277 + 0.085 \cdot \text{SL}$	$0.273 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.222	$0.145 + 0.038 \cdot \text{SL}$	$0.145 + 0.038 \cdot \text{SL}$	$0.145 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.229	$0.152 + 0.039 \cdot \text{SL}$	$0.152 + 0.039 \cdot \text{SL}$	$0.152 + 0.039 \cdot \text{SL}$
B to Y	$t_R$	0.490	$0.316 + 0.087 \cdot \text{SL}$	$0.311 + 0.088 \cdot \text{SL}$	$0.304 + 0.089 \cdot \text{SL}$
	$t_F$	0.514	$0.345 + 0.085 \cdot \text{SL}$	$0.337 + 0.087 \cdot \text{SL}$	$0.334 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.243	$0.165 + 0.039 \cdot \text{SL}$	$0.166 + 0.038 \cdot \text{SL}$	$0.167 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.271	$0.192 + 0.040 \cdot \text{SL}$	$0.192 + 0.039 \cdot \text{SL}$	$0.192 + 0.039 \cdot \text{SL}$
C to Y	$t_R$	0.487	$0.312 + 0.088 \cdot \text{SL}$	$0.308 + 0.089 \cdot \text{SL}$	$0.303 + 0.089 \cdot \text{SL}$
	$t_F$	0.574	$0.408 + 0.083 \cdot \text{SL}$	$0.400 + 0.085 \cdot \text{SL}$	$0.394 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.251	$0.174 + 0.039 \cdot \text{SL}$	$0.175 + 0.039 \cdot \text{SL}$	$0.176 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.296	$0.216 + 0.040 \cdot \text{SL}$	$0.218 + 0.039 \cdot \text{SL}$	$0.220 + 0.039 \cdot \text{SL}$
D to Y	$t_R$	0.243	$0.189 + 0.027 \cdot \text{SL}$	$0.181 + 0.029 \cdot \text{SL}$	$0.173 + 0.030 \cdot \text{SL}$
	$t_F$	0.573	$0.405 + 0.084 \cdot \text{SL}$	$0.401 + 0.085 \cdot \text{SL}$	$0.397 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.133	$0.105 + 0.014 \cdot \text{SL}$	$0.107 + 0.014 \cdot \text{SL}$	$0.107 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.330	$0.249 + 0.040 \cdot \text{SL}$	$0.252 + 0.040 \cdot \text{SL}$	$0.256 + 0.039 \cdot \text{SL}$
E to Y	$t_R$	0.255	$0.201 + 0.027 \cdot \text{SL}$	$0.195 + 0.029 \cdot \text{SL}$	$0.184 + 0.030 \cdot \text{SL}$
	$t_F$	0.573	$0.405 + 0.084 \cdot \text{SL}$	$0.400 + 0.085 \cdot \text{SL}$	$0.397 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.139	$0.111 + 0.014 \cdot \text{SL}$	$0.112 + 0.014 \cdot \text{SL}$	$0.113 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.335	$0.254 + 0.040 \cdot \text{SL}$	$0.257 + 0.040 \cdot \text{SL}$	$0.261 + 0.039 \cdot \text{SL}$
F to Y	$t_R$	0.268	$0.214 + 0.027 \cdot \text{SL}$	$0.207 + 0.029 \cdot \text{SL}$	$0.197 + 0.030 \cdot \text{SL}$
	$t_F$	0.572	$0.403 + 0.084 \cdot \text{SL}$	$0.400 + 0.085 \cdot \text{SL}$	$0.397 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.143	$0.115 + 0.014 \cdot \text{SL}$	$0.116 + 0.014 \cdot \text{SL}$	$0.117 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.338	$0.257 + 0.041 \cdot \text{SL}$	$0.260 + 0.040 \cdot \text{SL}$	$0.264 + 0.039 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## OA3111/OA3111D2

### 3-OR into 4-NAND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA3111D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.096	$0.068 + 0.014 \cdot \text{SL}$	$0.067 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.065 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.355	$0.337 + 0.009 \cdot \text{SL}$	$0.344 + 0.007 \cdot \text{SL}$	$0.351 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.375	$0.355 + 0.010 \cdot \text{SL}$	$0.363 + 0.008 \cdot \text{SL}$	$0.375 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.096	$0.068 + 0.014 \cdot \text{SL}$	$0.068 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.068 + 0.012 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.375	$0.357 + 0.009 \cdot \text{SL}$	$0.364 + 0.007 \cdot \text{SL}$	$0.371 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.425	$0.405 + 0.010 \cdot \text{SL}$	$0.413 + 0.008 \cdot \text{SL}$	$0.425 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.096	$0.069 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.068 + 0.013 \cdot \text{SL}$	$0.073 + 0.012 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.383	$0.366 + 0.009 \cdot \text{SL}$	$0.372 + 0.007 \cdot \text{SL}$	$0.379 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.458	$0.438 + 0.010 \cdot \text{SL}$	$0.446 + 0.008 \cdot \text{SL}$	$0.458 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.069 + 0.013 \cdot \text{SL}$	$0.073 + 0.012 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.266	$0.248 + 0.009 \cdot \text{SL}$	$0.254 + 0.007 \cdot \text{SL}$	$0.260 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.492	$0.472 + 0.010 \cdot \text{SL}$	$0.480 + 0.008 \cdot \text{SL}$	$0.492 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.069 + 0.013 \cdot \text{SL}$	$0.071 + 0.012 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.273	$0.256 + 0.009 \cdot \text{SL}$	$0.262 + 0.007 \cdot \text{SL}$	$0.268 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.497	$0.477 + 0.010 \cdot \text{SL}$	$0.485 + 0.008 \cdot \text{SL}$	$0.497 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.068 + 0.013 \cdot \text{SL}$	$0.073 + 0.012 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.279	$0.262 + 0.009 \cdot \text{SL}$	$0.268 + 0.007 \cdot \text{SL}$	$0.274 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.500	$0.480 + 0.010 \cdot \text{SL}$	$0.488 + 0.008 \cdot \text{SL}$	$0.500 + 0.007 \cdot \text{SL}$

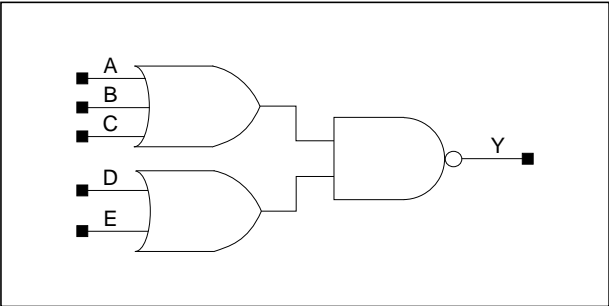
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



OA32/OA32D2/OA32D4

3-OR and 2-OR into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	x	x	1
x	x	x	0	0	1
Other States					0

Cell Data

Input Load (SL)														
OA32					OA32D2					OA32D4				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.8	0.9	0.9	0.8	0.9	0.8	0.9	0.9	0.9	0.9	0.8	0.9	0.9	0.8	0.9
Gate Count														
OA32					OA32D2					OA32D4				
2.33					3.33					4.00				



## OA32/OA32D2/OA32D4

### 3-OR and 2-OR into 2-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA32

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.499	$0.329 + 0.085 \cdot \text{SL}$	$0.317 + 0.088 \cdot \text{SL}$	$0.305 + 0.090 \cdot \text{SL}$
	$t_F$	0.361	$0.211 + 0.075 \cdot \text{SL}$	$0.205 + 0.076 \cdot \text{SL}$	$0.199 + 0.077 \cdot \text{SL}$
	$t_{PLH}$	0.198	$0.119 + 0.039 \cdot \text{SL}$	$0.121 + 0.039 \cdot \text{SL}$	$0.123 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.236	$0.162 + 0.037 \cdot \text{SL}$	$0.163 + 0.037 \cdot \text{SL}$	$0.164 + 0.037 \cdot \text{SL}$
B to Y	$t_R$	0.500	$0.327 + 0.086 \cdot \text{SL}$	$0.320 + 0.088 \cdot \text{SL}$	$0.310 + 0.089 \cdot \text{SL}$
	$t_F$	0.413	$0.263 + 0.075 \cdot \text{SL}$	$0.257 + 0.077 \cdot \text{SL}$	$0.252 + 0.077 \cdot \text{SL}$
	$t_{PLH}$	0.220	$0.141 + 0.040 \cdot \text{SL}$	$0.144 + 0.039 \cdot \text{SL}$	$0.147 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.271	$0.197 + 0.037 \cdot \text{SL}$	$0.198 + 0.037 \cdot \text{SL}$	$0.199 + 0.037 \cdot \text{SL}$
C to Y	$t_R$	0.496	$0.322 + 0.087 \cdot \text{SL}$	$0.316 + 0.088 \cdot \text{SL}$	$0.309 + 0.089 \cdot \text{SL}$
	$t_F$	0.469	$0.320 + 0.074 \cdot \text{SL}$	$0.313 + 0.076 \cdot \text{SL}$	$0.309 + 0.077 \cdot \text{SL}$
	$t_{PLH}$	0.230	$0.150 + 0.040 \cdot \text{SL}$	$0.154 + 0.039 \cdot \text{SL}$	$0.158 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.298	$0.222 + 0.038 \cdot \text{SL}$	$0.225 + 0.037 \cdot \text{SL}$	$0.228 + 0.037 \cdot \text{SL}$
D to Y	$t_R$	0.374	$0.264 + 0.055 \cdot \text{SL}$	$0.254 + 0.058 \cdot \text{SL}$	$0.240 + 0.059 \cdot \text{SL}$
	$t_F$	0.416	$0.265 + 0.076 \cdot \text{SL}$	$0.261 + 0.077 \cdot \text{SL}$	$0.258 + 0.077 \cdot \text{SL}$
	$t_{PLH}$	0.176	$0.124 + 0.026 \cdot \text{SL}$	$0.125 + 0.026 \cdot \text{SL}$	$0.127 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.280	$0.202 + 0.039 \cdot \text{SL}$	$0.207 + 0.038 \cdot \text{SL}$	$0.212 + 0.037 \cdot \text{SL}$
E to Y	$t_R$	0.367	$0.253 + 0.057 \cdot \text{SL}$	$0.246 + 0.058 \cdot \text{SL}$	$0.239 + 0.059 \cdot \text{SL}$
	$t_F$	0.465	$0.314 + 0.076 \cdot \text{SL}$	$0.311 + 0.076 \cdot \text{SL}$	$0.308 + 0.077 \cdot \text{SL}$
	$t_{PLH}$	0.177	$0.125 + 0.026 \cdot \text{SL}$	$0.126 + 0.026 \cdot \text{SL}$	$0.128 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.315	$0.239 + 0.038 \cdot \text{SL}$	$0.242 + 0.037 \cdot \text{SL}$	$0.246 + 0.037 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA32D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.097	$0.069 + 0.014 \cdot \text{SL}$	$0.069 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.058 + 0.013 \cdot \text{SL}$	$0.063 + 0.012 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.329	$0.311 + 0.009 \cdot \text{SL}$	$0.318 + 0.007 \cdot \text{SL}$	$0.325 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.363	$0.343 + 0.010 \cdot \text{SL}$	$0.351 + 0.008 \cdot \text{SL}$	$0.362 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.097	$0.069 + 0.014 \cdot \text{SL}$	$0.069 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.060 + 0.013 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.352	$0.334 + 0.009 \cdot \text{SL}$	$0.340 + 0.007 \cdot \text{SL}$	$0.348 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.408	$0.388 + 0.010 \cdot \text{SL}$	$0.396 + 0.008 \cdot \text{SL}$	$0.407 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.098	$0.071 + 0.013 \cdot \text{SL}$	$0.067 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.013 \cdot \text{SL}$	$0.066 + 0.012 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.360	$0.342 + 0.009 \cdot \text{SL}$	$0.348 + 0.007 \cdot \text{SL}$	$0.356 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.441	$0.421 + 0.010 \cdot \text{SL}$	$0.429 + 0.008 \cdot \text{SL}$	$0.440 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.097	$0.070 + 0.013 \cdot \text{SL}$	$0.067 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.013 \cdot \text{SL}$	$0.065 + 0.012 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.315	$0.297 + 0.009 \cdot \text{SL}$	$0.303 + 0.007 \cdot \text{SL}$	$0.310 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.414	$0.394 + 0.010 \cdot \text{SL}$	$0.402 + 0.008 \cdot \text{SL}$	$0.413 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.096	$0.068 + 0.014 \cdot \text{SL}$	$0.068 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.066 + 0.012 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.315	$0.298 + 0.009 \cdot \text{SL}$	$0.304 + 0.007 \cdot \text{SL}$	$0.311 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.457	$0.438 + 0.010 \cdot \text{SL}$	$0.446 + 0.008 \cdot \text{SL}$	$0.457 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## OA32/OA32D2/OA32D4

### 3-OR and 2-OR into 2-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA32D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.091	$0.078 + 0.006 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$
	$t_F$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$	$0.062 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.355	$0.345 + 0.005 \cdot \text{SL}$	$0.350 + 0.004 \cdot \text{SL}$	$0.362 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.374	$0.363 + 0.006 \cdot \text{SL}$	$0.369 + 0.004 \cdot \text{SL}$	$0.383 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.090	$0.077 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.065 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.367 + 0.005 \cdot \text{SL}$	$0.373 + 0.004 \cdot \text{SL}$	$0.385 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.420	$0.408 + 0.006 \cdot \text{SL}$	$0.414 + 0.004 \cdot \text{SL}$	$0.429 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.080	$0.067 + 0.007 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$	$0.064 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.386	$0.375 + 0.005 \cdot \text{SL}$	$0.381 + 0.004 \cdot \text{SL}$	$0.393 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.452	$0.441 + 0.006 \cdot \text{SL}$	$0.447 + 0.004 \cdot \text{SL}$	$0.462 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.089	$0.077 + 0.006 \cdot \text{SL}$	$0.074 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.325 + 0.005 \cdot \text{SL}$	$0.330 + 0.004 \cdot \text{SL}$	$0.342 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.426	$0.414 + 0.006 \cdot \text{SL}$	$0.420 + 0.004 \cdot \text{SL}$	$0.435 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.089	$0.076 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_F$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.336	$0.325 + 0.005 \cdot \text{SL}$	$0.331 + 0.004 \cdot \text{SL}$	$0.343 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.469	$0.457 + 0.006 \cdot \text{SL}$	$0.463 + 0.004 \cdot \text{SL}$	$0.478 + 0.004 \cdot \text{SL}$

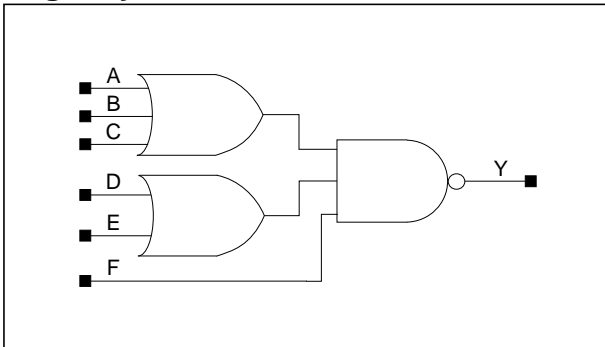
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## OA321/OA321D2/OA321D4

### 3-OR and 2-OR into 3-NAND with 1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	0	x	1
x	x	x	x	x	0	1
Other States						0

#### Cell Data

Input Load (SL)																	
OA321						OA321D2						OA321D4					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.9	0.9	0.90	0.9	0.9	0.9	0.9	0.9	0.90	0.9	0.9	0.9	0.9	0.9	0.90	0.9	0.9	0.9
Gate Count																	
OA321						OA321D2						OA321D4					
3.00						3.67						4.33					



## OA321/OA321D2/OA321D4

### 3-OR and 2-OR into 3-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA321

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.530	$0.359 + 0.086 \cdot \text{SL}$	$0.348 + 0.089 \cdot \text{SL}$	$0.337 + 0.090 \cdot \text{SL}$
	$t_F$	0.452	$0.281 + 0.085 \cdot \text{SL}$	$0.276 + 0.087 \cdot \text{SL}$	$0.273 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.135 + 0.039 \cdot \text{SL}$	$0.137 + 0.039 \cdot \text{SL}$	$0.139 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.258	$0.177 + 0.040 \cdot \text{SL}$	$0.178 + 0.040 \cdot \text{SL}$	$0.179 + 0.040 \cdot \text{SL}$
B to Y	$t_R$	0.531	$0.357 + 0.087 \cdot \text{SL}$	$0.352 + 0.088 \cdot \text{SL}$	$0.343 + 0.090 \cdot \text{SL}$
	$t_F$	0.511	$0.340 + 0.085 \cdot \text{SL}$	$0.334 + 0.087 \cdot \text{SL}$	$0.333 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.237	$0.157 + 0.040 \cdot \text{SL}$	$0.160 + 0.039 \cdot \text{SL}$	$0.164 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.298	$0.217 + 0.040 \cdot \text{SL}$	$0.218 + 0.040 \cdot \text{SL}$	$0.219 + 0.040 \cdot \text{SL}$
C to Y	$t_R$	0.528	$0.354 + 0.087 \cdot \text{SL}$	$0.348 + 0.089 \cdot \text{SL}$	$0.342 + 0.090 \cdot \text{SL}$
	$t_F$	0.575	$0.405 + 0.085 \cdot \text{SL}$	$0.399 + 0.086 \cdot \text{SL}$	$0.396 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.246	$0.166 + 0.040 \cdot \text{SL}$	$0.169 + 0.039 \cdot \text{SL}$	$0.173 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.329	$0.246 + 0.041 \cdot \text{SL}$	$0.249 + 0.041 \cdot \text{SL}$	$0.252 + 0.040 \cdot \text{SL}$
D to Y	$t_R$	0.401	$0.290 + 0.056 \cdot \text{SL}$	$0.282 + 0.058 \cdot \text{SL}$	$0.269 + 0.059 \cdot \text{SL}$
	$t_F$	0.515	$0.345 + 0.085 \cdot \text{SL}$	$0.340 + 0.086 \cdot \text{SL}$	$0.338 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.141 + 0.026 \cdot \text{SL}$	$0.142 + 0.026 \cdot \text{SL}$	$0.144 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.323	$0.239 + 0.042 \cdot \text{SL}$	$0.244 + 0.041 \cdot \text{SL}$	$0.248 + 0.040 \cdot \text{SL}$
E to Y	$t_R$	0.395	$0.281 + 0.057 \cdot \text{SL}$	$0.275 + 0.059 \cdot \text{SL}$	$0.269 + 0.059 \cdot \text{SL}$
	$t_F$	0.574	$0.403 + 0.086 \cdot \text{SL}$	$0.400 + 0.086 \cdot \text{SL}$	$0.398 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.142 + 0.026 \cdot \text{SL}$	$0.143 + 0.026 \cdot \text{SL}$	$0.145 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.363	$0.280 + 0.042 \cdot \text{SL}$	$0.283 + 0.041 \cdot \text{SL}$	$0.287 + 0.040 \cdot \text{SL}$
F to Y	$t_R$	0.285	$0.234 + 0.025 \cdot \text{SL}$	$0.226 + 0.027 \cdot \text{SL}$	$0.212 + 0.029 \cdot \text{SL}$
	$t_F$	0.574	$0.402 + 0.086 \cdot \text{SL}$	$0.400 + 0.086 \cdot \text{SL}$	$0.398 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.134	$0.106 + 0.014 \cdot \text{SL}$	$0.107 + 0.014 \cdot \text{SL}$	$0.109 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.372	$0.289 + 0.042 \cdot \text{SL}$	$0.292 + 0.041 \cdot \text{SL}$	$0.296 + 0.040 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA321D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.095	$0.068 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.338	$0.320 + 0.009 \cdot \text{SL}$	$0.327 + 0.007 \cdot \text{SL}$	$0.334 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.387	$0.368 + 0.010 \cdot \text{SL}$	$0.375 + 0.008 \cdot \text{SL}$	$0.385 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.095	$0.069 + 0.013 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.014 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.360	$0.342 + 0.009 \cdot \text{SL}$	$0.349 + 0.007 \cdot \text{SL}$	$0.356 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.437	$0.417 + 0.010 \cdot \text{SL}$	$0.425 + 0.008 \cdot \text{SL}$	$0.435 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.095	$0.068 + 0.014 \cdot \text{SL}$	$0.067 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.369	$0.351 + 0.009 \cdot \text{SL}$	$0.358 + 0.007 \cdot \text{SL}$	$0.364 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.475	$0.455 + 0.010 \cdot \text{SL}$	$0.463 + 0.008 \cdot \text{SL}$	$0.474 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.094	$0.066 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.062 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.324	$0.306 + 0.009 \cdot \text{SL}$	$0.313 + 0.007 \cdot \text{SL}$	$0.319 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.458	$0.438 + 0.010 \cdot \text{SL}$	$0.446 + 0.008 \cdot \text{SL}$	$0.456 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.094	$0.067 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.064 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.325	$0.308 + 0.009 \cdot \text{SL}$	$0.314 + 0.007 \cdot \text{SL}$	$0.321 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.509	$0.489 + 0.010 \cdot \text{SL}$	$0.497 + 0.008 \cdot \text{SL}$	$0.507 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.084	$0.057 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.065 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.260	$0.243 + 0.008 \cdot \text{SL}$	$0.249 + 0.007 \cdot \text{SL}$	$0.254 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.519	$0.499 + 0.010 \cdot \text{SL}$	$0.507 + 0.008 \cdot \text{SL}$	$0.517 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA321/OA321D2/OA321D4

## 3-OR and 2-OR into 3-NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA321D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.093	$0.080 + 0.006 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$	$0.067 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.367 + 0.005 \cdot \text{SL}$	$0.373 + 0.004 \cdot \text{SL}$	$0.385 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.410	$0.399 + 0.006 \cdot \text{SL}$	$0.405 + 0.004 \cdot \text{SL}$	$0.420 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.094	$0.081 + 0.006 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.073 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.400	$0.389 + 0.005 \cdot \text{SL}$	$0.395 + 0.004 \cdot \text{SL}$	$0.407 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.459	$0.448 + 0.006 \cdot \text{SL}$	$0.453 + 0.004 \cdot \text{SL}$	$0.469 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.092	$0.079 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.076 + 0.006 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.408	$0.397 + 0.005 \cdot \text{SL}$	$0.403 + 0.004 \cdot \text{SL}$	$0.416 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.498	$0.487 + 0.006 \cdot \text{SL}$	$0.493 + 0.004 \cdot \text{SL}$	$0.508 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.091	$0.078 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.359	$0.348 + 0.005 \cdot \text{SL}$	$0.354 + 0.004 \cdot \text{SL}$	$0.366 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.481	$0.469 + 0.006 \cdot \text{SL}$	$0.476 + 0.004 \cdot \text{SL}$	$0.491 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.091	$0.078 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.087	$0.074 + 0.006 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.360	$0.350 + 0.005 \cdot \text{SL}$	$0.355 + 0.004 \cdot \text{SL}$	$0.368 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.532	$0.521 + 0.006 \cdot \text{SL}$	$0.527 + 0.004 \cdot \text{SL}$	$0.542 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.083	$0.070 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.087	$0.075 + 0.006 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.285	$0.275 + 0.005 \cdot \text{SL}$	$0.280 + 0.004 \cdot \text{SL}$	$0.291 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.542	$0.530 + 0.006 \cdot \text{SL}$	$0.537 + 0.004 \cdot \text{SL}$	$0.552 + 0.004 \cdot \text{SL}$

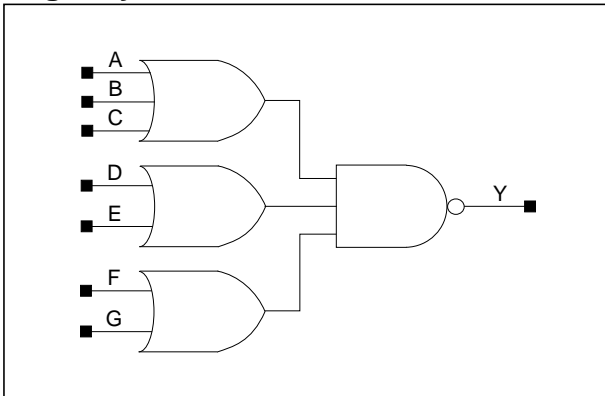
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## OA322/OA322D2/OA322D4

### 3-OR and Two 2-ORs into 3-NAND with 1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	C	D	E	F	G	Y
0	0	0	x	x	x	x	1
x	x	x	0	0	x	x	1
x	x	x	x	x	0	0	1
Other States							0

#### Cell Data

Input Load (SL)							Gate Count
OA322							OA322
A	B	C	D	E	F	G	
0.8	0.9	0.9	0.9	1.1	0.9	0.9	3.00
OA322D2							OA322D2
A	B	C	D	E	F	G	
0.9	0.9	0.9	0.9	1.1	0.9	0.9	4.00
OA322D4							OA322D4
A	B	C	D	E	F	G	
0.8	0.9	0.9	0.9	1.1	0.9	0.9	4.67



# OA322/OA322D2/OA322D4

## 3-OR and Two 2-ORs into 3-NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA322

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.618	$0.448 + 0.085 \cdot \text{SL}$	$0.437 + 0.088 \cdot \text{SL}$	$0.425 + 0.089 \cdot \text{SL}$
	$t_F$	0.560	$0.368 + 0.096 \cdot \text{SL}$	$0.364 + 0.097 \cdot \text{SL}$	$0.367 + 0.097 \cdot \text{SL}$
	$t_{PLH}$	0.230	$0.150 + 0.040 \cdot \text{SL}$	$0.154 + 0.039 \cdot \text{SL}$	$0.157 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.334	$0.243 + 0.045 \cdot \text{SL}$	$0.244 + 0.045 \cdot \text{SL}$	$0.246 + 0.045 \cdot \text{SL}$
B to Y	$t_R$	0.619	$0.446 + 0.086 \cdot \text{SL}$	$0.441 + 0.088 \cdot \text{SL}$	$0.431 + 0.089 \cdot \text{SL}$
	$t_F$	0.628	$0.435 + 0.096 \cdot \text{SL}$	$0.433 + 0.097 \cdot \text{SL}$	$0.435 + 0.097 \cdot \text{SL}$
	$t_{PLH}$	0.255	$0.175 + 0.040 \cdot \text{SL}$	$0.179 + 0.039 \cdot \text{SL}$	$0.183 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.380	$0.290 + 0.045 \cdot \text{SL}$	$0.291 + 0.045 \cdot \text{SL}$	$0.292 + 0.045 \cdot \text{SL}$
C to Y	$t_R$	0.616	$0.443 + 0.087 \cdot \text{SL}$	$0.437 + 0.088 \cdot \text{SL}$	$0.430 + 0.089 \cdot \text{SL}$
	$t_F$	0.695	$0.503 + 0.096 \cdot \text{SL}$	$0.501 + 0.097 \cdot \text{SL}$	$0.503 + 0.096 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.183 + 0.040 \cdot \text{SL}$	$0.187 + 0.039 \cdot \text{SL}$	$0.192 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.414	$0.323 + 0.046 \cdot \text{SL}$	$0.326 + 0.045 \cdot \text{SL}$	$0.328 + 0.045 \cdot \text{SL}$
D to Y	$t_R$	0.463	$0.351 + 0.056 \cdot \text{SL}$	$0.343 + 0.058 \cdot \text{SL}$	$0.329 + 0.060 \cdot \text{SL}$
	$t_F$	0.636	$0.443 + 0.096 \cdot \text{SL}$	$0.442 + 0.097 \cdot \text{SL}$	$0.440 + 0.097 \cdot \text{SL}$
	$t_{PLH}$	0.203	$0.149 + 0.027 \cdot \text{SL}$	$0.151 + 0.026 \cdot \text{SL}$	$0.154 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.411	$0.318 + 0.047 \cdot \text{SL}$	$0.322 + 0.046 \cdot \text{SL}$	$0.326 + 0.045 \cdot \text{SL}$
E to Y	$t_R$	0.456	$0.341 + 0.057 \cdot \text{SL}$	$0.336 + 0.059 \cdot \text{SL}$	$0.330 + 0.060 \cdot \text{SL}$
	$t_F$	0.696	$0.504 + 0.096 \cdot \text{SL}$	$0.504 + 0.096 \cdot \text{SL}$	$0.503 + 0.096 \cdot \text{SL}$
	$t_{PLH}$	0.206	$0.152 + 0.027 \cdot \text{SL}$	$0.155 + 0.026 \cdot \text{SL}$	$0.158 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.456	$0.364 + 0.046 \cdot \text{SL}$	$0.367 + 0.045 \cdot \text{SL}$	$0.370 + 0.045 \cdot \text{SL}$
F to Y	$t_R$	0.491	$0.380 + 0.055 \cdot \text{SL}$	$0.371 + 0.058 \cdot \text{SL}$	$0.357 + 0.059 \cdot \text{SL}$
	$t_F$	0.635	$0.443 + 0.096 \cdot \text{SL}$	$0.442 + 0.096 \cdot \text{SL}$	$0.440 + 0.097 \cdot \text{SL}$
	$t_{PLH}$	0.218	$0.165 + 0.027 \cdot \text{SL}$	$0.167 + 0.026 \cdot \text{SL}$	$0.170 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.421	$0.328 + 0.047 \cdot \text{SL}$	$0.332 + 0.046 \cdot \text{SL}$	$0.337 + 0.045 \cdot \text{SL}$
G to Y	$t_R$	0.484	$0.370 + 0.057 \cdot \text{SL}$	$0.364 + 0.058 \cdot \text{SL}$	$0.357 + 0.059 \cdot \text{SL}$
	$t_F$	0.696	$0.504 + 0.096 \cdot \text{SL}$	$0.503 + 0.096 \cdot \text{SL}$	$0.503 + 0.096 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.165 + 0.027 \cdot \text{SL}$	$0.168 + 0.026 \cdot \text{SL}$	$0.171 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.463	$0.371 + 0.046 \cdot \text{SL}$	$0.374 + 0.045 \cdot \text{SL}$	$0.378 + 0.045 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA322D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.066 + 0.013 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.371	$0.353 + 0.009 \cdot \text{SL}$	$0.360 + 0.007 \cdot \text{SL}$	$0.368 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.483	$0.463 + 0.010 \cdot \text{SL}$	$0.471 + 0.008 \cdot \text{SL}$	$0.482 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.067 + 0.014 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.395	$0.376 + 0.009 \cdot \text{SL}$	$0.384 + 0.007 \cdot \text{SL}$	$0.392 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.540	$0.520 + 0.010 \cdot \text{SL}$	$0.528 + 0.008 \cdot \text{SL}$	$0.539 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.102	$0.076 + 0.013 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.071 + 0.013 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.403	$0.384 + 0.009 \cdot \text{SL}$	$0.392 + 0.007 \cdot \text{SL}$	$0.400 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.584	$0.563 + 0.010 \cdot \text{SL}$	$0.571 + 0.008 \cdot \text{SL}$	$0.583 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.099	$0.071 + 0.014 \cdot \text{SL}$	$0.071 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.070 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.349	$0.331 + 0.009 \cdot \text{SL}$	$0.338 + 0.007 \cdot \text{SL}$	$0.346 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.567	$0.546 + 0.010 \cdot \text{SL}$	$0.554 + 0.008 \cdot \text{SL}$	$0.566 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.100	$0.074 + 0.013 \cdot \text{SL}$	$0.069 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.072 + 0.013 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.355	$0.337 + 0.009 \cdot \text{SL}$	$0.344 + 0.007 \cdot \text{SL}$	$0.352 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.627	$0.606 + 0.010 \cdot \text{SL}$	$0.614 + 0.008 \cdot \text{SL}$	$0.626 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.101	$0.073 + 0.014 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.068 + 0.014 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.366	$0.348 + 0.009 \cdot \text{SL}$	$0.355 + 0.007 \cdot \text{SL}$	$0.363 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.577	$0.556 + 0.010 \cdot \text{SL}$	$0.565 + 0.008 \cdot \text{SL}$	$0.576 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.101	$0.073 + 0.014 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.097	$0.071 + 0.013 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.368	$0.350 + 0.009 \cdot \text{SL}$	$0.357 + 0.007 \cdot \text{SL}$	$0.365 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.631	$0.610 + 0.010 \cdot \text{SL}$	$0.619 + 0.008 \cdot \text{SL}$	$0.630 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## OA322/OA322D2/OA322D4

### 3-OR and Two 2-ORs into 3-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA322D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.098	$0.084 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.086	$0.072 + 0.007 \cdot \text{SL}$	$0.075 + 0.006 \cdot \text{SL}$	$0.069 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.411	$0.400 + 0.006 \cdot \text{SL}$	$0.407 + 0.004 \cdot \text{SL}$	$0.420 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.499	$0.487 + 0.006 \cdot \text{SL}$	$0.493 + 0.004 \cdot \text{SL}$	$0.508 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.098	$0.084 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.088	$0.075 + 0.006 \cdot \text{SL}$	$0.077 + 0.006 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.435	$0.424 + 0.006 \cdot \text{SL}$	$0.430 + 0.004 \cdot \text{SL}$	$0.444 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.555	$0.543 + 0.006 \cdot \text{SL}$	$0.549 + 0.004 \cdot \text{SL}$	$0.565 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.099	$0.086 + 0.006 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.092	$0.078 + 0.007 \cdot \text{SL}$	$0.081 + 0.006 \cdot \text{SL}$	$0.073 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.444	$0.432 + 0.006 \cdot \text{SL}$	$0.439 + 0.004 \cdot \text{SL}$	$0.452 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.598	$0.586 + 0.006 \cdot \text{SL}$	$0.592 + 0.004 \cdot \text{SL}$	$0.608 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.095	$0.081 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$
	$t_F$	0.089	$0.075 + 0.007 \cdot \text{SL}$	$0.078 + 0.006 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.385	$0.374 + 0.005 \cdot \text{SL}$	$0.380 + 0.004 \cdot \text{SL}$	$0.393 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.581	$0.569 + 0.006 \cdot \text{SL}$	$0.575 + 0.004 \cdot \text{SL}$	$0.591 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.095	$0.082 + 0.006 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$
	$t_F$	0.092	$0.077 + 0.007 \cdot \text{SL}$	$0.081 + 0.006 \cdot \text{SL}$	$0.073 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.391	$0.380 + 0.006 \cdot \text{SL}$	$0.386 + 0.004 \cdot \text{SL}$	$0.399 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.641	$0.629 + 0.006 \cdot \text{SL}$	$0.635 + 0.004 \cdot \text{SL}$	$0.651 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.097	$0.084 + 0.006 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.089	$0.077 + 0.006 \cdot \text{SL}$	$0.076 + 0.006 \cdot \text{SL}$	$0.073 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.401	$0.390 + 0.005 \cdot \text{SL}$	$0.396 + 0.004 \cdot \text{SL}$	$0.409 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.592	$0.580 + 0.006 \cdot \text{SL}$	$0.586 + 0.004 \cdot \text{SL}$	$0.602 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.095	$0.082 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
	$t_F$	0.091	$0.078 + 0.007 \cdot \text{SL}$	$0.081 + 0.006 \cdot \text{SL}$	$0.075 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.402	$0.391 + 0.006 \cdot \text{SL}$	$0.398 + 0.004 \cdot \text{SL}$	$0.411 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.645	$0.633 + 0.006 \cdot \text{SL}$	$0.640 + 0.004 \cdot \text{SL}$	$0.655 + 0.004 \cdot \text{SL}$

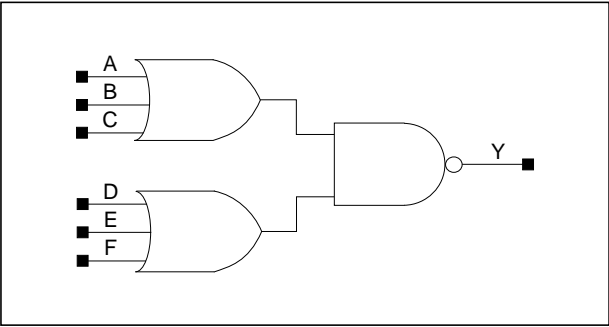
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



OA33/OA33D2/OA33D4

Two 3-ORs into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
Other States						0

Cell Data

Input Load (SL)																	
OA33						OA33D2						OA33D4					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.8	0.8	0.9	0.8	0.8	0.9	0.8	0.8	0.9	0.8	0.8	0.9	0.8	0.8	0.9	0.8	0.8	0.9
Gate Count																	
OA33						OA33D2						OA33D4					
2.33						3.33						4.00					



## OA33/OA33D2/OA33D4

### Two 3-ORs into 2-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.608	$0.441 + 0.083 \cdot \text{SL}$	$0.427 + 0.087 \cdot \text{SL}$	$0.411 + 0.089 \cdot \text{SL}$
	$t_F$	0.495	$0.315 + 0.090 \cdot \text{SL}$	$0.310 + 0.091 \cdot \text{SL}$	$0.310 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.198	$0.119 + 0.040 \cdot \text{SL}$	$0.120 + 0.039 \cdot \text{SL}$	$0.122 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.317	$0.227 + 0.045 \cdot \text{SL}$	$0.231 + 0.044 \cdot \text{SL}$	$0.235 + 0.044 \cdot \text{SL}$
B to Y	$t_R$	0.608	$0.438 + 0.085 \cdot \text{SL}$	$0.429 + 0.087 \cdot \text{SL}$	$0.417 + 0.089 \cdot \text{SL}$
	$t_F$	0.558	$0.377 + 0.090 \cdot \text{SL}$	$0.374 + 0.091 \cdot \text{SL}$	$0.374 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.223	$0.143 + 0.040 \cdot \text{SL}$	$0.145 + 0.040 \cdot \text{SL}$	$0.148 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.364	$0.274 + 0.045 \cdot \text{SL}$	$0.277 + 0.044 \cdot \text{SL}$	$0.281 + 0.044 \cdot \text{SL}$
C to Y	$t_R$	0.604	$0.433 + 0.085 \cdot \text{SL}$	$0.425 + 0.087 \cdot \text{SL}$	$0.415 + 0.089 \cdot \text{SL}$
	$t_F$	0.620	$0.440 + 0.090 \cdot \text{SL}$	$0.438 + 0.091 \cdot \text{SL}$	$0.437 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.231	$0.151 + 0.040 \cdot \text{SL}$	$0.153 + 0.040 \cdot \text{SL}$	$0.157 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.397	$0.307 + 0.045 \cdot \text{SL}$	$0.311 + 0.044 \cdot \text{SL}$	$0.315 + 0.044 \cdot \text{SL}$
D to Y	$t_R$	0.563	$0.392 + 0.086 \cdot \text{SL}$	$0.380 + 0.089 \cdot \text{SL}$	$0.369 + 0.090 \cdot \text{SL}$
	$t_F$	0.495	$0.314 + 0.090 \cdot \text{SL}$	$0.311 + 0.091 \cdot \text{SL}$	$0.310 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.235	$0.157 + 0.039 \cdot \text{SL}$	$0.159 + 0.039 \cdot \text{SL}$	$0.161 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.333	$0.242 + 0.046 \cdot \text{SL}$	$0.247 + 0.044 \cdot \text{SL}$	$0.252 + 0.044 \cdot \text{SL}$
E to Y	$t_R$	0.564	$0.390 + 0.087 \cdot \text{SL}$	$0.384 + 0.088 \cdot \text{SL}$	$0.375 + 0.090 \cdot \text{SL}$
	$t_F$	0.556	$0.374 + 0.091 \cdot \text{SL}$	$0.373 + 0.091 \cdot \text{SL}$	$0.372 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.259	$0.180 + 0.040 \cdot \text{SL}$	$0.183 + 0.039 \cdot \text{SL}$	$0.186 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.379	$0.289 + 0.045 \cdot \text{SL}$	$0.293 + 0.044 \cdot \text{SL}$	$0.297 + 0.044 \cdot \text{SL}$
F to Y	$t_R$	0.560	$0.385 + 0.088 \cdot \text{SL}$	$0.380 + 0.089 \cdot \text{SL}$	$0.374 + 0.090 \cdot \text{SL}$
	$t_F$	0.620	$0.440 + 0.090 \cdot \text{SL}$	$0.439 + 0.090 \cdot \text{SL}$	$0.437 + 0.091 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.190 + 0.040 \cdot \text{SL}$	$0.193 + 0.039 \cdot \text{SL}$	$0.196 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.416	$0.325 + 0.045 \cdot \text{SL}$	$0.330 + 0.044 \cdot \text{SL}$	$0.335 + 0.044 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

OA33D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.102	$0.075 + 0.013 \cdot \text{SL}$	$0.072 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.337	$0.318 + 0.009 \cdot \text{SL}$	$0.326 + 0.007 \cdot \text{SL}$	$0.334 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.442	$0.422 + 0.010 \cdot \text{SL}$	$0.430 + 0.008 \cdot \text{SL}$	$0.441 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.360	$0.342 + 0.009 \cdot \text{SL}$	$0.349 + 0.007 \cdot \text{SL}$	$0.358 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.498	$0.478 + 0.010 \cdot \text{SL}$	$0.486 + 0.008 \cdot \text{SL}$	$0.497 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.101	$0.073 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.066 + 0.014 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.369	$0.351 + 0.009 \cdot \text{SL}$	$0.358 + 0.007 \cdot \text{SL}$	$0.366 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.541	$0.521 + 0.010 \cdot \text{SL}$	$0.529 + 0.008 \cdot \text{SL}$	$0.540 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.104	$0.076 + 0.014 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.063 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.373	$0.355 + 0.009 \cdot \text{SL}$	$0.362 + 0.007 \cdot \text{SL}$	$0.371 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.460	$0.440 + 0.010 \cdot \text{SL}$	$0.448 + 0.008 \cdot \text{SL}$	$0.458 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.104	$0.077 + 0.014 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.398	$0.379 + 0.009 \cdot \text{SL}$	$0.387 + 0.007 \cdot \text{SL}$	$0.395 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.518	$0.497 + 0.010 \cdot \text{SL}$	$0.505 + 0.008 \cdot \text{SL}$	$0.516 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.105	$0.078 + 0.013 \cdot \text{SL}$	$0.075 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.066 + 0.014 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.407	$0.388 + 0.009 \cdot \text{SL}$	$0.396 + 0.007 \cdot \text{SL}$	$0.405 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.561	$0.541 + 0.010 \cdot \text{SL}$	$0.549 + 0.008 \cdot \text{SL}$	$0.560 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## OA33/OA33D2/OA33D4

### Two 3-ORs into 2-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA33D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.099	$0.086 + 0.007 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_F$	0.082	$0.069 + 0.007 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.367 + 0.006 \cdot \text{SL}$	$0.373 + 0.004 \cdot \text{SL}$	$0.387 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.462	$0.450 + 0.006 \cdot \text{SL}$	$0.456 + 0.004 \cdot \text{SL}$	$0.471 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.099	$0.086 + 0.007 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.401	$0.390 + 0.006 \cdot \text{SL}$	$0.396 + 0.004 \cdot \text{SL}$	$0.410 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.517	$0.505 + 0.006 \cdot \text{SL}$	$0.511 + 0.004 \cdot \text{SL}$	$0.527 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.098	$0.085 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.087	$0.074 + 0.007 \cdot \text{SL}$	$0.076 + 0.006 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.410	$0.399 + 0.006 \cdot \text{SL}$	$0.405 + 0.004 \cdot \text{SL}$	$0.419 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.560	$0.548 + 0.006 \cdot \text{SL}$	$0.554 + 0.004 \cdot \text{SL}$	$0.570 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.100	$0.087 + 0.006 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_F$	0.083	$0.069 + 0.007 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.415	$0.404 + 0.006 \cdot \text{SL}$	$0.410 + 0.004 \cdot \text{SL}$	$0.424 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.480	$0.468 + 0.006 \cdot \text{SL}$	$0.474 + 0.004 \cdot \text{SL}$	$0.489 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.100	$0.088 + 0.006 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.440	$0.428 + 0.006 \cdot \text{SL}$	$0.435 + 0.004 \cdot \text{SL}$	$0.449 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.536	$0.525 + 0.006 \cdot \text{SL}$	$0.531 + 0.004 \cdot \text{SL}$	$0.546 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.100	$0.087 + 0.007 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_F$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.076 + 0.006 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.449	$0.438 + 0.006 \cdot \text{SL}$	$0.444 + 0.004 \cdot \text{SL}$	$0.458 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.580	$0.568 + 0.006 \cdot \text{SL}$	$0.574 + 0.004 \cdot \text{SL}$	$0.590 + 0.004 \cdot \text{SL}$

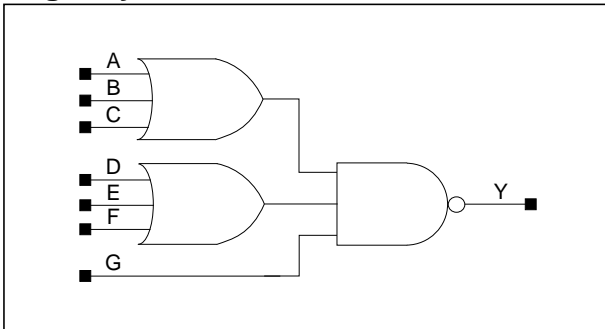
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## OA331/OA331D2/OA331D4

### Two 3-ORs into 3-NAND with 1X/2X/4X Drive

#### Logic Symbol



#### Truth Table

A	B	C	D	E	F	G	Y
0	0	0	x	x	x	x	1
x	x	x	0	0	0	x	1
x	x	x	x	x	x	0	1
Other States							0

#### Cell Data

Input Load (SL)							Gate Count
OA331							OA331
A	B	C	D	E	F	G	
0.9	0.9	1.0	0.9	0.9	0.9	0.9	3.00
OA331D2							OA331D2
A	B	C	D	E	F	G	
0.9	0.9	1.0	0.9	0.9	0.9	0.9	3.67
OA331D4							OA331D4
A	B	C	D	E	F	G	
0.9	0.9	1.0	0.9	0.9	0.9	0.9	4.33



# OA331/OA331D2/OA331D4

## Two 3-ORs into 3-NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA331

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.630	$0.462 + 0.084 \cdot \text{SL}$	$0.448 + 0.088 \cdot \text{SL}$	$0.435 + 0.089 \cdot \text{SL}$
	$t_F$	0.517	$0.346 + 0.085 \cdot \text{SL}$	$0.341 + 0.087 \cdot \text{SL}$	$0.340 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.213	$0.133 + 0.040 \cdot \text{SL}$	$0.135 + 0.039 \cdot \text{SL}$	$0.137 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.295	$0.211 + 0.042 \cdot \text{SL}$	$0.215 + 0.041 \cdot \text{SL}$	$0.219 + 0.040 \cdot \text{SL}$
B to Y	$t_R$	0.631	$0.460 + 0.085 \cdot \text{SL}$	$0.452 + 0.087 \cdot \text{SL}$	$0.441 + 0.089 \cdot \text{SL}$
	$t_F$	0.576	$0.404 + 0.086 \cdot \text{SL}$	$0.400 + 0.087 \cdot \text{SL}$	$0.400 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.237	$0.156 + 0.040 \cdot \text{SL}$	$0.159 + 0.040 \cdot \text{SL}$	$0.162 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.337	$0.254 + 0.041 \cdot \text{SL}$	$0.257 + 0.041 \cdot \text{SL}$	$0.260 + 0.040 \cdot \text{SL}$
C to Y	$t_R$	0.628	$0.456 + 0.086 \cdot \text{SL}$	$0.449 + 0.088 \cdot \text{SL}$	$0.440 + 0.089 \cdot \text{SL}$
	$t_F$	0.636	$0.465 + 0.085 \cdot \text{SL}$	$0.460 + 0.086 \cdot \text{SL}$	$0.461 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.246	$0.165 + 0.041 \cdot \text{SL}$	$0.167 + 0.040 \cdot \text{SL}$	$0.172 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.368	$0.285 + 0.042 \cdot \text{SL}$	$0.289 + 0.041 \cdot \text{SL}$	$0.293 + 0.040 \cdot \text{SL}$
D to Y	$t_R$	0.599	$0.427 + 0.086 \cdot \text{SL}$	$0.419 + 0.088 \cdot \text{SL}$	$0.410 + 0.089 \cdot \text{SL}$
	$t_F$	0.515	$0.345 + 0.085 \cdot \text{SL}$	$0.341 + 0.086 \cdot \text{SL}$	$0.338 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.185 + 0.039 \cdot \text{SL}$	$0.187 + 0.039 \cdot \text{SL}$	$0.189 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.325	$0.242 + 0.042 \cdot \text{SL}$	$0.246 + 0.041 \cdot \text{SL}$	$0.251 + 0.040 \cdot \text{SL}$
E to Y	$t_R$	0.602	$0.428 + 0.087 \cdot \text{SL}$	$0.423 + 0.088 \cdot \text{SL}$	$0.416 + 0.089 \cdot \text{SL}$
	$t_F$	0.576	$0.404 + 0.086 \cdot \text{SL}$	$0.402 + 0.086 \cdot \text{SL}$	$0.399 + 0.087 \cdot \text{SL}$
	$t_{PLH}$	0.287	$0.209 + 0.039 \cdot \text{SL}$	$0.211 + 0.039 \cdot \text{SL}$	$0.214 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.369	$0.286 + 0.042 \cdot \text{SL}$	$0.289 + 0.041 \cdot \text{SL}$	$0.293 + 0.040 \cdot \text{SL}$
F to Y	$t_R$	0.599	$0.424 + 0.087 \cdot \text{SL}$	$0.420 + 0.088 \cdot \text{SL}$	$0.415 + 0.089 \cdot \text{SL}$
	$t_F$	0.638	$0.467 + 0.085 \cdot \text{SL}$	$0.465 + 0.086 \cdot \text{SL}$	$0.462 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.298	$0.219 + 0.040 \cdot \text{SL}$	$0.222 + 0.039 \cdot \text{SL}$	$0.225 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.403	$0.319 + 0.042 \cdot \text{SL}$	$0.323 + 0.041 \cdot \text{SL}$	$0.328 + 0.040 \cdot \text{SL}$
G to Y	$t_R$	0.295	$0.243 + 0.026 \cdot \text{SL}$	$0.235 + 0.028 \cdot \text{SL}$	$0.221 + 0.030 \cdot \text{SL}$
	$t_F$	0.636	$0.465 + 0.086 \cdot \text{SL}$	$0.464 + 0.086 \cdot \text{SL}$	$0.462 + 0.086 \cdot \text{SL}$
	$t_{PLH}$	0.140	$0.112 + 0.014 \cdot \text{SL}$	$0.113 + 0.014 \cdot \text{SL}$	$0.115 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.415	$0.331 + 0.042 \cdot \text{SL}$	$0.335 + 0.041 \cdot \text{SL}$	$0.341 + 0.040 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA331D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.104	$0.077 + 0.013 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.064 + 0.014 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.359	$0.340 + 0.009 \cdot \text{SL}$	$0.348 + 0.007 \cdot \text{SL}$	$0.357 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.439	$0.419 + 0.010 \cdot \text{SL}$	$0.427 + 0.008 \cdot \text{SL}$	$0.438 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.104	$0.078 + 0.013 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.094	$0.067 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.382	$0.363 + 0.009 \cdot \text{SL}$	$0.371 + 0.007 \cdot \text{SL}$	$0.380 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.491	$0.471 + 0.010 \cdot \text{SL}$	$0.479 + 0.008 \cdot \text{SL}$	$0.490 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.103	$0.075 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.069 + 0.013 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.390	$0.372 + 0.009 \cdot \text{SL}$	$0.379 + 0.007 \cdot \text{SL}$	$0.388 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.531	$0.510 + 0.010 \cdot \text{SL}$	$0.518 + 0.008 \cdot \text{SL}$	$0.530 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.107	$0.081 + 0.013 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.064 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.406	$0.387 + 0.009 \cdot \text{SL}$	$0.395 + 0.007 \cdot \text{SL}$	$0.404 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.469	$0.448 + 0.010 \cdot \text{SL}$	$0.456 + 0.008 \cdot \text{SL}$	$0.468 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.107	$0.080 + 0.013 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.067 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.429	$0.410 + 0.009 \cdot \text{SL}$	$0.419 + 0.007 \cdot \text{SL}$	$0.428 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.522	$0.502 + 0.010 \cdot \text{SL}$	$0.510 + 0.008 \cdot \text{SL}$	$0.521 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.106	$0.079 + 0.014 \cdot \text{SL}$	$0.078 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.070 + 0.013 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.440	$0.421 + 0.009 \cdot \text{SL}$	$0.429 + 0.007 \cdot \text{SL}$	$0.438 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.565	$0.544 + 0.010 \cdot \text{SL}$	$0.553 + 0.008 \cdot \text{SL}$	$0.564 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.090	$0.061 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.069 + 0.014 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.275	$0.257 + 0.009 \cdot \text{SL}$	$0.263 + 0.007 \cdot \text{SL}$	$0.270 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.577	$0.557 + 0.010 \cdot \text{SL}$	$0.565 + 0.008 \cdot \text{SL}$	$0.576 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# OA331/OA331D2/OA331D4

## Two 3-ORs into 3-NAND with 1X/2X/4X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA331D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.099	$0.085 + 0.007 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.084	$0.071 + 0.007 \cdot \text{SL}$	$0.073 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.395	$0.384 + 0.006 \cdot \text{SL}$	$0.391 + 0.004 \cdot \text{SL}$	$0.404 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.455	$0.444 + 0.006 \cdot \text{SL}$	$0.449 + 0.004 \cdot \text{SL}$	$0.465 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.099	$0.086 + 0.007 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$
	$t_F$	0.087	$0.074 + 0.006 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.419	$0.407 + 0.006 \cdot \text{SL}$	$0.414 + 0.004 \cdot \text{SL}$	$0.428 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.507	$0.495 + 0.006 \cdot \text{SL}$	$0.501 + 0.004 \cdot \text{SL}$	$0.517 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.099	$0.086 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_F$	0.089	$0.076 + 0.007 \cdot \text{SL}$	$0.078 + 0.006 \cdot \text{SL}$	$0.073 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.427	$0.416 + 0.006 \cdot \text{SL}$	$0.422 + 0.004 \cdot \text{SL}$	$0.436 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.546	$0.534 + 0.006 \cdot \text{SL}$	$0.541 + 0.004 \cdot \text{SL}$	$0.556 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.102	$0.090 + 0.006 \cdot \text{SL}$	$0.088 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_F$	0.084	$0.071 + 0.006 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$	$0.069 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.443	$0.432 + 0.006 \cdot \text{SL}$	$0.439 + 0.004 \cdot \text{SL}$	$0.453 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.485	$0.473 + 0.006 \cdot \text{SL}$	$0.479 + 0.004 \cdot \text{SL}$	$0.495 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.102	$0.089 + 0.006 \cdot \text{SL}$	$0.088 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_F$	0.087	$0.073 + 0.007 \cdot \text{SL}$	$0.076 + 0.006 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.467	$0.456 + 0.006 \cdot \text{SL}$	$0.462 + 0.004 \cdot \text{SL}$	$0.477 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.538	$0.526 + 0.006 \cdot \text{SL}$	$0.532 + 0.004 \cdot \text{SL}$	$0.548 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.101	$0.088 + 0.006 \cdot \text{SL}$	$0.087 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_F$	0.089	$0.076 + 0.007 \cdot \text{SL}$	$0.079 + 0.006 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.478	$0.466 + 0.006 \cdot \text{SL}$	$0.473 + 0.004 \cdot \text{SL}$	$0.487 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.580	$0.568 + 0.006 \cdot \text{SL}$	$0.575 + 0.004 \cdot \text{SL}$	$0.591 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.086	$0.073 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_F$	0.089	$0.077 + 0.006 \cdot \text{SL}$	$0.076 + 0.006 \cdot \text{SL}$	$0.073 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.294	$0.283 + 0.005 \cdot \text{SL}$	$0.289 + 0.004 \cdot \text{SL}$	$0.300 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.593	$0.581 + 0.006 \cdot \text{SL}$	$0.587 + 0.004 \cdot \text{SL}$	$0.603 + 0.004 \cdot \text{SL}$

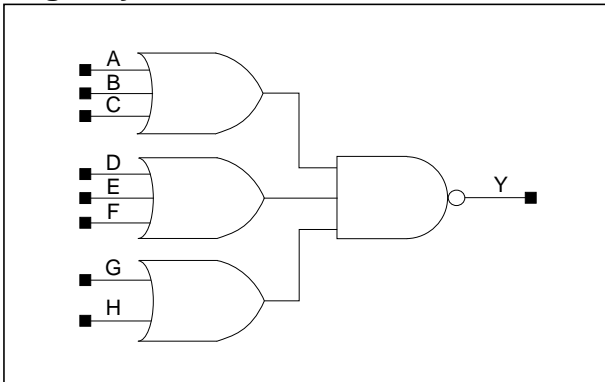
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## OA332/OA332D2/OA332D4

Two 3-ORs and 2-OR into 3-NAND with 1X/2X/4X Drive

### Logic Symbol



### Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	x	x	x	x	x	1
x	x	x	0	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

### Cell Data

Input Load (SL)								Gate Count
OA332								OA332
A	B	C	D	E	F	G	H	
0.8	0.9	0.9	0.8	0.9	0.9	0.8	0.9	3.33
OA332D2								OA332D2
A	B	C	D	E	F	G	H	
0.8	0.9	0.9	0.8	0.9	0.9	0.8	0.9	4.33
OA332D4								OA332D4
A	B	C	D	E	F	G	H	
0.8	0.9	0.9	0.8	0.9	0.9	0.8	0.9	5.00



## OA332/OA332D2/OA332D4

### Two 3-ORs and 2-OR into 3-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA332

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.716	$0.547 + 0.084 \cdot \text{SL}$	$0.535 + 0.087 \cdot \text{SL}$	$0.521 + 0.089 \cdot \text{SL}$
	$t_F$	0.534	$0.351 + 0.092 \cdot \text{SL}$	$0.346 + 0.093 \cdot \text{SL}$	$0.346 + 0.093 \cdot \text{SL}$
	$t_{PLH}$	0.230	$0.149 + 0.040 \cdot \text{SL}$	$0.152 + 0.040 \cdot \text{SL}$	$0.156 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.322	$0.232 + 0.045 \cdot \text{SL}$	$0.236 + 0.044 \cdot \text{SL}$	$0.240 + 0.044 \cdot \text{SL}$
B to Y	$t_R$	0.716	$0.545 + 0.086 \cdot \text{SL}$	$0.538 + 0.087 \cdot \text{SL}$	$0.526 + 0.089 \cdot \text{SL}$
	$t_F$	0.598	$0.413 + 0.092 \cdot \text{SL}$	$0.410 + 0.093 \cdot \text{SL}$	$0.411 + 0.093 \cdot \text{SL}$
	$t_{PLH}$	0.255	$0.174 + 0.041 \cdot \text{SL}$	$0.177 + 0.040 \cdot \text{SL}$	$0.182 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.369	$0.279 + 0.045 \cdot \text{SL}$	$0.282 + 0.044 \cdot \text{SL}$	$0.286 + 0.044 \cdot \text{SL}$
C to Y	$t_R$	0.713	$0.541 + 0.086 \cdot \text{SL}$	$0.534 + 0.088 \cdot \text{SL}$	$0.525 + 0.089 \cdot \text{SL}$
	$t_F$	0.661	$0.477 + 0.092 \cdot \text{SL}$	$0.475 + 0.093 \cdot \text{SL}$	$0.476 + 0.092 \cdot \text{SL}$
	$t_{PLH}$	0.264	$0.182 + 0.041 \cdot \text{SL}$	$0.186 + 0.040 \cdot \text{SL}$	$0.191 + 0.039 \cdot \text{SL}$
	$t_{PHL}$	0.403	$0.313 + 0.045 \cdot \text{SL}$	$0.317 + 0.044 \cdot \text{SL}$	$0.321 + 0.044 \cdot \text{SL}$
D to Y	$t_R$	0.675	$0.504 + 0.086 \cdot \text{SL}$	$0.494 + 0.088 \cdot \text{SL}$	$0.484 + 0.089 \cdot \text{SL}$
	$t_F$	0.711	$0.492 + 0.109 \cdot \text{SL}$	$0.491 + 0.110 \cdot \text{SL}$	$0.489 + 0.110 \cdot \text{SL}$
	$t_{PLH}$	0.271	$0.192 + 0.039 \cdot \text{SL}$	$0.195 + 0.039 \cdot \text{SL}$	$0.197 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.460	$0.354 + 0.053 \cdot \text{SL}$	$0.358 + 0.052 \cdot \text{SL}$	$0.363 + 0.051 \cdot \text{SL}$
E to Y	$t_R$	0.676	$0.503 + 0.087 \cdot \text{SL}$	$0.498 + 0.088 \cdot \text{SL}$	$0.490 + 0.089 \cdot \text{SL}$
	$t_F$	0.785	$0.565 + 0.110 \cdot \text{SL}$	$0.565 + 0.110 \cdot \text{SL}$	$0.564 + 0.110 \cdot \text{SL}$
	$t_{PLH}$	0.296	$0.217 + 0.040 \cdot \text{SL}$	$0.219 + 0.039 \cdot \text{SL}$	$0.223 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.514	$0.409 + 0.052 \cdot \text{SL}$	$0.412 + 0.052 \cdot \text{SL}$	$0.416 + 0.051 \cdot \text{SL}$
F to Y	$t_R$	0.673	$0.499 + 0.087 \cdot \text{SL}$	$0.494 + 0.088 \cdot \text{SL}$	$0.489 + 0.089 \cdot \text{SL}$
	$t_F$	0.862	$0.643 + 0.110 \cdot \text{SL}$	$0.643 + 0.109 \cdot \text{SL}$	$0.642 + 0.110 \cdot \text{SL}$
	$t_{PLH}$	0.306	$0.227 + 0.040 \cdot \text{SL}$	$0.230 + 0.039 \cdot \text{SL}$	$0.234 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.559	$0.454 + 0.052 \cdot \text{SL}$	$0.458 + 0.052 \cdot \text{SL}$	$0.462 + 0.051 \cdot \text{SL}$
G to Y	$t_R$	0.497	$0.387 + 0.055 \cdot \text{SL}$	$0.378 + 0.057 \cdot \text{SL}$	$0.364 + 0.059 \cdot \text{SL}$
	$t_F$	0.791	$0.573 + 0.109 \cdot \text{SL}$	$0.572 + 0.109 \cdot \text{SL}$	$0.570 + 0.109 \cdot \text{SL}$
	$t_{PLH}$	0.222	$0.168 + 0.027 \cdot \text{SL}$	$0.170 + 0.026 \cdot \text{SL}$	$0.174 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.532	$0.426 + 0.053 \cdot \text{SL}$	$0.431 + 0.052 \cdot \text{SL}$	$0.437 + 0.051 \cdot \text{SL}$
H to Y	$t_R$	0.491	$0.377 + 0.057 \cdot \text{SL}$	$0.371 + 0.058 \cdot \text{SL}$	$0.364 + 0.059 \cdot \text{SL}$
	$t_F$	0.862	$0.642 + 0.110 \cdot \text{SL}$	$0.643 + 0.110 \cdot \text{SL}$	$0.642 + 0.110 \cdot \text{SL}$
	$t_{PLH}$	0.222	$0.168 + 0.027 \cdot \text{SL}$	$0.171 + 0.026 \cdot \text{SL}$	$0.174 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.580	$0.475 + 0.053 \cdot \text{SL}$	$0.479 + 0.052 \cdot \text{SL}$	$0.484 + 0.051 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA332D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.108	$0.083 + 0.013 \cdot \text{SL}$	$0.078 + 0.014 \cdot \text{SL}$	$0.066 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.064 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.384	$0.366 + 0.009 \cdot \text{SL}$	$0.374 + 0.007 \cdot \text{SL}$	$0.383 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.469	$0.448 + 0.010 \cdot \text{SL}$	$0.456 + 0.008 \cdot \text{SL}$	$0.467 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.108	$0.083 + 0.013 \cdot \text{SL}$	$0.079 + 0.014 \cdot \text{SL}$	$0.066 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.068 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.409	$0.390 + 0.009 \cdot \text{SL}$	$0.398 + 0.007 \cdot \text{SL}$	$0.407 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.524	$0.504 + 0.010 \cdot \text{SL}$	$0.512 + 0.008 \cdot \text{SL}$	$0.523 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.108	$0.080 + 0.014 \cdot \text{SL}$	$0.080 + 0.014 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.071 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.418	$0.399 + 0.010 \cdot \text{SL}$	$0.407 + 0.007 \cdot \text{SL}$	$0.416 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.567	$0.546 + 0.010 \cdot \text{SL}$	$0.555 + 0.008 \cdot \text{SL}$	$0.566 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.110	$0.083 + 0.013 \cdot \text{SL}$	$0.081 + 0.014 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$
	$t_F$	0.099	$0.072 + 0.013 \cdot \text{SL}$	$0.075 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.423	$0.404 + 0.010 \cdot \text{SL}$	$0.413 + 0.007 \cdot \text{SL}$	$0.422 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.617	$0.596 + 0.010 \cdot \text{SL}$	$0.605 + 0.008 \cdot \text{SL}$	$0.616 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.110	$0.083 + 0.014 \cdot \text{SL}$	$0.082 + 0.014 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$
	$t_F$	0.101	$0.075 + 0.013 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.448	$0.429 + 0.010 \cdot \text{SL}$	$0.437 + 0.007 \cdot \text{SL}$	$0.447 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.683	$0.663 + 0.010 \cdot \text{SL}$	$0.671 + 0.008 \cdot \text{SL}$	$0.683 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.110	$0.083 + 0.014 \cdot \text{SL}$	$0.082 + 0.014 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$
	$t_F$	0.106	$0.080 + 0.013 \cdot \text{SL}$	$0.082 + 0.012 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.459	$0.439 + 0.010 \cdot \text{SL}$	$0.448 + 0.007 \cdot \text{SL}$	$0.457 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.739	$0.718 + 0.011 \cdot \text{SL}$	$0.727 + 0.008 \cdot \text{SL}$	$0.739 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.106	$0.078 + 0.014 \cdot \text{SL}$	$0.078 + 0.014 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.102	$0.076 + 0.013 \cdot \text{SL}$	$0.079 + 0.012 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.377	$0.358 + 0.009 \cdot \text{SL}$	$0.366 + 0.007 \cdot \text{SL}$	$0.375 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.700	$0.679 + 0.010 \cdot \text{SL}$	$0.688 + 0.008 \cdot \text{SL}$	$0.700 + 0.007 \cdot \text{SL}$
H to Y	$t_R$	0.105	$0.077 + 0.014 \cdot \text{SL}$	$0.078 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_F$	0.106	$0.080 + 0.013 \cdot \text{SL}$	$0.082 + 0.012 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.359 + 0.009 \cdot \text{SL}$	$0.367 + 0.007 \cdot \text{SL}$	$0.376 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.761	$0.740 + 0.010 \cdot \text{SL}$	$0.748 + 0.008 \cdot \text{SL}$	$0.761 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## OA332/OA332D2/OA332D4

### Two 3-ORs and 2-OR into 3-NAND with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA332D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.105	$0.092 + 0.006 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.072 + 0.006 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$	$0.069 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.425	$0.413 + 0.006 \cdot \text{SL}$	$0.420 + 0.004 \cdot \text{SL}$	$0.435 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.487	$0.475 + 0.006 \cdot \text{SL}$	$0.482 + 0.004 \cdot \text{SL}$	$0.497 + 0.004 \cdot \text{SL}$
B to Y	$t_R$	0.104	$0.091 + 0.007 \cdot \text{SL}$	$0.090 + 0.007 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$
	$t_F$	0.088	$0.074 + 0.007 \cdot \text{SL}$	$0.077 + 0.006 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.449	$0.438 + 0.006 \cdot \text{SL}$	$0.444 + 0.004 \cdot \text{SL}$	$0.459 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.542	$0.530 + 0.006 \cdot \text{SL}$	$0.537 + 0.004 \cdot \text{SL}$	$0.552 + 0.004 \cdot \text{SL}$
C to Y	$t_R$	0.103	$0.090 + 0.007 \cdot \text{SL}$	$0.089 + 0.007 \cdot \text{SL}$	$0.077 + 0.007 \cdot \text{SL}$
	$t_F$	0.090	$0.076 + 0.007 \cdot \text{SL}$	$0.079 + 0.006 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.458	$0.446 + 0.006 \cdot \text{SL}$	$0.453 + 0.004 \cdot \text{SL}$	$0.468 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.585	$0.573 + 0.006 \cdot \text{SL}$	$0.579 + 0.004 \cdot \text{SL}$	$0.595 + 0.004 \cdot \text{SL}$
D to Y	$t_R$	0.106	$0.093 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$
	$t_F$	0.093	$0.079 + 0.007 \cdot \text{SL}$	$0.082 + 0.006 \cdot \text{SL}$	$0.075 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.464	$0.452 + 0.006 \cdot \text{SL}$	$0.460 + 0.004 \cdot \text{SL}$	$0.475 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.639	$0.627 + 0.006 \cdot \text{SL}$	$0.633 + 0.004 \cdot \text{SL}$	$0.649 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.106	$0.093 + 0.007 \cdot \text{SL}$	$0.092 + 0.007 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$
	$t_F$	0.096	$0.082 + 0.007 \cdot \text{SL}$	$0.086 + 0.006 \cdot \text{SL}$	$0.079 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.489	$0.477 + 0.006 \cdot \text{SL}$	$0.484 + 0.004 \cdot \text{SL}$	$0.499 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.704	$0.692 + 0.006 \cdot \text{SL}$	$0.699 + 0.004 \cdot \text{SL}$	$0.715 + 0.004 \cdot \text{SL}$
F to Y	$t_R$	0.105	$0.093 + 0.006 \cdot \text{SL}$	$0.091 + 0.007 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$
	$t_F$	0.101	$0.088 + 0.006 \cdot \text{SL}$	$0.089 + 0.006 \cdot \text{SL}$	$0.082 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.500	$0.488 + 0.006 \cdot \text{SL}$	$0.495 + 0.004 \cdot \text{SL}$	$0.510 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.759	$0.747 + 0.006 \cdot \text{SL}$	$0.754 + 0.004 \cdot \text{SL}$	$0.771 + 0.004 \cdot \text{SL}$
G to Y	$t_R$	0.100	$0.087 + 0.006 \cdot \text{SL}$	$0.085 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_F$	0.097	$0.083 + 0.007 \cdot \text{SL}$	$0.086 + 0.006 \cdot \text{SL}$	$0.078 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.411	$0.399 + 0.006 \cdot \text{SL}$	$0.406 + 0.004 \cdot \text{SL}$	$0.420 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.721	$0.709 + 0.006 \cdot \text{SL}$	$0.716 + 0.004 \cdot \text{SL}$	$0.732 + 0.004 \cdot \text{SL}$
H to Y	$t_R$	0.101	$0.088 + 0.006 \cdot \text{SL}$	$0.086 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_F$	0.101	$0.088 + 0.006 \cdot \text{SL}$	$0.090 + 0.006 \cdot \text{SL}$	$0.082 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.412	$0.400 + 0.006 \cdot \text{SL}$	$0.407 + 0.004 \cdot \text{SL}$	$0.421 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.781	$0.769 + 0.006 \cdot \text{SL}$	$0.776 + 0.004 \cdot \text{SL}$	$0.792 + 0.004 \cdot \text{SL}$

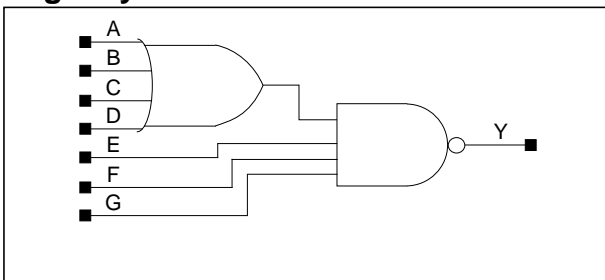
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# OA4111/OA4111D2

## 4-OR into 4-NAND with 1X/2X Drive

### Logic Symbol



### Truth Table

A	B	C	D	E	F	G	Y
0	0	0	0	x	x	x	1
x	x	x	x	0	x	x	1
x	x	x	x	x	0	x	1
x	x	x	x	x	x	0	1
Other States							0

### Cell Data

Input Load (SL)							Gate Count
OA4111							OA4111
A	B	C	D	E	F	G	2.67
0.9	0.9	0.9	0.9	1.0	1.0	0.9	
OA4111D2							OA4111D2
A	B	C	D	E	F	G	3.67
0.9	0.9	0.9	0.9	1.0	1.0	1.0	



## OA4111/OA4111D2

### 4-OR into 4-NAND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OA4111

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.670	$0.434 + 0.118 \cdot \text{SL}$	$0.426 + 0.120 \cdot \text{SL}$	$0.425 + 0.120 \cdot \text{SL}$
	$t_F$	0.531	$0.331 + 0.100 \cdot \text{SL}$	$0.325 + 0.102 \cdot \text{SL}$	$0.326 + 0.102 \cdot \text{SL}$
	$t_{PLH}$	0.266	$0.163 + 0.051 \cdot \text{SL}$	$0.163 + 0.051 \cdot \text{SL}$	$0.163 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.263	$0.171 + 0.046 \cdot \text{SL}$	$0.171 + 0.046 \cdot \text{SL}$	$0.172 + 0.046 \cdot \text{SL}$
B to Y	$t_R$	0.682	$0.447 + 0.117 \cdot \text{SL}$	$0.442 + 0.119 \cdot \text{SL}$	$0.438 + 0.119 \cdot \text{SL}$
	$t_F$	0.602	$0.401 + 0.100 \cdot \text{SL}$	$0.396 + 0.102 \cdot \text{SL}$	$0.398 + 0.101 \cdot \text{SL}$
	$t_{PLH}$	0.310	$0.207 + 0.052 \cdot \text{SL}$	$0.208 + 0.052 \cdot \text{SL}$	$0.210 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.310	$0.218 + 0.046 \cdot \text{SL}$	$0.218 + 0.046 \cdot \text{SL}$	$0.219 + 0.046 \cdot \text{SL}$
C to Y	$t_R$	0.682	$0.448 + 0.117 \cdot \text{SL}$	$0.442 + 0.119 \cdot \text{SL}$	$0.438 + 0.119 \cdot \text{SL}$
	$t_F$	0.676	$0.477 + 0.100 \cdot \text{SL}$	$0.470 + 0.101 \cdot \text{SL}$	$0.471 + 0.101 \cdot \text{SL}$
	$t_{PLH}$	0.340	$0.236 + 0.052 \cdot \text{SL}$	$0.238 + 0.052 \cdot \text{SL}$	$0.240 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.348	$0.254 + 0.047 \cdot \text{SL}$	$0.256 + 0.046 \cdot \text{SL}$	$0.259 + 0.046 \cdot \text{SL}$
D to Y	$t_R$	0.680	$0.445 + 0.118 \cdot \text{SL}$	$0.441 + 0.119 \cdot \text{SL}$	$0.438 + 0.119 \cdot \text{SL}$
	$t_F$	0.752	$0.554 + 0.099 \cdot \text{SL}$	$0.547 + 0.101 \cdot \text{SL}$	$0.548 + 0.101 \cdot \text{SL}$
	$t_{PLH}$	0.353	$0.248 + 0.052 \cdot \text{SL}$	$0.251 + 0.052 \cdot \text{SL}$	$0.254 + 0.051 \cdot \text{SL}$
	$t_{PHL}$	0.376	$0.279 + 0.048 \cdot \text{SL}$	$0.284 + 0.047 \cdot \text{SL}$	$0.290 + 0.046 \cdot \text{SL}$
E to Y	$t_R$	0.248	$0.194 + 0.027 \cdot \text{SL}$	$0.187 + 0.028 \cdot \text{SL}$	$0.179 + 0.029 \cdot \text{SL}$
	$t_F$	0.753	$0.554 + 0.100 \cdot \text{SL}$	$0.552 + 0.100 \cdot \text{SL}$	$0.550 + 0.100 \cdot \text{SL}$
	$t_{PLH}$	0.136	$0.109 + 0.014 \cdot \text{SL}$	$0.110 + 0.013 \cdot \text{SL}$	$0.111 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.434	$0.336 + 0.049 \cdot \text{SL}$	$0.342 + 0.048 \cdot \text{SL}$	$0.350 + 0.047 \cdot \text{SL}$
F to Y	$t_R$	0.262	$0.207 + 0.027 \cdot \text{SL}$	$0.202 + 0.029 \cdot \text{SL}$	$0.192 + 0.030 \cdot \text{SL}$
	$t_F$	0.754	$0.554 + 0.100 \cdot \text{SL}$	$0.552 + 0.100 \cdot \text{SL}$	$0.549 + 0.101 \cdot \text{SL}$
	$t_{PLH}$	0.144	$0.116 + 0.014 \cdot \text{SL}$	$0.117 + 0.014 \cdot \text{SL}$	$0.118 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.440	$0.342 + 0.049 \cdot \text{SL}$	$0.348 + 0.048 \cdot \text{SL}$	$0.356 + 0.047 \cdot \text{SL}$
G to Y	$t_R$	0.347	$0.294 + 0.026 \cdot \text{SL}$	$0.288 + 0.028 \cdot \text{SL}$	$0.275 + 0.029 \cdot \text{SL}$
	$t_F$	0.754	$0.554 + 0.100 \cdot \text{SL}$	$0.552 + 0.100 \cdot \text{SL}$	$0.550 + 0.100 \cdot \text{SL}$
	$t_{PLH}$	0.147	$0.119 + 0.014 \cdot \text{SL}$	$0.120 + 0.014 \cdot \text{SL}$	$0.121 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.438	$0.340 + 0.049 \cdot \text{SL}$	$0.346 + 0.048 \cdot \text{SL}$	$0.354 + 0.047 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**OA4111D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.068 + 0.012 \cdot \text{SL}$	$0.067 + 0.012 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.395	$0.376 + 0.009 \cdot \text{SL}$	$0.384 + 0.007 \cdot \text{SL}$	$0.392 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.407	$0.387 + 0.010 \cdot \text{SL}$	$0.395 + 0.008 \cdot \text{SL}$	$0.407 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.074 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.095	$0.071 + 0.012 \cdot \text{SL}$	$0.070 + 0.012 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.438	$0.420 + 0.009 \cdot \text{SL}$	$0.427 + 0.007 \cdot \text{SL}$	$0.435 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.466	$0.446 + 0.010 \cdot \text{SL}$	$0.454 + 0.008 \cdot \text{SL}$	$0.467 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.103	$0.076 + 0.013 \cdot \text{SL}$	$0.073 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$
	$t_F$	0.099	$0.074 + 0.012 \cdot \text{SL}$	$0.076 + 0.012 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.467	$0.449 + 0.009 \cdot \text{SL}$	$0.456 + 0.007 \cdot \text{SL}$	$0.464 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.514	$0.494 + 0.010 \cdot \text{SL}$	$0.502 + 0.008 \cdot \text{SL}$	$0.515 + 0.007 \cdot \text{SL}$
D to Y	$t_R$	0.102	$0.074 + 0.014 \cdot \text{SL}$	$0.075 + 0.014 \cdot \text{SL}$	$0.060 + 0.015 \cdot \text{SL}$
	$t_F$	0.101	$0.076 + 0.012 \cdot \text{SL}$	$0.077 + 0.012 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.480	$0.462 + 0.009 \cdot \text{SL}$	$0.469 + 0.007 \cdot \text{SL}$	$0.477 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.551	$0.531 + 0.010 \cdot \text{SL}$	$0.540 + 0.008 \cdot \text{SL}$	$0.553 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.088	$0.060 + 0.014 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.101	$0.077 + 0.012 \cdot \text{SL}$	$0.077 + 0.012 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.268	$0.251 + 0.009 \cdot \text{SL}$	$0.257 + 0.007 \cdot \text{SL}$	$0.263 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.610	$0.590 + 0.010 \cdot \text{SL}$	$0.599 + 0.008 \cdot \text{SL}$	$0.611 + 0.007 \cdot \text{SL}$
F to Y	$t_R$	0.088	$0.060 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.102	$0.077 + 0.013 \cdot \text{SL}$	$0.080 + 0.012 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.277	$0.259 + 0.009 \cdot \text{SL}$	$0.265 + 0.007 \cdot \text{SL}$	$0.272 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.616	$0.595 + 0.010 \cdot \text{SL}$	$0.604 + 0.008 \cdot \text{SL}$	$0.617 + 0.007 \cdot \text{SL}$
G to Y	$t_R$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.103	$0.078 + 0.012 \cdot \text{SL}$	$0.080 + 0.012 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.281	$0.264 + 0.009 \cdot \text{SL}$	$0.270 + 0.007 \cdot \text{SL}$	$0.276 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.617	$0.596 + 0.010 \cdot \text{SL}$	$0.606 + 0.008 \cdot \text{SL}$	$0.618 + 0.007 \cdot \text{SL}$

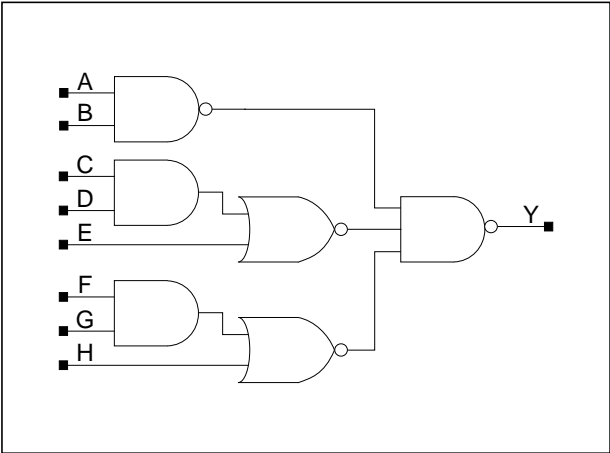
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG1/SCG1D2

2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	1
x	x	1	1	x	x	x	x	1
x	x	x	x	1	x	x	x	1
x	x	x	x	x	1	1	x	1
x	x	x	x	x	x	x	1	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
SCG1								SCG1
A	B	C	D	E	F	G	H	4.00
0.8	0.9	0.8	0.8	0.8	0.8	0.8	0.9	
SCG1D2								SCG1D2
A	B	C	D	E	F	G	H	5.00
0.8	0.9	0.8	0.8	0.8	0.8	0.8	0.8	



## 2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 1X/2X Drive

Switching Characteristics  
SCG1(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.165	$0.089 + 0.038 \cdot \text{SL}$	$0.086 + 0.039 \cdot \text{SL}$	$0.081 + 0.039 \cdot \text{SL}$
	$t_F$	0.194	$0.105 + 0.045 \cdot \text{SL}$	$0.102 + 0.045 \cdot \text{SL}$	$0.099 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.142 + 0.018 \cdot \text{SL}$	$0.146 + 0.017 \cdot \text{SL}$	$0.147 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.187	$0.143 + 0.022 \cdot \text{SL}$	$0.146 + 0.021 \cdot \text{SL}$	$0.146 + 0.021 \cdot \text{SL}$
B to Y	$t_R$	0.165	$0.089 + 0.038 \cdot \text{SL}$	$0.086 + 0.039 \cdot \text{SL}$	$0.081 + 0.039 \cdot \text{SL}$
	$t_F$	0.197	$0.109 + 0.044 \cdot \text{SL}$	$0.105 + 0.045 \cdot \text{SL}$	$0.100 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.174	$0.137 + 0.018 \cdot \text{SL}$	$0.141 + 0.017 \cdot \text{SL}$	$0.143 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.204	$0.160 + 0.022 \cdot \text{SL}$	$0.163 + 0.021 \cdot \text{SL}$	$0.164 + 0.021 \cdot \text{SL}$
C to Y	$t_R$	0.192	$0.121 + 0.036 \cdot \text{SL}$	$0.117 + 0.037 \cdot \text{SL}$	$0.110 + 0.037 \cdot \text{SL}$
	$t_F$	0.208	$0.120 + 0.044 \cdot \text{SL}$	$0.117 + 0.045 \cdot \text{SL}$	$0.112 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.238	$0.202 + 0.018 \cdot \text{SL}$	$0.207 + 0.017 \cdot \text{SL}$	$0.210 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.231	$0.185 + 0.023 \cdot \text{SL}$	$0.190 + 0.022 \cdot \text{SL}$	$0.195 + 0.021 \cdot \text{SL}$
D to Y	$t_R$	0.192	$0.121 + 0.036 \cdot \text{SL}$	$0.117 + 0.037 \cdot \text{SL}$	$0.110 + 0.037 \cdot \text{SL}$
	$t_F$	0.211	$0.124 + 0.044 \cdot \text{SL}$	$0.120 + 0.044 \cdot \text{SL}$	$0.114 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.232	$0.195 + 0.018 \cdot \text{SL}$	$0.201 + 0.017 \cdot \text{SL}$	$0.204 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.245	$0.199 + 0.023 \cdot \text{SL}$	$0.204 + 0.022 \cdot \text{SL}$	$0.209 + 0.021 \cdot \text{SL}$
E to Y	$t_R$	0.185	$0.113 + 0.036 \cdot \text{SL}$	$0.108 + 0.037 \cdot \text{SL}$	$0.102 + 0.038 \cdot \text{SL}$
	$t_F$	0.210	$0.123 + 0.044 \cdot \text{SL}$	$0.120 + 0.044 \cdot \text{SL}$	$0.114 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.231	$0.196 + 0.018 \cdot \text{SL}$	$0.199 + 0.017 \cdot \text{SL}$	$0.201 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.265	$0.219 + 0.023 \cdot \text{SL}$	$0.223 + 0.022 \cdot \text{SL}$	$0.228 + 0.021 \cdot \text{SL}$
F to Y	$t_R$	0.214	$0.141 + 0.036 \cdot \text{SL}$	$0.137 + 0.037 \cdot \text{SL}$	$0.130 + 0.038 \cdot \text{SL}$
	$t_F$	0.203	$0.114 + 0.044 \cdot \text{SL}$	$0.113 + 0.045 \cdot \text{SL}$	$0.108 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.246	$0.209 + 0.018 \cdot \text{SL}$	$0.213 + 0.017 \cdot \text{SL}$	$0.216 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.232	$0.187 + 0.023 \cdot \text{SL}$	$0.191 + 0.022 \cdot \text{SL}$	$0.195 + 0.021 \cdot \text{SL}$
G to Y	$t_R$	0.214	$0.142 + 0.036 \cdot \text{SL}$	$0.137 + 0.037 \cdot \text{SL}$	$0.130 + 0.038 \cdot \text{SL}$
	$t_F$	0.206	$0.118 + 0.044 \cdot \text{SL}$	$0.115 + 0.045 \cdot \text{SL}$	$0.110 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.238	$0.201 + 0.018 \cdot \text{SL}$	$0.206 + 0.017 \cdot \text{SL}$	$0.209 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.244	$0.199 + 0.023 \cdot \text{SL}$	$0.203 + 0.022 \cdot \text{SL}$	$0.207 + 0.021 \cdot \text{SL}$
H to Y	$t_R$	0.207	$0.135 + 0.036 \cdot \text{SL}$	$0.129 + 0.038 \cdot \text{SL}$	$0.122 + 0.038 \cdot \text{SL}$
	$t_F$	0.206	$0.118 + 0.044 \cdot \text{SL}$	$0.115 + 0.045 \cdot \text{SL}$	$0.110 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.240	$0.205 + 0.018 \cdot \text{SL}$	$0.208 + 0.017 \cdot \text{SL}$	$0.209 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.267	$0.221 + 0.023 \cdot \text{SL}$	$0.226 + 0.022 \cdot \text{SL}$	$0.229 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## SCG1/SCG1D2

### 2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 1X/2X Drive

#### Switching Characteristics SCG1D2

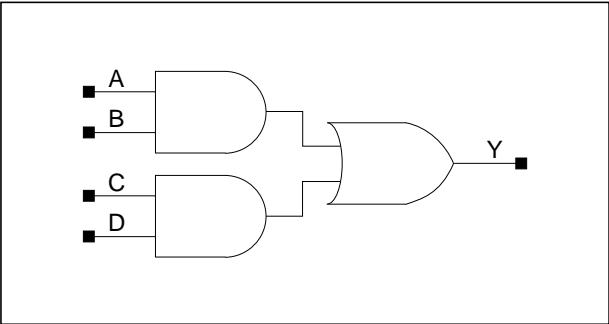
(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.124	$0.088 + 0.018 \cdot \text{SL}$	$0.086 + 0.019 \cdot \text{SL}$	$0.080 + 0.019 \cdot \text{SL}$
	$t_F$	0.143	$0.100 + 0.022 \cdot \text{SL}$	$0.098 + 0.022 \cdot \text{SL}$	$0.093 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.186	$0.165 + 0.010 \cdot \text{SL}$	$0.170 + 0.009 \cdot \text{SL}$	$0.177 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.186	$0.162 + 0.012 \cdot \text{SL}$	$0.166 + 0.011 \cdot \text{SL}$	$0.169 + 0.011 \cdot \text{SL}$
B to Y	$t_R$	0.127	$0.094 + 0.017 \cdot \text{SL}$	$0.085 + 0.019 \cdot \text{SL}$	$0.080 + 0.019 \cdot \text{SL}$
	$t_F$	0.146	$0.101 + 0.022 \cdot \text{SL}$	$0.101 + 0.022 \cdot \text{SL}$	$0.095 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.178	$0.157 + 0.011 \cdot \text{SL}$	$0.163 + 0.009 \cdot \text{SL}$	$0.170 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.198	$0.175 + 0.012 \cdot \text{SL}$	$0.179 + 0.011 \cdot \text{SL}$	$0.182 + 0.011 \cdot \text{SL}$
C to Y	$t_R$	0.165	$0.129 + 0.018 \cdot \text{SL}$	$0.129 + 0.018 \cdot \text{SL}$	$0.119 + 0.019 \cdot \text{SL}$
	$t_F$	0.164	$0.122 + 0.021 \cdot \text{SL}$	$0.119 + 0.022 \cdot \text{SL}$	$0.113 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.237 + 0.011 \cdot \text{SL}$	$0.242 + 0.009 \cdot \text{SL}$	$0.251 + 0.009 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.214 + 0.013 \cdot \text{SL}$	$0.219 + 0.011 \cdot \text{SL}$	$0.227 + 0.011 \cdot \text{SL}$
D to Y	$t_R$	0.166	$0.130 + 0.018 \cdot \text{SL}$	$0.128 + 0.018 \cdot \text{SL}$	$0.119 + 0.019 \cdot \text{SL}$
	$t_F$	0.169	$0.126 + 0.021 \cdot \text{SL}$	$0.124 + 0.022 \cdot \text{SL}$	$0.116 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.250	$0.229 + 0.011 \cdot \text{SL}$	$0.234 + 0.009 \cdot \text{SL}$	$0.244 + 0.009 \cdot \text{SL}$
	$t_{PHL}$	0.251	$0.225 + 0.013 \cdot \text{SL}$	$0.231 + 0.011 \cdot \text{SL}$	$0.239 + 0.011 \cdot \text{SL}$
E to Y	$t_R$	0.151	$0.117 + 0.017 \cdot \text{SL}$	$0.111 + 0.018 \cdot \text{SL}$	$0.102 + 0.019 \cdot \text{SL}$
	$t_F$	0.169	$0.126 + 0.022 \cdot \text{SL}$	$0.125 + 0.022 \cdot \text{SL}$	$0.116 + 0.022 \cdot \text{SL}$
	$t_{PLH}$	0.235	$0.216 + 0.010 \cdot \text{SL}$	$0.220 + 0.009 \cdot \text{SL}$	$0.225 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.270	$0.245 + 0.013 \cdot \text{SL}$	$0.250 + 0.011 \cdot \text{SL}$	$0.259 + 0.011 \cdot \text{SL}$
F to Y	$t_R$	0.188	$0.153 + 0.017 \cdot \text{SL}$	$0.151 + 0.018 \cdot \text{SL}$	$0.140 + 0.019 \cdot \text{SL}$
	$t_F$	0.160	$0.116 + 0.022 \cdot \text{SL}$	$0.116 + 0.022 \cdot \text{SL}$	$0.110 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.268	$0.247 + 0.010 \cdot \text{SL}$	$0.252 + 0.009 \cdot \text{SL}$	$0.260 + 0.009 \cdot \text{SL}$
	$t_{PHL}$	0.241	$0.216 + 0.012 \cdot \text{SL}$	$0.220 + 0.011 \cdot \text{SL}$	$0.228 + 0.011 \cdot \text{SL}$
G to Y	$t_R$	0.188	$0.153 + 0.017 \cdot \text{SL}$	$0.151 + 0.018 \cdot \text{SL}$	$0.141 + 0.019 \cdot \text{SL}$
	$t_F$	0.164	$0.122 + 0.021 \cdot \text{SL}$	$0.118 + 0.022 \cdot \text{SL}$	$0.112 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.261	$0.240 + 0.010 \cdot \text{SL}$	$0.245 + 0.009 \cdot \text{SL}$	$0.253 + 0.009 \cdot \text{SL}$
	$t_{PHL}$	0.252	$0.227 + 0.012 \cdot \text{SL}$	$0.232 + 0.011 \cdot \text{SL}$	$0.240 + 0.011 \cdot \text{SL}$
H to Y	$t_R$	0.172	$0.138 + 0.017 \cdot \text{SL}$	$0.133 + 0.018 \cdot \text{SL}$	$0.123 + 0.019 \cdot \text{SL}$
	$t_F$	0.164	$0.122 + 0.021 \cdot \text{SL}$	$0.119 + 0.022 \cdot \text{SL}$	$0.112 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.244	$0.225 + 0.010 \cdot \text{SL}$	$0.228 + 0.009 \cdot \text{SL}$	$0.233 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.271	$0.246 + 0.013 \cdot \text{SL}$	$0.250 + 0.011 \cdot \text{SL}$	$0.258 + 0.011 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	1
x	x	1	1	1
Other States				0

Cell Data

Input Load (SL)								Gate Count	
SCG2				SCG2D2				SCG2	SCG2D2
A	B	C	D	A	B	C	D		
0.8	0.8	0.9	0.8	0.8	0.8	0.9	0.8	2.00	2.33



## SCG2/SCG2D2

### Two 2-ANDs into 2-OR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.134	$0.076 + 0.029 \cdot \text{SL}$	$0.073 + 0.030 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$
	$t_F$	0.130	$0.077 + 0.027 \cdot \text{SL}$	$0.082 + 0.025 \cdot \text{SL}$	$0.080 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.188	$0.155 + 0.017 \cdot \text{SL}$	$0.164 + 0.014 \cdot \text{SL}$	$0.170 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.221	$0.184 + 0.019 \cdot \text{SL}$	$0.196 + 0.016 \cdot \text{SL}$	$0.208 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.134	$0.076 + 0.029 \cdot \text{SL}$	$0.073 + 0.030 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$
	$t_F$	0.137	$0.086 + 0.026 \cdot \text{SL}$	$0.089 + 0.025 \cdot \text{SL}$	$0.086 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.182	$0.148 + 0.017 \cdot \text{SL}$	$0.157 + 0.015 \cdot \text{SL}$	$0.164 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.201 + 0.019 \cdot \text{SL}$	$0.213 + 0.016 \cdot \text{SL}$	$0.226 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.140	$0.082 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$	$0.074 + 0.030 \cdot \text{SL}$
	$t_F$	0.130	$0.078 + 0.026 \cdot \text{SL}$	$0.082 + 0.025 \cdot \text{SL}$	$0.080 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.236	$0.202 + 0.017 \cdot \text{SL}$	$0.211 + 0.015 \cdot \text{SL}$	$0.218 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.242	$0.205 + 0.018 \cdot \text{SL}$	$0.216 + 0.016 \cdot \text{SL}$	$0.228 + 0.014 \cdot \text{SL}$
D to Y	$t_R$	0.141	$0.083 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$	$0.072 + 0.030 \cdot \text{SL}$
	$t_F$	0.136	$0.084 + 0.026 \cdot \text{SL}$	$0.088 + 0.025 \cdot \text{SL}$	$0.086 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.226	$0.192 + 0.017 \cdot \text{SL}$	$0.202 + 0.014 \cdot \text{SL}$	$0.208 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.259	$0.222 + 0.019 \cdot \text{SL}$	$0.234 + 0.016 \cdot \text{SL}$	$0.246 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

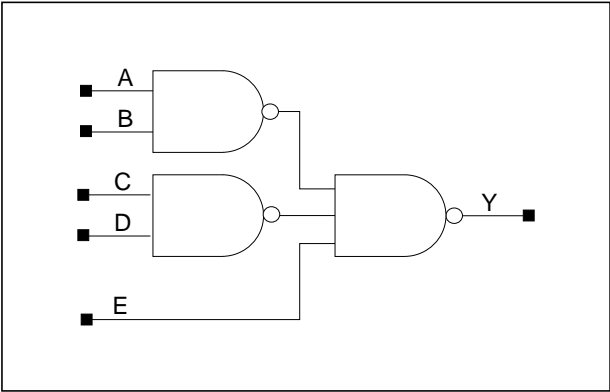
#### SCG2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.110	$0.080 + 0.015 \cdot \text{SL}$	$0.080 + 0.015 \cdot \text{SL}$	$0.077 + 0.015 \cdot \text{SL}$
	$t_F$	0.118	$0.090 + 0.014 \cdot \text{SL}$	$0.095 + 0.013 \cdot \text{SL}$	$0.100 + 0.012 \cdot \text{SL}$
	$t_{PLH}$	0.200	$0.180 + 0.010 \cdot \text{SL}$	$0.188 + 0.008 \cdot \text{SL}$	$0.202 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.237	$0.213 + 0.012 \cdot \text{SL}$	$0.225 + 0.009 \cdot \text{SL}$	$0.245 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.109	$0.079 + 0.015 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$	$0.078 + 0.015 \cdot \text{SL}$
	$t_F$	0.126	$0.098 + 0.014 \cdot \text{SL}$	$0.104 + 0.013 \cdot \text{SL}$	$0.106 + 0.012 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.173 + 0.010 \cdot \text{SL}$	$0.182 + 0.008 \cdot \text{SL}$	$0.196 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.254	$0.229 + 0.012 \cdot \text{SL}$	$0.242 + 0.009 \cdot \text{SL}$	$0.263 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.119	$0.090 + 0.015 \cdot \text{SL}$	$0.091 + 0.014 \cdot \text{SL}$	$0.085 + 0.015 \cdot \text{SL}$
	$t_F$	0.118	$0.091 + 0.014 \cdot \text{SL}$	$0.094 + 0.013 \cdot \text{SL}$	$0.098 + 0.012 \cdot \text{SL}$
	$t_{PLH}$	0.248	$0.226 + 0.011 \cdot \text{SL}$	$0.236 + 0.008 \cdot \text{SL}$	$0.251 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.259	$0.235 + 0.012 \cdot \text{SL}$	$0.246 + 0.009 \cdot \text{SL}$	$0.266 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.120	$0.092 + 0.014 \cdot \text{SL}$	$0.091 + 0.014 \cdot \text{SL}$	$0.084 + 0.015 \cdot \text{SL}$
	$t_F$	0.127	$0.099 + 0.014 \cdot \text{SL}$	$0.104 + 0.013 \cdot \text{SL}$	$0.107 + 0.012 \cdot \text{SL}$
	$t_{PLH}$	0.238	$0.216 + 0.011 \cdot \text{SL}$	$0.226 + 0.008 \cdot \text{SL}$	$0.241 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.275	$0.250 + 0.012 \cdot \text{SL}$	$0.263 + 0.009 \cdot \text{SL}$	$0.284 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	1
x	x	1	1	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)										Gate Count	
SCG3					SCG3D2					SCG3	SCG3D2
A	B	C	D	E	A	B	C	D	E		
0.8	0.9	0.8	0.9	1.0	0.8	0.9	0.8	0.8	2.2	2.67	3.33



## SCG3/SCG3D2

### Two 2-NANDs into 3-NAND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.162	$0.089 + 0.037 \cdot \text{SL}$	$0.085 + 0.038 \cdot \text{SL}$	$0.080 + 0.038 \cdot \text{SL}$
	$t_F$	0.195	$0.107 + 0.044 \cdot \text{SL}$	$0.102 + 0.045 \cdot \text{SL}$	$0.099 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.143 + 0.018 \cdot \text{SL}$	$0.147 + 0.017 \cdot \text{SL}$	$0.149 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.147 + 0.022 \cdot \text{SL}$	$0.150 + 0.021 \cdot \text{SL}$	$0.150 + 0.021 \cdot \text{SL}$
B to Y	$t_R$	0.162	$0.088 + 0.037 \cdot \text{SL}$	$0.085 + 0.038 \cdot \text{SL}$	$0.080 + 0.038 \cdot \text{SL}$
	$t_F$	0.197	$0.109 + 0.044 \cdot \text{SL}$	$0.105 + 0.045 \cdot \text{SL}$	$0.100 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.173	$0.137 + 0.018 \cdot \text{SL}$	$0.142 + 0.017 \cdot \text{SL}$	$0.143 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.205	$0.161 + 0.022 \cdot \text{SL}$	$0.164 + 0.021 \cdot \text{SL}$	$0.165 + 0.021 \cdot \text{SL}$
C to Y	$t_R$	0.183	$0.110 + 0.037 \cdot \text{SL}$	$0.104 + 0.038 \cdot \text{SL}$	$0.099 + 0.039 \cdot \text{SL}$
	$t_F$	0.194	$0.105 + 0.045 \cdot \text{SL}$	$0.102 + 0.045 \cdot \text{SL}$	$0.099 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.190	$0.154 + 0.018 \cdot \text{SL}$	$0.157 + 0.017 \cdot \text{SL}$	$0.159 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.198	$0.153 + 0.022 \cdot \text{SL}$	$0.156 + 0.021 \cdot \text{SL}$	$0.158 + 0.021 \cdot \text{SL}$
D to Y	$t_R$	0.183	$0.110 + 0.037 \cdot \text{SL}$	$0.104 + 0.038 \cdot \text{SL}$	$0.099 + 0.039 \cdot \text{SL}$
	$t_F$	0.195	$0.106 + 0.045 \cdot \text{SL}$	$0.104 + 0.045 \cdot \text{SL}$	$0.100 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.184	$0.149 + 0.018 \cdot \text{SL}$	$0.152 + 0.017 \cdot \text{SL}$	$0.153 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.167 + 0.022 \cdot \text{SL}$	$0.170 + 0.021 \cdot \text{SL}$	$0.171 + 0.021 \cdot \text{SL}$
E to Y	$t_R$	0.220	$0.153 + 0.034 \cdot \text{SL}$	$0.143 + 0.036 \cdot \text{SL}$	$0.128 + 0.038 \cdot \text{SL}$
	$t_F$	0.202	$0.116 + 0.043 \cdot \text{SL}$	$0.110 + 0.045 \cdot \text{SL}$	$0.104 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.134	$0.100 + 0.017 \cdot \text{SL}$	$0.101 + 0.017 \cdot \text{SL}$	$0.101 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.116	$0.071 + 0.022 \cdot \text{SL}$	$0.075 + 0.021 \cdot \text{SL}$	$0.076 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.124	$0.088 + 0.018 \cdot \text{SL}$	$0.086 + 0.019 \cdot \text{SL}$	$0.080 + 0.019 \cdot \text{SL}$
	$t_F$	0.143	$0.099 + 0.022 \cdot \text{SL}$	$0.098 + 0.022 \cdot \text{SL}$	$0.093 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.186	$0.165 + 0.010 \cdot \text{SL}$	$0.170 + 0.009 \cdot \text{SL}$	$0.177 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.185	$0.162 + 0.012 \cdot \text{SL}$	$0.166 + 0.011 \cdot \text{SL}$	$0.169 + 0.011 \cdot \text{SL}$
B to Y	$t_R$	0.127	$0.094 + 0.017 \cdot \text{SL}$	$0.085 + 0.019 \cdot \text{SL}$	$0.080 + 0.019 \cdot \text{SL}$
	$t_F$	0.146	$0.101 + 0.022 \cdot \text{SL}$	$0.102 + 0.022 \cdot \text{SL}$	$0.095 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.178	$0.157 + 0.010 \cdot \text{SL}$	$0.163 + 0.009 \cdot \text{SL}$	$0.169 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.198	$0.175 + 0.012 \cdot \text{SL}$	$0.178 + 0.011 \cdot \text{SL}$	$0.182 + 0.011 \cdot \text{SL}$
C to Y	$t_R$	0.147	$0.111 + 0.018 \cdot \text{SL}$	$0.109 + 0.018 \cdot \text{SL}$	$0.101 + 0.019 \cdot \text{SL}$
	$t_F$	0.144	$0.100 + 0.022 \cdot \text{SL}$	$0.099 + 0.022 \cdot \text{SL}$	$0.094 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.202	$0.182 + 0.010 \cdot \text{SL}$	$0.186 + 0.009 \cdot \text{SL}$	$0.191 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.196	$0.172 + 0.012 \cdot \text{SL}$	$0.176 + 0.011 \cdot \text{SL}$	$0.180 + 0.011 \cdot \text{SL}$
D to Y	$t_R$	0.147	$0.111 + 0.018 \cdot \text{SL}$	$0.109 + 0.018 \cdot \text{SL}$	$0.100 + 0.019 \cdot \text{SL}$
	$t_F$	0.146	$0.102 + 0.022 \cdot \text{SL}$	$0.101 + 0.022 \cdot \text{SL}$	$0.095 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.195	$0.175 + 0.010 \cdot \text{SL}$	$0.179 + 0.009 \cdot \text{SL}$	$0.185 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.207	$0.183 + 0.012 \cdot \text{SL}$	$0.187 + 0.011 \cdot \text{SL}$	$0.192 + 0.011 \cdot \text{SL}$
E to Y	$t_R$	0.177	$0.146 + 0.016 \cdot \text{SL}$	$0.139 + 0.018 \cdot \text{SL}$	$0.122 + 0.019 \cdot \text{SL}$
	$t_F$	0.149	$0.108 + 0.021 \cdot \text{SL}$	$0.102 + 0.022 \cdot \text{SL}$	$0.095 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.110	$0.091 + 0.009 \cdot \text{SL}$	$0.095 + 0.008 \cdot \text{SL}$	$0.096 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.087	$0.063 + 0.012 \cdot \text{SL}$	$0.068 + 0.011 \cdot \text{SL}$	$0.071 + 0.011 \cdot \text{SL}$

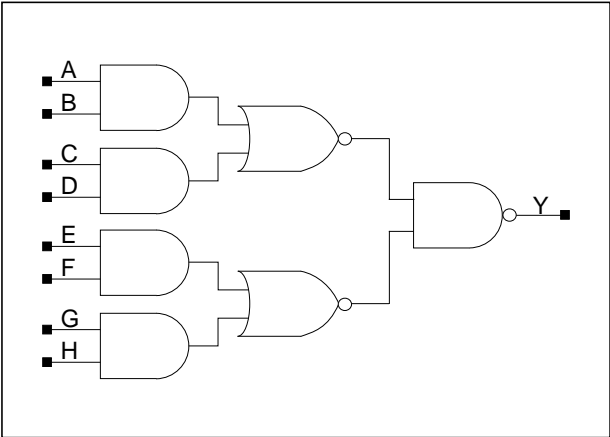
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG4/SCG4D2

Two (two 2-ANDs into 2-NOR)s into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	1
x	x	1	1	x	x	x	x	1
x	x	x	x	1	1	x	x	1
x	x	x	x	x	x	1	1	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
SCG4								SCG4
A	B	C	D	E	F	G	H	3.67
0.8	0.8	0.9	0.8	0.8	0.8	0.8	0.8	
SCG4D2								SCG4D2
A	B	C	D	E	F	G	H	4.67
0.8	0.8	0.8	0.8	0.8	0.8	0.7	0.8	



## Two (two 2-ANDs into 2-NOR)s into 2-NAND with 1X/2X Drive

## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.141	$0.083 + 0.029 \cdot \text{SL}$	$0.082 + 0.029 \cdot \text{SL}$	$0.077 + 0.030 \cdot \text{SL}$
	$t_F$	0.160	$0.098 + 0.031 \cdot \text{SL}$	$0.099 + 0.031 \cdot \text{SL}$	$0.096 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.204	$0.171 + 0.016 \cdot \text{SL}$	$0.180 + 0.014 \cdot \text{SL}$	$0.186 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.236	$0.197 + 0.019 \cdot \text{SL}$	$0.207 + 0.017 \cdot \text{SL}$	$0.217 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.141	$0.082 + 0.029 \cdot \text{SL}$	$0.083 + 0.029 \cdot \text{SL}$	$0.078 + 0.030 \cdot \text{SL}$
	$t_F$	0.164	$0.101 + 0.031 \cdot \text{SL}$	$0.104 + 0.031 \cdot \text{SL}$	$0.101 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.197	$0.164 + 0.017 \cdot \text{SL}$	$0.173 + 0.014 \cdot \text{SL}$	$0.180 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.251	$0.212 + 0.020 \cdot \text{SL}$	$0.222 + 0.017 \cdot \text{SL}$	$0.232 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.149	$0.093 + 0.028 \cdot \text{SL}$	$0.091 + 0.029 \cdot \text{SL}$	$0.083 + 0.030 \cdot \text{SL}$
	$t_F$	0.159	$0.097 + 0.031 \cdot \text{SL}$	$0.099 + 0.031 \cdot \text{SL}$	$0.096 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.254	$0.221 + 0.016 \cdot \text{SL}$	$0.229 + 0.014 \cdot \text{SL}$	$0.237 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.222 + 0.019 \cdot \text{SL}$	$0.232 + 0.017 \cdot \text{SL}$	$0.242 + 0.016 \cdot \text{SL}$
D to Y	$t_R$	0.150	$0.094 + 0.028 \cdot \text{SL}$	$0.092 + 0.029 \cdot \text{SL}$	$0.083 + 0.030 \cdot \text{SL}$
	$t_F$	0.165	$0.103 + 0.031 \cdot \text{SL}$	$0.104 + 0.030 \cdot \text{SL}$	$0.100 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.243	$0.210 + 0.016 \cdot \text{SL}$	$0.219 + 0.014 \cdot \text{SL}$	$0.225 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.273	$0.234 + 0.020 \cdot \text{SL}$	$0.244 + 0.017 \cdot \text{SL}$	$0.254 + 0.016 \cdot \text{SL}$
E to Y	$t_R$	0.157	$0.100 + 0.028 \cdot \text{SL}$	$0.099 + 0.029 \cdot \text{SL}$	$0.092 + 0.030 \cdot \text{SL}$
	$t_F$	0.151	$0.091 + 0.030 \cdot \text{SL}$	$0.089 + 0.031 \cdot \text{SL}$	$0.083 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.211	$0.180 + 0.016 \cdot \text{SL}$	$0.186 + 0.014 \cdot \text{SL}$	$0.191 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.230	$0.193 + 0.018 \cdot \text{SL}$	$0.200 + 0.017 \cdot \text{SL}$	$0.206 + 0.016 \cdot \text{SL}$
F to Y	$t_R$	0.158	$0.102 + 0.028 \cdot \text{SL}$	$0.099 + 0.029 \cdot \text{SL}$	$0.092 + 0.030 \cdot \text{SL}$
	$t_F$	0.156	$0.096 + 0.030 \cdot \text{SL}$	$0.094 + 0.031 \cdot \text{SL}$	$0.088 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.203	$0.171 + 0.016 \cdot \text{SL}$	$0.178 + 0.014 \cdot \text{SL}$	$0.183 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.245	$0.209 + 0.018 \cdot \text{SL}$	$0.216 + 0.017 \cdot \text{SL}$	$0.222 + 0.016 \cdot \text{SL}$
G to Y	$t_R$	0.170	$0.114 + 0.028 \cdot \text{SL}$	$0.112 + 0.028 \cdot \text{SL}$	$0.104 + 0.029 \cdot \text{SL}$
	$t_F$	0.152	$0.091 + 0.030 \cdot \text{SL}$	$0.089 + 0.031 \cdot \text{SL}$	$0.083 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.252	$0.220 + 0.016 \cdot \text{SL}$	$0.227 + 0.014 \cdot \text{SL}$	$0.234 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.253	$0.216 + 0.018 \cdot \text{SL}$	$0.223 + 0.016 \cdot \text{SL}$	$0.229 + 0.016 \cdot \text{SL}$
H to Y	$t_R$	0.170	$0.114 + 0.028 \cdot \text{SL}$	$0.111 + 0.028 \cdot \text{SL}$	$0.104 + 0.029 \cdot \text{SL}$
	$t_F$	0.155	$0.095 + 0.030 \cdot \text{SL}$	$0.093 + 0.031 \cdot \text{SL}$	$0.088 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.246	$0.213 + 0.016 \cdot \text{SL}$	$0.220 + 0.014 \cdot \text{SL}$	$0.227 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.269	$0.233 + 0.018 \cdot \text{SL}$	$0.239 + 0.017 \cdot \text{SL}$	$0.246 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## SCG4/SCG4D2

### Two (two 2-ANDs into 2-NOR)s into 2-NAND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

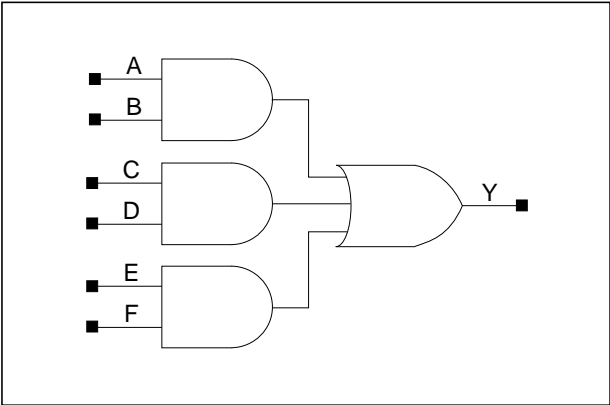
#### SCG4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.122	$0.092 + 0.015 \cdot \text{SL}$	$0.094 + 0.015 \cdot \text{SL}$	$0.089 + 0.015 \cdot \text{SL}$
	$t_F$	0.142	$0.112 + 0.015 \cdot \text{SL}$	$0.110 + 0.016 \cdot \text{SL}$	$0.112 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.220	$0.201 + 0.010 \cdot \text{SL}$	$0.208 + 0.008 \cdot \text{SL}$	$0.221 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.248	$0.225 + 0.012 \cdot \text{SL}$	$0.234 + 0.010 \cdot \text{SL}$	$0.250 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.123	$0.093 + 0.015 \cdot \text{SL}$	$0.093 + 0.015 \cdot \text{SL}$	$0.089 + 0.015 \cdot \text{SL}$
	$t_F$	0.150	$0.119 + 0.015 \cdot \text{SL}$	$0.119 + 0.015 \cdot \text{SL}$	$0.120 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.194 + 0.010 \cdot \text{SL}$	$0.201 + 0.008 \cdot \text{SL}$	$0.214 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.267	$0.243 + 0.012 \cdot \text{SL}$	$0.253 + 0.010 \cdot \text{SL}$	$0.270 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.136	$0.107 + 0.014 \cdot \text{SL}$	$0.108 + 0.014 \cdot \text{SL}$	$0.101 + 0.015 \cdot \text{SL}$
	$t_F$	0.144	$0.114 + 0.015 \cdot \text{SL}$	$0.112 + 0.015 \cdot \text{SL}$	$0.114 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.277	$0.257 + 0.010 \cdot \text{SL}$	$0.265 + 0.008 \cdot \text{SL}$	$0.279 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.286	$0.262 + 0.012 \cdot \text{SL}$	$0.271 + 0.010 \cdot \text{SL}$	$0.288 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.136	$0.107 + 0.014 \cdot \text{SL}$	$0.108 + 0.014 \cdot \text{SL}$	$0.101 + 0.015 \cdot \text{SL}$
	$t_F$	0.150	$0.120 + 0.015 \cdot \text{SL}$	$0.119 + 0.015 \cdot \text{SL}$	$0.119 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.270	$0.250 + 0.010 \cdot \text{SL}$	$0.258 + 0.008 \cdot \text{SL}$	$0.273 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.301	$0.277 + 0.012 \cdot \text{SL}$	$0.287 + 0.010 \cdot \text{SL}$	$0.305 + 0.008 \cdot \text{SL}$
E to Y	$t_R$	0.144	$0.115 + 0.015 \cdot \text{SL}$	$0.116 + 0.014 \cdot \text{SL}$	$0.110 + 0.015 \cdot \text{SL}$
	$t_F$	0.139	$0.110 + 0.014 \cdot \text{SL}$	$0.106 + 0.015 \cdot \text{SL}$	$0.103 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.238	$0.220 + 0.009 \cdot \text{SL}$	$0.225 + 0.008 \cdot \text{SL}$	$0.236 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.251	$0.229 + 0.011 \cdot \text{SL}$	$0.237 + 0.009 \cdot \text{SL}$	$0.249 + 0.008 \cdot \text{SL}$
F to Y	$t_R$	0.144	$0.115 + 0.014 \cdot \text{SL}$	$0.115 + 0.014 \cdot \text{SL}$	$0.109 + 0.015 \cdot \text{SL}$
	$t_F$	0.147	$0.119 + 0.014 \cdot \text{SL}$	$0.116 + 0.015 \cdot \text{SL}$	$0.109 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.232	$0.214 + 0.009 \cdot \text{SL}$	$0.219 + 0.008 \cdot \text{SL}$	$0.230 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.269	$0.246 + 0.011 \cdot \text{SL}$	$0.255 + 0.009 \cdot \text{SL}$	$0.268 + 0.008 \cdot \text{SL}$
G to Y	$t_R$	0.163	$0.134 + 0.014 \cdot \text{SL}$	$0.136 + 0.014 \cdot \text{SL}$	$0.127 + 0.015 \cdot \text{SL}$
	$t_F$	0.141	$0.112 + 0.014 \cdot \text{SL}$	$0.108 + 0.015 \cdot \text{SL}$	$0.104 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.289	$0.270 + 0.009 \cdot \text{SL}$	$0.276 + 0.008 \cdot \text{SL}$	$0.289 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.267 + 0.011 \cdot \text{SL}$	$0.275 + 0.009 \cdot \text{SL}$	$0.286 + 0.008 \cdot \text{SL}$
H to Y	$t_R$	0.163	$0.134 + 0.014 \cdot \text{SL}$	$0.136 + 0.014 \cdot \text{SL}$	$0.128 + 0.015 \cdot \text{SL}$
	$t_F$	0.148	$0.120 + 0.014 \cdot \text{SL}$	$0.116 + 0.015 \cdot \text{SL}$	$0.110 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.283	$0.264 + 0.009 \cdot \text{SL}$	$0.269 + 0.008 \cdot \text{SL}$	$0.282 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.303	$0.280 + 0.011 \cdot \text{SL}$	$0.289 + 0.009 \cdot \text{SL}$	$0.302 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	1
x	x	1	1	x	x	1
x	x	x	x	1	1	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
SCG5						SCG5
A	B	C	D	E	F	3.00
0.7	0.7	0.7	0.8	0.7	0.8	
SCG5D2						SCG5D2
A	B	C	D	E	F	3.33
0.7	0.7	0.7	0.8	0.7	0.8	



## SCG5/SCG5D2

### Three 2-ANDs into 3-OR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.143	$0.083 + 0.030 \cdot \text{SL}$	$0.085 + 0.030 \cdot \text{SL}$	$0.080 + 0.030 \cdot \text{SL}$
	$t_F$	0.173	$0.114 + 0.029 \cdot \text{SL}$	$0.122 + 0.027 \cdot \text{SL}$	$0.129 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.217	$0.181 + 0.018 \cdot \text{SL}$	$0.192 + 0.015 \cdot \text{SL}$	$0.202 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.284	$0.238 + 0.023 \cdot \text{SL}$	$0.255 + 0.019 \cdot \text{SL}$	$0.275 + 0.017 \cdot \text{SL}$
B to Y	$t_R$	0.144	$0.084 + 0.030 \cdot \text{SL}$	$0.087 + 0.029 \cdot \text{SL}$	$0.081 + 0.030 \cdot \text{SL}$
	$t_F$	0.182	$0.125 + 0.029 \cdot \text{SL}$	$0.131 + 0.027 \cdot \text{SL}$	$0.138 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.209	$0.173 + 0.018 \cdot \text{SL}$	$0.184 + 0.015 \cdot \text{SL}$	$0.195 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.302	$0.255 + 0.024 \cdot \text{SL}$	$0.273 + 0.019 \cdot \text{SL}$	$0.294 + 0.017 \cdot \text{SL}$
C to Y	$t_R$	0.158	$0.100 + 0.029 \cdot \text{SL}$	$0.100 + 0.029 \cdot \text{SL}$	$0.094 + 0.030 \cdot \text{SL}$
	$t_F$	0.179	$0.122 + 0.028 \cdot \text{SL}$	$0.127 + 0.027 \cdot \text{SL}$	$0.134 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.285	$0.248 + 0.019 \cdot \text{SL}$	$0.260 + 0.015 \cdot \text{SL}$	$0.272 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.363	$0.317 + 0.023 \cdot \text{SL}$	$0.334 + 0.019 \cdot \text{SL}$	$0.353 + 0.017 \cdot \text{SL}$
D to Y	$t_R$	0.158	$0.101 + 0.029 \cdot \text{SL}$	$0.100 + 0.029 \cdot \text{SL}$	$0.094 + 0.030 \cdot \text{SL}$
	$t_F$	0.187	$0.130 + 0.028 \cdot \text{SL}$	$0.136 + 0.027 \cdot \text{SL}$	$0.142 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.278	$0.241 + 0.019 \cdot \text{SL}$	$0.254 + 0.015 \cdot \text{SL}$	$0.265 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.383	$0.336 + 0.024 \cdot \text{SL}$	$0.354 + 0.019 \cdot \text{SL}$	$0.375 + 0.017 \cdot \text{SL}$
E to Y	$t_R$	0.172	$0.114 + 0.029 \cdot \text{SL}$	$0.115 + 0.029 \cdot \text{SL}$	$0.107 + 0.030 \cdot \text{SL}$
	$t_F$	0.179	$0.122 + 0.028 \cdot \text{SL}$	$0.126 + 0.027 \cdot \text{SL}$	$0.134 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.323	$0.285 + 0.019 \cdot \text{SL}$	$0.299 + 0.016 \cdot \text{SL}$	$0.312 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.394	$0.347 + 0.023 \cdot \text{SL}$	$0.364 + 0.019 \cdot \text{SL}$	$0.384 + 0.016 \cdot \text{SL}$
F to Y	$t_R$	0.172	$0.114 + 0.029 \cdot \text{SL}$	$0.115 + 0.029 \cdot \text{SL}$	$0.107 + 0.030 \cdot \text{SL}$
	$t_F$	0.186	$0.129 + 0.029 \cdot \text{SL}$	$0.136 + 0.027 \cdot \text{SL}$	$0.142 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.318	$0.279 + 0.019 \cdot \text{SL}$	$0.293 + 0.016 \cdot \text{SL}$	$0.306 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.415	$0.368 + 0.024 \cdot \text{SL}$	$0.387 + 0.019 \cdot \text{SL}$	$0.407 + 0.017 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.120	$0.089 + 0.015 \cdot \text{SL}$	$0.091 + 0.015 \cdot \text{SL}$	$0.091 + 0.015 \cdot \text{SL}$
	$t_F$	0.166	$0.133 + 0.017 \cdot \text{SL}$	$0.143 + 0.014 \cdot \text{SL}$	$0.152 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.227	$0.205 + 0.011 \cdot \text{SL}$	$0.215 + 0.009 \cdot \text{SL}$	$0.234 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.307	$0.276 + 0.015 \cdot \text{SL}$	$0.293 + 0.011 \cdot \text{SL}$	$0.322 + 0.009 \cdot \text{SL}$
B to Y	$t_R$	0.120	$0.090 + 0.015 \cdot \text{SL}$	$0.091 + 0.015 \cdot \text{SL}$	$0.090 + 0.015 \cdot \text{SL}$
	$t_F$	0.175	$0.141 + 0.017 \cdot \text{SL}$	$0.153 + 0.014 \cdot \text{SL}$	$0.162 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.220	$0.197 + 0.011 \cdot \text{SL}$	$0.208 + 0.009 \cdot \text{SL}$	$0.226 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.323	$0.292 + 0.016 \cdot \text{SL}$	$0.309 + 0.011 \cdot \text{SL}$	$0.341 + 0.009 \cdot \text{SL}$
C to Y	$t_R$	0.139	$0.109 + 0.015 \cdot \text{SL}$	$0.110 + 0.014 \cdot \text{SL}$	$0.107 + 0.015 \cdot \text{SL}$
	$t_F$	0.170	$0.137 + 0.016 \cdot \text{SL}$	$0.147 + 0.014 \cdot \text{SL}$	$0.155 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.294	$0.270 + 0.012 \cdot \text{SL}$	$0.283 + 0.009 \cdot \text{SL}$	$0.303 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.388	$0.357 + 0.015 \cdot \text{SL}$	$0.374 + 0.011 \cdot \text{SL}$	$0.403 + 0.009 \cdot \text{SL}$
D to Y	$t_R$	0.139	$0.109 + 0.015 \cdot \text{SL}$	$0.110 + 0.014 \cdot \text{SL}$	$0.106 + 0.015 \cdot \text{SL}$
	$t_F$	0.178	$0.144 + 0.017 \cdot \text{SL}$	$0.156 + 0.014 \cdot \text{SL}$	$0.165 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.288	$0.264 + 0.012 \cdot \text{SL}$	$0.277 + 0.009 \cdot \text{SL}$	$0.297 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.406	$0.375 + 0.015 \cdot \text{SL}$	$0.392 + 0.011 \cdot \text{SL}$	$0.424 + 0.009 \cdot \text{SL}$
E to Y	$t_R$	0.151	$0.123 + 0.014 \cdot \text{SL}$	$0.123 + 0.014 \cdot \text{SL}$	$0.121 + 0.015 \cdot \text{SL}$
	$t_F$	0.170	$0.137 + 0.016 \cdot \text{SL}$	$0.146 + 0.014 \cdot \text{SL}$	$0.155 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.334	$0.309 + 0.013 \cdot \text{SL}$	$0.323 + 0.009 \cdot \text{SL}$	$0.345 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.418	$0.388 + 0.015 \cdot \text{SL}$	$0.404 + 0.011 \cdot \text{SL}$	$0.434 + 0.009 \cdot \text{SL}$
F to Y	$t_R$	0.151	$0.123 + 0.014 \cdot \text{SL}$	$0.122 + 0.014 \cdot \text{SL}$	$0.121 + 0.015 \cdot \text{SL}$
	$t_F$	0.178	$0.145 + 0.016 \cdot \text{SL}$	$0.154 + 0.014 \cdot \text{SL}$	$0.164 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.329	$0.303 + 0.013 \cdot \text{SL}$	$0.318 + 0.009 \cdot \text{SL}$	$0.340 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.439	$0.408 + 0.015 \cdot \text{SL}$	$0.425 + 0.011 \cdot \text{SL}$	$0.456 + 0.009 \cdot \text{SL}$

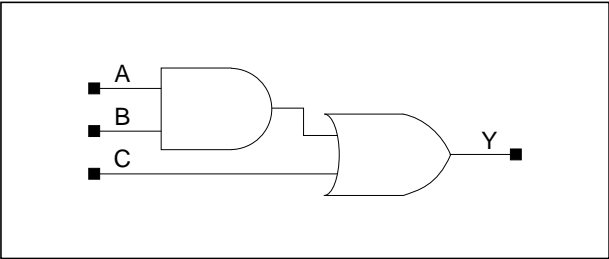
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG6/SCG6D2

2-AND into 2-OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	1
x	x	1	1
Other States			0

Cell Data

Input Load (SL)						Gate Count	
SCG6			SCG6D2			SCG6	SCG6D2
A	B	C	A	B	C	1.67	2.00
0.8	0.8	0.8	0.8	0.8	0.8		



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.128	$0.070 + 0.029 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$	$0.062 + 0.030 \cdot \text{SL}$
	$t_F$	0.123	$0.068 + 0.027 \cdot \text{SL}$	$0.072 + 0.026 \cdot \text{SL}$	$0.069 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.154 + 0.016 \cdot \text{SL}$	$0.162 + 0.014 \cdot \text{SL}$	$0.168 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.154 + 0.019 \cdot \text{SL}$	$0.165 + 0.016 \cdot \text{SL}$	$0.174 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.130	$0.074 + 0.028 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.126	$0.070 + 0.028 \cdot \text{SL}$	$0.076 + 0.026 \cdot \text{SL}$	$0.073 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.146 + 0.016 \cdot \text{SL}$	$0.155 + 0.014 \cdot \text{SL}$	$0.160 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.205	$0.168 + 0.019 \cdot \text{SL}$	$0.179 + 0.016 \cdot \text{SL}$	$0.189 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.120	$0.063 + 0.029 \cdot \text{SL}$	$0.058 + 0.030 \cdot \text{SL}$	$0.051 + 0.031 \cdot \text{SL}$
	$t_F$	0.128	$0.074 + 0.027 \cdot \text{SL}$	$0.077 + 0.026 \cdot \text{SL}$	$0.074 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.191	$0.160 + 0.015 \cdot \text{SL}$	$0.166 + 0.014 \cdot \text{SL}$	$0.168 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.225	$0.188 + 0.019 \cdot \text{SL}$	$0.199 + 0.016 \cdot \text{SL}$	$0.209 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ 

## SCG6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.105	$0.075 + 0.015 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$	$0.072 + 0.015 \cdot \text{SL}$
	$t_F$	0.103	$0.075 + 0.014 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$	$0.081 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.201	$0.181 + 0.010 \cdot \text{SL}$	$0.189 + 0.008 \cdot \text{SL}$	$0.203 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.203	$0.180 + 0.012 \cdot \text{SL}$	$0.190 + 0.009 \cdot \text{SL}$	$0.208 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.104	$0.074 + 0.015 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$
	$t_F$	0.109	$0.080 + 0.014 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$	$0.087 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.193	$0.172 + 0.010 \cdot \text{SL}$	$0.181 + 0.008 \cdot \text{SL}$	$0.195 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.215	$0.192 + 0.012 \cdot \text{SL}$	$0.203 + 0.009 \cdot \text{SL}$	$0.222 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.094	$0.065 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.110	$0.082 + 0.014 \cdot \text{SL}$	$0.084 + 0.013 \cdot \text{SL}$	$0.087 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.176 + 0.009 \cdot \text{SL}$	$0.183 + 0.007 \cdot \text{SL}$	$0.191 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.236	$0.212 + 0.012 \cdot \text{SL}$	$0.223 + 0.009 \cdot \text{SL}$	$0.242 + 0.008 \cdot \text{SL}$

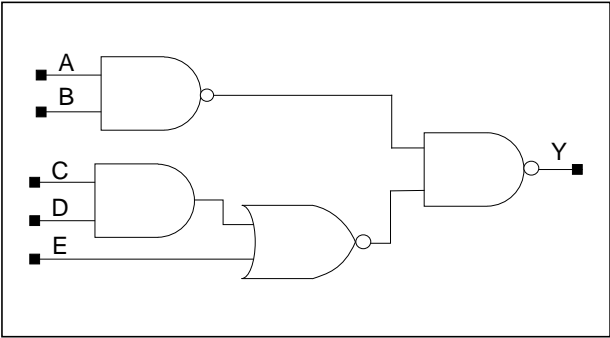
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG7/SCG7D2

2-NAND and (2-AND into 2-NOR) into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	1
x	x	1	1	x	1
x	x	x	x	1	1
Other States					0

Cell Data

Input Load (SL)										Gate Count	
SCG7					SCG7D2					SCG7	SCG7D2
A	B	C	D	E	A	B	C	D	E	3.00	3.33
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8		



## 2-NAND and (2-AND into 2-NOR) into 2-NAND with 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.125	$0.066 + 0.030 \cdot \text{SL}$	$0.064 + 0.030 \cdot \text{SL}$	$0.058 + 0.031 \cdot \text{SL}$
	$t_F$	0.132	$0.069 + 0.031 \cdot \text{SL}$	$0.066 + 0.032 \cdot \text{SL}$	$0.061 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.158	$0.128 + 0.015 \cdot \text{SL}$	$0.133 + 0.014 \cdot \text{SL}$	$0.136 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.167	$0.132 + 0.017 \cdot \text{SL}$	$0.137 + 0.016 \cdot \text{SL}$	$0.139 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.125	$0.067 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$	$0.058 + 0.031 \cdot \text{SL}$
	$t_F$	0.134	$0.072 + 0.031 \cdot \text{SL}$	$0.066 + 0.032 \cdot \text{SL}$	$0.064 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.151	$0.121 + 0.015 \cdot \text{SL}$	$0.127 + 0.014 \cdot \text{SL}$	$0.129 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.180	$0.145 + 0.017 \cdot \text{SL}$	$0.150 + 0.016 \cdot \text{SL}$	$0.152 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.153	$0.094 + 0.029 \cdot \text{SL}$	$0.092 + 0.030 \cdot \text{SL}$	$0.086 + 0.030 \cdot \text{SL}$
	$t_F$	0.141	$0.077 + 0.032 \cdot \text{SL}$	$0.077 + 0.032 \cdot \text{SL}$	$0.072 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.210	$0.179 + 0.016 \cdot \text{SL}$	$0.185 + 0.014 \cdot \text{SL}$	$0.189 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.198	$0.162 + 0.018 \cdot \text{SL}$	$0.168 + 0.017 \cdot \text{SL}$	$0.173 + 0.016 \cdot \text{SL}$
D to Y	$t_R$	0.153	$0.095 + 0.029 \cdot \text{SL}$	$0.092 + 0.029 \cdot \text{SL}$	$0.085 + 0.030 \cdot \text{SL}$
	$t_F$	0.145	$0.083 + 0.031 \cdot \text{SL}$	$0.081 + 0.032 \cdot \text{SL}$	$0.074 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.202	$0.171 + 0.016 \cdot \text{SL}$	$0.177 + 0.014 \cdot \text{SL}$	$0.181 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.175 + 0.018 \cdot \text{SL}$	$0.181 + 0.017 \cdot \text{SL}$	$0.186 + 0.016 \cdot \text{SL}$
E to Y	$t_R$	0.143	$0.087 + 0.028 \cdot \text{SL}$	$0.081 + 0.030 \cdot \text{SL}$	$0.073 + 0.031 \cdot \text{SL}$
	$t_F$	0.146	$0.084 + 0.031 \cdot \text{SL}$	$0.081 + 0.032 \cdot \text{SL}$	$0.074 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.210	$0.181 + 0.015 \cdot \text{SL}$	$0.185 + 0.014 \cdot \text{SL}$	$0.186 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.232	$0.195 + 0.018 \cdot \text{SL}$	$0.201 + 0.017 \cdot \text{SL}$	$0.206 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## SCG7/SCG7D2

### 2-NAND and (2-AND into 2-NOR) into 2-NAND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

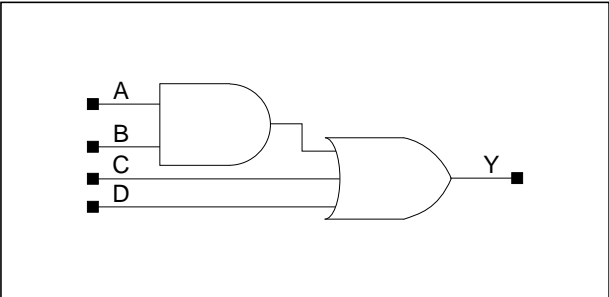
#### SCG7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.103	$0.075 + 0.014 \cdot \text{SL}$	$0.073 + 0.015 \cdot \text{SL}$	$0.069 + 0.015 \cdot \text{SL}$
	$t_F$	0.103	$0.071 + 0.016 \cdot \text{SL}$	$0.071 + 0.016 \cdot \text{SL}$	$0.068 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.174	$0.157 + 0.009 \cdot \text{SL}$	$0.162 + 0.008 \cdot \text{SL}$	$0.171 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.156 + 0.010 \cdot \text{SL}$	$0.162 + 0.009 \cdot \text{SL}$	$0.169 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.104	$0.075 + 0.014 \cdot \text{SL}$	$0.074 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$
	$t_F$	0.107	$0.075 + 0.016 \cdot \text{SL}$	$0.075 + 0.016 \cdot \text{SL}$	$0.070 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.166	$0.149 + 0.009 \cdot \text{SL}$	$0.154 + 0.008 \cdot \text{SL}$	$0.163 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.188	$0.168 + 0.010 \cdot \text{SL}$	$0.174 + 0.009 \cdot \text{SL}$	$0.181 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.144	$0.116 + 0.014 \cdot \text{SL}$	$0.114 + 0.014 \cdot \text{SL}$	$0.108 + 0.015 \cdot \text{SL}$
	$t_F$	0.127	$0.098 + 0.015 \cdot \text{SL}$	$0.095 + 0.016 \cdot \text{SL}$	$0.088 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.244	$0.226 + 0.009 \cdot \text{SL}$	$0.231 + 0.008 \cdot \text{SL}$	$0.242 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.225	$0.203 + 0.011 \cdot \text{SL}$	$0.210 + 0.009 \cdot \text{SL}$	$0.219 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.144	$0.116 + 0.014 \cdot \text{SL}$	$0.114 + 0.014 \cdot \text{SL}$	$0.107 + 0.015 \cdot \text{SL}$
	$t_F$	0.132	$0.103 + 0.014 \cdot \text{SL}$	$0.099 + 0.016 \cdot \text{SL}$	$0.094 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.236	$0.218 + 0.009 \cdot \text{SL}$	$0.223 + 0.008 \cdot \text{SL}$	$0.234 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.236	$0.215 + 0.011 \cdot \text{SL}$	$0.222 + 0.009 \cdot \text{SL}$	$0.232 + 0.008 \cdot \text{SL}$
E to Y	$t_R$	0.126	$0.098 + 0.014 \cdot \text{SL}$	$0.098 + 0.014 \cdot \text{SL}$	$0.084 + 0.015 \cdot \text{SL}$
	$t_F$	0.134	$0.105 + 0.014 \cdot \text{SL}$	$0.101 + 0.015 \cdot \text{SL}$	$0.093 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.227	$0.211 + 0.008 \cdot \text{SL}$	$0.215 + 0.007 \cdot \text{SL}$	$0.221 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.257	$0.236 + 0.011 \cdot \text{SL}$	$0.243 + 0.009 \cdot \text{SL}$	$0.253 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	1
x	x	1	x	1
x	x	x	1	1
Other States				0

Cell Data

Input Load (SL)								Gate Count	
SCG8				SCG8D2				SCG8	SCG8D2
A	B	C	D	A	B	C	D		
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	2.00	2.33



## SCG8/SCG8D2

### 2-AND into 3-OR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.133	$0.074 + 0.030 \cdot \text{SL}$	$0.075 + 0.029 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$
	$t_F$	0.152	$0.094 + 0.029 \cdot \text{SL}$	$0.101 + 0.027 \cdot \text{SL}$	$0.106 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.210	$0.176 + 0.017 \cdot \text{SL}$	$0.185 + 0.015 \cdot \text{SL}$	$0.193 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.195 + 0.022 \cdot \text{SL}$	$0.209 + 0.018 \cdot \text{SL}$	$0.227 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.134	$0.075 + 0.029 \cdot \text{SL}$	$0.075 + 0.029 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$
	$t_F$	0.158	$0.100 + 0.029 \cdot \text{SL}$	$0.107 + 0.027 \cdot \text{SL}$	$0.113 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.203	$0.168 + 0.017 \cdot \text{SL}$	$0.178 + 0.015 \cdot \text{SL}$	$0.186 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.255	$0.211 + 0.022 \cdot \text{SL}$	$0.226 + 0.018 \cdot \text{SL}$	$0.244 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.132	$0.076 + 0.028 \cdot \text{SL}$	$0.072 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.162	$0.104 + 0.029 \cdot \text{SL}$	$0.110 + 0.027 \cdot \text{SL}$	$0.115 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.234	$0.202 + 0.016 \cdot \text{SL}$	$0.210 + 0.014 \cdot \text{SL}$	$0.215 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.310	$0.267 + 0.022 \cdot \text{SL}$	$0.281 + 0.018 \cdot \text{SL}$	$0.299 + 0.016 \cdot \text{SL}$
D to Y	$t_R$	0.139	$0.084 + 0.028 \cdot \text{SL}$	$0.079 + 0.029 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.162	$0.105 + 0.029 \cdot \text{SL}$	$0.111 + 0.027 \cdot \text{SL}$	$0.116 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.251	$0.218 + 0.017 \cdot \text{SL}$	$0.227 + 0.014 \cdot \text{SL}$	$0.233 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.318	$0.274 + 0.022 \cdot \text{SL}$	$0.289 + 0.018 \cdot \text{SL}$	$0.307 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

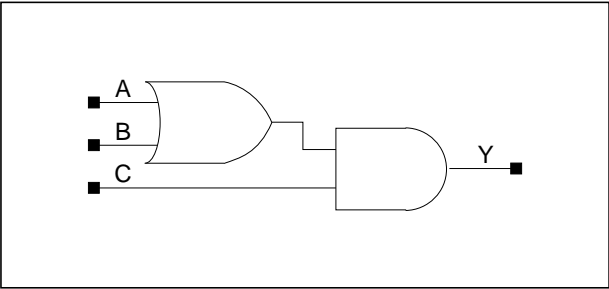
#### SCG8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.113	$0.083 + 0.015 \cdot \text{SL}$	$0.083 + 0.015 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$
	$t_F$	0.142	$0.110 + 0.016 \cdot \text{SL}$	$0.116 + 0.014 \cdot \text{SL}$	$0.127 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.226	$0.204 + 0.011 \cdot \text{SL}$	$0.214 + 0.008 \cdot \text{SL}$	$0.230 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.233 + 0.014 \cdot \text{SL}$	$0.247 + 0.010 \cdot \text{SL}$	$0.273 + 0.009 \cdot \text{SL}$
B to Y	$t_R$	0.112	$0.083 + 0.015 \cdot \text{SL}$	$0.083 + 0.015 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$
	$t_F$	0.150	$0.118 + 0.016 \cdot \text{SL}$	$0.126 + 0.014 \cdot \text{SL}$	$0.134 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.219	$0.197 + 0.011 \cdot \text{SL}$	$0.207 + 0.008 \cdot \text{SL}$	$0.223 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.248 + 0.014 \cdot \text{SL}$	$0.263 + 0.011 \cdot \text{SL}$	$0.289 + 0.009 \cdot \text{SL}$
C to Y	$t_R$	0.109	$0.081 + 0.014 \cdot \text{SL}$	$0.081 + 0.014 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$
	$t_F$	0.152	$0.121 + 0.015 \cdot \text{SL}$	$0.127 + 0.014 \cdot \text{SL}$	$0.136 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.242	$0.222 + 0.010 \cdot \text{SL}$	$0.232 + 0.008 \cdot \text{SL}$	$0.244 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.334	$0.306 + 0.014 \cdot \text{SL}$	$0.321 + 0.011 \cdot \text{SL}$	$0.347 + 0.009 \cdot \text{SL}$
D to Y	$t_R$	0.116	$0.088 + 0.014 \cdot \text{SL}$	$0.088 + 0.014 \cdot \text{SL}$	$0.079 + 0.015 \cdot \text{SL}$
	$t_F$	0.151	$0.120 + 0.016 \cdot \text{SL}$	$0.127 + 0.014 \cdot \text{SL}$	$0.136 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.259	$0.238 + 0.011 \cdot \text{SL}$	$0.248 + 0.008 \cdot \text{SL}$	$0.262 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.342	$0.314 + 0.014 \cdot \text{SL}$	$0.328 + 0.011 \cdot \text{SL}$	$0.355 + 0.009 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	Y
0	0	x	0
x	x	0	0
Other States			1

Cell Data

Input Load (SL)						Gate Count	
SCG9			SCG9D2			SCG9	SCG9D2
A	B	C	A	B	C	2.00	2.33
0.7	0.8	0.8	0.7	0.8	0.8		



## SCG9/SCG9D2

### 2-OR into 2-AND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### SCG9

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.132	$0.072 + 0.030 \cdot \text{SL}$	$0.072 + 0.030 \cdot \text{SL}$	$0.068 + 0.030 \cdot \text{SL}$
	$t_F$	0.125	$0.073 + 0.026 \cdot \text{SL}$	$0.077 + 0.025 \cdot \text{SL}$	$0.076 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.203	$0.170 + 0.017 \cdot \text{SL}$	$0.179 + 0.015 \cdot \text{SL}$	$0.186 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.174 + 0.018 \cdot \text{SL}$	$0.185 + 0.016 \cdot \text{SL}$	$0.197 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.140	$0.082 + 0.029 \cdot \text{SL}$	$0.082 + 0.029 \cdot \text{SL}$	$0.074 + 0.030 \cdot \text{SL}$
	$t_F$	0.126	$0.074 + 0.026 \cdot \text{SL}$	$0.078 + 0.025 \cdot \text{SL}$	$0.076 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.228	$0.194 + 0.017 \cdot \text{SL}$	$0.204 + 0.015 \cdot \text{SL}$	$0.212 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.174 + 0.018 \cdot \text{SL}$	$0.185 + 0.016 \cdot \text{SL}$	$0.197 + 0.014 \cdot \text{SL}$
C to Y	$t_R$	0.139	$0.080 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$	$0.074 + 0.030 \cdot \text{SL}$
	$t_F$	0.115	$0.063 + 0.026 \cdot \text{SL}$	$0.066 + 0.025 \cdot \text{SL}$	$0.062 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.235	$0.200 + 0.017 \cdot \text{SL}$	$0.210 + 0.015 \cdot \text{SL}$	$0.219 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.181	$0.146 + 0.017 \cdot \text{SL}$	$0.156 + 0.015 \cdot \text{SL}$	$0.164 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

##### SCG9D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.108	$0.078 + 0.015 \cdot \text{SL}$	$0.079 + 0.015 \cdot \text{SL}$	$0.078 + 0.015 \cdot \text{SL}$
	$t_F$	0.110	$0.082 + 0.014 \cdot \text{SL}$	$0.084 + 0.014 \cdot \text{SL}$	$0.089 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.193 + 0.011 \cdot \text{SL}$	$0.202 + 0.008 \cdot \text{SL}$	$0.218 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.225	$0.201 + 0.012 \cdot \text{SL}$	$0.212 + 0.009 \cdot \text{SL}$	$0.232 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.117	$0.088 + 0.015 \cdot \text{SL}$	$0.088 + 0.015 \cdot \text{SL}$	$0.086 + 0.015 \cdot \text{SL}$
	$t_F$	0.110	$0.081 + 0.015 \cdot \text{SL}$	$0.085 + 0.014 \cdot \text{SL}$	$0.090 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.238	$0.216 + 0.011 \cdot \text{SL}$	$0.226 + 0.008 \cdot \text{SL}$	$0.243 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.225	$0.201 + 0.012 \cdot \text{SL}$	$0.212 + 0.009 \cdot \text{SL}$	$0.232 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.117	$0.088 + 0.015 \cdot \text{SL}$	$0.089 + 0.015 \cdot \text{SL}$	$0.085 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.245	$0.222 + 0.011 \cdot \text{SL}$	$0.233 + 0.008 \cdot \text{SL}$	$0.250 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.180	$0.158 + 0.011 \cdot \text{SL}$	$0.167 + 0.009 \cdot \text{SL}$	$0.182 + 0.008 \cdot \text{SL}$

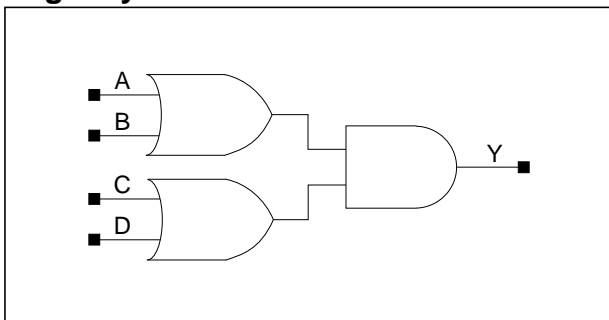
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## SCG10/SCG10D2

### Two 2-ORs into 2-AND with 1X/2X Drive

#### Logic Symbol



#### Truth Table

A	B	C	D	Y
0	0	x	x	0
x	x	0	0	0
Other States				1

#### Cell Data

Input Load (SL)								Gate Count	
SCG10				SCG10D2				SCG10	SCG10D2
A	B	C	D	A	B	C	D		
0.7	0.8	0.7	0.7	0.7	0.8	0.7	0.7	2.33	2.67



## SCG10/SCG10D2

### Two 2-ORs into 2-AND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### SCG10

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.140	$0.081 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$	$0.073 + 0.030 \cdot \text{SL}$
	$t_F$	0.140	$0.084 + 0.028 \cdot \text{SL}$	$0.090 + 0.026 \cdot \text{SL}$	$0.089 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.230	$0.195 + 0.017 \cdot \text{SL}$	$0.205 + 0.015 \cdot \text{SL}$	$0.214 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.214	$0.174 + 0.020 \cdot \text{SL}$	$0.187 + 0.017 \cdot \text{SL}$	$0.201 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.149	$0.091 + 0.029 \cdot \text{SL}$	$0.090 + 0.029 \cdot \text{SL}$	$0.083 + 0.030 \cdot \text{SL}$
	$t_F$	0.140	$0.084 + 0.028 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$	$0.089 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.262	$0.227 + 0.018 \cdot \text{SL}$	$0.238 + 0.015 \cdot \text{SL}$	$0.247 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.217	$0.176 + 0.020 \cdot \text{SL}$	$0.189 + 0.017 \cdot \text{SL}$	$0.204 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.140	$0.082 + 0.029 \cdot \text{SL}$	$0.081 + 0.029 \cdot \text{SL}$	$0.075 + 0.030 \cdot \text{SL}$
	$t_F$	0.150	$0.094 + 0.028 \cdot \text{SL}$	$0.100 + 0.026 \cdot \text{SL}$	$0.100 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.241	$0.207 + 0.017 \cdot \text{SL}$	$0.217 + 0.015 \cdot \text{SL}$	$0.225 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.246	$0.204 + 0.021 \cdot \text{SL}$	$0.218 + 0.017 \cdot \text{SL}$	$0.234 + 0.015 \cdot \text{SL}$
D to Y	$t_R$	0.150	$0.093 + 0.029 \cdot \text{SL}$	$0.092 + 0.029 \cdot \text{SL}$	$0.083 + 0.030 \cdot \text{SL}$
	$t_F$	0.150	$0.094 + 0.028 \cdot \text{SL}$	$0.101 + 0.026 \cdot \text{SL}$	$0.100 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.273	$0.237 + 0.018 \cdot \text{SL}$	$0.249 + 0.015 \cdot \text{SL}$	$0.258 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.247	$0.205 + 0.021 \cdot \text{SL}$	$0.219 + 0.017 \cdot \text{SL}$	$0.235 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

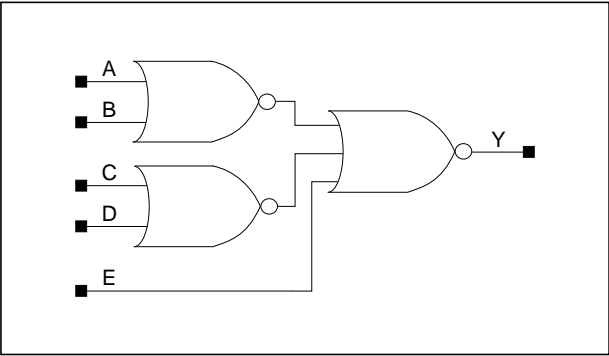
##### SCG10D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.120	$0.091 + 0.015 \cdot \text{SL}$	$0.091 + 0.015 \cdot \text{SL}$	$0.088 + 0.015 \cdot \text{SL}$
	$t_F$	0.122	$0.093 + 0.015 \cdot \text{SL}$	$0.097 + 0.014 \cdot \text{SL}$	$0.101 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.246	$0.224 + 0.011 \cdot \text{SL}$	$0.235 + 0.008 \cdot \text{SL}$	$0.252 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.225	$0.199 + 0.013 \cdot \text{SL}$	$0.212 + 0.010 \cdot \text{SL}$	$0.234 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.131	$0.102 + 0.015 \cdot \text{SL}$	$0.102 + 0.014 \cdot \text{SL}$	$0.099 + 0.015 \cdot \text{SL}$
	$t_F$	0.122	$0.092 + 0.015 \cdot \text{SL}$	$0.097 + 0.014 \cdot \text{SL}$	$0.103 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.278	$0.254 + 0.012 \cdot \text{SL}$	$0.267 + 0.009 \cdot \text{SL}$	$0.285 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.227	$0.202 + 0.013 \cdot \text{SL}$	$0.214 + 0.010 \cdot \text{SL}$	$0.236 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.120	$0.091 + 0.014 \cdot \text{SL}$	$0.090 + 0.015 \cdot \text{SL}$	$0.088 + 0.015 \cdot \text{SL}$
	$t_F$	0.133	$0.103 + 0.015 \cdot \text{SL}$	$0.109 + 0.013 \cdot \text{SL}$	$0.115 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.258	$0.236 + 0.011 \cdot \text{SL}$	$0.247 + 0.008 \cdot \text{SL}$	$0.264 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.254	$0.228 + 0.013 \cdot \text{SL}$	$0.242 + 0.010 \cdot \text{SL}$	$0.265 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.132	$0.103 + 0.014 \cdot \text{SL}$	$0.103 + 0.014 \cdot \text{SL}$	$0.099 + 0.015 \cdot \text{SL}$
	$t_F$	0.134	$0.105 + 0.015 \cdot \text{SL}$	$0.110 + 0.013 \cdot \text{SL}$	$0.114 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.288	$0.265 + 0.012 \cdot \text{SL}$	$0.278 + 0.009 \cdot \text{SL}$	$0.296 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.256	$0.229 + 0.013 \cdot \text{SL}$	$0.243 + 0.010 \cdot \text{SL}$	$0.266 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	0
x	x	0	0	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)										Gate Count	
SCG11					SCG11D2					SCG11	SCG11D2
A	B	C	D	E	A	B	C	D	E	2.67	3.67
0.8	0.8	0.8	0.8	1.0	0.8	0.8	0.8	0.8	2.0		



## SCG11/SCG11D2

### Two 2-NORs into 3-NOR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.342	$0.164 + 0.089 \cdot \text{SL}$	$0.162 + 0.089 \cdot \text{SL}$	$0.163 + 0.089 \cdot \text{SL}$
	$t_F$	0.150	$0.083 + 0.034 \cdot \text{SL}$	$0.082 + 0.034 \cdot \text{SL}$	$0.078 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.137 + 0.038 \cdot \text{SL}$	$0.137 + 0.038 \cdot \text{SL}$	$0.138 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.223	$0.180 + 0.022 \cdot \text{SL}$	$0.190 + 0.019 \cdot \text{SL}$	$0.197 + 0.018 \cdot \text{SL}$
B to Y	$t_R$	0.343	$0.166 + 0.089 \cdot \text{SL}$	$0.163 + 0.089 \cdot \text{SL}$	$0.163 + 0.089 \cdot \text{SL}$
	$t_F$	0.149	$0.081 + 0.034 \cdot \text{SL}$	$0.082 + 0.034 \cdot \text{SL}$	$0.078 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.231	$0.154 + 0.038 \cdot \text{SL}$	$0.154 + 0.038 \cdot \text{SL}$	$0.155 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.222	$0.178 + 0.022 \cdot \text{SL}$	$0.188 + 0.019 \cdot \text{SL}$	$0.196 + 0.018 \cdot \text{SL}$
C to Y	$t_R$	0.348	$0.173 + 0.088 \cdot \text{SL}$	$0.169 + 0.089 \cdot \text{SL}$	$0.166 + 0.089 \cdot \text{SL}$
	$t_F$	0.177	$0.111 + 0.033 \cdot \text{SL}$	$0.108 + 0.033 \cdot \text{SL}$	$0.102 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.245	$0.167 + 0.039 \cdot \text{SL}$	$0.168 + 0.039 \cdot \text{SL}$	$0.170 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.239	$0.197 + 0.021 \cdot \text{SL}$	$0.205 + 0.019 \cdot \text{SL}$	$0.211 + 0.018 \cdot \text{SL}$
D to Y	$t_R$	0.349	$0.174 + 0.088 \cdot \text{SL}$	$0.170 + 0.089 \cdot \text{SL}$	$0.167 + 0.089 \cdot \text{SL}$
	$t_F$	0.177	$0.111 + 0.033 \cdot \text{SL}$	$0.109 + 0.033 \cdot \text{SL}$	$0.102 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.260	$0.182 + 0.039 \cdot \text{SL}$	$0.184 + 0.039 \cdot \text{SL}$	$0.186 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.237	$0.195 + 0.021 \cdot \text{SL}$	$0.203 + 0.019 \cdot \text{SL}$	$0.209 + 0.018 \cdot \text{SL}$
E to Y	$t_R$	0.354	$0.181 + 0.087 \cdot \text{SL}$	$0.175 + 0.088 \cdot \text{SL}$	$0.168 + 0.089 \cdot \text{SL}$
	$t_F$	0.202	$0.141 + 0.030 \cdot \text{SL}$	$0.133 + 0.032 \cdot \text{SL}$	$0.120 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.193	$0.115 + 0.039 \cdot \text{SL}$	$0.116 + 0.038 \cdot \text{SL}$	$0.117 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.134	$0.095 + 0.019 \cdot \text{SL}$	$0.098 + 0.019 \cdot \text{SL}$	$0.100 + 0.018 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG11D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.235	$0.148 + 0.044 \cdot \text{SL}$	$0.144 + 0.044 \cdot \text{SL}$	$0.142 + 0.045 \cdot \text{SL}$
	$t_F$	0.124	$0.088 + 0.018 \cdot \text{SL}$	$0.093 + 0.017 \cdot \text{SL}$	$0.090 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.188	$0.150 + 0.019 \cdot \text{SL}$	$0.149 + 0.019 \cdot \text{SL}$	$0.150 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.232	$0.206 + 0.013 \cdot \text{SL}$	$0.215 + 0.011 \cdot \text{SL}$	$0.232 + 0.009 \cdot \text{SL}$
B to Y	$t_R$	0.237	$0.150 + 0.044 \cdot \text{SL}$	$0.147 + 0.044 \cdot \text{SL}$	$0.143 + 0.045 \cdot \text{SL}$
	$t_F$	0.125	$0.089 + 0.018 \cdot \text{SL}$	$0.094 + 0.017 \cdot \text{SL}$	$0.091 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.204	$0.166 + 0.019 \cdot \text{SL}$	$0.165 + 0.019 \cdot \text{SL}$	$0.165 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.230	$0.204 + 0.013 \cdot \text{SL}$	$0.214 + 0.011 \cdot \text{SL}$	$0.231 + 0.009 \cdot \text{SL}$
C to Y	$t_R$	0.245	$0.159 + 0.043 \cdot \text{SL}$	$0.155 + 0.044 \cdot \text{SL}$	$0.148 + 0.045 \cdot \text{SL}$
	$t_F$	0.156	$0.123 + 0.017 \cdot \text{SL}$	$0.124 + 0.016 \cdot \text{SL}$	$0.119 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.220	$0.180 + 0.020 \cdot \text{SL}$	$0.183 + 0.019 \cdot \text{SL}$	$0.186 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.255	$0.230 + 0.012 \cdot \text{SL}$	$0.238 + 0.010 \cdot \text{SL}$	$0.252 + 0.009 \cdot \text{SL}$
D to Y	$t_R$	0.246	$0.161 + 0.043 \cdot \text{SL}$	$0.156 + 0.044 \cdot \text{SL}$	$0.149 + 0.044 \cdot \text{SL}$
	$t_F$	0.156	$0.123 + 0.017 \cdot \text{SL}$	$0.123 + 0.016 \cdot \text{SL}$	$0.119 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.234	$0.193 + 0.020 \cdot \text{SL}$	$0.197 + 0.019 \cdot \text{SL}$	$0.199 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.253	$0.228 + 0.012 \cdot \text{SL}$	$0.236 + 0.010 \cdot \text{SL}$	$0.250 + 0.009 \cdot \text{SL}$
E to Y	$t_R$	0.251	$0.167 + 0.042 \cdot \text{SL}$	$0.160 + 0.044 \cdot \text{SL}$	$0.151 + 0.044 \cdot \text{SL}$
	$t_F$	0.167	$0.138 + 0.014 \cdot \text{SL}$	$0.133 + 0.016 \cdot \text{SL}$	$0.117 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.146	$0.106 + 0.020 \cdot \text{SL}$	$0.109 + 0.019 \cdot \text{SL}$	$0.111 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.108	$0.087 + 0.011 \cdot \text{SL}$	$0.092 + 0.009 \cdot \text{SL}$	$0.095 + 0.009 \cdot \text{SL}$

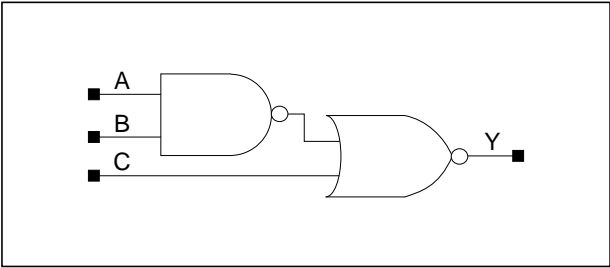
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG12/SCG12D2

2-NAND into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	0	1
Other States			0

Cell Data

Input Load (SL)						Gate Count	
SCG12			SCG12D2			SCG12	SCG12D2
A	B	C	A	B	C	1.67	2.33
0.8	0.9	1.0	0.8	0.9	2.1		



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**SCG12**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.219	$0.101 + 0.059 \cdot \text{SL}$	$0.096 + 0.060 \cdot \text{SL}$	$0.091 + 0.061 \cdot \text{SL}$
	$t_F$	0.106	$0.053 + 0.027 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$	$0.046 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.186	$0.132 + 0.027 \cdot \text{SL}$	$0.135 + 0.026 \cdot \text{SL}$	$0.136 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.162	$0.129 + 0.016 \cdot \text{SL}$	$0.136 + 0.015 \cdot \text{SL}$	$0.138 + 0.014 \cdot \text{SL}$
B to Y	$t_R$	0.219	$0.101 + 0.059 \cdot \text{SL}$	$0.096 + 0.060 \cdot \text{SL}$	$0.091 + 0.061 \cdot \text{SL}$
	$t_F$	0.108	$0.056 + 0.026 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.049 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.181	$0.127 + 0.027 \cdot \text{SL}$	$0.130 + 0.026 \cdot \text{SL}$	$0.131 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.143 + 0.017 \cdot \text{SL}$	$0.149 + 0.015 \cdot \text{SL}$	$0.153 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.229	$0.115 + 0.057 \cdot \text{SL}$	$0.104 + 0.060 \cdot \text{SL}$	$0.096 + 0.061 \cdot \text{SL}$
	$t_F$	0.153	$0.108 + 0.022 \cdot \text{SL}$	$0.099 + 0.025 \cdot \text{SL}$	$0.082 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.127	$0.073 + 0.027 \cdot \text{SL}$	$0.077 + 0.026 \cdot \text{SL}$	$0.076 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.100	$0.067 + 0.017 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ **SCG12D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.155	$0.096 + 0.029 \cdot \text{SL}$	$0.094 + 0.030 \cdot \text{SL}$	$0.087 + 0.030 \cdot \text{SL}$
	$t_F$	0.083	$0.057 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.055 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.182	$0.153 + 0.014 \cdot \text{SL}$	$0.158 + 0.013 \cdot \text{SL}$	$0.160 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.167	$0.147 + 0.010 \cdot \text{SL}$	$0.154 + 0.008 \cdot \text{SL}$	$0.164 + 0.007 \cdot \text{SL}$
B to Y	$t_R$	0.155	$0.097 + 0.029 \cdot \text{SL}$	$0.095 + 0.030 \cdot \text{SL}$	$0.087 + 0.030 \cdot \text{SL}$
	$t_F$	0.087	$0.060 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.175	$0.146 + 0.015 \cdot \text{SL}$	$0.151 + 0.013 \cdot \text{SL}$	$0.154 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.180	$0.160 + 0.010 \cdot \text{SL}$	$0.167 + 0.008 \cdot \text{SL}$	$0.177 + 0.007 \cdot \text{SL}$
C to Y	$t_R$	0.163	$0.109 + 0.027 \cdot \text{SL}$	$0.099 + 0.030 \cdot \text{SL}$	$0.090 + 0.030 \cdot \text{SL}$
	$t_F$	0.126	$0.104 + 0.011 \cdot \text{SL}$	$0.100 + 0.012 \cdot \text{SL}$	$0.082 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.095	$0.065 + 0.015 \cdot \text{SL}$	$0.072 + 0.013 \cdot \text{SL}$	$0.074 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.077	$0.057 + 0.010 \cdot \text{SL}$	$0.067 + 0.008 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$

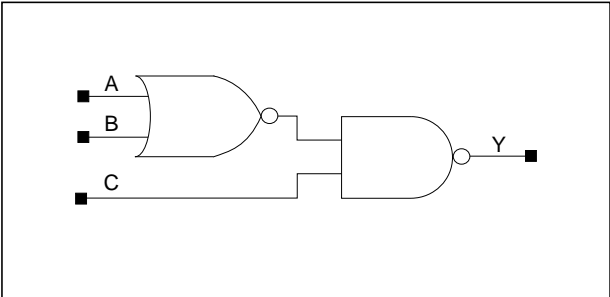
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG13/SCG13D2

2-NOR into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	1	0
Other States			1

Cell Data

Input Load (SL)						Gate Count	
SCG13			SCG13D2			SCG13	SCG13D2
A	B	C	A	B	C	1.67	2.33
0.8	0.8	1.1	0.8	0.8	2.4		



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.121	$0.062 + 0.030 \cdot \text{SL}$	$0.059 + 0.030 \cdot \text{SL}$	$0.054 + 0.031 \cdot \text{SL}$
	$t_F$	0.151	$0.086 + 0.032 \cdot \text{SL}$	$0.087 + 0.032 \cdot \text{SL}$	$0.083 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.148	$0.119 + 0.014 \cdot \text{SL}$	$0.122 + 0.014 \cdot \text{SL}$	$0.123 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.210	$0.172 + 0.019 \cdot \text{SL}$	$0.181 + 0.017 \cdot \text{SL}$	$0.188 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.124	$0.066 + 0.029 \cdot \text{SL}$	$0.060 + 0.030 \cdot \text{SL}$	$0.056 + 0.031 \cdot \text{SL}$
	$t_F$	0.151	$0.085 + 0.033 \cdot \text{SL}$	$0.089 + 0.032 \cdot \text{SL}$	$0.084 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.165	$0.136 + 0.014 \cdot \text{SL}$	$0.139 + 0.014 \cdot \text{SL}$	$0.140 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.209	$0.171 + 0.019 \cdot \text{SL}$	$0.180 + 0.017 \cdot \text{SL}$	$0.187 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.164	$0.112 + 0.026 \cdot \text{SL}$	$0.102 + 0.028 \cdot \text{SL}$	$0.090 + 0.030 \cdot \text{SL}$
	$t_F$	0.149	$0.089 + 0.030 \cdot \text{SL}$	$0.081 + 0.032 \cdot \text{SL}$	$0.073 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.101	$0.071 + 0.015 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.087	$0.051 + 0.018 \cdot \text{SL}$	$0.059 + 0.016 \cdot \text{SL}$	$0.060 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ 

## SCG13D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.095	$0.067 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.131	$0.098 + 0.016 \cdot \text{SL}$	$0.099 + 0.016 \cdot \text{SL}$	$0.098 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.158	$0.142 + 0.008 \cdot \text{SL}$	$0.146 + 0.007 \cdot \text{SL}$	$0.150 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.228	$0.205 + 0.011 \cdot \text{SL}$	$0.213 + 0.009 \cdot \text{SL}$	$0.227 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.098	$0.071 + 0.014 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.130	$0.097 + 0.016 \cdot \text{SL}$	$0.098 + 0.016 \cdot \text{SL}$	$0.098 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.173	$0.157 + 0.008 \cdot \text{SL}$	$0.161 + 0.007 \cdot \text{SL}$	$0.166 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.228	$0.205 + 0.011 \cdot \text{SL}$	$0.212 + 0.009 \cdot \text{SL}$	$0.226 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.135	$0.111 + 0.012 \cdot \text{SL}$	$0.105 + 0.013 \cdot \text{SL}$	$0.090 + 0.015 \cdot \text{SL}$
	$t_F$	0.114	$0.083 + 0.015 \cdot \text{SL}$	$0.082 + 0.016 \cdot \text{SL}$	$0.072 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.081	$0.063 + 0.009 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.075 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.066	$0.045 + 0.010 \cdot \text{SL}$	$0.052 + 0.009 \cdot \text{SL}$	$0.059 + 0.008 \cdot \text{SL}$

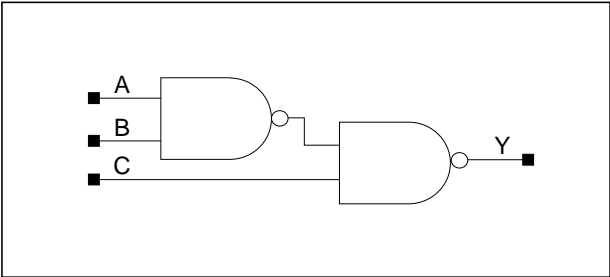
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG14/SCG14D2

2-NAND into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	1	0
x	0	1	0
Other States			1

Cell Data

Input Load (SL)						Gate Count	
SCG14			SCG14D2			SCG14	SCG14D2
A	B	C	A	B	C	1.67	2.33
0.8	0.9	1.2	0.8	0.9	2.4		



**Switching Characteristics**(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)**SCG14**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.129	$0.070 + 0.029 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$	$0.061 + 0.031 \cdot \text{SL}$
	$t_F$	0.134	$0.069 + 0.032 \cdot \text{SL}$	$0.068 + 0.032 \cdot \text{SL}$	$0.064 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.161	$0.130 + 0.015 \cdot \text{SL}$	$0.136 + 0.014 \cdot \text{SL}$	$0.139 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.170	$0.135 + 0.017 \cdot \text{SL}$	$0.140 + 0.016 \cdot \text{SL}$	$0.142 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.129	$0.070 + 0.029 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$	$0.061 + 0.031 \cdot \text{SL}$
	$t_F$	0.136	$0.073 + 0.032 \cdot \text{SL}$	$0.070 + 0.032 \cdot \text{SL}$	$0.066 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.155	$0.124 + 0.015 \cdot \text{SL}$	$0.130 + 0.014 \cdot \text{SL}$	$0.133 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.184	$0.149 + 0.017 \cdot \text{SL}$	$0.154 + 0.016 \cdot \text{SL}$	$0.156 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.164	$0.113 + 0.026 \cdot \text{SL}$	$0.101 + 0.029 \cdot \text{SL}$	$0.089 + 0.030 \cdot \text{SL}$
	$t_F$	0.148	$0.089 + 0.029 \cdot \text{SL}$	$0.080 + 0.031 \cdot \text{SL}$	$0.070 + 0.033 \cdot \text{SL}$
	$t_{PLH}$	0.102	$0.071 + 0.015 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.086	$0.051 + 0.018 \cdot \text{SL}$	$0.058 + 0.016 \cdot \text{SL}$	$0.059 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ **SCG14D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.105	$0.078 + 0.014 \cdot \text{SL}$	$0.073 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$
	$t_F$	0.105	$0.072 + 0.016 \cdot \text{SL}$	$0.073 + 0.016 \cdot \text{SL}$	$0.069 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.173	$0.156 + 0.009 \cdot \text{SL}$	$0.161 + 0.008 \cdot \text{SL}$	$0.170 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.156 + 0.010 \cdot \text{SL}$	$0.162 + 0.009 \cdot \text{SL}$	$0.169 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.106	$0.077 + 0.014 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$
	$t_F$	0.108	$0.076 + 0.016 \cdot \text{SL}$	$0.076 + 0.016 \cdot \text{SL}$	$0.071 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.166	$0.149 + 0.009 \cdot \text{SL}$	$0.154 + 0.008 \cdot \text{SL}$	$0.163 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.189	$0.169 + 0.010 \cdot \text{SL}$	$0.175 + 0.009 \cdot \text{SL}$	$0.182 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.135	$0.110 + 0.012 \cdot \text{SL}$	$0.105 + 0.013 \cdot \text{SL}$	$0.089 + 0.015 \cdot \text{SL}$
	$t_F$	0.114	$0.085 + 0.014 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$	$0.069 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.082	$0.064 + 0.009 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.065	$0.045 + 0.010 \cdot \text{SL}$	$0.052 + 0.008 \cdot \text{SL}$	$0.058 + 0.008 \cdot \text{SL}$

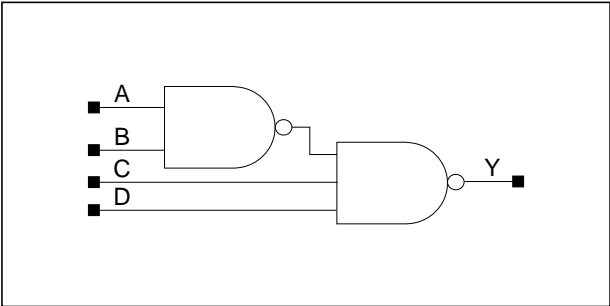
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG15/SCG15D2

2-NAND into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	1	1	0
x	0	1	1	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
SCG15				SCG15D2				SCG15	SCG15D2
A	B	C	D	A	B	C	D		
0.8	0.9	1.0	1.0	0.8	0.8	2.1	2.3	2.00	3.00



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG15

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.166	$0.092 + 0.037 \cdot \text{SL}$	$0.088 + 0.038 \cdot \text{SL}$	$0.083 + 0.039 \cdot \text{SL}$
	$t_F$	0.197	$0.109 + 0.044 \cdot \text{SL}$	$0.105 + 0.045 \cdot \text{SL}$	$0.100 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.182	$0.145 + 0.018 \cdot \text{SL}$	$0.149 + 0.017 \cdot \text{SL}$	$0.151 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.194	$0.150 + 0.022 \cdot \text{SL}$	$0.153 + 0.021 \cdot \text{SL}$	$0.153 + 0.021 \cdot \text{SL}$
B to Y	$t_R$	0.165	$0.090 + 0.038 \cdot \text{SL}$	$0.088 + 0.038 \cdot \text{SL}$	$0.083 + 0.039 \cdot \text{SL}$
	$t_F$	0.199	$0.111 + 0.044 \cdot \text{SL}$	$0.107 + 0.045 \cdot \text{SL}$	$0.102 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.176	$0.139 + 0.018 \cdot \text{SL}$	$0.144 + 0.017 \cdot \text{SL}$	$0.145 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.208	$0.164 + 0.022 \cdot \text{SL}$	$0.167 + 0.021 \cdot \text{SL}$	$0.167 + 0.021 \cdot \text{SL}$
C to Y	$t_R$	0.201	$0.133 + 0.034 \cdot \text{SL}$	$0.123 + 0.036 \cdot \text{SL}$	$0.109 + 0.038 \cdot \text{SL}$
	$t_F$	0.209	$0.125 + 0.042 \cdot \text{SL}$	$0.116 + 0.044 \cdot \text{SL}$	$0.108 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.125	$0.090 + 0.017 \cdot \text{SL}$	$0.093 + 0.017 \cdot \text{SL}$	$0.092 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.119	$0.074 + 0.022 \cdot \text{SL}$	$0.079 + 0.021 \cdot \text{SL}$	$0.079 + 0.021 \cdot \text{SL}$
D to Y	$t_R$	0.221	$0.153 + 0.034 \cdot \text{SL}$	$0.144 + 0.036 \cdot \text{SL}$	$0.129 + 0.038 \cdot \text{SL}$
	$t_F$	0.203	$0.117 + 0.043 \cdot \text{SL}$	$0.110 + 0.045 \cdot \text{SL}$	$0.105 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.135	$0.101 + 0.017 \cdot \text{SL}$	$0.103 + 0.017 \cdot \text{SL}$	$0.102 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.117	$0.073 + 0.022 \cdot \text{SL}$	$0.076 + 0.021 \cdot \text{SL}$	$0.076 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ 

## SCG15D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.126	$0.090 + 0.018 \cdot \text{SL}$	$0.088 + 0.019 \cdot \text{SL}$	$0.082 + 0.019 \cdot \text{SL}$
	$t_F$	0.146	$0.102 + 0.022 \cdot \text{SL}$	$0.100 + 0.022 \cdot \text{SL}$	$0.095 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.187	$0.167 + 0.010 \cdot \text{SL}$	$0.171 + 0.009 \cdot \text{SL}$	$0.178 + 0.009 \cdot \text{SL}$
	$t_{PHL}$	0.187	$0.163 + 0.012 \cdot \text{SL}$	$0.167 + 0.011 \cdot \text{SL}$	$0.171 + 0.011 \cdot \text{SL}$
B to Y	$t_R$	0.129	$0.096 + 0.017 \cdot \text{SL}$	$0.087 + 0.019 \cdot \text{SL}$	$0.082 + 0.019 \cdot \text{SL}$
	$t_F$	0.148	$0.104 + 0.022 \cdot \text{SL}$	$0.104 + 0.022 \cdot \text{SL}$	$0.098 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.179	$0.158 + 0.011 \cdot \text{SL}$	$0.165 + 0.009 \cdot \text{SL}$	$0.171 + 0.009 \cdot \text{SL}$
	$t_{PHL}$	0.200	$0.177 + 0.012 \cdot \text{SL}$	$0.181 + 0.011 \cdot \text{SL}$	$0.185 + 0.011 \cdot \text{SL}$
C to Y	$t_R$	0.157	$0.126 + 0.015 \cdot \text{SL}$	$0.117 + 0.018 \cdot \text{SL}$	$0.103 + 0.019 \cdot \text{SL}$
	$t_F$	0.157	$0.118 + 0.020 \cdot \text{SL}$	$0.111 + 0.022 \cdot \text{SL}$	$0.098 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.101	$0.081 + 0.010 \cdot \text{SL}$	$0.087 + 0.008 \cdot \text{SL}$	$0.087 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.088	$0.064 + 0.012 \cdot \text{SL}$	$0.070 + 0.011 \cdot \text{SL}$	$0.073 + 0.011 \cdot \text{SL}$
D to Y	$t_R$	0.178	$0.146 + 0.016 \cdot \text{SL}$	$0.139 + 0.018 \cdot \text{SL}$	$0.123 + 0.019 \cdot \text{SL}$
	$t_F$	0.149	$0.107 + 0.021 \cdot \text{SL}$	$0.101 + 0.022 \cdot \text{SL}$	$0.095 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.113	$0.094 + 0.009 \cdot \text{SL}$	$0.098 + 0.008 \cdot \text{SL}$	$0.098 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.088	$0.064 + 0.012 \cdot \text{SL}$	$0.069 + 0.011 \cdot \text{SL}$	$0.072 + 0.011 \cdot \text{SL}$

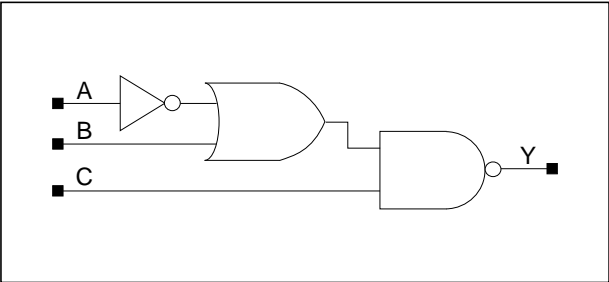
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG16/SCG16D2

2-OR with one inverted input into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	1	0
x	1	1	0
Other States			1

Cell Data

Input Load (SL)						Gate Count	
SCG16			SCG16D2			SCG16	SCG16D2
A	B	C	A	B	C	2.00	3.00
0.8	1.0	1.0	0.8	2.0	2.1		



## 2-OR with one inverted input into 2-NAND with 1X/2X Drive

## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.252	$0.133 + 0.059 \cdot \text{SL}$	$0.130 + 0.060 \cdot \text{SL}$	$0.128 + 0.060 \cdot \text{SL}$
	$t_F$	0.201	$0.104 + 0.049 \cdot \text{SL}$	$0.101 + 0.049 \cdot \text{SL}$	$0.098 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.191	$0.139 + 0.026 \cdot \text{SL}$	$0.139 + 0.026 \cdot \text{SL}$	$0.140 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.200	$0.151 + 0.024 \cdot \text{SL}$	$0.153 + 0.024 \cdot \text{SL}$	$0.154 + 0.024 \cdot \text{SL}$
B to Y	$t_R$	0.265	$0.150 + 0.057 \cdot \text{SL}$	$0.143 + 0.059 \cdot \text{SL}$	$0.136 + 0.060 \cdot \text{SL}$
	$t_F$	0.250	$0.160 + 0.045 \cdot \text{SL}$	$0.150 + 0.047 \cdot \text{SL}$	$0.138 + 0.049 \cdot \text{SL}$
	$t_{PLH}$	0.142	$0.089 + 0.026 \cdot \text{SL}$	$0.092 + 0.026 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.157	$0.110 + 0.024 \cdot \text{SL}$	$0.110 + 0.024 \cdot \text{SL}$	$0.110 + 0.024 \cdot \text{SL}$
C to Y	$t_R$	0.183	$0.130 + 0.026 \cdot \text{SL}$	$0.122 + 0.028 \cdot \text{SL}$	$0.110 + 0.030 \cdot \text{SL}$
	$t_F$	0.240	$0.146 + 0.047 \cdot \text{SL}$	$0.140 + 0.048 \cdot \text{SL}$	$0.133 + 0.049 \cdot \text{SL}$
	$t_{PLH}$	0.111	$0.082 + 0.015 \cdot \text{SL}$	$0.087 + 0.013 \cdot \text{SL}$	$0.087 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.161	$0.113 + 0.024 \cdot \text{SL}$	$0.114 + 0.024 \cdot \text{SL}$	$0.115 + 0.024 \cdot \text{SL}$

\*Group1 : SL < 4, \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ 

## SCG16D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.186	$0.128 + 0.029 \cdot \text{SL}$	$0.125 + 0.030 \cdot \text{SL}$	$0.119 + 0.030 \cdot \text{SL}$
	$t_F$	0.152	$0.103 + 0.024 \cdot \text{SL}$	$0.100 + 0.025 \cdot \text{SL}$	$0.096 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.181	$0.154 + 0.014 \cdot \text{SL}$	$0.157 + 0.013 \cdot \text{SL}$	$0.157 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.195	$0.169 + 0.013 \cdot \text{SL}$	$0.172 + 0.012 \cdot \text{SL}$	$0.175 + 0.012 \cdot \text{SL}$
B to Y	$t_R$	0.199	$0.144 + 0.027 \cdot \text{SL}$	$0.137 + 0.029 \cdot \text{SL}$	$0.128 + 0.030 \cdot \text{SL}$
	$t_F$	0.200	$0.158 + 0.021 \cdot \text{SL}$	$0.149 + 0.023 \cdot \text{SL}$	$0.132 + 0.024 \cdot \text{SL}$
	$t_{PLH}$	0.112	$0.083 + 0.014 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$	$0.089 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.128	$0.104 + 0.012 \cdot \text{SL}$	$0.105 + 0.012 \cdot \text{SL}$	$0.105 + 0.012 \cdot \text{SL}$
C to Y	$t_R$	0.150	$0.125 + 0.013 \cdot \text{SL}$	$0.121 + 0.014 \cdot \text{SL}$	$0.107 + 0.015 \cdot \text{SL}$
	$t_F$	0.185	$0.140 + 0.023 \cdot \text{SL}$	$0.136 + 0.024 \cdot \text{SL}$	$0.126 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.092	$0.075 + 0.008 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.130	$0.105 + 0.012 \cdot \text{SL}$	$0.107 + 0.012 \cdot \text{SL}$	$0.108 + 0.012 \cdot \text{SL}$

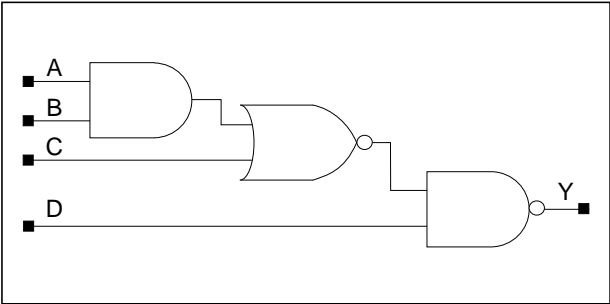
\*Group1 : SL < 4, \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG17/SCG17D2

2-AND into 2-NOR into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	0	1	0
x	0	0	1	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
SCG17				SCG17D2				SCG17	SCG17D2
A	B	C	D	A	B	C	D		
0.8	0.8	0.8	1.1	0.8	0.8	0.8	2.4	2.00	2.67



## Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG17

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.138	$0.079 + 0.029 \cdot \text{SL}$	$0.078 + 0.030 \cdot \text{SL}$	$0.072 + 0.030 \cdot \text{SL}$
	$t_F$	0.149	$0.085 + 0.032 \cdot \text{SL}$	$0.088 + 0.031 \cdot \text{SL}$	$0.085 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.204	$0.172 + 0.016 \cdot \text{SL}$	$0.179 + 0.014 \cdot \text{SL}$	$0.185 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.203	$0.165 + 0.019 \cdot \text{SL}$	$0.174 + 0.017 \cdot \text{SL}$	$0.182 + 0.016 \cdot \text{SL}$
B to Y	$t_R$	0.137	$0.077 + 0.030 \cdot \text{SL}$	$0.078 + 0.030 \cdot \text{SL}$	$0.073 + 0.030 \cdot \text{SL}$
	$t_F$	0.152	$0.088 + 0.032 \cdot \text{SL}$	$0.091 + 0.031 \cdot \text{SL}$	$0.088 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.196	$0.164 + 0.016 \cdot \text{SL}$	$0.171 + 0.014 \cdot \text{SL}$	$0.177 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.217	$0.179 + 0.019 \cdot \text{SL}$	$0.188 + 0.017 \cdot \text{SL}$	$0.196 + 0.016 \cdot \text{SL}$
C to Y	$t_R$	0.128	$0.071 + 0.029 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$	$0.061 + 0.031 \cdot \text{SL}$
	$t_F$	0.155	$0.092 + 0.031 \cdot \text{SL}$	$0.093 + 0.031 \cdot \text{SL}$	$0.089 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.203	$0.173 + 0.015 \cdot \text{SL}$	$0.178 + 0.014 \cdot \text{SL}$	$0.180 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.237	$0.198 + 0.019 \cdot \text{SL}$	$0.207 + 0.017 \cdot \text{SL}$	$0.216 + 0.016 \cdot \text{SL}$
D to Y	$t_R$	0.163	$0.111 + 0.026 \cdot \text{SL}$	$0.102 + 0.028 \cdot \text{SL}$	$0.090 + 0.030 \cdot \text{SL}$
	$t_F$	0.146	$0.088 + 0.029 \cdot \text{SL}$	$0.079 + 0.031 \cdot \text{SL}$	$0.072 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.101	$0.071 + 0.015 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.078 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.086	$0.050 + 0.018 \cdot \text{SL}$	$0.058 + 0.016 \cdot \text{SL}$	$0.060 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ 

## SCG17D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.122	$0.092 + 0.015 \cdot \text{SL}$	$0.093 + 0.015 \cdot \text{SL}$	$0.088 + 0.015 \cdot \text{SL}$
	$t_F$	0.129	$0.099 + 0.015 \cdot \text{SL}$	$0.097 + 0.016 \cdot \text{SL}$	$0.099 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.227	$0.208 + 0.010 \cdot \text{SL}$	$0.215 + 0.008 \cdot \text{SL}$	$0.227 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.220	$0.198 + 0.011 \cdot \text{SL}$	$0.205 + 0.009 \cdot \text{SL}$	$0.220 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.122	$0.092 + 0.015 \cdot \text{SL}$	$0.094 + 0.014 \cdot \text{SL}$	$0.088 + 0.015 \cdot \text{SL}$
	$t_F$	0.135	$0.104 + 0.016 \cdot \text{SL}$	$0.105 + 0.015 \cdot \text{SL}$	$0.103 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.220	$0.200 + 0.010 \cdot \text{SL}$	$0.207 + 0.008 \cdot \text{SL}$	$0.220 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.233	$0.210 + 0.011 \cdot \text{SL}$	$0.218 + 0.009 \cdot \text{SL}$	$0.233 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.108	$0.081 + 0.014 \cdot \text{SL}$	$0.079 + 0.014 \cdot \text{SL}$	$0.068 + 0.015 \cdot \text{SL}$
	$t_F$	0.135	$0.105 + 0.015 \cdot \text{SL}$	$0.102 + 0.016 \cdot \text{SL}$	$0.104 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.197 + 0.009 \cdot \text{SL}$	$0.202 + 0.007 \cdot \text{SL}$	$0.208 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.253	$0.231 + 0.011 \cdot \text{SL}$	$0.239 + 0.009 \cdot \text{SL}$	$0.254 + 0.008 \cdot \text{SL}$
D to Y	$t_R$	0.135	$0.111 + 0.012 \cdot \text{SL}$	$0.105 + 0.014 \cdot \text{SL}$	$0.090 + 0.015 \cdot \text{SL}$
	$t_F$	0.112	$0.083 + 0.015 \cdot \text{SL}$	$0.082 + 0.015 \cdot \text{SL}$	$0.071 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.083	$0.065 + 0.009 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$	$0.076 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.064	$0.044 + 0.010 \cdot \text{SL}$	$0.050 + 0.008 \cdot \text{SL}$	$0.058 + 0.008 \cdot \text{SL}$

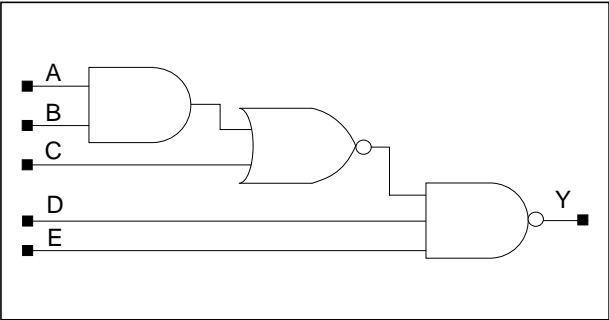
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SCG18/SCG18D2

2-AND into 2-NOR into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	0	1	1	0
x	0	0	1	1	0
Other States					1

Cell Data

Input Load (SL)										Gate Count	
SCG18					SCG18D2					SCG18	SCG18D2
A	B	C	D	E	A	B	C	D	E	2.33	3.33
0.8	0.8	0.8	1.0	1.0	0.8	0.8	0.8	2.1	2.2		



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## SCG18

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.173	$0.099 + 0.037 \cdot \text{SL}$	$0.096 + 0.038 \cdot \text{SL}$	$0.091 + 0.038 \cdot \text{SL}$
	$t_F$	0.212	$0.122 + 0.045 \cdot \text{SL}$	$0.122 + 0.045 \cdot \text{SL}$	$0.118 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.223	$0.185 + 0.019 \cdot \text{SL}$	$0.191 + 0.017 \cdot \text{SL}$	$0.195 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.227	$0.180 + 0.024 \cdot \text{SL}$	$0.186 + 0.022 \cdot \text{SL}$	$0.192 + 0.021 \cdot \text{SL}$
B to Y	$t_R$	0.173	$0.099 + 0.037 \cdot \text{SL}$	$0.096 + 0.038 \cdot \text{SL}$	$0.090 + 0.038 \cdot \text{SL}$
	$t_F$	0.216	$0.126 + 0.045 \cdot \text{SL}$	$0.126 + 0.045 \cdot \text{SL}$	$0.121 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.215	$0.177 + 0.019 \cdot \text{SL}$	$0.184 + 0.017 \cdot \text{SL}$	$0.187 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.241	$0.194 + 0.024 \cdot \text{SL}$	$0.201 + 0.022 \cdot \text{SL}$	$0.206 + 0.021 \cdot \text{SL}$
C to Y	$t_R$	0.164	$0.090 + 0.037 \cdot \text{SL}$	$0.085 + 0.038 \cdot \text{SL}$	$0.080 + 0.039 \cdot \text{SL}$
	$t_F$	0.216	$0.127 + 0.045 \cdot \text{SL}$	$0.127 + 0.045 \cdot \text{SL}$	$0.122 + 0.045 \cdot \text{SL}$
	$t_{PLH}$	0.221	$0.186 + 0.018 \cdot \text{SL}$	$0.189 + 0.017 \cdot \text{SL}$	$0.190 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.213 + 0.024 \cdot \text{SL}$	$0.220 + 0.022 \cdot \text{SL}$	$0.225 + 0.021 \cdot \text{SL}$
D to Y	$t_R$	0.199	$0.132 + 0.034 \cdot \text{SL}$	$0.122 + 0.036 \cdot \text{SL}$	$0.108 + 0.038 \cdot \text{SL}$
	$t_F$	0.210	$0.125 + 0.043 \cdot \text{SL}$	$0.117 + 0.045 \cdot \text{SL}$	$0.109 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.124	$0.090 + 0.017 \cdot \text{SL}$	$0.093 + 0.017 \cdot \text{SL}$	$0.092 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.119	$0.074 + 0.023 \cdot \text{SL}$	$0.079 + 0.021 \cdot \text{SL}$	$0.079 + 0.021 \cdot \text{SL}$
E to Y	$t_R$	0.221	$0.154 + 0.034 \cdot \text{SL}$	$0.145 + 0.036 \cdot \text{SL}$	$0.130 + 0.038 \cdot \text{SL}$
	$t_F$	0.203	$0.115 + 0.044 \cdot \text{SL}$	$0.110 + 0.045 \cdot \text{SL}$	$0.105 + 0.046 \cdot \text{SL}$
	$t_{PLH}$	0.135	$0.101 + 0.017 \cdot \text{SL}$	$0.102 + 0.017 \cdot \text{SL}$	$0.102 + 0.017 \cdot \text{SL}$
	$t_{PHL}$	0.119	$0.075 + 0.022 \cdot \text{SL}$	$0.078 + 0.022 \cdot \text{SL}$	$0.079 + 0.021 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## SCG18/SCG18D2

### 2-AND into 2-NOR into 3-NAND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG18D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.140	$0.105 + 0.018 \cdot \text{SL}$	$0.102 + 0.019 \cdot \text{SL}$	$0.097 + 0.019 \cdot \text{SL}$
	$t_F$	0.164	$0.119 + 0.023 \cdot \text{SL}$	$0.119 + 0.023 \cdot \text{SL}$	$0.118 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.235	$0.213 + 0.011 \cdot \text{SL}$	$0.219 + 0.009 \cdot \text{SL}$	$0.230 + 0.009 \cdot \text{SL}$
	$t_{PHL}$	0.228	$0.202 + 0.013 \cdot \text{SL}$	$0.208 + 0.012 \cdot \text{SL}$	$0.219 + 0.011 \cdot \text{SL}$
B to Y	$t_R$	0.140	$0.104 + 0.018 \cdot \text{SL}$	$0.102 + 0.018 \cdot \text{SL}$	$0.097 + 0.019 \cdot \text{SL}$
	$t_F$	0.170	$0.124 + 0.023 \cdot \text{SL}$	$0.126 + 0.022 \cdot \text{SL}$	$0.122 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.227	$0.205 + 0.011 \cdot \text{SL}$	$0.212 + 0.009 \cdot \text{SL}$	$0.223 + 0.009 \cdot \text{SL}$
	$t_{PHL}$	0.241	$0.214 + 0.013 \cdot \text{SL}$	$0.221 + 0.012 \cdot \text{SL}$	$0.232 + 0.011 \cdot \text{SL}$
C to Y	$t_R$	0.126	$0.090 + 0.018 \cdot \text{SL}$	$0.088 + 0.018 \cdot \text{SL}$	$0.078 + 0.019 \cdot \text{SL}$
	$t_F$	0.169	$0.125 + 0.022 \cdot \text{SL}$	$0.125 + 0.022 \cdot \text{SL}$	$0.122 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.223	$0.203 + 0.010 \cdot \text{SL}$	$0.208 + 0.009 \cdot \text{SL}$	$0.213 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.235 + 0.013 \cdot \text{SL}$	$0.241 + 0.012 \cdot \text{SL}$	$0.252 + 0.011 \cdot \text{SL}$
D to Y	$t_R$	0.156	$0.125 + 0.016 \cdot \text{SL}$	$0.117 + 0.018 \cdot \text{SL}$	$0.102 + 0.019 \cdot \text{SL}$
	$t_F$	0.156	$0.116 + 0.020 \cdot \text{SL}$	$0.109 + 0.022 \cdot \text{SL}$	$0.099 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.099	$0.079 + 0.010 \cdot \text{SL}$	$0.085 + 0.008 \cdot \text{SL}$	$0.086 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.088	$0.063 + 0.013 \cdot \text{SL}$	$0.069 + 0.011 \cdot \text{SL}$	$0.073 + 0.011 \cdot \text{SL}$
E to Y	$t_R$	0.177	$0.146 + 0.016 \cdot \text{SL}$	$0.139 + 0.017 \cdot \text{SL}$	$0.122 + 0.019 \cdot \text{SL}$
	$t_F$	0.148	$0.105 + 0.021 \cdot \text{SL}$	$0.100 + 0.023 \cdot \text{SL}$	$0.095 + 0.023 \cdot \text{SL}$
	$t_{PLH}$	0.111	$0.092 + 0.009 \cdot \text{SL}$	$0.096 + 0.008 \cdot \text{SL}$	$0.096 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.089	$0.064 + 0.012 \cdot \text{SL}$	$0.069 + 0.011 \cdot \text{SL}$	$0.073 + 0.011 \cdot \text{SL}$

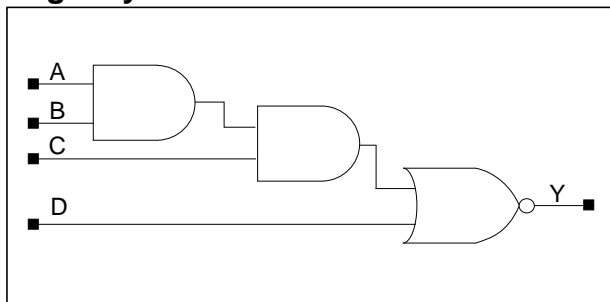
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## SCG19/SCG19D2

### 2-AND into 2-AND into 2-NOR with 1X/2X Drive

#### Logic Symbol



#### Truth Table

A	B	C	D	Y
1	1	1	x	0
x	x	x	1	0
Other States				1

#### Cell Data

Input Load (SL)								Gate Count	
SCG19				SCG19D2				SCG19	SCG19D2
A	B	C	D	A	B	C	D		
0.8	0.8	0.9	0.9	0.9	0.8	1.8	2.1	2.67	3.33



## SCG19/SCG19D2

### 2-AND into 2-AND into 2-NOR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG19

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.224	$0.103 + 0.060 \cdot \text{SL}$	$0.101 + 0.061 \cdot \text{SL}$	$0.100 + 0.061 \cdot \text{SL}$
	$t_F$	0.180	$0.078 + 0.051 \cdot \text{SL}$	$0.075 + 0.052 \cdot \text{SL}$	$0.071 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.241	$0.188 + 0.027 \cdot \text{SL}$	$0.189 + 0.026 \cdot \text{SL}$	$0.189 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.247	$0.195 + 0.026 \cdot \text{SL}$	$0.198 + 0.025 \cdot \text{SL}$	$0.199 + 0.025 \cdot \text{SL}$
B to Y	$t_R$	0.224	$0.104 + 0.060 \cdot \text{SL}$	$0.101 + 0.061 \cdot \text{SL}$	$0.100 + 0.061 \cdot \text{SL}$
	$t_F$	0.180	$0.078 + 0.051 \cdot \text{SL}$	$0.074 + 0.052 \cdot \text{SL}$	$0.071 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.257	$0.203 + 0.027 \cdot \text{SL}$	$0.205 + 0.026 \cdot \text{SL}$	$0.206 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.188 + 0.026 \cdot \text{SL}$	$0.191 + 0.025 \cdot \text{SL}$	$0.192 + 0.025 \cdot \text{SL}$
C to Y	$t_R$	0.268	$0.157 + 0.056 \cdot \text{SL}$	$0.143 + 0.059 \cdot \text{SL}$	$0.128 + 0.061 \cdot \text{SL}$
	$t_F$	0.192	$0.096 + 0.048 \cdot \text{SL}$	$0.086 + 0.051 \cdot \text{SL}$	$0.076 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.137	$0.085 + 0.026 \cdot \text{SL}$	$0.085 + 0.026 \cdot \text{SL}$	$0.084 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.121	$0.069 + 0.026 \cdot \text{SL}$	$0.073 + 0.025 \cdot \text{SL}$	$0.074 + 0.025 \cdot \text{SL}$
D to Y	$t_R$	0.257	$0.141 + 0.058 \cdot \text{SL}$	$0.133 + 0.060 \cdot \text{SL}$	$0.126 + 0.061 \cdot \text{SL}$
	$t_F$	0.185	$0.128 + 0.029 \cdot \text{SL}$	$0.120 + 0.031 \cdot \text{SL}$	$0.108 + 0.032 \cdot \text{SL}$
	$t_{PLH}$	0.154	$0.100 + 0.027 \cdot \text{SL}$	$0.102 + 0.026 \cdot \text{SL}$	$0.103 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.137	$0.102 + 0.017 \cdot \text{SL}$	$0.103 + 0.017 \cdot \text{SL}$	$0.104 + 0.017 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

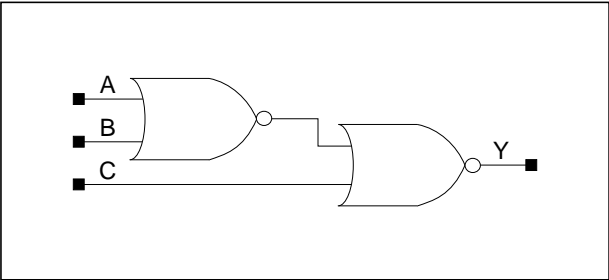
#### SCG19D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.177	$0.119 + 0.029 \cdot \text{SL}$	$0.117 + 0.030 \cdot \text{SL}$	$0.110 + 0.030 \cdot \text{SL}$
	$t_F$	0.143	$0.093 + 0.025 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$	$0.084 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.259	$0.231 + 0.014 \cdot \text{SL}$	$0.234 + 0.013 \cdot \text{SL}$	$0.236 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.253	$0.225 + 0.014 \cdot \text{SL}$	$0.230 + 0.013 \cdot \text{SL}$	$0.234 + 0.013 \cdot \text{SL}$
B to Y	$t_R$	0.178	$0.120 + 0.029 \cdot \text{SL}$	$0.117 + 0.030 \cdot \text{SL}$	$0.110 + 0.030 \cdot \text{SL}$
	$t_F$	0.143	$0.093 + 0.025 \cdot \text{SL}$	$0.090 + 0.026 \cdot \text{SL}$	$0.084 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.275	$0.247 + 0.014 \cdot \text{SL}$	$0.250 + 0.013 \cdot \text{SL}$	$0.252 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.247	$0.219 + 0.014 \cdot \text{SL}$	$0.224 + 0.013 \cdot \text{SL}$	$0.228 + 0.013 \cdot \text{SL}$
C to Y	$t_R$	0.215	$0.162 + 0.027 \cdot \text{SL}$	$0.153 + 0.029 \cdot \text{SL}$	$0.135 + 0.030 \cdot \text{SL}$
	$t_F$	0.149	$0.104 + 0.023 \cdot \text{SL}$	$0.094 + 0.025 \cdot \text{SL}$	$0.085 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.113	$0.085 + 0.014 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$	$0.086 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.097	$0.069 + 0.014 \cdot \text{SL}$	$0.075 + 0.013 \cdot \text{SL}$	$0.076 + 0.013 \cdot \text{SL}$
D to Y	$t_R$	0.204	$0.147 + 0.028 \cdot \text{SL}$	$0.141 + 0.030 \cdot \text{SL}$	$0.130 + 0.031 \cdot \text{SL}$
	$t_F$	0.155	$0.129 + 0.013 \cdot \text{SL}$	$0.123 + 0.015 \cdot \text{SL}$	$0.108 + 0.016 \cdot \text{SL}$
	$t_{PLH}$	0.125	$0.097 + 0.014 \cdot \text{SL}$	$0.100 + 0.013 \cdot \text{SL}$	$0.101 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.117	$0.098 + 0.009 \cdot \text{SL}$	$0.101 + 0.009 \cdot \text{SL}$	$0.102 + 0.009 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	Y
1	x	0	1
x	1	0	1
Other States			0

Cell Data

Input Load (SL)						Gate Count	
SCG20			SCG20D2			SCG20	SCG20D2
A	B	C	A	B	C	1.67	2.33
0.8	0.8	1.0	0.8	0.8	2.1		



## SCG20/SCG20D2

### 2-NOR into 2-NOR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG20

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.210	$0.093 + 0.058 \cdot \text{SL}$	$0.089 + 0.059 \cdot \text{SL}$	$0.085 + 0.060 \cdot \text{SL}$
	$t_F$	0.121	$0.066 + 0.028 \cdot \text{SL}$	$0.070 + 0.027 \cdot \text{SL}$	$0.067 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.173	$0.121 + 0.026 \cdot \text{SL}$	$0.122 + 0.026 \cdot \text{SL}$	$0.123 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.199	$0.162 + 0.018 \cdot \text{SL}$	$0.173 + 0.016 \cdot \text{SL}$	$0.182 + 0.015 \cdot \text{SL}$
B to Y	$t_R$	0.211	$0.096 + 0.058 \cdot \text{SL}$	$0.090 + 0.059 \cdot \text{SL}$	$0.086 + 0.060 \cdot \text{SL}$
	$t_F$	0.123	$0.069 + 0.027 \cdot \text{SL}$	$0.071 + 0.027 \cdot \text{SL}$	$0.067 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.191	$0.139 + 0.026 \cdot \text{SL}$	$0.140 + 0.026 \cdot \text{SL}$	$0.140 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.198	$0.161 + 0.018 \cdot \text{SL}$	$0.171 + 0.016 \cdot \text{SL}$	$0.180 + 0.015 \cdot \text{SL}$
C to Y	$t_R$	0.224	$0.113 + 0.056 \cdot \text{SL}$	$0.103 + 0.058 \cdot \text{SL}$	$0.094 + 0.059 \cdot \text{SL}$
	$t_F$	0.152	$0.108 + 0.022 \cdot \text{SL}$	$0.098 + 0.025 \cdot \text{SL}$	$0.082 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.124	$0.071 + 0.027 \cdot \text{SL}$	$0.075 + 0.025 \cdot \text{SL}$	$0.074 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.101	$0.067 + 0.017 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

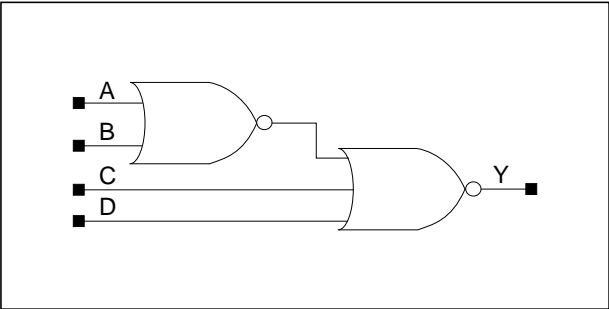
#### SCG20D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.147	$0.090 + 0.028 \cdot \text{SL}$	$0.086 + 0.029 \cdot \text{SL}$	$0.079 + 0.030 \cdot \text{SL}$
	$t_F$	0.108	$0.080 + 0.014 \cdot \text{SL}$	$0.084 + 0.013 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.167	$0.140 + 0.013 \cdot \text{SL}$	$0.143 + 0.013 \cdot \text{SL}$	$0.143 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.214	$0.191 + 0.011 \cdot \text{SL}$	$0.200 + 0.009 \cdot \text{SL}$	$0.218 + 0.008 \cdot \text{SL}$
B to Y	$t_R$	0.148	$0.091 + 0.028 \cdot \text{SL}$	$0.088 + 0.029 \cdot \text{SL}$	$0.080 + 0.030 \cdot \text{SL}$
	$t_F$	0.109	$0.080 + 0.014 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$	$0.084 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.183	$0.156 + 0.014 \cdot \text{SL}$	$0.159 + 0.013 \cdot \text{SL}$	$0.159 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.213	$0.190 + 0.011 \cdot \text{SL}$	$0.200 + 0.009 \cdot \text{SL}$	$0.218 + 0.008 \cdot \text{SL}$
C to Y	$t_R$	0.160	$0.108 + 0.026 \cdot \text{SL}$	$0.098 + 0.029 \cdot \text{SL}$	$0.088 + 0.030 \cdot \text{SL}$
	$t_F$	0.126	$0.105 + 0.011 \cdot \text{SL}$	$0.100 + 0.012 \cdot \text{SL}$	$0.082 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.093	$0.064 + 0.015 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.079	$0.059 + 0.010 \cdot \text{SL}$	$0.069 + 0.008 \cdot \text{SL}$	$0.073 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	D	Y
1	x	0	0	1
x	1	0	0	1
Other States				0

Cell Data

Input Load (SL)								Gate Count	
SCG21				SCG21D2				SCG21	SCG21D2
A	B	C	D	A	B	C	D		
0.8	0.8	0.9	0.9	0.8	0.8	1.9	2.0	2.00	3.00



## SCG21/SCG21D2

### 2-NOR into 3-NOR with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.343	$0.165 + 0.089 \cdot \text{SL}$	$0.163 + 0.089 \cdot \text{SL}$	$0.164 + 0.089 \cdot \text{SL}$
	$t_F$	0.150	$0.083 + 0.033 \cdot \text{SL}$	$0.081 + 0.034 \cdot \text{SL}$	$0.078 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.136 + 0.039 \cdot \text{SL}$	$0.137 + 0.038 \cdot \text{SL}$	$0.138 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.223	$0.179 + 0.022 \cdot \text{SL}$	$0.189 + 0.019 \cdot \text{SL}$	$0.196 + 0.018 \cdot \text{SL}$
B to Y	$t_R$	0.344	$0.167 + 0.089 \cdot \text{SL}$	$0.164 + 0.089 \cdot \text{SL}$	$0.164 + 0.089 \cdot \text{SL}$
	$t_F$	0.149	$0.082 + 0.034 \cdot \text{SL}$	$0.082 + 0.034 \cdot \text{SL}$	$0.078 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.231	$0.154 + 0.039 \cdot \text{SL}$	$0.154 + 0.038 \cdot \text{SL}$	$0.155 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.221	$0.178 + 0.022 \cdot \text{SL}$	$0.188 + 0.019 \cdot \text{SL}$	$0.195 + 0.018 \cdot \text{SL}$
C to Y	$t_R$	0.359	$0.188 + 0.086 \cdot \text{SL}$	$0.180 + 0.088 \cdot \text{SL}$	$0.171 + 0.089 \cdot \text{SL}$
	$t_F$	0.176	$0.117 + 0.030 \cdot \text{SL}$	$0.106 + 0.032 \cdot \text{SL}$	$0.091 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.184	$0.107 + 0.038 \cdot \text{SL}$	$0.108 + 0.038 \cdot \text{SL}$	$0.108 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.125	$0.087 + 0.019 \cdot \text{SL}$	$0.091 + 0.018 \cdot \text{SL}$	$0.091 + 0.018 \cdot \text{SL}$
D to Y	$t_R$	0.355	$0.181 + 0.087 \cdot \text{SL}$	$0.176 + 0.088 \cdot \text{SL}$	$0.169 + 0.089 \cdot \text{SL}$
	$t_F$	0.203	$0.142 + 0.031 \cdot \text{SL}$	$0.136 + 0.032 \cdot \text{SL}$	$0.121 + 0.034 \cdot \text{SL}$
	$t_{PLH}$	0.194	$0.117 + 0.039 \cdot \text{SL}$	$0.118 + 0.038 \cdot \text{SL}$	$0.119 + 0.038 \cdot \text{SL}$
	$t_{PHL}$	0.135	$0.096 + 0.019 \cdot \text{SL}$	$0.099 + 0.019 \cdot \text{SL}$	$0.101 + 0.018 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

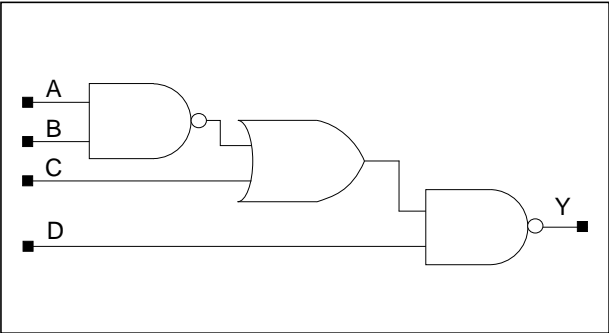
#### SCG21D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.233	$0.145 + 0.044 \cdot \text{SL}$	$0.141 + 0.045 \cdot \text{SL}$	$0.138 + 0.045 \cdot \text{SL}$
	$t_F$	0.122	$0.086 + 0.018 \cdot \text{SL}$	$0.091 + 0.017 \cdot \text{SL}$	$0.088 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.185	$0.147 + 0.019 \cdot \text{SL}$	$0.147 + 0.019 \cdot \text{SL}$	$0.147 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.227	$0.201 + 0.013 \cdot \text{SL}$	$0.211 + 0.011 \cdot \text{SL}$	$0.227 + 0.009 \cdot \text{SL}$
B to Y	$t_R$	0.234	$0.146 + 0.044 \cdot \text{SL}$	$0.143 + 0.045 \cdot \text{SL}$	$0.139 + 0.045 \cdot \text{SL}$
	$t_F$	0.122	$0.086 + 0.018 \cdot \text{SL}$	$0.091 + 0.017 \cdot \text{SL}$	$0.088 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.202	$0.163 + 0.019 \cdot \text{SL}$	$0.163 + 0.019 \cdot \text{SL}$	$0.163 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.226	$0.200 + 0.013 \cdot \text{SL}$	$0.210 + 0.011 \cdot \text{SL}$	$0.227 + 0.009 \cdot \text{SL}$
C to Y	$t_R$	0.251	$0.167 + 0.042 \cdot \text{SL}$	$0.159 + 0.044 \cdot \text{SL}$	$0.149 + 0.045 \cdot \text{SL}$
	$t_F$	0.140	$0.112 + 0.014 \cdot \text{SL}$	$0.106 + 0.015 \cdot \text{SL}$	$0.087 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.135	$0.094 + 0.020 \cdot \text{SL}$	$0.098 + 0.019 \cdot \text{SL}$	$0.099 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.098	$0.076 + 0.011 \cdot \text{SL}$	$0.083 + 0.009 \cdot \text{SL}$	$0.085 + 0.009 \cdot \text{SL}$
D to Y	$t_R$	0.246	$0.161 + 0.043 \cdot \text{SL}$	$0.155 + 0.044 \cdot \text{SL}$	$0.145 + 0.045 \cdot \text{SL}$
	$t_F$	0.166	$0.137 + 0.014 \cdot \text{SL}$	$0.132 + 0.016 \cdot \text{SL}$	$0.116 + 0.017 \cdot \text{SL}$
	$t_{PLH}$	0.145	$0.104 + 0.020 \cdot \text{SL}$	$0.108 + 0.019 \cdot \text{SL}$	$0.109 + 0.019 \cdot \text{SL}$
	$t_{PHL}$	0.108	$0.086 + 0.011 \cdot \text{SL}$	$0.092 + 0.009 \cdot \text{SL}$	$0.095 + 0.009 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



Logic Symbol



Truth Table

A	B	C	D	Y
1	1	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)								Gate Count	
SCG22				SCG22D2				SCG22	SCG22D2
A	B	C	D	A	B	C	D		
0.8	0.9	1.0	1.0	0.8	0.9	2.0	2.0	2.00	3.00



## SCG22/SCG22D2

### 2-NAND into 2-OR into 2-NAND with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### SCG22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.255	$0.137 + 0.059 \cdot \text{SL}$	$0.133 + 0.060 \cdot \text{SL}$	$0.129 + 0.061 \cdot \text{SL}$
	$t_F$	0.204	$0.106 + 0.049 \cdot \text{SL}$	$0.102 + 0.050 \cdot \text{SL}$	$0.098 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.205	$0.152 + 0.027 \cdot \text{SL}$	$0.154 + 0.026 \cdot \text{SL}$	$0.155 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.216	$0.165 + 0.025 \cdot \text{SL}$	$0.168 + 0.024 \cdot \text{SL}$	$0.169 + 0.024 \cdot \text{SL}$
B to Y	$t_R$	0.255	$0.137 + 0.059 \cdot \text{SL}$	$0.133 + 0.060 \cdot \text{SL}$	$0.129 + 0.061 \cdot \text{SL}$
	$t_F$	0.206	$0.107 + 0.049 \cdot \text{SL}$	$0.104 + 0.050 \cdot \text{SL}$	$0.099 + 0.051 \cdot \text{SL}$
	$t_{PLH}$	0.201	$0.147 + 0.027 \cdot \text{SL}$	$0.150 + 0.026 \cdot \text{SL}$	$0.151 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.226	$0.176 + 0.025 \cdot \text{SL}$	$0.178 + 0.024 \cdot \text{SL}$	$0.180 + 0.024 \cdot \text{SL}$
C to Y	$t_R$	0.263	$0.148 + 0.058 \cdot \text{SL}$	$0.140 + 0.060 \cdot \text{SL}$	$0.134 + 0.060 \cdot \text{SL}$
	$t_F$	0.251	$0.160 + 0.046 \cdot \text{SL}$	$0.149 + 0.048 \cdot \text{SL}$	$0.136 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.142	$0.088 + 0.027 \cdot \text{SL}$	$0.090 + 0.026 \cdot \text{SL}$	$0.091 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.157	$0.109 + 0.024 \cdot \text{SL}$	$0.109 + 0.024 \cdot \text{SL}$	$0.109 + 0.024 \cdot \text{SL}$
D to Y	$t_R$	0.182	$0.129 + 0.027 \cdot \text{SL}$	$0.120 + 0.029 \cdot \text{SL}$	$0.108 + 0.030 \cdot \text{SL}$
	$t_F$	0.241	$0.145 + 0.048 \cdot \text{SL}$	$0.139 + 0.049 \cdot \text{SL}$	$0.132 + 0.050 \cdot \text{SL}$
	$t_{PLH}$	0.111	$0.081 + 0.015 \cdot \text{SL}$	$0.087 + 0.013 \cdot \text{SL}$	$0.086 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.162	$0.113 + 0.025 \cdot \text{SL}$	$0.114 + 0.024 \cdot \text{SL}$	$0.115 + 0.024 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### SCG22D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.191	$0.133 + 0.029 \cdot \text{SL}$	$0.131 + 0.029 \cdot \text{SL}$	$0.125 + 0.030 \cdot \text{SL}$
	$t_F$	0.156	$0.105 + 0.025 \cdot \text{SL}$	$0.105 + 0.025 \cdot \text{SL}$	$0.098 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.196	$0.168 + 0.014 \cdot \text{SL}$	$0.172 + 0.013 \cdot \text{SL}$	$0.174 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.209	$0.182 + 0.014 \cdot \text{SL}$	$0.186 + 0.013 \cdot \text{SL}$	$0.189 + 0.012 \cdot \text{SL}$
B to Y	$t_R$	0.191	$0.134 + 0.029 \cdot \text{SL}$	$0.131 + 0.029 \cdot \text{SL}$	$0.125 + 0.030 \cdot \text{SL}$
	$t_F$	0.158	$0.108 + 0.025 \cdot \text{SL}$	$0.106 + 0.025 \cdot \text{SL}$	$0.100 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.189	$0.161 + 0.014 \cdot \text{SL}$	$0.165 + 0.013 \cdot \text{SL}$	$0.168 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.222	$0.195 + 0.014 \cdot \text{SL}$	$0.199 + 0.013 \cdot \text{SL}$	$0.202 + 0.012 \cdot \text{SL}$
C to Y	$t_R$	0.197	$0.142 + 0.027 \cdot \text{SL}$	$0.135 + 0.029 \cdot \text{SL}$	$0.127 + 0.030 \cdot \text{SL}$
	$t_F$	0.204	$0.160 + 0.022 \cdot \text{SL}$	$0.152 + 0.024 \cdot \text{SL}$	$0.133 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.110	$0.081 + 0.014 \cdot \text{SL}$	$0.086 + 0.013 \cdot \text{SL}$	$0.088 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.130	$0.105 + 0.013 \cdot \text{SL}$	$0.106 + 0.012 \cdot \text{SL}$	$0.106 + 0.012 \cdot \text{SL}$
D to Y	$t_R$	0.147	$0.122 + 0.013 \cdot \text{SL}$	$0.119 + 0.013 \cdot \text{SL}$	$0.104 + 0.015 \cdot \text{SL}$
	$t_F$	0.190	$0.143 + 0.023 \cdot \text{SL}$	$0.137 + 0.025 \cdot \text{SL}$	$0.129 + 0.025 \cdot \text{SL}$
	$t_{PLH}$	0.090	$0.073 + 0.008 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.132	$0.106 + 0.013 \cdot \text{SL}$	$0.108 + 0.012 \cdot \text{SL}$	$0.109 + 0.012 \cdot \text{SL}$

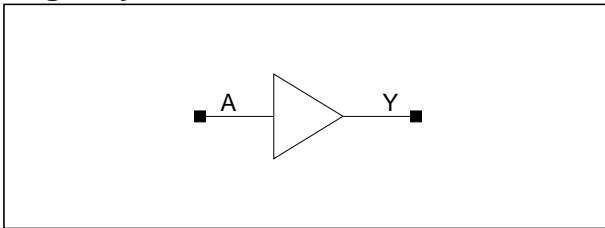
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# DL1D2/DL1D4

## 1ns Delay Cell with 2X/4X Drive

### Logic Symbol



### Truth Table

A	Y
0	0
1	1

### Cell Data

Input Load (SL)		Gate Count	
DL1D2	DL1D4	DL1D2	DL1D4
A	A	4.00	4.67
0.7	0.7		

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### DL1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.080	$0.052 + 0.014 \cdot \text{SL}$	$0.051 + 0.014 \cdot \text{SL}$	$0.041 + 0.015 \cdot \text{SL}$
	$t_F$	0.072	$0.046 + 0.013 \cdot \text{SL}$	$0.049 + 0.012 \cdot \text{SL}$	$0.042 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.987	$0.970 + 0.008 \cdot \text{SL}$	$0.976 + 0.007 \cdot \text{SL}$	$0.980 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.988	$0.970 + 0.009 \cdot \text{SL}$	$0.977 + 0.007 \cdot \text{SL}$	$0.984 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### DL1D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.081	$0.067 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.075	$0.062 + 0.006 \cdot \text{SL}$	$0.063 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	1.018	$1.008 + 0.005 \cdot \text{SL}$	$1.013 + 0.004 \cdot \text{SL}$	$1.023 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.017	$1.006 + 0.005 \cdot \text{SL}$	$1.011 + 0.004 \cdot \text{SL}$	$1.025 + 0.004 \cdot \text{SL}$

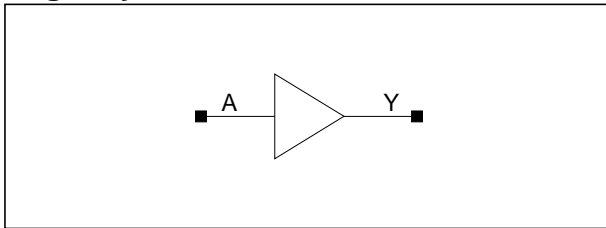
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## DL2D2/DL2D4

### 2ns Delay Cell with 2X/4X Drive

#### Logic Symbol



#### Truth Table

A	Y
0	0
1	1

#### Cell Data

Input Load (SL)		Gate Count	
DL2D2	DL2D4	DL2D2	DL2D4
A	A	4.67	5.33
0.7	0.7		

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### DL2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.091	$0.064 + 0.014 \cdot \text{SL}$	$0.063 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.013 \cdot \text{SL}$	$0.058 + 0.012 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	1.975	$1.958 + 0.008 \cdot \text{SL}$	$1.964 + 0.007 \cdot \text{SL}$	$1.969 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	1.984	$1.965 + 0.009 \cdot \text{SL}$	$1.972 + 0.008 \cdot \text{SL}$	$1.981 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### DL2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.094	$0.082 + 0.006 \cdot \text{SL}$	$0.079 + 0.007 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$
	$t_F$	0.085	$0.071 + 0.007 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$	$0.070 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	2.015	$2.004 + 0.005 \cdot \text{SL}$	$2.009 + 0.004 \cdot \text{SL}$	$2.022 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	2.017	$2.006 + 0.006 \cdot \text{SL}$	$2.012 + 0.004 \cdot \text{SL}$	$2.027 + 0.004 \cdot \text{SL}$

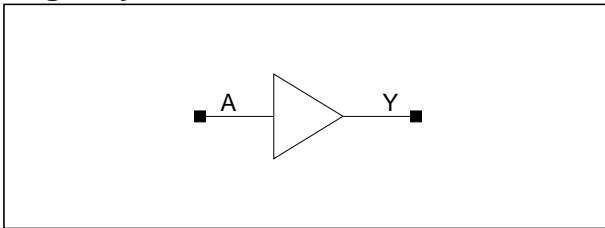
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## DL3D2/DL3D4

### 3ns Delay Cell with 2X/4X Drive

#### Logic Symbol



#### Truth Table

A	Y
0	0
1	1

#### Cell Data

Input Load (SL)		Gate Count	
DL3D2	DL3D4	DL3D2	DL3D4
A	A	5.33	6.33
0.7	0.7		

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### DL3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.081	$0.053 + 0.014 \cdot \text{SL}$	$0.052 + 0.014 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.075	$0.048 + 0.014 \cdot \text{SL}$	$0.052 + 0.012 \cdot \text{SL}$	$0.046 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	2.989	$2.972 + 0.008 \cdot \text{SL}$	$2.977 + 0.007 \cdot \text{SL}$	$2.982 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	3.039	$3.020 + 0.009 \cdot \text{SL}$	$3.027 + 0.008 \cdot \text{SL}$	$3.035 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### DL3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.064 + 0.007 \cdot \text{SL}$	$0.066 + 0.006 \cdot \text{SL}$	$0.063 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	3.017	$3.007 + 0.005 \cdot \text{SL}$	$3.012 + 0.004 \cdot \text{SL}$	$3.022 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	3.066	$3.055 + 0.006 \cdot \text{SL}$	$3.060 + 0.004 \cdot \text{SL}$	$3.075 + 0.004 \cdot \text{SL}$

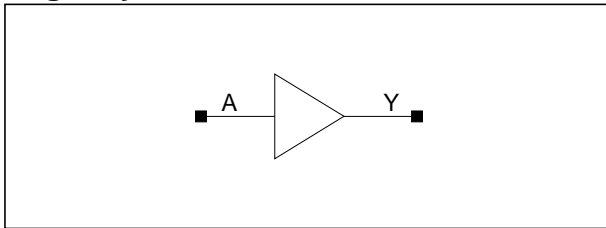
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## DL4D2/DL4D4

### 4ns Delay Cell with 2X/4X Drive

#### Logic Symbol



#### Truth Table

A	Y
0	0
1	1

#### Cell Data

Input Load (SL)		Gate Count	
DL4D2	DL4D4	DL4D2	DL4D4
A	A	6.00	6.67
0.7	0.7		

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### DL4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.081	$0.053 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.076	$0.049 + 0.013 \cdot \text{SL}$	$0.053 + 0.012 \cdot \text{SL}$	$0.046 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	4.080	$4.063 + 0.008 \cdot \text{SL}$	$4.069 + 0.007 \cdot \text{SL}$	$4.073 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	4.178	$4.160 + 0.009 \cdot \text{SL}$	$4.167 + 0.008 \cdot \text{SL}$	$4.175 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

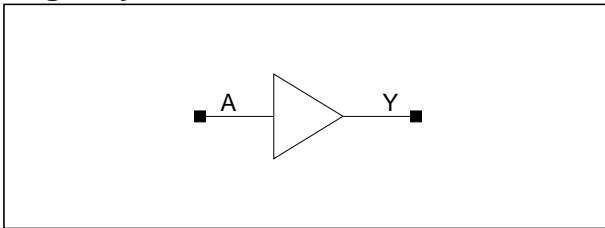
##### DL4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$	$0.065 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	4.107	$4.097 + 0.005 \cdot \text{SL}$	$4.102 + 0.004 \cdot \text{SL}$	$4.113 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	4.209	$4.197 + 0.006 \cdot \text{SL}$	$4.203 + 0.004 \cdot \text{SL}$	$4.218 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## Logic Symbol



## Truth Table

A	Y
0	0
1	1

## Cell Data

Input Load (SL)		Gate Count	
DL5D2	DL5D4	DL5D2	DL5D4
A	A	6.67	7.33
0.7	0.7		

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

## DL5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.081	$0.054 + 0.013 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.079	$0.053 + 0.013 \cdot \text{SL}$	$0.055 + 0.012 \cdot \text{SL}$	$0.046 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	5.104	$5.087 + 0.008 \cdot \text{SL}$	$5.092 + 0.007 \cdot \text{SL}$	$5.097 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	5.123	$5.105 + 0.009 \cdot \text{SL}$	$5.112 + 0.008 \cdot \text{SL}$	$5.119 + 0.007 \cdot \text{SL}$

\*Group1 : SL < 4, \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$ 

## DL5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.068 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_F$	0.080	$0.067 + 0.007 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	5.133	$5.123 + 0.005 \cdot \text{SL}$	$5.128 + 0.004 \cdot \text{SL}$	$5.138 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	5.152	$5.141 + 0.006 \cdot \text{SL}$	$5.147 + 0.004 \cdot \text{SL}$	$5.161 + 0.004 \cdot \text{SL}$

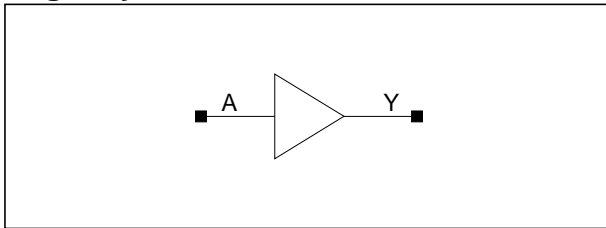
\*Group1 : SL < 4, \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## DL10D2/DL10D4

### 10ns Delay Cell with 2X/4X Drive

#### Logic Symbol



#### Truth Table

A	Y
0	0
1	1

#### Cell Data

Input Load (SL)		Gate Count	
DL10D2	DL10D4	DL10D2	DL2D4
A	A	8.67	9.33
0.7	0.7		

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### DL10D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.051 + 0.014 \cdot \text{SL}$	$0.043 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.055 + 0.013 \cdot \text{SL}$	$0.057 + 0.012 \cdot \text{SL}$	$0.050 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	10.138	$10.121 + 0.008 \cdot \text{SL}$	$10.127 + 0.007 \cdot \text{SL}$	$10.131 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	10.173	$10.154 + 0.009 \cdot \text{SL}$	$10.161 + 0.008 \cdot \text{SL}$	$10.169 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

##### DL10D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.083	$0.069 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.059 + 0.007 \cdot \text{SL}$
	$t_F$	0.083	$0.069 + 0.007 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$	$0.068 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	10.167	$10.157 + 0.005 \cdot \text{SL}$	$10.161 + 0.004 \cdot \text{SL}$	$10.173 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	10.202	$10.191 + 0.006 \cdot \text{SL}$	$10.197 + 0.004 \cdot \text{SL}$	$10.212 + 0.004 \cdot \text{SL}$

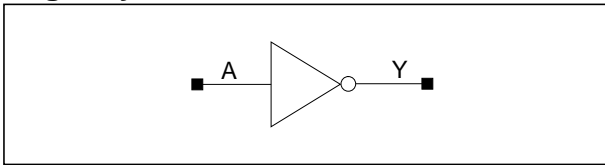
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



## IVDH/IV/IVD2/IVD3/IVD4/IVD6/IVD8/IVD16

Inverter with 0.5X/1X/2X/3X/4X/6X/8X/16X Drive

### Logic Symbol



### Truth Table

A	Y
0	1
1	0

### Cell Data

Input Load (SL)							
IVDH	IV	IVD2	IVD3	IVD4	IVD6	IVD8	IVD16
A	A	A	A	A	A	A	A
0.5	1.0	2.0	2.9	3.9	5.9	7.9	15.9
Gate Count							
IVDH	IV	IVD2	IVD3	IVD4	IVD6	IVD8	IVD16
0.67	0.67	1.00	1.33	1.67	2.33	2.67	5.00



# IVDH/IV/IVD2/IVD3/IVD4/IVD6/IVD8/IVD16

## Inverter with 0.5X/1X/2X/3X/4X/6X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### IVDH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.209	$0.090 + 0.059 \cdot \text{SL}$	$0.072 + 0.064 \cdot \text{SL}$	$0.053 + 0.066 \cdot \text{SL}$
	$t_F$	0.173	$0.082 + 0.045 \cdot \text{SL}$	$0.064 + 0.050 \cdot \text{SL}$	$0.045 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.123	$0.064 + 0.030 \cdot \text{SL}$	$0.069 + 0.028 \cdot \text{SL}$	$0.067 + 0.029 \cdot \text{SL}$
	$t_{PHL}$	0.114	$0.057 + 0.029 \cdot \text{SL}$	$0.064 + 0.027 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### IV

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.142	$0.090 + 0.026 \cdot \text{SL}$	$0.081 + 0.028 \cdot \text{SL}$	$0.067 + 0.030 \cdot \text{SL}$
	$t_F$	0.126	$0.082 + 0.022 \cdot \text{SL}$	$0.074 + 0.024 \cdot \text{SL}$	$0.059 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.083	$0.050 + 0.017 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.082	$0.047 + 0.017 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### IVD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.105	$0.077 + 0.014 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.062 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.068 + 0.013 \cdot \text{SL}$	$0.074 + 0.011 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.058	$0.038 + 0.010 \cdot \text{SL}$	$0.049 + 0.008 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.056	$0.034 + 0.011 \cdot \text{SL}$	$0.047 + 0.008 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### IVD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.098	$0.078 + 0.010 \cdot \text{SL}$	$0.082 + 0.009 \cdot \text{SL}$	$0.061 + 0.010 \cdot \text{SL}$
	$t_F$	0.087	$0.068 + 0.010 \cdot \text{SL}$	$0.076 + 0.008 \cdot \text{SL}$	$0.054 + 0.009 \cdot \text{SL}$
	$t_{PLH}$	0.053	$0.038 + 0.008 \cdot \text{SL}$	$0.048 + 0.005 \cdot \text{SL}$	$0.061 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.051	$0.035 + 0.008 \cdot \text{SL}$	$0.046 + 0.005 \cdot \text{SL}$	$0.059 + 0.005 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# IVDH/IV/IVD2/IVD3/IVD4/IVD6/IVD8/IVD16

## Inverter with 0.5X/1X/2X/3X/4X/6X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### IVD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.095	$0.080 + 0.008 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$
	$t_F$	0.084	$0.070 + 0.007 \cdot \text{SL}$	$0.076 + 0.006 \cdot \text{SL}$	$0.061 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.051	$0.039 + 0.006 \cdot \text{SL}$	$0.046 + 0.004 \cdot \text{SL}$	$0.063 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.049	$0.037 + 0.006 \cdot \text{SL}$	$0.045 + 0.004 \cdot \text{SL}$	$0.061 + 0.003 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$

#### IVD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.085	$0.073 + 0.006 \cdot \text{SL}$	$0.077 + 0.005 \cdot \text{SL}$	$0.042 + 0.005 \cdot \text{SL}$
	$t_F$	0.076	$0.066 + 0.005 \cdot \text{SL}$	$0.069 + 0.004 \cdot \text{SL}$	$0.035 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.043	$0.034 + 0.004 \cdot \text{SL}$	$0.042 + 0.002 \cdot \text{SL}$	$0.059 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.040	$0.031 + 0.005 \cdot \text{SL}$	$0.039 + 0.003 \cdot \text{SL}$	$0.056 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### IVD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.073 + 0.005 \cdot \text{SL}$	$0.077 + 0.003 \cdot \text{SL}$	$0.050 + 0.004 \cdot \text{SL}$
	$t_F$	0.073	$0.066 + 0.004 \cdot \text{SL}$	$0.069 + 0.003 \cdot \text{SL}$	$0.043 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.041	$0.034 + 0.003 \cdot \text{SL}$	$0.040 + 0.002 \cdot \text{SL}$	$0.060 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.038	$0.031 + 0.004 \cdot \text{SL}$	$0.038 + 0.002 \cdot \text{SL}$	$0.057 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### IVD16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.077	$0.072 + 0.002 \cdot \text{SL}$	$0.075 + 0.002 \cdot \text{SL}$	$0.065 + 0.002 \cdot \text{SL}$
	$t_F$	0.069	$0.066 + 0.002 \cdot \text{SL}$	$0.067 + 0.001 \cdot \text{SL}$	$0.059 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.037	$0.033 + 0.002 \cdot \text{SL}$	$0.037 + 0.001 \cdot \text{SL}$	$0.060 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.034	$0.030 + 0.002 \cdot \text{SL}$	$0.034 + 0.001 \cdot \text{SL}$	$0.058 + 0.001 \cdot \text{SL}$

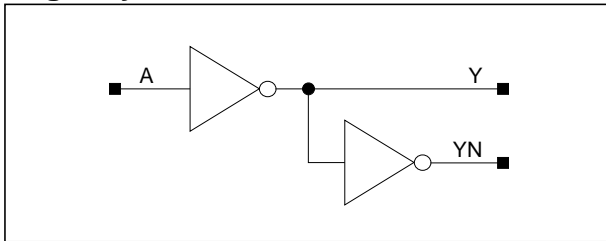
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$



# IVCD(11/13)/IVCD(22/26)/IVCD44

1X IV into (1X/3X) IV/2X IV into (2X/6X) IV/4X IV into 4X IV

## Logic Symbol



## Truth Table

A	Y	YN
1	0	1
0	1	0

## Cell Data

Input Load (SL)					Gate Count				
IVCD11	IVCD13	IVCD22	IVCD26	IVCD44	IVCD11	IVCD13	IVCD22	IVCD26	IVCD44
A	A	A	A	A					
1.0	1.0	2.0	1.9	3.8	1.00	1.67	1.67	2.67	3.00

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

### IVCD11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.176	$0.123 + 0.026 \cdot \text{SL}$	$0.115 + 0.028 \cdot \text{SL}$	$0.102 + 0.030 \cdot \text{SL}$
	$t_F$	0.158	$0.112 + 0.023 \cdot \text{SL}$	$0.103 + 0.025 \cdot \text{SL}$	$0.091 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.102	$0.071 + 0.015 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$	$0.079 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.103	$0.071 + 0.016 \cdot \text{SL}$	$0.079 + 0.014 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$
Y to YN	$t_R$	0.124	$0.082 + 0.021 \cdot \text{SL}$	$0.074 + 0.023 \cdot \text{SL}$	$0.059 + 0.025 \cdot \text{SL}$
	$t_F$	0.142	$0.090 + 0.026 \cdot \text{SL}$	$0.081 + 0.028 \cdot \text{SL}$	$0.067 + 0.030 \cdot \text{SL}$
	$t_{PLH}$	0.081	$0.047 + 0.017 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.084	$0.050 + 0.017 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

### IVCD13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.234	$0.181 + 0.027 \cdot \text{SL}$	$0.168 + 0.030 \cdot \text{SL}$	$0.139 + 0.031 \cdot \text{SL}$
	$t_F$	0.204	$0.160 + 0.022 \cdot \text{SL}$	$0.148 + 0.025 \cdot \text{SL}$	$0.118 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.131	$0.104 + 0.014 \cdot \text{SL}$	$0.105 + 0.013 \cdot \text{SL}$	$0.104 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.127	$0.099 + 0.014 \cdot \text{SL}$	$0.100 + 0.014 \cdot \text{SL}$	$0.099 + 0.014 \cdot \text{SL}$
Y to YN	$t_R$	0.087	$0.068 + 0.010 \cdot \text{SL}$	$0.076 + 0.008 \cdot \text{SL}$	$0.054 + 0.009 \cdot \text{SL}$
	$t_F$	0.098	$0.078 + 0.010 \cdot \text{SL}$	$0.082 + 0.009 \cdot \text{SL}$	$0.061 + 0.010 \cdot \text{SL}$
	$t_{PLH}$	0.051	$0.035 + 0.008 \cdot \text{SL}$	$0.046 + 0.005 \cdot \text{SL}$	$0.059 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.053	$0.038 + 0.008 \cdot \text{SL}$	$0.048 + 0.005 \cdot \text{SL}$	$0.061 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# IVCD(11/13)/IVCD(22/26)/IVCD44

## 1X IV into (1X/3X) IV/2X IV into (2X/6X) IV/4X IV into 4X IV

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### IVCD22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.139	$0.114 + 0.012 \cdot \text{SL}$	$0.109 + 0.014 \cdot \text{SL}$	$0.095 + 0.015 \cdot \text{SL}$
	$t_F$	0.124	$0.103 + 0.011 \cdot \text{SL}$	$0.100 + 0.011 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.079	$0.061 + 0.009 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$	$0.074 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.076	$0.057 + 0.009 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$
Y to YN	$t_R$	0.093	$0.068 + 0.013 \cdot \text{SL}$	$0.074 + 0.011 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_F$	0.105	$0.078 + 0.014 \cdot \text{SL}$	$0.078 + 0.014 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.056	$0.034 + 0.011 \cdot \text{SL}$	$0.047 + 0.008 \cdot \text{SL}$	$0.058 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.059	$0.038 + 0.010 \cdot \text{SL}$	$0.050 + 0.008 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### IVCD26

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.200	$0.174 + 0.013 \cdot \text{SL}$	$0.165 + 0.015 \cdot \text{SL}$	$0.126 + 0.016 \cdot \text{SL}$
	$t_F$	0.178	$0.156 + 0.011 \cdot \text{SL}$	$0.147 + 0.013 \cdot \text{SL}$	$0.108 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.112	$0.097 + 0.008 \cdot \text{SL}$	$0.100 + 0.007 \cdot \text{SL}$	$0.099 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.108	$0.092 + 0.008 \cdot \text{SL}$	$0.095 + 0.007 \cdot \text{SL}$	$0.094 + 0.007 \cdot \text{SL}$
Y to YN	$t_R$	0.076	$0.066 + 0.005 \cdot \text{SL}$	$0.070 + 0.004 \cdot \text{SL}$	$0.035 + 0.004 \cdot \text{SL}$
	$t_F$	0.085	$0.073 + 0.006 \cdot \text{SL}$	$0.078 + 0.005 \cdot \text{SL}$	$0.042 + 0.005 \cdot \text{SL}$
	$t_{PLH}$	0.041	$0.032 + 0.005 \cdot \text{SL}$	$0.040 + 0.003 \cdot \text{SL}$	$0.057 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.043	$0.035 + 0.004 \cdot \text{SL}$	$0.042 + 0.002 \cdot \text{SL}$	$0.059 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### IVCD44

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.126	$0.114 + 0.006 \cdot \text{SL}$	$0.111 + 0.007 \cdot \text{SL}$	$0.096 + 0.007 \cdot \text{SL}$
	$t_F$	0.113	$0.102 + 0.006 \cdot \text{SL}$	$0.102 + 0.006 \cdot \text{SL}$	$0.086 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.069	$0.059 + 0.005 \cdot \text{SL}$	$0.064 + 0.004 \cdot \text{SL}$	$0.074 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.067	$0.056 + 0.005 \cdot \text{SL}$	$0.061 + 0.004 \cdot \text{SL}$	$0.071 + 0.003 \cdot \text{SL}$
Y to YN	$t_R$	0.080	$0.066 + 0.007 \cdot \text{SL}$	$0.071 + 0.006 \cdot \text{SL}$	$0.057 + 0.006 \cdot \text{SL}$
	$t_F$	0.089	$0.074 + 0.008 \cdot \text{SL}$	$0.078 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.045	$0.032 + 0.006 \cdot \text{SL}$	$0.040 + 0.004 \cdot \text{SL}$	$0.058 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.047	$0.035 + 0.006 \cdot \text{SL}$	$0.043 + 0.004 \cdot \text{SL}$	$0.060 + 0.003 \cdot \text{SL}$

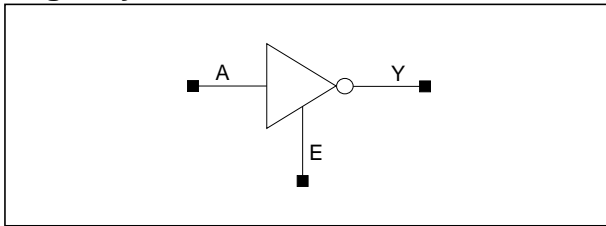
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# IVT/IVTD2/IVTD4/IVTD8/IVTD16

## Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X/16X Drive

### Logic Symbol



### Truth Table

A	E	Y
x	0	Hi-Z
0	1	1
1	1	0

### Cell Data

Input Load (SL)										Output Load (SL)				
IVT		IVTD2		IVTD4		IVTD8		IVTD16		IVT	IVTD2	IVTD4	IVTD8	IVTD16
A	E	A	E	A	E	A	E	A	E	Y	Y	Y	Y	Y
0.5	1.3	0.5	1.3	0.5	1.3	1.0	3.0	1.0	3.0	0.9	1.1	2.2	4.4	8.5
Gate Count														
IVT		IVTD2		IVTD4		IVTD8		IVTD16						
3.00		3.33		3.67		6.00		8.33						

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### IVT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.115	$0.056 + 0.029 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$	$0.049 + 0.031 \cdot \text{SL}$
	$t_F$	0.111	$0.055 + 0.028 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$	$0.057 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.252	$0.221 + 0.015 \cdot \text{SL}$	$0.227 + 0.014 \cdot \text{SL}$	$0.229 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.268	$0.231 + 0.019 \cdot \text{SL}$	$0.242 + 0.016 \cdot \text{SL}$	$0.250 + 0.015 \cdot \text{SL}$
E to Y	$t_R$	0.134	$0.069 + 0.032 \cdot \text{SL}$	$0.064 + 0.034 \cdot \text{SL}$	$0.057 + 0.034 \cdot \text{SL}$
	$t_F$	0.126	$0.068 + 0.029 \cdot \text{SL}$	$0.069 + 0.029 \cdot \text{SL}$	$0.064 + 0.029 \cdot \text{SL}$
	$t_{PLH}$	0.136	$0.103 + 0.016 \cdot \text{SL}$	$0.112 + 0.014 \cdot \text{SL}$	$0.115 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.220	$0.182 + 0.019 \cdot \text{SL}$	$0.194 + 0.016 \cdot \text{SL}$	$0.202 + 0.015 \cdot \text{SL}$
	$t_{PLZ}$	0.183	$0.183 + 0.000 \cdot \text{SL}$	$0.183 + 0.000 \cdot \text{SL}$	$0.183 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.138	$0.138 + 0.000 \cdot \text{SL}$	$0.138 + 0.000 \cdot \text{SL}$	$0.138 + 0.000 \cdot \text{SL}$

\*Group1 : SL < 4, \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### IVTD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.051 + 0.016 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.079	$0.047 + 0.016 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.246	$0.228 + 0.009 \cdot \text{SL}$	$0.235 + 0.008 \cdot \text{SL}$	$0.244 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.254	$0.232 + 0.011 \cdot \text{SL}$	$0.242 + 0.009 \cdot \text{SL}$	$0.258 + 0.008 \cdot \text{SL}$
E to Y	$t_R$	0.094	$0.062 + 0.016 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$	$0.054 + 0.016 \cdot \text{SL}$
	$t_F$	0.087	$0.054 + 0.017 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.129	$0.107 + 0.011 \cdot \text{SL}$	$0.119 + 0.008 \cdot \text{SL}$	$0.130 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.201	$0.176 + 0.012 \cdot \text{SL}$	$0.189 + 0.009 \cdot \text{SL}$	$0.208 + 0.008 \cdot \text{SL}$
	$t_{PLZ}$	0.197	$0.197 + 0.000 \cdot \text{SL}$	$0.197 + 0.000 \cdot \text{SL}$	$0.197 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.167	$0.167 + 0.000 \cdot \text{SL}$	$0.167 + 0.000 \cdot \text{SL}$	$0.167 + 0.000 \cdot \text{SL}$

\*Group1 : SL < 4, \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# IVT/IVTD2/IVTD4/IVTD8/IVTD16

## Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### IVTD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.076	$0.058 + 0.009 \cdot \text{SL}$	$0.064 + 0.008 \cdot \text{SL}$	$0.066 + 0.008 \cdot \text{SL}$
	$t_F$	0.077	$0.062 + 0.008 \cdot \text{SL}$	$0.065 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.265	$0.253 + 0.006 \cdot \text{SL}$	$0.259 + 0.004 \cdot \text{SL}$	$0.277 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.270	$0.257 + 0.006 \cdot \text{SL}$	$0.263 + 0.005 \cdot \text{SL}$	$0.283 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.089	$0.069 + 0.010 \cdot \text{SL}$	$0.080 + 0.007 \cdot \text{SL}$	$0.073 + 0.008 \cdot \text{SL}$
	$t_F$	0.079	$0.060 + 0.010 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.143	$0.129 + 0.007 \cdot \text{SL}$	$0.139 + 0.005 \cdot \text{SL}$	$0.163 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.210	$0.194 + 0.008 \cdot \text{SL}$	$0.205 + 0.005 \cdot \text{SL}$	$0.234 + 0.004 \cdot \text{SL}$
	$t_{PLZ}$	0.222	$0.222 + 0.000 \cdot \text{SL}$	$0.222 + 0.000 \cdot \text{SL}$	$0.222 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.221	$0.221 + 0.000 \cdot \text{SL}$	$0.222 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$

#### IVTD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.062	$0.054 + 0.004 \cdot \text{SL}$	$0.056 + 0.004 \cdot \text{SL}$	$0.046 + 0.004 \cdot \text{SL}$
	$t_F$	0.060	$0.053 + 0.004 \cdot \text{SL}$	$0.055 + 0.003 \cdot \text{SL}$	$0.054 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.241	$0.236 + 0.003 \cdot \text{SL}$	$0.239 + 0.002 \cdot \text{SL}$	$0.254 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.260	$0.254 + 0.003 \cdot \text{SL}$	$0.257 + 0.002 \cdot \text{SL}$	$0.282 + 0.002 \cdot \text{SL}$
E to Y	$t_R$	0.068	$0.060 + 0.004 \cdot \text{SL}$	$0.061 + 0.004 \cdot \text{SL}$	$0.050 + 0.004 \cdot \text{SL}$
	$t_F$	0.059	$0.050 + 0.004 \cdot \text{SL}$	$0.054 + 0.003 \cdot \text{SL}$	$0.057 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.112	$0.105 + 0.004 \cdot \text{SL}$	$0.112 + 0.002 \cdot \text{SL}$	$0.136 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.192	$0.184 + 0.004 \cdot \text{SL}$	$0.191 + 0.002 \cdot \text{SL}$	$0.224 + 0.002 \cdot \text{SL}$
	$t_{PLZ}$	0.223	$0.223 + 0.000 \cdot \text{SL}$	$0.223 + 0.000 \cdot \text{SL}$	$0.223 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.172	$0.172 + 0.000 \cdot \text{SL}$	$0.173 + 0.000 \cdot \text{SL}$	$0.172 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### IVTD16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.071	$0.066 + 0.002 \cdot \text{SL}$	$0.067 + 0.002 \cdot \text{SL}$	$0.074 + 0.002 \cdot \text{SL}$
	$t_F$	0.081	$0.078 + 0.002 \cdot \text{SL}$	$0.078 + 0.002 \cdot \text{SL}$	$0.080 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.277	$0.274 + 0.002 \cdot \text{SL}$	$0.276 + 0.001 \cdot \text{SL}$	$0.297 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.297	$0.293 + 0.002 \cdot \text{SL}$	$0.295 + 0.001 \cdot \text{SL}$	$0.316 + 0.001 \cdot \text{SL}$
E to Y	$t_R$	0.078	$0.073 + 0.002 \cdot \text{SL}$	$0.074 + 0.002 \cdot \text{SL}$	$0.082 + 0.002 \cdot \text{SL}$
	$t_F$	0.068	$0.062 + 0.003 \cdot \text{SL}$	$0.066 + 0.002 \cdot \text{SL}$	$0.085 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.140	$0.135 + 0.003 \cdot \text{SL}$	$0.140 + 0.001 \cdot \text{SL}$	$0.175 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.211	$0.206 + 0.003 \cdot \text{SL}$	$0.211 + 0.002 \cdot \text{SL}$	$0.250 + 0.001 \cdot \text{SL}$
	$t_{PLZ}$	0.265	$0.264 + 0.000 \cdot \text{SL}$	$0.265 + 0.000 \cdot \text{SL}$	$0.265 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.250	$0.249 + 0.000 \cdot \text{SL}$	$0.251 + 0.000 \cdot \text{SL}$	$0.251 + 0.000 \cdot \text{SL}$

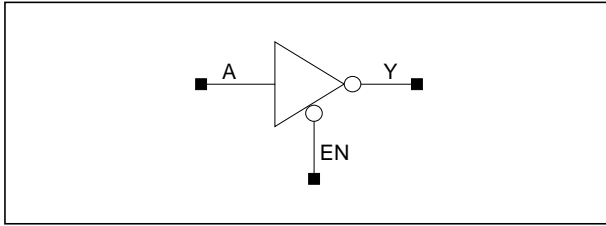
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$



# IVTN/IVTND2/IVTND4/IVTND8/IVTND16

## Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X/16X Drive

### Logic Symbol



### Truth Table

A	EN	Y
x	1	Hi-Z
0	0	1
1	0	0

### Cell Data

Input Load (SL)										Output Load (SL)				
IVTN		IVTND2		IVTND4		IVTND8		IVTND16		IVTN	IVTND2	IVTND4	IVTND8	IVTND16
A	EN	A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y	Y
0.5	1.1	0.5	1.1	0.5	1.1	1.0	2.1	1.0	2.1	0.9	1.1	2.2	4.4	8.4
Gate Count														
IVTN		IVTND2		IVTND4		IVTND8		IVTND16						
3.00		3.33		3.67		6.00		8.33						

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### IVTN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.116	$0.056 + 0.030 \cdot \text{SL}$	$0.054 + 0.030 \cdot \text{SL}$	$0.049 + 0.031 \cdot \text{SL}$
	$t_F$	0.111	$0.057 + 0.027 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$	$0.055 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.252	$0.222 + 0.015 \cdot \text{SL}$	$0.227 + 0.014 \cdot \text{SL}$	$0.230 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.266	$0.229 + 0.018 \cdot \text{SL}$	$0.240 + 0.016 \cdot \text{SL}$	$0.248 + 0.015 \cdot \text{SL}$
EN to Y	$t_R$	0.131	$0.066 + 0.033 \cdot \text{SL}$	$0.061 + 0.034 \cdot \text{SL}$	$0.056 + 0.034 \cdot \text{SL}$
	$t_F$	0.126	$0.068 + 0.029 \cdot \text{SL}$	$0.071 + 0.028 \cdot \text{SL}$	$0.065 + 0.029 \cdot \text{SL}$
	$t_{PLH}$	0.216	$0.184 + 0.016 \cdot \text{SL}$	$0.191 + 0.014 \cdot \text{SL}$	$0.194 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.166	$0.128 + 0.019 \cdot \text{SL}$	$0.140 + 0.016 \cdot \text{SL}$	$0.149 + 0.015 \cdot \text{SL}$
	$t_{PLZ}$	0.099	$0.099 + 0.000 \cdot \text{SL}$	$0.099 + 0.000 \cdot \text{SL}$	$0.099 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.193	$0.193 + 0.000 \cdot \text{SL}$	$0.193 + 0.000 \cdot \text{SL}$	$0.193 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### IVTND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.051 + 0.015 \cdot \text{SL}$	$0.052 + 0.015 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.079	$0.048 + 0.015 \cdot \text{SL}$	$0.055 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.247	$0.228 + 0.009 \cdot \text{SL}$	$0.235 + 0.008 \cdot \text{SL}$	$0.245 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.252	$0.230 + 0.011 \cdot \text{SL}$	$0.239 + 0.009 \cdot \text{SL}$	$0.255 + 0.008 \cdot \text{SL}$
EN to Y	$t_R$	0.090	$0.059 + 0.016 \cdot \text{SL}$	$0.059 + 0.016 \cdot \text{SL}$	$0.053 + 0.016 \cdot \text{SL}$
	$t_F$	0.092	$0.063 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.207	$0.186 + 0.010 \cdot \text{SL}$	$0.197 + 0.008 \cdot \text{SL}$	$0.208 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.148	$0.123 + 0.012 \cdot \text{SL}$	$0.137 + 0.009 \cdot \text{SL}$	$0.155 + 0.008 \cdot \text{SL}$
	$t_{PLZ}$	0.115	$0.115 + 0.000 \cdot \text{SL}$	$0.115 + 0.000 \cdot \text{SL}$	$0.116 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.221	$0.221 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# IVTN/IVTND2/IVTND4/IVTND8/IVTND16

## Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### IVTND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.076	$0.058 + 0.009 \cdot \text{SL}$	$0.064 + 0.008 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$
	$t_F$	0.078	$0.063 + 0.008 \cdot \text{SL}$	$0.066 + 0.007 \cdot \text{SL}$	$0.072 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.267	$0.255 + 0.006 \cdot \text{SL}$	$0.261 + 0.004 \cdot \text{SL}$	$0.279 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.270	$0.257 + 0.006 \cdot \text{SL}$	$0.263 + 0.005 \cdot \text{SL}$	$0.283 + 0.004 \cdot \text{SL}$
EN to Y	$t_R$	0.086	$0.068 + 0.009 \cdot \text{SL}$	$0.073 + 0.008 \cdot \text{SL}$	$0.073 + 0.008 \cdot \text{SL}$
	$t_F$	0.082	$0.064 + 0.009 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.083 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	0.221	$0.206 + 0.007 \cdot \text{SL}$	$0.217 + 0.005 \cdot \text{SL}$	$0.240 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.154	$0.138 + 0.008 \cdot \text{SL}$	$0.150 + 0.005 \cdot \text{SL}$	$0.179 + 0.004 \cdot \text{SL}$
	$t_{PLZ}$	0.145	$0.145 + 0.000 \cdot \text{SL}$	$0.145 + 0.000 \cdot \text{SL}$	$0.145 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.275	$0.275 + 0.000 \cdot \text{SL}$	$0.276 + 0.000 \cdot \text{SL}$	$0.275 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$

#### IVTND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.062	$0.053 + 0.004 \cdot \text{SL}$	$0.056 + 0.004 \cdot \text{SL}$	$0.048 + 0.004 \cdot \text{SL}$
	$t_F$	0.061	$0.053 + 0.004 \cdot \text{SL}$	$0.055 + 0.003 \cdot \text{SL}$	$0.054 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.244	$0.239 + 0.003 \cdot \text{SL}$	$0.242 + 0.002 \cdot \text{SL}$	$0.259 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.258	$0.252 + 0.003 \cdot \text{SL}$	$0.256 + 0.002 \cdot \text{SL}$	$0.280 + 0.002 \cdot \text{SL}$
EN to Y	$t_R$	0.067	$0.058 + 0.005 \cdot \text{SL}$	$0.061 + 0.004 \cdot \text{SL}$	$0.050 + 0.004 \cdot \text{SL}$
	$t_F$	0.063	$0.053 + 0.005 \cdot \text{SL}$	$0.059 + 0.003 \cdot \text{SL}$	$0.059 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.206 + 0.004 \cdot \text{SL}$	$0.213 + 0.002 \cdot \text{SL}$	$0.237 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.121	$0.113 + 0.004 \cdot \text{SL}$	$0.120 + 0.002 \cdot \text{SL}$	$0.154 + 0.002 \cdot \text{SL}$
	$t_{PLZ}$	0.122	$0.122 + 0.000 \cdot \text{SL}$	$0.122 + 0.000 \cdot \text{SL}$	$0.122 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.255	$0.254 + 0.000 \cdot \text{SL}$	$0.255 + 0.000 \cdot \text{SL}$	$0.255 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### IVTND16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.070	$0.065 + 0.002 \cdot \text{SL}$	$0.067 + 0.002 \cdot \text{SL}$	$0.074 + 0.002 \cdot \text{SL}$
	$t_F$	0.081	$0.077 + 0.002 \cdot \text{SL}$	$0.077 + 0.002 \cdot \text{SL}$	$0.080 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.279	$0.275 + 0.002 \cdot \text{SL}$	$0.277 + 0.001 \cdot \text{SL}$	$0.298 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.295	$0.291 + 0.002 \cdot \text{SL}$	$0.293 + 0.001 \cdot \text{SL}$	$0.314 + 0.001 \cdot \text{SL}$
EN to Y	$t_R$	0.075	$0.070 + 0.003 \cdot \text{SL}$	$0.072 + 0.002 \cdot \text{SL}$	$0.082 + 0.002 \cdot \text{SL}$
	$t_F$	0.070	$0.064 + 0.003 \cdot \text{SL}$	$0.067 + 0.002 \cdot \text{SL}$	$0.087 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.240	$0.234 + 0.003 \cdot \text{SL}$	$0.240 + 0.001 \cdot \text{SL}$	$0.275 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.143	$0.137 + 0.003 \cdot \text{SL}$	$0.142 + 0.002 \cdot \text{SL}$	$0.181 + 0.001 \cdot \text{SL}$
	$t_{PLZ}$	0.165	$0.165 + 0.000 \cdot \text{SL}$	$0.165 + 0.000 \cdot \text{SL}$	$0.165 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.332	$0.332 + 0.000 \cdot \text{SL}$	$0.333 + 0.000 \cdot \text{SL}$	$0.333 + 0.000 \cdot \text{SL}$

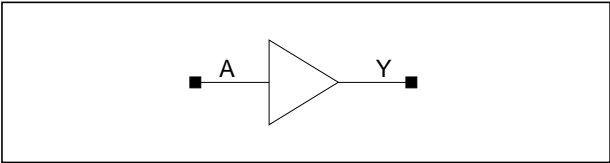
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$



NIDH/NID/NID2/NID3/NID4/NID6/NID8/NID16

Non-Inverting Buffer with 0.5X/1X/2X/3X/4X/6X/8X/16X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)							
NIDH	NID	NID2	NID3	NID4	NID6	NID8	NID16
A	A	A	A	A	A	A	A
0.6	0.6	0.7	0.8	1.0	1.4	1.9	3.9
Gate Count							
NIDH	NID	NID2	NID3	NID4	NID6	NID8	NID16
1.00	1.00	1.33	1.67	2.00	2.67	3.33	6.33



# NIDH/NID/NID2/NID3/NID4/NID6/NID8/NID16

## Non-Inverting Buffer with 0.5X/1X/2X/3X/4X/6X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NIDH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.197	$0.062 + 0.067 \cdot \text{SL}$	$0.056 + 0.069 \cdot \text{SL}$	$0.050 + 0.070 \cdot \text{SL}$
	$t_F$	0.157	$0.058 + 0.050 \cdot \text{SL}$	$0.050 + 0.052 \cdot \text{SL}$	$0.044 + 0.052 \cdot \text{SL}$
	$t_{PLH}$	0.178	$0.117 + 0.030 \cdot \text{SL}$	$0.119 + 0.030 \cdot \text{SL}$	$0.119 + 0.030 \cdot \text{SL}$
	$t_{PHL}$	0.189	$0.131 + 0.029 \cdot \text{SL}$	$0.137 + 0.027 \cdot \text{SL}$	$0.138 + 0.027 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### NID

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.119	$0.063 + 0.028 \cdot \text{SL}$	$0.059 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$
	$t_F$	0.109	$0.060 + 0.025 \cdot \text{SL}$	$0.058 + 0.025 \cdot \text{SL}$	$0.052 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.158	$0.129 + 0.014 \cdot \text{SL}$	$0.133 + 0.013 \cdot \text{SL}$	$0.135 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.166	$0.135 + 0.016 \cdot \text{SL}$	$0.141 + 0.014 \cdot \text{SL}$	$0.145 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### NID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.088	$0.059 + 0.014 \cdot \text{SL}$	$0.059 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.057 + 0.012 \cdot \text{SL}$	$0.057 + 0.012 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.163	$0.146 + 0.009 \cdot \text{SL}$	$0.152 + 0.007 \cdot \text{SL}$	$0.158 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.163	$0.144 + 0.010 \cdot \text{SL}$	$0.152 + 0.008 \cdot \text{SL}$	$0.162 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### NID3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.083	$0.064 + 0.010 \cdot \text{SL}$	$0.064 + 0.010 \cdot \text{SL}$	$0.052 + 0.010 \cdot \text{SL}$
	$t_F$	0.078	$0.061 + 0.009 \cdot \text{SL}$	$0.060 + 0.009 \cdot \text{SL}$	$0.055 + 0.009 \cdot \text{SL}$
	$t_{PLH}$	0.161	$0.149 + 0.006 \cdot \text{SL}$	$0.153 + 0.005 \cdot \text{SL}$	$0.162 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.164	$0.150 + 0.007 \cdot \text{SL}$	$0.156 + 0.005 \cdot \text{SL}$	$0.169 + 0.005 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# NIDH/NID/NID2/NID3/NID4/NID6/NID8/NID16

## Non-Inverting Buffer with 0.5X/1X/2X/3X/4X/6X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NID4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.077	$0.063 + 0.007 \cdot \text{SL}$	$0.061 + 0.007 \cdot \text{SL}$	$0.055 + 0.008 \cdot \text{SL}$
	$t_F$	0.072	$0.059 + 0.006 \cdot \text{SL}$	$0.060 + 0.006 \cdot \text{SL}$	$0.057 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.160	$0.151 + 0.005 \cdot \text{SL}$	$0.154 + 0.004 \cdot \text{SL}$	$0.164 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.159	$0.149 + 0.005 \cdot \text{SL}$	$0.154 + 0.004 \cdot \text{SL}$	$0.167 + 0.003 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$

#### NID6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.069	$0.061 + 0.004 \cdot \text{SL}$	$0.059 + 0.005 \cdot \text{SL}$	$0.040 + 0.005 \cdot \text{SL}$
	$t_F$	0.066	$0.057 + 0.005 \cdot \text{SL}$	$0.058 + 0.004 \cdot \text{SL}$	$0.043 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.149	$0.142 + 0.003 \cdot \text{SL}$	$0.146 + 0.002 \cdot \text{SL}$	$0.157 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.152	$0.144 + 0.004 \cdot \text{SL}$	$0.150 + 0.003 \cdot \text{SL}$	$0.167 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### NID8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.070	$0.062 + 0.004 \cdot \text{SL}$	$0.064 + 0.004 \cdot \text{SL}$	$0.042 + 0.004 \cdot \text{SL}$
	$t_F$	0.061	$0.054 + 0.004 \cdot \text{SL}$	$0.056 + 0.003 \cdot \text{SL}$	$0.045 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.144	$0.139 + 0.003 \cdot \text{SL}$	$0.142 + 0.002 \cdot \text{SL}$	$0.154 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.145	$0.139 + 0.003 \cdot \text{SL}$	$0.144 + 0.002 \cdot \text{SL}$	$0.162 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### NID16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.061	$0.057 + 0.002 \cdot \text{SL}$	$0.058 + 0.002 \cdot \text{SL}$	$0.049 + 0.002 \cdot \text{SL}$
	$t_F$	0.057	$0.053 + 0.002 \cdot \text{SL}$	$0.056 + 0.002 \cdot \text{SL}$	$0.054 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.140	$0.137 + 0.001 \cdot \text{SL}$	$0.139 + 0.001 \cdot \text{SL}$	$0.149 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.143	$0.140 + 0.002 \cdot \text{SL}$	$0.142 + 0.001 \cdot \text{SL}$	$0.158 + 0.001 \cdot \text{SL}$

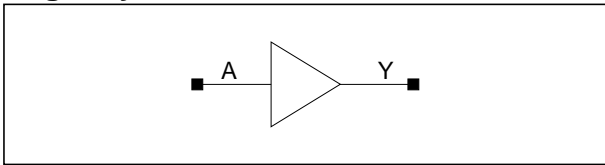
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$



## OAK\_NID10P/OAK\_NID20P

### Clock Buffer for 10pF/20pF Drive

#### Logic Symbol



#### Truth Table

A	Y
0	0
1	1

#### Cell Data

Input Load (SL)		Gate Count	
<i>OAK_NID10P</i>	<i>OAK_NID20P</i>	<i>OAK_NID10P</i>	<i>OAK_NID20P</i>
A	A	23.24	43.70
1.0	2.0		

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

##### OAK\_NID10P

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.064	$0.063 + 0.001 \cdot \text{SL}$	$0.050 + 0.001 \cdot \text{SL}$	$0.044 + 0.001 \cdot \text{SL}$
	$t_F$	0.048	$0.047 + 0.001 \cdot \text{SL}$	$0.037 + 0.001 \cdot \text{SL}$	$0.034 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	0.385	$0.384 + 0.000 \cdot \text{SL}$	$0.391 + 0.000 \cdot \text{SL}$	$0.391 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	0.298	$0.298 + 0.000 \cdot \text{SL}$	$0.302 + 0.000 \cdot \text{SL}$	$0.302 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 596$ , \*Group2 :  $596 \leq \text{SL} \leq 894$ , \*Group3 :  $894 < \text{SL}$

##### OAK\_NID20P

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.067	$0.066 + 0.000 \cdot \text{SL}$	$0.055 + 0.000 \cdot \text{SL}$	$0.046 + 0.000 \cdot \text{SL}$
	$t_F$	0.050	$0.049 + 0.000 \cdot \text{SL}$	$0.041 + 0.000 \cdot \text{SL}$	$0.035 + 0.000 \cdot \text{SL}$
	$t_{PLH}$	0.371	$0.371 + 0.000 \cdot \text{SL}$	$0.382 + 0.000 \cdot \text{SL}$	$0.383 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	0.285	$0.285 + 0.000 \cdot \text{SL}$	$0.293 + 0.000 \cdot \text{SL}$	$0.294 + 0.000 \cdot \text{SL}$

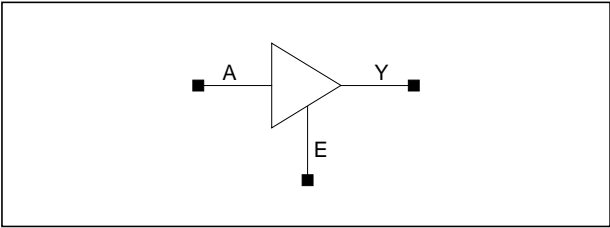
\*Group1 :  $\text{SL} < 745$ , \*Group2 :  $745 \leq \text{SL} \leq 1490$ , \*Group3 :  $1490 < \text{SL}$



NIT/NITD2/NITD4/NITD8/NITD16

Non-Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X/16X Drive

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	0
1	1	1

Cell Data

Input Load (SL)										Output Load (SL)				
NIT		NITD2		NITD4		NITD8		NITD16		NIT	NITD2	NITD4	NITD8	NITD16
A	E	A	E	A	E	A	E	A	E	Y	Y	Y	Y	Y
1.7	1.2	1.7	1.2	1.7	1.2	4.6	2.5	4.6	2.5	0.9	1.1	2.2	4.4	8.5
Gate Count														
NIT		NITD2		NITD4		NITD8		NITD16						
2.67		3.00		3.33		5.67		8.00						



# NIT/NITD2/NITD4/NITD8/NITD16

## Non-Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.116	$0.059 + 0.029 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$	$0.049 + 0.031 \cdot \text{SL}$
	$t_F$	0.112	$0.057 + 0.028 \cdot \text{SL}$	$0.060 + 0.027 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.134	$0.103 + 0.015 \cdot \text{SL}$	$0.109 + 0.014 \cdot \text{SL}$	$0.112 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.171	$0.135 + 0.018 \cdot \text{SL}$	$0.145 + 0.016 \cdot \text{SL}$	$0.153 + 0.015 \cdot \text{SL}$
E to Y	$t_R$	0.133	$0.069 + 0.032 \cdot \text{SL}$	$0.064 + 0.033 \cdot \text{SL}$	$0.056 + 0.034 \cdot \text{SL}$
	$t_F$	0.124	$0.065 + 0.030 \cdot \text{SL}$	$0.069 + 0.029 \cdot \text{SL}$	$0.063 + 0.029 \cdot \text{SL}$
	$t_{PLH}$	0.136	$0.103 + 0.016 \cdot \text{SL}$	$0.111 + 0.014 \cdot \text{SL}$	$0.115 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.219	$0.181 + 0.019 \cdot \text{SL}$	$0.193 + 0.016 \cdot \text{SL}$	$0.202 + 0.015 \cdot \text{SL}$
	$t_{PLZ}$	0.180	$0.180 + 0.000 \cdot \text{SL}$	$0.180 + 0.000 \cdot \text{SL}$	$0.180 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.138	$0.138 + 0.000 \cdot \text{SL}$	$0.138 + 0.000 \cdot \text{SL}$	$0.138 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### NITD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.051 + 0.016 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.051 + 0.015 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.129	$0.110 + 0.009 \cdot \text{SL}$	$0.117 + 0.007 \cdot \text{SL}$	$0.125 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.158	$0.137 + 0.011 \cdot \text{SL}$	$0.146 + 0.009 \cdot \text{SL}$	$0.161 + 0.007 \cdot \text{SL}$
E to Y	$t_R$	0.093	$0.062 + 0.015 \cdot \text{SL}$	$0.063 + 0.015 \cdot \text{SL}$	$0.054 + 0.016 \cdot \text{SL}$
	$t_F$	0.087	$0.054 + 0.016 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.128	$0.107 + 0.011 \cdot \text{SL}$	$0.118 + 0.008 \cdot \text{SL}$	$0.129 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.201	$0.176 + 0.012 \cdot \text{SL}$	$0.189 + 0.009 \cdot \text{SL}$	$0.208 + 0.008 \cdot \text{SL}$
	$t_{PLZ}$	0.194	$0.194 + 0.000 \cdot \text{SL}$	$0.194 + 0.000 \cdot \text{SL}$	$0.194 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.166	$0.165 + 0.000 \cdot \text{SL}$	$0.166 + 0.000 \cdot \text{SL}$	$0.165 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### NITD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.079	$0.066 + 0.007 \cdot \text{SL}$	$0.062 + 0.008 \cdot \text{SL}$	$0.064 + 0.008 \cdot \text{SL}$
	$t_F$	0.078	$0.063 + 0.008 \cdot \text{SL}$	$0.067 + 0.007 \cdot \text{SL}$	$0.074 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.148	$0.137 + 0.006 \cdot \text{SL}$	$0.142 + 0.004 \cdot \text{SL}$	$0.159 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.164 + 0.006 \cdot \text{SL}$	$0.170 + 0.005 \cdot \text{SL}$	$0.189 + 0.004 \cdot \text{SL}$
E to Y	$t_R$	0.086	$0.068 + 0.009 \cdot \text{SL}$	$0.074 + 0.008 \cdot \text{SL}$	$0.073 + 0.008 \cdot \text{SL}$
	$t_F$	0.079	$0.061 + 0.009 \cdot \text{SL}$	$0.069 + 0.007 \cdot \text{SL}$	$0.082 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.143	$0.128 + 0.007 \cdot \text{SL}$	$0.139 + 0.005 \cdot \text{SL}$	$0.162 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.207	$0.191 + 0.008 \cdot \text{SL}$	$0.203 + 0.005 \cdot \text{SL}$	$0.232 + 0.004 \cdot \text{SL}$
	$t_{PLZ}$	0.221	$0.221 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.220	$0.219 + 0.000 \cdot \text{SL}$	$0.220 + 0.000 \cdot \text{SL}$	$0.220 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# NIT/NITD2/NITD4/NITD8/NITD16

## Non-Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NITD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.062	$0.054 + 0.004 \cdot \text{SL}$	$0.056 + 0.004 \cdot \text{SL}$	$0.046 + 0.004 \cdot \text{SL}$
	$t_F$	0.063	$0.057 + 0.003 \cdot \text{SL}$	$0.056 + 0.003 \cdot \text{SL}$	$0.054 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.120	$0.115 + 0.003 \cdot \text{SL}$	$0.118 + 0.002 \cdot \text{SL}$	$0.132 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.141	$0.135 + 0.003 \cdot \text{SL}$	$0.138 + 0.002 \cdot \text{SL}$	$0.161 + 0.002 \cdot \text{SL}$
E to Y	$t_R$	0.068	$0.060 + 0.004 \cdot \text{SL}$	$0.061 + 0.004 \cdot \text{SL}$	$0.050 + 0.004 \cdot \text{SL}$
	$t_F$	0.059	$0.051 + 0.004 \cdot \text{SL}$	$0.054 + 0.003 \cdot \text{SL}$	$0.058 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.113	$0.105 + 0.004 \cdot \text{SL}$	$0.112 + 0.002 \cdot \text{SL}$	$0.136 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.192	$0.184 + 0.004 \cdot \text{SL}$	$0.191 + 0.002 \cdot \text{SL}$	$0.224 + 0.002 \cdot \text{SL}$
	$t_{PLZ}$	0.221	$0.221 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.173	$0.173 + 0.000 \cdot \text{SL}$	$0.173 + 0.000 \cdot \text{SL}$	$0.173 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### NITD16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.069	$0.060 + 0.004 \cdot \text{SL}$	$0.071 + 0.002 \cdot \text{SL}$	$0.073 + 0.002 \cdot \text{SL}$
	$t_F$	0.080	$0.076 + 0.002 \cdot \text{SL}$	$0.076 + 0.002 \cdot \text{SL}$	$0.080 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.153	$0.150 + 0.001 \cdot \text{SL}$	$0.151 + 0.001 \cdot \text{SL}$	$0.172 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.178	$0.174 + 0.002 \cdot \text{SL}$	$0.176 + 0.001 \cdot \text{SL}$	$0.196 + 0.001 \cdot \text{SL}$
E to Y	$t_R$	0.078	$0.073 + 0.002 \cdot \text{SL}$	$0.074 + 0.002 \cdot \text{SL}$	$0.081 + 0.002 \cdot \text{SL}$
	$t_F$	0.068	$0.062 + 0.003 \cdot \text{SL}$	$0.066 + 0.002 \cdot \text{SL}$	$0.085 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.140	$0.135 + 0.003 \cdot \text{SL}$	$0.140 + 0.001 \cdot \text{SL}$	$0.175 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.212	$0.207 + 0.003 \cdot \text{SL}$	$0.211 + 0.002 \cdot \text{SL}$	$0.250 + 0.001 \cdot \text{SL}$
	$t_{PLZ}$	0.265	$0.265 + 0.000 \cdot \text{SL}$	$0.265 + 0.000 \cdot \text{SL}$	$0.265 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.250	$0.250 + 0.000 \cdot \text{SL}$	$0.251 + 0.000 \cdot \text{SL}$	$0.251 + 0.000 \cdot \text{SL}$

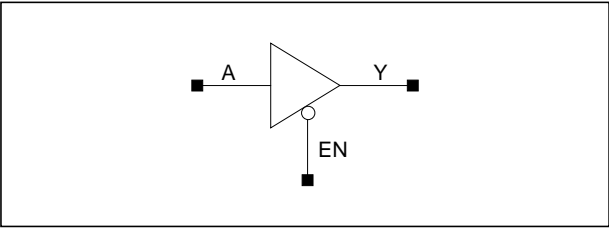
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$



NITN/NITND2/NITND4/NITND8/NITND16

Non-Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X/16X Drive

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	0
1	0	1

Cell Data

Input Load (SL)										Output Load (SL)				
NITN		NITND2		NITND4		NITND8		NITND16		NITN	NITND2	NITND4	NITND8	NITND16
A	EN	A	EN	A	EN	A	EN	A	EN	Y	Y	Y	Y	Y
1.7	1.3	1.7	1.3	1.7	1.3	4.6	2.7	4.5	2.7	0.9	1.1	2.3	4.4	8.4
Gate Count														
NITN				NITND2				NITND4				NITND8		NITND16
2.67				3.00				3.33				5.67		8.00



# NITN/NITND2/NITND4/NITND8/NITND16

## Non-Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NITN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.117	$0.059 + 0.029 \cdot \text{SL}$	$0.053 + 0.030 \cdot \text{SL}$	$0.049 + 0.031 \cdot \text{SL}$
	$t_F$	0.113	$0.059 + 0.027 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.135	$0.104 + 0.015 \cdot \text{SL}$	$0.110 + 0.014 \cdot \text{SL}$	$0.112 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.170	$0.134 + 0.018 \cdot \text{SL}$	$0.144 + 0.016 \cdot \text{SL}$	$0.152 + 0.015 \cdot \text{SL}$
EN to Y	$t_R$	0.130	$0.063 + 0.033 \cdot \text{SL}$	$0.061 + 0.034 \cdot \text{SL}$	$0.055 + 0.035 \cdot \text{SL}$
	$t_F$	0.127	$0.069 + 0.029 \cdot \text{SL}$	$0.071 + 0.028 \cdot \text{SL}$	$0.064 + 0.029 \cdot \text{SL}$
	$t_{PLH}$	0.212	$0.180 + 0.016 \cdot \text{SL}$	$0.187 + 0.014 \cdot \text{SL}$	$0.190 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.167	$0.129 + 0.019 \cdot \text{SL}$	$0.141 + 0.016 \cdot \text{SL}$	$0.150 + 0.015 \cdot \text{SL}$
	$t_{PLZ}$	0.100	$0.100 + 0.000 \cdot \text{SL}$	$0.100 + 0.000 \cdot \text{SL}$	$0.100 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.194	$0.194 + 0.000 \cdot \text{SL}$	$0.194 + 0.000 \cdot \text{SL}$	$0.194 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### NITND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.082	$0.050 + 0.016 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$	$0.048 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.057 + 0.013 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.129	$0.111 + 0.009 \cdot \text{SL}$	$0.118 + 0.008 \cdot \text{SL}$	$0.127 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.157	$0.136 + 0.011 \cdot \text{SL}$	$0.145 + 0.009 \cdot \text{SL}$	$0.159 + 0.008 \cdot \text{SL}$
EN to Y	$t_R$	0.090	$0.059 + 0.016 \cdot \text{SL}$	$0.059 + 0.016 \cdot \text{SL}$	$0.053 + 0.016 \cdot \text{SL}$
	$t_F$	0.092	$0.063 + 0.014 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$	$0.065 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.209	$0.188 + 0.010 \cdot \text{SL}$	$0.199 + 0.008 \cdot \text{SL}$	$0.210 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.148	$0.123 + 0.012 \cdot \text{SL}$	$0.136 + 0.009 \cdot \text{SL}$	$0.155 + 0.008 \cdot \text{SL}$
	$t_{PLZ}$	0.115	$0.115 + 0.000 \cdot \text{SL}$	$0.115 + 0.000 \cdot \text{SL}$	$0.115 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.221	$0.221 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$	$0.221 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### NITND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.076	$0.059 + 0.009 \cdot \text{SL}$	$0.062 + 0.008 \cdot \text{SL}$	$0.066 + 0.008 \cdot \text{SL}$
	$t_F$	0.079	$0.065 + 0.007 \cdot \text{SL}$	$0.068 + 0.007 \cdot \text{SL}$	$0.073 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.150	$0.138 + 0.006 \cdot \text{SL}$	$0.144 + 0.004 \cdot \text{SL}$	$0.162 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.176	$0.164 + 0.006 \cdot \text{SL}$	$0.170 + 0.005 \cdot \text{SL}$	$0.188 + 0.004 \cdot \text{SL}$
EN to Y	$t_R$	0.086	$0.069 + 0.009 \cdot \text{SL}$	$0.072 + 0.008 \cdot \text{SL}$	$0.073 + 0.008 \cdot \text{SL}$
	$t_F$	0.081	$0.064 + 0.009 \cdot \text{SL}$	$0.071 + 0.007 \cdot \text{SL}$	$0.084 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.220	$0.206 + 0.007 \cdot \text{SL}$	$0.216 + 0.005 \cdot \text{SL}$	$0.239 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.154	$0.138 + 0.008 \cdot \text{SL}$	$0.150 + 0.005 \cdot \text{SL}$	$0.179 + 0.004 \cdot \text{SL}$
	$t_{PLZ}$	0.146	$0.146 + 0.000 \cdot \text{SL}$	$0.147 + 0.000 \cdot \text{SL}$	$0.147 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.281	$0.281 + 0.000 \cdot \text{SL}$	$0.281 + 0.000 \cdot \text{SL}$	$0.281 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



# NITN/NITND2/NITND4/NITND8/NITND16

## Non-Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X/16X Drive

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### NITND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.061	$0.054 + 0.004 \cdot \text{SL}$	$0.054 + 0.004 \cdot \text{SL}$	$0.047 + 0.004 \cdot \text{SL}$
	$t_F$	0.064	$0.055 + 0.005 \cdot \text{SL}$	$0.061 + 0.003 \cdot \text{SL}$	$0.054 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.121	$0.116 + 0.003 \cdot \text{SL}$	$0.119 + 0.002 \cdot \text{SL}$	$0.134 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.140	$0.134 + 0.003 \cdot \text{SL}$	$0.137 + 0.002 \cdot \text{SL}$	$0.160 + 0.002 \cdot \text{SL}$
EN to Y	$t_R$	0.067	$0.059 + 0.004 \cdot \text{SL}$	$0.061 + 0.004 \cdot \text{SL}$	$0.050 + 0.004 \cdot \text{SL}$
	$t_F$	0.063	$0.053 + 0.005 \cdot \text{SL}$	$0.059 + 0.003 \cdot \text{SL}$	$0.058 + 0.003 \cdot \text{SL}$
	$t_{PLH}$	0.214	$0.206 + 0.004 \cdot \text{SL}$	$0.213 + 0.002 \cdot \text{SL}$	$0.237 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.121	$0.113 + 0.004 \cdot \text{SL}$	$0.120 + 0.002 \cdot \text{SL}$	$0.154 + 0.002 \cdot \text{SL}$
	$t_{PLZ}$	0.122	$0.122 + 0.000 \cdot \text{SL}$	$0.122 + 0.000 \cdot \text{SL}$	$0.122 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.255	$0.255 + 0.000 \cdot \text{SL}$	$0.255 + 0.000 \cdot \text{SL}$	$0.255 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### NITND16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.072	$0.067 + 0.003 \cdot \text{SL}$	$0.069 + 0.002 \cdot \text{SL}$	$0.074 + 0.002 \cdot \text{SL}$
	$t_F$	0.080	$0.076 + 0.002 \cdot \text{SL}$	$0.076 + 0.002 \cdot \text{SL}$	$0.078 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.153	$0.150 + 0.002 \cdot \text{SL}$	$0.151 + 0.001 \cdot \text{SL}$	$0.174 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.175	$0.171 + 0.002 \cdot \text{SL}$	$0.173 + 0.001 \cdot \text{SL}$	$0.192 + 0.001 \cdot \text{SL}$
EN to Y	$t_R$	0.076	$0.070 + 0.003 \cdot \text{SL}$	$0.074 + 0.002 \cdot \text{SL}$	$0.082 + 0.002 \cdot \text{SL}$
	$t_F$	0.067	$0.062 + 0.003 \cdot \text{SL}$	$0.065 + 0.002 \cdot \text{SL}$	$0.085 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.241	$0.236 + 0.003 \cdot \text{SL}$	$0.241 + 0.001 \cdot \text{SL}$	$0.277 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.140	$0.135 + 0.003 \cdot \text{SL}$	$0.139 + 0.002 \cdot \text{SL}$	$0.178 + 0.001 \cdot \text{SL}$
	$t_{PLZ}$	0.163	$0.163 + 0.000 \cdot \text{SL}$	$0.163 + 0.000 \cdot \text{SL}$	$0.163 + 0.000 \cdot \text{SL}$
	$t_{PHZ}$	0.333	$0.333 + 0.000 \cdot \text{SL}$	$0.334 + 0.000 \cdot \text{SL}$	$0.335 + 0.000 \cdot \text{SL}$

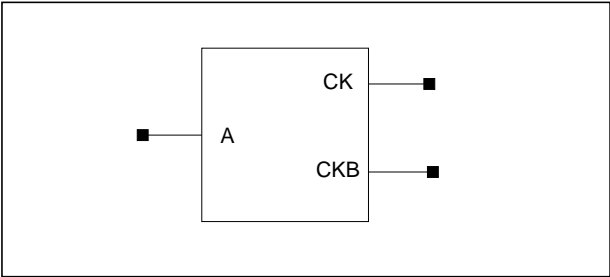
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$



OAK\_DUCLK10/OAK\_DUCLK16

2 Phase Clock Generator Buffer (1ns/1.6ns Non-overlapped)

Logic Symbol



Truth Table

A	CK	CKB
0	0	1
1	1	0

Cell Data

Input Load (SL)		Gate Count	
OAK_DUCLK10	OAK_DUCLK16	OAK_DUCLK10	OAK_DUCLK16
A	A	13.67	14.67
1.9	1.9		



## OAK\_DUCLK10/OAK\_DUCLK16

### 2 Phase Clock Generator Buffer (1ns/1.6ns Non-overlapped)

#### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### OAK\_DUCLK10

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to CK	$t_R$	0.079	$0.073 + 0.003 \cdot \text{SL}$	$0.070 + 0.004 \cdot \text{SL}$	$0.047 + 0.004 \cdot \text{SL}$
	$t_F$	0.081	$0.073 + 0.004 \cdot \text{SL}$	$0.074 + 0.004 \cdot \text{SL}$	$0.054 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	2.319	$2.313 + 0.003 \cdot \text{SL}$	$2.317 + 0.002 \cdot \text{SL}$	$2.331 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	1.349	$1.342 + 0.003 \cdot \text{SL}$	$1.347 + 0.002 \cdot \text{SL}$	$1.365 + 0.002 \cdot \text{SL}$
A to CKB	$t_R$	0.079	$0.071 + 0.004 \cdot \text{SL}$	$0.071 + 0.004 \cdot \text{SL}$	$0.048 + 0.004 \cdot \text{SL}$
	$t_F$	0.081	$0.073 + 0.004 \cdot \text{SL}$	$0.073 + 0.004 \cdot \text{SL}$	$0.054 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	2.391	$2.385 + 0.003 \cdot \text{SL}$	$2.389 + 0.002 \cdot \text{SL}$	$2.402 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	1.263	$1.256 + 0.003 \cdot \text{SL}$	$1.260 + 0.002 \cdot \text{SL}$	$1.278 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$

#### OAK\_DUCLK16

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to CK	$t_R$	0.088	$0.082 + 0.003 \cdot \text{SL}$	$0.080 + 0.004 \cdot \text{SL}$	$0.053 + 0.004 \cdot \text{SL}$
	$t_F$	0.094	$0.088 + 0.003 \cdot \text{SL}$	$0.085 + 0.004 \cdot \text{SL}$	$0.064 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	3.338	$3.332 + 0.003 \cdot \text{SL}$	$3.337 + 0.002 \cdot \text{SL}$	$3.352 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	1.875	$1.868 + 0.004 \cdot \text{SL}$	$1.873 + 0.002 \cdot \text{SL}$	$1.894 + 0.002 \cdot \text{SL}$
A to CKB	$t_R$	0.088	$0.082 + 0.003 \cdot \text{SL}$	$0.078 + 0.004 \cdot \text{SL}$	$0.053 + 0.004 \cdot \text{SL}$
	$t_F$	0.093	$0.086 + 0.003 \cdot \text{SL}$	$0.085 + 0.004 \cdot \text{SL}$	$0.064 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	3.409	$3.403 + 0.003 \cdot \text{SL}$	$3.408 + 0.002 \cdot \text{SL}$	$3.423 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	1.788	$1.781 + 0.004 \cdot \text{SL}$	$1.786 + 0.002 \cdot \text{SL}$	$1.807 + 0.002 \cdot \text{SL}$

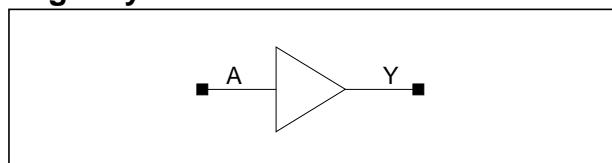
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$



# CTSB/D2/D3/D4/D6/D8/D16

## Clock Tree Synthesis Buffers

### Logic Symbol



### Truth Table

A	Y
0	0
1	1

### Cell Data

Input Load (SL)						
CTSB	CTSD2	CTSD3	CTSD4	CTSD6	CTSD8	CTSD16
A	A	A	A	A	A	A
0.8	0.9	0.9	0.9	1.7	1.8	3.5
Gate Count						
CTSB	CTSD2	CTSD3	CTSD4	CTSD6	CTSD8	CTSD16
1.00	1.33	1.67	2.00	2.67	3.33	6.33

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

#### CTSB

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.120	$0.064 + 0.028 \cdot \text{SL}$	$0.059 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$
	$t_F$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.167	$0.138 + 0.014 \cdot \text{SL}$	$0.143 + 0.013 \cdot \text{SL}$	$0.145 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.144	$0.109 + 0.017 \cdot \text{SL}$	$0.114 + 0.016 \cdot \text{SL}$	$0.115 + 0.016 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### CTSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.079	$0.049 + 0.015 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$	$0.041 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.162	$0.145 + 0.009 \cdot \text{SL}$	$0.151 + 0.007 \cdot \text{SL}$	$0.158 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.139	$0.118 + 0.010 \cdot \text{SL}$	$0.124 + 0.009 \cdot \text{SL}$	$0.130 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

#### CTSD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.090	$0.075 + 0.007 \cdot \text{SL}$	$0.066 + 0.010 \cdot \text{SL}$	$0.056 + 0.010 \cdot \text{SL}$
	$t_F$	0.080	$0.063 + 0.009 \cdot \text{SL}$	$0.056 + 0.010 \cdot \text{SL}$	$0.047 + 0.011 \cdot \text{SL}$
	$t_{PLH}$	0.169	$0.156 + 0.007 \cdot \text{SL}$	$0.163 + 0.005 \cdot \text{SL}$	$0.173 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.149	$0.134 + 0.007 \cdot \text{SL}$	$0.140 + 0.006 \cdot \text{SL}$	$0.148 + 0.006 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 0.21\text{ns}$ , SL: Standard Load)

**CTSBD4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.084	$0.070 + 0.007 \cdot \text{SL}$	$0.070 + 0.007 \cdot \text{SL}$	$0.064 + 0.007 \cdot \text{SL}$
	$t_F$	0.074	$0.060 + 0.007 \cdot \text{SL}$	$0.060 + 0.007 \cdot \text{SL}$	$0.054 + 0.008 \cdot \text{SL}$
	$t_{PLH}$	0.180	$0.169 + 0.005 \cdot \text{SL}$	$0.174 + 0.004 \cdot \text{SL}$	$0.187 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.159	$0.147 + 0.006 \cdot \text{SL}$	$0.152 + 0.005 \cdot \text{SL}$	$0.165 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 22$ , \*Group3 :  $22 < \text{SL}$ 
**CTSBD6**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.069	$0.058 + 0.005 \cdot \text{SL}$	$0.060 + 0.005 \cdot \text{SL}$	$0.040 + 0.005 \cdot \text{SL}$
	$t_F$	0.058	$0.047 + 0.006 \cdot \text{SL}$	$0.049 + 0.005 \cdot \text{SL}$	$0.033 + 0.005 \cdot \text{SL}$
	$t_{PLH}$	0.151	$0.144 + 0.004 \cdot \text{SL}$	$0.149 + 0.002 \cdot \text{SL}$	$0.161 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.128	$0.121 + 0.004 \cdot \text{SL}$	$0.125 + 0.003 \cdot \text{SL}$	$0.136 + 0.003 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$ 
**CTSBD8**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.072	$0.063 + 0.005 \cdot \text{SL}$	$0.067 + 0.004 \cdot \text{SL}$	$0.048 + 0.004 \cdot \text{SL}$
	$t_F$	0.063	$0.054 + 0.004 \cdot \text{SL}$	$0.056 + 0.004 \cdot \text{SL}$	$0.043 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.159	$0.154 + 0.002 \cdot \text{SL}$	$0.156 + 0.002 \cdot \text{SL}$	$0.172 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	0.144	$0.138 + 0.003 \cdot \text{SL}$	$0.142 + 0.002 \cdot \text{SL}$	$0.157 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$ 
**CTSBD16**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	$t_R$	0.071	$0.067 + 0.002 \cdot \text{SL}$	$0.069 + 0.002 \cdot \text{SL}$	$0.063 + 0.002 \cdot \text{SL}$
	$t_F$	0.058	$0.056 + 0.001 \cdot \text{SL}$	$0.054 + 0.002 \cdot \text{SL}$	$0.051 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	0.168	$0.165 + 0.002 \cdot \text{SL}$	$0.167 + 0.001 \cdot \text{SL}$	$0.183 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.140	$0.137 + 0.002 \cdot \text{SL}$	$0.139 + 0.001 \cdot \text{SL}$	$0.154 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 78$ , \*Group3 :  $78 < \text{SL}$



## FLIP-FLOPS

### Cell List

Cell Name	Function Description
FD1	D Flip-Flop
FD1D2	D Flip-Flop with 2X Drive
FD1CS	D Flip-Flop with Scan Clock
FD1CSD2	D Flip-Flop with Scan Clock, 2X Drive
FD1S	D Flip-Flop with Scan
FD1SD2	D Flip-Flop with Scan, 2X Drive
FD1SQ	D Flip-Flop with Scan, Q Output Only
FD1SQD2	D Flip-Flop with Scan, Q Output Only, 2X Drive
FD1Q	D Flip-Flop with Q Output Only
FD1QD2	D Flip-Flop with Q Output Only, 2X Drive
FD2	D Flip-Flop with Reset
FD2D2	D Flip-Flop with Reset, 2X Drive
FD2CS	D Flip-Flop with Reset, Scan Clock
FD2CSD2	D Flip-Flop with Reset, Scan Clock, 2X Drive
FD2S	D Flip-Flop with Reset, Scan
FD2SD2	D Flip-Flop with Reset, Scan, 2X Drive
FD2SQ	D Flip-Flop with Reset, Scan, Q Output Only
FD2SQD2	D Flip-Flop with Reset, Scan, Q Output Only, 2X Drive
FD2Q	D Flip-Flop with Reset, Q Output Only
FD2QD2	D Flip-Flop with Reset, Q Output Only, 2X Drive
FD3	D Flip-Flop with Set
FD3D2	D Flip-Flop with Set, 2X Drive
FD3CS	D Flip-Flop with Set, Scan Clock
FD3CSD2	D Flip-Flop with Set, Scan Clock, 2X Drive
FD3S	D Flip-Flop with Set, Scan
FD3SD2	D Flip-Flop with Set, Scan, 2X Drive
FD3SQ	D Flip-Flop with Set, Scan, Q Output Only
FD3SQD2	D Flip-Flop with Set, Scan, Q Output Only, 2X Drive
FD3Q	D Flip-Flop with Set, Q Output Only
FD3QD2	D Flip-Flop with Set, Q Output Only, 2X Drive
FD4	D Flip-Flop with Reset, Set
FD4D2	D Flip-Flop with Reset, Set, 2X Drive
FD4CS	D Flip-Flop with Reset, Set, Scan Clock
FD4CSD2	D Flip-Flop with Reset, Set, Scan Clock, 2X Drive
FD4S	D Flip-Flop with Reset, Set, Scan
FD4SD2	D Flip-Flop with Reset, Set, Scan, 2X Drive
FD4SQ	D Flip-Flop with Reset, Set, Scan, Q Output Only
FD4SQD2	D Flip-Flop with Reset, Set, Scan, Q Output Only, 2X Drive



## Cell List (Cont.)

Cell Name	Function Description
FD4Q	D Flip-Flop with Reset, Set, Q Output Only
FD4QD2	D Flip-Flop with Reset, Set, Q Output Only, 2X Drive
FD5	D Flip-Flop with Negative Edge Trigger
FD5D2	D Flip-Flop with Negative Edge Trigger, 2X Drive
FD5S	D Flip-Flop with Negative Edge Trigger, Scan
FD5SD2	D Flip-Flop with Negative Edge Trigger, Scan, 2X Drive
FD6	D Flip-Flop with Negative Edge Trigger, Reset
FD6D2	D Flip-Flop with Negative Edge Trigger, Reset, 2X Drive
FD6S	D Flip-Flop with Negative Edge Trigger, Reset, Scan
FD6SD2	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 2X Drive
FD7	D Flip-Flop with Negative Edge Trigger, Set
FD7D2	D Flip-Flop with Negative Edge Trigger, Set, 2X Drive
FD7S	D Flip-Flop with Negative Edge Trigger, Set, Scan
FD7SD2	D Flip-Flop with Negative Edge Trigger, Set, Scan, 2X Drive
FD8	D Flip-Flop with Negative Edge Trigger, Reset, Set
FD8D2	D Flip-Flop with Negative Edge Trigger, Reset, Set, 2X Drive
FD8S	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan
FD8SD2	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 2X Drive
FDS2	D Flip-Flop with Synchronous Clear
FDS2D2	D Flip-Flop with Synchronous Clear, 2X Drive
FDS2CS	D Flip-Flop with Synchronous Clear, Scan Clock
FDS2CSD2	D Flip-Flop with Synchronous Clear, Scan Clock, 2X Drive
FDS2S	D Flip-Flop with Synchronous Clear, Scan
FDS2SD2	D Flip-Flop with Synchronous Clear, Scan, 2X Drive
FDS3	D Flip-Flop with Synchronous Set
FDS3D2	D Flip-Flop with Synchronous Set, 2X Drive
FDS3CS	D Flip-Flop with Synchronous Set, Scan Clock
FDS3CSD2	D Flip-Flop with Synchronous Set, Scan Clock, 2X Drive
FDS3S	Flip-Flop with Synchronous Set, Scan
FDS3SD2	Flip-Flop with Synchronous Set, Scan, 2x Drive
FJ1	JK Flip-Flop
FJ1D2	JK Flip-Flop with 2X Drive
FJ1S	JK Flip-Flop with Scan
FJ1SD2	JK Flip-Flop with Scan, 2X Drive
FJ2	JK Flip-Flop with Reset
FJ2D2	JK Flip-Flop with Reset, 2X Drive
FJ2S	JK Flip-Flop with Reset, Scan
FJ2SD2	JK Flip-Flop with Reset, Scan, 2X Drive



## FLIP-FLOPS

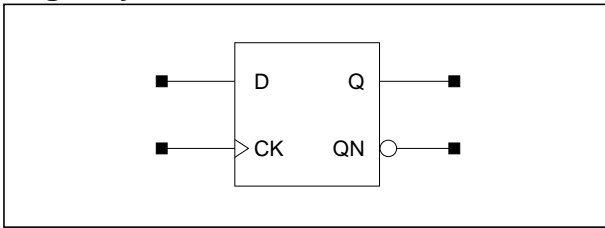
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### Cell List (Cont.)

Cell Name	Function Description
FJ4	JK Flip-Flop with Reset, Set
FJ4D2	JK Flip-Flop with Reset, Set, 2X Drive
FJ4S	JK Flip-Flop with Reset, Set, Scan
FJ4SD2	JK Flip-Flop with Reset, Set, Scan, 2X Drive
FT2	Toggle Flip-Flop with Reset
FT2D2	Toggle Flip-Flop with Reset, 2X Drive



## Logic Symbol



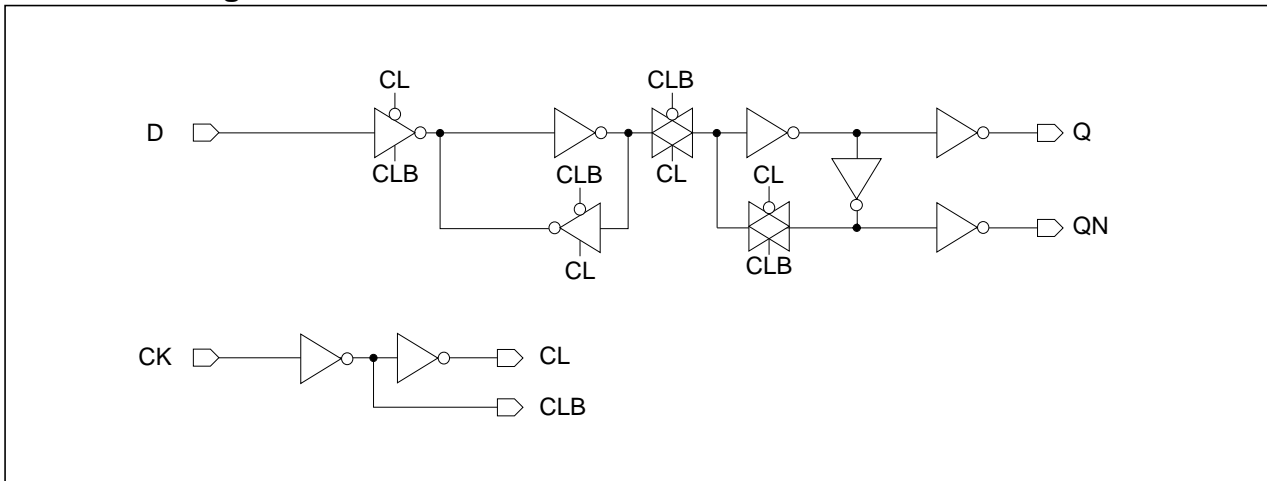
## Truth Table

D	CK	Q (n+1)	QN (n+1)
0		0	1
1		1	0
x		Q (n)	QN (n)

## Cell Data

Input Load (SL)				Gate Count	
FD1		FD1D2		FD1	FD1D2
D	CK	D	CK		
0.6	0.5	0.6	0.5	5.00	5.33

## Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1	FD1D2
Input Setup Time (D to CK)	$t_{SU}$	0.262	0.246
Input Hold Time (D to CK)	$t_{HD}$	0.140	0.130
Pulse Width Low (CK)	$t_{PWL}$	0.344	0.340
Pulse Width High (CK)	$t_{PWH}$	0.307	0.325



## FD1/FD1D2

### D Flip-Flop with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### FD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.122	$0.065 + 0.029 \cdot SL$	$0.060 + 0.030 \cdot SL$	$0.054 + 0.030 \cdot SL$
	$t_F$	0.111	$0.060 + 0.025 \cdot SL$	$0.062 + 0.025 \cdot SL$	$0.056 + 0.026 \cdot SL$
	$t_{PLH}$	0.386	$0.356 + 0.015 \cdot SL$	$0.361 + 0.014 \cdot SL$	$0.364 + 0.013 \cdot SL$
	$t_{PHL}$	0.401	$0.368 + 0.017 \cdot SL$	$0.376 + 0.015 \cdot SL$	$0.383 + 0.014 \cdot SL$
CK to QN	$t_R$	0.112	$0.054 + 0.029 \cdot SL$	$0.050 + 0.030 \cdot SL$	$0.044 + 0.031 \cdot SL$
	$t_F$	0.101	$0.051 + 0.025 \cdot SL$	$0.049 + 0.025 \cdot SL$	$0.043 + 0.026 \cdot SL$
	$t_{PLH}$	0.461	$0.431 + 0.015 \cdot SL$	$0.436 + 0.014 \cdot SL$	$0.437 + 0.013 \cdot SL$
	$t_{PHL}$	0.458	$0.426 + 0.016 \cdot SL$	$0.433 + 0.014 \cdot SL$	$0.436 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### FD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.093	$0.065 + 0.014 \cdot SL$	$0.062 + 0.015 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.088	$0.060 + 0.014 \cdot SL$	$0.063 + 0.013 \cdot SL$	$0.062 + 0.013 \cdot SL$
	$t_{PLH}$	0.386	$0.368 + 0.009 \cdot SL$	$0.375 + 0.007 \cdot SL$	$0.383 + 0.007 \cdot SL$
	$t_{PHL}$	0.403	$0.381 + 0.011 \cdot SL$	$0.390 + 0.008 \cdot SL$	$0.403 + 0.007 \cdot SL$
CK to QN	$t_R$	0.086	$0.058 + 0.014 \cdot SL$	$0.058 + 0.014 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.081	$0.052 + 0.015 \cdot SL$	$0.058 + 0.013 \cdot SL$	$0.051 + 0.014 \cdot SL$
	$t_{PLH}$	0.496	$0.479 + 0.009 \cdot SL$	$0.485 + 0.007 \cdot SL$	$0.491 + 0.007 \cdot SL$
	$t_{PHL}$	0.493	$0.473 + 0.010 \cdot SL$	$0.481 + 0.008 \cdot SL$	$0.491 + 0.007 \cdot SL$

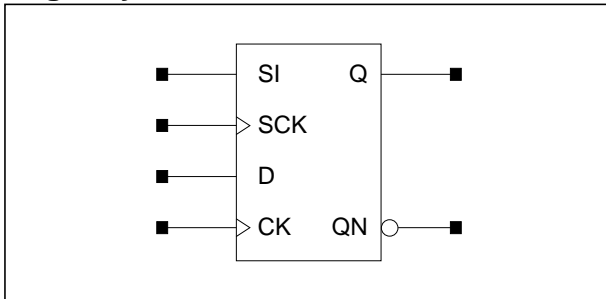
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FD1CS/FD1CSD2

### D Flip-Flop with Scan Clock, 1X/2X Drive

#### Logic Symbol



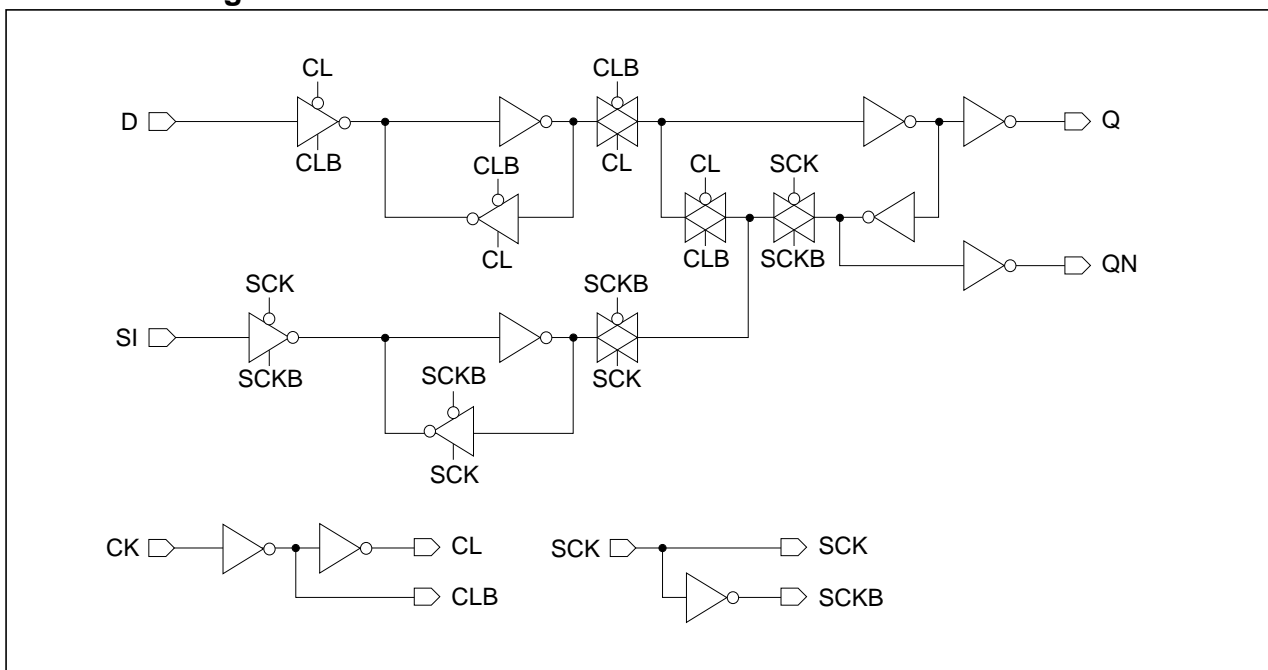
#### Truth Table

SI	SCK	D	CK	Q (n+1)	QN (n+1)
x	0	0		0	1
x	0	1		1	0
0		x	0	0	1
1		x	0	1	0
x	0	x		Q(n)	QN(n)
x		x	0	Q(n)	QN(n)

#### Cell Data

Input Load (SL)								Gate Count	
FD1CS				FD1CSD2				FD1CS	FD1CSD2
D	SI	CK	SCK	D	SI	CK	SCK		
0.6	0.5	0.5	1.4	0.6	0.5	0.5	1.4	8.00	8.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1CS	FD1CSD2
Input Setup Time (D to CK)	t <sub>SU</sub>	0.261	0.248
Input Hold Time (D to CK)	t <sub>HD</sub>	0.137	0.118
Input Setup Time (SI to SCK)	t <sub>SU</sub>	0.764	0.764
Input Hold Time (SI to SCK)	t <sub>HD</sub>	0.093	0.094
Pulse Width Low (CK)	t <sub>PWL</sub>	0.340	0.329
Pulse Width High (CK)	t <sub>PWH</sub>	0.316	0.336
Pulse Width Low (SCK)	t <sub>PWL</sub>	0.296	0.295
Pulse Width High (SCK)	t <sub>PWH</sub>	0.358	0.391



## FD1CS/FD1CSD2

### D Flip-Flop with Scan Clock, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### FD1CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.122	$0.065 + 0.029 \cdot SL$	$0.061 + 0.030 \cdot SL$	$0.053 + 0.031 \cdot SL$
	$t_F$	0.109	$0.059 + 0.025 \cdot SL$	$0.059 + 0.025 \cdot SL$	$0.054 + 0.026 \cdot SL$
	$t_{PLH}$	0.389	$0.359 + 0.015 \cdot SL$	$0.364 + 0.014 \cdot SL$	$0.367 + 0.014 \cdot SL$
	$t_{PHL}$	0.395	$0.362 + 0.017 \cdot SL$	$0.371 + 0.014 \cdot SL$	$0.376 + 0.014 \cdot SL$
SCK to Q	$t_R$	0.139	$0.084 + 0.027 \cdot SL$	$0.079 + 0.029 \cdot SL$	$0.067 + 0.030 \cdot SL$
	$t_F$	0.115	$0.066 + 0.025 \cdot SL$	$0.066 + 0.025 \cdot SL$	$0.059 + 0.026 \cdot SL$
	$t_{PLH}$	0.452	$0.419 + 0.016 \cdot SL$	$0.428 + 0.014 \cdot SL$	$0.432 + 0.013 \cdot SL$
	$t_{PHL}$	0.379	$0.345 + 0.017 \cdot SL$	$0.354 + 0.015 \cdot SL$	$0.361 + 0.014 \cdot SL$
CK to QN	$t_R$	0.126	$0.066 + 0.030 \cdot SL$	$0.066 + 0.030 \cdot SL$	$0.062 + 0.030 \cdot SL$
	$t_F$	0.111	$0.059 + 0.026 \cdot SL$	$0.059 + 0.026 \cdot SL$	$0.058 + 0.026 \cdot SL$
	$t_{PLH}$	0.475	$0.442 + 0.016 \cdot SL$	$0.451 + 0.014 \cdot SL$	$0.458 + 0.014 \cdot SL$
	$t_{PHL}$	0.484	$0.450 + 0.017 \cdot SL$	$0.458 + 0.015 \cdot SL$	$0.464 + 0.014 \cdot SL$
SCK to QN	$t_R$	0.113	$0.055 + 0.029 \cdot SL$	$0.051 + 0.030 \cdot SL$	$0.045 + 0.031 \cdot SL$
	$t_F$	0.103	$0.054 + 0.025 \cdot SL$	$0.052 + 0.025 \cdot SL$	$0.044 + 0.026 \cdot SL$
	$t_{PLH}$	0.438	$0.409 + 0.015 \cdot SL$	$0.413 + 0.014 \cdot SL$	$0.414 + 0.013 \cdot SL$
	$t_{PHL}$	0.524	$0.492 + 0.016 \cdot SL$	$0.499 + 0.014 \cdot SL$	$0.502 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### FD1CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.094	$0.065 + 0.014 \cdot SL$	$0.064 + 0.015 \cdot SL$	$0.056 + 0.015 \cdot SL$
	$t_F$	0.087	$0.059 + 0.014 \cdot SL$	$0.063 + 0.013 \cdot SL$	$0.060 + 0.013 \cdot SL$
	$t_{PLH}$	0.391	$0.372 + 0.009 \cdot SL$	$0.379 + 0.007 \cdot SL$	$0.388 + 0.007 \cdot SL$
	$t_{PHL}$	0.394	$0.372 + 0.011 \cdot SL$	$0.381 + 0.008 \cdot SL$	$0.394 + 0.007 \cdot SL$
SCK to Q	$t_R$	0.112	$0.084 + 0.014 \cdot SL$	$0.083 + 0.014 \cdot SL$	$0.074 + 0.015 \cdot SL$
	$t_F$	0.094	$0.067 + 0.013 \cdot SL$	$0.069 + 0.013 \cdot SL$	$0.067 + 0.013 \cdot SL$
	$t_{PLH}$	0.461	$0.440 + 0.010 \cdot SL$	$0.450 + 0.008 \cdot SL$	$0.462 + 0.007 \cdot SL$
	$t_{PHL}$	0.383	$0.362 + 0.011 \cdot SL$	$0.371 + 0.009 \cdot SL$	$0.385 + 0.007 \cdot SL$
CK to QN	$t_R$	0.098	$0.068 + 0.015 \cdot SL$	$0.070 + 0.015 \cdot SL$	$0.065 + 0.015 \cdot SL$
	$t_F$	0.090	$0.063 + 0.014 \cdot SL$	$0.063 + 0.014 \cdot SL$	$0.064 + 0.014 \cdot SL$
	$t_{PLH}$	0.509	$0.489 + 0.010 \cdot SL$	$0.497 + 0.008 \cdot SL$	$0.510 + 0.007 \cdot SL$
	$t_{PHL}$	0.521	$0.500 + 0.011 \cdot SL$	$0.508 + 0.009 \cdot SL$	$0.521 + 0.008 \cdot SL$
SCK to QN	$t_R$	0.085	$0.056 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.082	$0.056 + 0.013 \cdot SL$	$0.057 + 0.013 \cdot SL$	$0.051 + 0.013 \cdot SL$
	$t_{PLH}$	0.477	$0.460 + 0.009 \cdot SL$	$0.466 + 0.007 \cdot SL$	$0.471 + 0.007 \cdot SL$
	$t_{PHL}$	0.571	$0.551 + 0.010 \cdot SL$	$0.558 + 0.008 \cdot SL$	$0.568 + 0.007 \cdot SL$

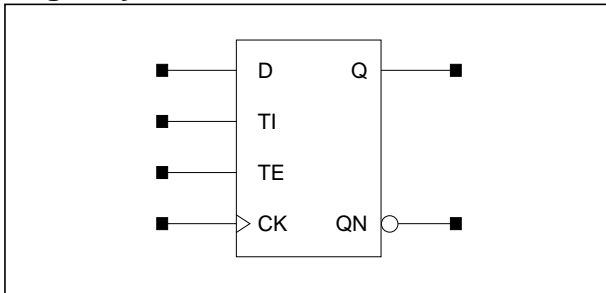
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# FD1S/FD1SD2

## D Flip-Flop with Scan, 1X/2X Drive

### Logic Symbol



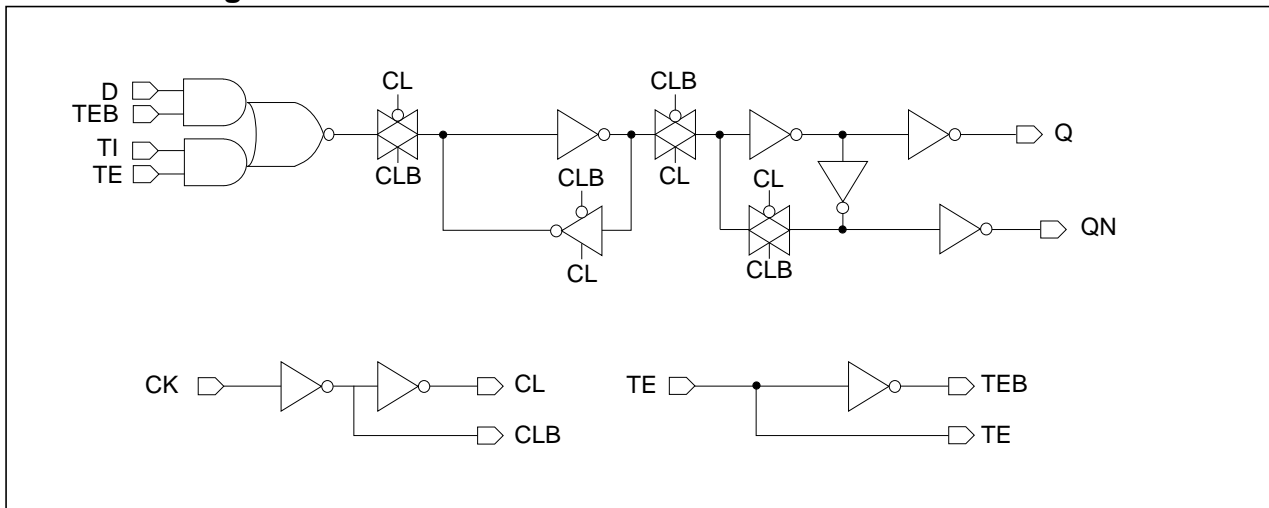
### Truth Table

D	TI	TE	CK	Q (n+1)	QN (n+1)
0	x	0		0	1
1	x	0		1	0
x	0	1		0	1
x	1	1		1	0
x	x	x		Q(n)	QN(n)

### Cell Data

Input Load (SL)								Gate Count	
FD1S				FD1SD2				FD1S	FD1SD2
D	CK	TI	TE	D	CK	TI	TE		
0.5	0.5	0.5	1.2	0.5	0.5	0.5	1.1	6.67	7.00

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1S	FD1SD2
Input Setup Time (D to CK)	$t_{SU}$	0.401	0.377
Input Hold Time (D to CK)	$t_{HD}$	0.036	0.045
Input Setup Time (TI to CK)	$t_{SU}$	0.483	0.473
Input Hold Time (TI to CK)	$t_{HD}$	0.045	0.041
Input Setup Time (TE to CK)	$t_{SU}$	0.523	0.522
Input Hold Time (TE to CK)	$t_{HD}$	0.047	0.063
Pulse Width Low (CK)	$t_{PWL}$	0.463	0.445
Pulse Width High (CK)	$t_{PWH}$	0.311	0.324



## FD1S/FD1SD2

### D Flip-Flop with Scan, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### FD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.123	$0.065 + 0.029 \cdot SL$	$0.062 + 0.030 \cdot SL$	$0.055 + 0.030 \cdot SL$
	$t_F$	0.110	$0.057 + 0.026 \cdot SL$	$0.061 + 0.025 \cdot SL$	$0.057 + 0.026 \cdot SL$
	$t_{PLH}$	0.393	$0.362 + 0.015 \cdot SL$	$0.368 + 0.014 \cdot SL$	$0.371 + 0.014 \cdot SL$
	$t_{PHL}$	0.413	$0.380 + 0.017 \cdot SL$	$0.388 + 0.015 \cdot SL$	$0.395 + 0.014 \cdot SL$
CK to QN	$t_R$	0.113	$0.055 + 0.029 \cdot SL$	$0.050 + 0.030 \cdot SL$	$0.045 + 0.031 \cdot SL$
	$t_F$	0.101	$0.051 + 0.025 \cdot SL$	$0.050 + 0.025 \cdot SL$	$0.044 + 0.026 \cdot SL$
	$t_{PLH}$	0.474	$0.445 + 0.015 \cdot SL$	$0.449 + 0.014 \cdot SL$	$0.450 + 0.013 \cdot SL$
	$t_{PHL}$	0.465	$0.434 + 0.016 \cdot SL$	$0.440 + 0.014 \cdot SL$	$0.444 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### FD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.094	$0.067 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.056 + 0.015 \cdot SL$
	$t_F$	0.090	$0.062 + 0.014 \cdot SL$	$0.064 + 0.014 \cdot SL$	$0.062 + 0.014 \cdot SL$
	$t_{PLH}$	0.391	$0.373 + 0.009 \cdot SL$	$0.380 + 0.007 \cdot SL$	$0.388 + 0.007 \cdot SL$
	$t_{PHL}$	0.416	$0.395 + 0.011 \cdot SL$	$0.403 + 0.009 \cdot SL$	$0.416 + 0.008 \cdot SL$
CK to QN	$t_R$	0.086	$0.057 + 0.014 \cdot SL$	$0.057 + 0.014 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.081	$0.053 + 0.014 \cdot SL$	$0.056 + 0.013 \cdot SL$	$0.050 + 0.014 \cdot SL$
	$t_{PLH}$	0.507	$0.490 + 0.009 \cdot SL$	$0.496 + 0.007 \cdot SL$	$0.502 + 0.007 \cdot SL$
	$t_{PHL}$	0.496	$0.476 + 0.010 \cdot SL$	$0.484 + 0.008 \cdot SL$	$0.494 + 0.007 \cdot SL$

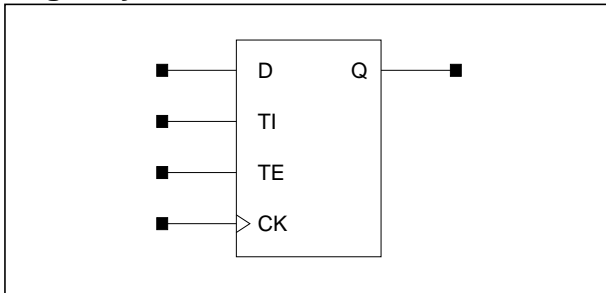
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FD1SQ/FD1SQD2

### D Flip-Flop with Scan, Q Output Only, 1X/2X Drive

#### Logic Symbol



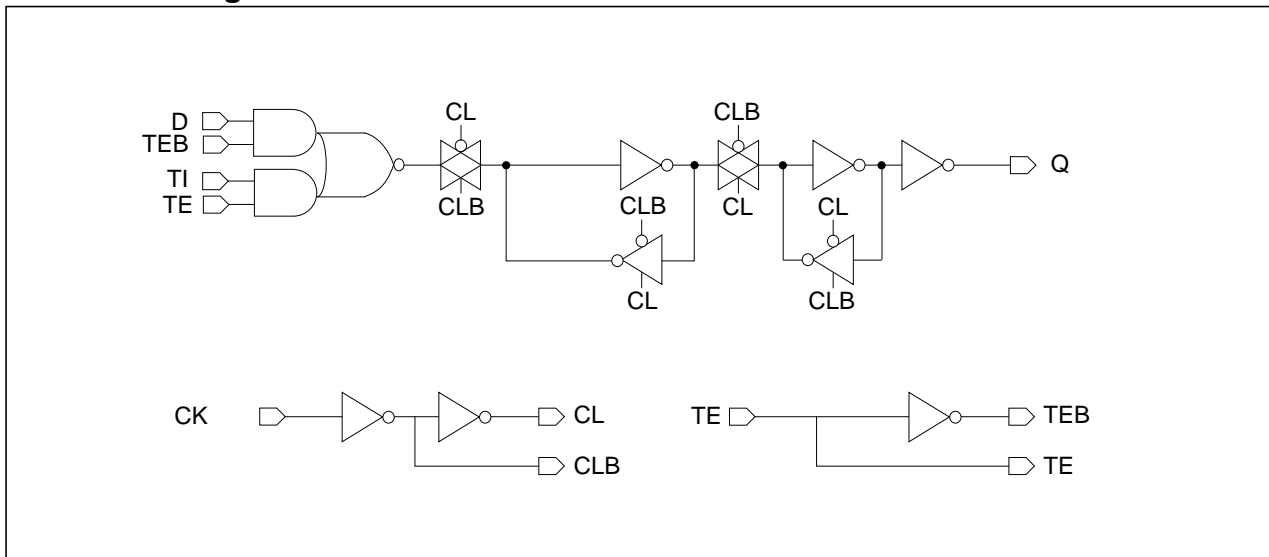
#### Truth Table

D	TI	TE	CK	Q (n+1)
0	x	0		0
1	x	0		1
x	0	1		0
x	1	1		1
x	x	x		Q(n)

#### Cell Data

Input Load (SL)								Gate Count	
FD1SQ				FD1SQD2				FD1SQ	FD1SQD2
D	CK	TI	TE	D	CK	TI	TE		
0.5	0.5	0.5	1.1	0.5	0.6	0.5	1.2	6.00	6.00

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1SQ	FD1SQD2
Input Setup Time (D to CK)	$t_{SU}$	0.370	0.402
Input Hold Time (D to CK)	$t_{HD}$	0.043	0.031
Input Setup Time (TI to CK)	$t_{SU}$	0.468	0.484
Input Hold Time (TI to CK)	$t_{HD}$	0.040	0.066
Input Setup Time (TE to CK)	$t_{SU}$	0.517	0.516
Input Hold Time (TE to CK)	$t_{HD}$	0.060	0.043
Pulse Width Low (CK)	$t_{PWL}$	0.442	0.461
Pulse Width High (CK)	$t_{PWH}$	0.292	0.328



## FD1SQ/FD1SQD2

### D Flip-Flop with Scan, Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### FD1SQ

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.118	$0.061 + 0.029 \cdot SL$	$0.055 + 0.030 \cdot SL$	$0.048 + 0.031 \cdot SL$
	$t_F$	0.108	$0.054 + 0.027 \cdot SL$	$0.054 + 0.027 \cdot SL$	$0.049 + 0.027 \cdot SL$
	$t_{PLH}$	0.369	$0.339 + 0.015 \cdot SL$	$0.345 + 0.014 \cdot SL$	$0.346 + 0.013 \cdot SL$
	$t_{PHL}$	0.396	$0.362 + 0.017 \cdot SL$	$0.369 + 0.015 \cdot SL$	$0.373 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### FD1SQD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.091	$0.062 + 0.014 \cdot SL$	$0.063 + 0.014 \cdot SL$	$0.051 + 0.015 \cdot SL$
	$t_F$	0.083	$0.055 + 0.014 \cdot SL$	$0.058 + 0.013 \cdot SL$	$0.054 + 0.014 \cdot SL$
	$t_{PLH}$	0.393	$0.375 + 0.009 \cdot SL$	$0.382 + 0.007 \cdot SL$	$0.389 + 0.007 \cdot SL$
	$t_{PHL}$	0.407	$0.386 + 0.010 \cdot SL$	$0.394 + 0.008 \cdot SL$	$0.405 + 0.007 \cdot SL$

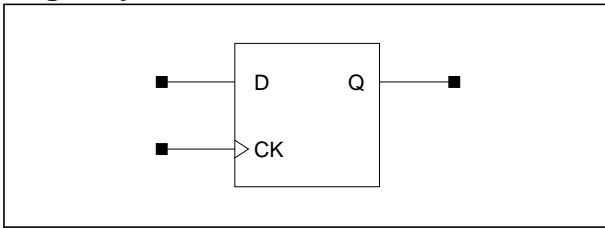
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FD1Q/FD1QD2

### D Flip-Flop with Q Output Only, 1X/2X Drive

#### Logic Symbol



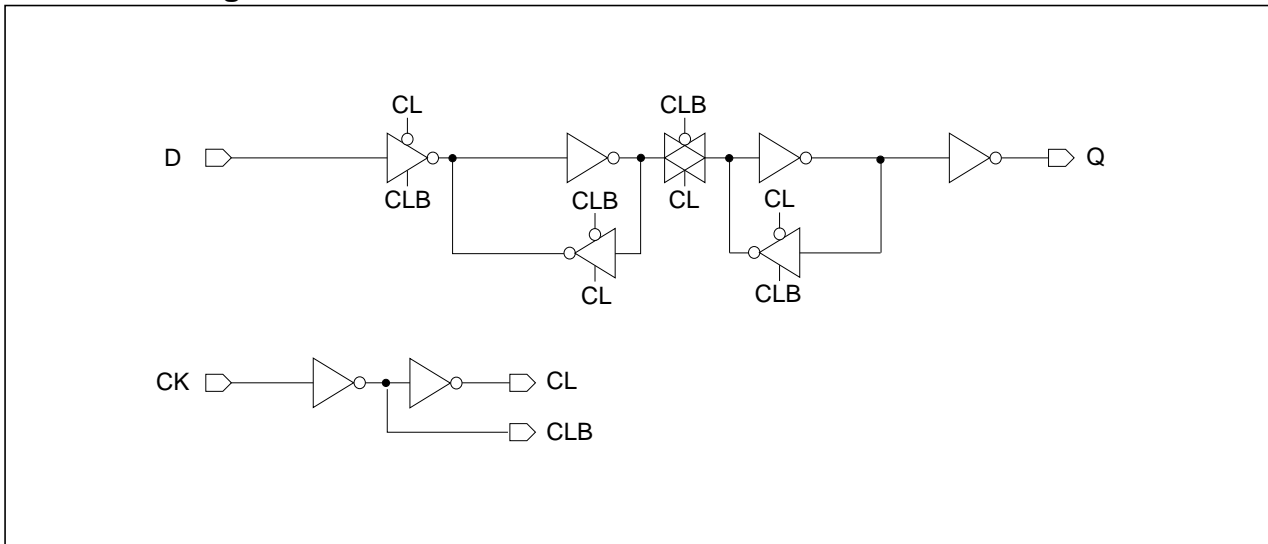
#### Truth Table

D	CK	Q (n+1)
0		0
1		1
x		Q (n)

#### Cell Data

Input Load (SL)				Gate Count	
FD1Q		FD1QD2		FD1Q	FD1QD2
D	CK	D	CK		
0.6	0.5	0.6	0.5	4.33	4.67

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1Q	FD1QD2
Input Setup Time (D to CK)	$t_{SU}$	0.246	0.246
Input Hold Time (D to CK)	$t_{HD}$	0.118	0.118
Pulse Width Low (CK)	$t_{PWL}$	0.334	0.334
Pulse Width High (CK)	$t_{PWH}$	0.294	0.294



## FD1Q/FD1QD2

### D Flip-Flop with Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### FD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.117	$0.061 + 0.028 \cdot SL$	$0.055 + 0.029 \cdot SL$	$0.049 + 0.030 \cdot SL$
	$t_F$	0.109	$0.056 + 0.026 \cdot SL$	$0.055 + 0.027 \cdot SL$	$0.049 + 0.027 \cdot SL$
	$t_{PLH}$	0.365	$0.336 + 0.015 \cdot SL$	$0.341 + 0.013 \cdot SL$	$0.343 + 0.013 \cdot SL$
	$t_{PHL}$	0.386	$0.352 + 0.017 \cdot SL$	$0.360 + 0.015 \cdot SL$	$0.364 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### FD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.089	$0.061 + 0.014 \cdot SL$	$0.059 + 0.015 \cdot SL$	$0.050 + 0.015 \cdot SL$
	$t_F$	0.081	$0.054 + 0.013 \cdot SL$	$0.057 + 0.012 \cdot SL$	$0.054 + 0.013 \cdot SL$
	$t_{PLH}$	0.371	$0.353 + 0.009 \cdot SL$	$0.360 + 0.007 \cdot SL$	$0.367 + 0.007 \cdot SL$
	$t_{PHL}$	0.385	$0.366 + 0.010 \cdot SL$	$0.374 + 0.008 \cdot SL$	$0.385 + 0.007 \cdot SL$

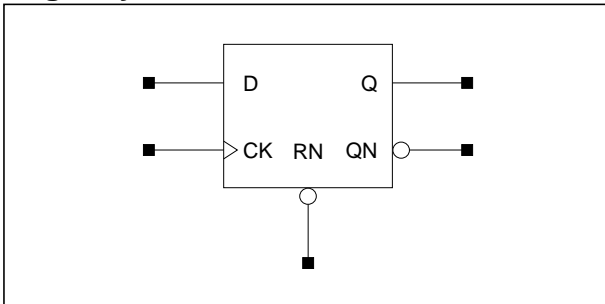
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FD2/FD2D2

### D Flip-Flop with Reset, 1X/2X Drive

#### Logic Symbol



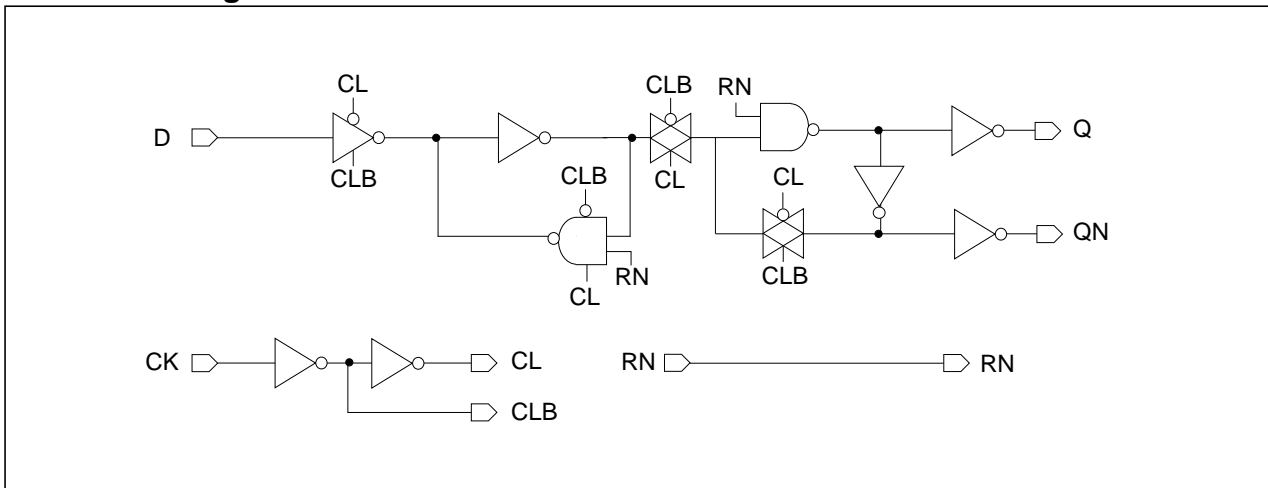
#### Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0		1	0	1
1		1	1	0
x	x	0	0	1
x		1	Q (n)	QN (n)

#### Cell Data

Input Load (SL)						Gate Count	
FD2			FD2D2			FD2	FD2D2
D	CK	RN	D	CK	RN		
0.6	0.5	1.4	0.5	0.5	1.4	5.67	6.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2	FD2D2
Input Setup Time (D to CK)	$t_{SU}$	0.278	0.256
Input Hold Time (D to CK)	$t_{HD}$	0.203	0.186
Pulse Width Low (CK)	$t_{PWL}$	0.363	0.371
Pulse Width High (CK)	$t_{PWH}$	0.340	0.349
Pulse Width Low (RN)	$t_{PWL}$	0.259	0.288
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.802	0.781



## FD2/FD2D2

### D Flip-Flop with Reset, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.137	$0.079 + 0.029 \cdot SL$	$0.079 + 0.029 \cdot SL$	$0.074 + 0.030 \cdot SL$
	$t_F$	0.118	$0.063 + 0.028 \cdot SL$	$0.066 + 0.027 \cdot SL$	$0.062 + 0.027 \cdot SL$
	$t_{PLH}$	0.436	$0.402 + 0.017 \cdot SL$	$0.411 + 0.015 \cdot SL$	$0.420 + 0.014 \cdot SL$
	$t_{PHL}$	0.420	$0.384 + 0.018 \cdot SL$	$0.393 + 0.016 \cdot SL$	$0.401 + 0.015 \cdot SL$
RN to Q	$t_F$	0.119	$0.064 + 0.027 \cdot SL$	$0.067 + 0.027 \cdot SL$	$0.063 + 0.027 \cdot SL$
	$t_{PHL}$	0.198	$0.163 + 0.018 \cdot SL$	$0.171 + 0.016 \cdot SL$	$0.179 + 0.015 \cdot SL$
CK to QN	$t_R$	0.112	$0.056 + 0.028 \cdot SL$	$0.050 + 0.030 \cdot SL$	$0.046 + 0.030 \cdot SL$
	$t_F$	0.107	$0.053 + 0.027 \cdot SL$	$0.054 + 0.027 \cdot SL$	$0.048 + 0.027 \cdot SL$
	$t_{PLH}$	0.478	$0.449 + 0.014 \cdot SL$	$0.453 + 0.013 \cdot SL$	$0.455 + 0.013 \cdot SL$
	$t_{PHL}$	0.517	$0.484 + 0.017 \cdot SL$	$0.491 + 0.015 \cdot SL$	$0.494 + 0.015 \cdot SL$
RN to QN	$t_R$	0.130	$0.071 + 0.029 \cdot SL$	$0.073 + 0.029 \cdot SL$	$0.069 + 0.030 \cdot SL$
	$t_{PLH}$	0.290	$0.256 + 0.017 \cdot SL$	$0.265 + 0.015 \cdot SL$	$0.274 + 0.013 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.107	$0.077 + 0.015 \cdot SL$	$0.078 + 0.015 \cdot SL$	$0.075 + 0.015 \cdot SL$
	$t_F$	0.091	$0.064 + 0.014 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$
	$t_{PLH}$	0.420	$0.399 + 0.010 \cdot SL$	$0.408 + 0.008 \cdot SL$	$0.422 + 0.007 \cdot SL$
	$t_{PHL}$	0.423	$0.402 + 0.011 \cdot SL$	$0.410 + 0.009 \cdot SL$	$0.424 + 0.008 \cdot SL$
RN to Q	$t_F$	0.089	$0.060 + 0.014 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	$t_{PHL}$	0.188	$0.166 + 0.011 \cdot SL$	$0.175 + 0.009 \cdot SL$	$0.189 + 0.008 \cdot SL$
CK to QN	$t_R$	0.088	$0.059 + 0.014 \cdot SL$	$0.059 + 0.014 \cdot SL$	$0.048 + 0.015 \cdot SL$
	$t_F$	0.086	$0.059 + 0.013 \cdot SL$	$0.062 + 0.013 \cdot SL$	$0.057 + 0.013 \cdot SL$
	$t_{PLH}$	0.524	$0.506 + 0.009 \cdot SL$	$0.512 + 0.007 \cdot SL$	$0.519 + 0.007 \cdot SL$
	$t_{PHL}$	0.539	$0.519 + 0.010 \cdot SL$	$0.527 + 0.008 \cdot SL$	$0.539 + 0.007 \cdot SL$
RN to QN	$t_R$	0.101	$0.071 + 0.015 \cdot SL$	$0.072 + 0.015 \cdot SL$	$0.068 + 0.015 \cdot SL$
	$t_{PLH}$	0.318	$0.298 + 0.010 \cdot SL$	$0.306 + 0.008 \cdot SL$	$0.320 + 0.007 \cdot SL$

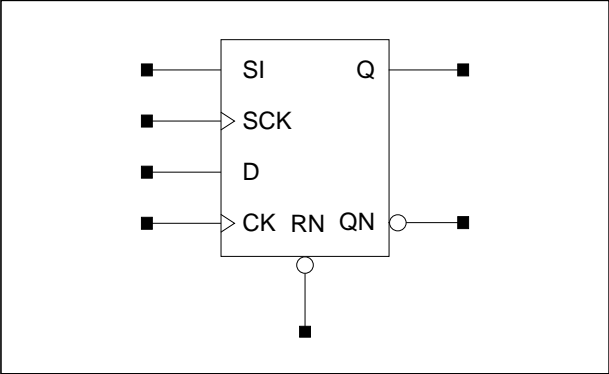
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



FD2CS/FD2CSD2

D Flip-Flop with Reset, Scan Clock, 1X/2X Drive

Logic Symbol



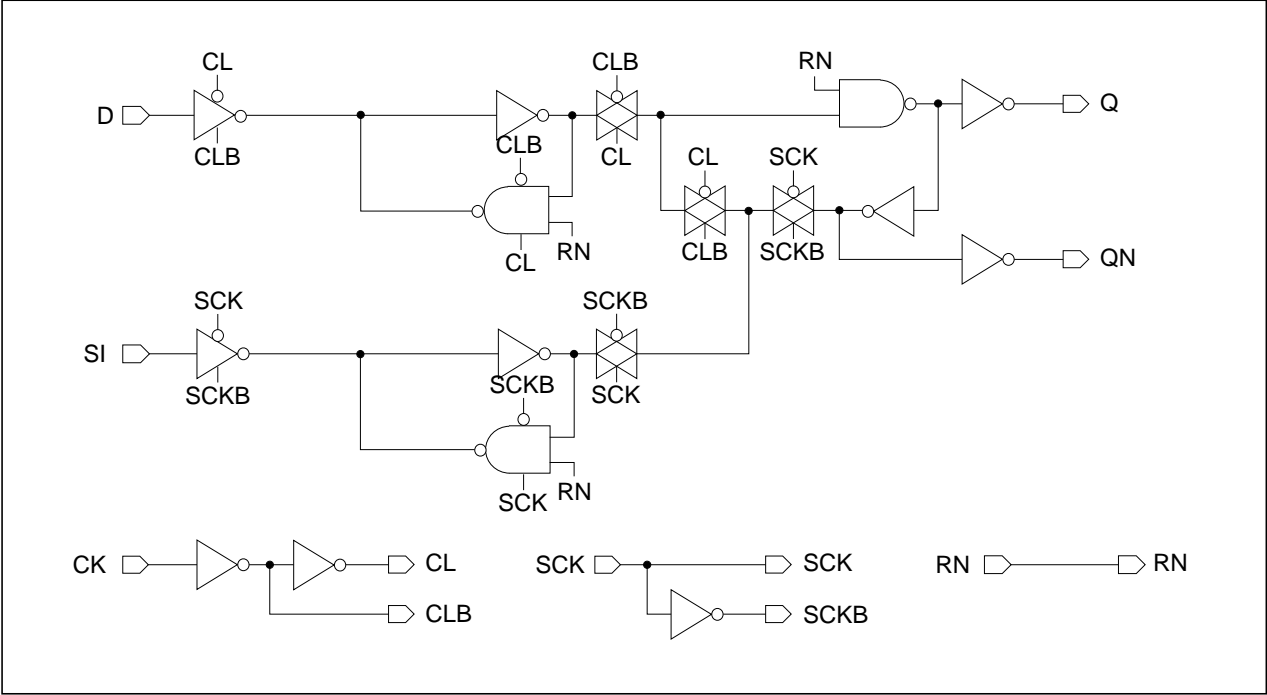
Truth Table

SI	SCK	D	CK	RN	Q (n+1)	QN (n+1)
x	0	0		1	0	1
x	0	1		1	1	0
0		x	0	1	0	1
1		x	0	1	1	0
x	x	x	x	0	0	1
x		x	0	1	Q(n)	QN(n)
x	0	x		1	Q(n)	QN(n)

Cell Data

Input Load (SL)										Gate Count	
FD2CS					FD2CSD2					FD2CS	FD2CSD2
D	SI	CK	SCK	RN	D	SI	CK	SCK	RN		
0.6	0.6	0.6	1.4	2.1	0.6	0.6	0.6	1.5	2.1	9.33	9.67

Schematic Diagram





## FD2CS/FD2CSD2

### D Flip-Flop with Reset, Scan Clock, 1X/2X Drive

#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2CS	FD2CSD2
Input Setup Time (D to CK)	$t_{SU}$	0.284	0.203
Input Hold Time (D to CK)	$t_{HD}$	0.190	0.278
Input Setup Time (SI to SCK)	$t_{SU}$	0.758	0.777
Input Hold Time (SI to SCK)	$t_{HD}$	0.046	0.039
Pulse Width Low (CK)	$t_{PWL}$	0.370	0.366
Pulse Width High (CK)	$t_{PWH}$	0.353	0.388
Pulse Width Low (SCK)	$t_{PWL}$	0.330	0.337
Pulse Width High (SCK)	$t_{PWH}$	0.410	0.440
Pulse Width Low (RN)	$t_{PWL}$	0.318	0.349
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.809	0.801
Recovery Time (RN to SCK)	$t_{RC}$	0.000	0.000
Removal Time (RN to SCK)	$t_{RM}$	0.718	0.768



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FD2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.137	$0.080 + 0.029 \cdot SL$	$0.080 + 0.029 \cdot SL$	$0.073 + 0.030 \cdot SL$
	$t_F$	0.116	$0.062 + 0.027 \cdot SL$	$0.065 + 0.026 \cdot SL$	$0.060 + 0.027 \cdot SL$
	$t_{PLH}$	0.440	$0.407 + 0.016 \cdot SL$	$0.415 + 0.014 \cdot SL$	$0.422 + 0.014 \cdot SL$
	$t_{PHL}$	0.417	$0.382 + 0.017 \cdot SL$	$0.390 + 0.015 \cdot SL$	$0.397 + 0.014 \cdot SL$
SCK to Q	$t_R$	0.153	$0.097 + 0.028 \cdot SL$	$0.097 + 0.028 \cdot SL$	$0.087 + 0.029 \cdot SL$
	$t_F$	0.122	$0.069 + 0.026 \cdot SL$	$0.071 + 0.026 \cdot SL$	$0.066 + 0.027 \cdot SL$
	$t_{PLH}$	0.509	$0.475 + 0.017 \cdot SL$	$0.485 + 0.015 \cdot SL$	$0.494 + 0.014 \cdot SL$
	$t_{PHL}$	0.406	$0.371 + 0.018 \cdot SL$	$0.379 + 0.015 \cdot SL$	$0.388 + 0.014 \cdot SL$
RN to Q	$t_F$	0.118	$0.064 + 0.027 \cdot SL$	$0.067 + 0.026 \cdot SL$	$0.062 + 0.027 \cdot SL$
	$t_{PHL}$	0.198	$0.163 + 0.017 \cdot SL$	$0.171 + 0.015 \cdot SL$	$0.178 + 0.015 \cdot SL$
CK to QN	$t_R$	0.132	$0.074 + 0.029 \cdot SL$	$0.074 + 0.029 \cdot SL$	$0.069 + 0.030 \cdot SL$
	$t_F$	0.125	$0.070 + 0.027 \cdot SL$	$0.071 + 0.027 \cdot SL$	$0.069 + 0.027 \cdot SL$
	$t_{PLH}$	0.509	$0.476 + 0.017 \cdot SL$	$0.485 + 0.015 \cdot SL$	$0.494 + 0.013 \cdot SL$
	$t_{PHL}$	0.565	$0.528 + 0.018 \cdot SL$	$0.537 + 0.016 \cdot SL$	$0.545 + 0.015 \cdot SL$
SCK to QN	$t_R$	0.116	$0.060 + 0.028 \cdot SL$	$0.054 + 0.029 \cdot SL$	$0.049 + 0.030 \cdot SL$
	$t_F$	0.115	$0.063 + 0.026 \cdot SL$	$0.061 + 0.026 \cdot SL$	$0.055 + 0.027 \cdot SL$
	$t_{PLH}$	0.476	$0.446 + 0.015 \cdot SL$	$0.452 + 0.013 \cdot SL$	$0.454 + 0.013 \cdot SL$
	$t_{PHL}$	0.605	$0.571 + 0.017 \cdot SL$	$0.579 + 0.015 \cdot SL$	$0.584 + 0.015 \cdot SL$
RN to QN	$t_R$	0.139	$0.076 + 0.032 \cdot SL$	$0.079 + 0.031 \cdot SL$	$0.087 + 0.030 \cdot SL$
	$t_{PLH}$	0.298	$0.263 + 0.018 \cdot SL$	$0.270 + 0.016 \cdot SL$	$0.281 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## FD2CS/FD2CSD2

### D Flip-Flop with Reset, Scan Clock, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

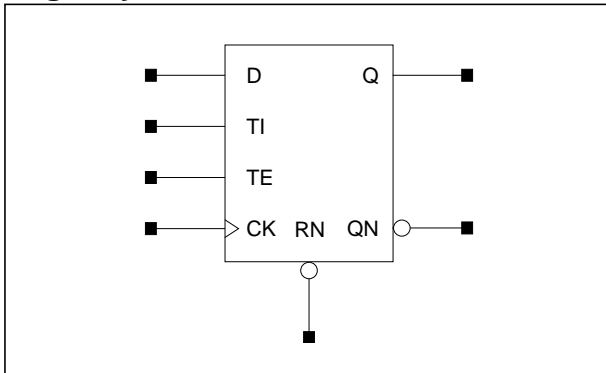
#### FD2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.110	$0.081 + 0.015 \cdot SL$	$0.082 + 0.014 \cdot SL$	$0.077 + 0.015 \cdot SL$
	$t_F$	0.093	$0.065 + 0.014 \cdot SL$	$0.067 + 0.014 \cdot SL$	$0.066 + 0.014 \cdot SL$
	$t_{PLH}$	0.458	$0.437 + 0.010 \cdot SL$	$0.446 + 0.008 \cdot SL$	$0.460 + 0.007 \cdot SL$
	$t_{PHL}$	0.430	$0.409 + 0.011 \cdot SL$	$0.417 + 0.009 \cdot SL$	$0.431 + 0.008 \cdot SL$
SCK to Q	$t_R$	0.127	$0.100 + 0.014 \cdot SL$	$0.099 + 0.014 \cdot SL$	$0.095 + 0.014 \cdot SL$
	$t_F$	0.100	$0.072 + 0.014 \cdot SL$	$0.074 + 0.013 \cdot SL$	$0.073 + 0.013 \cdot SL$
	$t_{PLH}$	0.522	$0.500 + 0.011 \cdot SL$	$0.511 + 0.008 \cdot SL$	$0.526 + 0.007 \cdot SL$
	$t_{PHL}$	0.422	$0.400 + 0.011 \cdot SL$	$0.409 + 0.009 \cdot SL$	$0.424 + 0.008 \cdot SL$
RN to Q	$t_F$	0.091	$0.062 + 0.015 \cdot SL$	$0.067 + 0.013 \cdot SL$	$0.064 + 0.014 \cdot SL$
	$t_{PHL}$	0.192	$0.171 + 0.011 \cdot SL$	$0.179 + 0.009 \cdot SL$	$0.193 + 0.008 \cdot SL$
CK to QN	$t_R$	0.100	$0.071 + 0.015 \cdot SL$	$0.072 + 0.014 \cdot SL$	$0.068 + 0.015 \cdot SL$
	$t_F$	0.097	$0.068 + 0.014 \cdot SL$	$0.071 + 0.014 \cdot SL$	$0.069 + 0.014 \cdot SL$
	$t_{PLH}$	0.548	$0.529 + 0.010 \cdot SL$	$0.537 + 0.008 \cdot SL$	$0.550 + 0.007 \cdot SL$
	$t_{PHL}$	0.608	$0.586 + 0.011 \cdot SL$	$0.595 + 0.009 \cdot SL$	$0.608 + 0.008 \cdot SL$
SCK to QN	$t_R$	0.088	$0.060 + 0.014 \cdot SL$	$0.060 + 0.014 \cdot SL$	$0.048 + 0.015 \cdot SL$
	$t_F$	0.088	$0.061 + 0.013 \cdot SL$	$0.062 + 0.013 \cdot SL$	$0.056 + 0.014 \cdot SL$
	$t_{PLH}$	0.520	$0.502 + 0.009 \cdot SL$	$0.508 + 0.007 \cdot SL$	$0.515 + 0.007 \cdot SL$
	$t_{PHL}$	0.647	$0.627 + 0.010 \cdot SL$	$0.635 + 0.008 \cdot SL$	$0.645 + 0.007 \cdot SL$
RN to QN	$t_R$	0.105	$0.075 + 0.015 \cdot SL$	$0.073 + 0.016 \cdot SL$	$0.080 + 0.015 \cdot SL$
	$t_{PLH}$	0.317	$0.296 + 0.010 \cdot SL$	$0.304 + 0.008 \cdot SL$	$0.316 + 0.008 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



### Logic Symbol



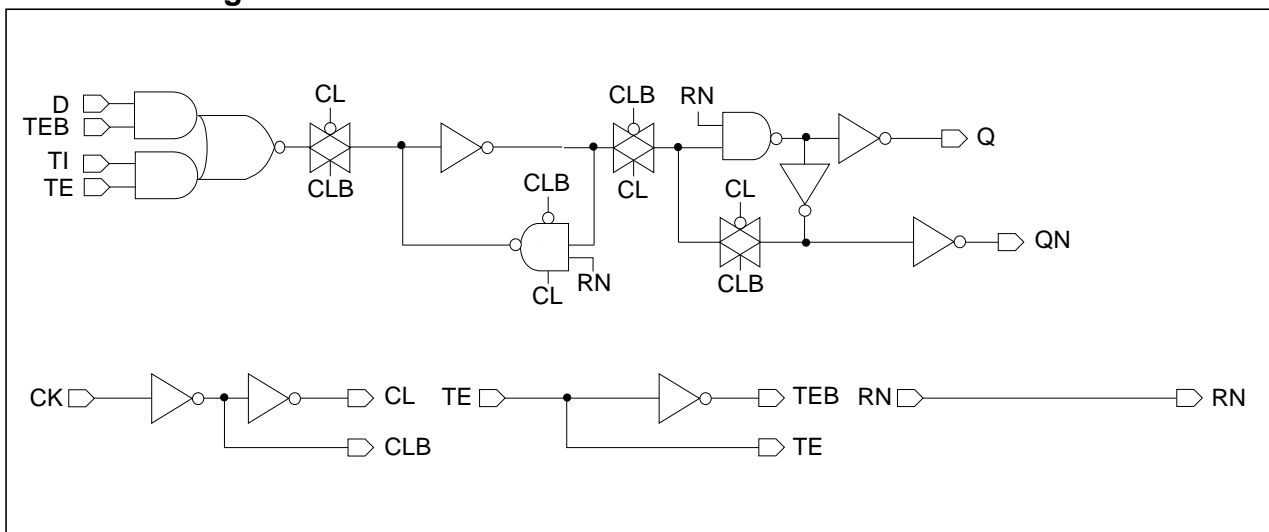
### Truth Table

D	TI	TE	CK	RN	Q (n+1)	QN (n+1)
0	x	0		1	0	1
1	x	0		1	1	0
x	0	1		1	0	1
x	1	1		1	1	0
x	x	x	x	0	0	1
x	x	x		1	Q(n)	QN(n)

### Cell Data

Input Load (SL)										Gate Count	
FD2S					FD2SD2					FD2S	FD2SD2
D	CK	RN	TI	TE	D	CK	RN	TI	TE		
0.5	0.6	1.4	0.5	1.2	0.5	0.6	1.4	0.5	1.2	7.67	8.00

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2S	FD2SD2
Input Setup Time (D to CK)	$t_{SU}$	0.405	0.409
Input Hold Time (D to CK)	$t_{HD}$	0.133	0.126
Input Setup Time (TI to CK)	$t_{SU}$	0.491	0.495
Input Hold Time (TI to CK)	$t_{HD}$	0.137	0.130
Input Setup Time (TE to CK)	$t_{SU}$	0.528	0.525
Input Hold Time (TE to CK)	$t_{HD}$	0.137	0.128
Pulse Width Low (CK)	$t_{PWL}$	0.480	0.483
Pulse Width High (CK)	$t_{PWH}$	0.348	0.372
Pulse Width Low (RN)	$t_{PWL}$	0.258	0.294
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.769	0.772



## FD2S/FD2SD2

### D Flip-Flop with Reset, Scan, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.138	$0.078 + 0.030 \cdot SL$	$0.078 + 0.030 \cdot SL$	$0.074 + 0.031 \cdot SL$
	$t_F$	0.114	$0.062 + 0.026 \cdot SL$	$0.066 + 0.025 \cdot SL$	$0.062 + 0.026 \cdot SL$
	$t_{PLH}$	0.448	$0.414 + 0.017 \cdot SL$	$0.422 + 0.015 \cdot SL$	$0.430 + 0.014 \cdot SL$
	$t_{PHL}$	0.434	$0.399 + 0.017 \cdot SL$	$0.408 + 0.015 \cdot SL$	$0.417 + 0.014 \cdot SL$
RN to Q	$t_F$	0.114	$0.062 + 0.026 \cdot SL$	$0.066 + 0.025 \cdot SL$	$0.062 + 0.026 \cdot SL$
	$t_{PHL}$	0.194	$0.160 + 0.017 \cdot SL$	$0.169 + 0.015 \cdot SL$	$0.176 + 0.014 \cdot SL$
CK to QN	$t_R$	0.113	$0.056 + 0.028 \cdot SL$	$0.052 + 0.030 \cdot SL$	$0.046 + 0.030 \cdot SL$
	$t_F$	0.105	$0.056 + 0.025 \cdot SL$	$0.055 + 0.025 \cdot SL$	$0.049 + 0.026 \cdot SL$
	$t_{PLH}$	0.496	$0.467 + 0.015 \cdot SL$	$0.472 + 0.013 \cdot SL$	$0.473 + 0.013 \cdot SL$
	$t_{PHL}$	0.527	$0.494 + 0.016 \cdot SL$	$0.502 + 0.014 \cdot SL$	$0.506 + 0.014 \cdot SL$
RN to QN	$t_R$	0.131	$0.072 + 0.029 \cdot SL$	$0.072 + 0.029 \cdot SL$	$0.068 + 0.030 \cdot SL$
	$t_{PLH}$	0.290	$0.256 + 0.017 \cdot SL$	$0.265 + 0.015 \cdot SL$	$0.275 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.109	$0.079 + 0.015 \cdot SL$	$0.081 + 0.015 \cdot SL$	$0.077 + 0.015 \cdot SL$
	$t_F$	0.090	$0.062 + 0.014 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.064 + 0.013 \cdot SL$
	$t_{PLH}$	0.450	$0.429 + 0.010 \cdot SL$	$0.438 + 0.008 \cdot SL$	$0.452 + 0.007 \cdot SL$
	$t_{PHL}$	0.433	$0.412 + 0.011 \cdot SL$	$0.420 + 0.009 \cdot SL$	$0.435 + 0.008 \cdot SL$
RN to Q	$t_F$	0.091	$0.062 + 0.014 \cdot SL$	$0.067 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$
	$t_{PHL}$	0.192	$0.171 + 0.011 \cdot SL$	$0.180 + 0.009 \cdot SL$	$0.194 + 0.008 \cdot SL$
CK to QN	$t_R$	0.086	$0.057 + 0.014 \cdot SL$	$0.057 + 0.014 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.085	$0.057 + 0.014 \cdot SL$	$0.061 + 0.013 \cdot SL$	$0.055 + 0.013 \cdot SL$
	$t_{PLH}$	0.529	$0.511 + 0.009 \cdot SL$	$0.518 + 0.007 \cdot SL$	$0.524 + 0.007 \cdot SL$
	$t_{PHL}$	0.568	$0.548 + 0.010 \cdot SL$	$0.556 + 0.008 \cdot SL$	$0.567 + 0.007 \cdot SL$
RN to QN	$t_R$	0.102	$0.072 + 0.015 \cdot SL$	$0.072 + 0.015 \cdot SL$	$0.070 + 0.015 \cdot SL$
	$t_{PLH}$	0.321	$0.301 + 0.010 \cdot SL$	$0.308 + 0.008 \cdot SL$	$0.323 + 0.007 \cdot SL$

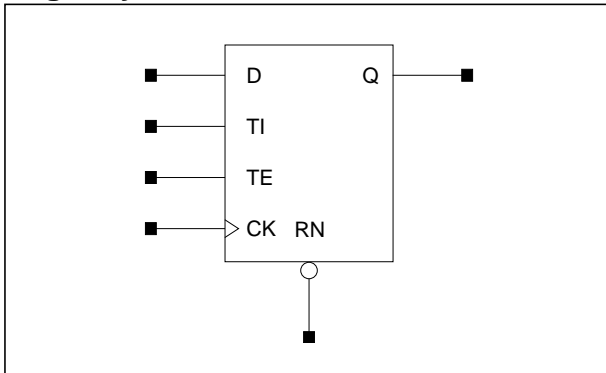
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FD2SQ/FD2SQD2

### D Flip-Flop with Reset, Scan, Q Output Only, 1X/2X Drive

#### Logic Symbol



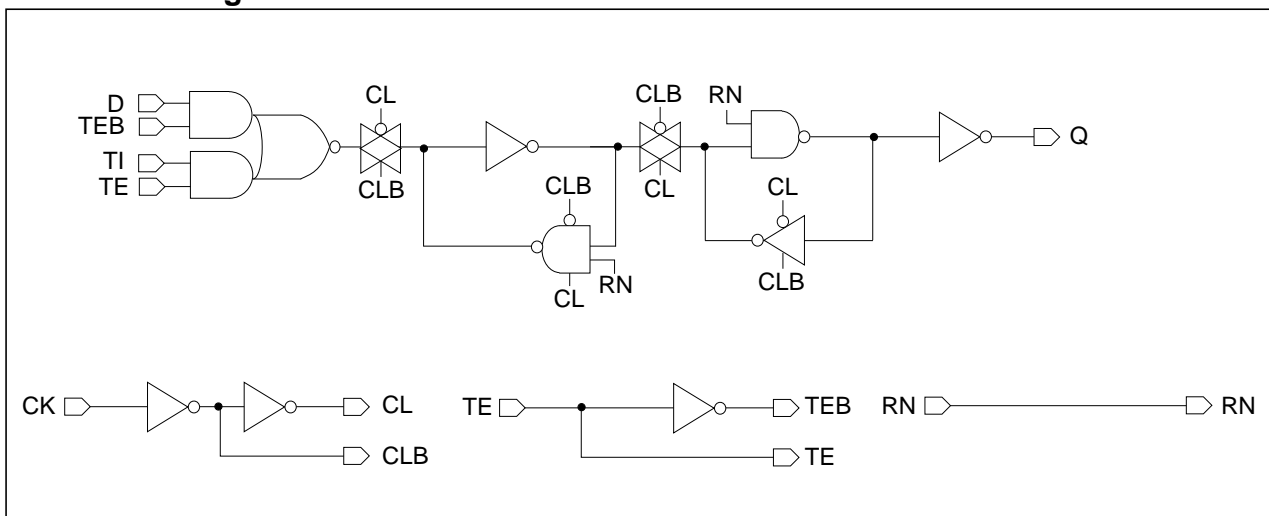
#### Truth Table

D	TI	TE	CK	RN	Q (n+1)
0	x	0		1	0
1	x	0		1	1
x	0	1		1	0
x	1	1		1	1
x	x	x	x	0	0
x	x	x		1	Q(n)

#### Cell Data

Input Load (SL)										Gate Count	
FD2SQ					FD2SQD2					FD2SQ	FD2SQD2
D	CK	RN	TI	TE	D	CK	RN	TI	TE		
0.5	0.6	1.3	0.5	1.2	0.5	0.6	1.3	0.5	1.2	7.00	7.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2SQ	FD2SQD2
Input Setup Time (D to CK)	$t_{SU}$	0.410	0.411
Input Hold Time (D to CK)	$t_{HD}$	0.125	0.117
Input Setup Time (TI to CK)	$t_{SU}$	0.496	0.496
Input Hold Time (TI to CK)	$t_{HD}$	0.129	0.123
Input Setup Time (TE to CK)	$t_{SU}$	0.529	0.531
Input Hold Time (TE to CK)	$t_{HD}$	0.126	0.122
Pulse Width Low (CK)	$t_{PWL}$	0.479	0.477
Pulse Width High (CK)	$t_{PWH}$	0.331	0.347
Pulse Width Low (RN)	$t_{PWL}$	0.218	0.236
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.777	0.778



## FD2SQ/FD2SQD2

### D Flip-Flop with Reset, Scan, Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD2SQ

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.129	$0.071 + 0.029 \cdot SL$	$0.067 + 0.030 \cdot SL$	$0.062 + 0.030 \cdot SL$
	$t_F$	0.106	$0.055 + 0.025 \cdot SL$	$0.056 + 0.025 \cdot SL$	$0.049 + 0.026 \cdot SL$
	$t_{PLH}$	0.422	$0.390 + 0.016 \cdot SL$	$0.398 + 0.014 \cdot SL$	$0.403 + 0.014 \cdot SL$
	$t_{PHL}$	0.412	$0.379 + 0.016 \cdot SL$	$0.387 + 0.014 \cdot SL$	$0.392 + 0.014 \cdot SL$
RN to Q	$t_F$	0.109	$0.061 + 0.024 \cdot SL$	$0.058 + 0.025 \cdot SL$	$0.052 + 0.026 \cdot SL$
	$t_{PHL}$	0.179	$0.146 + 0.016 \cdot SL$	$0.154 + 0.014 \cdot SL$	$0.159 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD2SQD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.102	$0.073 + 0.015 \cdot SL$	$0.073 + 0.015 \cdot SL$	$0.067 + 0.015 \cdot SL$
	$t_F$	0.085	$0.055 + 0.015 \cdot SL$	$0.061 + 0.013 \cdot SL$	$0.055 + 0.014 \cdot SL$
	$t_{PLH}$	0.429	$0.409 + 0.010 \cdot SL$	$0.418 + 0.008 \cdot SL$	$0.430 + 0.007 \cdot SL$
	$t_{PHL}$	0.414	$0.394 + 0.010 \cdot SL$	$0.402 + 0.008 \cdot SL$	$0.414 + 0.007 \cdot SL$
RN to Q	$t_F$	0.085	$0.057 + 0.014 \cdot SL$	$0.061 + 0.013 \cdot SL$	$0.055 + 0.013 \cdot SL$
	$t_{PHL}$	0.179	$0.159 + 0.010 \cdot SL$	$0.167 + 0.008 \cdot SL$	$0.179 + 0.007 \cdot SL$

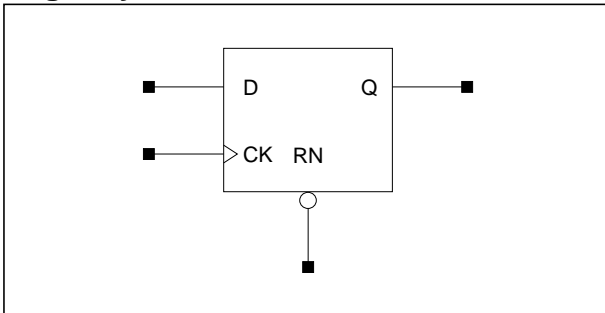
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$






## FD2Q/FD2QD2

### D Flip-Flop with Reset, Q Output Only, 1X/2X Drive

### Logic Symbol



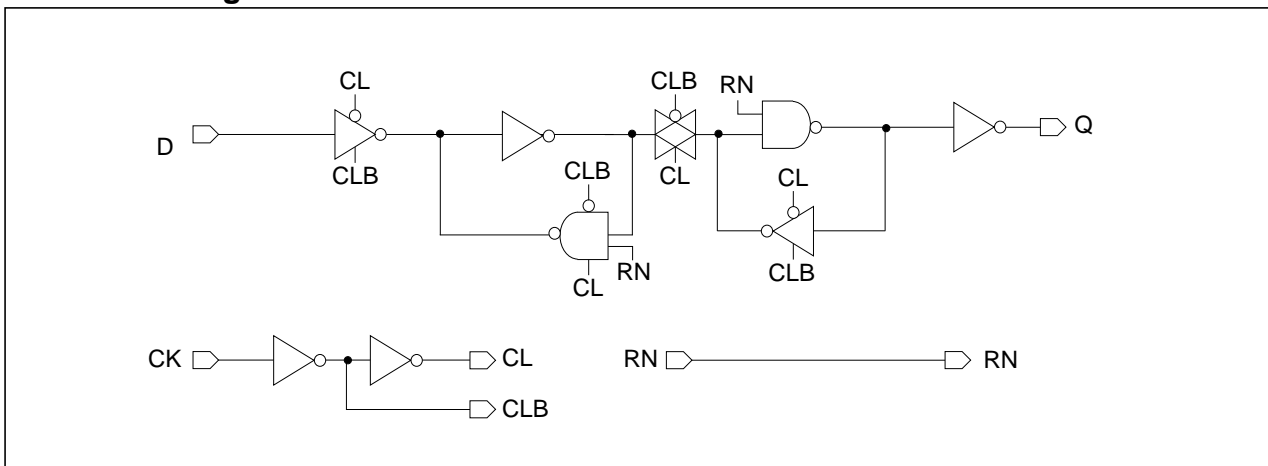
## Truth Table

D	CK	RN	Q (n+1)
0		1	0
1		1	1
x	x	0	0
x		x	Q (n)

## Cell Data

Input Load (SL)						Gate Count	
FD2Q			FD2QD2			FD2Q	FD2QD2
D	CK	RN	D	CK	RN		
0.6	0.6	1.4	0.6	0.6	1.4	5.33	5.67

### Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2Q	FD2QD2
Input Setup Time (D to CK)	t <sub>SU</sub>	0.273	0.261
Input Hold Time (D to CK)	t <sub>HD</sub>	0.162	0.175
Pulse Width Low (CK)	t <sub>PWL</sub>	0.359	0.351
Pulse Width High (CK)	t <sub>PWH</sub>	0.329	0.346
Pulse Width Low (RN)	t <sub>PWL</sub>	0.217	0.239
Recovery Time (RN to CK)	t <sub>RC</sub>	0.000	0.000
Removal Time (RN to CK)	t <sub>RM</sub>	0.831	0.810



## FD2Q/FD2QD2

### D Flip-Flop with Reset, Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD2Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.129	$0.073 + 0.028 \cdot SL$	$0.069 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.107	$0.057 + 0.025 \cdot SL$	$0.058 + 0.025 \cdot SL$	$0.051 + 0.026 \cdot SL$
	$t_{PLH}$	0.423	$0.391 + 0.016 \cdot SL$	$0.399 + 0.014 \cdot SL$	$0.405 + 0.013 \cdot SL$
	$t_{PHL}$	0.401	$0.368 + 0.016 \cdot SL$	$0.376 + 0.014 \cdot SL$	$0.381 + 0.014 \cdot SL$
RN to Q	$t_F$	0.108	$0.058 + 0.025 \cdot SL$	$0.058 + 0.025 \cdot SL$	$0.052 + 0.026 \cdot SL$
	$t_{PHL}$	0.179	$0.146 + 0.016 \cdot SL$	$0.154 + 0.014 \cdot SL$	$0.159 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

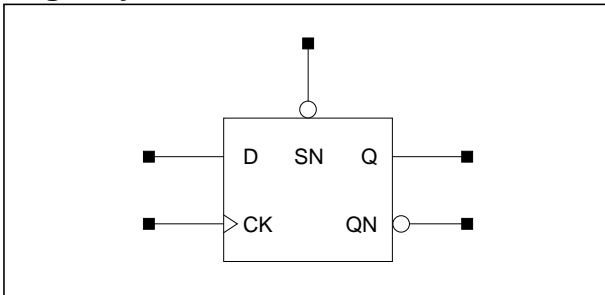
#### FD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.103	$0.072 + 0.015 \cdot SL$	$0.075 + 0.014 \cdot SL$	$0.068 + 0.015 \cdot SL$
	$t_F$	0.085	$0.056 + 0.014 \cdot SL$	$0.060 + 0.013 \cdot SL$	$0.057 + 0.013 \cdot SL$
	$t_{PLH}$	0.429	$0.409 + 0.010 \cdot SL$	$0.417 + 0.008 \cdot SL$	$0.430 + 0.007 \cdot SL$
	$t_{PHL}$	0.406	$0.386 + 0.010 \cdot SL$	$0.394 + 0.008 \cdot SL$	$0.406 + 0.007 \cdot SL$
RN to Q	$t_F$	0.085	$0.057 + 0.014 \cdot SL$	$0.062 + 0.013 \cdot SL$	$0.056 + 0.013 \cdot SL$
	$t_{PHL}$	0.181	$0.160 + 0.010 \cdot SL$	$0.168 + 0.008 \cdot SL$	$0.181 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## Logic Symbol



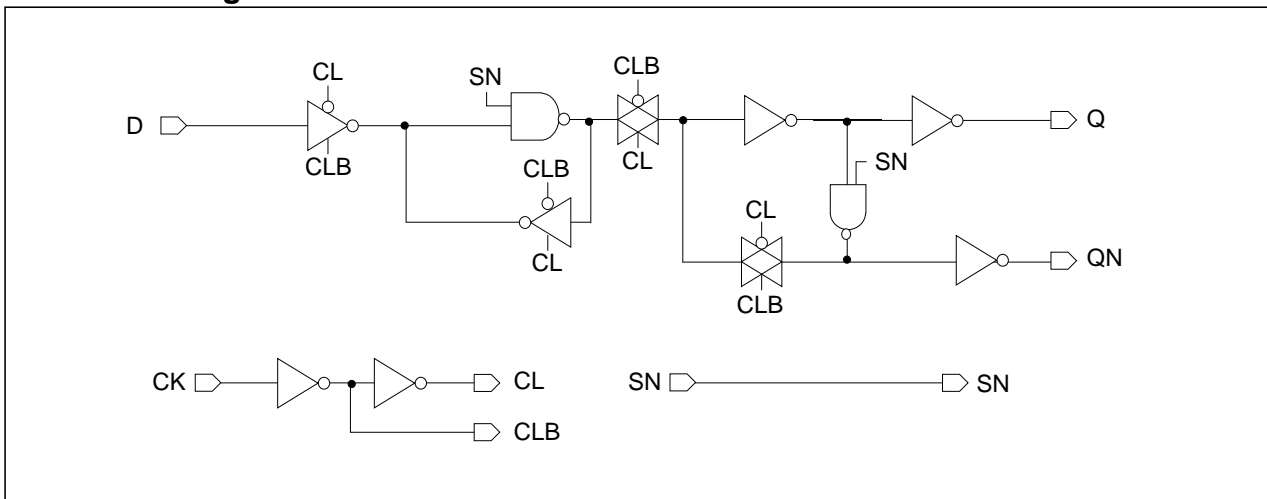
## Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0		1	0	1
1		1	1	0
x	x	0	1	0
x		1	Q (n)	QN (n)

## Cell Data

Input Load (SL)						Gate Count	
FD3			FD3D2			FD3	FD3D2
D	CK	SN	D	CK	SN		
0.5	0.5	1.5	0.5	0.5	1.5	5.67	6.33

## Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3	FD3D2
Input Setup Time (D to CK)	$t_{SU}$	0.272	0.271
Input Hold Time (D to CK)	$t_{HD}$	0.113	0.114
Pulse Width Low (CK)	$t_{PWL}$	0.378	0.378
Pulse Width High (CK)	$t_{PWH}$	0.317	0.339
Pulse Width Low (SN)	$t_{PWL}$	0.275	0.310
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.234	0.235



## FD3/FD3D2

### D Flip-Flop with Set, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.125	$0.069 + 0.028 \cdot SL$	$0.065 + 0.029 \cdot SL$	$0.057 + 0.030 \cdot SL$
	$t_F$	0.118	$0.064 + 0.027 \cdot SL$	$0.066 + 0.027 \cdot SL$	$0.062 + 0.027 \cdot SL$
	$t_{PLH}$	0.392	$0.362 + 0.015 \cdot SL$	$0.368 + 0.014 \cdot SL$	$0.371 + 0.013 \cdot SL$
	$t_{PHL}$	0.435	$0.400 + 0.018 \cdot SL$	$0.408 + 0.016 \cdot SL$	$0.415 + 0.015 \cdot SL$
SN to Q	$t_R$	0.128	$0.074 + 0.027 \cdot SL$	$0.067 + 0.029 \cdot SL$	$0.058 + 0.030 \cdot SL$
	$t_{PLH}$	0.364	$0.334 + 0.015 \cdot SL$	$0.341 + 0.014 \cdot SL$	$0.344 + 0.013 \cdot SL$
CK to QN	$t_R$	0.125	$0.068 + 0.029 \cdot SL$	$0.066 + 0.029 \cdot SL$	$0.061 + 0.030 \cdot SL$
	$t_F$	0.108	$0.058 + 0.025 \cdot SL$	$0.056 + 0.026 \cdot SL$	$0.051 + 0.026 \cdot SL$
	$t_{PLH}$	0.526	$0.495 + 0.016 \cdot SL$	$0.502 + 0.014 \cdot SL$	$0.508 + 0.013 \cdot SL$
	$t_{PHL}$	0.481	$0.448 + 0.017 \cdot SL$	$0.456 + 0.015 \cdot SL$	$0.461 + 0.014 \cdot SL$
SN to QN	$t_F$	0.124	$0.071 + 0.026 \cdot SL$	$0.074 + 0.025 \cdot SL$	$0.071 + 0.026 \cdot SL$
	$t_{PHL}$	0.211	$0.175 + 0.018 \cdot SL$	$0.184 + 0.016 \cdot SL$	$0.194 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.096	$0.068 + 0.014 \cdot SL$	$0.068 + 0.014 \cdot SL$	$0.057 + 0.015 \cdot SL$
	$t_F$	0.091	$0.063 + 0.014 \cdot SL$	$0.066 + 0.013 \cdot SL$	$0.064 + 0.013 \cdot SL$
	$t_{PLH}$	0.395	$0.376 + 0.009 \cdot SL$	$0.383 + 0.008 \cdot SL$	$0.392 + 0.007 \cdot SL$
	$t_{PHL}$	0.433	$0.412 + 0.011 \cdot SL$	$0.421 + 0.009 \cdot SL$	$0.434 + 0.008 \cdot SL$
SN to Q	$t_R$	0.100	$0.072 + 0.014 \cdot SL$	$0.073 + 0.014 \cdot SL$	$0.061 + 0.015 \cdot SL$
	$t_{PLH}$	0.398	$0.379 + 0.009 \cdot SL$	$0.387 + 0.008 \cdot SL$	$0.396 + 0.007 \cdot SL$
CK to QN	$t_R$	0.099	$0.070 + 0.015 \cdot SL$	$0.070 + 0.015 \cdot SL$	$0.067 + 0.015 \cdot SL$
	$t_F$	0.085	$0.058 + 0.014 \cdot SL$	$0.060 + 0.013 \cdot SL$	$0.057 + 0.013 \cdot SL$
	$t_{PLH}$	0.567	$0.547 + 0.010 \cdot SL$	$0.555 + 0.008 \cdot SL$	$0.568 + 0.007 \cdot SL$
	$t_{PHL}$	0.516	$0.495 + 0.010 \cdot SL$	$0.503 + 0.008 \cdot SL$	$0.515 + 0.007 \cdot SL$
SN to QN	$t_F$	0.100	$0.072 + 0.014 \cdot SL$	$0.074 + 0.014 \cdot SL$	$0.077 + 0.013 \cdot SL$
	$t_{PHL}$	0.209	$0.186 + 0.011 \cdot SL$	$0.196 + 0.009 \cdot SL$	$0.212 + 0.008 \cdot SL$

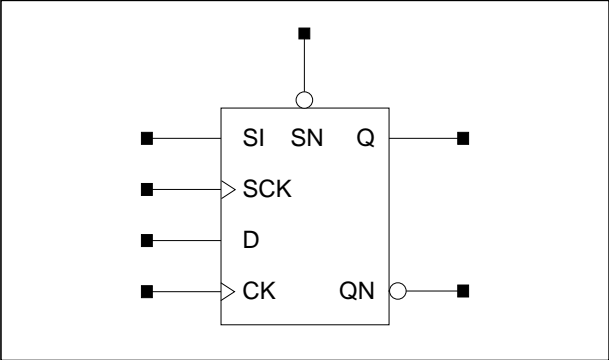
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



FD3CS/FD3CSD2

D Flip-Flop with Set, Scan Clock, 1X/2X Drive

Logic Symbol



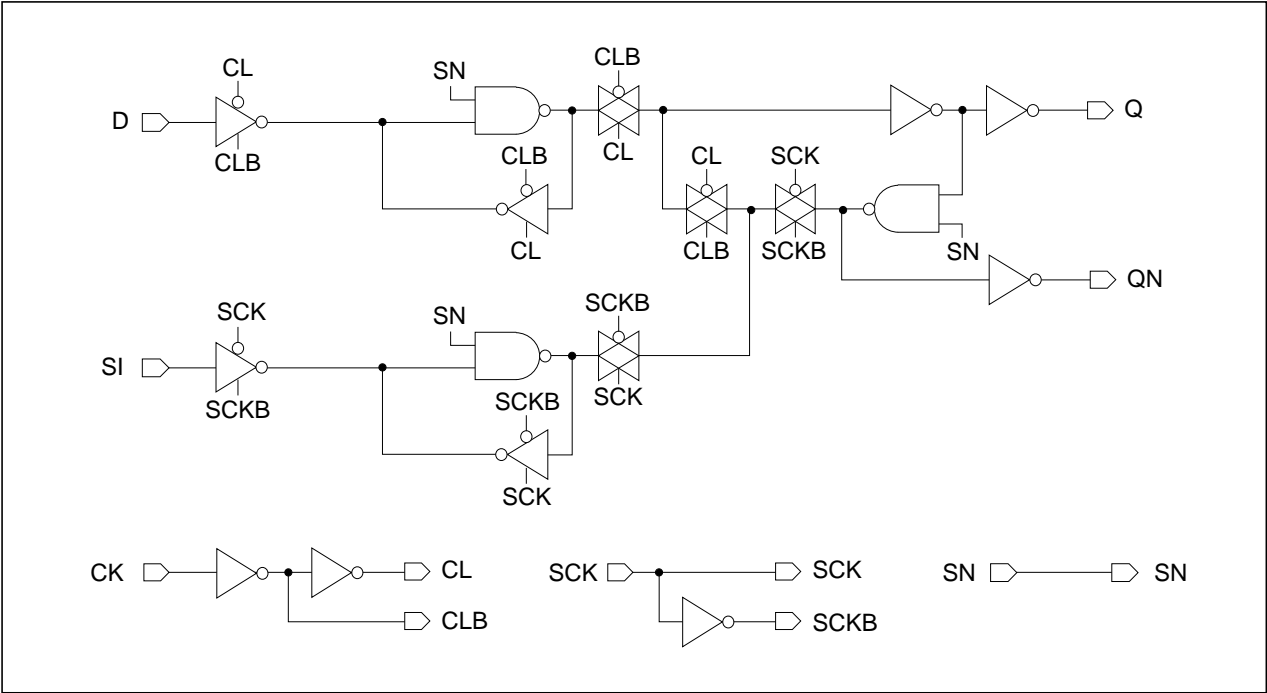
Truth Table

SI	SCK	D	CK	SN	Q (n+1)	QN (n+1)
x	0	0		1	0	1
x	0	1		1	1	0
0		x	0	1	0	1
1		x	0	1	1	0
x	x	x	x	0	1	0
x	0	x		1	Q(n)	QN(n)
x		x	0	1	Q(n)	QN(n)

Cell Data

Input Load (SL)										Gate Count	
FD3CS					FD3CSD2					FD3CS	FD3CSD2
D	SI	CK	SCK	SN	D	SI	CK	SCK	SN		
0.65	0.6	0.5	1.6	2.3	0.5	0.5	0.5	1.6	2.4	9.00	9.33

Schematic Diagram





## FD3CS/FD3CSD2

### D Flip-Flop with Set, Scan Clock, 1X/2X Drive

#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3CS	FD3CSD2
Input Setup Time (D to CK)	$t_{SU}$	0.272	0.272
Input Hold Time (D to CK)	$t_{HD}$	0.113	0.114
Input Setup Time (SI to SCK)	$t_{SU}$	0.782	0.784
Input Hold Time (SI to SCK)	$t_{HD}$	0.061	0.054
Pulse Width Low (CK)	$t_{PWL}$	0.377	0.378
Pulse Width High (CK)	$t_{PWH}$	0.330	0.356
Pulse Width Low (SCK)	$t_{PWL}$	0.309	0.311
Pulse Width High (SCK)	$t_{PWH}$	0.385	0.415
Pulse Width Low (SN)	$t_{PWL}$	0.354	0.389
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.236	0.236
Recovery Time (SN to SCK)	$t_{RC}$	0.220	0.219
RemovalTime (SN to SCK)	$t_{RM}$	0.008	0.009



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FD3CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.128	$0.071 + 0.028 \cdot SL$	$0.066 + 0.029 \cdot SL$	$0.058 + 0.030 \cdot SL$
	$t_F$	0.119	$0.066 + 0.026 \cdot SL$	$0.065 + 0.027 \cdot SL$	$0.062 + 0.027 \cdot SL$
	$t_{PLH}$	0.398	$0.368 + 0.015 \cdot SL$	$0.374 + 0.014 \cdot SL$	$0.377 + 0.014 \cdot SL$
	$t_{PHL}$	0.437	$0.402 + 0.018 \cdot SL$	$0.410 + 0.016 \cdot SL$	$0.416 + 0.015 \cdot SL$
SCK to Q	$t_R$	0.145	$0.090 + 0.028 \cdot SL$	$0.086 + 0.029 \cdot SL$	$0.074 + 0.030 \cdot SL$
	$t_F$	0.125	$0.072 + 0.027 \cdot SL$	$0.074 + 0.026 \cdot SL$	$0.069 + 0.027 \cdot SL$
	$t_{PLH}$	0.464	$0.432 + 0.016 \cdot SL$	$0.440 + 0.014 \cdot SL$	$0.446 + 0.014 \cdot SL$
	$t_{PHL}$	0.436	$0.400 + 0.018 \cdot SL$	$0.409 + 0.016 \cdot SL$	$0.417 + 0.015 \cdot SL$
SN to Q	$t_R$	0.147	$0.093 + 0.027 \cdot SL$	$0.088 + 0.028 \cdot SL$	$0.076 + 0.030 \cdot SL$
	$t_{PLH}$	0.510	$0.477 + 0.016 \cdot SL$	$0.486 + 0.014 \cdot SL$	$0.492 + 0.013 \cdot SL$
CK to QN	$t_R$	0.151	$0.092 + 0.029 \cdot SL$	$0.093 + 0.029 \cdot SL$	$0.091 + 0.029 \cdot SL$
	$t_F$	0.122	$0.069 + 0.026 \cdot SL$	$0.070 + 0.026 \cdot SL$	$0.069 + 0.026 \cdot SL$
	$t_{PLH}$	0.561	$0.525 + 0.018 \cdot SL$	$0.536 + 0.015 \cdot SL$	$0.549 + 0.014 \cdot SL$
	$t_{PHL}$	0.517	$0.481 + 0.018 \cdot SL$	$0.490 + 0.016 \cdot SL$	$0.498 + 0.015 \cdot SL$
SCK to QN	$t_R$	0.129	$0.073 + 0.028 \cdot SL$	$0.068 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.111	$0.061 + 0.025 \cdot SL$	$0.059 + 0.025 \cdot SL$	$0.055 + 0.026 \cdot SL$
	$t_{PLH}$	0.529	$0.497 + 0.016 \cdot SL$	$0.505 + 0.014 \cdot SL$	$0.510 + 0.013 \cdot SL$
	$t_{PHL}$	0.557	$0.524 + 0.017 \cdot SL$	$0.532 + 0.015 \cdot SL$	$0.537 + 0.014 \cdot SL$
SN to QN	$t_F$	0.134	$0.079 + 0.028 \cdot SL$	$0.083 + 0.027 \cdot SL$	$0.087 + 0.026 \cdot SL$
	$t_{PHL}$	0.229	$0.191 + 0.019 \cdot SL$	$0.200 + 0.017 \cdot SL$	$0.212 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## FD3CS/FD3CSD2

### D Flip-Flop with Set, Scan Clock, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD3CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.098	$0.069 + 0.014 \cdot SL$	$0.070 + 0.014 \cdot SL$	$0.058 + 0.015 \cdot SL$
	$t_F$	0.093	$0.066 + 0.014 \cdot SL$	$0.068 + 0.013 \cdot SL$	$0.064 + 0.013 \cdot SL$
	$t_{PLH}$	0.405	$0.386 + 0.009 \cdot SL$	$0.393 + 0.008 \cdot SL$	$0.402 + 0.007 \cdot SL$
	$t_{PHL}$	0.439	$0.418 + 0.011 \cdot SL$	$0.427 + 0.008 \cdot SL$	$0.440 + 0.008 \cdot SL$
SCK to Q	$t_R$	0.117	$0.090 + 0.014 \cdot SL$	$0.089 + 0.014 \cdot SL$	$0.079 + 0.015 \cdot SL$
	$t_F$	0.100	$0.073 + 0.014 \cdot SL$	$0.075 + 0.013 \cdot SL$	$0.072 + 0.013 \cdot SL$
	$t_{PLH}$	0.477	$0.457 + 0.010 \cdot SL$	$0.467 + 0.008 \cdot SL$	$0.479 + 0.007 \cdot SL$
	$t_{PHL}$	0.443	$0.421 + 0.011 \cdot SL$	$0.430 + 0.009 \cdot SL$	$0.443 + 0.008 \cdot SL$
SN to Q	$t_R$	0.122	$0.095 + 0.014 \cdot SL$	$0.094 + 0.014 \cdot SL$	$0.082 + 0.015 \cdot SL$
	$t_{PLH}$	0.553	$0.532 + 0.010 \cdot SL$	$0.542 + 0.008 \cdot SL$	$0.556 + 0.007 \cdot SL$
CK to QN	$t_R$	0.122	$0.091 + 0.015 \cdot SL$	$0.092 + 0.015 \cdot SL$	$0.093 + 0.015 \cdot SL$
	$t_F$	0.097	$0.067 + 0.015 \cdot SL$	$0.072 + 0.013 \cdot SL$	$0.071 + 0.014 \cdot SL$
	$t_{PLH}$	0.601	$0.578 + 0.012 \cdot SL$	$0.589 + 0.009 \cdot SL$	$0.608 + 0.007 \cdot SL$
	$t_{PHL}$	0.553	$0.530 + 0.011 \cdot SL$	$0.539 + 0.009 \cdot SL$	$0.554 + 0.008 \cdot SL$
SCK to QN	$t_R$	0.102	$0.073 + 0.014 \cdot SL$	$0.073 + 0.015 \cdot SL$	$0.068 + 0.015 \cdot SL$
	$t_F$	0.088	$0.061 + 0.013 \cdot SL$	$0.063 + 0.013 \cdot SL$	$0.058 + 0.013 \cdot SL$
	$t_{PLH}$	0.576	$0.556 + 0.010 \cdot SL$	$0.564 + 0.008 \cdot SL$	$0.577 + 0.007 \cdot SL$
	$t_{PHL}$	0.604	$0.583 + 0.010 \cdot SL$	$0.591 + 0.008 \cdot SL$	$0.604 + 0.007 \cdot SL$
SN to QN	$t_F$	0.108	$0.079 + 0.015 \cdot SL$	$0.081 + 0.014 \cdot SL$	$0.088 + 0.014 \cdot SL$
	$t_{PHL}$	0.226	$0.201 + 0.012 \cdot SL$	$0.212 + 0.009 \cdot SL$	$0.229 + 0.008 \cdot SL$

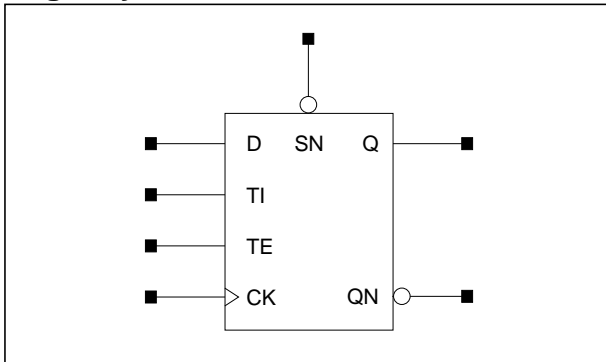
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# FD3S/FD3SD2

## D Flip-Flop with Set, Scan, 1X/2X Drive

### Logic Symbol



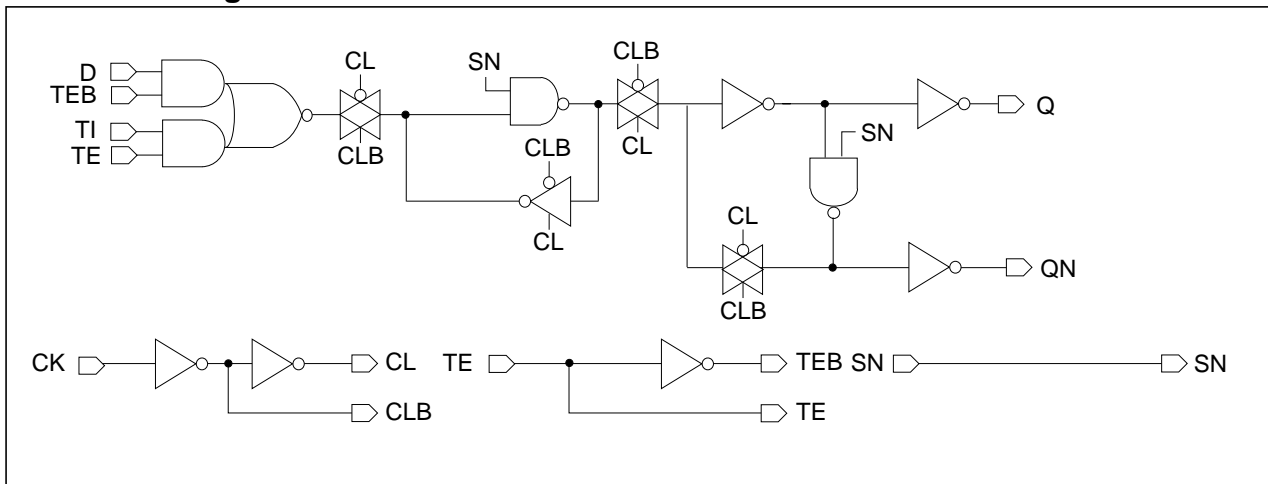
### Truth Table

D	TI	TE	CK	SN	Q (n+1)	QN (n+1)
0	x	0		1	0	1
1	x	0		1	1	0
x	0	1		1	0	1
x	1	1		1	1	0
x	x	x	x	0	1	0
x	x	x		1	Q (n)	QN (n)

### Cell Data

Input Load (SL)										Gate Count	
FD3S					FD3SD2					FD3S	FD3SD2
D	CK	SN	TI	TE	D	CK	SN	TI	TE		
0.5	0.5	1.5	0.6	1.1	0.5	0.5	1.5	0.5	1.1	7.33	8.00

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3S	FD3SD2
Input Setup Time (D to CK)	$t_{SU}$	0.457	0.451
Input Hold Time (D to CK)	$t_{HD}$	0.000	0.003
Pulse Width Low (CK)	$t_{PWL}$	0.515	0.504
Pulse Width High (CK)	$t_{PWH}$	0.319	0.341
Pulse Width Low (SN)	$t_{PWL}$	0.275	0.309
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.241	0.244
Input Setup Time (TI to CK)	$t_{SU}$	0.358	0.346
Input Hold Time (TI to CK)	$t_{HD}$	0.027	0.036
Input Setup Time (TE to CK)	$t_{SU}$	0.385	0.379
Input Hold Time (TE to CK)	$t_{HD}$	0.011	0.020



## FD3S/FD3SD2

### D Flip-Flop with Set, Scan, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD3S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.125	$0.069 + 0.028 \cdot SL$	$0.064 + 0.029 \cdot SL$	$0.057 + 0.030 \cdot SL$
	$t_F$	0.118	$0.064 + 0.027 \cdot SL$	$0.066 + 0.027 \cdot SL$	$0.062 + 0.027 \cdot SL$
	$t_{PLH}$	0.398	$0.367 + 0.015 \cdot SL$	$0.373 + 0.014 \cdot SL$	$0.376 + 0.013 \cdot SL$
	$t_{PHL}$	0.440	$0.405 + 0.017 \cdot SL$	$0.412 + 0.016 \cdot SL$	$0.419 + 0.015 \cdot SL$
SN to Q	$t_R$	0.128	$0.074 + 0.027 \cdot SL$	$0.066 + 0.029 \cdot SL$	$0.058 + 0.030 \cdot SL$
	$t_{PLH}$	0.363	$0.333 + 0.015 \cdot SL$	$0.340 + 0.014 \cdot SL$	$0.342 + 0.013 \cdot SL$
CK to QN	$t_R$	0.127	$0.069 + 0.029 \cdot SL$	$0.069 + 0.029 \cdot SL$	$0.062 + 0.030 \cdot SL$
	$t_F$	0.112	$0.060 + 0.026 \cdot SL$	$0.057 + 0.027 \cdot SL$	$0.052 + 0.027 \cdot SL$
	$t_{PLH}$	0.531	$0.499 + 0.016 \cdot SL$	$0.507 + 0.014 \cdot SL$	$0.513 + 0.013 \cdot SL$
	$t_{PHL}$	0.490	$0.456 + 0.017 \cdot SL$	$0.464 + 0.015 \cdot SL$	$0.468 + 0.015 \cdot SL$
SN to QN	$t_F$	0.127	$0.071 + 0.028 \cdot SL$	$0.077 + 0.026 \cdot SL$	$0.073 + 0.027 \cdot SL$
	$t_{PHL}$	0.215	$0.177 + 0.019 \cdot SL$	$0.187 + 0.016 \cdot SL$	$0.197 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD3SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.095	$0.066 + 0.015 \cdot SL$	$0.067 + 0.014 \cdot SL$	$0.059 + 0.015 \cdot SL$
	$t_F$	0.092	$0.064 + 0.014 \cdot SL$	$0.066 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	$t_{PLH}$	0.402	$0.383 + 0.009 \cdot SL$	$0.390 + 0.008 \cdot SL$	$0.399 + 0.007 \cdot SL$
	$t_{PHL}$	0.437	$0.416 + 0.011 \cdot SL$	$0.425 + 0.009 \cdot SL$	$0.437 + 0.008 \cdot SL$
SN to Q	$t_R$	0.101	$0.073 + 0.014 \cdot SL$	$0.073 + 0.014 \cdot SL$	$0.061 + 0.015 \cdot SL$
	$t_{PLH}$	0.398	$0.379 + 0.009 \cdot SL$	$0.387 + 0.008 \cdot SL$	$0.396 + 0.007 \cdot SL$
CK to QN	$t_R$	0.101	$0.071 + 0.015 \cdot SL$	$0.071 + 0.015 \cdot SL$	$0.067 + 0.015 \cdot SL$
	$t_F$	0.085	$0.056 + 0.015 \cdot SL$	$0.062 + 0.013 \cdot SL$	$0.057 + 0.013 \cdot SL$
	$t_{PLH}$	0.571	$0.551 + 0.010 \cdot SL$	$0.559 + 0.008 \cdot SL$	$0.572 + 0.007 \cdot SL$
	$t_{PHL}$	0.523	$0.502 + 0.010 \cdot SL$	$0.510 + 0.008 \cdot SL$	$0.523 + 0.007 \cdot SL$
SN to QN	$t_F$	0.100	$0.072 + 0.014 \cdot SL$	$0.074 + 0.014 \cdot SL$	$0.077 + 0.013 \cdot SL$
	$t_{PHL}$	0.209	$0.186 + 0.011 \cdot SL$	$0.196 + 0.009 \cdot SL$	$0.213 + 0.008 \cdot SL$

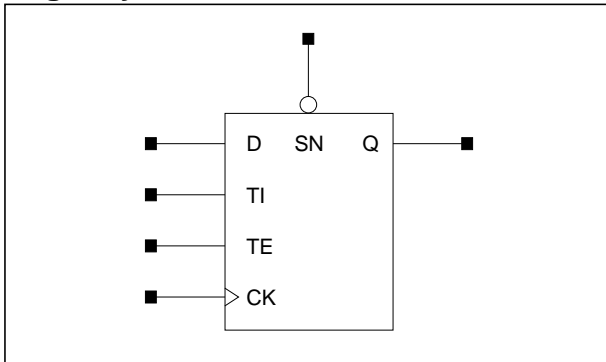
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FD3SQ/FD3SQD2

### D Flip-Flop with Set, Scan, Q Output Only, 1X/2X Drive

#### Logic Symbol



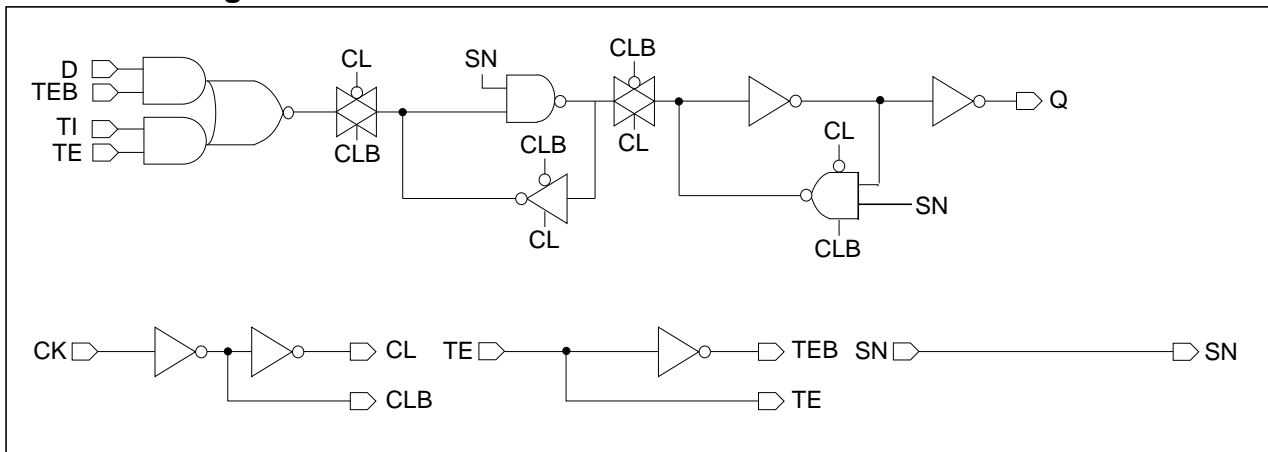
#### Truth Table

D	TI	TE	CK	SN	Q (n+1)
0	x	0		1	0
1	x	0		1	1
x	0	1		1	0
x	1	1		1	1
x	x	x	x	0	1
x	x	x		1	Q (n)

#### Cell Data

Input Load (SL)										Gate Count	
FD3SQ					FD3SQD2					FD3SQ	FD3SQD2
D	CK	SN	TI	TE	D	CK	SN	TI	TE		
0.5	0.5	1.1	0.5	1.1	0.5	0.5	1.1	0.5	1.1	7.00	7.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3SQ	FD3SQD2
Input Setup Time (D to CK)	$t_{SU}$	0.458	0.458
Input Hold Time (D to CK)	$t_{HD}$	0.000	0.000
Pulse Width Low (CK)	$t_{PWL}$	0.512	0.511
Pulse Width High (CK)	$t_{PWH}$	0.305	0.318
Pulse Width Low (SN)	$t_{PWL}$	0.553	0.577
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.242	0.244
Input Setup Time (TI to CK)	$t_{SU}$	0.353	0.352
Input Hold Time (TI to CK)	$t_{HD}$	0.029	0.029
Input Setup Time (TE to CK)	$t_{SU}$	0.382	0.382
Input Hold Time (TE to CK)	$t_{HD}$	0.010	0.011



## FD3SQ/FD3SQD2

### D Flip-Flop with Set, Scan, Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### FD3SQ

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.119	$0.062 + 0.029 \cdot SL$	$0.057 + 0.030 \cdot SL$	$0.050 + 0.031 \cdot SL$
	$t_F$	0.108	$0.058 + 0.025 \cdot SL$	$0.059 + 0.025 \cdot SL$	$0.051 + 0.026 \cdot SL$
	$t_{PLH}$	0.378	$0.348 + 0.015 \cdot SL$	$0.354 + 0.014 \cdot SL$	$0.356 + 0.013 \cdot SL$
	$t_{PHL}$	0.425	$0.392 + 0.016 \cdot SL$	$0.400 + 0.014 \cdot SL$	$0.405 + 0.014 \cdot SL$
SN to Q	$t_R$	0.134	$0.079 + 0.027 \cdot SL$	$0.073 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_{PLH}$	0.603	$0.572 + 0.016 \cdot SL$	$0.579 + 0.014 \cdot SL$	$0.582 + 0.013 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### FD3SQD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.093	$0.064 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.052 + 0.015 \cdot SL$
	$t_F$	0.089	$0.063 + 0.013 \cdot SL$	$0.067 + 0.012 \cdot SL$	$0.062 + 0.013 \cdot SL$
	$t_{PLH}$	0.386	$0.368 + 0.009 \cdot SL$	$0.375 + 0.007 \cdot SL$	$0.383 + 0.007 \cdot SL$
	$t_{PHL}$	0.435	$0.415 + 0.010 \cdot SL$	$0.424 + 0.008 \cdot SL$	$0.437 + 0.007 \cdot SL$
SN to Q	$t_R$	0.109	$0.082 + 0.014 \cdot SL$	$0.081 + 0.014 \cdot SL$	$0.067 + 0.015 \cdot SL$
	$t_{PLH}$	0.608	$0.587 + 0.010 \cdot SL$	$0.598 + 0.008 \cdot SL$	$0.609 + 0.007 \cdot SL$

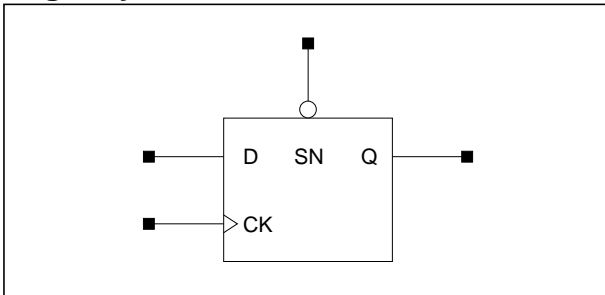
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FD3Q/FD3QD2

### D Flip-Flop with Set, Q Output Only, 1X/2X Drive

#### Logic Symbol



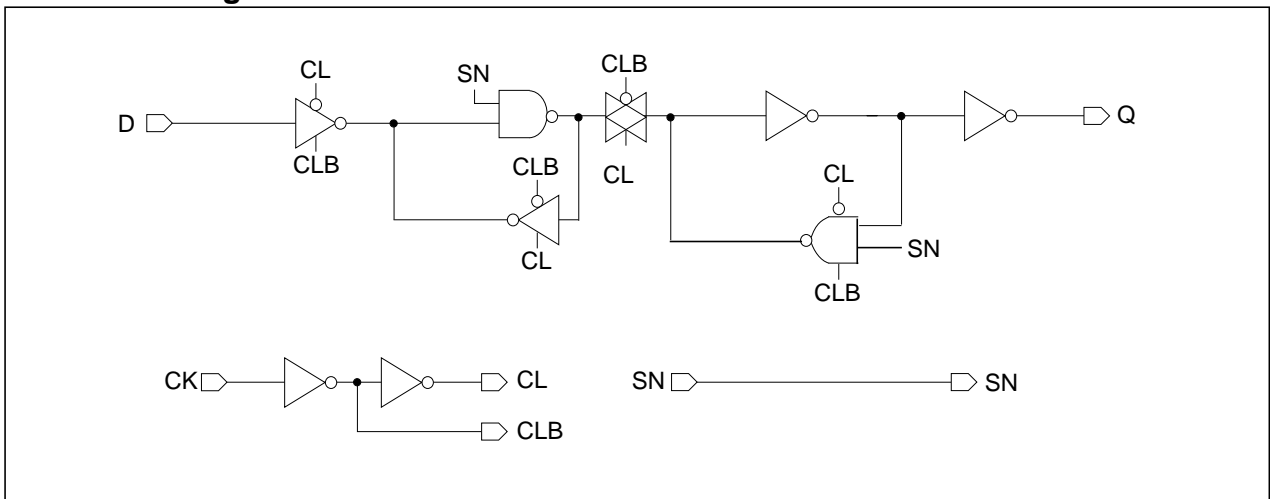
#### Truth Table

D	CK	SN	Q (n+1)
0		1	0
1		1	1
x	x	0	1
x		x	Q (n)

#### Cell Data

Input Load (SL)						Gate Count	
FD3Q			FD3QD2			FD3Q	FD3QD2
D	CK	SN	D	CK	SN		
0.5	0.5	1.1	0.5	0.5	1.1	5.33	5.67

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3Q	FD3QD2
Input Setup Time (D to CK)	$t_{SU}$	0.271	0.271
Input Hold Time (D to CK)	$t_{HD}$	0.110	0.110
Pulse Width Low (CK)	$t_{PWL}$	0.374	0.374
Pulse Width High (CK)	$t_{PWH}$	0.298	0.312
Pulse Width Low (SN)	$t_{PWL}$	0.525	0.549
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.243	0.243



## FD3Q/FD3QD2

### D Flip-Flop with Set, Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD3Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.118	$0.061 + 0.029 \cdot SL$	$0.057 + 0.030 \cdot SL$	$0.050 + 0.030 \cdot SL$
	$t_F$	0.107	$0.056 + 0.025 \cdot SL$	$0.058 + 0.025 \cdot SL$	$0.051 + 0.026 \cdot SL$
	$t_{PLH}$	0.370	$0.340 + 0.015 \cdot SL$	$0.346 + 0.014 \cdot SL$	$0.348 + 0.013 \cdot SL$
	$t_{PHL}$	0.405	$0.372 + 0.016 \cdot SL$	$0.380 + 0.014 \cdot SL$	$0.385 + 0.014 \cdot SL$
SN to Q	$t_R$	0.132	$0.078 + 0.027 \cdot SL$	$0.072 + 0.029 \cdot SL$	$0.062 + 0.030 \cdot SL$
	$t_{PLH}$	0.563	$0.532 + 0.016 \cdot SL$	$0.539 + 0.014 \cdot SL$	$0.542 + 0.013 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

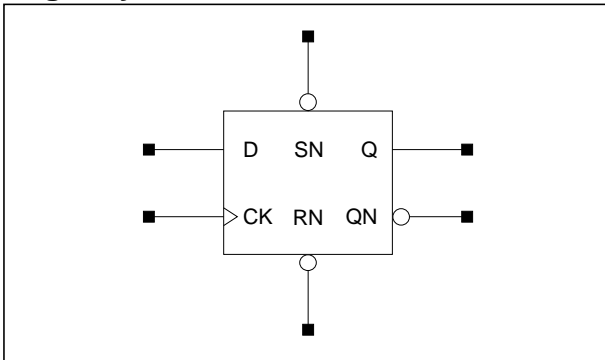
#### FD3QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.091	$0.063 + 0.014 \cdot SL$	$0.061 + 0.015 \cdot SL$	$0.053 + 0.015 \cdot SL$
	$t_F$	0.085	$0.059 + 0.013 \cdot SL$	$0.063 + 0.012 \cdot SL$	$0.057 + 0.013 \cdot SL$
	$t_{PLH}$	0.378	$0.360 + 0.009 \cdot SL$	$0.366 + 0.007 \cdot SL$	$0.374 + 0.007 \cdot SL$
	$t_{PHL}$	0.410	$0.390 + 0.010 \cdot SL$	$0.398 + 0.008 \cdot SL$	$0.411 + 0.007 \cdot SL$
SN to Q	$t_R$	0.107	$0.079 + 0.014 \cdot SL$	$0.079 + 0.014 \cdot SL$	$0.066 + 0.015 \cdot SL$
	$t_{PLH}$	0.576	$0.557 + 0.009 \cdot SL$	$0.565 + 0.007 \cdot SL$	$0.574 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## Logic Symbol



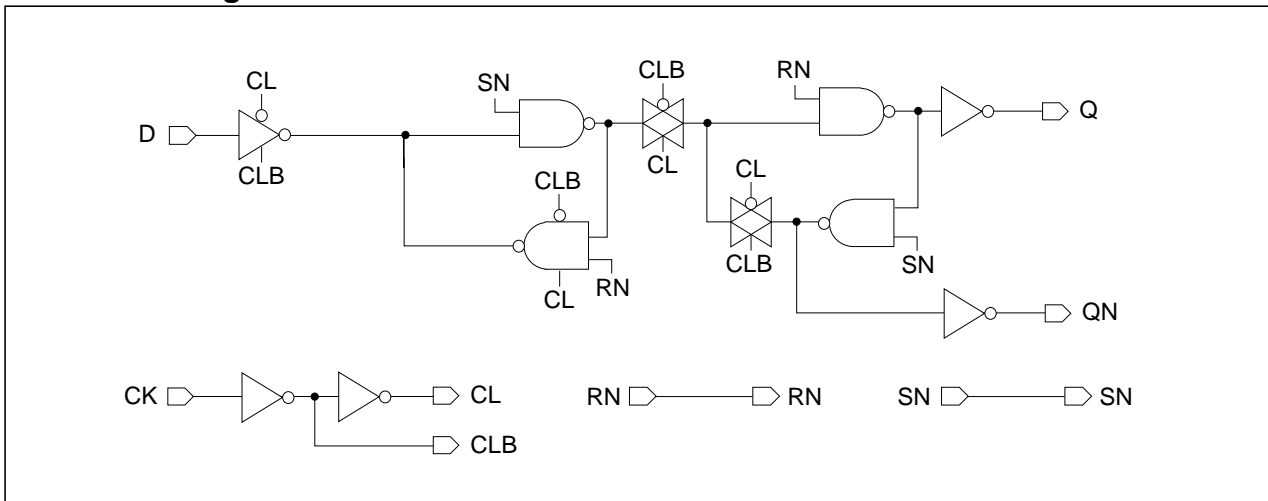
## Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0		1	1	0	1
1		1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x		1	1	Q (n)	QN (n)

## Cell Data

Input Load (SL)								Gate Count	
FD4				FD4D2				FD4	FD4D2
D	CK	RN	SN	D	CK	RN	SN		
0.6	0.5	1.5	1.6	0.5	0.5	1.5	1.5	6.67	7.00

## Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4	FD4D2
Input Setup Time (D to CK)	$t_{SU}$	0.258	0.255
Input Hold Time (D to CK)	$t_{HD}$	0.168	0.189
Pulse Width Low (CK)	$t_{PWL}$	0.377	0.372
Pulse Width High (CK)	$t_{PWH}$	0.337	0.364
Pulse Width Low (RN)	$t_{PWL}$	0.278	0.316
Pulse Width Low (SN)	$t_{PWL}$	0.287	0.327
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.818	0.802
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.270	0.281
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000
Recovery Time (SN to RN)	$t_{RC}$	0.231	0.221



## FD4/FD4D2

### D Flip-Flop with Reset, Set, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.137	$0.078 + 0.030 \cdot SL$	$0.078 + 0.029 \cdot SL$	$0.072 + 0.030 \cdot SL$
	$t_F$	0.116	$0.065 + 0.025 \cdot SL$	$0.067 + 0.025 \cdot SL$	$0.063 + 0.026 \cdot SL$
	$t_{PLH}$	0.433	$0.399 + 0.017 \cdot SL$	$0.407 + 0.015 \cdot SL$	$0.415 + 0.014 \cdot SL$
	$t_{PHL}$	0.440	$0.406 + 0.017 \cdot SL$	$0.414 + 0.015 \cdot SL$	$0.422 + 0.014 \cdot SL$
RN to Q	$t_R$	0.131	$0.072 + 0.029 \cdot SL$	$0.070 + 0.030 \cdot SL$	$0.065 + 0.030 \cdot SL$
	$t_F$	0.113	$0.062 + 0.026 \cdot SL$	$0.065 + 0.025 \cdot SL$	$0.061 + 0.026 \cdot SL$
	$t_{PLH}$	0.177	$0.144 + 0.016 \cdot SL$	$0.153 + 0.014 \cdot SL$	$0.159 + 0.014 \cdot SL$
	$t_{PHL}$	0.195	$0.161 + 0.017 \cdot SL$	$0.170 + 0.015 \cdot SL$	$0.176 + 0.014 \cdot SL$
SN to Q	$t_R$	0.138	$0.081 + 0.028 \cdot SL$	$0.078 + 0.029 \cdot SL$	$0.071 + 0.030 \cdot SL$
	$t_{PLH}$	0.392	$0.359 + 0.017 \cdot SL$	$0.368 + 0.014 \cdot SL$	$0.374 + 0.014 \cdot SL$
CK to QN	$t_R$	0.125	$0.068 + 0.029 \cdot SL$	$0.065 + 0.029 \cdot SL$	$0.060 + 0.030 \cdot SL$
	$t_F$	0.112	$0.060 + 0.026 \cdot SL$	$0.058 + 0.027 \cdot SL$	$0.052 + 0.027 \cdot SL$
	$t_{PLH}$	0.536	$0.504 + 0.016 \cdot SL$	$0.512 + 0.014 \cdot SL$	$0.517 + 0.013 \cdot SL$
	$t_{PHL}$	0.525	$0.490 + 0.017 \cdot SL$	$0.499 + 0.015 \cdot SL$	$0.504 + 0.015 \cdot SL$
RN to QN	$t_R$	0.148	$0.087 + 0.030 \cdot SL$	$0.093 + 0.029 \cdot SL$	$0.090 + 0.029 \cdot SL$
	$t_{PLH}$	0.332	$0.294 + 0.019 \cdot SL$	$0.307 + 0.016 \cdot SL$	$0.321 + 0.014 \cdot SL$
SN to QN	$t_R$	0.145	$0.084 + 0.030 \cdot SL$	$0.088 + 0.029 \cdot SL$	$0.087 + 0.029 \cdot SL$
	$t_F$	0.125	$0.071 + 0.027 \cdot SL$	$0.072 + 0.027 \cdot SL$	$0.071 + 0.027 \cdot SL$
	$t_{PLH}$	0.198	$0.161 + 0.019 \cdot SL$	$0.173 + 0.016 \cdot SL$	$0.187 + 0.014 \cdot SL$
	$t_{PHL}$	0.214	$0.177 + 0.019 \cdot SL$	$0.187 + 0.016 \cdot SL$	$0.197 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.109	$0.079 + 0.015*SL$	$0.079 + 0.015*SL$	$0.076 + 0.015*SL$
	$t_F$	0.093	$0.066 + 0.014*SL$	$0.068 + 0.013*SL$	$0.066 + 0.013*SL$
	$t_{PLH}$	0.435	$0.415 + 0.010*SL$	$0.424 + 0.008*SL$	$0.438 + 0.007*SL$
	$t_{PHL}$	0.444	$0.422 + 0.011*SL$	$0.431 + 0.009*SL$	$0.444 + 0.008*SL$
RN to Q	$t_R$	0.101	$0.073 + 0.014*SL$	$0.071 + 0.015*SL$	$0.068 + 0.015*SL$
	$t_F$	0.091	$0.061 + 0.015*SL$	$0.068 + 0.013*SL$	$0.064 + 0.013*SL$
	$t_{PLH}$	0.178	$0.157 + 0.010*SL$	$0.166 + 0.008*SL$	$0.180 + 0.007*SL$
	$t_{PHL}$	0.192	$0.170 + 0.011*SL$	$0.179 + 0.009*SL$	$0.193 + 0.008*SL$
SN to Q	$t_R$	0.110	$0.081 + 0.015*SL$	$0.082 + 0.014*SL$	$0.076 + 0.015*SL$
	$t_{PLH}$	0.431	$0.410 + 0.010*SL$	$0.419 + 0.008*SL$	$0.433 + 0.007*SL$
CK to QN	$t_R$	0.101	$0.071 + 0.015*SL$	$0.072 + 0.015*SL$	$0.066 + 0.015*SL$
	$t_F$	0.089	$0.060 + 0.014*SL$	$0.065 + 0.013*SL$	$0.060 + 0.013*SL$
	$t_{PLH}$	0.578	$0.558 + 0.010*SL$	$0.567 + 0.008*SL$	$0.580 + 0.007*SL$
	$t_{PHL}$	0.563	$0.542 + 0.011*SL$	$0.551 + 0.008*SL$	$0.563 + 0.007*SL$
RN to QN	$t_R$	0.122	$0.091 + 0.015*SL$	$0.092 + 0.015*SL$	$0.095 + 0.015*SL$
	$t_{PLH}$	0.367	$0.343 + 0.012*SL$	$0.355 + 0.009*SL$	$0.375 + 0.007*SL$
SN to QN	$t_R$	0.117	$0.085 + 0.016*SL$	$0.087 + 0.015*SL$	$0.091 + 0.015*SL$
	$t_F$	0.101	$0.072 + 0.015*SL$	$0.076 + 0.013*SL$	$0.077 + 0.013*SL$
	$t_{PLH}$	0.201	$0.178 + 0.012*SL$	$0.189 + 0.009*SL$	$0.208 + 0.007*SL$
	$t_{PHL}$	0.213	$0.190 + 0.012*SL$	$0.200 + 0.009*SL$	$0.217 + 0.008*SL$

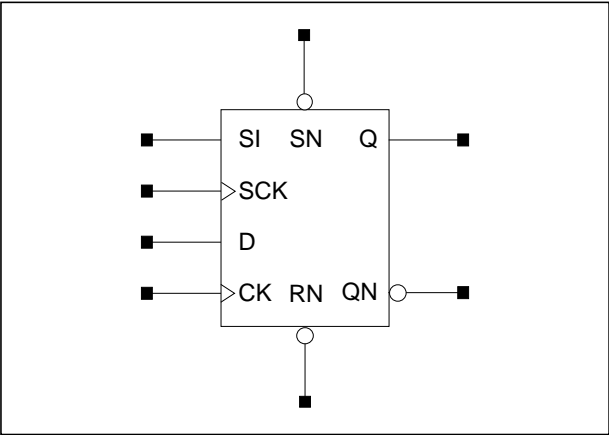
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



FD4CS/FD4CSD2

D Flip-Flop with Reset, Set, Scan Clock, 1X/2X Drive

Logic Symbol



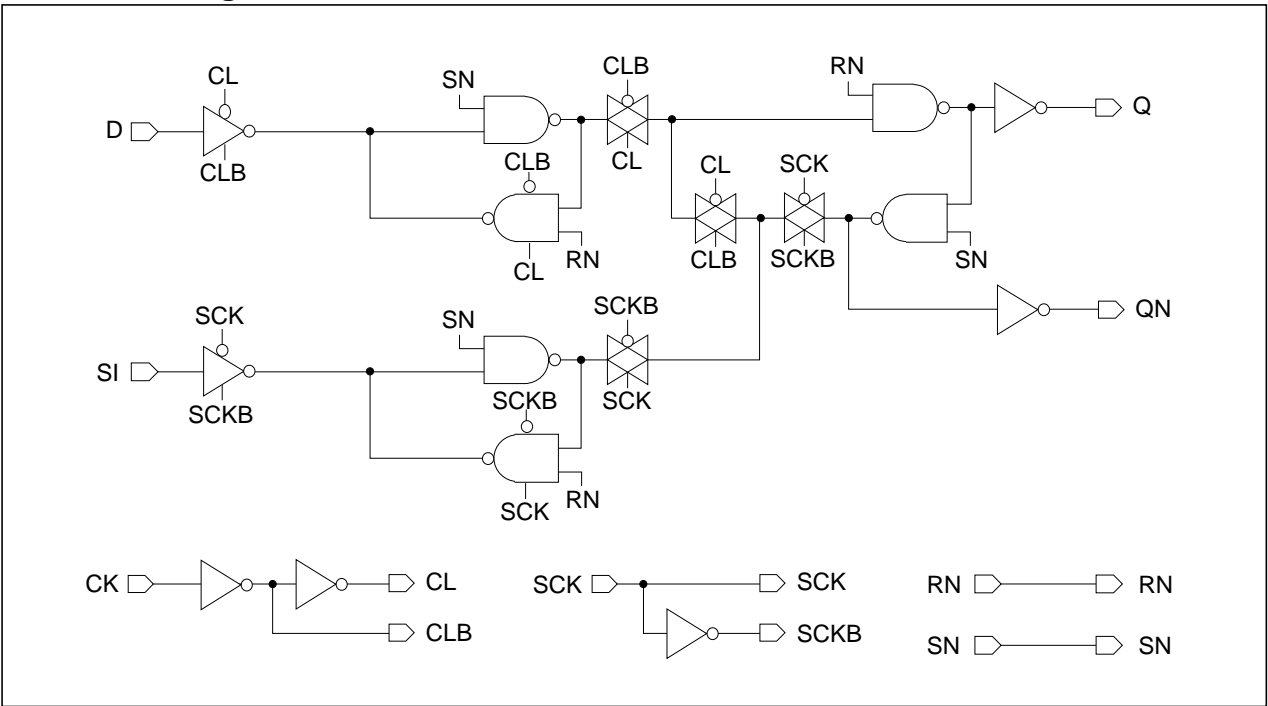
Truth Table

SI	SCK	D	CK	RN	SN	Q (n+1)	QN (n+1)
x	0	0		1	1	0	1
x	0	1		1	1	1	0
0		x	0	1	1	0	1
1		x	0	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	0	x		1	1	Q(n)	QN(n)
x		x	0	1	1	Q(n)	QN(n)

Cell Data

Input Load (SL)												Gate Count	
FD4CS						FD4CSD2						FD4CS	FD4CSD2
D	SI	CK	SCK	SN	RN	D	SI	CK	SCK	SN	RN		
0.6	0.6	0.6	1.4	2.4	2.1	0.6	0.6	0.6	1.4	2.4	2.1	10.33	11.00

Schematic Diagram





**FD4CS/FD4CSD2****D Flip-Flop with Reset, Set, Scan Clock, 1X/2X Drive****Timing Requirements**

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4CS	FD4CSD2
Input Setup Time (D to CK)	$t_{SU}$	0.268	0.268
Input Hold Time (D to CK)	$t_{HD}$	0.148	0.148
Input Setup Time (SI to SCK)	$t_{SU}$	0.778	0.779
Input Hold Time (SI to SCK)	$t_{HD}$	0.045	0.049
Pulse Width Low (CK)	$t_{PWL}$	0.401	0.401
Pulse Width High (CK)	$t_{PWH}$	0.354	0.385
Pulse Width Low (SCK)	$t_{PWL}$	0.334	0.334
Pulse Width High (SCK)	$t_{PWH}$	0.402	0.443
Pulse Width Low (SN)	$t_{PWL}$	0.379	0.422
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.313	0.314
Recovery Time (SN to SCK)	$t_{RC}$	0.177	0.174
Removal Time (SN to SCK)	$t_{RM}$	0.111	0.111
Pulse Width Low (RN)	$t_{PWL}$	0.345	0.385
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.841	0.840
Recovery Time (RN to SCK)	$t_{RC}$	0.000	0.000
Removal Time (RN to SCK)	$t_{RM}$	0.749	0.757
Removal Time (SN to RN)	$t_{RM}$	0.026	0.025
Recovery Time (SN to RN)	$t_{RC}$	0.194	0.1945



## FD4CS/FD4CSD2

### D Flip-Flop with Reset, Set, Scan Clock, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD4CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.139	$0.080 + 0.030 \cdot SL$	$0.077 + 0.030 \cdot SL$	$0.072 + 0.031 \cdot SL$
	$t_F$	0.118	$0.067 + 0.026 \cdot SL$	$0.066 + 0.026 \cdot SL$	$0.063 + 0.026 \cdot SL$
	$t_{PLH}$	0.437	$0.403 + 0.017 \cdot SL$	$0.412 + 0.015 \cdot SL$	$0.418 + 0.014 \cdot SL$
	$t_{PHL}$	0.438	$0.403 + 0.017 \cdot SL$	$0.412 + 0.015 \cdot SL$	$0.418 + 0.014 \cdot SL$
SCK to Q	$t_R$	0.154	$0.095 + 0.030 \cdot SL$	$0.095 + 0.030 \cdot SL$	$0.088 + 0.031 \cdot SL$
	$t_F$	0.124	$0.072 + 0.026 \cdot SL$	$0.074 + 0.025 \cdot SL$	$0.070 + 0.026 \cdot SL$
	$t_{PLH}$	0.506	$0.470 + 0.018 \cdot SL$	$0.480 + 0.015 \cdot SL$	$0.489 + 0.014 \cdot SL$
	$t_{PHL}$	0.444	$0.409 + 0.018 \cdot SL$	$0.418 + 0.015 \cdot SL$	$0.426 + 0.014 \cdot SL$
SN to Q	$t_R$	0.155	$0.097 + 0.029 \cdot SL$	$0.094 + 0.030 \cdot SL$	$0.086 + 0.031 \cdot SL$
	$t_{PLH}$	0.541	$0.506 + 0.018 \cdot SL$	$0.516 + 0.015 \cdot SL$	$0.525 + 0.014 \cdot SL$
RN to Q	$t_R$	0.134	$0.077 + 0.029 \cdot SL$	$0.069 + 0.030 \cdot SL$	$0.063 + 0.031 \cdot SL$
	$t_F$	0.114	$0.062 + 0.026 \cdot SL$	$0.064 + 0.026 \cdot SL$	$0.058 + 0.026 \cdot SL$
	$t_{PLH}$	0.174	$0.140 + 0.017 \cdot SL$	$0.149 + 0.015 \cdot SL$	$0.155 + 0.014 \cdot SL$
	$t_{PHL}$	0.190	$0.156 + 0.017 \cdot SL$	$0.164 + 0.015 \cdot SL$	$0.170 + 0.014 \cdot SL$
CK to QN	$t_R$	0.154	$0.093 + 0.030 \cdot SL$	$0.096 + 0.030 \cdot SL$	$0.095 + 0.030 \cdot SL$
	$t_F$	0.127	$0.075 + 0.026 \cdot SL$	$0.075 + 0.026 \cdot SL$	$0.075 + 0.026 \cdot SL$
	$t_{PLH}$	0.571	$0.534 + 0.019 \cdot SL$	$0.545 + 0.016 \cdot SL$	$0.559 + 0.014 \cdot SL$
	$t_{PHL}$	0.569	$0.533 + 0.018 \cdot SL$	$0.542 + 0.016 \cdot SL$	$0.551 + 0.015 \cdot SL$
SCK to QN	$t_R$	0.132	$0.073 + 0.029 \cdot SL$	$0.072 + 0.030 \cdot SL$	$0.066 + 0.030 \cdot SL$
	$t_F$	0.116	$0.066 + 0.025 \cdot SL$	$0.064 + 0.025 \cdot SL$	$0.058 + 0.026 \cdot SL$
	$t_{PLH}$	0.544	$0.512 + 0.016 \cdot SL$	$0.520 + 0.014 \cdot SL$	$0.525 + 0.014 \cdot SL$
	$t_{PHL}$	0.606	$0.572 + 0.017 \cdot SL$	$0.581 + 0.015 \cdot SL$	$0.586 + 0.014 \cdot SL$
SN to QN	$t_R$	0.164	$0.096 + 0.034 \cdot SL$	$0.104 + 0.032 \cdot SL$	$0.118 + 0.031 \cdot SL$
	$t_F$	0.135	$0.080 + 0.028 \cdot SL$	$0.083 + 0.027 \cdot SL$	$0.088 + 0.026 \cdot SL$
	$t_{PLH}$	0.214	$0.173 + 0.020 \cdot SL$	$0.183 + 0.018 \cdot SL$	$0.200 + 0.016 \cdot SL$
	$t_{PHL}$	0.234	$0.195 + 0.019 \cdot SL$	$0.205 + 0.017 \cdot SL$	$0.217 + 0.015 \cdot SL$
RN to QN	$t_R$	0.169	$0.101 + 0.034 \cdot SL$	$0.108 + 0.032 \cdot SL$	$0.122 + 0.030 \cdot SL$
	$t_{PLH}$	0.337	$0.296 + 0.021 \cdot SL$	$0.307 + 0.018 \cdot SL$	$0.324 + 0.016 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## D Flip-Flop with Reset, Set, Scan Clock, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FD4CSD2

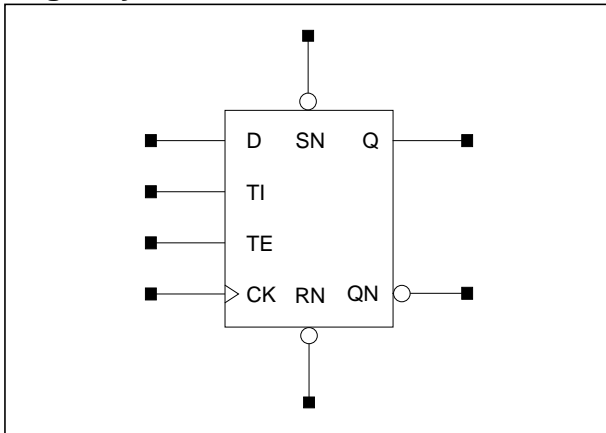
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.111	$0.083 + 0.014 \cdot SL$	$0.082 + 0.014 \cdot SL$	$0.078 + 0.015 \cdot SL$
	$t_F$	0.096	$0.068 + 0.014 \cdot SL$	$0.073 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$
	$t_{PLH}$	0.446	$0.425 + 0.010 \cdot SL$	$0.434 + 0.008 \cdot SL$	$0.448 + 0.007 \cdot SL$
	$t_{PHL}$	0.442	$0.421 + 0.011 \cdot SL$	$0.430 + 0.009 \cdot SL$	$0.443 + 0.008 \cdot SL$
SCK to Q	$t_R$	0.128	$0.100 + 0.014 \cdot SL$	$0.100 + 0.014 \cdot SL$	$0.095 + 0.014 \cdot SL$
	$t_F$	0.103	$0.076 + 0.013 \cdot SL$	$0.077 + 0.013 \cdot SL$	$0.075 + 0.013 \cdot SL$
	$t_{PLH}$	0.520	$0.499 + 0.011 \cdot SL$	$0.509 + 0.008 \cdot SL$	$0.524 + 0.007 \cdot SL$
	$t_{PHL}$	0.456	$0.434 + 0.011 \cdot SL$	$0.443 + 0.009 \cdot SL$	$0.457 + 0.008 \cdot SL$
SN to Q	$t_R$	0.131	$0.104 + 0.014 \cdot SL$	$0.104 + 0.014 \cdot SL$	$0.098 + 0.014 \cdot SL$
	$t_{PLH}$	0.582	$0.561 + 0.011 \cdot SL$	$0.571 + 0.008 \cdot SL$	$0.587 + 0.007 \cdot SL$
RN to Q	$t_R$	0.103	$0.075 + 0.014 \cdot SL$	$0.073 + 0.014 \cdot SL$	$0.070 + 0.015 \cdot SL$
	$t_F$	0.093	$0.064 + 0.015 \cdot SL$	$0.070 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	$t_{PLH}$	0.177	$0.158 + 0.010 \cdot SL$	$0.166 + 0.008 \cdot SL$	$0.179 + 0.007 \cdot SL$
	$t_{PHL}$	0.194	$0.173 + 0.011 \cdot SL$	$0.182 + 0.009 \cdot SL$	$0.195 + 0.008 \cdot SL$
CK to QN	$t_R$	0.124	$0.094 + 0.015 \cdot SL$	$0.095 + 0.015 \cdot SL$	$0.097 + 0.014 \cdot SL$
	$t_F$	0.104	$0.076 + 0.014 \cdot SL$	$0.079 + 0.013 \cdot SL$	$0.078 + 0.013 \cdot SL$
	$t_{PLH}$	0.607	$0.584 + 0.011 \cdot SL$	$0.595 + 0.009 \cdot SL$	$0.614 + 0.007 \cdot SL$
	$t_{PHL}$	0.615	$0.592 + 0.011 \cdot SL$	$0.602 + 0.009 \cdot SL$	$0.617 + 0.008 \cdot SL$
SCK to QN	$t_R$	0.105	$0.076 + 0.014 \cdot SL$	$0.077 + 0.014 \cdot SL$	$0.071 + 0.015 \cdot SL$
	$t_F$	0.095	$0.067 + 0.014 \cdot SL$	$0.071 + 0.013 \cdot SL$	$0.067 + 0.013 \cdot SL$
	$t_{PLH}$	0.593	$0.573 + 0.010 \cdot SL$	$0.581 + 0.008 \cdot SL$	$0.595 + 0.007 \cdot SL$
	$t_{PHL}$	0.664	$0.643 + 0.011 \cdot SL$	$0.651 + 0.008 \cdot SL$	$0.664 + 0.007 \cdot SL$
SN to QN	$t_R$	0.128	$0.095 + 0.017 \cdot SL$	$0.097 + 0.016 \cdot SL$	$0.111 + 0.015 \cdot SL$
	$t_F$	0.111	$0.082 + 0.015 \cdot SL$	$0.085 + 0.014 \cdot SL$	$0.089 + 0.014 \cdot SL$
	$t_{PLH}$	0.211	$0.187 + 0.012 \cdot SL$	$0.197 + 0.010 \cdot SL$	$0.217 + 0.008 \cdot SL$
	$t_{PHL}$	0.230	$0.206 + 0.012 \cdot SL$	$0.216 + 0.009 \cdot SL$	$0.234 + 0.008 \cdot SL$
RN to QN	$t_R$	0.135	$0.102 + 0.016 \cdot SL$	$0.103 + 0.016 \cdot SL$	$0.117 + 0.015 \cdot SL$
	$t_{PLH}$	0.375	$0.350 + 0.012 \cdot SL$	$0.361 + 0.010 \cdot SL$	$0.381 + 0.008 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$








### D Flip-Flop with Reset, Set, Scan, 1X/2X Drive

## Logic Symbol



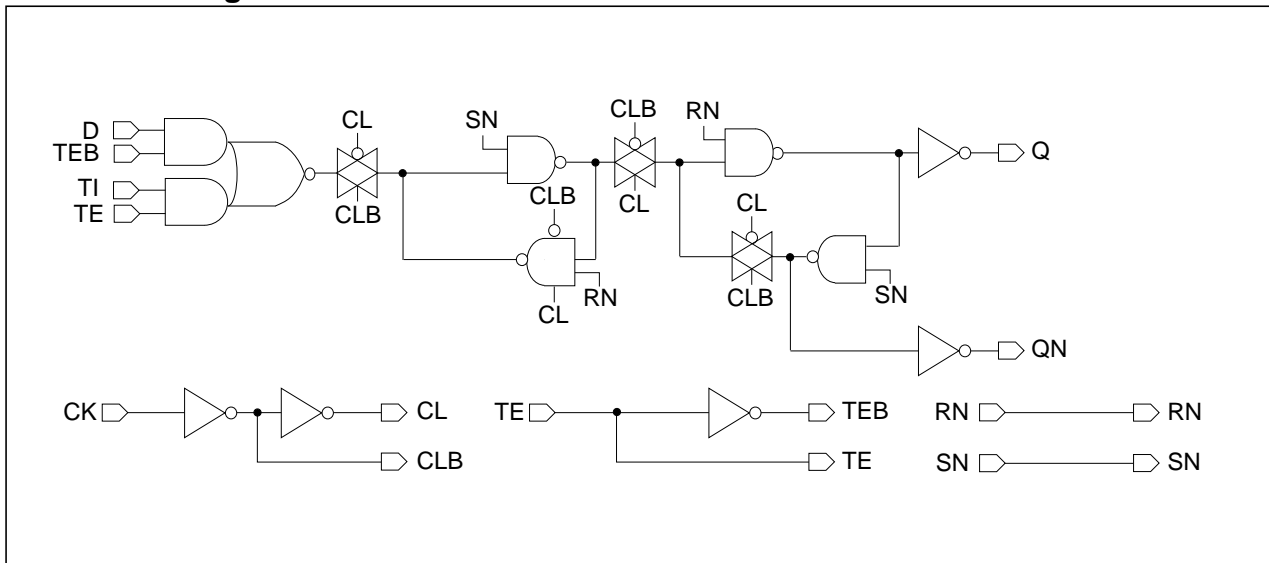
## Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)	QN (n+1)
0	x	0		1	1	0	1
1	x	0		1	1	1	0
x	0	1		1	1	0	1
x	1	1		1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x		1	1	Q (n)	QN (n)

## Cell Data

Input Load (SL)												Gate Count	
FD4S						FD4SD2						FD4S	FD4SD2
D	CK	RN	SN	TI	IE	D	CK	RN	SN	TI	IE		
0.5	0.6	1.4	1.5	0.5	1.2	0.5	0.6	1.5	1.6	0.5	1.2	8.67	9.00

### Schematic Diagram





**Timing Requirements**

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4S	FD4SD2
Input Setup Time (D to CK)	$t_{SU}$	0.456	0.446
Input Hold Time (D to CK)	$t_{HD}$	0.075	0.074
Pulse Width Low (CK)	$t_{PWL}$	0.524	0.529
Pulse Width High (CK)	$t_{PWH}$	0.357	0.380
Pulse Width Low (RN)	$t_{PWL}$	0.279	0.322
Pulse Width Low (SN)	$t_{PWL}$	0.296	0.339
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.806	0.812
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.299	0.303
Input Setup Time (TI to CK)	$t_{SU}$	0.363	0.368
Input Hold Time (TI to CK)	$t_{HD}$	0.091	0.087
Input Setup Time (TE to CK)	$t_{SU}$	0.390	0.394
Input Hold Time (TE to CK)	$t_{HD}$	0.084	0.078
Recovery Time (SN to RN)	$t_{RC}$	0.236	0.232
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000



## FD4S/FD4SD2

### D Flip-Flop with Reset, Set, Scan, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.136	$0.078 + 0.029 \cdot SL$	$0.078 + 0.029 \cdot SL$	$0.071 + 0.030 \cdot SL$
	$t_F$	0.120	$0.066 + 0.027 \cdot SL$	$0.066 + 0.027 \cdot SL$	$0.063 + 0.027 \cdot SL$
	$t_{PLH}$	0.458	$0.424 + 0.017 \cdot SL$	$0.433 + 0.015 \cdot SL$	$0.440 + 0.014 \cdot SL$
	$t_{PHL}$	0.461	$0.425 + 0.018 \cdot SL$	$0.434 + 0.016 \cdot SL$	$0.441 + 0.015 \cdot SL$
RN to Q	$t_R$	0.128	$0.070 + 0.029 \cdot SL$	$0.068 + 0.030 \cdot SL$	$0.064 + 0.030 \cdot SL$
	$t_F$	0.116	$0.062 + 0.027 \cdot SL$	$0.063 + 0.027 \cdot SL$	$0.059 + 0.027 \cdot SL$
	$t_{PLH}$	0.172	$0.139 + 0.016 \cdot SL$	$0.147 + 0.014 \cdot SL$	$0.153 + 0.014 \cdot SL$
	$t_{PHL}$	0.193	$0.158 + 0.018 \cdot SL$	$0.166 + 0.016 \cdot SL$	$0.171 + 0.015 \cdot SL$
SN to Q	$t_R$	0.138	$0.081 + 0.028 \cdot SL$	$0.077 + 0.029 \cdot SL$	$0.071 + 0.030 \cdot SL$
	$t_{PLH}$	0.401	$0.368 + 0.017 \cdot SL$	$0.377 + 0.014 \cdot SL$	$0.383 + 0.014 \cdot SL$
CK to QN	$t_R$	0.127	$0.069 + 0.029 \cdot SL$	$0.066 + 0.030 \cdot SL$	$0.060 + 0.031 \cdot SL$
	$t_F$	0.113	$0.061 + 0.026 \cdot SL$	$0.058 + 0.027 \cdot SL$	$0.053 + 0.027 \cdot SL$
	$t_{PLH}$	0.552	$0.519 + 0.016 \cdot SL$	$0.527 + 0.014 \cdot SL$	$0.532 + 0.014 \cdot SL$
	$t_{PHL}$	0.550	$0.516 + 0.017 \cdot SL$	$0.524 + 0.015 \cdot SL$	$0.529 + 0.015 \cdot SL$
RN to QN	$t_R$	0.153	$0.090 + 0.031 \cdot SL$	$0.095 + 0.030 \cdot SL$	$0.096 + 0.030 \cdot SL$
	$t_{PLH}$	0.328	$0.289 + 0.019 \cdot SL$	$0.302 + 0.016 \cdot SL$	$0.318 + 0.014 \cdot SL$
SN to QN	$t_R$	0.150	$0.087 + 0.031 \cdot SL$	$0.093 + 0.030 \cdot SL$	$0.093 + 0.030 \cdot SL$
	$t_F$	0.130	$0.074 + 0.028 \cdot SL$	$0.078 + 0.027 \cdot SL$	$0.074 + 0.027 \cdot SL$
	$t_{PLH}$	0.200	$0.161 + 0.019 \cdot SL$	$0.174 + 0.016 \cdot SL$	$0.189 + 0.014 \cdot SL$
	$t_{PHL}$	0.221	$0.183 + 0.019 \cdot SL$	$0.193 + 0.017 \cdot SL$	$0.204 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## D Flip-Flop with Reset, Set, Scan, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FD4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.110	$0.080 + 0.015*SL$	$0.081 + 0.015*SL$	$0.078 + 0.015*SL$
	$t_F$	0.094	$0.066 + 0.014*SL$	$0.070 + 0.013*SL$	$0.067 + 0.013*SL$
	$t_{PLH}$	0.457	$0.436 + 0.010*SL$	$0.445 + 0.008*SL$	$0.459 + 0.007*SL$
	$t_{PHL}$	0.459	$0.437 + 0.011*SL$	$0.446 + 0.009*SL$	$0.460 + 0.008*SL$
RN to Q	$t_R$	0.101	$0.072 + 0.014*SL$	$0.071 + 0.015*SL$	$0.067 + 0.015*SL$
	$t_F$	0.090	$0.061 + 0.015*SL$	$0.067 + 0.013*SL$	$0.064 + 0.013*SL$
	$t_{PLH}$	0.177	$0.157 + 0.010*SL$	$0.165 + 0.008*SL$	$0.178 + 0.007*SL$
	$t_{PHL}$	0.191	$0.169 + 0.011*SL$	$0.178 + 0.009*SL$	$0.191 + 0.008*SL$
SN to Q	$t_R$	0.112	$0.083 + 0.014*SL$	$0.083 + 0.014*SL$	$0.077 + 0.015*SL$
	$t_{PLH}$	0.445	$0.424 + 0.010*SL$	$0.433 + 0.008*SL$	$0.447 + 0.007*SL$
CK to QN	$t_R$	0.103	$0.073 + 0.015*SL$	$0.074 + 0.015*SL$	$0.069 + 0.015*SL$
	$t_F$	0.091	$0.064 + 0.014*SL$	$0.066 + 0.013*SL$	$0.063 + 0.013*SL$
	$t_{PLH}$	0.599	$0.578 + 0.010*SL$	$0.587 + 0.008*SL$	$0.601 + 0.007*SL$
	$t_{PHL}$	0.593	$0.572 + 0.011*SL$	$0.581 + 0.008*SL$	$0.594 + 0.007*SL$
RN to QN	$t_R$	0.125	$0.095 + 0.015*SL$	$0.095 + 0.015*SL$	$0.100 + 0.015*SL$
	$t_{PLH}$	0.372	$0.348 + 0.012*SL$	$0.360 + 0.009*SL$	$0.381 + 0.007*SL$
SN to QN	$t_R$	0.120	$0.088 + 0.016*SL$	$0.091 + 0.015*SL$	$0.097 + 0.015*SL$
	$t_F$	0.105	$0.076 + 0.014*SL$	$0.079 + 0.014*SL$	$0.083 + 0.013*SL$
	$t_{PLH}$	0.207	$0.183 + 0.012*SL$	$0.195 + 0.009*SL$	$0.216 + 0.007*SL$
	$t_{PHL}$	0.221	$0.198 + 0.012*SL$	$0.208 + 0.009*SL$	$0.227 + 0.008*SL$

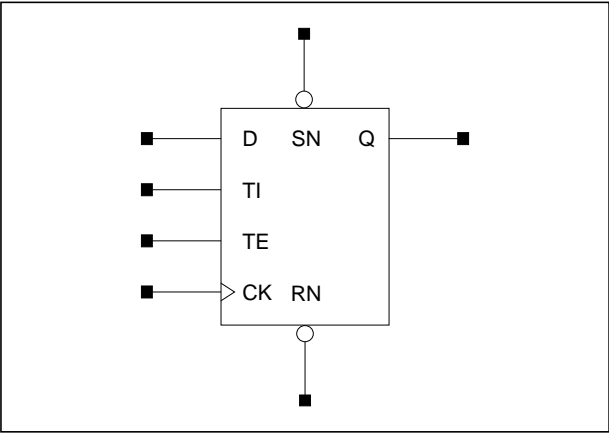
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



FD4SQ/FD4SQD2

D Flip-Flop with Reset, Set, Scan, Q Output Only, 1X/2X Drive

Logic Symbol



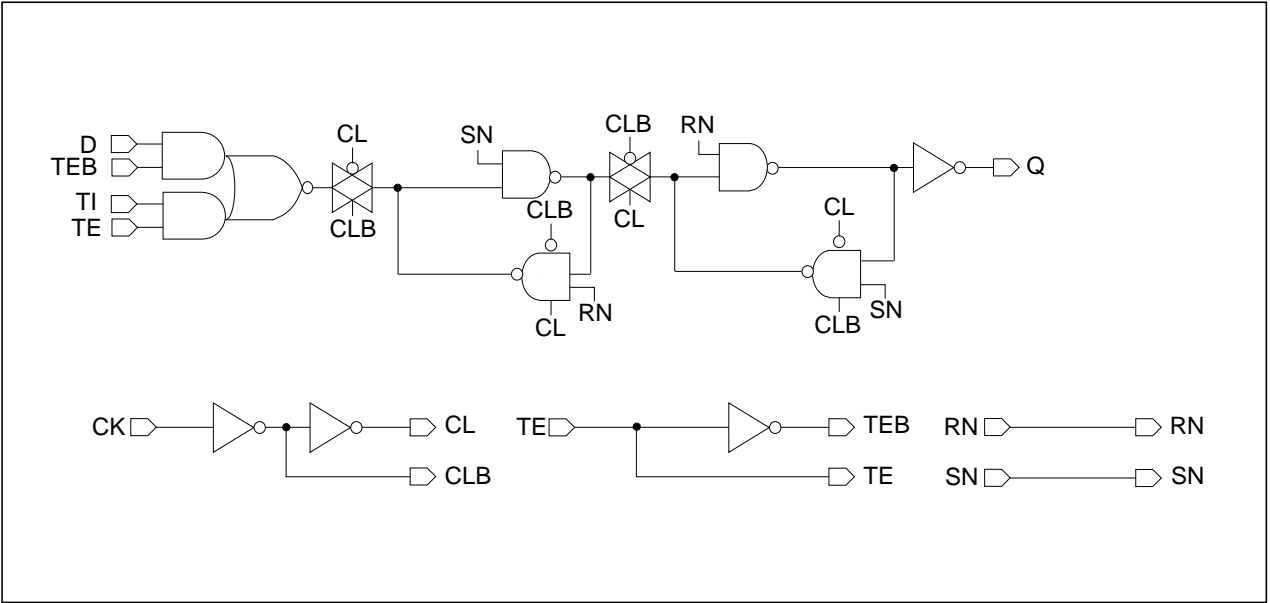
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)
0	x	0		1	1	0
1	x	0		1	1	1
x	0	1		1	1	0
x	1	1		1	1	1
x	x	x	x	1	0	1
x	x	x	x	0	1	0
x	x	x	x	0	0	0
x	x	x		1	1	Q (n)

Cell Data

Input Load (SL)												Gate Count	
FD4SQ						FD4SQD2						FD4SQ	FD4SQD2
D	CK	RN	SN	TI	TE	D	CK	RN	SN	TI	TE		
0.5	0.6	1.5	1.1	0.5	1.2	0.5	0.6	1.5	1.1	0.5	1.2	8.00	8.33

Schematic Diagram





**FD4SQ/FD4SQD2****D Flip-Flop with Reset, Set, Scan, Q Output Only, 1X/2X Drive****Timing Requirements**

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4SQ	FD4SQD2
Input Setup Time (D to CK)	$t_{SU}$	0.478	0.462
Input Hold Time (D to CK)	$t_{HD}$	0.075	0.075
Pulse Width Low (CK)	$t_{PWL}$	0.546	0.545
Pulse Width High (CK)	$t_{PWH}$	0.321	0.338
Pulse Width Low (RN)	$t_{PWL}$	0.251	0.270
Pulse Width Low (SN)	$t_{PWL}$	0.560	0.584
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.801	0.801
Recovery Time (SN to CK)	$t_{RC}$	0.004	0.004
Removal Time (SN to CK)	$t_{RM}$	0.303	0.304
Input Setup Time (TI to CK)	$t_{SU}$	0.473	0.472
Input Hold Time (TI to CK)	$t_{HD}$	0.088	0.088
Input Setup Time (TE to CK)	$t_{SU}$	0.400	0.400
Input Hold Time (TE to CK)	$t_{HD}$	0.082	0.081
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000
Recovery Time (SN to RN)	$t_{RC}$	0.004	0.228



## FD4SQ/FD4SQD2

### D Flip-Flop with Reset, Set, Scan, Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD4SQ

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.132	$0.073 + 0.029 \cdot SL$	$0.072 + 0.030 \cdot SL$	$0.066 + 0.030 \cdot SL$
	$t_F$	0.113	$0.063 + 0.025 \cdot SL$	$0.062 + 0.025 \cdot SL$	$0.057 + 0.026 \cdot SL$
	$t_{PLH}$	0.413	$0.381 + 0.016 \cdot SL$	$0.389 + 0.014 \cdot SL$	$0.394 + 0.014 \cdot SL$
	$t_{PHL}$	0.437	$0.404 + 0.017 \cdot SL$	$0.413 + 0.014 \cdot SL$	$0.418 + 0.014 \cdot SL$
RN to Q	$t_R$	0.128	$0.069 + 0.029 \cdot SL$	$0.066 + 0.030 \cdot SL$	$0.061 + 0.030 \cdot SL$
	$t_F$	0.110	$0.061 + 0.025 \cdot SL$	$0.060 + 0.025 \cdot SL$	$0.053 + 0.026 \cdot SL$
	$t_{PLH}$	0.167	$0.135 + 0.016 \cdot SL$	$0.142 + 0.014 \cdot SL$	$0.147 + 0.014 \cdot SL$
	$t_{PHL}$	0.182	$0.149 + 0.016 \cdot SL$	$0.157 + 0.014 \cdot SL$	$0.161 + 0.014 \cdot SL$
SN to Q	$t_R$	0.142	$0.085 + 0.028 \cdot SL$	$0.082 + 0.029 \cdot SL$	$0.074 + 0.030 \cdot SL$
	$t_{PLH}$	0.620	$0.587 + 0.016 \cdot SL$	$0.595 + 0.014 \cdot SL$	$0.602 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD4SQD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.104	$0.074 + 0.015 \cdot SL$	$0.077 + 0.014 \cdot SL$	$0.070 + 0.015 \cdot SL$
	$t_F$	0.089	$0.063 + 0.013 \cdot SL$	$0.066 + 0.012 \cdot SL$	$0.063 + 0.013 \cdot SL$
	$t_{PLH}$	0.421	$0.401 + 0.010 \cdot SL$	$0.409 + 0.008 \cdot SL$	$0.422 + 0.007 \cdot SL$
	$t_{PHL}$	0.439	$0.419 + 0.010 \cdot SL$	$0.428 + 0.008 \cdot SL$	$0.441 + 0.007 \cdot SL$
RN to Q	$t_R$	0.098	$0.069 + 0.015 \cdot SL$	$0.068 + 0.015 \cdot SL$	$0.064 + 0.015 \cdot SL$
	$t_F$	0.085	$0.058 + 0.013 \cdot SL$	$0.063 + 0.012 \cdot SL$	$0.058 + 0.013 \cdot SL$
	$t_{PLH}$	0.172	$0.153 + 0.010 \cdot SL$	$0.160 + 0.008 \cdot SL$	$0.172 + 0.007 \cdot SL$
	$t_{PHL}$	0.180	$0.160 + 0.010 \cdot SL$	$0.169 + 0.008 \cdot SL$	$0.181 + 0.007 \cdot SL$
SN to Q	$t_R$	0.114	$0.086 + 0.014 \cdot SL$	$0.086 + 0.014 \cdot SL$	$0.079 + 0.015 \cdot SL$
	$t_{PLH}$	0.631	$0.610 + 0.010 \cdot SL$	$0.619 + 0.008 \cdot SL$	$0.632 + 0.007 \cdot SL$

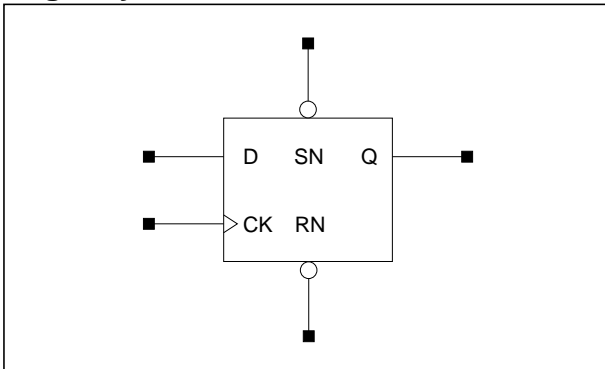
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FD4Q/FD4QD2

### D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

#### Logic Symbol



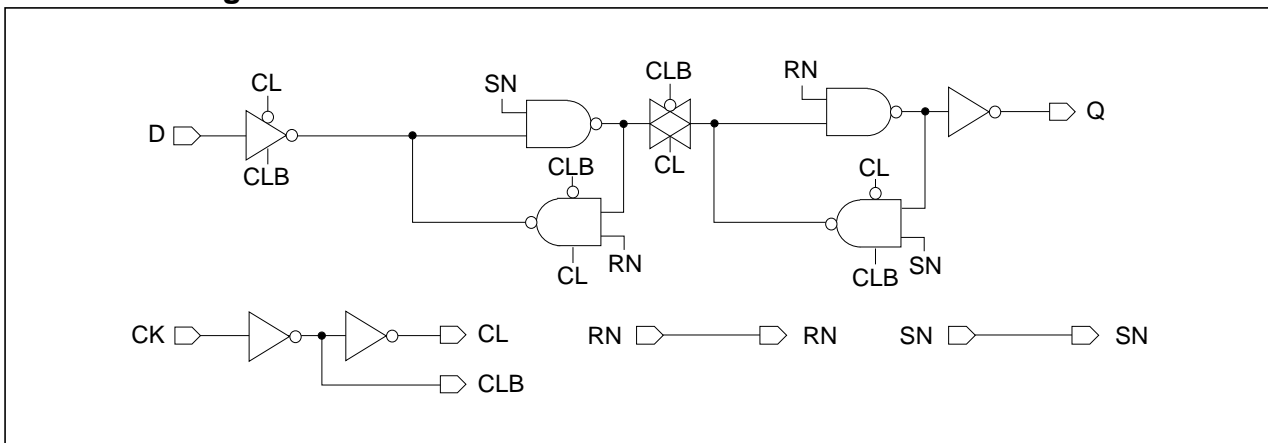
#### Truth Table

D	CK	RN	SN	Q (n+1)
0		1	1	0
1		1	1	1
x	x	1	0	1
x	x	0	1	0
x	x	0	0	0
x		1	1	Q (n)

#### Cell Data

Input Load (SL)								Gate Count	
FD4Q				FD4QD2				FD4Q	FD4QD2
D	CK	RN	SN	D	CK	RN	SN		
0.5	0.5	1.4	1.2	0.5	0.5	1.4	1.2	6.00	6.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4Q	FD4QD2
Input Setup Time (D to CK)	$t_{SU}$	0.259	0.259
Input Hold Time (D to CK)	$t_{HD}$	0.168	0.168
Pulse Width Low (CK)	$t_{PWL}$	0.379	0.378
Pulse Width High (CK)	$t_{PWH}$	0.319	0.337
Pulse Width Low (RN)	$t_{PWL}$	0.250	0.272
Pulse Width Low (SN)	$t_{PWL}$	0.551	0.578
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.822	0.822
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.275	0.276
Recovery Time (SN to RN)	$t_{RC}$	0.240	0.240
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000



## FD4Q/FD4QD2

### D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### FD4Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.131	$0.073 + 0.029 \cdot SL$	$0.070 + 0.030 \cdot SL$	$0.065 + 0.030 \cdot SL$
	$t_F$	0.111	$0.061 + 0.025 \cdot SL$	$0.063 + 0.025 \cdot SL$	$0.055 + 0.026 \cdot SL$
	$t_{PLH}$	0.414	$0.381 + 0.016 \cdot SL$	$0.390 + 0.014 \cdot SL$	$0.396 + 0.014 \cdot SL$
	$t_{PHL}$	0.429	$0.396 + 0.017 \cdot SL$	$0.404 + 0.015 \cdot SL$	$0.410 + 0.014 \cdot SL$
RN to Q	$t_R$	0.126	$0.068 + 0.029 \cdot SL$	$0.065 + 0.030 \cdot SL$	$0.061 + 0.030 \cdot SL$
	$t_F$	0.110	$0.060 + 0.025 \cdot SL$	$0.060 + 0.025 \cdot SL$	$0.053 + 0.026 \cdot SL$
	$t_{PLH}$	0.167	$0.135 + 0.016 \cdot SL$	$0.143 + 0.014 \cdot SL$	$0.147 + 0.014 \cdot SL$
	$t_{PHL}$	0.184	$0.151 + 0.017 \cdot SL$	$0.159 + 0.014 \cdot SL$	$0.164 + 0.014 \cdot SL$
SN to Q	$t_R$	0.141	$0.085 + 0.028 \cdot SL$	$0.082 + 0.029 \cdot SL$	$0.072 + 0.030 \cdot SL$
	$t_{PLH}$	0.599	$0.564 + 0.017 \cdot SL$	$0.575 + 0.014 \cdot SL$	$0.582 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### FD4QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.105	$0.076 + 0.014 \cdot SL$	$0.076 + 0.015 \cdot SL$	$0.071 + 0.015 \cdot SL$
	$t_F$	0.089	$0.063 + 0.013 \cdot SL$	$0.066 + 0.012 \cdot SL$	$0.063 + 0.013 \cdot SL$
	$t_{PLH}$	0.425	$0.405 + 0.010 \cdot SL$	$0.413 + 0.008 \cdot SL$	$0.426 + 0.007 \cdot SL$
	$t_{PHL}$	0.434	$0.414 + 0.010 \cdot SL$	$0.422 + 0.008 \cdot SL$	$0.435 + 0.007 \cdot SL$
RN to Q	$t_R$	0.099	$0.071 + 0.014 \cdot SL$	$0.069 + 0.015 \cdot SL$	$0.065 + 0.015 \cdot SL$
	$t_F$	0.087	$0.059 + 0.014 \cdot SL$	$0.066 + 0.012 \cdot SL$	$0.059 + 0.013 \cdot SL$
	$t_{PLH}$	0.175	$0.155 + 0.010 \cdot SL$	$0.162 + 0.008 \cdot SL$	$0.175 + 0.007 \cdot SL$
	$t_{PHL}$	0.185	$0.165 + 0.010 \cdot SL$	$0.173 + 0.008 \cdot SL$	$0.186 + 0.007 \cdot SL$
SN to Q	$t_R$	0.116	$0.089 + 0.014 \cdot SL$	$0.086 + 0.014 \cdot SL$	$0.080 + 0.015 \cdot SL$
	$t_{PLH}$	0.614	$0.592 + 0.011 \cdot SL$	$0.603 + 0.008 \cdot SL$	$0.617 + 0.007 \cdot SL$

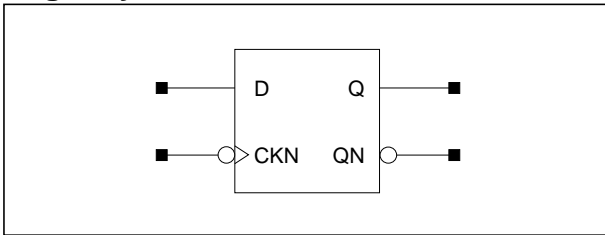
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$






## FD5/FD5D2

### D Flip-Flop with Negative Edge Trigger, 1X/2X Drive

## Logic Symbol



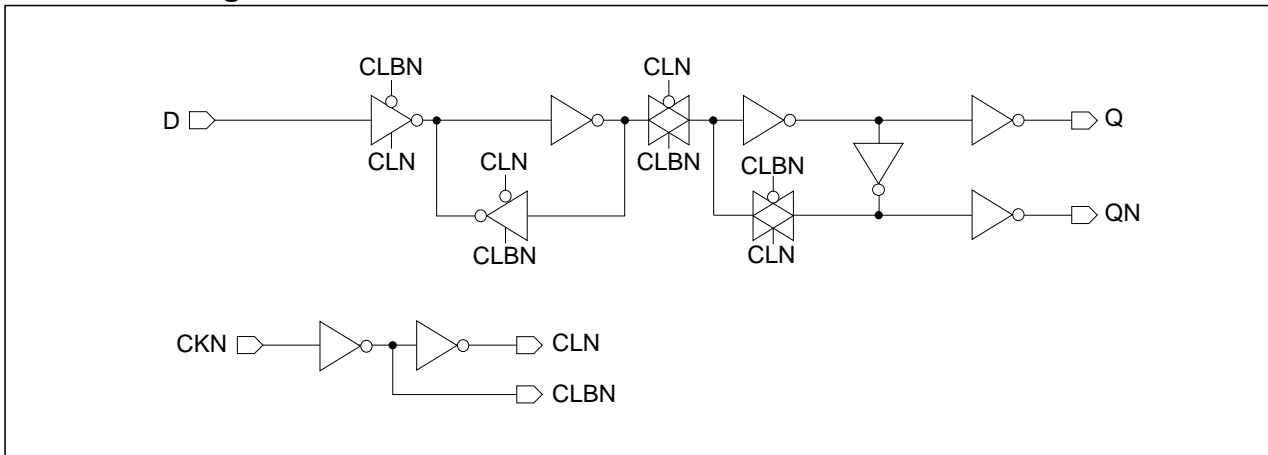
## Truth Table

D	CKN	Q (n+1)	QN (n+1)
0		0	1
1		1	0
x		Q (n)	QN (n)

## Cell Data

Input Load (SL)				Gate Count	
FD5		FD5D2		FD5	FD5D2
D	CKN	D	CKN		
0.6	0.5	0.6	0.5	5.00	5.33

### Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD5	FD5D2
Input Setup Time (D to CKN)	t <sub>SU</sub>	0.278	0.287
Input Hold Time (D to CKN)	t <sub>HD</sub>	0.376	0.376
Pulse Width Low (CKN)	t <sub>PWL</sub>	0.314	0.322
Pulse Width High (CKN)	t <sub>PWH</sub>	0.314	0.322



## FD5/FD5D2

### D Flip-Flop with Negative Edge Trigger, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.123	$0.066 + 0.029 \cdot SL$	$0.061 + 0.030 \cdot SL$	$0.054 + 0.031 \cdot SL$
	$t_F$	0.111	$0.059 + 0.026 \cdot SL$	$0.062 + 0.025 \cdot SL$	$0.057 + 0.026 \cdot SL$
	$t_{PLH}$	0.445	$0.414 + 0.015 \cdot SL$	$0.420 + 0.014 \cdot SL$	$0.423 + 0.013 \cdot SL$
	$t_{PHL}$	0.392	$0.359 + 0.017 \cdot SL$	$0.367 + 0.015 \cdot SL$	$0.374 + 0.014 \cdot SL$
CKN to QN	$t_R$	0.113	$0.055 + 0.029 \cdot SL$	$0.050 + 0.030 \cdot SL$	$0.045 + 0.031 \cdot SL$
	$t_F$	0.099	$0.048 + 0.026 \cdot SL$	$0.049 + 0.025 \cdot SL$	$0.044 + 0.026 \cdot SL$
	$t_{PLH}$	0.452	$0.423 + 0.015 \cdot SL$	$0.427 + 0.014 \cdot SL$	$0.428 + 0.014 \cdot SL$
	$t_{PHL}$	0.516	$0.484 + 0.016 \cdot SL$	$0.491 + 0.014 \cdot SL$	$0.494 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD5D2

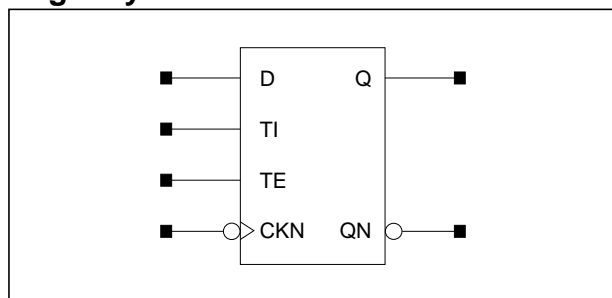
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.093	$0.064 + 0.015 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.088	$0.059 + 0.014 \cdot SL$	$0.063 + 0.013 \cdot SL$	$0.061 + 0.013 \cdot SL$
	$t_{PLH}$	0.438	$0.419 + 0.009 \cdot SL$	$0.426 + 0.007 \cdot SL$	$0.434 + 0.007 \cdot SL$
	$t_{PHL}$	0.379	$0.358 + 0.011 \cdot SL$	$0.366 + 0.008 \cdot SL$	$0.379 + 0.007 \cdot SL$
CKN to QN	$t_R$	0.086	$0.057 + 0.014 \cdot SL$	$0.058 + 0.014 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.082	$0.055 + 0.014 \cdot SL$	$0.057 + 0.013 \cdot SL$	$0.052 + 0.014 \cdot SL$
	$t_{PLH}$	0.472	$0.455 + 0.009 \cdot SL$	$0.461 + 0.007 \cdot SL$	$0.467 + 0.007 \cdot SL$
	$t_{PHL}$	0.545	$0.525 + 0.010 \cdot SL$	$0.533 + 0.008 \cdot SL$	$0.543 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## D Flip-Flop with Negative Edge Trigger, Scan, 1X/2X Drive

## Logic Symbol



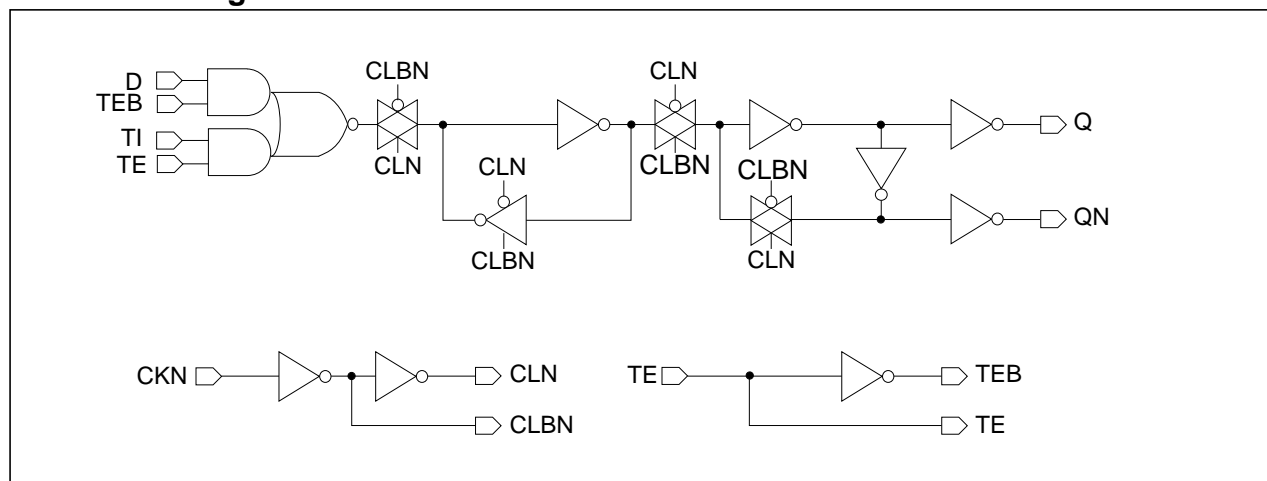
## Truth Table

D	TI	TE	CKN	Q (n+1)	QN (n+1)
0	x	0		0	1
1	x	0		1	0
x	0	1		0	1
x	1	1		1	0
x	x	x		Q (n)	QN (n)

## Cell Data

Input Load (SL)								Gate Count	
FD5S				FD5SD2				FD5S	FD5SD2
D	CKN	TI	TE	D	CKN	TI	TE		
0.4	0.6	0.5	1.2	0.4	0.5	0.5	1.1	6.67	7.00

## Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD5S	FD5SD2
Input Setup Time (D to CKN)	$t_{SU}$	0.511	0.492
Input Hold Time (D to CKN)	$t_{HD}$	0.323	0.320
Pulse Width Low (CKN)	$t_{PWL}$	0.316	0.326
Pulse Width High (CKN)	$t_{PWH}$	0.316	0.326
Input Setup Time (TI to CKN)	$t_{SU}$	0.423	0.413
Input Hold Time (TI to CKN)	$t_{HD}$	0.253	0.249
Input Setup Time (TE to CKN)	$t_{SU}$	0.377	0.359
Input Hold Time (TE to CKN)	$t_{HD}$	0.338	0.343



## FD5S/FD5SD2

### D Flip-Flop with Negative Edge Trigger, Scan, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.123	$0.066 + 0.029 \cdot SL$	$0.062 + 0.030 \cdot SL$	$0.055 + 0.031 \cdot SL$
	$t_F$	0.110	$0.058 + 0.026 \cdot SL$	$0.060 + 0.025 \cdot SL$	$0.056 + 0.026 \cdot SL$
	$t_{PLH}$	0.453	$0.423 + 0.015 \cdot SL$	$0.428 + 0.014 \cdot SL$	$0.431 + 0.014 \cdot SL$
	$t_{PHL}$	0.391	$0.358 + 0.017 \cdot SL$	$0.366 + 0.015 \cdot SL$	$0.373 + 0.014 \cdot SL$
CKN to QN	$t_R$	0.113	$0.055 + 0.029 \cdot SL$	$0.050 + 0.030 \cdot SL$	$0.045 + 0.031 \cdot SL$
	$t_F$	0.100	$0.048 + 0.026 \cdot SL$	$0.049 + 0.025 \cdot SL$	$0.044 + 0.026 \cdot SL$
	$t_{PLH}$	0.452	$0.423 + 0.015 \cdot SL$	$0.427 + 0.014 \cdot SL$	$0.428 + 0.014 \cdot SL$
	$t_{PHL}$	0.525	$0.494 + 0.016 \cdot SL$	$0.501 + 0.014 \cdot SL$	$0.504 + 0.014 \cdot SL$

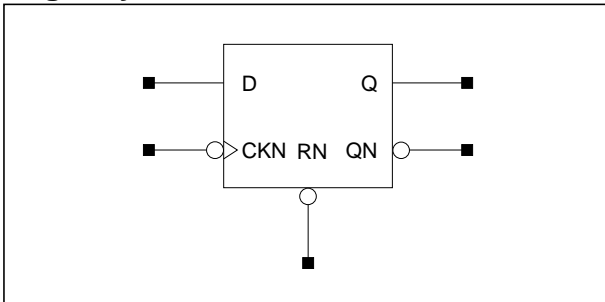
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.093	$0.065 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.089	$0.060 + 0.014 \cdot SL$	$0.064 + 0.013 \cdot SL$	$0.060 + 0.014 \cdot SL$
	$t_{PLH}$	0.446	$0.427 + 0.009 \cdot SL$	$0.435 + 0.007 \cdot SL$	$0.443 + 0.007 \cdot SL$
	$t_{PHL}$	0.391	$0.370 + 0.011 \cdot SL$	$0.378 + 0.009 \cdot SL$	$0.391 + 0.008 \cdot SL$
CKN to QN	$t_R$	0.086	$0.057 + 0.014 \cdot SL$	$0.056 + 0.014 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.081	$0.053 + 0.014 \cdot SL$	$0.056 + 0.013 \cdot SL$	$0.050 + 0.014 \cdot SL$
	$t_{PLH}$	0.482	$0.465 + 0.009 \cdot SL$	$0.471 + 0.007 \cdot SL$	$0.477 + 0.007 \cdot SL$
	$t_{PHL}$	0.550	$0.530 + 0.010 \cdot SL$	$0.538 + 0.008 \cdot SL$	$0.548 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$

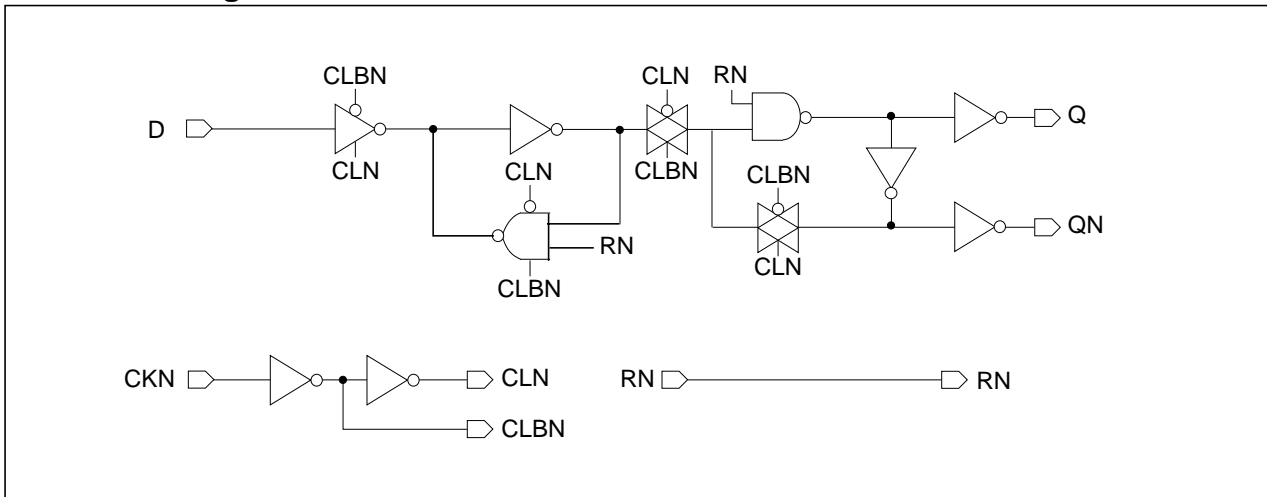


**D Flip-Flop with Negative Edge Trigger, Reset, 1X/2X Drive****Logic Symbol****Truth Table**

D	CKN	RN	Q (n+1)	QN (n+1)
0		1	0	1
1		1	1	0
x	x	0	0	1
x		1	Q (n)	QN (n)

**Cell Data**

Input Load (SL)						Gate Count	
FD6			FD6D2			FD6	FD6D2
D	CKN	RN	D	CKN	RN		
0.6	0.6	1.4	0.6	0.5	1.4	5.67	6.33

**Schematic Diagram****Timing Requirements**

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD6	FD6D2
Input Setup Time (D to CKN)	$t_{SU}$	0.312	0.308
Input Hold Time (D to CKN)	$t_{HD}$	0.309	0.378
Pulse Width Low (CKN)	$t_{PWL}$	0.328	0.349
Pulse Width High (CKN)	$t_{PWH}$	0.328	0.349
Pulse Width Low (RN)	$t_{PWL}$	0.436	0.401
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.962	0.960



## FD6/FD6D2

### D Flip-Flop with Negative Edge Trigger, Reset, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t <sub>R</sub>	0.138	$0.079 + 0.029 \cdot SL$	$0.080 + 0.029 \cdot SL$	$0.075 + 0.030 \cdot SL$
	t <sub>F</sub>	0.119	$0.064 + 0.027 \cdot SL$	$0.066 + 0.027 \cdot SL$	$0.062 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.477	$0.443 + 0.017 \cdot SL$	$0.452 + 0.015 \cdot SL$	$0.460 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.393	$0.357 + 0.018 \cdot SL$	$0.366 + 0.016 \cdot SL$	$0.374 + 0.015 \cdot SL$
RN to Q	t <sub>F</sub>	0.119	$0.064 + 0.028 \cdot SL$	$0.068 + 0.027 \cdot SL$	$0.062 + 0.027 \cdot SL$
	t <sub>PHL</sub>	0.198	$0.162 + 0.018 \cdot SL$	$0.171 + 0.016 \cdot SL$	$0.178 + 0.015 \cdot SL$
CKN to QN	t <sub>R</sub>	0.113	$0.057 + 0.028 \cdot SL$	$0.051 + 0.029 \cdot SL$	$0.046 + 0.030 \cdot SL$
	t <sub>F</sub>	0.109	$0.055 + 0.027 \cdot SL$	$0.055 + 0.027 \cdot SL$	$0.049 + 0.028 \cdot SL$
	t <sub>PLH</sub>	0.450	$0.421 + 0.014 \cdot SL$	$0.425 + 0.013 \cdot SL$	$0.427 + 0.013 \cdot SL$
	t <sub>PHL</sub>	0.558	$0.524 + 0.017 \cdot SL$	$0.531 + 0.015 \cdot SL$	$0.535 + 0.015 \cdot SL$
RN to QN	t <sub>R</sub>	0.130	$0.071 + 0.029 \cdot SL$	$0.072 + 0.029 \cdot SL$	$0.069 + 0.030 \cdot SL$
	t <sub>PLH</sub>	0.289	$0.255 + 0.017 \cdot SL$	$0.264 + 0.015 \cdot SL$	$0.273 + 0.013 \cdot SL$

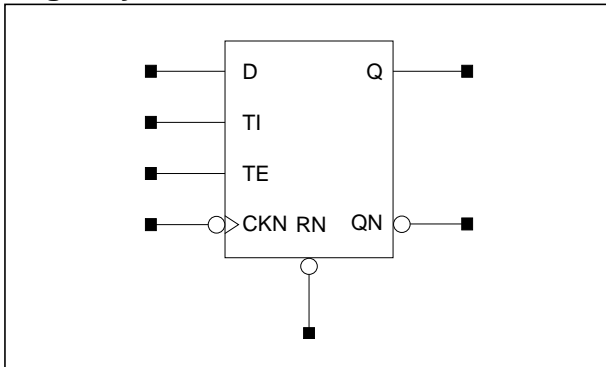
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t <sub>R</sub>	0.107	$0.078 + 0.015 \cdot SL$	$0.077 + 0.015 \cdot SL$	$0.076 + 0.015 \cdot SL$
	t <sub>F</sub>	0.091	$0.064 + 0.013 \cdot SL$	$0.064 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	t <sub>PLH</sub>	0.477	$0.456 + 0.010 \cdot SL$	$0.465 + 0.008 \cdot SL$	$0.479 + 0.007 \cdot SL$
	t <sub>PHL</sub>	0.400	$0.378 + 0.011 \cdot SL$	$0.387 + 0.009 \cdot SL$	$0.401 + 0.008 \cdot SL$
RN to Q	t <sub>F</sub>	0.089	$0.060 + 0.014 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	t <sub>PHL</sub>	0.188	$0.166 + 0.011 \cdot SL$	$0.175 + 0.009 \cdot SL$	$0.189 + 0.008 \cdot SL$
CKN to QN	t <sub>R</sub>	0.087	$0.058 + 0.015 \cdot SL$	$0.059 + 0.014 \cdot SL$	$0.047 + 0.015 \cdot SL$
	t <sub>F</sub>	0.085	$0.057 + 0.014 \cdot SL$	$0.063 + 0.013 \cdot SL$	$0.056 + 0.013 \cdot SL$
	t <sub>PLH</sub>	0.501	$0.483 + 0.009 \cdot SL$	$0.489 + 0.007 \cdot SL$	$0.496 + 0.007 \cdot SL$
	t <sub>PHL</sub>	0.596	$0.576 + 0.010 \cdot SL$	$0.585 + 0.008 \cdot SL$	$0.596 + 0.007 \cdot SL$
RN to QN	t <sub>R</sub>	0.101	$0.071 + 0.015 \cdot SL$	$0.072 + 0.015 \cdot SL$	$0.068 + 0.015 \cdot SL$
	t <sub>PLH</sub>	0.318	$0.298 + 0.010 \cdot SL$	$0.306 + 0.008 \cdot SL$	$0.320 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$

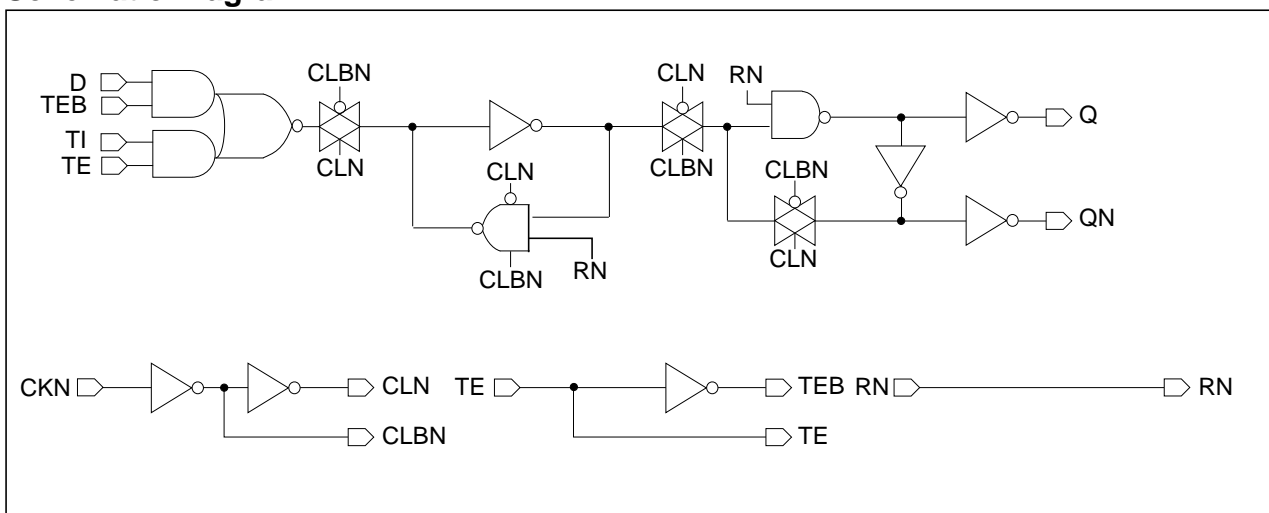


**D Flip-Flop with Negative Edge Trigger, Reset, Scan, 1X/2X Drive****Logic Symbol****Truth Table**

D	TI	TE	CKN	RN	Q (n+1)	QN (n+1)
0	x	0		1	0	1
1	x	0		1	1	0
x	0	1		1	0	1
x	1	1		1	1	0
x	x	x	x	0	0	1
x	x	x		1	Q (n)	QN (n)

**Cell Data**

Input Load (SL)										Gate Count	
FD6S					FD6SD2					FD6S	FD6SD2
D	CKN	RN	TI	TE	D	CKN	RN	TI	TE		
0.4	0.5	1.4	0.5	1.2	0.4	0.6	1.4	0.5	1.2	7.67	8.00

**Schematic Diagram****Timing Requirements**

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD6S	FD6SD2
Input Setup Time (D to CKN)	$t_{SU}$	0.536	0.538
Input Hold Time (D to CKN)	$t_{HD}$	0.310	0.308
Pulse Width Low (CKN)	$t_{PWL}$	0.338	0.362
Pulse Width High (CKN)	$t_{PWH}$	0.338	0.362
Pulse Width Low (RN)	$t_{PWL}$	0.412	0.414
Recovery Time (RN to CKN)	$t_{RC}$	0.000	0.000
Removal Time (RN to CKN)	$t_{RM}$	0.953	0.955
Input Setup Time (TI to CKN)	$t_{SU}$	0.434	0.435
Input Hold Time (TI to CKN)	$t_{HD}$	0.236	0.233
Input Setup Time (TE to CKN)	$t_{SU}$	0.382	0.384
Input Hold Time (TE to CKN)	$t_{HD}$	0.325	0.322



## FD6S/FD6SD2

### D Flip-Flop with Negative Edge Trigger, Reset, Scan, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD6S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.139	$0.080 + 0.030 \cdot SL$	$0.079 + 0.030 \cdot SL$	$0.074 + 0.030 \cdot SL$
	$t_F$	0.114	$0.063 + 0.026 \cdot SL$	$0.066 + 0.025 \cdot SL$	$0.061 + 0.026 \cdot SL$
	$t_{PLH}$	0.502	$0.469 + 0.017 \cdot SL$	$0.477 + 0.015 \cdot SL$	$0.485 + 0.014 \cdot SL$
	$t_{PHL}$	0.407	$0.373 + 0.017 \cdot SL$	$0.382 + 0.015 \cdot SL$	$0.390 + 0.014 \cdot SL$
RN to Q	$t_F$	0.114	$0.062 + 0.026 \cdot SL$	$0.066 + 0.025 \cdot SL$	$0.060 + 0.026 \cdot SL$
	$t_{PHL}$	0.193	$0.160 + 0.017 \cdot SL$	$0.168 + 0.015 \cdot SL$	$0.175 + 0.014 \cdot SL$
CKN to QN	$t_R$	0.115	$0.057 + 0.029 \cdot SL$	$0.053 + 0.030 \cdot SL$	$0.047 + 0.031 \cdot SL$
	$t_F$	0.106	$0.057 + 0.024 \cdot SL$	$0.054 + 0.025 \cdot SL$	$0.048 + 0.026 \cdot SL$
	$t_{PLH}$	0.469	$0.440 + 0.015 \cdot SL$	$0.444 + 0.013 \cdot SL$	$0.445 + 0.013 \cdot SL$
	$t_{PHL}$	0.577	$0.545 + 0.016 \cdot SL$	$0.552 + 0.014 \cdot SL$	$0.556 + 0.014 \cdot SL$
RN to QN	$t_R$	0.133	$0.073 + 0.030 \cdot SL$	$0.074 + 0.030 \cdot SL$	$0.070 + 0.030 \cdot SL$
	$t_{PLH}$	0.289	$0.255 + 0.017 \cdot SL$	$0.264 + 0.015 \cdot SL$	$0.273 + 0.014 \cdot SL$

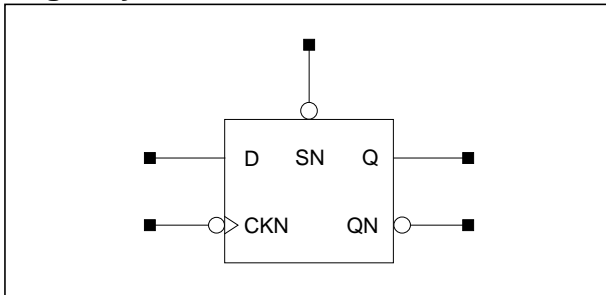
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD6SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.109	$0.080 + 0.015 \cdot SL$	$0.079 + 0.015 \cdot SL$	$0.078 + 0.015 \cdot SL$
	$t_F$	0.091	$0.063 + 0.014 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$
	$t_{PLH}$	0.506	$0.485 + 0.010 \cdot SL$	$0.494 + 0.008 \cdot SL$	$0.508 + 0.007 \cdot SL$
	$t_{PHL}$	0.407	$0.386 + 0.011 \cdot SL$	$0.394 + 0.009 \cdot SL$	$0.409 + 0.008 \cdot SL$
RN to Q	$t_F$	0.091	$0.062 + 0.014 \cdot SL$	$0.067 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$
	$t_{PHL}$	0.192	$0.170 + 0.011 \cdot SL$	$0.179 + 0.009 \cdot SL$	$0.193 + 0.008 \cdot SL$
CKN to QN	$t_R$	0.086	$0.058 + 0.014 \cdot SL$	$0.057 + 0.014 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.084	$0.058 + 0.013 \cdot SL$	$0.059 + 0.013 \cdot SL$	$0.053 + 0.013 \cdot SL$
	$t_{PLH}$	0.504	$0.486 + 0.009 \cdot SL$	$0.492 + 0.007 \cdot SL$	$0.499 + 0.007 \cdot SL$
	$t_{PHL}$	0.621	$0.600 + 0.010 \cdot SL$	$0.608 + 0.008 \cdot SL$	$0.619 + 0.007 \cdot SL$
RN to QN	$t_R$	0.101	$0.071 + 0.015 \cdot SL$	$0.073 + 0.015 \cdot SL$	$0.069 + 0.015 \cdot SL$
	$t_{PLH}$	0.319	$0.299 + 0.010 \cdot SL$	$0.307 + 0.008 \cdot SL$	$0.322 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$

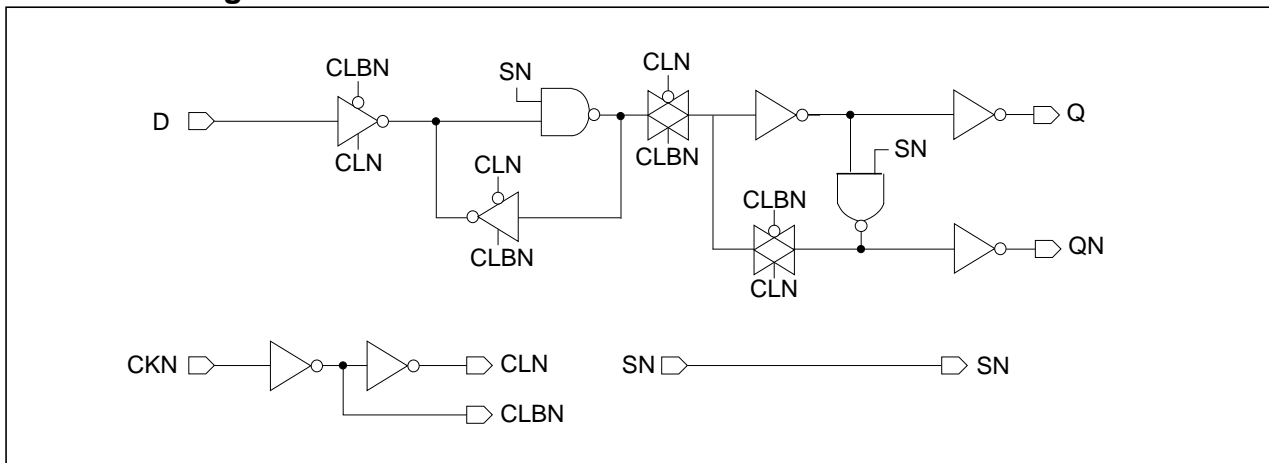


**D Flip-Flop with Negative Edge Trigger, Set, 1X/2X Drive****Logic Symbol****Truth Table**

D	CKN	SN	Q (n+1)	QN (n+1)
0		1	0	1
1		1	1	0
x	x	0	1	0
x		1	Q (n)	QN (n)

**Cell Data**

Input Load (SL)						Gate Count	
FD7			FD7D2			FD7	FD7D2
D	CKN	SN	D	CKN	SN		
0.6	0.6	1.5	0.6	0.6	1.5	5.67	6.33

**Schematic Diagram****Timing Requirements**

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD7	FD7D2
Input Setup Time (D to CKN)	$t_{SU}$	0.303	0.302
Input Hold Time (D to CKN)	$t_{HD}$	0.369	0.370
Pulse Width Low (CKN)	$t_{PWL}$	0.321	0.342
Pulse Width High (CKN)	$t_{PWH}$	0.321	0.342
Pulse Width Low (SN)	$t_{PWL}$	0.272	0.273
Recovery Time (SN to CKN)	$t_{RC}$	0.000	0.000
Removal Time (SN to CKN)	$t_{RM}$	0.327	0.326



## FD7/FD7D2

### D Flip-Flop with Negative Edge Trigger, Set, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.126	$0.070 + 0.028 \cdot SL$	$0.067 + 0.029 \cdot SL$	$0.059 + 0.030 \cdot SL$
	$t_F$	0.120	$0.066 + 0.027 \cdot SL$	$0.067 + 0.027 \cdot SL$	$0.063 + 0.027 \cdot SL$
	$t_{PLH}$	0.457	$0.427 + 0.015 \cdot SL$	$0.433 + 0.014 \cdot SL$	$0.436 + 0.013 \cdot SL$
	$t_{PHL}$	0.421	$0.386 + 0.018 \cdot SL$	$0.394 + 0.016 \cdot SL$	$0.401 + 0.015 \cdot SL$
SN to Q	$t_R$	0.128	$0.074 + 0.027 \cdot SL$	$0.068 + 0.029 \cdot SL$	$0.060 + 0.030 \cdot SL$
	$t_{PLH}$	0.364	$0.334 + 0.015 \cdot SL$	$0.340 + 0.014 \cdot SL$	$0.344 + 0.013 \cdot SL$
CKN to QN	$t_R$	0.127	$0.070 + 0.028 \cdot SL$	$0.067 + 0.029 \cdot SL$	$0.062 + 0.030 \cdot SL$
	$t_F$	0.109	$0.059 + 0.025 \cdot SL$	$0.057 + 0.025 \cdot SL$	$0.052 + 0.026 \cdot SL$
	$t_{PLH}$	0.514	$0.482 + 0.016 \cdot SL$	$0.491 + 0.014 \cdot SL$	$0.496 + 0.013 \cdot SL$
	$t_{PHL}$	0.547	$0.514 + 0.017 \cdot SL$	$0.522 + 0.015 \cdot SL$	$0.528 + 0.014 \cdot SL$
SN to QN	$t_F$	0.123	$0.070 + 0.027 \cdot SL$	$0.075 + 0.025 \cdot SL$	$0.074 + 0.026 \cdot SL$
	$t_{PHL}$	0.212	$0.176 + 0.018 \cdot SL$	$0.185 + 0.016 \cdot SL$	$0.196 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.096	$0.068 + 0.014 \cdot SL$	$0.066 + 0.015 \cdot SL$	$0.060 + 0.015 \cdot SL$
	$t_F$	0.092	$0.064 + 0.014 \cdot SL$	$0.066 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	$t_{PLH}$	0.461	$0.442 + 0.009 \cdot SL$	$0.449 + 0.008 \cdot SL$	$0.458 + 0.007 \cdot SL$
	$t_{PHL}$	0.418	$0.397 + 0.011 \cdot SL$	$0.406 + 0.009 \cdot SL$	$0.419 + 0.008 \cdot SL$
SN to Q	$t_R$	0.101	$0.073 + 0.014 \cdot SL$	$0.073 + 0.014 \cdot SL$	$0.060 + 0.015 \cdot SL$
	$t_{PLH}$	0.397	$0.379 + 0.009 \cdot SL$	$0.386 + 0.008 \cdot SL$	$0.396 + 0.007 \cdot SL$
CKN to QN	$t_R$	0.101	$0.071 + 0.015 \cdot SL$	$0.071 + 0.015 \cdot SL$	$0.067 + 0.015 \cdot SL$
	$t_F$	0.087	$0.060 + 0.014 \cdot SL$	$0.061 + 0.013 \cdot SL$	$0.058 + 0.013 \cdot SL$
	$t_{PLH}$	0.553	$0.533 + 0.010 \cdot SL$	$0.541 + 0.008 \cdot SL$	$0.554 + 0.007 \cdot SL$
	$t_{PHL}$	0.584	$0.563 + 0.010 \cdot SL$	$0.571 + 0.008 \cdot SL$	$0.584 + 0.007 \cdot SL$
SN to QN	$t_F$	0.100	$0.071 + 0.014 \cdot SL$	$0.075 + 0.013 \cdot SL$	$0.076 + 0.013 \cdot SL$
	$t_{PHL}$	0.208	$0.185 + 0.011 \cdot SL$	$0.195 + 0.009 \cdot SL$	$0.212 + 0.008 \cdot SL$

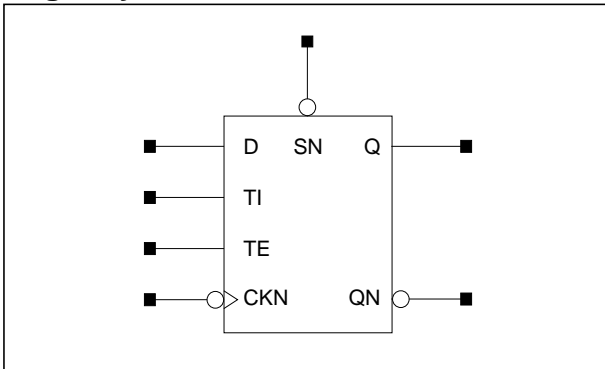
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$








## FD7S/FD7SD2

### D Flip-Flop with Negative Edge Trigger, Set, Scan, 1X/2X Drive

## Logic Symbol



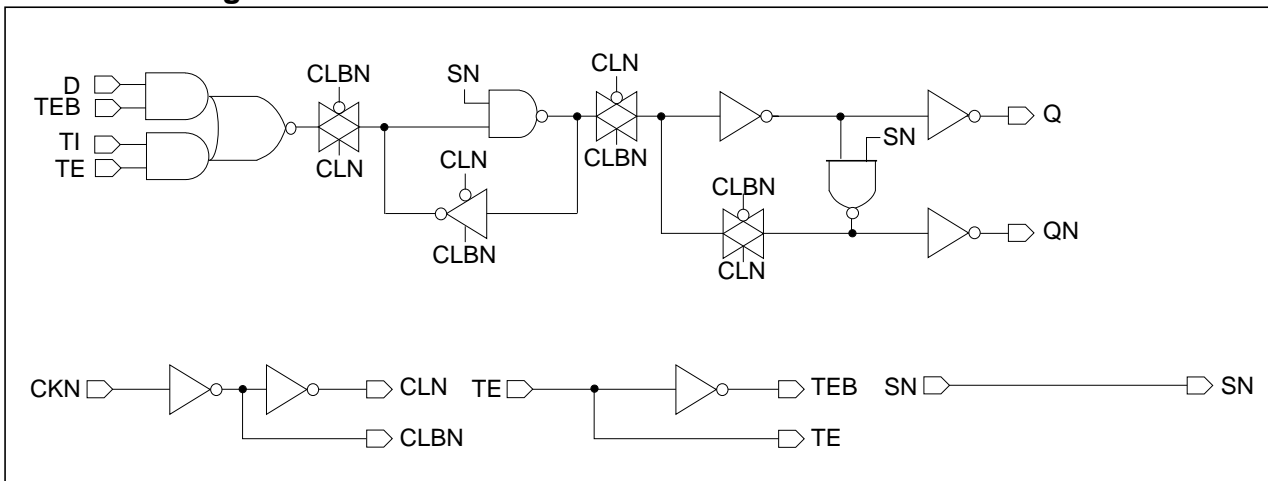
## Truth Table

D	TI	TE	CKN	SN	Q (n+1)	QN (n+1)
0	x	0		1	0	1
1	x	0		1	1	0
x	0	1		1	0	1
x	1	1		1	1	0
x	x	x	x	0	1	0
x	x	x		1	Q (n)	QN (n)

## Cell Data

Input Load (SL)										Gate Count	
FD7S					FD7SD2					FD7S	FD7SD2
D	CKN	SN	TI	TE	D	CKN	SN	TI	TE		
0.4	0.5	1.5	0.6	1.2	0.4	0.6	1.5	0.6	1.2	7.67	8.33

### Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD7S	FD7SD2
Input Setup Time (D to CKN)	$t_{SU}$	0.567	0.566
Input Hold Time (D to CKN)	$t_{HD}$	0.308	0.309
Pulse Width Low (CKN)	$t_{PWL}$	0.328	0.347
Pulse Width High (CKN)	$t_{PWH}$	0.328	0.347
Pulse Width Low (SN)	$t_{PWL}$	0.265	0.265
Recovery Time (SN to CKN)	$t_{RC}$	0.000	0.000
Removal Time (SN to CKN)	$t_{RM}$	0.322	0.323
Input Setup Time (TI to CKN)	$t_{SU}$	0.449	0.444
Input Hold Time (TI to CKN)	$t_{HD}$	0.229	0.230
Input Setup Time (TE to CKN)	$t_{SU}$	0.494	0.426
Input Hold Time (TE to CKN)	$t_{HD}$	0.326	0.326



## FD7S/FD7SD2

### D Flip-Flop with Negative Edge Trigger, Set, Scan, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD7S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.126	$0.071 + 0.028 \cdot SL$	$0.065 + 0.029 \cdot SL$	$0.058 + 0.030 \cdot SL$
	$t_F$	0.119	$0.065 + 0.027 \cdot SL$	$0.067 + 0.027 \cdot SL$	$0.061 + 0.027 \cdot SL$
	$t_{PLH}$	0.469	$0.438 + 0.015 \cdot SL$	$0.444 + 0.014 \cdot SL$	$0.447 + 0.013 \cdot SL$
	$t_{PHL}$	0.428	$0.393 + 0.017 \cdot SL$	$0.401 + 0.016 \cdot SL$	$0.408 + 0.015 \cdot SL$
SN to Q	$t_R$	0.129	$0.074 + 0.027 \cdot SL$	$0.067 + 0.029 \cdot SL$	$0.059 + 0.030 \cdot SL$
	$t_{PLH}$	0.364	$0.334 + 0.015 \cdot SL$	$0.340 + 0.014 \cdot SL$	$0.343 + 0.013 \cdot SL$
CKN to QN	$t_R$	0.126	$0.068 + 0.029 \cdot SL$	$0.067 + 0.029 \cdot SL$	$0.061 + 0.030 \cdot SL$
	$t_F$	0.110	$0.056 + 0.027 \cdot SL$	$0.058 + 0.026 \cdot SL$	$0.052 + 0.027 \cdot SL$
	$t_{PLH}$	0.519	$0.487 + 0.016 \cdot SL$	$0.495 + 0.014 \cdot SL$	$0.500 + 0.013 \cdot SL$
	$t_{PHL}$	0.559	$0.525 + 0.017 \cdot SL$	$0.533 + 0.015 \cdot SL$	$0.538 + 0.014 \cdot SL$
SN to QN	$t_F$	0.126	$0.071 + 0.027 \cdot SL$	$0.073 + 0.027 \cdot SL$	$0.072 + 0.027 \cdot SL$
	$t_{PHL}$	0.213	$0.175 + 0.019 \cdot SL$	$0.186 + 0.016 \cdot SL$	$0.195 + 0.015 \cdot SL$

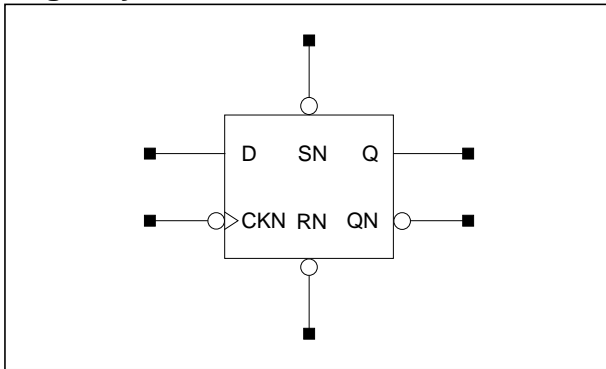
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FD7SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.097	$0.067 + 0.015 \cdot SL$	$0.068 + 0.014 \cdot SL$	$0.059 + 0.015 \cdot SL$
	$t_F$	0.092	$0.064 + 0.014 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	$t_{PLH}$	0.472	$0.453 + 0.009 \cdot SL$	$0.461 + 0.008 \cdot SL$	$0.470 + 0.007 \cdot SL$
	$t_{PHL}$	0.428	$0.407 + 0.011 \cdot SL$	$0.416 + 0.009 \cdot SL$	$0.429 + 0.008 \cdot SL$
SN to Q	$t_R$	0.100	$0.071 + 0.014 \cdot SL$	$0.073 + 0.014 \cdot SL$	$0.061 + 0.015 \cdot SL$
	$t_{PLH}$	0.398	$0.379 + 0.009 \cdot SL$	$0.387 + 0.008 \cdot SL$	$0.397 + 0.007 \cdot SL$
CKN to QN	$t_R$	0.101	$0.071 + 0.015 \cdot SL$	$0.072 + 0.015 \cdot SL$	$0.067 + 0.015 \cdot SL$
	$t_F$	0.086	$0.057 + 0.014 \cdot SL$	$0.061 + 0.013 \cdot SL$	$0.058 + 0.013 \cdot SL$
	$t_{PLH}$	0.562	$0.542 + 0.010 \cdot SL$	$0.550 + 0.008 \cdot SL$	$0.563 + 0.007 \cdot SL$
	$t_{PHL}$	0.595	$0.574 + 0.010 \cdot SL$	$0.582 + 0.008 \cdot SL$	$0.595 + 0.007 \cdot SL$
SN to QN	$t_F$	0.100	$0.072 + 0.014 \cdot SL$	$0.074 + 0.014 \cdot SL$	$0.077 + 0.013 \cdot SL$
	$t_{PHL}$	0.208	$0.186 + 0.011 \cdot SL$	$0.195 + 0.009 \cdot SL$	$0.212 + 0.008 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$

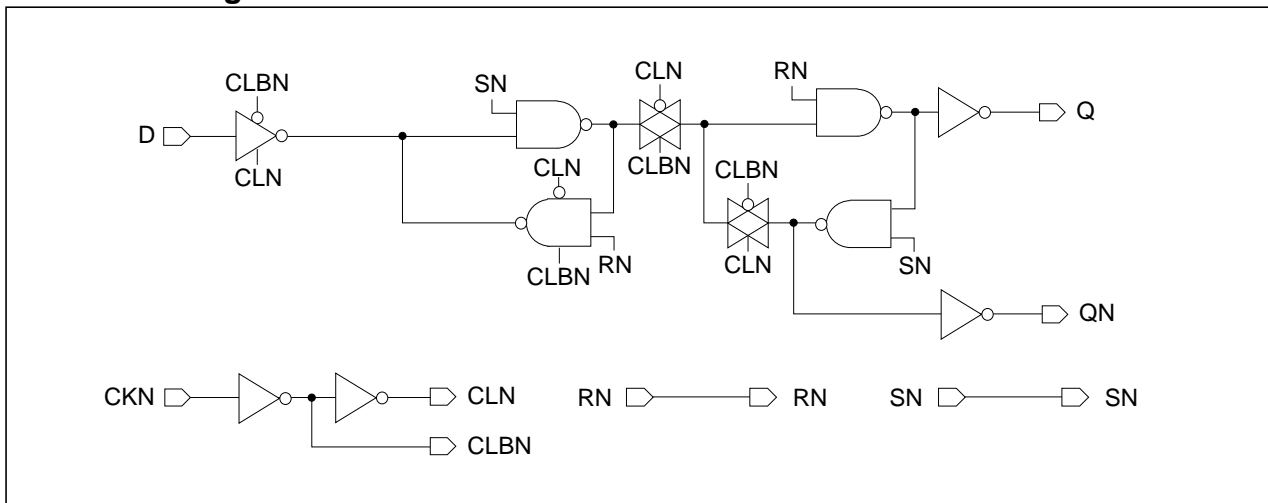


**D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X/2X Drive****Logic Symbol****Truth Table**

D	CKN	RN	SN	Q (n+1)	QN (n+1)
0		1	1	0	1
1		1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x		1	1	Q (n)	QN (n)

**Cell Data**

Input Load (SL)								Gate Count	
FD8				FD8D2				FD8	FD8D2
D	CKN	RN	SN	D	CKN	RN	SN		
0.6	0.5	1.5	1.6	0.6	0.5	1.5	1.6	6.67	7.00

**Schematic Diagram****Timing Requirements**

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD8	FD8D2
Input Setup Time (D to CKN)	$t_{SU}$	0.301	0.302
Input Hold Time (D to CKN)	$t_{HD}$	0.356	0.357
Pulse Width Low (CKN)	$t_{PWL}$	0.331	0.359
Pulse Width High (CKN)	$t_{PWH}$	0.331	0.359
Pulse Width Low (RN)	$t_{PWL}$	0.427	0.429
Pulse Width Low (SN)	$t_{PWL}$	0.296	0.297
Recovery Time (RN to CKN)	$t_{RC}$	0.000	0.000
Removal Time (RN to CKN)	$t_{RM}$	0.973	0.975
Recovery Time (SN to CKN)	$t_{RC}$	0.000	0.000
Removal Time (SN to CKN)	$t_{RM}$	0.331	0.330
Recovery Time (SN to RN)	$t_{RC}$	0.236	0.227
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000



## FD8/FD8D2

### D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.138	$0.080 + 0.029 \cdot SL$	$0.077 + 0.030 \cdot SL$	$0.072 + 0.030 \cdot SL$
	$t_F$	0.115	$0.064 + 0.025 \cdot SL$	$0.064 + 0.025 \cdot SL$	$0.062 + 0.026 \cdot SL$
	$t_{PLH}$	0.486	$0.452 + 0.017 \cdot SL$	$0.461 + 0.015 \cdot SL$	$0.468 + 0.014 \cdot SL$
	$t_{PHL}$	0.415	$0.381 + 0.017 \cdot SL$	$0.390 + 0.015 \cdot SL$	$0.397 + 0.014 \cdot SL$
RN to Q	$t_R$	0.131	$0.073 + 0.029 \cdot SL$	$0.071 + 0.030 \cdot SL$	$0.065 + 0.030 \cdot SL$
	$t_F$	0.113	$0.061 + 0.026 \cdot SL$	$0.064 + 0.025 \cdot SL$	$0.059 + 0.026 \cdot SL$
	$t_{PLH}$	0.179	$0.146 + 0.016 \cdot SL$	$0.155 + 0.014 \cdot SL$	$0.161 + 0.014 \cdot SL$
	$t_{PHL}$	0.192	$0.159 + 0.017 \cdot SL$	$0.167 + 0.015 \cdot SL$	$0.173 + 0.014 \cdot SL$
SN to Q	$t_R$	0.139	$0.082 + 0.028 \cdot SL$	$0.079 + 0.029 \cdot SL$	$0.071 + 0.030 \cdot SL$
	$t_{PLH}$	0.393	$0.359 + 0.017 \cdot SL$	$0.368 + 0.014 \cdot SL$	$0.375 + 0.014 \cdot SL$
CKN to QN	$t_R$	0.128	$0.069 + 0.029 \cdot SL$	$0.066 + 0.030 \cdot SL$	$0.060 + 0.031 \cdot SL$
	$t_F$	0.108	$0.057 + 0.025 \cdot SL$	$0.059 + 0.025 \cdot SL$	$0.053 + 0.026 \cdot SL$
	$t_{PLH}$	0.513	$0.480 + 0.016 \cdot SL$	$0.488 + 0.014 \cdot SL$	$0.493 + 0.014 \cdot SL$
	$t_{PHL}$	0.575	$0.542 + 0.017 \cdot SL$	$0.551 + 0.015 \cdot SL$	$0.557 + 0.014 \cdot SL$
RN to QN	$t_R$	0.150	$0.088 + 0.031 \cdot SL$	$0.093 + 0.030 \cdot SL$	$0.092 + 0.030 \cdot SL$
	$t_{PLH}$	0.332	$0.293 + 0.019 \cdot SL$	$0.306 + 0.016 \cdot SL$	$0.320 + 0.014 \cdot SL$
SN to QN	$t_R$	0.147	$0.084 + 0.031 \cdot SL$	$0.090 + 0.030 \cdot SL$	$0.087 + 0.030 \cdot SL$
	$t_F$	0.122	$0.070 + 0.026 \cdot SL$	$0.072 + 0.025 \cdot SL$	$0.071 + 0.026 \cdot SL$
	$t_{PLH}$	0.201	$0.164 + 0.019 \cdot SL$	$0.175 + 0.016 \cdot SL$	$0.189 + 0.014 \cdot SL$
	$t_{PHL}$	0.212	$0.175 + 0.018 \cdot SL$	$0.185 + 0.016 \cdot SL$	$0.196 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



**D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X/2X Drive****Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)**FD8D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.111	$0.082 + 0.014 \cdot SL$	$0.081 + 0.015 \cdot SL$	$0.078 + 0.015 \cdot SL$
	$t_F$	0.092	$0.067 + 0.013 \cdot SL$	$0.067 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$
	$t_{PLH}$	0.494	$0.473 + 0.010 \cdot SL$	$0.482 + 0.008 \cdot SL$	$0.496 + 0.007 \cdot SL$
	$t_{PHL}$	0.418	$0.397 + 0.010 \cdot SL$	$0.406 + 0.008 \cdot SL$	$0.420 + 0.007 \cdot SL$
RN to Q	$t_R$	0.102	$0.072 + 0.015 \cdot SL$	$0.073 + 0.015 \cdot SL$	$0.070 + 0.015 \cdot SL$
	$t_F$	0.091	$0.063 + 0.014 \cdot SL$	$0.070 + 0.012 \cdot SL$	$0.066 + 0.013 \cdot SL$
	$t_{PLH}$	0.182	$0.162 + 0.010 \cdot SL$	$0.170 + 0.008 \cdot SL$	$0.184 + 0.007 \cdot SL$
	$t_{PHL}$	0.193	$0.172 + 0.011 \cdot SL$	$0.182 + 0.008 \cdot SL$	$0.196 + 0.007 \cdot SL$
SN to Q	$t_R$	0.112	$0.084 + 0.014 \cdot SL$	$0.082 + 0.015 \cdot SL$	$0.078 + 0.015 \cdot SL$
	$t_{PLH}$	0.432	$0.412 + 0.010 \cdot SL$	$0.420 + 0.008 \cdot SL$	$0.434 + 0.007 \cdot SL$
CKN to QN	$t_R$	0.102	$0.072 + 0.015 \cdot SL$	$0.073 + 0.015 \cdot SL$	$0.067 + 0.015 \cdot SL$
	$t_F$	0.089	$0.061 + 0.014 \cdot SL$	$0.067 + 0.012 \cdot SL$	$0.061 + 0.013 \cdot SL$
	$t_{PLH}$	0.556	$0.536 + 0.010 \cdot SL$	$0.544 + 0.008 \cdot SL$	$0.557 + 0.007 \cdot SL$
	$t_{PHL}$	0.620	$0.600 + 0.010 \cdot SL$	$0.609 + 0.008 \cdot SL$	$0.622 + 0.007 \cdot SL$
RN to QN	$t_R$	0.122	$0.090 + 0.016 \cdot SL$	$0.094 + 0.015 \cdot SL$	$0.096 + 0.015 \cdot SL$
	$t_{PLH}$	0.372	$0.348 + 0.012 \cdot SL$	$0.360 + 0.009 \cdot SL$	$0.379 + 0.007 \cdot SL$
SN to QN	$t_R$	0.117	$0.085 + 0.016 \cdot SL$	$0.088 + 0.015 \cdot SL$	$0.092 + 0.015 \cdot SL$
	$t_F$	0.099	$0.071 + 0.014 \cdot SL$	$0.076 + 0.013 \cdot SL$	$0.077 + 0.013 \cdot SL$
	$t_{PLH}$	0.203	$0.180 + 0.011 \cdot SL$	$0.191 + 0.009 \cdot SL$	$0.210 + 0.007 \cdot SL$
	$t_{PHL}$	0.209	$0.187 + 0.011 \cdot SL$	$0.197 + 0.009 \cdot SL$	$0.214 + 0.007 \cdot SL$

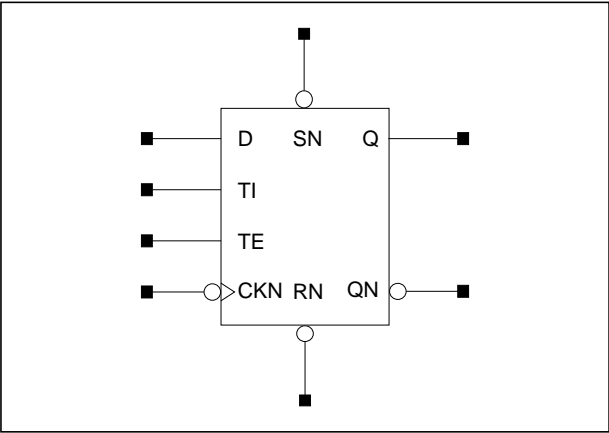
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



FD8S/FD8SD2

D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

Logic Symbol



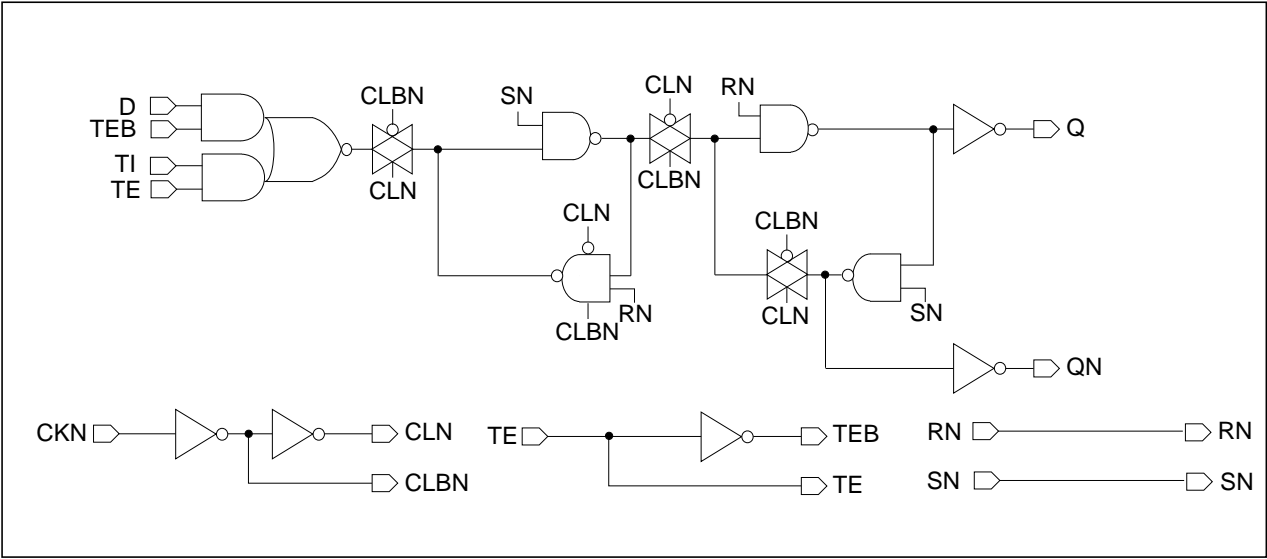
Truth Table

D	TI	TE	CKN	RN	SN	Q (n+1)	QN (n+1)
0	x	0		1	1	0	1
1	x	0		1	1	1	0
x	0	1		1	1	0	1
x	1	1		1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x		1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
FD8S						FD8SD2						FD8S	FD8SD2
D	CKN	RN	SN	TI	TE	D	CKN	RN	SN	TI	TE		
0.4	0.6	1.5	1.6	0.6	1.2	0.4	0.6	1.5	1.6	0.6	1.2	8.67	9.00

Schematic Diagram





D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD8S	FD8SD2
Input Setup Time (D to CKN)	$t_{SU}$	0.562	0.547
Input Hold Time (D to CKN)	$t_{HD}$	0.323	0.322
Pulse Width Low (CKN)	$t_{PWL}$	0.353	0.378
Pulse Width High (CKN)	$t_{PWH}$	0.353	0.378
Pulse Width Low (RN)	$t_{PWL}$	0.438	0.440
Pulse Width Low (SN)	$t_{PWL}$	0.308	0.310
Recovery Time (RN to CKN)	$t_{RC}$	0.000	0.000
Removal Time(RN to CKN)	$t_{RM}$	0.984	1.002
Recovery Time (SN to CKN)	$t_{RC}$	0.000	0.000
Removal Time (SN to CKN)	$t_{RM}$	0.331	0.330
Input Setup Time (TI to CKN)	$t_{SU}$	0.446	0.450
Input Hold Time (TI to CKN)	$t_{HD}$	0.251	0.249
Input Setup Time (TE to CKN)	$t_{SU}$	0.501	0.481
Input Hold Time (TE to CKN)	$t_{HD}$	0.333	0.332
Recovery Time (SN to RN)	$t_{RC}$	0.232	0.234
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000



## FD8S/FD8SD2

### D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FD8S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.138	$0.079 + 0.029 \cdot SL$	$0.081 + 0.029 \cdot SL$	$0.074 + 0.030 \cdot SL$
	$t_F$	0.115	$0.064 + 0.026 \cdot SL$	$0.064 + 0.025 \cdot SL$	$0.062 + 0.026 \cdot SL$
	$t_{PLH}$	0.519	$0.486 + 0.017 \cdot SL$	$0.495 + 0.014 \cdot SL$	$0.502 + 0.014 \cdot SL$
	$t_{PHL}$	0.439	$0.405 + 0.017 \cdot SL$	$0.414 + 0.015 \cdot SL$	$0.421 + 0.014 \cdot SL$
RN to Q	$t_R$	0.131	$0.077 + 0.027 \cdot SL$	$0.070 + 0.029 \cdot SL$	$0.065 + 0.030 \cdot SL$
	$t_F$	0.113	$0.062 + 0.026 \cdot SL$	$0.064 + 0.025 \cdot SL$	$0.059 + 0.026 \cdot SL$
	$t_{PLH}$	0.175	$0.143 + 0.016 \cdot SL$	$0.152 + 0.014 \cdot SL$	$0.158 + 0.013 \cdot SL$
	$t_{PHL}$	0.191	$0.157 + 0.017 \cdot SL$	$0.166 + 0.015 \cdot SL$	$0.171 + 0.014 \cdot SL$
SN to Q	$t_R$	0.137	$0.080 + 0.028 \cdot SL$	$0.079 + 0.029 \cdot SL$	$0.072 + 0.029 \cdot SL$
	$t_{PLH}$	0.408	$0.376 + 0.016 \cdot SL$	$0.384 + 0.014 \cdot SL$	$0.392 + 0.013 \cdot SL$
CKN to QN	$t_R$	0.126	$0.068 + 0.029 \cdot SL$	$0.067 + 0.029 \cdot SL$	$0.062 + 0.030 \cdot SL$
	$t_F$	0.110	$0.060 + 0.025 \cdot SL$	$0.060 + 0.025 \cdot SL$	$0.054 + 0.026 \cdot SL$
	$t_{PLH}$	0.536	$0.504 + 0.016 \cdot SL$	$0.512 + 0.014 \cdot SL$	$0.518 + 0.013 \cdot SL$
	$t_{PHL}$	0.614	$0.580 + 0.017 \cdot SL$	$0.589 + 0.015 \cdot SL$	$0.595 + 0.014 \cdot SL$
RN to QN	$t_R$	0.152	$0.090 + 0.031 \cdot SL$	$0.096 + 0.029 \cdot SL$	$0.098 + 0.029 \cdot SL$
	$t_{PLH}$	0.333	$0.294 + 0.019 \cdot SL$	$0.307 + 0.016 \cdot SL$	$0.323 + 0.014 \cdot SL$
SN to QN	$t_R$	0.148	$0.085 + 0.031 \cdot SL$	$0.094 + 0.029 \cdot SL$	$0.095 + 0.029 \cdot SL$
	$t_F$	0.125	$0.073 + 0.026 \cdot SL$	$0.075 + 0.026 \cdot SL$	$0.075 + 0.026 \cdot SL$
	$t_{PLH}$	0.204	$0.166 + 0.019 \cdot SL$	$0.178 + 0.016 \cdot SL$	$0.193 + 0.014 \cdot SL$
	$t_{PHL}$	0.216	$0.180 + 0.018 \cdot SL$	$0.190 + 0.016 \cdot SL$	$0.201 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



**D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive****Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)**FD8SD2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	$t_R$	0.112	$0.082 + 0.015 \cdot SL$	$0.083 + 0.015 \cdot SL$	$0.079 + 0.015 \cdot SL$
	$t_F$	0.093	$0.065 + 0.014 \cdot SL$	$0.068 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$
	$t_{PLH}$	0.526	$0.505 + 0.010 \cdot SL$	$0.514 + 0.008 \cdot SL$	$0.529 + 0.007 \cdot SL$
	$t_{PHL}$	0.442	$0.420 + 0.011 \cdot SL$	$0.429 + 0.009 \cdot SL$	$0.443 + 0.008 \cdot SL$
RN to Q	$t_R$	0.102	$0.073 + 0.014 \cdot SL$	$0.071 + 0.015 \cdot SL$	$0.068 + 0.015 \cdot SL$
	$t_F$	0.089	$0.060 + 0.015 \cdot SL$	$0.066 + 0.013 \cdot SL$	$0.063 + 0.013 \cdot SL$
	$t_{PLH}$	0.177	$0.157 + 0.010 \cdot SL$	$0.166 + 0.008 \cdot SL$	$0.179 + 0.007 \cdot SL$
	$t_{PHL}$	0.189	$0.167 + 0.011 \cdot SL$	$0.176 + 0.008 \cdot SL$	$0.189 + 0.008 \cdot SL$
SN to Q	$t_R$	0.112	$0.083 + 0.015 \cdot SL$	$0.084 + 0.014 \cdot SL$	$0.078 + 0.015 \cdot SL$
	$t_{PLH}$	0.446	$0.426 + 0.010 \cdot SL$	$0.434 + 0.008 \cdot SL$	$0.449 + 0.007 \cdot SL$
CKN to QN	$t_R$	0.102	$0.073 + 0.015 \cdot SL$	$0.073 + 0.015 \cdot SL$	$0.069 + 0.015 \cdot SL$
	$t_F$	0.091	$0.064 + 0.014 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.062 + 0.013 \cdot SL$
	$t_{PLH}$	0.577	$0.557 + 0.010 \cdot SL$	$0.565 + 0.008 \cdot SL$	$0.579 + 0.007 \cdot SL$
	$t_{PHL}$	0.658	$0.637 + 0.011 \cdot SL$	$0.645 + 0.008 \cdot SL$	$0.658 + 0.007 \cdot SL$
RN to QN	$t_R$	0.127	$0.095 + 0.016 \cdot SL$	$0.098 + 0.015 \cdot SL$	$0.101 + 0.015 \cdot SL$
	$t_{PLH}$	0.365	$0.341 + 0.012 \cdot SL$	$0.353 + 0.009 \cdot SL$	$0.374 + 0.008 \cdot SL$
SN to QN	$t_R$	0.121	$0.088 + 0.016 \cdot SL$	$0.091 + 0.015 \cdot SL$	$0.099 + 0.015 \cdot SL$
	$t_F$	0.104	$0.075 + 0.014 \cdot SL$	$0.078 + 0.014 \cdot SL$	$0.080 + 0.013 \cdot SL$
	$t_{PLH}$	0.206	$0.182 + 0.012 \cdot SL$	$0.193 + 0.009 \cdot SL$	$0.214 + 0.008 \cdot SL$
	$t_{PHL}$	0.216	$0.192 + 0.012 \cdot SL$	$0.203 + 0.009 \cdot SL$	$0.220 + 0.008 \cdot SL$

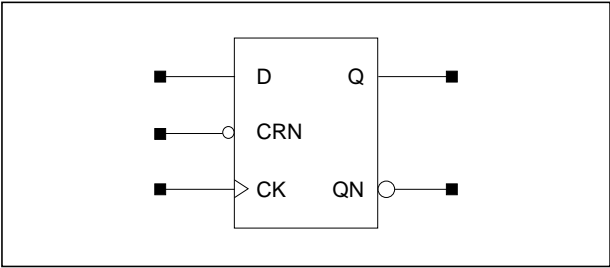
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# FDS2/FDS2D2

## D Flip-Flop with Synchronous Clear, 1X/2X Drive

### Logic Symbol



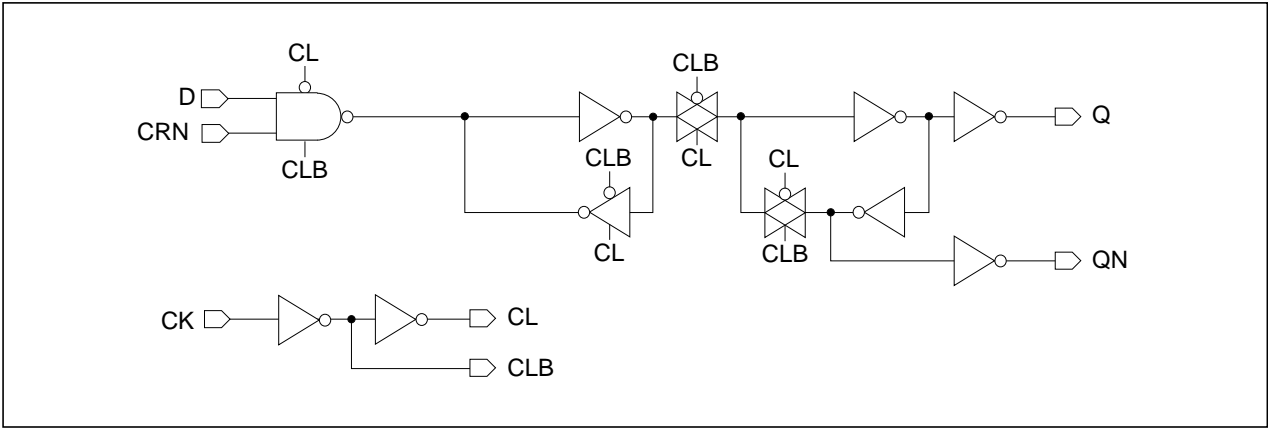
### Truth Table

D	CRN	CK	Q (n+1)	QN (n+1)
0	1		0	1
1	1		1	0
x	0		0	1
x	x		Q (n)	QN (n)

### Cell Data

Input Load (SL)						Gate Count	
FDS2			FDS2D2			FDS2	FDS2D2
D	CRN	CK	D	CRN	CK		
0.6	0.6	0.6	0.6	0.6	0.6	5.33	6.00

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS2	FDS2D2
Input Setup Time (D to CK)	t <sub>SU</sub>	0.428	0.425
Input Hold Time (D to CK)	t <sub>HD</sub>	0.109	0.119
Pulse Width Low (CK)	t <sub>PWL</sub>	0.385	0.385
Pulse Width High (CK)	t <sub>PWH</sub>	0.313	0.336
Input Setup Time (CRN to CK)	t <sub>SU</sub>	0.379	0.377
Input Hold Time (CRN to CK)	t <sub>HD</sub>	0.098	0.109



## D Flip-Flop with Synchronous Clear, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.126	$0.068 + 0.029 \cdot SL$	$0.065 + 0.030 \cdot SL$	$0.058 + 0.031 \cdot SL$
	$t_F$	0.116	$0.064 + 0.026 \cdot SL$	$0.066 + 0.025 \cdot SL$	$0.061 + 0.026 \cdot SL$
	$t_{PLH}$	0.393	$0.362 + 0.015 \cdot SL$	$0.368 + 0.014 \cdot SL$	$0.371 + 0.013 \cdot SL$
	$t_{PHL}$	0.409	$0.374 + 0.017 \cdot SL$	$0.383 + 0.015 \cdot SL$	$0.391 + 0.014 \cdot SL$
CK to QN	$t_R$	0.116	$0.056 + 0.030 \cdot SL$	$0.052 + 0.031 \cdot SL$	$0.046 + 0.031 \cdot SL$
	$t_F$	0.103	$0.050 + 0.026 \cdot SL$	$0.051 + 0.026 \cdot SL$	$0.045 + 0.027 \cdot SL$
	$t_{PLH}$	0.468	$0.439 + 0.015 \cdot SL$	$0.443 + 0.014 \cdot SL$	$0.444 + 0.014 \cdot SL$
	$t_{PHL}$	0.465	$0.433 + 0.016 \cdot SL$	$0.440 + 0.014 \cdot SL$	$0.443 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FDS2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.094	$0.067 + 0.014 \cdot SL$	$0.064 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.088	$0.060 + 0.014 \cdot SL$	$0.062 + 0.013 \cdot SL$	$0.061 + 0.013 \cdot SL$
	$t_{PLH}$	0.398	$0.379 + 0.009 \cdot SL$	$0.386 + 0.007 \cdot SL$	$0.394 + 0.007 \cdot SL$
	$t_{PHL}$	0.410	$0.389 + 0.011 \cdot SL$	$0.397 + 0.008 \cdot SL$	$0.410 + 0.007 \cdot SL$
CK to QN	$t_R$	0.085	$0.056 + 0.014 \cdot SL$	$0.056 + 0.014 \cdot SL$	$0.045 + 0.015 \cdot SL$
	$t_F$	0.081	$0.054 + 0.013 \cdot SL$	$0.056 + 0.013 \cdot SL$	$0.050 + 0.014 \cdot SL$
	$t_{PLH}$	0.503	$0.486 + 0.009 \cdot SL$	$0.492 + 0.007 \cdot SL$	$0.498 + 0.007 \cdot SL$
	$t_{PHL}$	0.503	$0.483 + 0.010 \cdot SL$	$0.491 + 0.008 \cdot SL$	$0.501 + 0.007 \cdot SL$

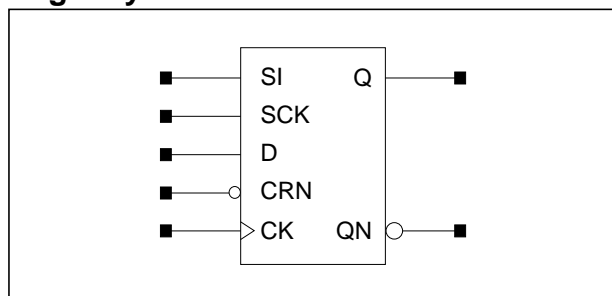
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# FDS2CS/FDS2CSD2

## D Flip-Flop with Synchronous Clear, Scan Clock, 1X/2X Drive

### Logic Symbol



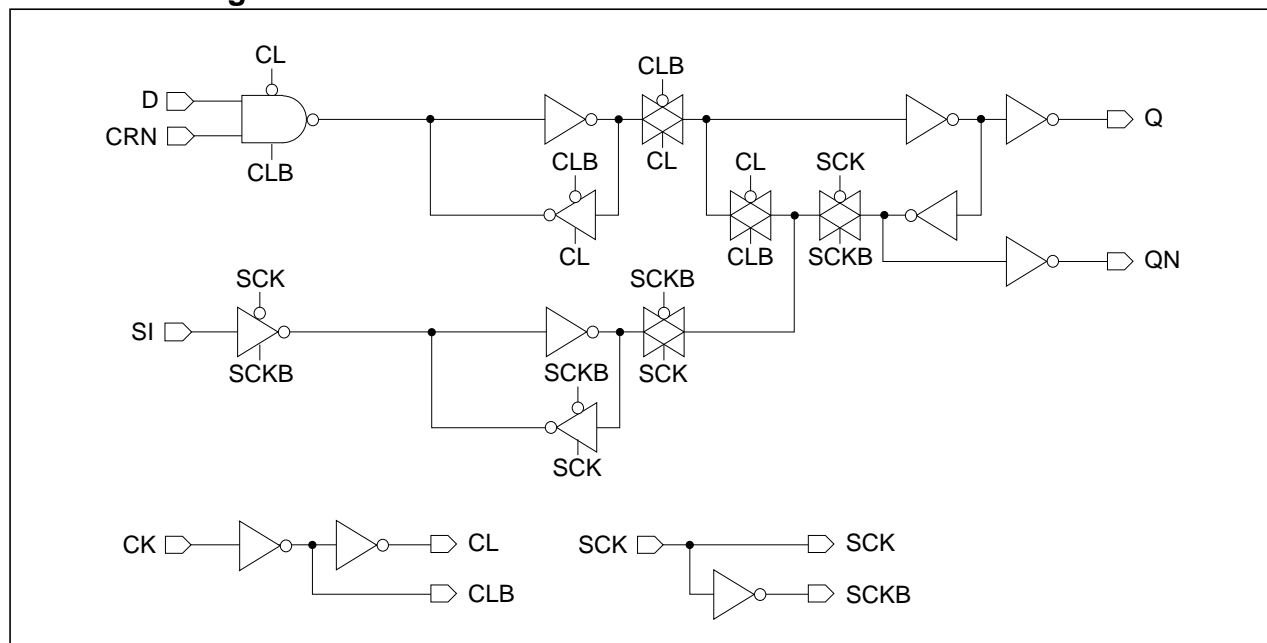
### Truth Table

SI	SCK	D	CRN	CK	Q (n+1)	QN (n+1)
x	0	0	1		0	1
x	0	1	1		1	0
0		x	x	0	0	1
1		x	x	0	1	0
x	0	x	0		0	1
x	0	x	x		Q(n)	QN(n)
x		x	x	0	Q(n)	QN(n)

### Cell Data

Input Load (SL)										Gate Count	
FDS2CS					FDS2CSD2					FDS2CS	FDS2CSD2
D	SI	CK	SCK	CRN	D	SI	CK	SCK	CRN		
0.6	0.6	0.6	1.5	0.6	0.6	0.6	0.6	1.5	0.6	8.67	9.33

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS2CS	FDS2CSD2
Input Setup Time (D to CK)	$t_{SU}$	0.427	0.428
Input Hold Time (D to CK)	$t_{HD}$	0.111	0.113
Input Setup Time (SI to SCK)	$t_{SU}$	0.769	0.769
Input Hold Time (SI to SCK)	$t_{HD}$	0.068	0.068
Pulse Width Low (CK)	$t_{PWL}$	0.386	0.387
Pulse Width High (CK)	$t_{PWH}$	0.328	0.350
Pulse Width Low (SCK)	$t_{PWL}$	0.299	0.299
Pulse Width High (SCK)	$t_{PWH}$	0.375	0.412
Input Setup Time (CRN to CK)	$t_{SU}$	0.378	0.376
Input Hold Time (CRN to CK)	$t_{HD}$	0.100	0.101



## D Flip-Flop with Synchronous Clear, Scan Clock, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FDS2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.126	$0.070 + 0.028 \cdot SL$	$0.065 + 0.029 \cdot SL$	$0.057 + 0.030 \cdot SL$
	$t_F$	0.114	$0.063 + 0.026 \cdot SL$	$0.064 + 0.025 \cdot SL$	$0.058 + 0.026 \cdot SL$
	$t_{PLH}$	0.401	$0.370 + 0.015 \cdot SL$	$0.376 + 0.014 \cdot SL$	$0.379 + 0.013 \cdot SL$
	$t_{PHL}$	0.408	$0.375 + 0.017 \cdot SL$	$0.382 + 0.015 \cdot SL$	$0.388 + 0.014 \cdot SL$
SCK to Q	$t_R$	0.141	$0.086 + 0.028 \cdot SL$	$0.083 + 0.028 \cdot SL$	$0.073 + 0.030 \cdot SL$
	$t_F$	0.119	$0.067 + 0.026 \cdot SL$	$0.070 + 0.025 \cdot SL$	$0.065 + 0.026 \cdot SL$
	$t_{PLH}$	0.457	$0.425 + 0.016 \cdot SL$	$0.433 + 0.014 \cdot SL$	$0.438 + 0.013 \cdot SL$
	$t_{PHL}$	0.390	$0.356 + 0.017 \cdot SL$	$0.364 + 0.015 \cdot SL$	$0.372 + 0.014 \cdot SL$
CK to QN	$t_R$	0.137	$0.078 + 0.029 \cdot SL$	$0.076 + 0.030 \cdot SL$	$0.071 + 0.030 \cdot SL$
	$t_F$	0.123	$0.070 + 0.026 \cdot SL$	$0.071 + 0.026 \cdot SL$	$0.069 + 0.026 \cdot SL$
	$t_{PLH}$	0.508	$0.474 + 0.017 \cdot SL$	$0.483 + 0.015 \cdot SL$	$0.490 + 0.014 \cdot SL$
	$t_{PHL}$	0.516	$0.481 + 0.018 \cdot SL$	$0.490 + 0.016 \cdot SL$	$0.498 + 0.015 \cdot SL$
SCK to QN	$t_R$	0.122	$0.064 + 0.029 \cdot SL$	$0.059 + 0.030 \cdot SL$	$0.053 + 0.031 \cdot SL$
	$t_F$	0.113	$0.061 + 0.026 \cdot SL$	$0.062 + 0.026 \cdot SL$	$0.056 + 0.026 \cdot SL$
	$t_{PLH}$	0.468	$0.438 + 0.015 \cdot SL$	$0.443 + 0.014 \cdot SL$	$0.445 + 0.014 \cdot SL$
	$t_{PHL}$	0.550	$0.517 + 0.017 \cdot SL$	$0.525 + 0.015 \cdot SL$	$0.530 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FDS2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.094	$0.066 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.056 + 0.015 \cdot SL$
	$t_F$	0.087	$0.058 + 0.014 \cdot SL$	$0.062 + 0.013 \cdot SL$	$0.060 + 0.013 \cdot SL$
	$t_{PLH}$	0.401	$0.383 + 0.009 \cdot SL$	$0.390 + 0.007 \cdot SL$	$0.398 + 0.007 \cdot SL$
	$t_{PHL}$	0.407	$0.386 + 0.011 \cdot SL$	$0.395 + 0.008 \cdot SL$	$0.407 + 0.007 \cdot SL$
SCK to Q	$t_R$	0.114	$0.086 + 0.014 \cdot SL$	$0.085 + 0.014 \cdot SL$	$0.075 + 0.015 \cdot SL$
	$t_F$	0.093	$0.065 + 0.014 \cdot SL$	$0.068 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	$t_{PLH}$	0.467	$0.446 + 0.010 \cdot SL$	$0.456 + 0.008 \cdot SL$	$0.468 + 0.007 \cdot SL$
	$t_{PHL}$	0.395	$0.373 + 0.011 \cdot SL$	$0.382 + 0.009 \cdot SL$	$0.396 + 0.008 \cdot SL$
CK to QN	$t_R$	0.102	$0.072 + 0.015 \cdot SL$	$0.074 + 0.015 \cdot SL$	$0.068 + 0.015 \cdot SL$
	$t_F$	0.096	$0.067 + 0.014 \cdot SL$	$0.070 + 0.014 \cdot SL$	$0.071 + 0.013 \cdot SL$
	$t_{PLH}$	0.537	$0.517 + 0.010 \cdot SL$	$0.525 + 0.008 \cdot SL$	$0.539 + 0.007 \cdot SL$
	$t_{PHL}$	0.549	$0.527 + 0.011 \cdot SL$	$0.536 + 0.009 \cdot SL$	$0.551 + 0.008 \cdot SL$
SCK to QN	$t_R$	0.089	$0.060 + 0.015 \cdot SL$	$0.061 + 0.014 \cdot SL$	$0.051 + 0.015 \cdot SL$
	$t_F$	0.088	$0.060 + 0.014 \cdot SL$	$0.064 + 0.013 \cdot SL$	$0.058 + 0.013 \cdot SL$
	$t_{PLH}$	0.504	$0.486 + 0.009 \cdot SL$	$0.493 + 0.007 \cdot SL$	$0.501 + 0.007 \cdot SL$
	$t_{PHL}$	0.596	$0.575 + 0.010 \cdot SL$	$0.583 + 0.008 \cdot SL$	$0.596 + 0.007 \cdot SL$

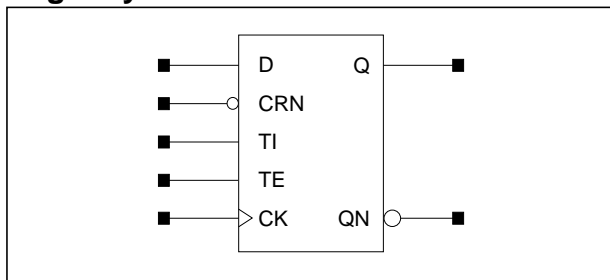
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FDS2S/FDS2SD2

### D Flip-Flop with Synchronous Clear, Scan, 1X/2X Drive

#### Logic Symbol



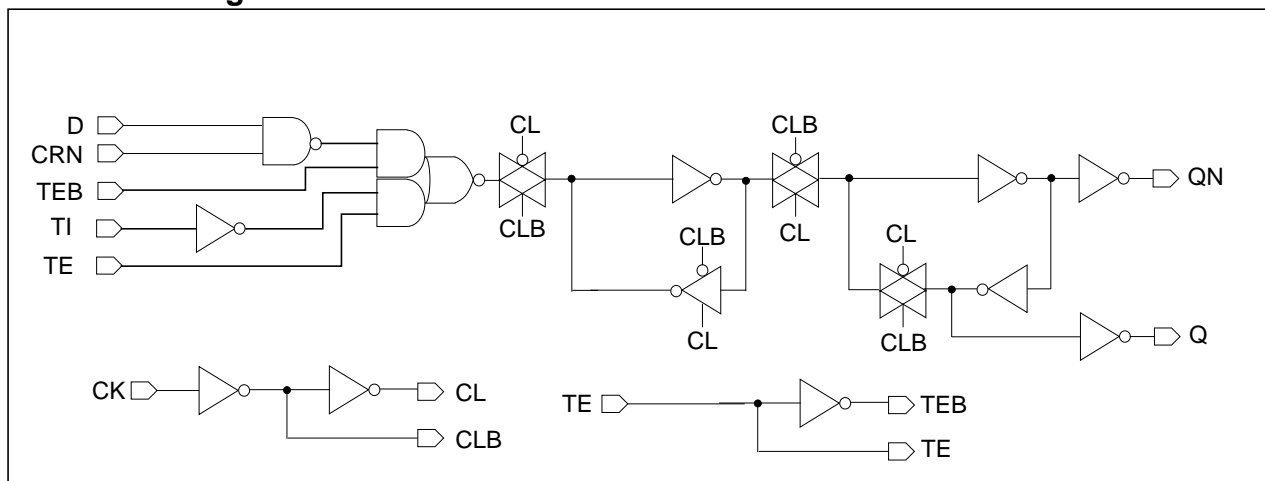
#### Truth Table

D	CRN	TI	TE	CK	Q (n+1)	QN (n+1)
0	1	x	0		0	1
1	1	x	0		1	0
x	0	x	0		0	1
x	x	0	1		0	1
x	x	1	1		1	0
x	x	x	x		Q (n)	QN (n)

#### Cell Data

Input Load (SL)										Gate Count	
FDS2S					FDS2SD2					FDS2S	FDS2SD2
D	CRN	CK	TI	TE	D	CRN	CK	TI	TE		
0.5	0.6	0.6	0.5	1.2	0.5	0.6	0.6	0.6	1.2	8.00	8.67

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS2S	FDS2SD2
Input Setup Time (D to CK)	$t_{SU}$	0.498	0.500
Input Hold Time (D to CK)	$t_{HD}$	0.000	0.000
Input Setup Time (CRN to CK)	$t_{SU}$	0.522	0.521
Input Hold Time (CRN to CK)	$t_{HD}$	0.000	0.000
Pulse Width Low (CK)	$t_{PWL}$	0.440	0.431
Pulse Width High (CK)	$t_{PWH}$	0.311	0.329
Input Setup Time (TI to CK)	$t_{SU}$	0.627	0.609
Input Hold Time (TI to CK)	$t_{HD}$	0.000	0.000
Input Setup Time (TE to CK)	$t_{SU}$	0.506	0.382
Input Hold Time (TE to CK)	$t_{HD}$	0.016	0.033



## D Flip-Flop with Synchronous Clear, Scan, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FDS2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.114	$0.057 + 0.029 \cdot SL$	$0.052 + 0.030 \cdot SL$	$0.047 + 0.031 \cdot SL$
	$t_F$	0.109	$0.057 + 0.026 \cdot SL$	$0.052 + 0.028 \cdot SL$	$0.047 + 0.028 \cdot SL$
	$t_{PLH}$	0.479	$0.450 + 0.014 \cdot SL$	$0.454 + 0.013 \cdot SL$	$0.455 + 0.013 \cdot SL$
	$t_{PHL}$	0.473	$0.440 + 0.017 \cdot SL$	$0.446 + 0.015 \cdot SL$	$0.449 + 0.015 \cdot SL$
CK to QN	$t_R$	0.123	$0.067 + 0.028 \cdot SL$	$0.063 + 0.029 \cdot SL$	$0.055 + 0.030 \cdot SL$
	$t_F$	0.113	$0.062 + 0.026 \cdot SL$	$0.064 + 0.025 \cdot SL$	$0.058 + 0.026 \cdot SL$
	$t_{PLH}$	0.394	$0.363 + 0.015 \cdot SL$	$0.370 + 0.014 \cdot SL$	$0.373 + 0.013 \cdot SL$
	$t_{PHL}$	0.419	$0.385 + 0.017 \cdot SL$	$0.394 + 0.015 \cdot SL$	$0.402 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FDS2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.085	$0.057 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.081	$0.053 + 0.014 \cdot SL$	$0.057 + 0.013 \cdot SL$	$0.050 + 0.014 \cdot SL$
	$t_{PLH}$	0.506	$0.489 + 0.009 \cdot SL$	$0.495 + 0.007 \cdot SL$	$0.501 + 0.007 \cdot SL$
	$t_{PHL}$	0.500	$0.480 + 0.010 \cdot SL$	$0.488 + 0.008 \cdot SL$	$0.498 + 0.007 \cdot SL$
CK to QN	$t_R$	0.093	$0.065 + 0.014 \cdot SL$	$0.063 + 0.015 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.089	$0.061 + 0.014 \cdot SL$	$0.064 + 0.013 \cdot SL$	$0.062 + 0.013 \cdot SL$
	$t_{PLH}$	0.393	$0.375 + 0.009 \cdot SL$	$0.382 + 0.007 \cdot SL$	$0.390 + 0.007 \cdot SL$
	$t_{PHL}$	0.415	$0.394 + 0.011 \cdot SL$	$0.402 + 0.008 \cdot SL$	$0.415 + 0.007 \cdot SL$

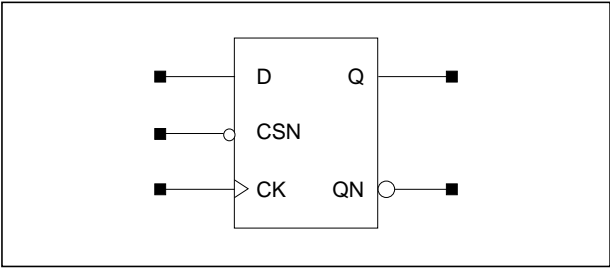
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# FDS3/FDS3D2

## D Flip-Flop with Synchronous Set, 1X/2X Drive

### Logic Symbol



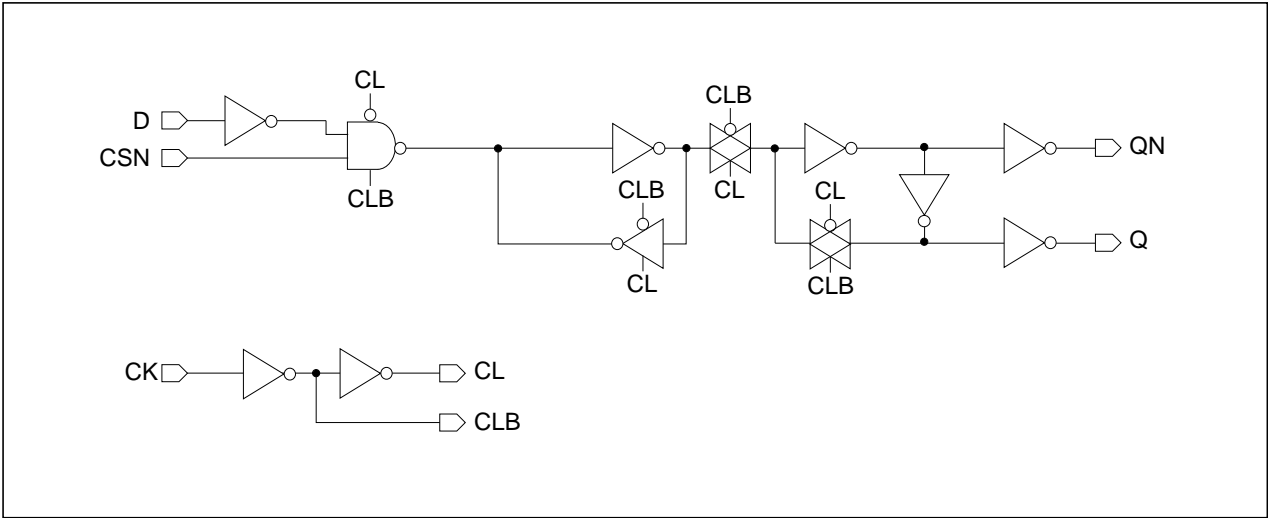
### Truth Table

D	CSN	CK	Q (n+1)	QN (n+1)
0	1		0	1
1	1		1	0
x	0		1	0
x	x		Q (n)	QN (n)

### Cell Data

Input Load (SL)						Gate Count	
FDS3			FDS3D2			FDS3	FDS3D2
D	CSN	CK	D	CSN	CK		
0.6	0.5	0.6	0.6	0.5	0.6	6.00	6.67

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS3	FDS3D2
Input Setup Time (D to CK)	t <sub>SU</sub>	0.484	0.484
Input Hold Time (D to CK)	t <sub>HD</sub>	0.096	0.095
Input Setup Time (CSN to CK)	t <sub>SU</sub>	0.363	0.364
Input Hold Time (CSN to CK)	t <sub>HD</sub>	0.132	0.131
Pulse Width Low (CK)	t <sub>PWL</sub>	0.378	0.380
Pulse Width High (CK)	t <sub>PWH</sub>	0.319	0.338



## D Flip-Flop with Synchronous Set, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FDS3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.113	$0.055 + 0.029 \cdot SL$	$0.050 + 0.030 \cdot SL$	$0.045 + 0.031 \cdot SL$
	$t_F$	0.104	$0.050 + 0.027 \cdot SL$	$0.050 + 0.027 \cdot SL$	$0.044 + 0.027 \cdot SL$
	$t_{PLH}$	0.473	$0.444 + 0.015 \cdot SL$	$0.448 + 0.014 \cdot SL$	$0.449 + 0.013 \cdot SL$
	$t_{PHL}$	0.476	$0.443 + 0.017 \cdot SL$	$0.450 + 0.015 \cdot SL$	$0.453 + 0.014 \cdot SL$
CK to QN	$t_R$	0.125	$0.067 + 0.029 \cdot SL$	$0.064 + 0.030 \cdot SL$	$0.057 + 0.030 \cdot SL$
	$t_F$	0.115	$0.061 + 0.027 \cdot SL$	$0.062 + 0.027 \cdot SL$	$0.058 + 0.027 \cdot SL$
	$t_{PLH}$	0.401	$0.370 + 0.015 \cdot SL$	$0.376 + 0.014 \cdot SL$	$0.380 + 0.014 \cdot SL$
	$t_{PHL}$	0.417	$0.382 + 0.018 \cdot SL$	$0.390 + 0.015 \cdot SL$	$0.398 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FDS3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.085	$0.056 + 0.015 \cdot SL$	$0.056 + 0.014 \cdot SL$	$0.045 + 0.015 \cdot SL$
	$t_F$	0.080	$0.051 + 0.015 \cdot SL$	$0.057 + 0.013 \cdot SL$	$0.050 + 0.014 \cdot SL$
	$t_{PLH}$	0.511	$0.493 + 0.009 \cdot SL$	$0.500 + 0.007 \cdot SL$	$0.506 + 0.007 \cdot SL$
	$t_{PHL}$	0.507	$0.487 + 0.010 \cdot SL$	$0.495 + 0.008 \cdot SL$	$0.505 + 0.007 \cdot SL$
CK to QN	$t_R$	0.093	$0.066 + 0.014 \cdot SL$	$0.063 + 0.015 \cdot SL$	$0.056 + 0.015 \cdot SL$
	$t_F$	0.087	$0.059 + 0.014 \cdot SL$	$0.063 + 0.013 \cdot SL$	$0.060 + 0.013 \cdot SL$
	$t_{PLH}$	0.402	$0.383 + 0.009 \cdot SL$	$0.390 + 0.007 \cdot SL$	$0.398 + 0.007 \cdot SL$
	$t_{PHL}$	0.417	$0.396 + 0.011 \cdot SL$	$0.405 + 0.008 \cdot SL$	$0.417 + 0.007 \cdot SL$

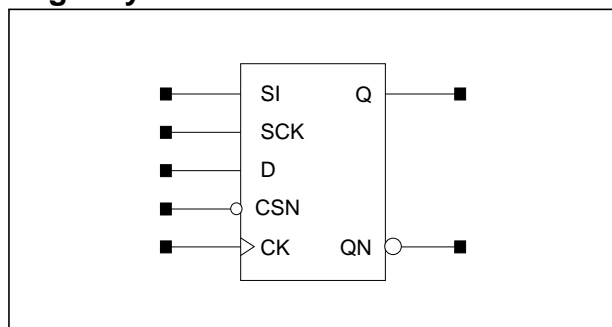
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# FDS3CS/FDS3CSD2

## D Flip-Flop with Synchronous Set, 1X/2X Drive

### Logic Symbol



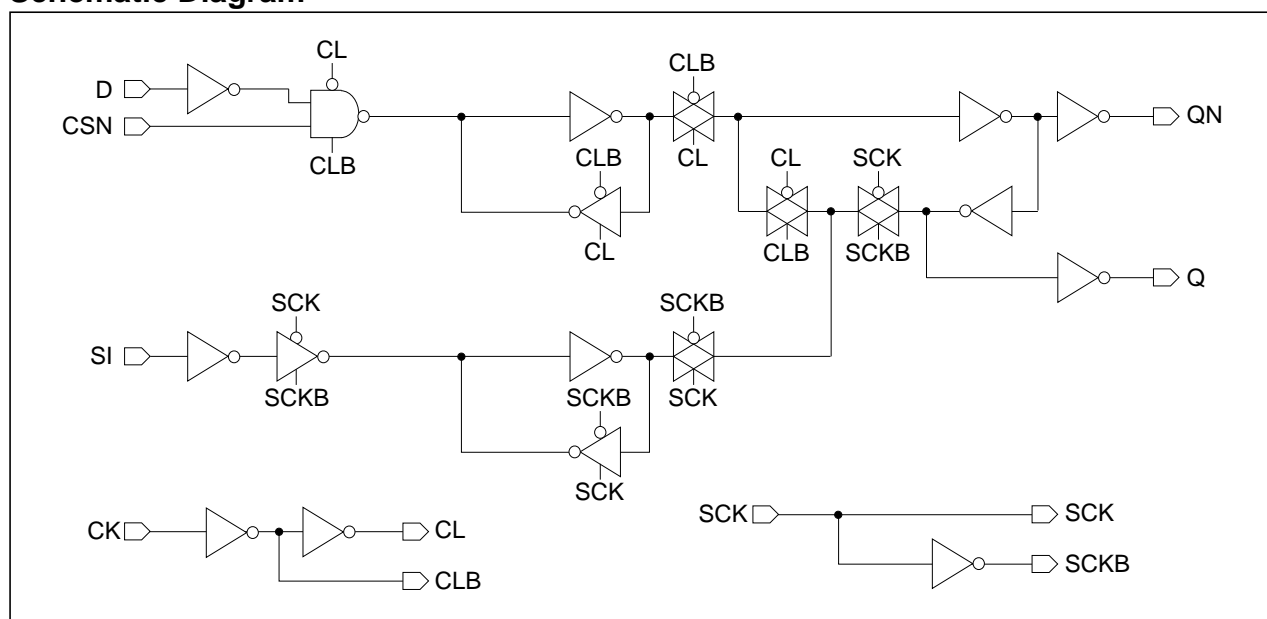
### Truth Table

SI	SCK	D	CSN	CK	Q(n+1)	QN(n+1)
x	0	0	1		0	1
x	0	1	1		1	0
0		x	x	0	0	1
1		x	x	0	1	0
x	0	x	0		1	0
x	0	x	x		Q(n)	QN(n)
x		x	x	0	Q(n)	QN(n)

### Cell Data

Input Load (SL)										Gate Count	
FDS3CS					FDS3CSD2					FDS3CS	FDS3CSD2
D	SI	CK	SCK	CSN	D	SI	CK	SCK	CSN		
0.6	0.6	0.6	1.6	0.5	0.6	0.6	0.6	1.6	0.5	9.67	10.33

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS3CS	FDS3CSD2
Input Setup Time (D to CK)	t <sub>SU</sub>	0.483	0.483
Input Hold Time (D to CK)	t <sub>HD</sub>	0.096	0.094
Input Setup Time (SI to SCK)	t <sub>SU</sub>	0.690	0.691
Input Hold Time (SI to SCK)	t <sub>HD</sub>	0.000	0.000
Pulse Width Low (CK)	t <sub>PWL</sub>	0.379	0.380
Pulse Width High (CK)	t <sub>PWH</sub>	0.330	0.349
Pulse Width Low (SCK)	t <sub>PWL</sub>	0.302	0.302
Pulse Width High (SCK)	t <sub>PWH</sub>	0.369	0.399
Input Setup Time (CSN to CK)	t <sub>SU</sub>	0.364	0.365
Input Hold Time (CSN to CK)	t <sub>HD</sub>	0.132	0.130



## D Flip-Flop with Synchronous Set, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FDS3CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.130	$0.071 + 0.029 \cdot SL$	$0.073 + 0.029 \cdot SL$	$0.067 + 0.030 \cdot SL$
	$t_F$	0.120	$0.067 + 0.027 \cdot SL$	$0.068 + 0.026 \cdot SL$	$0.066 + 0.026 \cdot SL$
	$t_{PLH}$	0.513	$0.479 + 0.017 \cdot SL$	$0.488 + 0.014 \cdot SL$	$0.496 + 0.013 \cdot SL$
	$t_{PHL}$	0.519	$0.483 + 0.018 \cdot SL$	$0.492 + 0.016 \cdot SL$	$0.500 + 0.015 \cdot SL$
SCK to Q	$t_R$	0.118	$0.061 + 0.028 \cdot SL$	$0.056 + 0.029 \cdot SL$	$0.051 + 0.030 \cdot SL$
	$t_F$	0.111	$0.060 + 0.026 \cdot SL$	$0.060 + 0.026 \cdot SL$	$0.053 + 0.026 \cdot SL$
	$t_{PLH}$	0.464	$0.434 + 0.015 \cdot SL$	$0.439 + 0.013 \cdot SL$	$0.441 + 0.013 \cdot SL$
	$t_{PHL}$	0.546	$0.512 + 0.017 \cdot SL$	$0.520 + 0.015 \cdot SL$	$0.525 + 0.014 \cdot SL$
CK to QN	$t_R$	0.123	$0.067 + 0.028 \cdot SL$	$0.063 + 0.029 \cdot SL$	$0.055 + 0.030 \cdot SL$
	$t_F$	0.111	$0.059 + 0.026 \cdot SL$	$0.062 + 0.025 \cdot SL$	$0.056 + 0.026 \cdot SL$
	$t_{PLH}$	0.403	$0.372 + 0.015 \cdot SL$	$0.378 + 0.014 \cdot SL$	$0.381 + 0.013 \cdot SL$
	$t_{PHL}$	0.415	$0.381 + 0.017 \cdot SL$	$0.389 + 0.015 \cdot SL$	$0.395 + 0.014 \cdot SL$
SCK to QN	$t_R$	0.140	$0.085 + 0.028 \cdot SL$	$0.082 + 0.028 \cdot SL$	$0.070 + 0.030 \cdot SL$
	$t_F$	0.117	$0.066 + 0.025 \cdot SL$	$0.067 + 0.025 \cdot SL$	$0.061 + 0.026 \cdot SL$
	$t_{PLH}$	0.453	$0.421 + 0.016 \cdot SL$	$0.429 + 0.014 \cdot SL$	$0.434 + 0.013 \cdot SL$
	$t_{PHL}$	0.387	$0.353 + 0.017 \cdot SL$	$0.362 + 0.015 \cdot SL$	$0.370 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FDS3CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.101	$0.071 + 0.015 \cdot SL$	$0.073 + 0.014 \cdot SL$	$0.067 + 0.015 \cdot SL$
	$t_F$	0.094	$0.065 + 0.015 \cdot SL$	$0.070 + 0.013 \cdot SL$	$0.068 + 0.013 \cdot SL$
	$t_{PLH}$	0.543	$0.523 + 0.010 \cdot SL$	$0.531 + 0.008 \cdot SL$	$0.545 + 0.007 \cdot SL$
	$t_{PHL}$	0.547	$0.525 + 0.011 \cdot SL$	$0.534 + 0.009 \cdot SL$	$0.549 + 0.008 \cdot SL$
SCK to Q	$t_R$	0.090	$0.061 + 0.014 \cdot SL$	$0.061 + 0.014 \cdot SL$	$0.050 + 0.015 \cdot SL$
	$t_F$	0.086	$0.059 + 0.014 \cdot SL$	$0.061 + 0.013 \cdot SL$	$0.058 + 0.013 \cdot SL$
	$t_{PLH}$	0.499	$0.481 + 0.009 \cdot SL$	$0.487 + 0.007 \cdot SL$	$0.495 + 0.007 \cdot SL$
	$t_{PHL}$	0.584	$0.563 + 0.010 \cdot SL$	$0.571 + 0.008 \cdot SL$	$0.584 + 0.007 \cdot SL$
CK to QN	$t_R$	0.093	$0.065 + 0.014 \cdot SL$	$0.064 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.087	$0.059 + 0.014 \cdot SL$	$0.062 + 0.013 \cdot SL$	$0.058 + 0.013 \cdot SL$
	$t_{PLH}$	0.404	$0.385 + 0.009 \cdot SL$	$0.393 + 0.007 \cdot SL$	$0.401 + 0.007 \cdot SL$
	$t_{PHL}$	0.414	$0.393 + 0.011 \cdot SL$	$0.402 + 0.008 \cdot SL$	$0.414 + 0.007 \cdot SL$
SCK to QN	$t_R$	0.111	$0.084 + 0.014 \cdot SL$	$0.082 + 0.014 \cdot SL$	$0.072 + 0.015 \cdot SL$
	$t_F$	0.092	$0.065 + 0.014 \cdot SL$	$0.067 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	$t_{PLH}$	0.458	$0.438 + 0.010 \cdot SL$	$0.448 + 0.008 \cdot SL$	$0.459 + 0.007 \cdot SL$
	$t_{PHL}$	0.389	$0.367 + 0.011 \cdot SL$	$0.376 + 0.009 \cdot SL$	$0.390 + 0.007 \cdot SL$

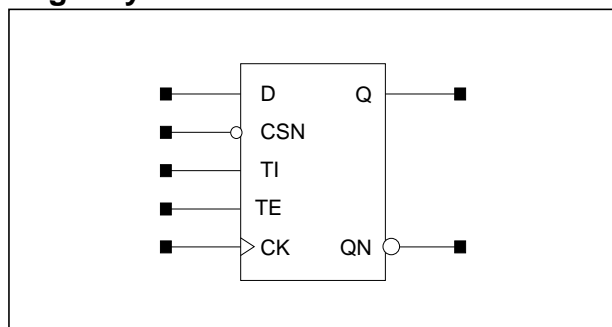
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FDS3S/FDS3SD2

### Flip-Flop with Synchronous Set, Scan, 1X/2X Drive

#### Logic Symbol



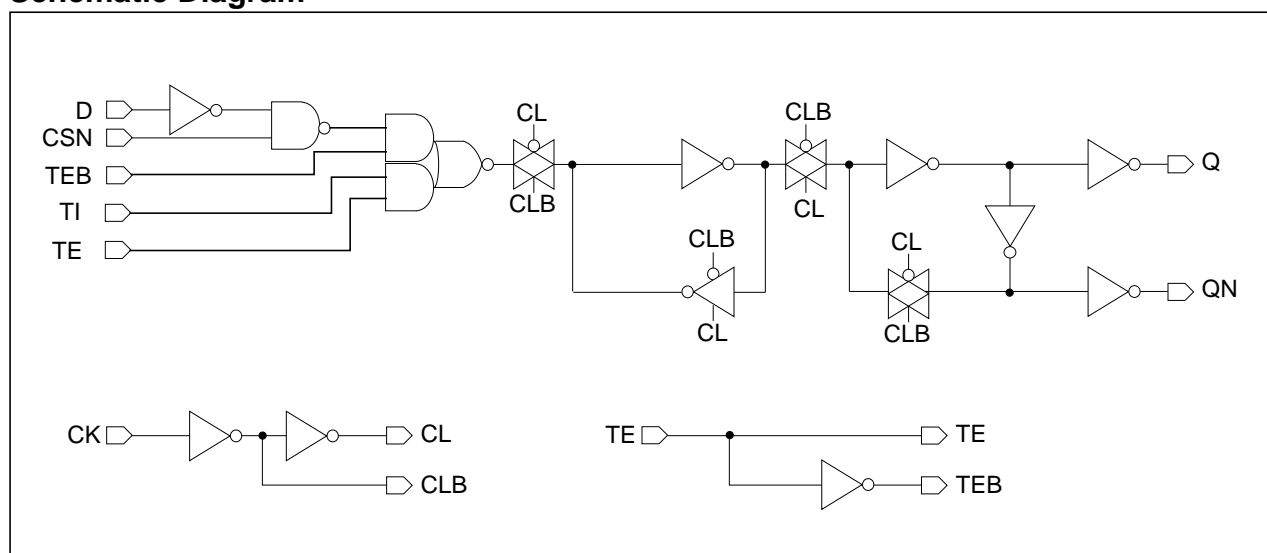
#### Truth Table

D	CSN	TI	TE	CK	Q(n+1)	QN(n+1)
0	1	x	0		0	1
1	1	x	0		1	0
x	x	0	1		0	1
x	x	1	1		1	0
x	0	x	0		1	0
x	x	x	x		Q(n)	QN(n+1)

#### Cell Data

Input Load (SL)										Gate Count	
FDS3S					FDS3SD2					FDS3S	FDS3SD2
D	CSN	CK	TI	TE	D	CSN	CK	TI	TE		
0.6	0.5	0.5	0.6	1.2	0.6	0.5	0.6	0.6	1.2	8.00	8.67

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS3S	FDS3SD2
Input Setup Time (D to CK)	$t_{SU}$	0.530	0.527
Input Hold Time (D to CK)	$t_{HD}$	0.000	0.000
Input Setup Time (CSN to CK)	$t_{SU}$	0.359	0.533
Input Hold Time (CSN to CK)	$t_{HD}$	0.002	0.000
Pulse Width Low (CK)	$t_{PWL}$	0.433	0.429
Pulse Width High (CK)	$t_{PWH}$	0.309	0.329
Input Setup Time (TI to CK)	$t_{SU}$	0.335	0.339
Input Hold Time (TI to CK)	$t_{HD}$	0.033	0.027
Input Setup Time (TE to CK)	$t_{SU}$	0.384	0.383
Input Hold Time (TE to CK)	$t_{HD}$	0.025	0.019



## Flip-Flop with Synchronous Set, Scan, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FDS3S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.126	$0.067 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$	$0.056 + 0.031 \cdot SL$
	$t_F$	0.115	$0.062 + 0.027 \cdot SL$	$0.062 + 0.027 \cdot SL$	$0.057 + 0.027 \cdot SL$
	$t_{PLH}$	0.391	$0.360 + 0.016 \cdot SL$	$0.366 + 0.014 \cdot SL$	$0.369 + 0.014 \cdot SL$
	$t_{PHL}$	0.413	$0.378 + 0.018 \cdot SL$	$0.387 + 0.015 \cdot SL$	$0.394 + 0.015 \cdot SL$
CK to QN	$t_R$	0.113	$0.056 + 0.028 \cdot SL$	$0.052 + 0.030 \cdot SL$	$0.047 + 0.030 \cdot SL$
	$t_F$	0.106	$0.054 + 0.026 \cdot SL$	$0.051 + 0.027 \cdot SL$	$0.046 + 0.027 \cdot SL$
	$t_{PLH}$	0.469	$0.440 + 0.014 \cdot SL$	$0.445 + 0.013 \cdot SL$	$0.445 + 0.013 \cdot SL$
	$t_{PHL}$	0.466	$0.433 + 0.016 \cdot SL$	$0.439 + 0.015 \cdot SL$	$0.442 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FDS3SD2

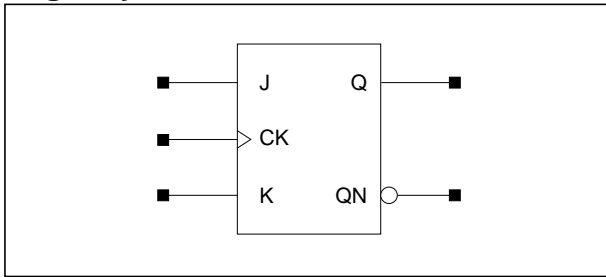
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.094	$0.065 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.087	$0.059 + 0.014 \cdot SL$	$0.062 + 0.013 \cdot SL$	$0.059 + 0.013 \cdot SL$
	$t_{PLH}$	0.393	$0.374 + 0.009 \cdot SL$	$0.381 + 0.007 \cdot SL$	$0.389 + 0.007 \cdot SL$
	$t_{PHL}$	0.408	$0.386 + 0.011 \cdot SL$	$0.395 + 0.008 \cdot SL$	$0.408 + 0.007 \cdot SL$
CK to QN	$t_R$	0.085	$0.057 + 0.014 \cdot SL$	$0.056 + 0.014 \cdot SL$	$0.045 + 0.015 \cdot SL$
	$t_F$	0.081	$0.053 + 0.014 \cdot SL$	$0.056 + 0.013 \cdot SL$	$0.050 + 0.014 \cdot SL$
	$t_{PLH}$	0.502	$0.484 + 0.009 \cdot SL$	$0.491 + 0.007 \cdot SL$	$0.497 + 0.007 \cdot SL$
	$t_{PHL}$	0.498	$0.478 + 0.010 \cdot SL$	$0.486 + 0.008 \cdot SL$	$0.496 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$








## JK Flip-Flop with 1X/2X Drive

## Logic Symbol



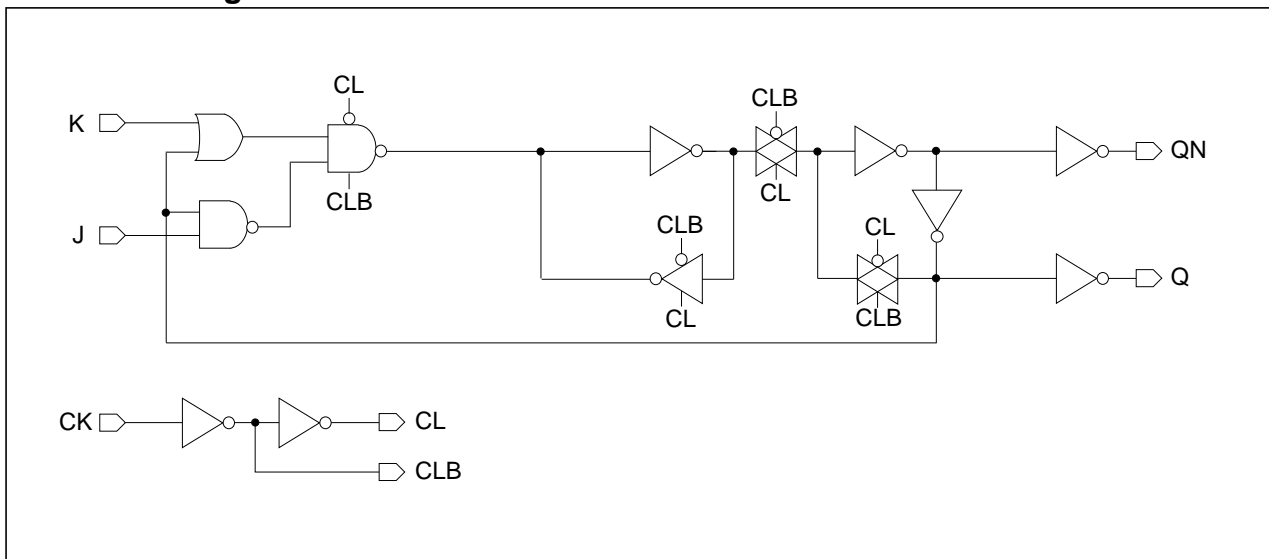
## Truth Table

J	CK	K	Q (n+1)	QN (n+1)
0		1	0	1
1		0	1	0
0		0	Q (n)	QN (n)
1		1	QN (n)	Q (n)
x		x	Q (n)	QN (n)

## Cell Data

Input Load (SL)						Gate Count	
FJ1			FJ1D2			FJ1	FJ1D2
J	K	CK	J	K	CK		
0.4	0.6	0.6	0.4	0.6	0.6	6.67	7.33

### Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ1	FJ1D2
Input Setup Time (J to CK)	$t_{SU}$	0.419	0.417
Input Hold Time (J to CK)	$t_{HD}$	0.083	0.089
Input Setup Time (K to CK)	$t_{SU}$	0.419	0.417
Input Hold Time (K to CK)	$t_{HD}$	0.083	0.089
Pulse Width Low (CK)	$t_{PWL}$	0.386	0.382
Pulse Width High (CK)	$t_{PWH}$	0.321	0.343



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FJ1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.122	$0.064 + 0.029 \cdot SL$	$0.060 + 0.030 \cdot SL$	$0.054 + 0.031 \cdot SL$
	$t_F$	0.114	$0.061 + 0.027 \cdot SL$	$0.061 + 0.027 \cdot SL$	$0.057 + 0.027 \cdot SL$
	$t_{PLH}$	0.514	$0.483 + 0.016 \cdot SL$	$0.490 + 0.014 \cdot SL$	$0.493 + 0.014 \cdot SL$
	$t_{PHL}$	0.501	$0.466 + 0.018 \cdot SL$	$0.475 + 0.015 \cdot SL$	$0.482 + 0.015 \cdot SL$
CK to QN	$t_R$	0.121	$0.064 + 0.028 \cdot SL$	$0.062 + 0.029 \cdot SL$	$0.054 + 0.030 \cdot SL$
	$t_F$	0.114	$0.061 + 0.027 \cdot SL$	$0.061 + 0.027 \cdot SL$	$0.057 + 0.027 \cdot SL$
	$t_{PLH}$	0.396	$0.366 + 0.015 \cdot SL$	$0.371 + 0.014 \cdot SL$	$0.374 + 0.013 \cdot SL$
	$t_{PHL}$	0.427	$0.392 + 0.017 \cdot SL$	$0.400 + 0.015 \cdot SL$	$0.407 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FJ1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.094	$0.065 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.056 + 0.015 \cdot SL$
	$t_F$	0.089	$0.061 + 0.014 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.063 + 0.013 \cdot SL$
	$t_{PLH}$	0.550	$0.531 + 0.009 \cdot SL$	$0.539 + 0.008 \cdot SL$	$0.548 + 0.007 \cdot SL$
	$t_{PHL}$	0.533	$0.511 + 0.011 \cdot SL$	$0.520 + 0.009 \cdot SL$	$0.534 + 0.007 \cdot SL$
CK to QN	$t_R$	0.094	$0.065 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.089	$0.061 + 0.014 \cdot SL$	$0.064 + 0.013 \cdot SL$	$0.062 + 0.013 \cdot SL$
	$t_{PLH}$	0.401	$0.382 + 0.009 \cdot SL$	$0.390 + 0.007 \cdot SL$	$0.397 + 0.007 \cdot SL$
	$t_{PHL}$	0.428	$0.407 + 0.011 \cdot SL$	$0.416 + 0.008 \cdot SL$	$0.428 + 0.008 \cdot SL$

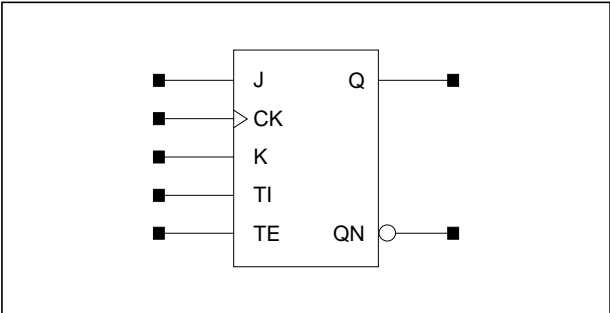
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# FJ1S/FJ1SD2

## JK Flip-Flop with Scan, 1X/2X Drive

Logic Symbol



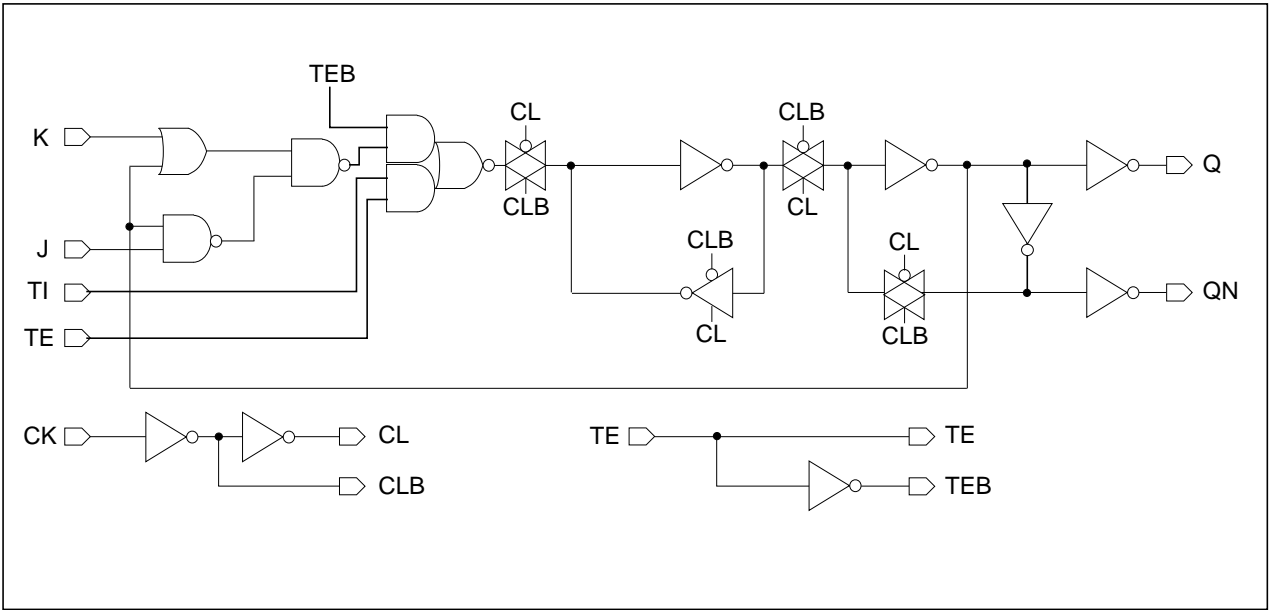
Truth Table

J	CK	K	TI	TE	Q (n+1)	QN (n+1)
0		1	x	0	0	1
1		0	x	0	1	0
0		0	x	0	Q (n)	QN (n)
1		1	x	0	QN (n)	Q (n)
x		x	x	x	Q (n)	QN (n)
x		x	0	1	0	1
x		x	1	1	1	0

Cell Data

Input Load (SL)										Gate Count	
FJ1S					FJ1SD2					FJ1S	FJ1SD2
J	K	CK	TI	TE	J	K	CK	TI	TE		
0.5	0.5	0.5	0.5	1.2	0.5	0.5	0.5	0.5	1.2	8.67	9.33

Schematic Diagram





# FJ1S/FJ1SD2

## JK Flip-Flop with Scan, 1X/2X Drive

### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ1S	FJ1SD2
Input Setup Time (J to CK)	$t_{SU}$	0.605	0.602
Input Hold Time (J to CK)	$t_{HD}$	0.000	0.000
Input Setup Time (K to CK)	$t_{SU}$	0.605	0.602
Input Hold Time (K to CK)	$t_{HD}$	0.000	0.000
Pulse Width Low (CK)	$t_{PWL}$	0.428	0.428
Pulse Width High (CK)	$t_{PWH}$	0.327	0.350
Input Setup Time (TI to CK)	$t_{SU}$	0.338	0.337
Input Hold Time (TI to CK)	$t_{HD}$	0.035	0.035
Input Setup Time (TE to CK)	$t_{SU}$	0.316	0.315
Input Hold Time (TE to CK)	$t_{HD}$	0.029	0.029

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FJ1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.135	$0.077 + 0.029 \cdot SL$	$0.074 + 0.030 \cdot SL$	$0.065 + 0.031 \cdot SL$
	$t_F$	0.123	$0.069 + 0.027 \cdot SL$	$0.073 + 0.026 \cdot SL$	$0.069 + 0.027 \cdot SL$
	$t_{PLH}$	0.426	$0.393 + 0.017 \cdot SL$	$0.401 + 0.015 \cdot SL$	$0.406 + 0.014 \cdot SL$
	$t_{PHL}$	0.446	$0.409 + 0.018 \cdot SL$	$0.420 + 0.016 \cdot SL$	$0.430 + 0.015 \cdot SL$
CK to QN	$t_R$	0.114	$0.057 + 0.028 \cdot SL$	$0.052 + 0.030 \cdot SL$	$0.047 + 0.030 \cdot SL$
	$t_F$	0.102	$0.052 + 0.025 \cdot SL$	$0.050 + 0.026 \cdot SL$	$0.047 + 0.026 \cdot SL$
	$t_{PLH}$	0.505	$0.477 + 0.014 \cdot SL$	$0.481 + 0.013 \cdot SL$	$0.482 + 0.013 \cdot SL$
	$t_{PHL}$	0.498	$0.467 + 0.016 \cdot SL$	$0.473 + 0.014 \cdot SL$	$0.477 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

#### FJ1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.103	$0.074 + 0.015 \cdot SL$	$0.075 + 0.014 \cdot SL$	$0.068 + 0.015 \cdot SL$
	$t_F$	0.096	$0.069 + 0.014 \cdot SL$	$0.073 + 0.013 \cdot SL$	$0.075 + 0.013 \cdot SL$
	$t_{PLH}$	0.427	$0.407 + 0.010 \cdot SL$	$0.416 + 0.008 \cdot SL$	$0.427 + 0.007 \cdot SL$
	$t_{PHL}$	0.443	$0.421 + 0.011 \cdot SL$	$0.431 + 0.009 \cdot SL$	$0.448 + 0.007 \cdot SL$
CK to QN	$t_R$	0.088	$0.060 + 0.014 \cdot SL$	$0.059 + 0.014 \cdot SL$	$0.048 + 0.015 \cdot SL$
	$t_F$	0.080	$0.054 + 0.013 \cdot SL$	$0.056 + 0.012 \cdot SL$	$0.051 + 0.013 \cdot SL$
	$t_{PLH}$	0.545	$0.528 + 0.009 \cdot SL$	$0.534 + 0.007 \cdot SL$	$0.540 + 0.007 \cdot SL$
	$t_{PHL}$	0.533	$0.514 + 0.010 \cdot SL$	$0.522 + 0.008 \cdot SL$	$0.532 + 0.007 \cdot SL$

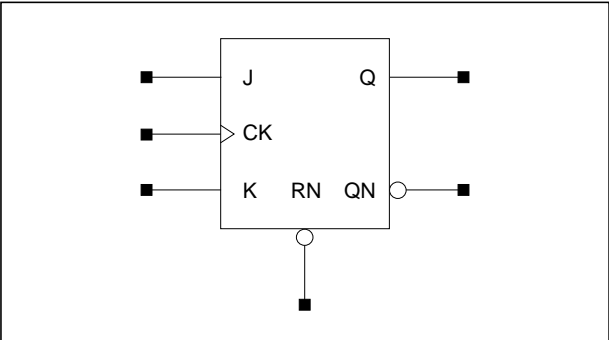
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



FJ2/FJ2D2

JK Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



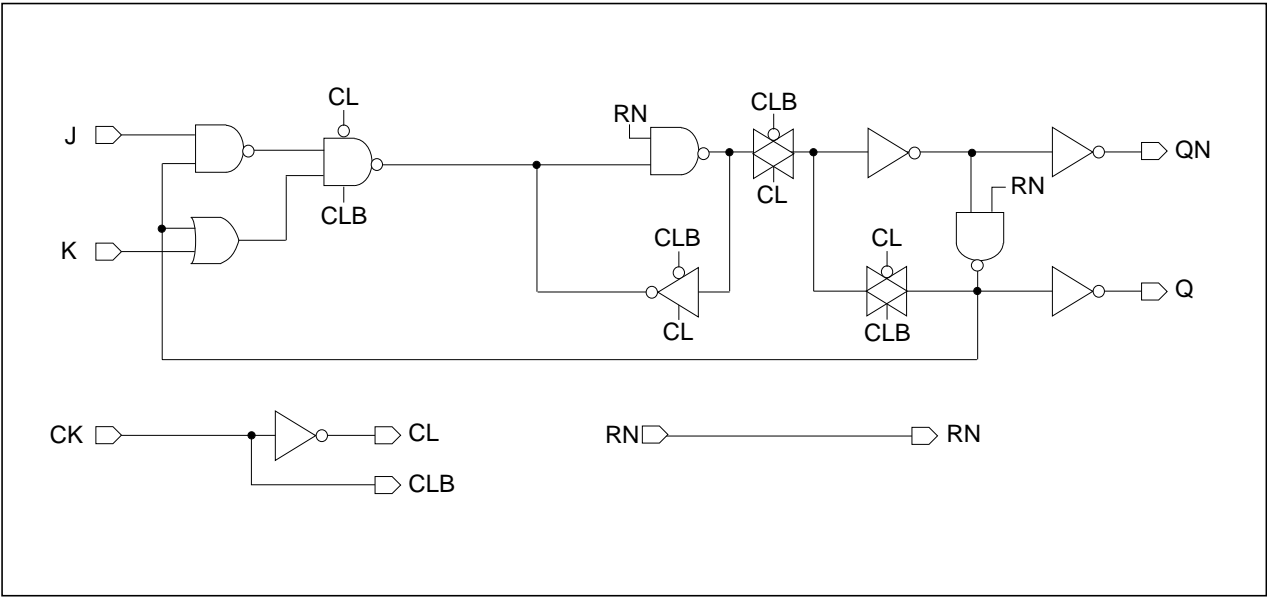
Truth Table

J	CK	K	RN	Q (n+1)	QN (n+1)
0		1	1	0	1
1		0	1	1	0
0		0	1	Q (n)	QN (n)
1		1	1	QN (n)	Q (n)
x		x	1	Q (n)	QN (n)
x	x	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
FJ2				FJ2D2				FJ2	FJ2D2
J	K	CK	RN	J	K	CK	RN		
0.4	0.5	0.6	1.5	0.4	0.5	0.6	1.5	8.00	8.33

Schematic Diagram





## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ2	FJ2D2
Input Setup Time (J to CK)	$t_{SU}$	0.286	0.286
Input Hold Time (J to CK)	$t_{HD}$	0.045	0.045
Input Setup Time (K to CK)	$t_{SU}$	0.286	0.286
Input Hold Time (K to CK)	$t_{HD}$	0.045	0.045
Pulse Width Low (CK)	$t_{PWL}$	0.423	0.424
Pulse Width High (CK)	$t_{PWH}$	0.323	0.344
Pulse Width Low (RN)	$t_{PWL}$	0.296	0.328
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.253	0.253

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FJ2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.136	$0.076 + 0.030 \cdot SL$	$0.077 + 0.030 \cdot SL$	$0.071 + 0.031 \cdot SL$
	$t_F$	0.114	$0.064 + 0.025 \cdot SL$	$0.064 + 0.025 \cdot SL$	$0.061 + 0.026 \cdot SL$
	$t_{PLH}$	0.569	$0.534 + 0.017 \cdot SL$	$0.544 + 0.015 \cdot SL$	$0.552 + 0.014 \cdot SL$
	$t_{PHL}$	0.508	$0.473 + 0.017 \cdot SL$	$0.483 + 0.015 \cdot SL$	$0.491 + 0.014 \cdot SL$
RN to Q	$t_F$	0.133	$0.080 + 0.026 \cdot SL$	$0.087 + 0.025 \cdot SL$	$0.083 + 0.025 \cdot SL$
	$t_{PHL}$	0.239	$0.201 + 0.019 \cdot SL$	$0.214 + 0.016 \cdot SL$	$0.227 + 0.014 \cdot SL$
CK to QN	$t_R$	0.125	$0.068 + 0.029 \cdot SL$	$0.064 + 0.030 \cdot SL$	$0.056 + 0.031 \cdot SL$
	$t_F$	0.115	$0.066 + 0.025 \cdot SL$	$0.063 + 0.025 \cdot SL$	$0.061 + 0.026 \cdot SL$
	$t_{PLH}$	0.396	$0.365 + 0.015 \cdot SL$	$0.371 + 0.014 \cdot SL$	$0.373 + 0.014 \cdot SL$
	$t_{PHL}$	0.444	$0.410 + 0.017 \cdot SL$	$0.418 + 0.015 \cdot SL$	$0.424 + 0.014 \cdot SL$
RN to QN	$t_R$	0.129	$0.073 + 0.028 \cdot SL$	$0.067 + 0.029 \cdot SL$	$0.059 + 0.030 \cdot SL$
	$t_{PLH}$	0.393	$0.362 + 0.015 \cdot SL$	$0.369 + 0.014 \cdot SL$	$0.371 + 0.013 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FJ2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.109	$0.078 + 0.015 \cdot SL$	$0.081 + 0.015 \cdot SL$	$0.078 + 0.015 \cdot SL$
	$t_F$	0.093	$0.063 + 0.015 \cdot SL$	$0.070 + 0.013 \cdot SL$	$0.069 + 0.013 \cdot SL$
	$t_{PLH}$	0.606	$0.584 + 0.011 \cdot SL$	$0.594 + 0.008 \cdot SL$	$0.609 + 0.007 \cdot SL$
	$t_{PHL}$	0.541	$0.519 + 0.011 \cdot SL$	$0.529 + 0.009 \cdot SL$	$0.545 + 0.008 \cdot SL$
RN to Q	$t_F$	0.111	$0.081 + 0.015 \cdot SL$	$0.089 + 0.013 \cdot SL$	$0.088 + 0.013 \cdot SL$
	$t_{PHL}$	0.235	$0.210 + 0.012 \cdot SL$	$0.223 + 0.009 \cdot SL$	$0.244 + 0.008 \cdot SL$
CK to QN	$t_R$	0.094	$0.067 + 0.014 \cdot SL$	$0.063 + 0.014 \cdot SL$	$0.055 + 0.015 \cdot SL$
	$t_F$	0.092	$0.065 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$	$0.062 + 0.013 \cdot SL$
	$t_{PLH}$	0.397	$0.378 + 0.009 \cdot SL$	$0.386 + 0.007 \cdot SL$	$0.394 + 0.007 \cdot SL$
	$t_{PHL}$	0.448	$0.426 + 0.011 \cdot SL$	$0.435 + 0.008 \cdot SL$	$0.448 + 0.008 \cdot SL$
RN to QN	$t_R$	0.101	$0.074 + 0.013 \cdot SL$	$0.071 + 0.014 \cdot SL$	$0.060 + 0.015 \cdot SL$
	$t_{PLH}$	0.423	$0.404 + 0.009 \cdot SL$	$0.412 + 0.007 \cdot SL$	$0.422 + 0.007 \cdot SL$

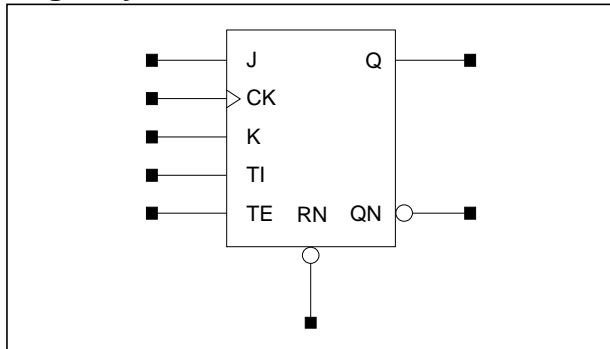
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## FJ2S/FJ2SD2

### JK Flip-Flop with Reset, Scan, 1X/2X Drive

#### Logic Symbol



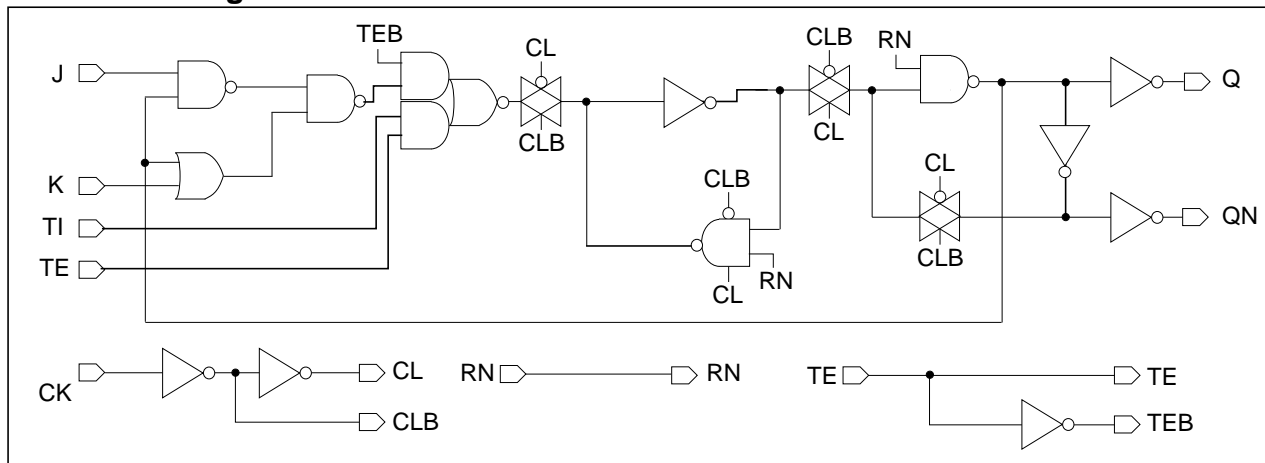
#### Truth Table

J	CK	K	TI	TE	RN	Q (n+1)	QN (n+1)
0		1	x	0	1	0	1
1		0	x	0	1	1	0
0		0	x	0	1	Q (n)	QN (n)
1		1	x	0	1	QN (n)	Q (n)
x		x	x	x	1	Q (n)	QN (n)
x	x	x	x	x	0	0	1
x		x	0	1	1	0	1
x		x	1	1	1	1	0

#### Cell Data

Input Load (SL)												Gate Count	
FJ2S						FJ2SD2						FJ2S	FJ2SD2
J	K	CK	RN	TI	TE	J	K	CK	RN	TI	TE		
0.5	0.5	0.6	1.6	0.5	1.2	0.5	0.5	0.6	1.5	0.5	1.2	9.67	10.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ2S	FJ2SD2
Input Setup Time (J to CK)	t <sub>SU</sub>	0.601	0.603
Input Hold Time (J to CK)	t <sub>HD</sub>	0.000	0.000
Input Setup Time (K to CK)	t <sub>SU</sub>	0.601	0.603
Input Hold Time (K to CK)	t <sub>HD</sub>	0.000	0.000
Pulse Width Low (CK)	t <sub>PWL</sub>	0.487	0.481
Pulse Width High (CK)	t <sub>PWH</sub>	0.368	0.404
Pulse Width Low (RN)	t <sub>PWL</sub>	0.279	0.315
Recovery Time (RN to CK)	t <sub>RC</sub>	0.000	0.000
Removal Time (RN to CK)	t <sub>RM</sub>	0.770	0.763
Input Setup Time (TI to CK)	t <sub>SU</sub>	0.355	0.495
Input Hold Time (TI to CK)	t <sub>HD</sub>	0.122	0.135
Input Setup Time (TE to CK)	t <sub>SU</sub>	0.393	0.515
Input Hold Time (TE to CK)	t <sub>HD</sub>	0.110	0.124



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FJ2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.150	$0.090 + 0.030 \cdot SL$	$0.092 + 0.030 \cdot SL$	$0.086 + 0.031 \cdot SL$
	$t_F$	0.122	$0.069 + 0.026 \cdot SL$	$0.076 + 0.025 \cdot SL$	$0.070 + 0.025 \cdot SL$
	$t_{PLH}$	0.485	$0.448 + 0.018 \cdot SL$	$0.459 + 0.016 \cdot SL$	$0.470 + 0.014 \cdot SL$
	$t_{PHL}$	0.473	$0.437 + 0.018 \cdot SL$	$0.448 + 0.015 \cdot SL$	$0.458 + 0.014 \cdot SL$
RN to Q	$t_F$	0.124	$0.073 + 0.025 \cdot SL$	$0.077 + 0.024 \cdot SL$	$0.072 + 0.025 \cdot SL$
	$t_{PHL}$	0.220	$0.184 + 0.018 \cdot SL$	$0.195 + 0.015 \cdot SL$	$0.206 + 0.014 \cdot SL$
CK to QN	$t_R$	0.116	$0.059 + 0.028 \cdot SL$	$0.055 + 0.030 \cdot SL$	$0.049 + 0.030 \cdot SL$
	$t_F$	0.108	$0.060 + 0.024 \cdot SL$	$0.055 + 0.025 \cdot SL$	$0.051 + 0.026 \cdot SL$
	$t_{PLH}$	0.537	$0.508 + 0.014 \cdot SL$	$0.513 + 0.013 \cdot SL$	$0.514 + 0.013 \cdot SL$
	$t_{PHL}$	0.565	$0.533 + 0.016 \cdot SL$	$0.540 + 0.014 \cdot SL$	$0.544 + 0.014 \cdot SL$
RN to QN	$t_R$	0.133	$0.074 + 0.029 \cdot SL$	$0.075 + 0.029 \cdot SL$	$0.071 + 0.030 \cdot SL$
	$t_{PLH}$	0.330	$0.297 + 0.016 \cdot SL$	$0.305 + 0.014 \cdot SL$	$0.313 + 0.013 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## FJ2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.122	$0.092 + 0.015 \cdot SL$	$0.092 + 0.015 \cdot SL$	$0.092 + 0.015 \cdot SL$
	$t_F$	0.100	$0.071 + 0.014 \cdot SL$	$0.076 + 0.013 \cdot SL$	$0.078 + 0.013 \cdot SL$
	$t_{PLH}$	0.496	$0.473 + 0.011 \cdot SL$	$0.484 + 0.009 \cdot SL$	$0.502 + 0.007 \cdot SL$
	$t_{PHL}$	0.482	$0.459 + 0.012 \cdot SL$	$0.469 + 0.009 \cdot SL$	$0.487 + 0.008 \cdot SL$
RN to Q	$t_F$	0.102	$0.073 + 0.015 \cdot SL$	$0.079 + 0.013 \cdot SL$	$0.077 + 0.013 \cdot SL$
	$t_{PHL}$	0.218	$0.195 + 0.012 \cdot SL$	$0.206 + 0.009 \cdot SL$	$0.225 + 0.008 \cdot SL$
CK to QN	$t_R$	0.090	$0.061 + 0.014 \cdot SL$	$0.061 + 0.014 \cdot SL$	$0.049 + 0.015 \cdot SL$
	$t_F$	0.087	$0.060 + 0.014 \cdot SL$	$0.063 + 0.013 \cdot SL$	$0.057 + 0.013 \cdot SL$
	$t_{PLH}$	0.582	$0.565 + 0.009 \cdot SL$	$0.571 + 0.007 \cdot SL$	$0.578 + 0.007 \cdot SL$
	$t_{PHL}$	0.621	$0.600 + 0.010 \cdot SL$	$0.608 + 0.008 \cdot SL$	$0.619 + 0.007 \cdot SL$
RN to QN	$t_R$	0.104	$0.074 + 0.015 \cdot SL$	$0.075 + 0.015 \cdot SL$	$0.069 + 0.015 \cdot SL$
	$t_{PLH}$	0.363	$0.343 + 0.010 \cdot SL$	$0.351 + 0.008 \cdot SL$	$0.364 + 0.007 \cdot SL$

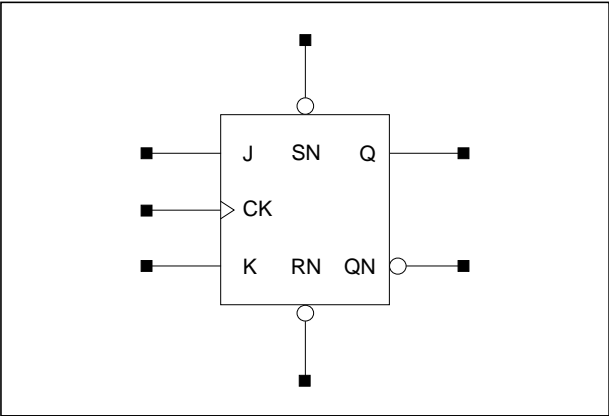
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



FJ4/FJ4D2

JK Flip-Flop with Reset, Set, 1X/2X Drive

Logic Symbol5



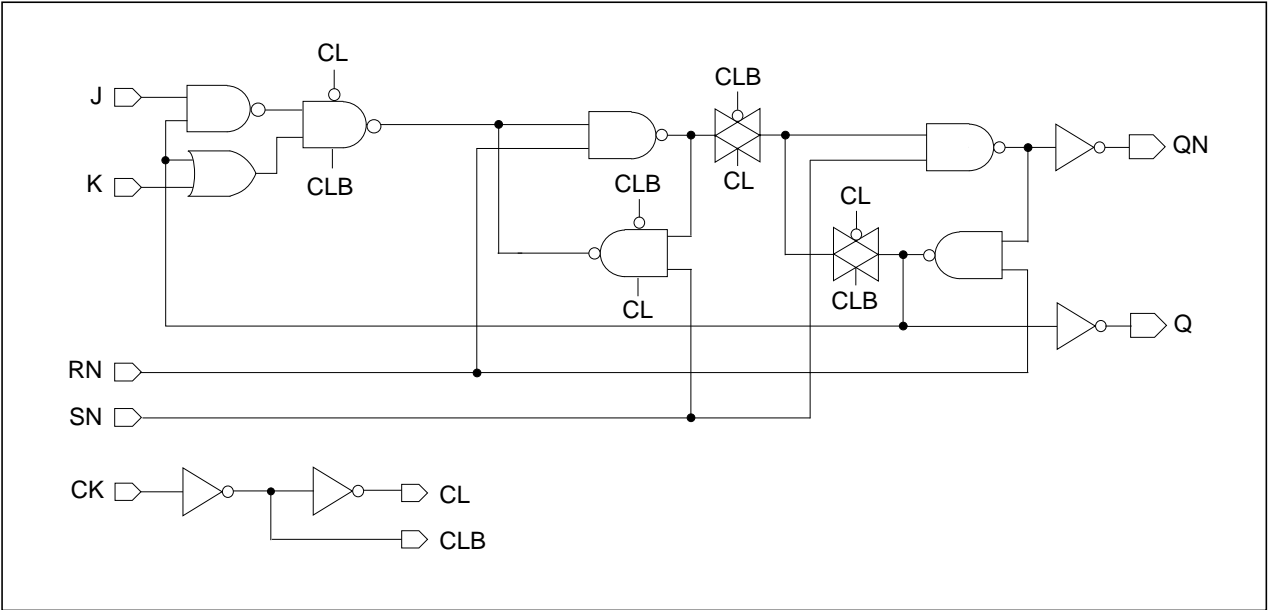
Truth Table

J	CK	K	RN	SN	Q (n+1)	QN (n+1)
0		1	1	1	0	1
1		0	1	1	1	0
0		0	1	1	Q (n)	QN (n)
1		1	1	1	QN (n)	Q (n)
x		x	1	1	Q (n)	QN (n)
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

Cell Data

Input Load (SL)										Gate Count	
FJ4					FJ4D2					FJ4	FJ4D2
J	K	CK	RN	SN	J	K	CK	RN	SN		
0.4	0.6	0.6	1.6	1.5	0.4	0.6	0.6	1.6	1.5	8.33	8.67

Schematic Diagram





## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ4	FJ4D2
Input Setup Time (J to CK)	$t_{SU}$	0.439	0.441
Input Hold Time (J to CK)	$t_{HD}$	0.066	0.067
Input Setup Time (K to CK)	$t_{SU}$	0.439	0.441
Input Hold Time (K to CK)	$t_{HD}$	0.066	0.067
Pulse Width Low (CK)	$t_{PWL}$	0.451	0.452
Pulse Width High (CK)	$t_{PWH}$	0.348	0.377
Pulse Width Low (RN)	$t_{PWL}$	0.313	0.352
Pulse Width Low (SN)	$t_{PWL}$	0.299	0.337
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.304	0.302
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.861	0.862
Recovery Time (SN to RN)	$t_{RC}$	0.004	0.003
Removal Time (SN to RN)	$t_{RM}$	0.216	0.217

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FJ4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.140	$0.082 + 0.029 \cdot SL$	$0.081 + 0.029 \cdot SL$	$0.076 + 0.030 \cdot SL$
	$t_F$	0.123	$0.069 + 0.027 \cdot SL$	$0.071 + 0.026 \cdot SL$	$0.067 + 0.027 \cdot SL$
	$t_{PLH}$	0.584	$0.549 + 0.018 \cdot SL$	$0.560 + 0.015 \cdot SL$	$0.569 + 0.014 \cdot SL$
	$t_{PHL}$	0.566	$0.529 + 0.018 \cdot SL$	$0.540 + 0.016 \cdot SL$	$0.549 + 0.015 \cdot SL$
RN to Q	$t_R$	0.160	$0.099 + 0.031 \cdot SL$	$0.104 + 0.029 \cdot SL$	$0.102 + 0.030 \cdot SL$
	$t_F$	0.139	$0.085 + 0.027 \cdot SL$	$0.088 + 0.026 \cdot SL$	$0.085 + 0.027 \cdot SL$
	$t_{PLH}$	0.240	$0.201 + 0.020 \cdot SL$	$0.215 + 0.016 \cdot SL$	$0.230 + 0.014 \cdot SL$
	$t_{PHL}$	0.249	$0.209 + 0.020 \cdot SL$	$0.222 + 0.017 \cdot SL$	$0.236 + 0.015 \cdot SL$
SN to Q	$t_R$	0.162	$0.101 + 0.031 \cdot SL$	$0.106 + 0.029 \cdot SL$	$0.104 + 0.029 \cdot SL$
	$t_{PLH}$	0.371	$0.332 + 0.020 \cdot SL$	$0.346 + 0.016 \cdot SL$	$0.362 + 0.014 \cdot SL$
CK to QN	$t_R$	0.137	$0.079 + 0.029 \cdot SL$	$0.076 + 0.030 \cdot SL$	$0.070 + 0.030 \cdot SL$
	$t_F$	0.116	$0.067 + 0.025 \cdot SL$	$0.065 + 0.025 \cdot SL$	$0.060 + 0.026 \cdot SL$
	$t_{PLH}$	0.441	$0.408 + 0.017 \cdot SL$	$0.416 + 0.015 \cdot SL$	$0.423 + 0.014 \cdot SL$
	$t_{PHL}$	0.450	$0.416 + 0.017 \cdot SL$	$0.425 + 0.015 \cdot SL$	$0.430 + 0.014 \cdot SL$
RN to QN	$t_R$	0.140	$0.084 + 0.028 \cdot SL$	$0.080 + 0.029 \cdot SL$	$0.072 + 0.030 \cdot SL$
	$t_{PLH}$	0.429	$0.395 + 0.017 \cdot SL$	$0.404 + 0.014 \cdot SL$	$0.411 + 0.014 \cdot SL$
SN to QN	$t_R$	0.131	$0.073 + 0.029 \cdot SL$	$0.070 + 0.030 \cdot SL$	$0.065 + 0.030 \cdot SL$
	$t_F$	0.114	$0.063 + 0.025 \cdot SL$	$0.063 + 0.025 \cdot SL$	$0.059 + 0.026 \cdot SL$
	$t_{PLH}$	0.177	$0.144 + 0.016 \cdot SL$	$0.153 + 0.014 \cdot SL$	$0.159 + 0.014 \cdot SL$
	$t_{PHL}$	0.195	$0.161 + 0.017 \cdot SL$	$0.170 + 0.015 \cdot SL$	$0.175 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## FJ4/FJ4D2

### JK Flip-Flop with Reset, Set, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FJ4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.113	$0.083 + 0.015 \cdot SL$	$0.084 + 0.015 \cdot SL$	$0.083 + 0.015 \cdot SL$
	$t_F$	0.099	$0.069 + 0.015 \cdot SL$	$0.076 + 0.013 \cdot SL$	$0.073 + 0.013 \cdot SL$
	$t_{PLH}$	0.628	$0.607 + 0.011 \cdot SL$	$0.617 + 0.008 \cdot SL$	$0.633 + 0.007 \cdot SL$
	$t_{PHL}$	0.607	$0.585 + 0.011 \cdot SL$	$0.595 + 0.009 \cdot SL$	$0.611 + 0.008 \cdot SL$
RN to Q	$t_R$	0.130	$0.098 + 0.016 \cdot SL$	$0.100 + 0.015 \cdot SL$	$0.107 + 0.015 \cdot SL$
	$t_F$	0.113	$0.084 + 0.015 \cdot SL$	$0.089 + 0.013 \cdot SL$	$0.092 + 0.013 \cdot SL$
	$t_{PLH}$	0.238	$0.214 + 0.012 \cdot SL$	$0.227 + 0.009 \cdot SL$	$0.249 + 0.008 \cdot SL$
	$t_{PHL}$	0.241	$0.216 + 0.013 \cdot SL$	$0.229 + 0.010 \cdot SL$	$0.250 + 0.008 \cdot SL$
SN to Q	$t_R$	0.134	$0.102 + 0.016 \cdot SL$	$0.105 + 0.015 \cdot SL$	$0.108 + 0.015 \cdot SL$
	$t_{PLH}$	0.406	$0.381 + 0.013 \cdot SL$	$0.394 + 0.009 \cdot SL$	$0.416 + 0.008 \cdot SL$
CK to QN	$t_R$	0.109	$0.080 + 0.015 \cdot SL$	$0.081 + 0.014 \cdot SL$	$0.077 + 0.015 \cdot SL$
	$t_F$	0.096	$0.067 + 0.014 \cdot SL$	$0.072 + 0.013 \cdot SL$	$0.068 + 0.013 \cdot SL$
	$t_{PLH}$	0.448	$0.428 + 0.010 \cdot SL$	$0.437 + 0.008 \cdot SL$	$0.451 + 0.007 \cdot SL$
	$t_{PHL}$	0.459	$0.438 + 0.011 \cdot SL$	$0.447 + 0.009 \cdot SL$	$0.460 + 0.008 \cdot SL$
RN to QN	$t_R$	0.114	$0.087 + 0.014 \cdot SL$	$0.085 + 0.014 \cdot SL$	$0.081 + 0.015 \cdot SL$
	$t_{PLH}$	0.468	$0.448 + 0.010 \cdot SL$	$0.457 + 0.008 \cdot SL$	$0.471 + 0.007 \cdot SL$
SN to QN	$t_R$	0.101	$0.071 + 0.015 \cdot SL$	$0.073 + 0.015 \cdot SL$	$0.070 + 0.015 \cdot SL$
	$t_F$	0.092	$0.063 + 0.015 \cdot SL$	$0.070 + 0.013 \cdot SL$	$0.065 + 0.013 \cdot SL$
	$t_{PLH}$	0.181	$0.161 + 0.010 \cdot SL$	$0.169 + 0.008 \cdot SL$	$0.183 + 0.007 \cdot SL$
	$t_{PHL}$	0.195	$0.174 + 0.011 \cdot SL$	$0.183 + 0.009 \cdot SL$	$0.196 + 0.008 \cdot SL$

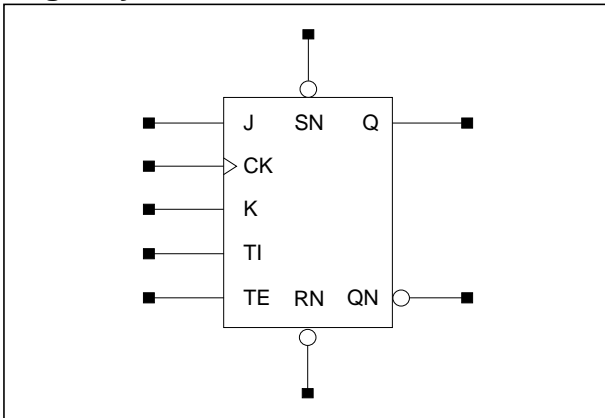
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# FJ4S/FJ4SD2

## JK Flip-Flop with Reset, Set, Scan, 1X/2X Drive

### Logic Symbol



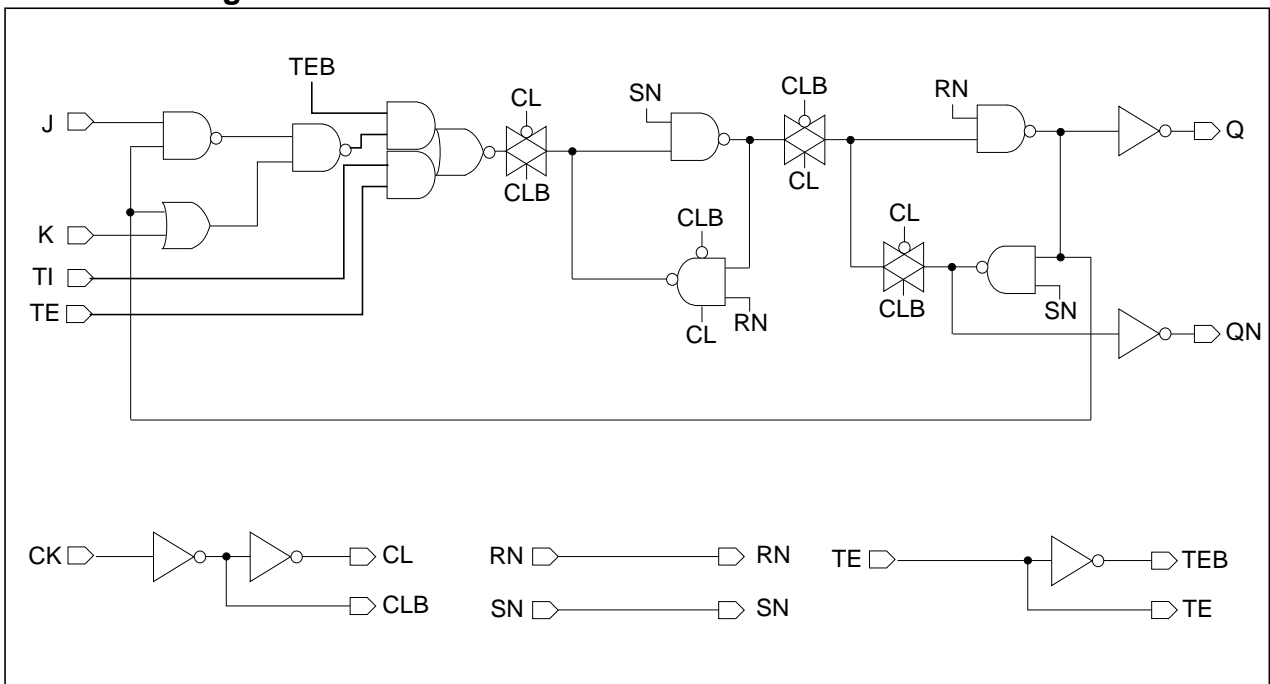
### Truth Table

J	CK	K	TI	TE	RN	SN	Q (n+1)	QN (n+1)
0		1	x	0	1	1	0	1
1		0	x	0	1	1	1	0
0		0	x	0	1	1	Q (n)	QN (n)
1		1	x	0	1	1	QN (n)	Q (n)
x		x	x	x	1	1	Q (n)	QN (n)
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0
x		x	0	1	1	1	0	1
x		x	1	1	1	1	1	0

### Cell Data

Input Load (SL)														Gate Count	
FJ4S							FJ4SD2							FJ4S	FJ4SD2
J	K	CK	RN	SN	TI	TE	J	K	CK	RN	SN	TI	TE		
0.5	0.5	0.6	1.6	1.6	0.6	1.2	0.5	0.5	0.6	1.6	1.6	0.6	1.2	10.67	11.00

### Schematic Diagram





## FJ4S/FJ4SD2

### JK Flip-Flop with Reset, Set, Scan, 1X/2X Drive

#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ4S	FJ4SD2
Input Setup Time (J to CK)	$t_{SU}$	0.611	0.603
Input Hold Time (J to CK)	$t_{HD}$	0.000	0.000
Input Setup Time (K to CK)	$t_{SU}$	0.611	0.603
Input Hold Time (K to CK)	$t_{HD}$	0.000	0.000
Pulse Width Low (CK)	$t_{PWL}$	0.511	0.511
Pulse Width High (CK)	$t_{PWH}$	0.380	0.407
Pulse Width Low(RN)	$t_{PWL}$	0.309	0.348
Pulse Width Low (SN)	$t_{PWL}$	0.319	0.355
Recovery Time (RN to CK)	$t_{RC}$	0.000	0.000
Removal Time (RN to CK)	$t_{RM}$	0.812	0.812
Recovery Time (SN to CK)	$t_{RC}$	0.000	0.000
Removal Time (SN to CK)	$t_{RM}$	0.315	0.315
Input Setup Time (TI to CK)	$t_{SU}$	0.385	0.385
Input Hold Time (TI to CK)	$t_{HD}$	0.087	0.087
Input Setup Time (TE to CK)	$t_{SU}$	0.396	0.396
Input Hold Time (TE to CK)	$t_{HD}$	0.075	0.075
Recovery Time (SN to RN)	$t_{RC}$	0.223	0.224
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### FJ4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.150	$0.091 + 0.029 \cdot SL$	$0.095 + 0.028 \cdot SL$	$0.088 + 0.029 \cdot SL$
	$t_F$	0.127	$0.075 + 0.026 \cdot SL$	$0.079 + 0.025 \cdot SL$	$0.076 + 0.025 \cdot SL$
	$t_{PLH}$	0.498	$0.463 + 0.018 \cdot SL$	$0.474 + 0.015 \cdot SL$	$0.485 + 0.014 \cdot SL$
	$t_{PHL}$	0.491	$0.455 + 0.018 \cdot SL$	$0.466 + 0.016 \cdot SL$	$0.476 + 0.014 \cdot SL$
RN to Q	$t_R$	0.139	$0.081 + 0.029 \cdot SL$	$0.082 + 0.029 \cdot SL$	$0.076 + 0.029 \cdot SL$
	$t_F$	0.126	$0.074 + 0.026 \cdot SL$	$0.079 + 0.025 \cdot SL$	$0.074 + 0.025 \cdot SL$
	$t_{PLH}$	0.206	$0.172 + 0.017 \cdot SL$	$0.182 + 0.015 \cdot SL$	$0.192 + 0.014 \cdot SL$
	$t_{PHL}$	0.223	$0.187 + 0.018 \cdot SL$	$0.198 + 0.015 \cdot SL$	$0.208 + 0.014 \cdot SL$
SN to Q	$t_R$	0.146	$0.089 + 0.029 \cdot SL$	$0.090 + 0.028 \cdot SL$	$0.084 + 0.029 \cdot SL$
	$t_{PLH}$	0.445	$0.410 + 0.017 \cdot SL$	$0.421 + 0.015 \cdot SL$	$0.431 + 0.014 \cdot SL$
CK to QN	$t_R$	0.130	$0.072 + 0.029 \cdot SL$	$0.070 + 0.029 \cdot SL$	$0.064 + 0.030 \cdot SL$
	$t_F$	0.112	$0.062 + 0.025 \cdot SL$	$0.061 + 0.025 \cdot SL$	$0.057 + 0.026 \cdot SL$
	$t_{PLH}$	0.594	$0.561 + 0.016 \cdot SL$	$0.569 + 0.014 \cdot SL$	$0.575 + 0.013 \cdot SL$
	$t_{PHL}$	0.596	$0.563 + 0.017 \cdot SL$	$0.571 + 0.015 \cdot SL$	$0.577 + 0.014 \cdot SL$
RN to QN	$t_R$	0.157	$0.096 + 0.031 \cdot SL$	$0.101 + 0.029 \cdot SL$	$0.099 + 0.030 \cdot SL$
	$t_{PLH}$	0.373	$0.334 + 0.019 \cdot SL$	$0.347 + 0.016 \cdot SL$	$0.362 + 0.014 \cdot SL$
SN to QN	$t_R$	0.151	$0.088 + 0.032 \cdot SL$	$0.096 + 0.030 \cdot SL$	$0.097 + 0.030 \cdot SL$
	$t_F$	0.127	$0.074 + 0.026 \cdot SL$	$0.077 + 0.026 \cdot SL$	$0.077 + 0.026 \cdot SL$
	$t_{PLH}$	0.204	$0.167 + 0.019 \cdot SL$	$0.178 + 0.016 \cdot SL$	$0.193 + 0.014 \cdot SL$
	$t_{PHL}$	0.220	$0.183 + 0.018 \cdot SL$	$0.193 + 0.016 \cdot SL$	$0.204 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## JK Flip-Flop with Reset, Set, Scan, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FJ4SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	$t_R$	0.122	$0.092 + 0.015 \cdot SL$	$0.092 + 0.015 \cdot SL$	$0.093 + 0.015 \cdot SL$
	$t_F$	0.104	$0.076 + 0.014 \cdot SL$	$0.080 + 0.013 \cdot SL$	$0.080 + 0.013 \cdot SL$
	$t_{PLH}$	0.500	$0.478 + 0.011 \cdot SL$	$0.488 + 0.009 \cdot SL$	$0.506 + 0.007 \cdot SL$
	$t_{PHL}$	0.491	$0.468 + 0.012 \cdot SL$	$0.479 + 0.009 \cdot SL$	$0.496 + 0.008 \cdot SL$
RN to Q	$t_R$	0.111	$0.081 + 0.015 \cdot SL$	$0.082 + 0.015 \cdot SL$	$0.080 + 0.015 \cdot SL$
	$t_F$	0.102	$0.073 + 0.014 \cdot SL$	$0.077 + 0.013 \cdot SL$	$0.079 + 0.013 \cdot SL$
	$t_{PLH}$	0.207	$0.185 + 0.011 \cdot SL$	$0.195 + 0.008 \cdot SL$	$0.212 + 0.007 \cdot SL$
	$t_{PHL}$	0.220	$0.196 + 0.012 \cdot SL$	$0.207 + 0.009 \cdot SL$	$0.225 + 0.008 \cdot SL$
SN to Q	$t_R$	0.122	$0.092 + 0.015 \cdot SL$	$0.094 + 0.014 \cdot SL$	$0.090 + 0.015 \cdot SL$
	$t_{PLH}$	0.478	$0.455 + 0.011 \cdot SL$	$0.466 + 0.008 \cdot SL$	$0.484 + 0.007 \cdot SL$
CK to QN	$t_R$	0.105	$0.077 + 0.014 \cdot SL$	$0.073 + 0.015 \cdot SL$	$0.070 + 0.015 \cdot SL$
	$t_F$	0.092	$0.064 + 0.014 \cdot SL$	$0.068 + 0.013 \cdot SL$	$0.063 + 0.013 \cdot SL$
	$t_{PLH}$	0.632	$0.612 + 0.010 \cdot SL$	$0.620 + 0.008 \cdot SL$	$0.633 + 0.007 \cdot SL$
	$t_{PHL}$	0.637	$0.616 + 0.010 \cdot SL$	$0.624 + 0.008 \cdot SL$	$0.637 + 0.007 \cdot SL$
RN to QN	$t_R$	0.127	$0.097 + 0.015 \cdot SL$	$0.097 + 0.015 \cdot SL$	$0.103 + 0.015 \cdot SL$
	$t_{PLH}$	0.405	$0.381 + 0.012 \cdot SL$	$0.392 + 0.009 \cdot SL$	$0.413 + 0.008 \cdot SL$
SN to QN	$t_R$	0.122	$0.090 + 0.016 \cdot SL$	$0.093 + 0.015 \cdot SL$	$0.097 + 0.015 \cdot SL$
	$t_F$	0.104	$0.075 + 0.015 \cdot SL$	$0.079 + 0.014 \cdot SL$	$0.080 + 0.013 \cdot SL$
	$t_{PLH}$	0.204	$0.180 + 0.012 \cdot SL$	$0.191 + 0.009 \cdot SL$	$0.212 + 0.008 \cdot SL$
	$t_{PHL}$	0.218	$0.194 + 0.012 \cdot SL$	$0.204 + 0.009 \cdot SL$	$0.221 + 0.008 \cdot SL$

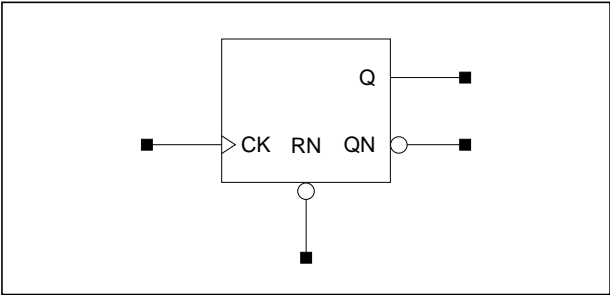
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



FT2/FT2D2

Toggle Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



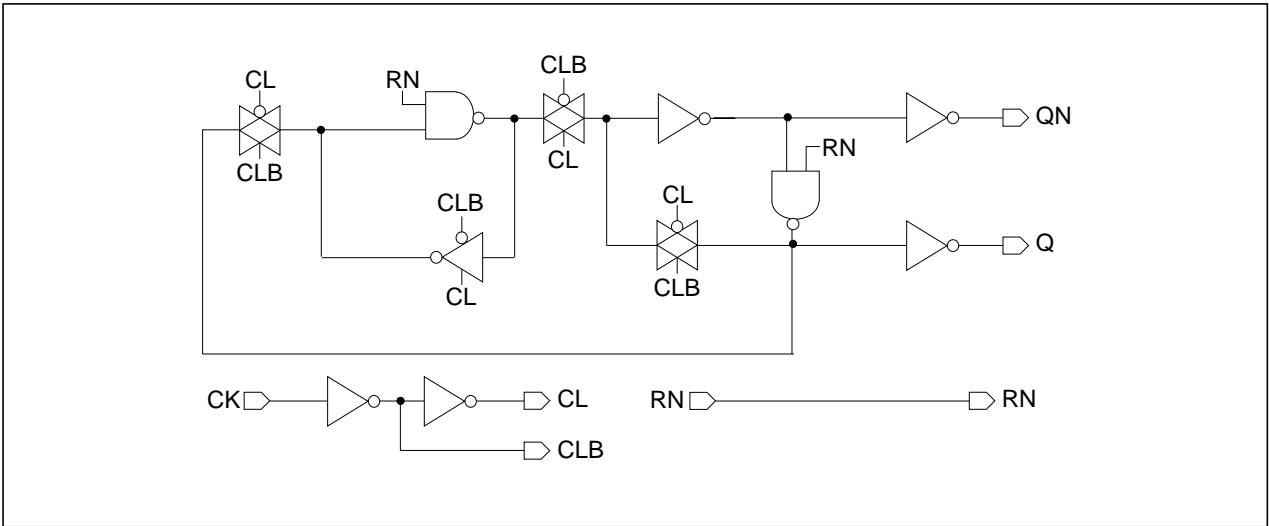
Truth Table

CK	RN	Q (n+1)	QN (n+1)
	1	QN (n)	Q (n)
	1	Q (n)	QN (n)
x	0	0	1

Cell Data

Input Load (SL)				Gate Count	
FT2		FT2D2		FT2	FT2D2
CK	RN	CK	RN		
0.6	1.5	0.6	1.5	6.00	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FT2	FT2D2
Pulse Width Low (CK)	t <sub>PWL</sub>	0.269	0.302
Pulse Width High (CK)	t <sub>PWH</sub>	0.338	0.359
Pulse Width Low (RN)	t <sub>PWL</sub>	0.321	0.357
Recovery Time (RN to CK)	t <sub>RC</sub>	0.000	0.000
Removal Time (RN to CK)	t <sub>RM</sub>	0.222	0.222



Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

FT2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t <sub>R</sub>	0.133	$0.075 + 0.029 \cdot SL$	$0.076 + 0.029 \cdot SL$	$0.069 + 0.030 \cdot SL$
	t <sub>F</sub>	0.118	$0.065 + 0.027 \cdot SL$	$0.066 + 0.026 \cdot SL$	$0.061 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.547	$0.514 + 0.017 \cdot SL$	$0.523 + 0.014 \cdot SL$	$0.531 + 0.013 \cdot SL$
	t <sub>PHL</sub>	0.521	$0.485 + 0.018 \cdot SL$	$0.495 + 0.016 \cdot SL$	$0.502 + 0.015 \cdot SL$
RN to Q	t <sub>F</sub>	0.120	$0.065 + 0.027 \cdot SL$	$0.068 + 0.027 \cdot SL$	$0.065 + 0.027 \cdot SL$
	t <sub>PHL</sub>	0.206	$0.170 + 0.018 \cdot SL$	$0.179 + 0.016 \cdot SL$	$0.187 + 0.015 \cdot SL$
CK to QN	t <sub>R</sub>	0.124	$0.069 + 0.027 \cdot SL$	$0.063 + 0.029 \cdot SL$	$0.056 + 0.030 \cdot SL$
	t <sub>F</sub>	0.118	$0.065 + 0.026 \cdot SL$	$0.063 + 0.027 \cdot SL$	$0.060 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.406	$0.376 + 0.015 \cdot SL$	$0.382 + 0.014 \cdot SL$	$0.384 + 0.013 \cdot SL$
	t <sub>PHL</sub>	0.432	$0.397 + 0.017 \cdot SL$	$0.405 + 0.015 \cdot SL$	$0.411 + 0.015 \cdot SL$
RN to QN	t <sub>R</sub>	0.123	$0.067 + 0.028 \cdot SL$	$0.062 + 0.029 \cdot SL$	$0.054 + 0.030 \cdot SL$
	t <sub>PLH</sub>	0.381	$0.351 + 0.015 \cdot SL$	$0.357 + 0.013 \cdot SL$	$0.359 + 0.013 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

FT2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t <sub>R</sub>	0.108	$0.077 + 0.015 \cdot SL$	$0.079 + 0.015 \cdot SL$	$0.075 + 0.015 \cdot SL$
	t <sub>F</sub>	0.093	$0.063 + 0.015 \cdot SL$	$0.070 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$
	t <sub>PLH</sub>	0.586	$0.565 + 0.011 \cdot SL$	$0.574 + 0.008 \cdot SL$	$0.589 + 0.007 \cdot SL$
	t <sub>PHL</sub>	0.551	$0.529 + 0.011 \cdot SL$	$0.539 + 0.009 \cdot SL$	$0.554 + 0.008 \cdot SL$
RN to Q	t <sub>F</sub>	0.094	$0.066 + 0.014 \cdot SL$	$0.069 + 0.013 \cdot SL$	$0.069 + 0.013 \cdot SL$
	t <sub>PHL</sub>	0.202	$0.180 + 0.011 \cdot SL$	$0.189 + 0.009 \cdot SL$	$0.205 + 0.008 \cdot SL$
CK to QN	t <sub>R</sub>	0.097	$0.069 + 0.014 \cdot SL$	$0.067 + 0.014 \cdot SL$	$0.057 + 0.015 \cdot SL$
	t <sub>F</sub>	0.092	$0.065 + 0.013 \cdot SL$	$0.066 + 0.013 \cdot SL$	$0.062 + 0.013 \cdot SL$
	t <sub>PLH</sub>	0.411	$0.393 + 0.009 \cdot SL$	$0.400 + 0.008 \cdot SL$	$0.408 + 0.007 \cdot SL$
	t <sub>PHL</sub>	0.433	$0.412 + 0.011 \cdot SL$	$0.421 + 0.008 \cdot SL$	$0.433 + 0.008 \cdot SL$
RN to QN	t <sub>R</sub>	0.095	$0.067 + 0.014 \cdot SL$	$0.064 + 0.015 \cdot SL$	$0.055 + 0.015 \cdot SL$
	t <sub>PLH</sub>	0.388	$0.369 + 0.009 \cdot SL$	$0.376 + 0.007 \cdot SL$	$0.385 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# LATCHES

## Cell List

Cell Name	Function Description
LD1	D Latch with Active High
LD1D2	D Latch with Active High, 2X Drive
LD1A	D Latch with Active High, Tri-State Output
LD1D2A	D Latch with Active High, Tri-State Output, 2x Drive
LD1Q	D Latch with Active High, Q Output Only
LD1QD2	D Latch with Active High, Q Output Only, 2X Drive
LD2	D Latch with Active High, Reset
LD2D2	D Latch with Active High, Reset, 2X Drive
LD2Q	D Latch with Active High, Reset, Q Output Only
LD2QD2	D Latch with Active High, Reset, Q Output Only, 2X Drive
LD3	D Latch with Active High, Set
LD3D2	D Latch with Active High, Set, 2X Drive
LD4	D Latch with Active High, Reset, Set
LD4D2	D Latch with Active High, Reset, Set, 2X Drive
LD5	D Latch with Active Low
LD5D2	D Latch with Active Low, 2X Drive
LD5Q	D Latch with Active Low, Q Output Only
LD5QD2	D Latch with Active Low, Q Output Only, 2X Drive
LD6	D Latch with Active Low, Reset
LD6D2	D Latch with Active Low, Reset, 2X Drive
LD6Q	D Latch with Active Low, Reset, Q Output Only
LD6QD2	D Latch with Active Low, Reset, Q Output Only, 2X Drive
LD7	D Latch with Active Low, Set
LD7D2	D Latch with Active Low, Set, 2X Drive
LD8	D Latch with Active Low, Reset, Set
LD8D2	D Latch with Active Low, Reset, Set, 2X Drive
LDI2	D Latch with 2 Input, 2 Active High
LDI2D2	D Latch with 2 Input, 2 Active High, 2X Drive
LDI3	D Latch with 3 Input, 3 Active High
LDI3D2	D Latch with 3 Input, 3 Active High, 2X Drive



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### Cell List

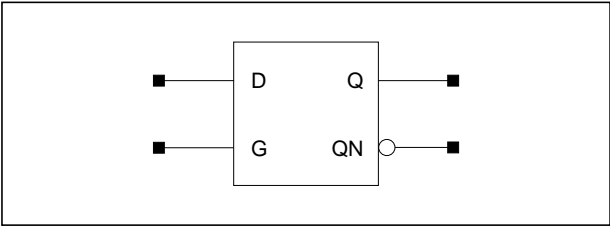
Cell Name	Function Description
LS0	SR Latch
LS0D2	SR Latch with 2X Drive
LS1	SR Latch with Separate Inputs
LS1D2	SR Latch with Separate Inputs, 2X Drive



# LD1/LD1D2

## D Latch with Active High, 1X/2X Drive

### Logic Symbol



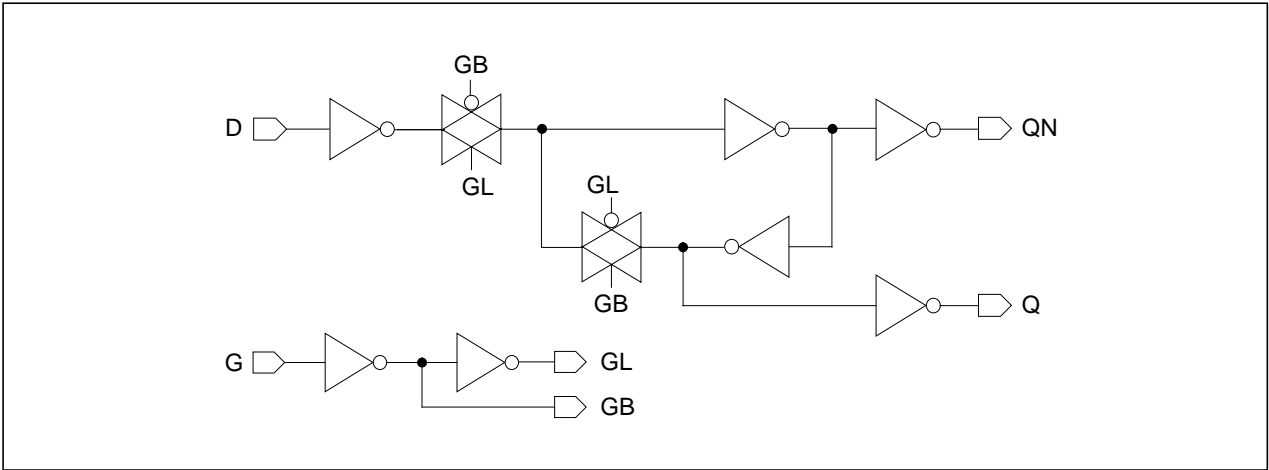
### Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

### Cell Data

Input Load (SL)				Gate Count	
LD1		LD1D2		LD1	LD1D2
D	G	D	G		
0.6	0.5	0.6	0.6	4.00	4.33

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD1	LD1D2
Input Setup Time (D to G)	t <sub>SU</sub>	0.320	0.347
Input Hold Time (D to G)	t <sub>HD</sub>	0.094	0.062
Pulse Width High (G)	t <sub>PWH</sub>	0.289	0.317



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

## LD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.112	$0.054 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.105	$0.053 + 0.026 \cdot \text{SL}$	$0.050 + 0.027 \cdot \text{SL}$	$0.044 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.355	$0.326 + 0.015 \cdot \text{SL}$	$0.330 + 0.014 \cdot \text{SL}$	$0.331 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.380	$0.347 + 0.017 \cdot \text{SL}$	$0.353 + 0.015 \cdot \text{SL}$	$0.356 + 0.015 \cdot \text{SL}$
G to Q	$t_R$	0.112	$0.054 + 0.029 \cdot \text{SL}$	$0.048 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.105	$0.053 + 0.026 \cdot \text{SL}$	$0.050 + 0.027 \cdot \text{SL}$	$0.044 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.417	$0.387 + 0.015 \cdot \text{SL}$	$0.392 + 0.014 \cdot \text{SL}$	$0.393 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.431	$0.398 + 0.017 \cdot \text{SL}$	$0.404 + 0.015 \cdot \text{SL}$	$0.407 + 0.015 \cdot \text{SL}$
D to QN	$t_R$	0.123	$0.065 + 0.029 \cdot \text{SL}$	$0.061 + 0.030 \cdot \text{SL}$	$0.054 + 0.031 \cdot \text{SL}$
	$t_F$	0.114	$0.061 + 0.027 \cdot \text{SL}$	$0.060 + 0.027 \cdot \text{SL}$	$0.056 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.305	$0.274 + 0.015 \cdot \text{SL}$	$0.280 + 0.014 \cdot \text{SL}$	$0.282 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.301	$0.265 + 0.018 \cdot \text{SL}$	$0.274 + 0.016 \cdot \text{SL}$	$0.281 + 0.015 \cdot \text{SL}$
G to QN	$t_R$	0.122	$0.064 + 0.029 \cdot \text{SL}$	$0.061 + 0.030 \cdot \text{SL}$	$0.053 + 0.031 \cdot \text{SL}$
	$t_F$	0.114	$0.059 + 0.027 \cdot \text{SL}$	$0.062 + 0.027 \cdot \text{SL}$	$0.055 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.356	$0.325 + 0.015 \cdot \text{SL}$	$0.331 + 0.014 \cdot \text{SL}$	$0.334 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.362	$0.327 + 0.018 \cdot \text{SL}$	$0.335 + 0.016 \cdot \text{SL}$	$0.342 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ 

## LD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.053 + 0.014 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.392	$0.374 + 0.009 \cdot \text{SL}$	$0.380 + 0.007 \cdot \text{SL}$	$0.386 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.412	$0.392 + 0.010 \cdot \text{SL}$	$0.400 + 0.008 \cdot \text{SL}$	$0.410 + 0.007 \cdot \text{SL}$
G to Q	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.054 + 0.013 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.457	$0.440 + 0.009 \cdot \text{SL}$	$0.446 + 0.007 \cdot \text{SL}$	$0.452 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.472	$0.452 + 0.010 \cdot \text{SL}$	$0.460 + 0.008 \cdot \text{SL}$	$0.470 + 0.007 \cdot \text{SL}$
D to QN	$t_R$	0.092	$0.063 + 0.015 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.060 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.290 + 0.009 \cdot \text{SL}$	$0.298 + 0.007 \cdot \text{SL}$	$0.305 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.279 + 0.010 \cdot \text{SL}$	$0.287 + 0.008 \cdot \text{SL}$	$0.300 + 0.007 \cdot \text{SL}$
G to QN	$t_R$	0.092	$0.062 + 0.015 \cdot \text{SL}$	$0.063 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.369	$0.350 + 0.009 \cdot \text{SL}$	$0.357 + 0.007 \cdot \text{SL}$	$0.365 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.365	$0.344 + 0.011 \cdot \text{SL}$	$0.353 + 0.008 \cdot \text{SL}$	$0.365 + 0.007 \cdot \text{SL}$

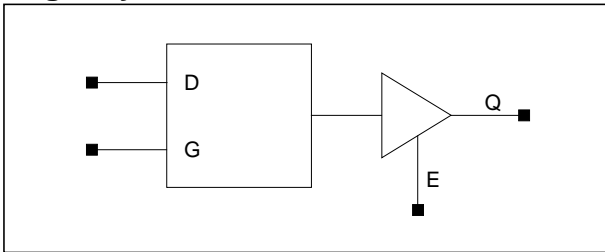
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## LD1A/LD1D2A

### D Latch with Active High, Tri-State Output, 1x/2x Drive

## Logic Symbol



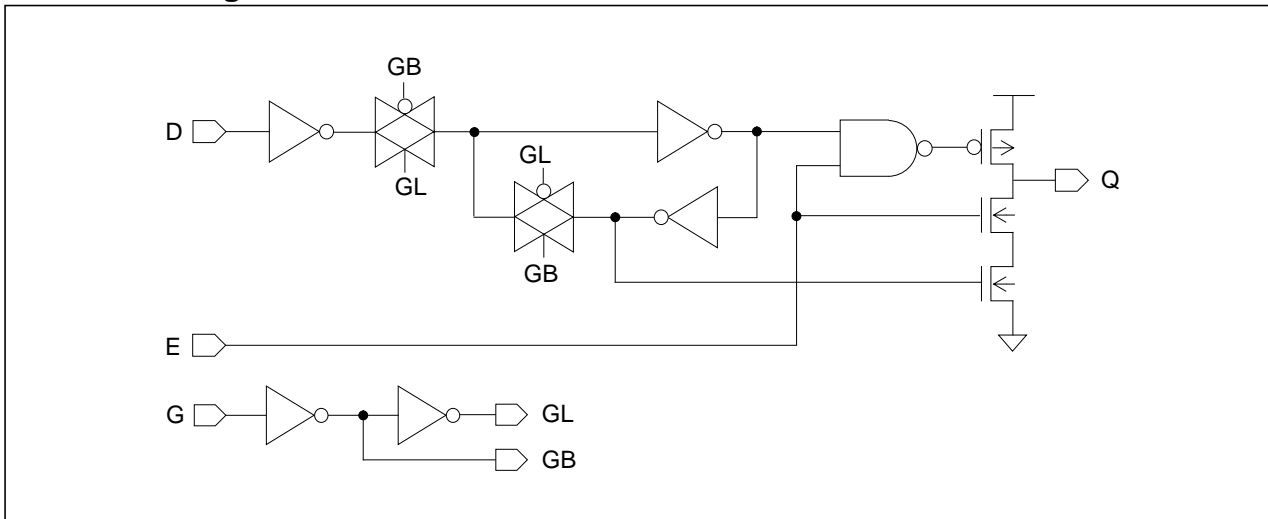
## Truth Table

D	G	E	Q (n+1)
x	x	0	Hi-Z
0	1	1	0
1	1	1	1
x	0	1	Q (n)

## Cell Data

Input Load (SL)						Output Load (SL)		Gate Count	
LD1A			LD1D2A			LD1A	LD1D2A	LD1A	LD1D2A
D	G	E	D	G	E	Q	Q	4.33	5.00
0.6	0.5	1.3	0.6	0.6	1.6	1.0	1.2		

### Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD1A	LD1D2A
Input Setup Time (D to G)	t <sub>SU</sub>	0.322	0.321
Input Hold Time (D to G)	t <sub>HD</sub>	0.086	0.089
Pulse Width High (G)	t <sub>PWH</sub>	0.284	0.293



## D Latch with Active High, Tri-State Output 1x/2x Drive

## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17$  ns, SL: Standard Load)

## LD1A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.128	$0.070 + 0.029 \cdot SL$	$0.067 + 0.030 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.126	$0.056 + 0.035 \cdot SL$	$0.052 + 0.036 \cdot SL$	$0.048 + 0.036 \cdot SL$
	$t_{PLH}$	0.365	$0.335 + 0.015 \cdot SL$	$0.340 + 0.014 \cdot SL$	$0.343 + 0.013 \cdot SL$
	$t_{PHL}$	0.374	$0.338 + 0.018 \cdot SL$	$0.341 + 0.018 \cdot SL$	$0.342 + 0.017 \cdot SL$
G to Q	$t_R$	0.128	$0.069 + 0.029 \cdot SL$	$0.067 + 0.030 \cdot SL$	$0.062 + 0.030 \cdot SL$
	$t_F$	0.126	$0.056 + 0.035 \cdot SL$	$0.052 + 0.036 \cdot SL$	$0.048 + 0.036 \cdot SL$
	$t_{PLH}$	0.422	$0.392 + 0.015 \cdot SL$	$0.397 + 0.014 \cdot SL$	$0.400 + 0.013 \cdot SL$
	$t_{PHL}$	0.421	$0.384 + 0.018 \cdot SL$	$0.387 + 0.018 \cdot SL$	$0.388 + 0.017 \cdot SL$
E to Q	$t_R$	0.154	$0.094 + 0.030 \cdot SL$	$0.084 + 0.033 \cdot SL$	$0.075 + 0.034 \cdot SL$
	$t_F$	0.180	$0.111 + 0.035 \cdot SL$	$0.101 + 0.037 \cdot SL$	$0.082 + 0.039 \cdot SL$
	$t_{PLH}$	0.134	$0.102 + 0.016 \cdot SL$	$0.109 + 0.014 \cdot SL$	$0.112 + 0.014 \cdot SL$
	$t_{PHL}$	0.079	$0.033 + 0.023 \cdot SL$	$0.053 + 0.018 \cdot SL$	$0.053 + 0.018 \cdot SL$
	$t_{PLZ}$	0.107	$0.107 + 0.000 \cdot SL$	$0.107 + 0.000 \cdot SL$	$0.107 + 0.000 \cdot SL$
	$t_{PHZ}$	0.154	$0.154 + 0.000 \cdot SL$	$0.154 + 0.000 \cdot SL$	$0.154 + 0.000 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## LD1D2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.097	$0.067 + 0.015 \cdot SL$	$0.067 + 0.015 \cdot SL$	$0.064 + 0.015 \cdot SL$
	$t_F$	0.083	$0.049 + 0.017 \cdot SL$	$0.047 + 0.018 \cdot SL$	$0.041 + 0.018 \cdot SL$
	$t_{PLH}$	0.359	$0.341 + 0.009 \cdot SL$	$0.347 + 0.007 \cdot SL$	$0.355 + 0.007 \cdot SL$
	$t_{PHL}$	0.358	$0.339 + 0.010 \cdot SL$	$0.342 + 0.009 \cdot SL$	$0.344 + 0.009 \cdot SL$
G to Q	$t_R$	0.098	$0.067 + 0.015 \cdot SL$	$0.068 + 0.015 \cdot SL$	$0.063 + 0.015 \cdot SL$
	$t_F$	0.083	$0.049 + 0.017 \cdot SL$	$0.047 + 0.018 \cdot SL$	$0.040 + 0.018 \cdot SL$
	$t_{PLH}$	0.425	$0.407 + 0.009 \cdot SL$	$0.413 + 0.007 \cdot SL$	$0.421 + 0.007 \cdot SL$
	$t_{PHL}$	0.418	$0.398 + 0.010 \cdot SL$	$0.401 + 0.009 \cdot SL$	$0.404 + 0.009 \cdot SL$
E to Q	$t_R$	0.124	$0.100 + 0.012 \cdot SL$	$0.090 + 0.015 \cdot SL$	$0.075 + 0.016 \cdot SL$
	$t_F$	0.123	$0.086 + 0.019 \cdot SL$	$0.093 + 0.017 \cdot SL$	$0.074 + 0.018 \cdot SL$
	$t_{PLH}$	0.127	$0.107 + 0.010 \cdot SL$	$0.116 + 0.008 \cdot SL$	$0.127 + 0.007 \cdot SL$
	$t_{PHL}$	0.040	$0.010 + 0.015 \cdot SL$	$0.032 + 0.010 \cdot SL$	$0.046 + 0.009 \cdot SL$
	$t_{PLZ}$	0.107	$0.107 + 0.000 \cdot SL$	$0.107 + 0.000 \cdot SL$	$0.107 + 0.000 \cdot SL$
	$t_{PHZ}$	0.182	$0.182 + 0.000 \cdot SL$	$0.182 + 0.000 \cdot SL$	$0.182 + 0.000 \cdot SL$

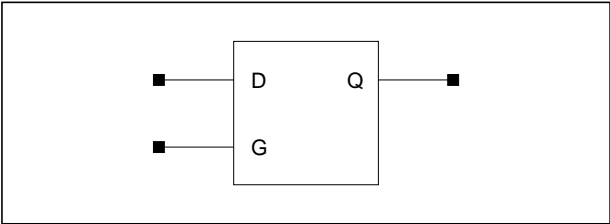
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



# LD1Q/LD1QD2

D Latch with Active High, Q Output Only, 1X/2X Drive

## Logic Symbol



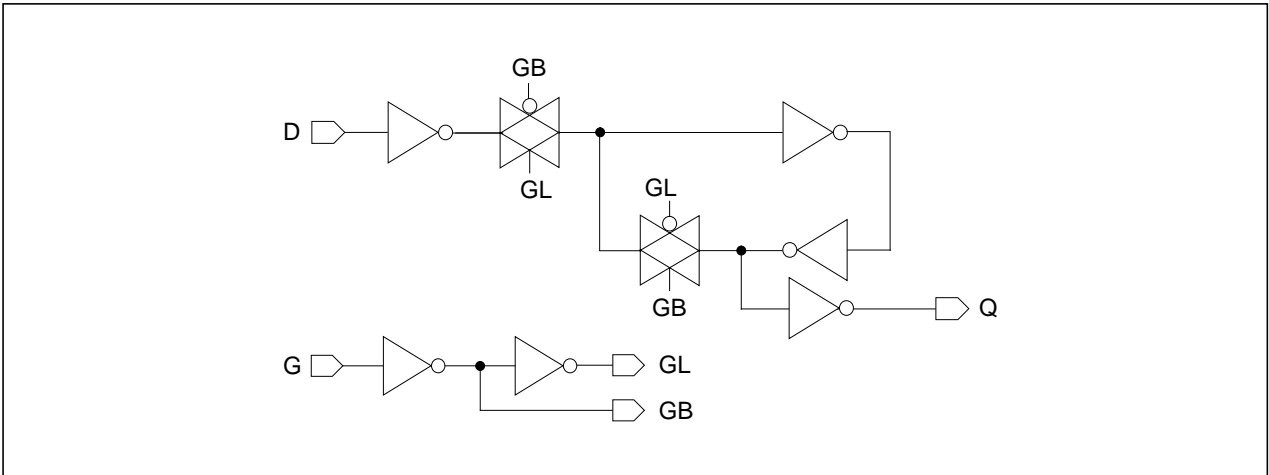
## Truth Table

D	G	Q (n+1)
0	1	0
1	1	1
x	0	Q (n)

## Cell Data

Input Load (SL)				Gate Count	
LD1Q		LD1QD2		LD1Q	LD1QD2
D	G	D	G		
0.6	0.6	0.6	0.6	3.33	3.67

## Schematic Diagram



## Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD1Q	LD1QD2
Input Setup Time (D to G)	t <sub>SU</sub>	0.287	0.304
Input Hold Time (D to G)	t <sub>HD</sub>	0.113	0.102
Pulse Width High (G)	t <sub>PWH</sub>	0.272	0.280



**D Latch with Active High, Q Output Only, 1X/2X Drive****Switching Characteristics**(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ ns}$ , SL: Standard Load)**LD1Q**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.110	$0.051 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$	$0.042 + 0.031 \cdot \text{SL}$
	$t_F$	0.102	$0.049 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$	$0.042 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.320	$0.291 + 0.015 \cdot \text{SL}$	$0.295 + 0.014 \cdot \text{SL}$	$0.295 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.340	$0.307 + 0.016 \cdot \text{SL}$	$0.313 + 0.015 \cdot \text{SL}$	$0.316 + 0.014 \cdot \text{SL}$
G to Q	$t_R$	0.110	$0.052 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.102	$0.048 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$	$0.042 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.381	$0.352 + 0.015 \cdot \text{SL}$	$0.356 + 0.014 \cdot \text{SL}$	$0.357 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.398	$0.365 + 0.016 \cdot \text{SL}$	$0.371 + 0.015 \cdot \text{SL}$	$0.374 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ **LD1QD2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.079	$0.050 + 0.015 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.076	$0.047 + 0.014 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$	$0.046 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.322	$0.305 + 0.009 \cdot \text{SL}$	$0.310 + 0.007 \cdot \text{SL}$	$0.316 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.340	$0.320 + 0.010 \cdot \text{SL}$	$0.328 + 0.008 \cdot \text{SL}$	$0.338 + 0.007 \cdot \text{SL}$
G to Q	$t_R$	0.079	$0.050 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.077	$0.050 + 0.013 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$	$0.047 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.387	$0.370 + 0.009 \cdot \text{SL}$	$0.376 + 0.007 \cdot \text{SL}$	$0.381 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.400	$0.380 + 0.010 \cdot \text{SL}$	$0.388 + 0.008 \cdot \text{SL}$	$0.397 + 0.007 \cdot \text{SL}$

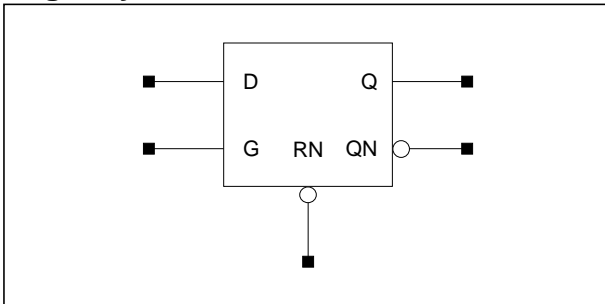
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## LD2/LD2D2

### D Latch with Active High, Reset, 1X/2X Drive

#### Logic Symbol



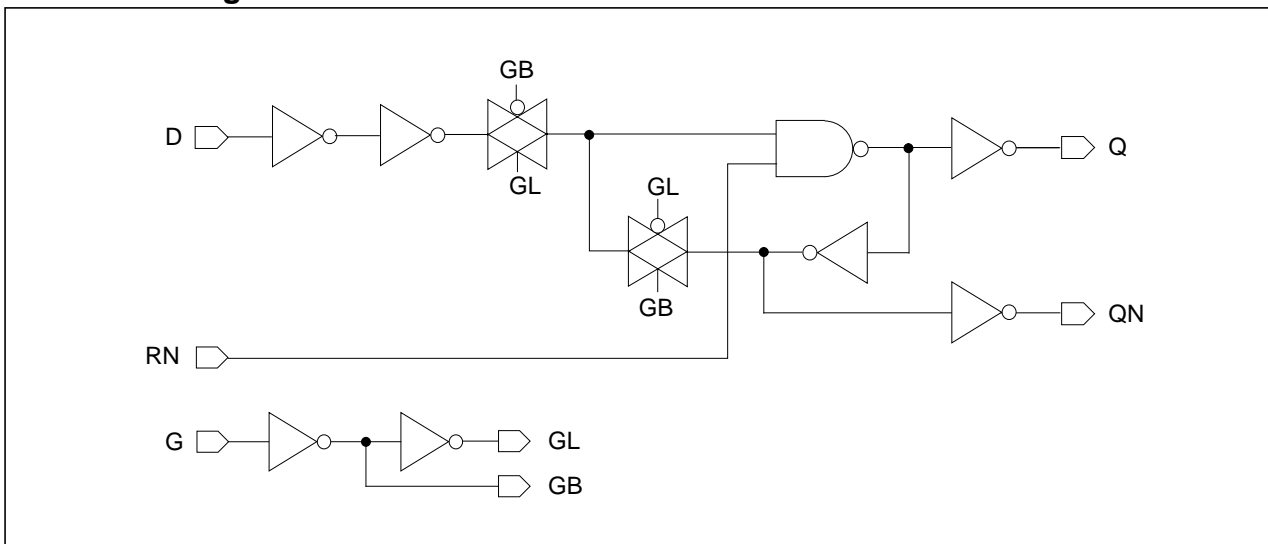
#### Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

#### Cell Data

Input Load (SL)						Gate Count	
LD2			LD2D2			LD2	LD2D2
D	G	RN	D	G	RN		
0.6	0.5	0.8	0.6	0.5	0.8	4.67	5.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD2	LD2D2
Input Setup Time (D to G)	$t_{SU}$	0.292	0.312
Input Hold Time (D to G)	$t_{HD}$	0.003	0.000
Pulse Width High (G)	$t_{PWH}$	0.308	0.336
Pulse Width Low (RN)	$t_{PWL}$	0.250	0.287
Recovery Time (RN to G)	$t_{RC}$	0.000	0.005
Removal Time (RN to G)	$t_{RM}$	0.267	0.215



## LD2/LD2D2

### D Latch with Active High, Reset, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### LD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.135	$0.075 + 0.030 \cdot \text{SL}$	$0.074 + 0.030 \cdot \text{SL}$	$0.069 + 0.031 \cdot \text{SL}$
	$t_F$	0.115	$0.061 + 0.027 \cdot \text{SL}$	$0.064 + 0.026 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.344 + 0.017 \cdot \text{SL}$	$0.352 + 0.015 \cdot \text{SL}$	$0.360 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.376	$0.341 + 0.018 \cdot \text{SL}$	$0.350 + 0.016 \cdot \text{SL}$	$0.357 + 0.015 \cdot \text{SL}$
G to Q	$t_R$	0.133	$0.073 + 0.030 \cdot \text{SL}$	$0.073 + 0.030 \cdot \text{SL}$	$0.069 + 0.031 \cdot \text{SL}$
	$t_F$	0.114	$0.060 + 0.027 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.386	$0.352 + 0.017 \cdot \text{SL}$	$0.360 + 0.015 \cdot \text{SL}$	$0.368 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.376	$0.341 + 0.018 \cdot \text{SL}$	$0.349 + 0.016 \cdot \text{SL}$	$0.357 + 0.015 \cdot \text{SL}$
RN to Q	$t_R$	0.131	$0.071 + 0.030 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$	$0.067 + 0.031 \cdot \text{SL}$
	$t_F$	0.115	$0.061 + 0.027 \cdot \text{SL}$	$0.063 + 0.026 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.175	$0.142 + 0.017 \cdot \text{SL}$	$0.150 + 0.015 \cdot \text{SL}$	$0.157 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.190	$0.155 + 0.018 \cdot \text{SL}$	$0.164 + 0.015 \cdot \text{SL}$	$0.171 + 0.015 \cdot \text{SL}$
D to QN	$t_R$	0.112	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.030 \cdot \text{SL}$
	$t_F$	0.107	$0.055 + 0.026 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.435	$0.405 + 0.015 \cdot \text{SL}$	$0.410 + 0.013 \cdot \text{SL}$	$0.411 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.455	$0.422 + 0.017 \cdot \text{SL}$	$0.429 + 0.015 \cdot \text{SL}$	$0.432 + 0.014 \cdot \text{SL}$
G to QN	$t_R$	0.113	$0.056 + 0.028 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.030 \cdot \text{SL}$
	$t_F$	0.105	$0.051 + 0.027 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.434	$0.405 + 0.015 \cdot \text{SL}$	$0.410 + 0.013 \cdot \text{SL}$	$0.411 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.463	$0.429 + 0.017 \cdot \text{SL}$	$0.436 + 0.015 \cdot \text{SL}$	$0.440 + 0.014 \cdot \text{SL}$
RN to QN	$t_R$	0.112	$0.055 + 0.028 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.044 + 0.030 \cdot \text{SL}$
	$t_F$	0.107	$0.056 + 0.026 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$	$0.046 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.249	$0.220 + 0.015 \cdot \text{SL}$	$0.224 + 0.013 \cdot \text{SL}$	$0.225 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.252	$0.219 + 0.017 \cdot \text{SL}$	$0.226 + 0.015 \cdot \text{SL}$	$0.229 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## D Latch with Active High, Reset, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ ns}$ , SL: Standard Load)

## LD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.105	$0.075 + 0.015 \cdot \text{SL}$	$0.074 + 0.015 \cdot \text{SL}$	$0.073 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.384	$0.363 + 0.010 \cdot \text{SL}$	$0.372 + 0.008 \cdot \text{SL}$	$0.385 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.377	$0.356 + 0.011 \cdot \text{SL}$	$0.365 + 0.009 \cdot \text{SL}$	$0.378 + 0.008 \cdot \text{SL}$
G to Q	$t_R$	0.105	$0.076 + 0.015 \cdot \text{SL}$	$0.076 + 0.015 \cdot \text{SL}$	$0.073 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.062 + 0.014 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.062 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.391	$0.371 + 0.010 \cdot \text{SL}$	$0.380 + 0.008 \cdot \text{SL}$	$0.393 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.377	$0.356 + 0.011 \cdot \text{SL}$	$0.364 + 0.009 \cdot \text{SL}$	$0.378 + 0.008 \cdot \text{SL}$
RN to Q	$t_R$	0.100	$0.069 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$	$0.069 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.060 + 0.015 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.178	$0.158 + 0.010 \cdot \text{SL}$	$0.166 + 0.008 \cdot \text{SL}$	$0.179 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.188	$0.167 + 0.011 \cdot \text{SL}$	$0.176 + 0.009 \cdot \text{SL}$	$0.189 + 0.008 \cdot \text{SL}$
D to QN	$t_R$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.055 + 0.015 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.053 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.473	$0.455 + 0.009 \cdot \text{SL}$	$0.462 + 0.007 \cdot \text{SL}$	$0.468 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.497	$0.477 + 0.010 \cdot \text{SL}$	$0.485 + 0.008 \cdot \text{SL}$	$0.496 + 0.007 \cdot \text{SL}$
G to QN	$t_R$	0.086	$0.057 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.053 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.473	$0.455 + 0.009 \cdot \text{SL}$	$0.461 + 0.007 \cdot \text{SL}$	$0.468 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.505	$0.484 + 0.010 \cdot \text{SL}$	$0.493 + 0.008 \cdot \text{SL}$	$0.503 + 0.007 \cdot \text{SL}$
RN to QN	$t_R$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.054 + 0.015 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.055 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.284	$0.266 + 0.009 \cdot \text{SL}$	$0.272 + 0.007 \cdot \text{SL}$	$0.278 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.288	$0.269 + 0.010 \cdot \text{SL}$	$0.275 + 0.008 \cdot \text{SL}$	$0.286 + 0.007 \cdot \text{SL}$

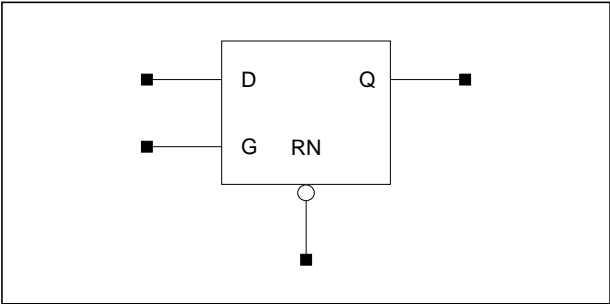
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



LD2Q/LD2QD2

D Latch with Active High, Reset, Q Output Only, 1X/2X Drive

Logic Symbol



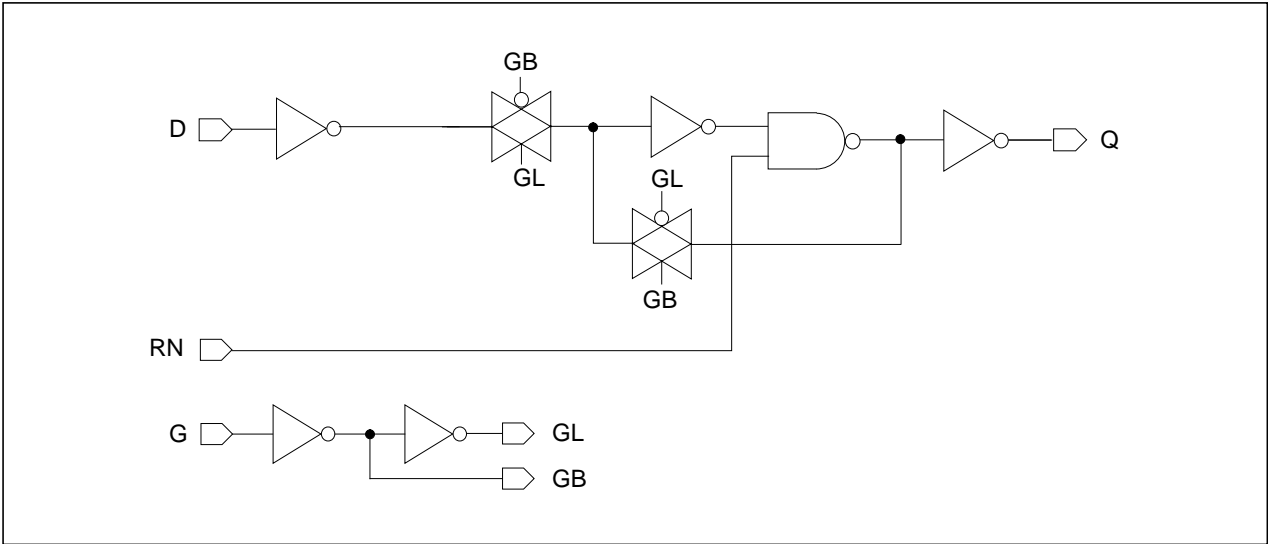
Truth Table

D	G	RN	Q (n+1)
0	1	1	0
1	1	1	1
x	0	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
LD2Q			LD2QD2			LD2Q	LD2QD2
D	G	RN	D	G	RN		
0.6	0.6	0.8	0.6	0.6	0.8	4.00	4.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD2Q	LD2QD2
Input Setup Time (D to G)	t <sub>SU</sub>	0.296	0.306
Input Hold Time (D to G)	t <sub>HD</sub>	0.113	0.099
Pulse Width High (G)	t <sub>PWH</sub>	0.284	0.290
Pulse Width Low (RN)	t <sub>PWL</sub>	0.250	0.271
Recovery Time (RN to G)	t <sub>RC</sub>	0.000	0.000
Removal Time (RN to G)	t <sub>RM</sub>	0.599	0.551



**D Latch with Active High, Reset, Q Output Only, 1X/2X Drive****Switching Characteristics**(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ ns}$ , SL: Standard Load)**LD2Q**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.125	$0.067 + 0.029 \cdot \text{SL}$	$0.065 + 0.030 \cdot \text{SL}$	$0.059 + 0.030 \cdot \text{SL}$
	$t_F$	0.104	$0.053 + 0.025 \cdot \text{SL}$	$0.053 + 0.025 \cdot \text{SL}$	$0.047 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.359	$0.327 + 0.016 \cdot \text{SL}$	$0.334 + 0.014 \cdot \text{SL}$	$0.339 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.359	$0.327 + 0.016 \cdot \text{SL}$	$0.334 + 0.014 \cdot \text{SL}$	$0.338 + 0.014 \cdot \text{SL}$
G to Q	$t_R$	0.125	$0.067 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$	$0.059 + 0.030 \cdot \text{SL}$
	$t_F$	0.105	$0.055 + 0.025 \cdot \text{SL}$	$0.053 + 0.025 \cdot \text{SL}$	$0.048 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.427	$0.395 + 0.016 \cdot \text{SL}$	$0.403 + 0.014 \cdot \text{SL}$	$0.408 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.423	$0.390 + 0.016 \cdot \text{SL}$	$0.398 + 0.014 \cdot \text{SL}$	$0.402 + 0.014 \cdot \text{SL}$
RN to Q	$t_R$	0.129	$0.074 + 0.028 \cdot \text{SL}$	$0.065 + 0.030 \cdot \text{SL}$	$0.060 + 0.030 \cdot \text{SL}$
	$t_F$	0.108	$0.057 + 0.025 \cdot \text{SL}$	$0.059 + 0.025 \cdot \text{SL}$	$0.052 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.167	$0.135 + 0.016 \cdot \text{SL}$	$0.143 + 0.014 \cdot \text{SL}$	$0.147 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.179	$0.146 + 0.016 \cdot \text{SL}$	$0.154 + 0.014 \cdot \text{SL}$	$0.159 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ **LD2QD2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.096	$0.067 + 0.015 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.079	$0.051 + 0.014 \cdot \text{SL}$	$0.057 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.364	$0.345 + 0.010 \cdot \text{SL}$	$0.353 + 0.008 \cdot \text{SL}$	$0.365 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.359	$0.339 + 0.010 \cdot \text{SL}$	$0.347 + 0.008 \cdot \text{SL}$	$0.359 + 0.007 \cdot \text{SL}$
G to Q	$t_R$	0.096	$0.066 + 0.015 \cdot \text{SL}$	$0.068 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.053 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.434	$0.415 + 0.010 \cdot \text{SL}$	$0.422 + 0.008 \cdot \text{SL}$	$0.434 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.423	$0.404 + 0.010 \cdot \text{SL}$	$0.411 + 0.008 \cdot \text{SL}$	$0.423 + 0.007 \cdot \text{SL}$
RN to Q	$t_R$	0.097	$0.068 + 0.015 \cdot \text{SL}$	$0.068 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.172	$0.153 + 0.010 \cdot \text{SL}$	$0.161 + 0.008 \cdot \text{SL}$	$0.173 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.179	$0.159 + 0.010 \cdot \text{SL}$	$0.167 + 0.008 \cdot \text{SL}$	$0.179 + 0.007 \cdot \text{SL}$

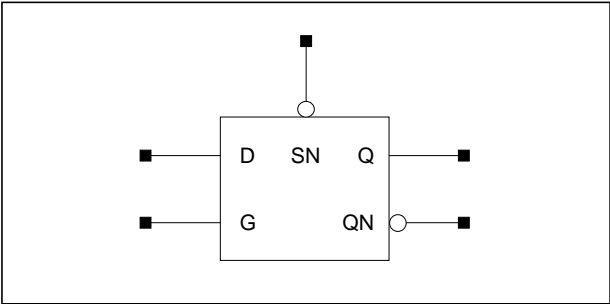
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# LD3/LD3D2

## D Latch with Active High, Set, 1X/2X Drive

### Logic Symbol



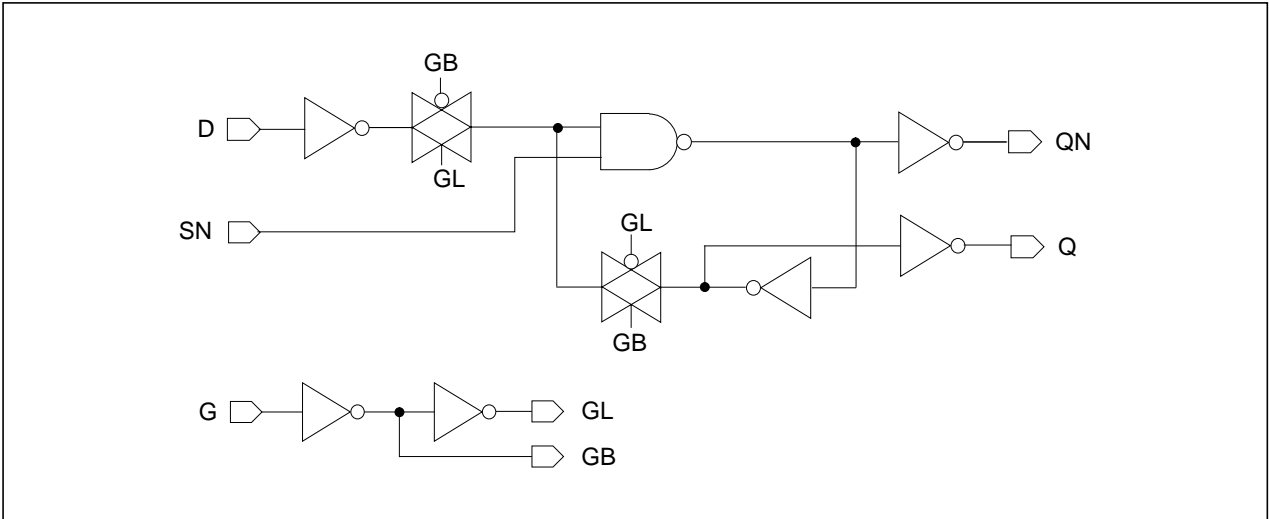
### Truth Table

D	G	SN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	1	0

### Cell Data

Input Load (SL)						Gate Count	
LD3			LD3D2			LD3	LD3D2
D	G	SN	D	G	SN		
0.6	0.5	0.8	0.6	0.6	0.8	4.33	4.67

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD3	LD3D2
Input Setup Time (D to G)	t <sub>SU</sub>	0.353	0.369
Input Hold Time (D to G)	t <sub>HD</sub>	0.075	0.051
Pulse Width High (G)	t <sub>PWH</sub>	0.311	0.340
Pulse Width Low (SN)	t <sub>PWL</sub>	0.250	0.289
Recovery Time (SN to G)	t <sub>RC</sub>	0.000	0.000
Removal Time (SN to G)	t <sub>RM</sub>	0.257	0.220



## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

## LD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.107	$0.056 + 0.026 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.046 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.367	$0.338 + 0.015 \cdot \text{SL}$	$0.342 + 0.014 \cdot \text{SL}$	$0.343 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.414	$0.380 + 0.017 \cdot \text{SL}$	$0.387 + 0.015 \cdot \text{SL}$	$0.391 + 0.014 \cdot \text{SL}$
G to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.106	$0.053 + 0.027 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.429	$0.400 + 0.015 \cdot \text{SL}$	$0.404 + 0.014 \cdot \text{SL}$	$0.405 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.467	$0.433 + 0.017 \cdot \text{SL}$	$0.440 + 0.015 \cdot \text{SL}$	$0.444 + 0.014 \cdot \text{SL}$
SN to Q	$t_R$	0.112	$0.055 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.106	$0.052 + 0.027 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.249	$0.220 + 0.015 \cdot \text{SL}$	$0.224 + 0.014 \cdot \text{SL}$	$0.226 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.256	$0.222 + 0.017 \cdot \text{SL}$	$0.229 + 0.015 \cdot \text{SL}$	$0.233 + 0.014 \cdot \text{SL}$
D to QN	$t_R$	0.135	$0.075 + 0.030 \cdot \text{SL}$	$0.076 + 0.029 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.114	$0.060 + 0.027 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.301 + 0.017 \cdot \text{SL}$	$0.310 + 0.015 \cdot \text{SL}$	$0.317 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.310	$0.275 + 0.018 \cdot \text{SL}$	$0.283 + 0.016 \cdot \text{SL}$	$0.291 + 0.015 \cdot \text{SL}$
G to QN	$t_R$	0.133	$0.073 + 0.030 \cdot \text{SL}$	$0.076 + 0.030 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.114	$0.060 + 0.027 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.388	$0.354 + 0.017 \cdot \text{SL}$	$0.363 + 0.015 \cdot \text{SL}$	$0.370 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.372	$0.337 + 0.018 \cdot \text{SL}$	$0.345 + 0.016 \cdot \text{SL}$	$0.353 + 0.015 \cdot \text{SL}$
SN to QN	$t_R$	0.134	$0.079 + 0.028 \cdot \text{SL}$	$0.070 + 0.030 \cdot \text{SL}$	$0.067 + 0.030 \cdot \text{SL}$
	$t_F$	0.115	$0.061 + 0.027 \cdot \text{SL}$	$0.064 + 0.027 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.177	$0.143 + 0.017 \cdot \text{SL}$	$0.152 + 0.015 \cdot \text{SL}$	$0.159 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.156 + 0.018 \cdot \text{SL}$	$0.165 + 0.016 \cdot \text{SL}$	$0.172 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## LD3/LD3D2

### D Latch with Active High, Reset, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### LD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.086	$0.057 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.406	$0.389 + 0.009 \cdot \text{SL}$	$0.395 + 0.007 \cdot \text{SL}$	$0.401 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.453	$0.433 + 0.010 \cdot \text{SL}$	$0.441 + 0.008 \cdot \text{SL}$	$0.452 + 0.007 \cdot \text{SL}$
G to Q	$t_R$	0.087	$0.058 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.473	$0.455 + 0.009 \cdot \text{SL}$	$0.461 + 0.007 \cdot \text{SL}$	$0.468 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.513	$0.493 + 0.010 \cdot \text{SL}$	$0.501 + 0.008 \cdot \text{SL}$	$0.512 + 0.007 \cdot \text{SL}$
SN to Q	$t_R$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.057 + 0.015 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.288	$0.270 + 0.009 \cdot \text{SL}$	$0.276 + 0.007 \cdot \text{SL}$	$0.282 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.291	$0.271 + 0.010 \cdot \text{SL}$	$0.278 + 0.008 \cdot \text{SL}$	$0.287 + 0.007 \cdot \text{SL}$
D to QN	$t_R$	0.106	$0.075 + 0.015 \cdot \text{SL}$	$0.077 + 0.015 \cdot \text{SL}$	$0.073 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.340	$0.319 + 0.010 \cdot \text{SL}$	$0.328 + 0.008 \cdot \text{SL}$	$0.342 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.312	$0.291 + 0.011 \cdot \text{SL}$	$0.299 + 0.009 \cdot \text{SL}$	$0.313 + 0.007 \cdot \text{SL}$
G to QN	$t_R$	0.105	$0.076 + 0.015 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$	$0.074 + 0.015 \cdot \text{SL}$
	$t_F$	0.090	$0.062 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.400	$0.380 + 0.010 \cdot \text{SL}$	$0.388 + 0.008 \cdot \text{SL}$	$0.402 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.378	$0.357 + 0.011 \cdot \text{SL}$	$0.366 + 0.009 \cdot \text{SL}$	$0.379 + 0.008 \cdot \text{SL}$
SN to QN	$t_R$	0.101	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.062 + 0.014 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.180	$0.160 + 0.010 \cdot \text{SL}$	$0.169 + 0.008 \cdot \text{SL}$	$0.182 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.192	$0.171 + 0.011 \cdot \text{SL}$	$0.180 + 0.009 \cdot \text{SL}$	$0.193 + 0.008 \cdot \text{SL}$

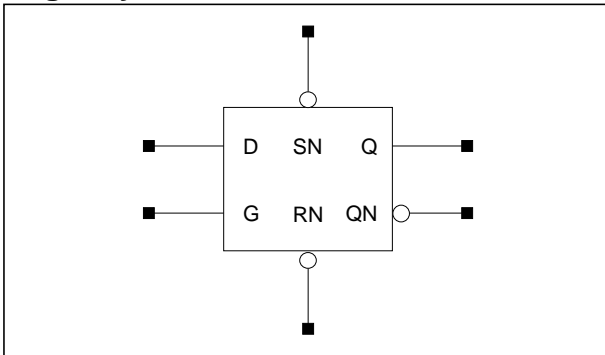
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## LD4/LD4D2

### D Latch with Active High, Reset, Set, 1X/2X Drive

#### Logic Symbol



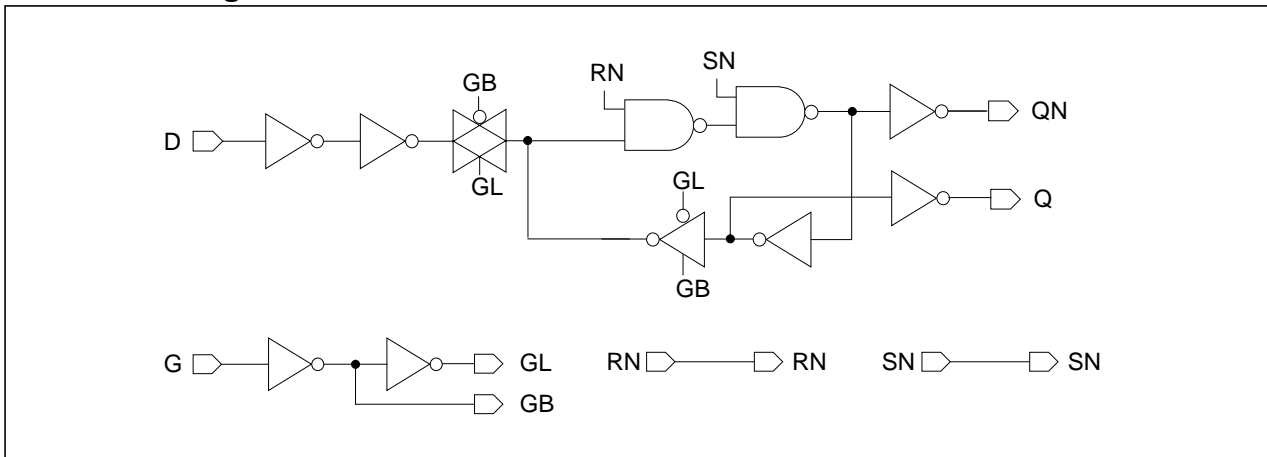
#### Truth Table

D	G	RN	SN	Q (n+1)	QN (n+1)
0	1	1	1	0	1
1	1	1	1	1	0
x	0	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

#### Cell Data

Input Load (SL)								Gate Count	
LD4				LD4D2				LD4	LD4D2
D	G	SN	RN	D	G	SN	RN		
0.6	0.5	0.8	0.8	0.6	0.5	0.8	0.8	6.00	6.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD4	LD4D2
Input Setup Time (D to G)	$t_{SU}$	0.320	0.341
Input Hold Time (D to G)	$t_{HD}$	0.015	0.007
Pulse Width High (G)	$t_{PWH}$	0.359	0.392
Pulse Width Low (SN)	$t_{PWL}$	0.501	0.520
Recovery Time (SN to G)	$t_{RC}$	0.000	0.000
Removal Time (SN to G)	$t_{RM}$	0.543	0.481
Pulse Width Low (RN)	$t_{PWL}$	0.304	0.350
Recovery Time (RN to G)	$t_{RC}$	0.019	0.058
Removal Time (RN to G)	$t_{RM}$	0.211	0.172
Recovery Time (SN to RN)	$t_{RC}$	0.343	0.405
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000



## LD4/LD4D2

### D Latch with Active High, Reset, Set, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### LD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.114	$0.058 + 0.028 \cdot \text{SL}$	$0.052 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$
	$t_F$	0.106	$0.056 + 0.025 \cdot \text{SL}$	$0.055 + 0.025 \cdot \text{SL}$	$0.050 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.514	$0.484 + 0.015 \cdot \text{SL}$	$0.489 + 0.013 \cdot \text{SL}$	$0.491 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.531	$0.498 + 0.016 \cdot \text{SL}$	$0.506 + 0.014 \cdot \text{SL}$	$0.511 + 0.014 \cdot \text{SL}$
G to Q	$t_R$	0.114	$0.058 + 0.028 \cdot \text{SL}$	$0.053 + 0.029 \cdot \text{SL}$	$0.048 + 0.030 \cdot \text{SL}$
	$t_F$	0.106	$0.056 + 0.025 \cdot \text{SL}$	$0.054 + 0.025 \cdot \text{SL}$	$0.050 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.523	$0.494 + 0.015 \cdot \text{SL}$	$0.499 + 0.013 \cdot \text{SL}$	$0.501 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.531	$0.498 + 0.016 \cdot \text{SL}$	$0.506 + 0.014 \cdot \text{SL}$	$0.510 + 0.014 \cdot \text{SL}$
SN to Q	$t_R$	0.114	$0.058 + 0.028 \cdot \text{SL}$	$0.053 + 0.029 \cdot \text{SL}$	$0.046 + 0.030 \cdot \text{SL}$
	$t_F$	0.106	$0.056 + 0.025 \cdot \text{SL}$	$0.056 + 0.025 \cdot \text{SL}$	$0.049 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.262	$0.233 + 0.015 \cdot \text{SL}$	$0.238 + 0.013 \cdot \text{SL}$	$0.240 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.261	$0.229 + 0.016 \cdot \text{SL}$	$0.237 + 0.014 \cdot \text{SL}$	$0.241 + 0.014 \cdot \text{SL}$
RN to Q	$t_R$	0.114	$0.058 + 0.028 \cdot \text{SL}$	$0.052 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$
	$t_F$	0.106	$0.057 + 0.025 \cdot \text{SL}$	$0.054 + 0.025 \cdot \text{SL}$	$0.050 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.310	$0.281 + 0.015 \cdot \text{SL}$	$0.286 + 0.013 \cdot \text{SL}$	$0.287 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.346	$0.314 + 0.016 \cdot \text{SL}$	$0.322 + 0.014 \cdot \text{SL}$	$0.326 + 0.014 \cdot \text{SL}$
D to QN	$t_R$	0.129	$0.068 + 0.030 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$	$0.065 + 0.031 \cdot \text{SL}$
	$t_F$	0.109	$0.058 + 0.026 \cdot \text{SL}$	$0.060 + 0.025 \cdot \text{SL}$	$0.056 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.447	$0.414 + 0.017 \cdot \text{SL}$	$0.422 + 0.015 \cdot \text{SL}$	$0.429 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.443	$0.409 + 0.017 \cdot \text{SL}$	$0.418 + 0.015 \cdot \text{SL}$	$0.425 + 0.014 \cdot \text{SL}$
G to QN	$t_R$	0.130	$0.069 + 0.030 \cdot \text{SL}$	$0.071 + 0.030 \cdot \text{SL}$	$0.065 + 0.031 \cdot \text{SL}$
	$t_F$	0.110	$0.059 + 0.026 \cdot \text{SL}$	$0.061 + 0.025 \cdot \text{SL}$	$0.055 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.447	$0.413 + 0.017 \cdot \text{SL}$	$0.422 + 0.015 \cdot \text{SL}$	$0.428 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.453	$0.419 + 0.017 \cdot \text{SL}$	$0.427 + 0.015 \cdot \text{SL}$	$0.435 + 0.014 \cdot \text{SL}$
SN to QN	$t_R$	0.134	$0.079 + 0.028 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$	$0.066 + 0.031 \cdot \text{SL}$
	$t_F$	0.112	$0.060 + 0.026 \cdot \text{SL}$	$0.065 + 0.025 \cdot \text{SL}$	$0.058 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.177	$0.144 + 0.017 \cdot \text{SL}$	$0.152 + 0.015 \cdot \text{SL}$	$0.159 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.192	$0.158 + 0.017 \cdot \text{SL}$	$0.167 + 0.015 \cdot \text{SL}$	$0.174 + 0.014 \cdot \text{SL}$
RN to QN	$t_R$	0.130	$0.070 + 0.030 \cdot \text{SL}$	$0.070 + 0.030 \cdot \text{SL}$	$0.065 + 0.031 \cdot \text{SL}$
	$t_F$	0.110	$0.058 + 0.026 \cdot \text{SL}$	$0.061 + 0.025 \cdot \text{SL}$	$0.056 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.229 + 0.017 \cdot \text{SL}$	$0.238 + 0.015 \cdot \text{SL}$	$0.245 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.206 + 0.017 \cdot \text{SL}$	$0.214 + 0.015 \cdot \text{SL}$	$0.222 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## D Latch with Active High, Reset, Set, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ ns}$ , SL: Standard Load)

## LD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.088	$0.059 + 0.014 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.551	$0.533 + 0.009 \cdot \text{SL}$	$0.540 + 0.007 \cdot \text{SL}$	$0.547 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.574	$0.553 + 0.010 \cdot \text{SL}$	$0.561 + 0.008 \cdot \text{SL}$	$0.573 + 0.007 \cdot \text{SL}$
G to Q	$t_R$	0.088	$0.061 + 0.013 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.561	$0.543 + 0.009 \cdot \text{SL}$	$0.550 + 0.007 \cdot \text{SL}$	$0.557 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.574	$0.553 + 0.010 \cdot \text{SL}$	$0.561 + 0.008 \cdot \text{SL}$	$0.573 + 0.007 \cdot \text{SL}$
SN to Q	$t_R$	0.089	$0.060 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.298	$0.280 + 0.009 \cdot \text{SL}$	$0.287 + 0.007 \cdot \text{SL}$	$0.294 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.303	$0.282 + 0.010 \cdot \text{SL}$	$0.291 + 0.008 \cdot \text{SL}$	$0.302 + 0.007 \cdot \text{SL}$
RN to Q	$t_R$	0.089	$0.060 + 0.014 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.061 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.346	$0.329 + 0.009 \cdot \text{SL}$	$0.335 + 0.007 \cdot \text{SL}$	$0.343 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.389	$0.368 + 0.010 \cdot \text{SL}$	$0.376 + 0.008 \cdot \text{SL}$	$0.388 + 0.007 \cdot \text{SL}$
D to QN	$t_R$	0.100	$0.070 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.451	$0.431 + 0.010 \cdot \text{SL}$	$0.439 + 0.008 \cdot \text{SL}$	$0.453 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.445	$0.424 + 0.011 \cdot \text{SL}$	$0.433 + 0.008 \cdot \text{SL}$	$0.447 + 0.007 \cdot \text{SL}$
G to QN	$t_R$	0.100	$0.068 + 0.016 \cdot \text{SL}$	$0.073 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.058 + 0.014 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.451	$0.431 + 0.010 \cdot \text{SL}$	$0.439 + 0.008 \cdot \text{SL}$	$0.453 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.455	$0.434 + 0.011 \cdot \text{SL}$	$0.443 + 0.008 \cdot \text{SL}$	$0.457 + 0.007 \cdot \text{SL}$
SN to QN	$t_R$	0.100	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.181	$0.160 + 0.010 \cdot \text{SL}$	$0.169 + 0.008 \cdot \text{SL}$	$0.182 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.193	$0.171 + 0.011 \cdot \text{SL}$	$0.181 + 0.008 \cdot \text{SL}$	$0.195 + 0.007 \cdot \text{SL}$
RN to QN	$t_R$	0.100	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.060 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.266	$0.246 + 0.010 \cdot \text{SL}$	$0.254 + 0.008 \cdot \text{SL}$	$0.268 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.242	$0.220 + 0.011 \cdot \text{SL}$	$0.229 + 0.008 \cdot \text{SL}$	$0.243 + 0.007 \cdot \text{SL}$

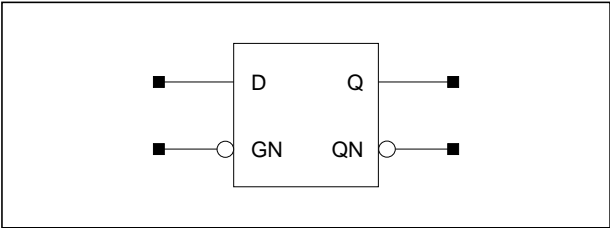
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# LD5/LD5D2

## D Latch with Active Low, 1X/2X Drive

### Logic Symbol



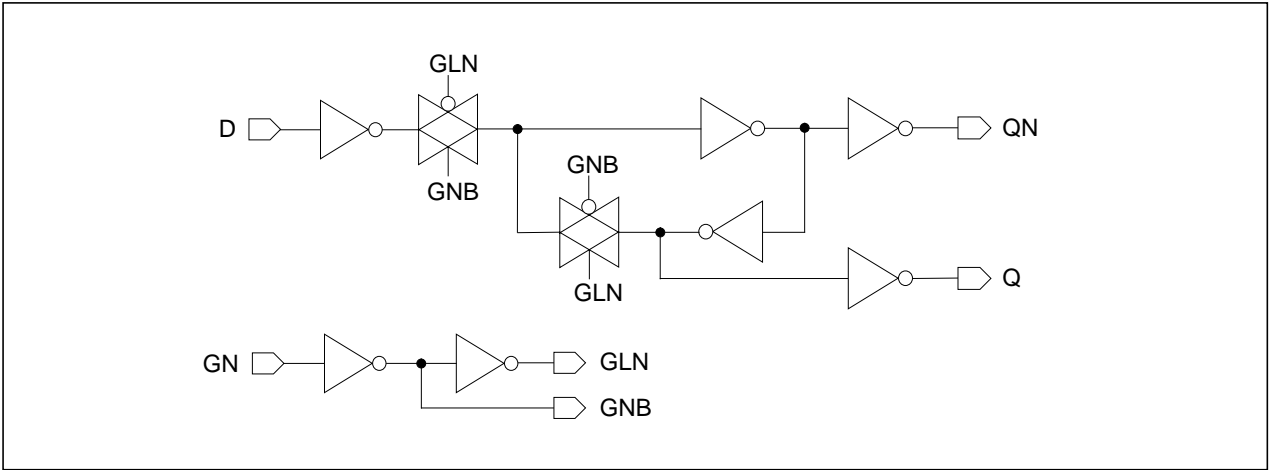
### Truth Table

D	GN	Q (n+1)	QN (n+1)
0	0	0	1
1	0	1	0
x	1	Q (n)	QN (n)

### Cell Data

Input Load (SL)				Gate Count	
LD5		LD5D2		LD5	LD5D2
D	GN	D	GN		
0.6	0.6	0.6	0.6	4.00	4.33

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD5	LD5D2
Input Setup Time (D to GN)	t <sub>SU</sub>	0.315	0.326
Input Hold Time (D to GN)	t <sub>HD</sub>	0.000	0.000
Pulse Width Low (GN)	t <sub>PWL</sub>	0.285	0.304



## D Latch with Active Low, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ ns}$ , SL: Standard Load)

## LD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.112	$0.054 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.105	$0.053 + 0.026 \cdot \text{SL}$	$0.049 + 0.027 \cdot \text{SL}$	$0.044 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.355	$0.325 + 0.015 \cdot \text{SL}$	$0.330 + 0.014 \cdot \text{SL}$	$0.330 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.377	$0.344 + 0.017 \cdot \text{SL}$	$0.350 + 0.015 \cdot \text{SL}$	$0.353 + 0.015 \cdot \text{SL}$
GN to Q	$t_R$	0.112	$0.054 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.105	$0.053 + 0.026 \cdot \text{SL}$	$0.049 + 0.027 \cdot \text{SL}$	$0.043 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.416	$0.386 + 0.015 \cdot \text{SL}$	$0.391 + 0.014 \cdot \text{SL}$	$0.391 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.469	$0.436 + 0.017 \cdot \text{SL}$	$0.443 + 0.015 \cdot \text{SL}$	$0.446 + 0.015 \cdot \text{SL}$
D to QN	$t_R$	0.122	$0.065 + 0.029 \cdot \text{SL}$	$0.061 + 0.030 \cdot \text{SL}$	$0.054 + 0.031 \cdot \text{SL}$
	$t_F$	0.114	$0.060 + 0.027 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$	$0.056 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.303	$0.272 + 0.015 \cdot \text{SL}$	$0.278 + 0.014 \cdot \text{SL}$	$0.281 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.301	$0.265 + 0.018 \cdot \text{SL}$	$0.274 + 0.016 \cdot \text{SL}$	$0.281 + 0.015 \cdot \text{SL}$
GN to QN	$t_R$	0.122	$0.065 + 0.029 \cdot \text{SL}$	$0.060 + 0.030 \cdot \text{SL}$	$0.053 + 0.031 \cdot \text{SL}$
	$t_F$	0.114	$0.061 + 0.027 \cdot \text{SL}$	$0.060 + 0.027 \cdot \text{SL}$	$0.056 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.395	$0.364 + 0.015 \cdot \text{SL}$	$0.370 + 0.014 \cdot \text{SL}$	$0.373 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.362	$0.326 + 0.018 \cdot \text{SL}$	$0.335 + 0.016 \cdot \text{SL}$	$0.342 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ 

## LD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$
	$t_F$	0.081	$0.053 + 0.014 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.049 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.392	$0.375 + 0.009 \cdot \text{SL}$	$0.381 + 0.007 \cdot \text{SL}$	$0.387 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.412	$0.392 + 0.010 \cdot \text{SL}$	$0.400 + 0.008 \cdot \text{SL}$	$0.410 + 0.007 \cdot \text{SL}$
GN to Q	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.045 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.053 + 0.014 \cdot \text{SL}$	$0.055 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.451	$0.433 + 0.009 \cdot \text{SL}$	$0.439 + 0.007 \cdot \text{SL}$	$0.445 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.497	$0.477 + 0.010 \cdot \text{SL}$	$0.485 + 0.008 \cdot \text{SL}$	$0.495 + 0.007 \cdot \text{SL}$
D to QN	$t_R$	0.092	$0.063 + 0.015 \cdot \text{SL}$	$0.064 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.060 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.309	$0.291 + 0.009 \cdot \text{SL}$	$0.298 + 0.007 \cdot \text{SL}$	$0.306 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.300	$0.279 + 0.010 \cdot \text{SL}$	$0.288 + 0.008 \cdot \text{SL}$	$0.300 + 0.007 \cdot \text{SL}$
GN to QN	$t_R$	0.093	$0.066 + 0.014 \cdot \text{SL}$	$0.063 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.394	$0.376 + 0.009 \cdot \text{SL}$	$0.383 + 0.007 \cdot \text{SL}$	$0.391 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.359	$0.338 + 0.010 \cdot \text{SL}$	$0.347 + 0.008 \cdot \text{SL}$	$0.359 + 0.007 \cdot \text{SL}$

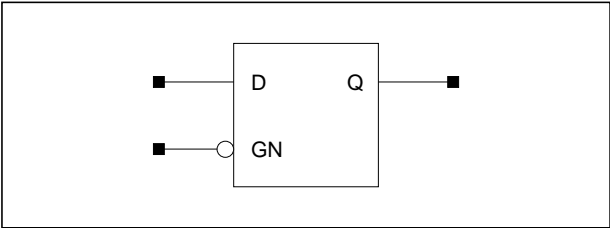
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# LD5Q/LD5QD2

## D Latch with Active Low,Q Output Only, 1X/2X Drive

### Logic Symbol



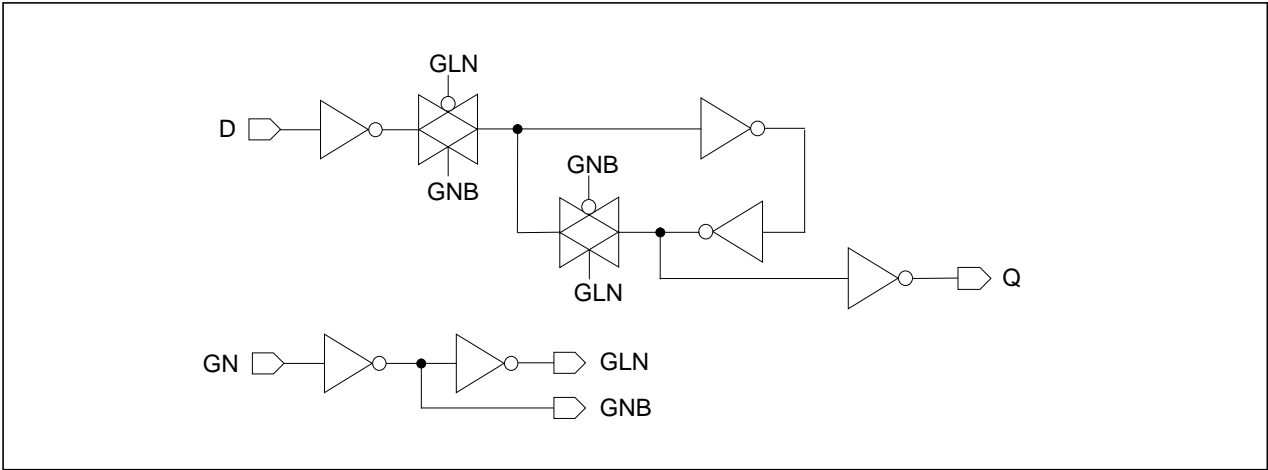
### Truth Table

D	GN	Q (n+1)
0	0	0
1	0	1
x	1	Q (n)

### Cell Data

Input Load (SL)				Gate Count	
LD5Q		LD5QD2		LD5Q	LD5QD2
D	GN	D	GN		
0.6	0.6	0.6	0.6	3.33	3.67

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD5Q	LD5QD2
Input Setup Time (D to GN)	t <sub>SU</sub>	0.295	0.293
Input Hold Time (D to GN)	t <sub>HD</sub>	0.000	0.000
Pulse Width Low (GN)	t <sub>PWL</sub>	0.267	0.269



**D Latch with Active Low, Q Output Only, 1X/2X Drive****Switching Characteristics**(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ ns}$ , SL: Standard Load)**LD5Q**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.110	$0.052 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.102	$0.048 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$	$0.042 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.321	$0.293 + 0.014 \cdot \text{SL}$	$0.296 + 0.014 \cdot \text{SL}$	$0.297 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.341	$0.308 + 0.016 \cdot \text{SL}$	$0.314 + 0.015 \cdot \text{SL}$	$0.317 + 0.014 \cdot \text{SL}$
GN to Q	$t_R$	0.110	$0.052 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$	$0.043 + 0.031 \cdot \text{SL}$
	$t_F$	0.103	$0.051 + 0.026 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$	$0.042 + 0.028 \cdot \text{SL}$
	$t_{PLH}$	0.382	$0.353 + 0.014 \cdot \text{SL}$	$0.356 + 0.014 \cdot \text{SL}$	$0.357 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.428	$0.395 + 0.016 \cdot \text{SL}$	$0.402 + 0.015 \cdot \text{SL}$	$0.404 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$ **LD5QD2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.079	$0.050 + 0.015 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$	$0.042 + 0.015 \cdot \text{SL}$
	$t_F$	0.076	$0.047 + 0.014 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$	$0.046 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.322	$0.305 + 0.009 \cdot \text{SL}$	$0.310 + 0.007 \cdot \text{SL}$	$0.316 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.340	$0.320 + 0.010 \cdot \text{SL}$	$0.328 + 0.008 \cdot \text{SL}$	$0.338 + 0.007 \cdot \text{SL}$
GN to Q	$t_R$	0.079	$0.049 + 0.015 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$	$0.041 + 0.015 \cdot \text{SL}$
	$t_F$	0.075	$0.046 + 0.014 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$	$0.046 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.380	$0.363 + 0.009 \cdot \text{SL}$	$0.369 + 0.007 \cdot \text{SL}$	$0.374 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.426	$0.406 + 0.010 \cdot \text{SL}$	$0.413 + 0.008 \cdot \text{SL}$	$0.423 + 0.007 \cdot \text{SL}$

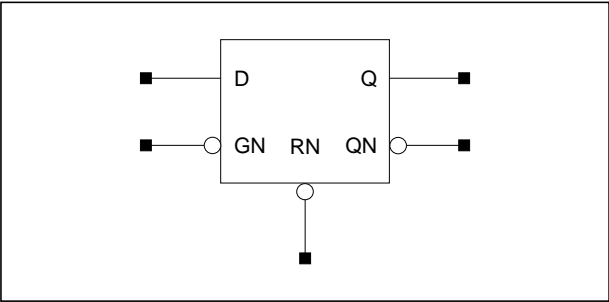
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



LD6/LD6D2

D Latch with Active Low, Reset, 1X/2X Drive

Logic Symbol



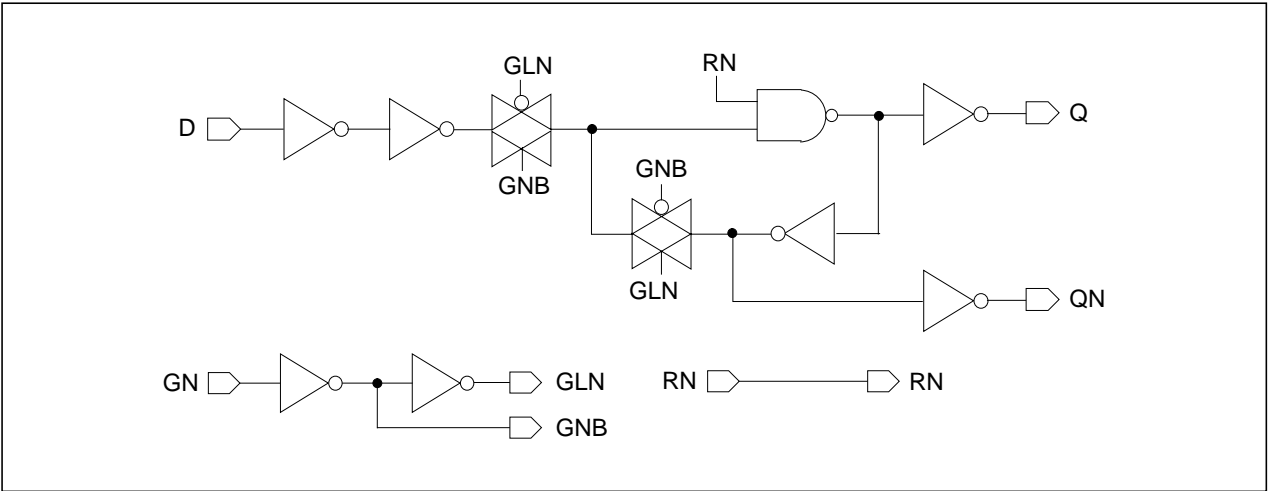
Truth Table

D	GN	RN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
LD6			LD6D2			LD6	LD6D2
D	GN	RN	D	GN	RN		
0.6	0.6	0.8	0.6	0.6	0.8	4.67	5.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD6	LD6D2
Input Setup Time (D to GN)	t <sub>SU</sub>	0.394	0.411
Input Hold Time (D to GN)	t <sub>HD</sub>	0.000	0.000
Pulse Width Low (GN)	t <sub>PWL</sub>	0.296	0.324
Pulse Width Low (RN)	t <sub>PWL</sub>	0.251	0.287
Recovery Time (RN to GN)	t <sub>RC</sub>	0.000	0.033
Removal Time (RN to GN)	t <sub>RM</sub>	0.241	0.188



## D Latch with Active Low, Reset, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

## LD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.134	$0.075 + 0.030 \cdot \text{SL}$	$0.074 + 0.030 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.115	$0.062 + 0.027 \cdot \text{SL}$	$0.062 + 0.027 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.378	$0.344 + 0.017 \cdot \text{SL}$	$0.353 + 0.015 \cdot \text{SL}$	$0.360 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.376	$0.341 + 0.018 \cdot \text{SL}$	$0.350 + 0.016 \cdot \text{SL}$	$0.357 + 0.015 \cdot \text{SL}$
GN to Q	$t_R$	0.134	$0.075 + 0.029 \cdot \text{SL}$	$0.073 + 0.030 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.114	$0.059 + 0.027 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.422	$0.388 + 0.017 \cdot \text{SL}$	$0.397 + 0.015 \cdot \text{SL}$	$0.404 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.372	$0.337 + 0.018 \cdot \text{SL}$	$0.345 + 0.016 \cdot \text{SL}$	$0.353 + 0.015 \cdot \text{SL}$
RN to Q	$t_R$	0.131	$0.071 + 0.030 \cdot \text{SL}$	$0.070 + 0.030 \cdot \text{SL}$	$0.066 + 0.031 \cdot \text{SL}$
	$t_F$	0.115	$0.061 + 0.027 \cdot \text{SL}$	$0.064 + 0.026 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.175	$0.142 + 0.017 \cdot \text{SL}$	$0.150 + 0.015 \cdot \text{SL}$	$0.157 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.156 + 0.018 \cdot \text{SL}$	$0.165 + 0.015 \cdot \text{SL}$	$0.172 + 0.015 \cdot \text{SL}$
D to QN	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.107	$0.056 + 0.026 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$	$0.046 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.434	$0.405 + 0.015 \cdot \text{SL}$	$0.410 + 0.013 \cdot \text{SL}$	$0.411 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.455	$0.422 + 0.017 \cdot \text{SL}$	$0.429 + 0.015 \cdot \text{SL}$	$0.433 + 0.014 \cdot \text{SL}$
GN to QN	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.106	$0.053 + 0.027 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.430	$0.401 + 0.015 \cdot \text{SL}$	$0.405 + 0.014 \cdot \text{SL}$	$0.406 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.500	$0.466 + 0.017 \cdot \text{SL}$	$0.473 + 0.015 \cdot \text{SL}$	$0.477 + 0.014 \cdot \text{SL}$
RN to QN	$t_R$	0.112	$0.054 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.107	$0.056 + 0.026 \cdot \text{SL}$	$0.052 + 0.027 \cdot \text{SL}$	$0.046 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.250	$0.220 + 0.015 \cdot \text{SL}$	$0.225 + 0.014 \cdot \text{SL}$	$0.226 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.253	$0.219 + 0.017 \cdot \text{SL}$	$0.226 + 0.015 \cdot \text{SL}$	$0.230 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## LD6/LD6D2

### D Latch with Active Low, Reset, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### LD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.105	$0.075 + 0.015 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$	$0.072 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.384	$0.363 + 0.010 \cdot \text{SL}$	$0.372 + 0.008 \cdot \text{SL}$	$0.385 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.377	$0.355 + 0.011 \cdot \text{SL}$	$0.364 + 0.009 \cdot \text{SL}$	$0.378 + 0.008 \cdot \text{SL}$
GN to Q	$t_R$	0.105	$0.075 + 0.015 \cdot \text{SL}$	$0.075 + 0.015 \cdot \text{SL}$	$0.074 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.428	$0.407 + 0.010 \cdot \text{SL}$	$0.416 + 0.008 \cdot \text{SL}$	$0.429 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.372	$0.351 + 0.011 \cdot \text{SL}$	$0.360 + 0.009 \cdot \text{SL}$	$0.373 + 0.008 \cdot \text{SL}$
RN to Q	$t_R$	0.100	$0.069 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$	$0.069 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.060 + 0.015 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.178	$0.157 + 0.010 \cdot \text{SL}$	$0.166 + 0.008 \cdot \text{SL}$	$0.179 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.188	$0.167 + 0.011 \cdot \text{SL}$	$0.175 + 0.009 \cdot \text{SL}$	$0.189 + 0.008 \cdot \text{SL}$
D to QN	$t_R$	0.085	$0.058 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.473	$0.455 + 0.009 \cdot \text{SL}$	$0.461 + 0.007 \cdot \text{SL}$	$0.467 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.498	$0.478 + 0.010 \cdot \text{SL}$	$0.486 + 0.008 \cdot \text{SL}$	$0.497 + 0.007 \cdot \text{SL}$
GN to QN	$t_R$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.055 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.468	$0.450 + 0.009 \cdot \text{SL}$	$0.456 + 0.007 \cdot \text{SL}$	$0.463 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.542	$0.522 + 0.010 \cdot \text{SL}$	$0.530 + 0.008 \cdot \text{SL}$	$0.541 + 0.007 \cdot \text{SL}$
RN to QN	$t_R$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.055 + 0.015 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.283	$0.266 + 0.009 \cdot \text{SL}$	$0.272 + 0.007 \cdot \text{SL}$	$0.278 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.289	$0.270 + 0.010 \cdot \text{SL}$	$0.276 + 0.008 \cdot \text{SL}$	$0.287 + 0.007 \cdot \text{SL}$

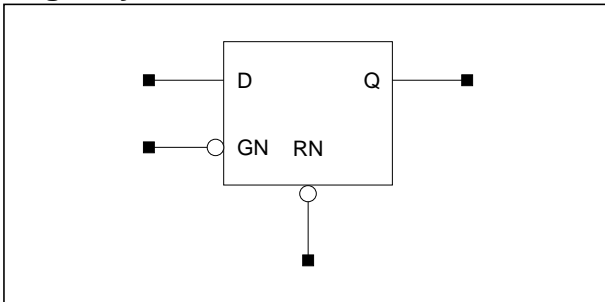
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## LD6Q/LD6QD2

### D Latch with Active Low, Reset, Q Output Only, 1X/2X Drive

#### Logic Symbol



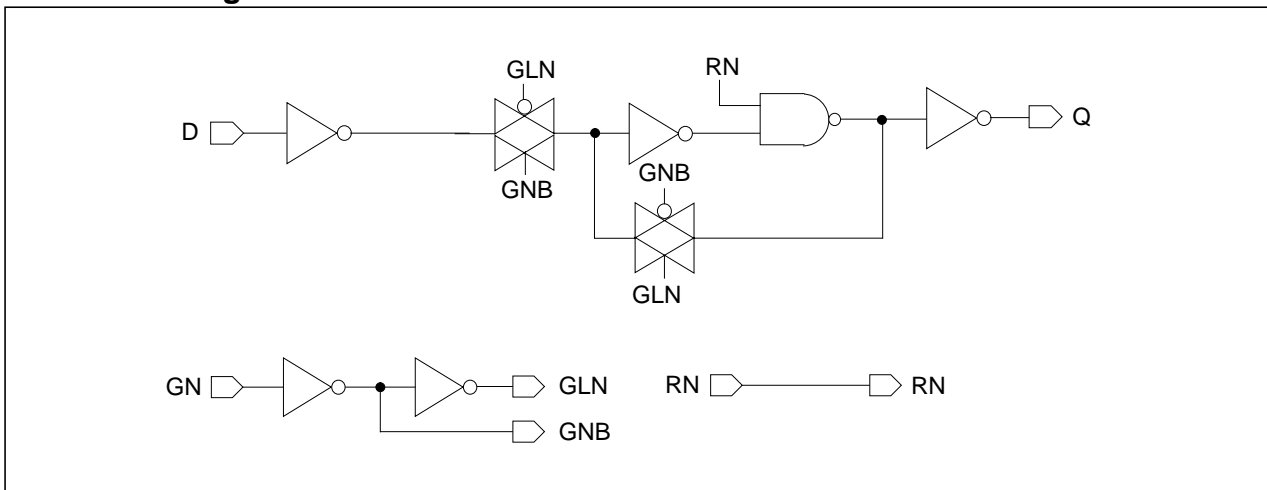
#### Truth Table

D	GN	RN	Q (n+1)
0	0	1	0
1	0	1	1
x	1	1	Q (n)
x	x	0	0

#### Cell Data

Input Load (SL)						Gate Count	
LD6Q			LD6QD2			LD6Q	LD6QD2
D	GN	RN	D	GN	RN		
0.6	0.6	0.8	0.6	0.6	0.8	4.00	4.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD6Q	LD6QD2
Input Setup Time (D to GN)	$t_{SU}$	0.303	0.300
Input Hold Time (D to GN)	$t_{HD}$	0.000	0.000
Pulse Width Low (GN)	$t_{PWL}$	0.273	0.275
Pulse Width Low (RN)	$t_{PWL}$	0.250	0.271
Recovery Time (RN to GN)	$t_{RC}$	0.000	0.000
Removal Time (RN to GN)	$t_{RM}$	0.489	0.448



## LD6Q/LD6QD2

### D Latch with Active Low, Reset, Q Output Only, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### LD6Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.125	$0.067 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$	$0.059 + 0.030 \cdot \text{SL}$
	$t_F$	0.105	$0.055 + 0.025 \cdot \text{SL}$	$0.053 + 0.025 \cdot \text{SL}$	$0.048 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.358	$0.326 + 0.016 \cdot \text{SL}$	$0.333 + 0.014 \cdot \text{SL}$	$0.338 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.357	$0.325 + 0.016 \cdot \text{SL}$	$0.332 + 0.014 \cdot \text{SL}$	$0.337 + 0.014 \cdot \text{SL}$
GN to Q	$t_R$	0.125	$0.067 + 0.029 \cdot \text{SL}$	$0.064 + 0.030 \cdot \text{SL}$	$0.059 + 0.030 \cdot \text{SL}$
	$t_F$	0.104	$0.054 + 0.025 \cdot \text{SL}$	$0.053 + 0.025 \cdot \text{SL}$	$0.047 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.420	$0.388 + 0.016 \cdot \text{SL}$	$0.395 + 0.014 \cdot \text{SL}$	$0.400 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.445	$0.413 + 0.016 \cdot \text{SL}$	$0.420 + 0.014 \cdot \text{SL}$	$0.424 + 0.014 \cdot \text{SL}$
RN to Q	$t_R$	0.129	$0.074 + 0.028 \cdot \text{SL}$	$0.065 + 0.030 \cdot \text{SL}$	$0.060 + 0.030 \cdot \text{SL}$
	$t_F$	0.108	$0.057 + 0.025 \cdot \text{SL}$	$0.059 + 0.025 \cdot \text{SL}$	$0.053 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.167	$0.135 + 0.016 \cdot \text{SL}$	$0.143 + 0.014 \cdot \text{SL}$	$0.148 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.179	$0.146 + 0.016 \cdot \text{SL}$	$0.155 + 0.014 \cdot \text{SL}$	$0.159 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

#### LD6QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.096	$0.065 + 0.015 \cdot \text{SL}$	$0.068 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.078	$0.050 + 0.014 \cdot \text{SL}$	$0.057 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.363	$0.344 + 0.010 \cdot \text{SL}$	$0.351 + 0.008 \cdot \text{SL}$	$0.364 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.357	$0.337 + 0.010 \cdot \text{SL}$	$0.345 + 0.008 \cdot \text{SL}$	$0.357 + 0.007 \cdot \text{SL}$
GN to Q	$t_R$	0.096	$0.066 + 0.015 \cdot \text{SL}$	$0.068 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.078	$0.050 + 0.014 \cdot \text{SL}$	$0.057 + 0.012 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.423	$0.404 + 0.010 \cdot \text{SL}$	$0.411 + 0.008 \cdot \text{SL}$	$0.424 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.443	$0.423 + 0.010 \cdot \text{SL}$	$0.431 + 0.008 \cdot \text{SL}$	$0.443 + 0.007 \cdot \text{SL}$
RN to Q	$t_R$	0.097	$0.068 + 0.015 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$	$0.064 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.057 + 0.013 \cdot \text{SL}$	$0.059 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.173	$0.153 + 0.010 \cdot \text{SL}$	$0.161 + 0.008 \cdot \text{SL}$	$0.173 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.179	$0.159 + 0.010 \cdot \text{SL}$	$0.167 + 0.008 \cdot \text{SL}$	$0.179 + 0.007 \cdot \text{SL}$

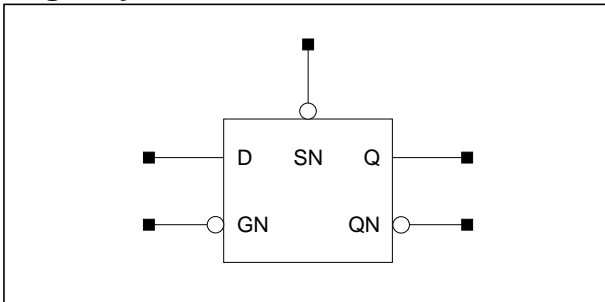
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## LD7/LD7D2

### D Latch with Active Low, Set, 1X/2X Drive

#### Logic Symbol



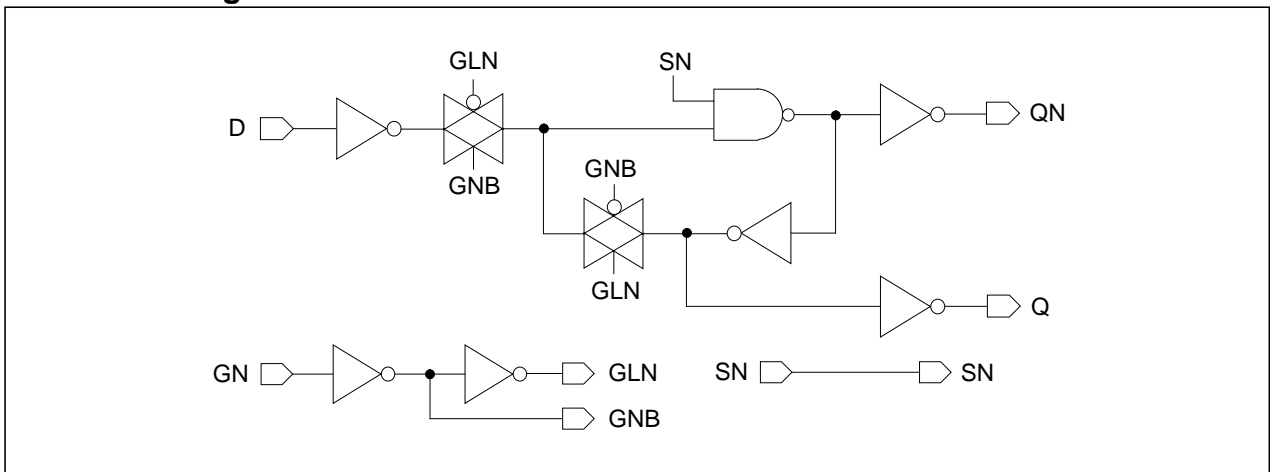
#### Truth Table

D	GN	SN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	1	0

#### Cell Data

Input Load (SL)						Gate Count	
LD7			LD7D2			LD7	LD7D2
D	GN	SN	D	GN	SN		
0.6	0.6	0.8	0.6	0.6	0.8	4.33	4.67

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD7	LD7D2
Input Setup Time (D to GN)	$t_{SU}$	0.315	0.333
Input Hold Time (D to GN)	$t_{HD}$	0.000	0.000
Pulse Width Low (GN)	$t_{PWL}$	0.298	0.325
Pulse Width Low (SN)	$t_{PWL}$	0.250	0.290
Recovery Time (SN to GN)	$t_{RC}$	0.000	0.046
Removal Time (SN to GN)	$t_{RM}$	0.226	0.174



## LD7/LD7D2

### D Latch with Active Low, Set, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### LD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.108	$0.056 + 0.026 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.046 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.367	$0.338 + 0.015 \cdot \text{SL}$	$0.342 + 0.014 \cdot \text{SL}$	$0.343 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.414	$0.381 + 0.017 \cdot \text{SL}$	$0.388 + 0.015 \cdot \text{SL}$	$0.391 + 0.014 \cdot \text{SL}$
GN to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.106	$0.052 + 0.027 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.424	$0.395 + 0.015 \cdot \text{SL}$	$0.399 + 0.014 \cdot \text{SL}$	$0.400 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.501	$0.468 + 0.017 \cdot \text{SL}$	$0.475 + 0.015 \cdot \text{SL}$	$0.478 + 0.014 \cdot \text{SL}$
SN to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.049 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.105	$0.051 + 0.027 \cdot \text{SL}$	$0.053 + 0.027 \cdot \text{SL}$	$0.047 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.249	$0.219 + 0.015 \cdot \text{SL}$	$0.224 + 0.014 \cdot \text{SL}$	$0.225 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.256	$0.223 + 0.017 \cdot \text{SL}$	$0.230 + 0.015 \cdot \text{SL}$	$0.233 + 0.014 \cdot \text{SL}$
D to QN	$t_R$	0.135	$0.075 + 0.030 \cdot \text{SL}$	$0.076 + 0.029 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.114	$0.060 + 0.027 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.335	$0.301 + 0.017 \cdot \text{SL}$	$0.310 + 0.015 \cdot \text{SL}$	$0.317 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.310	$0.275 + 0.018 \cdot \text{SL}$	$0.283 + 0.016 \cdot \text{SL}$	$0.291 + 0.015 \cdot \text{SL}$
GN to QN	$t_R$	0.134	$0.075 + 0.030 \cdot \text{SL}$	$0.076 + 0.029 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$
	$t_F$	0.115	$0.061 + 0.027 \cdot \text{SL}$	$0.064 + 0.026 \cdot \text{SL}$	$0.057 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.422	$0.388 + 0.017 \cdot \text{SL}$	$0.397 + 0.015 \cdot \text{SL}$	$0.404 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.367	$0.332 + 0.018 \cdot \text{SL}$	$0.340 + 0.016 \cdot \text{SL}$	$0.348 + 0.015 \cdot \text{SL}$
SN to QN	$t_R$	0.131	$0.072 + 0.029 \cdot \text{SL}$	$0.070 + 0.030 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$
	$t_F$	0.115	$0.061 + 0.027 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.177	$0.144 + 0.017 \cdot \text{SL}$	$0.152 + 0.015 \cdot \text{SL}$	$0.159 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.191	$0.156 + 0.018 \cdot \text{SL}$	$0.164 + 0.015 \cdot \text{SL}$	$0.172 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

## LD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.086	$0.057 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.053 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.406	$0.389 + 0.009 \cdot \text{SL}$	$0.395 + 0.007 \cdot \text{SL}$	$0.401 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.453	$0.433 + 0.010 \cdot \text{SL}$	$0.441 + 0.008 \cdot \text{SL}$	$0.452 + 0.007 \cdot \text{SL}$
GN to Q	$t_R$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.084	$0.056 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.466	$0.449 + 0.009 \cdot \text{SL}$	$0.455 + 0.007 \cdot \text{SL}$	$0.461 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.539	$0.519 + 0.010 \cdot \text{SL}$	$0.527 + 0.008 \cdot \text{SL}$	$0.537 + 0.007 \cdot \text{SL}$
SN to Q	$t_R$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.056 + 0.015 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.056 + 0.015 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.287	$0.270 + 0.009 \cdot \text{SL}$	$0.276 + 0.007 \cdot \text{SL}$	$0.282 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.290	$0.271 + 0.010 \cdot \text{SL}$	$0.278 + 0.008 \cdot \text{SL}$	$0.287 + 0.007 \cdot \text{SL}$
D to QN	$t_R$	0.106	$0.075 + 0.015 \cdot \text{SL}$	$0.077 + 0.015 \cdot \text{SL}$	$0.073 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.060 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.340	$0.320 + 0.010 \cdot \text{SL}$	$0.328 + 0.008 \cdot \text{SL}$	$0.342 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.312	$0.291 + 0.011 \cdot \text{SL}$	$0.300 + 0.009 \cdot \text{SL}$	$0.313 + 0.007 \cdot \text{SL}$
GN to QN	$t_R$	0.106	$0.076 + 0.015 \cdot \text{SL}$	$0.077 + 0.015 \cdot \text{SL}$	$0.074 + 0.015 \cdot \text{SL}$
	$t_F$	0.089	$0.062 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.426	$0.405 + 0.010 \cdot \text{SL}$	$0.414 + 0.008 \cdot \text{SL}$	$0.428 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.372	$0.350 + 0.011 \cdot \text{SL}$	$0.359 + 0.009 \cdot \text{SL}$	$0.372 + 0.007 \cdot \text{SL}$
SN to QN	$t_R$	0.101	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.062 + 0.014 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.180	$0.160 + 0.010 \cdot \text{SL}$	$0.168 + 0.008 \cdot \text{SL}$	$0.181 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.192	$0.170 + 0.011 \cdot \text{SL}$	$0.179 + 0.009 \cdot \text{SL}$	$0.193 + 0.008 \cdot \text{SL}$

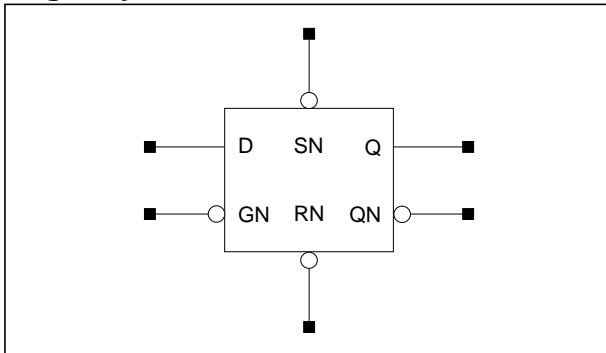
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## LD8/LD8D2

### D Latch with Active Low, Reset, Set, 1X/2X Drive

#### Logic Symbol



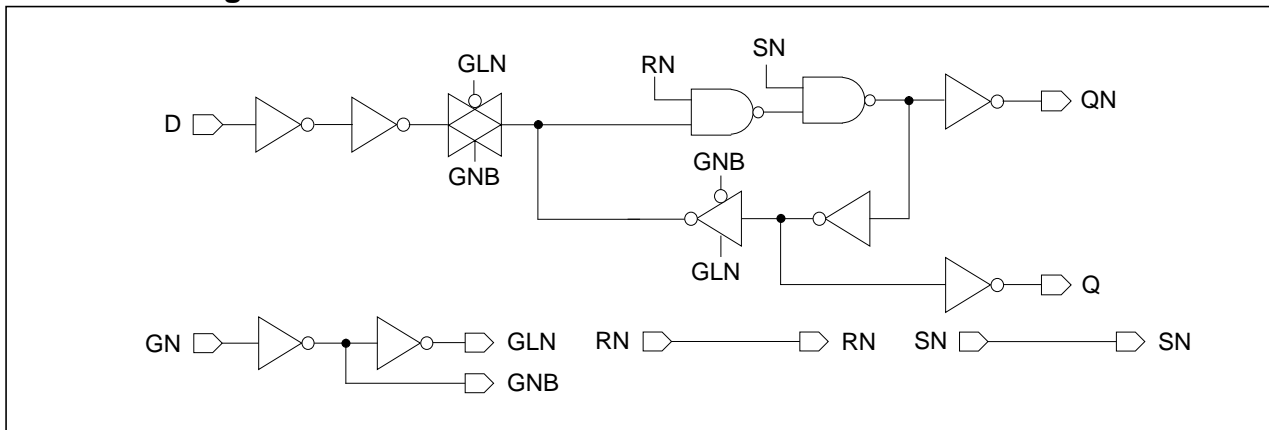
#### Truth Table

D	GN	RN	SN	Q (n+1)	QN (n+1)
0	0	1	1	0	1
1	0	1	1	1	0
x	1	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

#### Cell Data

Input Load (SL)								Gate Count	
LD8				LD8D2				LD8	LD8D2
D	GN	SN	RN	D	GN	SN	RN		
0.6	0.6	0.8	0.8	0.6	0.6	0.8	0.8	6.00	6.33

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD8	LD8D2
Input Setup Time (D to GN)	$t_{SU}$	0.410	0.314
Input Hold Time (D to GN)	$t_{HD}$	0.000	0.000
Pulse Width Low (GN)	$t_{PWL}$	0.329	0.357
Pulse Width Low (SN)	$t_{PWL}$	0.503	0.519
Recovery Time (SN to GN)	$t_{RC}$	0.000	0.000
Removal Time (SN to GN)	$t_{RM}$	0.405	0.338
Pulse Width Low (RN)	$t_{PWL}$	0.304	0.353
Recovery Time (RN to GN)	$t_{RC}$	0.028	0.067
Removal Time (RN to GN)	$t_{RM}$	0.196	0.157
Recovery Time (SN to RN)	$t_{RC}$	0.345	0.408
Removal Time (SN to RN)	$t_{RM}$	0.000	0.000



## D Latch with Active Low, Reset, Set, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ ns}$ , SL: Standard Load)

## LD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.114	$0.058 + 0.028 \cdot \text{SL}$	$0.053 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$
	$t_F$	0.105	$0.056 + 0.025 \cdot \text{SL}$	$0.054 + 0.025 \cdot \text{SL}$	$0.049 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.515	$0.485 + 0.015 \cdot \text{SL}$	$0.490 + 0.013 \cdot \text{SL}$	$0.492 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.532	$0.499 + 0.016 \cdot \text{SL}$	$0.507 + 0.014 \cdot \text{SL}$	$0.512 + 0.014 \cdot \text{SL}$
GN to Q	$t_R$	0.114	$0.058 + 0.028 \cdot \text{SL}$	$0.052 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$
	$t_F$	0.105	$0.055 + 0.025 \cdot \text{SL}$	$0.053 + 0.025 \cdot \text{SL}$	$0.050 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.553	$0.524 + 0.015 \cdot \text{SL}$	$0.529 + 0.013 \cdot \text{SL}$	$0.531 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.520	$0.488 + 0.016 \cdot \text{SL}$	$0.496 + 0.014 \cdot \text{SL}$	$0.500 + 0.014 \cdot \text{SL}$
SN to Q	$t_R$	0.114	$0.058 + 0.028 \cdot \text{SL}$	$0.052 + 0.029 \cdot \text{SL}$	$0.046 + 0.030 \cdot \text{SL}$
	$t_F$	0.105	$0.054 + 0.026 \cdot \text{SL}$	$0.056 + 0.025 \cdot \text{SL}$	$0.049 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.233 + 0.015 \cdot \text{SL}$	$0.238 + 0.013 \cdot \text{SL}$	$0.240 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.262	$0.229 + 0.016 \cdot \text{SL}$	$0.237 + 0.014 \cdot \text{SL}$	$0.241 + 0.014 \cdot \text{SL}$
RN to Q	$t_R$	0.114	$0.058 + 0.028 \cdot \text{SL}$	$0.052 + 0.029 \cdot \text{SL}$	$0.047 + 0.030 \cdot \text{SL}$
	$t_F$	0.106	$0.057 + 0.025 \cdot \text{SL}$	$0.054 + 0.025 \cdot \text{SL}$	$0.050 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.310	$0.281 + 0.015 \cdot \text{SL}$	$0.286 + 0.013 \cdot \text{SL}$	$0.288 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.346	$0.314 + 0.016 \cdot \text{SL}$	$0.322 + 0.014 \cdot \text{SL}$	$0.326 + 0.014 \cdot \text{SL}$
D to QN	$t_R$	0.129	$0.069 + 0.030 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$
	$t_F$	0.110	$0.058 + 0.026 \cdot \text{SL}$	$0.061 + 0.025 \cdot \text{SL}$	$0.056 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.448	$0.415 + 0.017 \cdot \text{SL}$	$0.423 + 0.015 \cdot \text{SL}$	$0.430 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.444	$0.410 + 0.017 \cdot \text{SL}$	$0.419 + 0.015 \cdot \text{SL}$	$0.426 + 0.014 \cdot \text{SL}$
GN to QN	$t_R$	0.129	$0.070 + 0.030 \cdot \text{SL}$	$0.070 + 0.030 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$
	$t_F$	0.110	$0.058 + 0.026 \cdot \text{SL}$	$0.061 + 0.025 \cdot \text{SL}$	$0.056 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.436	$0.403 + 0.017 \cdot \text{SL}$	$0.411 + 0.015 \cdot \text{SL}$	$0.418 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.483	$0.449 + 0.017 \cdot \text{SL}$	$0.457 + 0.015 \cdot \text{SL}$	$0.465 + 0.014 \cdot \text{SL}$
SN to QN	$t_R$	0.134	$0.079 + 0.028 \cdot \text{SL}$	$0.069 + 0.030 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$
	$t_F$	0.112	$0.060 + 0.026 \cdot \text{SL}$	$0.065 + 0.025 \cdot \text{SL}$	$0.058 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.177	$0.143 + 0.017 \cdot \text{SL}$	$0.152 + 0.015 \cdot \text{SL}$	$0.159 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.192	$0.158 + 0.017 \cdot \text{SL}$	$0.167 + 0.015 \cdot \text{SL}$	$0.174 + 0.014 \cdot \text{SL}$
RN to QN	$t_R$	0.130	$0.070 + 0.030 \cdot \text{SL}$	$0.070 + 0.030 \cdot \text{SL}$	$0.065 + 0.030 \cdot \text{SL}$
	$t_F$	0.110	$0.059 + 0.026 \cdot \text{SL}$	$0.061 + 0.025 \cdot \text{SL}$	$0.056 + 0.026 \cdot \text{SL}$
	$t_{PLH}$	0.263	$0.229 + 0.017 \cdot \text{SL}$	$0.237 + 0.015 \cdot \text{SL}$	$0.244 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.206 + 0.017 \cdot \text{SL}$	$0.215 + 0.015 \cdot \text{SL}$	$0.222 + 0.014 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## LD8/LD8D2

### D Latch with Active Low, Reset, Set, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### LD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	$t_R$	0.088	$0.061 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.549	$0.531 + 0.009 \cdot \text{SL}$	$0.538 + 0.007 \cdot \text{SL}$	$0.545 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.577	$0.556 + 0.010 \cdot \text{SL}$	$0.564 + 0.008 \cdot \text{SL}$	$0.576 + 0.007 \cdot \text{SL}$
GN to Q	$t_R$	0.088	$0.061 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.588	$0.570 + 0.009 \cdot \text{SL}$	$0.576 + 0.007 \cdot \text{SL}$	$0.584 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.566	$0.545 + 0.010 \cdot \text{SL}$	$0.553 + 0.008 \cdot \text{SL}$	$0.565 + 0.007 \cdot \text{SL}$
SN to Q	$t_R$	0.089	$0.061 + 0.014 \cdot \text{SL}$	$0.061 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.088	$0.061 + 0.014 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.299	$0.281 + 0.009 \cdot \text{SL}$	$0.288 + 0.007 \cdot \text{SL}$	$0.295 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.305	$0.284 + 0.010 \cdot \text{SL}$	$0.292 + 0.008 \cdot \text{SL}$	$0.304 + 0.007 \cdot \text{SL}$
RN to Q	$t_R$	0.089	$0.060 + 0.014 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.049 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.063 + 0.013 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.344	$0.326 + 0.009 \cdot \text{SL}$	$0.333 + 0.007 \cdot \text{SL}$	$0.340 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.391	$0.370 + 0.010 \cdot \text{SL}$	$0.378 + 0.008 \cdot \text{SL}$	$0.390 + 0.007 \cdot \text{SL}$
D to QN	$t_R$	0.101	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.453	$0.433 + 0.010 \cdot \text{SL}$	$0.441 + 0.008 \cdot \text{SL}$	$0.455 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.444	$0.423 + 0.011 \cdot \text{SL}$	$0.432 + 0.008 \cdot \text{SL}$	$0.445 + 0.007 \cdot \text{SL}$
GN to QN	$t_R$	0.100	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$	$0.070 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.060 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.442	$0.421 + 0.010 \cdot \text{SL}$	$0.430 + 0.008 \cdot \text{SL}$	$0.444 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.483	$0.462 + 0.011 \cdot \text{SL}$	$0.471 + 0.008 \cdot \text{SL}$	$0.484 + 0.007 \cdot \text{SL}$
SN to QN	$t_R$	0.101	$0.071 + 0.015 \cdot \text{SL}$	$0.072 + 0.015 \cdot \text{SL}$	$0.072 + 0.015 \cdot \text{SL}$
	$t_F$	0.091	$0.063 + 0.014 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.182	$0.161 + 0.010 \cdot \text{SL}$	$0.170 + 0.008 \cdot \text{SL}$	$0.184 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.194	$0.173 + 0.011 \cdot \text{SL}$	$0.182 + 0.008 \cdot \text{SL}$	$0.196 + 0.007 \cdot \text{SL}$
RN to QN	$t_R$	0.101	$0.072 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.268	$0.247 + 0.010 \cdot \text{SL}$	$0.256 + 0.008 \cdot \text{SL}$	$0.270 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.240	$0.219 + 0.011 \cdot \text{SL}$	$0.228 + 0.008 \cdot \text{SL}$	$0.241 + 0.007 \cdot \text{SL}$

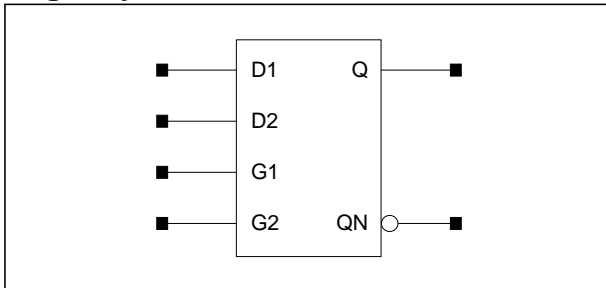
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## OAK\_LDI2/OAK\_LDI2D2

### D Latch with 2 Input, 2 Active High, 1X/2X Drive

#### Logic Symbol



#### Truth Table

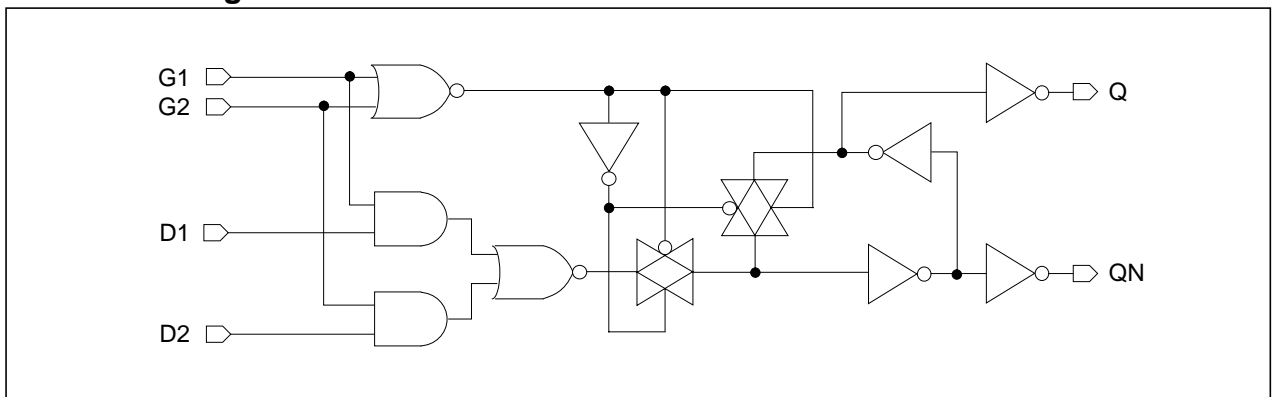
D1	G1	D2	G2	Q (n+1)	QN (n+1)
x	0	x	0	Q (n)	QN (n)
x	0	1	1	1	0
x	0	0	1	0	1
1	1	x	0	1	0
0	1	x	0	0	1
x	1	x	1	*	*

\* Both Q and QN will be UNKNOWN when G1 and G2 are both HIGH

#### Cell Data

Input Load (SL)								Gate Count	
OAK_LDI2				OAK_LDI2D2				OAK_LDI2	OAK_LDI2D2
D1	D2	G1	G2	D1	D2	G1	G2		
0.4	0.6	0.8	1.1	0.4	0.6	0.8	1.1	5.67	6.00

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		OAK_LDI2	OAK_LDI2D2
Input Setup Time (D1 to G1)	$t_{SU}$	0.679	0.694
Input Hold Time (D1 to G1)	$t_{HD}$	0.104	0.060
Input Setup Time (D2 to G2)	$t_{SU}$	0.789	0.801
Input Hold Time (D2 to G2)	$t_{HD}$	0.055	0.013
Pulse Width High (G1)	$t_{PWH}$	0.370	0.393
Pulse Width High (G2)	$t_{PWH}$	0.411	0.433



## OAK\_LDI2/OAK\_LDI2D2

### D Latch with 2 Input, 2 Active High, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### OAK\_LDI2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to Q	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.107	$0.055 + 0.026 \cdot \text{SL}$	$0.051 + 0.027 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.465	$0.436 + 0.015 \cdot \text{SL}$	$0.440 + 0.014 \cdot \text{SL}$	$0.441 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.537	$0.504 + 0.016 \cdot \text{SL}$	$0.510 + 0.015 \cdot \text{SL}$	$0.513 + 0.014 \cdot \text{SL}$
D2 to Q	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.052 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.107	$0.055 + 0.026 \cdot \text{SL}$	$0.051 + 0.027 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.514	$0.485 + 0.015 \cdot \text{SL}$	$0.489 + 0.014 \cdot \text{SL}$	$0.490 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.555	$0.523 + 0.016 \cdot \text{SL}$	$0.529 + 0.015 \cdot \text{SL}$	$0.532 + 0.014 \cdot \text{SL}$
G1 to Q	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.105	$0.053 + 0.026 \cdot \text{SL}$	$0.051 + 0.027 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.460	$0.431 + 0.015 \cdot \text{SL}$	$0.435 + 0.014 \cdot \text{SL}$	$0.436 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.451	$0.418 + 0.016 \cdot \text{SL}$	$0.424 + 0.015 \cdot \text{SL}$	$0.427 + 0.014 \cdot \text{SL}$
G2 to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.104	$0.050 + 0.027 \cdot \text{SL}$	$0.050 + 0.027 \cdot \text{SL}$	$0.044 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.508	$0.478 + 0.015 \cdot \text{SL}$	$0.482 + 0.014 \cdot \text{SL}$	$0.484 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.460	$0.427 + 0.016 \cdot \text{SL}$	$0.434 + 0.015 \cdot \text{SL}$	$0.436 + 0.014 \cdot \text{SL}$
D1 to QN	$t_R$	0.135	$0.080 + 0.028 \cdot \text{SL}$	$0.074 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.118	$0.065 + 0.026 \cdot \text{SL}$	$0.065 + 0.026 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.461	$0.430 + 0.016 \cdot \text{SL}$	$0.437 + 0.014 \cdot \text{SL}$	$0.440 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.409	$0.374 + 0.017 \cdot \text{SL}$	$0.383 + 0.015 \cdot \text{SL}$	$0.390 + 0.015 \cdot \text{SL}$
D2 to QN	$t_R$	0.134	$0.079 + 0.028 \cdot \text{SL}$	$0.073 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.119	$0.066 + 0.026 \cdot \text{SL}$	$0.067 + 0.026 \cdot \text{SL}$	$0.060 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.480	$0.449 + 0.016 \cdot \text{SL}$	$0.456 + 0.014 \cdot \text{SL}$	$0.459 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.459	$0.424 + 0.017 \cdot \text{SL}$	$0.432 + 0.015 \cdot \text{SL}$	$0.439 + 0.015 \cdot \text{SL}$
G1 to QN	$t_R$	0.125	$0.068 + 0.028 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$	$0.055 + 0.031 \cdot \text{SL}$
	$t_F$	0.117	$0.064 + 0.026 \cdot \text{SL}$	$0.064 + 0.026 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.377	$0.346 + 0.015 \cdot \text{SL}$	$0.352 + 0.014 \cdot \text{SL}$	$0.355 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.405	$0.370 + 0.017 \cdot \text{SL}$	$0.378 + 0.015 \cdot \text{SL}$	$0.385 + 0.015 \cdot \text{SL}$
G2 to QN	$t_R$	0.124	$0.067 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$	$0.056 + 0.031 \cdot \text{SL}$
	$t_F$	0.117	$0.063 + 0.027 \cdot \text{SL}$	$0.064 + 0.027 \cdot \text{SL}$	$0.060 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.386	$0.355 + 0.015 \cdot \text{SL}$	$0.361 + 0.014 \cdot \text{SL}$	$0.364 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.452	$0.417 + 0.017 \cdot \text{SL}$	$0.425 + 0.015 \cdot \text{SL}$	$0.432 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OAK\_LDI2/OAK\_LDI2D2

## D Latch with 2 Input, 2 Active High, 1X/2X Drive

### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### OAK\_LDI2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to Q	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.506	$0.488 + 0.009 \cdot \text{SL}$	$0.495 + 0.007 \cdot \text{SL}$	$0.501 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.578	$0.558 + 0.010 \cdot \text{SL}$	$0.566 + 0.008 \cdot \text{SL}$	$0.576 + 0.007 \cdot \text{SL}$
D2 to Q	$t_R$	0.086	$0.057 + 0.015 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.082	$0.055 + 0.014 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.555	$0.538 + 0.009 \cdot \text{SL}$	$0.544 + 0.007 \cdot \text{SL}$	$0.550 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.596	$0.576 + 0.010 \cdot \text{SL}$	$0.584 + 0.008 \cdot \text{SL}$	$0.594 + 0.007 \cdot \text{SL}$
G1 to Q	$t_R$	0.086	$0.057 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.052 + 0.014 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.501	$0.483 + 0.009 \cdot \text{SL}$	$0.489 + 0.007 \cdot \text{SL}$	$0.496 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.488	$0.468 + 0.010 \cdot \text{SL}$	$0.476 + 0.008 \cdot \text{SL}$	$0.486 + 0.007 \cdot \text{SL}$
G2 to Q	$t_R$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.051 + 0.014 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.549	$0.531 + 0.009 \cdot \text{SL}$	$0.537 + 0.007 \cdot \text{SL}$	$0.543 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.497	$0.476 + 0.010 \cdot \text{SL}$	$0.485 + 0.008 \cdot \text{SL}$	$0.495 + 0.007 \cdot \text{SL}$
D1 to QN	$t_R$	0.106	$0.079 + 0.014 \cdot \text{SL}$	$0.077 + 0.014 \cdot \text{SL}$	$0.067 + 0.015 \cdot \text{SL}$
	$t_F$	0.094	$0.066 + 0.014 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.470	$0.451 + 0.010 \cdot \text{SL}$	$0.460 + 0.008 \cdot \text{SL}$	$0.469 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.412	$0.391 + 0.011 \cdot \text{SL}$	$0.400 + 0.008 \cdot \text{SL}$	$0.413 + 0.007 \cdot \text{SL}$
D2 to QN	$t_R$	0.105	$0.078 + 0.014 \cdot \text{SL}$	$0.076 + 0.014 \cdot \text{SL}$	$0.066 + 0.015 \cdot \text{SL}$
	$t_F$	0.094	$0.067 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.489	$0.470 + 0.010 \cdot \text{SL}$	$0.478 + 0.008 \cdot \text{SL}$	$0.488 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.462	$0.441 + 0.011 \cdot \text{SL}$	$0.449 + 0.008 \cdot \text{SL}$	$0.463 + 0.007 \cdot \text{SL}$
G1 to QN	$t_R$	0.097	$0.068 + 0.014 \cdot \text{SL}$	$0.068 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$
	$t_F$	0.092	$0.065 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.383	$0.364 + 0.009 \cdot \text{SL}$	$0.372 + 0.007 \cdot \text{SL}$	$0.380 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.408	$0.386 + 0.011 \cdot \text{SL}$	$0.395 + 0.008 \cdot \text{SL}$	$0.408 + 0.007 \cdot \text{SL}$
G2 to QN	$t_R$	0.097	$0.070 + 0.014 \cdot \text{SL}$	$0.066 + 0.014 \cdot \text{SL}$	$0.057 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.067 + 0.013 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$	$0.065 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.392	$0.373 + 0.010 \cdot \text{SL}$	$0.381 + 0.007 \cdot \text{SL}$	$0.390 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.455	$0.434 + 0.011 \cdot \text{SL}$	$0.443 + 0.008 \cdot \text{SL}$	$0.456 + 0.007 \cdot \text{SL}$

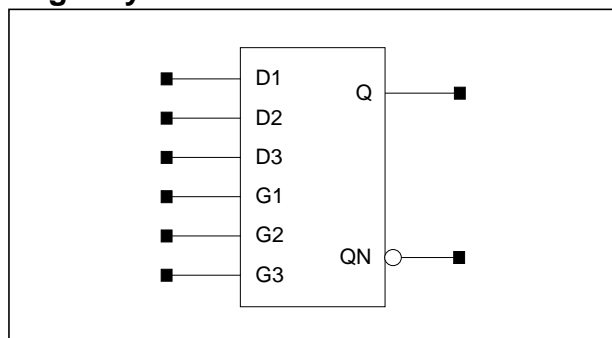
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



## OAK\_LDI3/OAK\_LDI3D2

### D Latch with 3 Input, 3 Active High, 1X/2X Drive

#### Logic Symbol



#### Truth Table

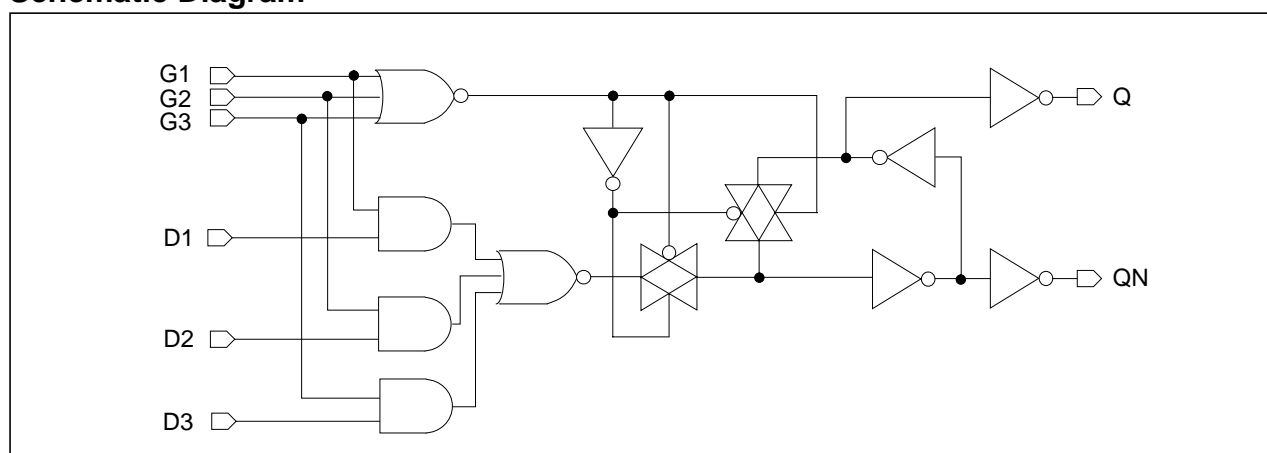
D1	G1	D2	G2	D3	G3	Q (n+1)	QN (n+1)
x	0	x	0	x	0	Q (n)	QN (n)
x	0	x	0	1	1	1	0
x	0	x	0	0	1	0	1
1	1	x	0	x	0	1	0
0	1	x	0	x	0	0	1
x	0	1	1	x	0	1	0
x	0	0	1	x	0	0	1
x	x	x	1	x	1	*	*
x	1	x	1	x	x	*	*
x	1	x	x	x	1	*	*

\* Q and QN are both UNKNOWN, at least two of control signals are HIGH at the same time.

#### Cell Data

Input Load (SL)												Gate Count	
OAK_LDI3						OAK_LDI3D2						OAK_LDI3	OAK_LDI3D2
D1	D2	D3	G1	G2	G3	D1	D2	D3	G1	G2	G3		
0.4	0.6	0.5	1.0	1.0	1.1	0.4	0.6	0.5	1.0	1.0	1.1	6.67	7.00

#### Schematic Diagram



#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		OAK_LDI3	OAK_LDI3D2
Input Setup Time (D1 to G1)	$t_{SU}$	0.680	0.696
Input Hold Time (D1 to G1)	$t_{HD}$	0.045	0.000
Input Setup Time (D2 to G2)	$t_{SU}$	0.794	0.811
Input Hold Time (D2 to G2)	$t_{HD}$	0.000	0.000
Input Setup Time (D3 to G3)	$t_{SU}$	0.882	0.897
Input Hold Time (D3 to G3)	$t_{HD}$	0.000	0.000
Pulse Width High (G1)	$t_{PWH}$	0.397	0.417
Pulse Width High (G2)	$t_{PWH}$	0.449	0.468
Pulse Width High (G3)	$t_{PWH}$	0.599	0.518



## Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ ns}$ , SL: Standard Load)

## OAK\_LDI3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to Q	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.106	$0.055 + 0.025 \cdot \text{SL}$	$0.051 + 0.026 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.488	$0.459 + 0.015 \cdot \text{SL}$	$0.463 + 0.014 \cdot \text{SL}$	$0.464 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.539	$0.506 + 0.016 \cdot \text{SL}$	$0.513 + 0.015 \cdot \text{SL}$	$0.516 + 0.014 \cdot \text{SL}$
D2 to Q	$t_R$	0.113	$0.056 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.045 + 0.031 \cdot \text{SL}$
	$t_F$	0.106	$0.055 + 0.026 \cdot \text{SL}$	$0.052 + 0.026 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.559	$0.529 + 0.015 \cdot \text{SL}$	$0.534 + 0.014 \cdot \text{SL}$	$0.535 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.600	$0.567 + 0.016 \cdot \text{SL}$	$0.573 + 0.015 \cdot \text{SL}$	$0.577 + 0.014 \cdot \text{SL}$
D3 to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.106	$0.055 + 0.026 \cdot \text{SL}$	$0.052 + 0.026 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.609	$0.580 + 0.015 \cdot \text{SL}$	$0.584 + 0.014 \cdot \text{SL}$	$0.585 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.639	$0.607 + 0.016 \cdot \text{SL}$	$0.613 + 0.015 \cdot \text{SL}$	$0.616 + 0.014 \cdot \text{SL}$
G1 to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.044 + 0.031 \cdot \text{SL}$
	$t_F$	0.104	$0.052 + 0.026 \cdot \text{SL}$	$0.050 + 0.027 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.488	$0.459 + 0.015 \cdot \text{SL}$	$0.463 + 0.014 \cdot \text{SL}$	$0.464 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.456	$0.423 + 0.016 \cdot \text{SL}$	$0.430 + 0.015 \cdot \text{SL}$	$0.433 + 0.014 \cdot \text{SL}$
G2 to Q	$t_R$	0.114	$0.056 + 0.029 \cdot \text{SL}$	$0.051 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.103	$0.050 + 0.027 \cdot \text{SL}$	$0.050 + 0.027 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.549	$0.520 + 0.015 \cdot \text{SL}$	$0.524 + 0.014 \cdot \text{SL}$	$0.525 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.466	$0.433 + 0.016 \cdot \text{SL}$	$0.439 + 0.015 \cdot \text{SL}$	$0.442 + 0.014 \cdot \text{SL}$
G3 to Q	$t_R$	0.113	$0.055 + 0.029 \cdot \text{SL}$	$0.050 + 0.030 \cdot \text{SL}$	$0.046 + 0.031 \cdot \text{SL}$
	$t_F$	0.103	$0.050 + 0.027 \cdot \text{SL}$	$0.051 + 0.026 \cdot \text{SL}$	$0.045 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.601	$0.572 + 0.015 \cdot \text{SL}$	$0.576 + 0.014 \cdot \text{SL}$	$0.577 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.472	$0.439 + 0.016 \cdot \text{SL}$	$0.446 + 0.015 \cdot \text{SL}$	$0.449 + 0.014 \cdot \text{SL}$
D1 to QN	$t_R$	0.135	$0.080 + 0.028 \cdot \text{SL}$	$0.075 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$
	$t_F$	0.118	$0.066 + 0.026 \cdot \text{SL}$	$0.065 + 0.026 \cdot \text{SL}$	$0.059 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.463	$0.432 + 0.016 \cdot \text{SL}$	$0.439 + 0.014 \cdot \text{SL}$	$0.443 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.432	$0.397 + 0.017 \cdot \text{SL}$	$0.405 + 0.015 \cdot \text{SL}$	$0.412 + 0.015 \cdot \text{SL}$
D2 to QN	$t_R$	0.137	$0.082 + 0.028 \cdot \text{SL}$	$0.077 + 0.029 \cdot \text{SL}$	$0.065 + 0.030 \cdot \text{SL}$
	$t_F$	0.120	$0.067 + 0.026 \cdot \text{SL}$	$0.069 + 0.026 \cdot \text{SL}$	$0.061 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.524	$0.492 + 0.016 \cdot \text{SL}$	$0.500 + 0.014 \cdot \text{SL}$	$0.504 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.502	$0.467 + 0.018 \cdot \text{SL}$	$0.475 + 0.015 \cdot \text{SL}$	$0.483 + 0.015 \cdot \text{SL}$
D3 to QN	$t_R$	0.138	$0.083 + 0.028 \cdot \text{SL}$	$0.079 + 0.029 \cdot \text{SL}$	$0.066 + 0.030 \cdot \text{SL}$
	$t_F$	0.121	$0.068 + 0.026 \cdot \text{SL}$	$0.069 + 0.026 \cdot \text{SL}$	$0.063 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.563	$0.531 + 0.016 \cdot \text{SL}$	$0.539 + 0.014 \cdot \text{SL}$	$0.543 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.552	$0.517 + 0.018 \cdot \text{SL}$	$0.526 + 0.015 \cdot \text{SL}$	$0.533 + 0.015 \cdot \text{SL}$
G1 to QN	$t_R$	0.126	$0.069 + 0.028 \cdot \text{SL}$	$0.065 + 0.029 \cdot \text{SL}$	$0.056 + 0.031 \cdot \text{SL}$
	$t_F$	0.117	$0.064 + 0.026 \cdot \text{SL}$	$0.065 + 0.026 \cdot \text{SL}$	$0.058 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.382	$0.351 + 0.015 \cdot \text{SL}$	$0.357 + 0.014 \cdot \text{SL}$	$0.360 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.432	$0.397 + 0.017 \cdot \text{SL}$	$0.405 + 0.015 \cdot \text{SL}$	$0.412 + 0.015 \cdot \text{SL}$



## OAK\_LDI3/OAK\_LDI3D2

### D Latch with 3 Input, 3 Active High, 1X/2X Drive

**Switching Characteristics(Cont.)** (Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### OAK\_LDI3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
G2 to QN	$t_R$	0.125	$0.067 + 0.029 \cdot \text{SL}$	$0.064 + 0.030 \cdot \text{SL}$	$0.056 + 0.031 \cdot \text{SL}$
	$t_F$	0.119	$0.066 + 0.026 \cdot \text{SL}$	$0.066 + 0.026 \cdot \text{SL}$	$0.060 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.391	$0.360 + 0.016 \cdot \text{SL}$	$0.367 + 0.014 \cdot \text{SL}$	$0.370 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.492	$0.457 + 0.018 \cdot \text{SL}$	$0.466 + 0.015 \cdot \text{SL}$	$0.473 + 0.015 \cdot \text{SL}$
G3 to QN	$t_R$	0.124	$0.067 + 0.029 \cdot \text{SL}$	$0.063 + 0.030 \cdot \text{SL}$	$0.056 + 0.031 \cdot \text{SL}$
	$t_F$	0.121	$0.068 + 0.026 \cdot \text{SL}$	$0.068 + 0.026 \cdot \text{SL}$	$0.062 + 0.027 \cdot \text{SL}$
	$t_{PLH}$	0.398	$0.367 + 0.015 \cdot \text{SL}$	$0.373 + 0.014 \cdot \text{SL}$	$0.376 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.544	$0.509 + 0.018 \cdot \text{SL}$	$0.518 + 0.015 \cdot \text{SL}$	$0.525 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



# OAK\_LDI3/OAK\_LDI3D2

## D Latch with 3 Input, 3 Active High, 1X/2X Drive

### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### OAK\_LDI3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to Q	$t_R$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.054 + 0.015 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.013 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.530	$0.512 + 0.009 \cdot \text{SL}$	$0.518 + 0.007 \cdot \text{SL}$	$0.524 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.582	$0.562 + 0.010 \cdot \text{SL}$	$0.570 + 0.008 \cdot \text{SL}$	$0.580 + 0.007 \cdot \text{SL}$
D2 to Q	$t_R$	0.086	$0.057 + 0.015 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.013 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.601	$0.584 + 0.009 \cdot \text{SL}$	$0.590 + 0.007 \cdot \text{SL}$	$0.596 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.645	$0.625 + 0.010 \cdot \text{SL}$	$0.632 + 0.008 \cdot \text{SL}$	$0.642 + 0.007 \cdot \text{SL}$
D3 to Q	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.057 + 0.014 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.083	$0.056 + 0.014 \cdot \text{SL}$	$0.058 + 0.013 \cdot \text{SL}$	$0.052 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.653	$0.635 + 0.009 \cdot \text{SL}$	$0.641 + 0.007 \cdot \text{SL}$	$0.648 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.685	$0.665 + 0.010 \cdot \text{SL}$	$0.673 + 0.008 \cdot \text{SL}$	$0.683 + 0.007 \cdot \text{SL}$
G1 to Q	$t_R$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.052 + 0.014 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.050 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.530	$0.512 + 0.009 \cdot \text{SL}$	$0.519 + 0.007 \cdot \text{SL}$	$0.524 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.497	$0.476 + 0.010 \cdot \text{SL}$	$0.484 + 0.008 \cdot \text{SL}$	$0.494 + 0.007 \cdot \text{SL}$
G2 to Q	$t_R$	0.086	$0.059 + 0.014 \cdot \text{SL}$	$0.055 + 0.015 \cdot \text{SL}$	$0.047 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.051 + 0.014 \cdot \text{SL}$	$0.056 + 0.013 \cdot \text{SL}$	$0.051 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.592	$0.574 + 0.009 \cdot \text{SL}$	$0.580 + 0.007 \cdot \text{SL}$	$0.587 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.506	$0.485 + 0.010 \cdot \text{SL}$	$0.494 + 0.008 \cdot \text{SL}$	$0.504 + 0.007 \cdot \text{SL}$
G3 to Q	$t_R$	0.087	$0.059 + 0.014 \cdot \text{SL}$	$0.058 + 0.014 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.080	$0.051 + 0.015 \cdot \text{SL}$	$0.057 + 0.013 \cdot \text{SL}$	$0.051 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.645	$0.627 + 0.009 \cdot \text{SL}$	$0.633 + 0.007 \cdot \text{SL}$	$0.640 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.512	$0.492 + 0.010 \cdot \text{SL}$	$0.500 + 0.008 \cdot \text{SL}$	$0.510 + 0.007 \cdot \text{SL}$
D1 to QN	$t_R$	0.108	$0.081 + 0.014 \cdot \text{SL}$	$0.079 + 0.014 \cdot \text{SL}$	$0.069 + 0.015 \cdot \text{SL}$
	$t_F$	0.094	$0.067 + 0.014 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.474	$0.454 + 0.010 \cdot \text{SL}$	$0.463 + 0.008 \cdot \text{SL}$	$0.473 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.436	$0.414 + 0.011 \cdot \text{SL}$	$0.423 + 0.008 \cdot \text{SL}$	$0.437 + 0.007 \cdot \text{SL}$
D2 to QN	$t_R$	0.111	$0.084 + 0.013 \cdot \text{SL}$	$0.082 + 0.014 \cdot \text{SL}$	$0.071 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.070 + 0.013 \cdot \text{SL}$	$0.069 + 0.013 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.535	$0.515 + 0.010 \cdot \text{SL}$	$0.524 + 0.008 \cdot \text{SL}$	$0.535 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.507	$0.486 + 0.011 \cdot \text{SL}$	$0.494 + 0.009 \cdot \text{SL}$	$0.508 + 0.007 \cdot \text{SL}$
D3 to QN	$t_R$	0.112	$0.085 + 0.013 \cdot \text{SL}$	$0.083 + 0.014 \cdot \text{SL}$	$0.072 + 0.015 \cdot \text{SL}$
	$t_F$	0.099	$0.072 + 0.013 \cdot \text{SL}$	$0.074 + 0.013 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.575	$0.555 + 0.010 \cdot \text{SL}$	$0.565 + 0.008 \cdot \text{SL}$	$0.575 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.558	$0.536 + 0.011 \cdot \text{SL}$	$0.546 + 0.009 \cdot \text{SL}$	$0.559 + 0.007 \cdot \text{SL}$
G1 to QN	$t_R$	0.099	$0.071 + 0.014 \cdot \text{SL}$	$0.070 + 0.014 \cdot \text{SL}$	$0.061 + 0.015 \cdot \text{SL}$
	$t_F$	0.093	$0.066 + 0.014 \cdot \text{SL}$	$0.068 + 0.013 \cdot \text{SL}$	$0.066 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.390	$0.371 + 0.010 \cdot \text{SL}$	$0.379 + 0.008 \cdot \text{SL}$	$0.388 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.436	$0.415 + 0.011 \cdot \text{SL}$	$0.423 + 0.009 \cdot \text{SL}$	$0.437 + 0.007 \cdot \text{SL}$



## OAK\_LDI3/OAK\_LDI3D2

### D Latch with 3 Input, 3 Active High, 1X/2X Drive

**Switching Characteristics(Cont.)** (Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### OAK\_LDI3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
G2 to QN	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.070 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.096	$0.069 + 0.014 \cdot \text{SL}$	$0.071 + 0.013 \cdot \text{SL}$	$0.067 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.399	$0.380 + 0.010 \cdot \text{SL}$	$0.389 + 0.008 \cdot \text{SL}$	$0.398 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.498	$0.476 + 0.011 \cdot \text{SL}$	$0.485 + 0.009 \cdot \text{SL}$	$0.499 + 0.007 \cdot \text{SL}$
G3 to QN	$t_R$	0.098	$0.070 + 0.014 \cdot \text{SL}$	$0.069 + 0.014 \cdot \text{SL}$	$0.059 + 0.015 \cdot \text{SL}$
	$t_F$	0.099	$0.072 + 0.013 \cdot \text{SL}$	$0.073 + 0.013 \cdot \text{SL}$	$0.070 + 0.013 \cdot \text{SL}$
	$t_{PLH}$	0.406	$0.387 + 0.009 \cdot \text{SL}$	$0.395 + 0.008 \cdot \text{SL}$	$0.404 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.550	$0.528 + 0.011 \cdot \text{SL}$	$0.537 + 0.009 \cdot \text{SL}$	$0.551 + 0.007 \cdot \text{SL}$

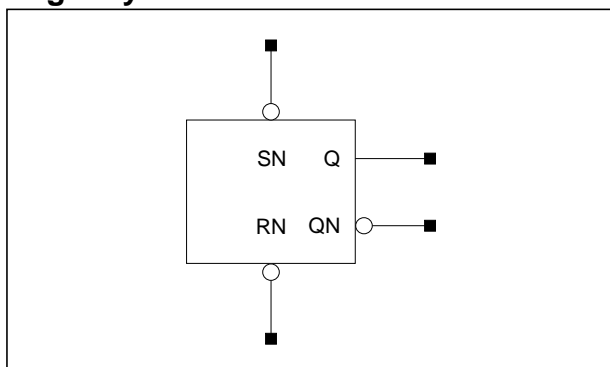
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



# LS0/LS0D2

## SR Latch with 1X/2X Drive

### Logic Symbol



### Truth Table

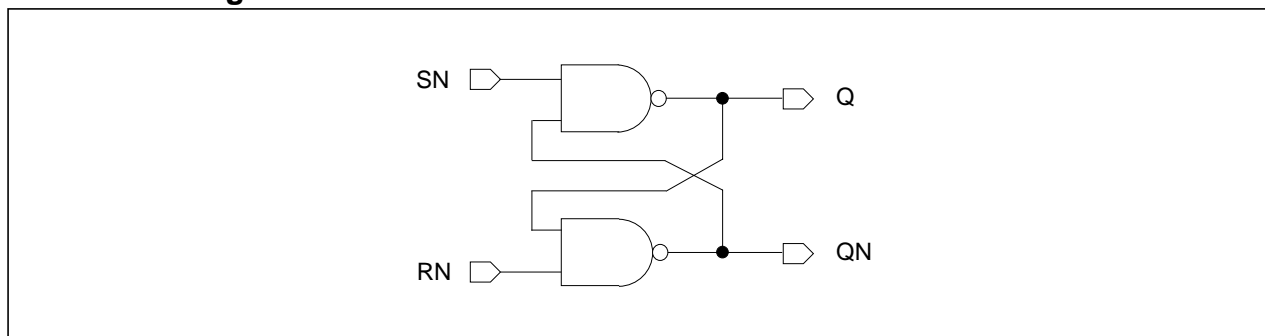
RN	SN	Q (n+1)	QN (n+1)
0	0	*	*
1	0	1	0
0	1	0	1
1	1	Q (n)	QN (n)

\* Both Q and QN outputs will remain high during RN and SN are low. However, if RN and SN go high simultaneously, the output states are unpredictable.

### Cell Data

Input Load (SL)				Gate Count	
LS0		LS0D2		LS0	LS0D2
RN	SN	RN	SN		
1.1	1.1	2.2	2.2	1.67	3.00

### Schematic Diagram



### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LS0	LS0D2
Pulse Width Low (SN)	$t_{PWL}$	0.237	0.208
Removal Time (SN to RN)	$t_{RM}$	0.016	0.057
Recovery Time (Sn to RN)	$t_{RC}$	0.190	0.159
Pulse Width Low (RN)	$t_{PWL}$	0.238	0.208



## LS0/LS0D2

### SR Latch with 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5 V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

##### LS0

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	$t_R$	0.172	$0.130 + 0.021 \cdot \text{SL}$	$0.133 + 0.020 \cdot \text{SL}$	$0.130 + 0.020 \cdot \text{SL}$
	$t_F$	0.182	$0.127 + 0.028 \cdot \text{SL}$	$0.119 + 0.030 \cdot \text{SL}$	$0.108 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.109	$0.079 + 0.015 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.109	$0.076 + 0.016 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$	$0.080 + 0.015 \cdot \text{SL}$
RN to Q	$t_F$	0.156	$0.094 + 0.031 \cdot \text{SL}$	$0.091 + 0.032 \cdot \text{SL}$	$0.088 + 0.032 \cdot \text{SL}$
	$t_{PHL}$	0.171	$0.138 + 0.016 \cdot \text{SL}$	$0.141 + 0.016 \cdot \text{SL}$	$0.142 + 0.015 \cdot \text{SL}$
SN to QN	$t_F$	0.156	$0.094 + 0.031 \cdot \text{SL}$	$0.092 + 0.032 \cdot \text{SL}$	$0.089 + 0.032 \cdot \text{SL}$
	$t_{PHL}$	0.171	$0.139 + 0.016 \cdot \text{SL}$	$0.141 + 0.016 \cdot \text{SL}$	$0.142 + 0.015 \cdot \text{SL}$
RN to QN	$t_R$	0.172	$0.130 + 0.021 \cdot \text{SL}$	$0.133 + 0.020 \cdot \text{SL}$	$0.130 + 0.020 \cdot \text{SL}$
	$t_F$	0.183	$0.128 + 0.028 \cdot \text{SL}$	$0.119 + 0.030 \cdot \text{SL}$	$0.108 + 0.031 \cdot \text{SL}$
	$t_{PLH}$	0.109	$0.079 + 0.015 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$	$0.085 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.109	$0.076 + 0.016 \cdot \text{SL}$	$0.081 + 0.015 \cdot \text{SL}$	$0.080 + 0.015 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$

##### LS0D2

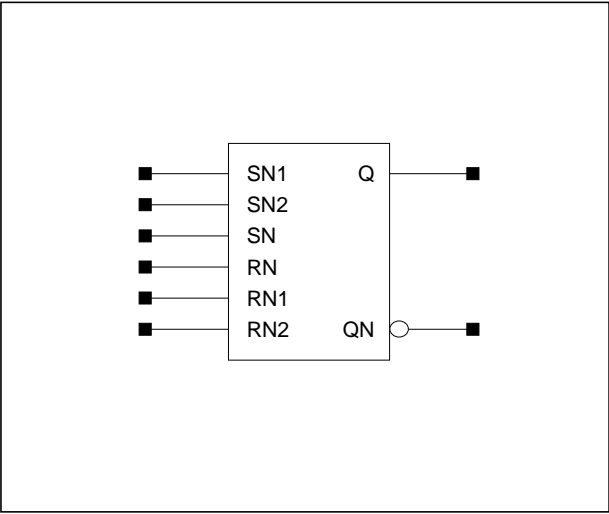
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	$t_R$	0.149	$0.128 + 0.011 \cdot \text{SL}$	$0.130 + 0.010 \cdot \text{SL}$	$0.129 + 0.010 \cdot \text{SL}$
	$t_F$	0.153	$0.126 + 0.014 \cdot \text{SL}$	$0.123 + 0.014 \cdot \text{SL}$	$0.109 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.092	$0.075 + 0.008 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.091	$0.072 + 0.009 \cdot \text{SL}$	$0.078 + 0.008 \cdot \text{SL}$	$0.079 + 0.008 \cdot \text{SL}$
RN to Q	$t_F$	0.123	$0.093 + 0.015 \cdot \text{SL}$	$0.091 + 0.016 \cdot \text{SL}$	$0.087 + 0.016 \cdot \text{SL}$
	$t_{PHL}$	0.152	$0.135 + 0.008 \cdot \text{SL}$	$0.137 + 0.008 \cdot \text{SL}$	$0.139 + 0.008 \cdot \text{SL}$
SN to QN	$t_F$	0.123	$0.092 + 0.015 \cdot \text{SL}$	$0.091 + 0.016 \cdot \text{SL}$	$0.087 + 0.016 \cdot \text{SL}$
	$t_{PHL}$	0.152	$0.136 + 0.008 \cdot \text{SL}$	$0.138 + 0.008 \cdot \text{SL}$	$0.139 + 0.008 \cdot \text{SL}$
RN to QN	$t_R$	0.149	$0.128 + 0.011 \cdot \text{SL}$	$0.130 + 0.010 \cdot \text{SL}$	$0.129 + 0.010 \cdot \text{SL}$
	$t_F$	0.153	$0.126 + 0.014 \cdot \text{SL}$	$0.123 + 0.014 \cdot \text{SL}$	$0.109 + 0.015 \cdot \text{SL}$
	$t_{PLH}$	0.092	$0.075 + 0.008 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$	$0.084 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.090	$0.072 + 0.009 \cdot \text{SL}$	$0.078 + 0.008 \cdot \text{SL}$	$0.079 + 0.008 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$



SR Latch with Separate Inputs, 1X/2X Drive

Logic Symbol



Truth Table

RN	SN	RN*	SN*	Q (n+1)	QN (n+1)
0	0	x	x	*	*
x	0	0	x	*	*
x	x	0	0	*	*
0	x	x	0	*	*
1	0	1	x	1	0
0	1	x	1	0	1
1	x	1	0	1	0
x	1	0	1	0	1
1	1	1	1	Q (n)	QN (n)

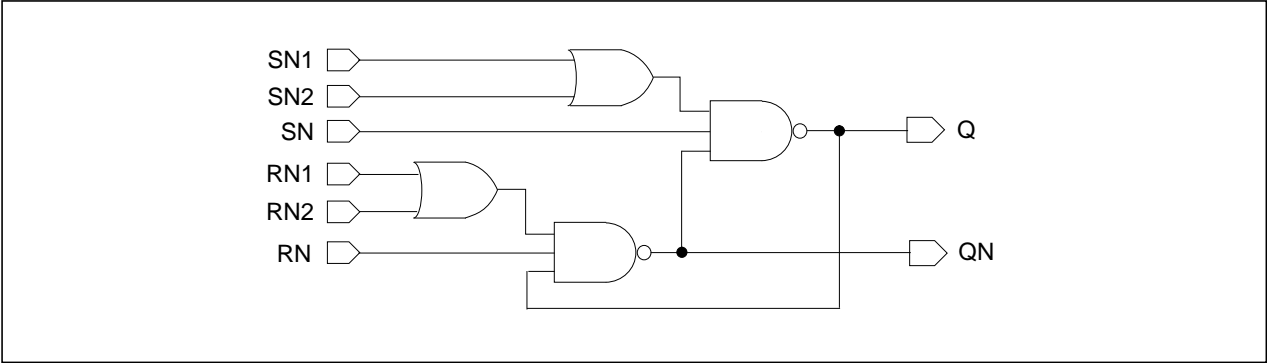
$RN^* = RN1 + RN2, SN^* = SN1 + SN2$

\* Both Q and QN outputs will be unknown when RN (RN\*) and SN (SN\*) are low.

Cell Data

Input Load (SL)												Gate Count	
LS1						LS1D2						LS1	LS1D2
SN1	SN2	SN	RN1	RN2	RN	SN1	SN2	SN	RN1	RN2	RN		
1.0	1.0	1.1	1.0	1.0	1.1	1.0	1.0	1.1	1.0	1.0	1.1	3.00	5.00

Schematic Diagram





## LS1/LS1D2

### SR Latch with Separate Inputs, 1X/2X Drive

#### Timing Requirements

(Typical process, 25°C, 2.5V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LS1	LS1D2
Pulse Width Low (SN1)	$t_{PWL}$	0.400	0.334
Removal Time (SN1 to RN1)	$t_{RM}$	0.000	0.103
Recovery Time (SN1 to RN1)	$t_{RC}$	0.235	0.114
Removal Time (SN1 to RN2)	$t_{RM}$	0.046	0.162
Recovery Time (SN1 to RN2)	$t_{RC}$	0.162	0.051
Removal Time (SN1 to RN)	$t_{RM}$	0.009	0.124
Recovery Time (SN1 to RN)	$t_{RC}$	0.213	0.094
Pulse Width Low (SN2)	$t_{PWL}$	0.404	0.336
Removal Time (SN2 to RN1)	$t_{RM}$	0.000	0.048
Recovery Time (SN2 to RN1)	$t_{RC}$	0.280	0.171
Removal Time (SN2 to RN2)	$t_{RM}$	0.001	0.110
Recovery Time (SN2 to RN2)	$t_{RC}$	0.220	0.108
Removal Time (SN2 to RN)	$t_{RM}$	0.000	0.066
Recovery Time (SN2 to RN)	$t_{RC}$	0.254	0.154
Pulse Width Low (SN)	$t_{PWL}$	0.299	0.266
Removal Time (SN to RN1)	$t_{RM}$	0.000	0.084
Recovery Time (SN to RN1)	$t_{RC}$	0.240	0.136
Removal Time (SN to RN2)	$t_{RM}$	0.039	0.141
Recovery Time (SN to RN2)	$t_{RC}$	0.177	0.078
Removal Time (SN to RN)	$t_{RM}$	0.005	0.105
Recovery Time (SN to RN)	$t_{RC}$	0.215	0.116
Pulse Width Low (RN1)	$t_{PWL}$	0.400	0.332
Pulse Width Low (RN2)	$t_{PWL}$	0.405	0.334
Pulse Width Low (RN)	$t_{PWL}$	0.299	0.266



## SR Latch with Separate Inputs, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

## LS1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	$t_R$	0.298	$0.223 + 0.037 \cdot \text{SL}$	$0.226 + 0.037 \cdot \text{SL}$	$0.228 + 0.036 \cdot \text{SL}$
	$t_F$	0.314	$0.207 + 0.054 \cdot \text{SL}$	$0.201 + 0.055 \cdot \text{SL}$	$0.189 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.176	$0.123 + 0.026 \cdot \text{SL}$	$0.123 + 0.026 \cdot \text{SL}$	$0.123 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.172	$0.121 + 0.026 \cdot \text{SL}$	$0.120 + 0.026 \cdot \text{SL}$	$0.119 + 0.026 \cdot \text{SL}$
SN2 to Q	$t_R$	0.304	$0.222 + 0.041 \cdot \text{SL}$	$0.232 + 0.038 \cdot \text{SL}$	$0.244 + 0.037 \cdot \text{SL}$
	$t_F$	0.353	$0.247 + 0.053 \cdot \text{SL}$	$0.240 + 0.055 \cdot \text{SL}$	$0.228 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.177	$0.124 + 0.026 \cdot \text{SL}$	$0.124 + 0.026 \cdot \text{SL}$	$0.125 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.195	$0.143 + 0.026 \cdot \text{SL}$	$0.142 + 0.026 \cdot \text{SL}$	$0.142 + 0.026 \cdot \text{SL}$
SN to Q	$t_R$	0.214	$0.168 + 0.023 \cdot \text{SL}$	$0.173 + 0.022 \cdot \text{SL}$	$0.175 + 0.022 \cdot \text{SL}$
	$t_F$	0.312	$0.203 + 0.054 \cdot \text{SL}$	$0.198 + 0.056 \cdot \text{SL}$	$0.191 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.128	$0.100 + 0.014 \cdot \text{SL}$	$0.102 + 0.013 \cdot \text{SL}$	$0.102 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.182	$0.130 + 0.026 \cdot \text{SL}$	$0.130 + 0.026 \cdot \text{SL}$	$0.130 + 0.026 \cdot \text{SL}$
RN1 to Q	$t_F$	0.313	$0.202 + 0.055 \cdot \text{SL}$	$0.199 + 0.056 \cdot \text{SL}$	$0.195 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.308	$0.253 + 0.027 \cdot \text{SL}$	$0.256 + 0.027 \cdot \text{SL}$	$0.259 + 0.026 \cdot \text{SL}$
RN2 to Q	$t_F$	0.349	$0.239 + 0.055 \cdot \text{SL}$	$0.236 + 0.056 \cdot \text{SL}$	$0.233 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.337	$0.282 + 0.027 \cdot \text{SL}$	$0.285 + 0.027 \cdot \text{SL}$	$0.288 + 0.026 \cdot \text{SL}$
RN to Q	$t_F$	0.305	$0.194 + 0.056 \cdot \text{SL}$	$0.191 + 0.056 \cdot \text{SL}$	$0.188 + 0.057 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.223 + 0.027 \cdot \text{SL}$	$0.225 + 0.027 \cdot \text{SL}$	$0.226 + 0.026 \cdot \text{SL}$
SN1 to QN	$t_F$	0.313	$0.203 + 0.055 \cdot \text{SL}$	$0.199 + 0.056 \cdot \text{SL}$	$0.196 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.308	$0.253 + 0.027 \cdot \text{SL}$	$0.256 + 0.027 \cdot \text{SL}$	$0.259 + 0.026 \cdot \text{SL}$
SN2 to QN	$t_F$	0.349	$0.239 + 0.055 \cdot \text{SL}$	$0.237 + 0.056 \cdot \text{SL}$	$0.233 + 0.056 \cdot \text{SL}$
	$t_{PHL}$	0.337	$0.282 + 0.027 \cdot \text{SL}$	$0.285 + 0.027 \cdot \text{SL}$	$0.288 + 0.026 \cdot \text{SL}$
SN to QN	$t_F$	0.305	$0.194 + 0.056 \cdot \text{SL}$	$0.191 + 0.056 \cdot \text{SL}$	$0.189 + 0.057 \cdot \text{SL}$
	$t_{PHL}$	0.277	$0.223 + 0.027 \cdot \text{SL}$	$0.225 + 0.027 \cdot \text{SL}$	$0.227 + 0.026 \cdot \text{SL}$
RN1 to QN	$t_R$	0.298	$0.223 + 0.037 \cdot \text{SL}$	$0.226 + 0.037 \cdot \text{SL}$	$0.228 + 0.036 \cdot \text{SL}$
	$t_F$	0.315	$0.208 + 0.054 \cdot \text{SL}$	$0.201 + 0.055 \cdot \text{SL}$	$0.190 + 0.057 \cdot \text{SL}$
	$t_{PLH}$	0.176	$0.123 + 0.026 \cdot \text{SL}$	$0.123 + 0.026 \cdot \text{SL}$	$0.123 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.172	$0.121 + 0.026 \cdot \text{SL}$	$0.120 + 0.026 \cdot \text{SL}$	$0.120 + 0.026 \cdot \text{SL}$
RN2 to QN	$t_R$	0.304	$0.222 + 0.041 \cdot \text{SL}$	$0.232 + 0.038 \cdot \text{SL}$	$0.244 + 0.037 \cdot \text{SL}$
	$t_F$	0.353	$0.248 + 0.053 \cdot \text{SL}$	$0.240 + 0.055 \cdot \text{SL}$	$0.228 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.177	$0.124 + 0.026 \cdot \text{SL}$	$0.124 + 0.026 \cdot \text{SL}$	$0.125 + 0.026 \cdot \text{SL}$
	$t_{PHL}$	0.195	$0.143 + 0.026 \cdot \text{SL}$	$0.143 + 0.026 \cdot \text{SL}$	$0.143 + 0.026 \cdot \text{SL}$
RN to QN	$t_R$	0.214	$0.168 + 0.023 \cdot \text{SL}$	$0.173 + 0.022 \cdot \text{SL}$	$0.175 + 0.022 \cdot \text{SL}$
	$t_F$	0.312	$0.203 + 0.054 \cdot \text{SL}$	$0.198 + 0.056 \cdot \text{SL}$	$0.192 + 0.056 \cdot \text{SL}$
	$t_{PLH}$	0.128	$0.100 + 0.014 \cdot \text{SL}$	$0.102 + 0.013 \cdot \text{SL}$	$0.102 + 0.013 \cdot \text{SL}$
	$t_{PHL}$	0.182	$0.130 + 0.026 \cdot \text{SL}$	$0.130 + 0.026 \cdot \text{SL}$	$0.130 + 0.026 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 8$ , \*Group3 :  $8 < \text{SL}$



## LS1/LS1D2

### SR Latch with Separate Inputs, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , SL: Standard Load)

#### LS1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	$t_R$	0.089	$0.062 + 0.014 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.305	$0.288 + 0.009 \cdot \text{SL}$	$0.294 + 0.007 \cdot \text{SL}$	$0.300 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.313	$0.293 + 0.010 \cdot \text{SL}$	$0.301 + 0.008 \cdot \text{SL}$	$0.311 + 0.007 \cdot \text{SL}$
SN2 to Q	$t_R$	0.090	$0.062 + 0.014 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.058 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.055 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.305	$0.288 + 0.009 \cdot \text{SL}$	$0.294 + 0.007 \cdot \text{SL}$	$0.300 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.342	$0.321 + 0.010 \cdot \text{SL}$	$0.330 + 0.008 \cdot \text{SL}$	$0.340 + 0.007 \cdot \text{SL}$
SN to Q	$t_R$	0.083	$0.054 + 0.015 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.014 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.251	$0.233 + 0.009 \cdot \text{SL}$	$0.239 + 0.007 \cdot \text{SL}$	$0.244 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.323	$0.302 + 0.010 \cdot \text{SL}$	$0.310 + 0.008 \cdot \text{SL}$	$0.320 + 0.007 \cdot \text{SL}$
RN1 to Q	$t_F$	0.086	$0.059 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.474	$0.454 + 0.010 \cdot \text{SL}$	$0.462 + 0.008 \cdot \text{SL}$	$0.472 + 0.007 \cdot \text{SL}$
RN2 to Q	$t_F$	0.087	$0.060 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.055 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.510	$0.489 + 0.010 \cdot \text{SL}$	$0.497 + 0.008 \cdot \text{SL}$	$0.508 + 0.007 \cdot \text{SL}$
RN to Q	$t_F$	0.085	$0.057 + 0.014 \cdot \text{SL}$	$0.061 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.430	$0.410 + 0.010 \cdot \text{SL}$	$0.418 + 0.008 \cdot \text{SL}$	$0.429 + 0.007 \cdot \text{SL}$
SN1 to QN	$t_F$	0.086	$0.060 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.474	$0.454 + 0.010 \cdot \text{SL}$	$0.462 + 0.008 \cdot \text{SL}$	$0.473 + 0.007 \cdot \text{SL}$
SN2 to QN	$t_F$	0.087	$0.058 + 0.014 \cdot \text{SL}$	$0.064 + 0.013 \cdot \text{SL}$	$0.055 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.511	$0.490 + 0.010 \cdot \text{SL}$	$0.499 + 0.008 \cdot \text{SL}$	$0.509 + 0.007 \cdot \text{SL}$
SN to QN	$t_F$	0.086	$0.059 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PHL}$	0.430	$0.409 + 0.010 \cdot \text{SL}$	$0.418 + 0.008 \cdot \text{SL}$	$0.428 + 0.007 \cdot \text{SL}$
RN1 to QN	$t_R$	0.089	$0.062 + 0.014 \cdot \text{SL}$	$0.058 + 0.015 \cdot \text{SL}$	$0.050 + 0.015 \cdot \text{SL}$
	$t_F$	0.086	$0.059 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.302	$0.284 + 0.009 \cdot \text{SL}$	$0.290 + 0.007 \cdot \text{SL}$	$0.296 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.310	$0.290 + 0.010 \cdot \text{SL}$	$0.298 + 0.008 \cdot \text{SL}$	$0.308 + 0.007 \cdot \text{SL}$
RN2 to QN	$t_R$	0.090	$0.061 + 0.014 \cdot \text{SL}$	$0.060 + 0.014 \cdot \text{SL}$	$0.051 + 0.015 \cdot \text{SL}$
	$t_F$	0.087	$0.060 + 0.013 \cdot \text{SL}$	$0.060 + 0.013 \cdot \text{SL}$	$0.056 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.302	$0.284 + 0.009 \cdot \text{SL}$	$0.291 + 0.007 \cdot \text{SL}$	$0.297 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.339	$0.319 + 0.010 \cdot \text{SL}$	$0.327 + 0.008 \cdot \text{SL}$	$0.337 + 0.007 \cdot \text{SL}$
RN to QN	$t_R$	0.083	$0.055 + 0.014 \cdot \text{SL}$	$0.053 + 0.015 \cdot \text{SL}$	$0.046 + 0.015 \cdot \text{SL}$
	$t_F$	0.085	$0.056 + 0.014 \cdot \text{SL}$	$0.062 + 0.013 \cdot \text{SL}$	$0.054 + 0.014 \cdot \text{SL}$
	$t_{PLH}$	0.248	$0.231 + 0.009 \cdot \text{SL}$	$0.236 + 0.007 \cdot \text{SL}$	$0.242 + 0.007 \cdot \text{SL}$
	$t_{PHL}$	0.318	$0.297 + 0.010 \cdot \text{SL}$	$0.305 + 0.008 \cdot \text{SL}$	$0.316 + 0.007 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 13$ , \*Group3 :  $13 < \text{SL}$

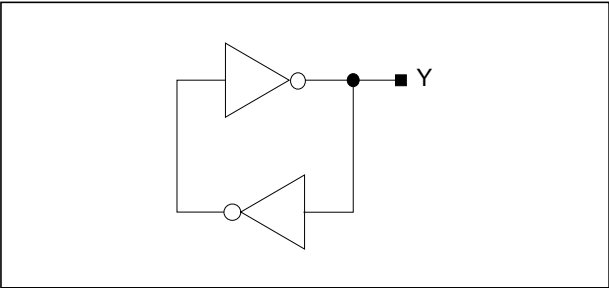


# BUSHOLDER

## Cell List

Cell Name	Function Description
BUSHOLDER	Bus Holder

## Logic Symbol



## Cell Data

Input Load (SL)	Gate Count
Y	1.33
9.3	

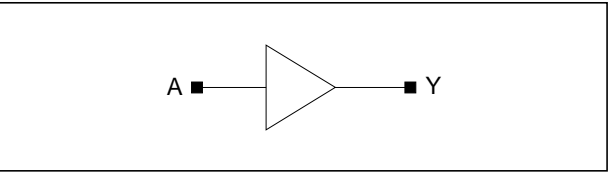


# INTERNAL CLOCK DRIVERS

## Cell List

Cell Name	Function Description
CK2	Internal Clock Driver CMOS 2mA
CK4	Internal Clock Driver CMOS 4mA
CK6	Internal Clock Driver CMOS 6mA
CK8	Internal Clock Driver CMOS 8mA

## Logic Symbol



## Truth Table

A	Y
0	0
1	1

## Cell Data

Standard Load (SL)				I/O Slot			
CK2	CK4	CK6	CK8	CK2	CK4	CK6	CK8
A	A	A	A				
17.524	17.551	25.277	25.271	1.0	1.0	1.0	1.0



## CK2/CK4/CK6/CK8

### Internal Clock Driver CMOS 2/4/6/8mA

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### CK2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t <sub>R</sub>	0.059	$0.053 + 0.003 \cdot SL$	$0.052 + 0.003 \cdot SL$	$0.052 + 0.003 \cdot SL$
	t <sub>F</sub>	0.055	$0.047 + 0.004 \cdot SL$	$0.046 + 0.004 \cdot SL$	$0.045 + 0.004 \cdot SL$
	t <sub>PLH</sub>	0.119	$0.116 + 0.001 \cdot SL$	$0.116 + 0.001 \cdot SL$	$0.116 + 0.001 \cdot SL$
	t <sub>PHL</sub>	0.158	$0.154 + 0.002 \cdot SL$	$0.155 + 0.002 \cdot SL$	$0.155 + 0.002 \cdot SL$

\*Group1 :  $SL < 482$ , \*Group2 :  $482 \leq SL \leq 722$ , \*Group3 :  $722 < SL$

##### CK4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t <sub>R</sub>	0.059	$0.056 + 0.002 \cdot SL$	$0.054 + 0.002 \cdot SL$	$0.054 + 0.002 \cdot SL$
	t <sub>F</sub>	0.056	$0.052 + 0.002 \cdot SL$	$0.049 + 0.002 \cdot SL$	$0.048 + 0.002 \cdot SL$
	t <sub>PLH</sub>	0.145	$0.143 + 0.001 \cdot SL$	$0.144 + 0.001 \cdot SL$	$0.144 + 0.001 \cdot SL$
	t <sub>PHL</sub>	0.191	$0.189 + 0.001 \cdot SL$	$0.190 + 0.001 \cdot SL$	$0.190 + 0.001 \cdot SL$

\*Group1 :  $SL < 962$ , \*Group2 :  $962 \leq SL \leq 1443$ , \*Group3 :  $1443 < SL$

##### CK6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t <sub>R</sub>	0.060	$0.057 + 0.001 \cdot SL$	$0.055 + 0.001 \cdot SL$	$0.054 + 0.001 \cdot SL$
	t <sub>F</sub>	0.055	$0.052 + 0.001 \cdot SL$	$0.049 + 0.001 \cdot SL$	$0.048 + 0.001 \cdot SL$
	t <sub>PLH</sub>	0.154	$0.153 + 0.000 \cdot SL$	$0.153 + 0.000 \cdot SL$	$0.153 + 0.000 \cdot SL$
	t <sub>PHL</sub>	0.189	$0.188 + 0.001 \cdot SL$	$0.189 + 0.001 \cdot SL$	$0.189 + 0.001 \cdot SL$

\*Group1 :  $SL < 1443$ , \*Group2 :  $1443 \leq SL \leq 2165$ , \*Group3 :  $2165 < SL$

##### CK8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t <sub>R</sub>	0.062	$0.061 + 0.001 \cdot SL$	$0.057 + 0.001 \cdot SL$	$0.056 + 0.001 \cdot SL$
	t <sub>F</sub>	0.058	$0.056 + 0.001 \cdot SL$	$0.051 + 0.001 \cdot SL$	$0.050 + 0.001 \cdot SL$
	t <sub>PLH</sub>	0.173	$0.172 + 0.000 \cdot SL$	$0.173 + 0.000 \cdot SL$	$0.173 + 0.000 \cdot SL$
	t <sub>PHL</sub>	0.212	$0.211 + 0.000 \cdot SL$	$0.212 + 0.000 \cdot SL$	$0.212 + 0.000 \cdot SL$

\*Group1 :  $SL < 1923$ , \*Group2 :  $1923 \leq SL \leq 2887$ , \*Group3 :  $2887 < SL$



### Cell List

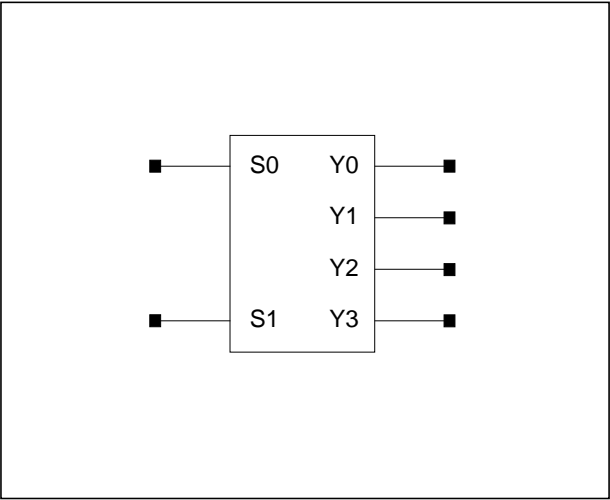
Cell Name	Function Description
DC4	2 > 4 Non-Inverting Decoder
DC4I	2 > 4 Inverting Decoder
DC8I	3 > 8 Inverting Decoder



DC4

2 > 4 Non-Inverting Decoder

Logic Symbol



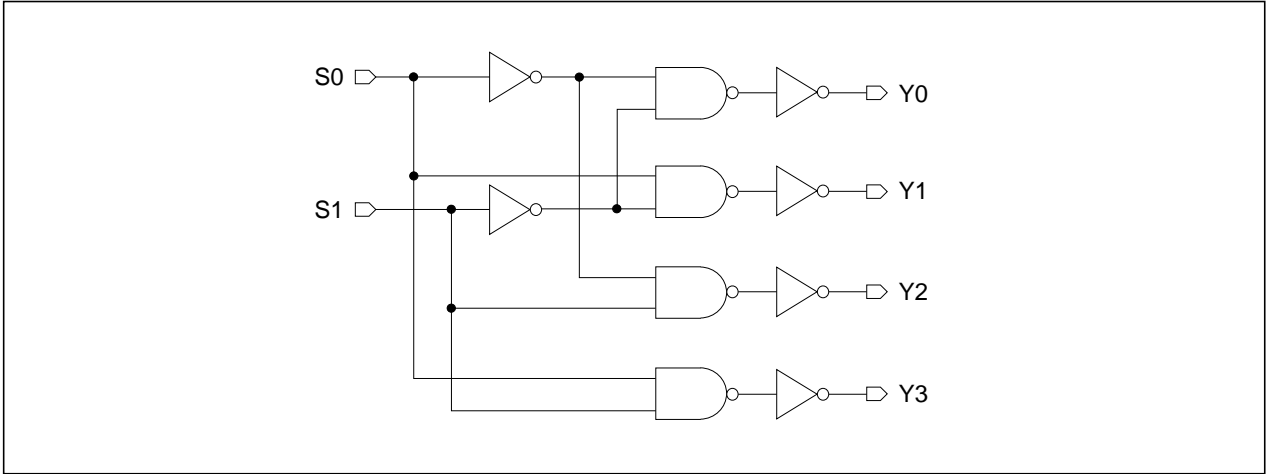
Truth Table

S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Cell Data

Input Load (SL)		Gate Count
S0	S1	
2.5	2.4	6.33

Schematic Diagram





## 2 &gt; 4 Non-Inverting Decoder

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## DC4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to Y0	t <sub>R</sub>	0.118	$0.058 + 0.030 \cdot SL$	$0.057 + 0.030 \cdot SL$	$0.052 + 0.031 \cdot SL$
	t <sub>F</sub>	0.103	$0.048 + 0.027 \cdot SL$	$0.050 + 0.027 \cdot SL$	$0.044 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.235	$0.204 + 0.016 \cdot SL$	$0.211 + 0.014 \cdot SL$	$0.214 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.226	$0.193 + 0.017 \cdot SL$	$0.200 + 0.015 \cdot SL$	$0.203 + 0.014 \cdot SL$
S1 to Y0	t <sub>R</sub>	0.117	$0.059 + 0.029 \cdot SL$	$0.056 + 0.030 \cdot SL$	$0.051 + 0.031 \cdot SL$
	t <sub>F</sub>	0.107	$0.056 + 0.026 \cdot SL$	$0.052 + 0.027 \cdot SL$	$0.046 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.237	$0.206 + 0.016 \cdot SL$	$0.213 + 0.014 \cdot SL$	$0.216 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.243	$0.209 + 0.017 \cdot SL$	$0.217 + 0.015 \cdot SL$	$0.220 + 0.015 \cdot SL$
S0 to Y1	t <sub>R</sub>	0.118	$0.059 + 0.029 \cdot SL$	$0.056 + 0.030 \cdot SL$	$0.052 + 0.031 \cdot SL$
	t <sub>F</sub>	0.104	$0.051 + 0.027 \cdot SL$	$0.050 + 0.027 \cdot SL$	$0.045 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.148	$0.117 + 0.015 \cdot SL$	$0.123 + 0.014 \cdot SL$	$0.126 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.158	$0.126 + 0.016 \cdot SL$	$0.132 + 0.015 \cdot SL$	$0.135 + 0.014 \cdot SL$
S1 to Y1	t <sub>R</sub>	0.119	$0.061 + 0.029 \cdot SL$	$0.058 + 0.030 \cdot SL$	$0.052 + 0.031 \cdot SL$
	t <sub>F</sub>	0.106	$0.054 + 0.026 \cdot SL$	$0.051 + 0.027 \cdot SL$	$0.045 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.231	$0.200 + 0.015 \cdot SL$	$0.206 + 0.014 \cdot SL$	$0.209 + 0.013 \cdot SL$
	t <sub>PHL</sub>	0.238	$0.205 + 0.016 \cdot SL$	$0.212 + 0.015 \cdot SL$	$0.215 + 0.014 \cdot SL$
S0 to Y2	t <sub>R</sub>	0.119	$0.060 + 0.029 \cdot SL$	$0.057 + 0.030 \cdot SL$	$0.052 + 0.031 \cdot SL$
	t <sub>F</sub>	0.104	$0.050 + 0.027 \cdot SL$	$0.050 + 0.027 \cdot SL$	$0.045 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.236	$0.204 + 0.016 \cdot SL$	$0.211 + 0.014 \cdot SL$	$0.215 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.226	$0.193 + 0.017 \cdot SL$	$0.200 + 0.015 \cdot SL$	$0.203 + 0.014 \cdot SL$
S1 to Y2	t <sub>R</sub>	0.120	$0.061 + 0.029 \cdot SL$	$0.060 + 0.030 \cdot SL$	$0.053 + 0.031 \cdot SL$
	t <sub>F</sub>	0.108	$0.055 + 0.026 \cdot SL$	$0.054 + 0.027 \cdot SL$	$0.047 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.148	$0.117 + 0.016 \cdot SL$	$0.124 + 0.014 \cdot SL$	$0.127 + 0.013 \cdot SL$
	t <sub>PHL</sub>	0.177	$0.144 + 0.017 \cdot SL$	$0.151 + 0.015 \cdot SL$	$0.154 + 0.014 \cdot SL$
S0 to Y3	t <sub>R</sub>	0.120	$0.061 + 0.029 \cdot SL$	$0.059 + 0.030 \cdot SL$	$0.053 + 0.031 \cdot SL$
	t <sub>F</sub>	0.102	$0.051 + 0.025 \cdot SL$	$0.051 + 0.025 \cdot SL$	$0.046 + 0.026 \cdot SL$
	t <sub>PLH</sub>	0.151	$0.121 + 0.015 \cdot SL$	$0.126 + 0.014 \cdot SL$	$0.130 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.159	$0.127 + 0.016 \cdot SL$	$0.133 + 0.014 \cdot SL$	$0.137 + 0.014 \cdot SL$
S1 to Y3	t <sub>R</sub>	0.120	$0.062 + 0.029 \cdot SL$	$0.059 + 0.030 \cdot SL$	$0.053 + 0.031 \cdot SL$
	t <sub>F</sub>	0.104	$0.054 + 0.025 \cdot SL$	$0.053 + 0.025 \cdot SL$	$0.047 + 0.026 \cdot SL$
	t <sub>PLH</sub>	0.143	$0.113 + 0.015 \cdot SL$	$0.119 + 0.014 \cdot SL$	$0.122 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.171	$0.139 + 0.016 \cdot SL$	$0.145 + 0.014 \cdot SL$	$0.149 + 0.014 \cdot SL$

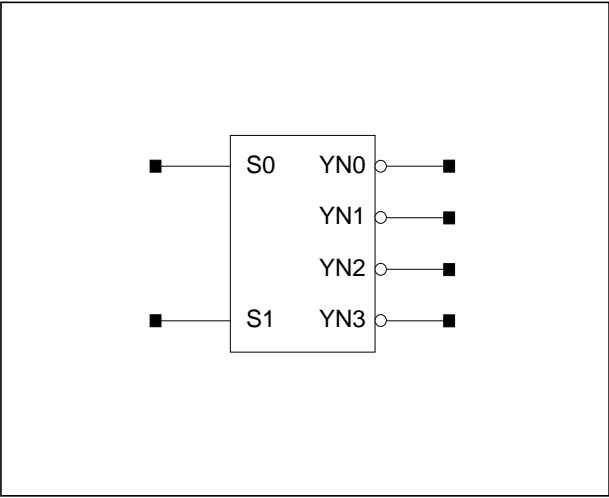
\*Group1 : SL < 4, \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



DC4I

2 > 4 Inverting Decoder

Logic Symbol



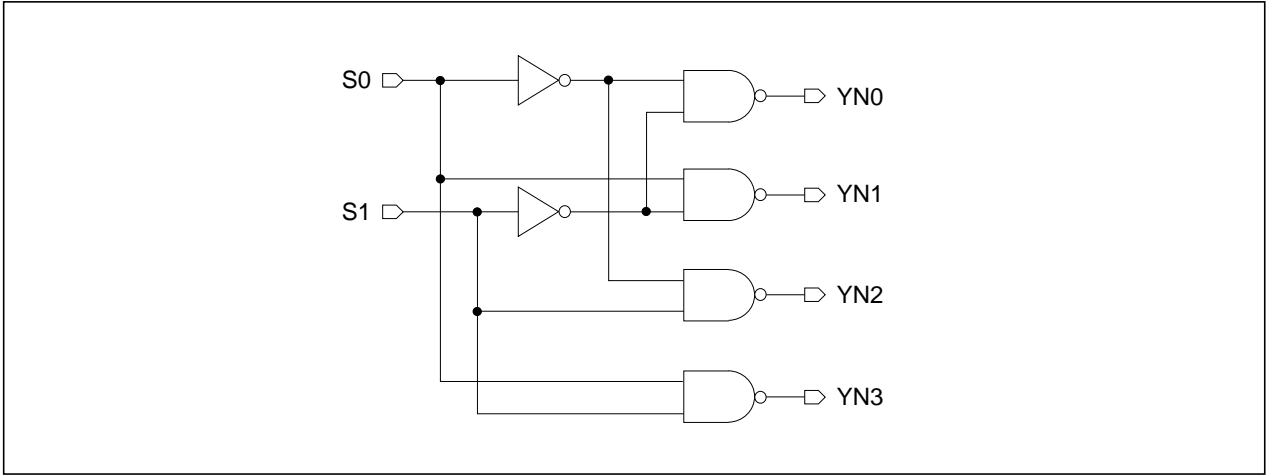
Truth Table

S1	S0	YN0	YN1	YN2	YN3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)		Gate Count
S0	S1	
2.9	3.1	
		4.00

Schematic Diagram





## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## DC4I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	$t_R$	0.124	$0.067 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$	$0.057 + 0.031 \cdot SL$
	$t_F$	0.138	$0.076 + 0.031 \cdot SL$	$0.073 + 0.032 \cdot SL$	$0.067 + 0.033 \cdot SL$
	$t_{PLH}$	0.172	$0.141 + 0.015 \cdot SL$	$0.147 + 0.014 \cdot SL$	$0.150 + 0.013 \cdot SL$
	$t_{PHL}$	0.190	$0.154 + 0.018 \cdot SL$	$0.161 + 0.016 \cdot SL$	$0.165 + 0.016 \cdot SL$
S1 to YN0	$t_R$	0.141	$0.084 + 0.028 \cdot SL$	$0.078 + 0.030 \cdot SL$	$0.071 + 0.031 \cdot SL$
	$t_F$	0.133	$0.071 + 0.031 \cdot SL$	$0.067 + 0.032 \cdot SL$	$0.061 + 0.033 \cdot SL$
	$t_{PLH}$	0.183	$0.154 + 0.015 \cdot SL$	$0.157 + 0.014 \cdot SL$	$0.159 + 0.014 \cdot SL$
	$t_{PHL}$	0.191	$0.156 + 0.017 \cdot SL$	$0.161 + 0.016 \cdot SL$	$0.163 + 0.016 \cdot SL$
S0 to YN1	$t_R$	0.144	$0.092 + 0.026 \cdot SL$	$0.082 + 0.029 \cdot SL$	$0.070 + 0.030 \cdot SL$
	$t_F$	0.152	$0.096 + 0.028 \cdot SL$	$0.086 + 0.030 \cdot SL$	$0.071 + 0.032 \cdot SL$
	$t_{PLH}$	0.089	$0.056 + 0.016 \cdot SL$	$0.068 + 0.013 \cdot SL$	$0.068 + 0.013 \cdot SL$
	$t_{PHL}$	0.090	$0.054 + 0.018 \cdot SL$	$0.064 + 0.015 \cdot SL$	$0.062 + 0.016 \cdot SL$
S1 to YN1	$t_R$	0.140	$0.083 + 0.029 \cdot SL$	$0.078 + 0.030 \cdot SL$	$0.072 + 0.031 \cdot SL$
	$t_F$	0.133	$0.070 + 0.031 \cdot SL$	$0.067 + 0.032 \cdot SL$	$0.061 + 0.033 \cdot SL$
	$t_{PLH}$	0.184	$0.155 + 0.014 \cdot SL$	$0.159 + 0.014 \cdot SL$	$0.160 + 0.013 \cdot SL$
	$t_{PHL}$	0.192	$0.157 + 0.017 \cdot SL$	$0.162 + 0.016 \cdot SL$	$0.164 + 0.016 \cdot SL$
S0 to YN2	$t_R$	0.126	$0.069 + 0.029 \cdot SL$	$0.062 + 0.030 \cdot SL$	$0.058 + 0.031 \cdot SL$
	$t_F$	0.138	$0.075 + 0.031 \cdot SL$	$0.073 + 0.032 \cdot SL$	$0.068 + 0.033 \cdot SL$
	$t_{PLH}$	0.174	$0.144 + 0.015 \cdot SL$	$0.149 + 0.014 \cdot SL$	$0.152 + 0.014 \cdot SL$
	$t_{PHL}$	0.193	$0.157 + 0.018 \cdot SL$	$0.164 + 0.016 \cdot SL$	$0.167 + 0.016 \cdot SL$
S1 to YN2	$t_R$	0.160	$0.110 + 0.025 \cdot SL$	$0.098 + 0.028 \cdot SL$	$0.086 + 0.030 \cdot SL$
	$t_F$	0.144	$0.089 + 0.028 \cdot SL$	$0.077 + 0.031 \cdot SL$	$0.064 + 0.032 \cdot SL$
	$t_{PLH}$	0.100	$0.069 + 0.015 \cdot SL$	$0.078 + 0.013 \cdot SL$	$0.078 + 0.013 \cdot SL$
	$t_{PHL}$	0.085	$0.049 + 0.018 \cdot SL$	$0.059 + 0.015 \cdot SL$	$0.058 + 0.015 \cdot SL$
S0 to YN3	$t_R$	0.144	$0.092 + 0.026 \cdot SL$	$0.083 + 0.028 \cdot SL$	$0.071 + 0.030 \cdot SL$
	$t_F$	0.152	$0.096 + 0.028 \cdot SL$	$0.086 + 0.030 \cdot SL$	$0.073 + 0.032 \cdot SL$
	$t_{PLH}$	0.090	$0.058 + 0.016 \cdot SL$	$0.070 + 0.013 \cdot SL$	$0.070 + 0.013 \cdot SL$
	$t_{PHL}$	0.092	$0.056 + 0.018 \cdot SL$	$0.066 + 0.016 \cdot SL$	$0.065 + 0.016 \cdot SL$
S1 to YN3	$t_R$	0.161	$0.108 + 0.026 \cdot SL$	$0.099 + 0.028 \cdot SL$	$0.086 + 0.030 \cdot SL$
	$t_F$	0.144	$0.087 + 0.028 \cdot SL$	$0.076 + 0.031 \cdot SL$	$0.066 + 0.032 \cdot SL$
	$t_{PLH}$	0.102	$0.071 + 0.015 \cdot SL$	$0.079 + 0.013 \cdot SL$	$0.078 + 0.013 \cdot SL$
	$t_{PHL}$	0.084	$0.049 + 0.018 \cdot SL$	$0.056 + 0.016 \cdot SL$	$0.056 + 0.016 \cdot SL$

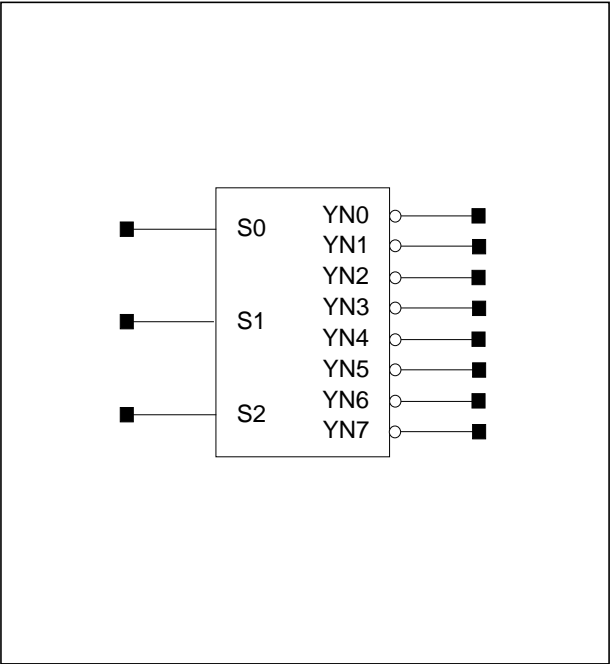
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



DC8I

3 > 8 Inverting Decoder

Logic Symbol



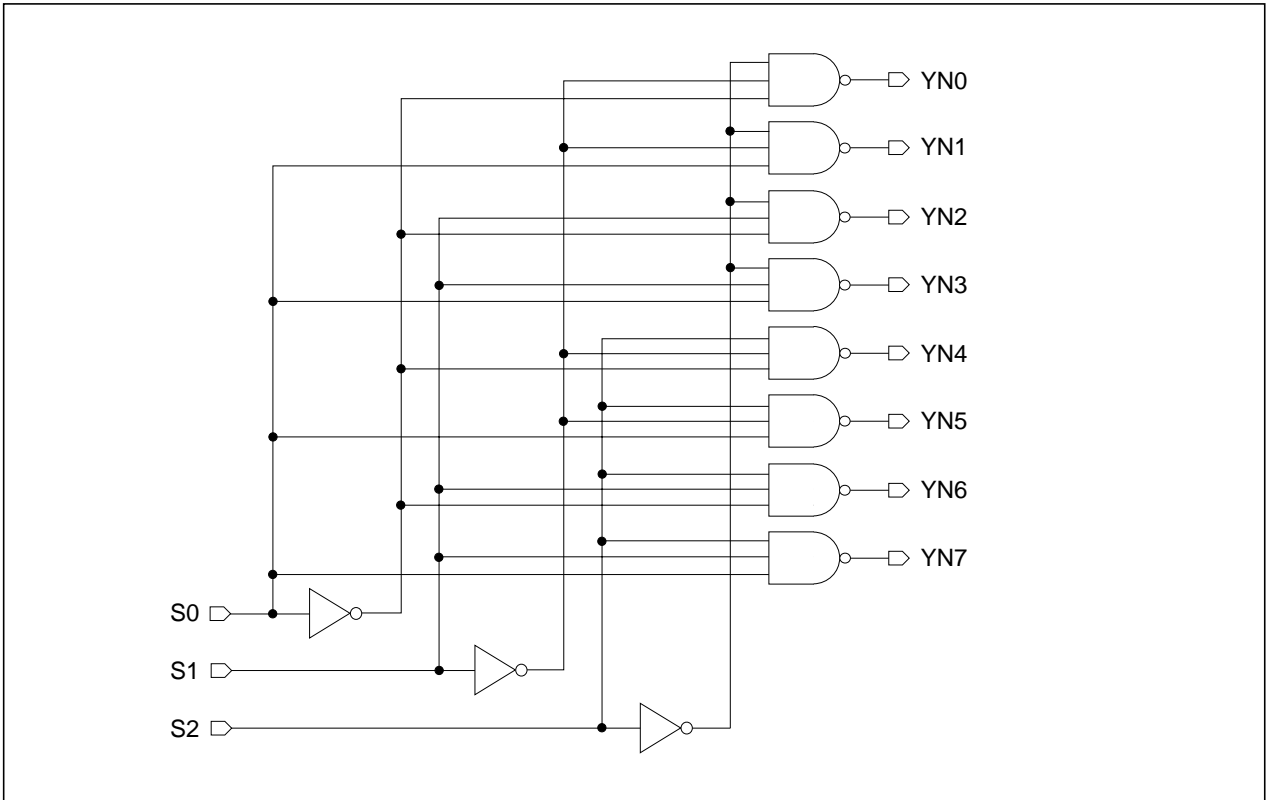
Truth Table

S2	S1	S0	YN0	YN1	YN2	YN3	YN4	YN5	YN6	YN7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Cell Data

Input Load (SL)			Gate Count
S0	S1	S2	
5.0	5.0	5.1	10.67

Schematic Diagram





## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	$t_R$	0.181	$0.099 + 0.041 \cdot SL$	$0.097 + 0.042 \cdot SL$	$0.090 + 0.042 \cdot SL$
	$t_F$	0.200	$0.113 + 0.043 \cdot SL$	$0.109 + 0.044 \cdot SL$	$0.103 + 0.045 \cdot SL$
	$t_{PLH}$	0.235	$0.194 + 0.021 \cdot SL$	$0.200 + 0.019 \cdot SL$	$0.203 + 0.019 \cdot SL$
	$t_{PHL}$	0.228	$0.183 + 0.022 \cdot SL$	$0.188 + 0.021 \cdot SL$	$0.189 + 0.021 \cdot SL$
S1 to YN0	$t_R$	0.195	$0.120 + 0.038 \cdot SL$	$0.115 + 0.039 \cdot SL$	$0.108 + 0.040 \cdot SL$
	$t_F$	0.198	$0.112 + 0.043 \cdot SL$	$0.107 + 0.045 \cdot SL$	$0.100 + 0.045 \cdot SL$
	$t_{PLH}$	0.256	$0.217 + 0.019 \cdot SL$	$0.222 + 0.018 \cdot SL$	$0.226 + 0.018 \cdot SL$
	$t_{PHL}$	0.236	$0.191 + 0.023 \cdot SL$	$0.195 + 0.021 \cdot SL$	$0.198 + 0.021 \cdot SL$
S2 to YN0	$t_R$	0.226	$0.147 + 0.040 \cdot SL$	$0.140 + 0.041 \cdot SL$	$0.131 + 0.042 \cdot SL$
	$t_F$	0.193	$0.105 + 0.044 \cdot SL$	$0.100 + 0.045 \cdot SL$	$0.096 + 0.046 \cdot SL$
	$t_{PLH}$	0.266	$0.227 + 0.020 \cdot SL$	$0.230 + 0.019 \cdot SL$	$0.232 + 0.019 \cdot SL$
	$t_{PHL}$	0.230	$0.186 + 0.022 \cdot SL$	$0.188 + 0.021 \cdot SL$	$0.190 + 0.021 \cdot SL$
S0 to YN1	$t_R$	0.181	$0.110 + 0.035 \cdot SL$	$0.099 + 0.038 \cdot SL$	$0.086 + 0.040 \cdot SL$
	$t_F$	0.207	$0.125 + 0.041 \cdot SL$	$0.116 + 0.043 \cdot SL$	$0.102 + 0.045 \cdot SL$
	$t_{PLH}$	0.114	$0.076 + 0.019 \cdot SL$	$0.083 + 0.017 \cdot SL$	$0.081 + 0.017 \cdot SL$
	$t_{PHL}$	0.114	$0.071 + 0.022 \cdot SL$	$0.075 + 0.021 \cdot SL$	$0.073 + 0.021 \cdot SL$
S1 to YN1	$t_R$	0.204	$0.125 + 0.040 \cdot SL$	$0.120 + 0.041 \cdot SL$	$0.113 + 0.042 \cdot SL$
	$t_F$	0.199	$0.112 + 0.043 \cdot SL$	$0.107 + 0.045 \cdot SL$	$0.100 + 0.045 \cdot SL$
	$t_{PLH}$	0.261	$0.221 + 0.020 \cdot SL$	$0.226 + 0.019 \cdot SL$	$0.228 + 0.018 \cdot SL$
	$t_{PHL}$	0.236	$0.191 + 0.023 \cdot SL$	$0.195 + 0.021 \cdot SL$	$0.197 + 0.021 \cdot SL$
S2 to YN1	$t_R$	0.216	$0.142 + 0.037 \cdot SL$	$0.135 + 0.039 \cdot SL$	$0.127 + 0.040 \cdot SL$
	$t_F$	0.193	$0.105 + 0.044 \cdot SL$	$0.100 + 0.045 \cdot SL$	$0.096 + 0.045 \cdot SL$
	$t_{PLH}$	0.260	$0.223 + 0.019 \cdot SL$	$0.227 + 0.018 \cdot SL$	$0.228 + 0.018 \cdot SL$
	$t_{PHL}$	0.231	$0.186 + 0.022 \cdot SL$	$0.189 + 0.021 \cdot SL$	$0.191 + 0.021 \cdot SL$
S0 to YN2	$t_R$	0.182	$0.101 + 0.040 \cdot SL$	$0.098 + 0.041 \cdot SL$	$0.092 + 0.042 \cdot SL$
	$t_F$	0.204	$0.117 + 0.044 \cdot SL$	$0.114 + 0.044 \cdot SL$	$0.106 + 0.045 \cdot SL$
	$t_{PLH}$	0.235	$0.195 + 0.020 \cdot SL$	$0.201 + 0.019 \cdot SL$	$0.204 + 0.018 \cdot SL$
	$t_{PHL}$	0.230	$0.185 + 0.023 \cdot SL$	$0.190 + 0.021 \cdot SL$	$0.192 + 0.021 \cdot SL$
S1 to YN2	$t_R$	0.204	$0.132 + 0.036 \cdot SL$	$0.120 + 0.039 \cdot SL$	$0.109 + 0.040 \cdot SL$
	$t_F$	0.207	$0.124 + 0.041 \cdot SL$	$0.115 + 0.044 \cdot SL$	$0.103 + 0.045 \cdot SL$
	$t_{PLH}$	0.135	$0.098 + 0.018 \cdot SL$	$0.100 + 0.018 \cdot SL$	$0.101 + 0.018 \cdot SL$
	$t_{PHL}$	0.122	$0.078 + 0.022 \cdot SL$	$0.083 + 0.021 \cdot SL$	$0.083 + 0.021 \cdot SL$
S2 to YN2	$t_R$	0.224	$0.147 + 0.038 \cdot SL$	$0.140 + 0.040 \cdot SL$	$0.131 + 0.041 \cdot SL$
	$t_F$	0.196	$0.108 + 0.044 \cdot SL$	$0.104 + 0.045 \cdot SL$	$0.099 + 0.046 \cdot SL$
	$t_{PLH}$	0.265	$0.226 + 0.019 \cdot SL$	$0.230 + 0.018 \cdot SL$	$0.232 + 0.018 \cdot SL$
	$t_{PHL}$	0.232	$0.188 + 0.022 \cdot SL$	$0.191 + 0.021 \cdot SL$	$0.192 + 0.021 \cdot SL$
S0 to YN3	$t_R$	0.181	$0.110 + 0.036 \cdot SL$	$0.100 + 0.038 \cdot SL$	$0.087 + 0.040 \cdot SL$
	$t_F$	0.209	$0.127 + 0.041 \cdot SL$	$0.118 + 0.043 \cdot SL$	$0.104 + 0.045 \cdot SL$
	$t_{PLH}$	0.114	$0.076 + 0.019 \cdot SL$	$0.083 + 0.017 \cdot SL$	$0.082 + 0.017 \cdot SL$
	$t_{PHL}$	0.115	$0.071 + 0.022 \cdot SL$	$0.075 + 0.021 \cdot SL$	$0.074 + 0.021 \cdot SL$



## DC8I

### 3 > 8 Inverting Decoder

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S1 to YN3	$t_R$	0.202	$0.129 + 0.037 \cdot SL$	$0.118 + 0.039 \cdot SL$	$0.107 + 0.041 \cdot SL$
	$t_F$	0.204	$0.120 + 0.042 \cdot SL$	$0.111 + 0.044 \cdot SL$	$0.101 + 0.045 \cdot SL$
	$t_{PLH}$	0.135	$0.099 + 0.018 \cdot SL$	$0.100 + 0.018 \cdot SL$	$0.099 + 0.018 \cdot SL$
	$t_{PHL}$	0.121	$0.077 + 0.022 \cdot SL$	$0.081 + 0.021 \cdot SL$	$0.080 + 0.021 \cdot SL$
S2 to YN3	$t_R$	0.220	$0.144 + 0.038 \cdot SL$	$0.138 + 0.039 \cdot SL$	$0.129 + 0.041 \cdot SL$
	$t_F$	0.195	$0.107 + 0.044 \cdot SL$	$0.102 + 0.045 \cdot SL$	$0.098 + 0.046 \cdot SL$
	$t_{PLH}$	0.264	$0.226 + 0.019 \cdot SL$	$0.230 + 0.018 \cdot SL$	$0.231 + 0.018 \cdot SL$
	$t_{PHL}$	0.232	$0.188 + 0.022 \cdot SL$	$0.191 + 0.021 \cdot SL$	$0.193 + 0.021 \cdot SL$
S0 to YN4	$t_R$	0.182	$0.099 + 0.041 \cdot SL$	$0.097 + 0.042 \cdot SL$	$0.091 + 0.042 \cdot SL$
	$t_F$	0.200	$0.114 + 0.043 \cdot SL$	$0.110 + 0.044 \cdot SL$	$0.103 + 0.045 \cdot SL$
	$t_{PLH}$	0.235	$0.194 + 0.021 \cdot SL$	$0.200 + 0.019 \cdot SL$	$0.203 + 0.019 \cdot SL$
	$t_{PHL}$	0.228	$0.183 + 0.023 \cdot SL$	$0.188 + 0.021 \cdot SL$	$0.190 + 0.021 \cdot SL$
S1 to YN4	$t_R$	0.197	$0.121 + 0.038 \cdot SL$	$0.116 + 0.039 \cdot SL$	$0.109 + 0.040 \cdot SL$
	$t_F$	0.199	$0.112 + 0.043 \cdot SL$	$0.107 + 0.045 \cdot SL$	$0.101 + 0.045 \cdot SL$
	$t_{PLH}$	0.255	$0.217 + 0.019 \cdot SL$	$0.222 + 0.018 \cdot SL$	$0.225 + 0.018 \cdot SL$
	$t_{PHL}$	0.237	$0.191 + 0.023 \cdot SL$	$0.196 + 0.021 \cdot SL$	$0.198 + 0.021 \cdot SL$
S2 to YN4	$t_R$	0.230	$0.154 + 0.038 \cdot SL$	$0.143 + 0.041 \cdot SL$	$0.131 + 0.042 \cdot SL$
	$t_F$	0.198	$0.114 + 0.042 \cdot SL$	$0.105 + 0.044 \cdot SL$	$0.096 + 0.045 \cdot SL$
	$t_{PLH}$	0.143	$0.106 + 0.019 \cdot SL$	$0.107 + 0.019 \cdot SL$	$0.107 + 0.018 \cdot SL$
	$t_{PHL}$	0.113	$0.069 + 0.022 \cdot SL$	$0.074 + 0.021 \cdot SL$	$0.075 + 0.021 \cdot SL$
S0 to YN5	$t_R$	0.180	$0.109 + 0.036 \cdot SL$	$0.099 + 0.038 \cdot SL$	$0.086 + 0.040 \cdot SL$
	$t_F$	0.207	$0.124 + 0.041 \cdot SL$	$0.115 + 0.043 \cdot SL$	$0.102 + 0.045 \cdot SL$
	$t_{PLH}$	0.114	$0.076 + 0.019 \cdot SL$	$0.083 + 0.017 \cdot SL$	$0.081 + 0.017 \cdot SL$
	$t_{PHL}$	0.115	$0.071 + 0.022 \cdot SL$	$0.075 + 0.021 \cdot SL$	$0.073 + 0.021 \cdot SL$
S1 to YN5	$t_R$	0.206	$0.125 + 0.040 \cdot SL$	$0.121 + 0.041 \cdot SL$	$0.113 + 0.042 \cdot SL$
	$t_F$	0.199	$0.112 + 0.043 \cdot SL$	$0.107 + 0.045 \cdot SL$	$0.101 + 0.045 \cdot SL$
	$t_{PLH}$	0.261	$0.220 + 0.020 \cdot SL$	$0.225 + 0.019 \cdot SL$	$0.228 + 0.019 \cdot SL$
	$t_{PHL}$	0.236	$0.191 + 0.023 \cdot SL$	$0.195 + 0.021 \cdot SL$	$0.197 + 0.021 \cdot SL$
S2 to YN5	$t_R$	0.221	$0.150 + 0.035 \cdot SL$	$0.141 + 0.038 \cdot SL$	$0.127 + 0.040 \cdot SL$
	$t_F$	0.197	$0.113 + 0.042 \cdot SL$	$0.104 + 0.045 \cdot SL$	$0.097 + 0.045 \cdot SL$
	$t_{PLH}$	0.137	$0.102 + 0.018 \cdot SL$	$0.103 + 0.017 \cdot SL$	$0.103 + 0.017 \cdot SL$
	$t_{PHL}$	0.113	$0.069 + 0.022 \cdot SL$	$0.072 + 0.021 \cdot SL$	$0.073 + 0.021 \cdot SL$
S0 to YN6	$t_R$	0.181	$0.101 + 0.040 \cdot SL$	$0.098 + 0.041 \cdot SL$	$0.091 + 0.042 \cdot SL$
	$t_F$	0.203	$0.116 + 0.044 \cdot SL$	$0.113 + 0.044 \cdot SL$	$0.106 + 0.045 \cdot SL$
	$t_{PLH}$	0.235	$0.194 + 0.020 \cdot SL$	$0.201 + 0.019 \cdot SL$	$0.204 + 0.018 \cdot SL$
	$t_{PHL}$	0.230	$0.185 + 0.023 \cdot SL$	$0.190 + 0.021 \cdot SL$	$0.192 + 0.021 \cdot SL$
S1 to YN6	$t_R$	0.204	$0.131 + 0.036 \cdot SL$	$0.121 + 0.039 \cdot SL$	$0.109 + 0.040 \cdot SL$
	$t_F$	0.205	$0.122 + 0.041 \cdot SL$	$0.113 + 0.044 \cdot SL$	$0.102 + 0.045 \cdot SL$
	$t_{PLH}$	0.130	$0.093 + 0.018 \cdot SL$	$0.095 + 0.018 \cdot SL$	$0.096 + 0.018 \cdot SL$
	$t_{PHL}$	0.117	$0.073 + 0.022 \cdot SL$	$0.078 + 0.021 \cdot SL$	$0.078 + 0.021 \cdot SL$

(Continued)



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## DC8I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to YN6	$t_R$	0.226	$0.153 + 0.037 \cdot SL$	$0.142 + 0.039 \cdot SL$	$0.130 + 0.041 \cdot SL$
	$t_F$	0.199	$0.114 + 0.042 \cdot SL$	$0.106 + 0.044 \cdot SL$	$0.098 + 0.045 \cdot SL$
	$t_{PLH}$	0.141	$0.105 + 0.018 \cdot SL$	$0.105 + 0.018 \cdot SL$	$0.106 + 0.018 \cdot SL$
	$t_{PHL}$	0.114	$0.070 + 0.022 \cdot SL$	$0.075 + 0.021 \cdot SL$	$0.075 + 0.021 \cdot SL$
S0 to YN7	$t_R$	0.181	$0.110 + 0.036 \cdot SL$	$0.100 + 0.038 \cdot SL$	$0.087 + 0.040 \cdot SL$
	$t_F$	0.209	$0.127 + 0.041 \cdot SL$	$0.118 + 0.043 \cdot SL$	$0.105 + 0.045 \cdot SL$
	$t_{PLH}$	0.114	$0.077 + 0.019 \cdot SL$	$0.083 + 0.017 \cdot SL$	$0.082 + 0.017 \cdot SL$
	$t_{PHL}$	0.115	$0.072 + 0.022 \cdot SL$	$0.075 + 0.021 \cdot SL$	$0.074 + 0.021 \cdot SL$
S1 to YN7	$t_R$	0.204	$0.129 + 0.037 \cdot SL$	$0.118 + 0.040 \cdot SL$	$0.108 + 0.041 \cdot SL$
	$t_F$	0.202	$0.119 + 0.042 \cdot SL$	$0.109 + 0.044 \cdot SL$	$0.100 + 0.045 \cdot SL$
	$t_{PLH}$	0.131	$0.094 + 0.018 \cdot SL$	$0.096 + 0.018 \cdot SL$	$0.095 + 0.018 \cdot SL$
	$t_{PHL}$	0.116	$0.072 + 0.022 \cdot SL$	$0.076 + 0.021 \cdot SL$	$0.074 + 0.021 \cdot SL$
S2 to YN7	$t_R$	0.222	$0.150 + 0.036 \cdot SL$	$0.141 + 0.038 \cdot SL$	$0.128 + 0.040 \cdot SL$
	$t_F$	0.197	$0.112 + 0.043 \cdot SL$	$0.104 + 0.045 \cdot SL$	$0.098 + 0.045 \cdot SL$
	$t_{PLH}$	0.139	$0.103 + 0.018 \cdot SL$	$0.104 + 0.018 \cdot SL$	$0.104 + 0.018 \cdot SL$
	$t_{PHL}$	0.113	$0.070 + 0.022 \cdot SL$	$0.073 + 0.021 \cdot SL$	$0.072 + 0.021 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## ADDERS

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### Cell List

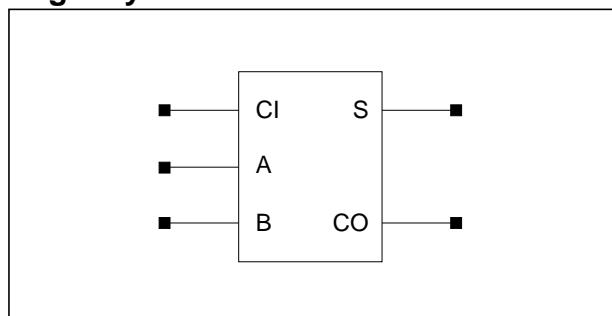
Cell Name	Function Description
FADH	Full Adder with 0.5X Drive
FA	Full Adder with 1X Drive
FAD2	Full Adder with 2X Drive
HADH	Half Adder with 0.5x Drive
HA	Half Adder with 1x Drive
HAD2	Half Adder with 2X Drive
SCG23	Full Adder with one inverted input, 1X Drive
SCG23D2	Full Adder with one inverted input, 2X Drive



# FADH/FA/FAD2

## Full Adder with 0.5X/1X/2X Drive

### Logic Symbol



### Truth Table

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	0	1	1	0
1	0	1	0	1
0	1	0	1	0
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

### Cell Data

Input Load (SL)									Gate Count		
FADH			FA			FAD2			FADH	FA	FAD2
CI	A	B	CI	A	B	CI	A	B			
0.5	0.8	0.8	0.5	1.0	1.0	0.5	1.0	1.0	6.00	6.33	6.67

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### FADH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	$t_R$	0.224	$0.093 + 0.066 \cdot SL$	$0.086 + 0.067 \cdot SL$	$0.076 + 0.069 \cdot SL$
	$t_F$	0.192	$0.089 + 0.051 \cdot SL$	$0.093 + 0.050 \cdot SL$	$0.087 + 0.051 \cdot SL$
	$t_{PLH}$	0.448	$0.381 + 0.033 \cdot SL$	$0.392 + 0.031 \cdot SL$	$0.396 + 0.030 \cdot SL$
	$t_{PHL}$	0.462	$0.395 + 0.033 \cdot SL$	$0.412 + 0.029 \cdot SL$	$0.426 + 0.028 \cdot SL$
B to S	$t_R$	0.227	$0.096 + 0.065 \cdot SL$	$0.088 + 0.067 \cdot SL$	$0.077 + 0.069 \cdot SL$
	$t_F$	0.195	$0.092 + 0.051 \cdot SL$	$0.095 + 0.050 \cdot SL$	$0.089 + 0.051 \cdot SL$
	$t_{PLH}$	0.511	$0.445 + 0.033 \cdot SL$	$0.456 + 0.031 \cdot SL$	$0.459 + 0.030 \cdot SL$
	$t_{PHL}$	0.530	$0.463 + 0.034 \cdot SL$	$0.481 + 0.029 \cdot SL$	$0.495 + 0.028 \cdot SL$
CI to S	$t_R$	0.230	$0.100 + 0.065 \cdot SL$	$0.092 + 0.067 \cdot SL$	$0.079 + 0.069 \cdot SL$
	$t_F$	0.214	$0.114 + 0.050 \cdot SL$	$0.118 + 0.049 \cdot SL$	$0.106 + 0.050 \cdot SL$
	$t_{PLH}$	0.422	$0.357 + 0.033 \cdot SL$	$0.367 + 0.030 \cdot SL$	$0.369 + 0.030 \cdot SL$
	$t_{PHL}$	0.407	$0.341 + 0.033 \cdot SL$	$0.359 + 0.029 \cdot SL$	$0.369 + 0.027 \cdot SL$
A to CO	$t_R$	0.220	$0.088 + 0.066 \cdot SL$	$0.081 + 0.068 \cdot SL$	$0.072 + 0.069 \cdot SL$
	$t_F$	0.190	$0.087 + 0.052 \cdot SL$	$0.091 + 0.051 \cdot SL$	$0.087 + 0.051 \cdot SL$
	$t_{PLH}$	0.430	$0.365 + 0.032 \cdot SL$	$0.374 + 0.030 \cdot SL$	$0.377 + 0.030 \cdot SL$
	$t_{PHL}$	0.444	$0.379 + 0.032 \cdot SL$	$0.395 + 0.029 \cdot SL$	$0.405 + 0.027 \cdot SL$
B to CO	$t_R$	0.261	$0.142 + 0.060 \cdot SL$	$0.122 + 0.065 \cdot SL$	$0.095 + 0.068 \cdot SL$
	$t_F$	0.221	$0.126 + 0.048 \cdot SL$	$0.124 + 0.048 \cdot SL$	$0.105 + 0.050 \cdot SL$
	$t_{PLH}$	0.493	$0.428 + 0.032 \cdot SL$	$0.436 + 0.030 \cdot SL$	$0.439 + 0.030 \cdot SL$
	$t_{PHL}$	0.521	$0.456 + 0.033 \cdot SL$	$0.472 + 0.029 \cdot SL$	$0.482 + 0.027 \cdot SL$
CI to CO	$t_R$	0.230	$0.101 + 0.065 \cdot SL$	$0.091 + 0.067 \cdot SL$	$0.081 + 0.068 \cdot SL$
	$t_F$	0.214	$0.111 + 0.051 \cdot SL$	$0.119 + 0.049 \cdot SL$	$0.112 + 0.050 \cdot SL$
	$t_{PLH}$	0.309	$0.240 + 0.035 \cdot SL$	$0.256 + 0.031 \cdot SL$	$0.261 + 0.030 \cdot SL$
	$t_{PHL}$	0.324	$0.249 + 0.037 \cdot SL$	$0.278 + 0.030 \cdot SL$	$0.298 + 0.028 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## FADH/FA/FAD2

### Full Adder with 0.5X/1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

FA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	$t_R$	0.151	$0.092 + 0.029 \cdot SL$	$0.093 + 0.029 \cdot SL$	$0.087 + 0.030 \cdot SL$
	$t_F$	0.149	$0.094 + 0.028 \cdot SL$	$0.100 + 0.026 \cdot SL$	$0.105 + 0.025 \cdot SL$
	$t_{PLH}$	0.424	$0.389 + 0.018 \cdot SL$	$0.399 + 0.015 \cdot SL$	$0.409 + 0.014 \cdot SL$
	$t_{PHL}$	0.427	$0.386 + 0.020 \cdot SL$	$0.398 + 0.017 \cdot SL$	$0.415 + 0.015 \cdot SL$
B to S	$t_R$	0.153	$0.095 + 0.029 \cdot SL$	$0.094 + 0.029 \cdot SL$	$0.090 + 0.030 \cdot SL$
	$t_F$	0.153	$0.098 + 0.028 \cdot SL$	$0.104 + 0.026 \cdot SL$	$0.111 + 0.025 \cdot SL$
	$t_{PLH}$	0.491	$0.455 + 0.018 \cdot SL$	$0.465 + 0.015 \cdot SL$	$0.475 + 0.014 \cdot SL$
	$t_{PHL}$	0.502	$0.462 + 0.020 \cdot SL$	$0.475 + 0.017 \cdot SL$	$0.491 + 0.015 \cdot SL$
CI to S	$t_R$	0.159	$0.099 + 0.030 \cdot SL$	$0.103 + 0.029 \cdot SL$	$0.098 + 0.030 \cdot SL$
	$t_F$	0.175	$0.121 + 0.027 \cdot SL$	$0.128 + 0.025 \cdot SL$	$0.133 + 0.025 \cdot SL$
	$t_{PLH}$	0.458	$0.423 + 0.018 \cdot SL$	$0.433 + 0.015 \cdot SL$	$0.443 + 0.014 \cdot SL$
	$t_{PHL}$	0.442	$0.402 + 0.020 \cdot SL$	$0.416 + 0.017 \cdot SL$	$0.432 + 0.015 \cdot SL$
A to CO	$t_R$	0.143	$0.082 + 0.030 \cdot SL$	$0.084 + 0.030 \cdot SL$	$0.083 + 0.030 \cdot SL$
	$t_F$	0.144	$0.087 + 0.029 \cdot SL$	$0.095 + 0.026 \cdot SL$	$0.103 + 0.026 \cdot SL$
	$t_{PLH}$	0.396	$0.363 + 0.016 \cdot SL$	$0.371 + 0.014 \cdot SL$	$0.377 + 0.014 \cdot SL$
	$t_{PHL}$	0.392	$0.356 + 0.018 \cdot SL$	$0.366 + 0.016 \cdot SL$	$0.377 + 0.014 \cdot SL$
B to CO	$t_R$	0.193	$0.138 + 0.027 \cdot SL$	$0.139 + 0.027 \cdot SL$	$0.127 + 0.028 \cdot SL$
	$t_F$	0.178	$0.128 + 0.025 \cdot SL$	$0.131 + 0.024 \cdot SL$	$0.128 + 0.025 \cdot SL$
	$t_{PLH}$	0.461	$0.427 + 0.017 \cdot SL$	$0.436 + 0.014 \cdot SL$	$0.442 + 0.014 \cdot SL$
	$t_{PHL}$	0.470	$0.434 + 0.018 \cdot SL$	$0.444 + 0.016 \cdot SL$	$0.455 + 0.014 \cdot SL$
CI to CO	$t_R$	0.159	$0.100 + 0.030 \cdot SL$	$0.103 + 0.029 \cdot SL$	$0.097 + 0.030 \cdot SL$
	$t_F$	0.173	$0.118 + 0.027 \cdot SL$	$0.124 + 0.026 \cdot SL$	$0.132 + 0.025 \cdot SL$
	$t_{PLH}$	0.297	$0.259 + 0.019 \cdot SL$	$0.272 + 0.016 \cdot SL$	$0.284 + 0.014 \cdot SL$
	$t_{PHL}$	0.320	$0.275 + 0.023 \cdot SL$	$0.293 + 0.018 \cdot SL$	$0.313 + 0.016 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## FAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	$t_R$	0.135	$0.107 + 0.014 \cdot SL$	$0.106 + 0.014 \cdot SL$	$0.107 + 0.014 \cdot SL$
	$t_F$	0.139	$0.108 + 0.016 \cdot SL$	$0.114 + 0.014 \cdot SL$	$0.124 + 0.013 \cdot SL$
	$t_{PLH}$	0.429	$0.406 + 0.011 \cdot SL$	$0.417 + 0.009 \cdot SL$	$0.435 + 0.007 \cdot SL$
	$t_{PHL}$	0.438	$0.410 + 0.014 \cdot SL$	$0.424 + 0.010 \cdot SL$	$0.448 + 0.009 \cdot SL$
B to S	$t_R$	0.131	$0.103 + 0.014 \cdot SL$	$0.100 + 0.015 \cdot SL$	$0.102 + 0.014 \cdot SL$
	$t_F$	0.143	$0.111 + 0.016 \cdot SL$	$0.118 + 0.014 \cdot SL$	$0.127 + 0.013 \cdot SL$
	$t_{PLH}$	0.492	$0.469 + 0.012 \cdot SL$	$0.481 + 0.009 \cdot SL$	$0.499 + 0.007 \cdot SL$
	$t_{PHL}$	0.510	$0.482 + 0.014 \cdot SL$	$0.496 + 0.010 \cdot SL$	$0.521 + 0.009 \cdot SL$
CI to S	$t_R$	0.134	$0.104 + 0.015 \cdot SL$	$0.106 + 0.014 \cdot SL$	$0.107 + 0.014 \cdot SL$
	$t_F$	0.162	$0.129 + 0.016 \cdot SL$	$0.140 + 0.014 \cdot SL$	$0.147 + 0.013 \cdot SL$
	$t_{PLH}$	0.505	$0.482 + 0.012 \cdot SL$	$0.494 + 0.009 \cdot SL$	$0.513 + 0.007 \cdot SL$
	$t_{PHL}$	0.488	$0.461 + 0.014 \cdot SL$	$0.475 + 0.010 \cdot SL$	$0.499 + 0.008 \cdot SL$
A to CO	$t_R$	0.121	$0.092 + 0.015 \cdot SL$	$0.091 + 0.015 \cdot SL$	$0.094 + 0.015 \cdot SL$
	$t_F$	0.138	$0.107 + 0.016 \cdot SL$	$0.112 + 0.014 \cdot SL$	$0.123 + 0.014 \cdot SL$
	$t_{PLH}$	0.400	$0.379 + 0.010 \cdot SL$	$0.389 + 0.008 \cdot SL$	$0.402 + 0.007 \cdot SL$
	$t_{PHL}$	0.400	$0.376 + 0.012 \cdot SL$	$0.386 + 0.009 \cdot SL$	$0.405 + 0.008 \cdot SL$
B to CO	$t_R$	0.188	$0.166 + 0.011 \cdot SL$	$0.160 + 0.012 \cdot SL$	$0.146 + 0.014 \cdot SL$
	$t_F$	0.181	$0.157 + 0.012 \cdot SL$	$0.156 + 0.012 \cdot SL$	$0.152 + 0.013 \cdot SL$
	$t_{PLH}$	0.462	$0.440 + 0.011 \cdot SL$	$0.451 + 0.008 \cdot SL$	$0.465 + 0.007 \cdot SL$
	$t_{PHL}$	0.474	$0.450 + 0.012 \cdot SL$	$0.461 + 0.009 \cdot SL$	$0.481 + 0.008 \cdot SL$
CI to CO	$t_R$	0.133	$0.104 + 0.015 \cdot SL$	$0.103 + 0.015 \cdot SL$	$0.107 + 0.014 \cdot SL$
	$t_F$	0.160	$0.128 + 0.016 \cdot SL$	$0.136 + 0.014 \cdot SL$	$0.146 + 0.013 \cdot SL$
	$t_{PLH}$	0.302	$0.277 + 0.012 \cdot SL$	$0.290 + 0.009 \cdot SL$	$0.311 + 0.007 \cdot SL$
	$t_{PHL}$	0.333	$0.303 + 0.015 \cdot SL$	$0.319 + 0.011 \cdot SL$	$0.349 + 0.009 \cdot SL$

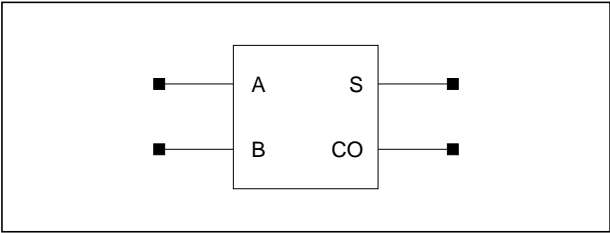
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



HADH/HA/HAD2

Half Adder with 0.5X/1X/2X Drive

Logic Symbol



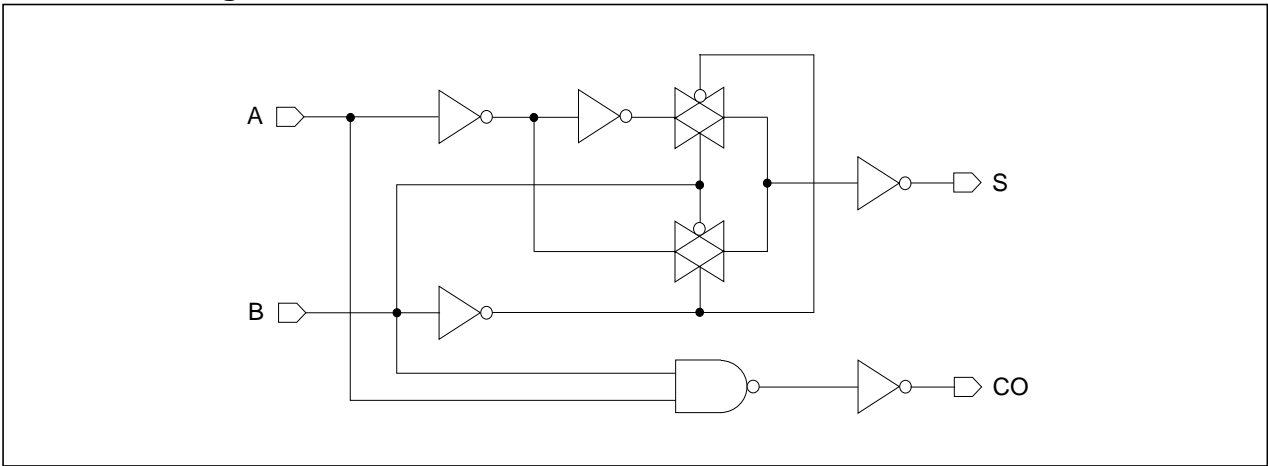
Truth Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Data

Input Load (SL)						Gate Count		
HADH		HA		HAD2		HADH	HA	HAD2
A	B	A	B	A	B			
1.1	1.6	1.3	1.9	1.3	2.2	3.67	3.67	4.00

Schematic Diagram





## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## HADH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	$t_R$	0.206	$0.081 + 0.063*SL$	$0.074 + 0.064*SL$	$0.063 + 0.066*SL$
	$t_F$	0.198	$0.099 + 0.050*SL$	$0.101 + 0.049*SL$	$0.087 + 0.051*SL$
	$t_{PLH}$	0.302	$0.241 + 0.031*SL$	$0.248 + 0.029*SL$	$0.250 + 0.029*SL$
	$t_{PHL}$	0.306	$0.239 + 0.033*SL$	$0.258 + 0.029*SL$	$0.268 + 0.027*SL$
B to S	$t_R$	0.201	$0.073 + 0.064*SL$	$0.069 + 0.065*SL$	$0.060 + 0.066*SL$
	$t_F$	0.183	$0.082 + 0.051*SL$	$0.084 + 0.050*SL$	$0.075 + 0.051*SL$
	$t_{PLH}$	0.242	$0.180 + 0.031*SL$	$0.189 + 0.029*SL$	$0.191 + 0.029*SL$
	$t_{PHL}$	0.254	$0.188 + 0.033*SL$	$0.205 + 0.029*SL$	$0.216 + 0.027*SL$
A to CO	$t_R$	0.199	$0.068 + 0.066*SL$	$0.060 + 0.068*SL$	$0.053 + 0.068*SL$
	$t_F$	0.157	$0.057 + 0.050*SL$	$0.052 + 0.051*SL$	$0.044 + 0.052*SL$
	$t_{PLH}$	0.187	$0.125 + 0.031*SL$	$0.130 + 0.030*SL$	$0.131 + 0.030*SL$
	$t_{PHL}$	0.203	$0.145 + 0.029*SL$	$0.152 + 0.027*SL$	$0.153 + 0.027*SL$
B to CO	$t_R$	0.199	$0.068 + 0.066*SL$	$0.060 + 0.068*SL$	$0.053 + 0.068*SL$
	$t_F$	0.156	$0.057 + 0.050*SL$	$0.048 + 0.052*SL$	$0.042 + 0.052*SL$
	$t_{PLH}$	0.192	$0.130 + 0.031*SL$	$0.135 + 0.030*SL$	$0.135 + 0.030*SL$
	$t_{PHL}$	0.189	$0.131 + 0.029*SL$	$0.137 + 0.027*SL$	$0.138 + 0.027*SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$ 

## HA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	$t_R$	0.143	$0.084 + 0.029*SL$	$0.084 + 0.029*SL$	$0.079 + 0.030*SL$
	$t_F$	0.153	$0.100 + 0.026*SL$	$0.106 + 0.025*SL$	$0.107 + 0.025*SL$
	$t_{PLH}$	0.303	$0.268 + 0.017*SL$	$0.278 + 0.015*SL$	$0.286 + 0.014*SL$
	$t_{PHL}$	0.304	$0.265 + 0.020*SL$	$0.278 + 0.016*SL$	$0.294 + 0.015*SL$
B to S	$t_R$	0.136	$0.076 + 0.030*SL$	$0.078 + 0.030*SL$	$0.073 + 0.030*SL$
	$t_F$	0.138	$0.084 + 0.027*SL$	$0.089 + 0.025*SL$	$0.092 + 0.025*SL$
	$t_{PLH}$	0.223	$0.188 + 0.017*SL$	$0.198 + 0.015*SL$	$0.207 + 0.014*SL$
	$t_{PHL}$	0.237	$0.197 + 0.020*SL$	$0.211 + 0.016*SL$	$0.226 + 0.015*SL$
A to CO	$t_R$	0.119	$0.060 + 0.030*SL$	$0.058 + 0.030*SL$	$0.051 + 0.031*SL$
	$t_F$	0.106	$0.054 + 0.026*SL$	$0.051 + 0.027*SL$	$0.045 + 0.027*SL$
	$t_{PLH}$	0.146	$0.115 + 0.016*SL$	$0.122 + 0.014*SL$	$0.125 + 0.013*SL$
	$t_{PHL}$	0.169	$0.136 + 0.016*SL$	$0.142 + 0.015*SL$	$0.145 + 0.014*SL$
B to CO	$t_R$	0.118	$0.059 + 0.030*SL$	$0.058 + 0.030*SL$	$0.051 + 0.031*SL$
	$t_F$	0.105	$0.055 + 0.025*SL$	$0.049 + 0.027*SL$	$0.042 + 0.028*SL$
	$t_{PLH}$	0.152	$0.121 + 0.015*SL$	$0.127 + 0.014*SL$	$0.130 + 0.013*SL$
	$t_{PHL}$	0.155	$0.123 + 0.016*SL$	$0.129 + 0.015*SL$	$0.131 + 0.014*SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## HADH/HA/HAD2

### Half Adder with 0.5X/1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

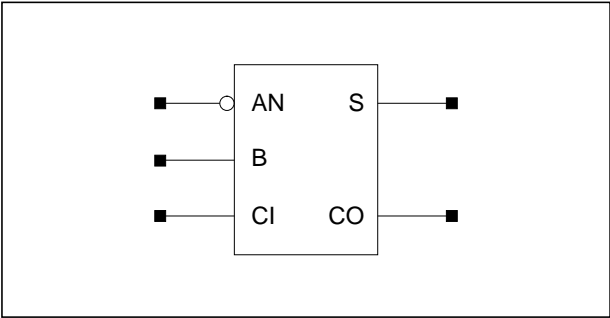
#### HAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	$t_R$	0.119	$0.089 + 0.015 \cdot SL$	$0.090 + 0.015 \cdot SL$	$0.090 + 0.015 \cdot SL$
	$t_F$	0.141	$0.110 + 0.015 \cdot SL$	$0.118 + 0.013 \cdot SL$	$0.126 + 0.013 \cdot SL$
	$t_{PLH}$	0.318	$0.296 + 0.011 \cdot SL$	$0.306 + 0.008 \cdot SL$	$0.323 + 0.007 \cdot SL$
	$t_{PHL}$	0.322	$0.296 + 0.013 \cdot SL$	$0.309 + 0.010 \cdot SL$	$0.334 + 0.008 \cdot SL$
B to S	$t_R$	0.115	$0.086 + 0.015 \cdot SL$	$0.084 + 0.015 \cdot SL$	$0.086 + 0.015 \cdot SL$
	$t_F$	0.130	$0.099 + 0.016 \cdot SL$	$0.107 + 0.014 \cdot SL$	$0.117 + 0.013 \cdot SL$
	$t_{PLH}$	0.233	$0.210 + 0.011 \cdot SL$	$0.221 + 0.009 \cdot SL$	$0.238 + 0.007 \cdot SL$
	$t_{PHL}$	0.249	$0.223 + 0.013 \cdot SL$	$0.236 + 0.010 \cdot SL$	$0.261 + 0.008 \cdot SL$
A to CO	$t_R$	0.093	$0.063 + 0.015 \cdot SL$	$0.064 + 0.015 \cdot SL$	$0.058 + 0.015 \cdot SL$
	$t_F$	0.083	$0.055 + 0.014 \cdot SL$	$0.058 + 0.013 \cdot SL$	$0.052 + 0.013 \cdot SL$
	$t_{PLH}$	0.157	$0.138 + 0.010 \cdot SL$	$0.146 + 0.008 \cdot SL$	$0.157 + 0.007 \cdot SL$
	$t_{PHL}$	0.174	$0.154 + 0.010 \cdot SL$	$0.162 + 0.008 \cdot SL$	$0.173 + 0.007 \cdot SL$
B to CO	$t_R$	0.095	$0.068 + 0.014 \cdot SL$	$0.064 + 0.015 \cdot SL$	$0.057 + 0.015 \cdot SL$
	$t_F$	0.079	$0.053 + 0.013 \cdot SL$	$0.053 + 0.013 \cdot SL$	$0.050 + 0.014 \cdot SL$
	$t_{PLH}$	0.169	$0.150 + 0.010 \cdot SL$	$0.158 + 0.008 \cdot SL$	$0.169 + 0.007 \cdot SL$
	$t_{PHL}$	0.167	$0.147 + 0.010 \cdot SL$	$0.155 + 0.008 \cdot SL$	$0.165 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



Logic Symbol



Truth Table

AN	B	CI	S	CO
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

Cell Data

Input Load (SL)						Gate Count	
SCG23			SCG23D2			SCG23	SCG23D2
CI	AN	B	CI	AN	B		
0.5	0.5	1.0	0.5	0.6	1.0	6.67	7.00



## SCG23/SCG23D2

### Full Adder with one inverted input, 1X/2X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

SCG23

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to S	$t_R$	0.151	$0.092 + 0.030 \cdot SL$	$0.092 + 0.029 \cdot SL$	$0.088 + 0.030 \cdot SL$
	$t_F$	0.145	$0.088 + 0.029 \cdot SL$	$0.097 + 0.026 \cdot SL$	$0.105 + 0.026 \cdot SL$
	$t_{PLH}$	0.527	$0.492 + 0.018 \cdot SL$	$0.502 + 0.015 \cdot SL$	$0.512 + 0.014 \cdot SL$
	$t_{PHL}$	0.512	$0.471 + 0.021 \cdot SL$	$0.484 + 0.017 \cdot SL$	$0.500 + 0.015 \cdot SL$
B to S	$t_R$	0.157	$0.099 + 0.029 \cdot SL$	$0.099 + 0.029 \cdot SL$	$0.093 + 0.030 \cdot SL$
	$t_F$	0.156	$0.101 + 0.028 \cdot SL$	$0.107 + 0.026 \cdot SL$	$0.114 + 0.025 \cdot SL$
	$t_{PLH}$	0.503	$0.468 + 0.018 \cdot SL$	$0.478 + 0.015 \cdot SL$	$0.488 + 0.014 \cdot SL$
	$t_{PHL}$	0.507	$0.465 + 0.021 \cdot SL$	$0.479 + 0.017 \cdot SL$	$0.495 + 0.015 \cdot SL$
CI to S	$t_R$	0.159	$0.099 + 0.030 \cdot SL$	$0.103 + 0.029 \cdot SL$	$0.098 + 0.030 \cdot SL$
	$t_F$	0.178	$0.124 + 0.027 \cdot SL$	$0.131 + 0.025 \cdot SL$	$0.137 + 0.025 \cdot SL$
	$t_{PLH}$	0.468	$0.433 + 0.018 \cdot SL$	$0.444 + 0.015 \cdot SL$	$0.454 + 0.014 \cdot SL$
	$t_{PHL}$	0.443	$0.402 + 0.020 \cdot SL$	$0.416 + 0.017 \cdot SL$	$0.432 + 0.015 \cdot SL$
AN to CO	$t_R$	0.144	$0.084 + 0.030 \cdot SL$	$0.085 + 0.030 \cdot SL$	$0.083 + 0.030 \cdot SL$
	$t_F$	0.148	$0.092 + 0.028 \cdot SL$	$0.097 + 0.027 \cdot SL$	$0.107 + 0.026 \cdot SL$
	$t_{PLH}$	0.497	$0.464 + 0.016 \cdot SL$	$0.472 + 0.014 \cdot SL$	$0.479 + 0.014 \cdot SL$
	$t_{PHL}$	0.469	$0.432 + 0.018 \cdot SL$	$0.442 + 0.016 \cdot SL$	$0.454 + 0.014 \cdot SL$
B to CO	$t_R$	0.198	$0.144 + 0.027 \cdot SL$	$0.144 + 0.027 \cdot SL$	$0.134 + 0.028 \cdot SL$
	$t_F$	0.179	$0.129 + 0.025 \cdot SL$	$0.131 + 0.024 \cdot SL$	$0.129 + 0.025 \cdot SL$
	$t_{PLH}$	0.471	$0.438 + 0.017 \cdot SL$	$0.447 + 0.014 \cdot SL$	$0.453 + 0.014 \cdot SL$
	$t_{PHL}$	0.472	$0.435 + 0.018 \cdot SL$	$0.446 + 0.016 \cdot SL$	$0.457 + 0.014 \cdot SL$
CI to CO	$t_R$	0.159	$0.099 + 0.030 \cdot SL$	$0.102 + 0.029 \cdot SL$	$0.097 + 0.030 \cdot SL$
	$t_F$	0.176	$0.120 + 0.028 \cdot SL$	$0.129 + 0.026 \cdot SL$	$0.136 + 0.025 \cdot SL$
	$t_{PLH}$	0.297	$0.259 + 0.019 \cdot SL$	$0.271 + 0.016 \cdot SL$	$0.284 + 0.014 \cdot SL$
	$t_{PHL}$	0.329	$0.283 + 0.023 \cdot SL$	$0.302 + 0.018 \cdot SL$	$0.323 + 0.016 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## Full Adder with one inverted input, 1X/2X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

SCG23D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to S	$t_R$	0.137	$0.107 + 0.015 \cdot SL$	$0.107 + 0.015 \cdot SL$	$0.107 + 0.015 \cdot SL$
	$t_F$	0.138	$0.106 + 0.016 \cdot SL$	$0.112 + 0.014 \cdot SL$	$0.122 + 0.013 \cdot SL$
	$t_{PLH}$	0.532	$0.509 + 0.012 \cdot SL$	$0.520 + 0.009 \cdot SL$	$0.538 + 0.007 \cdot SL$
	$t_{PHL}$	0.535	$0.508 + 0.014 \cdot SL$	$0.521 + 0.010 \cdot SL$	$0.545 + 0.009 \cdot SL$
B to S	$t_R$	0.134	$0.104 + 0.015 \cdot SL$	$0.104 + 0.015 \cdot SL$	$0.102 + 0.015 \cdot SL$
	$t_F$	0.144	$0.113 + 0.016 \cdot SL$	$0.119 + 0.014 \cdot SL$	$0.131 + 0.013 \cdot SL$
	$t_{PLH}$	0.504	$0.481 + 0.012 \cdot SL$	$0.493 + 0.009 \cdot SL$	$0.511 + 0.007 \cdot SL$
	$t_{PHL}$	0.512	$0.484 + 0.014 \cdot SL$	$0.498 + 0.011 \cdot SL$	$0.524 + 0.009 \cdot SL$
CI to S	$t_R$	0.134	$0.104 + 0.015 \cdot SL$	$0.106 + 0.015 \cdot SL$	$0.106 + 0.015 \cdot SL$
	$t_F$	0.166	$0.134 + 0.016 \cdot SL$	$0.143 + 0.014 \cdot SL$	$0.153 + 0.013 \cdot SL$
	$t_{PLH}$	0.520	$0.497 + 0.012 \cdot SL$	$0.509 + 0.009 \cdot SL$	$0.528 + 0.007 \cdot SL$
	$t_{PHL}$	0.487	$0.459 + 0.014 \cdot SL$	$0.473 + 0.010 \cdot SL$	$0.498 + 0.008 \cdot SL$
AN to CO	$t_R$	0.122	$0.091 + 0.015 \cdot SL$	$0.093 + 0.015 \cdot SL$	$0.093 + 0.015 \cdot SL$
	$t_F$	0.140	$0.108 + 0.016 \cdot SL$	$0.114 + 0.015 \cdot SL$	$0.127 + 0.014 \cdot SL$
	$t_{PLH}$	0.503	$0.482 + 0.011 \cdot SL$	$0.491 + 0.008 \cdot SL$	$0.505 + 0.007 \cdot SL$
	$t_{PHL}$	0.473	$0.445 + 0.014 \cdot SL$	$0.459 + 0.011 \cdot SL$	$0.484 + 0.009 \cdot SL$
B to CO	$t_R$	0.193	$0.170 + 0.011 \cdot SL$	$0.166 + 0.013 \cdot SL$	$0.150 + 0.014 \cdot SL$
	$t_F$	0.181	$0.156 + 0.013 \cdot SL$	$0.156 + 0.013 \cdot SL$	$0.152 + 0.013 \cdot SL$
	$t_{PLH}$	0.472	$0.451 + 0.011 \cdot SL$	$0.461 + 0.008 \cdot SL$	$0.476 + 0.007 \cdot SL$
	$t_{PHL}$	0.474	$0.450 + 0.012 \cdot SL$	$0.461 + 0.009 \cdot SL$	$0.481 + 0.008 \cdot SL$
CI to CO	$t_R$	0.134	$0.105 + 0.015 \cdot SL$	$0.104 + 0.015 \cdot SL$	$0.107 + 0.015 \cdot SL$
	$t_F$	0.164	$0.130 + 0.017 \cdot SL$	$0.142 + 0.014 \cdot SL$	$0.151 + 0.013 \cdot SL$
	$t_{PLH}$	0.303	$0.278 + 0.012 \cdot SL$	$0.292 + 0.009 \cdot SL$	$0.312 + 0.007 \cdot SL$
	$t_{PHL}$	0.343	$0.313 + 0.015 \cdot SL$	$0.329 + 0.011 \cdot SL$	$0.360 + 0.009 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## MULTIPLEXERS

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### Cell List

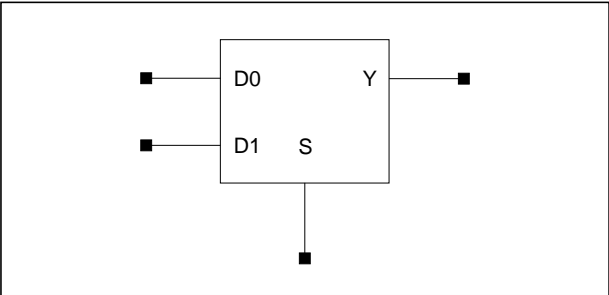
Cell Name	Function Description
MX2DH	2 > 1 Non-Inverting Mux with 0.5X Drive
MX2	2 > 1 Non-Inverting Mux
MX2D2	2 > 1 Non-Inverting Mux with 2X Drive
MX2D4	2 > 1 Non-Inverting Mux with 4X Drive
MX2X4	4-Bit 2 > 1 Non-Inverting Mux
MX2IDH	2 > 1 Inverting Mux with 0.5X Drive
MX2I	2 > 1 Inverting Mux
MX2ID2	2 > 1 Inverting Mux with 2X Drive
MX2ID4	2 > 1 Inverting Mux with 4X Drive
MX2IDHA	2 > 1 Inverting Mux with Separate S and SN Inputs, 0.5X Drive
MX2IA	2 > 1 Inverting Mux with Separate S and SN Inputs
MX2ID2A	2 > 1 Inverting Mux with Separate S and SN Inputs, 2X Drive
MX2ID4A	2 > 1 Inverting Mux with Separate S and SN Inputs, 4X Drive
MX2IX4	4-Bit 2 > 1 Inverting Mux
MX3I	3 > 1 Inverting Mux
MX3ID2	3 > 1 Inverting Mux with 2X Drive
MX3ID4	3 > 1 Inverting Mux with 4X Drive
MX4	4 > 1 Non-Inverting Mux
MX4D2	4 > 1 Non-Inverting Mux with 2X Drive
MX4D4	4 > 1 Non-Inverting Mux with 4X Drive
MX8	8 > 1 Non-Inverting Mux
MX8D2	8 > 1 Non-Inverting Mux with 2X Drive
MX8D4	8 > 1 Non-inverting Mux with 4X Drive



**MX2DH/MX2/MX2D2/MX2D4**

**2 > 1 Non-Inverting MUX with 0.5X/1X/2X/4X Drive**

**Logic Symbol**



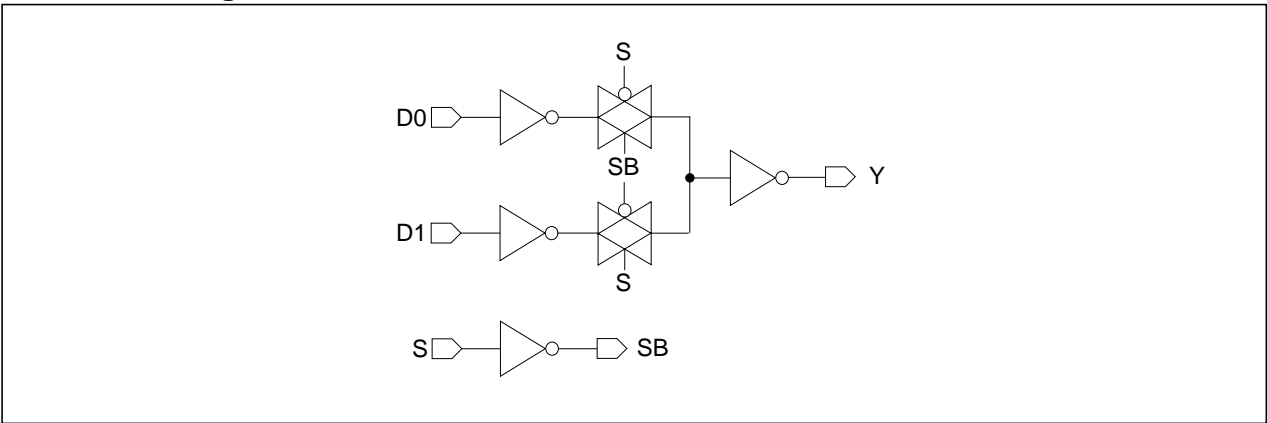
**Truth Table**

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

**Cell Data**

Input Load (SL)											
MX2DH			MX2			MX2D2			MX2D4		
D0	D1	S	D0	D1	S	D0	D1	S	D0	D1	S
0.6	0.6	1.0	0.8	0.8	1.0	0.8	0.8	1.0	0.8	0.8	1.0
Gate Count											
MX2DH			MX2			MX2D2			MX2D4		
2.33			2.33			2.67			3.33		

**Schematic Diagram**





## MX2DH/MX2/MX2D2/MX2D4

### 2 > 1 Non-Inverting MUX with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### MX2DH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t <sub>R</sub>	0.205	$0.079 + 0.063 \cdot SL$	$0.073 + 0.065 \cdot SL$	$0.063 + 0.066 \cdot SL$
	t <sub>F</sub>	0.187	$0.086 + 0.050 \cdot SL$	$0.087 + 0.050 \cdot SL$	$0.077 + 0.051 \cdot SL$
	t <sub>PLH</sub>	0.247	$0.185 + 0.031 \cdot SL$	$0.194 + 0.029 \cdot SL$	$0.196 + 0.029 \cdot SL$
	t <sub>PHL</sub>	0.262	$0.196 + 0.033 \cdot SL$	$0.214 + 0.029 \cdot SL$	$0.224 + 0.027 \cdot SL$
D1 to Y	t <sub>R</sub>	0.206	$0.080 + 0.063 \cdot SL$	$0.072 + 0.065 \cdot SL$	$0.063 + 0.066 \cdot SL$
	t <sub>F</sub>	0.186	$0.086 + 0.050 \cdot SL$	$0.086 + 0.050 \cdot SL$	$0.077 + 0.051 \cdot SL$
	t <sub>PLH</sub>	0.249	$0.187 + 0.031 \cdot SL$	$0.196 + 0.029 \cdot SL$	$0.198 + 0.029 \cdot SL$
	t <sub>PHL</sub>	0.265	$0.199 + 0.033 \cdot SL$	$0.217 + 0.029 \cdot SL$	$0.227 + 0.027 \cdot SL$
S to Y	t <sub>R</sub>	0.205	$0.078 + 0.063 \cdot SL$	$0.074 + 0.065 \cdot SL$	$0.063 + 0.066 \cdot SL$
	t <sub>F</sub>	0.182	$0.079 + 0.051 \cdot SL$	$0.084 + 0.050 \cdot SL$	$0.075 + 0.051 \cdot SL$
	t <sub>PLH</sub>	0.252	$0.189 + 0.031 \cdot SL$	$0.198 + 0.029 \cdot SL$	$0.201 + 0.029 \cdot SL$
	t <sub>PHL</sub>	0.255	$0.189 + 0.033 \cdot SL$	$0.206 + 0.029 \cdot SL$	$0.216 + 0.027 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### MX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t <sub>R</sub>	0.130	$0.072 + 0.029 \cdot SL$	$0.070 + 0.030 \cdot SL$	$0.065 + 0.030 \cdot SL$
	t <sub>F</sub>	0.133	$0.077 + 0.028 \cdot SL$	$0.084 + 0.026 \cdot SL$	$0.081 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.194	$0.161 + 0.016 \cdot SL$	$0.170 + 0.014 \cdot SL$	$0.176 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.216	$0.177 + 0.019 \cdot SL$	$0.189 + 0.016 \cdot SL$	$0.201 + 0.015 \cdot SL$
D1 to Y	t <sub>R</sub>	0.129	$0.070 + 0.029 \cdot SL$	$0.070 + 0.029 \cdot SL$	$0.064 + 0.030 \cdot SL$
	t <sub>F</sub>	0.133	$0.077 + 0.028 \cdot SL$	$0.083 + 0.026 \cdot SL$	$0.081 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.193	$0.160 + 0.016 \cdot SL$	$0.169 + 0.014 \cdot SL$	$0.175 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.218	$0.180 + 0.019 \cdot SL$	$0.191 + 0.016 \cdot SL$	$0.203 + 0.015 \cdot SL$
S to Y	t <sub>R</sub>	0.132	$0.075 + 0.029 \cdot SL$	$0.072 + 0.029 \cdot SL$	$0.065 + 0.030 \cdot SL$
	t <sub>F</sub>	0.131	$0.075 + 0.028 \cdot SL$	$0.081 + 0.027 \cdot SL$	$0.079 + 0.027 \cdot SL$
	t <sub>PLH</sub>	0.219	$0.186 + 0.016 \cdot SL$	$0.195 + 0.014 \cdot SL$	$0.201 + 0.014 \cdot SL$
	t <sub>PHL</sub>	0.228	$0.189 + 0.019 \cdot SL$	$0.201 + 0.016 \cdot SL$	$0.213 + 0.015 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## MX2DH/MX2/MX2D2/MX2D4

### 2 > 1 Non-Inverting MUX with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### MX2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	$t_R$	0.109	$0.080 + 0.015 \cdot SL$	$0.080 + 0.015 \cdot SL$	$0.077 + 0.015 \cdot SL$
	$t_F$	0.118	$0.089 + 0.014 \cdot SL$	$0.092 + 0.013 \cdot SL$	$0.099 + 0.013 \cdot SL$
	$t_{PLH}$	0.205	$0.184 + 0.011 \cdot SL$	$0.193 + 0.008 \cdot SL$	$0.208 + 0.007 \cdot SL$
	$t_{PHL}$	0.224	$0.199 + 0.012 \cdot SL$	$0.211 + 0.009 \cdot SL$	$0.233 + 0.008 \cdot SL$
D1 to Y	$t_R$	0.108	$0.079 + 0.015 \cdot SL$	$0.079 + 0.015 \cdot SL$	$0.076 + 0.015 \cdot SL$
	$t_F$	0.118	$0.090 + 0.014 \cdot SL$	$0.093 + 0.013 \cdot SL$	$0.099 + 0.013 \cdot SL$
	$t_{PLH}$	0.203	$0.182 + 0.010 \cdot SL$	$0.191 + 0.008 \cdot SL$	$0.206 + 0.007 \cdot SL$
	$t_{PHL}$	0.226	$0.201 + 0.012 \cdot SL$	$0.213 + 0.009 \cdot SL$	$0.235 + 0.008 \cdot SL$
S to Y	$t_R$	0.111	$0.082 + 0.014 \cdot SL$	$0.081 + 0.015 \cdot SL$	$0.079 + 0.015 \cdot SL$
	$t_F$	0.116	$0.087 + 0.015 \cdot SL$	$0.091 + 0.013 \cdot SL$	$0.098 + 0.013 \cdot SL$
	$t_{PLH}$	0.226	$0.205 + 0.011 \cdot SL$	$0.215 + 0.008 \cdot SL$	$0.230 + 0.007 \cdot SL$
	$t_{PHL}$	0.233	$0.208 + 0.012 \cdot SL$	$0.219 + 0.009 \cdot SL$	$0.242 + 0.008 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$

##### MX2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	$t_R$	0.132	$0.117 + 0.007 \cdot SL$	$0.117 + 0.007 \cdot SL$	$0.116 + 0.007 \cdot SL$
	$t_F$	0.149	$0.132 + 0.008 \cdot SL$	$0.137 + 0.007 \cdot SL$	$0.147 + 0.007 \cdot SL$
	$t_{PLH}$	0.254	$0.240 + 0.007 \cdot SL$	$0.249 + 0.005 \cdot SL$	$0.273 + 0.004 \cdot SL$
	$t_{PHL}$	0.285	$0.268 + 0.008 \cdot SL$	$0.278 + 0.006 \cdot SL$	$0.309 + 0.004 \cdot SL$
D1 to Y	$t_R$	0.130	$0.115 + 0.007 \cdot SL$	$0.116 + 0.007 \cdot SL$	$0.114 + 0.007 \cdot SL$
	$t_F$	0.149	$0.132 + 0.008 \cdot SL$	$0.137 + 0.007 \cdot SL$	$0.148 + 0.007 \cdot SL$
	$t_{PLH}$	0.252	$0.238 + 0.007 \cdot SL$	$0.247 + 0.005 \cdot SL$	$0.271 + 0.004 \cdot SL$
	$t_{PHL}$	0.287	$0.270 + 0.008 \cdot SL$	$0.280 + 0.006 \cdot SL$	$0.311 + 0.004 \cdot SL$
S to Y	$t_R$	0.132	$0.118 + 0.007 \cdot SL$	$0.117 + 0.007 \cdot SL$	$0.118 + 0.007 \cdot SL$
	$t_F$	0.149	$0.132 + 0.008 \cdot SL$	$0.137 + 0.007 \cdot SL$	$0.147 + 0.007 \cdot SL$
	$t_{PLH}$	0.270	$0.256 + 0.007 \cdot SL$	$0.265 + 0.005 \cdot SL$	$0.289 + 0.004 \cdot SL$
	$t_{PHL}$	0.288	$0.272 + 0.008 \cdot SL$	$0.281 + 0.006 \cdot SL$	$0.313 + 0.004 \cdot SL$

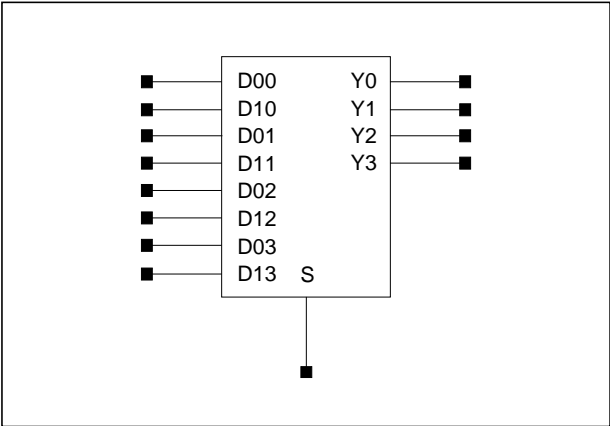
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 22$ , \*Group3 :  $22 < SL$



MX2X4

4-Bit 2 > 1 Non-Inverting MUX

Logic Symbol



Truth Table

S	Y0	Y1	Y2	Y3
0	D00	D01	D02	D03
1	D10	D11	D12	D13

Cell Data

Input Load (SL)									Gate Count
D00	D10	D01	D11	D02	D12	D03	D13	S	8.67
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	3.3	



## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to Y0	$t_R$	0.128	$0.071 + 0.028 \cdot SL$	$0.069 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.128	$0.074 + 0.027 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.192	$0.160 + 0.016 \cdot SL$	$0.168 + 0.014 \cdot SL$	$0.174 + 0.013 \cdot SL$
	$t_{PHL}$	0.212	$0.175 + 0.019 \cdot SL$	$0.186 + 0.016 \cdot SL$	$0.198 + 0.014 \cdot SL$
D10 to Y0	$t_R$	0.127	$0.070 + 0.029 \cdot SL$	$0.068 + 0.029 \cdot SL$	$0.064 + 0.030 \cdot SL$
	$t_F$	0.129	$0.076 + 0.026 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.193	$0.161 + 0.016 \cdot SL$	$0.170 + 0.014 \cdot SL$	$0.176 + 0.013 \cdot SL$
	$t_{PHL}$	0.215	$0.178 + 0.019 \cdot SL$	$0.189 + 0.016 \cdot SL$	$0.201 + 0.014 \cdot SL$
S to Y0	$t_R$	0.132	$0.076 + 0.028 \cdot SL$	$0.072 + 0.029 \cdot SL$	$0.065 + 0.030 \cdot SL$
	$t_F$	0.128	$0.075 + 0.026 \cdot SL$	$0.080 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.222	$0.189 + 0.016 \cdot SL$	$0.198 + 0.014 \cdot SL$	$0.204 + 0.013 \cdot SL$
	$t_{PHL}$	0.238	$0.200 + 0.019 \cdot SL$	$0.212 + 0.016 \cdot SL$	$0.224 + 0.014 \cdot SL$
D01 to Y1	$t_R$	0.128	$0.071 + 0.028 \cdot SL$	$0.069 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.128	$0.075 + 0.027 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.193	$0.160 + 0.016 \cdot SL$	$0.169 + 0.014 \cdot SL$	$0.175 + 0.013 \cdot SL$
	$t_{PHL}$	0.212	$0.175 + 0.019 \cdot SL$	$0.187 + 0.016 \cdot SL$	$0.199 + 0.014 \cdot SL$
D11 to Y1	$t_R$	0.127	$0.070 + 0.029 \cdot SL$	$0.068 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.128	$0.075 + 0.027 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.191	$0.159 + 0.016 \cdot SL$	$0.168 + 0.014 \cdot SL$	$0.174 + 0.013 \cdot SL$
	$t_{PHL}$	0.213	$0.175 + 0.019 \cdot SL$	$0.187 + 0.016 \cdot SL$	$0.199 + 0.014 \cdot SL$
S to Y1	$t_R$	0.132	$0.076 + 0.028 \cdot SL$	$0.073 + 0.029 \cdot SL$	$0.066 + 0.030 \cdot SL$
	$t_F$	0.128	$0.075 + 0.026 \cdot SL$	$0.080 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.224	$0.191 + 0.016 \cdot SL$	$0.200 + 0.014 \cdot SL$	$0.206 + 0.013 \cdot SL$
	$t_{PHL}$	0.239	$0.202 + 0.019 \cdot SL$	$0.213 + 0.016 \cdot SL$	$0.226 + 0.014 \cdot SL$
D02 to Y2	$t_R$	0.128	$0.071 + 0.028 \cdot SL$	$0.069 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.128	$0.075 + 0.027 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.192	$0.160 + 0.016 \cdot SL$	$0.169 + 0.014 \cdot SL$	$0.174 + 0.013 \cdot SL$
	$t_{PHL}$	0.212	$0.175 + 0.019 \cdot SL$	$0.186 + 0.016 \cdot SL$	$0.198 + 0.014 \cdot SL$
D12 to Y2	$t_R$	0.128	$0.071 + 0.029 \cdot SL$	$0.068 + 0.029 \cdot SL$	$0.064 + 0.030 \cdot SL$
	$t_F$	0.129	$0.076 + 0.026 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.080 + 0.025 \cdot SL$
	$t_{PLH}$	0.194	$0.161 + 0.016 \cdot SL$	$0.170 + 0.014 \cdot SL$	$0.176 + 0.013 \cdot SL$
	$t_{PHL}$	0.215	$0.178 + 0.019 \cdot SL$	$0.189 + 0.016 \cdot SL$	$0.201 + 0.014 \cdot SL$
S to Y2	$t_R$	0.132	$0.077 + 0.028 \cdot SL$	$0.072 + 0.029 \cdot SL$	$0.066 + 0.030 \cdot SL$
	$t_F$	0.129	$0.076 + 0.026 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.080 + 0.025 \cdot SL$
	$t_{PLH}$	0.222	$0.190 + 0.016 \cdot SL$	$0.198 + 0.014 \cdot SL$	$0.204 + 0.013 \cdot SL$
	$t_{PHL}$	0.238	$0.200 + 0.019 \cdot SL$	$0.212 + 0.016 \cdot SL$	$0.224 + 0.014 \cdot SL$
D03 to Y3	$t_R$	0.128	$0.071 + 0.028 \cdot SL$	$0.069 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.128	$0.075 + 0.027 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.193	$0.160 + 0.016 \cdot SL$	$0.169 + 0.014 \cdot SL$	$0.175 + 0.013 \cdot SL$
	$t_{PHL}$	0.212	$0.175 + 0.019 \cdot SL$	$0.187 + 0.016 \cdot SL$	$0.199 + 0.014 \cdot SL$



## MX2X4

### 4-Bit 2 > 1 Non-Inverting MUX

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### MX2X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to Y3	$t_R$	0.127	$0.070 + 0.029 \cdot SL$	$0.068 + 0.029 \cdot SL$	$0.063 + 0.030 \cdot SL$
	$t_F$	0.128	$0.075 + 0.027 \cdot SL$	$0.081 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.191	$0.159 + 0.016 \cdot SL$	$0.168 + 0.014 \cdot SL$	$0.174 + 0.013 \cdot SL$
	$t_{PHL}$	0.213	$0.175 + 0.019 \cdot SL$	$0.187 + 0.016 \cdot SL$	$0.199 + 0.014 \cdot SL$
S to Y3	$t_R$	0.132	$0.076 + 0.028 \cdot SL$	$0.073 + 0.029 \cdot SL$	$0.066 + 0.030 \cdot SL$
	$t_F$	0.128	$0.075 + 0.026 \cdot SL$	$0.080 + 0.025 \cdot SL$	$0.079 + 0.025 \cdot SL$
	$t_{PLH}$	0.224	$0.191 + 0.016 \cdot SL$	$0.200 + 0.014 \cdot SL$	$0.206 + 0.013 \cdot SL$
	$t_{PHL}$	0.239	$0.202 + 0.019 \cdot SL$	$0.213 + 0.016 \cdot SL$	$0.226 + 0.014 \cdot SL$

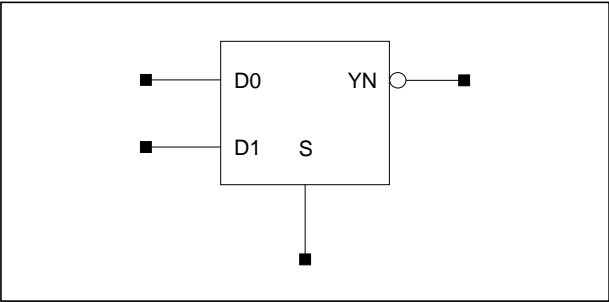
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



MX2IDH/MX2I/MX2ID2/MX2ID4

2 > 1 Inverting MUX with 0.5X/1X/2X/4X Drive

Logic Symbol



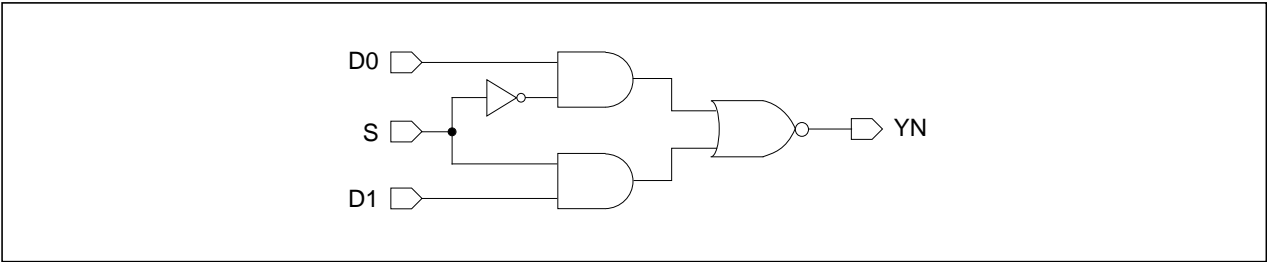
Truth Table

D0	D1	S	YN
0	x	0	1
1	x	0	0
x	0	1	1
x	1	1	0

Cell Data

Input Load (SL)											
MX2IDH			MX2I			MX2ID2			MX2ID4		
D0	D1	S	D0	D1	S	D0	D1	S	D0	D1	S
0.5	0.5	1.0	1.0	1.1	1.5	1.0	1.1	1.5	1.0	1.1	1.5
Gate Count											
MX2IDH			MX2I			MX2ID2			MX2ID4		
2.00			2.00			3.00			3.67		

Schematic Diagram





## MX2IDH/MX2I/MX2ID2/MX2ID4

### 2 > 1 Inverting MUX with 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### MX2IDH

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.476	$0.215 + 0.131 \cdot SL$	$0.200 + 0.134 \cdot SL$	$0.198 + 0.134 \cdot SL$
	$t_F$	0.338	$0.169 + 0.085 \cdot SL$	$0.152 + 0.089 \cdot SL$	$0.137 + 0.091 \cdot SL$
	$t_{PLH}$	0.245	$0.129 + 0.058 \cdot SL$	$0.129 + 0.058 \cdot SL$	$0.130 + 0.058 \cdot SL$
	$t_{PHL}$	0.182	$0.093 + 0.044 \cdot SL$	$0.096 + 0.044 \cdot SL$	$0.099 + 0.043 \cdot SL$
D1 to YN	$t_R$	0.455	$0.191 + 0.132 \cdot SL$	$0.182 + 0.134 \cdot SL$	$0.178 + 0.135 \cdot SL$
	$t_F$	0.381	$0.211 + 0.085 \cdot SL$	$0.194 + 0.089 \cdot SL$	$0.180 + 0.091 \cdot SL$
	$t_{PLH}$	0.261	$0.144 + 0.059 \cdot SL$	$0.145 + 0.058 \cdot SL$	$0.147 + 0.058 \cdot SL$
	$t_{PHL}$	0.221	$0.133 + 0.044 \cdot SL$	$0.135 + 0.044 \cdot SL$	$0.136 + 0.043 \cdot SL$
S to YN	$t_R$	0.474	$0.210 + 0.132 \cdot SL$	$0.202 + 0.134 \cdot SL$	$0.199 + 0.134 \cdot SL$
	$t_F$	0.349	$0.171 + 0.089 \cdot SL$	$0.161 + 0.091 \cdot SL$	$0.161 + 0.091 \cdot SL$
	$t_{PLH}$	0.270	$0.154 + 0.058 \cdot SL$	$0.155 + 0.058 \cdot SL$	$0.155 + 0.058 \cdot SL$
	$t_{PHL}$	0.239	$0.153 + 0.043 \cdot SL$	$0.153 + 0.043 \cdot SL$	$0.154 + 0.043 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### MX2I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.269	$0.158 + 0.055 \cdot SL$	$0.148 + 0.058 \cdot SL$	$0.136 + 0.059 \cdot SL$
	$t_F$	0.199	$0.124 + 0.038 \cdot SL$	$0.114 + 0.040 \cdot SL$	$0.100 + 0.042 \cdot SL$
	$t_{PLH}$	0.142	$0.092 + 0.025 \cdot SL$	$0.091 + 0.025 \cdot SL$	$0.090 + 0.026 \cdot SL$
	$t_{PHL}$	0.118	$0.075 + 0.022 \cdot SL$	$0.080 + 0.020 \cdot SL$	$0.080 + 0.020 \cdot SL$
D1 to YN	$t_R$	0.269	$0.152 + 0.058 \cdot SL$	$0.146 + 0.060 \cdot SL$	$0.139 + 0.061 \cdot SL$
	$t_F$	0.260	$0.185 + 0.037 \cdot SL$	$0.175 + 0.040 \cdot SL$	$0.160 + 0.042 \cdot SL$
	$t_{PLH}$	0.170	$0.116 + 0.027 \cdot SL$	$0.118 + 0.026 \cdot SL$	$0.119 + 0.026 \cdot SL$
	$t_{PHL}$	0.160	$0.118 + 0.021 \cdot SL$	$0.119 + 0.021 \cdot SL$	$0.120 + 0.020 \cdot SL$
S to YN	$t_R$	0.259	$0.140 + 0.059 \cdot SL$	$0.136 + 0.061 \cdot SL$	$0.133 + 0.061 \cdot SL$
	$t_F$	0.223	$0.145 + 0.039 \cdot SL$	$0.135 + 0.041 \cdot SL$	$0.125 + 0.043 \cdot SL$
	$t_{PLH}$	0.208	$0.156 + 0.026 \cdot SL$	$0.156 + 0.026 \cdot SL$	$0.156 + 0.026 \cdot SL$
	$t_{PHL}$	0.197	$0.154 + 0.021 \cdot SL$	$0.158 + 0.021 \cdot SL$	$0.159 + 0.020 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



**MX2IDH/MX2I/MX2ID2/MX2ID4****2 > 1 Inverting MUX with 0.5X/1X/2X/4X Drive****Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)**MX2ID2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.083	$0.054 + 0.014 \cdot SL$	$0.054 + 0.014 \cdot SL$	$0.043 + 0.015 \cdot SL$
	$t_F$	0.078	$0.052 + 0.013 \cdot SL$	$0.054 + 0.013 \cdot SL$	$0.047 + 0.013 \cdot SL$
	$t_{PLH}$	0.252	$0.235 + 0.009 \cdot SL$	$0.240 + 0.007 \cdot SL$	$0.246 + 0.007 \cdot SL$
	$t_{PHL}$	0.236	$0.216 + 0.010 \cdot SL$	$0.224 + 0.008 \cdot SL$	$0.233 + 0.007 \cdot SL$
D1 to YN	$t_R$	0.083	$0.054 + 0.014 \cdot SL$	$0.054 + 0.014 \cdot SL$	$0.044 + 0.015 \cdot SL$
	$t_F$	0.079	$0.051 + 0.014 \cdot SL$	$0.055 + 0.013 \cdot SL$	$0.050 + 0.013 \cdot SL$
	$t_{PLH}$	0.279	$0.262 + 0.009 \cdot SL$	$0.268 + 0.007 \cdot SL$	$0.273 + 0.007 \cdot SL$
	$t_{PHL}$	0.286	$0.267 + 0.010 \cdot SL$	$0.275 + 0.008 \cdot SL$	$0.284 + 0.007 \cdot SL$
S to YN	$t_R$	0.083	$0.055 + 0.014 \cdot SL$	$0.054 + 0.015 \cdot SL$	$0.044 + 0.015 \cdot SL$
	$t_F$	0.078	$0.051 + 0.014 \cdot SL$	$0.054 + 0.013 \cdot SL$	$0.049 + 0.013 \cdot SL$
	$t_{PLH}$	0.319	$0.302 + 0.009 \cdot SL$	$0.308 + 0.007 \cdot SL$	$0.313 + 0.007 \cdot SL$
	$t_{PHL}$	0.310	$0.290 + 0.010 \cdot SL$	$0.298 + 0.008 \cdot SL$	$0.307 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$ **MX2ID4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.088	$0.074 + 0.007 \cdot SL$	$0.073 + 0.007 \cdot SL$	$0.065 + 0.007 \cdot SL$
	$t_F$	0.086	$0.073 + 0.007 \cdot SL$	$0.074 + 0.007 \cdot SL$	$0.075 + 0.007 \cdot SL$
	$t_{PLH}$	0.291	$0.281 + 0.005 \cdot SL$	$0.286 + 0.004 \cdot SL$	$0.299 + 0.003 \cdot SL$
	$t_{PHL}$	0.278	$0.265 + 0.006 \cdot SL$	$0.272 + 0.005 \cdot SL$	$0.290 + 0.004 \cdot SL$
D1 to YN	$t_R$	0.089	$0.076 + 0.006 \cdot SL$	$0.073 + 0.007 \cdot SL$	$0.065 + 0.007 \cdot SL$
	$t_F$	0.088	$0.074 + 0.007 \cdot SL$	$0.076 + 0.007 \cdot SL$	$0.077 + 0.007 \cdot SL$
	$t_{PLH}$	0.318	$0.307 + 0.005 \cdot SL$	$0.313 + 0.004 \cdot SL$	$0.326 + 0.003 \cdot SL$
	$t_{PHL}$	0.328	$0.315 + 0.006 \cdot SL$	$0.322 + 0.005 \cdot SL$	$0.340 + 0.004 \cdot SL$
S to YN	$t_R$	0.088	$0.074 + 0.007 \cdot SL$	$0.073 + 0.007 \cdot SL$	$0.065 + 0.007 \cdot SL$
	$t_F$	0.088	$0.073 + 0.007 \cdot SL$	$0.076 + 0.007 \cdot SL$	$0.076 + 0.007 \cdot SL$
	$t_{PLH}$	0.358	$0.347 + 0.005 \cdot SL$	$0.352 + 0.004 \cdot SL$	$0.365 + 0.003 \cdot SL$
	$t_{PHL}$	0.350	$0.337 + 0.006 \cdot SL$	$0.344 + 0.005 \cdot SL$	$0.362 + 0.004 \cdot SL$

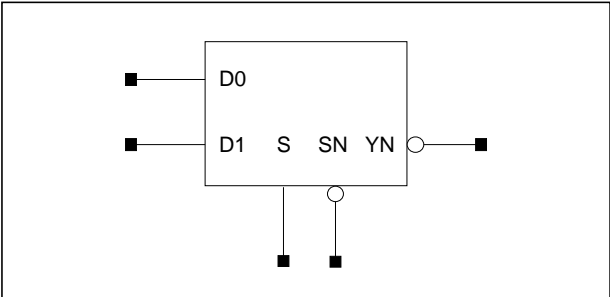
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 22$ , \*Group3 :  $22 < SL$



MX2IDHA/MX2IA/MX2ID2A/MX2ID4A

2 > 1 Inverting MUX with Separate S and SN Inputs, 0.5X/1X/2X/4X Drive

Logic Symbol



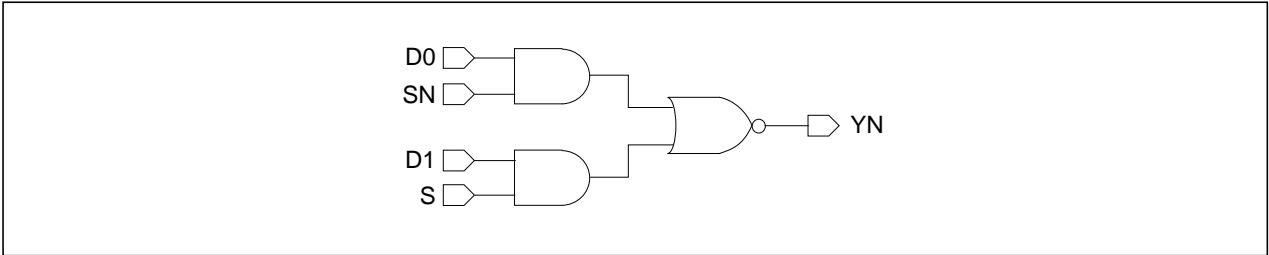
Truth Table

D0	D1	S	SN	YN
0	x	0	1	1
1	x	0	1	0
x	0	1	0	1
x	1	1	0	0

Cell Data

Input Load (SL)															
MX2IDHA				MX2IA				MX2ID2A				MX2ID4A			
D0	D1	S	SN	D0	D1	S	SN	D0	D1	S	SN	D0	D1	S	SN
0.5	0.5	0.5	0.5	1.0	1.0	1.0	1.0	1.0	1.2	1.0	1.1	1.0	1.1	1.0	1.1
Gate Count															
MX2IDHA				MX2IA				MX2ID2A				MX2ID4A			
1.67				1.67				2.67				3.33			

Schematic Diagram





## MX2IDHA/MX2IA/MX2ID2A/MX2ID4A

### 2 > 1 Inverting MUX with Separate S and SN Inputs, 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### MX2IDHA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.444	$0.184 + 0.130 \cdot SL$	$0.167 + 0.134 \cdot SL$	$0.163 + 0.135 \cdot SL$
	$t_F$	0.299	$0.129 + 0.085 \cdot SL$	$0.113 + 0.089 \cdot SL$	$0.099 + 0.091 \cdot SL$
	$t_{PLH}$	0.216	$0.102 + 0.057 \cdot SL$	$0.101 + 0.058 \cdot SL$	$0.100 + 0.058 \cdot SL$
	$t_{PHL}$	0.174	$0.088 + 0.043 \cdot SL$	$0.088 + 0.043 \cdot SL$	$0.088 + 0.043 \cdot SL$
D1 to YN	$t_R$	0.444	$0.182 + 0.131 \cdot SL$	$0.171 + 0.134 \cdot SL$	$0.167 + 0.134 \cdot SL$
	$t_F$	0.360	$0.188 + 0.086 \cdot SL$	$0.174 + 0.089 \cdot SL$	$0.163 + 0.091 \cdot SL$
	$t_{PLH}$	0.260	$0.143 + 0.058 \cdot SL$	$0.145 + 0.058 \cdot SL$	$0.146 + 0.058 \cdot SL$
	$t_{PHL}$	0.225	$0.137 + 0.044 \cdot SL$	$0.140 + 0.044 \cdot SL$	$0.142 + 0.043 \cdot SL$
S to YN	$t_R$	0.468	$0.205 + 0.132 \cdot SL$	$0.196 + 0.134 \cdot SL$	$0.191 + 0.134 \cdot SL$
	$t_F$	0.356	$0.181 + 0.087 \cdot SL$	$0.172 + 0.090 \cdot SL$	$0.164 + 0.091 \cdot SL$
	$t_{PLH}$	0.274	$0.158 + 0.058 \cdot SL$	$0.159 + 0.058 \cdot SL$	$0.160 + 0.058 \cdot SL$
	$t_{PHL}$	0.219	$0.130 + 0.045 \cdot SL$	$0.133 + 0.044 \cdot SL$	$0.136 + 0.043 \cdot SL$
SN to YN	$t_R$	0.468	$0.208 + 0.130 \cdot SL$	$0.191 + 0.134 \cdot SL$	$0.188 + 0.135 \cdot SL$
	$t_F$	0.294	$0.121 + 0.087 \cdot SL$	$0.109 + 0.090 \cdot SL$	$0.100 + 0.091 \cdot SL$
	$t_{PLH}$	0.230	$0.116 + 0.057 \cdot SL$	$0.114 + 0.058 \cdot SL$	$0.113 + 0.058 \cdot SL$
	$t_{PHL}$	0.167	$0.080 + 0.044 \cdot SL$	$0.081 + 0.043 \cdot SL$	$0.082 + 0.043 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$

##### MX2IA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.277	$0.164 + 0.057 \cdot SL$	$0.155 + 0.059 \cdot SL$	$0.143 + 0.060 \cdot SL$
	$t_F$	0.200	$0.125 + 0.038 \cdot SL$	$0.114 + 0.040 \cdot SL$	$0.101 + 0.042 \cdot SL$
	$t_{PLH}$	0.144	$0.093 + 0.026 \cdot SL$	$0.092 + 0.026 \cdot SL$	$0.091 + 0.026 \cdot SL$
	$t_{PHL}$	0.120	$0.077 + 0.021 \cdot SL$	$0.081 + 0.020 \cdot SL$	$0.081 + 0.020 \cdot SL$
D1 to YN	$t_R$	0.274	$0.158 + 0.058 \cdot SL$	$0.151 + 0.060 \cdot SL$	$0.144 + 0.060 \cdot SL$
	$t_F$	0.250	$0.172 + 0.039 \cdot SL$	$0.165 + 0.041 \cdot SL$	$0.155 + 0.042 \cdot SL$
	$t_{PLH}$	0.174	$0.121 + 0.027 \cdot SL$	$0.123 + 0.026 \cdot SL$	$0.123 + 0.026 \cdot SL$
	$t_{PHL}$	0.167	$0.125 + 0.021 \cdot SL$	$0.126 + 0.021 \cdot SL$	$0.128 + 0.020 \cdot SL$
S to YN	$t_R$	0.295	$0.178 + 0.058 \cdot SL$	$0.172 + 0.060 \cdot SL$	$0.166 + 0.060 \cdot SL$
	$t_F$	0.245	$0.165 + 0.040 \cdot SL$	$0.160 + 0.041 \cdot SL$	$0.152 + 0.042 \cdot SL$
	$t_{PLH}$	0.188	$0.135 + 0.026 \cdot SL$	$0.136 + 0.026 \cdot SL$	$0.137 + 0.026 \cdot SL$
	$t_{PHL}$	0.159	$0.117 + 0.021 \cdot SL$	$0.119 + 0.021 \cdot SL$	$0.121 + 0.021 \cdot SL$
SN to YN	$t_R$	0.300	$0.186 + 0.057 \cdot SL$	$0.177 + 0.059 \cdot SL$	$0.165 + 0.060 \cdot SL$
	$t_F$	0.192	$0.115 + 0.038 \cdot SL$	$0.104 + 0.041 \cdot SL$	$0.097 + 0.042 \cdot SL$
	$t_{PLH}$	0.157	$0.107 + 0.025 \cdot SL$	$0.105 + 0.026 \cdot SL$	$0.104 + 0.026 \cdot SL$
	$t_{PHL}$	0.112	$0.069 + 0.022 \cdot SL$	$0.074 + 0.020 \cdot SL$	$0.074 + 0.020 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## MX2IDHA/MX2IA/MX2ID2A/MX2ID4A

### 2 > 1 Inverting MUX with Separate S and SN Inputs, 0.5X/1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

##### MX2ID2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.086	$0.057 + 0.014 \cdot SL$	$0.056 + 0.015 \cdot SL$	$0.047 + 0.015 \cdot SL$
	$t_F$	0.080	$0.055 + 0.013 \cdot SL$	$0.055 + 0.012 \cdot SL$	$0.051 + 0.013 \cdot SL$
	$t_{PLH}$	0.261	$0.244 + 0.009 \cdot SL$	$0.250 + 0.007 \cdot SL$	$0.256 + 0.007 \cdot SL$
	$t_{PHL}$	0.241	$0.222 + 0.010 \cdot SL$	$0.230 + 0.008 \cdot SL$	$0.240 + 0.007 \cdot SL$
D1 to YN	$t_R$	0.086	$0.056 + 0.015 \cdot SL$	$0.057 + 0.014 \cdot SL$	$0.046 + 0.015 \cdot SL$
	$t_F$	0.080	$0.053 + 0.013 \cdot SL$	$0.058 + 0.012 \cdot SL$	$0.050 + 0.013 \cdot SL$
	$t_{PLH}$	0.282	$0.264 + 0.009 \cdot SL$	$0.270 + 0.007 \cdot SL$	$0.276 + 0.007 \cdot SL$
	$t_{PHL}$	0.288	$0.268 + 0.010 \cdot SL$	$0.276 + 0.008 \cdot SL$	$0.286 + 0.007 \cdot SL$
S to YN	$t_R$	0.086	$0.058 + 0.014 \cdot SL$	$0.058 + 0.014 \cdot SL$	$0.047 + 0.015 \cdot SL$
	$t_F$	0.080	$0.053 + 0.013 \cdot SL$	$0.057 + 0.012 \cdot SL$	$0.051 + 0.013 \cdot SL$
	$t_{PLH}$	0.299	$0.281 + 0.009 \cdot SL$	$0.287 + 0.007 \cdot SL$	$0.293 + 0.007 \cdot SL$
	$t_{PHL}$	0.280	$0.260 + 0.010 \cdot SL$	$0.268 + 0.008 \cdot SL$	$0.279 + 0.007 \cdot SL$
SN to YN	$t_R$	0.087	$0.058 + 0.014 \cdot SL$	$0.058 + 0.014 \cdot SL$	$0.047 + 0.015 \cdot SL$
	$t_F$	0.079	$0.052 + 0.013 \cdot SL$	$0.056 + 0.012 \cdot SL$	$0.051 + 0.013 \cdot SL$
	$t_{PLH}$	0.280	$0.263 + 0.009 \cdot SL$	$0.269 + 0.007 \cdot SL$	$0.275 + 0.007 \cdot SL$
	$t_{PHL}$	0.234	$0.214 + 0.010 \cdot SL$	$0.222 + 0.008 \cdot SL$	$0.233 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$

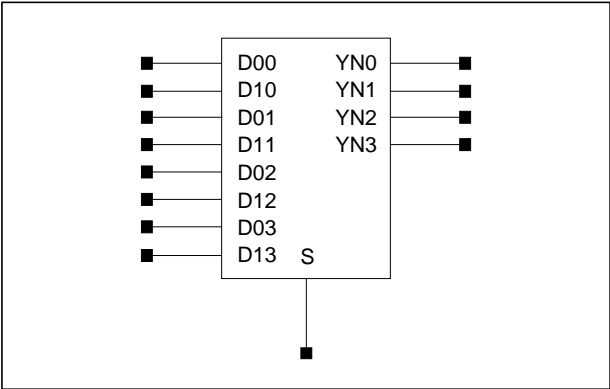
##### MX2ID4A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.079	$0.064 + 0.007 \cdot SL$	$0.065 + 0.007 \cdot SL$	$0.056 + 0.008 \cdot SL$
	$t_F$	0.070	$0.054 + 0.008 \cdot SL$	$0.060 + 0.006 \cdot SL$	$0.056 + 0.007 \cdot SL$
	$t_{PLH}$	0.280	$0.270 + 0.005 \cdot SL$	$0.275 + 0.004 \cdot SL$	$0.286 + 0.003 \cdot SL$
	$t_{PHL}$	0.249	$0.238 + 0.006 \cdot SL$	$0.244 + 0.004 \cdot SL$	$0.257 + 0.004 \cdot SL$
D1 to YN	$t_R$	0.079	$0.065 + 0.007 \cdot SL$	$0.065 + 0.007 \cdot SL$	$0.056 + 0.008 \cdot SL$
	$t_F$	0.072	$0.057 + 0.007 \cdot SL$	$0.060 + 0.007 \cdot SL$	$0.057 + 0.007 \cdot SL$
	$t_{PLH}$	0.301	$0.291 + 0.005 \cdot SL$	$0.295 + 0.004 \cdot SL$	$0.306 + 0.003 \cdot SL$
	$t_{PHL}$	0.295	$0.284 + 0.006 \cdot SL$	$0.289 + 0.004 \cdot SL$	$0.303 + 0.004 \cdot SL$
S to YN	$t_R$	0.080	$0.066 + 0.007 \cdot SL$	$0.066 + 0.007 \cdot SL$	$0.056 + 0.008 \cdot SL$
	$t_F$	0.072	$0.059 + 0.007 \cdot SL$	$0.060 + 0.007 \cdot SL$	$0.057 + 0.007 \cdot SL$
	$t_{PLH}$	0.318	$0.308 + 0.005 \cdot SL$	$0.313 + 0.004 \cdot SL$	$0.324 + 0.003 \cdot SL$
	$t_{PHL}$	0.288	$0.277 + 0.006 \cdot SL$	$0.282 + 0.004 \cdot SL$	$0.296 + 0.004 \cdot SL$
SN to YN	$t_R$	0.080	$0.065 + 0.007 \cdot SL$	$0.065 + 0.007 \cdot SL$	$0.056 + 0.008 \cdot SL$
	$t_F$	0.071	$0.056 + 0.008 \cdot SL$	$0.060 + 0.006 \cdot SL$	$0.056 + 0.007 \cdot SL$
	$t_{PLH}$	0.300	$0.290 + 0.005 \cdot SL$	$0.294 + 0.004 \cdot SL$	$0.305 + 0.003 \cdot SL$
	$t_{PHL}$	0.242	$0.231 + 0.006 \cdot SL$	$0.236 + 0.004 \cdot SL$	$0.250 + 0.004 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 22$ , \*Group3 :  $22 < SL$



Logic Symbol



Truth Table

S	YN0	YN1	YN2	YN3
0	$\overline{D00}$	$\overline{D01}$	$\overline{D02}$	$\overline{D03}$
1	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$

Cell Data

Input Load (SL)									Gate Count
D00	D10	D01	D11	D02	D12	D03	D13	S	6.00
1.0	1.1	1.0	1.1	1.0	1.1	1.0	1.1	5.3	



## MX2IX4

### 4-Bit 2 > 1 Inverting MUX

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### MX2IX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to YN0	$t_R$	0.269	$0.157 + 0.056 \cdot SL$	$0.147 + 0.058 \cdot SL$	$0.135 + 0.060 \cdot SL$
	$t_F$	0.199	$0.124 + 0.037 \cdot SL$	$0.114 + 0.040 \cdot SL$	$0.099 + 0.042 \cdot SL$
	$t_{PLH}$	0.144	$0.093 + 0.026 \cdot SL$	$0.092 + 0.026 \cdot SL$	$0.091 + 0.026 \cdot SL$
	$t_{PHL}$	0.117	$0.074 + 0.022 \cdot SL$	$0.079 + 0.020 \cdot SL$	$0.079 + 0.020 \cdot SL$
D10 to YN0	$t_R$	0.266	$0.150 + 0.058 \cdot SL$	$0.143 + 0.060 \cdot SL$	$0.136 + 0.060 \cdot SL$
	$t_F$	0.262	$0.186 + 0.038 \cdot SL$	$0.175 + 0.041 \cdot SL$	$0.160 + 0.043 \cdot SL$
	$t_{PLH}$	0.167	$0.114 + 0.027 \cdot SL$	$0.115 + 0.026 \cdot SL$	$0.116 + 0.026 \cdot SL$
	$t_{PHL}$	0.161	$0.118 + 0.021 \cdot SL$	$0.119 + 0.021 \cdot SL$	$0.120 + 0.021 \cdot SL$
S to YN0	$t_R$	0.261	$0.145 + 0.058 \cdot SL$	$0.137 + 0.060 \cdot SL$	$0.131 + 0.061 \cdot SL$
	$t_F$	0.222	$0.140 + 0.041 \cdot SL$	$0.136 + 0.042 \cdot SL$	$0.125 + 0.043 \cdot SL$
	$t_{PLH}$	0.248	$0.196 + 0.026 \cdot SL$	$0.197 + 0.026 \cdot SL$	$0.195 + 0.026 \cdot SL$
	$t_{PHL}$	0.200	$0.157 + 0.022 \cdot SL$	$0.161 + 0.021 \cdot SL$	$0.164 + 0.020 \cdot SL$
D01 to YN1	$t_R$	0.269	$0.156 + 0.057 \cdot SL$	$0.146 + 0.059 \cdot SL$	$0.134 + 0.060 \cdot SL$
	$t_F$	0.199	$0.124 + 0.037 \cdot SL$	$0.113 + 0.040 \cdot SL$	$0.098 + 0.042 \cdot SL$
	$t_{PLH}$	0.144	$0.093 + 0.026 \cdot SL$	$0.092 + 0.026 \cdot SL$	$0.091 + 0.026 \cdot SL$
	$t_{PHL}$	0.117	$0.074 + 0.022 \cdot SL$	$0.079 + 0.020 \cdot SL$	$0.079 + 0.020 \cdot SL$
D11 to YN1	$t_R$	0.266	$0.150 + 0.058 \cdot SL$	$0.143 + 0.060 \cdot SL$	$0.136 + 0.060 \cdot SL$
	$t_F$	0.257	$0.182 + 0.037 \cdot SL$	$0.172 + 0.040 \cdot SL$	$0.157 + 0.042 \cdot SL$
	$t_{PLH}$	0.167	$0.113 + 0.027 \cdot SL$	$0.115 + 0.026 \cdot SL$	$0.116 + 0.026 \cdot SL$
	$t_{PHL}$	0.158	$0.116 + 0.021 \cdot SL$	$0.117 + 0.021 \cdot SL$	$0.118 + 0.020 \cdot SL$
S to YN1	$t_R$	0.261	$0.146 + 0.058 \cdot SL$	$0.137 + 0.060 \cdot SL$	$0.131 + 0.061 \cdot SL$
	$t_F$	0.217	$0.137 + 0.040 \cdot SL$	$0.132 + 0.041 \cdot SL$	$0.122 + 0.042 \cdot SL$
	$t_{PLH}$	0.248	$0.196 + 0.026 \cdot SL$	$0.196 + 0.026 \cdot SL$	$0.195 + 0.026 \cdot SL$
	$t_{PHL}$	0.200	$0.157 + 0.022 \cdot SL$	$0.162 + 0.021 \cdot SL$	$0.164 + 0.020 \cdot SL$
D02 to YN2	$t_R$	0.271	$0.157 + 0.057 \cdot SL$	$0.148 + 0.059 \cdot SL$	$0.136 + 0.061 \cdot SL$
	$t_F$	0.199	$0.124 + 0.037 \cdot SL$	$0.114 + 0.040 \cdot SL$	$0.099 + 0.042 \cdot SL$
	$t_{PLH}$	0.145	$0.094 + 0.026 \cdot SL$	$0.093 + 0.026 \cdot SL$	$0.092 + 0.026 \cdot SL$
	$t_{PHL}$	0.117	$0.074 + 0.022 \cdot SL$	$0.079 + 0.020 \cdot SL$	$0.079 + 0.020 \cdot SL$
D12 to YN2	$t_R$	0.267	$0.151 + 0.058 \cdot SL$	$0.144 + 0.060 \cdot SL$	$0.137 + 0.061 \cdot SL$
	$t_F$	0.256	$0.181 + 0.037 \cdot SL$	$0.171 + 0.040 \cdot SL$	$0.156 + 0.042 \cdot SL$
	$t_{PLH}$	0.167	$0.113 + 0.027 \cdot SL$	$0.115 + 0.026 \cdot SL$	$0.116 + 0.026 \cdot SL$
	$t_{PHL}$	0.157	$0.116 + 0.021 \cdot SL$	$0.117 + 0.021 \cdot SL$	$0.118 + 0.020 \cdot SL$
S to YN2	$t_R$	0.260	$0.142 + 0.059 \cdot SL$	$0.137 + 0.060 \cdot SL$	$0.131 + 0.061 \cdot SL$
	$t_F$	0.216	$0.136 + 0.040 \cdot SL$	$0.131 + 0.041 \cdot SL$	$0.120 + 0.042 \cdot SL$
	$t_{PLH}$	0.249	$0.197 + 0.026 \cdot SL$	$0.197 + 0.026 \cdot SL$	$0.196 + 0.026 \cdot SL$
	$t_{PHL}$	0.201	$0.157 + 0.022 \cdot SL$	$0.162 + 0.021 \cdot SL$	$0.164 + 0.020 \cdot SL$
D03 to YN3	$t_R$	0.272	$0.157 + 0.057 \cdot SL$	$0.148 + 0.060 \cdot SL$	$0.136 + 0.061 \cdot SL$
	$t_F$	0.199	$0.124 + 0.037 \cdot SL$	$0.113 + 0.040 \cdot SL$	$0.098 + 0.042 \cdot SL$
	$t_{PLH}$	0.145	$0.093 + 0.026 \cdot SL$	$0.093 + 0.026 \cdot SL$	$0.092 + 0.026 \cdot SL$
	$t_{PHL}$	0.117	$0.074 + 0.022 \cdot SL$	$0.079 + 0.020 \cdot SL$	$0.079 + 0.020 \cdot SL$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)**MX2IX4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to YN3	$t_R$	0.266	$0.150 + 0.058 \cdot SL$	$0.143 + 0.060 \cdot SL$	$0.136 + 0.060 \cdot SL$
	$t_F$	0.255	$0.180 + 0.037 \cdot SL$	$0.171 + 0.040 \cdot SL$	$0.155 + 0.042 \cdot SL$
	$t_{PLH}$	0.166	$0.113 + 0.027 \cdot SL$	$0.114 + 0.026 \cdot SL$	$0.116 + 0.026 \cdot SL$
	$t_{PHL}$	0.157	$0.116 + 0.021 \cdot SL$	$0.117 + 0.021 \cdot SL$	$0.118 + 0.020 \cdot SL$
S to YN3	$t_R$	0.261	$0.142 + 0.059 \cdot SL$	$0.137 + 0.061 \cdot SL$	$0.131 + 0.061 \cdot SL$
	$t_F$	0.216	$0.136 + 0.040 \cdot SL$	$0.130 + 0.041 \cdot SL$	$0.120 + 0.042 \cdot SL$
	$t_{PLH}$	0.248	$0.196 + 0.026 \cdot SL$	$0.197 + 0.026 \cdot SL$	$0.195 + 0.026 \cdot SL$
	$t_{PHL}$	0.201	$0.157 + 0.022 \cdot SL$	$0.162 + 0.021 \cdot SL$	$0.164 + 0.020 \cdot SL$

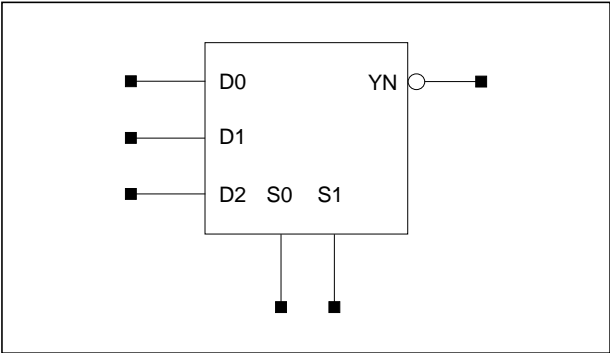
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



MX3I/MX3ID2/MX3ID4

3 > 1 Inverting MUX with 1X/2X/4X Drive

Logic Symbol



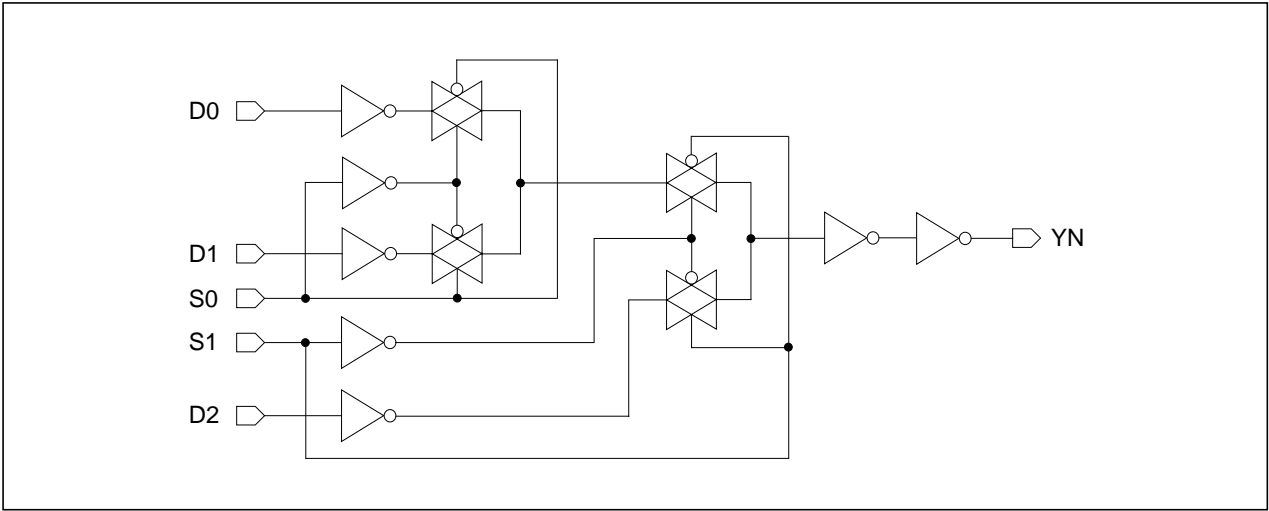
Truth Table

S0	S1	YN
0	0	D0
1	0	D1
x	1	D2

Cell Data

Input Load (SL)															
MX3I					MX3ID2					MX3ID4					
D0	D1	D2	S0	S1	D0	D1	D2	S0	S1	D0	D1	D2	S0	S1	
0.8	0.8	0.8	1.0	0.9	0.8	0.8	0.8	1.0	0.9	0.8	0.8	0.8	1.0	0.9	
Gate Count															
MX3I					MX3ID2					MX3ID4					
5.00					5.33					6.00					

Schematic Diagram





## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## MX3I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.121	$0.065 + 0.028 \cdot SL$	$0.057 + 0.030 \cdot SL$	$0.049 + 0.031 \cdot SL$
	$t_F$	0.103	$0.054 + 0.025 \cdot SL$	$0.050 + 0.025 \cdot SL$	$0.046 + 0.026 \cdot SL$
	$t_{PLH}$	0.350	$0.321 + 0.015 \cdot SL$	$0.326 + 0.014 \cdot SL$	$0.327 + 0.014 \cdot SL$
	$t_{PHL}$	0.349	$0.317 + 0.016 \cdot SL$	$0.324 + 0.014 \cdot SL$	$0.327 + 0.014 \cdot SL$
D1 to YN	$t_R$	0.121	$0.064 + 0.028 \cdot SL$	$0.057 + 0.030 \cdot SL$	$0.049 + 0.031 \cdot SL$
	$t_F$	0.104	$0.055 + 0.024 \cdot SL$	$0.051 + 0.025 \cdot SL$	$0.046 + 0.026 \cdot SL$
	$t_{PLH}$	0.353	$0.323 + 0.015 \cdot SL$	$0.328 + 0.014 \cdot SL$	$0.329 + 0.014 \cdot SL$
	$t_{PHL}$	0.345	$0.314 + 0.016 \cdot SL$	$0.321 + 0.014 \cdot SL$	$0.323 + 0.014 \cdot SL$
D2 to YN	$t_R$	0.112	$0.053 + 0.029 \cdot SL$	$0.047 + 0.031 \cdot SL$	$0.043 + 0.031 \cdot SL$
	$t_F$	0.099	$0.050 + 0.025 \cdot SL$	$0.046 + 0.026 \cdot SL$	$0.042 + 0.026 \cdot SL$
	$t_{PLH}$	0.252	$0.223 + 0.015 \cdot SL$	$0.227 + 0.014 \cdot SL$	$0.227 + 0.014 \cdot SL$
	$t_{PHL}$	0.246	$0.215 + 0.016 \cdot SL$	$0.222 + 0.014 \cdot SL$	$0.224 + 0.014 \cdot SL$
S0 to YN	$t_R$	0.121	$0.065 + 0.028 \cdot SL$	$0.057 + 0.030 \cdot SL$	$0.049 + 0.031 \cdot SL$
	$t_F$	0.103	$0.055 + 0.024 \cdot SL$	$0.051 + 0.025 \cdot SL$	$0.044 + 0.026 \cdot SL$
	$t_{PLH}$	0.359	$0.330 + 0.015 \cdot SL$	$0.335 + 0.014 \cdot SL$	$0.336 + 0.014 \cdot SL$
	$t_{PHL}$	0.370	$0.339 + 0.016 \cdot SL$	$0.345 + 0.014 \cdot SL$	$0.348 + 0.014 \cdot SL$
S1 to YN	$t_R$	0.115	$0.058 + 0.029 \cdot SL$	$0.051 + 0.030 \cdot SL$	$0.046 + 0.031 \cdot SL$
	$t_F$	0.102	$0.053 + 0.025 \cdot SL$	$0.050 + 0.025 \cdot SL$	$0.045 + 0.026 \cdot SL$
	$t_{PLH}$	0.271	$0.242 + 0.015 \cdot SL$	$0.246 + 0.014 \cdot SL$	$0.247 + 0.014 \cdot SL$
	$t_{PHL}$	0.298	$0.267 + 0.016 \cdot SL$	$0.274 + 0.014 \cdot SL$	$0.276 + 0.014 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## MX3I/MX3ID2/MX3ID4

### 3 > 1 Inverting MUX with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### MX3ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.095	$0.067 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.052 + 0.015 \cdot SL$
	$t_F$	0.082	$0.056 + 0.013 \cdot SL$	$0.058 + 0.012 \cdot SL$	$0.053 + 0.013 \cdot SL$
	$t_{PLH}$	0.364	$0.347 + 0.009 \cdot SL$	$0.353 + 0.007 \cdot SL$	$0.359 + 0.007 \cdot SL$
	$t_{PHL}$	0.357	$0.338 + 0.010 \cdot SL$	$0.346 + 0.008 \cdot SL$	$0.356 + 0.007 \cdot SL$
D1 to YN	$t_R$	0.094	$0.066 + 0.014 \cdot SL$	$0.066 + 0.014 \cdot SL$	$0.052 + 0.015 \cdot SL$
	$t_F$	0.082	$0.057 + 0.013 \cdot SL$	$0.058 + 0.012 \cdot SL$	$0.053 + 0.013 \cdot SL$
	$t_{PLH}$	0.367	$0.349 + 0.009 \cdot SL$	$0.355 + 0.007 \cdot SL$	$0.362 + 0.007 \cdot SL$
	$t_{PHL}$	0.354	$0.335 + 0.010 \cdot SL$	$0.343 + 0.008 \cdot SL$	$0.353 + 0.007 \cdot SL$
D2 to YN	$t_R$	0.083	$0.055 + 0.014 \cdot SL$	$0.052 + 0.015 \cdot SL$	$0.044 + 0.015 \cdot SL$
	$t_F$	0.076	$0.049 + 0.013 \cdot SL$	$0.053 + 0.012 \cdot SL$	$0.047 + 0.013 \cdot SL$
	$t_{PLH}$	0.260	$0.243 + 0.009 \cdot SL$	$0.249 + 0.007 \cdot SL$	$0.254 + 0.007 \cdot SL$
	$t_{PHL}$	0.252	$0.232 + 0.010 \cdot SL$	$0.240 + 0.008 \cdot SL$	$0.250 + 0.007 \cdot SL$
S0 to YN	$t_R$	0.095	$0.067 + 0.014 \cdot SL$	$0.065 + 0.014 \cdot SL$	$0.052 + 0.015 \cdot SL$
	$t_F$	0.082	$0.056 + 0.013 \cdot SL$	$0.060 + 0.012 \cdot SL$	$0.051 + 0.013 \cdot SL$
	$t_{PLH}$	0.373	$0.356 + 0.009 \cdot SL$	$0.362 + 0.007 \cdot SL$	$0.369 + 0.007 \cdot SL$
	$t_{PHL}$	0.379	$0.360 + 0.010 \cdot SL$	$0.368 + 0.008 \cdot SL$	$0.378 + 0.007 \cdot SL$
S1 to YN	$t_R$	0.090	$0.061 + 0.014 \cdot SL$	$0.061 + 0.014 \cdot SL$	$0.048 + 0.015 \cdot SL$
	$t_F$	0.082	$0.056 + 0.013 \cdot SL$	$0.058 + 0.012 \cdot SL$	$0.053 + 0.013 \cdot SL$
	$t_{PLH}$	0.283	$0.265 + 0.009 \cdot SL$	$0.271 + 0.007 \cdot SL$	$0.278 + 0.007 \cdot SL$
	$t_{PHL}$	0.307	$0.288 + 0.010 \cdot SL$	$0.295 + 0.008 \cdot SL$	$0.306 + 0.007 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)**MX3ID4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	$t_R$	0.092	$0.078 + 0.007 \cdot SL$	$0.077 + 0.007 \cdot SL$	$0.068 + 0.007 \cdot SL$
	$t_F$	0.079	$0.065 + 0.007 \cdot SL$	$0.067 + 0.006 \cdot SL$	$0.064 + 0.006 \cdot SL$
	$t_{PLH}$	0.405	$0.394 + 0.005 \cdot SL$	$0.400 + 0.004 \cdot SL$	$0.412 + 0.003 \cdot SL$
	$t_{PHL}$	0.378	$0.367 + 0.006 \cdot SL$	$0.373 + 0.004 \cdot SL$	$0.388 + 0.004 \cdot SL$
D1 to YN	$t_R$	0.092	$0.079 + 0.007 \cdot SL$	$0.078 + 0.007 \cdot SL$	$0.068 + 0.007 \cdot SL$
	$t_F$	0.079	$0.066 + 0.007 \cdot SL$	$0.067 + 0.006 \cdot SL$	$0.064 + 0.006 \cdot SL$
	$t_{PLH}$	0.407	$0.397 + 0.005 \cdot SL$	$0.402 + 0.004 \cdot SL$	$0.414 + 0.003 \cdot SL$
	$t_{PHL}$	0.375	$0.364 + 0.006 \cdot SL$	$0.370 + 0.004 \cdot SL$	$0.385 + 0.004 \cdot SL$
D2 to YN	$t_R$	0.080	$0.066 + 0.007 \cdot SL$	$0.066 + 0.007 \cdot SL$	$0.057 + 0.008 \cdot SL$
	$t_F$	0.071	$0.057 + 0.007 \cdot SL$	$0.060 + 0.006 \cdot SL$	$0.058 + 0.006 \cdot SL$
	$t_{PLH}$	0.290	$0.280 + 0.005 \cdot SL$	$0.285 + 0.004 \cdot SL$	$0.295 + 0.003 \cdot SL$
	$t_{PHL}$	0.268	$0.256 + 0.006 \cdot SL$	$0.262 + 0.004 \cdot SL$	$0.277 + 0.004 \cdot SL$
S0 to YN	$t_R$	0.093	$0.080 + 0.006 \cdot SL$	$0.078 + 0.007 \cdot SL$	$0.066 + 0.007 \cdot SL$
	$t_F$	0.078	$0.065 + 0.007 \cdot SL$	$0.067 + 0.006 \cdot SL$	$0.063 + 0.006 \cdot SL$
	$t_{PLH}$	0.414	$0.403 + 0.005 \cdot SL$	$0.409 + 0.004 \cdot SL$	$0.421 + 0.003 \cdot SL$
	$t_{PHL}$	0.400	$0.388 + 0.006 \cdot SL$	$0.394 + 0.004 \cdot SL$	$0.410 + 0.004 \cdot SL$
S1 to YN	$t_R$	0.088	$0.074 + 0.007 \cdot SL$	$0.074 + 0.007 \cdot SL$	$0.064 + 0.007 \cdot SL$
	$t_F$	0.077	$0.064 + 0.007 \cdot SL$	$0.066 + 0.006 \cdot SL$	$0.063 + 0.006 \cdot SL$
	$t_{PLH}$	0.323	$0.313 + 0.005 \cdot SL$	$0.318 + 0.004 \cdot SL$	$0.330 + 0.003 \cdot SL$
	$t_{PHL}$	0.327	$0.316 + 0.006 \cdot SL$	$0.322 + 0.004 \cdot SL$	$0.337 + 0.004 \cdot SL$

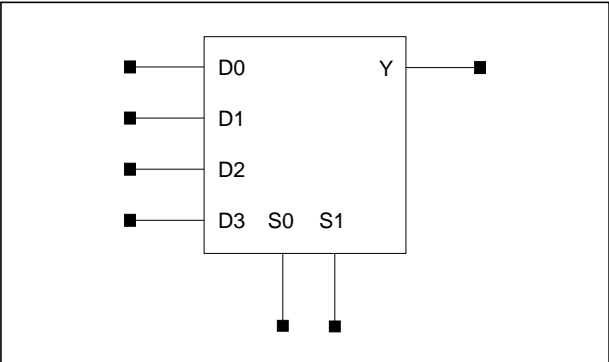
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 22$ , \*Group3 :  $22 < SL$



MX4/MX4D2/MX4D4

4 > 1 Non-Inverting MUX with 1X/2X/4X Drive

Logic Symbol



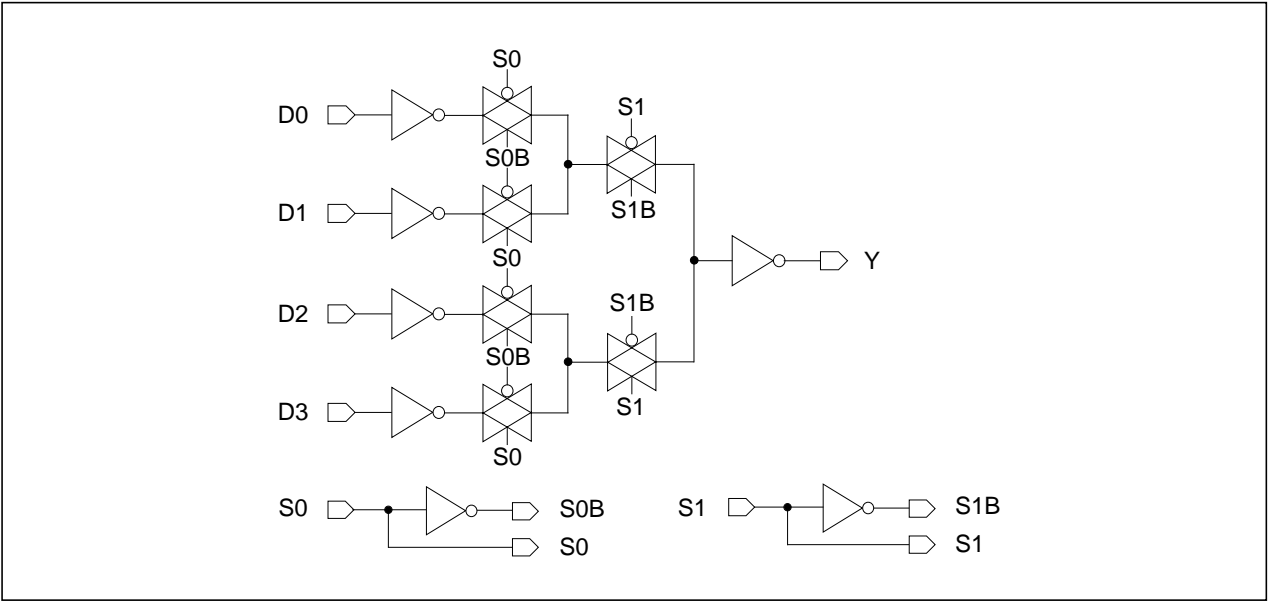
Truth Table

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)																	
MX4						MX4D2						MX4D4					
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1
0.8	0.8	0.8	0.8	1.8	1.0	0.8	0.8	0.8	0.8	1.8	1.0	0.8	0.8	0.8	0.8	1.8	1.0
Gate Count																	
MX4						MX4D2						MX4D4					
5.67						6.00						6.67					

Schematic Diagram





## 4 &gt; 1 Non-Inverting MUX with 1X/2X/4X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## MX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	$t_R$	0.163	$0.102 + 0.030 \cdot SL$	$0.106 + 0.029 \cdot SL$	$0.103 + 0.030 \cdot SL$
	$t_F$	0.185	$0.127 + 0.029 \cdot SL$	$0.133 + 0.028 \cdot SL$	$0.143 + 0.026 \cdot SL$
	$t_{PLH}$	0.294	$0.255 + 0.019 \cdot SL$	$0.268 + 0.016 \cdot SL$	$0.282 + 0.014 \cdot SL$
	$t_{PHL}$	0.322	$0.274 + 0.024 \cdot SL$	$0.293 + 0.019 \cdot SL$	$0.315 + 0.017 \cdot SL$
D1 to Y	$t_R$	0.163	$0.102 + 0.030 \cdot SL$	$0.105 + 0.029 \cdot SL$	$0.103 + 0.030 \cdot SL$
	$t_F$	0.185	$0.127 + 0.029 \cdot SL$	$0.132 + 0.028 \cdot SL$	$0.143 + 0.026 \cdot SL$
	$t_{PLH}$	0.294	$0.255 + 0.019 \cdot SL$	$0.268 + 0.016 \cdot SL$	$0.282 + 0.014 \cdot SL$
	$t_{PHL}$	0.323	$0.275 + 0.024 \cdot SL$	$0.294 + 0.019 \cdot SL$	$0.316 + 0.017 \cdot SL$
D2 to Y	$t_R$	0.161	$0.100 + 0.031 \cdot SL$	$0.105 + 0.029 \cdot SL$	$0.101 + 0.030 \cdot SL$
	$t_F$	0.183	$0.125 + 0.029 \cdot SL$	$0.132 + 0.027 \cdot SL$	$0.140 + 0.026 \cdot SL$
	$t_{PLH}$	0.289	$0.251 + 0.019 \cdot SL$	$0.264 + 0.016 \cdot SL$	$0.278 + 0.014 \cdot SL$
	$t_{PHL}$	0.319	$0.271 + 0.024 \cdot SL$	$0.290 + 0.019 \cdot SL$	$0.311 + 0.017 \cdot SL$
D3 to Y	$t_R$	0.160	$0.099 + 0.031 \cdot SL$	$0.104 + 0.029 \cdot SL$	$0.101 + 0.030 \cdot SL$
	$t_F$	0.184	$0.125 + 0.029 \cdot SL$	$0.132 + 0.027 \cdot SL$	$0.141 + 0.026 \cdot SL$
	$t_{PLH}$	0.288	$0.249 + 0.019 \cdot SL$	$0.262 + 0.016 \cdot SL$	$0.276 + 0.014 \cdot SL$
	$t_{PHL}$	0.320	$0.272 + 0.024 \cdot SL$	$0.291 + 0.019 \cdot SL$	$0.312 + 0.017 \cdot SL$
S0 to Y	$t_R$	0.165	$0.105 + 0.030 \cdot SL$	$0.106 + 0.030 \cdot SL$	$0.105 + 0.030 \cdot SL$
	$t_F$	0.185	$0.126 + 0.029 \cdot SL$	$0.133 + 0.027 \cdot SL$	$0.142 + 0.026 \cdot SL$
	$t_{PLH}$	0.319	$0.280 + 0.019 \cdot SL$	$0.293 + 0.016 \cdot SL$	$0.307 + 0.014 \cdot SL$
	$t_{PHL}$	0.336	$0.288 + 0.024 \cdot SL$	$0.307 + 0.019 \cdot SL$	$0.329 + 0.017 \cdot SL$
S1 to Y	$t_R$	0.153	$0.091 + 0.031 \cdot SL$	$0.095 + 0.030 \cdot SL$	$0.096 + 0.030 \cdot SL$
	$t_F$	0.167	$0.106 + 0.030 \cdot SL$	$0.115 + 0.028 \cdot SL$	$0.126 + 0.027 \cdot SL$
	$t_{PLH}$	0.237	$0.198 + 0.019 \cdot SL$	$0.211 + 0.016 \cdot SL$	$0.225 + 0.014 \cdot SL$
	$t_{PHL}$	0.255	$0.207 + 0.024 \cdot SL$	$0.225 + 0.019 \cdot SL$	$0.246 + 0.017 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## MX4/MX4D2/MX4D4

### 4 > 1 Non-Inverting MUX with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### MX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	$t_R$	0.149	$0.119 + 0.015 \cdot SL$	$0.118 + 0.015 \cdot SL$	$0.122 + 0.015 \cdot SL$
	$t_F$	0.178	$0.143 + 0.018 \cdot SL$	$0.156 + 0.014 \cdot SL$	$0.168 + 0.013 \cdot SL$
	$t_{PLH}$	0.312	$0.286 + 0.013 \cdot SL$	$0.300 + 0.009 \cdot SL$	$0.323 + 0.008 \cdot SL$
	$t_{PHL}$	0.341	$0.310 + 0.016 \cdot SL$	$0.326 + 0.012 \cdot SL$	$0.360 + 0.009 \cdot SL$
D1 to Y	$t_R$	0.148	$0.118 + 0.015 \cdot SL$	$0.118 + 0.015 \cdot SL$	$0.121 + 0.015 \cdot SL$
	$t_F$	0.178	$0.143 + 0.018 \cdot SL$	$0.156 + 0.014 \cdot SL$	$0.168 + 0.013 \cdot SL$
	$t_{PLH}$	0.312	$0.286 + 0.013 \cdot SL$	$0.300 + 0.009 \cdot SL$	$0.323 + 0.008 \cdot SL$
	$t_{PHL}$	0.342	$0.310 + 0.016 \cdot SL$	$0.327 + 0.012 \cdot SL$	$0.360 + 0.009 \cdot SL$
D2 to Y	$t_R$	0.147	$0.117 + 0.015 \cdot SL$	$0.116 + 0.015 \cdot SL$	$0.121 + 0.015 \cdot SL$
	$t_F$	0.177	$0.143 + 0.017 \cdot SL$	$0.155 + 0.014 \cdot SL$	$0.166 + 0.013 \cdot SL$
	$t_{PLH}$	0.308	$0.282 + 0.013 \cdot SL$	$0.296 + 0.009 \cdot SL$	$0.318 + 0.008 \cdot SL$
	$t_{PHL}$	0.338	$0.307 + 0.016 \cdot SL$	$0.324 + 0.012 \cdot SL$	$0.356 + 0.009 \cdot SL$
D3 to Y	$t_R$	0.147	$0.117 + 0.015 \cdot SL$	$0.116 + 0.015 \cdot SL$	$0.121 + 0.015 \cdot SL$
	$t_F$	0.178	$0.143 + 0.017 \cdot SL$	$0.155 + 0.014 \cdot SL$	$0.167 + 0.013 \cdot SL$
	$t_{PLH}$	0.306	$0.280 + 0.013 \cdot SL$	$0.294 + 0.009 \cdot SL$	$0.317 + 0.008 \cdot SL$
	$t_{PHL}$	0.340	$0.308 + 0.016 \cdot SL$	$0.325 + 0.012 \cdot SL$	$0.358 + 0.009 \cdot SL$
S0 to Y	$t_R$	0.150	$0.120 + 0.015 \cdot SL$	$0.120 + 0.015 \cdot SL$	$0.122 + 0.015 \cdot SL$
	$t_F$	0.179	$0.144 + 0.017 \cdot SL$	$0.155 + 0.014 \cdot SL$	$0.168 + 0.013 \cdot SL$
	$t_{PLH}$	0.336	$0.310 + 0.013 \cdot SL$	$0.324 + 0.009 \cdot SL$	$0.347 + 0.008 \cdot SL$
	$t_{PHL}$	0.354	$0.323 + 0.016 \cdot SL$	$0.339 + 0.012 \cdot SL$	$0.373 + 0.009 \cdot SL$
S1 to Y	$t_R$	0.141	$0.111 + 0.015 \cdot SL$	$0.110 + 0.015 \cdot SL$	$0.117 + 0.015 \cdot SL$
	$t_F$	0.167	$0.132 + 0.017 \cdot SL$	$0.143 + 0.015 \cdot SL$	$0.157 + 0.014 \cdot SL$
	$t_{PLH}$	0.252	$0.226 + 0.013 \cdot SL$	$0.240 + 0.009 \cdot SL$	$0.263 + 0.008 \cdot SL$
	$t_{PHL}$	0.272	$0.241 + 0.016 \cdot SL$	$0.258 + 0.012 \cdot SL$	$0.291 + 0.009 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## 4 &gt; 1 Non-Inverting MUX with 1X/2X/4X Drive

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

## MX4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	$t_R$	0.189	$0.175 + 0.007 \cdot SL$	$0.173 + 0.008 \cdot SL$	$0.175 + 0.007 \cdot SL$
	$t_F$	0.234	$0.216 + 0.009 \cdot SL$	$0.220 + 0.008 \cdot SL$	$0.242 + 0.007 \cdot SL$
	$t_{PLH}$	0.387	$0.369 + 0.009 \cdot SL$	$0.380 + 0.006 \cdot SL$	$0.415 + 0.004 \cdot SL$
	$t_{PHL}$	0.431	$0.412 + 0.010 \cdot SL$	$0.423 + 0.007 \cdot SL$	$0.466 + 0.005 \cdot SL$
D1 to Y	$t_R$	0.189	$0.175 + 0.007 \cdot SL$	$0.173 + 0.007 \cdot SL$	$0.174 + 0.007 \cdot SL$
	$t_F$	0.233	$0.215 + 0.009 \cdot SL$	$0.219 + 0.008 \cdot SL$	$0.241 + 0.007 \cdot SL$
	$t_{PLH}$	0.386	$0.369 + 0.009 \cdot SL$	$0.380 + 0.006 \cdot SL$	$0.414 + 0.004 \cdot SL$
	$t_{PHL}$	0.432	$0.412 + 0.010 \cdot SL$	$0.423 + 0.007 \cdot SL$	$0.466 + 0.005 \cdot SL$
D2 to Y	$t_R$	0.188	$0.173 + 0.007 \cdot SL$	$0.172 + 0.008 \cdot SL$	$0.174 + 0.007 \cdot SL$
	$t_F$	0.232	$0.214 + 0.009 \cdot SL$	$0.219 + 0.008 \cdot SL$	$0.240 + 0.007 \cdot SL$
	$t_{PLH}$	0.382	$0.365 + 0.009 \cdot SL$	$0.376 + 0.006 \cdot SL$	$0.410 + 0.004 \cdot SL$
	$t_{PHL}$	0.428	$0.408 + 0.010 \cdot SL$	$0.420 + 0.007 \cdot SL$	$0.462 + 0.005 \cdot SL$
D3 to Y	$t_R$	0.187	$0.173 + 0.007 \cdot SL$	$0.172 + 0.008 \cdot SL$	$0.174 + 0.007 \cdot SL$
	$t_F$	0.232	$0.215 + 0.009 \cdot SL$	$0.219 + 0.008 \cdot SL$	$0.240 + 0.007 \cdot SL$
	$t_{PLH}$	0.380	$0.363 + 0.009 \cdot SL$	$0.374 + 0.006 \cdot SL$	$0.408 + 0.004 \cdot SL$
	$t_{PHL}$	0.429	$0.410 + 0.010 \cdot SL$	$0.421 + 0.007 \cdot SL$	$0.464 + 0.005 \cdot SL$
S0 to Y	$t_R$	0.190	$0.176 + 0.007 \cdot SL$	$0.174 + 0.007 \cdot SL$	$0.175 + 0.007 \cdot SL$
	$t_F$	0.232	$0.213 + 0.009 \cdot SL$	$0.220 + 0.008 \cdot SL$	$0.241 + 0.007 \cdot SL$
	$t_{PLH}$	0.409	$0.392 + 0.009 \cdot SL$	$0.403 + 0.006 \cdot SL$	$0.437 + 0.004 \cdot SL$
	$t_{PHL}$	0.442	$0.422 + 0.010 \cdot SL$	$0.434 + 0.007 \cdot SL$	$0.477 + 0.005 \cdot SL$
S1 to Y	$t_R$	0.187	$0.173 + 0.007 \cdot SL$	$0.171 + 0.008 \cdot SL$	$0.173 + 0.007 \cdot SL$
	$t_F$	0.230	$0.212 + 0.009 \cdot SL$	$0.216 + 0.008 \cdot SL$	$0.237 + 0.007 \cdot SL$
	$t_{PLH}$	0.323	$0.305 + 0.009 \cdot SL$	$0.317 + 0.006 \cdot SL$	$0.351 + 0.004 \cdot SL$
	$t_{PHL}$	0.362	$0.342 + 0.010 \cdot SL$	$0.354 + 0.007 \cdot SL$	$0.397 + 0.005 \cdot SL$

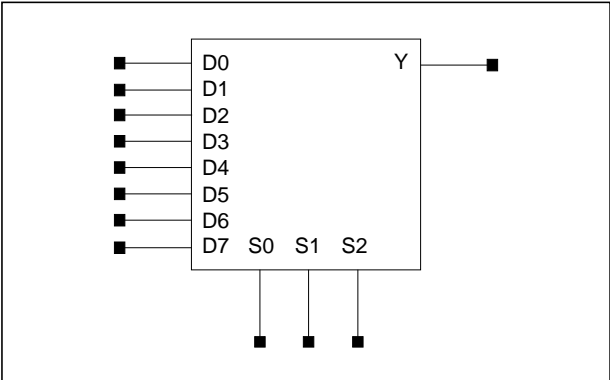
\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 22$ , \*Group3 :  $22 < SL$



MX8/MX8D2/MX8D4

8 > 1 Non-Inverting MUX with 1X/2X/4X Drive

Logic Symbol



Truth Table

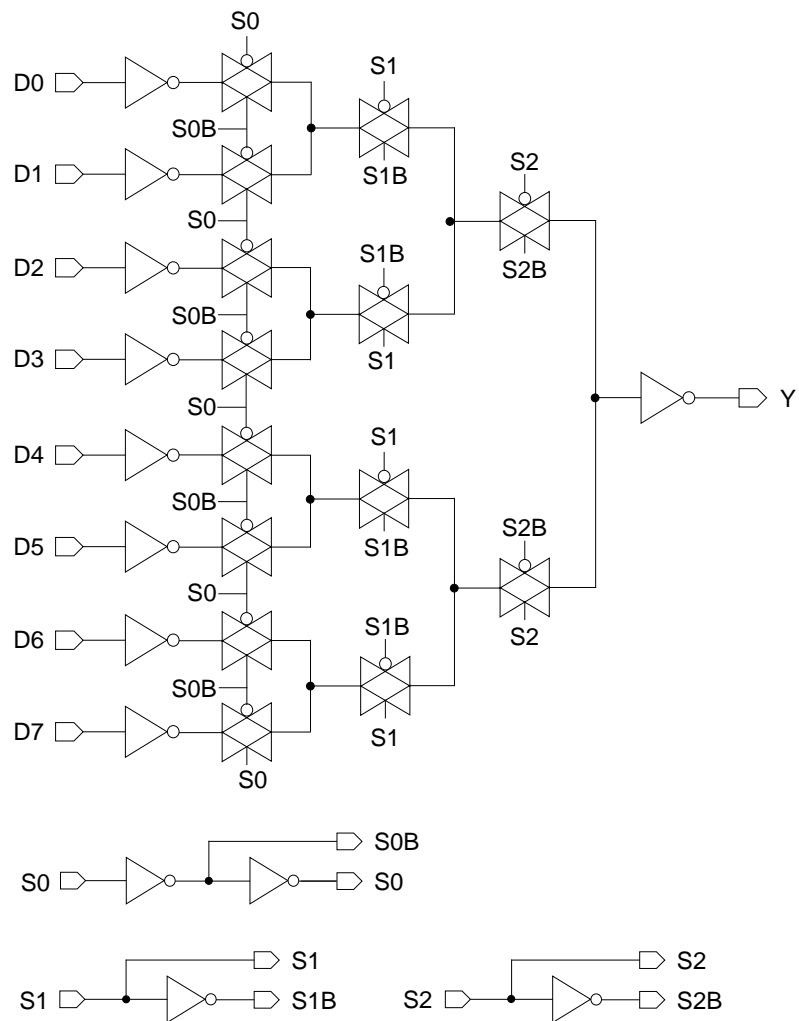
S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

Cell Data

Input Load (SL)											Gate Count
MX8											MX8
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.7	1.0	10.67
MX8D2											MX8D2
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.7	1.0	11.00
MX8D4											MX8D4
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.7	1.0	11.67



## Schematic Diagram





## MX8/MX8D2/MX8D4

### 8 > 1 Non-Inverting MUX with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### MX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	$t_R$	0.196	$0.136 + 0.030 \cdot SL$	$0.139 + 0.029 \cdot SL$	$0.142 + 0.029 \cdot SL$
	$t_F$	0.245	$0.185 + 0.030 \cdot SL$	$0.200 + 0.026 \cdot SL$	$0.208 + 0.025 \cdot SL$
	$t_{PLH}$	0.414	$0.372 + 0.021 \cdot SL$	$0.389 + 0.017 \cdot SL$	$0.406 + 0.015 \cdot SL$
	$t_{PHL}$	0.480	$0.426 + 0.027 \cdot SL$	$0.450 + 0.021 \cdot SL$	$0.479 + 0.018 \cdot SL$
D1 to Y	$t_R$	0.196	$0.136 + 0.030 \cdot SL$	$0.139 + 0.029 \cdot SL$	$0.142 + 0.029 \cdot SL$
	$t_F$	0.245	$0.185 + 0.030 \cdot SL$	$0.200 + 0.026 \cdot SL$	$0.208 + 0.025 \cdot SL$
	$t_{PLH}$	0.415	$0.372 + 0.021 \cdot SL$	$0.389 + 0.017 \cdot SL$	$0.406 + 0.015 \cdot SL$
	$t_{PHL}$	0.481	$0.427 + 0.027 \cdot SL$	$0.450 + 0.021 \cdot SL$	$0.479 + 0.018 \cdot SL$
D2 to Y	$t_R$	0.193	$0.133 + 0.030 \cdot SL$	$0.137 + 0.029 \cdot SL$	$0.140 + 0.029 \cdot SL$
	$t_F$	0.243	$0.184 + 0.030 \cdot SL$	$0.195 + 0.027 \cdot SL$	$0.206 + 0.025 \cdot SL$
	$t_{PLH}$	0.407	$0.364 + 0.021 \cdot SL$	$0.381 + 0.017 \cdot SL$	$0.398 + 0.015 \cdot SL$
	$t_{PHL}$	0.473	$0.419 + 0.027 \cdot SL$	$0.443 + 0.021 \cdot SL$	$0.471 + 0.018 \cdot SL$
D3 to Y	$t_R$	0.193	$0.133 + 0.030 \cdot SL$	$0.137 + 0.029 \cdot SL$	$0.140 + 0.029 \cdot SL$
	$t_F$	0.243	$0.184 + 0.030 \cdot SL$	$0.195 + 0.027 \cdot SL$	$0.206 + 0.025 \cdot SL$
	$t_{PLH}$	0.406	$0.364 + 0.021 \cdot SL$	$0.381 + 0.017 \cdot SL$	$0.398 + 0.015 \cdot SL$
	$t_{PHL}$	0.473	$0.419 + 0.027 \cdot SL$	$0.443 + 0.021 \cdot SL$	$0.472 + 0.018 \cdot SL$
D4 to Y	$t_R$	0.193	$0.132 + 0.030 \cdot SL$	$0.136 + 0.029 \cdot SL$	$0.140 + 0.029 \cdot SL$
	$t_F$	0.241	$0.182 + 0.030 \cdot SL$	$0.195 + 0.027 \cdot SL$	$0.205 + 0.025 \cdot SL$
	$t_{PLH}$	0.403	$0.361 + 0.021 \cdot SL$	$0.378 + 0.017 \cdot SL$	$0.395 + 0.015 \cdot SL$
	$t_{PHL}$	0.470	$0.416 + 0.027 \cdot SL$	$0.440 + 0.021 \cdot SL$	$0.468 + 0.018 \cdot SL$
D5 to Y	$t_R$	0.193	$0.132 + 0.030 \cdot SL$	$0.136 + 0.029 \cdot SL$	$0.140 + 0.029 \cdot SL$
	$t_F$	0.241	$0.182 + 0.030 \cdot SL$	$0.195 + 0.027 \cdot SL$	$0.205 + 0.025 \cdot SL$
	$t_{PLH}$	0.403	$0.361 + 0.021 \cdot SL$	$0.377 + 0.017 \cdot SL$	$0.395 + 0.015 \cdot SL$
	$t_{PHL}$	0.470	$0.416 + 0.027 \cdot SL$	$0.440 + 0.021 \cdot SL$	$0.468 + 0.018 \cdot SL$
D6 to Y	$t_R$	0.193	$0.133 + 0.030 \cdot SL$	$0.135 + 0.029 \cdot SL$	$0.139 + 0.029 \cdot SL$
	$t_F$	0.240	$0.180 + 0.030 \cdot SL$	$0.194 + 0.026 \cdot SL$	$0.204 + 0.025 \cdot SL$
	$t_{PLH}$	0.400	$0.357 + 0.021 \cdot SL$	$0.374 + 0.017 \cdot SL$	$0.391 + 0.015 \cdot SL$
	$t_{PHL}$	0.467	$0.414 + 0.027 \cdot SL$	$0.437 + 0.021 \cdot SL$	$0.465 + 0.017 \cdot SL$
D7 to Y	$t_R$	0.192	$0.133 + 0.030 \cdot SL$	$0.135 + 0.029 \cdot SL$	$0.139 + 0.029 \cdot SL$
	$t_F$	0.240	$0.180 + 0.030 \cdot SL$	$0.194 + 0.026 \cdot SL$	$0.204 + 0.025 \cdot SL$
	$t_{PLH}$	0.399	$0.357 + 0.021 \cdot SL$	$0.374 + 0.017 \cdot SL$	$0.391 + 0.015 \cdot SL$
	$t_{PHL}$	0.467	$0.414 + 0.027 \cdot SL$	$0.437 + 0.021 \cdot SL$	$0.465 + 0.017 \cdot SL$
S0 to Y	$t_R$	0.195	$0.135 + 0.030 \cdot SL$	$0.139 + 0.029 \cdot SL$	$0.141 + 0.029 \cdot SL$
	$t_F$	0.243	$0.183 + 0.030 \cdot SL$	$0.196 + 0.026 \cdot SL$	$0.206 + 0.025 \cdot SL$
	$t_{PLH}$	0.599	$0.557 + 0.021 \cdot SL$	$0.573 + 0.017 \cdot SL$	$0.590 + 0.015 \cdot SL$
	$t_{PHL}$	0.662	$0.609 + 0.027 \cdot SL$	$0.632 + 0.021 \cdot SL$	$0.660 + 0.018 \cdot SL$
S1 to Y	$t_R$	0.188	$0.128 + 0.030 \cdot SL$	$0.130 + 0.029 \cdot SL$	$0.134 + 0.029 \cdot SL$
	$t_F$	0.225	$0.165 + 0.030 \cdot SL$	$0.177 + 0.027 \cdot SL$	$0.190 + 0.026 \cdot SL$
	$t_{PLH}$	0.339	$0.297 + 0.021 \cdot SL$	$0.313 + 0.017 \cdot SL$	$0.331 + 0.015 \cdot SL$
	$t_{PHL}$	0.366	$0.313 + 0.027 \cdot SL$	$0.336 + 0.021 \cdot SL$	$0.364 + 0.017 \cdot SL$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)**MX8**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to Y	$t_R$	0.168	$0.104 + 0.032 \cdot SL$	$0.111 + 0.030 \cdot SL$	$0.117 + 0.029 \cdot SL$
	$t_F$	0.185	$0.120 + 0.033 \cdot SL$	$0.136 + 0.028 \cdot SL$	$0.152 + 0.027 \cdot SL$
	$t_{PLH}$	0.252	$0.211 + 0.020 \cdot SL$	$0.225 + 0.017 \cdot SL$	$0.241 + 0.015 \cdot SL$
	$t_{PHL}$	0.267	$0.216 + 0.025 \cdot SL$	$0.237 + 0.020 \cdot SL$	$0.262 + 0.017 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 8$ , \*Group3 :  $8 < SL$



## MX8/MX8D2/MX8D4

### 8 > 1 Non-Inverting MUX with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### MX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	$t_R$	0.189	$0.159 + 0.015 \cdot SL$	$0.160 + 0.015 \cdot SL$	$0.164 + 0.015 \cdot SL$
	$t_F$	0.248	$0.212 + 0.018 \cdot SL$	$0.227 + 0.014 \cdot SL$	$0.245 + 0.013 \cdot SL$
	$t_{PLH}$	0.444	$0.416 + 0.014 \cdot SL$	$0.432 + 0.010 \cdot SL$	$0.460 + 0.008 \cdot SL$
	$t_{PHL}$	0.514	$0.480 + 0.017 \cdot SL$	$0.498 + 0.013 \cdot SL$	$0.539 + 0.010 \cdot SL$
D1 to Y	$t_R$	0.189	$0.159 + 0.015 \cdot SL$	$0.159 + 0.015 \cdot SL$	$0.164 + 0.015 \cdot SL$
	$t_F$	0.248	$0.212 + 0.018 \cdot SL$	$0.227 + 0.014 \cdot SL$	$0.245 + 0.013 \cdot SL$
	$t_{PLH}$	0.445	$0.416 + 0.014 \cdot SL$	$0.433 + 0.010 \cdot SL$	$0.460 + 0.008 \cdot SL$
	$t_{PHL}$	0.515	$0.480 + 0.017 \cdot SL$	$0.498 + 0.013 \cdot SL$	$0.539 + 0.010 \cdot SL$
D2 to Y	$t_R$	0.188	$0.157 + 0.016 \cdot SL$	$0.160 + 0.015 \cdot SL$	$0.163 + 0.015 \cdot SL$
	$t_F$	0.245	$0.209 + 0.018 \cdot SL$	$0.223 + 0.014 \cdot SL$	$0.242 + 0.013 \cdot SL$
	$t_{PLH}$	0.437	$0.408 + 0.014 \cdot SL$	$0.424 + 0.010 \cdot SL$	$0.452 + 0.008 \cdot SL$
	$t_{PHL}$	0.507	$0.473 + 0.017 \cdot SL$	$0.491 + 0.013 \cdot SL$	$0.531 + 0.010 \cdot SL$
D3 to Y	$t_R$	0.188	$0.157 + 0.016 \cdot SL$	$0.160 + 0.015 \cdot SL$	$0.163 + 0.015 \cdot SL$
	$t_F$	0.245	$0.209 + 0.018 \cdot SL$	$0.223 + 0.014 \cdot SL$	$0.242 + 0.013 \cdot SL$
	$t_{PLH}$	0.436	$0.408 + 0.014 \cdot SL$	$0.424 + 0.010 \cdot SL$	$0.451 + 0.008 \cdot SL$
	$t_{PHL}$	0.507	$0.473 + 0.017 \cdot SL$	$0.491 + 0.013 \cdot SL$	$0.532 + 0.010 \cdot SL$
D4 to Y	$t_R$	0.187	$0.156 + 0.016 \cdot SL$	$0.159 + 0.015 \cdot SL$	$0.161 + 0.015 \cdot SL$
	$t_F$	0.245	$0.209 + 0.018 \cdot SL$	$0.223 + 0.014 \cdot SL$	$0.241 + 0.013 \cdot SL$
	$t_{PLH}$	0.434	$0.405 + 0.014 \cdot SL$	$0.421 + 0.010 \cdot SL$	$0.449 + 0.008 \cdot SL$
	$t_{PHL}$	0.505	$0.470 + 0.017 \cdot SL$	$0.488 + 0.013 \cdot SL$	$0.529 + 0.010 \cdot SL$
D5 to Y	$t_R$	0.187	$0.156 + 0.016 \cdot SL$	$0.159 + 0.015 \cdot SL$	$0.161 + 0.015 \cdot SL$
	$t_F$	0.245	$0.209 + 0.018 \cdot SL$	$0.223 + 0.014 \cdot SL$	$0.241 + 0.013 \cdot SL$
	$t_{PLH}$	0.434	$0.405 + 0.014 \cdot SL$	$0.421 + 0.010 \cdot SL$	$0.449 + 0.008 \cdot SL$
	$t_{PHL}$	0.505	$0.470 + 0.017 \cdot SL$	$0.488 + 0.013 \cdot SL$	$0.529 + 0.010 \cdot SL$
D6 to Y	$t_R$	0.187	$0.156 + 0.015 \cdot SL$	$0.158 + 0.015 \cdot SL$	$0.161 + 0.015 \cdot SL$
	$t_F$	0.244	$0.208 + 0.018 \cdot SL$	$0.223 + 0.014 \cdot SL$	$0.240 + 0.013 \cdot SL$
	$t_{PLH}$	0.430	$0.402 + 0.014 \cdot SL$	$0.418 + 0.010 \cdot SL$	$0.445 + 0.008 \cdot SL$
	$t_{PHL}$	0.502	$0.468 + 0.017 \cdot SL$	$0.486 + 0.013 \cdot SL$	$0.526 + 0.010 \cdot SL$
D7 to Y	$t_R$	0.187	$0.156 + 0.015 \cdot SL$	$0.158 + 0.015 \cdot SL$	$0.161 + 0.015 \cdot SL$
	$t_F$	0.244	$0.208 + 0.018 \cdot SL$	$0.223 + 0.014 \cdot SL$	$0.240 + 0.013 \cdot SL$
	$t_{PLH}$	0.430	$0.401 + 0.014 \cdot SL$	$0.418 + 0.010 \cdot SL$	$0.445 + 0.008 \cdot SL$
	$t_{PHL}$	0.502	$0.468 + 0.017 \cdot SL$	$0.486 + 0.013 \cdot SL$	$0.526 + 0.010 \cdot SL$
S0 to Y	$t_R$	0.189	$0.159 + 0.015 \cdot SL$	$0.161 + 0.015 \cdot SL$	$0.163 + 0.015 \cdot SL$
	$t_F$	0.244	$0.208 + 0.018 \cdot SL$	$0.223 + 0.014 \cdot SL$	$0.241 + 0.013 \cdot SL$
	$t_{PLH}$	0.629	$0.601 + 0.014 \cdot SL$	$0.617 + 0.010 \cdot SL$	$0.644 + 0.008 \cdot SL$
	$t_{PHL}$	0.697	$0.663 + 0.017 \cdot SL$	$0.680 + 0.013 \cdot SL$	$0.721 + 0.010 \cdot SL$
S1 to Y	$t_R$	0.184	$0.154 + 0.015 \cdot SL$	$0.154 + 0.015 \cdot SL$	$0.158 + 0.015 \cdot SL$
	$t_F$	0.233	$0.197 + 0.018 \cdot SL$	$0.211 + 0.014 \cdot SL$	$0.229 + 0.013 \cdot SL$
	$t_{PLH}$	0.369	$0.340 + 0.014 \cdot SL$	$0.356 + 0.010 \cdot SL$	$0.383 + 0.008 \cdot SL$
	$t_{PHL}$	0.399	$0.364 + 0.017 \cdot SL$	$0.382 + 0.013 \cdot SL$	$0.423 + 0.010 \cdot SL$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)**MX8D2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to Y	$t_R$	0.169	$0.138 + 0.016 \cdot SL$	$0.139 + 0.015 \cdot SL$	$0.146 + 0.015 \cdot SL$
	$t_F$	0.201	$0.163 + 0.019 \cdot SL$	$0.178 + 0.015 \cdot SL$	$0.200 + 0.013 \cdot SL$
	$t_{PLH}$	0.276	$0.248 + 0.014 \cdot SL$	$0.263 + 0.010 \cdot SL$	$0.290 + 0.008 \cdot SL$
	$t_{PHL}$	0.294	$0.260 + 0.017 \cdot SL$	$0.278 + 0.013 \cdot SL$	$0.318 + 0.010 \cdot SL$

\*Group1 :  $SL < 4$ , \*Group2 :  $4 \leq SL \leq 13$ , \*Group3 :  $13 < SL$



## MX8/MX8D2/MX8D4

### 8 > 1 Non-Inverting MUX with 1X/2X/4X Drive

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.21$  ns, SL: Standard Load)

#### MX8D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t <sub>R</sub>	0.247	$0.234 + 0.007 \cdot SL$	$0.231 + 0.007 \cdot SL$	$0.231 + 0.007 \cdot SL$
	t <sub>F</sub>	0.323	$0.308 + 0.008 \cdot SL$	$0.307 + 0.008 \cdot SL$	$0.338 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.543	$0.525 + 0.009 \cdot SL$	$0.536 + 0.006 \cdot SL$	$0.576 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.635	$0.614 + 0.011 \cdot SL$	$0.626 + 0.008 \cdot SL$	$0.673 + 0.005 \cdot SL$
D1 to Y	t <sub>R</sub>	0.247	$0.234 + 0.007 \cdot SL$	$0.231 + 0.007 \cdot SL$	$0.231 + 0.007 \cdot SL$
	t <sub>F</sub>	0.323	$0.308 + 0.008 \cdot SL$	$0.306 + 0.008 \cdot SL$	$0.338 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.544	$0.525 + 0.009 \cdot SL$	$0.537 + 0.006 \cdot SL$	$0.576 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.636	$0.615 + 0.011 \cdot SL$	$0.627 + 0.008 \cdot SL$	$0.674 + 0.005 \cdot SL$
D2 to Y	t <sub>R</sub>	0.247	$0.234 + 0.006 \cdot SL$	$0.229 + 0.007 \cdot SL$	$0.229 + 0.007 \cdot SL$
	t <sub>F</sub>	0.322	$0.306 + 0.008 \cdot SL$	$0.305 + 0.008 \cdot SL$	$0.336 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.535	$0.516 + 0.009 \cdot SL$	$0.528 + 0.006 \cdot SL$	$0.567 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.628	$0.607 + 0.010 \cdot SL$	$0.619 + 0.008 \cdot SL$	$0.666 + 0.005 \cdot SL$
D3 to Y	t <sub>R</sub>	0.247	$0.234 + 0.006 \cdot SL$	$0.229 + 0.007 \cdot SL$	$0.229 + 0.007 \cdot SL$
	t <sub>F</sub>	0.322	$0.306 + 0.008 \cdot SL$	$0.305 + 0.008 \cdot SL$	$0.336 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.535	$0.516 + 0.009 \cdot SL$	$0.528 + 0.006 \cdot SL$	$0.567 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.628	$0.607 + 0.011 \cdot SL$	$0.619 + 0.008 \cdot SL$	$0.666 + 0.005 \cdot SL$
D4 to Y	t <sub>R</sub>	0.245	$0.233 + 0.006 \cdot SL$	$0.228 + 0.007 \cdot SL$	$0.228 + 0.007 \cdot SL$
	t <sub>F</sub>	0.321	$0.305 + 0.008 \cdot SL$	$0.304 + 0.008 \cdot SL$	$0.335 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.532	$0.514 + 0.009 \cdot SL$	$0.525 + 0.006 \cdot SL$	$0.564 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.626	$0.605 + 0.010 \cdot SL$	$0.617 + 0.008 \cdot SL$	$0.663 + 0.005 \cdot SL$
D5 to Y	t <sub>R</sub>	0.245	$0.232 + 0.006 \cdot SL$	$0.228 + 0.007 \cdot SL$	$0.228 + 0.007 \cdot SL$
	t <sub>F</sub>	0.321	$0.305 + 0.008 \cdot SL$	$0.304 + 0.008 \cdot SL$	$0.335 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.532	$0.514 + 0.009 \cdot SL$	$0.525 + 0.006 \cdot SL$	$0.564 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.626	$0.605 + 0.010 \cdot SL$	$0.617 + 0.008 \cdot SL$	$0.664 + 0.005 \cdot SL$
D6 to Y	t <sub>R</sub>	0.245	$0.232 + 0.007 \cdot SL$	$0.228 + 0.007 \cdot SL$	$0.227 + 0.007 \cdot SL$
	t <sub>F</sub>	0.320	$0.304 + 0.008 \cdot SL$	$0.303 + 0.008 \cdot SL$	$0.334 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.528	$0.510 + 0.009 \cdot SL$	$0.522 + 0.006 \cdot SL$	$0.561 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.624	$0.603 + 0.010 \cdot SL$	$0.614 + 0.008 \cdot SL$	$0.661 + 0.005 \cdot SL$
D7 to Y	t <sub>R</sub>	0.245	$0.231 + 0.007 \cdot SL$	$0.228 + 0.007 \cdot SL$	$0.227 + 0.007 \cdot SL$
	t <sub>F</sub>	0.320	$0.304 + 0.008 \cdot SL$	$0.303 + 0.008 \cdot SL$	$0.334 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.528	$0.510 + 0.009 \cdot SL$	$0.522 + 0.006 \cdot SL$	$0.560 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.624	$0.603 + 0.010 \cdot SL$	$0.614 + 0.008 \cdot SL$	$0.661 + 0.005 \cdot SL$
S0 to Y	t <sub>R</sub>	0.246	$0.233 + 0.007 \cdot SL$	$0.230 + 0.007 \cdot SL$	$0.229 + 0.007 \cdot SL$
	t <sub>F</sub>	0.321	$0.305 + 0.008 \cdot SL$	$0.304 + 0.008 \cdot SL$	$0.335 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.728	$0.710 + 0.009 \cdot SL$	$0.721 + 0.006 \cdot SL$	$0.760 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.819	$0.798 + 0.011 \cdot SL$	$0.810 + 0.008 \cdot SL$	$0.856 + 0.005 \cdot SL$
S1 to Y	t <sub>R</sub>	0.244	$0.230 + 0.007 \cdot SL$	$0.227 + 0.007 \cdot SL$	$0.227 + 0.007 \cdot SL$
	t <sub>F</sub>	0.315	$0.299 + 0.008 \cdot SL$	$0.299 + 0.008 \cdot SL$	$0.329 + 0.007 \cdot SL$
	t <sub>PLH</sub>	0.466	$0.448 + 0.009 \cdot SL$	$0.460 + 0.006 \cdot SL$	$0.498 + 0.005 \cdot SL$
	t <sub>PHL</sub>	0.519	$0.498 + 0.011 \cdot SL$	$0.510 + 0.008 \cdot SL$	$0.557 + 0.005 \cdot SL$



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## Input/Output Cells

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4



**Contents**

Overview ..... 4-1

Summary Tables ..... 4-2

Input Buffers ..... 4-8

Output Buffers..... 4-20

Bi-Directional Buffers ..... 4-59

Input Clock Drivers ..... 4-61

Oscillators ..... 4-70

PCI Buffers ..... 4-88

USB (Universal Serial Bus) I/O Buffers ..... 4-93

Power Pads..... 4-104

Analog Interface..... 4-105

Slot Cells ..... 4-113



## OVERVIEW

The fourth chapter describes various kinds of Input/Output cells only (2.5V/ 3.3V/ 5V-tolerant) in STD110 library.

The switching characteristics of each cell are attached to its basic cell information. The AC characteristics of bi-directional buffers are not included in this data sheet. However, they can be derived from different combinations of input and output buffers.

There are so many possible combinations of input/output cells, therefore, the naming conventions are adopted to help you memorize and use this cell library efficiently. You can refer to the naming conventions contained in "Summary Tables" section.

The "Summary Tables" section shows the list of 2.5V, 3.3V and 5V-tolerant I/O cells separated by the category (input, output, bi-directional, etc.), and the more detailed description tables can be found on the leading part of each category.

All 2.5V, 3.3V-interface and 5V-tolerant buffers use 1 I/O slot. The default pitch of a regular I/O buffer is 52  $\mu\text{m}$  (in case of no limitation of bonding equipments). All 2.5V, 3.3V-interface and 5V-tolerant buffers use this regular I/O slot if the data sheet do not state differently.

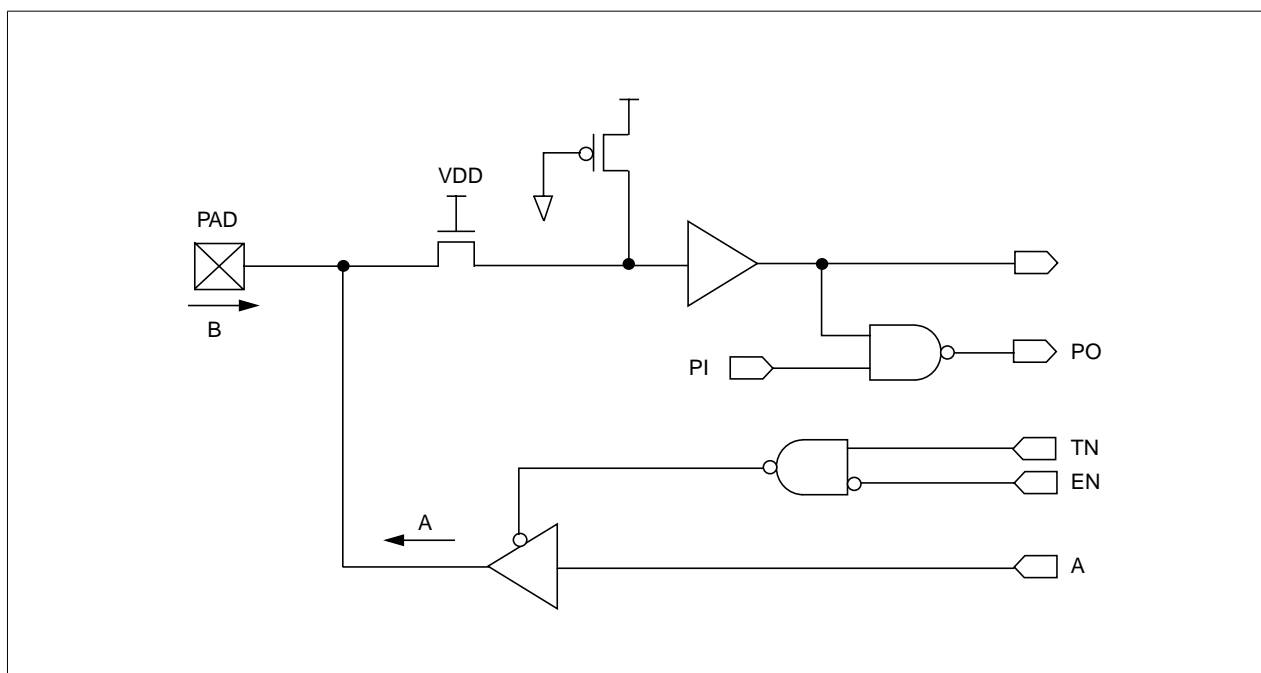


Figure 4-1.

### NOTES:

1. As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.
2. When both A and B driving signals do not exist, SEC tolerant IO's pad voltage goes high state. However, those 5V tolerant input and bi-directional cells with 100k $\Omega$  pull-up resistor have NMOS pass transistor like Figure 4.1. Therefore, pad voltage of 5V tolerant IO for 3.3V interface could be 1.7V instead of VDD.



## SUMMARY TABLES

### Input Buffers

Cell Type	Cell Name	Page
CMOS Level	PIC/PICD/PICU	4-9
	PHIC/PHICD/PHICU	
	PTIC/PTICD/PTICU	
CMOS Schmitt Trigger Level	PIS/PISD/PISU	4-13
	PHIS/PHISD/PHISU	
	PTIS/PTISD/PTISU	
LVTTL Level	PHIT/PHITD/PHITU	4-17
	PTIT/PTITD/PTITU	

#### <Naming Convention of Input Buffers>

Pvlab					
v		a		b	
None	Normal operation	C	CMOS level	None	No resistor
H	3.3V interface	S	Schmitt trigger level	D	Pull-down resistor
T	5V-tolerant	T	LVTTL level	U	Pull-up resistor

### Output Buffers

Cell Type	Cell Name	Current Drive (mA)	Page
Normal	POBy	1/2/4/6/8/10/12	4-21
	POBySM	4/6/8/10/12	
	POBySH	10/12	
	PHOBy	1/2/4/6/8/10/12	
	PHOBySM	4/6/8/10/12	
	PHOBySH	10/12	
Open Drain	PODy	1/2/4/6/8/10/12	4-30
	PODySM	4/6/8/10/12	
	PODySH	10/12	
	PHODy	1/2/4/6/8/10/12	
	PHODySM	4/6/8/10/12	
	PHODySH	10/12	
	PTODy	1/2/3	



Cell Type	Cell Name	Current Drive (mA)	Page
Tri-State	POTy	1/2/4/6/8/10/12	4-40
	POTySM	4/6/8/10/12	
	POTySH	10/12	
	PHOTy	1/2/4/6/8/10/12	
	PHOTySM	4/6/8/10/12	
	PHOTySH	10/12	
	PTOTy	1/2/3	

## &lt;Naming Convention of Output Buffers&gt;

P wO x y z			
w		y	
None	Normal operation	1	1 mA drive
H	3.3V interface	2	2mA drive
x		4	4mA drive
B	Normal buffer	6	6mA drive
D	Open drain buffer	8	8mA drive
T	Tri-state buffer	10	10mA drive
z		12	12mA drive
None	No slew-rate control		
SM	Medium slew-rate control		
SH	High slew-rate control		
P T O x y			
x		y	
D	Open drain buffer	1	1 mA drive
T	Tri-state buffer	2	2mA drive
		3	3mA drive

## NC Pads

Cell Type	Cell Name
NC pad for 2.5V interface	PNC
NC pad for 3.3V interface	PHNC



**Bi-Directional Buffers**

Cell Type	Cell Name	Page
Open Drain	PBaDyz/PBaUDyz	4-60
	PHBaDyz/PHBaUDyz	
	PTBaDyz/PTBaUDyz	
Tri-State	PBaTyz/PBaDTyz/PBaUTyz	
	PHBaTy/PHBaDTy/PHBaUTy	
	PTBaTy/PTBaDTy/PTBaUTy	

**<Naming Convention of Bi-Directional Buffers>**

Pw B a b x y z			
w		y	
None	Normal	1	1 mA drive
H	3.3V interface	2	2mA drive
a		4	4mA drive
C	LVC MOS level	6	6mA drive
S	LVC MOS Schmitt trigger level	8	8mA drive
T	LVTTL level	10	10mA drive
b		12	12mA drive
None	No resistor	z	
D	Pull-down resistor	None	No slew-rate control
U	Pull-up resistor	SM	Medium slew -rate control
x		SH	High slew-rate control
D	Open drain buffer		
T	Tri-state buffer		
PTB a b x y			
a		x	
C	LVC MOS level	D	Open drain buffer
S	LVC MOS Schmitt trigger level	T	Tri-state buffer
T	LVTTL level	y	
b		1	1 mA drive
None	No resistor	2	2mA drive
D	Pull-down resistor	3	3mA drive
U	Pull-up resistor		



**Input Clock Drivers with PAD**

Cell Type	Cell Name	Current Drive (mA)	Page
LVC MOS Level	PSCKDCaby	2/4/6/8	4-62
LVC MOS Schmitt Trigger Level	PSCKDSaby	2/4/6/8	4-66

**<Naming Convention of Input Clock Drivers>**

PSCKD a b y			
a		y	
C	LVC MOS Level	2	2mA drive
S	LVC MOS Schmitt Trigger Level	4	4mA drive
b		6	6mA drive
None	No Resistor	8	8mA drive
D	Pull-Down Resistor		
U	Pull-Up Resistor		

**Oscillators**

Cell Type	Cell Name	Page
Oscillator	PHSOSCK1/K2/M1/M2/M3	4-71
	PHSOSCK17/K27/M16/M26/M36	4-77
	PSOSCK1/K2/M1/M2	4-83

**PCI Buffers**

Cell Type	Cell Name	Page
5V-tolerant PCI Input	PTIPCI	4-90
5V-tolerant PCI Output	PTOPCI	4-91
5V-tolerant PCI Bi-Directional	PTBPCI	4-92

**USB (Universal Serial Bus) I/O Buffers (Under Development)**

Cell Type	Cell Name	Page
Bi-directional USB Buffer	PBUSB/PBUSB1	4-95
	PBOSB_LS	4-96
	PBOSB_FS	4-97



**Power Pads**

Cell Type	Cell Name	Page
2.5V VDD	VDD2(I/P/O/IP/OP/T)	4-104
3.3V VDD	VDD3(P/O/OP)	
VSS	VSS2(I/P/O/IP/OP/T)	
	VSS3(P/O/OP)	
Analog VDD Power Pad	VDD2I_ABB/VDD2OP_ABB/VDD2T_ABB	4-104
Analog VSS Power Pads	VSS2I_ABB/VSS2OP_ABB/VSS2T_ABB	
	VBB_ABB/VSSBB_ABB	

**Analog Interface**

Cell Type	Cell Name	Page
Analog Input with Separated Bulk-Bias	PNC_ABB PIA_ABB/PIAR10_ABB/PIAR50_ABB PIC_ABB/PICC_ABB/PICEN_ABB	4-106
Analog Output with Separated Bulk-Bias	POA_ABB/POAR10_ABB/POAR50_ABB POT(1/2/4/8)_ABB	4-109
Analog Bi-Directional with Separated Bulk-Bias	PBCT(1/2/4/8)_ABB	4-109

**NOTE:** As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.

**Slot Cells**

Cell Type	Cell Name	Page
ESD Slot Cells	EV2I/EV2P/EV2O/EV2IP/EV2OP/EV2T	4-112
	EV3P/EV3O/EV3OP	
	EV2I_ABB/EV2OP_ABB/EV2T/ABB	
Common Slot Cells	EC0C0/EC0C0D	4-113
	EC0CA0/EC0CA0D	
Analog Output with Separated Bulk-Bias	EC0C0_BB/EC0C0D_BB/ EC0C0_VBB/EC0C0D_VBB	4-113



NOTE



## INPUT BUFFERS

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### Cell List

Cell Name	Function Description
PIC/PICD/PICU	2.5V LVCMOS Level Input Buffers
PHIC/PHICD/PHICU	3.3V LVCMOS Level Input Buffers
PTIC/PTICD/PTICU	5V-tolerant LVCMOS Level Input Buffers
PIS/PISD/PISU	2.5V LVCMOS Schmitt Trigger Level Input Buffers
PHIS/PHISD/PHISU	3.3V LVCMOS Schmitt Trigger Level Input Buffers
PTIS/PTISD/PTISU	5V-tolerant LVCMOS Schmitt Trigger Level Input Buffers
PHIT/PHITD/PHITU	3.3V LVTTL Level Input Buffers
PTIT/PTITD/PTITU	5V-tolerant LVTTL Level Input Buffers



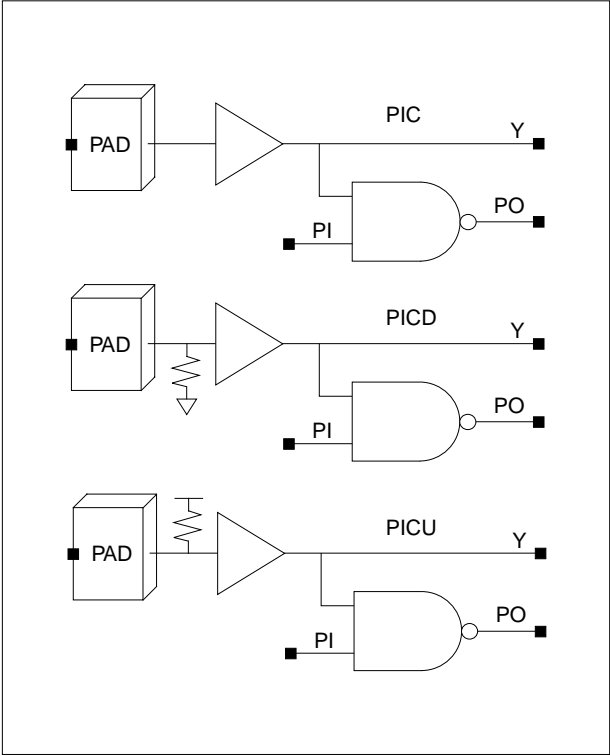
# PvIC/PvICD/PvICU

## LVC MOS Level Input Buffers

### Cell Availability

2.5V Only	3.3V Interface	5V Tolerant
PIC/PICD/PICU	PHIC/PHICD/PHICU	PTIC/PTICD/PTICU

### Logic Symbol



### Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

### Standard Load (SL)

Cell Name	PI
PIC/PICD/PICU	2.897
PHIC/PHICD/PHICU	2.897
PTIC/PTICD/PTICU	2.897



## PvIC/PvICD/PvICU

### LVC MOS Level Input Buffers

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

##### PIC

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.204	$0.186 + 0.009 \cdot \text{SL}$	$0.184 + 0.010 \cdot \text{SL}$	$0.165 + 0.010 \cdot \text{SL}$
	$t_F$	0.151	$0.138 + 0.006 \cdot \text{SL}$	$0.141 + 0.006 \cdot \text{SL}$	$0.128 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.629	$0.615 + 0.007 \cdot \text{SL}$	$0.621 + 0.005 \cdot \text{SL}$	$0.637 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.547	$0.535 + 0.006 \cdot \text{SL}$	$0.542 + 0.004 \cdot \text{SL}$	$0.571 + 0.003 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PICD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.204	$0.186 + 0.009 \cdot \text{SL}$	$0.183 + 0.010 \cdot \text{SL}$	$0.165 + 0.010 \cdot \text{SL}$
	$t_F$	0.153	$0.141 + 0.006 \cdot \text{SL}$	$0.143 + 0.006 \cdot \text{SL}$	$0.131 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.684	$0.669 + 0.007 \cdot \text{SL}$	$0.675 + 0.005 \cdot \text{SL}$	$0.692 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.518	$0.506 + 0.006 \cdot \text{SL}$	$0.512 + 0.004 \cdot \text{SL}$	$0.542 + 0.003 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PICU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.206	$0.188 + 0.009 \cdot \text{SL}$	$0.186 + 0.010 \cdot \text{SL}$	$0.166 + 0.010 \cdot \text{SL}$
	$t_F$	0.151	$0.139 + 0.006 \cdot \text{SL}$	$0.140 + 0.006 \cdot \text{SL}$	$0.128 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.588	$0.574 + 0.007 \cdot \text{SL}$	$0.580 + 0.005 \cdot \text{SL}$	$0.597 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.603	$0.591 + 0.006 \cdot \text{SL}$	$0.598 + 0.004 \cdot \text{SL}$	$0.627 + 0.003 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

**NOTE:** The delay measure point of LVC MOS input buffer is from PAD(VDD/2) to Y(VDD/2).



# PvIC/PvICD/PvICU

## LVC MOS Level Input Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

#### PHIC

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.124 + 0.005 \cdot \text{SL}$	$0.124 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.770	$0.763 + 0.003 \cdot \text{SL}$	$0.765 + 0.003 \cdot \text{SL}$	$0.775 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.893	$0.885 + 0.004 \cdot \text{SL}$	$0.888 + 0.003 \cdot \text{SL}$	$0.913 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

#### PHICD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.123 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.004 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.847	$0.840 + 0.003 \cdot \text{SL}$	$0.842 + 0.003 \cdot \text{SL}$	$0.853 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.856	$0.849 + 0.004 \cdot \text{SL}$	$0.852 + 0.003 \cdot \text{SL}$	$0.877 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

#### PHICU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.124 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.129 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.714	$0.708 + 0.003 \cdot \text{SL}$	$0.710 + 0.003 \cdot \text{SL}$	$0.720 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.968	$0.960 + 0.004 \cdot \text{SL}$	$0.964 + 0.003 \cdot \text{SL}$	$0.989 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

**NOTE:** The delay measure point of LVC MOS input buffer is from PAD(VDD/2) to Y(VDD/2).



## PvIC/PvICD/PvICU

### LVCMOS Level Input Buffers

#### Switching Characteristics (Typical process, 25°C, 2.5V, 3.3V, $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

##### PTIC

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.134	$0.124 + 0.005 \cdot \text{SL}$	$0.124 + 0.005 \cdot \text{SL}$	$0.118 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.129 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.920	$0.913 + 0.003 \cdot \text{SL}$	$0.916 + 0.003 \cdot \text{SL}$	$0.926 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.274	$1.266 + 0.004 \cdot \text{SL}$	$1.270 + 0.003 \cdot \text{SL}$	$1.294 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PTICD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.134	$0.124 + 0.005 \cdot \text{SL}$	$0.124 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	1.002	$0.995 + 0.003 \cdot \text{SL}$	$0.997 + 0.003 \cdot \text{SL}$	$1.008 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.239	$1.231 + 0.004 \cdot \text{SL}$	$1.234 + 0.003 \cdot \text{SL}$	$1.259 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PTICU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.134	$0.124 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.118 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.004 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.136 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.767	$0.760 + 0.003 \cdot \text{SL}$	$0.762 + 0.003 \cdot \text{SL}$	$0.772 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.469	$1.461 + 0.004 \cdot \text{SL}$	$1.464 + 0.003 \cdot \text{SL}$	$1.489 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

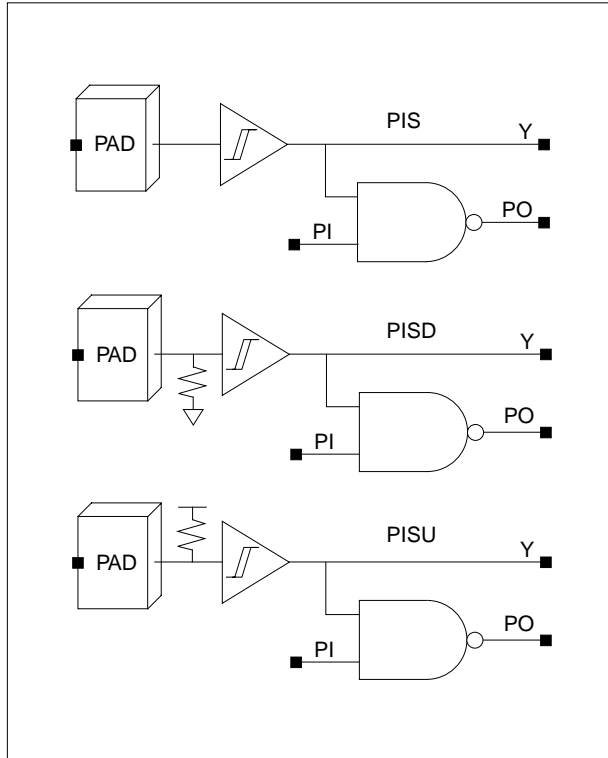
**NOTE:** The delay measure point of LVCMOS input buffer is from PAD(VDD/2) to Y(VDD/2).



### Cell Availability

2.5V Only	3.3V Interface	5V Tolerant
PIS/PISD/PISU	PHIS/PHISD/PHISU	PTIS/PTISD/PTISU

### Logic Symbol



### Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

### Standard Load (SL)

Cell Name	PI
PIS/PISD/PISU	2.897
PHIS/PHISD/PHISU	2.897
PTIS/PTISD/PTISU	2.897



## PvIS/PvISD/PvISU

### LVC MOS Schmitt Trigger Level Input Buffers

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

##### PIS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.225	$0.203 + 0.011 \cdot \text{SL}$	$0.206 + 0.010 \cdot \text{SL}$	$0.199 + 0.010 \cdot \text{SL}$
	$t_F$	0.165	$0.150 + 0.008 \cdot \text{SL}$	$0.155 + 0.006 \cdot \text{SL}$	$0.173 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.992	$0.976 + 0.008 \cdot \text{SL}$	$0.983 + 0.006 \cdot \text{SL}$	$1.019 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.935	$0.921 + 0.007 \cdot \text{SL}$	$0.928 + 0.005 \cdot \text{SL}$	$0.973 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PISD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.224	$0.203 + 0.011 \cdot \text{SL}$	$0.206 + 0.010 \cdot \text{SL}$	$0.198 + 0.010 \cdot \text{SL}$
	$t_F$	0.167	$0.152 + 0.007 \cdot \text{SL}$	$0.156 + 0.006 \cdot \text{SL}$	$0.174 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	1.045	$1.029 + 0.008 \cdot \text{SL}$	$1.036 + 0.006 \cdot \text{SL}$	$1.072 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.921	$0.908 + 0.007 \cdot \text{SL}$	$0.914 + 0.005 \cdot \text{SL}$	$0.960 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PISU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.226	$0.205 + 0.011 \cdot \text{SL}$	$0.208 + 0.010 \cdot \text{SL}$	$0.201 + 0.010 \cdot \text{SL}$
	$t_F$	0.165	$0.150 + 0.008 \cdot \text{SL}$	$0.155 + 0.006 \cdot \text{SL}$	$0.173 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.961	$0.944 + 0.008 \cdot \text{SL}$	$0.952 + 0.006 \cdot \text{SL}$	$0.989 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.991	$0.978 + 0.007 \cdot \text{SL}$	$0.985 + 0.005 \cdot \text{SL}$	$1.029 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



## LVCMOS Schmitt Trigger Level Input Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)**PHIS**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.123 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.998	$0.992 + 0.003 \cdot \text{SL}$	$0.994 + 0.003 \cdot \text{SL}$	$1.004 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.339	$1.331 + 0.004 \cdot \text{SL}$	$1.334 + 0.003 \cdot \text{SL}$	$1.359 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$ **PHISD**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.123 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.004 \cdot \text{SL}$	$0.131 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	1.076	$1.069 + 0.003 \cdot \text{SL}$	$1.071 + 0.003 \cdot \text{SL}$	$1.081 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.337	$1.329 + 0.004 \cdot \text{SL}$	$1.332 + 0.003 \cdot \text{SL}$	$1.357 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$ **PHISU**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.123 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.129 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.136 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.944	$0.937 + 0.003 \cdot \text{SL}$	$0.939 + 0.003 \cdot \text{SL}$	$0.949 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.416	$1.408 + 0.004 \cdot \text{SL}$	$1.412 + 0.003 \cdot \text{SL}$	$1.437 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



## PvIS/PvISD/PvISU

### LVC MOS Schmitt Trigger Level Input Buffers

#### Switching Characteristics (Typical process, 25°C, 2.5V, 3.3V, $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

##### PTIS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.136	$0.126 + 0.005 \cdot \text{SL}$	$0.126 + 0.005 \cdot \text{SL}$	$0.119 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.004 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	1.164	$1.158 + 0.003 \cdot \text{SL}$	$1.160 + 0.003 \cdot \text{SL}$	$1.170 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.387	$1.379 + 0.004 \cdot \text{SL}$	$1.382 + 0.003 \cdot \text{SL}$	$1.407 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PTISD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.136	$0.127 + 0.005 \cdot \text{SL}$	$0.126 + 0.005 \cdot \text{SL}$	$0.119 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.129 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	1.248	$1.241 + 0.003 \cdot \text{SL}$	$1.243 + 0.003 \cdot \text{SL}$	$1.253 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.374	$1.366 + 0.004 \cdot \text{SL}$	$1.370 + 0.003 \cdot \text{SL}$	$1.394 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PTISU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.136	$0.126 + 0.005 \cdot \text{SL}$	$0.126 + 0.005 \cdot \text{SL}$	$0.119 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.129 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	1.017	$1.010 + 0.003 \cdot \text{SL}$	$1.013 + 0.003 \cdot \text{SL}$	$1.023 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.536	$1.528 + 0.004 \cdot \text{SL}$	$1.532 + 0.003 \cdot \text{SL}$	$1.557 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

**NOTE:** The delay measure point of LVC MOS input buffer is from PAD(VDD/2) to Y(VDD/2).



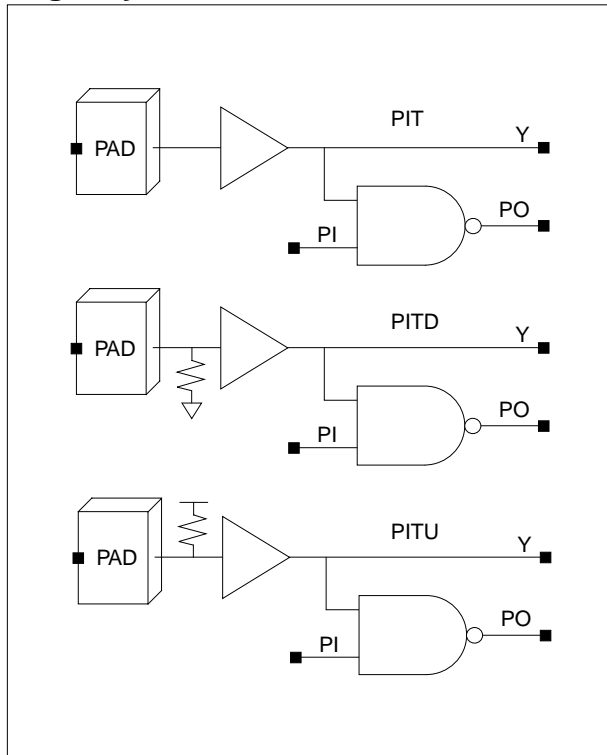
# PvIT/PvITD/PvITU

## LVTTL Level Input Buffers

### Cell Availability

3.3V Interface	5V Tolerant
PHIT/PHITD/PHITU	PTIT/PTITD/PTITU

### Logic Symbol



### Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

### Standard Load (SL)

Cell Name	PI
PHIT/PHITD/PHITU	2.897
PTIT/PTITD/PTITU	2.897



## PvIT/PvITD/PvITU

### LVTTL Level Input Buffers

#### Switching Characteristics (Typical process, 25°C, 2.5V, 3.3V, $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

##### PHIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.123 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.665	$0.658 + 0.003 \cdot \text{SL}$	$0.660 + 0.003 \cdot \text{SL}$	$0.670 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.930	$0.922 + 0.004 \cdot \text{SL}$	$0.925 + 0.003 \cdot \text{SL}$	$0.950 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PHITD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.124 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.004 \cdot \text{SL}$	$0.131 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.750	$0.743 + 0.003 \cdot \text{SL}$	$0.746 + 0.003 \cdot \text{SL}$	$0.756 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.905	$0.897 + 0.004 \cdot \text{SL}$	$0.900 + 0.003 \cdot \text{SL}$	$0.925 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

##### PHITU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.123 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.129 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.601	$0.594 + 0.003 \cdot \text{SL}$	$0.596 + 0.003 \cdot \text{SL}$	$0.606 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.006	$0.998 + 0.004 \cdot \text{SL}$	$1.001 + 0.003 \cdot \text{SL}$	$1.026 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

**NOTE:** The delay measure point of LVTTL input buffer is from PAD(1.4) to Y(VDD/2).



# PvIT/PvITD/PvITU

## LVTTL Level Input Buffers

### Switching Characteristics (Typical process, 25°C, 2.5V, 3.3V, $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

#### PTIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.123 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.751	$0.744 + 0.003 \cdot \text{SL}$	$0.746 + 0.003 \cdot \text{SL}$	$0.757 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.194	$1.186 + 0.004 \cdot \text{SL}$	$1.190 + 0.003 \cdot \text{SL}$	$1.215 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

#### PTITD

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.123 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.129 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.899	$0.892 + 0.003 \cdot \text{SL}$	$0.895 + 0.003 \cdot \text{SL}$	$0.905 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.194	$1.186 + 0.004 \cdot \text{SL}$	$1.189 + 0.003 \cdot \text{SL}$	$1.214 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$

#### PTITU

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.133	$0.124 + 0.005 \cdot \text{SL}$	$0.123 + 0.005 \cdot \text{SL}$	$0.117 + 0.005 \cdot \text{SL}$
	$t_F$	0.139	$0.130 + 0.005 \cdot \text{SL}$	$0.132 + 0.004 \cdot \text{SL}$	$0.137 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.653	$0.646 + 0.003 \cdot \text{SL}$	$0.648 + 0.003 \cdot \text{SL}$	$0.658 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.438	$1.430 + 0.004 \cdot \text{SL}$	$1.433 + 0.003 \cdot \text{SL}$	$1.458 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



## OUTPUT BUFFERS

### Cell List

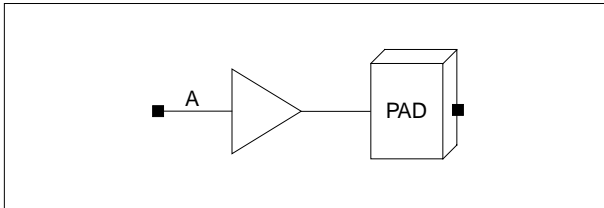
Cell Name	Function Description
POB(1/2/4/6/8/10/12)	2.5V LVCMOS Normal Output Buffers
POB(4/6/8/10/12)SM	2.5V LVCMOS Normal Output Buffers with Medium Slew-Rate
POB(10/12)SH	2.5V LVCMOS Normal Output Buffers with High Slew-Rate
PHOB(1/2/4/6/8/10/12)	3.3V LVCMOS Normal Output Buffers
PHOB(4/6/8/10/12)SM	3.3V LVCMOS Normal Output Buffers with Medium Slew-Rate
PHOB(10/12)SH	3.3V LVCMOS Normal Output Buffers with High Slew-Rate
POD(1/2/4/6/8/10/12)	2.5V LVCMOS Open Drain Output Buffers
POD(4/6/8/10/12)SM	2.5V LVCMOS Open Drain Output Buffers with Medium Slew-Rate
POD(10/12)SH	2.5V LVCMOS Open Drain Output Buffers with High Slew-Rate
PHOD(1/2/4/6/8/10/12)	3.3V LVCMOS Open Drain Output Buffers
PHOD(4/6/8/10/12)SM	3.3V LVCMOS Open Drain Output Buffers with Medium Slew-Rate
PHOD(10/12)SH	3.3V LVCMOS Open Drain Output Buffers with High Slew-Rate
PTOD(1/2/3)	5V Tolerant Open Drain Output Buffers
POT(1/2/4/6/8/10/12)	2.5V LVCMOS Tri-State Output Buffers
POT(4/6/8/10/12)SM	2.5V LVCMOS Tri-State Output Buffers with Medium Slew-Rate
POT(10/12)SH	2.5V LVCMOS Tri-State Output Buffers with High Slew-Rate
PHOT(1/2/4/6/8/10/12)	3.3V LVCMOS Tri-State Output Buffers
PHOT(4/6/8/10/12)SM	3.3V LVCMOS Tri-State Output Buffers with Medium Slew-Rate
PHOT(10/12)SH	3.3V LVCMOS Tri-State Output Buffers with High Slew-Rate
PTOT(1/2/3)	5V Tolerant Tri-State Output Buffers



### Cell Availability

Only 2.5V	3.3V Interface
POB(1/2/4/6/8/10/12) POB(4/6/8/10/12)SM POB(10/12)SH	PHOB(1/2/4/6/8/10/12) PHOB(4/6/8/10/12)SM PHOB(10/12)SH

### Logic Symbol



### Truth Table

A	PAD
0	0
1	1

### Standard Load (SL)

Cell Name	A
POB(1/2/4/6/8)	9.801
POB(8/10/12)SM	16.532
POB(10/12)	19.614
POB(10/12)SH	25.576
PHOB(1/2/4/6/8/10/12)	5.444
PHOB(4/6/8/10/12)SM	5.444
PHOB(10/12)SH	5.444



# PvOByz

## Normal Output Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### POB1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	31.508	$1.210 + 0.606 \cdot \text{CL}$	$1.212 + 0.606 \cdot \text{CL}$	$1.209 + 0.606 \cdot \text{CL}$
	$t_F$	33.275	$1.275 + 0.640 \cdot \text{CL}$	$1.279 + 0.640 \cdot \text{CL}$	$1.276 + 0.640 \cdot \text{CL}$
	$t_{PLH}$	15.295	$0.789 + 0.290 \cdot \text{CL}$	$0.787 + 0.290 \cdot \text{CL}$	$0.790 + 0.290 \cdot \text{CL}$
	$t_{PHL}$	17.054	$0.944 + 0.322 \cdot \text{CL}$	$0.946 + 0.322 \cdot \text{CL}$	$0.946 + 0.322 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POB2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	15.772	$0.624 + 0.303 \cdot \text{CL}$	$0.622 + 0.303 \cdot \text{CL}$	$0.625 + 0.303 \cdot \text{CL}$
	$t_F$	18.210	$0.685 + 0.351 \cdot \text{CL}$	$0.688 + 0.350 \cdot \text{CL}$	$0.685 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	7.843	$0.590 + 0.145 \cdot \text{CL}$	$0.590 + 0.145 \cdot \text{CL}$	$0.589 + 0.145 \cdot \text{CL}$
	$t_{PHL}$	9.699	$0.580 + 0.182 \cdot \text{CL}$	$0.580 + 0.182 \cdot \text{CL}$	$0.578 + 0.182 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POB4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	7.917	$0.348 + 0.151 \cdot \text{CL}$	$0.342 + 0.151 \cdot \text{CL}$	$0.343 + 0.151 \cdot \text{CL}$
	$t_F$	9.121	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	4.271	$0.643 + 0.073 \cdot \text{CL}$	$0.644 + 0.073 \cdot \text{CL}$	$0.644 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	5.026	$0.468 + 0.091 \cdot \text{CL}$	$0.467 + 0.091 \cdot \text{CL}$	$0.466 + 0.091 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POB6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.317	$0.308 + 0.100 \cdot \text{CL}$	$0.280 + 0.101 \cdot \text{CL}$	$0.265 + 0.101 \cdot \text{CL}$
	$t_F$	6.097	$0.261 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$
	$t_{PLH}$	3.204	$0.785 + 0.048 \cdot \text{CL}$	$0.786 + 0.048 \cdot \text{CL}$	$0.786 + 0.048 \cdot \text{CL}$
	$t_{PHL}$	3.520	$0.487 + 0.061 \cdot \text{CL}$	$0.483 + 0.061 \cdot \text{CL}$	$0.481 + 0.061 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**POB8**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.293	$0.230 + 0.101 \cdot \text{CL}$	$0.228 + 0.101 \cdot \text{CL}$	$0.228 + 0.101 \cdot \text{CL}$
	$t_F$	4.572	$0.205 + 0.087 \cdot \text{CL}$	$0.202 + 0.087 \cdot \text{CL}$	$0.201 + 0.087 \cdot \text{CL}$
	$t_{PLH}$	3.470	$1.129 + 0.047 \cdot \text{CL}$	$1.128 + 0.047 \cdot \text{CL}$	$1.127 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	3.069	$0.845 + 0.044 \cdot \text{CL}$	$0.845 + 0.044 \cdot \text{CL}$	$0.845 + 0.044 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POB10**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	3.217	$0.236 + 0.060 \cdot \text{CL}$	$0.207 + 0.060 \cdot \text{CL}$	$0.189 + 0.060 \cdot \text{CL}$
	$t_F$	3.668	$0.174 + 0.070 \cdot \text{CL}$	$0.166 + 0.070 \cdot \text{CL}$	$0.163 + 0.070 \cdot \text{CL}$
	$t_{PLH}$	2.107	$0.654 + 0.029 \cdot \text{CL}$	$0.656 + 0.029 \cdot \text{CL}$	$0.656 + 0.029 \cdot \text{CL}$
	$t_{PHL}$	2.218	$0.401 + 0.036 \cdot \text{CL}$	$0.397 + 0.036 \cdot \text{CL}$	$0.395 + 0.036 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POB12**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	2.719	$0.264 + 0.049 \cdot \text{CL}$	$0.229 + 0.050 \cdot \text{CL}$	$0.202 + 0.050 \cdot \text{CL}$
	$t_F$	3.069	$0.166 + 0.058 \cdot \text{CL}$	$0.154 + 0.058 \cdot \text{CL}$	$0.148 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	1.950	$0.734 + 0.024 \cdot \text{CL}$	$0.739 + 0.024 \cdot \text{CL}$	$0.740 + 0.024 \cdot \text{CL}$
	$t_{PHL}$	1.942	$0.433 + 0.030 \cdot \text{CL}$	$0.427 + 0.030 \cdot \text{CL}$	$0.424 + 0.030 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOByz

## Normal Output Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### POB4SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	8.135	$0.752 + 0.148 \cdot \text{CL}$	$0.660 + 0.149 \cdot \text{CL}$	$0.586 + 0.150 \cdot \text{CL}$
	$t_F$	9.483	$1.001 + 0.170 \cdot \text{CL}$	$0.889 + 0.172 \cdot \text{CL}$	$0.787 + 0.173 \cdot \text{CL}$
	$t_{PLH}$	5.457	$1.802 + 0.073 \cdot \text{CL}$	$1.823 + 0.073 \cdot \text{CL}$	$1.829 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	6.998	$2.362 + 0.093 \cdot \text{CL}$	$2.422 + 0.092 \cdot \text{CL}$	$2.439 + 0.091 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POB6SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	6.045	$1.305 + 0.095 \cdot \text{CL}$	$1.245 + 0.096 \cdot \text{CL}$	$1.147 + 0.097 \cdot \text{CL}$
	$t_F$	6.980	$1.447 + 0.111 \cdot \text{CL}$	$1.410 + 0.111 \cdot \text{CL}$	$1.318 + 0.113 \cdot \text{CL}$
	$t_{PLH}$	5.100	$2.394 + 0.054 \cdot \text{CL}$	$2.575 + 0.051 \cdot \text{CL}$	$2.676 + 0.049 \cdot \text{CL}$
	$t_{PHL}$	6.308	$2.898 + 0.068 \cdot \text{CL}$	$3.119 + 0.064 \cdot \text{CL}$	$3.254 + 0.062 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POB8SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.152	$1.648 + 0.070 \cdot \text{CL}$	$1.663 + 0.070 \cdot \text{CL}$	$1.594 + 0.071 \cdot \text{CL}$
	$t_F$	5.708	$1.557 + 0.083 \cdot \text{CL}$	$1.595 + 0.082 \cdot \text{CL}$	$1.543 + 0.083 \cdot \text{CL}$
	$t_{PLH}$	4.762	$2.427 + 0.047 \cdot \text{CL}$	$2.708 + 0.041 \cdot \text{CL}$	$2.900 + 0.039 \cdot \text{CL}$
	$t_{PHL}$	5.616	$2.839 + 0.056 \cdot \text{CL}$	$3.103 + 0.050 \cdot \text{CL}$	$3.289 + 0.048 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POB10SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.204	$1.322 + 0.058 \cdot \text{CL}$	$1.361 + 0.057 \cdot \text{CL}$	$1.342 + 0.057 \cdot \text{CL}$
	$t_F$	4.729	$1.356 + 0.067 \cdot \text{CL}$	$1.416 + 0.066 \cdot \text{CL}$	$1.403 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	4.405	$2.495 + 0.038 \cdot \text{CL}$	$2.718 + 0.034 \cdot \text{CL}$	$2.886 + 0.032 \cdot \text{CL}$
	$t_{PHL}$	5.175	$2.861 + 0.046 \cdot \text{CL}$	$3.101 + 0.041 \cdot \text{CL}$	$3.281 + 0.039 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**POB12SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.190	$1.629 + 0.051 \cdot \text{CL}$	$1.774 + 0.048 \cdot \text{CL}$	$1.847 + 0.047 \cdot \text{CL}$
	$t_F$	4.546	$1.542 + 0.060 \cdot \text{CL}$	$1.723 + 0.056 \cdot \text{CL}$	$1.811 + 0.055 \cdot \text{CL}$
	$t_{PLH}$	4.640	$2.688 + 0.039 \cdot \text{CL}$	$2.990 + 0.033 \cdot \text{CL}$	$3.244 + 0.030 \cdot \text{CL}$
	$t_{PHL}$	5.372	$3.145 + 0.045 \cdot \text{CL}$	$3.432 + 0.039 \cdot \text{CL}$	$3.677 + 0.036 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POB10SH**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	6.202	$2.922 + 0.066 \cdot \text{CL}$	$3.205 + 0.060 \cdot \text{CL}$	$3.394 + 0.057 \cdot \text{CL}$
	$t_F$	6.442	$2.722 + 0.074 \cdot \text{CL}$	$2.995 + 0.069 \cdot \text{CL}$	$3.168 + 0.067 \cdot \text{CL}$
	$t_{PLH}$	7.316	$4.395 + 0.058 \cdot \text{CL}$	$4.943 + 0.047 \cdot \text{CL}$	$5.408 + 0.041 \cdot \text{CL}$
	$t_{PHL}$	7.953	$4.743 + 0.064 \cdot \text{CL}$	$5.265 + 0.054 \cdot \text{CL}$	$5.711 + 0.048 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POB12SH**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	6.575	$3.532 + 0.061 \cdot \text{CL}$	$3.914 + 0.053 \cdot \text{CL}$	$4.189 + 0.050 \cdot \text{CL}$
	$t_F$	6.532	$3.087 + 0.069 \cdot \text{CL}$	$3.482 + 0.061 \cdot \text{CL}$	$3.754 + 0.057 \cdot \text{CL}$
	$t_{PLH}$	7.825	$4.698 + 0.063 \cdot \text{CL}$	$5.373 + 0.049 \cdot \text{CL}$	$5.946 + 0.041 \cdot \text{CL}$
	$t_{PHL}$	8.410	$5.170 + 0.065 \cdot \text{CL}$	$5.765 + 0.053 \cdot \text{CL}$	$6.283 + 0.046 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOByz

## Normal Output Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

### PHOB1

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	42.148	$1.623 + 0.811 \cdot \text{CL}$	$1.624 + 0.810 \cdot \text{CL}$	$1.621 + 0.811 \cdot \text{CL}$
	$t_F$	33.014	$1.269 + 0.635 \cdot \text{CL}$	$1.270 + 0.635 \cdot \text{CL}$	$1.267 + 0.635 \cdot \text{CL}$
	$t_{PLH}$	20.150	$1.403 + 0.375 \cdot \text{CL}$	$1.404 + 0.375 \cdot \text{CL}$	$1.401 + 0.375 \cdot \text{CL}$
	$t_{PHL}$	16.887	$1.325 + 0.311 \cdot \text{CL}$	$1.321 + 0.311 \cdot \text{CL}$	$1.324 + 0.311 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOB2

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	21.098	$0.836 + 0.405 \cdot \text{CL}$	$0.836 + 0.405 \cdot \text{CL}$	$0.833 + 0.405 \cdot \text{CL}$
	$t_F$	18.188	$0.706 + 0.350 \cdot \text{CL}$	$0.702 + 0.350 \cdot \text{CL}$	$0.705 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	10.450	$1.078 + 0.187 \cdot \text{CL}$	$1.076 + 0.187 \cdot \text{CL}$	$1.076 + 0.187 \cdot \text{CL}$
	$t_{PHL}$	9.844	$0.948 + 0.178 \cdot \text{CL}$	$0.949 + 0.178 \cdot \text{CL}$	$0.947 + 0.178 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOB4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	10.563	$0.433 + 0.203 \cdot \text{CL}$	$0.431 + 0.203 \cdot \text{CL}$	$0.431 + 0.203 \cdot \text{CL}$
	$t_F$	9.114	$0.371 + 0.175 \cdot \text{CL}$	$0.371 + 0.175 \cdot \text{CL}$	$0.372 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	5.676	$0.991 + 0.094 \cdot \text{CL}$	$0.990 + 0.094 \cdot \text{CL}$	$0.990 + 0.094 \cdot \text{CL}$
	$t_{PHL}$	5.280	$0.832 + 0.089 \cdot \text{CL}$	$0.832 + 0.089 \cdot \text{CL}$	$0.833 + 0.089 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOB6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	7.047	$0.294 + 0.135 \cdot \text{CL}$	$0.294 + 0.135 \cdot \text{CL}$	$0.293 + 0.135 \cdot \text{CL}$
	$t_F$	6.082	$0.254 + 0.117 \cdot \text{CL}$	$0.254 + 0.117 \cdot \text{CL}$	$0.255 + 0.117 \cdot \text{CL}$
	$t_{PLH}$	4.232	$1.109 + 0.062 \cdot \text{CL}$	$1.108 + 0.062 \cdot \text{CL}$	$1.108 + 0.062 \cdot \text{CL}$
	$t_{PHL}$	3.804	$0.839 + 0.059 \cdot \text{CL}$	$0.839 + 0.059 \cdot \text{CL}$	$0.840 + 0.059 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PHOB8**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.293	$0.230 + 0.101 \cdot \text{CL}$	$0.228 + 0.101 \cdot \text{CL}$	$0.228 + 0.101 \cdot \text{CL}$
	$t_F$	4.572	$0.205 + 0.087 \cdot \text{CL}$	$0.202 + 0.087 \cdot \text{CL}$	$0.201 + 0.087 \cdot \text{CL}$
	$t_{PLH}$	3.470	$1.129 + 0.047 \cdot \text{CL}$	$1.128 + 0.047 \cdot \text{CL}$	$1.127 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	3.069	$0.845 + 0.044 \cdot \text{CL}$	$0.845 + 0.044 \cdot \text{CL}$	$0.845 + 0.044 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOB10**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.243	$0.197 + 0.081 \cdot \text{CL}$	$0.191 + 0.081 \cdot \text{CL}$	$0.190 + 0.081 \cdot \text{CL}$
	$t_F$	3.669	$0.183 + 0.070 \cdot \text{CL}$	$0.174 + 0.070 \cdot \text{CL}$	$0.172 + 0.070 \cdot \text{CL}$
	$t_{PLH}$	3.030	$1.160 + 0.037 \cdot \text{CL}$	$1.157 + 0.037 \cdot \text{CL}$	$1.156 + 0.037 \cdot \text{CL}$
	$t_{PHL}$	2.643	$0.863 + 0.036 \cdot \text{CL}$	$0.863 + 0.036 \cdot \text{CL}$	$0.863 + 0.036 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOB12**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	3.544	$0.181 + 0.067 \cdot \text{CL}$	$0.170 + 0.067 \cdot \text{CL}$	$0.167 + 0.068 \cdot \text{CL}$
	$t_F$	3.070	$0.176 + 0.058 \cdot \text{CL}$	$0.162 + 0.058 \cdot \text{CL}$	$0.156 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	2.751	$1.197 + 0.031 \cdot \text{CL}$	$1.193 + 0.031 \cdot \text{CL}$	$1.190 + 0.031 \cdot \text{CL}$
	$t_{PHL}$	2.370	$0.887 + 0.030 \cdot \text{CL}$	$0.887 + 0.030 \cdot \text{CL}$	$0.887 + 0.030 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOByz

## Normal Output Buffers

**Switching Characteristics** (Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

### PHOB4SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	10.608	$0.517 + 0.202 \cdot \text{CL}$	$0.486 + 0.202 \cdot \text{CL}$	$0.477 + 0.203 \cdot \text{CL}$
	$t_F$	9.435	$0.947 + 0.170 \cdot \text{CL}$	$0.842 + 0.172 \cdot \text{CL}$	$0.750 + 0.173 \cdot \text{CL}$
	$t_{PLH}$	6.404	$1.715 + 0.094 \cdot \text{CL}$	$1.716 + 0.094 \cdot \text{CL}$	$1.718 + 0.094 \cdot \text{CL}$
	$t_{PHL}$	7.039	$2.530 + 0.090 \cdot \text{CL}$	$2.579 + 0.089 \cdot \text{CL}$	$2.594 + 0.089 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOB6SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	7.211	$0.618 + 0.132 \cdot \text{CL}$	$0.540 + 0.133 \cdot \text{CL}$	$0.478 + 0.134 \cdot \text{CL}$
	$t_F$	6.910	$1.355 + 0.111 \cdot \text{CL}$	$1.328 + 0.112 \cdot \text{CL}$	$1.248 + 0.113 \cdot \text{CL}$
	$t_{PLH}$	5.165	$2.022 + 0.063 \cdot \text{CL}$	$2.037 + 0.063 \cdot \text{CL}$	$2.041 + 0.063 \cdot \text{CL}$
	$t_{PHL}$	6.311	$3.000 + 0.066 \cdot \text{CL}$	$3.208 + 0.062 \cdot \text{CL}$	$3.333 + 0.060 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOB8SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.691	$0.888 + 0.096 \cdot \text{CL}$	$0.802 + 0.098 \cdot \text{CL}$	$0.711 + 0.099 \cdot \text{CL}$
	$t_F$	6.059	$1.788 + 0.085 \cdot \text{CL}$	$1.905 + 0.083 \cdot \text{CL}$	$1.926 + 0.083 \cdot \text{CL}$
	$t_{PLH}$	4.807	$2.352 + 0.049 \cdot \text{CL}$	$2.434 + 0.047 \cdot \text{CL}$	$2.466 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	6.336	$3.367 + 0.059 \cdot \text{CL}$	$3.714 + 0.052 \cdot \text{CL}$	$3.984 + 0.049 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOB10SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.501	$0.614 + 0.078 \cdot \text{CL}$	$0.553 + 0.079 \cdot \text{CL}$	$0.502 + 0.080 \cdot \text{CL}$
	$t_F$	5.283	$1.821 + 0.069 \cdot \text{CL}$	$1.971 + 0.066 \cdot \text{CL}$	$2.023 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	4.008	$2.093 + 0.038 \cdot \text{CL}$	$2.129 + 0.038 \cdot \text{CL}$	$2.140 + 0.037 \cdot \text{CL}$
	$t_{PHL}$	5.781	$3.176 + 0.052 \cdot \text{CL}$	$3.541 + 0.045 \cdot \text{CL}$	$3.833 + 0.041 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PHOB12SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.002	$0.794 + 0.064 \cdot \text{CL}$	$0.770 + 0.065 \cdot \text{CL}$	$0.723 + 0.065 \cdot \text{CL}$
	$t_F$	4.483	$1.509 + 0.059 \cdot \text{CL}$	$1.656 + 0.057 \cdot \text{CL}$	$1.734 + 0.056 \cdot \text{CL}$
	$t_{PLH}$	3.970	$2.249 + 0.034 \cdot \text{CL}$	$2.350 + 0.032 \cdot \text{CL}$	$2.408 + 0.032 \cdot \text{CL}$
	$t_{PHL}$	5.356	$3.141 + 0.044 \cdot \text{CL}$	$3.442 + 0.038 \cdot \text{CL}$	$3.692 + 0.035 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOB10SH**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.281	$1.455 + 0.077 \cdot \text{CL}$	$1.475 + 0.076 \cdot \text{CL}$	$1.424 + 0.077 \cdot \text{CL}$
	$t_F$	6.213	$2.435 + 0.076 \cdot \text{CL}$	$2.714 + 0.070 \cdot \text{CL}$	$2.902 + 0.067 \cdot \text{CL}$
	$t_{PLH}$	5.749	$3.412 + 0.047 \cdot \text{CL}$	$3.654 + 0.042 \cdot \text{CL}$	$3.825 + 0.040 \cdot \text{CL}$
	$t_{PHL}$	7.639	$4.521 + 0.062 \cdot \text{CL}$	$5.020 + 0.052 \cdot \text{CL}$	$5.446 + 0.047 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOB12SH**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.972	$1.688 + 0.066 \cdot \text{CL}$	$1.804 + 0.063 \cdot \text{CL}$	$1.821 + 0.063 \cdot \text{CL}$
	$t_F$	6.233	$2.772 + 0.069 \cdot \text{CL}$	$3.130 + 0.062 \cdot \text{CL}$	$3.403 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	5.899	$3.670 + 0.045 \cdot \text{CL}$	$3.971 + 0.039 \cdot \text{CL}$	$4.210 + 0.035 \cdot \text{CL}$
	$t_{PHL}$	7.963	$4.796 + 0.063 \cdot \text{CL}$	$5.374 + 0.052 \cdot \text{CL}$	$5.877 + 0.045 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



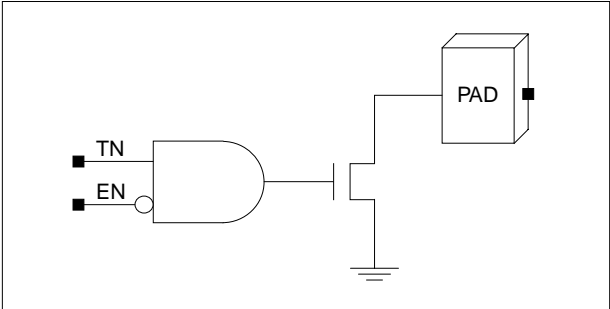
# PvODyz

## Open Drain Output Buffers

### Cell Availability

2.5V Only	3.3V Interface	5V Tolerant
POD(1/2/4/6/8/10/12) POD(4/6/8/10/12)SM POD(10/12)SH	PHOD(1/2/4/6/8/10/12) PHOD(4/6/8/10/12)SM PHOD(10/12)SH	PTOD(1/2/3)

### Logic Symbol



### Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

### Standard Load (SL)

Cell Name	TN	EN
POD(1/2/4/6/8/10/12)	2.897	2.916
POD(4/6/8/10/12)SM	2.897	2.916
POD(10/12)SH	2.897	2.916
PHOD(1/2/4/6/8/10/12)	2.897	2.916
PHOD(4/6/8/10/12)SM	2.897	2.916
PHOD(10/12)SH	2.897	2.916
PTOD(1/2/3)	2.897	2.916



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**POD1**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	33.275	$1.275 + 0.640 \cdot \text{CL}$	$1.279 + 0.640 \cdot \text{CL}$	$1.276 + 0.640 \cdot \text{CL}$
	t <sub>PHL</sub>	24.790	$1.900 + 0.458 \cdot \text{CL}$	$1.764 + 0.461 \cdot \text{CL}$	$1.764 + 0.461 \cdot \text{CL}$
	t <sub>PLZ</sub>	0.875	$0.874 + 0.000 \cdot \text{CL}$	$0.875 + 0.000 \cdot \text{CL}$	$0.875 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	33.275	$1.275 + 0.640 \cdot \text{CL}$	$1.279 + 0.640 \cdot \text{CL}$	$1.276 + 0.640 \cdot \text{CL}$
	t <sub>PHL</sub>	24.888	$1.998 + 0.458 \cdot \text{CL}$	$1.862 + 0.461 \cdot \text{CL}$	$1.862 + 0.461 \cdot \text{CL}$
	t <sub>PLZ</sub>	0.917	$0.917 + 0.000 \cdot \text{CL}$	$0.917 + 0.000 \cdot \text{CL}$	$0.917 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POD2**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	18.210	$0.685 + 0.351 \cdot \text{CL}$	$0.688 + 0.350 \cdot \text{CL}$	$0.685 + 0.350 \cdot \text{CL}$
	t <sub>PHL</sub>	14.231	$1.304 + 0.259 \cdot \text{CL}$	$1.229 + 0.260 \cdot \text{CL}$	$1.229 + 0.260 \cdot \text{CL}$
	t <sub>PLZ</sub>	0.728	$0.728 + 0.000 \cdot \text{CL}$	$0.728 + 0.000 \cdot \text{CL}$	$0.728 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	18.210	$0.685 + 0.351 \cdot \text{CL}$	$0.688 + 0.350 \cdot \text{CL}$	$0.685 + 0.350 \cdot \text{CL}$
	t <sub>PHL</sub>	14.329	$1.403 + 0.259 \cdot \text{CL}$	$1.327 + 0.260 \cdot \text{CL}$	$1.324 + 0.260 \cdot \text{CL}$
	t <sub>PLZ</sub>	0.772	$0.772 + 0.000 \cdot \text{CL}$	$0.771 + 0.000 \cdot \text{CL}$	$0.772 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POD4**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	9.121	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$
	t <sub>PHL</sub>	7.510	$1.047 + 0.129 \cdot \text{CL}$	$1.008 + 0.130 \cdot \text{CL}$	$1.011 + 0.130 \cdot \text{CL}$
	t <sub>PLZ</sub>	0.857	$0.857 + 0.000 \cdot \text{CL}$	$0.857 + 0.000 \cdot \text{CL}$	$0.857 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	9.121	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$
	t <sub>PHL</sub>	7.609	$1.146 + 0.129 \cdot \text{CL}$	$1.106 + 0.130 \cdot \text{CL}$	$1.110 + 0.130 \cdot \text{CL}$
	t <sub>PLZ</sub>	0.900	$0.900 + 0.000 \cdot \text{CL}$	$0.900 + 0.000 \cdot \text{CL}$	$0.900 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POD6**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	6.097	$0.255 + 0.117 \cdot \text{CL}$	$0.255 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$
	t <sub>PHL</sub>	5.319	$1.010 + 0.086 \cdot \text{CL}$	$0.984 + 0.087 \cdot \text{CL}$	$0.984 + 0.087 \cdot \text{CL}$
	t <sub>PLZ</sub>	0.984	$0.984 + 0.000 \cdot \text{CL}$	$0.984 + 0.000 \cdot \text{CL}$	$0.984 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	6.097	$0.255 + 0.117 \cdot \text{CL}$	$0.255 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$
	t <sub>PHL</sub>	5.418	$1.108 + 0.086 \cdot \text{CL}$	$1.083 + 0.087 \cdot \text{CL}$	$1.083 + 0.087 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.026	$1.026 + 0.000 \cdot \text{CL}$	$1.026 + 0.000 \cdot \text{CL}$	$1.026 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvODyz

## Open Drain Output Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### POD8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	tF	4.588	$0.206 + 0.088 \cdot \text{CL}$	$0.207 + 0.088 \cdot \text{CL}$	$0.207 + 0.088 \cdot \text{CL}$
	tPHL	4.260	$1.028 + 0.065 \cdot \text{CL}$	$1.009 + 0.065 \cdot \text{CL}$	$1.009 + 0.065 \cdot \text{CL}$
	tPLZ	1.111	$1.111 + 0.000 \cdot \text{CL}$	$1.111 + 0.000 \cdot \text{CL}$	$1.111 + 0.000 \cdot \text{CL}$
EN to PAD	tF	4.588	$0.206 + 0.088 \cdot \text{CL}$	$0.207 + 0.088 \cdot \text{CL}$	$0.207 + 0.088 \cdot \text{CL}$
	tPHL	4.358	$1.126 + 0.065 \cdot \text{CL}$	$1.107 + 0.065 \cdot \text{CL}$	$1.108 + 0.065 \cdot \text{CL}$
	tPLZ	1.153	$1.153 + 0.000 \cdot \text{CL}$	$1.153 + 0.000 \cdot \text{CL}$	$1.153 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POD10

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	tF	3.667	$0.161 + 0.070 \cdot \text{CL}$	$0.162 + 0.070 \cdot \text{CL}$	$0.162 + 0.070 \cdot \text{CL}$
	tPHL	3.524	$0.938 + 0.052 \cdot \text{CL}$	$0.923 + 0.052 \cdot \text{CL}$	$0.923 + 0.052 \cdot \text{CL}$
	tPLZ	0.968	$0.968 + 0.000 \cdot \text{CL}$	$0.968 + 0.000 \cdot \text{CL}$	$0.968 + 0.000 \cdot \text{CL}$
EN to PAD	tF	3.667	$0.161 + 0.070 \cdot \text{CL}$	$0.162 + 0.070 \cdot \text{CL}$	$0.162 + 0.070 \cdot \text{CL}$
	tPHL	3.623	$1.037 + 0.052 \cdot \text{CL}$	$1.022 + 0.052 \cdot \text{CL}$	$1.022 + 0.052 \cdot \text{CL}$
	tPLZ	1.011	$1.011 + 0.000 \cdot \text{CL}$	$1.011 + 0.000 \cdot \text{CL}$	$1.011 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POD12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	tF	3.064	$0.143 + 0.058 \cdot \text{CL}$	$0.143 + 0.058 \cdot \text{CL}$	$0.144 + 0.058 \cdot \text{CL}$
	tPHL	3.108	$0.953 + 0.043 \cdot \text{CL}$	$0.941 + 0.043 \cdot \text{CL}$	$0.941 + 0.043 \cdot \text{CL}$
	tPLZ	1.032	$1.031 + 0.000 \cdot \text{CL}$	$1.032 + 0.000 \cdot \text{CL}$	$1.032 + 0.000 \cdot \text{CL}$
EN to PAD	tF	3.064	$0.143 + 0.058 \cdot \text{CL}$	$0.143 + 0.058 \cdot \text{CL}$	$0.144 + 0.058 \cdot \text{CL}$
	tPHL	3.207	$1.052 + 0.043 \cdot \text{CL}$	$1.039 + 0.043 \cdot \text{CL}$	$1.040 + 0.043 \cdot \text{CL}$
	tPLZ	1.075	$1.075 + 0.000 \cdot \text{CL}$	$1.075 + 0.000 \cdot \text{CL}$	$1.075 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**POD4SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	9.279	$0.637 + 0.173 \cdot \text{CL}$	$0.549 + 0.175 \cdot \text{CL}$	$0.510 + 0.175 \cdot \text{CL}$
	t <sub>PHL</sub>	9.580	$3.085 + 0.130 \cdot \text{CL}$	$3.073 + 0.130 \cdot \text{CL}$	$3.078 + 0.130 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.000	$0.999 + 0.000 \cdot \text{CL}$	$1.000 + 0.000 \cdot \text{CL}$	$1.000 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	9.279	$0.637 + 0.173 \cdot \text{CL}$	$0.549 + 0.175 \cdot \text{CL}$	$0.510 + 0.175 \cdot \text{CL}$
	t <sub>PHL</sub>	9.679	$3.183 + 0.130 \cdot \text{CL}$	$3.172 + 0.130 \cdot \text{CL}$	$3.177 + 0.130 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.043	$1.042 + 0.000 \cdot \text{CL}$	$1.043 + 0.000 \cdot \text{CL}$	$1.043 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POD6SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	6.521	$0.979 + 0.111 \cdot \text{CL}$	$0.863 + 0.113 \cdot \text{CL}$	$0.735 + 0.115 \cdot \text{CL}$
	t <sub>PHL</sub>	8.285	$3.720 + 0.091 \cdot \text{CL}$	$3.870 + 0.088 \cdot \text{CL}$	$3.952 + 0.087 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.275	$1.275 + 0.000 \cdot \text{CL}$	$1.275 + 0.000 \cdot \text{CL}$	$1.275 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	6.521	$0.979 + 0.111 \cdot \text{CL}$	$0.863 + 0.113 \cdot \text{CL}$	$0.735 + 0.115 \cdot \text{CL}$
	t <sub>PHL</sub>	8.383	$3.819 + 0.091 \cdot \text{CL}$	$3.968 + 0.088 \cdot \text{CL}$	$4.054 + 0.087 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.317	$1.317 + 0.000 \cdot \text{CL}$	$1.317 + 0.000 \cdot \text{CL}$	$1.317 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POD8SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	5.166	$1.112 + 0.081 \cdot \text{CL}$	$1.028 + 0.083 \cdot \text{CL}$	$0.893 + 0.085 \cdot \text{CL}$
	t <sub>PHL</sub>	7.288	$3.655 + 0.073 \cdot \text{CL}$	$3.883 + 0.068 \cdot \text{CL}$	$4.028 + 0.066 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.883	$1.882 + 0.000 \cdot \text{CL}$	$1.883 + 0.000 \cdot \text{CL}$	$1.883 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	5.166	$1.112 + 0.081 \cdot \text{CL}$	$1.028 + 0.083 \cdot \text{CL}$	$0.893 + 0.085 \cdot \text{CL}$
	t <sub>PHL</sub>	7.387	$3.754 + 0.073 \cdot \text{CL}$	$3.981 + 0.068 \cdot \text{CL}$	$4.126 + 0.066 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.926	$1.924 + 0.000 \cdot \text{CL}$	$1.925 + 0.000 \cdot \text{CL}$	$1.925 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvODyz

## Open Drain Output Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### POD10SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	4.261	$0.986 + 0.066 \cdot \text{CL}$	$0.954 + 0.066 \cdot \text{CL}$	$0.867 + 0.067 \cdot \text{CL}$
	$t_{PHL}$	6.653	$3.655 + 0.060 \cdot \text{CL}$	$3.871 + 0.056 \cdot \text{CL}$	$4.025 + 0.054 \cdot \text{CL}$
	$t_{PLZ}$	1.883	$1.882 + 0.000 \cdot \text{CL}$	$1.883 + 0.000 \cdot \text{CL}$	$1.883 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	4.261	$0.985 + 0.066 \cdot \text{CL}$	$0.955 + 0.066 \cdot \text{CL}$	$0.867 + 0.067 \cdot \text{CL}$
	$t_{PHL}$	6.752	$3.754 + 0.060 \cdot \text{CL}$	$3.970 + 0.056 \cdot \text{CL}$	$4.123 + 0.054 \cdot \text{CL}$
	$t_{PLZ}$	1.926	$1.924 + 0.000 \cdot \text{CL}$	$1.925 + 0.000 \cdot \text{CL}$	$1.925 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POD12SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	3.987	$1.230 + 0.055 \cdot \text{CL}$	$1.278 + 0.054 \cdot \text{CL}$	$1.248 + 0.055 \cdot \text{CL}$
	$t_{PHL}$	6.787	$3.941 + 0.057 \cdot \text{CL}$	$4.253 + 0.051 \cdot \text{CL}$	$4.507 + 0.047 \cdot \text{CL}$
	$t_{PLZ}$	2.251	$2.250 + 0.000 \cdot \text{CL}$	$2.251 + 0.000 \cdot \text{CL}$	$2.251 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	3.987	$1.230 + 0.055 \cdot \text{CL}$	$1.278 + 0.054 \cdot \text{CL}$	$1.248 + 0.055 \cdot \text{CL}$
	$t_{PHL}$	6.886	$4.040 + 0.057 \cdot \text{CL}$	$4.351 + 0.051 \cdot \text{CL}$	$4.606 + 0.047 \cdot \text{CL}$
	$t_{PLZ}$	2.294	$2.292 + 0.000 \cdot \text{CL}$	$2.293 + 0.000 \cdot \text{CL}$	$2.293 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POD10SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	5.431	$2.047 + 0.068 \cdot \text{CL}$	$2.179 + 0.065 \cdot \text{CL}$	$2.213 + 0.065 \cdot \text{CL}$
	$t_{PHL}$	9.785	$5.852 + 0.079 \cdot \text{CL}$	$6.395 + 0.068 \cdot \text{CL}$	$6.860 + 0.062 \cdot \text{CL}$
	$t_{PLZ}$	2.322	$2.321 + 0.000 \cdot \text{CL}$	$2.322 + 0.000 \cdot \text{CL}$	$2.322 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	5.431	$2.047 + 0.068 \cdot \text{CL}$	$2.179 + 0.065 \cdot \text{CL}$	$2.213 + 0.065 \cdot \text{CL}$
	$t_{PHL}$	9.884	$5.950 + 0.079 \cdot \text{CL}$	$6.494 + 0.068 \cdot \text{CL}$	$6.959 + 0.062 \cdot \text{CL}$
	$t_{PLZ}$	2.365	$2.363 + 0.000 \cdot \text{CL}$	$2.364 + 0.000 \cdot \text{CL}$	$2.365 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POD12SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	5.378	$2.451 + 0.059 \cdot \text{CL}$	$2.627 + 0.055 \cdot \text{CL}$	$2.722 + 0.054 \cdot \text{CL}$
	$t_{PHL}$	10.235	$6.317 + 0.078 \cdot \text{CL}$	$6.969 + 0.065 \cdot \text{CL}$	$7.539 + 0.058 \cdot \text{CL}$
	$t_{PLZ}$	2.690	$2.688 + 0.000 \cdot \text{CL}$	$2.689 + 0.000 \cdot \text{CL}$	$2.690 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	5.378	$2.451 + 0.059 \cdot \text{CL}$	$2.627 + 0.055 \cdot \text{CL}$	$2.722 + 0.054 \cdot \text{CL}$
	$t_{PHL}$	10.334	$6.416 + 0.078 \cdot \text{CL}$	$7.068 + 0.065 \cdot \text{CL}$	$7.638 + 0.058 \cdot \text{CL}$
	$t_{PLZ}$	2.733	$2.730 + 0.000 \cdot \text{CL}$	$2.732 + 0.000 \cdot \text{CL}$	$2.733 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PHOD1**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	33.014	$1.269 + 0.635 \cdot \text{CL}$	$1.270 + 0.635 \cdot \text{CL}$	$1.267 + 0.635 \cdot \text{CL}$
	t <sub>PHL</sub>	17.228	$1.663 + 0.311 \cdot \text{CL}$	$1.664 + 0.311 \cdot \text{CL}$	$1.664 + 0.311 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.199	$1.198 + 0.000 \cdot \text{CL}$	$1.199 + 0.000 \cdot \text{CL}$	$1.199 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	33.014	$1.269 + 0.635 \cdot \text{CL}$	$1.270 + 0.635 \cdot \text{CL}$	$1.267 + 0.635 \cdot \text{CL}$
	t <sub>PHL</sub>	17.327	$1.762 + 0.311 \cdot \text{CL}$	$1.763 + 0.311 \cdot \text{CL}$	$1.763 + 0.311 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.242	$1.242 + 0.000 \cdot \text{CL}$	$1.242 + 0.000 \cdot \text{CL}$	$1.242 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOD2**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	18.188	$0.706 + 0.350 \cdot \text{CL}$	$0.702 + 0.350 \cdot \text{CL}$	$0.705 + 0.350 \cdot \text{CL}$
	t <sub>PHL</sub>	10.187	$1.292 + 0.178 \cdot \text{CL}$	$1.291 + 0.178 \cdot \text{CL}$	$1.294 + 0.178 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.056	$1.056 + 0.000 \cdot \text{CL}$	$1.056 + 0.000 \cdot \text{CL}$	$1.056 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	18.188	$0.706 + 0.350 \cdot \text{CL}$	$0.702 + 0.350 \cdot \text{CL}$	$0.705 + 0.350 \cdot \text{CL}$
	t <sub>PHL</sub>	10.286	$1.391 + 0.178 \cdot \text{CL}$	$1.390 + 0.178 \cdot \text{CL}$	$1.393 + 0.178 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.100	$1.100 + 0.000 \cdot \text{CL}$	$1.100 + 0.000 \cdot \text{CL}$	$1.100 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOD4**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	9.114	$0.371 + 0.175 \cdot \text{CL}$	$0.371 + 0.175 \cdot \text{CL}$	$0.372 + 0.175 \cdot \text{CL}$
	t <sub>PHL</sub>	5.622	$1.175 + 0.089 \cdot \text{CL}$	$1.175 + 0.089 \cdot \text{CL}$	$1.175 + 0.089 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.206	$1.206 + 0.000 \cdot \text{CL}$	$1.206 + 0.000 \cdot \text{CL}$	$1.206 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	9.114	$0.371 + 0.175 \cdot \text{CL}$	$0.371 + 0.175 \cdot \text{CL}$	$0.372 + 0.175 \cdot \text{CL}$
	t <sub>PHL</sub>	5.721	$1.273 + 0.089 \cdot \text{CL}$	$1.274 + 0.089 \cdot \text{CL}$	$1.274 + 0.089 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.249	$1.249 + 0.000 \cdot \text{CL}$	$1.249 + 0.000 \cdot \text{CL}$	$1.249 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOD6**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	6.082	$0.254 + 0.117 \cdot \text{CL}$	$0.254 + 0.117 \cdot \text{CL}$	$0.255 + 0.117 \cdot \text{CL}$
	t <sub>PHL</sub>	4.080	$1.115 + 0.059 \cdot \text{CL}$	$1.115 + 0.059 \cdot \text{CL}$	$1.115 + 0.059 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.166	$1.166 + 0.000 \cdot \text{CL}$	$1.166 + 0.000 \cdot \text{CL}$	$1.166 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	6.082	$0.254 + 0.117 \cdot \text{CL}$	$0.254 + 0.117 \cdot \text{CL}$	$0.255 + 0.117 \cdot \text{CL}$
	t <sub>PHL</sub>	4.179	$1.214 + 0.059 \cdot \text{CL}$	$1.214 + 0.059 \cdot \text{CL}$	$1.214 + 0.059 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.209	$1.209 + 0.000 \cdot \text{CL}$	$1.209 + 0.000 \cdot \text{CL}$	$1.209 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



## PvODyz

### Open Drain Output Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### PHOD8

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	tF	4.572	$0.205 + 0.087 \cdot \text{CL}$	$0.202 + 0.087 \cdot \text{CL}$	$0.201 + 0.087 \cdot \text{CL}$
	tPHL	3.344	$1.120 + 0.044 \cdot \text{CL}$	$1.120 + 0.044 \cdot \text{CL}$	$1.120 + 0.044 \cdot \text{CL}$
	tPLZ	1.240	$1.240 + 0.000 \cdot \text{CL}$	$1.240 + 0.000 \cdot \text{CL}$	$1.240 + 0.000 \cdot \text{CL}$
EN to PAD	tF	4.572	$0.205 + 0.087 \cdot \text{CL}$	$0.202 + 0.087 \cdot \text{CL}$	$0.201 + 0.087 \cdot \text{CL}$
	tPHL	3.443	$1.219 + 0.044 \cdot \text{CL}$	$1.219 + 0.044 \cdot \text{CL}$	$1.219 + 0.044 \cdot \text{CL}$
	tPLZ	1.284	$1.284 + 0.000 \cdot \text{CL}$	$1.284 + 0.000 \cdot \text{CL}$	$1.284 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### PHOD10

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	tF	3.669	$0.183 + 0.070 \cdot \text{CL}$	$0.175 + 0.070 \cdot \text{CL}$	$0.172 + 0.070 \cdot \text{CL}$
	tPHL	2.917	$1.137 + 0.036 \cdot \text{CL}$	$1.138 + 0.036 \cdot \text{CL}$	$1.137 + 0.036 \cdot \text{CL}$
	tPLZ	1.315	$1.315 + 0.000 \cdot \text{CL}$	$1.315 + 0.000 \cdot \text{CL}$	$1.315 + 0.000 \cdot \text{CL}$
EN to PAD	tF	3.669	$0.183 + 0.070 \cdot \text{CL}$	$0.175 + 0.070 \cdot \text{CL}$	$0.172 + 0.070 \cdot \text{CL}$
	tPHL	3.016	$1.236 + 0.036 \cdot \text{CL}$	$1.236 + 0.036 \cdot \text{CL}$	$1.237 + 0.036 \cdot \text{CL}$
	tPLZ	1.359	$1.359 + 0.000 \cdot \text{CL}$	$1.359 + 0.000 \cdot \text{CL}$	$1.359 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### PHOD12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	tF	3.071	$0.177 + 0.058 \cdot \text{CL}$	$0.163 + 0.058 \cdot \text{CL}$	$0.156 + 0.058 \cdot \text{CL}$
	tPHL	2.644	$1.161 + 0.030 \cdot \text{CL}$	$1.161 + 0.030 \cdot \text{CL}$	$1.161 + 0.030 \cdot \text{CL}$
	tPLZ	1.390	$1.390 + 0.000 \cdot \text{CL}$	$1.390 + 0.000 \cdot \text{CL}$	$1.390 + 0.000 \cdot \text{CL}$
EN to PAD	tF	3.071	$0.177 + 0.058 \cdot \text{CL}$	$0.163 + 0.058 \cdot \text{CL}$	$0.156 + 0.058 \cdot \text{CL}$
	tPHL	2.743	$1.260 + 0.030 \cdot \text{CL}$	$1.260 + 0.030 \cdot \text{CL}$	$1.260 + 0.030 \cdot \text{CL}$
	tPLZ	1.433	$1.433 + 0.000 \cdot \text{CL}$	$1.433 + 0.000 \cdot \text{CL}$	$1.433 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PHOD4SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	9.439	$0.956 + 0.170 \cdot \text{CL}$	$0.850 + 0.172 \cdot \text{CL}$	$0.752 + 0.173 \cdot \text{CL}$
	t <sub>PHL</sub>	7.343	$2.833 + 0.090 \cdot \text{CL}$	$2.883 + 0.089 \cdot \text{CL}$	$2.896 + 0.089 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.304	$1.305 + 0.000 \cdot \text{CL}$	$1.303 + 0.000 \cdot \text{CL}$	$1.305 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	9.439	$0.956 + 0.170 \cdot \text{CL}$	$0.850 + 0.172 \cdot \text{CL}$	$0.752 + 0.173 \cdot \text{CL}$
	t <sub>PHL</sub>	7.441	$2.932 + 0.090 \cdot \text{CL}$	$2.981 + 0.089 \cdot \text{CL}$	$2.995 + 0.089 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.349	$1.348 + 0.000 \cdot \text{CL}$	$1.349 + 0.000 \cdot \text{CL}$	$1.349 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOD6SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	6.922	$1.379 + 0.111 \cdot \text{CL}$	$1.347 + 0.111 \cdot \text{CL}$	$1.264 + 0.113 \cdot \text{CL}$
	t <sub>PHL</sub>	6.621	$3.306 + 0.066 \cdot \text{CL}$	$3.516 + 0.062 \cdot \text{CL}$	$3.643 + 0.060 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.609	$1.609 + 0.000 \cdot \text{CL}$	$1.609 + 0.000 \cdot \text{CL}$	$1.609 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	6.922	$1.379 + 0.111 \cdot \text{CL}$	$1.347 + 0.111 \cdot \text{CL}$	$1.264 + 0.113 \cdot \text{CL}$
	t <sub>PHL</sub>	6.720	$3.405 + 0.066 \cdot \text{CL}$	$3.615 + 0.062 \cdot \text{CL}$	$3.742 + 0.060 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.653	$1.653 + 0.000 \cdot \text{CL}$	$1.653 + 0.000 \cdot \text{CL}$	$1.653 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOD8SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t <sub>F</sub>	6.080	$1.825 + 0.085 \cdot \text{CL}$	$1.936 + 0.083 \cdot \text{CL}$	$1.953 + 0.083 \cdot \text{CL}$
	t <sub>PHL</sub>	6.644	$3.669 + 0.059 \cdot \text{CL}$	$4.019 + 0.052 \cdot \text{CL}$	$4.291 + 0.049 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.913	$1.913 + 0.000 \cdot \text{CL}$	$1.913 + 0.000 \cdot \text{CL}$	$1.913 + 0.000 \cdot \text{CL}$
EN to PAD	t <sub>F</sub>	6.080	$1.825 + 0.085 \cdot \text{CL}$	$1.936 + 0.083 \cdot \text{CL}$	$1.953 + 0.083 \cdot \text{CL}$
	t <sub>PHL</sub>	6.743	$3.768 + 0.059 \cdot \text{CL}$	$4.118 + 0.053 \cdot \text{CL}$	$4.390 + 0.049 \cdot \text{CL}$
	t <sub>PLZ</sub>	1.957	$1.957 + 0.000 \cdot \text{CL}$	$1.956 + 0.000 \cdot \text{CL}$	$1.957 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvODyz

## Open Drain Output Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

### PHOD10SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	5.308	$1.865 + 0.069 \cdot \text{CL}$	$2.008 + 0.066 \cdot \text{CL}$	$2.054 + 0.065 \cdot \text{CL}$
	$t_{PHL}$	6.099	$3.486 + 0.052 \cdot \text{CL}$	$3.855 + 0.045 \cdot \text{CL}$	$4.150 + 0.041 \cdot \text{CL}$
	$t_{PLZ}$	2.661	$2.661 + 0.000 \cdot \text{CL}$	$2.661 + 0.000 \cdot \text{CL}$	$2.661 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	5.308	$1.865 + 0.069 \cdot \text{CL}$	$2.008 + 0.066 \cdot \text{CL}$	$2.054 + 0.065 \cdot \text{CL}$
	$t_{PHL}$	6.198	$3.585 + 0.052 \cdot \text{CL}$	$3.955 + 0.045 \cdot \text{CL}$	$4.249 + 0.041 \cdot \text{CL}$
	$t_{PLZ}$	2.705	$2.705 + 0.000 \cdot \text{CL}$	$2.705 + 0.000 \cdot \text{CL}$	$2.704 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOD12SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	4.505	$1.544 + 0.059 \cdot \text{CL}$	$1.686 + 0.056 \cdot \text{CL}$	$1.760 + 0.055 \cdot \text{CL}$
	$t_{PHL}$	5.672	$3.452 + 0.044 \cdot \text{CL}$	$3.756 + 0.038 \cdot \text{CL}$	$4.008 + 0.035 \cdot \text{CL}$
	$t_{PLZ}$	2.661	$2.661 + 0.000 \cdot \text{CL}$	$2.661 + 0.000 \cdot \text{CL}$	$2.661 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	4.505	$1.544 + 0.059 \cdot \text{CL}$	$1.686 + 0.056 \cdot \text{CL}$	$1.760 + 0.055 \cdot \text{CL}$
	$t_{PHL}$	5.771	$3.551 + 0.044 \cdot \text{CL}$	$3.855 + 0.038 \cdot \text{CL}$	$4.107 + 0.035 \cdot \text{CL}$
	$t_{PLZ}$	2.705	$2.705 + 0.000 \cdot \text{CL}$	$2.705 + 0.000 \cdot \text{CL}$	$2.705 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOD10SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	6.249	$2.489 + 0.075 \cdot \text{CL}$	$2.762 + 0.070 \cdot \text{CL}$	$2.945 + 0.067 \cdot \text{CL}$
	$t_{PHL}$	7.897	$4.768 + 0.063 \cdot \text{CL}$	$5.272 + 0.052 \cdot \text{CL}$	$5.704 + 0.047 \cdot \text{CL}$
	$t_{PLZ}$	2.715	$2.715 + 0.000 \cdot \text{CL}$	$2.715 + 0.000 \cdot \text{CL}$	$2.715 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	6.249	$2.489 + 0.075 \cdot \text{CL}$	$2.762 + 0.070 \cdot \text{CL}$	$2.945 + 0.067 \cdot \text{CL}$
	$t_{PHL}$	7.996	$4.867 + 0.063 \cdot \text{CL}$	$5.371 + 0.052 \cdot \text{CL}$	$5.803 + 0.047 \cdot \text{CL}$
	$t_{PLZ}$	2.757	$2.757 + 0.000 \cdot \text{CL}$	$2.757 + 0.000 \cdot \text{CL}$	$2.757 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOD12SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	6.277	$2.841 + 0.069 \cdot \text{CL}$	$3.190 + 0.062 \cdot \text{CL}$	$3.455 + 0.058 \cdot \text{CL}$
	$t_{PHL}$	8.214	$5.033 + 0.064 \cdot \text{CL}$	$5.618 + 0.052 \cdot \text{CL}$	$6.126 + 0.045 \cdot \text{CL}$
	$t_{PLZ}$	3.120	$3.119 + 0.000 \cdot \text{CL}$	$3.120 + 0.000 \cdot \text{CL}$	$3.120 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	6.277	$2.841 + 0.069 \cdot \text{CL}$	$3.190 + 0.062 \cdot \text{CL}$	$3.455 + 0.058 \cdot \text{CL}$
	$t_{PHL}$	8.313	$5.132 + 0.064 \cdot \text{CL}$	$5.717 + 0.052 \cdot \text{CL}$	$6.226 + 0.045 \cdot \text{CL}$
	$t_{PLZ}$	3.162	$3.161 + 0.000 \cdot \text{CL}$	$3.162 + 0.000 \cdot \text{CL}$	$3.162 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PTOD1**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	33.498	$2.496 + 0.620 \cdot \text{CL}$	$2.456 + 0.621 \cdot \text{CL}$	$2.426 + 0.621 \cdot \text{CL}$
	$t_{PHL}$	16.998	$1.635 + 0.307 \cdot \text{CL}$	$1.632 + 0.307 \cdot \text{CL}$	$1.641 + 0.307 \cdot \text{CL}$
	$t_{PLZ}$	1.028	$1.028 + 0.000 \cdot \text{CL}$	$1.028 + 0.000 \cdot \text{CL}$	$1.028 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	33.498	$2.496 + 0.620 \cdot \text{CL}$	$2.456 + 0.621 \cdot \text{CL}$	$2.426 + 0.621 \cdot \text{CL}$
	$t_{PHL}$	17.097	$1.734 + 0.307 \cdot \text{CL}$	$1.733 + 0.307 \cdot \text{CL}$	$1.736 + 0.307 \cdot \text{CL}$
	$t_{PLZ}$	1.072	$1.072 + 0.000 \cdot \text{CL}$	$1.072 + 0.000 \cdot \text{CL}$	$1.072 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PTOD2**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	16.748	$1.240 + 0.310 \cdot \text{CL}$	$1.234 + 0.310 \cdot \text{CL}$	$1.222 + 0.310 \cdot \text{CL}$
	$t_{PHL}$	8.985	$1.312 + 0.153 \cdot \text{CL}$	$1.315 + 0.153 \cdot \text{CL}$	$1.312 + 0.153 \cdot \text{CL}$
	$t_{PLZ}$	1.151	$1.151 + 0.000 \cdot \text{CL}$	$1.151 + 0.000 \cdot \text{CL}$	$1.151 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	16.748	$1.240 + 0.310 \cdot \text{CL}$	$1.234 + 0.310 \cdot \text{CL}$	$1.222 + 0.310 \cdot \text{CL}$
	$t_{PHL}$	9.084	$1.411 + 0.153 \cdot \text{CL}$	$1.414 + 0.153 \cdot \text{CL}$	$1.411 + 0.153 \cdot \text{CL}$
	$t_{PLZ}$	1.195	$1.195 + 0.000 \cdot \text{CL}$	$1.195 + 0.000 \cdot \text{CL}$	$1.195 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PTOD3**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	$t_F$	11.158	$0.810 + 0.207 \cdot \text{CL}$	$0.812 + 0.207 \cdot \text{CL}$	$0.809 + 0.207 \cdot \text{CL}$
	$t_{PHL}$	6.351	$1.235 + 0.102 \cdot \text{CL}$	$1.238 + 0.102 \cdot \text{CL}$	$1.239 + 0.102 \cdot \text{CL}$
	$t_{PLZ}$	1.272	$1.272 + 0.000 \cdot \text{CL}$	$1.272 + 0.000 \cdot \text{CL}$	$1.272 + 0.000 \cdot \text{CL}$
EN to PAD	$t_F$	11.158	$0.810 + 0.207 \cdot \text{CL}$	$0.812 + 0.207 \cdot \text{CL}$	$0.809 + 0.207 \cdot \text{CL}$
	$t_{PHL}$	6.450	$1.334 + 0.102 \cdot \text{CL}$	$1.337 + 0.102 \cdot \text{CL}$	$1.338 + 0.102 \cdot \text{CL}$
	$t_{PLZ}$	1.316	$1.316 + 0.000 \cdot \text{CL}$	$1.316 + 0.000 \cdot \text{CL}$	$1.316 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



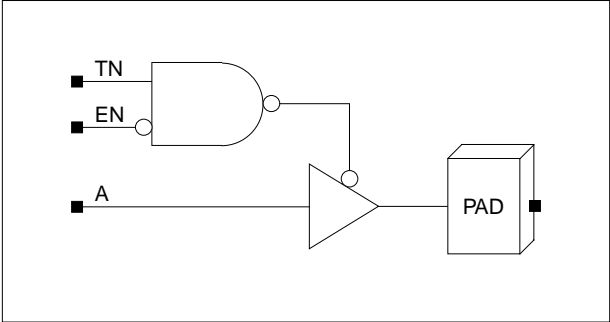
# PvOTyz

## Tri-State Output Buffers

### Cell Availability

2.5V Only	3.3V Interface	5V Tolerant
POT(1/2/4/6/8/10/12) POT(4/6/8/10/12)SM POT(10/12)SH	PHOT(1/2/4/6/8/10/12) PHOT(4/6/8/10/12)SM PHOT(10/12)SH	PTOT(1/2/3)

### Logic Symbol



### Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

### Standard Load (SL)

Cell Name	TN	EN	A
POT(1/2/4/6/8/10/12)	2.898	2.916	3.023
POT(4/6/8/10/12)SM	2.898	2.916	3.023
POT(10/12)SH	2.898	2.916	3.023
PHOT(1/2/4/6/8/10/12)	2.898	2.916	5.444
PHOT(4/6/8/10/12)SM	2.898	2.916	5.444
PHOT(10/12)SH	2.898	2.916	5.444
PTOT(1/2/3)	2.898	2.916	5.444



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**POT1**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	31.508	$1.210 + 0.606 \cdot \text{CL}$	$1.212 + 0.606 \cdot \text{CL}$	$1.209 + 0.606 \cdot \text{CL}$
	$t_F$	33.275	$1.275 + 0.640 \cdot \text{CL}$	$1.279 + 0.640 \cdot \text{CL}$	$1.276 + 0.640 \cdot \text{CL}$
	$t_{PLH}$	15.732	$1.226 + 0.290 \cdot \text{CL}$	$1.224 + 0.290 \cdot \text{CL}$	$1.224 + 0.290 \cdot \text{CL}$
	$t_{PHL}$	17.556	$1.448 + 0.322 \cdot \text{CL}$	$1.448 + 0.322 \cdot \text{CL}$	$1.445 + 0.322 \cdot \text{CL}$
TN to PAD	$t_R$	31.508	$1.210 + 0.606 \cdot \text{CL}$	$1.212 + 0.606 \cdot \text{CL}$	$1.209 + 0.606 \cdot \text{CL}$
	$t_F$	33.275	$1.275 + 0.640 \cdot \text{CL}$	$1.279 + 0.640 \cdot \text{CL}$	$1.276 + 0.640 \cdot \text{CL}$
	$t_{PLH}$	15.780	$1.271 + 0.290 \cdot \text{CL}$	$1.272 + 0.290 \cdot \text{CL}$	$1.275 + 0.290 \cdot \text{CL}$
	$t_{PHL}$	17.679	$1.572 + 0.322 \cdot \text{CL}$	$1.569 + 0.322 \cdot \text{CL}$	$1.572 + 0.322 \cdot \text{CL}$
	$t_{PLZ}$	0.958	$0.958 + 0.000 \cdot \text{CL}$	$0.958 + 0.000 \cdot \text{CL}$	$0.958 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.662	$0.662 + 0.000 \cdot \text{CL}$	$0.662 + 0.000 \cdot \text{CL}$	$0.662 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	31.508	$1.210 + 0.606 \cdot \text{CL}$	$1.212 + 0.606 \cdot \text{CL}$	$1.209 + 0.606 \cdot \text{CL}$
	$t_F$	33.274	$1.277 + 0.640 \cdot \text{CL}$	$1.276 + 0.640 \cdot \text{CL}$	$1.276 + 0.640 \cdot \text{CL}$
	$t_{PLH}$	15.882	$1.375 + 0.290 \cdot \text{CL}$	$1.374 + 0.290 \cdot \text{CL}$	$1.377 + 0.290 \cdot \text{CL}$
	$t_{PHL}$	17.782	$1.675 + 0.322 \cdot \text{CL}$	$1.674 + 0.322 \cdot \text{CL}$	$1.671 + 0.322 \cdot \text{CL}$
	$t_{PLZ}$	1.000	$1.000 + 0.000 \cdot \text{CL}$	$1.000 + 0.000 \cdot \text{CL}$	$1.000 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.705	$0.705 + 0.000 \cdot \text{CL}$	$0.705 + 0.000 \cdot \text{CL}$	$0.705 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POT2**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	15.772	$0.624 + 0.303 \cdot \text{CL}$	$0.622 + 0.303 \cdot \text{CL}$	$0.625 + 0.303 \cdot \text{CL}$
	$t_F$	18.210	$0.685 + 0.351 \cdot \text{CL}$	$0.688 + 0.350 \cdot \text{CL}$	$0.685 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	8.290	$1.036 + 0.145 \cdot \text{CL}$	$1.037 + 0.145 \cdot \text{CL}$	$1.035 + 0.145 \cdot \text{CL}$
	$t_{PHL}$	10.194	$1.074 + 0.182 \cdot \text{CL}$	$1.076 + 0.182 \cdot \text{CL}$	$1.073 + 0.182 \cdot \text{CL}$
TN to PAD	$t_R$	15.772	$0.624 + 0.303 \cdot \text{CL}$	$0.622 + 0.303 \cdot \text{CL}$	$0.625 + 0.303 \cdot \text{CL}$
	$t_F$	18.210	$0.685 + 0.351 \cdot \text{CL}$	$0.688 + 0.350 \cdot \text{CL}$	$0.685 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	8.337	$1.083 + 0.145 \cdot \text{CL}$	$1.083 + 0.145 \cdot \text{CL}$	$1.083 + 0.145 \cdot \text{CL}$
	$t_{PHL}$	10.317	$1.197 + 0.182 \cdot \text{CL}$	$1.197 + 0.182 \cdot \text{CL}$	$1.200 + 0.182 \cdot \text{CL}$
	$t_{PLZ}$	0.808	$0.808 + 0.000 \cdot \text{CL}$	$0.808 + 0.000 \cdot \text{CL}$	$0.808 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.768	$0.768 + 0.000 \cdot \text{CL}$	$0.768 + 0.000 \cdot \text{CL}$	$0.768 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	15.772	$0.624 + 0.303 \cdot \text{CL}$	$0.622 + 0.303 \cdot \text{CL}$	$0.625 + 0.303 \cdot \text{CL}$
	$t_F$	18.210	$0.685 + 0.351 \cdot \text{CL}$	$0.688 + 0.350 \cdot \text{CL}$	$0.685 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	8.440	$1.186 + 0.145 \cdot \text{CL}$	$1.187 + 0.145 \cdot \text{CL}$	$1.185 + 0.145 \cdot \text{CL}$
	$t_{PHL}$	10.420	$1.300 + 0.182 \cdot \text{CL}$	$1.302 + 0.182 \cdot \text{CL}$	$1.299 + 0.182 \cdot \text{CL}$
	$t_{PLZ}$	0.851	$0.851 + 0.000 \cdot \text{CL}$	$0.851 + 0.000 \cdot \text{CL}$	$0.851 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.810	$0.810 + 0.000 \cdot \text{CL}$	$0.810 + 0.000 \cdot \text{CL}$	$0.810 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOTyz

## Tri-State Output Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### POT4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	7.917	$0.348 + 0.151 \cdot \text{CL}$	$0.342 + 0.151 \cdot \text{CL}$	$0.343 + 0.151 \cdot \text{CL}$
	$t_F$	9.121	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	4.724	$1.097 + 0.073 \cdot \text{CL}$	$1.097 + 0.073 \cdot \text{CL}$	$1.097 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	5.527	$0.969 + 0.091 \cdot \text{CL}$	$0.968 + 0.091 \cdot \text{CL}$	$0.969 + 0.091 \cdot \text{CL}$
TN to PAD	$t_R$	7.917	$0.348 + 0.151 \cdot \text{CL}$	$0.342 + 0.151 \cdot \text{CL}$	$0.343 + 0.151 \cdot \text{CL}$
	$t_F$	9.121	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	4.772	$1.144 + 0.073 \cdot \text{CL}$	$1.144 + 0.073 \cdot \text{CL}$	$1.145 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	5.649	$1.088 + 0.091 \cdot \text{CL}$	$1.089 + 0.091 \cdot \text{CL}$	$1.090 + 0.091 \cdot \text{CL}$
	$t_{PLZ}$	0.940	$0.940 + 0.000 \cdot \text{CL}$	$0.940 + 0.000 \cdot \text{CL}$	$0.940 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.978	$0.978 + 0.000 \cdot \text{CL}$	$0.978 + 0.000 \cdot \text{CL}$	$0.978 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	7.917	$0.348 + 0.151 \cdot \text{CL}$	$0.342 + 0.151 \cdot \text{CL}$	$0.343 + 0.151 \cdot \text{CL}$
	$t_F$	9.121	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$	$0.359 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	4.874	$1.247 + 0.073 \cdot \text{CL}$	$1.247 + 0.073 \cdot \text{CL}$	$1.247 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	5.752	$1.192 + 0.091 \cdot \text{CL}$	$1.192 + 0.091 \cdot \text{CL}$	$1.191 + 0.091 \cdot \text{CL}$
	$t_{PLZ}$	0.982	$0.982 + 0.000 \cdot \text{CL}$	$0.982 + 0.000 \cdot \text{CL}$	$0.982 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.020	$1.020 + 0.000 \cdot \text{CL}$	$1.020 + 0.000 \cdot \text{CL}$	$1.020 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POT6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.317	$0.309 + 0.100 \cdot \text{CL}$	$0.280 + 0.101 \cdot \text{CL}$	$0.265 + 0.101 \cdot \text{CL}$
	$t_F$	6.097	$0.261 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$
	$t_{PLH}$	3.660	$1.240 + 0.048 \cdot \text{CL}$	$1.241 + 0.048 \cdot \text{CL}$	$1.242 + 0.048 \cdot \text{CL}$
	$t_{PHL}$	4.024	$0.989 + 0.061 \cdot \text{CL}$	$0.986 + 0.061 \cdot \text{CL}$	$0.985 + 0.061 \cdot \text{CL}$
TN to PAD	$t_R$	5.317	$0.309 + 0.100 \cdot \text{CL}$	$0.280 + 0.101 \cdot \text{CL}$	$0.265 + 0.101 \cdot \text{CL}$
	$t_F$	6.097	$0.260 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$
	$t_{PLH}$	3.708	$1.288 + 0.048 \cdot \text{CL}$	$1.289 + 0.048 \cdot \text{CL}$	$1.289 + 0.048 \cdot \text{CL}$
	$t_{PHL}$	4.142	$1.099 + 0.061 \cdot \text{CL}$	$1.101 + 0.061 \cdot \text{CL}$	$1.102 + 0.061 \cdot \text{CL}$
	$t_{PLZ}$	1.067	$1.067 + 0.000 \cdot \text{CL}$	$1.067 + 0.000 \cdot \text{CL}$	$1.067 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.188	$1.187 + 0.000 \cdot \text{CL}$	$1.188 + 0.000 \cdot \text{CL}$	$1.188 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	5.317	$0.309 + 0.100 \cdot \text{CL}$	$0.280 + 0.101 \cdot \text{CL}$	$0.265 + 0.101 \cdot \text{CL}$
	$t_F$	6.097	$0.260 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$	$0.256 + 0.117 \cdot \text{CL}$
	$t_{PLH}$	3.810	$1.391 + 0.048 \cdot \text{CL}$	$1.392 + 0.048 \cdot \text{CL}$	$1.392 + 0.048 \cdot \text{CL}$
	$t_{PHL}$	4.245	$1.203 + 0.061 \cdot \text{CL}$	$1.204 + 0.061 \cdot \text{CL}$	$1.205 + 0.061 \cdot \text{CL}$
	$t_{PLZ}$	1.111	$1.111 + 0.000 \cdot \text{CL}$	$1.111 + 0.000 \cdot \text{CL}$	$1.111 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.230	$1.230 + 0.000 \cdot \text{CL}$	$1.230 + 0.000 \cdot \text{CL}$	$1.230 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**POT8**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.049	$0.351 + 0.074 \cdot \text{CL}$	$0.303 + 0.075 \cdot \text{CL}$	$0.269 + 0.075 \cdot \text{CL}$
	$t_F$	4.592	$0.229 + 0.087 \cdot \text{CL}$	$0.216 + 0.088 \cdot \text{CL}$	$0.210 + 0.088 \cdot \text{CL}$
	$t_{PLH}$	3.220	$1.401 + 0.036 \cdot \text{CL}$	$1.406 + 0.036 \cdot \text{CL}$	$1.407 + 0.036 \cdot \text{CL}$
	$t_{PHL}$	3.313	$1.044 + 0.045 \cdot \text{CL}$	$1.038 + 0.045 \cdot \text{CL}$	$1.035 + 0.046 \cdot \text{CL}$
TN to PAD	$t_R$	4.049	$0.351 + 0.074 \cdot \text{CL}$	$0.303 + 0.075 \cdot \text{CL}$	$0.269 + 0.075 \cdot \text{CL}$
	$t_F$	4.591	$0.227 + 0.087 \cdot \text{CL}$	$0.214 + 0.088 \cdot \text{CL}$	$0.209 + 0.088 \cdot \text{CL}$
	$t_{PLH}$	3.268	$1.448 + 0.036 \cdot \text{CL}$	$1.453 + 0.036 \cdot \text{CL}$	$1.454 + 0.036 \cdot \text{CL}$
	$t_{PHL}$	3.424	$1.140 + 0.046 \cdot \text{CL}$	$1.143 + 0.046 \cdot \text{CL}$	$1.144 + 0.046 \cdot \text{CL}$
	$t_{PLZ}$	1.195	$1.195 + 0.000 \cdot \text{CL}$	$1.195 + 0.000 \cdot \text{CL}$	$1.195 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.397	$1.397 + 0.000 \cdot \text{CL}$	$1.397 + 0.000 \cdot \text{CL}$	$1.397 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	4.049	$0.351 + 0.074 \cdot \text{CL}$	$0.303 + 0.075 \cdot \text{CL}$	$0.269 + 0.075 \cdot \text{CL}$
	$t_F$	4.591	$0.227 + 0.087 \cdot \text{CL}$	$0.214 + 0.088 \cdot \text{CL}$	$0.209 + 0.088 \cdot \text{CL}$
	$t_{PLH}$	3.371	$1.552 + 0.036 \cdot \text{CL}$	$1.556 + 0.036 \cdot \text{CL}$	$1.557 + 0.036 \cdot \text{CL}$
	$t_{PHL}$	3.527	$1.243 + 0.046 \cdot \text{CL}$	$1.245 + 0.046 \cdot \text{CL}$	$1.247 + 0.046 \cdot \text{CL}$
	$t_{PLZ}$	1.238	$1.238 + 0.000 \cdot \text{CL}$	$1.238 + 0.000 \cdot \text{CL}$	$1.238 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.439	$1.439 + 0.000 \cdot \text{CL}$	$1.439 + 0.000 \cdot \text{CL}$	$1.439 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POT10**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	3.219	$0.240 + 0.060 \cdot \text{CL}$	$0.210 + 0.060 \cdot \text{CL}$	$0.190 + 0.060 \cdot \text{CL}$
	$t_F$	3.669	$0.176 + 0.070 \cdot \text{CL}$	$0.166 + 0.070 \cdot \text{CL}$	$0.164 + 0.070 \cdot \text{CL}$
	$t_{PLH}$	2.653	$1.200 + 0.029 \cdot \text{CL}$	$1.201 + 0.029 \cdot \text{CL}$	$1.202 + 0.029 \cdot \text{CL}$
	$t_{PHL}$	2.807	$0.985 + 0.036 \cdot \text{CL}$	$0.984 + 0.036 \cdot \text{CL}$	$0.983 + 0.036 \cdot \text{CL}$
TN to PAD	$t_R$	3.218	$0.240 + 0.060 \cdot \text{CL}$	$0.209 + 0.060 \cdot \text{CL}$	$0.191 + 0.060 \cdot \text{CL}$
	$t_F$	3.668	$0.174 + 0.070 \cdot \text{CL}$	$0.166 + 0.070 \cdot \text{CL}$	$0.163 + 0.070 \cdot \text{CL}$
	$t_{PLH}$	2.704	$1.250 + 0.029 \cdot \text{CL}$	$1.253 + 0.029 \cdot \text{CL}$	$1.253 + 0.029 \cdot \text{CL}$
	$t_{PHL}$	2.925	$1.097 + 0.037 \cdot \text{CL}$	$1.099 + 0.037 \cdot \text{CL}$	$1.100 + 0.036 \cdot \text{CL}$
	$t_{PLZ}$	1.095	$1.095 + 0.000 \cdot \text{CL}$	$1.095 + 0.000 \cdot \text{CL}$	$1.095 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.144	$1.144 + 0.000 \cdot \text{CL}$	$1.143 + 0.000 \cdot \text{CL}$	$1.144 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	3.218	$0.240 + 0.060 \cdot \text{CL}$	$0.209 + 0.060 \cdot \text{CL}$	$0.191 + 0.060 \cdot \text{CL}$
	$t_F$	3.668	$0.174 + 0.070 \cdot \text{CL}$	$0.166 + 0.070 \cdot \text{CL}$	$0.163 + 0.070 \cdot \text{CL}$
	$t_{PLH}$	2.807	$1.354 + 0.029 \cdot \text{CL}$	$1.355 + 0.029 \cdot \text{CL}$	$1.356 + 0.029 \cdot \text{CL}$
	$t_{PHL}$	3.027	$1.201 + 0.037 \cdot \text{CL}$	$1.202 + 0.036 \cdot \text{CL}$	$1.203 + 0.036 \cdot \text{CL}$
	$t_{PLZ}$	1.138	$1.138 + 0.000 \cdot \text{CL}$	$1.138 + 0.000 \cdot \text{CL}$	$1.138 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.186	$1.185 + 0.000 \cdot \text{CL}$	$1.186 + 0.000 \cdot \text{CL}$	$1.186 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOTyz

## Tri-State Output Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### POT12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	2.721	$0.269 + 0.049 \cdot \text{CL}$	$0.232 + 0.050 \cdot \text{CL}$	$0.204 + 0.050 \cdot \text{CL}$
	$t_F$	3.069	$0.169 + 0.058 \cdot \text{CL}$	$0.155 + 0.058 \cdot \text{CL}$	$0.148 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	2.497	$1.281 + 0.024 \cdot \text{CL}$	$1.286 + 0.024 \cdot \text{CL}$	$1.287 + 0.024 \cdot \text{CL}$
	$t_{PHL}$	2.531	$1.016 + 0.030 \cdot \text{CL}$	$1.014 + 0.030 \cdot \text{CL}$	$1.012 + 0.030 \cdot \text{CL}$
TN to PAD	$t_R$	2.721	$0.269 + 0.049 \cdot \text{CL}$	$0.232 + 0.050 \cdot \text{CL}$	$0.204 + 0.050 \cdot \text{CL}$
	$t_F$	3.069	$0.167 + 0.058 \cdot \text{CL}$	$0.154 + 0.058 \cdot \text{CL}$	$0.147 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	2.548	$1.332 + 0.024 \cdot \text{CL}$	$1.338 + 0.024 \cdot \text{CL}$	$1.339 + 0.024 \cdot \text{CL}$
	$t_{PHL}$	2.646	$1.122 + 0.030 \cdot \text{CL}$	$1.125 + 0.030 \cdot \text{CL}$	$1.126 + 0.030 \cdot \text{CL}$
	$t_{PLZ}$	1.160	$1.160 + 0.000 \cdot \text{CL}$	$1.160 + 0.000 \cdot \text{CL}$	$1.160 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.248	$1.248 + 0.000 \cdot \text{CL}$	$1.248 + 0.000 \cdot \text{CL}$	$1.248 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	2.721	$0.269 + 0.049 \cdot \text{CL}$	$0.232 + 0.050 \cdot \text{CL}$	$0.204 + 0.050 \cdot \text{CL}$
	$t_F$	3.069	$0.167 + 0.058 \cdot \text{CL}$	$0.154 + 0.058 \cdot \text{CL}$	$0.147 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	2.651	$1.435 + 0.024 \cdot \text{CL}$	$1.440 + 0.024 \cdot \text{CL}$	$1.442 + 0.024 \cdot \text{CL}$
	$t_{PHL}$	2.749	$1.225 + 0.030 \cdot \text{CL}$	$1.228 + 0.030 \cdot \text{CL}$	$1.229 + 0.030 \cdot \text{CL}$
	$t_{PLZ}$	1.203	$1.203 + 0.000 \cdot \text{CL}$	$1.203 + 0.000 \cdot \text{CL}$	$1.203 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.290	$1.290 + 0.000 \cdot \text{CL}$	$1.290 + 0.000 \cdot \text{CL}$	$1.290 + 0.000 \cdot \text{CL}$

\*Group1 :  $\text{CL} < 50$ , \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**POT4SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	8.136	$0.756 + 0.148 \cdot \text{CL}$	$0.663 + 0.149 \cdot \text{CL}$	$0.590 + 0.150 \cdot \text{CL}$
	$t_F$	9.485	$1.005 + 0.170 \cdot \text{CL}$	$0.893 + 0.172 \cdot \text{CL}$	$0.791 + 0.173 \cdot \text{CL}$
	$t_{PLH}$	5.943	$2.288 + 0.073 \cdot \text{CL}$	$2.310 + 0.073 \cdot \text{CL}$	$2.315 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	7.625	$2.988 + 0.093 \cdot \text{CL}$	$3.050 + 0.092 \cdot \text{CL}$	$3.069 + 0.091 \cdot \text{CL}$
TN to PAD	$t_R$	8.136	$0.756 + 0.148 \cdot \text{CL}$	$0.663 + 0.149 \cdot \text{CL}$	$0.590 + 0.150 \cdot \text{CL}$
	$t_F$	9.485	$1.005 + 0.170 \cdot \text{CL}$	$0.893 + 0.172 \cdot \text{CL}$	$0.791 + 0.173 \cdot \text{CL}$
	$t_{PLH}$	5.992	$2.336 + 0.073 \cdot \text{CL}$	$2.358 + 0.073 \cdot \text{CL}$	$2.364 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	7.747	$3.110 + 0.093 \cdot \text{CL}$	$3.171 + 0.092 \cdot \text{CL}$	$3.189 + 0.091 \cdot \text{CL}$
	$t_{PLZ}$	1.169	$1.169 + 0.000 \cdot \text{CL}$	$1.169 + 0.000 \cdot \text{CL}$	$1.169 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.521	$1.521 + 0.000 \cdot \text{CL}$	$1.521 + 0.000 \cdot \text{CL}$	$1.521 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	8.136	$0.756 + 0.148 \cdot \text{CL}$	$0.663 + 0.149 \cdot \text{CL}$	$0.590 + 0.150 \cdot \text{CL}$
	$t_F$	9.485	$1.005 + 0.170 \cdot \text{CL}$	$0.893 + 0.172 \cdot \text{CL}$	$0.791 + 0.173 \cdot \text{CL}$
	$t_{PLH}$	6.094	$2.439 + 0.073 \cdot \text{CL}$	$2.461 + 0.073 \cdot \text{CL}$	$2.466 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	7.850	$3.213 + 0.093 \cdot \text{CL}$	$3.275 + 0.091 \cdot \text{CL}$	$3.291 + 0.091 \cdot \text{CL}$
	$t_{PLZ}$	1.212	$1.212 + 0.000 \cdot \text{CL}$	$1.212 + 0.000 \cdot \text{CL}$	$1.212 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.563	$1.563 + 0.000 \cdot \text{CL}$	$1.563 + 0.000 \cdot \text{CL}$	$1.563 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **POT6SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	6.049	$1.312 + 0.095 \cdot \text{CL}$	$1.251 + 0.096 \cdot \text{CL}$	$1.155 + 0.097 \cdot \text{CL}$
	$t_F$	6.982	$1.450 + 0.111 \cdot \text{CL}$	$1.413 + 0.111 \cdot \text{CL}$	$1.321 + 0.113 \cdot \text{CL}$
	$t_{PLH}$	5.589	$2.881 + 0.054 \cdot \text{CL}$	$3.063 + 0.051 \cdot \text{CL}$	$3.165 + 0.049 \cdot \text{CL}$
	$t_{PHL}$	6.936	$3.524 + 0.068 \cdot \text{CL}$	$3.747 + 0.064 \cdot \text{CL}$	$3.882 + 0.062 \cdot \text{CL}$
TN to PAD	$t_R$	6.049	$1.312 + 0.095 \cdot \text{CL}$	$1.252 + 0.096 \cdot \text{CL}$	$1.155 + 0.097 \cdot \text{CL}$
	$t_F$	6.982	$1.451 + 0.111 \cdot \text{CL}$	$1.414 + 0.111 \cdot \text{CL}$	$1.322 + 0.113 \cdot \text{CL}$
	$t_{PLH}$	5.638	$2.930 + 0.054 \cdot \text{CL}$	$3.112 + 0.051 \cdot \text{CL}$	$3.214 + 0.049 \cdot \text{CL}$
	$t_{PHL}$	7.057	$3.645 + 0.068 \cdot \text{CL}$	$3.868 + 0.064 \cdot \text{CL}$	$4.002 + 0.062 \cdot \text{CL}$
	$t_{PLZ}$	1.448	$1.448 + 0.000 \cdot \text{CL}$	$1.448 + 0.000 \cdot \text{CL}$	$1.448 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.401	$2.401 + 0.000 \cdot \text{CL}$	$2.401 + 0.000 \cdot \text{CL}$	$2.400 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	6.049	$1.312 + 0.095 \cdot \text{CL}$	$1.252 + 0.096 \cdot \text{CL}$	$1.155 + 0.097 \cdot \text{CL}$
	$t_F$	6.982	$1.451 + 0.111 \cdot \text{CL}$	$1.414 + 0.111 \cdot \text{CL}$	$1.322 + 0.113 \cdot \text{CL}$
	$t_{PLH}$	5.740	$3.034 + 0.054 \cdot \text{CL}$	$3.215 + 0.051 \cdot \text{CL}$	$3.316 + 0.049 \cdot \text{CL}$
	$t_{PHL}$	7.160	$3.748 + 0.068 \cdot \text{CL}$	$3.971 + 0.064 \cdot \text{CL}$	$4.106 + 0.062 \cdot \text{CL}$
	$t_{PLZ}$	1.491	$1.491 + 0.000 \cdot \text{CL}$	$1.491 + 0.000 \cdot \text{CL}$	$1.491 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.443	$2.442 + 0.000 \cdot \text{CL}$	$2.443 + 0.000 \cdot \text{CL}$	$2.443 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOTyz

## Tri-State Output Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### POT8SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.157	$1.658 + 0.070 \cdot \text{CL}$	$1.671 + 0.070 \cdot \text{CL}$	$1.601 + 0.071 \cdot \text{CL}$
	$t_F$	5.712	$1.575 + 0.083 \cdot \text{CL}$	$1.605 + 0.082 \cdot \text{CL}$	$1.549 + 0.083 \cdot \text{CL}$
	$t_{PLH}$	5.234	$2.895 + 0.047 \cdot \text{CL}$	$3.178 + 0.041 \cdot \text{CL}$	$3.371 + 0.039 \cdot \text{CL}$
	$t_{PHL}$	6.241	$3.455 + 0.056 \cdot \text{CL}$	$3.724 + 0.050 \cdot \text{CL}$	$3.913 + 0.048 \cdot \text{CL}$
TN to PAD	$t_R$	5.158	$1.661 + 0.070 \cdot \text{CL}$	$1.673 + 0.070 \cdot \text{CL}$	$1.602 + 0.071 \cdot \text{CL}$
	$t_F$	5.723	$1.615 + 0.082 \cdot \text{CL}$	$1.625 + 0.082 \cdot \text{CL}$	$1.561 + 0.083 \cdot \text{CL}$
	$t_{PLH}$	5.282	$2.942 + 0.047 \cdot \text{CL}$	$3.226 + 0.041 \cdot \text{CL}$	$3.419 + 0.039 \cdot \text{CL}$
	$t_{PHL}$	6.351	$3.546 + 0.056 \cdot \text{CL}$	$3.827 + 0.050 \cdot \text{CL}$	$4.021 + 0.048 \cdot \text{CL}$
	$t_{PLZ}$	2.053	$2.053 + 0.000 \cdot \text{CL}$	$2.053 + 0.000 \cdot \text{CL}$	$2.053 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	3.255	$3.255 + 0.000 \cdot \text{CL}$	$3.255 + 0.000 \cdot \text{CL}$	$3.255 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	5.158	$1.661 + 0.070 \cdot \text{CL}$	$1.673 + 0.070 \cdot \text{CL}$	$1.602 + 0.071 \cdot \text{CL}$
	$t_F$	5.723	$1.615 + 0.082 \cdot \text{CL}$	$1.625 + 0.082 \cdot \text{CL}$	$1.561 + 0.083 \cdot \text{CL}$
	$t_{PLH}$	5.385	$3.046 + 0.047 \cdot \text{CL}$	$3.329 + 0.041 \cdot \text{CL}$	$3.522 + 0.039 \cdot \text{CL}$
	$t_{PHL}$	6.454	$3.649 + 0.056 \cdot \text{CL}$	$3.930 + 0.050 \cdot \text{CL}$	$4.125 + 0.048 \cdot \text{CL}$
	$t_{PLZ}$	2.096	$2.096 + 0.000 \cdot \text{CL}$	$2.096 + 0.000 \cdot \text{CL}$	$2.096 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	3.297	$3.297 + 0.000 \cdot \text{CL}$	$3.297 + 0.000 \cdot \text{CL}$	$3.297 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POT10SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.208	$1.327 + 0.058 \cdot \text{CL}$	$1.366 + 0.057 \cdot \text{CL}$	$1.346 + 0.057 \cdot \text{CL}$
	$t_F$	4.733	$1.366 + 0.067 \cdot \text{CL}$	$1.422 + 0.066 \cdot \text{CL}$	$1.407 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	4.875	$2.962 + 0.038 \cdot \text{CL}$	$3.187 + 0.034 \cdot \text{CL}$	$3.355 + 0.032 \cdot \text{CL}$
	$t_{PHL}$	5.800	$3.480 + 0.046 \cdot \text{CL}$	$3.724 + 0.042 \cdot \text{CL}$	$3.905 + 0.039 \cdot \text{CL}$
TN to PAD	$t_R$	4.208	$1.327 + 0.058 \cdot \text{CL}$	$1.366 + 0.057 \cdot \text{CL}$	$1.346 + 0.057 \cdot \text{CL}$
	$t_F$	4.736	$1.381 + 0.067 \cdot \text{CL}$	$1.430 + 0.066 \cdot \text{CL}$	$1.412 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	4.924	$3.012 + 0.038 \cdot \text{CL}$	$3.236 + 0.034 \cdot \text{CL}$	$3.404 + 0.032 \cdot \text{CL}$
	$t_{PHL}$	5.917	$3.591 + 0.047 \cdot \text{CL}$	$3.839 + 0.042 \cdot \text{CL}$	$4.023 + 0.039 \cdot \text{CL}$
	$t_{PLZ}$	2.053	$2.053 + 0.000 \cdot \text{CL}$	$2.053 + 0.000 \cdot \text{CL}$	$2.053 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	3.255	$3.254 + 0.000 \cdot \text{CL}$	$3.255 + 0.000 \cdot \text{CL}$	$3.255 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	4.208	$1.327 + 0.058 \cdot \text{CL}$	$1.366 + 0.057 \cdot \text{CL}$	$1.346 + 0.057 \cdot \text{CL}$
	$t_F$	4.736	$1.381 + 0.067 \cdot \text{CL}$	$1.430 + 0.066 \cdot \text{CL}$	$1.412 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	5.027	$3.115 + 0.038 \cdot \text{CL}$	$3.339 + 0.034 \cdot \text{CL}$	$3.507 + 0.032 \cdot \text{CL}$
	$t_{PHL}$	6.020	$3.694 + 0.047 \cdot \text{CL}$	$3.942 + 0.042 \cdot \text{CL}$	$4.126 + 0.039 \cdot \text{CL}$
	$t_{PLZ}$	2.095	$2.096 + 0.000 \cdot \text{CL}$	$2.095 + 0.000 \cdot \text{CL}$	$2.095 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	3.297	$3.297 + 0.000 \cdot \text{CL}$	$3.297 + 0.000 \cdot \text{CL}$	$3.297 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**POT12SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.196	$1.635 + 0.051 \cdot \text{CL}$	$1.781 + 0.048 \cdot \text{CL}$	$1.853 + 0.047 \cdot \text{CL}$
	$t_F$	4.558	$1.568 + 0.060 \cdot \text{CL}$	$1.742 + 0.056 \cdot \text{CL}$	$1.824 + 0.055 \cdot \text{CL}$
	$t_{PLH}$	5.110	$3.154 + 0.039 \cdot \text{CL}$	$3.458 + 0.033 \cdot \text{CL}$	$3.713 + 0.030 \cdot \text{CL}$
	$t_{PHL}$	5.995	$3.754 + 0.045 \cdot \text{CL}$	$4.049 + 0.039 \cdot \text{CL}$	$4.298 + 0.036 \cdot \text{CL}$
TN to PAD	$t_R$	4.196	$1.637 + 0.051 \cdot \text{CL}$	$1.781 + 0.048 \cdot \text{CL}$	$1.854 + 0.047 \cdot \text{CL}$
	$t_F$	4.583	$1.655 + 0.059 \cdot \text{CL}$	$1.791 + 0.056 \cdot \text{CL}$	$1.853 + 0.055 \cdot \text{CL}$
	$t_{PLH}$	5.159	$3.203 + 0.039 \cdot \text{CL}$	$3.507 + 0.033 \cdot \text{CL}$	$3.763 + 0.030 \cdot \text{CL}$
	$t_{PHL}$	6.095	$3.815 + 0.046 \cdot \text{CL}$	$4.134 + 0.039 \cdot \text{CL}$	$4.395 + 0.036 \cdot \text{CL}$
	$t_{PLZ}$	2.421	$2.421 + 0.000 \cdot \text{CL}$	$2.421 + 0.000 \cdot \text{CL}$	$2.421 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	4.133	$4.133 + 0.000 \cdot \text{CL}$	$4.133 + 0.000 \cdot \text{CL}$	$4.133 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	4.196	$1.637 + 0.051 \cdot \text{CL}$	$1.782 + 0.048 \cdot \text{CL}$	$1.854 + 0.047 \cdot \text{CL}$
	$t_F$	4.583	$1.655 + 0.059 \cdot \text{CL}$	$1.790 + 0.056 \cdot \text{CL}$	$1.854 + 0.055 \cdot \text{CL}$
	$t_{PLH}$	5.261	$3.307 + 0.039 \cdot \text{CL}$	$3.610 + 0.033 \cdot \text{CL}$	$3.865 + 0.030 \cdot \text{CL}$
	$t_{PHL}$	6.197	$3.918 + 0.046 \cdot \text{CL}$	$4.236 + 0.039 \cdot \text{CL}$	$4.498 + 0.036 \cdot \text{CL}$
	$t_{PLZ}$	2.464	$2.464 + 0.000 \cdot \text{CL}$	$2.464 + 0.000 \cdot \text{CL}$	$2.464 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	4.175	$4.175 + 0.000 \cdot \text{CL}$	$4.175 + 0.000 \cdot \text{CL}$	$4.175 + 0.000 \cdot \text{CL}$

\*Group1 :  $\text{CL} < 50$ , \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOTyz

## Tri-State Output Buffers

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

#### POT10SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	6.218	$2.940 + 0.066 \cdot \text{CL}$	$3.224 + 0.060 \cdot \text{CL}$	$3.412 + 0.057 \cdot \text{CL}$
	$t_F$	6.448	$2.737 + 0.074 \cdot \text{CL}$	$3.005 + 0.069 \cdot \text{CL}$	$3.175 + 0.067 \cdot \text{CL}$
	$t_{PLH}$	7.876	$4.948 + 0.059 \cdot \text{CL}$	$5.499 + 0.048 \cdot \text{CL}$	$5.966 + 0.041 \cdot \text{CL}$
	$t_{PHL}$	8.633	$5.417 + 0.064 \cdot \text{CL}$	$5.943 + 0.054 \cdot \text{CL}$	$6.389 + 0.048 \cdot \text{CL}$
TN to PAD	$t_R$	6.219	$2.942 + 0.066 \cdot \text{CL}$	$3.225 + 0.060 \cdot \text{CL}$	$3.414 + 0.057 \cdot \text{CL}$
	$t_F$	6.460	$2.782 + 0.074 \cdot \text{CL}$	$3.029 + 0.069 \cdot \text{CL}$	$3.189 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	7.929	$5.001 + 0.059 \cdot \text{CL}$	$5.553 + 0.048 \cdot \text{CL}$	$6.019 + 0.041 \cdot \text{CL}$
	$t_{PHL}$	8.748	$5.516 + 0.065 \cdot \text{CL}$	$6.051 + 0.054 \cdot \text{CL}$	$6.505 + 0.048 \cdot \text{CL}$
	$t_{PLZ}$	2.532	$2.532 + 0.000 \cdot \text{CL}$	$2.532 + 0.000 \cdot \text{CL}$	$2.532 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	4.231	$4.230 + 0.000 \cdot \text{CL}$	$4.231 + 0.000 \cdot \text{CL}$	$4.231 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	6.219	$2.942 + 0.066 \cdot \text{CL}$	$3.226 + 0.060 \cdot \text{CL}$	$3.413 + 0.057 \cdot \text{CL}$
	$t_F$	6.460	$2.782 + 0.074 \cdot \text{CL}$	$3.029 + 0.069 \cdot \text{CL}$	$3.189 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	8.031	$5.105 + 0.059 \cdot \text{CL}$	$5.655 + 0.048 \cdot \text{CL}$	$6.122 + 0.041 \cdot \text{CL}$
	$t_{PHL}$	8.850	$5.620 + 0.065 \cdot \text{CL}$	$6.155 + 0.054 \cdot \text{CL}$	$6.607 + 0.048 \cdot \text{CL}$
	$t_{PLZ}$	2.575	$2.575 + 0.000 \cdot \text{CL}$	$2.575 + 0.000 \cdot \text{CL}$	$2.575 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	4.273	$4.272 + 0.000 \cdot \text{CL}$	$4.273 + 0.000 \cdot \text{CL}$	$4.273 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### POT12SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	6.593	$3.555 + 0.061 \cdot \text{CL}$	$3.937 + 0.053 \cdot \text{CL}$	$4.211 + 0.049 \cdot \text{CL}$
	$t_F$	6.548	$3.126 + 0.068 \cdot \text{CL}$	$3.509 + 0.061 \cdot \text{CL}$	$3.773 + 0.057 \cdot \text{CL}$
	$t_{PLH}$	8.385	$5.248 + 0.063 \cdot \text{CL}$	$5.928 + 0.049 \cdot \text{CL}$	$6.505 + 0.041 \cdot \text{CL}$
	$t_{PHL}$	9.094	$5.840 + 0.065 \cdot \text{CL}$	$6.443 + 0.053 \cdot \text{CL}$	$6.966 + 0.046 \cdot \text{CL}$
TN to PAD	$t_R$	6.596	$3.560 + 0.061 \cdot \text{CL}$	$3.941 + 0.053 \cdot \text{CL}$	$4.213 + 0.049 \cdot \text{CL}$
	$t_F$	6.599	$3.299 + 0.066 \cdot \text{CL}$	$3.606 + 0.060 \cdot \text{CL}$	$3.832 + 0.057 \cdot \text{CL}$
	$t_{PLH}$	8.439	$5.302 + 0.063 \cdot \text{CL}$	$5.982 + 0.049 \cdot \text{CL}$	$6.558 + 0.041 \cdot \text{CL}$
	$t_{PHL}$	9.189	$5.880 + 0.066 \cdot \text{CL}$	$6.518 + 0.053 \cdot \text{CL}$	$7.056 + 0.046 \cdot \text{CL}$
	$t_{PLZ}$	2.900	$2.900 + 0.000 \cdot \text{CL}$	$2.900 + 0.000 \cdot \text{CL}$	$2.900 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	5.109	$5.108 + 0.000 \cdot \text{CL}$	$5.109 + 0.000 \cdot \text{CL}$	$5.109 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	6.596	$3.560 + 0.061 \cdot \text{CL}$	$3.941 + 0.053 \cdot \text{CL}$	$4.214 + 0.049 \cdot \text{CL}$
	$t_F$	6.599	$3.299 + 0.066 \cdot \text{CL}$	$3.606 + 0.060 \cdot \text{CL}$	$3.832 + 0.057 \cdot \text{CL}$
	$t_{PLH}$	8.541	$5.405 + 0.063 \cdot \text{CL}$	$6.085 + 0.049 \cdot \text{CL}$	$6.661 + 0.041 \cdot \text{CL}$
	$t_{PHL}$	9.291	$5.983 + 0.066 \cdot \text{CL}$	$6.620 + 0.053 \cdot \text{CL}$	$7.159 + 0.046 \cdot \text{CL}$
	$t_{PLZ}$	2.943	$2.943 + 0.000 \cdot \text{CL}$	$2.943 + 0.000 \cdot \text{CL}$	$2.943 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	5.151	$5.150 + 0.000 \cdot \text{CL}$	$5.150 + 0.000 \cdot \text{CL}$	$5.151 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PHOT1**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	42.148	$1.623 + 0.811 \cdot \text{CL}$	$1.624 + 0.810 \cdot \text{CL}$	$1.621 + 0.811 \cdot \text{CL}$
	$t_F$	33.014	$1.269 + 0.635 \cdot \text{CL}$	$1.270 + 0.635 \cdot \text{CL}$	$1.267 + 0.635 \cdot \text{CL}$
	$t_{PLH}$	20.296	$1.549 + 0.375 \cdot \text{CL}$	$1.548 + 0.375 \cdot \text{CL}$	$1.548 + 0.375 \cdot \text{CL}$
	$t_{PHL}$	17.148	$1.586 + 0.311 \cdot \text{CL}$	$1.584 + 0.311 \cdot \text{CL}$	$1.581 + 0.311 \cdot \text{CL}$
TN to PAD	$t_R$	42.146	$1.623 + 0.810 \cdot \text{CL}$	$1.620 + 0.811 \cdot \text{CL}$	$1.623 + 0.810 \cdot \text{CL}$
	$t_F$	33.014	$1.269 + 0.635 \cdot \text{CL}$	$1.270 + 0.635 \cdot \text{CL}$	$1.267 + 0.635 \cdot \text{CL}$
	$t_{PLH}$	20.383	$1.633 + 0.375 \cdot \text{CL}$	$1.635 + 0.375 \cdot \text{CL}$	$1.635 + 0.375 \cdot \text{CL}$
	$t_{PHL}$	17.350	$1.785 + 0.311 \cdot \text{CL}$	$1.786 + 0.311 \cdot \text{CL}$	$1.783 + 0.311 \cdot \text{CL}$
	$t_{PLZ}$	1.249	$1.249 + 0.000 \cdot \text{CL}$	$1.249 + 0.000 \cdot \text{CL}$	$1.249 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.951	$0.951 + 0.000 \cdot \text{CL}$	$0.951 + 0.000 \cdot \text{CL}$	$0.951 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	42.146	$1.623 + 0.810 \cdot \text{CL}$	$1.620 + 0.811 \cdot \text{CL}$	$1.623 + 0.810 \cdot \text{CL}$
	$t_F$	33.014	$1.269 + 0.635 \cdot \text{CL}$	$1.270 + 0.635 \cdot \text{CL}$	$1.267 + 0.635 \cdot \text{CL}$
	$t_{PLH}$	20.485	$1.738 + 0.375 \cdot \text{CL}$	$1.737 + 0.375 \cdot \text{CL}$	$1.737 + 0.375 \cdot \text{CL}$
	$t_{PHL}$	17.453	$1.888 + 0.311 \cdot \text{CL}$	$1.889 + 0.311 \cdot \text{CL}$	$1.889 + 0.311 \cdot \text{CL}$
	$t_{PLZ}$	1.292	$1.292 + 0.000 \cdot \text{CL}$	$1.292 + 0.000 \cdot \text{CL}$	$1.292 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.995	$0.995 + 0.000 \cdot \text{CL}$	$0.995 + 0.000 \cdot \text{CL}$	$0.995 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOT2**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	21.098	$0.836 + 0.405 \cdot \text{CL}$	$0.836 + 0.405 \cdot \text{CL}$	$0.833 + 0.405 \cdot \text{CL}$
	$t_F$	18.188	$0.706 + 0.350 \cdot \text{CL}$	$0.702 + 0.350 \cdot \text{CL}$	$0.705 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	10.592	$1.218 + 0.187 \cdot \text{CL}$	$1.218 + 0.187 \cdot \text{CL}$	$1.218 + 0.187 \cdot \text{CL}$
	$t_{PHL}$	10.105	$1.209 + 0.178 \cdot \text{CL}$	$1.211 + 0.178 \cdot \text{CL}$	$1.208 + 0.178 \cdot \text{CL}$
TN to PAD	$t_R$	21.098	$0.836 + 0.405 \cdot \text{CL}$	$0.836 + 0.405 \cdot \text{CL}$	$0.833 + 0.405 \cdot \text{CL}$
	$t_F$	18.188	$0.706 + 0.350 \cdot \text{CL}$	$0.702 + 0.350 \cdot \text{CL}$	$0.705 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	10.678	$1.304 + 0.187 \cdot \text{CL}$	$1.304 + 0.187 \cdot \text{CL}$	$1.304 + 0.187 \cdot \text{CL}$
	$t_{PHL}$	10.306	$1.411 + 0.178 \cdot \text{CL}$	$1.410 + 0.178 \cdot \text{CL}$	$1.410 + 0.178 \cdot \text{CL}$
	$t_{PLZ}$	1.104	$1.104 + 0.000 \cdot \text{CL}$	$1.104 + 0.000 \cdot \text{CL}$	$1.104 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.998	$0.998 + 0.000 \cdot \text{CL}$	$0.998 + 0.000 \cdot \text{CL}$	$0.998 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	21.098	$0.836 + 0.405 \cdot \text{CL}$	$0.836 + 0.405 \cdot \text{CL}$	$0.833 + 0.405 \cdot \text{CL}$
	$t_F$	18.188	$0.706 + 0.350 \cdot \text{CL}$	$0.702 + 0.350 \cdot \text{CL}$	$0.705 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	10.781	$1.406 + 0.187 \cdot \text{CL}$	$1.407 + 0.187 \cdot \text{CL}$	$1.410 + 0.187 \cdot \text{CL}$
	$t_{PHL}$	10.409	$1.513 + 0.178 \cdot \text{CL}$	$1.513 + 0.178 \cdot \text{CL}$	$1.516 + 0.178 \cdot \text{CL}$
	$t_{PLZ}$	1.149	$1.149 + 0.000 \cdot \text{CL}$	$1.149 + 0.000 \cdot \text{CL}$	$1.149 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.042	$1.042 + 0.000 \cdot \text{CL}$	$1.042 + 0.000 \cdot \text{CL}$	$1.042 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOTyz

## Tri-State Output Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

### PHOT4

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	10.563	$0.433 + 0.203 \cdot \text{CL}$	$0.431 + 0.203 \cdot \text{CL}$	$0.431 + 0.203 \cdot \text{CL}$
	$t_F$	9.114	$0.371 + 0.175 \cdot \text{CL}$	$0.371 + 0.175 \cdot \text{CL}$	$0.372 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	5.815	$1.128 + 0.094 \cdot \text{CL}$	$1.128 + 0.094 \cdot \text{CL}$	$1.128 + 0.094 \cdot \text{CL}$
	$t_{PHL}$	5.544	$1.096 + 0.089 \cdot \text{CL}$	$1.096 + 0.089 \cdot \text{CL}$	$1.096 + 0.089 \cdot \text{CL}$
TN to PAD	$t_R$	10.563	$0.433 + 0.203 \cdot \text{CL}$	$0.431 + 0.203 \cdot \text{CL}$	$0.431 + 0.203 \cdot \text{CL}$
	$t_F$	9.114	$0.371 + 0.175 \cdot \text{CL}$	$0.371 + 0.175 \cdot \text{CL}$	$0.372 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	5.901	$1.213 + 0.094 \cdot \text{CL}$	$1.214 + 0.094 \cdot \text{CL}$	$1.215 + 0.094 \cdot \text{CL}$
	$t_{PHL}$	5.746	$1.297 + 0.089 \cdot \text{CL}$	$1.297 + 0.089 \cdot \text{CL}$	$1.298 + 0.089 \cdot \text{CL}$
	$t_{PLZ}$	1.255	$1.256 + 0.000 \cdot \text{CL}$	$1.255 + 0.000 \cdot \text{CL}$	$1.255 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.091	$1.091 + 0.000 \cdot \text{CL}$	$1.091 + 0.000 \cdot \text{CL}$	$1.091 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	10.563	$0.433 + 0.203 \cdot \text{CL}$	$0.431 + 0.203 \cdot \text{CL}$	$0.431 + 0.203 \cdot \text{CL}$
	$t_F$	9.114	$0.371 + 0.175 \cdot \text{CL}$	$0.371 + 0.175 \cdot \text{CL}$	$0.372 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	6.003	$1.316 + 0.094 \cdot \text{CL}$	$1.317 + 0.094 \cdot \text{CL}$	$1.318 + 0.094 \cdot \text{CL}$
	$t_{PHL}$	5.848	$1.400 + 0.089 \cdot \text{CL}$	$1.401 + 0.089 \cdot \text{CL}$	$1.401 + 0.089 \cdot \text{CL}$
	$t_{PLZ}$	1.300	$1.300 + 0.000 \cdot \text{CL}$	$1.300 + 0.000 \cdot \text{CL}$	$1.300 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.135	$1.135 + 0.000 \cdot \text{CL}$	$1.135 + 0.000 \cdot \text{CL}$	$1.135 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOT6

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	7.047	$0.293 + 0.135 \cdot \text{CL}$	$0.294 + 0.135 \cdot \text{CL}$	$0.293 + 0.135 \cdot \text{CL}$
	$t_F$	6.082	$0.254 + 0.117 \cdot \text{CL}$	$0.254 + 0.117 \cdot \text{CL}$	$0.255 + 0.117 \cdot \text{CL}$
	$t_{PLH}$	4.212	$1.087 + 0.063 \cdot \text{CL}$	$1.087 + 0.062 \cdot \text{CL}$	$1.087 + 0.062 \cdot \text{CL}$
	$t_{PHL}$	4.022	$1.057 + 0.059 \cdot \text{CL}$	$1.057 + 0.059 \cdot \text{CL}$	$1.057 + 0.059 \cdot \text{CL}$
TN to PAD	$t_R$	7.047	$0.293 + 0.135 \cdot \text{CL}$	$0.294 + 0.135 \cdot \text{CL}$	$0.293 + 0.135 \cdot \text{CL}$
	$t_F$	6.082	$0.254 + 0.117 \cdot \text{CL}$	$0.254 + 0.117 \cdot \text{CL}$	$0.255 + 0.117 \cdot \text{CL}$
	$t_{PLH}$	4.298	$1.172 + 0.063 \cdot \text{CL}$	$1.173 + 0.063 \cdot \text{CL}$	$1.173 + 0.063 \cdot \text{CL}$
	$t_{PHL}$	4.223	$1.256 + 0.059 \cdot \text{CL}$	$1.257 + 0.059 \cdot \text{CL}$	$1.257 + 0.059 \cdot \text{CL}$
	$t_{PLZ}$	1.246	$1.246 + 0.000 \cdot \text{CL}$	$1.246 + 0.000 \cdot \text{CL}$	$1.246 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.094	$1.094 + 0.000 \cdot \text{CL}$	$1.094 + 0.000 \cdot \text{CL}$	$1.094 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	7.047	$0.293 + 0.135 \cdot \text{CL}$	$0.294 + 0.135 \cdot \text{CL}$	$0.293 + 0.135 \cdot \text{CL}$
	$t_F$	6.082	$0.254 + 0.117 \cdot \text{CL}$	$0.254 + 0.117 \cdot \text{CL}$	$0.255 + 0.117 \cdot \text{CL}$
	$t_{PLH}$	4.400	$1.275 + 0.063 \cdot \text{CL}$	$1.276 + 0.062 \cdot \text{CL}$	$1.276 + 0.062 \cdot \text{CL}$
	$t_{PHL}$	4.325	$1.359 + 0.059 \cdot \text{CL}$	$1.360 + 0.059 \cdot \text{CL}$	$1.359 + 0.059 \cdot \text{CL}$
	$t_{PLZ}$	1.289	$1.290 + 0.000 \cdot \text{CL}$	$1.289 + 0.000 \cdot \text{CL}$	$1.289 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.137	$1.137 + 0.000 \cdot \text{CL}$	$1.137 + 0.000 \cdot \text{CL}$	$1.137 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PHOT8**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.293	$0.229 + 0.101 \cdot \text{CL}$	$0.228 + 0.101 \cdot \text{CL}$	$0.227 + 0.101 \cdot \text{CL}$
	$t_F$	4.572	$0.205 + 0.087 \cdot \text{CL}$	$0.202 + 0.087 \cdot \text{CL}$	$0.201 + 0.087 \cdot \text{CL}$
	$t_{PLH}$	3.444	$1.100 + 0.047 \cdot \text{CL}$	$1.101 + 0.047 \cdot \text{CL}$	$1.101 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	3.289	$1.064 + 0.044 \cdot \text{CL}$	$1.065 + 0.044 \cdot \text{CL}$	$1.065 + 0.044 \cdot \text{CL}$
TN to PAD	$t_R$	5.293	$0.229 + 0.101 \cdot \text{CL}$	$0.228 + 0.101 \cdot \text{CL}$	$0.227 + 0.101 \cdot \text{CL}$
	$t_F$	4.572	$0.205 + 0.087 \cdot \text{CL}$	$0.202 + 0.087 \cdot \text{CL}$	$0.201 + 0.087 \cdot \text{CL}$
	$t_{PLH}$	3.530	$1.185 + 0.047 \cdot \text{CL}$	$1.186 + 0.047 \cdot \text{CL}$	$1.186 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	3.489	$1.263 + 0.045 \cdot \text{CL}$	$1.264 + 0.044 \cdot \text{CL}$	$1.265 + 0.044 \cdot \text{CL}$
	$t_{PLZ}$	1.322	$1.322 + 0.000 \cdot \text{CL}$	$1.322 + 0.000 \cdot \text{CL}$	$1.322 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.140	$1.140 + 0.000 \cdot \text{CL}$	$1.140 + 0.000 \cdot \text{CL}$	$1.140 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	5.293	$0.229 + 0.101 \cdot \text{CL}$	$0.228 + 0.101 \cdot \text{CL}$	$0.227 + 0.101 \cdot \text{CL}$
	$t_F$	4.572	$0.205 + 0.087 \cdot \text{CL}$	$0.202 + 0.087 \cdot \text{CL}$	$0.201 + 0.087 \cdot \text{CL}$
	$t_{PLH}$	3.632	$1.288 + 0.047 \cdot \text{CL}$	$1.288 + 0.047 \cdot \text{CL}$	$1.289 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	3.591	$1.367 + 0.044 \cdot \text{CL}$	$1.367 + 0.044 \cdot \text{CL}$	$1.367 + 0.044 \cdot \text{CL}$
	$t_{PLZ}$	1.366	$1.366 + 0.000 \cdot \text{CL}$	$1.366 + 0.000 \cdot \text{CL}$	$1.366 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.184	$1.184 + 0.000 \cdot \text{CL}$	$1.184 + 0.000 \cdot \text{CL}$	$1.184 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOT10**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.242	$0.194 + 0.081 \cdot \text{CL}$	$0.191 + 0.081 \cdot \text{CL}$	$0.190 + 0.081 \cdot \text{CL}$
	$t_F$	3.669	$0.183 + 0.070 \cdot \text{CL}$	$0.175 + 0.070 \cdot \text{CL}$	$0.172 + 0.070 \cdot \text{CL}$
	$t_{PLH}$	3.000	$1.124 + 0.038 \cdot \text{CL}$	$1.125 + 0.037 \cdot \text{CL}$	$1.125 + 0.037 \cdot \text{CL}$
	$t_{PHL}$	2.863	$1.083 + 0.036 \cdot \text{CL}$	$1.084 + 0.036 \cdot \text{CL}$	$1.084 + 0.036 \cdot \text{CL}$
TN to PAD	$t_R$	4.242	$0.194 + 0.081 \cdot \text{CL}$	$0.191 + 0.081 \cdot \text{CL}$	$0.190 + 0.081 \cdot \text{CL}$
	$t_F$	3.669	$0.183 + 0.070 \cdot \text{CL}$	$0.175 + 0.070 \cdot \text{CL}$	$0.172 + 0.070 \cdot \text{CL}$
	$t_{PLH}$	3.085	$1.208 + 0.038 \cdot \text{CL}$	$1.209 + 0.038 \cdot \text{CL}$	$1.210 + 0.038 \cdot \text{CL}$
	$t_{PHL}$	3.063	$1.282 + 0.036 \cdot \text{CL}$	$1.283 + 0.036 \cdot \text{CL}$	$1.284 + 0.036 \cdot \text{CL}$
	$t_{PLZ}$	1.397	$1.397 + 0.000 \cdot \text{CL}$	$1.397 + 0.000 \cdot \text{CL}$	$1.397 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.186	$1.186 + 0.000 \cdot \text{CL}$	$1.186 + 0.000 \cdot \text{CL}$	$1.186 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	4.242	$0.195 + 0.081 \cdot \text{CL}$	$0.190 + 0.081 \cdot \text{CL}$	$0.190 + 0.081 \cdot \text{CL}$
	$t_F$	3.669	$0.183 + 0.070 \cdot \text{CL}$	$0.175 + 0.070 \cdot \text{CL}$	$0.172 + 0.070 \cdot \text{CL}$
	$t_{PLH}$	3.188	$1.311 + 0.038 \cdot \text{CL}$	$1.312 + 0.038 \cdot \text{CL}$	$1.313 + 0.037 \cdot \text{CL}$
	$t_{PHL}$	3.166	$1.386 + 0.036 \cdot \text{CL}$	$1.386 + 0.036 \cdot \text{CL}$	$1.387 + 0.036 \cdot \text{CL}$
	$t_{PLZ}$	1.441	$1.441 + 0.000 \cdot \text{CL}$	$1.441 + 0.000 \cdot \text{CL}$	$1.441 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.230	$1.230 + 0.000 \cdot \text{CL}$	$1.230 + 0.000 \cdot \text{CL}$	$1.230 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



## PvOTyz

### Tri-State Output Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

PHOT12

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	3.544	$0.178 + 0.067 \cdot \text{CL}$	$0.169 + 0.067 \cdot \text{CL}$	$0.166 + 0.068 \cdot \text{CL}$
	$t_F$	3.071	$0.176 + 0.058 \cdot \text{CL}$	$0.163 + 0.058 \cdot \text{CL}$	$0.156 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	2.717	$1.154 + 0.031 \cdot \text{CL}$	$1.154 + 0.031 \cdot \text{CL}$	$1.154 + 0.031 \cdot \text{CL}$
	$t_{PHL}$	2.592	$1.108 + 0.030 \cdot \text{CL}$	$1.109 + 0.030 \cdot \text{CL}$	$1.109 + 0.030 \cdot \text{CL}$
TN to PAD	$t_R$	3.544	$0.178 + 0.067 \cdot \text{CL}$	$0.169 + 0.067 \cdot \text{CL}$	$0.166 + 0.068 \cdot \text{CL}$
	$t_F$	3.071	$0.176 + 0.058 \cdot \text{CL}$	$0.163 + 0.058 \cdot \text{CL}$	$0.156 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	2.802	$1.236 + 0.031 \cdot \text{CL}$	$1.238 + 0.031 \cdot \text{CL}$	$1.239 + 0.031 \cdot \text{CL}$
	$t_{PHL}$	2.792	$1.307 + 0.030 \cdot \text{CL}$	$1.308 + 0.030 \cdot \text{CL}$	$1.309 + 0.030 \cdot \text{CL}$
	$t_{PLZ}$	1.471	$1.472 + 0.000 \cdot \text{CL}$	$1.471 + 0.000 \cdot \text{CL}$	$1.471 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.232	$1.232 + 0.000 \cdot \text{CL}$	$1.232 + 0.000 \cdot \text{CL}$	$1.232 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	3.544	$0.178 + 0.067 \cdot \text{CL}$	$0.169 + 0.067 \cdot \text{CL}$	$0.166 + 0.068 \cdot \text{CL}$
	$t_F$	3.071	$0.176 + 0.058 \cdot \text{CL}$	$0.163 + 0.058 \cdot \text{CL}$	$0.156 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	2.904	$1.340 + 0.031 \cdot \text{CL}$	$1.341 + 0.031 \cdot \text{CL}$	$1.341 + 0.031 \cdot \text{CL}$
	$t_{PHL}$	2.894	$1.410 + 0.030 \cdot \text{CL}$	$1.411 + 0.030 \cdot \text{CL}$	$1.411 + 0.030 \cdot \text{CL}$
	$t_{PLZ}$	1.515	$1.516 + 0.000 \cdot \text{CL}$	$1.515 + 0.000 \cdot \text{CL}$	$1.515 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.276	$1.276 + 0.000 \cdot \text{CL}$	$1.276 + 0.000 \cdot \text{CL}$	$1.276 + 0.000 \cdot \text{CL}$

\*Group1 :  $\text{CL} < 50$ , \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PHOT4SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	10.608	$0.513 + 0.202 \cdot \text{CL}$	$0.486 + 0.202 \cdot \text{CL}$	$0.477 + 0.203 \cdot \text{CL}$
	$t_F$	9.436	$0.949 + 0.170 \cdot \text{CL}$	$0.845 + 0.172 \cdot \text{CL}$	$0.747 + 0.173 \cdot \text{CL}$
	$t_{PLH}$	6.340	$1.651 + 0.094 \cdot \text{CL}$	$1.652 + 0.094 \cdot \text{CL}$	$1.653 + 0.094 \cdot \text{CL}$
	$t_{PHL}$	7.303	$2.794 + 0.090 \cdot \text{CL}$	$2.843 + 0.089 \cdot \text{CL}$	$2.855 + 0.089 \cdot \text{CL}$
TN to PAD	$t_R$	10.608	$0.513 + 0.202 \cdot \text{CL}$	$0.486 + 0.202 \cdot \text{CL}$	$0.477 + 0.203 \cdot \text{CL}$
	$t_F$	9.436	$0.949 + 0.170 \cdot \text{CL}$	$0.845 + 0.172 \cdot \text{CL}$	$0.747 + 0.173 \cdot \text{CL}$
	$t_{PLH}$	6.426	$1.736 + 0.094 \cdot \text{CL}$	$1.738 + 0.094 \cdot \text{CL}$	$1.739 + 0.094 \cdot \text{CL}$
	$t_{PHL}$	7.503	$2.993 + 0.090 \cdot \text{CL}$	$3.043 + 0.089 \cdot \text{CL}$	$3.057 + 0.089 \cdot \text{CL}$
	$t_{PLZ}$	1.417	$1.417 + 0.000 \cdot \text{CL}$	$1.417 + 0.000 \cdot \text{CL}$	$1.417 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.355	$1.355 + 0.000 \cdot \text{CL}$	$1.355 + 0.000 \cdot \text{CL}$	$1.355 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	10.608	$0.513 + 0.202 \cdot \text{CL}$	$0.486 + 0.202 \cdot \text{CL}$	$0.477 + 0.203 \cdot \text{CL}$
	$t_F$	9.436	$0.949 + 0.170 \cdot \text{CL}$	$0.845 + 0.172 \cdot \text{CL}$	$0.747 + 0.173 \cdot \text{CL}$
	$t_{PLH}$	6.529	$1.840 + 0.094 \cdot \text{CL}$	$1.841 + 0.094 \cdot \text{CL}$	$1.842 + 0.094 \cdot \text{CL}$
	$t_{PHL}$	7.606	$3.097 + 0.090 \cdot \text{CL}$	$3.146 + 0.089 \cdot \text{CL}$	$3.160 + 0.089 \cdot \text{CL}$
	$t_{PLZ}$	1.461	$1.461 + 0.000 \cdot \text{CL}$	$1.461 + 0.000 \cdot \text{CL}$	$1.460 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.399	$1.399 + 0.000 \cdot \text{CL}$	$1.399 + 0.000 \cdot \text{CL}$	$1.399 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PHOT6SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	7.208	$0.611 + 0.132 \cdot \text{CL}$	$0.535 + 0.133 \cdot \text{CL}$	$0.477 + 0.134 \cdot \text{CL}$
	$t_F$	6.913	$1.361 + 0.111 \cdot \text{CL}$	$1.333 + 0.112 \cdot \text{CL}$	$1.254 + 0.113 \cdot \text{CL}$
	$t_{PLH}$	5.098	$1.955 + 0.063 \cdot \text{CL}$	$1.969 + 0.063 \cdot \text{CL}$	$1.973 + 0.063 \cdot \text{CL}$
	$t_{PHL}$	6.581	$3.267 + 0.066 \cdot \text{CL}$	$3.476 + 0.062 \cdot \text{CL}$	$3.603 + 0.060 \cdot \text{CL}$
TN to PAD	$t_R$	7.208	$0.611 + 0.132 \cdot \text{CL}$	$0.535 + 0.133 \cdot \text{CL}$	$0.477 + 0.134 \cdot \text{CL}$
	$t_F$	6.914	$1.361 + 0.111 \cdot \text{CL}$	$1.334 + 0.112 \cdot \text{CL}$	$1.251 + 0.113 \cdot \text{CL}$
	$t_{PLH}$	5.184	$2.040 + 0.063 \cdot \text{CL}$	$2.056 + 0.063 \cdot \text{CL}$	$2.059 + 0.063 \cdot \text{CL}$
	$t_{PHL}$	6.781	$3.468 + 0.066 \cdot \text{CL}$	$3.677 + 0.062 \cdot \text{CL}$	$3.803 + 0.060 \cdot \text{CL}$
	$t_{PLZ}$	1.724	$1.724 + 0.000 \cdot \text{CL}$	$1.724 + 0.000 \cdot \text{CL}$	$1.724 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.742	$1.742 + 0.000 \cdot \text{CL}$	$1.742 + 0.000 \cdot \text{CL}$	$1.742 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	7.208	$0.611 + 0.132 \cdot \text{CL}$	$0.535 + 0.133 \cdot \text{CL}$	$0.477 + 0.134 \cdot \text{CL}$
	$t_F$	6.914	$1.361 + 0.111 \cdot \text{CL}$	$1.334 + 0.112 \cdot \text{CL}$	$1.251 + 0.113 \cdot \text{CL}$
	$t_{PLH}$	5.287	$2.144 + 0.063 \cdot \text{CL}$	$2.158 + 0.063 \cdot \text{CL}$	$2.162 + 0.063 \cdot \text{CL}$
	$t_{PHL}$	6.884	$3.571 + 0.066 \cdot \text{CL}$	$3.779 + 0.062 \cdot \text{CL}$	$3.906 + 0.060 \cdot \text{CL}$
	$t_{PLZ}$	1.768	$1.768 + 0.000 \cdot \text{CL}$	$1.768 + 0.000 \cdot \text{CL}$	$1.768 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.786	$1.786 + 0.000 \cdot \text{CL}$	$1.786 + 0.000 \cdot \text{CL}$	$1.786 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOTyz

## Tri-State Output Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

### PHOT8SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.686	$0.878 + 0.096 \cdot \text{CL}$	$0.794 + 0.098 \cdot \text{CL}$	$0.705 + 0.099 \cdot \text{CL}$
	$t_F$	6.065	$1.797 + 0.085 \cdot \text{CL}$	$1.914 + 0.083 \cdot \text{CL}$	$1.934 + 0.083 \cdot \text{CL}$
	$t_{PLH}$	4.736	$2.280 + 0.049 \cdot \text{CL}$	$2.363 + 0.047 \cdot \text{CL}$	$2.395 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	6.607	$3.635 + 0.059 \cdot \text{CL}$	$3.984 + 0.052 \cdot \text{CL}$	$4.255 + 0.049 \cdot \text{CL}$
TN to PAD	$t_R$	5.687	$0.884 + 0.096 \cdot \text{CL}$	$0.796 + 0.098 \cdot \text{CL}$	$0.707 + 0.099 \cdot \text{CL}$
	$t_F$	6.065	$1.798 + 0.085 \cdot \text{CL}$	$1.915 + 0.083 \cdot \text{CL}$	$1.935 + 0.083 \cdot \text{CL}$
	$t_{PLH}$	4.821	$2.363 + 0.049 \cdot \text{CL}$	$2.447 + 0.047 \cdot \text{CL}$	$2.480 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	6.807	$3.835 + 0.059 \cdot \text{CL}$	$4.184 + 0.052 \cdot \text{CL}$	$4.454 + 0.049 \cdot \text{CL}$
	$t_{PLZ}$	2.028	$2.029 + 0.000 \cdot \text{CL}$	$2.028 + 0.000 \cdot \text{CL}$	$2.028 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.128	$2.128 + 0.000 \cdot \text{CL}$	$2.128 + 0.000 \cdot \text{CL}$	$2.128 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	5.687	$0.884 + 0.096 \cdot \text{CL}$	$0.797 + 0.098 \cdot \text{CL}$	$0.707 + 0.099 \cdot \text{CL}$
	$t_F$	6.065	$1.798 + 0.085 \cdot \text{CL}$	$1.915 + 0.083 \cdot \text{CL}$	$1.935 + 0.083 \cdot \text{CL}$
	$t_{PLH}$	4.924	$2.466 + 0.049 \cdot \text{CL}$	$2.550 + 0.047 \cdot \text{CL}$	$2.582 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	6.910	$3.939 + 0.059 \cdot \text{CL}$	$4.287 + 0.052 \cdot \text{CL}$	$4.557 + 0.049 \cdot \text{CL}$
	$t_{PLZ}$	2.072	$2.072 + 0.000 \cdot \text{CL}$	$2.072 + 0.000 \cdot \text{CL}$	$2.072 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.172	$2.172 + 0.000 \cdot \text{CL}$	$2.172 + 0.000 \cdot \text{CL}$	$2.172 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOT10SM

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.499	$0.605 + 0.078 \cdot \text{CL}$	$0.551 + 0.079 \cdot \text{CL}$	$0.500 + 0.080 \cdot \text{CL}$
	$t_F$	5.289	$1.831 + 0.069 \cdot \text{CL}$	$1.980 + 0.066 \cdot \text{CL}$	$2.030 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	3.975	$2.054 + 0.038 \cdot \text{CL}$	$2.093 + 0.038 \cdot \text{CL}$	$2.105 + 0.037 \cdot \text{CL}$
	$t_{PHL}$	6.063	$3.455 + 0.052 \cdot \text{CL}$	$3.822 + 0.045 \cdot \text{CL}$	$4.115 + 0.041 \cdot \text{CL}$
TN to PAD	$t_R$	4.509	$0.633 + 0.078 \cdot \text{CL}$	$0.572 + 0.079 \cdot \text{CL}$	$0.511 + 0.080 \cdot \text{CL}$
	$t_F$	5.290	$1.834 + 0.069 \cdot \text{CL}$	$1.981 + 0.066 \cdot \text{CL}$	$2.031 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	4.038	$2.086 + 0.039 \cdot \text{CL}$	$2.142 + 0.038 \cdot \text{CL}$	$2.163 + 0.038 \cdot \text{CL}$
	$t_{PHL}$	6.264	$3.655 + 0.052 \cdot \text{CL}$	$4.022 + 0.045 \cdot \text{CL}$	$4.315 + 0.041 \cdot \text{CL}$
	$t_{PLZ}$	2.773	$2.774 + 0.000 \cdot \text{CL}$	$2.773 + 0.000 \cdot \text{CL}$	$2.773 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.109	$2.110 + 0.000 \cdot \text{CL}$	$2.109 + 0.000 \cdot \text{CL}$	$2.109 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	4.509	$0.633 + 0.078 \cdot \text{CL}$	$0.572 + 0.079 \cdot \text{CL}$	$0.511 + 0.080 \cdot \text{CL}$
	$t_F$	5.290	$1.834 + 0.069 \cdot \text{CL}$	$1.981 + 0.066 \cdot \text{CL}$	$2.031 + 0.066 \cdot \text{CL}$
	$t_{PLH}$	4.140	$2.189 + 0.039 \cdot \text{CL}$	$2.245 + 0.038 \cdot \text{CL}$	$2.266 + 0.038 \cdot \text{CL}$
	$t_{PHL}$	6.366	$3.758 + 0.052 \cdot \text{CL}$	$4.125 + 0.045 \cdot \text{CL}$	$4.418 + 0.041 \cdot \text{CL}$
	$t_{PLZ}$	2.817	$2.817 + 0.000 \cdot \text{CL}$	$2.817 + 0.000 \cdot \text{CL}$	$2.817 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.153	$2.153 + 0.000 \cdot \text{CL}$	$2.153 + 0.000 \cdot \text{CL}$	$2.153 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PHOT12SM**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	3.998	$0.788 + 0.064 \cdot \text{CL}$	$0.767 + 0.065 \cdot \text{CL}$	$0.718 + 0.065 \cdot \text{CL}$
	$t_F$	4.487	$1.515 + 0.059 \cdot \text{CL}$	$1.662 + 0.057 \cdot \text{CL}$	$1.739 + 0.055 \cdot \text{CL}$
	$t_{PLH}$	3.937	$2.211 + 0.035 \cdot \text{CL}$	$2.314 + 0.032 \cdot \text{CL}$	$2.373 + 0.032 \cdot \text{CL}$
	$t_{PHL}$	5.635	$3.418 + 0.044 \cdot \text{CL}$	$3.720 + 0.038 \cdot \text{CL}$	$3.971 + 0.035 \cdot \text{CL}$
TN to PAD	$t_R$	4.011	$0.830 + 0.064 \cdot \text{CL}$	$0.793 + 0.064 \cdot \text{CL}$	$0.733 + 0.065 \cdot \text{CL}$
	$t_F$	4.489	$1.518 + 0.059 \cdot \text{CL}$	$1.664 + 0.056 \cdot \text{CL}$	$1.740 + 0.055 \cdot \text{CL}$
	$t_{PLH}$	4.005	$2.253 + 0.035 \cdot \text{CL}$	$2.372 + 0.033 \cdot \text{CL}$	$2.438 + 0.032 \cdot \text{CL}$
	$t_{PHL}$	5.835	$3.617 + 0.044 \cdot \text{CL}$	$3.920 + 0.038 \cdot \text{CL}$	$4.170 + 0.035 \cdot \text{CL}$
	$t_{PLZ}$	2.773	$2.774 + 0.000 \cdot \text{CL}$	$2.773 + 0.000 \cdot \text{CL}$	$2.773 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.495	$2.495 + 0.000 \cdot \text{CL}$	$2.495 + 0.000 \cdot \text{CL}$	$2.495 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	4.011	$0.830 + 0.064 \cdot \text{CL}$	$0.793 + 0.064 \cdot \text{CL}$	$0.733 + 0.065 \cdot \text{CL}$
	$t_F$	4.489	$1.518 + 0.059 \cdot \text{CL}$	$1.664 + 0.056 \cdot \text{CL}$	$1.740 + 0.055 \cdot \text{CL}$
	$t_{PLH}$	4.108	$2.356 + 0.035 \cdot \text{CL}$	$2.475 + 0.033 \cdot \text{CL}$	$2.542 + 0.032 \cdot \text{CL}$
	$t_{PHL}$	5.938	$3.720 + 0.044 \cdot \text{CL}$	$4.023 + 0.038 \cdot \text{CL}$	$4.274 + 0.035 \cdot \text{CL}$
	$t_{PLZ}$	2.817	$2.818 + 0.000 \cdot \text{CL}$	$2.817 + 0.000 \cdot \text{CL}$	$2.817 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.538	$2.539 + 0.000 \cdot \text{CL}$	$2.538 + 0.000 \cdot \text{CL}$	$2.538 + 0.000 \cdot \text{CL}$

\*Group1 :  $\text{CL} < 50$ , \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



# PvOTyz

## Tri-State Output Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

### PHOT10SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	5.273	$1.448 + 0.077 \cdot \text{CL}$	$1.465 + 0.076 \cdot \text{CL}$	$1.414 + 0.077 \cdot \text{CL}$
	$t_F$	6.224	$2.449 + 0.075 \cdot \text{CL}$	$2.727 + 0.070 \cdot \text{CL}$	$2.915 + 0.067 \cdot \text{CL}$
	$t_{PLH}$	5.546	$3.210 + 0.047 \cdot \text{CL}$	$3.452 + 0.042 \cdot \text{CL}$	$3.622 + 0.040 \cdot \text{CL}$
	$t_{PHL}$	7.875	$4.751 + 0.062 \cdot \text{CL}$	$5.253 + 0.052 \cdot \text{CL}$	$5.682 + 0.047 \cdot \text{CL}$
TN to PAD	$t_R$	5.279	$1.469 + 0.076 \cdot \text{CL}$	$1.475 + 0.076 \cdot \text{CL}$	$1.420 + 0.077 \cdot \text{CL}$
	$t_F$	6.225	$2.451 + 0.075 \cdot \text{CL}$	$2.728 + 0.070 \cdot \text{CL}$	$2.916 + 0.067 \cdot \text{CL}$
	$t_{PLH}$	5.629	$3.285 + 0.047 \cdot \text{CL}$	$3.532 + 0.042 \cdot \text{CL}$	$3.704 + 0.040 \cdot \text{CL}$
	$t_{PHL}$	8.076	$4.952 + 0.062 \cdot \text{CL}$	$5.454 + 0.052 \cdot \text{CL}$	$5.882 + 0.047 \cdot \text{CL}$
	$t_{PLZ}$	2.857	$2.857 + 0.000 \cdot \text{CL}$	$2.857 + 0.000 \cdot \text{CL}$	$2.856 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.572	$2.572 + 0.000 \cdot \text{CL}$	$2.572 + 0.000 \cdot \text{CL}$	$2.571 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	5.279	$1.469 + 0.076 \cdot \text{CL}$	$1.475 + 0.076 \cdot \text{CL}$	$1.419 + 0.077 \cdot \text{CL}$
	$t_F$	6.225	$2.451 + 0.075 \cdot \text{CL}$	$2.728 + 0.070 \cdot \text{CL}$	$2.916 + 0.067 \cdot \text{CL}$
	$t_{PLH}$	5.732	$3.388 + 0.047 \cdot \text{CL}$	$3.635 + 0.042 \cdot \text{CL}$	$3.807 + 0.040 \cdot \text{CL}$
	$t_{PHL}$	8.178	$5.056 + 0.062 \cdot \text{CL}$	$5.557 + 0.052 \cdot \text{CL}$	$5.985 + 0.047 \cdot \text{CL}$
	$t_{PLZ}$	2.900	$2.901 + 0.000 \cdot \text{CL}$	$2.900 + 0.000 \cdot \text{CL}$	$2.900 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.615	$2.616 + 0.000 \cdot \text{CL}$	$2.615 + 0.000 \cdot \text{CL}$	$2.615 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

### PHOT12SH

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.965	$1.691 + 0.065 \cdot \text{CL}$	$1.798 + 0.063 \cdot \text{CL}$	$1.812 + 0.063 \cdot \text{CL}$
	$t_F$	6.246	$2.790 + 0.069 \cdot \text{CL}$	$3.146 + 0.062 \cdot \text{CL}$	$3.418 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	5.693	$3.462 + 0.045 \cdot \text{CL}$	$3.765 + 0.039 \cdot \text{CL}$	$4.004 + 0.035 \cdot \text{CL}$
	$t_{PHL}$	8.197	$5.024 + 0.063 \cdot \text{CL}$	$5.605 + 0.052 \cdot \text{CL}$	$6.112 + 0.045 \cdot \text{CL}$
TN to PAD	$t_R$	4.983	$1.756 + 0.065 \cdot \text{CL}$	$1.833 + 0.063 \cdot \text{CL}$	$1.833 + 0.063 \cdot \text{CL}$
	$t_F$	6.248	$2.799 + 0.069 \cdot \text{CL}$	$3.151 + 0.062 \cdot \text{CL}$	$3.421 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	5.769	$3.514 + 0.045 \cdot \text{CL}$	$3.832 + 0.039 \cdot \text{CL}$	$4.077 + 0.035 \cdot \text{CL}$
	$t_{PHL}$	8.397	$5.221 + 0.064 \cdot \text{CL}$	$5.805 + 0.052 \cdot \text{CL}$	$6.310 + 0.045 \cdot \text{CL}$
	$t_{PLZ}$	3.262	$3.262 + 0.000 \cdot \text{CL}$	$3.262 + 0.000 \cdot \text{CL}$	$3.261 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.957	$2.957 + 0.000 \cdot \text{CL}$	$2.957 + 0.000 \cdot \text{CL}$	$2.957 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	4.983	$1.756 + 0.065 \cdot \text{CL}$	$1.833 + 0.063 \cdot \text{CL}$	$1.833 + 0.063 \cdot \text{CL}$
	$t_F$	6.248	$2.799 + 0.069 \cdot \text{CL}$	$3.151 + 0.062 \cdot \text{CL}$	$3.421 + 0.058 \cdot \text{CL}$
	$t_{PLH}$	5.871	$3.618 + 0.045 \cdot \text{CL}$	$3.935 + 0.039 \cdot \text{CL}$	$4.180 + 0.035 \cdot \text{CL}$
	$t_{PHL}$	8.500	$5.325 + 0.063 \cdot \text{CL}$	$5.908 + 0.052 \cdot \text{CL}$	$6.413 + 0.045 \cdot \text{CL}$
	$t_{PLZ}$	3.306	$3.306 + 0.000 \cdot \text{CL}$	$3.306 + 0.000 \cdot \text{CL}$	$3.305 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	3.001	$3.001 + 0.000 \cdot \text{CL}$	$3.001 + 0.000 \cdot \text{CL}$	$3.001 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])**PTOT1**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	44.026	$2.843 + 0.824 \cdot \text{CL}$	$2.992 + 0.821 \cdot \text{CL}$	$3.100 + 0.819 \cdot \text{CL}$
	$t_F$	33.890	$2.747 + 0.623 \cdot \text{CL}$	$2.704 + 0.624 \cdot \text{CL}$	$2.677 + 0.624 \cdot \text{CL}$
	$t_{PLH}$	21.514	$2.654 + 0.377 \cdot \text{CL}$	$2.712 + 0.376 \cdot \text{CL}$	$2.748 + 0.376 \cdot \text{CL}$
	$t_{PHL}$	17.371	$1.761 + 0.312 \cdot \text{CL}$	$1.781 + 0.312 \cdot \text{CL}$	$1.799 + 0.312 \cdot \text{CL}$
TN to PAD	$t_R$	44.026	$2.843 + 0.824 \cdot \text{CL}$	$2.992 + 0.821 \cdot \text{CL}$	$3.100 + 0.819 \cdot \text{CL}$
	$t_F$	33.854	$2.744 + 0.622 \cdot \text{CL}$	$2.692 + 0.623 \cdot \text{CL}$	$2.662 + 0.624 \cdot \text{CL}$
	$t_{PLH}$	21.600	$2.740 + 0.377 \cdot \text{CL}$	$2.798 + 0.376 \cdot \text{CL}$	$2.834 + 0.376 \cdot \text{CL}$
	$t_{PHL}$	17.491	$1.944 + 0.311 \cdot \text{CL}$	$1.951 + 0.311 \cdot \text{CL}$	$1.963 + 0.311 \cdot \text{CL}$
	$t_{PLZ}$	1.075	$1.075 + 0.000 \cdot \text{CL}$	$1.075 + 0.000 \cdot \text{CL}$	$1.075 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.801	$1.800 + 0.000 \cdot \text{CL}$	$1.800 + 0.000 \cdot \text{CL}$	$1.801 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	44.026	$2.843 + 0.824 \cdot \text{CL}$	$2.992 + 0.821 \cdot \text{CL}$	$3.100 + 0.819 \cdot \text{CL}$
	$t_F$	33.854	$2.744 + 0.622 \cdot \text{CL}$	$2.692 + 0.623 \cdot \text{CL}$	$2.662 + 0.624 \cdot \text{CL}$
	$t_{PLH}$	21.702	$2.845 + 0.377 \cdot \text{CL}$	$2.900 + 0.376 \cdot \text{CL}$	$2.936 + 0.376 \cdot \text{CL}$
	$t_{PHL}$	17.593	$2.048 + 0.311 \cdot \text{CL}$	$2.051 + 0.311 \cdot \text{CL}$	$2.069 + 0.311 \cdot \text{CL}$
	$t_{PLZ}$	1.120	$1.120 + 0.000 \cdot \text{CL}$	$1.120 + 0.000 \cdot \text{CL}$	$1.120 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.844	$1.844 + 0.000 \cdot \text{CL}$	$1.844 + 0.000 \cdot \text{CL}$	$1.844 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ **PTOT2**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	22.250	$1.485 + 0.415 \cdot \text{CL}$	$1.620 + 0.413 \cdot \text{CL}$	$1.725 + 0.411 \cdot \text{CL}$
	$t_F$	17.034	$1.379 + 0.313 \cdot \text{CL}$	$1.416 + 0.312 \cdot \text{CL}$	$1.419 + 0.312 \cdot \text{CL}$
	$t_{PLH}$	11.348	$1.857 + 0.190 \cdot \text{CL}$	$1.908 + 0.189 \cdot \text{CL}$	$1.947 + 0.188 \cdot \text{CL}$
	$t_{PHL}$	9.224	$1.372 + 0.157 \cdot \text{CL}$	$1.399 + 0.157 \cdot \text{CL}$	$1.422 + 0.156 \cdot \text{CL}$
TN to PAD	$t_R$	22.250	$1.485 + 0.415 \cdot \text{CL}$	$1.620 + 0.413 \cdot \text{CL}$	$1.725 + 0.411 \cdot \text{CL}$
	$t_F$	16.992	$1.367 + 0.312 \cdot \text{CL}$	$1.396 + 0.312 \cdot \text{CL}$	$1.402 + 0.312 \cdot \text{CL}$
	$t_{PLH}$	11.434	$1.944 + 0.190 \cdot \text{CL}$	$1.994 + 0.189 \cdot \text{CL}$	$2.030 + 0.188 \cdot \text{CL}$
	$t_{PHL}$	9.348	$1.545 + 0.156 \cdot \text{CL}$	$1.563 + 0.156 \cdot \text{CL}$	$1.579 + 0.155 \cdot \text{CL}$
	$t_{PLZ}$	1.201	$1.201 + 0.000 \cdot \text{CL}$	$1.201 + 0.000 \cdot \text{CL}$	$1.201 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.304	$2.304 + 0.000 \cdot \text{CL}$	$2.304 + 0.000 \cdot \text{CL}$	$2.303 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	22.250	$1.485 + 0.415 \cdot \text{CL}$	$1.620 + 0.413 \cdot \text{CL}$	$1.725 + 0.411 \cdot \text{CL}$
	$t_F$	16.992	$1.367 + 0.312 \cdot \text{CL}$	$1.396 + 0.312 \cdot \text{CL}$	$1.402 + 0.312 \cdot \text{CL}$
	$t_{PLH}$	11.537	$2.046 + 0.190 \cdot \text{CL}$	$2.097 + 0.189 \cdot \text{CL}$	$2.136 + 0.188 \cdot \text{CL}$
	$t_{PHL}$	9.450	$1.648 + 0.156 \cdot \text{CL}$	$1.664 + 0.156 \cdot \text{CL}$	$1.685 + 0.155 \cdot \text{CL}$
	$t_{PLZ}$	1.245	$1.245 + 0.000 \cdot \text{CL}$	$1.245 + 0.000 \cdot \text{CL}$	$1.245 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.347	$2.347 + 0.000 \cdot \text{CL}$	$2.347 + 0.000 \cdot \text{CL}$	$2.347 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



## PvOTyz

### Tri-State Output Buffers

**Switching Characteristics**(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load[pf])

PTOT3

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	14.950	$1.003 + 0.279 \cdot \text{CL}$	$1.124 + 0.277 \cdot \text{CL}$	$1.223 + 0.275 \cdot \text{CL}$
	$t_F$	11.398	$0.929 + 0.209 \cdot \text{CL}$	$0.952 + 0.209 \cdot \text{CL}$	$0.976 + 0.209 \cdot \text{CL}$
	$t_{PLH}$	7.984	$1.628 + 0.127 \cdot \text{CL}$	$1.665 + 0.126 \cdot \text{CL}$	$1.702 + 0.126 \cdot \text{CL}$
	$t_{PHL}$	6.545	$1.288 + 0.105 \cdot \text{CL}$	$1.308 + 0.105 \cdot \text{CL}$	$1.327 + 0.104 \cdot \text{CL}$
TN to PAD	$t_R$	14.950	$1.005 + 0.279 \cdot \text{CL}$	$1.122 + 0.277 \cdot \text{CL}$	$1.227 + 0.275 \cdot \text{CL}$
	$t_F$	11.350	$0.906 + 0.209 \cdot \text{CL}$	$0.926 + 0.208 \cdot \text{CL}$	$0.947 + 0.208 \cdot \text{CL}$
	$t_{PLH}$	8.070	$1.714 + 0.127 \cdot \text{CL}$	$1.751 + 0.126 \cdot \text{CL}$	$1.789 + 0.126 \cdot \text{CL}$
	$t_{PHL}$	6.666	$1.450 + 0.104 \cdot \text{CL}$	$1.462 + 0.104 \cdot \text{CL}$	$1.481 + 0.104 \cdot \text{CL}$
	$t_{PLZ}$	1.323	$1.323 + 0.000 \cdot \text{CL}$	$1.323 + 0.000 \cdot \text{CL}$	$1.323 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.808	$2.809 + 0.000 \cdot \text{CL}$	$2.808 + 0.000 \cdot \text{CL}$	$2.808 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	14.950	$1.005 + 0.279 \cdot \text{CL}$	$1.122 + 0.277 \cdot \text{CL}$	$1.227 + 0.275 \cdot \text{CL}$
	$t_F$	11.350	$0.906 + 0.209 \cdot \text{CL}$	$0.926 + 0.208 \cdot \text{CL}$	$0.947 + 0.208 \cdot \text{CL}$
	$t_{PLH}$	8.173	$1.817 + 0.127 \cdot \text{CL}$	$1.855 + 0.126 \cdot \text{CL}$	$1.891 + 0.126 \cdot \text{CL}$
	$t_{PHL}$	6.768	$1.553 + 0.104 \cdot \text{CL}$	$1.565 + 0.104 \cdot \text{CL}$	$1.584 + 0.104 \cdot \text{CL}$
	$t_{PLZ}$	1.367	$1.367 + 0.000 \cdot \text{CL}$	$1.367 + 0.000 \cdot \text{CL}$	$1.367 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.852	$2.853 + 0.000 \cdot \text{CL}$	$2.852 + 0.000 \cdot \text{CL}$	$2.851 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



## BI-DIRECTIONAL BUFFERS

### Cell List

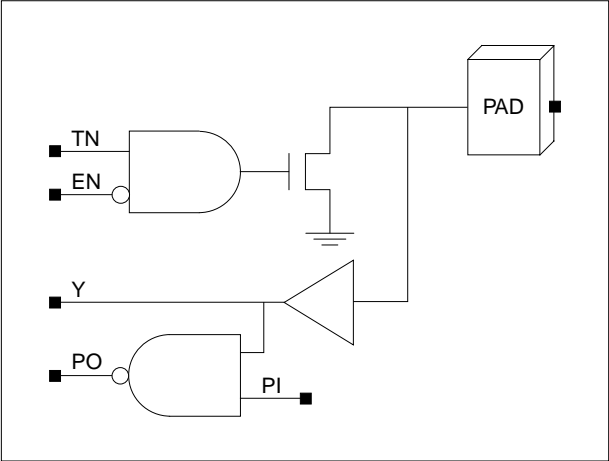
Cell Name	Function Description
PBaDyz	2.5V Open-Drain Bi-Directional Buffers
PBaUDyz	2.5 V Open-Drain Bi-Directional Buffers with Pull-Up
PHBaDyz	3.3V Interface Open-Drain Bi-Directional Buffers with Pull-Down
PHBaUDyz	3.3 V Interface Open-Drain Bi-Directional Buffers with Pull-Up
PTBaDy	5V - Tolerant Open-Drain Bi-Directional Buffers
PTBaUDy	5V - Tolerant Open-Drain Bi-Directional Buffers with Pull-Up
PBaTyz	2.5V Tri-State Bi-Directional Buffers
PBaDTyz	2.5V Tri-State Bi-Directional Buffers with Pull-Down
PBaUTyz	2.5V Tri-State Bi-Directional Buffers with Pull-Up
PHBaTyz	3.3V Interface Tri-State Bi-Directional Buffers
PHBaDTyz	3.3V Interface Tri-State Bi-Directional Buffers with Pull-Down
PHBaUTyz	3.3V Interface Tri-State Bi-Directional Buffers with Pull-Up
PTBaTy	5V - Tolerant Tri-State Bi-Directional Buffers
PTBaDTy	5V - Tolerant Tri-State Bi-Directional Buffers with Pull-Down
PTBaUTy	5V - Tolerant Tri-State Bi-Directional Buffers with Pull-Up



# BI-DIRECTIONAL BUFFERS

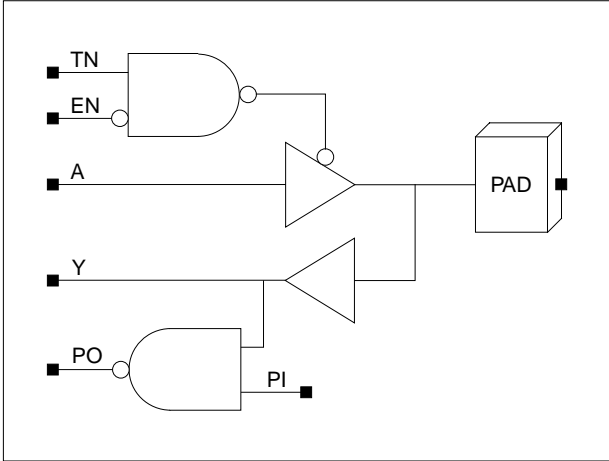
## Open Drain Bi-Directional Buffers

PvBaDyz

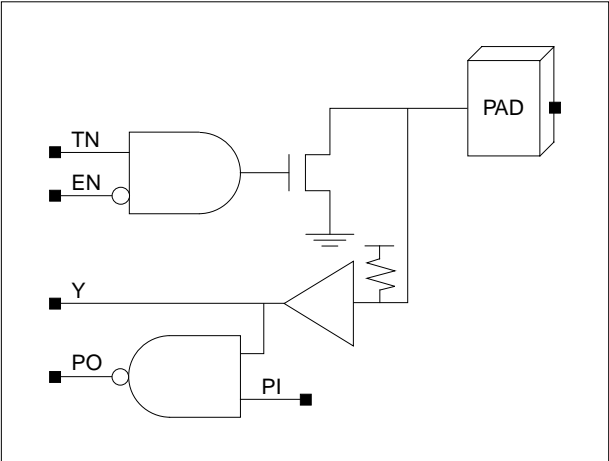


## Tri-State Bi-Directional Buffers

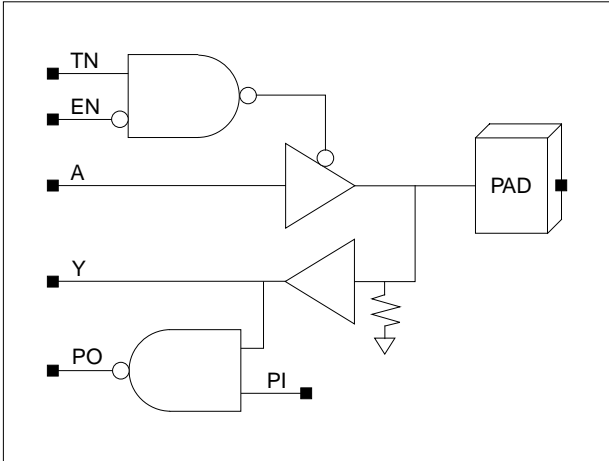
PvBaTyz



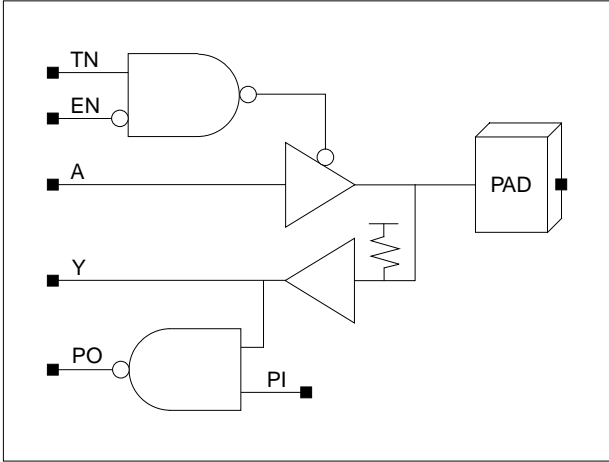
PvBaUDyz



PvBaDTyz



PvBaUTyz





## INPUT CLOCK DRIVERS

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### Cell List

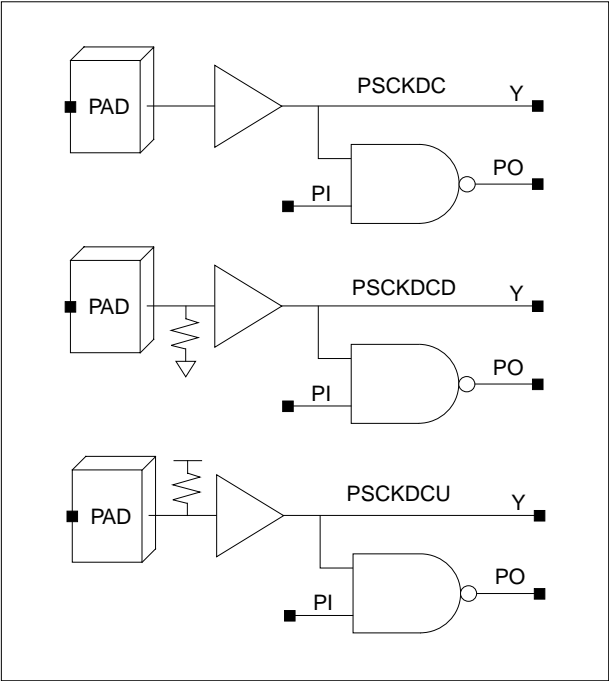
Cell Name	Function Description
PSCKDC(2/4/6/8)	2.5V LVCMOS Level Input Clock Driver
PSCKDCD(2/4/6/8)	2.5V LVCMOS Level Input Clock Driver with Pull-Down
PSCKDCU(2/4/6/8)	2.5V LVCMOS Level Input Clock Driver with Pull-Up
PSCKDS(2/4/6/8)	2.5V LVCMOS-Schmitt Trigger Level Input Clock Driver
PSCKDSD(2/4/6/8)	2.5V LVCMOS-Schmitt Trigger Level Input Clock Driver with Pull-Down
PSCKDSU(2/4/6/8)	2.5V LVCMOS-Schmitt Trigger Level Input Clock Driver with Pull-Up



# PSCKDCby

## LVC MOS Level Input Clock Drivers

### Logic Symbol



### Cell Availability

Only 2.5V
PSCKDC/PSCKDCD/PSCKDCU (2/4/6/8)

### Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

### Standard Load (SL)

Cell Name	PI
PSCKDC/PSCKDCD/PSCKDCU (2/4/6/8)	4.193



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

**PSCKDC2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.175	$0.169 + 0.003 \cdot \text{SL}$	$0.124 + 0.003 \cdot \text{SL}$	$0.100 + 0.003 \cdot \text{SL}$
	$t_F$	0.142	$0.134 + 0.004 \cdot \text{SL}$	$0.101 + 0.004 \cdot \text{SL}$	$0.086 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.813	$0.811 + 0.001 \cdot \text{SL}$	$0.807 + 0.001 \cdot \text{SL}$	$0.806 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.795	$0.791 + 0.002 \cdot \text{SL}$	$0.788 + 0.002 \cdot \text{SL}$	$0.789 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 482$ , \*Group2 :  $482 \leq \text{SL} \leq 722$ , \*Group3 :  $722 < \text{SL}$ 
**PSCKDC4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.235	$0.232 + 0.002 \cdot \text{SL}$	$0.175 + 0.002 \cdot \text{SL}$	$0.136 + 0.002 \cdot \text{SL}$
	$t_F$	0.182	$0.178 + 0.002 \cdot \text{SL}$	$0.126 + 0.002 \cdot \text{SL}$	$0.099 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	1.051	$1.049 + 0.001 \cdot \text{SL}$	$1.050 + 0.001 \cdot \text{SL}$	$1.048 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	1.036	$1.034 + 0.001 \cdot \text{SL}$	$1.031 + 0.001 \cdot \text{SL}$	$1.028 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 962$ , \*Group2 :  $962 \leq \text{SL} \leq 1443$ , \*Group3 :  $1443 < \text{SL}$ 
**PSCKDC6**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.291	$0.289 + 0.001 \cdot \text{SL}$	$0.226 + 0.001 \cdot \text{SL}$	$0.181 + 0.001 \cdot \text{SL}$
	$t_F$	0.224	$0.222 + 0.001 \cdot \text{SL}$	$0.160 + 0.001 \cdot \text{SL}$	$0.122 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	1.246	$1.245 + 0.000 \cdot \text{SL}$	$1.254 + 0.000 \cdot \text{SL}$	$1.251 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	1.237	$1.235 + 0.001 \cdot \text{SL}$	$1.232 + 0.001 \cdot \text{SL}$	$1.227 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 1443$ , \*Group2 :  $1443 \leq \text{SL} \leq 2165$ , \*Group3 :  $2165 < \text{SL}$ 
**PSCKDC8**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.341	$0.340 + 0.001 \cdot \text{SL}$	$0.273 + 0.001 \cdot \text{SL}$	$0.224 + 0.001 \cdot \text{SL}$
	$t_F$	0.263	$0.262 + 0.001 \cdot \text{SL}$	$0.196 + 0.001 \cdot \text{SL}$	$0.149 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	1.415	$1.414 + 0.000 \cdot \text{SL}$	$1.431 + 0.000 \cdot \text{SL}$	$1.429 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	1.410	$1.409 + 0.000 \cdot \text{SL}$	$1.407 + 0.000 \cdot \text{SL}$	$1.402 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 1923$ , \*Group2 :  $1923 \leq \text{SL} \leq 2887$ , \*Group3 :  $2887 < \text{SL}$



# PSCKDCby

## LVCMOS Level Input Clock Drivers

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 3.00ns$ , SL: Standard Load)

#### PSCKDCD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.172	$0.165 + 0.003*SL$	$0.122 + 0.003*SL$	$0.099 + 0.003*SL$
	$t_F$	0.146	$0.139 + 0.004*SL$	$0.104 + 0.004*SL$	$0.087 + 0.004*SL$
	$t_{PLH}$	0.903	$0.900 + 0.001*SL$	$0.897 + 0.001*SL$	$0.896 + 0.001*SL$
	$t_{PHL}$	0.796	$0.792 + 0.002*SL$	$0.789 + 0.002*SL$	$0.790 + 0.002*SL$

\*Group1 :  $SL < 482$ , \*Group2 :  $482 \leq SL \leq 722$ , \*Group3 :  $722 < SL$

#### PSCKDCD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.231	$0.228 + 0.002*SL$	$0.171 + 0.002*SL$	$0.135 + 0.002*SL$
	$t_F$	0.189	$0.185 + 0.002*SL$	$0.130 + 0.002*SL$	$0.102 + 0.002*SL$
	$t_{PLH}$	1.137	$1.135 + 0.001*SL$	$1.136 + 0.001*SL$	$1.133 + 0.001*SL$
	$t_{PHL}$	1.048	$1.046 + 0.001*SL$	$1.042 + 0.001*SL$	$1.039 + 0.001*SL$

\*Group1 :  $SL < 962$ , \*Group2 :  $962 \leq SL \leq 1443$ , \*Group3 :  $1443 < SL$

#### PSCKDCD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.287	$0.285 + 0.001*SL$	$0.222 + 0.001*SL$	$0.178 + 0.001*SL$
	$t_F$	0.234	$0.231 + 0.001*SL$	$0.167 + 0.001*SL$	$0.127 + 0.001*SL$
	$t_{PLH}$	1.330	$1.329 + 0.000*SL$	$1.338 + 0.000*SL$	$1.334 + 0.000*SL$
	$t_{PHL}$	1.256	$1.255 + 0.001*SL$	$1.252 + 0.001*SL$	$1.246 + 0.001*SL$

\*Group1 :  $SL < 1443$ , \*Group2 :  $1443 \leq SL \leq 2165$ , \*Group3 :  $2165 < SL$

#### PSCKDCD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.337	$0.335 + 0.001*SL$	$0.270 + 0.001*SL$	$0.222 + 0.001*SL$
	$t_F$	0.274	$0.273 + 0.001*SL$	$0.205 + 0.001*SL$	$0.156 + 0.001*SL$
	$t_{PLH}$	1.497	$1.496 + 0.000*SL$	$1.513 + 0.000*SL$	$1.511 + 0.000*SL$
	$t_{PHL}$	1.436	$1.435 + 0.000*SL$	$1.434 + 0.000*SL$	$1.427 + 0.000*SL$

\*Group1 :  $SL < 1923$ , \*Group2 :  $1923 \leq SL \leq 2887$ , \*Group3 :  $2887 < SL$



**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

**PSCKDCU2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.181	$0.174 + 0.003 \cdot \text{SL}$	$0.128 + 0.003 \cdot \text{SL}$	$0.102 + 0.003 \cdot \text{SL}$
	$t_F$	0.140	$0.133 + 0.004 \cdot \text{SL}$	$0.100 + 0.004 \cdot \text{SL}$	$0.086 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	0.810	$0.807 + 0.001 \cdot \text{SL}$	$0.804 + 0.001 \cdot \text{SL}$	$0.802 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	0.879	$0.875 + 0.002 \cdot \text{SL}$	$0.873 + 0.002 \cdot \text{SL}$	$0.873 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 482$ , \*Group2 :  $482 \leq \text{SL} \leq 722$ , \*Group3 :  $722 < \text{SL}$ 
**PSCKDCU4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.243	$0.240 + 0.002 \cdot \text{SL}$	$0.181 + 0.002 \cdot \text{SL}$	$0.141 + 0.002 \cdot \text{SL}$
	$t_F$	0.179	$0.175 + 0.002 \cdot \text{SL}$	$0.124 + 0.002 \cdot \text{SL}$	$0.098 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	1.055	$1.053 + 0.001 \cdot \text{SL}$	$1.054 + 0.001 \cdot \text{SL}$	$1.052 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	1.117	$1.115 + 0.001 \cdot \text{SL}$	$1.112 + 0.001 \cdot \text{SL}$	$1.108 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 962$ , \*Group2 :  $962 \leq \text{SL} \leq 1443$ , \*Group3 :  $1443 < \text{SL}$ 
**PSCKDCU6**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.301	$0.299 + 0.001 \cdot \text{SL}$	$0.233 + 0.001 \cdot \text{SL}$	$0.187 + 0.001 \cdot \text{SL}$
	$t_F$	0.221	$0.219 + 0.001 \cdot \text{SL}$	$0.158 + 0.001 \cdot \text{SL}$	$0.121 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	1.255	$1.254 + 0.000 \cdot \text{SL}$	$1.264 + 0.000 \cdot \text{SL}$	$1.261 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	1.315	$1.314 + 0.001 \cdot \text{SL}$	$1.311 + 0.001 \cdot \text{SL}$	$1.306 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 1443$ , \*Group2 :  $1443 \leq \text{SL} \leq 2165$ , \*Group3 :  $2165 < \text{SL}$ 
**PSCKDCU8**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.352	$0.350 + 0.001 \cdot \text{SL}$	$0.282 + 0.001 \cdot \text{SL}$	$0.231 + 0.001 \cdot \text{SL}$
	$t_F$	0.260	$0.258 + 0.001 \cdot \text{SL}$	$0.194 + 0.001 \cdot \text{SL}$	$0.148 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	1.428	$1.427 + 0.000 \cdot \text{SL}$	$1.446 + 0.000 \cdot \text{SL}$	$1.444 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	1.487	$1.486 + 0.000 \cdot \text{SL}$	$1.484 + 0.000 \cdot \text{SL}$	$1.479 + 0.000 \cdot \text{SL}$

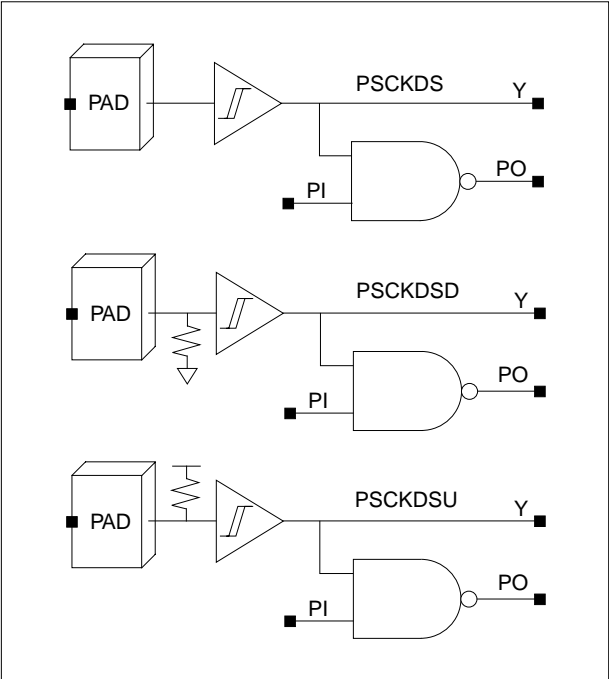
\*Group1 :  $\text{SL} < 1923$ , \*Group2 :  $1923 \leq \text{SL} \leq 2887$ , \*Group3 :  $2887 < \text{SL}$



PSCKDSby

LVC MOS Schmitt Trigger Level Input Clock Drivers

Logic Symbol



Cell Availability

Only 2.5V
PSCKDS/PSCKDSD/PSCKDSU(2/4/6/8)

Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

	PI
PSCKDS/PSCKDSD/PSCKDSU (2/4/6/8)	4.193



**LVC MOS Schmitt Trigger Level Input Clock Drivers**
**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

**PSCKDS2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.201	$0.195 + 0.003 \cdot \text{SL}$	$0.157 + 0.003 \cdot \text{SL}$	$0.130 + 0.003 \cdot \text{SL}$
	$t_F$	0.194	$0.187 + 0.004 \cdot \text{SL}$	$0.149 + 0.004 \cdot \text{SL}$	$0.124 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	1.142	$1.139 + 0.001 \cdot \text{SL}$	$1.142 + 0.001 \cdot \text{SL}$	$1.142 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	1.195	$1.191 + 0.002 \cdot \text{SL}$	$1.197 + 0.002 \cdot \text{SL}$	$1.196 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 482$ , \*Group2 :  $482 \leq \text{SL} \leq 722$ , \*Group3 :  $722 < \text{SL}$ 
**PSCKDS4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.270	$0.267 + 0.002 \cdot \text{SL}$	$0.219 + 0.002 \cdot \text{SL}$	$0.182 + 0.002 \cdot \text{SL}$
	$t_F$	0.264	$0.260 + 0.002 \cdot \text{SL}$	$0.215 + 0.002 \cdot \text{SL}$	$0.178 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	1.401	$1.399 + 0.001 \cdot \text{SL}$	$1.415 + 0.001 \cdot \text{SL}$	$1.418 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	1.484	$1.482 + 0.001 \cdot \text{SL}$	$1.500 + 0.001 \cdot \text{SL}$	$1.501 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 962$ , \*Group2 :  $962 \leq \text{SL} \leq 1443$ , \*Group3 :  $1443 < \text{SL}$ 
**PSCKDS6**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.331	$0.329 + 0.001 \cdot \text{SL}$	$0.278 + 0.001 \cdot \text{SL}$	$0.239 + 0.001 \cdot \text{SL}$
	$t_F$	0.356	$0.354 + 0.001 \cdot \text{SL}$	$0.307 + 0.001 \cdot \text{SL}$	$0.261 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	1.610	$1.609 + 0.001 \cdot \text{SL}$	$1.639 + 0.000 \cdot \text{SL}$	$1.645 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	1.743	$1.742 + 0.001 \cdot \text{SL}$	$1.775 + 0.001 \cdot \text{SL}$	$1.783 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 1443$ , \*Group2 :  $1443 \leq \text{SL} \leq 2165$ , \*Group3 :  $2165 < \text{SL}$ 
**PSCKDS8**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.384	$0.383 + 0.001 \cdot \text{SL}$	$0.334 + 0.001 \cdot \text{SL}$	$0.293 + 0.001 \cdot \text{SL}$
	$t_F$	0.456	$0.454 + 0.001 \cdot \text{SL}$	$0.406 + 0.001 \cdot \text{SL}$	$0.359 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	1.788	$1.788 + 0.000 \cdot \text{SL}$	$1.829 + 0.000 \cdot \text{SL}$	$1.841 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	1.990	$1.989 + 0.001 \cdot \text{SL}$	$2.039 + 0.000 \cdot \text{SL}$	$2.055 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 1923$ , \*Group2 :  $1923 \leq \text{SL} \leq 2887$ , \*Group3 :  $2887 < \text{SL}$



# PSCKDSby

## LVCMOS Schmitt Trigger Level Input Clock Drivers

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 3.00ns$ , SL: Standard Load)

#### PSCKDSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.199	$0.193 + 0.003*SL$	$0.155 + 0.003*SL$	$0.129 + 0.003*SL$
	$t_F$	0.198	$0.191 + 0.004*SL$	$0.153 + 0.004*SL$	$0.127 + 0.004*SL$
	$t_{PLH}$	1.208	$1.205 + 0.001*SL$	$1.208 + 0.001*SL$	$1.209 + 0.001*SL$
	$t_{PHL}$	1.243	$1.239 + 0.002*SL$	$1.246 + 0.002*SL$	$1.245 + 0.002*SL$

\*Group1 :  $SL < 482$ , \*Group2 :  $482 \leq SL \leq 722$ , \*Group3 :  $722 < SL$

#### PSCKDSD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.267	$0.264 + 0.002*SL$	$0.217 + 0.002*SL$	$0.181 + 0.002*SL$
	$t_F$	0.269	$0.266 + 0.002*SL$	$0.220 + 0.002*SL$	$0.182 + 0.002*SL$
	$t_{PLH}$	1.464	$1.463 + 0.001*SL$	$1.478 + 0.001*SL$	$1.481 + 0.001*SL$
	$t_{PHL}$	1.547	$1.545 + 0.001*SL$	$1.562 + 0.001*SL$	$1.564 + 0.001*SL$

\*Group1 :  $SL < 962$ , \*Group2 :  $962 \leq SL \leq 1443$ , \*Group3 :  $1443 < SL$

#### PSCKDSD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.328	$0.326 + 0.001*SL$	$0.276 + 0.001*SL$	$0.237 + 0.001*SL$
	$t_F$	0.361	$0.358 + 0.001*SL$	$0.310 + 0.001*SL$	$0.264 + 0.001*SL$
	$t_{PLH}$	1.671	$1.670 + 0.001*SL$	$1.700 + 0.000*SL$	$1.706 + 0.000*SL$
	$t_{PHL}$	1.815	$1.813 + 0.001*SL$	$1.846 + 0.001*SL$	$1.853 + 0.001*SL$

\*Group1 :  $SL < 1443$ , \*Group2 :  $1443 \leq SL \leq 2165$ , \*Group3 :  $2165 < SL$

#### PSCKDSD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.382	$0.381 + 0.001*SL$	$0.332 + 0.001*SL$	$0.291 + 0.001*SL$
	$t_F$	0.458	$0.457 + 0.001*SL$	$0.408 + 0.001*SL$	$0.360 + 0.001*SL$
	$t_{PLH}$	1.849	$1.848 + 0.000*SL$	$1.889 + 0.000*SL$	$1.901 + 0.000*SL$
	$t_{PHL}$	2.066	$2.065 + 0.001*SL$	$2.115 + 0.000*SL$	$2.131 + 0.000*SL$

\*Group1 :  $SL < 1923$ , \*Group2 :  $1923 \leq SL \leq 2887$ , \*Group3 :  $2887 < SL$



**LVC MOS Schmitt Trigger Level Input Clock Drivers**
**Switching Characteristics**

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

**PSCKDSU2**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.206	$0.200 + 0.003 \cdot \text{SL}$	$0.160 + 0.003 \cdot \text{SL}$	$0.133 + 0.003 \cdot \text{SL}$
	$t_F$	0.193	$0.186 + 0.004 \cdot \text{SL}$	$0.149 + 0.004 \cdot \text{SL}$	$0.124 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	1.168	$1.165 + 0.001 \cdot \text{SL}$	$1.168 + 0.001 \cdot \text{SL}$	$1.168 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	1.253	$1.249 + 0.002 \cdot \text{SL}$	$1.256 + 0.002 \cdot \text{SL}$	$1.255 + 0.002 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 482$ , \*Group2 :  $482 \leq \text{SL} \leq 722$ , \*Group3 :  $722 < \text{SL}$ 
**PSCKDSU4**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.276	$0.273 + 0.002 \cdot \text{SL}$	$0.225 + 0.002 \cdot \text{SL}$	$0.187 + 0.002 \cdot \text{SL}$
	$t_F$	0.268	$0.264 + 0.002 \cdot \text{SL}$	$0.220 + 0.002 \cdot \text{SL}$	$0.182 + 0.002 \cdot \text{SL}$
	$t_{PLH}$	1.435	$1.434 + 0.001 \cdot \text{SL}$	$1.451 + 0.001 \cdot \text{SL}$	$1.453 + 0.001 \cdot \text{SL}$
	$t_{PHL}$	1.545	$1.543 + 0.001 \cdot \text{SL}$	$1.562 + 0.001 \cdot \text{SL}$	$1.564 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 962$ , \*Group2 :  $962 \leq \text{SL} \leq 1443$ , \*Group3 :  $1443 < \text{SL}$ 
**PSCKDSU6**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.339	$0.337 + 0.001 \cdot \text{SL}$	$0.285 + 0.001 \cdot \text{SL}$	$0.245 + 0.001 \cdot \text{SL}$
	$t_F$	0.365	$0.362 + 0.001 \cdot \text{SL}$	$0.315 + 0.001 \cdot \text{SL}$	$0.269 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	1.651	$1.650 + 0.001 \cdot \text{SL}$	$1.681 + 0.000 \cdot \text{SL}$	$1.688 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	1.811	$1.810 + 0.001 \cdot \text{SL}$	$1.845 + 0.001 \cdot \text{SL}$	$1.853 + 0.001 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 1443$ , \*Group2 :  $1443 \leq \text{SL} \leq 2165$ , \*Group3 :  $2165 < \text{SL}$ 
**PSCKDSU8**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.394	$0.392 + 0.001 \cdot \text{SL}$	$0.342 + 0.001 \cdot \text{SL}$	$0.300 + 0.001 \cdot \text{SL}$
	$t_F$	0.469	$0.467 + 0.001 \cdot \text{SL}$	$0.418 + 0.001 \cdot \text{SL}$	$0.370 + 0.001 \cdot \text{SL}$
	$t_{PLH}$	1.835	$1.834 + 0.000 \cdot \text{SL}$	$1.877 + 0.000 \cdot \text{SL}$	$1.890 + 0.000 \cdot \text{SL}$
	$t_{PHL}$	2.066	$2.065 + 0.001 \cdot \text{SL}$	$2.117 + 0.000 \cdot \text{SL}$	$2.134 + 0.000 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 1923$ , \*Group2 :  $1923 \leq \text{SL} \leq 2887$ , \*Group3 :  $2887 < \text{SL}$



## OSCILLATORS

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### Cell List

Cell Name	Function Description
PHSOSCK1	Oscillator Cell with Enable (~ 100kHz)
PHSOSCK2	Oscillator Cell with Enable (100K ~ 1MHz)
PHSOSCK17	Oscillator Cell with Enable and Feedback Resistor 10M $\Omega$ (~ 100kHz)
PHSOSCK27	Oscillator Cell with Enable and Feedback Resistor 10M $\Omega$ (100K ~ 1MHz)
PHSOSCM1	Oscillator Cell with Enable (1M ~ 10MHz)
PHSOSCM2	Oscillator Cell with Enable (10M ~ 40MHz)
PHSOSCM3	Oscillator Cell with Enable (40M ~ 100MHz)
PHSOSCM16	Oscillator Cell with Enable and Feedback Resistor 1M $\Omega$ (1M ~ 10MHz)
PHSOSCM26	Oscillator Cell with Enable and Feedback Resistor 1M $\Omega$ (10M ~ 40MHz)
PHSOSCM36	Oscillator Cell with Enable and Feedback Resistor 1M $\Omega$ (40M ~ 100MHz)

**NOTE:** Use I/O 3.3V and Core 2.5V

Cell Name	Function Description
PSOSCK1	Oscillator Cell with Enable (~ 100kHz)
PSOSCK2	Oscillator Cell with Enable (100K ~ 1MHz)
PSOSCM1	Oscillator Cell with Enable (1M ~ 10MHz)
PSOSCM2	Oscillator Cell with Enable (10M ~ 40MHz)

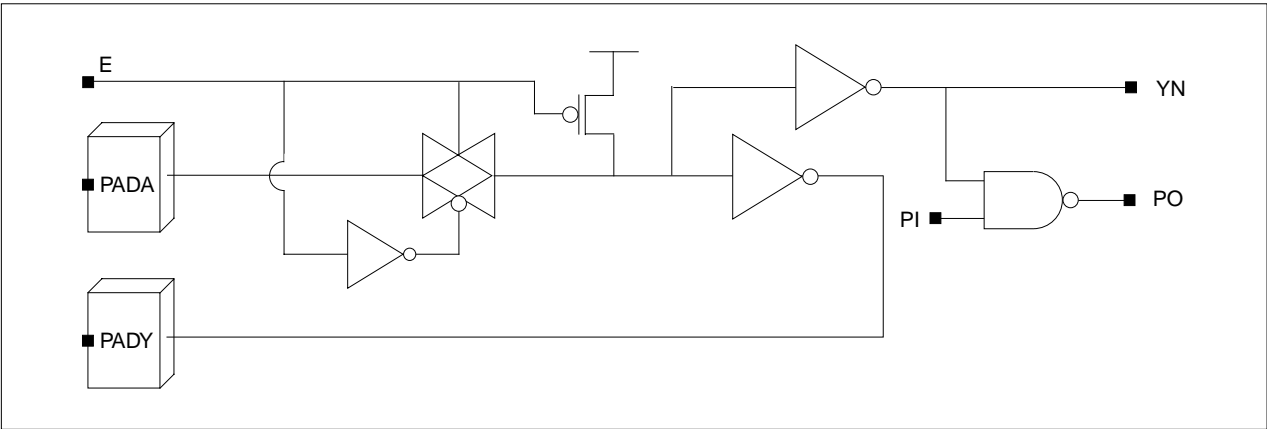
**NOTE:** Use I/O 2.5V and Core 2.5V



PHSOSCK1/K2/M1/M2/M3

Oscillator Cell with Enable

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)		I/O Sizes	
PHSOSCK1/K2	PHSOSCM1/M2/M3	PHSOSCK1/K2	PHSOSCM1/M2/M3
E	E		
3.55	3.55	2 I/O Slots	2 I/O Slots



# PHSOSCK1/K2/M1/M2/M3

## Oscillator Cell with Enable

### Switching Characteristics

#### PHSOSCK1

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	2030.800	$40.550 + 39.805 \cdot \text{CL}$	$40.800 + 39.800 \cdot \text{CL}$	$40.500 + 39.804 \cdot \text{CL}$
	$t_F$	1973.700	$39.450 + 38.685 \cdot \text{CL}$	$39.300 + 38.688 \cdot \text{CL}$	$39.600 + 38.684 \cdot \text{CL}$
	$t_{PLH}$	909.370	$19.320 + 17.801 \cdot \text{CL}$	$19.310 + 17.801 \cdot \text{CL}$	$19.400 + 17.800 \cdot \text{CL}$
	$t_{PHL}$	957.810	$20.335 + 18.749 \cdot \text{CL}$	$20.430 + 18.748 \cdot \text{CL}$	$20.100 + 18.752 \cdot \text{CL}$
E to PADY	$t_R$	2030.800	$40.550 + 39.805 \cdot \text{CL}$	$40.800 + 39.800 \cdot \text{CL}$	$40.500 + 39.804 \cdot \text{CL}$
	$t_F$	1973.700	$39.450 + 38.685 \cdot \text{CL}$	$39.300 + 38.688 \cdot \text{CL}$	$39.600 + 38.684 \cdot \text{CL}$
	$t_{PLH}$	909.250	$19.200 + 17.801 \cdot \text{CL}$	$19.150 + 17.802 \cdot \text{CL}$	$19.300 + 17.800 \cdot \text{CL}$
	$t_{PHL}$	957.470	$20.020 + 18.749 \cdot \text{CL}$	$20.010 + 18.749 \cdot \text{CL}$	$20.100 + 18.748 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.203	$0.187 + 0.008 \cdot \text{SL}$	$0.190 + 0.007 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$
	$t_F$	0.201	$0.186 + 0.007 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$	$0.200 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	10.400	$10.389 + 0.006 \cdot \text{SL}$	$10.394 + 0.004 \cdot \text{SL}$	$10.426 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	12.561	$12.550 + 0.006 \cdot \text{SL}$	$12.555 + 0.004 \cdot \text{SL}$	$12.592 + 0.004 \cdot \text{SL}$
E to YN	$t_R$	0.203	$0.187 + 0.008 \cdot \text{SL}$	$0.190 + 0.007 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$
	$t_F$	0.201	$0.186 + 0.008 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$	$0.199 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	9.676	$9.665 + 0.006 \cdot \text{SL}$	$9.669 + 0.004 \cdot \text{SL}$	$9.702 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	12.364	$12.353 + 0.006 \cdot \text{SL}$	$12.357 + 0.004 \cdot \text{SL}$	$12.396 + 0.004 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



## Switching Characteristics

## PHSOSCK2

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	261.510	$5.285 + 5.124 \cdot \text{CL}$	$5.270 + 5.125 \cdot \text{CL}$	$5.270 + 5.125 \cdot \text{CL}$
	$t_F$	246.440	$4.965 + 4.830 \cdot \text{CL}$	$4.940 + 4.830 \cdot \text{CL}$	$4.940 + 4.830 \cdot \text{CL}$
	$t_{PLH}$	96.965	$2.873 + 1.882 \cdot \text{CL}$	$2.875 + 1.882 \cdot \text{CL}$	$2.860 + 1.882 \cdot \text{CL}$
	$t_{PHL}$	97.991	$2.901 + 1.902 \cdot \text{CL}$	$2.893 + 1.902 \cdot \text{CL}$	$2.920 + 1.902 \cdot \text{CL}$
E to PADY	$t_R$	261.510	$5.285 + 5.124 \cdot \text{CL}$	$5.270 + 5.125 \cdot \text{CL}$	$5.270 + 5.125 \cdot \text{CL}$
	$t_F$	246.440	$4.965 + 4.830 \cdot \text{CL}$	$4.940 + 4.830 \cdot \text{CL}$	$4.970 + 4.830 \cdot \text{CL}$
	$t_{PLH}$	96.810	$2.720 + 1.882 \cdot \text{CL}$	$2.710 + 1.882 \cdot \text{CL}$	$2.710 + 1.882 \cdot \text{CL}$
	$t_{PHL}$	97.596	$2.503 + 1.902 \cdot \text{CL}$	$2.508 + 1.902 \cdot \text{CL}$	$2.490 + 1.902 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ (Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.187	$0.170 + 0.008 \cdot \text{SL}$	$0.175 + 0.007 \cdot \text{SL}$	$0.168 + 0.007 \cdot \text{SL}$
	$t_F$	0.177	$0.162 + 0.008 \cdot \text{SL}$	$0.166 + 0.007 \cdot \text{SL}$	$0.172 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	2.286	$2.276 + 0.005 \cdot \text{SL}$	$2.280 + 0.004 \cdot \text{SL}$	$2.306 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	2.131	$2.119 + 0.006 \cdot \text{SL}$	$2.124 + 0.004 \cdot \text{SL}$	$2.157 + 0.004 \cdot \text{SL}$
E to YN	$t_R$	0.186	$0.170 + 0.008 \cdot \text{SL}$	$0.175 + 0.007 \cdot \text{SL}$	$0.168 + 0.007 \cdot \text{SL}$
	$t_F$	0.177	$0.162 + 0.008 \cdot \text{SL}$	$0.166 + 0.007 \cdot \text{SL}$	$0.172 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	2.149	$2.138 + 0.005 \cdot \text{SL}$	$2.143 + 0.004 \cdot \text{SL}$	$2.169 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.687	$1.676 + 0.006 \cdot \text{SL}$	$1.681 + 0.004 \cdot \text{SL}$	$1.714 + 0.004 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PHSOSCK1/K2/M1/M2/M3

## Oscillator Cell with Enable

### Switching Characteristics

#### PHSOSCM1

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	16.399	$0.541 + 0.317 \cdot \text{CL}$	$0.289 + 0.322 \cdot \text{CL}$	$0.310 + 0.322 \cdot \text{CL}$
	$t_F$	17.023	$0.453 + 0.331 \cdot \text{CL}$	$0.571 + 0.329 \cdot \text{CL}$	$0.331 + 0.332 \cdot \text{CL}$
	$t_{PLH}$	8.556	$1.164 + 0.148 \cdot \text{CL}$	$1.131 + 0.149 \cdot \text{CL}$	$1.139 + 0.148 \cdot \text{CL}$
	$t_{PHL}$	9.600	$1.162 + 0.169 \cdot \text{CL}$	$1.138 + 0.169 \cdot \text{CL}$	$1.147 + 0.169 \cdot \text{CL}$
E to PADY	$t_R$	16.474	$0.549 + 0.319 \cdot \text{CL}$	$0.448 + 0.321 \cdot \text{CL}$	$0.454 + 0.320 \cdot \text{CL}$
	$t_F$	17.028	$0.513 + 0.330 \cdot \text{CL}$	$0.532 + 0.330 \cdot \text{CL}$	$0.484 + 0.331 \cdot \text{CL}$
	$t_{PLH}$	8.505	$1.045 + 0.149 \cdot \text{CL}$	$1.110 + 0.148 \cdot \text{CL}$	$1.073 + 0.148 \cdot \text{CL}$
	$t_{PHL}$	9.491	$1.019 + 0.169 \cdot \text{CL}$	$1.036 + 0.169 \cdot \text{CL}$	$1.026 + 0.169 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.140	$0.125 + 0.007 \cdot \text{SL}$	$0.126 + 0.007 \cdot \text{SL}$	$0.121 + 0.007 \cdot \text{SL}$
	$t_F$	0.128	$0.113 + 0.007 \cdot \text{SL}$	$0.116 + 0.007 \cdot \text{SL}$	$0.114 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	1.378	$1.369 + 0.004 \cdot \text{SL}$	$1.372 + 0.004 \cdot \text{SL}$	$1.384 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.140	$1.131 + 0.005 \cdot \text{SL}$	$1.134 + 0.004 \cdot \text{SL}$	$1.149 + 0.003 \cdot \text{SL}$
E to YN	$t_R$	0.139	$0.123 + 0.008 \cdot \text{SL}$	$0.126 + 0.007 \cdot \text{SL}$	$0.121 + 0.007 \cdot \text{SL}$
	$t_F$	0.128	$0.114 + 0.007 \cdot \text{SL}$	$0.116 + 0.007 \cdot \text{SL}$	$0.115 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	1.558	$1.549 + 0.004 \cdot \text{SL}$	$1.552 + 0.004 \cdot \text{SL}$	$1.565 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.243	$1.234 + 0.005 \cdot \text{SL}$	$1.237 + 0.004 \cdot \text{SL}$	$1.251 + 0.003 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



## Switching Characteristics

## PHSOSCM2

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	4.378	$0.613 + 0.075 \cdot \text{CL}$	$0.480 + 0.078 \cdot \text{CL}$	$0.361 + 0.080 \cdot \text{CL}$
	$t_F$	4.588	$0.819 + 0.075 \cdot \text{CL}$	$0.650 + 0.079 \cdot \text{CL}$	$0.499 + 0.081 \cdot \text{CL}$
	$t_{PLH}$	3.414	$1.536 + 0.038 \cdot \text{CL}$	$1.548 + 0.037 \cdot \text{CL}$	$1.546 + 0.037 \cdot \text{CL}$
	$t_{PHL}$	3.720	$1.579 + 0.043 \cdot \text{CL}$	$1.610 + 0.042 \cdot \text{CL}$	$1.612 + 0.042 \cdot \text{CL}$
E to PADY	$t_R$	4.294	$0.370 + 0.078 \cdot \text{CL}$	$0.310 + 0.080 \cdot \text{CL}$	$0.263 + 0.080 \cdot \text{CL}$
	$t_F$	4.466	$0.504 + 0.079 \cdot \text{CL}$	$0.423 + 0.081 \cdot \text{CL}$	$0.358 + 0.082 \cdot \text{CL}$
	$t_{PLH}$	3.458	$1.565 + 0.038 \cdot \text{CL}$	$1.580 + 0.038 \cdot \text{CL}$	$1.584 + 0.038 \cdot \text{CL}$
	$t_{PHL}$	3.971	$1.827 + 0.043 \cdot \text{CL}$	$1.851 + 0.042 \cdot \text{CL}$	$1.856 + 0.042 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$ (Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.109	$0.096 + 0.006 \cdot \text{SL}$	$0.095 + 0.007 \cdot \text{SL}$	$0.094 + 0.007 \cdot \text{SL}$
	$t_F$	0.095	$0.082 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	1.719	$1.711 + 0.004 \cdot \text{SL}$	$1.713 + 0.003 \cdot \text{SL}$	$1.718 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.436	$1.428 + 0.004 \cdot \text{SL}$	$1.430 + 0.004 \cdot \text{SL}$	$1.437 + 0.003 \cdot \text{SL}$
E to YN	$t_R$	0.109	$0.096 + 0.006 \cdot \text{SL}$	$0.095 + 0.007 \cdot \text{SL}$	$0.094 + 0.007 \cdot \text{SL}$
	$t_F$	0.095	$0.082 + 0.006 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	1.862	$1.855 + 0.004 \cdot \text{SL}$	$1.857 + 0.003 \cdot \text{SL}$	$1.862 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.827	$1.819 + 0.004 \cdot \text{SL}$	$1.821 + 0.004 \cdot \text{SL}$	$1.827 + 0.003 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PHSOSCK1/K2/M1/M2/M3

## Oscillator Cell with Enable

### Switching Characteristics

#### PHSOSCM3

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	2.653	$0.973 + 0.034 \cdot \text{CL}$	$1.264 + 0.028 \cdot \text{CL}$	$1.165 + 0.029 \cdot \text{CL}$
	$t_F$	2.830	$1.187 + 0.033 \cdot \text{CL}$	$1.297 + 0.031 \cdot \text{CL}$	$1.220 + 0.032 \cdot \text{CL}$
	$t_{PLH}$	3.235	$2.217 + 0.020 \cdot \text{CL}$	$2.343 + 0.018 \cdot \text{CL}$	$2.425 + 0.017 \cdot \text{CL}$
	$t_{PHL}$	3.349	$2.145 + 0.024 \cdot \text{CL}$	$2.286 + 0.021 \cdot \text{CL}$	$2.416 + 0.020 \cdot \text{CL}$
E to PADY	$t_R$	2.570	$1.026 + 0.031 \cdot \text{CL}$	$1.207 + 0.027 \cdot \text{CL}$	$0.867 + 0.032 \cdot \text{CL}$
	$t_F$	2.801	$1.194 + 0.032 \cdot \text{CL}$	$1.223 + 0.032 \cdot \text{CL}$	$1.346 + 0.030 \cdot \text{CL}$
	$t_{PLH}$	3.433	$2.410 + 0.020 \cdot \text{CL}$	$2.530 + 0.018 \cdot \text{CL}$	$2.625 + 0.017 \cdot \text{CL}$
	$t_{PHL}$	4.374	$3.161 + 0.024 \cdot \text{CL}$	$3.311 + 0.021 \cdot \text{CL}$	$3.446 + 0.019 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.093	$0.086 + 0.003 \cdot \text{SL}$	$0.086 + 0.003 \cdot \text{SL}$	$0.084 + 0.004 \cdot \text{SL}$
	$t_F$	0.074	$0.067 + 0.003 \cdot \text{SL}$	$0.067 + 0.003 \cdot \text{SL}$	$0.067 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	2.577	$2.573 + 0.002 \cdot \text{SL}$	$2.574 + 0.002 \cdot \text{SL}$	$2.582 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	2.203	$2.198 + 0.002 \cdot \text{SL}$	$2.199 + 0.002 \cdot \text{SL}$	$2.207 + 0.002 \cdot \text{SL}$
E to YN	$t_R$	0.093	$0.087 + 0.003 \cdot \text{SL}$	$0.085 + 0.003 \cdot \text{SL}$	$0.084 + 0.004 \cdot \text{SL}$
	$t_F$	0.074	$0.067 + 0.004 \cdot \text{SL}$	$0.067 + 0.003 \cdot \text{SL}$	$0.067 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	2.759	$2.755 + 0.002 \cdot \text{SL}$	$2.756 + 0.002 \cdot \text{SL}$	$2.763 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	3.209	$3.205 + 0.002 \cdot \text{SL}$	$3.206 + 0.002 \cdot \text{SL}$	$3.213 + 0.002 \cdot \text{SL}$

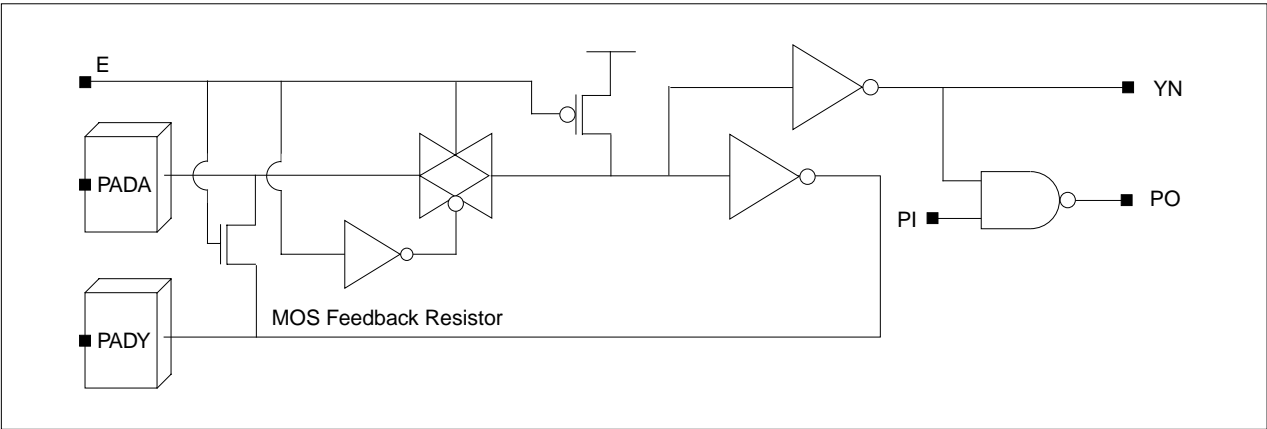
\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



PHSOSCK17/K27/M16/M26/M36

Oscillator Cell with Enable and Feedback Resistor

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)		I/O Sizes	
PHSOSCK17/K27	PHSOSCM16/M26/M36	PHSOSCK17/K27	PHSOSCM16/M26/M36
E	E		
3.55	3.55	2 I/O Slots	2 I/O Slots



# PHSOSCK17/K27/M16/M26/M36

## Oscillator Cell with Enable and 10Mohm Resistor

### Switching Characteristics

#### PHSOSCK17

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	2042.700	$42.700 + 40.000 \cdot \text{CL}$	$43.100 + 39.992 \cdot \text{CL}$	$42.800 + 39.996 \cdot \text{CL}$
	$t_F$	1997.600	$40.850 + 39.135 \cdot \text{CL}$	$41.000 + 39.132 \cdot \text{CL}$	$41.000 + 39.132 \cdot \text{CL}$
	$t_{PLH}$	905.240	$19.065 + 17.724 \cdot \text{CL}$	$19.120 + 17.722 \cdot \text{CL}$	$19.000 + 17.724 \cdot \text{CL}$
	$t_{PHL}$	959.380	$21.530 + 18.757 \cdot \text{CL}$	$21.540 + 18.757 \cdot \text{CL}$	$21.600 + 18.756 \cdot \text{CL}$
E to PADY	$t_R$	2043.000	$43.500 + 39.990 \cdot \text{CL}$	$43.400 + 39.992 \cdot \text{CL}$	$43.400 + 39.992 \cdot \text{CL}$
	$t_F$	1973.800	$39.550 + 38.685 \cdot \text{CL}$	$39.600 + 38.684 \cdot \text{CL}$	$39.300 + 38.688 \cdot \text{CL}$
	$t_{PLH}$	909.710	$19.560 + 17.803 \cdot \text{CL}$	$19.530 + 17.804 \cdot \text{CL}$	$19.800 + 17.800 \cdot \text{CL}$
	$t_{PHL}$	953.620	$21.120 + 18.650 \cdot \text{CL}$	$21.060 + 18.651 \cdot \text{CL}$	$21.300 + 18.648 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.202	$0.186 + 0.008 \cdot \text{SL}$	$0.190 + 0.007 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$
	$t_F$	0.201	$0.185 + 0.008 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$	$0.199 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	10.406	$10.396 + 0.005 \cdot \text{SL}$	$10.400 + 0.004 \cdot \text{SL}$	$10.432 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	12.617	$12.606 + 0.006 \cdot \text{SL}$	$12.611 + 0.004 \cdot \text{SL}$	$12.648 + 0.004 \cdot \text{SL}$
E to YN	$t_R$	0.202	$0.187 + 0.008 \cdot \text{SL}$	$0.190 + 0.007 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$
	$t_F$	0.201	$0.186 + 0.007 \cdot \text{SL}$	$0.189 + 0.007 \cdot \text{SL}$	$0.199 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	9.695	$9.684 + 0.006 \cdot \text{SL}$	$9.688 + 0.004 \cdot \text{SL}$	$9.720 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	12.361	$12.350 + 0.006 \cdot \text{SL}$	$12.355 + 0.004 \cdot \text{SL}$	$12.392 + 0.004 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PHSOSCK17/K27/M16/M26/M36

## Oscillator Cell with Enable and Feedback Resistor

### Switching Characteristics

#### PHSOSCK27

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	261.840	$5.415 + 5.128 \cdot \text{CL}$	$5.400 + 5.129 \cdot \text{CL}$	$5.400 + 5.129 \cdot \text{CL}$
	$t_F$	246.770	$4.995 + 4.836 \cdot \text{CL}$	$4.990 + 4.836 \cdot \text{CL}$	$4.960 + 4.836 \cdot \text{CL}$
	$t_{PLH}$	96.999	$2.934 + 1.881 \cdot \text{CL}$	$2.917 + 1.882 \cdot \text{CL}$	$2.950 + 1.881 \cdot \text{CL}$
	$t_{PHL}$	98.217	$3.074 + 1.903 \cdot \text{CL}$	$3.071 + 1.903 \cdot \text{CL}$	$3.080 + 1.903 \cdot \text{CL}$
E to PADY	$t_R$	261.890	$5.465 + 5.128 \cdot \text{CL}$	$5.470 + 5.128 \cdot \text{CL}$	$5.470 + 5.128 \cdot \text{CL}$
	$t_F$	246.440	$4.965 + 4.830 \cdot \text{CL}$	$4.940 + 4.830 \cdot \text{CL}$	$4.940 + 4.830 \cdot \text{CL}$
	$t_{PLH}$	96.895	$2.798 + 1.882 \cdot \text{CL}$	$2.785 + 1.882 \cdot \text{CL}$	$2.800 + 1.882 \cdot \text{CL}$
	$t_{PHL}$	97.654	$2.607 + 1.901 \cdot \text{CL}$	$2.602 + 1.901 \cdot \text{CL}$	$2.590 + 1.901 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.187	$0.171 + 0.008 \cdot \text{SL}$	$0.175 + 0.007 \cdot \text{SL}$	$0.168 + 0.007 \cdot \text{SL}$
	$t_F$	0.177	$0.162 + 0.008 \cdot \text{SL}$	$0.166 + 0.007 \cdot \text{SL}$	$0.172 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	2.302	$2.292 + 0.005 \cdot \text{SL}$	$2.296 + 0.004 \cdot \text{SL}$	$2.323 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	2.183	$2.172 + 0.006 \cdot \text{SL}$	$2.177 + 0.004 \cdot \text{SL}$	$2.209 + 0.004 \cdot \text{SL}$
E to YN	$t_R$	0.187	$0.171 + 0.008 \cdot \text{SL}$	$0.175 + 0.007 \cdot \text{SL}$	$0.168 + 0.007 \cdot \text{SL}$
	$t_F$	0.177	$0.163 + 0.007 \cdot \text{SL}$	$0.165 + 0.007 \cdot \text{SL}$	$0.172 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	2.161	$2.150 + 0.005 \cdot \text{SL}$	$2.154 + 0.004 \cdot \text{SL}$	$2.181 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.685	$1.674 + 0.006 \cdot \text{SL}$	$1.679 + 0.004 \cdot \text{SL}$	$1.712 + 0.004 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PHSOSCK17/K27/M16/M26/M36

## Oscillator Cell with Enable and Feedback Resistor

### Switching Characteristics

#### PHSOSCM16

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	16.421	$0.399 + 0.320 \cdot \text{CL}$	$0.367 + 0.321 \cdot \text{CL}$	$0.250 + 0.323 \cdot \text{CL}$
	$t_F$	17.016	$0.619 + 0.328 \cdot \text{CL}$	$0.498 + 0.330 \cdot \text{CL}$	$0.309 + 0.333 \cdot \text{CL}$
	$t_{PLH}$	8.557	$1.168 + 0.148 \cdot \text{CL}$	$1.122 + 0.149 \cdot \text{CL}$	$1.154 + 0.148 \cdot \text{CL}$
	$t_{PHL}$	9.628	$1.153 + 0.169 \cdot \text{CL}$	$1.179 + 0.169 \cdot \text{CL}$	$1.166 + 0.169 \cdot \text{CL}$
E to PADY	$t_R$	16.450	$0.607 + 0.317 \cdot \text{CL}$	$0.360 + 0.322 \cdot \text{CL}$	$0.420 + 0.321 \cdot \text{CL}$
	$t_F$	17.030	$0.557 + 0.329 \cdot \text{CL}$	$0.522 + 0.330 \cdot \text{CL}$	$0.543 + 0.330 \cdot \text{CL}$
	$t_{PLH}$	8.503	$1.070 + 0.149 \cdot \text{CL}$	$1.110 + 0.148 \cdot \text{CL}$	$1.034 + 0.149 \cdot \text{CL}$
	$t_{PHL}$	9.492	$1.021 + 0.169 \cdot \text{CL}$	$1.037 + 0.169 \cdot \text{CL}$	$1.029 + 0.169 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.139	$0.125 + 0.007 \cdot \text{SL}$	$0.125 + 0.007 \cdot \text{SL}$	$0.121 + 0.007 \cdot \text{SL}$
	$t_F$	0.129	$0.116 + 0.007 \cdot \text{SL}$	$0.116 + 0.007 \cdot \text{SL}$	$0.114 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	1.386	$1.378 + 0.004 \cdot \text{SL}$	$1.380 + 0.004 \cdot \text{SL}$	$1.392 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.146	$1.137 + 0.005 \cdot \text{SL}$	$1.140 + 0.004 \cdot \text{SL}$	$1.155 + 0.003 \cdot \text{SL}$
E to YN	$t_R$	0.139	$0.123 + 0.008 \cdot \text{SL}$	$0.126 + 0.007 \cdot \text{SL}$	$0.121 + 0.007 \cdot \text{SL}$
	$t_F$	0.128	$0.114 + 0.007 \cdot \text{SL}$	$0.116 + 0.007 \cdot \text{SL}$	$0.115 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	1.562	$1.553 + 0.004 \cdot \text{SL}$	$1.556 + 0.004 \cdot \text{SL}$	$1.568 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.242	$1.232 + 0.005 \cdot \text{SL}$	$1.236 + 0.004 \cdot \text{SL}$	$1.250 + 0.003 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PHSOSCK17/K27/M16/M26/M36

## Oscillator Cell with Enable and Feedback Resistor

### Switching Characteristics

#### PHSOSCM26

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	4.379	$0.612 + 0.075 \cdot \text{CL}$	$0.479 + 0.078 \cdot \text{CL}$	$0.361 + 0.080 \cdot \text{CL}$
	$t_F$	4.598	$0.829 + 0.075 \cdot \text{CL}$	$0.659 + 0.079 \cdot \text{CL}$	$0.508 + 0.081 \cdot \text{CL}$
	$t_{PLH}$	3.419	$1.540 + 0.038 \cdot \text{CL}$	$1.553 + 0.037 \cdot \text{CL}$	$1.550 + 0.037 \cdot \text{CL}$
	$t_{PHL}$	3.732	$1.588 + 0.043 \cdot \text{CL}$	$1.620 + 0.042 \cdot \text{CL}$	$1.623 + 0.042 \cdot \text{CL}$
E to PADY	$t_R$	4.297	$0.372 + 0.078 \cdot \text{CL}$	$0.312 + 0.080 \cdot \text{CL}$	$0.265 + 0.080 \cdot \text{CL}$
	$t_F$	4.466	$0.504 + 0.079 \cdot \text{CL}$	$0.423 + 0.081 \cdot \text{CL}$	$0.358 + 0.082 \cdot \text{CL}$
	$t_{PLH}$	3.463	$1.570 + 0.038 \cdot \text{CL}$	$1.585 + 0.038 \cdot \text{CL}$	$1.589 + 0.038 \cdot \text{CL}$
	$t_{PHL}$	3.970	$1.826 + 0.043 \cdot \text{CL}$	$1.851 + 0.042 \cdot \text{CL}$	$1.856 + 0.042 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.109	$0.096 + 0.006 \cdot \text{SL}$	$0.095 + 0.007 \cdot \text{SL}$	$0.093 + 0.007 \cdot \text{SL}$
	$t_F$	0.095	$0.082 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	1.725	$1.718 + 0.004 \cdot \text{SL}$	$1.719 + 0.003 \cdot \text{SL}$	$1.724 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.440	$1.432 + 0.004 \cdot \text{SL}$	$1.434 + 0.004 \cdot \text{SL}$	$1.440 + 0.003 \cdot \text{SL}$
E to YN	$t_R$	0.109	$0.096 + 0.006 \cdot \text{SL}$	$0.095 + 0.007 \cdot \text{SL}$	$0.094 + 0.007 \cdot \text{SL}$
	$t_F$	0.095	$0.081 + 0.007 \cdot \text{SL}$	$0.082 + 0.007 \cdot \text{SL}$	$0.081 + 0.007 \cdot \text{SL}$
	$t_{PLH}$	1.867	$1.860 + 0.004 \cdot \text{SL}$	$1.861 + 0.003 \cdot \text{SL}$	$1.866 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	1.826	$1.818 + 0.004 \cdot \text{SL}$	$1.820 + 0.004 \cdot \text{SL}$	$1.826 + 0.003 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PHSOSCK17/K27/M16/M26/M36

## Oscillator Cell with Enable and Feedback Resistor

### Switching Characteristics

#### PHSOSCM36

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	2.542	$0.991 + 0.031 \cdot \text{CL}$	$0.980 + 0.031 \cdot \text{CL}$	$1.262 + 0.027 \cdot \text{CL}$
	$t_F$	2.837	$1.210 + 0.033 \cdot \text{CL}$	$1.305 + 0.031 \cdot \text{CL}$	$1.221 + 0.032 \cdot \text{CL}$
	$t_{PLH}$	3.238	$2.222 + 0.020 \cdot \text{CL}$	$2.339 + 0.018 \cdot \text{CL}$	$2.440 + 0.017 \cdot \text{CL}$
	$t_{PHL}$	3.357	$2.147 + 0.024 \cdot \text{CL}$	$2.296 + 0.021 \cdot \text{CL}$	$2.419 + 0.020 \cdot \text{CL}$
E to PADY	$t_R$	2.482	$1.095 + 0.028 \cdot \text{CL}$	$0.589 + 0.038 \cdot \text{CL}$	$1.624 + 0.024 \cdot \text{CL}$
	$t_F$	2.797	$1.165 + 0.033 \cdot \text{CL}$	$1.216 + 0.032 \cdot \text{CL}$	$1.349 + 0.030 \cdot \text{CL}$
	$t_{PLH}$	3.437	$2.415 + 0.020 \cdot \text{CL}$	$2.533 + 0.018 \cdot \text{CL}$	$2.633 + 0.017 \cdot \text{CL}$
	$t_{PHL}$	4.373	$3.160 + 0.024 \cdot \text{CL}$	$3.310 + 0.021 \cdot \text{CL}$	$3.443 + 0.019 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

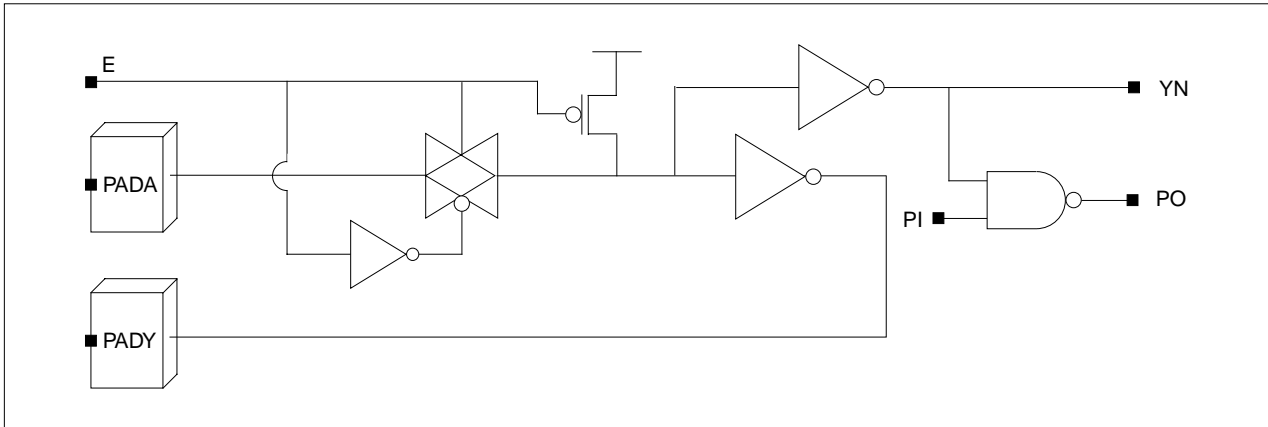
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.093	$0.086 + 0.003 \cdot \text{SL}$	$0.086 + 0.003 \cdot \text{SL}$	$0.084 + 0.004 \cdot \text{SL}$
	$t_F$	0.074	$0.067 + 0.003 \cdot \text{SL}$	$0.067 + 0.003 \cdot \text{SL}$	$0.066 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	2.582	$2.577 + 0.002 \cdot \text{SL}$	$2.579 + 0.002 \cdot \text{SL}$	$2.586 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	2.207	$2.202 + 0.002 \cdot \text{SL}$	$2.204 + 0.002 \cdot \text{SL}$	$2.211 + 0.002 \cdot \text{SL}$
E to YN	$t_R$	0.093	$0.087 + 0.003 \cdot \text{SL}$	$0.085 + 0.003 \cdot \text{SL}$	$0.084 + 0.004 \cdot \text{SL}$
	$t_F$	0.074	$0.067 + 0.003 \cdot \text{SL}$	$0.066 + 0.004 \cdot \text{SL}$	$0.066 + 0.004 \cdot \text{SL}$
	$t_{PLH}$	2.764	$2.760 + 0.002 \cdot \text{SL}$	$2.761 + 0.002 \cdot \text{SL}$	$2.769 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	3.207	$3.202 + 0.002 \cdot \text{SL}$	$3.204 + 0.002 \cdot \text{SL}$	$3.211 + 0.002 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



## Oscillator Cell with Enable

## Logic Symbol



## Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

## Cell Data

Input Load (SL)		I/O Sizes	
<i>PSOSCK1/K2</i>	<i>PSOSCM1/M2</i>	<i>PSOSCK1/K2</i>	<i>PSOSCM1/M2</i>
E	E		
3.49	3.49	2 I/O Slots	2 I/O Slots



# PSOSCK1/K2/M1/M2

## Oscillator Cell with Enable

### Switching Characteristics

#### PSOSCK1

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	2059.600	$79.600 + 39.600 \cdot \text{CL}$	$79.400 + 39.604 \cdot \text{CL}$	$79.400 + 39.604 \cdot \text{CL}$
	$t_F$	1941.400	$72.400 + 37.380 \cdot \text{CL}$	$72.400 + 37.380 \cdot \text{CL}$	$72.100 + 37.384 \cdot \text{CL}$
	$t_{PLH}$	885.410	$33.110 + 17.046 \cdot \text{CL}$	$33.030 + 17.048 \cdot \text{CL}$	$33.300 + 17.044 \cdot \text{CL}$
	$t_{PHL}$	872.610	$36.035 + 16.732 \cdot \text{CL}$	$36.030 + 16.732 \cdot \text{CL}$	$36.000 + 16.732 \cdot \text{CL}$
E to PADY	$t_R$	2059.600	$79.600 + 39.600 \cdot \text{CL}$	$79.400 + 39.604 \cdot \text{CL}$	$79.400 + 39.604 \cdot \text{CL}$
	$t_F$	1941.400	$72.400 + 37.380 \cdot \text{CL}$	$72.400 + 37.380 \cdot \text{CL}$	$72.100 + 37.384 \cdot \text{CL}$
	$t_{PLH}$	884.940	$32.615 + 17.047 \cdot \text{CL}$	$32.620 + 17.046 \cdot \text{CL}$	$32.800 + 17.044 \cdot \text{CL}$
	$t_{PHL}$	872.030	$35.455 + 16.732 \cdot \text{CL}$	$35.490 + 16.731 \cdot \text{CL}$	$35.400 + 16.732 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.179	$0.164 + 0.008 \cdot \text{SL}$	$0.167 + 0.007 \cdot \text{SL}$	$0.161 + 0.007 \cdot \text{SL}$
	$t_F$	0.169	$0.153 + 0.008 \cdot \text{SL}$	$0.158 + 0.006 \cdot \text{SL}$	$0.160 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	9.684	$9.674 + 0.005 \cdot \text{SL}$	$9.678 + 0.004 \cdot \text{SL}$	$9.702 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	9.212	$9.201 + 0.005 \cdot \text{SL}$	$9.205 + 0.004 \cdot \text{SL}$	$9.234 + 0.003 \cdot \text{SL}$
E to YN	$t_R$	0.179	$0.162 + 0.009 \cdot \text{SL}$	$0.168 + 0.007 \cdot \text{SL}$	$0.162 + 0.007 \cdot \text{SL}$
	$t_F$	0.169	$0.153 + 0.008 \cdot \text{SL}$	$0.158 + 0.006 \cdot \text{SL}$	$0.160 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	8.619	$8.609 + 0.005 \cdot \text{SL}$	$8.613 + 0.004 \cdot \text{SL}$	$8.637 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	8.790	$8.779 + 0.005 \cdot \text{SL}$	$8.783 + 0.004 \cdot \text{SL}$	$8.812 + 0.003 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PSOSCK1/K2/M1/M2

## Oscillator Cell with Enable

### Switching Characteristics

#### PSOSCK2

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	312.740	$12.140 + 6.012 \cdot \text{CL}$	$12.160 + 6.012 \cdot \text{CL}$	$12.160 + 6.012 \cdot \text{CL}$
	$t_F$	302.800	$11.250 + 5.831 \cdot \text{CL}$	$11.260 + 5.831 \cdot \text{CL}$	$11.230 + 5.831 \cdot \text{CL}$
	$t_{PLH}$	113.550	$4.822 + 2.175 \cdot \text{CL}$	$4.830 + 2.174 \cdot \text{CL}$	$4.830 + 2.174 \cdot \text{CL}$
	$t_{PHL}$	126.860	$5.765 + 2.422 \cdot \text{CL}$	$5.760 + 2.422 \cdot \text{CL}$	$5.760 + 2.422 \cdot \text{CL}$
E to PADY	$t_R$	312.730	$12.155 + 6.012 \cdot \text{CL}$	$12.130 + 6.012 \cdot \text{CL}$	$12.160 + 6.012 \cdot \text{CL}$
	$t_F$	302.800	$11.250 + 5.831 \cdot \text{CL}$	$11.260 + 5.831 \cdot \text{CL}$	$11.230 + 5.831 \cdot \text{CL}$
	$t_{PLH}$	113.090	$4.375 + 2.174 \cdot \text{CL}$	$4.350 + 2.175 \cdot \text{CL}$	$4.380 + 2.174 \cdot \text{CL}$
	$t_{PHL}$	126.470	$5.363 + 2.422 \cdot \text{CL}$	$5.370 + 2.422 \cdot \text{CL}$	$5.370 + 2.422 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.183	$0.168 + 0.008 \cdot \text{SL}$	$0.171 + 0.007 \cdot \text{SL}$	$0.165 + 0.007 \cdot \text{SL}$
	$t_F$	0.174	$0.159 + 0.007 \cdot \text{SL}$	$0.163 + 0.006 \cdot \text{SL}$	$0.165 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	1.034	$1.024 + 0.005 \cdot \text{SL}$	$1.028 + 0.004 \cdot \text{SL}$	$1.052 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.984	$0.973 + 0.005 \cdot \text{SL}$	$0.977 + 0.004 \cdot \text{SL}$	$1.006 + 0.003 \cdot \text{SL}$
E to YN	$t_R$	0.173	$0.156 + 0.008 \cdot \text{SL}$	$0.161 + 0.007 \cdot \text{SL}$	$0.156 + 0.007 \cdot \text{SL}$
	$t_F$	0.162	$0.147 + 0.008 \cdot \text{SL}$	$0.151 + 0.006 \cdot \text{SL}$	$0.154 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.760	$0.750 + 0.005 \cdot \text{SL}$	$0.754 + 0.004 \cdot \text{SL}$	$0.777 + 0.003 \cdot \text{SL}$
	$t_{PHL}$	0.737	$0.726 + 0.005 \cdot \text{SL}$	$0.731 + 0.004 \cdot \text{SL}$	$0.758 + 0.003 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PSOSCK1/K2/M1/M2

## Oscillator Cell with Enable

### Switching Characteristics

#### PSOSCM1

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	17.123	$0.623 + 0.330 \cdot \text{CL}$	$0.771 + 0.327 \cdot \text{CL}$	$0.726 + 0.328 \cdot \text{CL}$
	$t_F$	14.433	$0.838 + 0.272 \cdot \text{CL}$	$0.601 + 0.277 \cdot \text{CL}$	$0.520 + 0.278 \cdot \text{CL}$
	$t_{PLH}$	8.392	$1.252 + 0.143 \cdot \text{CL}$	$1.187 + 0.144 \cdot \text{CL}$	$1.210 + 0.144 \cdot \text{CL}$
	$t_{PHL}$	7.916	$1.254 + 0.133 \cdot \text{CL}$	$1.215 + 0.134 \cdot \text{CL}$	$1.264 + 0.133 \cdot \text{CL}$
E to PADY	$t_R$	17.057	$0.557 + 0.330 \cdot \text{CL}$	$0.597 + 0.329 \cdot \text{CL}$	$0.738 + 0.327 \cdot \text{CL}$
	$t_F$	14.461	$0.695 + 0.275 \cdot \text{CL}$	$0.651 + 0.276 \cdot \text{CL}$	$0.576 + 0.277 \cdot \text{CL}$
	$t_{PLH}$	8.003	$0.780 + 0.144 \cdot \text{CL}$	$0.823 + 0.144 \cdot \text{CL}$	$0.826 + 0.144 \cdot \text{CL}$
	$t_{PHL}$	7.640	$0.925 + 0.134 \cdot \text{CL}$	$0.937 + 0.134 \cdot \text{CL}$	$0.986 + 0.133 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.259	$0.229 + 0.015 \cdot \text{SL}$	$0.224 + 0.016 \cdot \text{SL}$	$0.192 + 0.017 \cdot \text{SL}$
	$t_F$	0.235	$0.198 + 0.018 \cdot \text{SL}$	$0.200 + 0.018 \cdot \text{SL}$	$0.179 + 0.018 \cdot \text{SL}$
	$t_{PLH}$	1.022	$1.003 + 0.009 \cdot \text{SL}$	$1.008 + 0.008 \cdot \text{SL}$	$1.021 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	1.065	$1.043 + 0.011 \cdot \text{SL}$	$1.048 + 0.010 \cdot \text{SL}$	$1.065 + 0.009 \cdot \text{SL}$
E to YN	$t_R$	0.252	$0.222 + 0.015 \cdot \text{SL}$	$0.217 + 0.017 \cdot \text{SL}$	$0.188 + 0.017 \cdot \text{SL}$
	$t_F$	0.228	$0.192 + 0.018 \cdot \text{SL}$	$0.192 + 0.018 \cdot \text{SL}$	$0.174 + 0.018 \cdot \text{SL}$
	$t_{PLH}$	0.825	$0.807 + 0.009 \cdot \text{SL}$	$0.811 + 0.008 \cdot \text{SL}$	$0.823 + 0.008 \cdot \text{SL}$
	$t_{PHL}$	0.989	$0.966 + 0.011 \cdot \text{SL}$	$0.971 + 0.010 \cdot \text{SL}$	$0.986 + 0.009 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PSOSCK1/K2/M1/M2

## Oscillator Cell with Enable

### Switching Characteristics

#### PSOSCM2

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	$t_R$	4.764	$0.945 + 0.076 \cdot \text{CL}$	$1.199 + 0.071 \cdot \text{CL}$	$0.774 + 0.077 \cdot \text{CL}$
	$t_F$	4.163	$1.162 + 0.060 \cdot \text{CL}$	$0.909 + 0.065 \cdot \text{CL}$	$0.914 + 0.065 \cdot \text{CL}$
	$t_{PLH}$	3.306	$1.509 + 0.036 \cdot \text{CL}$	$1.509 + 0.036 \cdot \text{CL}$	$1.556 + 0.035 \cdot \text{CL}$
	$t_{PHL}$	3.235	$1.479 + 0.035 \cdot \text{CL}$	$1.541 + 0.034 \cdot \text{CL}$	$1.581 + 0.033 \cdot \text{CL}$
E to PADY	$t_R$	4.631	$0.496 + 0.083 \cdot \text{CL}$	$0.768 + 0.077 \cdot \text{CL}$	$0.667 + 0.079 \cdot \text{CL}$
	$t_F$	3.953	$0.486 + 0.069 \cdot \text{CL}$	$0.520 + 0.069 \cdot \text{CL}$	$0.462 + 0.069 \cdot \text{CL}$
	$t_{PLH}$	2.971	$1.152 + 0.036 \cdot \text{CL}$	$1.177 + 0.036 \cdot \text{CL}$	$1.139 + 0.036 \cdot \text{CL}$
	$t_{PHL}$	3.245	$1.505 + 0.035 \cdot \text{CL}$	$1.565 + 0.034 \cdot \text{CL}$	$1.577 + 0.033 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	$t_R$	0.094	$0.083 + 0.005 \cdot \text{SL}$	$0.083 + 0.005 \cdot \text{SL}$	$0.078 + 0.005 \cdot \text{SL}$
	$t_F$	0.097	$0.087 + 0.005 \cdot \text{SL}$	$0.085 + 0.005 \cdot \text{SL}$	$0.079 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	1.123	$1.117 + 0.003 \cdot \text{SL}$	$1.118 + 0.003 \cdot \text{SL}$	$1.122 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	1.082	$1.074 + 0.004 \cdot \text{SL}$	$1.076 + 0.003 \cdot \text{SL}$	$1.083 + 0.003 \cdot \text{SL}$
E to YN	$t_R$	0.086	$0.075 + 0.005 \cdot \text{SL}$	$0.075 + 0.005 \cdot \text{SL}$	$0.074 + 0.005 \cdot \text{SL}$
	$t_F$	0.088	$0.077 + 0.006 \cdot \text{SL}$	$0.077 + 0.006 \cdot \text{SL}$	$0.072 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.928	$0.922 + 0.003 \cdot \text{SL}$	$0.923 + 0.003 \cdot \text{SL}$	$0.926 + 0.002 \cdot \text{SL}$
	$t_{PHL}$	1.263	$1.255 + 0.004 \cdot \text{SL}$	$1.257 + 0.003 \cdot \text{SL}$	$1.262 + 0.003 \cdot \text{SL}$

\*Group1 : SL < 3, \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



# PCI BUFFERS

## Overview

PCI buffers are designed for PCI local bus application which is intended for high-performance 32-bit or 64-bit bus architecture.

SEC supports PCI input, output and bi-directional buffers for 3.3V and 5V signaling environment.

## Features

- 0.24  $\mu\text{m}$ , low-power, high performance CMOS Technology
- Input, output, and bi-directional PCI buffers
- PCI local bus specification rev2.1 compliant
- Operating at up to 66MHz, including 33MHz
- Electrically compliant interface in 3.3V and 5V bus environments

## Description

These PCI buffers are designed for 3.3V and 5V environments. These buffers are compliant with the PCI local bus specification rev2.1. The PCI buffers for 66MHz can be available in 33MHz interface, but require more power pads due to their fast and noisy characteristics. The 5V tolerant PCI buffers can be used for 33MHz, 5V environment. These tolerant PCI buffers require 5V power for bulk of PMOS driver for 5V bus environment or 3.3V power for 3.3V environment. The 5V tolerant PCI drivers support 5V environment while EN5V is low. Although tolerant PCI buffers support 5V environment, they do not drive 5V.

**NOTE:** If you want to use PCI buffers, please contact SEC.

## Cell List

Cell Name	Description	Operating Frequency	Operating Voltage
PTBPCI	bi-direction	Up to 33MHz at 5V signaling <sup>(note1)</sup> Up to 66MHz at 3.3V signaling	3.3V
PTOPCI	driver	Up to 33MHz at 5V signaling Up to 66MHz at 3.3V signaling	
PTIPCI	receiver	Up to 33MHz at 5V signaling Up to 66MHz at 3.3V signaling	

**NOTE1:** 3.3V signaling conditions: EN5V=high, VIO=3.3V, 5V tolerant is not supported.  
5V signaling conditions: EN5V=low, VIO=5V, and 5V tolerant is supported.

Power Cell Name	Description
VDD2I_PCI	2.5V Power cell for internal core and PCI I/Os
VDD3OP_PCI	3.3V Power cell for PCI I/Os
VDD5O_PCI	VIO(3.3V or 5V) Power cell for PCI I/Os <sup>(note2)</sup>
VSSI_PCI	Gnd Power cell for internal core; not used for PCI I/Os
VSSOP_PCI	Gnd Power cell for PCI I/Os

**NOTE2:** In 3.3V signaling, VIO is 3.3V, which is provided through the vdd5o\_pci power cell.  
In 5V signaling, VIO is 5V, which is provided through the vdd5o\_pci power cell.



## Option <sup>(note3)</sup>

Cell Name	Description
vdet_110pci	3.3V or 5V voltage detector

**NOTE3:** Voltage detector circuit will automatically set the EN5V pin either high or low according to VIO voltage level.

## Electrical Characteristics

### DC Characteristics

Symbol	Parameter	3.3V Signaling			5V Signaling			Unit
		Condition	Min	Max	Condition	Min	Max	
V <sub>CC</sub>	Supply Voltage		3.0	3.6		3.0	3.6	V
V <sub>IO</sub>	V <sub>dd5o</sub> Voltage		V <sub>CC</sub>			4.75	5.25	V
V <sub>ih</sub>	Input high voltage		0.47V <sub>CC</sub>	V <sub>CC</sub> +0.5		1.9	V <sub>IO</sub> +0.5	V
V <sub>il</sub>	Input low voltage		− 0.5	0.33V <sub>CC</sub>		− 0.5	0.9	V
I <sub>i</sub>	Input leakage current	0 < V <sub>IN</sub> < V <sub>CC</sub>	−10	10	0 < V <sub>IN</sub> < V <sub>IO</sub>	−70	70	μA
V <sub>oh</sub>	Output high voltage	I <sub>OUT</sub> = −500 μA	0.9V <sub>CC</sub>	−	I <sub>OUT</sub> = −2mA	2.4	−	V
V <sub>ol</sub>	Output low voltage	I <sub>OUT</sub> = 1500 μA	−	0.1V <sub>CC</sub>	I <sub>OUT</sub> = 6mA	−	0.55	V

### AC Characteristics

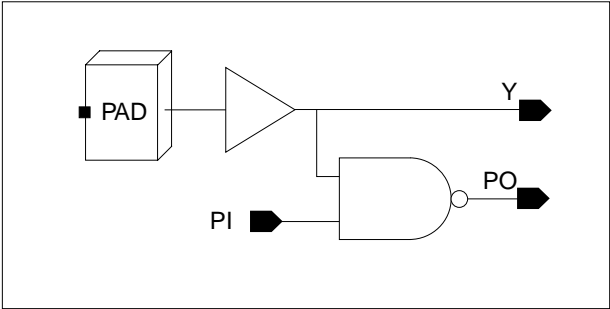
Symbol	Parameter	3.3V Signaling			5V Signaling			Unit
		Condition	Min	Max	Condition	Min	Max	
I <sub>oh</sub> (AC)	Switching current high	V <sub>OUT</sub> = 0.3V <sub>CC</sub>	−12V <sub>CC</sub>		V <sub>OUT</sub> = 1.4V	−44		mA
		V <sub>OUT</sub> = 0.7V <sub>CC</sub>		−32V <sub>CC</sub>	V <sub>OUT</sub> = 2.4V	− 2.33		
		V <sub>OUT</sub> = 0.9V <sub>CC</sub>	−1.71V <sub>CC</sub>		V <sub>OUT</sub> = 3.0V		− 142	
I <sub>ol</sub> (AC)	Switching current low	V <sub>OUT</sub> = 0.6V <sub>CC</sub>	16V <sub>CC</sub>		V <sub>OUT</sub> = 2.2V	95		mA
		V <sub>OUT</sub> = 0.1V <sub>CC</sub>	2.67V <sub>CC</sub>		V <sub>OUT</sub> = 0.55V	23.9		
		V <sub>OUT</sub> = 0.18V <sub>CC</sub>		38V <sub>CC</sub>	V <sub>OUT</sub> = 0.71V		206	
I <sub>cl</sub>	Low clamp current	− 3 < V <sub>IN</sub> ≤ −1	−25 + (V <sub>IN</sub> + 1) / 0.015		− 5 < V <sub>IN</sub> ≤ −1	−25 + (V <sub>IN</sub> + 1) / 0.015		mA
I <sub>ch</sub>	High clamp current	V <sub>CC</sub> +1 ≤ V <sub>IN</sub> < V <sub>CC</sub> +4	25 + (V <sub>IN</sub> − V <sub>CC</sub> − 1) / 0.015					mA
T <sub>r</sub>	Output rise time	0.3V <sub>CC</sub> to 0.6V <sub>CC</sub>	1.0	4.0	0.4V to 2.4V	1.0	5.0	V/ns
T <sub>f</sub>	Output fall time	0.6V <sub>CC</sub> to 0.3V <sub>CC</sub>	1.0	4.0	2.4V to 0.4V	1.0	5.0	V/ns



# PTIPCI

## 5V-tolerant PCI Input Buffers

Logic Symbol



Truth Table

Input Truth Table			
PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

### Switching Characteristics

(Typical process, 25°C, 2.5V, 3.3V, t<sub>R</sub>/t<sub>F</sub> = 3.00ns, SL: Standard Load)

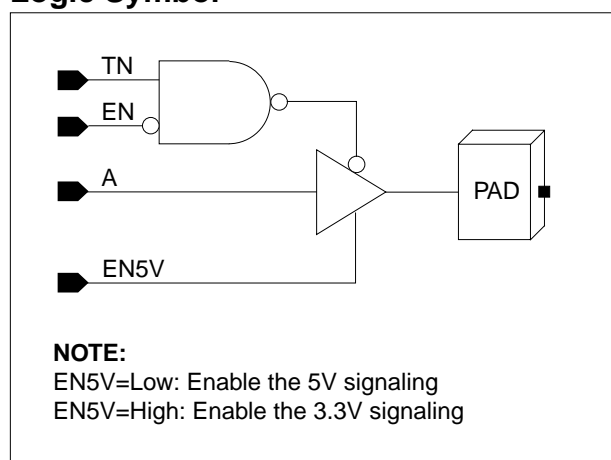
PTIPCI

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t <sub>R</sub>	0.271	0.261 + 0.005*SL	0.261 + 0.005*SL	0.265 + 0.005*SL
	t <sub>F</sub>	0.135	0.131 + 0.002*SL	0.132 + 0.002*SL	0.143 + 0.001*SL
	t <sub>PLH</sub>	0.322	0.318 + 0.002*SL	0.319 + 0.002*SL	0.326 + 0.002*SL
	t <sub>PHL</sub>	0.798	0.793 + 0.002*SL	0.795 + 0.002*SL	0.818 + 0.001*SL

\*Group1 : SL < 3, \*Group2 : 3 ≤ SL ≤ 45, \*Group3 : 45 < SL



## Logic Symbol



## Truth Table

Output Truth Table			
A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

Switching Characteristics (Typical process, 25°C, 2.5V, 3.3V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load)

## PTOPCI

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	2.110	$0.782 + 0.026 \cdot \text{CL}$	$0.764 + 0.027 \cdot \text{CL}$	$0.706 + 0.028 \cdot \text{CL}$
	$t_F$	2.513	$0.718 + 0.035 \cdot \text{CL}$	$0.675 + 0.037 \cdot \text{CL}$	$0.611 + 0.038 \cdot \text{CL}$
	$t_{PLH}$	2.452	$1.374 + 0.024 \cdot \text{CL}$	$1.557 + 0.018 \cdot \text{CL}$	$1.663 + 0.016 \cdot \text{CL}$
	$t_{PHL}$	2.087	$0.994 + 0.022 \cdot \text{CL}$	$1.039 + 0.021 \cdot \text{CL}$	$1.069 + 0.020 \cdot \text{CL}$
TN to PAD	$t_R$	2.111	$0.792 + 0.026 \cdot \text{CL}$	$0.767 + 0.027 \cdot \text{CL}$	$0.707 + 0.028 \cdot \text{CL}$
	$t_F$	2.289	$0.355 + 0.039 \cdot \text{CL}$	$0.349 + 0.039 \cdot \text{CL}$	$0.337 + 0.039 \cdot \text{CL}$
	$t_{PLH}$	2.635	$1.554 + 0.024 \cdot \text{CL}$	$1.739 + 0.018 \cdot \text{CL}$	$1.845 + 0.016 \cdot \text{CL}$
	$t_{PHL}$	2.081	$0.981 + 0.023 \cdot \text{CL}$	$1.035 + 0.021 \cdot \text{CL}$	$1.060 + 0.020 \cdot \text{CL}$
	$t_{PLZ}$	0.727	$0.727 + 0.000 \cdot \text{CL}$	$0.727 + 0.000 \cdot \text{CL}$	$0.727 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.274	$1.274 + 0.000 \cdot \text{CL}$	$1.273 + 0.000 \cdot \text{CL}$	$1.273 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	2.111	$0.792 + 0.026 \cdot \text{CL}$	$0.768 + 0.027 \cdot \text{CL}$	$0.707 + 0.028 \cdot \text{CL}$
	$t_F$	2.289	$0.354 + 0.039 \cdot \text{CL}$	$0.349 + 0.039 \cdot \text{CL}$	$0.337 + 0.039 \cdot \text{CL}$
	$t_{PLH}$	2.693	$1.612 + 0.024 \cdot \text{CL}$	$1.798 + 0.018 \cdot \text{CL}$	$1.904 + 0.016 \cdot \text{CL}$
	$t_{PHL}$	2.139	$1.039 + 0.023 \cdot \text{CL}$	$1.094 + 0.021 \cdot \text{CL}$	$1.118 + 0.020 \cdot \text{CL}$
	$t_{PLZ}$	0.742	$0.742 + 0.000 \cdot \text{CL}$	$0.742 + 0.000 \cdot \text{CL}$	$0.742 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.289	$1.289 + 0.000 \cdot \text{CL}$	$1.288 + 0.000 \cdot \text{CL}$	$1.288 + 0.000 \cdot \text{CL}$

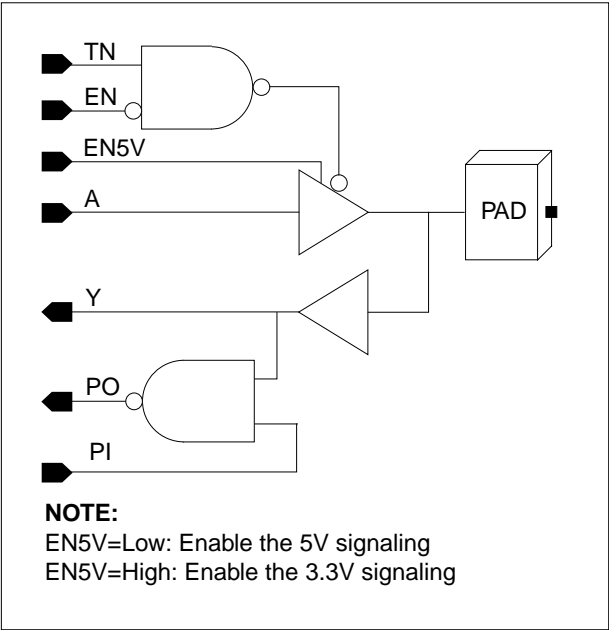
\*Group1 : CL < 30, \*Group2 :  $30 \leq \text{CL} \leq 50$ , \*Group3 :  $50 < \text{CL}$



PTBPCI

5V-Tolerant PCI Bidirectional Buffer

Logic Symbol



Truth Table

Input Truth Table

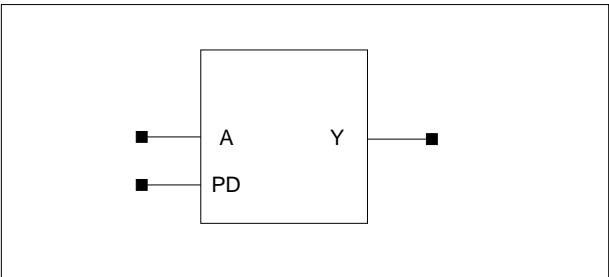
PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

Option:

Logic Symbol



Truth Table

Input		Output
A	PD	Y
3.3V		1
5V		0
X	0	Last Y
X	1	Last Y

Cell Data

Cell Name	Detecting Voltage
vdet_110pci	3.3V, 5V



## USB (Universal Serial Bus) I/O Buffers *(Under Development)*

### Overview

USB I/O buffer consists of a differential input receiver, a differential output driver, two single-ended receivers, and two pads. The differential input receiver has the 0.8V ~ 2.5V common mode input voltage range and both of the two single-ended receivers have 0.8V and 2.0V as their low and high input threshold voltages,  $V_{IL}$ ,  $V_{IH}$ , respectively.

For low power consumption in a stand-by mode, the suspend pin (SUSPND) of the receiver and the driver should be in the high state. The differential output drivers have a Low/Full speed control pin (SPEED) to select the operation speed and have Output Enable Negative pin (OEN) to achieve a bi-directional half duplex operation.

### Features

- Complies with universal serial bus specification 1.0
- Supports 12Mbps “Full speed” and 1.5Mbps “Low speed” serial data transmission
- Supports both “Full speed” and “Low speed” Design Kits
- Supports both “Full speed only” and “Low speed only” cells to reduce silicon area

### Electrical Specifications

#### DC Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2)	Min	Max	Unit
Supply Current					
Suspend Device	I <sub>CCS</sub>			10	μA
Leakage Current					
Hi-Z State Input Leakage	I <sub>LO</sub>	0V < VIN < 3.3V	−10	10	μA
Input Levels					
Differential Input Sensitivity	V <sub>DI</sub>	I (D+) – (D-) I	0.2		V
Differential Common Mode Range	V <sub>CM</sub>	Includes V <sub>DI</sub> range	0.8	2.5	
Single Ended Receiver Threshold	V <sub>SE</sub>		0.8	2.0	
Output Levels					
Static Output Low	V <sub>OL</sub>	R <sub>L</sub> of 1.5kΩ to 3.6V		0.3	V
Static Output High	V <sub>OH</sub>	R <sub>L</sub> of 15kΩ to GND	2.8	3.6	
Capacitance					
Transceiver Capacitance	C <sub>IN</sub>	Pin to GND		20	pF

#### Full Speed Output Buffer Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2, 3)	Min	Max	Unit
<b>Driver Characteristics</b>					
Transition Time		Notes 5 and Figure 1			ns
Rise Time	$T_R$	$C_L = 50pF$	4.0	20.0	
Fall Time	$T_F$	$C_L = 50pF$	4.0	20.0	
Rise/Fall Time Matching	$T_{RFM}$	$(T_R/T_F)$	90	110	%
Output Signal Crossover Voltage	$V_{CRS}$		1.3	2.0	V
Drive Output Resistance	$Z_{DRV}$	Steady state drive	28	43	$\Omega$



## USB (Universal Serial Bus) I/O Buffers *(Under Development)*

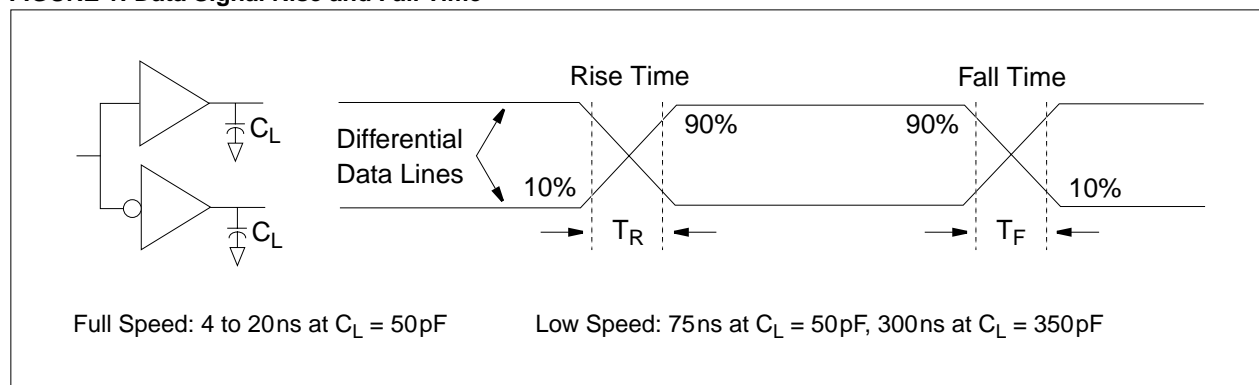
### Low Speed Output Buffer Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2, 4)	Min	Max	Unit
<b>Driver Characteristics</b>					
Transition Time Rise Time	$T_R$	Notes 5 and Figure 1 $C_L = 50\text{pF}$	75		ns
Fall Time	$T_F$	$C_L = 350\text{pF}$ $C_L = 50\text{pF}$ $C_L = 350\text{pF}$	75	300	
Rise/Fall Time Matching	$T_{RFM}$	$(T_R/T_F)$	80	120	%
Output Signal Crossover Voltage	$V_{CRS}$		1.3	2.0	V

#### NOTES:

1. All voltages are measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load ( $C_L$ ) to ground of 50pF, unless otherwise specified.
3. Full speed timings have a 1.5k $\Omega$  pull-up to 2.8V on the DP data line.
4. Low speed timings have a 1.5k $\Omega$  pull-up to 2.8V on the DN data line.
5. Measured from 10% to 90% of the data signal.

**FIGURE 1: Data Signal Rise and Fall Time**



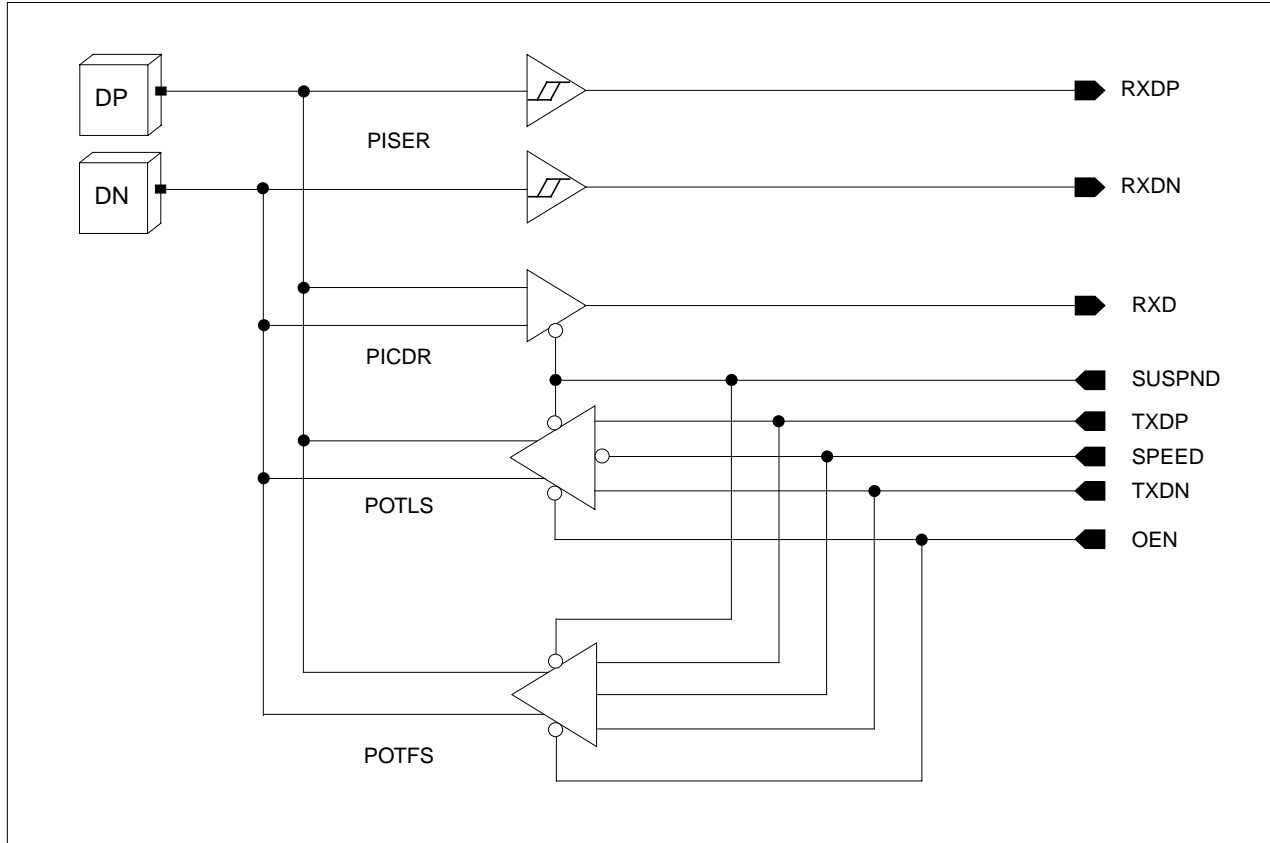
### Cell List

Cell Name	Function Description
PBUSB/PBUSB1	Low/Full speed USB Buffer (1.5MHz/12MHz select)
PBUSB_LS	Low speed only USB Buffer (1.5MHz only, reduced cell size)
PBUSB_FS	Full speed only USB Buffer (12MHz only, reduced cell size)



## PBUSB/PBUSB1

### Symbol



### Pin Connection

Input	Output	Bi-Direction
TXDP	RXDP	DP
TXDN	RXDN	DN
SUSPND	RXD	
OEN		
SPEED		

### Cell Structure

**PBUSB** = PISER + PICDR + POTLS + POTFS

**PBUSB1** = PISER + PICDR + POTLS + POTFS

There only exists PBUSB not PBUSB1 in the physical DB. The division of cell name (PBUSB/PBUSB1) is caused to notify their different working-mode. PBUSB selects POTLS (SPEED=0) to work on the Low Speed Mode. PBUSB1 selects POTFS (SPEED=1) to work on the Full Speed Mode. In case that the physical area is critical, Low speed only (PBUSB\_LS) or Full speed only (PBUSB\_FS) USB IO cell would be provided at the request of the customer, i.e.

**PBUSB\_LS** = PISER + PICDR + POTLS

**PBUSB\_FS** = PISER + PICDR + POTFS

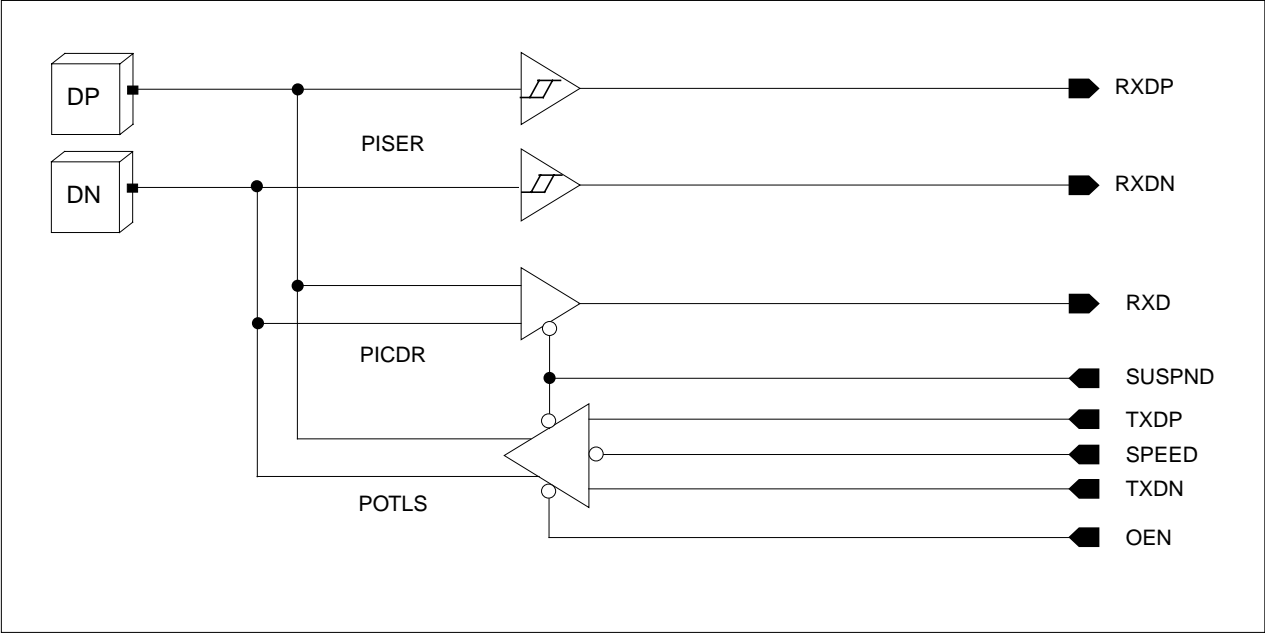


PBUSB/PBUSB1/PBUSB\_LS/PBUSB\_FS (Under Development)

Universal Serial Bus I/O Buffer

PBUSB\_LS

Symbol



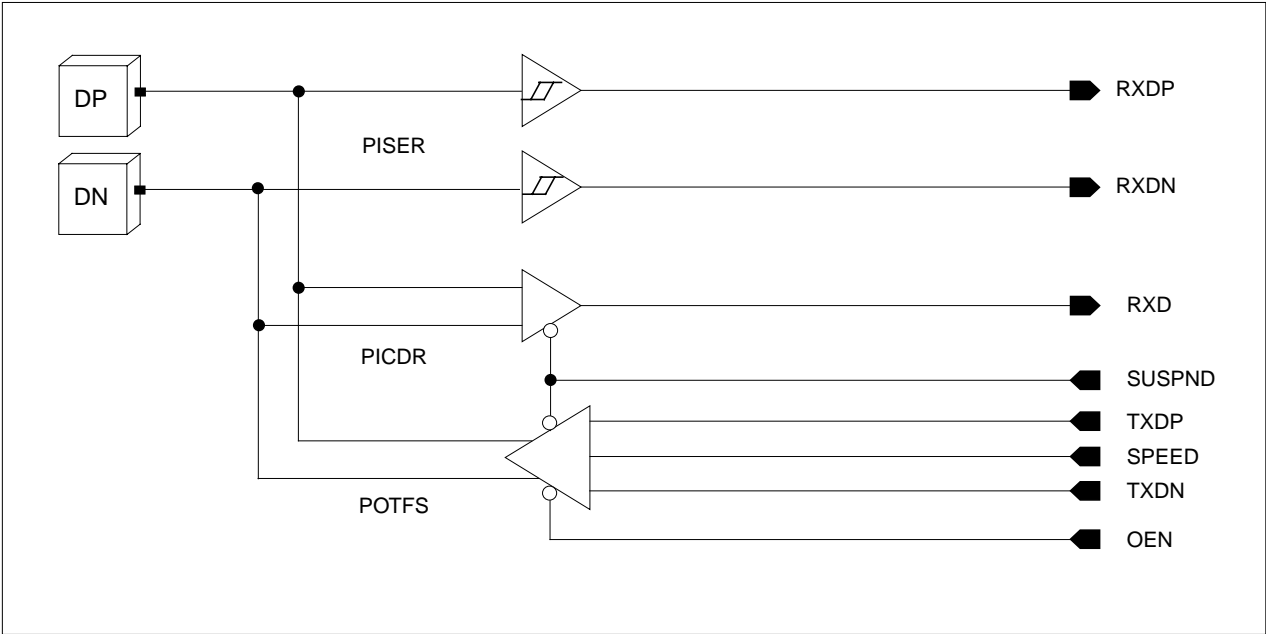
Pin Connection

Input	Output	Bi-Direction
TXDP	RXDP	DP
TXDN	RXDN	DN
SUSPND	RXD	
OEN		
SPEED		



PBUSB\_FS

Symbol



Pin Connection

Input	Output	Bi-Direction
TXDP	RXDP	DP
TXDN	RXDN	DN
SUSPND	RXD	
OEN		
SPEED		



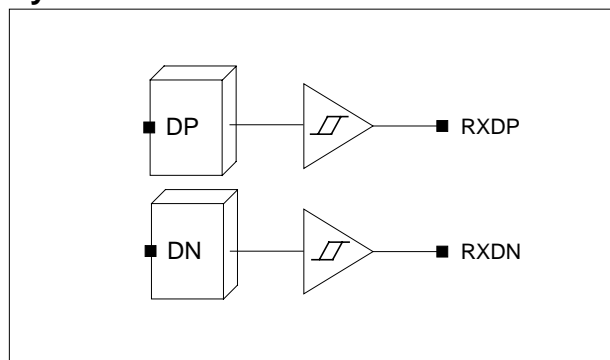
# PBUSB/PBUSB1/PBUSB\_LS/PBUSB\_FS(Under Development)

## Universal Serial Bus I/O Buffer

### PISER

Single-Ended Receiver

### Symbol



### Pin Connection

Input	Output
DP	RXDP
DN	RXDN

### Truth Table

DP	DN	RXDP	RXDN
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.80\text{ns}$ , SL: Standard Load)

### PISER

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
DP to RXDP	$t_R$	0.109	$0.094 + 0.008 \cdot \text{SL}$	$0.092 + 0.008 \cdot \text{SL}$	$0.080 + 0.008 \cdot \text{SL}$
	$t_F$	0.103	$0.086 + 0.008 \cdot \text{SL}$	$0.087 + 0.008 \cdot \text{SL}$	$0.076 + 0.008 \cdot \text{SL}$
	$t_{PLH}$	0.598	$0.587 + 0.005 \cdot \text{SL}$	$0.591 + 0.004 \cdot \text{SL}$	$0.599 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.585	$0.573 + 0.006 \cdot \text{SL}$	$0.579 + 0.005 \cdot \text{SL}$	$0.595 + 0.004 \cdot \text{SL}$
DN to RXDN	$t_R$	0.109	$0.094 + 0.008 \cdot \text{SL}$	$0.092 + 0.008 \cdot \text{SL}$	$0.080 + 0.008 \cdot \text{SL}$
	$t_F$	0.103	$0.086 + 0.008 \cdot \text{SL}$	$0.087 + 0.008 \cdot \text{SL}$	$0.076 + 0.008 \cdot \text{SL}$
	$t_{PLH}$	0.598	$0.587 + 0.005 \cdot \text{SL}$	$0.591 + 0.004 \cdot \text{SL}$	$0.599 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	0.585	$0.573 + 0.006 \cdot \text{SL}$	$0.579 + 0.005 \cdot \text{SL}$	$0.595 + 0.004 \cdot \text{SL}$

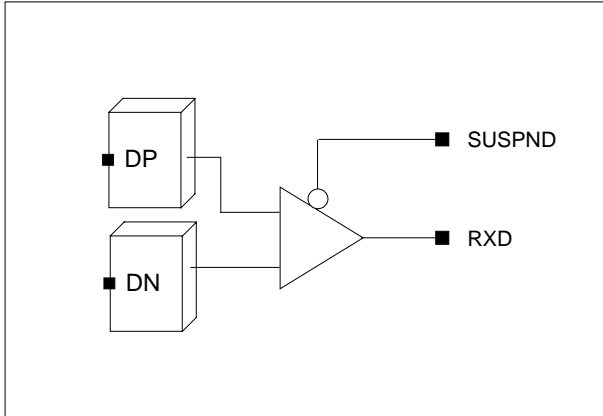
\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 60$ , \*Group3 :  $60 < \text{SL}$



## PICDR

Differential Receiver

### Symbol



### Pin Connection

Input	Output
DP DN SUSPND	RXD

### Truth Table

DP	DN	SUSPND	RXD
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	x
x	x	1	0

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.80\text{ns}$ , SL: Standard Load)

#### PICDR

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
DP to RXD	$t_R$	0.198	$0.179 + 0.010 \cdot \text{SL}$	$0.186 + 0.008 \cdot \text{SL}$	$0.168 + 0.008 \cdot \text{SL}$
	$t_F$	0.188	$0.167 + 0.010 \cdot \text{SL}$	$0.187 + 0.006 \cdot \text{SL}$	$0.252 + 0.005 \cdot \text{SL}$
	$t_{PLH}$	9.606	$9.588 + 0.009 \cdot \text{SL}$	$9.604 + 0.005 \cdot \text{SL}$	$9.656 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	8.896	$8.876 + 0.010 \cdot \text{SL}$	$8.897 + 0.005 \cdot \text{SL}$	$9.013 + 0.003 \cdot \text{SL}$
DN to RXD	$t_R$	0.213	$0.192 + 0.010 \cdot \text{SL}$	$0.203 + 0.008 \cdot \text{SL}$	$0.190 + 0.008 \cdot \text{SL}$
	$t_F$	0.219	$0.195 + 0.012 \cdot \text{SL}$	$0.219 + 0.006 \cdot \text{SL}$	$0.303 + 0.005 \cdot \text{SL}$
	$t_{PLH}$	3.600	$3.578 + 0.011 \cdot \text{SL}$	$3.602 + 0.006 \cdot \text{SL}$	$3.677 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	4.510	$4.487 + 0.011 \cdot \text{SL}$	$4.510 + 0.006 \cdot \text{SL}$	$4.647 + 0.004 \cdot \text{SL}$
SUSPND to RXD	$t_R$	0.168	$0.150 + 0.009 \cdot \text{SL}$	$0.154 + 0.008 \cdot \text{SL}$	$0.133 + 0.008 \cdot \text{SL}$
	$t_F$	0.226	$0.200 + 0.013 \cdot \text{SL}$	$0.226 + 0.007 \cdot \text{SL}$	$0.337 + 0.005 \cdot \text{SL}$
	$t_{PLH}$	1.360	$1.344 + 0.008 \cdot \text{SL}$	$1.358 + 0.005 \cdot \text{SL}$	$1.404 + 0.004 \cdot \text{SL}$
	$t_{PHL}$	1.628	$1.604 + 0.012 \cdot \text{SL}$	$1.628 + 0.007 \cdot \text{SL}$	$1.779 + 0.004 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 4$ , \*Group2 :  $4 \leq \text{SL} \leq 60$ , \*Group3 :  $60 < \text{SL}$



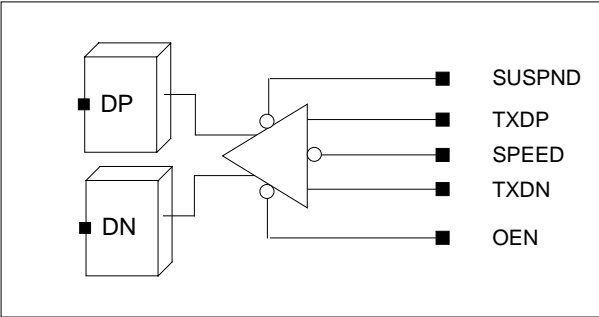
PBUSB/PBUSB1/PBUSB\_LS/PBUSB\_FS (Under Development)

Universal Serial Bus I/O Buffer

POTLS

Tri-State Output Buffer with Low Speed

Symbol



Pin Connection

Input	Output
TXDP	DP
TXDN	DN
SPEED	
SUSPND	
OEN	

Truth Table

TXDP	TXDN	SUSPND	OEN	SPEED	DP	DN
0	0	0	0	0	0	0
0	1	0	0	0	0	1
1	0	0	0	0	1	0
1	1	0	0	0	1	1
x	x	1	x	x	Hi-Z	Hi-Z
x	x	x	1	x	Hi-Z	Hi-Z
x	x	x	x	1	Hi-Z	Hi-Z

**NOTE:** SUSPND is the Suspend Mode control signal for the output driver. SUSPND=1 or OEN=1, both Low speed driver and Full speed driver are suspended. SPEED is the Low/Full speed output mode selecting signal, SPEED=0, SUSPND=0, OEN=0 Low speed mode transmitting.



# PBUSB/PBUSB1/PBUSB\_LS/PBUSB\_FS (Under Development)

## Universal Serial Bus I/O Buffer

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.80\text{ns}$ , CL: Capacitive Load)

#### POTLS

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TXDP to DP	$t_R$	116.330	$115.030 + 0.026 \cdot \text{CL}$	$120.870 + 0.000 \cdot \text{CL}$	$122.130 + 0.000 \cdot \text{CL}$
	$t_F$	135.200	$135.200 + 0.000 \cdot \text{CL}$	$122.110 + 0.053 \cdot \text{CL}$	$135.790 + 0.000 \cdot \text{CL}$
	$t_{PLH}$	111.850	$111.850 + 0.000 \cdot \text{CL}$	$105.020 + 0.078 \cdot \text{CL}$	$104.630 + 0.083 \cdot \text{CL}$
	$t_{PHL}$	112.920	$108.320 + 0.092 \cdot \text{CL}$	$119.180 + 0.000 \cdot \text{CL}$	$109.490 + 0.004 \cdot \text{CL}$
OEN to DP	$t_R$	114.230	$114.230 + 0.000 \cdot \text{CL}$	$113.240 + 0.009 \cdot \text{CL}$	$113.210 + 0.009 \cdot \text{CL}$
	$t_F$	129.430	$129.430 + 0.000 \cdot \text{CL}$	$131.350 + 0.000 \cdot \text{CL}$	$127.390 + 0.000 \cdot \text{CL}$
	$t_{PLH}$	79.258	$79.258 + 0.000 \cdot \text{CL}$	$77.803 + 0.028 \cdot \text{CL}$	$73.459 + 0.086 \cdot \text{CL}$
	$t_{PHL}$	113.000	$108.925 + 0.081 \cdot \text{CL}$	$110.840 + 0.043 \cdot \text{CL}$	$119.360 + 0.000 \cdot \text{CL}$
	$t_{PLZ}$	2.272	$2.272 + 0.000 \cdot \text{CL}$	$2.272 + 0.000 \cdot \text{CL}$	$2.272 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.474	$2.474 + 0.000 \cdot \text{CL}$	$2.473 + 0.000 \cdot \text{CL}$	$2.474 + 0.000 \cdot \text{CL}$
SPEED to DP	$t_R$	114.230	$114.230 + 0.000 \cdot \text{CL}$	$113.220 + 0.009 \cdot \text{CL}$	$113.190 + 0.010 \cdot \text{CL}$
	$t_F$	129.355	$129.355 + 0.000 \cdot \text{CL}$	$131.370 + 0.000 \cdot \text{CL}$	$127.380 + 0.000 \cdot \text{CL}$
	$t_{PLH}$	79.233	$79.233 + 0.000 \cdot \text{CL}$	$77.772 + 0.028 \cdot \text{CL}$	$73.473 + 0.086 \cdot \text{CL}$
	$t_{PHL}$	113.010	$108.910 + 0.082 \cdot \text{CL}$	$110.990 + 0.040 \cdot \text{CL}$	$119.270 + 0.000 \cdot \text{CL}$
	$t_{PLZ}$	2.261	$2.261 + 0.000 \cdot \text{CL}$	$2.261 + 0.000 \cdot \text{CL}$	$2.261 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.455	$2.455 + 0.000 \cdot \text{CL}$	$2.458 + 0.000 \cdot \text{CL}$	$2.454 + 0.000 \cdot \text{CL}$
SUSPND to DP	$t_R$	114.230	$114.230 + 0.000 \cdot \text{CL}$	$113.220 + 0.009 \cdot \text{CL}$	$113.190 + 0.010 \cdot \text{CL}$
	$t_F$	129.395	$129.395 + 0.000 \cdot \text{CL}$	$131.340 + 0.000 \cdot \text{CL}$	$127.380 + 0.000 \cdot \text{CL}$
	$t_{PLH}$	79.047	$79.047 + 0.000 \cdot \text{CL}$	$77.598 + 0.028 \cdot \text{CL}$	$73.290 + 0.086 \cdot \text{CL}$
	$t_{PHL}$	112.830	$108.730 + 0.082 \cdot \text{CL}$	$110.830 + 0.040 \cdot \text{CL}$	$119.050 + 0.000 \cdot \text{CL}$
	$t_{PLZ}$	2.084	$2.084 + 0.000 \cdot \text{CL}$	$2.084 + 0.000 \cdot \text{CL}$	$2.084 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	2.284	$2.283 + 0.000 \cdot \text{CL}$	$2.285 + 0.000 \cdot \text{CL}$	$2.284 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



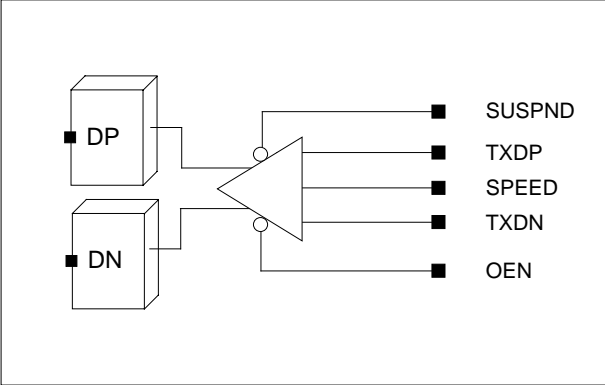
PBUSB/PBUSB1/PBUSB\_LS/PBUSB\_FS (Under Development)

Universal Serial Bus I/O Buffer

POTFS

Tri-State Output Buffer with Full Speed

Symbol



Pin Connection

Input	Output
TXDP	DP
TXDN	DN
SPEED	
SUSPND	
OEN	

Truth Table

TXDP	TXDN	SUSPND	OEN	SPEED	DP	DN
0	0	0	0	1	0	0
0	1	0	0	1	0	1
1	0	0	0	1	1	0
1	1	0	0	1	1	1
x	x	1	x	x	Hi-z	Hi-z
x	x	x	1	x	Hi-z	Hi-z
x	x	x	x	0	Hi-z	Hi-z

**NOTE:** SUSPND is the Suspend Mode control signal for the output driver. SUSPND=1 or OEN=1, both Low speed driver and Full speed driver are suspended. SPEED is the Low/Full speed output mode selecting signal, SPEED=1, SUSPND=0, OEN=0 Low speed mode transmitting.



# PBUSB/PBUSB1/PBUSB\_LS/PBUSB\_FS (Under Development)

## Universal Serial Bus I/O Buffer

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load)

#### POTFS

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TXDP to DP	$t_R$	7.537	$4.664 + 0.057 \cdot \text{CL}$	$5.798 + 0.035 \cdot \text{CL}$	$5.770 + 0.035 \cdot \text{CL}$
	$t_F$	7.794	$4.733 + 0.061 \cdot \text{CL}$	$5.879 + 0.038 \cdot \text{CL}$	$5.900 + 0.038 \cdot \text{CL}$
	$t_{PLH}$	7.961	$5.205 + 0.055 \cdot \text{CL}$	$6.073 + 0.038 \cdot \text{CL}$	$5.998 + 0.039 \cdot \text{CL}$
	$t_{PHL}$	7.565	$5.466 + 0.042 \cdot \text{CL}$	$5.457 + 0.042 \cdot \text{CL}$	$6.008 + 0.035 \cdot \text{CL}$
OEN to DP	$t_R$	7.878	$5.429 + 0.049 \cdot \text{CL}$	$5.129 + 0.055 \cdot \text{CL}$	$5.407 + 0.051 \cdot \text{CL}$
	$t_F$	7.602	$4.896 + 0.054 \cdot \text{CL}$	$4.948 + 0.053 \cdot \text{CL}$	$5.180 + 0.050 \cdot \text{CL}$
	$t_{PLH}$	7.628	$5.244 + 0.048 \cdot \text{CL}$	$4.558 + 0.061 \cdot \text{CL}$	$5.973 + 0.043 \cdot \text{CL}$
	$t_{PHL}$	7.809	$5.049 + 0.055 \cdot \text{CL}$	$5.525 + 0.046 \cdot \text{CL}$	$4.734 + 0.056 \cdot \text{CL}$
	$t_{PLZ}$	1.251	$1.251 + 0.000 \cdot \text{CL}$	$1.251 + 0.000 \cdot \text{CL}$	$1.248 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.851	$1.850 + 0.000 \cdot \text{CL}$	$1.851 + 0.000 \cdot \text{CL}$	$1.851 + 0.000 \cdot \text{CL}$
SPEED to DP	$t_R$	7.678	$3.979 + 0.074 \cdot \text{CL}$	$5.169 + 0.050 \cdot \text{CL}$	$5.687 + 0.043 \cdot \text{CL}$
	$t_F$	7.842	$3.786 + 0.081 \cdot \text{CL}$	$5.228 + 0.052 \cdot \text{CL}$	$5.699 + 0.046 \cdot \text{CL}$
	$t_{PLH}$	7.969	$5.082 + 0.058 \cdot \text{CL}$	$5.499 + 0.049 \cdot \text{CL}$	$5.714 + 0.047 \cdot \text{CL}$
	$t_{PHL}$	7.830	$5.117 + 0.054 \cdot \text{CL}$	$5.686 + 0.043 \cdot \text{CL}$	$5.014 + 0.052 \cdot \text{CL}$
SUSPND to DP	$t_R$	7.578	$5.329 + 0.045 \cdot \text{CL}$	$5.629 + 0.039 \cdot \text{CL}$	$5.906 + 0.035 \cdot \text{CL}$
	$t_F$	7.882	$5.476 + 0.048 \cdot \text{CL}$	$5.788 + 0.042 \cdot \text{CL}$	$6.080 + 0.038 \cdot \text{CL}$
	$t_{PLH}$	7.940	$5.053 + 0.058 \cdot \text{CL}$	$5.470 + 0.049 \cdot \text{CL}$	$5.985 + 0.043 \cdot \text{CL}$
	$t_{PHL}$	7.621	$4.605 + 0.060 \cdot \text{CL}$	$5.257 + 0.047 \cdot \text{CL}$	$5.309 + 0.047 \cdot \text{CL}$
	$t_{PLZ}$	1.046	$1.046 + 0.000 \cdot \text{CL}$	$1.045 + 0.000 \cdot \text{CL}$	$1.046 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.646	$1.646 + 0.000 \cdot \text{CL}$	$1.646 + 0.000 \cdot \text{CL}$	$1.646 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

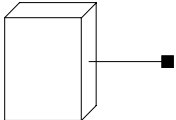


# POWER PADS

## Cell List

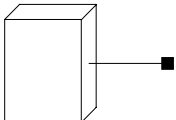
Cell Name		Function Description
VDD Power Pads	VSS Power Pads	
VDD2I	VSS2I	2.5V Internal
VDD2P	VSS2P	2.5V Pre-Driver
VDD2O	VSS2O	2.5V Output-Driver
VDD2IP	VSS2IP	2.5V Internal and Pre-Driver
VDD2OP	VSS2OP	2.5V Output-Driver and Pre-Driver
VDD2T	VSS2T	2.5V Total
VDD3P	VSS3P	3.3V Pre-Driver
VDD3O	VSS3O	3.3V Output-Driver
VDD3OP	VSS3OP	3.3V Output-Driver and Pre-Driver

Logic Symbol



Cell Name		Function Description
VDD Power Pads	VSS Power Pads	
VDD2I_ABB	VSS2I_ABB	2.5V Internal with Separate Bulk Bias
VDD2OP_ABB	VSS2OP_ABB	2.5V Pre-Driver and Output-Driver with Separate Bulk Bias
VDD2T_ABB	VSS2T_ABB	2.5V Total with Separate Bulk Bias
	VBB_ABB	Bulk Bias Power Pad
	VSSBB_ABB	Bulk Bias and VSS Power Pad

Logic Symbol





## ANALOG INTERFACE

### Analog Input

Cell Name	Function Description
PIA_ABB	Analog Normal Input Pad for 2.5V Interface with Separated Bulk-Bias
PIAR10_ABB	Analog Normal Input Pad for 2.5V Interface with Resistor 10ohm and Separated Bulk-Bias
PIAR50_ABB	Analog Normal Input Pad for 2.5V Interface with Resistor 50ohm and Separated Bulk-Bias
PNC_ABB	Analog No Connection Pad for 2.5V Interface with Separated Bulk-Bias
PIC_ABB	Analog CMOS Level Input Buffer for 2.5V Interface with Separated Bulk-Bias
PICC_ABB	Analog CMOS Level Input Buffer for 2.5V Interface with Separated Bulk-Bias and without Nand-Tree
PICEN_ABB	Analog CMOS Level Input Buffer for 2.5V Interface with Enable Port and Separated Bulk-Bias

### Analog Output

Cell Name	Function Description
POA_ABB	Analog Normal Output Pad for 2.5V Interface with Separated Bulk-Bias
POAR10_ABB	Analog Normal Output Pad for 2.5V Interface with Resistor 10ohm and Separated Bulk-Bias
POAR50_ABB	Analog Normal Output Pad for 2.5V Interface with Resistor 50ohm and Separated Bulk-Bias
POT1/2/4/8_ABB	Analog Tri-State Output Buffer for 2.5V Interface with Separate Bulk Bias, 1/2/4/8mA Drive

### Analog Bi-Direction

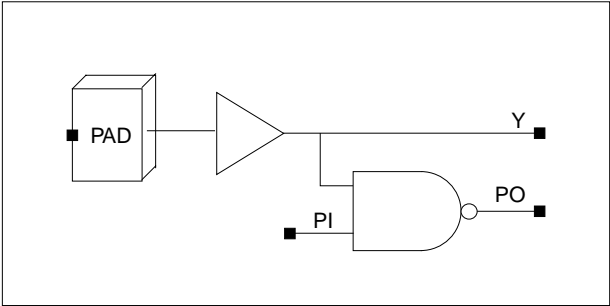
Cell Name	Function Description
PBCT1/2/4/8_ABB	Analog Bi-Directional Buffer for 2.5V Interface with CMOS Level Input, Tri-State Output Pad with Separated Bulk-Bias, 1/2/4/8mA Drive



PIC\_ABB

Analog CMOS Level Input Buffers with Separate Bulk-Bias

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PIC_ABB	3.620

Switching Characteristics

(Typical process, 25°C, 2.5V, t<sub>R</sub>/t<sub>F</sub> = 3.00ns, SL: Standard Load)

PIC\_ABB

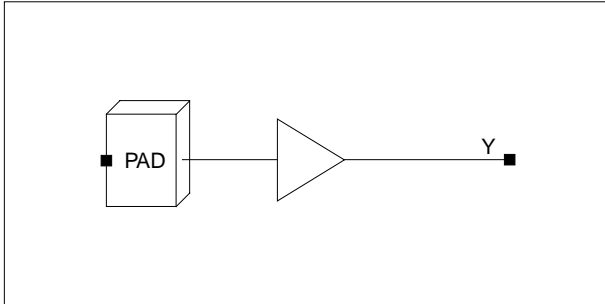
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t <sub>R</sub>	0.205	0.186 + 0.010*SL	0.186 + 0.010*SL	0.166 + 0.010*SL
	t <sub>F</sub>	0.149	0.136 + 0.006*SL	0.138 + 0.006*SL	0.125 + 0.006*SL
	t <sub>PLH</sub>	1.051	1.036 + 0.007*SL	1.042 + 0.005*SL	1.059 + 0.005*SL
	t <sub>PHL</sub>	0.991	0.979 + 0.006*SL	0.986 + 0.004*SL	1.014 + 0.003*SL

\*Group1 : SL < 3, \*Group2 : 3 ≤ SL ≤ 45, \*Group3 : 45 < SL



## Analog CMOS Level Input Buffers with Separate Bulk-Bias

### Logic Symbol



### Truth Table

PAD	Y
0	0
1	1

### Switching Characteristics

(Typical process, 25 °C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

#### PICC\_ABB

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.176	$0.157 + 0.010 \cdot \text{SL}$	$0.157 + 0.009 \cdot \text{SL}$	$0.126 + 0.010 \cdot \text{SL}$
	$t_F$	0.127	$0.112 + 0.007 \cdot \text{SL}$	$0.119 + 0.006 \cdot \text{SL}$	$0.106 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	1.027	$1.010 + 0.008 \cdot \text{SL}$	$1.019 + 0.006 \cdot \text{SL}$	$1.044 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.973	$0.960 + 0.007 \cdot \text{SL}$	$0.969 + 0.004 \cdot \text{SL}$	$1.003 + 0.003 \cdot \text{SL}$

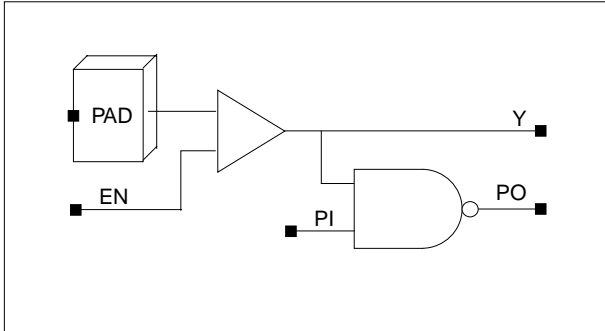
\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



## PICEN\_ABB

### Analog CMOS Level Input Buffers with Enable Port and Separate Bulk-Bias

#### Logic Symbol



#### Truth Table

PAD	PI	EN	Y	PO
1	1	1	1	0
0	x	1	0	1
1	0	1	1	1
x	x	0	0	1

#### Standard Load (SL)

Cell Name	PI	EN
PICEN_ABB	2.897	2.897

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 3.00\text{ns}$ , SL: Standard Load)

#### PICEN\_ABB

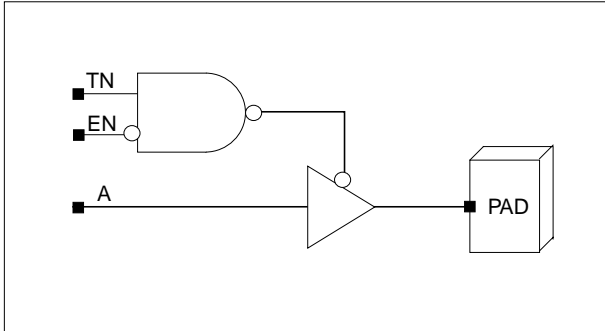
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	$t_R$	0.231	$0.211 + 0.010 \cdot \text{SL}$	$0.212 + 0.010 \cdot \text{SL}$	$0.198 + 0.010 \cdot \text{SL}$
	$t_F$	0.177	$0.164 + 0.007 \cdot \text{SL}$	$0.167 + 0.006 \cdot \text{SL}$	$0.166 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	1.104	$1.088 + 0.008 \cdot \text{SL}$	$1.096 + 0.006 \cdot \text{SL}$	$1.128 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	1.174	$1.160 + 0.007 \cdot \text{SL}$	$1.169 + 0.004 \cdot \text{SL}$	$1.212 + 0.003 \cdot \text{SL}$
EN to Y	$t_R$	0.176	$0.155 + 0.011 \cdot \text{SL}$	$0.156 + 0.010 \cdot \text{SL}$	$0.152 + 0.010 \cdot \text{SL}$
	$t_F$	0.131	$0.117 + 0.007 \cdot \text{SL}$	$0.120 + 0.006 \cdot \text{SL}$	$0.121 + 0.006 \cdot \text{SL}$
	$t_{PLH}$	0.315	$0.301 + 0.007 \cdot \text{SL}$	$0.306 + 0.005 \cdot \text{SL}$	$0.323 + 0.005 \cdot \text{SL}$
	$t_{PHL}$	0.329	$0.318 + 0.006 \cdot \text{SL}$	$0.323 + 0.004 \cdot \text{SL}$	$0.352 + 0.003 \cdot \text{SL}$

\*Group1 :  $\text{SL} < 3$ , \*Group2 :  $3 \leq \text{SL} \leq 45$ , \*Group3 :  $45 < \text{SL}$



## Analog Tri-state Output Buffers with Enable Port and Separate Bulk-Bias

### Logic Symbol



### Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi - z
0	x	x	Hi - z

### Standard Load (SL)

Cell Name	TN	EN	A
POT1_ABB	2.898	2.916	3.023
POT2_ABB	2.898	2.916	3.023
POT4_ABB	2.898	2.916	3.023
POT8_ABB	2.898	2.916	3.023

### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load)

#### POT1\_ABB

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	32.056	$1.759 + 0.606 \cdot \text{CL}$	$1.758 + 0.606 \cdot \text{CL}$	$1.761 + 0.606 \cdot \text{CL}$
	$t_F$	33.870	$1.873 + 0.640 \cdot \text{CL}$	$1.872 + 0.640 \cdot \text{CL}$	$1.872 + 0.640 \cdot \text{CL}$
	$t_{PLH}$	16.015	$1.507 + 0.290 \cdot \text{CL}$	$1.507 + 0.290 \cdot \text{CL}$	$1.507 + 0.290 \cdot \text{CL}$
	$t_{PHL}$	17.839	$1.729 + 0.322 \cdot \text{CL}$	$1.731 + 0.322 \cdot \text{CL}$	$1.731 + 0.322 \cdot \text{CL}$
TN to PAD	$t_R$	32.056	$1.759 + 0.606 \cdot \text{CL}$	$1.758 + 0.606 \cdot \text{CL}$	$1.761 + 0.606 \cdot \text{CL}$
	$t_F$	33.870	$1.873 + 0.640 \cdot \text{CL}$	$1.872 + 0.640 \cdot \text{CL}$	$1.872 + 0.640 \cdot \text{CL}$
	$t_{PLH}$	16.063	$1.553 + 0.290 \cdot \text{CL}$	$1.557 + 0.290 \cdot \text{CL}$	$1.554 + 0.290 \cdot \text{CL}$
	$t_{PHL}$	17.962	$1.852 + 0.322 \cdot \text{CL}$	$1.854 + 0.322 \cdot \text{CL}$	$1.851 + 0.322 \cdot \text{CL}$
	$t_{PLZ}$	0.958	$0.958 + 0.000 \cdot \text{CL}$	$0.958 + 0.000 \cdot \text{CL}$	$0.958 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.662	$0.662 + 0.000 \cdot \text{CL}$	$0.662 + 0.000 \cdot \text{CL}$	$0.662 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	32.056	$1.759 + 0.606 \cdot \text{CL}$	$1.758 + 0.606 \cdot \text{CL}$	$1.761 + 0.606 \cdot \text{CL}$
	$t_F$	33.870	$1.873 + 0.640 \cdot \text{CL}$	$1.872 + 0.640 \cdot \text{CL}$	$1.872 + 0.640 \cdot \text{CL}$
	$t_{PLH}$	16.165	$1.658 + 0.290 \cdot \text{CL}$	$1.657 + 0.290 \cdot \text{CL}$	$1.660 + 0.290 \cdot \text{CL}$
	$t_{PHL}$	18.064	$1.957 + 0.322 \cdot \text{CL}$	$1.954 + 0.322 \cdot \text{CL}$	$1.957 + 0.322 \cdot \text{CL}$
	$t_{PLZ}$	1.000	$1.000 + 0.000 \cdot \text{CL}$	$1.000 + 0.000 \cdot \text{CL}$	$1.000 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.705	$0.705 + 0.000 \cdot \text{CL}$	$0.705 + 0.000 \cdot \text{CL}$	$0.705 + 0.000 \cdot \text{CL}$

\*Group1 :  $\text{CL} < 50$ , \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



## POT1/2/4/8\_ABB

### Analog Tri-state Output Buffers with Enable Port and Separate Bulk-Bias

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load)

#### POT2\_ABB

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	16.047	$0.897 + 0.303 \cdot \text{CL}$	$0.899 + 0.303 \cdot \text{CL}$	$0.899 + 0.303 \cdot \text{CL}$
	$t_F$	18.535	$1.010 + 0.350 \cdot \text{CL}$	$1.011 + 0.350 \cdot \text{CL}$	$1.011 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	8.431	$1.177 + 0.145 \cdot \text{CL}$	$1.177 + 0.145 \cdot \text{CL}$	$1.177 + 0.145 \cdot \text{CL}$
	$t_{PHL}$	10.353	$1.235 + 0.182 \cdot \text{CL}$	$1.233 + 0.182 \cdot \text{CL}$	$1.236 + 0.182 \cdot \text{CL}$
TN to PAD	$t_R$	16.047	$0.897 + 0.303 \cdot \text{CL}$	$0.899 + 0.303 \cdot \text{CL}$	$0.899 + 0.303 \cdot \text{CL}$
	$t_F$	18.535	$1.010 + 0.350 \cdot \text{CL}$	$1.011 + 0.350 \cdot \text{CL}$	$1.011 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	8.479	$1.224 + 0.145 \cdot \text{CL}$	$1.224 + 0.145 \cdot \text{CL}$	$1.228 + 0.145 \cdot \text{CL}$
	$t_{PHL}$	10.477	$1.357 + 0.182 \cdot \text{CL}$	$1.357 + 0.182 \cdot \text{CL}$	$1.360 + 0.182 \cdot \text{CL}$
	$t_{PLZ}$	0.808	$0.808 + 0.000 \cdot \text{CL}$	$0.808 + 0.000 \cdot \text{CL}$	$0.808 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.768	$0.768 + 0.000 \cdot \text{CL}$	$0.768 + 0.000 \cdot \text{CL}$	$0.768 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	16.047	$0.897 + 0.303 \cdot \text{CL}$	$0.899 + 0.303 \cdot \text{CL}$	$0.899 + 0.303 \cdot \text{CL}$
	$t_F$	18.535	$1.010 + 0.350 \cdot \text{CL}$	$1.011 + 0.350 \cdot \text{CL}$	$1.011 + 0.350 \cdot \text{CL}$
	$t_{PLH}$	8.581	$1.327 + 0.145 \cdot \text{CL}$	$1.327 + 0.145 \cdot \text{CL}$	$1.327 + 0.145 \cdot \text{CL}$
	$t_{PHL}$	10.580	$1.460 + 0.182 \cdot \text{CL}$	$1.462 + 0.182 \cdot \text{CL}$	$1.462 + 0.182 \cdot \text{CL}$
	$t_{PLZ}$	0.851	$0.851 + 0.000 \cdot \text{CL}$	$0.851 + 0.000 \cdot \text{CL}$	$0.851 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.810	$0.810 + 0.000 \cdot \text{CL}$	$0.810 + 0.000 \cdot \text{CL}$	$0.810 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$

#### Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load)

#### POT4\_ABB

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	8.054	$0.484 + 0.151 \cdot \text{CL}$	$0.480 + 0.151 \cdot \text{CL}$	$0.480 + 0.151 \cdot \text{CL}$
	$t_F$	9.284	$0.522 + 0.175 \cdot \text{CL}$	$0.521 + 0.175 \cdot \text{CL}$	$0.522 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	4.795	$1.167 + 0.073 \cdot \text{CL}$	$1.168 + 0.073 \cdot \text{CL}$	$1.168 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	5.607	$1.048 + 0.091 \cdot \text{CL}$	$1.048 + 0.091 \cdot \text{CL}$	$1.048 + 0.091 \cdot \text{CL}$
TN to PAD	$t_R$	8.054	$0.484 + 0.151 \cdot \text{CL}$	$0.480 + 0.151 \cdot \text{CL}$	$0.480 + 0.151 \cdot \text{CL}$
	$t_F$	9.284	$0.522 + 0.175 \cdot \text{CL}$	$0.521 + 0.175 \cdot \text{CL}$	$0.522 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	4.842	$1.214 + 0.073 \cdot \text{CL}$	$1.215 + 0.073 \cdot \text{CL}$	$1.216 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	5.729	$1.168 + 0.091 \cdot \text{CL}$	$1.169 + 0.091 \cdot \text{CL}$	$1.170 + 0.091 \cdot \text{CL}$
	$t_{PLZ}$	0.940	$0.940 + 0.000 \cdot \text{CL}$	$0.940 + 0.000 \cdot \text{CL}$	$0.940 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	0.978	$0.978 + 0.000 \cdot \text{CL}$	$0.978 + 0.000 \cdot \text{CL}$	$0.978 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	8.054	$0.484 + 0.151 \cdot \text{CL}$	$0.480 + 0.151 \cdot \text{CL}$	$0.480 + 0.151 \cdot \text{CL}$
	$t_F$	9.284	$0.522 + 0.175 \cdot \text{CL}$	$0.521 + 0.175 \cdot \text{CL}$	$0.522 + 0.175 \cdot \text{CL}$
	$t_{PLH}$	4.945	$1.318 + 0.073 \cdot \text{CL}$	$1.318 + 0.073 \cdot \text{CL}$	$1.318 + 0.073 \cdot \text{CL}$
	$t_{PHL}$	5.832	$1.271 + 0.091 \cdot \text{CL}$	$1.272 + 0.091 \cdot \text{CL}$	$1.274 + 0.091 \cdot \text{CL}$
	$t_{PLZ}$	0.982	$0.982 + 0.000 \cdot \text{CL}$	$0.982 + 0.000 \cdot \text{CL}$	$0.982 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.020	$1.020 + 0.000 \cdot \text{CL}$	$1.020 + 0.000 \cdot \text{CL}$	$1.020 + 0.000 \cdot \text{CL}$

\*Group1 : CL < 50, \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



## Analog Tri-state Output Buffers with Enable Port and Separate Bulk-Bias

## Switching Characteristics

(Typical process, 25°C, 2.5V,  $t_R/t_F = 0.17\text{ns}$ , CL: Capacitive Load)

## POT8\_ABB

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	$t_R$	4.117	$0.414 + 0.074 \cdot \text{CL}$	$0.368 + 0.075 \cdot \text{CL}$	$0.336 + 0.075 \cdot \text{CL}$
	$t_F$	4.673	$0.309 + 0.087 \cdot \text{CL}$	$0.297 + 0.088 \cdot \text{CL}$	$0.292 + 0.088 \cdot \text{CL}$
	$t_{PLH}$	3.256	$1.437 + 0.036 \cdot \text{CL}$	$1.441 + 0.036 \cdot \text{CL}$	$1.442 + 0.036 \cdot \text{CL}$
	$t_{PHL}$	3.352	$1.084 + 0.045 \cdot \text{CL}$	$1.078 + 0.045 \cdot \text{CL}$	$1.074 + 0.046 \cdot \text{CL}$
TN to PAD	$t_R$	4.117	$0.414 + 0.074 \cdot \text{CL}$	$0.368 + 0.075 \cdot \text{CL}$	$0.336 + 0.075 \cdot \text{CL}$
	$t_F$	4.672	$0.307 + 0.087 \cdot \text{CL}$	$0.295 + 0.088 \cdot \text{CL}$	$0.290 + 0.088 \cdot \text{CL}$
	$t_{PLH}$	3.304	$1.484 + 0.036 \cdot \text{CL}$	$1.489 + 0.036 \cdot \text{CL}$	$1.490 + 0.036 \cdot \text{CL}$
	$t_{PHL}$	3.464	$1.180 + 0.046 \cdot \text{CL}$	$1.183 + 0.046 \cdot \text{CL}$	$1.184 + 0.046 \cdot \text{CL}$
	$t_{PLZ}$	1.195	$1.195 + 0.000 \cdot \text{CL}$	$1.195 + 0.000 \cdot \text{CL}$	$1.195 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.397	$1.397 + 0.000 \cdot \text{CL}$	$1.397 + 0.000 \cdot \text{CL}$	$1.397 + 0.000 \cdot \text{CL}$
EN to PAD	$t_R$	4.117	$0.414 + 0.074 \cdot \text{CL}$	$0.369 + 0.075 \cdot \text{CL}$	$0.336 + 0.075 \cdot \text{CL}$
	$t_F$	4.672	$0.307 + 0.087 \cdot \text{CL}$	$0.295 + 0.088 \cdot \text{CL}$	$0.291 + 0.088 \cdot \text{CL}$
	$t_{PLH}$	3.406	$1.588 + 0.036 \cdot \text{CL}$	$1.592 + 0.036 \cdot \text{CL}$	$1.592 + 0.036 \cdot \text{CL}$
	$t_{PHL}$	3.567	$1.284 + 0.046 \cdot \text{CL}$	$1.285 + 0.046 \cdot \text{CL}$	$1.287 + 0.046 \cdot \text{CL}$
	$t_{PLZ}$	1.238	$1.238 + 0.000 \cdot \text{CL}$	$1.238 + 0.000 \cdot \text{CL}$	$1.238 + 0.000 \cdot \text{CL}$
	$t_{PHZ}$	1.439	$1.439 + 0.000 \cdot \text{CL}$	$1.439 + 0.000 \cdot \text{CL}$	$1.439 + 0.000 \cdot \text{CL}$

\*Group1 :  $\text{CL} < 50$ , \*Group2 :  $50 \leq \text{CL} \leq 75$ , \*Group3 :  $75 < \text{CL}$



## ESD Slot Cells

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### Cell List

Cell Name	Function Description
EV2I	2.5V Internal ESD Protection
EV2P	2.5V Pre-Driver ESD Protection
EV2O	2.5V Output-Driver ESD Protection
EV2IP	2.5V Internal and Pre-Driver ESD Protection
EV2OP	2.5V Output-Driver and Pre-Driver ESD Protection
EV2T	2.5V Total ESD Protection
EV3P	3.3V Pre-Driver ESD Protection
EV3O	3.3V Output-Driver ESD Protection
EV3OP	3.3V Output-Driver and Pre-Driver ESD Protection
EV2I_ABB	2.5V Internal ESD Protection with Separated Bulk-Bias
EV2OP_ABB	2.5V Output-Driver and Pre-Driver ESD Protection with Separated Bulk-Bias
EV2T_ABB	2.5V Total ESD Protection with Separated Bulk-Bias

**NOTE:** All of Slot Cells have no Pad and can be added automatically by using SEC utility CubicPlan.



## Common Slot Cells

### Cell List

Cell Name	Function Description
EC0C0	Metal Ring Separator between Different Digital Blocks
EC0C0D <sup>1</sup>	Metal Ring Separator between Different Digital Blocks for Noise Critical Design
EC0CA0	Metal Ring Separator between Digital to Analog
EC0CA0D <sup>1</sup>	Metal Ring Separator between Digital to Analog for Noise Critical Design
EC0C0_BB	Metal Ring Separator between Different Analog Blocks with VBB Ring Separated
EC0C0D_BB <sup>1</sup>	Metal Ring Separator between Different Analog Blocks for Noise Critical Design with VBB Ring Separated
EC0C0_VBB <sup>2</sup>	Metal Ring Separator between Different Analog Blocks with VBB Ring Connected
EC0C0D_VBB <sup>1,2</sup>	Metal Ring Separator between Different Analog Blocks for Noise Critical Design with VBB Ring Connected

#### NOTES:

1. If CDL ring connected with bi-directional diode, ESD protection level can be dropped.
2. If analog blocks have only one VBB power pad, metal connected VBB ring type should be used.
3. All of Slot Cells can be added automatically by using SEC utility CubicPlan, or by Manual.



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## Compiled Macrocells

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5



## Contents

Overview to Compiled Memory .....	5-1
Compiled Memory Naming Convention.....	5-1
Characteristics for Timing and Power .....	5-2
Built-In Self Test for Compiled Memory .....	5-3
Selection Guide for Compiled Memory .....	5-4
High-Density Compiled Memory	
SPSRAM_HD     High-Density Single-Port Synchronous SRAM .....	5-7
SPSRAMBW_HD   High-Density Single-Port Synchronous SRAM with Bit-Write.....	5-17
DPSRAM_HD     High-Density Dual-Port Synchronous SRAM.....	5-27
SPARAM_HD     High-Density Single-Port Asynchronous SRAM .....	5-35
DROM_HD       High-Density Synchronous Diffusion Programmable ROM .....	5-46
MROM_HD       High-Density Synchronous Metal Programmable ROM.....	5-54
ARFRAM_HD     High-Density Multi-port Asynchronous Register File.....	5-62
FIFO_HD        High-Density Synchronous First-In First-Out Memory.....	5-73
Low-Power Compiled Memory	
SPSRAM_LP     Low Power Single-Port Synchronous SRAM .....	5-83
DPSRAM_LP     Low Power Dual-Port Synchronous SRAM.....	5-93
SPARAM_LP     Low Power Single-Port Asynchronous SRAM .....	5-101
DROM_LP       Low Power Synchronous Diffusion Programmable ROM .....	5-111
MROM_LP       Low Power Synchronous Metal Programmable ROM.....	5-119
Overview to Compiled Datapath .....	5-127
Datapath Module Design Flow .....	5-127
Selection Guide for Compiled Datapath .....	5-130
ADDER           Adder/Subtractor.....	5-131
BS               Barrel Shifter.....	5-136
MPY             Modified Booth Multiplier .....	5-141



## OVERVIEW TO COMPILED MEMORY

This section contains the overview of STD110 compiled memory. In STD110 compiled memory, we provide application-specific memory solution - high-density and low-power application. That is, two different library set of compiled memory are available in STD110 cell library. One is the high-density compiled memory, called STD110-HD compiled memory and the other is the low-power compiled memory, called STD110-LP compiled memory. The high-density compiled memories are suitable for high integration application with high-performance whereas the low-power compiled memories are suitable for portable applications. These are complete memories that are customized to satisfy the requirements of the circuit at hand. Depending on the function to be generated, the final memory will be implemented as a stand-alone, pitch-matched and customized leafcells. In addition, to implement optimized memory, we apply the state-of-the-art design architecture techniques. In STD110 cell library, the compiled memory is fully generated by a user-configurable compiler, called memory compiler. It allows you to configure a memory through memory-related specification such as word depth, bit per word, column mux type and so on. The compiler allows you to select and customize any of memory to satisfy the specific circuit requirements. When the required specifications have been fully given, you may get any or all of the following items:

- Area-optimized and speed-optimized layout blocks
- Schematic netlist for simulation and verification
- Phantom cell to use in chip-level layout
- Tabular model for timing and power characteristics
- Automatic datasheet for a specific instance

For more detailed information regarding to memory compiler, contact your local representative or headquarters.

## COMPILED MEMORY NAMING CONVENTION

The naming convention of compiled memory in this section will be shown as Fig. 5-1. The memory name consists of the following convention.

**[memory\_code]\_[appl\_code]\_[opt\_code]\_[config\_code]**

**Figure 5-1. Compiled Memory Naming Convention**

The first string, '*memory\_code*', means the name of memory type. In STD110 compiled memory, the available memory types are as follows:

- SPSRAM : Single-Port Synchronous SRAM
- SPSRAMBW : Single-Port Synchronous SRAM with Bit-Write
- DPSRAM : Dual-Port Synchronous SRAM
- SPARAM : Single-Port Asynchronous SRAM
- DROM : Synchronous Diffusion-Programmable ROM
- MROM : Synchronous Metal-Programmable ROM
- ARFRAM : Multi-Port Asynchronous Register File
- FIFO : Synchronous First-In First-Out Memory



The second string, '*appl\_code*', means the specific application to suitably support the compiled memory and the application code is one of HD (High-Density), LP (Low-Power) and HS (High-Speed). In STD110 compiled memory, the high-speed compiled memory is not supported as another library set. Instead, the high-density compiled memory can be applied for the high-performance application.

The third string, '*opt\_code*', represents the number of read and write ports for multi-port memory and the option code is composed of the following convention:

$$\text{opt\_code} = \langle n \rangle r \langle m \rangle w$$

Currently this field is only used for ARFRAM, where *n* is the total number of read ports (1~2) and *m* is the total number of write ports (1~2). The last string, '*config\_code*', represents the configuration of the memory to be specified. This configuration code is composed of the following convention:

$$\langle \text{WORD} \rangle \text{ x } \langle \text{BPW} \rangle \text{ m } \langle \text{YMUX} \rangle \text{ b } \langle \text{BANK} \rangle$$

Here, WORD is the word depth, BPW is bit per word, YMUX is the available column mux type and BANK is the number of bank to be used. For example, '*spsram\_hd\_1024x32m16b2*' refers to a High-Density single-port synchronous SRAM with 1024 words, 32 bits, 16 column mux and 2 bank. Second, '*arfram\_hd\_1r2w\_32x32m2*' refers to a High-Density three-port (1 read/2 write) asynchronous register file with 32 word, 32 bits and 2 column mux and '*spsram\_lp\_1024x32m16b2*' refers to a Low-Power single-port synchronous SRAM with 1024 words, 32 bits, 16 column mux and 2 bank.

## CHARACTERISTICS FOR TIMING AND POWER

STD110-HD compiled memory is only supported at 2.5V supply voltage whereas STD110-LP compiled memory is supported at both 2.5V supply voltage and 1.8V supply voltage. Compiled memory in this section has been characterized using typical-case at 25 degree and 2.5V supply. The values of worst-case or best-case can be derived by using derating factors provided in Chapter 1.

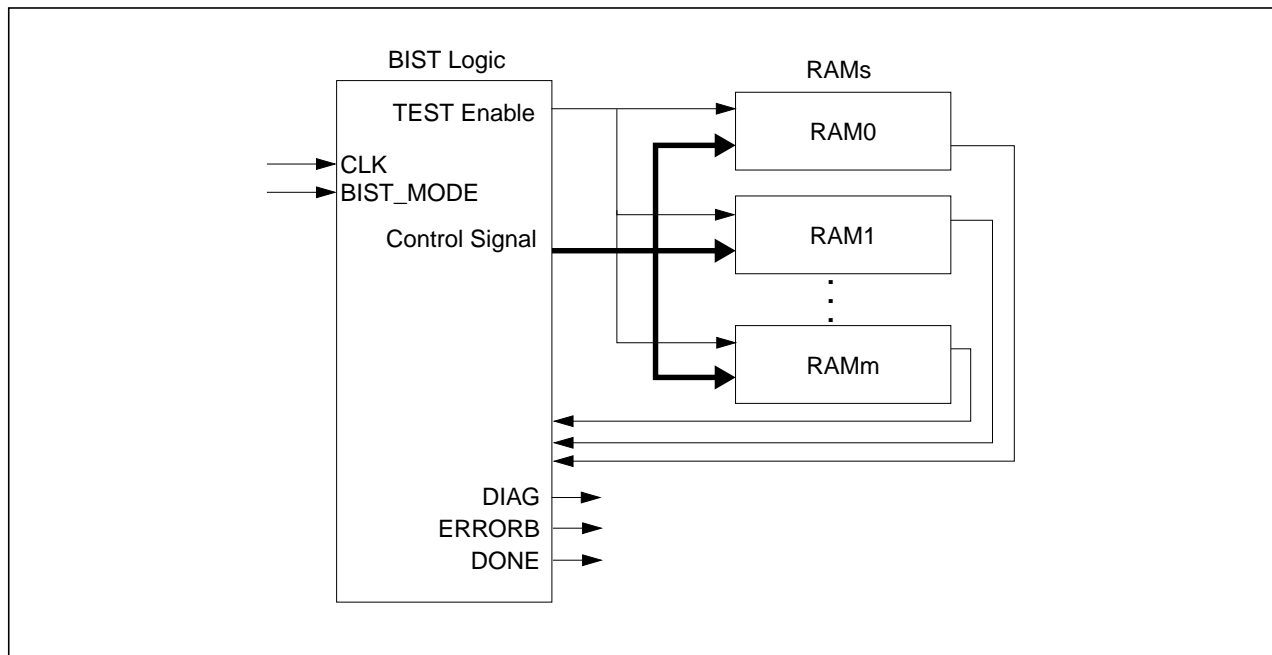
For the timing characteristics, 2-dimensional table look-up model has been adopted to yield more accuracy. Based on the combination of input slopes and output loads, the propagation delay is measured from the input crossing 50% VDD to the output crossing 50% VDD. The timing values reported in the tables are also taken from the same voltage level as the switching characteristics with 0.2ns for input slope and 10SL(Standard Load) for output load.

For the power characteristics, the average power consumption is measured on the condition that input slope is 0.2ns and output load is 10SL. Also, the power consumption depends on input switching activity. The power values reported in the tables are also taken from 50% input switching activity. For compiled memory macrocells, average read power consumption, average write power consumption and average standby power consumption are available, except that the standby power consumption is not available in ARFRAM and FIFO. Average standby power consumption is measured on the condition that CSN (Chip Select Negative) is in disable mode and other signals are in normal operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while disabling CSN signal, if possible. In dual-port memory, the average power consumption is measured on the condition that only one port is in active mode and the other port is isolated.



## BUILT-IN SELF TEST FOR COMPILED MEMORY

SEC provides engineering design services to support Built-In Self-Test (BIST) for the compiled memory macrocell. BIST circuits are designed to detect a set of fault types, such as stuck-at faults, transition faults, coupling faults and address decoder faults that adversely impact the functionality of the memory block. As shown in Fig.5-2, SEC adopts BIST architecture which is called SOA(Single Ordered Addressing) algorithm.



**Figure 5-2. Memory BIST Architecture**

From Fig.5-2, although several memory macrocells of the same types or the different types exist together in a circuit, SEC supports it as single BIST architecture. For more detailed information regarding to the BIST for compiled memory macrocells, please contact your local representative or headquarters.



## SELECTION GUIDE FOR COMPILED MEMORY

### STD110-HD (High-Density) Compiled Memory

Application	Memory Type	Description
High-Density with High-Performance	SPSRAM_HD	<ul style="list-style-type: none"> <li>- High-Density Single-port Synchronous Static RAM</li> <li>- Positive-edge clock operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio (ymux=4, 8, 16, 32)</li> </ul>
	SPSRAMBW_HD	<ul style="list-style-type: none"> <li>- High-Density Single-port Synchronous Static RAM with Bit-Write</li> <li>- Positive-edge clock operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio (ymux=4, 8, 16, 32)</li> </ul>
	DPSRAM_HD	<ul style="list-style-type: none"> <li>- High-Density Dual-port Synchronous Static RAM</li> <li>- Positive-edge clock operation</li> <li>- Flexible aspect ratio (ymux=2, 4, 8, 16)</li> </ul>
	SPARAM_HD	<ul style="list-style-type: none"> <li>- High-Density Single-port Asynchronous Static RAM</li> <li>- Synchronous write operation / Asynchronous read operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio (ymux=2, 4, 8, 16, 32)</li> </ul>
	DROM_HD	<ul style="list-style-type: none"> <li>- High-Density Synchronous Diffusion programmable ROM</li> <li>- Diffusion programmable coded</li> <li>- Positive-edge clock operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio (ymux=8, 16, 32)</li> </ul>
	MROM_HD	<ul style="list-style-type: none"> <li>- High-Density Synchronous Metal programmable ROM</li> <li>- Metal-2 programmable coded</li> <li>- Positive-edge clock operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio (ymux=8, 16, 32)</li> </ul>
	ARFRAM_HD	<ul style="list-style-type: none"> <li>- High-Density Multi-port Asynchronous Register File</li> <li>- Synchronous write operation / Asynchronous read operation</li> <li>- 1-to-2 write ports / 1-to-2 read ports</li> <li>- Flexible aspect ratio (ymux=2,4,8)</li> </ul>
	FIFO_HD	<ul style="list-style-type: none"> <li>- High-Density Synchronous First-In First-Out Memory</li> <li>- Positive-edge clock operation</li> <li>- Reset and re-transmit operation available</li> <li>- Flexible aspect ratio (ymux=4, 8, 16, 32)</li> </ul>



**STD110-LP (Low-Power) Compiled Memory**

Application	Memory Type	Description
Low-Power	SPSRAM_LP	<ul style="list-style-type: none"> <li>- Low-Power Single-port Synchronous Static RAM</li> <li>- Positive-edge clock operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio (ymux=4, 8, 16, 32)</li> </ul>
	DPSRAM_LP	<ul style="list-style-type: none"> <li>- Low-Power Dual-port Synchronous Static RAM</li> <li>- Positive-edge clock operation</li> <li>- Flexible aspect ratio (ymux=4, 8, 16, 32)</li> </ul>
	SPARAM_LP	<ul style="list-style-type: none"> <li>- Low-Power Single-port Asynchronous Static RAM</li> <li>- Synchronous write operation / Asynchronous read operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio (ymux=4, 8, 16, 32)</li> </ul>
	DROM_LP	<ul style="list-style-type: none"> <li>- Low-Power Synchronous Diffusion programmable ROM</li> <li>- Diffusion programmable coded</li> <li>- Positive-edge clock operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio (ymux=8, 16, 32)</li> </ul>
	MROM_LP	<ul style="list-style-type: none"> <li>- Low-Power Synchronous Metal programmable ROM</li> <li>- Metal-2 programmable coded</li> <li>- Positive-edge clock operation</li> <li>- Dual bank available</li> <li>- Flexible aspect ratio(ymux=8, 16, 32)</li> </ul>

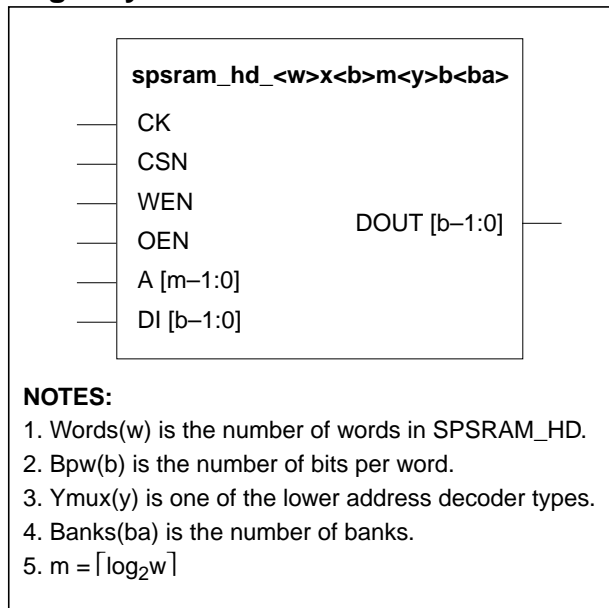


## NOTE

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### Logic Symbol



### Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

### Function Description

SPSRAM\_HD is a single-port synchronous static RAM which is provided as a compiler. SPSRAM\_HD is intended for use in high-density applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data on DI[] is written into the memory location specified on A[]. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

CK	CSN	WEN	OEN	A	DI	DOUT	COMMENT
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read Cycle

### Parameter Description

SPSRAM\_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba).



## SPSRAM\_HD

### High Density Single-Port Synchronous Static RAM

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	ba = 1	Min	32	64	128	256
		Max	1024	2048	4096	8192
		Step	16	32	64	128
	ba = 2	Min	64	128	256	512
		Max	2048	4096	8192	16384
		Step	32	64	128	256
Bpw (b)		Min	1	1	1	1
		Max	128	64	32	16
		Step	1	1	1	1

### Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If CSN is low and WEN is high on the rising edge of CK, the RAM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

### Pin Capacitance

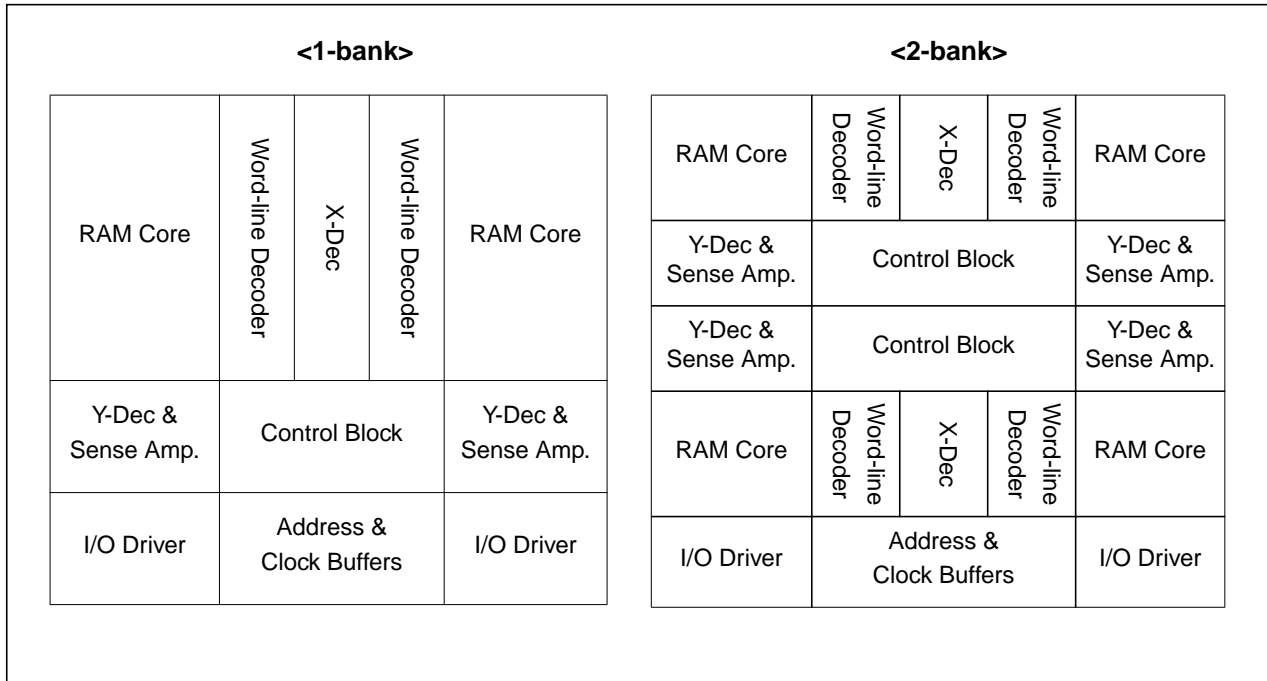
Unit: [SL]

CK	CSN	WEN	OEN	A	DI	DOUT
9.08	7.03	6.95	4.73	7.14	4.26	8.79



## Block Diagrams

SPSRAM\_HD has 2 different physical architectures due to the word depth. For a specific configuration, only one of these architectures is generated from SPSRAM\_HD compiler. In dual bank, the bank selected by the address is only activated while the other bank is in idle mode.



## Application Notes

1. Permitting Over-the-cell routing.  
In chip-level layout, over-the-cell routing in SPSRAM\_HD is permitted only for Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of SPSRAM\_HD.
4. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## SPSRAM\_HD

### High Density Single-Port Synchronous Static RAM

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#### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Clock cycle time	tckh	Clock pulse width high
tckl	Clock pulse width low	tas	Address setup time
tah	Address hold time	tcs	CSN setup time
tch	CSN hold time	tds	Data-In setup time
tdh	Data-In hold time	twc	WEN setup time
twh	WEN hold time	tacc	Data access time
tda	De-access time	tdz	DOUT drive to high-Z time
tzd	DOUT high-Z to drive time	tod	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## High Density Single-Port Synchronous Static RAM

## Reference Table

\* For Ymux=4

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	256	512	512	1024	768	1536	1024	2048
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	2.67	2.75	2.90	3.01	3.04	3.19	3.11	3.30
t <sub>ckl</sub>	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.72
t <sub>ckh</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>as</sub>	0.45	0.48	0.50	0.51	0.53	0.58	0.54	0.68
t <sub>ah</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>cs</sub>	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t <sub>ch</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ds</sub>	0.35	0.35	0.30	0.30	0.27	0.26	0.26	0.25
t <sub>dh</sub>	0.16	0.16	0.24	0.25	0.34	0.34	0.44	0.44
t <sub>ws</sub>	0.55	0.56	0.50	0.51	0.48	0.50	0.50	0.53
t <sub>wh</sub>	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t <sub>acc</sub>	2.14	2.21	2.34	2.45	2.48	2.61	2.54	2.70
t <sub>da</sub>	1.39	1.41	1.56	1.59	1.66	1.70	1.68	1.73
t <sub>dz</sub>	0.20	0.20	0.23	0.23	0.24	0.24	0.24	0.26
t <sub>zd</sub>	0.23	0.23	0.26	0.26	0.28	0.28	0.28	0.28
t <sub>od</sub>	0.72	0.72	0.81	0.81	0.92	0.92	1.03	1.03
Power (μW/MHz)								
Power_read	241.57	268.41	442.37	488.18	644.43	713.65	847.72	944.82
Power_write	291.60	322.60	584.59	641.00	921.25	1009.78	1301.57	1428.97
Power_standby	57.06	73.89	106.31	141.11	155.35	216.27	204.19	299.40
Area (μm)								
Width	1145.58	1145.58	2087.66	2087.66	3029.74	3029.74	3971.82	3971.82
Height	247.02	444.94	375.54	701.97	504.05	959.01	632.57	1216.04

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



# SPSRAM\_HD

## High Density Single-Port Synchronous Static RAM

### Reference Table

\* For Ymux=8

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	2.67	2.75	2.90	3.02	3.05	3.20	3.11	3.30
t <sub>ckl</sub>	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.72
t <sub>ckh</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>as</sub>	0.43	0.47	0.46	0.50	0.48	0.53	0.47	0.56
t <sub>ah</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>cs</sub>	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t <sub>ch</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ds</sub>	0.37	0.36	0.33	0.33	0.31	0.30	0.30	0.29
t <sub>dh</sub>	0.14	0.14	0.20	0.20	0.26	0.26	0.33	0.33
t <sub>ws</sub>	0.55	0.56	0.50	0.52	0.48	0.50	0.50	0.52
t <sub>wh</sub>	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t <sub>acc</sub>	2.14	2.21	2.35	2.45	2.48	2.62	2.54	2.71
t <sub>da</sub>	1.39	1.41	1.56	1.59	1.66	1.70	1.69	1.73
t <sub>dz</sub>	0.19	0.19	0.21	0.21	0.22	0.22	0.23	0.23
t <sub>zd</sub>	0.22	0.22	0.24	0.24	0.26	0.26	0.26	0.26
t <sub>od</sub>	0.70	0.70	0.77	0.77	0.84	0.84	0.92	0.92
Power (μW/MHz)								
Power_read	207.03	229.54	369.82	404.52	533.06	581.99	696.75	761.96
Power_write	244.00	270.27	464.85	508.31	707.23	771.09	971.11	1058.63
Power_standby	31.58	45.74	54.37	79.95	76.86	118.01	99.04	159.92
Area (μm)								
Width	1145.58	1145.58	2087.66	2087.66	3029.74	3029.74	3971.82	3971.82
Height	247.02	444.94	375.54	701.97	504.05	959.01	632.57	1216.04

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



## High Density Single-Port Synchronous Static RAM

## Reference Table

\* For Ymux=16

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	2.70	2.81	2.93	3.07	3.08	3.26	3.15	3.36
t <sub>ckl</sub>	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.72
t <sub>ckh</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>as</sub>	0.57	0.61	0.60	0.65	0.63	0.68	0.66	0.72
t <sub>ah</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>cs</sub>	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t <sub>ch</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ds</sub>	0.37	0.37	0.34	0.35	0.32	0.35	0.31	0.35
t <sub>dh</sub>	0.13	0.13	0.17	0.17	0.23	0.23	0.28	0.28
t <sub>ws</sub>	0.55	0.56	0.50	0.52	0.48	0.50	0.50	0.52
t <sub>wh</sub>	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t <sub>acc</sub>	2.17	2.26	2.38	2.50	2.51	2.67	2.57	2.76
t <sub>da</sub>	1.39	1.41	1.56	1.59	1.66	1.70	1.69	1.73
t <sub>dz</sub>	0.18	0.18	0.20	0.20	0.21	0.21	0.22	0.22
t <sub>zd</sub>	0.21	0.21	0.23	0.23	0.24	0.24	0.25	0.25
t <sub>od</sub>	0.69	0.69	0.75	0.75	0.80	0.80	0.86	0.86
Power (μW/MHz)								
Power_read	189.69	211.57	335.71	368.00	481.75	525.63	627.82	684.07
Power_write	220.81	245.81	408.49	447.98	606.72	662.40	815.51	889.07
Power_standby	26.07	43.74	41.79	70.58	57.20	99.25	72.30	129.73
Area (μm)								
Width	1145.58	1145.58	2087.66	2087.66	3029.74	3029.74	3971.82	3971.82
Height	247.02	444.94	375.54	701.97	504.05	959.01	632.57	1216.04

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



# SPSRAM\_HD

## High Density Single-Port Synchronous Static RAM

### Reference Table

\* For Ymux=32

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

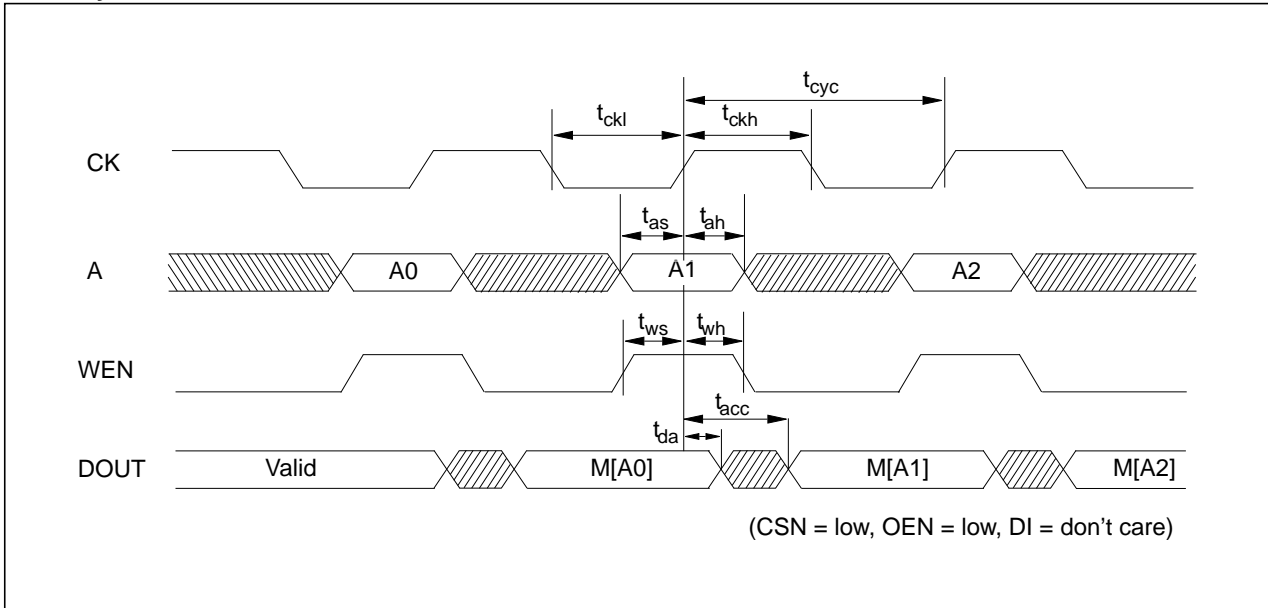
Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	4	4	8	8	12	12	16	16
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	2.75	2.91	2.99	3.18	3.15	3.37	3.22	3.47
t <sub>ckl</sub>	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.72
t <sub>ckh</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>as</sub>	0.56	0.59	0.57	0.61	0.57	0.63	0.58	0.64
t <sub>ah</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>cs</sub>	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t <sub>ch</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ds</sub>	0.37	0.60	0.35	0.60	0.33	0.62	0.32	0.64
t <sub>dh</sub>	0.12	0.12	0.17	0.17	0.21	0.21	0.25	0.25
t <sub>ws</sub>	0.56	0.57	0.50	0.52	0.48	0.50	0.50	0.52
t <sub>wh</sub>	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t <sub>acc</sub>	2.21	2.35	2.43	2.60	2.57	2.77	2.63	2.86
t <sub>da</sub>	1.38	1.40	1.56	1.59	1.66	1.70	1.68	1.73
t <sub>dz</sub>	0.18	0.18	0.20	0.20	0.21	0.21	0.21	0.21
t <sub>zd</sub>	0.21	0.21	0.22	0.22	0.24	0.24	0.24	0.24
t <sub>od</sub>	0.69	0.69	0.74	0.74	0.78	0.78	0.83	0.83
Power (μW/MHz)								
Power_read	180.53	201.95	318.87	350.17	456.78	498.53	594.26	647.71
Power_write	207.22	231.24	378.35	415.74	554.34	605.89	735.19	801.71
Power_standby	19.88	35.95	29.68	55.03	39.17	74.90	48.36	95.57
Area (μm)								
Width	1145.58	1145.58	2087.66	2087.66	3029.74	3029.74	3971.82	3971.82
Height	247.02	444.94	375.54	701.97	504.05	959.01	632.57	1216.04

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.

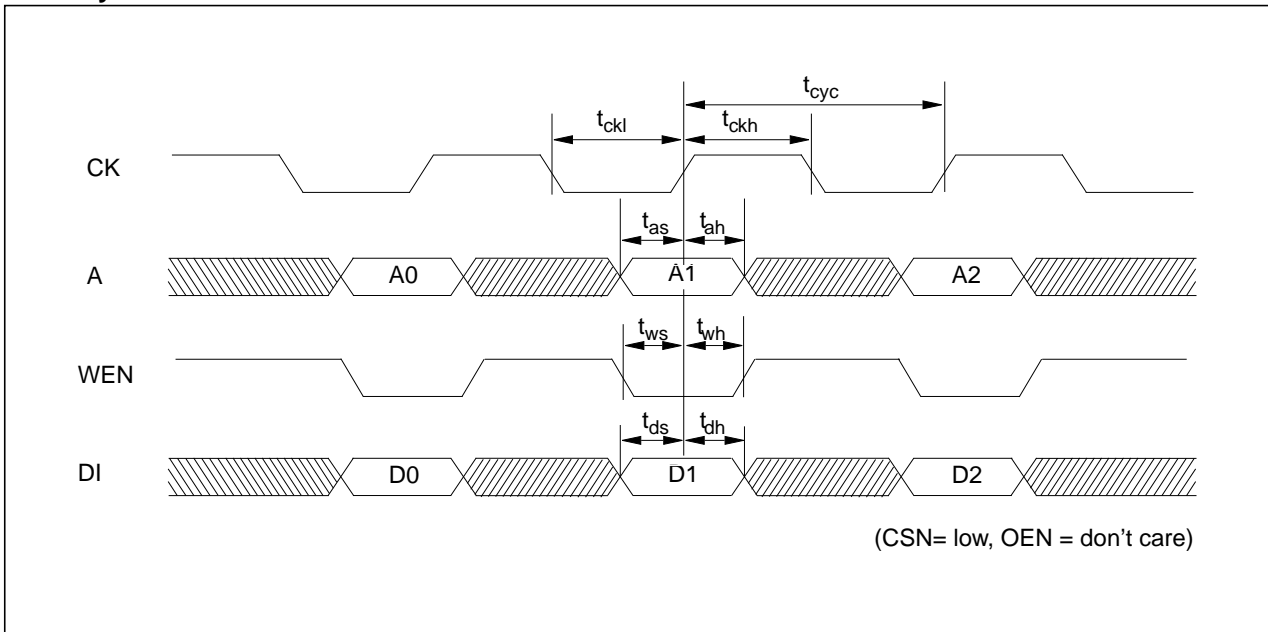


## High Density Single-Port Synchronous Static RAM

## Read Cycle



## Write Cycle

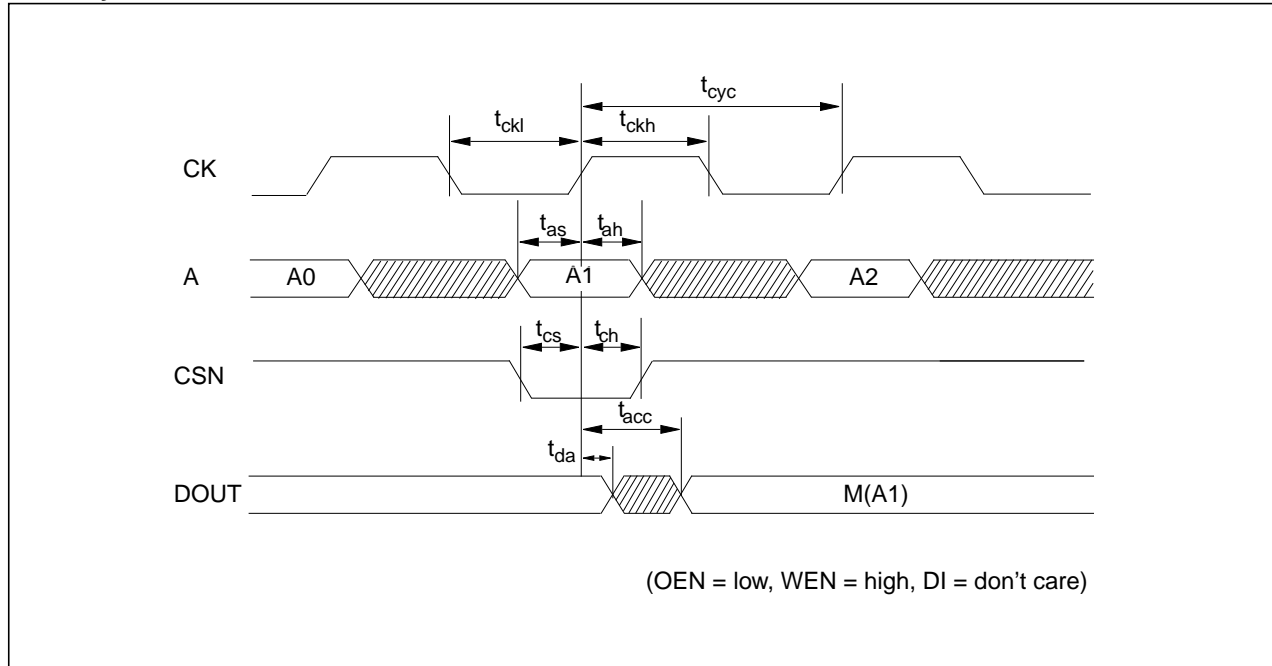




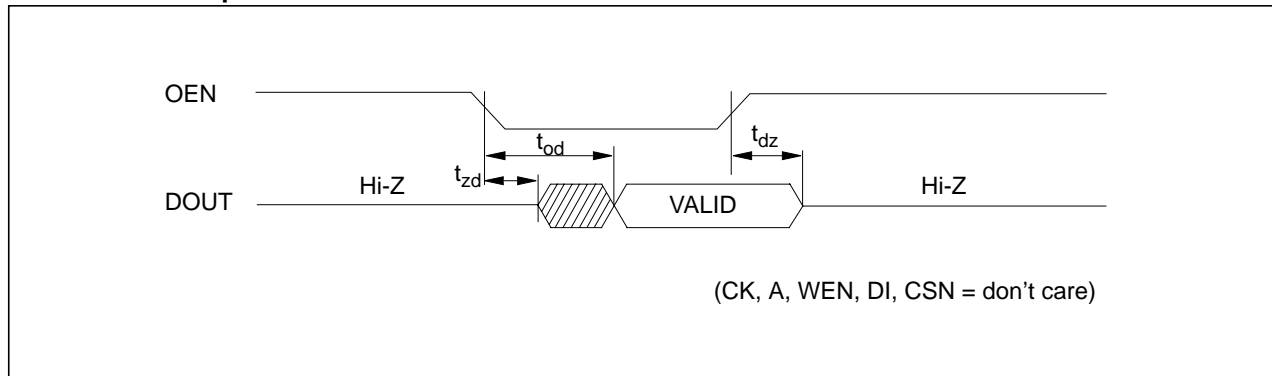
## SPSRAM\_HD

### High Density Single-Port Synchronous Static RAM

#### Read Cycle with CSN Controlled



#### OEN Control Output Enable

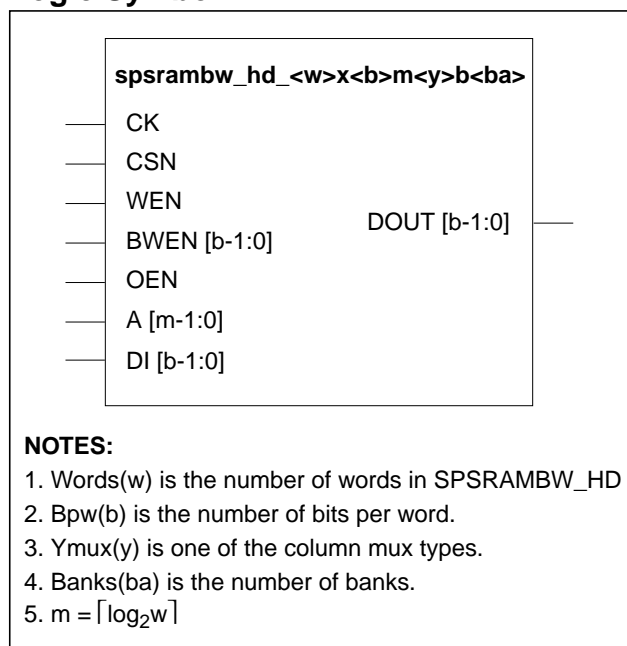


**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## High Density Single-Port Synchronous SRAM with Bit-write

## Logic Symbol



## Features

- Suitable for high-density application
- Bit-Write capability
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tristate output
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 256Kbits capacity
- Up to 8K number of words
- Up to 256 number of bit per word

## Function Description

SPSRAMBW\_HD is a single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMBW\_HD is intended for use in high-density applications. Basically, its functionality is exactly same as SPSRAM\_HD except a bit-write operation which is controlled by BWEN[], named bit-write enable signal bus. Each bit of BWEN[] enables or disables the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data bits in DI[], which their corresponding bit(s) in BWEN[] are low, are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM\_HD. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

## SPSRAMBW\_HD Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	OEN makes tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read Cycle



# SPSRAMBW\_HD

## High Density Single-Port Synchronous SRAM with Bit-write

### Parameter Description

SPSRAMBW\_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and number of banks(ba)

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	ba = 1	Min	32	64	128	256
		Max	1024	2048	4096	8192
		Step	16	32	64	128
	ba = 2	Min	64	128	256	512
		Max	2048	4096	8192	16384
		Step	32	64	128	256
Bpw (b)		Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

### Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If CSN is low and WEN is high on the rising edge of CK, the RAM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
BWEN[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A[]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI[]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT[]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.



## High Density Single-Port Synchronous SRAM with Bit-write

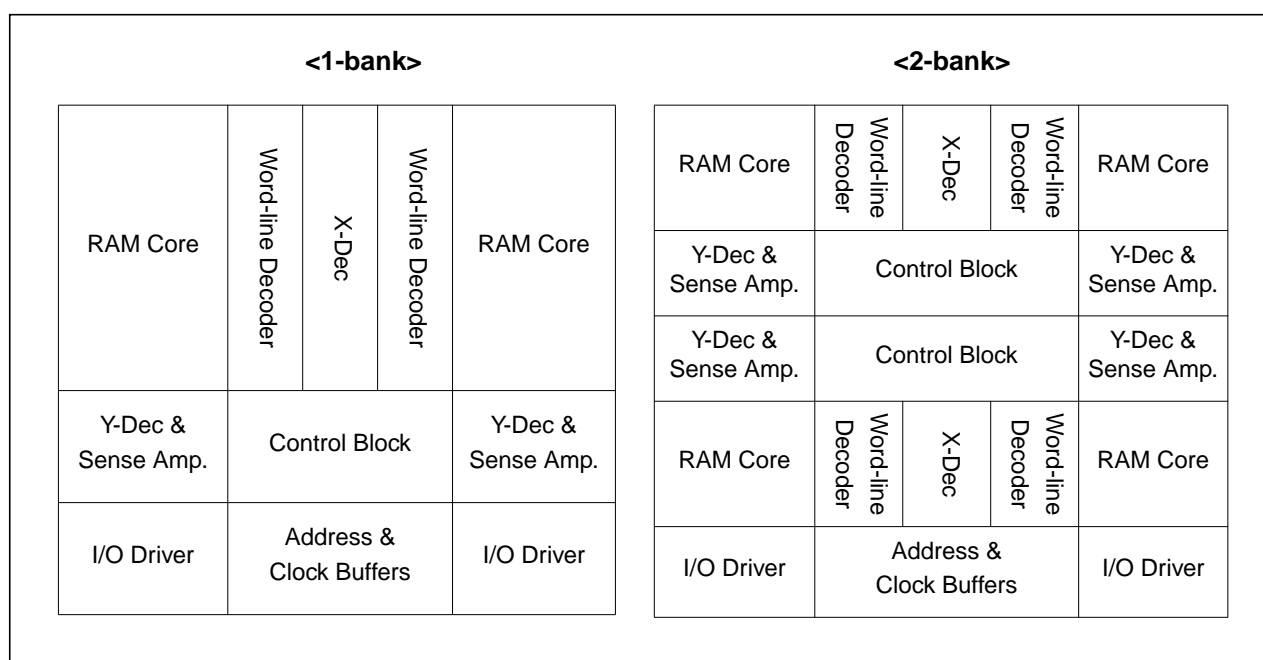
## Pin Capacitance

Unit: [SL]

CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
9.08	7.03	6.95	4.26	4.73	7.14	4.26	8.79

## Block Diagrams

SPSRAMBW\_HD has 2 different physical architectures due to the word depth. For a specific configuration, only one of these architectures is generated from SPSRAMBW\_HD compiler. In dual bank, the bank selected by the address is only activated while the other bank is in idle mode.



## Application Notes

1. Permitting Over-the-cell routing  
In chip-level layout, over-the-cell routing in SPSRAMBW\_HD is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of SPSRAMBW\_HD.
4. A byte-write or word-write operation will be supported with SPSRAMBW\_HD.  
Please refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPSRAM\_HD. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.
5. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## SPSRAMBW\_HD

### High Density Single-Port Synchronous SRAM with Bit-write

#### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Clock cycle time	tckh	Clock pulse width high
tckl	Clock pulse width low	tas	Address setup time
tah	Address hold time	tcs	CSN setup time
tch	CSN hold time	tds	Data-In setup time
tdh	Data-In hold time	tws	WEN setup time
twh	WEN hold time	tbws	BWEN setup time
tbwh	BWEN hold time	tacc	Data access time
tda	De-access time	tdz	DOUT drive to high-Z time
tzd	DOUT high-Z to drive time	tod	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## High Density Single-Port Synchronous SRAM with Bit-write

## Reference Table

\* For Ymux=4

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	256	512	512	1024	768	1536	1024	2048
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	2.67	2.75	2.90	3.01	3.04	3.19	3.11	3.30
t <sub>ckl</sub>	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.72
t <sub>ckh</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>as</sub>	0.45	0.48	0.50	0.51	0.53	0.58	0.54	0.68
t <sub>ah</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>cs</sub>	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t <sub>ch</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ds</sub>	0.35	0.35	0.30	0.30	0.27	0.26	0.26	0.25
t <sub>dh</sub>	0.16	0.16	0.24	0.25	0.34	0.34	0.44	0.44
t <sub>ws</sub>	0.55	0.56	0.50	0.51	0.48	0.50	0.50	0.53
t <sub>wh</sub>	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t <sub>bws</sub>	0.42	0.45	0.38	0.44	0.35	0.44	0.33	0.45
t <sub>bwh</sub>	0.14	0.14	0.22	0.22	0.31	0.31	0.41	0.41
t <sub>acc</sub>	2.14	2.21	2.34	2.45	2.48	2.61	2.54	2.70
t <sub>da</sub>	1.39	1.41	1.56	1.59	1.66	1.70	1.68	1.73
t <sub>dz</sub>	0.20	0.20	0.23	0.23	0.24	0.24	0.24	0.24
t <sub>zd</sub>	0.23	0.23	0.26	0.26	0.28	0.28	0.28	0.28
t <sub>od</sub>	0.72	0.72	0.81	0.81	0.92	0.92	1.03	1.03
Power (μW/MHz)								
Power_read	255.46	287.55	470.50	534.89	686.77	796.08	904.26	1071.12
Power_write	304.34	337.62	610.64	671.87	960.30	1056.66	1353.31	1492.00
Power_standby	69.94	89.11	132.72	172.39	195.27	263.75	257.60	363.18
Area (μm)								
Width	1145.58	1145.58	2087.66	2087.66	3029.74	3029.74	3971.82	3971.82
Height	247.02	444.94	375.54	701.97	504.05	959.01	632.57	1216.04

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



# SPSRAMBW\_HD

## High Density Single-Port Synchronous SRAM with Bit-write

### Reference Table

\* For Ymux=8

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	2.67	2.75	2.90	3.02	3.05	3.20	3.11	3.30
t <sub>ckl</sub>	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.72
t <sub>ckh</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>as</sub>	0.43	0.47	0.46	0.50	0.48	0.53	0.47	0.56
t <sub>ah</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>cs</sub>	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t <sub>ch</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ds</sub>	0.37	0.36	0.33	0.33	0.31	0.30	0.30	0.29
t <sub>dh</sub>	0.14	0.14	0.20	0.20	0.26	0.26	0.33	0.33
t <sub>ws</sub>	0.55	0.56	0.50	0.52	0.48	0.50	0.50	0.52
t <sub>wh</sub>	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t <sub>bws</sub>	0.42	0.45	0.38	0.45	0.35	0.44	0.33	0.44
t <sub>bwh</sub>	0.12	0.12	0.18	0.18	0.24	0.24	0.31	0.31
t <sub>acc</sub>	2.14	2.21	2.35	2.45	2.48	2.62	2.54	2.71
t <sub>da</sub>	1.39	1.41	1.56	1.59	1.66	1.70	1.69	1.73
t <sub>dz</sub>	0.19	0.19	0.21	0.21	0.22	0.22	0.23	0.23
t <sub>zd</sub>	0.22	0.22	0.24	0.24	0.26	0.26	0.26	0.26
t <sub>od</sub>	0.70	0.70	0.77	0.77	0.84	0.84	0.92	0.92
Power (μW/MHz)								
Power_read	214.55	239.49	385.13	428.85	556.10	624.86	727.48	827.51
Power_write	250.40	279.24	478.61	526.86	728.29	799.36	999.45	1096.73
Power_standby	38.12	54.83	68.24	98.86	98.06	146.85	127.56	198.79
Area (μm)								
Width	1145.58	1145.58	2087.66	2087.66	3029.74	3029.74	3971.82	3971.82
Height	247.02	444.94	375.54	701.97	504.05	959.01	632.57	1216.04

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



## High Density Single-Port Synchronous SRAM with Bit-write

## Reference Table

\* For Ymux=16

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	2.70	2.81	2.93	3.07	3.08	3.26	3.15	3.36
t <sub>ckl</sub>	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.72
t <sub>ckh</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>as</sub>	0.57	0.61	0.60	0.65	0.63	0.68	0.66	0.72
t <sub>ah</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>cs</sub>	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t <sub>ch</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ds</sub>	0.37	0.37	0.34	0.35	0.32	0.35	0.31	0.35
t <sub>dh</sub>	0.13	0.13	0.17	0.17	0.23	0.23	0.28	0.28
t <sub>ws</sub>	0.55	0.56	0.50	0.52	0.48	0.50	0.50	0.52
t <sub>wh</sub>	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t <sub>bws</sub>	0.43	0.48	0.39	0.47	0.37	0.47	0.35	0.47
t <sub>bwh</sub>	0.11	0.11	0.16	0.16	0.21	0.21	0.26	0.26
t <sub>acc</sub>	2.17	2.26	2.38	2.50	2.51	2.67	2.57	2.76
t <sub>da</sub>	1.39	1.41	1.56	1.59	1.66	1.70	1.69	1.73
t <sub>dz</sub>	0.18	0.18	1.20	0.20	0.21	0.21	0.22	0.22
t <sub>zd</sub>	0.21	0.21	0.23	0.23	0.24	0.24	0.25	0.25
t <sub>od</sub>	0.69	0.69	0.75	0.75	0.80	0.80	0.86	0.86
Power (μW/MHz)								
Power_read	194.40	217.74	345.29	382.79	496.26	551.18	647.29	722.90
Power_write	224.02	251.54	415.78	460.27	618.19	681.30	831.26	914.62
Power_standby	29.41	49.55	49.30	83.11	68.88	118.58	88.15	155.97
Area (μm)								
Width	1145.58	1145.58	2087.66	2087.66	3029.74	3029.74	3971.82	3971.82
Height	247.02	444.94	375.54	701.97	504.05	959.01	632.57	1216.04

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



# SPSRAMBW\_HD

## High Density Single-Port Synchronous SRAM with Bit-write

### Reference Table

\* For Ymux=32

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

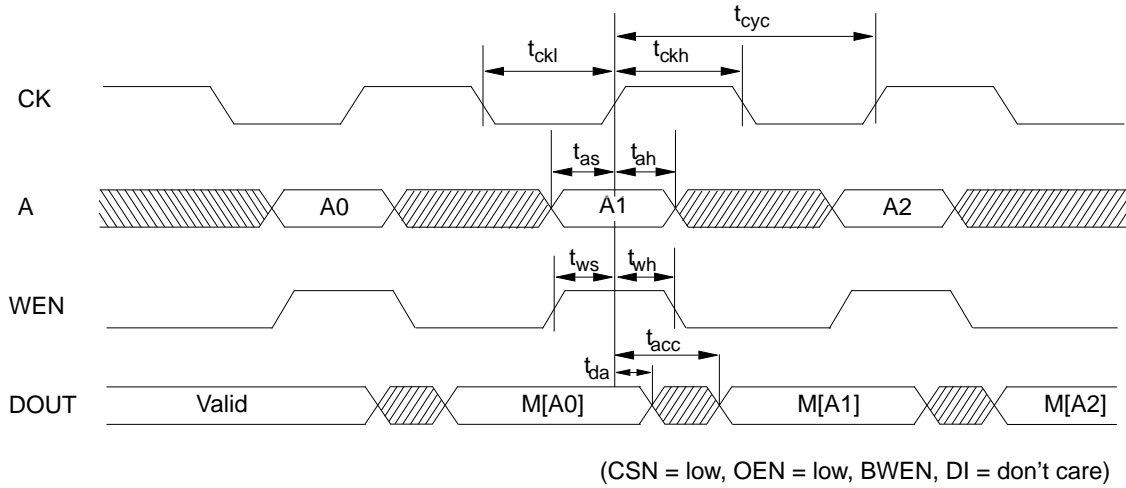
Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	4	4	8	8	12	12	16	16
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	2.75	2.91	2.99	3.18	3.15	3.37	3.22	3.47
t <sub>ckl</sub>	0.72	0.72	0.72	0.72	0.72	0.72	0.72	0.72
t <sub>ckh</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>as</sub>	0.56	0.59	0.57	0.61	0.57	0.63	0.58	0.64
t <sub>ah</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>cs</sub>	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29
t <sub>ch</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ds</sub>	0.37	0.60	0.35	0.60	0.33	0.62	0.32	0.64
t <sub>dh</sub>	0.12	0.12	0.17	0.17	0.21	0.21	0.25	0.25
t <sub>ws</sub>	0.56	0.57	0.50	0.52	0.48	0.50	0.50	0.52
t <sub>wh</sub>	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t <sub>bws</sub>	0.46	0.52	0.42	0.52	0.39	0.53	0.37	0.54
t <sub>bwh</sub>	0.10	0.10	0.15	0.15	0.19	0.19	0.23	0.23
t <sub>acc</sub>	2.21	2.35	2.43	2.60	2.57	2.77	2.63	2.86
t <sub>da</sub>	1.38	1.40	1.56	1.59	1.66	1.70	1.68	1.73
t <sub>dz</sub>	0.18	0.18	0.20	0.20	0.21	0.21	0.21	0.21
t <sub>zd</sub>	0.21	0.21	0.22	0.22	0.24	0.24	0.24	0.24
t <sub>od</sub>	0.69	0.69	0.74	0.74	0.78	0.78	0.83	0.83
Power (μW/MHz)								
Power_read	183.69	206.04	325.65	360.13	467.36	515.57	608.81	672.35
Power_write	208.66	234.93	382.40	424.64	561.15	620.17	744.92	821.51
Power_standby	21.53	39.89	33.97	64.20	46.10	89.42	57.93	115.55
Area (μm)								
Width	1145.58	1144.58	2087.66	2087.66	3029.74	3029.74	3971.82	3971.82
Height	247.02	444.94	375.54	701.97	504.05	959.01	632.57	1216.04

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.

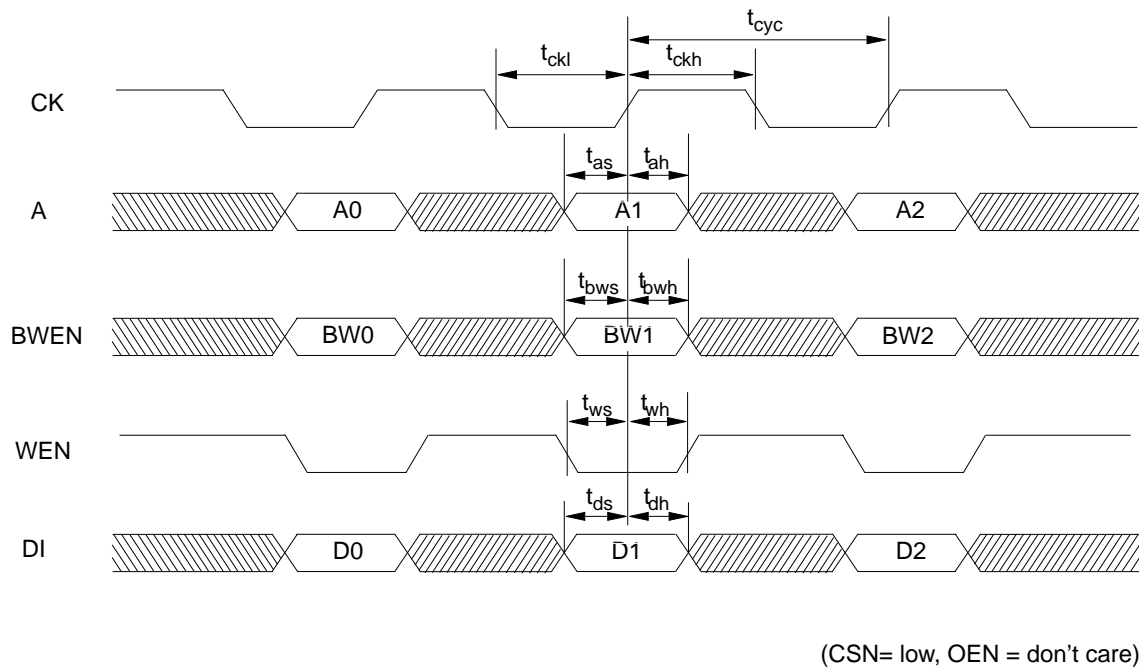


## High Density Single-Port Synchronous SRAM with Bit-write

## Read Cycle



## Write Cycle

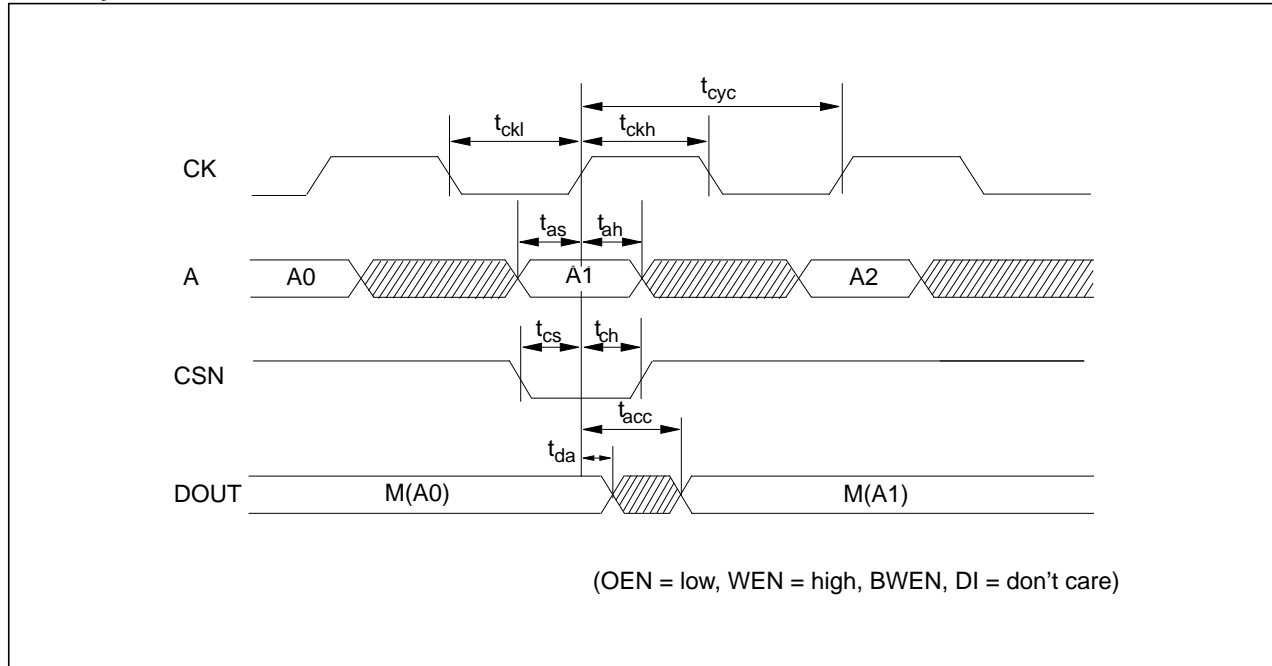




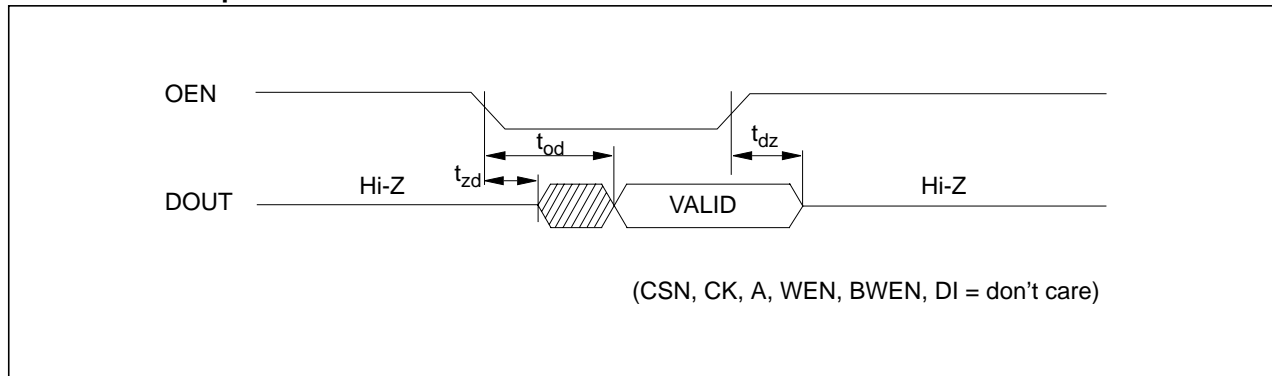
## SPSRAMBW\_HD

### High Density Single-Port Synchronous SRAM with Bit-write

#### Read Cycle with CSN Controlled



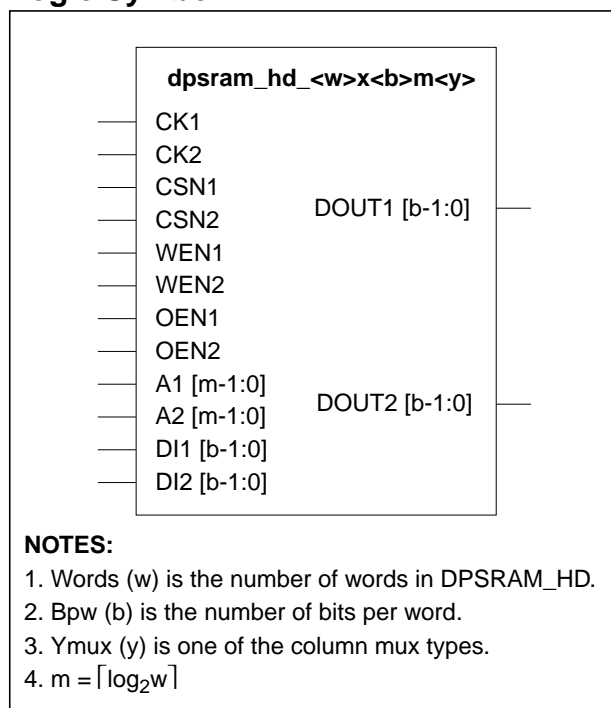
#### OEN Control Output Enable



**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## Logic Symbol



## Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 128Kbits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

## Function Description

DPSRAM\_HD is a dual-port synchronous static RAM which is provided as a compiler. DPSRAM\_HD is intended for use in high-density applications. Each port is fully independent. On the rising edge of CK1(CK2), the write cycle is initiated when WEN1 (WEN2) is low and CSN1 (CSN2) is low. The data on DI1[] (DI2[]) is written into the memory location specified on A1[(A2)]. During the write cycle, DOUT1[] (DOUT2[]) remains stable. On the rising edge of CK1(CK2), the read cycle is initiated when WEN1 (WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[] (DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, DI1[] (DI2[]) are disabled, data stored in the memory is retained and DOUT1[] (DOUT2[]) remains stable. When OEN1 (OEN2) is high, DOUT1[] (DOUT2[]) is placed in a high-impedance state.

DPSRAM\_HD Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read Cycle



# DPSRAM\_HD

## High-Density Dual-Port Synchronous Static RAM

### Parameter Description

DPSRAM\_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y).

Parameters		YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16
Words (w)	Min	16	32	64	128
	Max	1024	2048	4096	8192
	Step	8	16	32	64
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

### Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode.
CSN1 CSN2	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [] A2 []	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [] DI2 []	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [] DOUT2 []	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

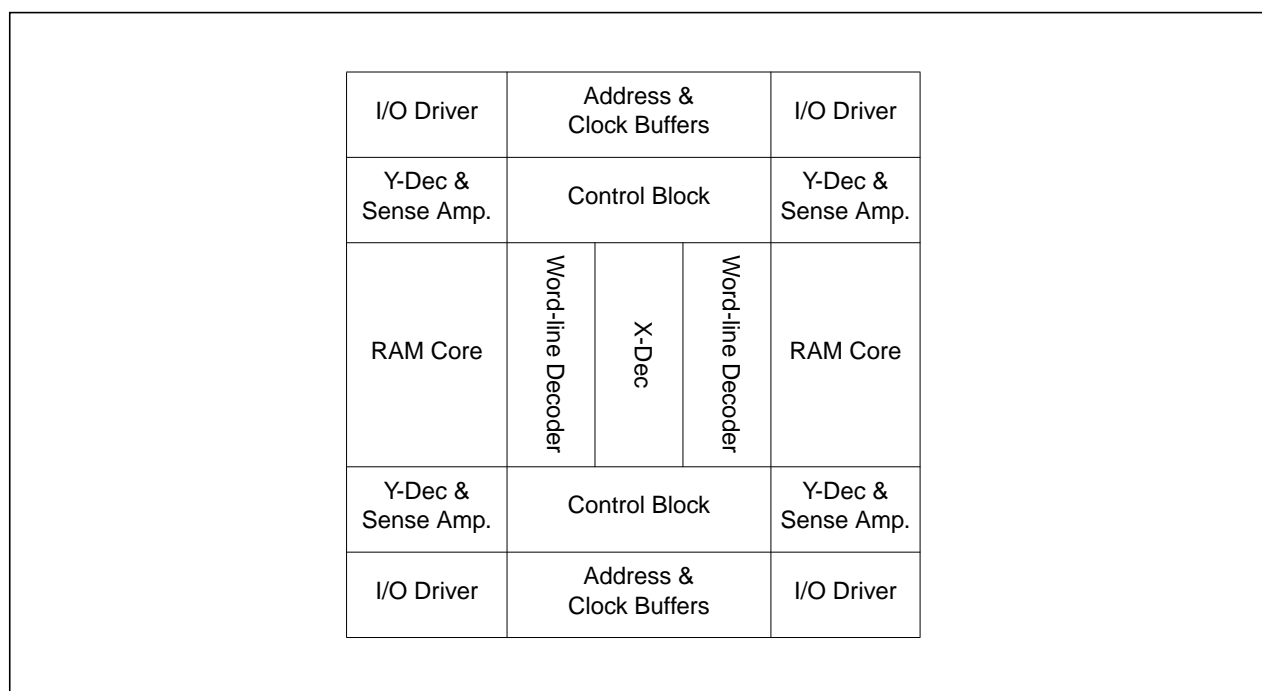
### Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT
28.53	8.37	7.68	5.66	8.23	4.60	9.13



## Block Diagram



## Application Notes

1. Permitting Over-the-cell routing  
In chip-level layout, over-the-cell routing in DPSRAM\_HD is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of DPSRAM\_HD.
4. Contention mode in same address access  
In DPSRAM\_HD, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAM\_HD has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.
5. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while stanby mode.



# DPSRAM\_HD

## High-Density Dual-Port Synchronous Static RAM

### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Clock cycle time	tckl	Clock pulse width low
tckh	Clock pulse width high	tcc	Clock to Clock Setup time
tas	Address setup time	tah	Address hold time
tcs	CSN setup time	tch	CSN hold time
tds	Data-In setup time	tdh	Data-In hold time
twS	WEN setup time	twh	WEN hold time
tacc	Data access time	tda	De-access time
tdz	DOUT drive to high-Z time	tzd	DOUT high-Z to drive time
tod	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## Reference Table

\* For Ymux=2 (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	256	512	768	1024
bpw	32	64	96	128
Timing (ns)				
t <sub>cyc</sub>	3.43	3.94	4.36	4.70
t <sub>ckl</sub>	0.88	0.86	0.86	0.86
t <sub>ckh</sub>	0.59	0.63	0.69	0.78
t <sub>cc</sub>	1.74	2.25	2.46	2.92
t <sub>as</sub>	0.41	0.40	0.40	0.39
t <sub>ah</sub>	0.27	0.27	0.27	0.27
t <sub>cs</sub>	0.36	0.35	0.36	0.36
t <sub>ch</sub>	0.27	0.27	0.27	0.27
t <sub>ds</sub>	0.26	0.26	0.26	0.26
t <sub>dh</sub>	0.56	0.64	0.70	0.77
t <sub>ws</sub>	0.38	0.38	0.38	0.38
t <sub>wh</sub>	0.27	0.27	0.27	0.27
t <sub>acc</sub>	2.81	3.29	3.64	3.88
t <sub>da</sub>	1.88	2.24	2.50	2.68
t <sub>dz</sub>	0.52	0.59	0.67	0.75
t <sub>zd</sub>	0.63	0.70	0.77	0.84
t <sub>od</sub>	0.73	0.80	0.87	0.96
Power (μW/MHz)				
Power_read	252.60	467.66	715.73	996.83
Power_write	330.45	661.87	1066.43	1544.15
Power_standby	42.46	49.53	56.46	63.27
Area (μm)				
Width	954.08	1645.28	2336.48	3027.68
Height	541.34	839.85	1138.35	1436.86

## NOTES:

1. In power consumption of DPSRAM\_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## Reference Table

\* For Ymux=4 (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	512	1024	1536	2048
bpw	16	32	48	64
Timing (ns)				
t <sub>cyc</sub>	3.19	3.66	4.13	4.60
t <sub>ckl</sub>	0.88	0.86	0.85	0.86
t <sub>ckh</sub>	0.59	0.59	0.61	0.63
t <sub>cc</sub>	1.74	2.25	2.64	2.92
t <sub>as</sub>	0.41	0.40	0.40	0.39
t <sub>ah</sub>	0.27	0.27	0.27	0.27
t <sub>cs</sub>	0.35	0.35	0.35	0.35
t <sub>ch</sub>	0.27	0.27	0.27	0.27
t <sub>ds</sub>	0.10	0.10	0.10	0.10
t <sub>dh</sub>	0.48	0.52	0.57	0.62
t <sub>ws</sub>	0.38	0.38	0.38	0.38
t <sub>wh</sub>	0.27	0.27	0.27	0.27
t <sub>acc</sub>	2.78	3.25	3.60	3.84
t <sub>da</sub>	1.85	2.21	2.47	2.64
t <sub>dz</sub>	0.50	0.54	0.59	0.64
t <sub>zd</sub>	0.60	0.65	0.70	0.74
t <sub>od</sub>	0.70	0.75	0.80	0.85
Power (μW/MHz)				
Power_read	225.40	417.84	643.21	901.51
Power_write	272.29	524.02	823.22	1169.90
Power_standby	35.66	41.21	46.81	52.46
Area (μm)				
Width	954.08	1645.28	2336.48	3027.68
Height	541.34	839.85	1138.35	1436.86

## NOTES:

1. In power consumption of DPSRAM\_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



# DPSRAM\_HD

## High-Density Dual-Port Synchronous Static RAM

### Reference Table

\* For Ymux=8 (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	512	1024	1536	2048
bpw	16	32	48	64
Timing (ns)				
t <sub>cyc</sub>	3.19	3.66	4.13	4.60
t <sub>ckl</sub>	0.88	0.86	0.85	0.86
t <sub>ckh</sub>	0.59	0.59	0.61	0.63
t <sub>cc</sub>	1.74	2.25	2.64	2.92
t <sub>as</sub>	0.41	0.40	0.40	0.39
t <sub>ah</sub>	0.27	0.27	0.27	0.27
t <sub>cs</sub>	0.35	0.35	0.35	0.35
t <sub>ch</sub>	0.27	0.27	0.27	0.27
t <sub>ds</sub>	0.10	0.10	0.10	0.10
t <sub>dh</sub>	0.48	0.52	0.57	0.62
t <sub>ws</sub>	0.38	0.38	0.38	0.38
t <sub>wh</sub>	0.27	0.27	0.27	0.27
t <sub>acc</sub>	2.78	3.25	3.60	3.84
t <sub>da</sub>	1.85	2.21	2.47	2.64
t <sub>dz</sub>	0.50	0.54	0.59	0.64
t <sub>zd</sub>	0.60	0.65	0.70	0.74
t <sub>od</sub>	0.70	0.75	0.80	0.85
Power (μW/MHz)				
Power_read	225.40	417.84	643.21	901.51
Power_write	272.29	524.02	823.22	1169.90
Power_standby	35.66	41.21	46.81	52.46
Area (μm)				
Width	954.08	1645.28	2336.48	3027.68
Height	541.34	839.85	1138.35	1436.86

#### NOTES:

1. In power consumption of DPSRAM\_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



# DPSRAM\_HD

## High-Density Dual-Port Synchronous Static RAM

### Reference Table

\* For Ymux=16 (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	2048	4096	6144	8192
bpw	4	8	12	16
Timing (ns)				
t <sub>cyc</sub>	3.26	3.72	4.17	4.63
t <sub>ckl</sub>	0.90	0.90	0.91	0.93
t <sub>ckh</sub>	0.59	0.59	0.59	0.59
t <sub>cc</sub>	1.75	2.25	2.64	2.92
t <sub>as</sub>	0.53	0.53	0.53	0.55
t <sub>ah</sub>	0.27	0.27	0.27	0.27
t <sub>cs</sub>	0.36	0.35	0.36	0.36
t <sub>ch</sub>	0.27	0.27	0.27	0.27
t <sub>ds</sub>	0.10	0.10	0.10	0.10
t <sub>dh</sub>	0.46	0.48	0.51	0.54
t <sub>ws</sub>	0.38	0.38	0.38	0.38
t <sub>wh</sub>	0.27	0.27	0.27	0.27
t <sub>acc</sub>	2.85	3.31	3.67	3.91
t <sub>da</sub>	1.91	2.26	2.53	2.70
t <sub>dz</sub>	0.48	0.50	0.53	0.56
t <sub>zd</sub>	0.58	0.61	0.63	0.66
t <sub>od</sub>	0.69	0.71	0.74	0.77
Power (μW/MHz)				
Power_read	215.68	391.61	599.53	839.42
Power_write	220.61	395.55	598.37	829.10
Power_standby	36.67	42.75	48.88	55.05
Area (μm)				
Width	954.08	1645.28	2336.48	3027.68
Height	541.34	839.85	1138.35	1436.86

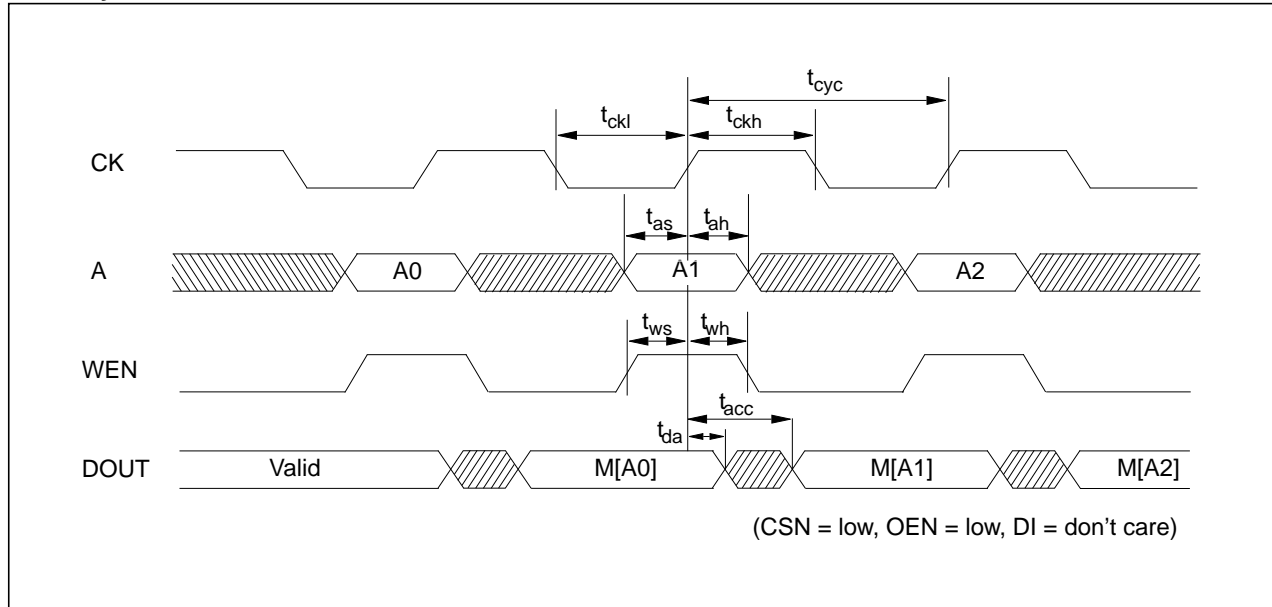
#### NOTES:

1. In power consumption of DPSRAM\_HD, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

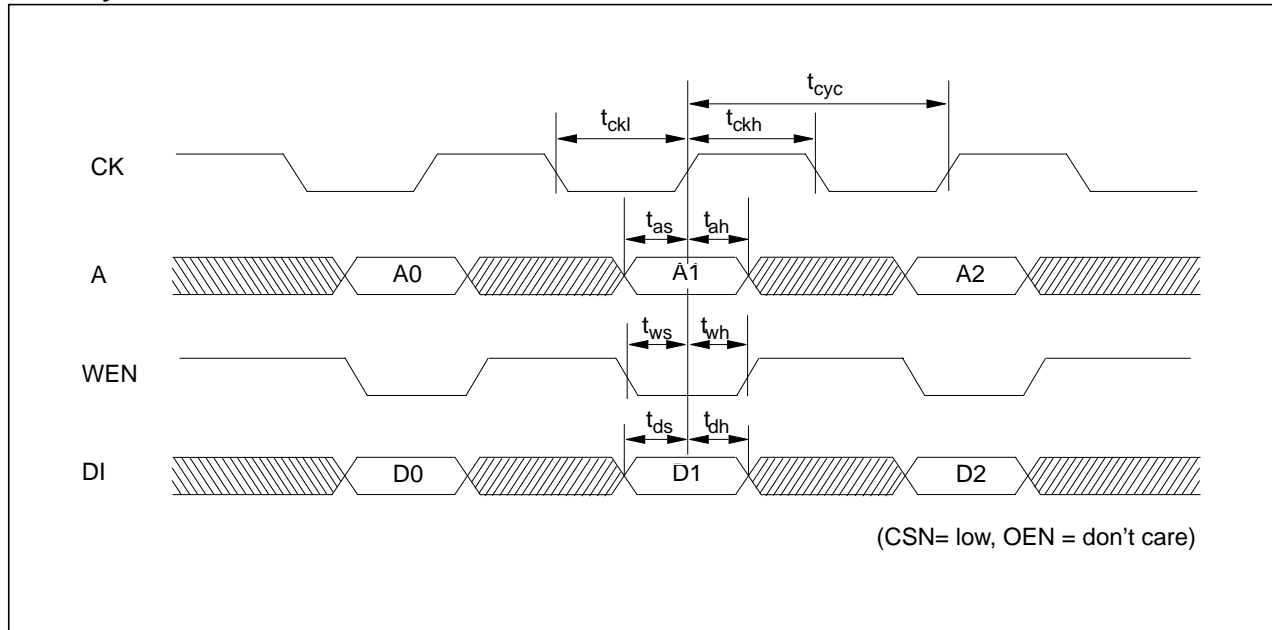


## Timing Diagrams

## Read Cycle



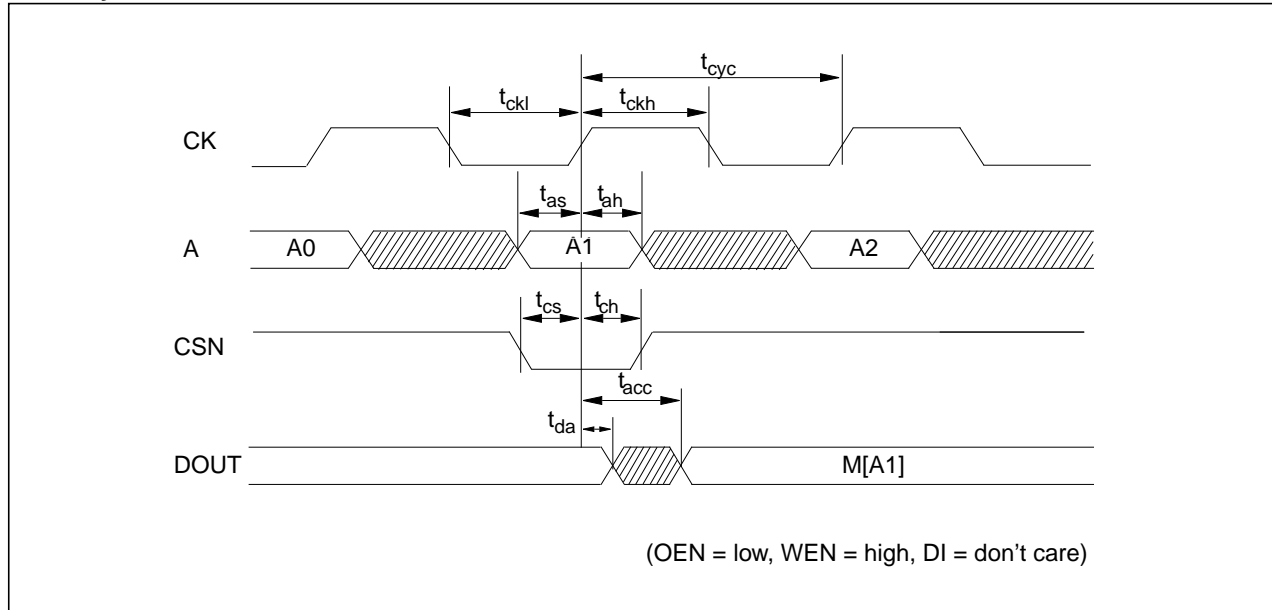
## Write Cycle



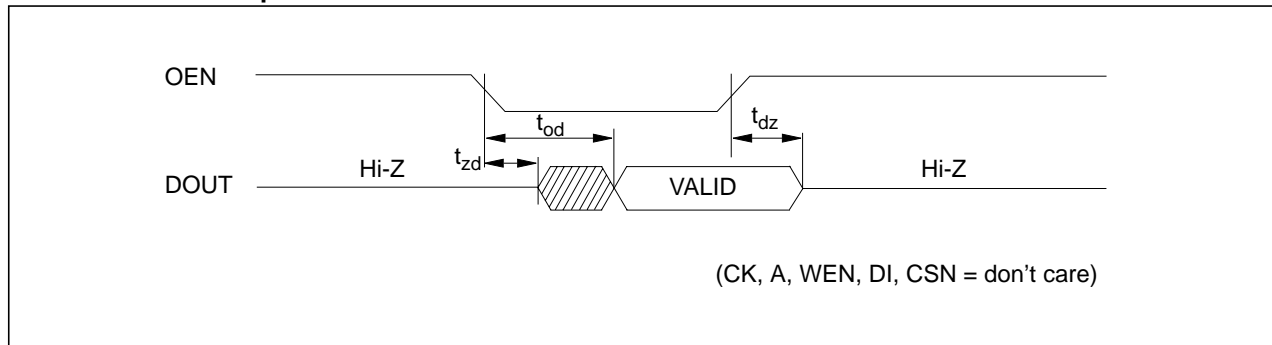


## High-Density Dual-Port Synchronous Static RAM

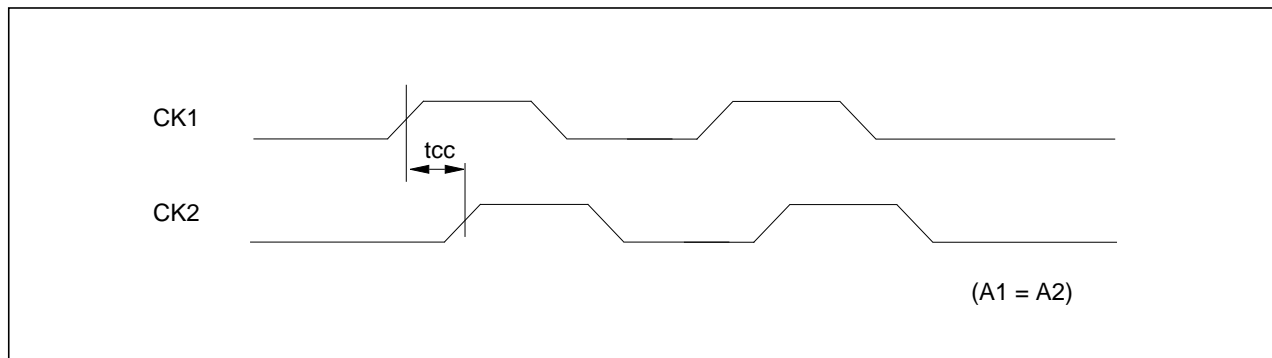
### Read Cycle with CSN Controlled



## OEN Controlled Output Enable



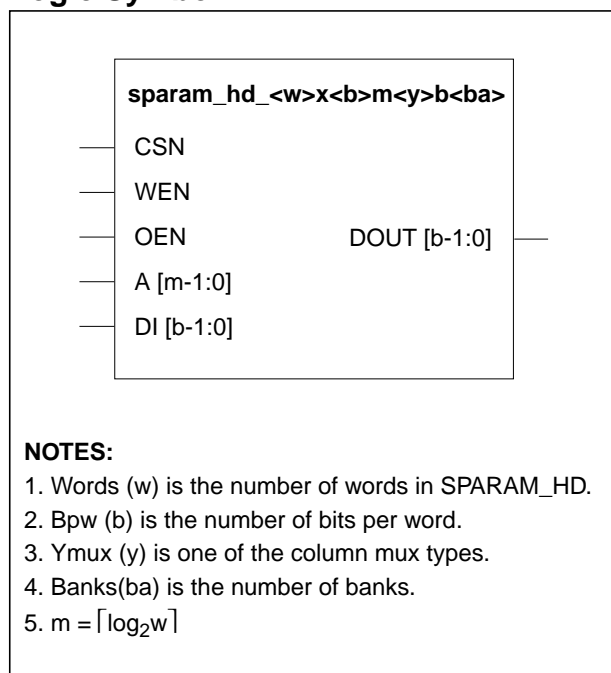
## Contention Mode



**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## Logic Symbol



## Features

- Suitable for high-density application
- Standby (power down) mode available
- Separated data I/O
- Asynchronous operation
- Asynchronous tri-state output
- Address transition detector
- Write-enable transition detector
- Chip-select transition detector
- Bank-select transition detector
- Automatic power-down
- Low noise output optimization
- Zero standby current
- Flexible aspect ratio
- Dual bank scheme available
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bit per word

## Function Description

SPARAM\_HD is a single-port asynchronous static RAM which is provided as a compiler. SPARAM\_HD is intended for use in high-density applications. At the falling edge of WEN, the write cycle is initiated. At the rising edge of WEN, the write cycle is ended. During the write cycle, the data on DI[] is written into the memory location specified on A[]. The read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay whenever A[] transition is detected. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

## SPARAM\_HD Function Table

CSN	WEN	OEN	A	DI	DOUT	Comment
X	X	H	X	X	Z	Unconditional tri-state output
H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
L	↓	L	Valid	Valid	DOUT(t-1)	Write cycle starts
L	↑	L	Valid	Valid	MEM(A)	Write cycle ends and Read Cycle starts
L	L	L	Stable	Valid	DOUT(t-1)	Write Cycle
L	H	L	Toggle	X	MEM(A)	Read Cycle



# SPARAM\_HD

## High-Density Single-Port Asynchronous Static RAM

### Parameter Description

SPARAM\_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y) and Number of banks(ba).

Parameters			YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words(w)	ba = 1	Min	16	32	64	128	256
		Max	512	1024	2048	4096	8192
		Step	8	16	32	64	128
	ba = 2	Min	32	64	128	256	512
		Max	1024	2048	4096	8192	16384
		Step	16	32	64	128	256
Bpw(b)		Min	1	1	1	1	
		Max	256	128	64	32	16
		Step	1	1	1	1	1

### Pin Descriptions

Name	I/O	Description
CSN	Chip Enable	Chip Select Input. The chip select signal acts as the memory enable signal for selections of multiple blocks. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if low, a read or write access can occur. When CSN falls, an access is initiated.
WEN	Read/Write Enable	Write Enable Input. The write enable signal selects the type of memory access. The high state for a read access and the low state for a write access. Upon the rising edge of WEN, a write access completed and a read access initiated.
OEN	Data Output Enable	Output Enable Input. The output enable signal controls the output drivers from driven to tri-state condition unconditionally.
A [ ]	Address	Address input bus. A[] should be stable when WEN is low. The address selects the location to be accessed. When the address changes, the transition is detected and the internal clock pulse is generated.
DI [ ]	Data Input	Data Input bus. The data input is written to the accessed location when WEN is low.
DOUT [ ]	Data Output	Data Output bus. The data output is data stored in the accessed location during a read access. Data output driver has tri-state logic. When OEN is low, the driver drives a certain value. Otherwise, data output keeps Hi-Z state. During a write access, data on DOUT is predictable.

### Pin Capacitance

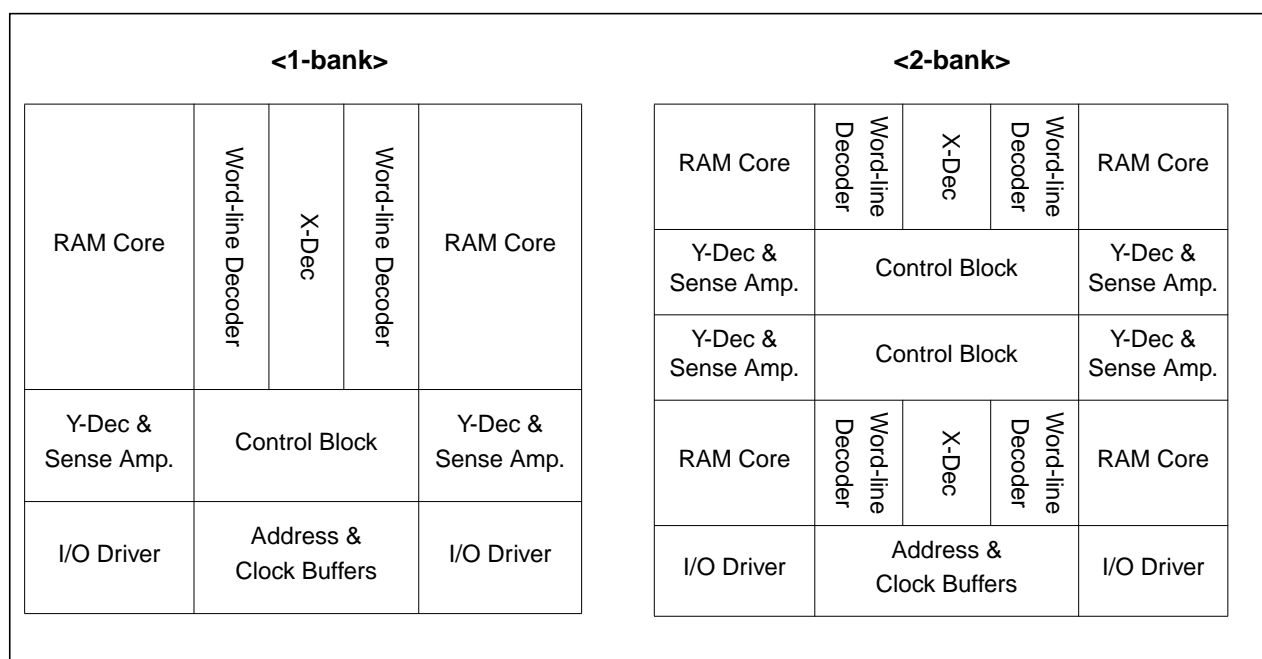
Unit: [SL]

	CSN	WEN	OEN	A	DI/DOUT				
					Ymux=2	Ymux=4	Ymux=8	Ymux=16	Ymux=32
ba = 1	1.87	1.87	1.87	3.91	1.87/7.12	1.87/7.12	1.87/7.12	1.87/7.12	1.87/7.12
ba = 2	1.87	1.87	1.87	3.91	1.87/7.12	1.87/7.12	1.87/7.12	1.87/7.12	1.87/7.12



## Block Diagrams

SPARAM\_HD has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPARAM\_HD compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode.



## Application Notes

1. Permitting Over-the-cell routing  
In chip-level layout, over-the-cell routing in SPARAM\_HD is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of SPARAM\_HD.
4. Avoiding short transition on the address bus  
In SPARAM\_HD, rather than the write operation which is synchronously performed by WEN signal, the read operation is asynchronously performed whenever the address transition is occurred. In this case, if the short transition on the address, called a skew, is happened, since SPARAM\_HD recognizes the short address transition as the stable address transition and do perform a read operation. At that time, while in the read operation, the data stored in the memory may be corrupted due to the short transition. To prevent such fail, the stable address cycle time (tcyc) is required. The essential requirement to recognize valid address transition is that at least minimum address period should be equal or greater than tacc (access time).
5. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## SPARAM\_HD

### High-Density Single-Port Asynchronous Static RAM

#### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Address cycle time	tas	Address setup time
tcas	Address setup time for CSN rise	tah	Address hold time
twh	WEN hold time	tcs	CSN setup time
tch	CSN hold time	tds	Data-In setup time
tdh	Data-In hold time	twen	WEN pulse width low
tacc	Data access time for read cycle	twacc	Data access time for WEN rise
tda	De-access time	twda	De-access time for WEN rise
tzd	DOUT high-Z to drive time	tdz	DOUT drive to high-Z time
tod	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## High-Density Single-Port Asynchronous Static RAM

## Reference Table

\* For Ymux=2

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	128	256	256	512	384	768	512	1024
bpw	64	64	128	128	192	192	256	256
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	3.54	3.62	3.80	3.92	4.06	4.21	4.32	4.51
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	3.76	3.85	4.02	4.14	4.28	4.44	4.54	4.73
t <sub>ah</sub>	0.49	0.51	0.72	0.75	1.01	1.04	1.36	1.39
t <sub>wh</sub>	3.76	3.85	4.02	4.14	4.28	4.44	4.54	4.73
t <sub>ds</sub>	0.14	0.16	0.14	0.17	0.14	0.16	0.14	0.15
t <sub>dh</sub>	0.76	0.75	0.84	0.84	0.94	0.93	1.04	1.03
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.61	1.72	1.70	1.84	1.79	1.97	1.89	2.11
t <sub>wen</sub>	2.43	2.47	2.66	2.70	2.88	2.93	3.10	3.17
t <sub>acc</sub>	3.54	3.62	3.80	3.92	4.06	4.21	4.32	4.51
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.39	1.49	1.47	1.62	1.57	1.74	1.67	1.88
t <sub>dz</sub>	0.51	0.51	0.55	0.55	0.58	0.58	0.61	0.61
t <sub>zd</sub>	0.33	0.33	0.36	0.36	0.40	0.40	0.43	0.43
t <sub>od</sub>	0.55	0.55	0.58	0.58	0.62	0.62	0.65	0.66
Power (μW/MHz)								
Power_read	296.01	315.80	565.87	618.94	850.87	951.64	1151.00	1313.90
Power_write	397.43	427.42	890.37	972.44	1513.74	1670.46	2267.53	2521.46
Power_standby	31.21	75.63	56.71	147.15	82.31	227.53	107.99	316.78
Area (μm)								
Width	1207.22	1207.22	2157.05	2157.05	3106.87	3106.87	4056.69	4056.69
Height	342.44	646.60	471.08	903.88	599.72	1161.16	728.36	1418.44

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



# SPARAM\_HD

## High-Density Single-Port Asynchronous Static RAM

### Reference Table

\* For Ymux=4 (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	256	512	512	1024	768	1536	1024	2048
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	3.51	3.59	3.74	3.86	3.97	4.13	4.20	4.40
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	3.74	3.82	3.97	4.09	4.20	4.35	4.43	4.62
t <sub>ah</sub>	0.52	0.54	0.75	0.78	1.04	1.07	1.39	1.43
t <sub>wh</sub>	3.74	3.82	3.97	4.09	4.20	4.35	4.43	4.62
t <sub>ds</sub>	0.15	0.16	0.15	0.16	0.15	0.16	0.15	0.14
t <sub>dh</sub>	0.74	0.73	0.80	0.78	0.86	0.84	0.91	0.91
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.59	1.69	1.65	1.79	1.71	1.88	1.77	1.98
t <sub>wen</sub>	2.45	2.49	2.67	2.72	2.90	2.95	3.12	3.18
t <sub>acc</sub>	3.51	3.59	3.74	3.86	3.97	4.13	4.20	4.40
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.36	1.47	1.42	1.56	1.48	1.66	1.54	1.75
t <sub>dz</sub>	0.51	0.51	0.55	0.55	0.58	0.58	0.61	0.61
t <sub>zd</sub>	0.33	0.33	0.36	0.36	0.40	0.40	0.43	0.43
t <sub>od</sub>	0.55	0.55	0.59	0.58	0.62	0.62	0.66	0.65
Power (μW/MHz)								
Power_read	237.40	247.96	447.05	474.50	669.40	721.00	904.45	987.49
Power_write	294.56	309.83	627.93	669.30	1030.91	1109.77	1503.48	1631.23
Power_standby	20.26	48.08	34.13	86.35	48.14	129.20	62.27	176.64
Area (μm)								
Width	1207.22	1207.22	2157.05	2157.05	3106.87	3106.87	4056.69	4056.69
Height	342.44	646.60	471.08	903.88	599.72	1161.16	728.36	1418.44

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## High-Density Single-Port Asynchronous Static RAM

## Reference Table

\* For Ymux=8

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	3.53	3.62	3.76	3.89	3.99	4.16	4.23	4.43
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	3.75	3.85	3.99	4.12	4.22	4.38	4.45	4.65
t <sub>ah</sub>	0.52	0.54	0.75	0.78	1.04	1.07	1.39	1.43
t <sub>wh</sub>	3.75	3.85	3.99	4.12	4.22	4.38	4.45	4.65
t <sub>ds</sub>	0.15	0.16	0.15	0.17	0.15	0.16	0.15	0.14
t <sub>dh</sub>	0.70	0.67	0.76	0.72	0.83	0.78	0.89	0.85
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.61	1.72	1.67	1.82	1.73	1.91	1.79	2.01
t <sub>wen</sub>	2.44	2.47	2.67	2.70	2.89	2.93	3.11	3.17
t <sub>acc</sub>	3.53	3.62	3.76	3.89	3.99	4.16	4.23	4.43
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.38	1.50	1.44	1.59	1.50	1.69	1.56	1.78
t <sub>dz</sub>	0.51	0.51	0.55	0.54	0.58	0.58	0.61	0.61
t <sub>zd</sub>	0.33	0.33	0.36	0.36	0.40	0.40	0.43	0.43
t <sub>od</sub>	0.55	0.55	0.58	0.58	0.62	0.62	0.65	0.65
Power (μW/MHz)								
Power_read	211.43	219.32	399.31	417.73	600.08	632.62	813.75	863.97
Power_write	232.50	247.38	483.89	512.41	773.59	824.42	1104.59	1183.43
Power_standby	17.12	41.09	27.84	69.75	38.67	100.88	49.61	134.50
Area (μm)								
Width	1207.22	1207.22	2157.05	2175.05	3106.87	3106.87	4056.69	4056.69
Height	342.44	646.60	471.08	903.88	599.72	1161.16	728.36	1418.44

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



# SPARAM\_HD

## High-Density Single-Port Asynchronous Static RAM

### Reference Table

\* For Ymux=16 (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	3.56	3.68	3.80	3.95	4.03	4.21	4.27	4.48
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	3.78	3.91	4.02	4.18	4.25	4.45	4.49	4.72
t <sub>ah</sub>	0.52	0.54	0.75	0.78	1.04	1.07	1.39	1.43
t <sub>wh</sub>	3.78	3.91	4.02	4.18	4.25	4.45	4.49	4.72
t <sub>ds</sub>	0.16	0.16	0.17	0.19	0.16	0.20	0.14	0.17
t <sub>dh</sub>	0.65	0.56	0.71	0.62	0.77	0.68	0.84	0.75
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.64	1.79	1.70	1.88	1.76	1.98	1.82	2.07
t <sub>wen</sub>	2.43	2.44	2.65	2.67	2.87	2.90	3.10	3.13
t <sub>acc</sub>	3.56	3.68	3.80	3.95	4.03	4.21	4.27	4.48
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.41	1.55	1.48	1.65	1.54	1.74	1.60	1.84
t <sub>dz</sub>	0.51	0.51	0.54	0.54	0.58	0.58	0.61	0.61
t <sub>zd</sub>	0.33	0.33	0.36	0.36	0.40	0.40	0.43	0.43
t <sub>od</sub>	0.55	0.55	0.58	0.58	0.62	0.62	0.65	0.65
Power (μW/MHz)								
Power_read	194.95	201.50	373.63	387.64	565.45	588.69	770.41	804.65
Power_write	203.19	215.26	410.81	434.92	645.75	684.69	908.00	964.57
Power_standby	15.82	39.97	25.12	64.23	34.53	89.89	44.06	116.95
Area (μm)								
Width	1207.22	1207.22	2157.05	2157.05	3106.87	3106.87	4056.69	4056.69
Height	342.44	646.60	471.08	903.88	599.72	1161.16	728.36	1418.44

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## High-Density Single-Port Asynchronous Static RAM

## Reference Table

\* For Ymux=32

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	4	4	8	8	12	12	16	16
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	3.61	3.77	3.85	4.05	4.09	4.32	4.33	4.60
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	3.84	4.03	4.08	4.31	4.32	4.58	4.56	4.86
t <sub>ah</sub>	0.52	0.54	0.75	0.78	1.04	1.08	1.39	1.43
t <sub>wh</sub>	3.84	4.03	4.08	4.31	4.32	4.58	4.56	4.86
t <sub>ds</sub>	0.15	0.23	0.18	0.31	0.19	0.36	0.16	0.39
t <sub>dh</sub>	0.54	0.36	0.60	0.42	0.66	0.47	0.72	0.52
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.70	1.92	1.76	2.01	1.82	2.11	1.88	2.20
t <sub>wen</sub>	2.40	2.38	2.62	2.61	2.84	2.83	3.06	3.06
t <sub>acc</sub>	3.61	3.77	3.85	4.05	4.09	4.32	4.33	4.60
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.47	1.66	1.53	1.75	1.59	1.85	1.66	1.94
t <sub>dz</sub>	0.51	0.51	0.54	0.54	0.58	0.58	0.61	0.61
t <sub>zd</sub>	0.33	0.33	0.36	0.36	0.40	0.40	0.43	0.43
t <sub>od</sub>	0.55	0.55	0.58	0.58	0.62	0.62	0.65	0.66
Power (μW/MHz)								
Power_read	179.77	185.70	356.81	368.61	547.31	565.88	751.28	777.49
Power_write	182.59	202.06	372.72	402.17	583.36	624.20	814.52	868.18
Power_standby	16.11	48.56	24.84	71.16	33.67	94.59	42.61	118.85
Area (μm)								
Width	1207.22	1207.22	2157.05	2157.05	3106.87	3106.87	4056.69	4056.69
Height	342.44	646.60	471.08	903.88	599.72	1161.16	728.36	1418.44

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

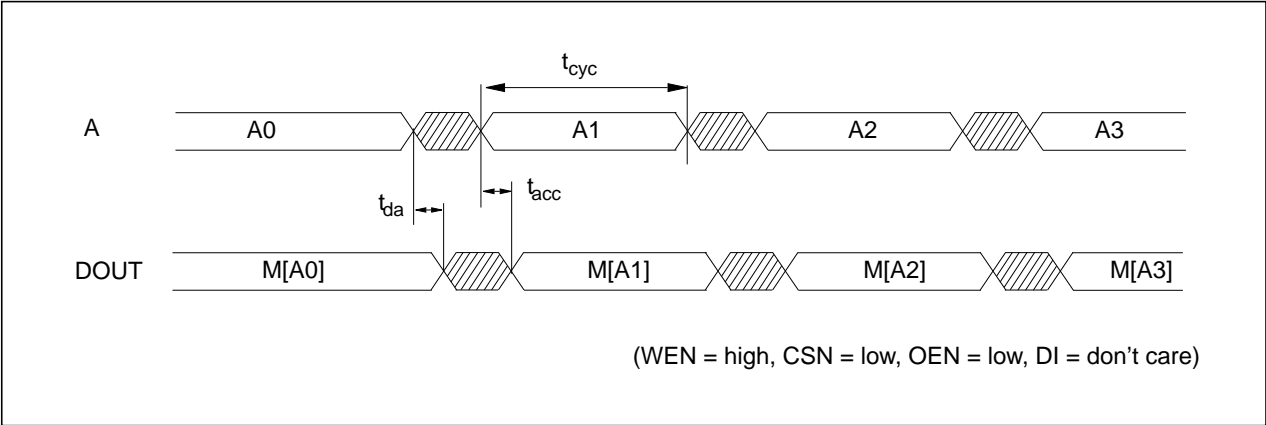


SPARAM\_HD

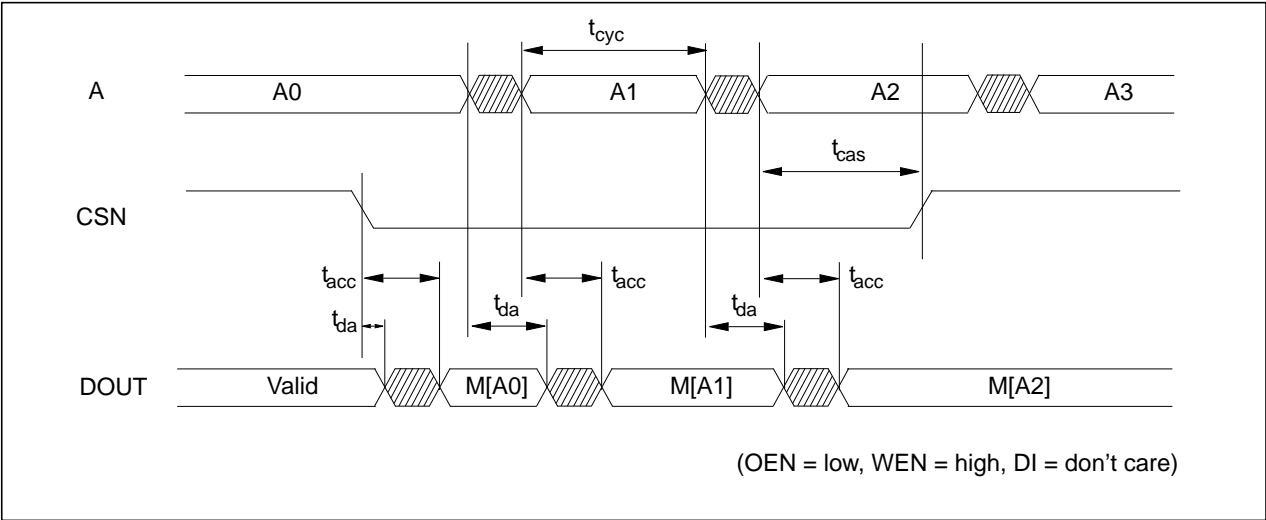
High-Density Single-Port Asynchronous Static RAM

Timing Diagrams

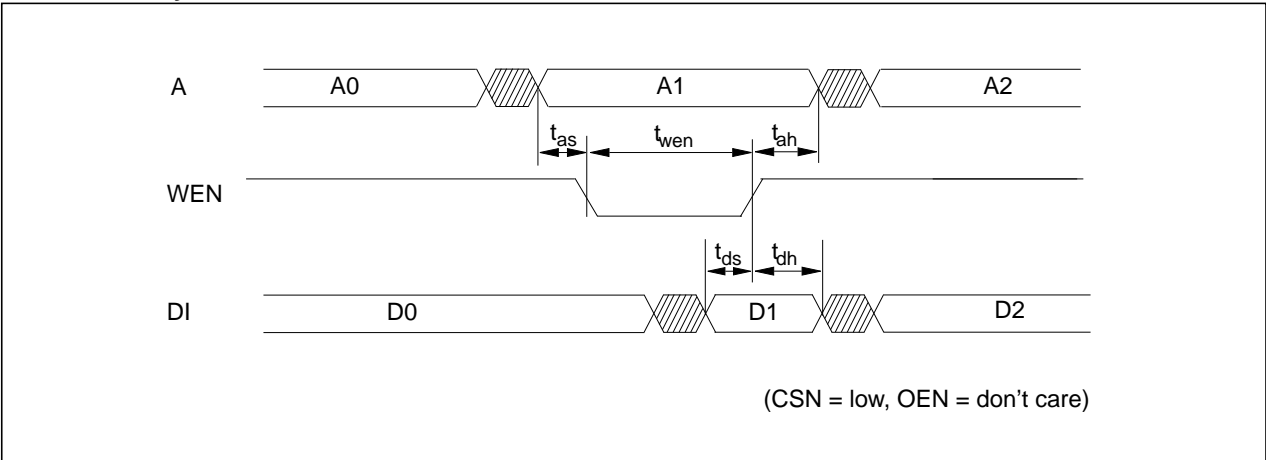
Read Cycle



Read Cycle with CSN-Controlled

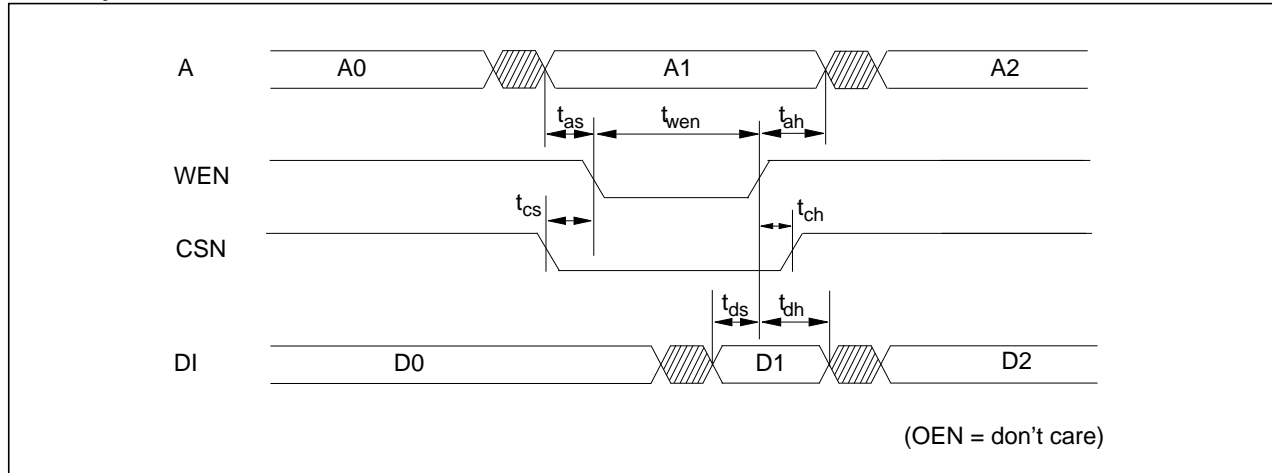


Basic Write Cycle

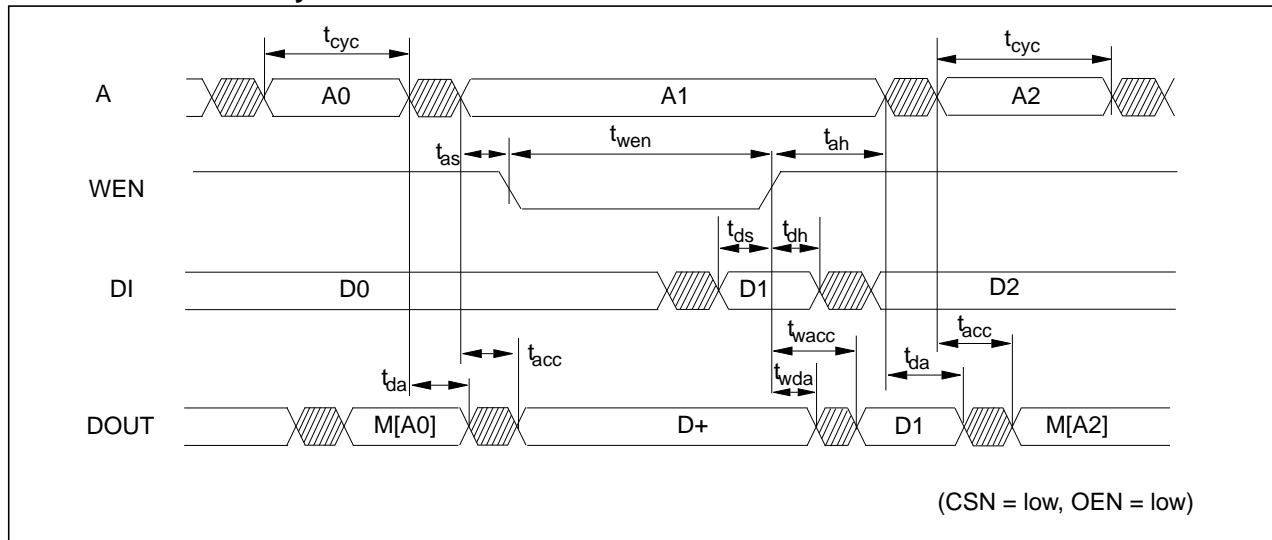




## Write Cycle with CSN Controlled



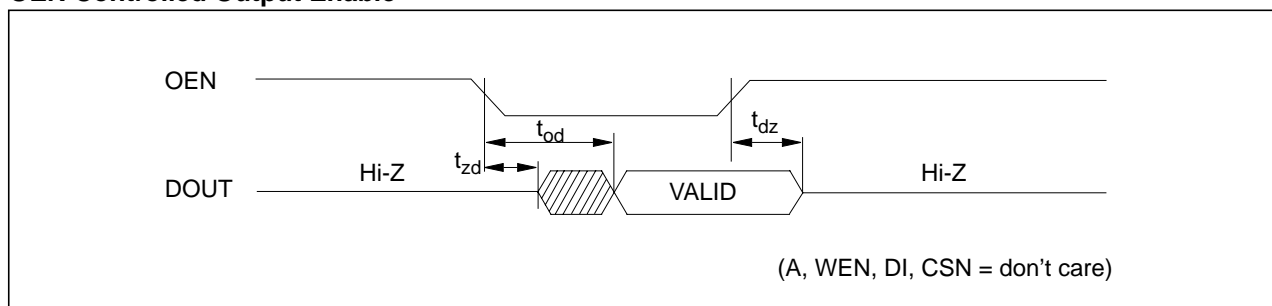
## Read-Modified-Write Cycle



## NOTES:

1. When the wen hold time after the last address bit transition is satisfied, D+ will toggle in response to a successful read of the initial contents of address A1. When the wen hold time after the last address bit transition is not satisfied, D+ will go to unknown state.
2. Address bits are not allowed to change while WEN is low. If they do change, then the data for one or more addresses in the memory array may be corrupted.

## OEN Controlled Output Enable



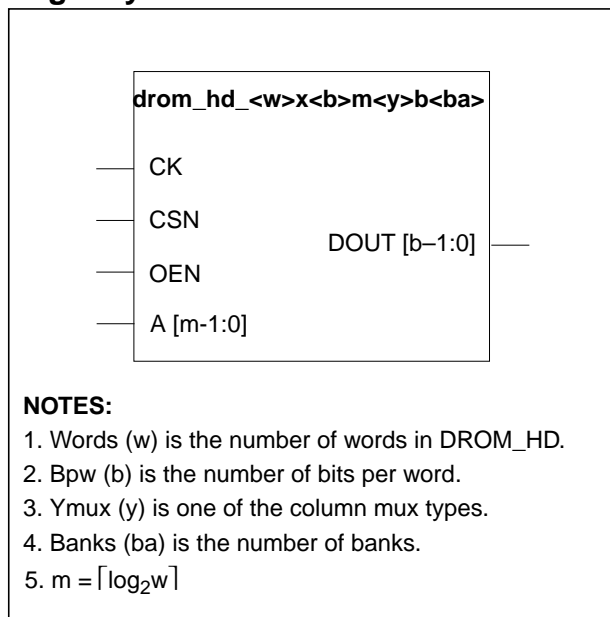
**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## DROM\_HD

### High-Density Synchronous Diffusion Programmable ROM

#### Logic Symbol



#### Features

- Suitable for high-density applications
- Diffusion-programmable code available
- Synchronous operation
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down
- Low noise output optimization
- Zero standby current
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

#### Function Description

DROM\_HD is a synchronous diffusion programmable ROM which is provided as a compiler. DROM\_HD is intended for use in high-density applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

#### DROM Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read Cycle

#### Parameter Description

DROM\_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y) and Number of banks(ba).



## High-Density Synchronous Diffusion Programmable ROM

Parameters			YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	ba = 1	Min	64	128	256
		Max	2048	4096	8192
		Step	32	64	128
	ba = 2	Min	128	256	512
		Max	4096	8192	16384
		Step	64	128	256
Bpw (b)		Min	2	2	2
		Max	128	64	32
		Step	1	1	1

## Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

## Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT		
					Ymux=8	Ymux=16	Ymux=32
ba = 1	8.74	6.626	3.724	7.248	9.408	9.408	9.408
ba = 2	5.336	4.904	3.736	4.880	9.436	9.436	9.436

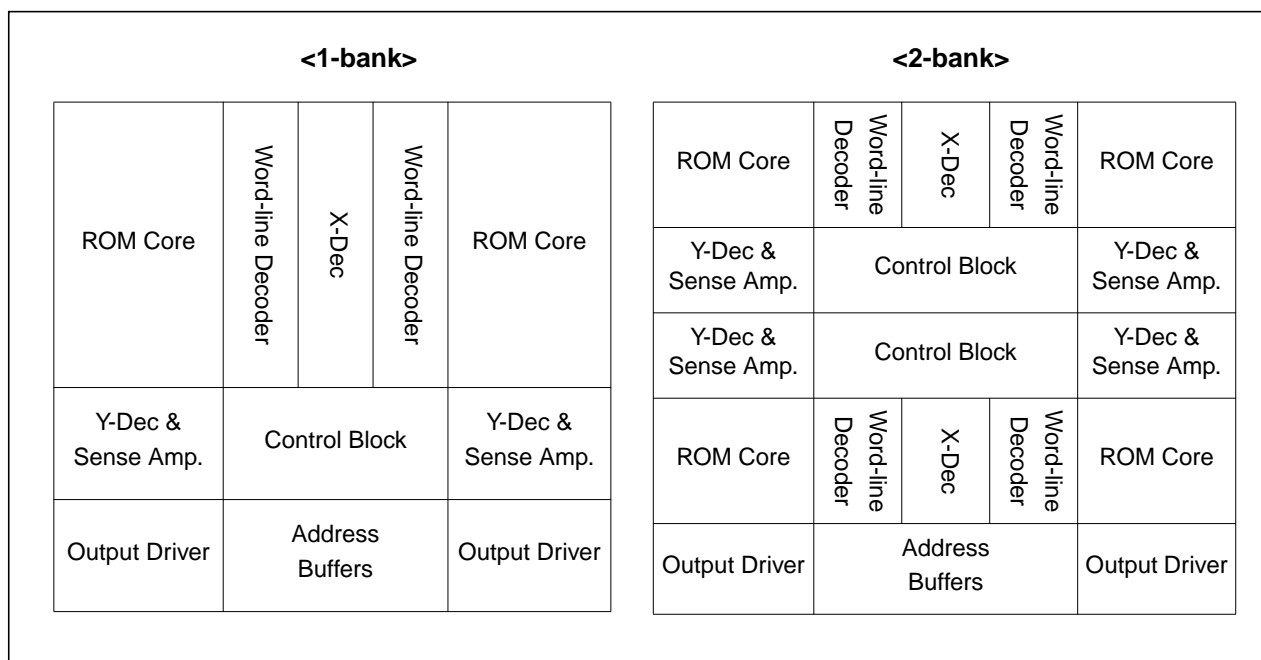


# DROM\_HD

## High-Density Synchronous Diffusion Programmable ROM

### Block Diagrams

DROM\_HD has 2 different physical architectures due to the word depth. For a specific configuration, only one of these architectures is generated from DROM\_HD compiler. Power is consumed by the bank that is selected by the address whereas the other bank will be in idle mode.



### Application Notes

1. Permitting over-the-cell routing  
In chip-level layout, over-the-cell routing in DROM\_HD is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of DROM\_HD.
4. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## Characteristics

Definition for AC Timing (ns)			
Symbol		Description	
tcyc		Clock cycle time	
tckl		Clock pulse width low	
tckh		Clock pulse width high	
tas		Address setup time	
tah		Address hold time	
tcs		CSN setup time	
Symbol		Description	
tch		CSN hold time from CK rise	
tacc		Data access time	
tda		De-access time	
tdz		DOUT drive to high-Z time	
tzd		DOUT high-Z to drive time	
tod		OEN to Valid Output	
Definition for Power Consumption (μW/MHz)			
Power_read		The dynamic average power consumption while in a read cycle	
Power_standby		The standby power consumption while CSN is high	
Definition for Area (μm)			
Width		The physical width in X-direction	
Height		The physical height in Y-direction	



## DROM\_HD

### High-Density Synchronous Diffusion Programmable ROM

#### Reference Table

\* For Ymux=8

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.05	4.29	4.46	4.72	4.86	5.15	5.26	5.58
t <sub>ckl</sub>	0.44	0.68	0.44	0.72	0.44	0.75	0.45	0.78
t <sub>ckh</sub>	1.12	1.35	1.12	1.38	1.12	1.41	1.12	1.44
t <sub>as</sub>	0.16	0.84	0.18	0.90	0.22	0.98	0.26	1.06
t <sub>ah</sub>	0.61	0.86	0.61	0.90	0.61	0.93	0.61	0.97
t <sub>cs</sub>	0.44	0.68	0.44	0.72	0.44	0.75	0.44	0.78
t <sub>ch</sub>	0.52	0.78	0.52	0.81	0.52	0.85	0.52	0.88
t <sub>acc</sub>	2.94	3.25	3.06	3.41	3.25	3.64	3.51	3.94
t <sub>da</sub>	2.49	2.74	2.71	2.99	2.93	3.25	3.16	3.51
t <sub>dz</sub>	0.75	0.75	0.89	0.88	1.03	1.03	1.19	1.19
t <sub>zd</sub>	0.87	0.87	1.00	1.00	1.13	1.13	1.28	1.27
t <sub>od</sub>	0.96	0.96	1.09	1.09	1.22	1.22	1.37	1.37
Power (μW/MHz)								
Power_read	284.25	287.74	601.59	605.65	1003.35	1007.62	1489.53	1493.63
Power_standby	32.63	79.37	52.54	121.27	72.61	163.47	92.83	205.98
Area (μm)								
Width	611.11	611.11	983.51	983.51	1355.64	1355.64	1727.51	1727.51
Height	222.56	427.50	303.20	588.78	383.84	750.06	464.48	911.34

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## High-Density Synchronous Diffusion Programmable ROM

## Reference Table

\* For Ymux=16

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.05	4.29	4.46	4.72	4.86	5.15	5.26	5.58
t <sub>ckl</sub>	0.44	0.68	0.44	0.72	0.44	0.75	0.44	0.78
t <sub>ckh</sub>	1.12	1.35	1.12	1.38	1.12	1.41	1.12	1.44
t <sub>as</sub>	0.16	0.84	0.18	0.90	0.22	0.98	0.26	1.06
t <sub>ah</sub>	0.61	0.86	0.61	0.90	0.61	0.93	0.61	0.97
t <sub>cs</sub>	0.45	0.68	0.45	0.72	0.45	0.75	0.44	0.78
t <sub>ch</sub>	0.52	0.78	0.52	0.81	0.52	0.85	0.52	0.88
t <sub>acc</sub>	2.98	3.25	3.10	3.41	3.29	3.64	3.54	3.94
t <sub>da</sub>	2.50	2.75	2.72	3.01	2.94	3.26	3.17	3.52
t <sub>dz</sub>	0.72	0.71	0.80	0.80	0.88	0.88	0.96	0.96
t <sub>zd</sub>	0.84	0.84	0.92	0.91	0.99	0.99	1.07	1.07
t <sub>od</sub>	0.92	0.2	1.00	1.00	1.08	1.08	1.16	1.16
Power (μW/MHz)								
Power_read	283.62	286.97	601.73	605.51	1003.47	1007.47	1488.83	1492.86
Power_standby	32.61	79.35	52.51	121.20	72.57	163.36	92.79	205.83
Area (μm)								
Width	610.82	610.82	983.44	983.44	1355.64	1355.64	1727.44	1727.44
Height	222.56	427.50	303.20	588.78	383.84	750.06	464.48	911.34

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode



## DROM\_HD

### High-Density Synchronous Diffusion Programmable ROM

#### Reference Table

\* For Ymux=32

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

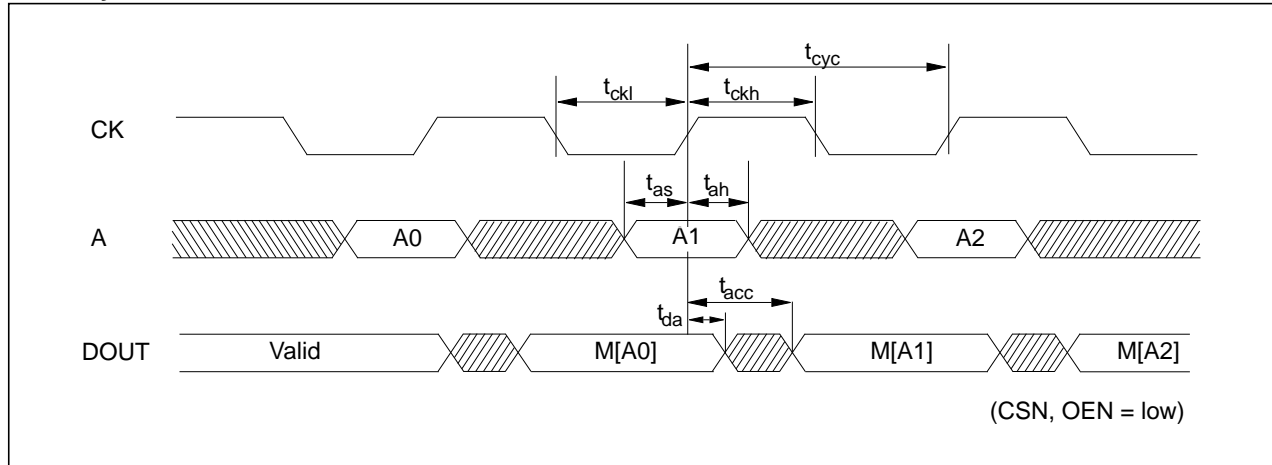
Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.05	4.29	4.46	4.72	4.86	5.15	5.26	5.58
t <sub>ckl</sub>	0.44	0.68	0.44	0.72	0.45	0.75	0.45	0.78
t <sub>ckh</sub>	1.12	1.35	1.12	1.38	1.12	1.41	1.12	1.44
t <sub>as</sub>	0.17	0.84	0.19	0.90	0.22	0.98	0.26	1.06
t <sub>ah</sub>	0.61	0.86	0.61	0.90	0.61	0.93	0.61	0.96
t <sub>cs</sub>	0.45	0.68	0.45	0.72	0.45	0.75	0.45	0.78
t <sub>ch</sub>	0.52	0.78	0.52	0.81	0.52	0.84	0.52	0.88
t <sub>acc</sub>	3.06	3.46	3.17	3.62	3.36	3.84	3.61	4.14
t <sub>da</sub>	2.51	2.77	2.74	3.03	2.96	3.29	3.19	3.54
t <sub>dz</sub>	0.70	0.69	0.75	0.75	0.81	0.81	0.87	0.87
t <sub>zd</sub>	0.82	0.82	0.87	0.87	0.93	0.93	0.99	0.99
t <sub>od</sub>	0.91	0.90	0.96	0.96	1.02	1.02	1.08	1.08
Power (μW/MHz)								
Power_read	281.73	284.99	601.01	604.96	1003.42	1007.94	1488.97	1493.94
Power_standby	32.61	79.35	52.49	121.20	72.54	163.40	92.77	205.95
Area (μm)								
Width	610.23	610.23	983.27	983.27	1355.64	1355.64	1727.34	1727.34
Height	222.56	427.50	303.20	588.78	383.84	750.06	464.48	911.34

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode

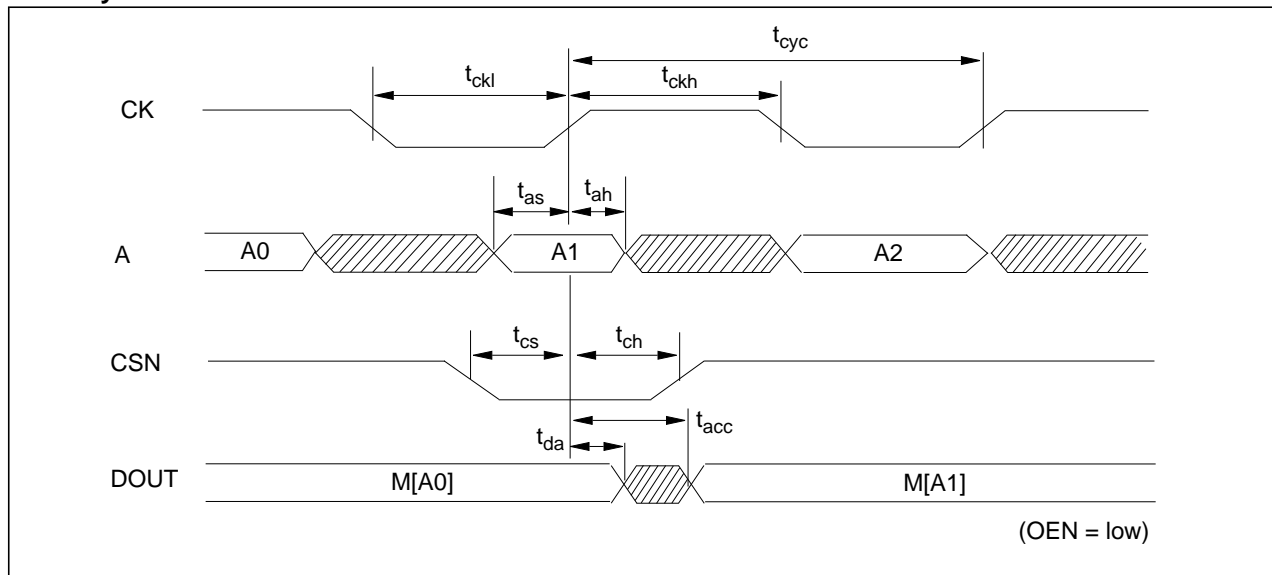


## Timing Diagrams

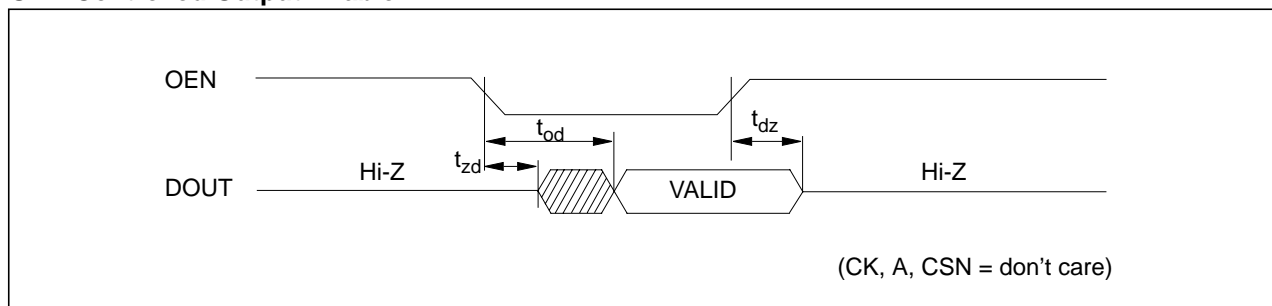
## Read Cycle



## Read Cycle with CSN Controlled



## OEN Controlled Output Enable



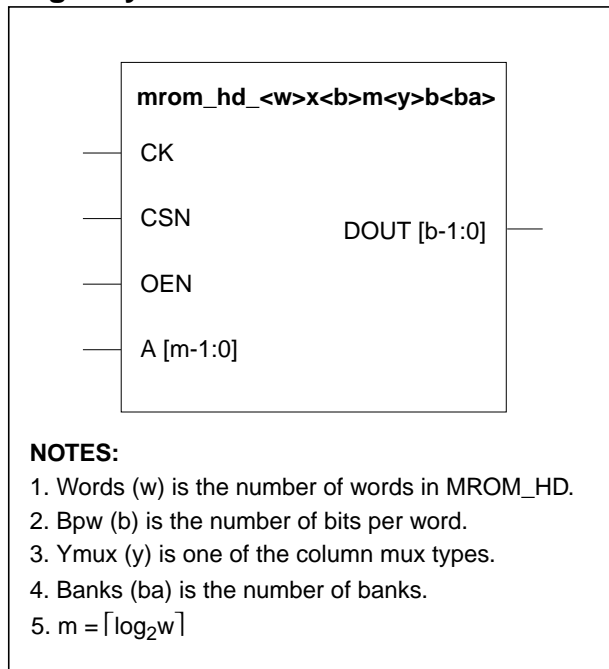
**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## MROM\_HD

### High-Density Synchronous Metal Programmable ROM

#### Logic Symbol



#### Features

- Suitable for high-density applications
- Metal-2 programmable code available
- Synchronous operation
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Low noise output optimization
- Zero standby current
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

#### Function Description

MROM\_HD is a synchronous metal-2 programmable ROM which is provided as a compiler. MROM\_HD is intended for use in high-density applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

#### MROM Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read cycle



## Parameter Description

MROM\_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba).

Parameters			YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	ba = 1	Min	64	128	256
		Max	2048	4096	8192
		Step	32	64	128
	ba = 2	Min	128	256	512
		Max	4096	8192	16384
		Step	64	128	256
Bpw (b)		Min	2	2	2
		Max	128	64	32
		Step	1	1	1

## Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

## Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT		
					Ymux=8	Ymux=16	Ymux=32
ba = 1	13.386	4.88	4.20	5.74	8.86	8.86	8.86
ba = 2	14.436	5.16	3.84	5.44	8.86	8.86	8.86

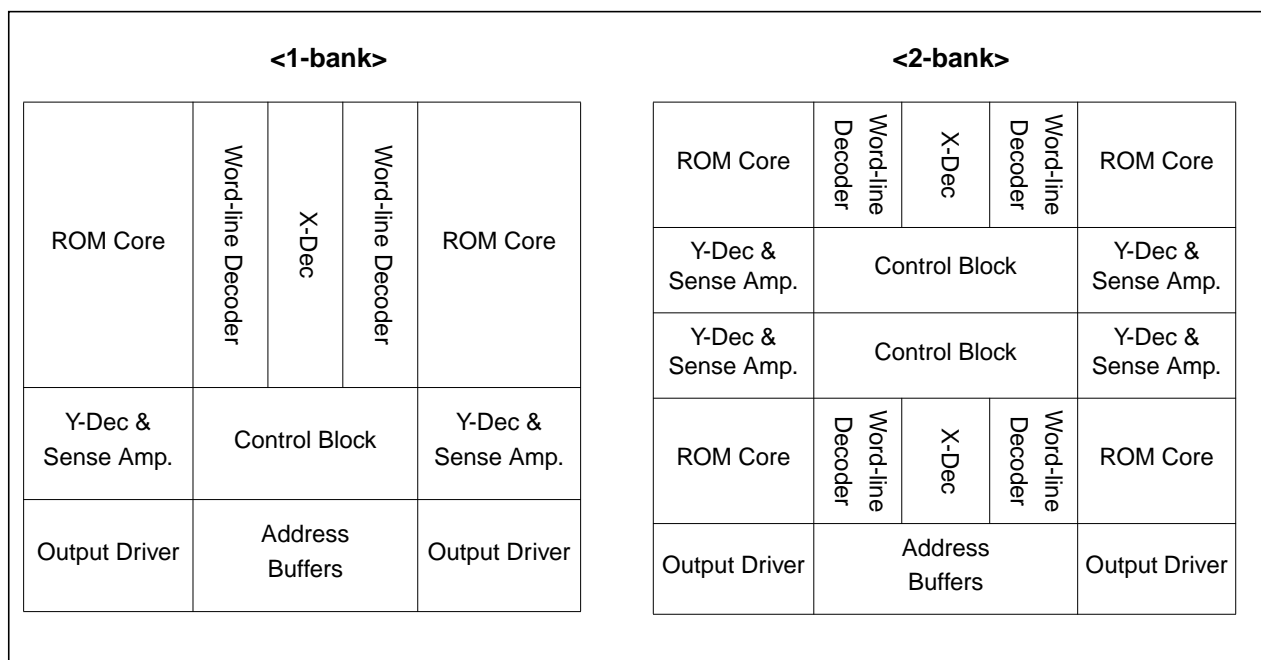


## MROM\_HD

### High-Density Synchronous Metal Programmable ROM

#### Block Diagrams

MROM\_HD has 2 different physical architectures due to the word depth. For a specific configuration, only one of these architectures is generated from MROM\_HD compiler. Power is consumed by the bank that is selected by the address whereas the other bank will be in idle mode.



#### Application Notes

1. Permitting over-the-cell routing  
In chip-level layout, over-the-cell routing in MROM\_HD is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of MROM\_HD.
4. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Clock cycle time	tch	CSN hold time from CK rise
tckl	Clock pulse width low	tacc	Data access time
tckh	Clock pulse width high	tda	De-access time
tas	Address setup time	tdz	DOUT drive to high-Z time
tah	Address hold time	tzd	DOUT high-Z to drive time
tcs	CSN setup time	tod	OEN to Valid Output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## MROM\_HD

### High-Density Synchronous Metal Programmable ROMReference Table

#### Reference Table

\* For Ymux=8

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.17	4.44	4.77	5.09	5.34	5.71	5.90	6.31
t <sub>ckl</sub>	0.60	0.85	0.60	0.91	0.60	0.97	0.60	1.03
t <sub>ckh</sub>	1.18	1.45	1.18	1.50	1.18	1.55	1.18	1.60
t <sub>as</sub>	0.10	0.97	0.13	1.02	0.24	1.17	0.44	1.40
t <sub>ah</sub>	0.69	1.00	0.69	1.07	0.69	1.13	0.69	1.19
t <sub>cs</sub>	0.60	0.85	0.60	0.91	0.60	0.97	0.60	1.03
t <sub>ch</sub>	0.61	0.92	0.61	0.99	0.61	1.05	0.61	1.11
t <sub>acc</sub>	2.95	3.25	3.29	3.65	3.68	4.10	4.12	4.60
t <sub>da</sub>	2.52	2.81	2.93	3.28	3.33	3.73	3.72	4.17
t <sub>dz</sub>	0.64	0.64	0.74	0.73	0.83	0.83	0.92	0.92
t <sub>zd</sub>	0.76	0.75	0.85	0.84	0.93	0.93	1.02	1.01
t <sub>od</sub>	0.83	0.83	0.95	0.92	1.01	1.01	1.09	1.09
Power (μW/MHz)								
Power_read	368.42	371.97	847.64	852.19	1498.81	1504.22	2321.92	2328.06
Power_standby	38.49	88.04	61.32	137.55	85.20	188.99	110.04	242.36
Area (μm)								
Width	567.93	567.93	997.77	997.77	1426.75	1426.75	1854.86	1854.86
Height	285.40	555.34	428.76	842.06	572.12	1128.78	715.48	1415.50

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## High-Density Synchronous Metal Programmable ROM Reference Table

## Reference Table

\* For Ymux=16

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.18	4.45	4.77	5.08	5.34	5.70	5.90	6.32
t <sub>ckl</sub>	0.60	0.85	0.60	0.91	0.60	0.97	0.60	1.03
t <sub>ckh</sub>	1.18	1.45	1.18	1.50	1.18	1.55	1.18	1.60
t <sub>as</sub>	0.10	0.97	0.13	1.03	0.24	1.17	0.44	1.40
t <sub>ah</sub>	0.69	1.00	0.69	1.07	0.69	1.13	0.69	1.19
t <sub>cs</sub>	0.60	0.85	0.60	0.91	0.60	0.97	0.60	1.03
t <sub>ch</sub>	0.61	0.92	0.61	0.99	0.61	1.05	0.61	1.11
t <sub>acc</sub>	2.95	3.32	3.29	3.72	3.68	4.17	4.12	4.67
t <sub>da</sub>	2.53	2.82	2.94	3.29	3.34	3.75	3.74	4.19
t <sub>dz</sub>	0.60	0.60	0.66	0.66	0.72	0.72	0.78	0.78
t <sub>zd</sub>	0.72	0.72	0.78	0.78	0.84	0.83	0.89	0.88
t <sub>od</sub>	0.80	0.79	0.85	0.85	0.91	0.91	0.96	0.96
Power (μW/MHz)								
Power_read	367.69	371.16	847.48	852.11	1498.70	1504.41	2321.34	2328.06
Power_standby	38.39	89.04	61.30	138.50	85.15	189.87	109.95	243.15
Area (μm)								
Width	567.62	567.62	997.69	997.69	1426.75	1426.75	1854.80	1854.80
Height	285.40	555.34	428.76	842.06	572.12	1128.78	715.48	1415.50

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode



## MROM\_HD

### High-Density Synchronous Metal Programmable ROM

#### Reference Table

\* For Ymux=32

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

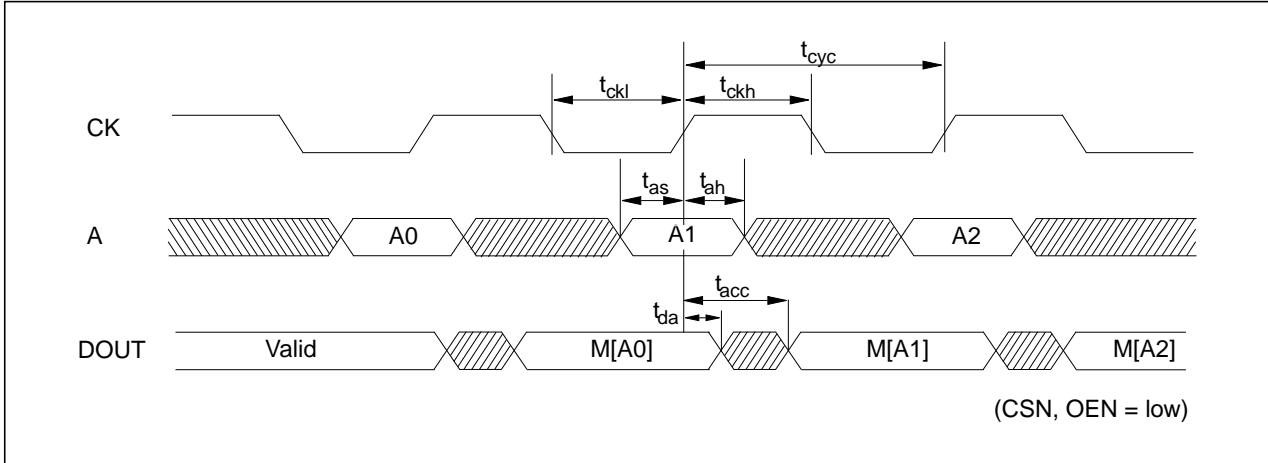
Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.18	4.44	4.77	5.08	5.34	5.70	5.90	6.30
t <sub>ckl</sub>	0.60	0.85	0.60	0.91	0.60	0.97	0.60	1.02
t <sub>ckh</sub>	1.18	1.45	1.18	1.50	1.18	1.55	1.18	1.60
t <sub>as</sub>	0.10	0.97	0.13	1.03	0.24	1.17	0.44	1.40
t <sub>ah</sub>	0.69	1.00	0.69	1.07	0.69	1.13	0.69	1.19
t <sub>cs</sub>	0.60	0.85	0.60	0.91	0.60	0.96	0.60	1.02
t <sub>ch</sub>	0.61	0.92	0.61	0.99	0.61	1.05	0.61	1.11
t <sub>acc</sub>	3.03	3.47	3.36	3.72	3.75	4.29	4.19	4.78
t <sub>da</sub>	2.55	2.85	2.96	3.29	3.36	3.76	3.76	4.19
t <sub>dz</sub>	0.59	0.58	0.63	0.66	0.67	0.67	0.71	0.71
t <sub>zd</sub>	0.70	0.70	0.74	0.78	0.78	0.78	0.82	0.82
t <sub>od</sub>	0.78	0.77	0.82	0.85	0.86	0.85	0.90	0.89
Power (μW/MHz)								
Power_read	365.71	369.21	846.96	852.11	1498.49	1504.40	2320.31	2327.77
Power_standby	38.41	89.10	61.30	138.50	85.13	189.88	109.89	243.14
Area (μm)								
Width	566.98	566.98	997.51	997.69	1426.75	1426.75	1854.71	1854.71
Height	285.40	555.34	428.76	842.06	572.12	1128.78	715.48	1415.50

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode

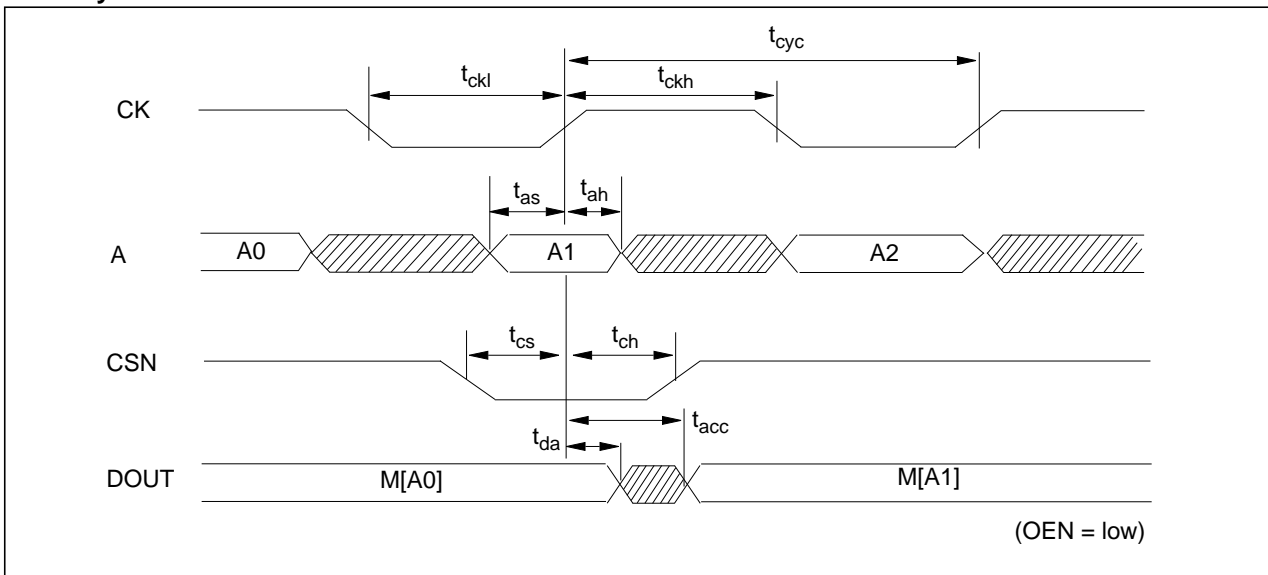


## Timing Diagrams

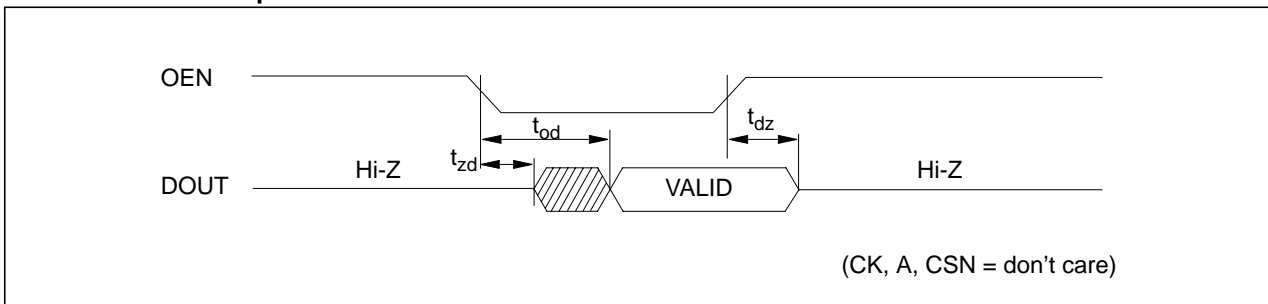
## Read Cycle



## Read Cycle with CSN Controlled



## OEN Controlled Output Enable



**NOTE:** "don't care" means the condition that these pins are in normal operation mode.

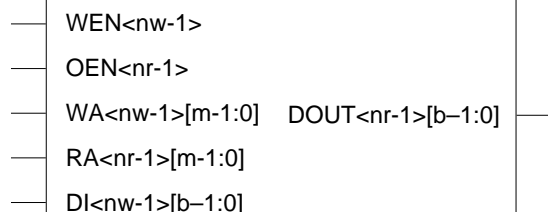


# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Logic Symbol

arfram\_hd\_<nr>r<nw>w\_<w>x<b>m<y>



#### NOTES:

1. Words (w) is the number of words in ARFRAM\_HD.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Writes (nw) is the number of write ports (1-to-2).
5. Reads (nr) is the number of read ports (1-to-2).
6.  $m = \lceil \log_2 w \rceil$

### Features

- Suitable for high-density applications
- Separated data I/O
- Fully independent ports
- Synchronous write operation
- Asynchronous read operation
- Latched inputs and outputs
- Asynchronous tri-state output control
- Configurable 1-to-2 read ports
- Configurable 1-to-2 write ports
- Flexible aspect ratio
- Up to 16Kbits capacity
- Up to 1024 number of words
- Up to 64 number of bits per word

### Function Description

ARFRAM\_HD is a multi-port asynchronous register file which is provided as a compiler. ARFRAM\_HD is intended for use in high-density applications. It allows maximum 4 ports with configurable 1-to-2 read ports and 1-to-2 write ports. All read and write ports are fully independent. At the falling edge of WEN, the write cycle is initiated. While WEN is low, the data at DI[] is written into the memory location specified on WA[]. At the rising edge of WEN, the write cycle ends. Regardless of WEN signal, the read cycle is always enabled. The data stored in the memory location specified on RA[] becomes valid through DOUT[] after a delay. When OEN is high, DOUT[] is placed in a high-impedance state.

### ARFRAM\_HD Write Function Table

WEN	WA	DI	Comment
H	X	X	Write disable mode
↓	Valid	X	Write cycle starts
↑	X	Valid	Write cycle ends

### ARFRAM\_HD Read Function Table

RA	OEN	DOUT	Comment
Valid	L	MEM (RA)	Read cycle
X	H	Z	Unconditional tri-state output



## Parameter Description

ARFRAM\_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y), Number of read ports(nr) and Number of write ports(nw).

Parameters		YMUX = 2	YMUX = 4	YMUX = 8
Words (w)	Min	4	8	16
	Max	256	512	1024
	Step	2	4	8
Bpw (b)	Min	1	1	1
	Max	64	32	16
	Step	1	1	1
Write ports (nw)		1, 2		
Read ports (nr)		1, 2		

## Pin Descriptions

Name	I/O	Description
WEN<nw-1>	Write Enable	Write Enable input on each write port. While it is high, it prevents a write-operation. The write-operation starts when it becomes low. At the rising edge of WEN, write-operation completed at the memory location.
WA<nw-1>[ ]	Write Address	Write Address bus on each write port. It specifies the location that the data will be written in the write-operation. WA[] is latched at the falling edge of WEN.
DI<nw-1>[ ]	Data Input	Data Input bus on each write port. It contains data values to be written into the memory during the write-cycle. DI[] is latched at the rising edge of WEN.
OEN<nr-1>	Data Output Enable	Output Enable input on each read port. The output enable signal controls the output drivers from driven to tri-state condition unconditionally.
RA<nr-1>[ ]	Read Address	Read Address bus on each read port. It specifies the location to be read in the read-operation.
DOUT<nr-1>[ ]	Data Output	Data Output bus on each read port. It presents the data word stored in the location specified by RA[] address bus. Data output is in the high-impedance state when OEN is high.

## Pin Capacitance

Unit: [SL]

WEN	OEN	WA	RA	DI/DOUT		
				Ymux=2	Ymux=4	Ymux=8
1	0.4	0.36	1.66	0.2/1.19	0.2/1.19	0.2/1.19

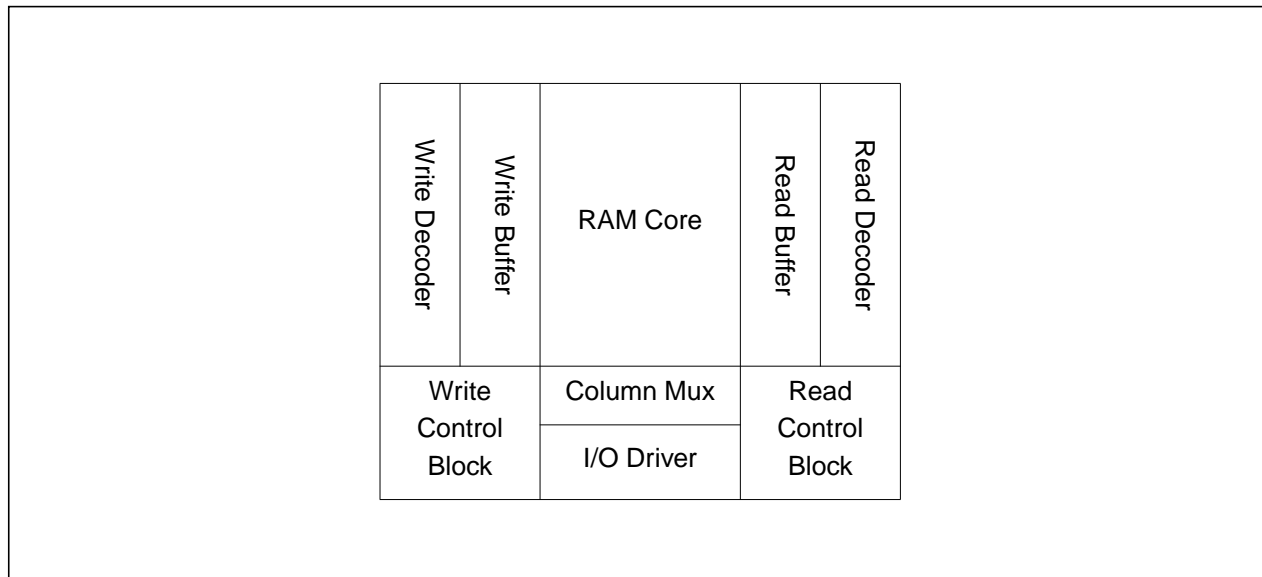


## ARFRAM\_HD

### High-Density Multi-port Asynchronous Register File

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#### Block Diagrams



#### Application Notes

1. Permitting Over-the-cell routing  
In ARFRAM\_HD, the over-the-cell routing is permitted. While doing layout on the chip-level, any signals to be routed can be crossed over the area of Register File generated by ARFRAM\_HD compiler.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of ARFRAM\_HD.
4. Contention mode under same addresses (RA[]=WA[]).  
In ARFRAM\_HD, simultaneous operations by both ports on the same address (RA[]=WA[]) as read/write, write/read, write/write operation, cause a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal. ARFRAM\_HD has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot complete and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports.



## Characteristics

Definition for AC Timing (ns)	
Symbol	Description
tcyc	Minimum address cycle time for read cycle
tas	Address Setup time from WA[] to WEN fall
tah	Address Hold time from WEN fall to WA[]
tds	Data-in Setup time from DI[] to WEN rise
tdh	Data-in Hold time from WEN rise to DI[]
twen	Minimum WEN pulse width low to guarantee write cycle
twenh	Minimum WEN pulse width high to guarantee write cycle
twwc	Write-Write contention time from one WA[] to the other WA[]
tda	De-Access time from RA to DOUT
tacc	Data Access time for read cycle
twda	De-access time from WEN fall to DOUT
twacc	Data Access time for WEN rise
tzd	DOUT high-Z to Drive time
tdz	DOUT Drive to high-Z time
tod	OEN to valid output time
Definition for Power Consumption ( $\mu$ W/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Definition for Area ( $\mu$ m)	
Width	The physical width in X-direction
Height	The physical height in Y-direction



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=2 (nr=1, nw=1) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	32	64	128	256
bpw	8	16	32	64
Timing (ns)				
t <sub>cyc</sub>	1.47	1.71	2.15	2.81
t <sub>as</sub>	0.45	0.57	0.79	1.20
t <sub>ah</sub>	0.58	0.65	0.79	1.08
t <sub>ds</sub>	0.50	0.49	0.47	0.43
t <sub>dh</sub>	0.12	0.13	0.15	0.19
t <sub>wen</sub>	1.15	1.25	1.45	1.85
t <sub>wenh</sub>	0.58	0.63	0.72	0.93
t <sub>acc</sub>	1.47	1.71	2.15	2.81
t <sub>da</sub>	0.30	0.30	0.30	0.30
t <sub>wacc</sub>	1.69	1.95	2.41	3.12
t <sub>wda</sub>	0.45	0.45	0.45	0.45
t <sub>dz</sub>	0.18	0.20	0.24	0.33
t <sub>zd</sub>	0.56	0.59	0.66	0.80
t <sub>od</sub>	1.36	1.39	1.45	1.59
Power (μW/MHz)				
Power_read	15.17	32.57	75.86	196.42
Power_write	53.36	121.72	316.18	936.13
Area (μm)				
Width	215.33	315.42	515.58	915.91
Height	228.40	342.57	570.91	1027.60



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=4 (nr=1, nw=1) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	64	128	256	512
bpw	4	8	16	32
Timing (ns)				
t <sub>cyc</sub>	1.53	1.77	2.20	2.91
t <sub>as</sub>	0.38	0.45	0.59	0.81
t <sub>ah</sub>	0.57	0.63	0.76	1.01
t <sub>ds</sub>	0.48	0.50	0.54	0.61
t <sub>dh</sub>	0.11	0.12	0.12	0.14
t <sub>wen</sub>	1.16	1.27	1.47	1.89
t <sub>wenh</sub>	0.58	0.63	0.74	0.95
t <sub>acc</sub>	1.53	1.77	2.20	2.91
t <sub>da</sub>	0.30	0.30	0.30	0.30
t <sub>wacc</sub>	1.75	1.98	2.42	3.14
t <sub>wda</sub>	0.45	0.45	0.45	0.45
t <sub>dz</sub>	0.18	0.20	0.25	0.34
t <sub>zd</sub>	0.56	0.60	0.67	0.82
t <sub>od</sub>	1.44	1.47	1.54	1.68
Power (μW/MHz)				
Power_read	15.38	33.05	76.42	195.34
Power_write	42.72	108.88	285.62	856.81
Area (μm)				
Width	216.53	316.54	516.57	916.61
Height	212.88	327.08	555.48	1012.30



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=8 (nr=1, nw=1) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	128	256	512	1024
bpw	2	4	8	16
Timing (ns)				
t <sub>cyc</sub>	1.70	1.95	2.40	3.07
t <sub>as</sub>	0.36	0.40	0.49	0.61
t <sub>ah</sub>	0.57	0.63	0.74	0.98
t <sub>ds</sub>	0.56	0.61	0.71	0.91
t <sub>dh</sub>	0.11	0.11	0.12	0.13
t <sub>wen</sub>	1.26	1.38	1.62	2.12
t <sub>wenh</sub>	0.63	0.69	0.81	1.06
t <sub>acc</sub>	1.70	1.95	2.40	3.07
t <sub>da</sub>	0.30	0.30	0.30	0.30
t <sub>wacc</sub>	1.90	2.15	2.60	3.26
t <sub>wda</sub>	0.45	0.45	0.45	0.45
t <sub>dz</sub>	0.18	0.20	0.25	0.34
t <sub>zd</sub>	0.56	0.59	0.66	0.81
t <sub>od</sub>	1.60	1.63	1.70	1.83
Power (μW/MHz)				
Power_read	16.36	34.81	78.97	196.35
Power_write	46.03	103.92	273.24	826.00
Area (μm)				
Width	216.94	316.62	515.99	914.72
Height	212.06	326.29	554.75	1011.67



## Reference Table

\* For Ymux=2 (nr=1, nw=2)

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	32	64	128	256
bpw	8	16	32	64
Timing (ns)				
t <sub>cyc</sub>	1.56	1.81	2.23	2.78
t <sub>as</sub>	0.99	1.14	1.43	2.02
t <sub>ah</sub>	0.58	0.65	0.80	1.10
t <sub>ds</sub>	0.51	0.49	0.47	0.40
t <sub>dh</sub>	0.14	0.15	0.18	0.24
t <sub>wen</sub>	1.19	1.30	1.52	1.97
t <sub>wenh</sub>	0.60	0.65	0.76	0.99
t <sub>acc</sub>	1.56	1.81	2.23	2.78
t <sub>da</sub>	0.32	0.32	0.32	0.32
t <sub>wacc</sub>	1.83	2.11	2.61	3.32
t <sub>wda</sub>	0.46	0.46	0.46	0.46
t <sub>dz</sub>	0.20	0.25	0.35	0.56
t <sub>zd</sub>	0.60	0.67	0.83	1.15
t <sub>od</sub>	1.22	1.28	1.40	1.69
t <sub>wwc</sub>	1.19	1.30	1.52	1.97
Power (μW/MHz)				
Power_read	20.58	43.05	96.84	239.84
Power_write	57.96	132.63	348.16	1.43.89
Area (μm)				
Width	271.86	395.38	642.41	1136.49
Height	276.38	399.91	646.98	1141.12



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=4 (nr=1, nw=2) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	64	128	256	512
bpw	4	8	16	32
Timing (ns)				
t <sub>cyc</sub>	1.77	1.99	2.39	3.04
t <sub>as</sub>	0.42	0.51	0.69	1.01
t <sub>ah</sub>	0.57	0.64	0.77	1.05
t <sub>ds</sub>	0.50	0.51	0.53	0.58
t <sub>dh</sub>	0.12	0.13	0.14	0.17
t <sub>wen</sub>	1.20	1.32	1.54	2.00
t <sub>wenh</sub>	0.60	0.66	0.77	1.00
t <sub>acc</sub>	1.77	1.99	2.39	3.04
t <sub>da</sub>	0.32	0.32	0.32	0.32
t <sub>wacc</sub>	2.03	2.28	2.75	3.49
t <sub>wda</sub>	0.47	0.47	0.47	0.47
t <sub>dz</sub>	0.18	0.22	0.28	0.42
t <sub>zd</sub>	0.57	0.62	0.72	0.93
t <sub>od</sub>	1.31	1.35	1.43	1.58
t <sub>wwc</sub>	1.20	1.32	1.54	2.00
Power (μW/MHz)				
Power_read	19.18	40.01	89.66	220.93
Power_write	51.85	119.44	317.63	966.11
Area (μm)				
Width	273.54	396.96	643.80	1137.47
Height	276.70	400.23	647.43	1141.73



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=8 (nr=1, nw=2) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	128	256	512	1024
bpw	2	4	8	16
Timing (ns)				
t <sub>cyc</sub>	1.78	2.03	2.46	3.02
t <sub>as</sub>	0.41	0.47	0.58	0.76
t <sub>ah</sub>	0.57	0.63	0.75	1.01
t <sub>ds</sub>	0.75	0.81	0.91	1.10
t <sub>dh</sub>	0.12	0.12	0.12	0.13
t <sub>wen</sub>	1.52	1.65	1.91	2.45
t <sub>wenh</sub>	0.76	0.82	0.95	1.23
t <sub>acc</sub>	1.78	2.03	2.46	3.02
t <sub>da</sub>	0.32	0.32	0.32	0.32
t <sub>wacc</sub>	2.03	2.30	2.78	3.42
t <sub>wda</sub>	0.47	0.47	0.47	0.47
t <sub>dz</sub>	0.18	0.20	0.25	0.34
t <sub>zd</sub>	0.56	0.59	0.67	0.83
t <sub>od</sub>	1.41	1.44	1.49	1.60
t <sub>wwc</sub>	1.52	1.65	1.91	2.45
Power (μW/MHz)				
Power_read	19.29	39.70	88.26	216.35
Power_write	52.86	119.27	315.12	959.01
Area (μm)				
Width	274.12	397.07	642.99	1134.81
Height	275.60	399.21	646.44	1140.89



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=2 (nr=2, nw=1) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	32	64	128	256
bpw	8	16	32	64
Timing (ns)				
t <sub>cyc</sub>	1.60	1.88	2.35	2.87
t <sub>as</sub>	0.78	0.92	1.20	1.76
t <sub>ah</sub>	0.57	0.64	0.77	1.05
t <sub>ds</sub>	0.50	0.49	0.46	0.44
t <sub>dh</sub>	0.12	0.13	0.15	0.19
t <sub>wen</sub>	1.17	1.27	1.47	1.90
t <sub>wenh</sub>	0.58	0.63	0.74	0.95
t <sub>acc</sub>	1.60	1.88	2.35	2.87
t <sub>da</sub>	0.32	0.32	0.32	0.32
t <sub>wacc</sub>	1.84	2.16	2.69	3.35
t <sub>wda</sub>	0.45	0.45	0.45	0.46
t <sub>dz</sub>	0.19	0.21	0.26	0.36
t <sub>zd</sub>	0.49	0.53	0.61	0.78
t <sub>od</sub>	1.18	1.21	1.28	1.41
Power (μW/MHz)				
Power_read	18.94	40.44	92.85	235.25
Power_write	56.79	130.16	341.79	1024.63
Area (μm)				
Width	289.55	417.32	672.85	1183.92
Height	255.39	380.63	631.11	1132.06



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=4 (nr=2, nw=1) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	64	128	256	512
bpw	4	8	16	32
Timing (ns)				
t <sub>cyc</sub>	1.87	2.12	2.57	3.20
t <sub>as</sub>	0.42	0.52	0.69	1.02
t <sub>ah</sub>	0.57	0.62	0.74	1.00
t <sub>ds</sub>	0.50	0.52	0.56	0.64
t <sub>dh</sub>	0.11	0.12	0.12	0.14
t <sub>wen</sub>	1.19	1.30	1.52	1.98
t <sub>wenh</sub>	0.59	0.65	0.76	0.99
t <sub>acc</sub>	1.87	2.12	2.57	3.20
t <sub>da</sub>	0.32	0.32	0.32	0.32
t <sub>wacc</sub>	2.11	2.38	2.88	3.62
t <sub>wda</sub>	0.47	0.47	0.47	0.47
t <sub>dz</sub>	0.18	0.21	0.26	0.35
t <sub>zd</sub>	0.49	0.53	0.61	0.76
t <sub>od</sub>	1.29	1.32	1.38	1.49
Power (μW/MHz)				
Power_read	17.80	37.84	86.62	218.91
Power_write	51.35	117.91	313.81	956.66
Area (μm)				
Width	291.46	419.11	674.42	1185.03
Height	255.79	381.09	631.67	1132.84



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=8 (nr=2, nw=1) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	128	256	512	1024
bpw	2	4	8	16
Timing (ns)				
t <sub>cyc</sub>	1.96	2.25	2.72	3.24
t <sub>as</sub>	0.36	0.42	0.53	0.70
t <sub>ah</sub>	0.57	0.62	0.74	0.97
t <sub>ds</sub>	0.76	0.82	0.94	1.18
t <sub>dh</sub>	0.11	0.11	0.12	0.13
t <sub>wen</sub>	1.47	1.60	1.87	2.44
t <sub>wenh</sub>	0.74	0.80	0.94	1.22
t <sub>acc</sub>	1.96	2.25	2.72	3.24
t <sub>da</sub>	0.32	0.32	0.32	0.32
t <sub>wacc</sub>	2.19	2.50	3.01	3.62
t <sub>wda</sub>	0.47	0.47	0.47	0.47
t <sub>dz</sub>	0.18	0.21	0.25	0.35
t <sub>zd</sub>	0.49	0.53	0.60	0.76
t <sub>od</sub>	1.53	1.56	1.61	1.72
Power (μW/MHz)				
Power_read	18.49	39.36	89.50	223.34
Power_write	51.94	117.44	309.85	940.41
Area (μm)				
Width	292.10	419.23	673.50	1182.02
Height	254.40	379.74	630.42	1131.77



## Reference Table

\* For Ymux=2 (nr=2, nw=2)

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	32	64	128	256
bpw	8	16	32	64
Timing (ns)				
t <sub>cyc</sub>	1.57	1.82	2.24	2.77
t <sub>as</sub>	0.63	0.79	1.10	1.71
t <sub>ah</sub>	0.58	0.65	0.80	1.12
t <sub>ds</sub>	0.45	0.44	0.42	0.34
t <sub>dh</sub>	0.09	0.09	0.11	0.23
t <sub>wen</sub>	1.18	1.29	1.51	1.96
t <sub>wenh</sub>	0.59	0.65	0.76	0.98
t <sub>acc</sub>	1.57	1.82	2.24	2.77
t <sub>da</sub>	0.31	0.31	0.31	0.31
t <sub>wacc</sub>	1.83	2.12	2.61	3.29
t <sub>wda</sub>	0.45	0.45	0.45	0.45
t <sub>dz</sub>	0.20	0.24	0.34	0.55
t <sub>zd</sub>	0.59	0.67	0.82	1.14
t <sub>od</sub>	1.22	1.27	1.39	1.68
t <sub>wwc</sub>	1.18	1.29	1.51	1.96
Power (μW/MHz)				
Power_read	20.09	43.55	100.05	251.39
Power_write	58.58	137.61	371.51	1142.60
Area (μm)				
Width	354.11	513.31	831.72	1468.54
Height	263.96	387.98	636.02	1132.10



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=4 (nr=2, nw=2) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	64	128	256	512
bpw	4	8	16	32
Timing (ns)				
t <sub>cyc</sub>	1.92	2.15	2.55	3.18
t <sub>as</sub>	0.39	0.48	0.66	1.00
t <sub>ah</sub>	0.57	0.64	0.77	1.05
t <sub>ds</sub>	0.49	0.50	0.52	0.57
t <sub>dh</sub>	0.10	0.10	0.10	0.14
t <sub>wen</sub>	1.20	1.31	1.53	1.98
t <sub>wenh</sub>	0.60	0.65	0.77	0.99
t <sub>acc</sub>	1.92	2.15	2.55	3.18
t <sub>da</sub>	0.31	0.31	0.31	0.31
t <sub>wacc</sub>	2.12	2.37	2.83	3.55
t <sub>wda</sub>	0.47	0.47	0.47	0.47
t <sub>dz</sub>	0.18	0.21	0.27	0.41
t <sub>zd</sub>	0.57	0.62	0.72	0.93
t <sub>od</sub>	1.31	1.35	1.43	1.58
t <sub>wwc</sub>	1.20	1.31	1.53	1.98
Power (μW/MHz)				
Power_read	19.28	41.23	93.76	233.36
Power_write	52.93	124.67	341.57	1069.11
Area (μm)				
Width	356.51	515.57	833.69	1469.94
Height	264.31	388.38	636.51	1132.77



# ARFRAM\_HD

## High-Density Multi-port Asynchronous Register File

### Reference Table

\* For Ymux=8 (nr=2, nw=2) (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters				
words	128	256	512	1024
bpw	2	4	8	16
Timing (ns)				
t <sub>cyc</sub>	1.78	2.03	2.46	3.02
t <sub>as</sub>	0.36	0.41	0.52	0.74
t <sub>ah</sub>	0.57	0.63	0.75	1.01
t <sub>ds</sub>	0.75	0.81	0.92	1.12
t <sub>dh</sub>	0.10	0.10	0.10	0.10
t <sub>wen</sub>	1.52	1.63	1.87	2.42
t <sub>wenh</sub>	0.76	0.82	0.94	1.21
t <sub>acc</sub>	1.78	2.03	2.46	3.02
t <sub>da</sub>	0.31	0.31	0.31	0.31
t <sub>wacc</sub>	2.03	2.30	2.77	3.40
t <sub>wda</sub>	0.47	0.47	0.47	0.47
t <sub>dz</sub>	0.17	0.20	0.24	0.34
t <sub>zd</sub>	0.55	0.59	0.66	0.82
t <sub>od</sub>	1.41	1.43	1.48	1.60
t <sub>wwc</sub>	1.52	1.63	1.87	2.42
Power (μW/MHz)				
Power_read	20.24	43.27	98.07	242.66
Power_write	53.78	125.16	340.83	1063.80
Area (μm)				
Width	357.32	515.72	832.53	1466.16
Height	263.10	387.20	635.42	1131.84

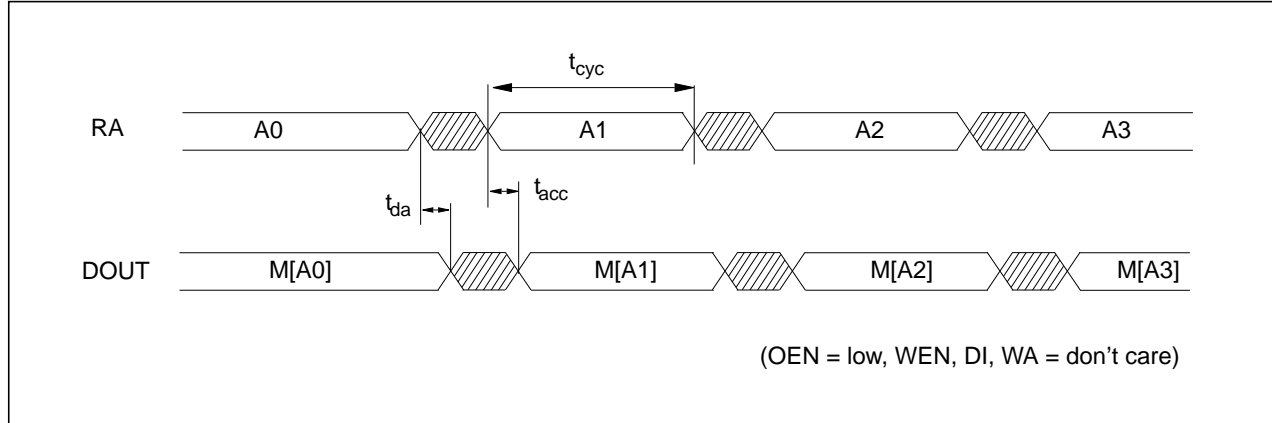


# ARFRAM\_HD

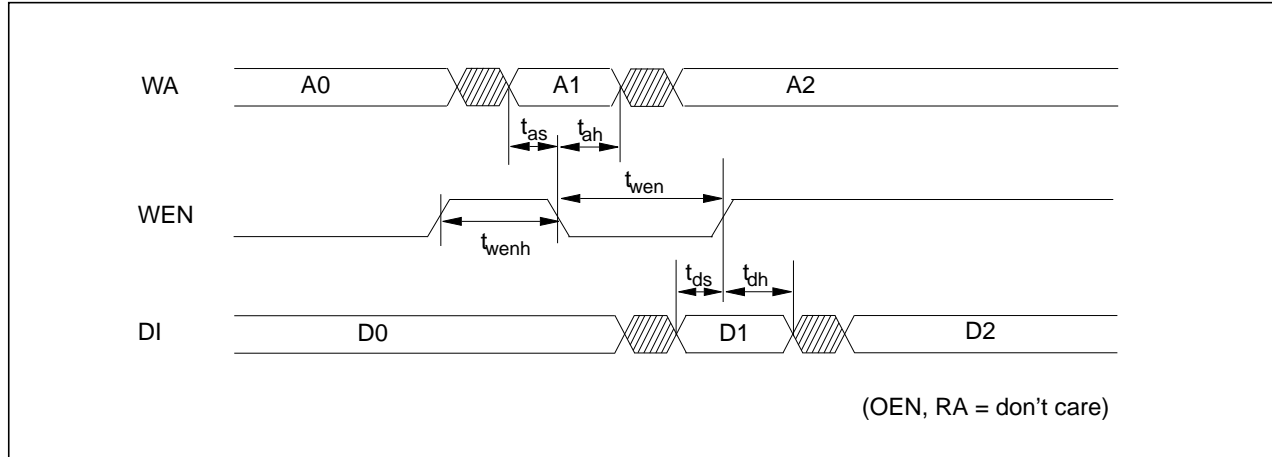
## High-Density Multi-port Asynchronous Register File

### Timing Diagrams

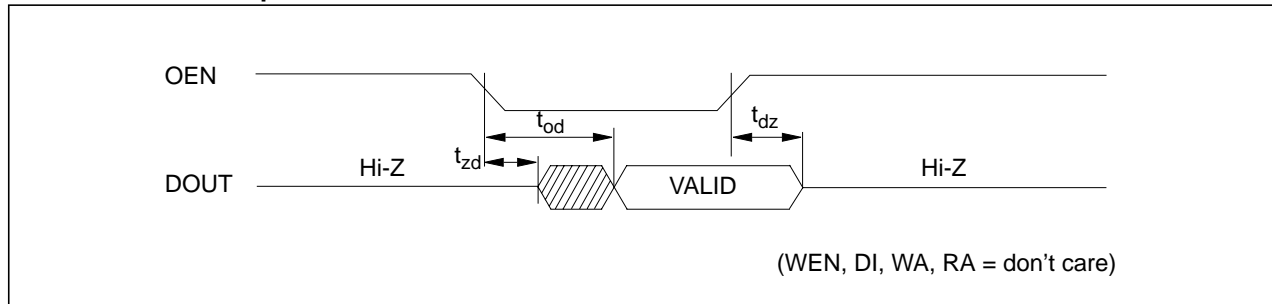
#### Read Cycle



#### Write Cycle



#### OEN Controlled Output Enable

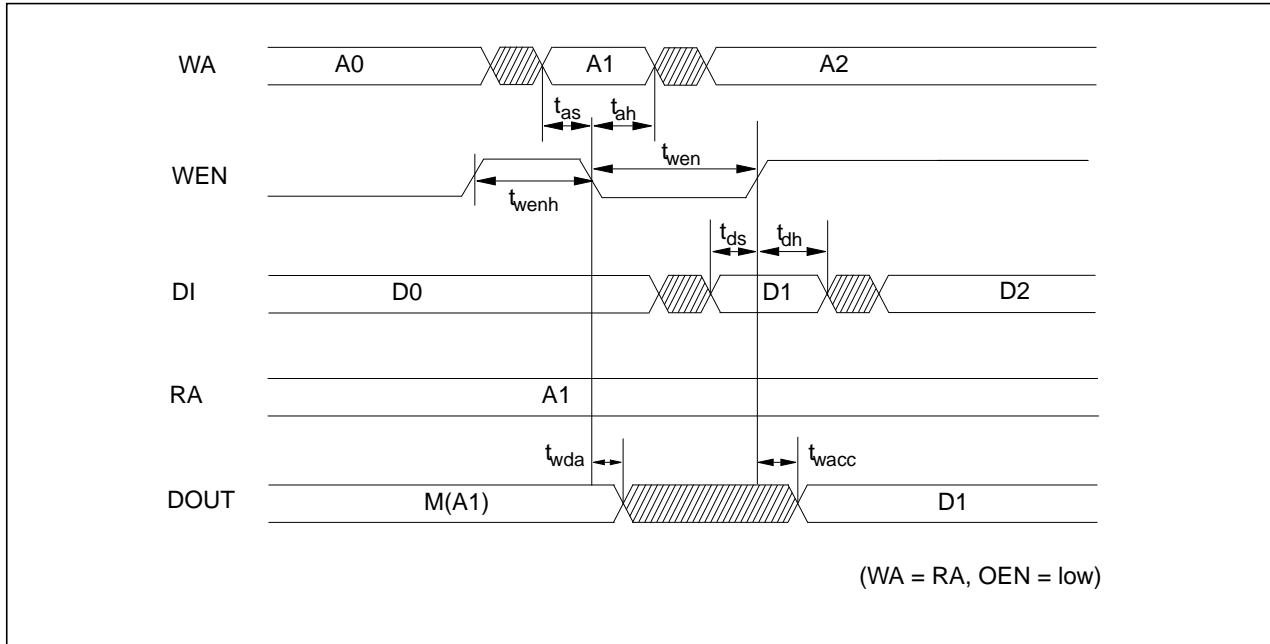


**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



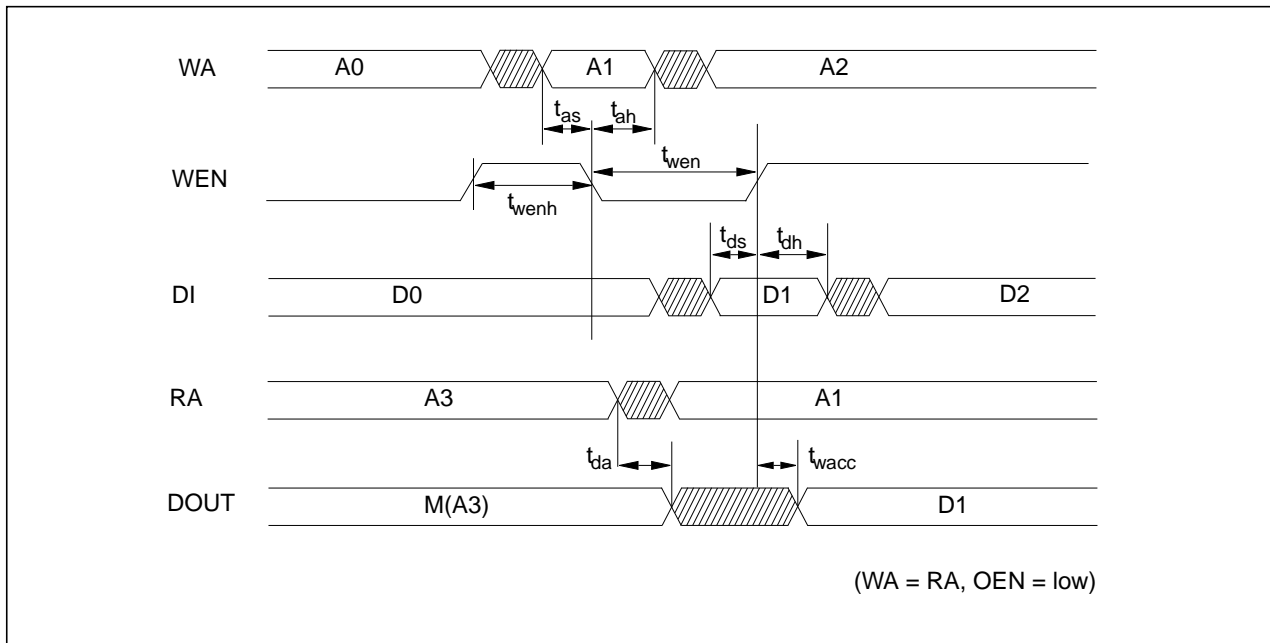
## High-Density Multi-port Asynchronous Register File

## Read-Write Contention



**NOTE:** If WEN[] falls while WA[] is same as RA[], it is a read-write contention. While WEN[] is low, DOUT[] is UNKNOWN and write data is valid. After  $t_{wacc}$  from the rising edge of WEN, the read data (D1) is valid.

## Write-Read Contention



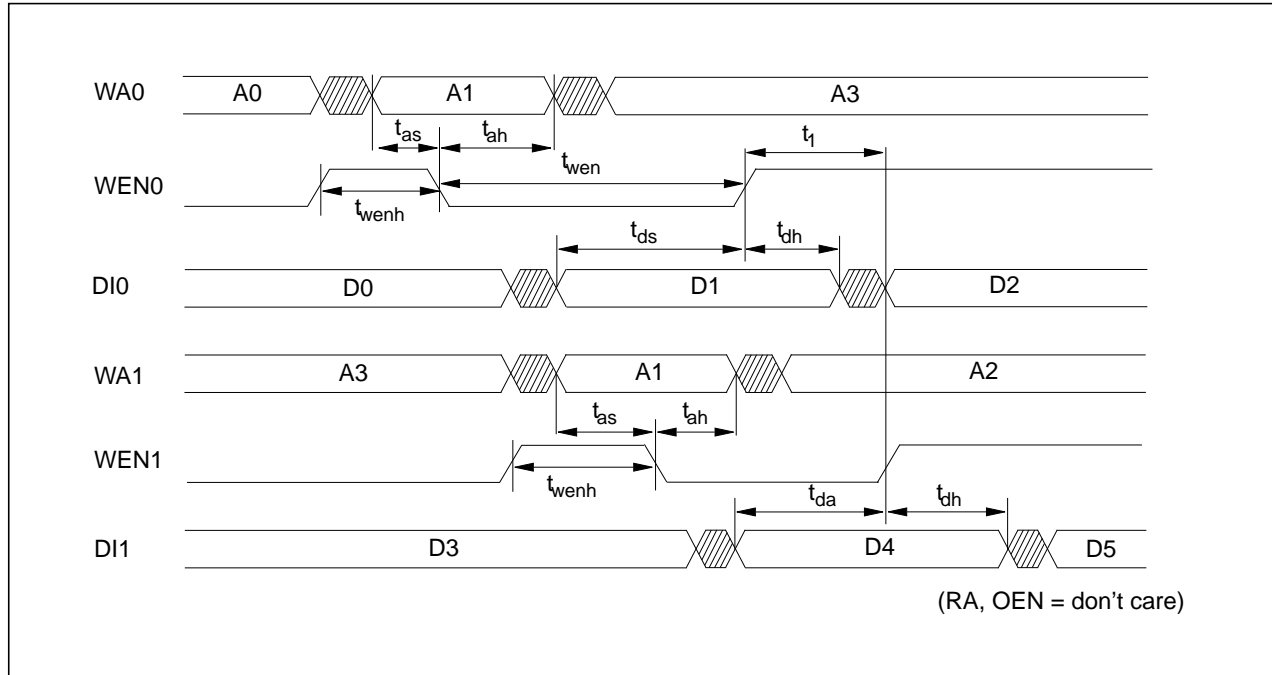
**NOTE:** While WEN is low, if read access begins by RA<>[] which is same as WA<>[] latched at the falling edge of WEN, it is Write-read contention. The read data is invalid whereas the write is still valid. After transition of RA[], DOUT[] is UNKNOWN and write is valid. After  $t_{wacc}$  from the rising edge of WEN, DOUT[] is valid.



## ARFRAM\_HD

### High-Density Multi-port Asynchronous Register File

#### Write-Write Contention

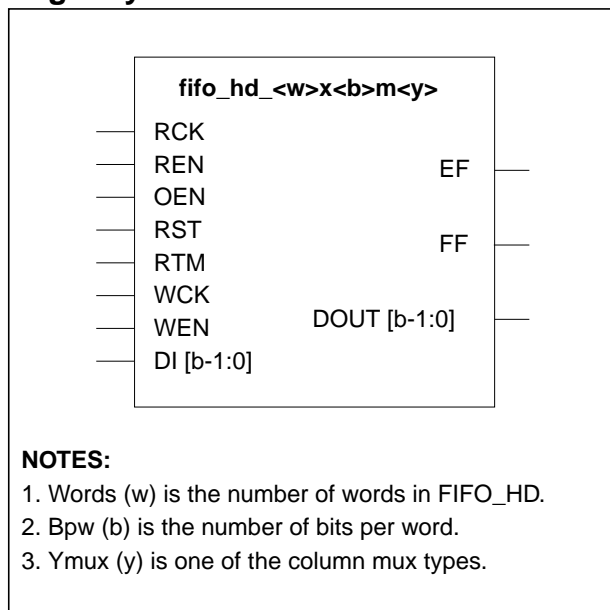


**NOTE:** If address latched at the falling edge of write ports are same and  $t_l$  is smaller than or equal to  $twwc$ , it is write-write contention. The data stored at current address will be unpredictable.



## High-Density Synchronous First-In First-Out Memory

## Logic Symbol



## Features

- Suitable for high-density applications
- Over-read and over-write protection capability
- Retransmit capability
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched full and empty status flag output
- Automatic power-down
- Flexible aspect ratio
- Up to 32Kbits capacity
- Up to 4K number of words
- Up to 64 number of bits per word

## Function Description

FIFO\_HD is a synchronous first-in first-out buffer memory which is provided as a compiler. FIFO\_HD is intended for use in high-density applications. After valid reset, on the rising of WCK, the write cycle is initiated when WEN is low, RST is high and FF is low. The data on DI[] is written into the memory location specified by the write pointer. During normal write operation, the rising edge of WCK will reset EF if it is set. At the last available memory location, write operation will set FF. DI[] and WEN must satisfy the setup and hold requirements with respect to the rising edge of WCK.

On the rising edge of RCK, the read cycle is initiated when REN is low, RST is high, RTM is high and EF is low. The data located in the memory specified by the read pointer comes in DOUT[] after some delay. During normal read operation, the rising edge of RCK will reset FF if it is set. At the last available memory location with available data, read operation will set EF. A valid DOUT[] will be possibly in some specified time after the rising edge of RCK, under that OEN is low. And the output data will remain unchanged until the next read, reset, or retransmit mode come in. REN must satisfy the setup and hold requirements with respect to the rising edge of RCK. When OEN is high, DOUT[] is placed in a high-impedance state.

In reset mode, a reset is globally initiated at the falling edge of RST. The reset operation will set EF and reset FF and make the data output zero. The reset operation will initiate the read pointer and the write pointer as 0. After reset operation, the status of EF will make RCK inoperable. The valid write input signal will become operable as RST is high. The read input signal will remain inoperable until EF is reset by the first read input signal valid write.

In retransmit mode, a retransmit is initiated at the falling edge of RTM only if the total number of writes after a reset operation is less than the word size of the memory in FIFO\_HD and more than 0 ( $0 < \text{total number of write} < W-1$ ). The retransmit operation will initiate the read pointer as 0 to allow the retransmission of data, make DOUT[] zero and make EF reset if it is set.

The valid read input signal will become operable as RTM is high.



## FIFO\_HD

### High-Density Synchronous First-In First-Out Memory

**FIFO\_HD Function Table**

RST	WEN	WCK	REN	RCK	RTM	OEN	EF	FF	DI	DOUT	COMMENT
↓	X	X	X	X	X	X	↑	↓	X	L	Reset mode
H	X	X	X	X	↓	X	↓	X	X	L	Retransmit mode
H	X	X	L	↑	H	L	L	↓	X	DOUT(t)	Read mode
H	L	↑	X	X	X	X	↓	L	valid	DOUT(t-1)	Write mode
H	X	X	L	↑	H	L	↑	L	X	DOUT(t)	Read and Empty mode
H	L	↑	X	X	X	X	L	↑	valid	DOUT(t-1)	Write and Full mode
H	X	X	H	↑	H	L	X	X	X	DOUT(t-1)	Note 1
H	X	X	L	↑	H	L	H	X	X	DOUT(t-1)	Note 2
X	X	X	X	X	X	H	X	X	X	Hi-Z	Note 3
H	H	↑	X	X	X	X	X	X	valid	DOUT(t-1)	Note 4
H	L	↑	X	X	X	X	X	H	valid	DOUT(t-1)	Note 5

**NOTES:**

1. Read is blocked when REN is high and the read port is in disable mode.
2. Read is blocked when EF is high (overread protection).
3. Under that OEN is high, DOUT[] goes to tri-state output mode.
4. Write is blocked when WEN is high and the write port is in disable mode.
5. Write is blocked when FF is high (overwrite protection).

### Parameter Description

FIFO\_HD is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	32	64	128	256
	Max	512	1024	2048	4096
	Step	32	64	128	256
Bpw (b)	Min	2	2	2	2
	Max	64	32	16	8
	Step	1	1	1	1



## High-Density Synchronous First-In First-Out Memory

## Pin Descriptions

Name	I/O	Description
RCK	Read Clock	Read Clock input. Upon the rising edge of RCK, it begins a read operation when REN is low, RST is high, RTM is high and EF is low.
REN	Read Enable	Read Enable input. When REN is low, the read access occurs properly. Conversely when REN is high, no read access can occur and the read port of the FIFO_HD goes to power down mode. REN is latched at the rising edge of RCK.
OEN	Data Output Enable	Output Enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
RST	Reset	Reset input. Upon the falling edge of RST, the reset mode is initiated. RST resets the read and write pointer to their initial position. RST sets EF and resets FF. RST makes DOUT[] zero.
RTM	Retransmit	Retransmit input. Upon the falling edge of RTM, the retransmit mode is initiated, provided that RST is high. RTM resets the read pointer to its initial position. RTM makes DOUT[] zero.
WCK	Write Clock	Write Clock input. Upon the rising edge of WCK, it begins a write operation when WE is low, RST is high and FF is low.
WEN	Write Enable	Write Enable input. When WEN is low, a write access occurs properly. Conversely when WEN is high, no write access can occur and the write port of the FIFO_HD goes to power down mode. WEN is latched at the rising edge of WCK.
DI	Date In	Data input bus. DI[] is latched on the rising edge of WCK. Data input is written into the addressed location in write mode.
EF	Empty Flag	Empty Flag. If the memory has no data to be read, EF goes high. Valid reset makes EF high and valid retransmit makes it low.
FF	Full Flag	Full Flag. If the memory has no vacancy to write data, FF goes high. Valid reset makes FF low.
DOUT	Data Out	Data output bus. Data output is valid after the rising edge of RCK while the FIFO_HD is in read mode when OEN is low. Conversely when OEN is high, DOUT[] goes to high-impedance state. By reset or retransmit operation. DOUT[] goes to 0.

## Pin Capacitance

Unit: [SL]

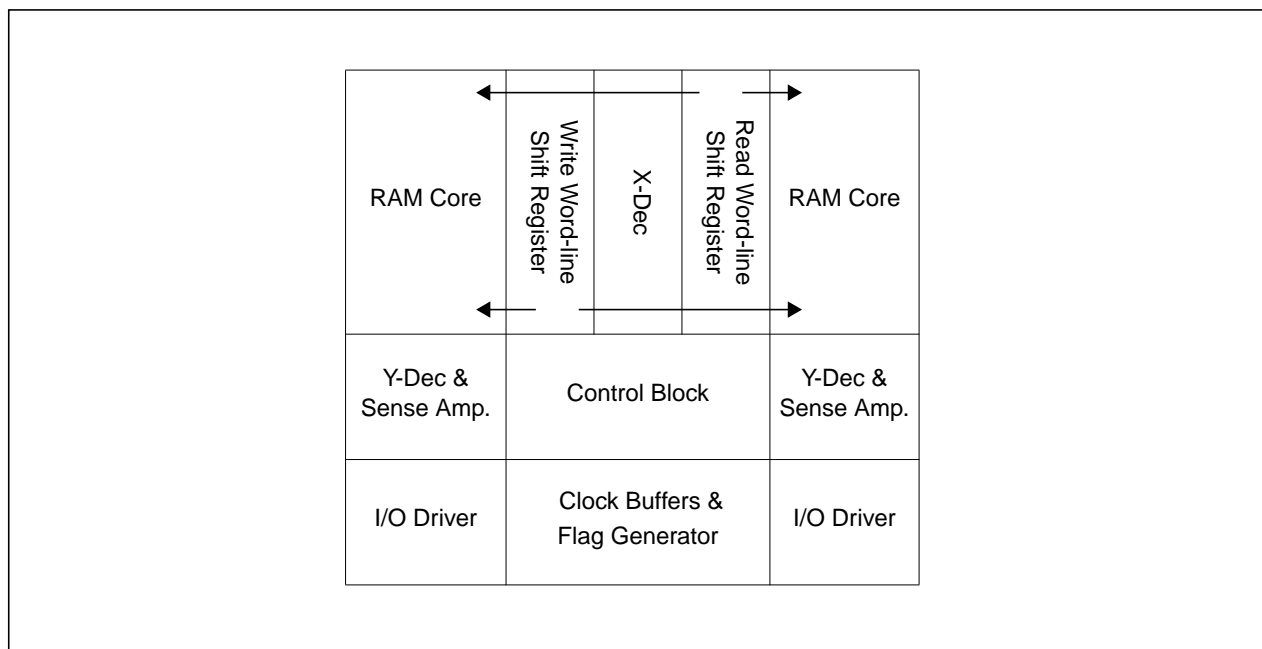
RST	RTM	WCK	RCK	OEN	WEN	REN	DI/DOUT
7.3	4.3	7.7	4.8	3.5	2.2	1.3	1.2/6.2



## FIFO\_HD

### High-Density Synchronous First-In First-Out Memory

#### Block Diagrams



#### Application Notes

1. Permitting Over-the-cell routing.  
In chip-level layout, over-the-cell routing in FIFO\_HD is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of FIFO\_HD.
4. FIFO\_HD must be reset before any operation performed.  
The reset operation initiates the read pointer and the write pointer as 0.
5. FIFO\_HD should be reset again before resuming normal operation if abnormal operation is performed.  
Abnormal operations are invalid retransmit attempt, and read/write operation causing timing requirement violations.
6. The retransmit operation initiates the read pointer as 0.
7. The retransmit is useful only when the total number of writes after a reset is less than the total word capacity of the FIFO\_HD and more than 0.
8. Outputs are not changed until the first valid read after a reset or retransmit.



## Characteristics

Definition for AC Timing (ns)	
Symbol	Description
trst	Min RST pulse width low
trtm	Min RTM pulse width low
trcyc	Read clock cycle time
trckh	Read clock pulse width high
trckl	Read clock pulse width low
twcyc	Write clock cycle time
twckh	Write clock pulse width high
twckl	Write clock pulse width low
trs	REN setup to RCK rising
trh	REN hold from RCK rising
tw	WEN setup to WCK rising
twh	WEN hold from WCK rising
twrcs	WCK setup to RCK rising
trwcs	RCK setup to WCK rising
tds	DI setup to WCK rising
tdh	DI hold from WCK rising
trstw	RST setup to WCK rising
trtmr	RTM setup to RCK rising
trste	Delay from RST falling to EF rising
trstf	Delay from RST falling to FF falling
trstd	Delay from RST falling to DOUT zero
trstda	Output hold time from RST falling to DOUT
trtme	Delay from RTM falling to EF falling
trtmd	Delay from RTM falling to DOUT zero
trtmda	Output hold time from RTM falling to DOUT
twe	Delay from WCK rising to EF falling
twf	Delay from WCK rising to FF rising
trf	Delay from RCK rising to FF falling
tre	Delay from RCK rising to EF rising
tacc	Data access time delay from RCK rising to DOUT[] transition
tda	De-access time output hold time from RCK rising to DOUT[]
tdz	DOUT drive to high-Z time
tzd	DOUT high-Z to drive time
tod	OEN to valid output time
Definition for Power Consumption ( $\mu$ W/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Definition for Area ( $\mu$ m)	
Width	The physical width in X-direction
Height	The physical height in Y-direction



# FIFO\_HD

## High-Density Synchronous First-In First-Out Memory

### Reference Table

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Symbol	Ymux=4				Ymux=8			
words	128	256	384	512	256	512	768	1024
bpw	16	32	48	64	8	16	24	32
<b>Timing (ns)</b>								
t <sub>rst</sub>	2.73	2.98	3.22	3.47	2.74	2.99	3.23	3.48
t <sub>rtm</sub>	3.32	3.54	3.81	4.14	3.33	3.55	3.82	4.15
t <sub>rcyc</sub>	2.65	2.96	3.26	3.56	2.67	2.98	3.28	3.57
t <sub>rckl</sub>	0.76	0.76	0.76	0.76	0.76	0.76	0.77	0.77
t <sub>rckh</sub>	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.54
t <sub>wcyc</sub>	2.60	2.90	3.21	3.51	2.61	2.91	3.21	3.52
t <sub>wckl</sub>	1.09	1.13	1.17	1.21	1.09	1.12	1.15	1.18
t <sub>wckh</sub>	0.65	0.68	0.72	0.76	0.66	0.69	0.72	0.75
t <sub>rs</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>rh</sub>	0.11	0.11	0.11	0.11	0.11	0.11	0.11	0.11
t <sub>ws</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>wh</sub>	0.11	0.11	0.11	0.11	0.11	0.11	0.11	0.11
t <sub>ds</sub>	0.08	0.06	0.04	0.02	0.09	0.07	0.05	0.04
t <sub>dh</sub>	0.49	0.52	0.56	0.60	0.48	0.51	0.54	0.58
t <sub>rstw</sub>	0.60	0.60	0.60	0.60	0.60	0.60	0.60	0.60
t <sub>rtmr</sub>	0.70	0.70	0.70	0.70	0.56	0.56	0.56	0.56
t <sub>wrcs</sub>	1.22	1.22	1.22	1.22	1.22	1.22	1.22	1.22
t <sub>rwcs</sub>	1.26	1.32	1.42	1.55	1.26	1.32	1.41	1.55
t <sub>rstd</sub>	2.71	2.98	3.26	3.55	2.80	3.07	3.35	3.64
t <sub>rstda</sub>	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t <sub>rste</sub>	2.72	2.96	3.21	3.45	2.72	2.96	3.21	3.47
t <sub>rstf</sub>	2.72	2.96	3.21	3.45	2.72	2.96	3.21	3.47
t <sub>rtmd</sub>	2.70	2.97	3.25	3.55	2.79	3.06	3.34	3.63
t <sub>rtmda</sub>	0.31	0.31	0.31	0.31	0.31	0.31	0.30	0.30
t <sub>rtme</sub>	3.35	3.57	3.85	4.17	3.37	3.59	3.86	4.19
t <sub>we</sub>	0.68	0.68	0.68	0.68	0.68	0.68	0.68	0.68
t <sub>wf</sub>	2.23	2.42	2.62	2.82	2.23	2.41	2.61	2.81
t <sub>re</sub>	2.08	2.27	2.46	2.67	2.09	2.27	2.47	2.67
t <sub>rf</sub>	0.69	0.69	0.70	0.70	0.69	0.69	0.69	0.69
t <sub>acc</sub>	2.15	2.37	2.61	2.85	2.17	2.40	2.63	2.87
t <sub>da</sub>	1.73	1.94	2.15	2.38	1.71	1.92	2.14	2.37
t <sub>dz</sub>	0.39	0.47	0.54	0.61	0.38	0.43	0.49	0.55
t <sub>zd</sub>	0.45	0.47	0.50	0.52	0.45	0.47	0.49	0.51
t <sub>od</sub>	0.70	0.75	0.80	0.85	0.69	0.72	0.75	0.77
<b>Power (μW/MHz)</b>								
Power_read	173.60	303.03	440.99	587.45	150.94	256.35	369.00	488.88
Power_write	169.14	299.42	439.63	589.78	131.96	220.73	315.77	417.07
<b>Area (μm)</b>								
Width	577.92	969.60	1361.28	1752.96	577.92	969.60	1361.28	1752.96
Height	367.20	541.92	716.64	891.36	384.18	558.90	733.62	908.34



## High-Density Synchronous First-In First-Out Memory

Reference Table

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Symbol	Ymux=16				Ymux=32			
words	512	1024	1536	2048	1024	2048	3072	4096
bpw	4	8	12	16	2	4	6	8
<b>Timing (ns)</b>								
t <sub>rst</sub>	2.74	2.99	3.23	3.48	2.74	2.99	3.24	3.49
t <sub>rtm</sub>	3.33	3.55	3.83	4.15	3.34	3.56	3.84	4.17
t <sub>rcyc</sub>	2.73	3.00	3.28	3.56	2.79	3.06	3.33	3.59
t <sub>rckl</sub>	0.76	0.76	0.77	0.77	0.76	0.76	0.77	0.77
t <sub>rckh</sub>	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.54
t <sub>wcyc</sub>	2.61	2.91	3.22	3.52	2.61	2.92	3.22	3.53
t <sub>wckl</sub>	1.08	1.11	1.14	1.17	1.08	1.11	1.14	1.16
t <sub>wckh</sub>	0.68	0.71	0.74	0.77	0.74	0.76	0.79	0.81
t <sub>rs</sub>	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
t <sub>rh</sub>	0.11	0.11	0.11	0.11	0.11	0.11	0.11	0.11
t <sub>ws</sub>	0.48	0.48	0.48	0.48	0.48	0.48	0.48	0.48
t <sub>wh</sub>	0.11	0.11	0.11	0.11	0.11	0.11	0.11	0.11
t <sub>ds</sub>	0.09	0.07	0.06	0.04	0.10	0.08	0.06	0.05
t <sub>dh</sub>	0.48	0.51	0.53	0.56	0.48	0.50	0.53	0.56
t <sub>rstw</sub>	0.60	0.60	0.60	0.60	0.60	0.60	0.60	0.60
t <sub>rtmr</sub>	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56
t <sub>wrcs</sub>	1.22	1.22	1.22	1.22	1.22	1.22	1.22	1.22
t <sub>rwcs</sub>	1.26	1.32	1.41	1.55	1.26	1.32	1.41	1.55
t <sub>rstd</sub>	2.97	3.24	3.52	3.81	3.29	3.57	3.85	4.13
t <sub>rstda</sub>	0.32	0.32	0.32	0.32	0.32	0.32	0.32	0.32
t <sub>rste</sub>	2.71	2.95	3.20	3.46	2.71	2.96	3.21	3.47
t <sub>rstf</sub>	2.71	2.95	3.20	3.46	2.71	2.96	3.21	3.47
t <sub>rtmd</sub>	2.96	3.23	3.51	3.80	3.28	3.56	3.84	4.12
t <sub>rtmda</sub>	0.31	0.31	0.30	0.30	0.31	0.31	0.31	0.31
t <sub>rtme</sub>	3.37	3.59	3.86	4.19	3.37	3.60	3.87	4.21
t <sub>we</sub>	0.68	0.68	0.68	0.68	0.68	0.68	0.68	0.68
t <sub>wf</sub>	2.23	2.42	2.61	2.81	2.23	2.42	2.62	2.81
t <sub>re</sub>	2.08	2.27	2.47	2.67	2.08	2.27	2.46	2.66
t <sub>rf</sub>	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69
t <sub>acc</sub>	2.22	2.45	2.68	2.92	2.30	2.53	2.76	3.00
t <sub>da</sub>	1.68	1.89	2.11	2.34	1.62	1.83	2.05	2.26
t <sub>dz</sub>	0.37	0.42	0.47	0.52	0.37	0.41	0.45	0.50
t <sub>zd</sub>	0.45	0.46	0.48	0.50	0.45	0.46	0.48	0.49
t <sub>od</sub>	0.69	0.71	0.74	0.76	0.69	0.71	0.73	0.75
<b>Power (μW/MHz)</b>								
Power_read	135.27	226.91	326.22	433.20	126.21	208.85	299.06	396.82
Power_write	110.48	178.15	250.39	327.19	97.58	154.68	215.62	280.39
<b>Area (μm)</b>								
Width	577.92	969.60	1361.28	1752.96	577.92	969.60	1361.28	1752.96
Height	388.10	562.82	737.54	912.26	405.36	580.08	754.80	929.52

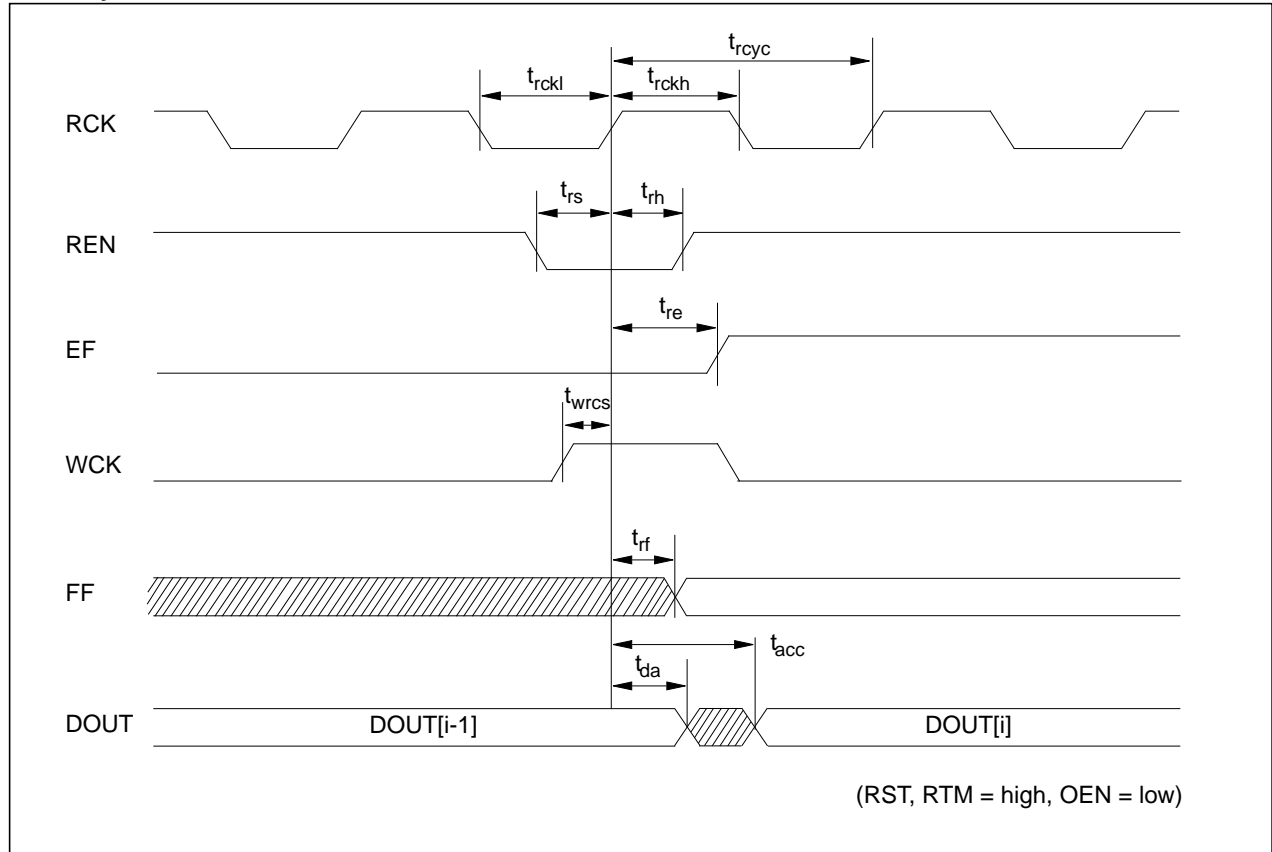


## FIFO\_HD

### High-Density Synchronous First-In First-Out Memory

#### Timing Diagrams

##### Read Cycle



##### NOTES:

1. Read cycle is blocked during empty state (over-read protected)
2. Twrcs is the timing related between first write on empty state and first subsequent read. If it is not satisfied, DOUT[i] will be unpredictable.
3. The is the timing related the read and empty mode.



1. Write cycle is blocked during full state (over-write protected)
2. Trwcs is the timing related between first read on full state and first subsequent write. If it is not satisfied, DOUT[j] (not shown) will be unpredictable.
3. Twf is the timing related the write and full mode.

The diagram shows the timing relationships between several signals during a reset sequence. A vertical line marks the start of the reset event.

- RST**: A reset signal that transitions from high to low and then back to high. The duration of the low pulse is  $t_{rst}$ . The time from the rising edge of RST to the rising edge of WCK/RCK is  $t_{rstw}$ .
- WCK, RCK**: Clock signals that transition from low to high and then back to low. The duration of the high pulse is marked with  $*NOTE$ .
- EF**: A signal that transitions from high to low. The time from the rising edge of RST to the falling edge of EF is  $t_{rste}$ .
- FF**: A signal that transitions from high to low. The time from the rising edge of RST to the falling edge of FF is  $t_{rstf}$ .
- DOUT**: A data output signal. Before the reset, it shows a value  $DOUT[i-1]$ . At the rising edge of RST, it transitions to a high-impedance state (indicated by a hatched box) for a duration  $t_{rstda}$ . After the reset, it transitions to  $All\ 0's$ . The time from the rising edge of RST to the falling edge of the high-impedance state is  $t_{rstd}$ .

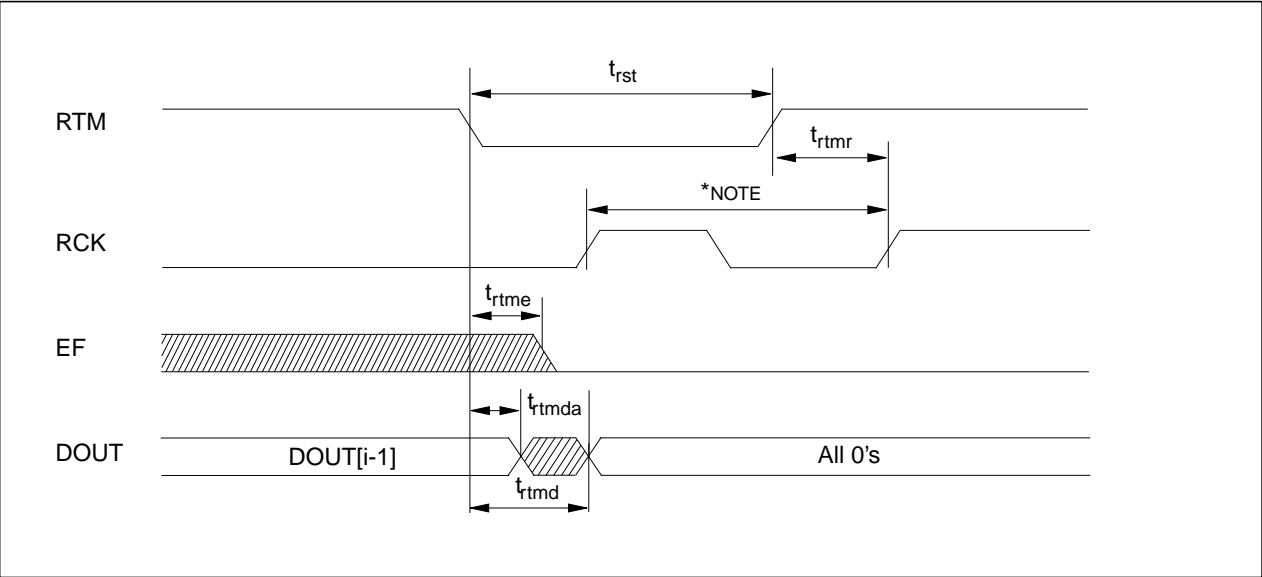
**NOTE:** Read cycle and write cycle are blocked when RST is low.



FIFO\_HD

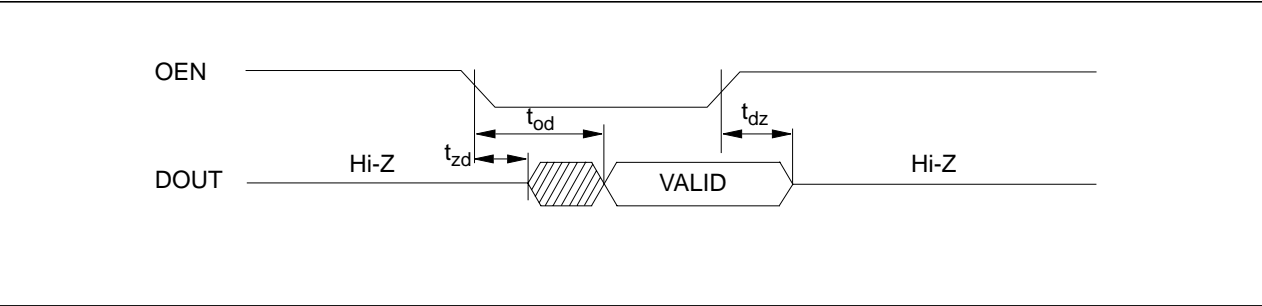
High-Density Synchronous First-In First-Out Memory

Retransmit Cycle



NOTE: Read cycle is blocked when RTM is low.

OEN Controlled Output Enable

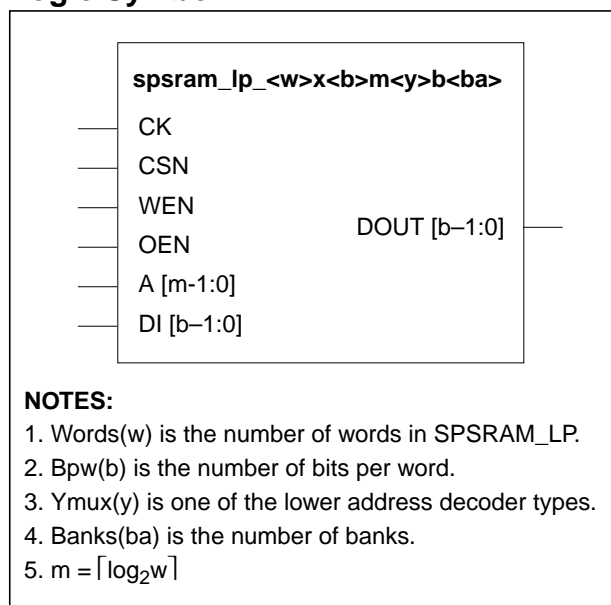




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## Logic Symbol



## Features

- Suitable for low-power application
- Separated data I/O
- Synchronous operation
- Asynchronous tristate output
- Latched inputs and outputs
- Automatic power-down mode available
- Self-controlled circuit available
- Zero standby current
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bit per word

## Function Description

SPSRAM\_LP is a single-port synchronous static RAM which is provided as a compiler. SPSRAM\_LP is intended for use in low-power applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data on DI[] is written into the memory location specified on A[]. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

CK	CSN	WEN	OEN	A	DI	DOUT	COMMENT
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read Cycle

## Parameter Description

SPSRAM\_LP is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y) and Number of banks(ba).



## SPSRAM\_LP

### Low-Power Single-Port Synchronous Static RAM

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	ba = 1	Min	32	64	128	256
		Max	1024	2048	4096	8192
		Step	16	32	64	128
	ba = 2	Min	64	128	256	512
		Max	2048	4096	8192	16384
		Step	32	64	128	256
Bpw (b)		Min	1	1	1	1
		Max	128	64	32	16
		Step	1	1	1	1

### Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

### Pin Capacitance

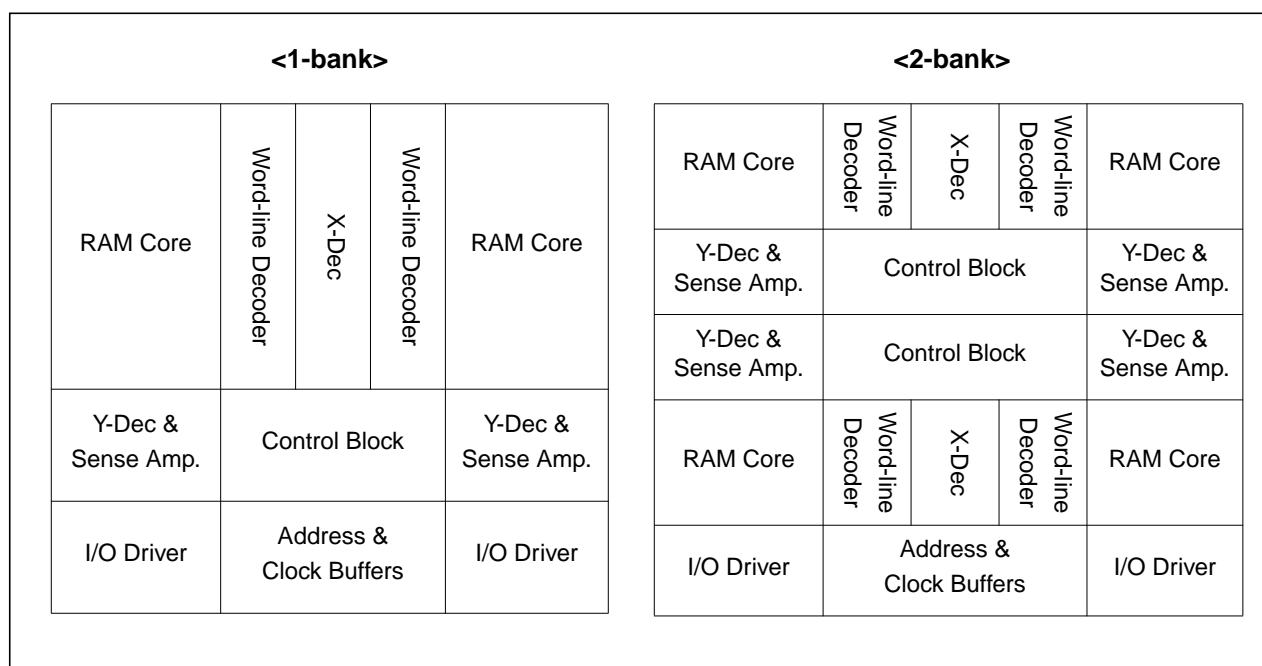
Unit: [SL]

CK	CSN	WEN	OEN	A	DI	DOUT
8.15	14.34	7.73	5.75	9.02	3.07	9.44



## Block Diagrams

SPSRAM\_LP has 2 different physical architectures due to the word depth. For a specific configuration, only one of these architectures is generated from SPSRAM\_LP compiler. Power is only consumed by the bank that is selected by the address and the other bank will be in idle mode.



## Application Notes

1. Permitting Over-the-cell routing.  
In chip-level layout, over-the-cell routing in SPSRAM\_LP is permitted only for Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of SPSRAM\_LP.
4. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## SPSRAM\_LP

### Low-Power Single-Port Synchronous Static RAM

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#### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
t <sub>cyc</sub>	Clock cycle time	t <sub>ckh</sub>	Clock pulse width high
t <sub>ckl</sub>	Clock pulse width low	t <sub>as</sub>	Address setup time
t <sub>ah</sub>	Address hold time	t <sub>cs</sub>	CSN setup time
t <sub>ch</sub>	CSN hold time	t <sub>ds</sub>	Data-In setup time
t <sub>dh</sub>	Data-In hold time	t <sub>ws</sub>	WEN setup time
t <sub>wh</sub>	WEN hold time	t <sub>acc</sub>	Data access time
t <sub>da</sub>	De-access time	t <sub>dz</sub>	DOUT drive to high-Z time
t <sub>zd</sub>	DOUT high-Z to drive time	t <sub>od</sub>	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## Low-Power Single-Port Synchronous Static RAM

## Reference Table

\* For Ymux=4

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	256	512	512	1024	768	1536	1024	2048
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.92	5.67	5.92	6.79	6.95	7.86	8.02	8.90
t <sub>ckl</sub>	1.48	1.84	1.59	2.03	1.71	2.21	1.84	2.38
t <sub>ckh</sub>	2.45	2.69	2.99	3.30	3.49	3.88	3.96	4.43
t <sub>as</sub>	0.61	0.87	0.64	0.94	0.74	1.02	0.90	1.09
t <sub>ah</sub>	0.81	1.00	0.84	1.10	0.86	1.19	0.87	1.26
t <sub>cs</sub>	1.21	1.69	1.34	1.91	1.46	2.11	1.58	2.30
t <sub>ch</sub>	0.39	0.63	0.39	0.71	0.39	0.79	0.39	0.87
t <sub>ds</sub>	0.52	0.66	0.52	0.75	0.52	0.84	0.52	0.93
t <sub>dh</sub>	0.93	1.34	1.02	1.51	1.10	1.67	1.16	1.81
t <sub>ws</sub>	0.86	1.10	0.92	1.20	0.96	1.28	0.96	1.34
t <sub>wh</sub>	0.81	1.00	0.84	1.10	0.86	1.19	0.87	1.26
t <sub>acc</sub>	3.31	3.63	3.98	4.42	4.62	5.18	5.23	5.92
t <sub>da</sub>	2.92	3.18	3.58	3.94	4.22	4.66	4.83	5.35
t <sub>dz</sub>	0.72	0.71	0.82	0.82	0.90	0.90	0.97	0.97
t <sub>zd</sub>	0.85	0.84	0.96	0.94	1.05	1.04	1.13	1.14
t <sub>od</sub>	0.99	0.99	1.10	1.10	1.19	1.19	1.27	1.27
Power (μW/MHz)								
Power_read	143.46	163.94	281.99	335.50	432.10	537.16	593.77	768.90
Power_write	172.57	186.29	376.58	406.40	629.80	684.41	932.24	1020.33
Power_standby	0.99	4.15	1.12	5.11	1.14	5.95	1.04	6.65
Area (μm)								
Width	700.90	700.90	1303.55	1303.55	1906.21	1906.21	2508.86	2508.86
Height	483.42	927.14	807.26	1574.82	1131.10	2222.50	1454.94	2870.18

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



# SPSRAM\_LP

## Low-Power Single-Port Synchronous Static RAM

### Reference Table

\* For Ymux=8

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.92	5.66	5.91	6.76	6.94	7.82	8.02	8.83
t <sub>ckl</sub>	1.48	1.84	1.55	2.03	1.62	2.21	1.69	2.39
t <sub>ckh</sub>	2.46	2.69	2.99	3.30	3.49	3.88	3.96	4.43
t <sub>as</sub>	0.62	0.87	0.62	0.94	0.67	1.02	0.76	1.09
t <sub>ah</sub>	0.81	1.00	0.84	1.09	0.86	1.18	0.87	1.28
t <sub>cs</sub>	1.20	1.68	1.28	1.88	1.35	2.07	1.39	2.25
t <sub>ch</sub>	0.39	0.63	0.39	0.71	0.39	0.79	0.39	0.87
t <sub>ds</sub>	0.52	0.66	0.52	0.75	0.52	0.84	0.52	0.93
t <sub>dh</sub>	0.92	1.31	0.99	1.46	1.05	1.62	1.10	1.76
t <sub>ws</sub>	0.86	1.10	0.92	1.18	0.96	1.27	0.96	1.35
t <sub>wh</sub>	0.81	1.00	0.84	1.09	0.86	1.18	0.87	1.28
t <sub>acc</sub>	3.35	3.68	4.02	4.47	4.65	5.23	5.26	5.96
t <sub>da</sub>	2.93	3.21	3.60	3.96	4.24	4.68	4.84	5.36
t <sub>dz</sub>	0.69	0.69	0.77	0.77	0.86	0.83	0.88	0.88
t <sub>zd</sub>	0.82	0.82	0.91	0.91	0.98	0.98	1.03	1.03
t <sub>od</sub>	0.96	0.96	1.05	1.05	1.12	1.12	1.17	1.17
Power (μW/MHz)								
Power_read	101.97	118.37	188.68	225.33	281.29	347.48	379.81	484.83
Power_write	119.22	130.03	243.99	264.23	395.25	429.37	573.01	625.45
Power_standby	1.06	4.16	1.18	5.08	1.28	6.03	1.35	7.02
Area (μm)								
Width	700.90	700.90	1303.55	1303.55	1906.21	1906.21	2508.86	2508.86
Height	483.42	927.14	807.26	1574.82	1131.10	2222.50	1454.94	2870.18

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



## Reference Table

\* For Ymux=16

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.92	5.65	5.90	6.75	6.94	7.80	8.03	8.80
t <sub>ckl</sub>	1.48	1.84	1.54	2.04	1.59	2.22	1.63	2.39
t <sub>ckh</sub>	2.46	2.70	2.99	3.30	3.49	3.88	3.96	4.42
t <sub>as</sub>	0.62	0.87	0.65	0.94	0.66	1.02	0.66	1.09
t <sub>ah</sub>	0.81	1.00	0.84	1.10	0.86	1.19	0.87	1.26
t <sub>cs</sub>	1.20	1.68	1.26	1.87	1.31	2.05	1.34	2.22
t <sub>ch</sub>	0.39	0.63	0.39	0.71	0.39	0.79	0.39	0.87
t <sub>ds</sub>	0.52	0.66	0.52	0.75	0.52	0.84	0.52	0.93
t <sub>dh</sub>	0.91	1.31	0.98	1.46	1.03	1.60	1.07	1.71
t <sub>ws</sub>	0.86	1.10	0.92	1.20	0.96	1.28	0.97	1.34
t <sub>wh</sub>	0.81	1.00	0.84	1.10	0.86	1.19	0.87	1.26
t <sub>acc</sub>	3.39	3.74	4.06	4.53	4.70	5.29	5.31	6.02
t <sub>da</sub>	2.96	3.23	3.61	3.98	4.25	4.69	4.86	5.37
t <sub>dz</sub>	0.68	0.68	0.74	0.74	0.80	0.80	0.83	0.84
t <sub>zd</sub>	0.81	0.80	0.88	0.87	0.94	0.93	0.98	0.99
t <sub>od</sub>	0.95	0.95	1.02	1.02	1.08	1.08	1.12	1.12
Power (μW/MHz)								
Power_read	79.66	92.67	139.36	164.69	202.03	244.30	267.66	331.51
Power_write	92.55	101.98	178.34	193.64	279.29	302.67	395.39	429.07
Power_standby	1.03	4.20	1.13	5.18	1.20	6.13	1.24	7.04
Area (μm)								
Width	700.90	700.90	1303.55	1303.55	1906.21	1906.21	2508.86	2508.86
Height	483.42	927.14	807.26	1574.82	1131.10	2222.50	1454.94	2870.18

**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



# SPSRAM\_LP

## Low-Power Single-Port Synchronous Static RAM

### Reference Table

\* For Ymux=32

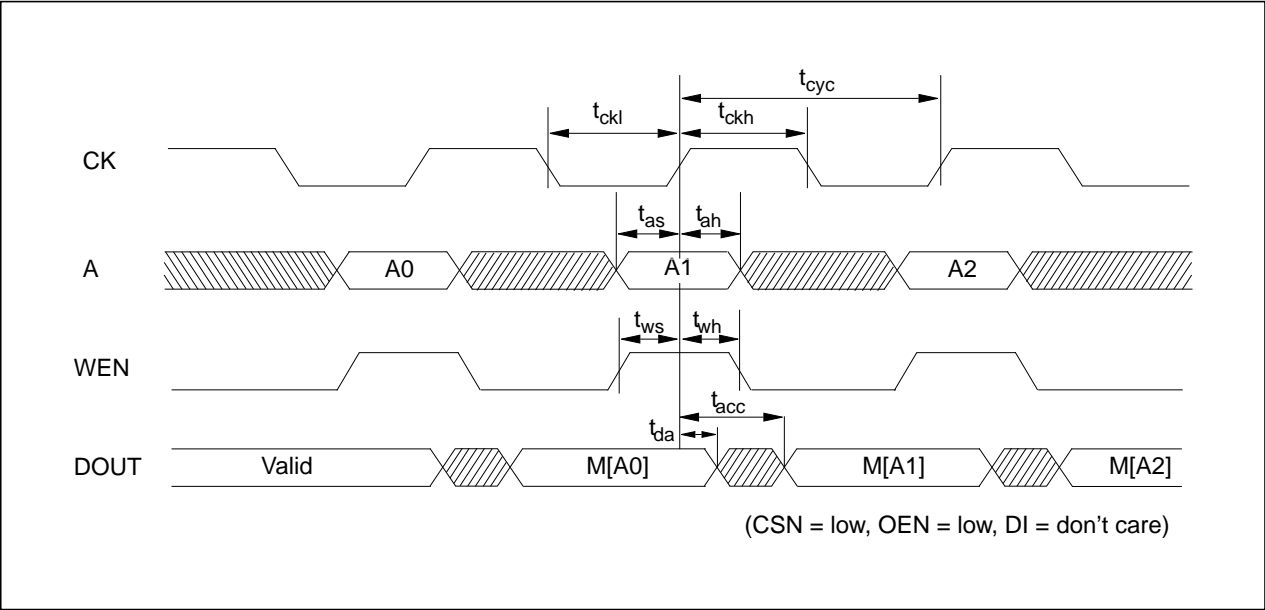
(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	4	4	8	8	12	12	16	16
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.97	5.73	5.97	6.82	7.03	7.87	8.14	8.87
t <sub>ckl</sub>	1.45	1.84	1.51	2.04	1.57	2.22	1.61	2.39
t <sub>ckh</sub>	2.54	2.78	3.06	3.38	3.56	3.95	4.02	4.49
t <sub>as</sub>	0.62	0.87	0.64	0.94	0.64	1.02	0.63	1.09
t <sub>ah</sub>	0.80	1.00	0.84	1.10	0.86	1.19	0.87	1.26
t <sub>cs</sub>	1.18	1.68	1.24	1.87	1.29	2.05	1.31	2.22
t <sub>ch</sub>	0.39	0.63	0.39	0.71	0.39	0.79	0.39	0.87
t <sub>ds</sub>	0.52	0.66	0.52	0.75	0.52	0.84	0.52	0.93
t <sub>dh</sub>	0.92	1.31	0.99	1.47	1.04	1.60	1.07	1.71
t <sub>ws</sub>	0.84	1.10	0.91	1.20	0.95	1.28	0.97	1.33
t <sub>wh</sub>	0.80	1.00	0.84	1.10	0.86	1.19	0.87	1.26
t <sub>acc</sub>	3.57	3.94	4.24	4.74	4.89	5.50	5.50	6.24
t <sub>da</sub>	3.09	3.37	3.75	4.12	4.39	4.83	4.99	5.51
t <sub>dz</sub>	0.68	0.68	0.75	0.75	0.79	0.79	0.82	0.82
t <sub>zd</sub>	0.81	0.81	0.88	0.88	0.94	0.94	0.97	0.97
t <sub>od</sub>	0.95	0.95	1.02	1.03	1.08	1.08	1.11	1.11
Power (μW/MHz)								
Power_read	69.74	80.33	118.40	137.56	168.63	198.70	220.43	263.75
Power_write	80.77	88.55	149.52	161.64	227.80	245.38	315.63	339.75
Power_standby	1.03	4.17	1.12	5.12	1.21	6.06	1.29	7.00
Area (μm)								
Width	686.34	686.34	1295.06	1295.06	1903.78	1903.78	2512.50	2512.50
Height	483.42	927.14	807.26	1574.82	1131.10	2222.50	1454.94	2870.18

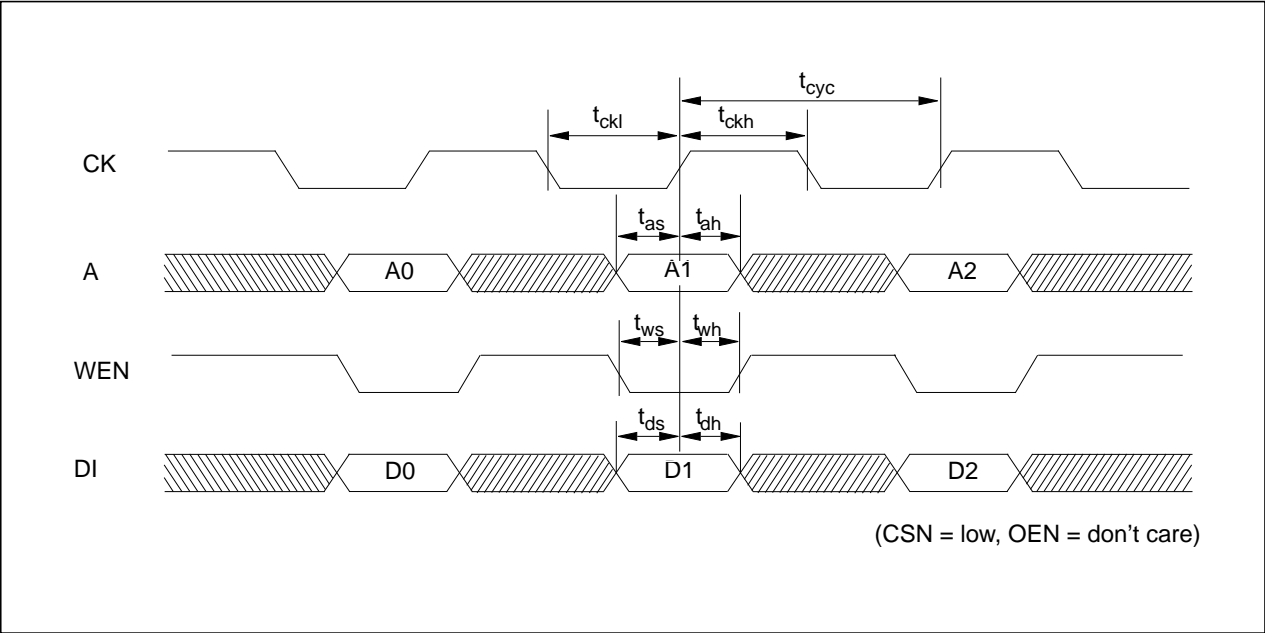
**NOTE:** Standby power is measured on condition that CSN is High and the others are in normal operation mode.



Read Cycle



Write Cycle

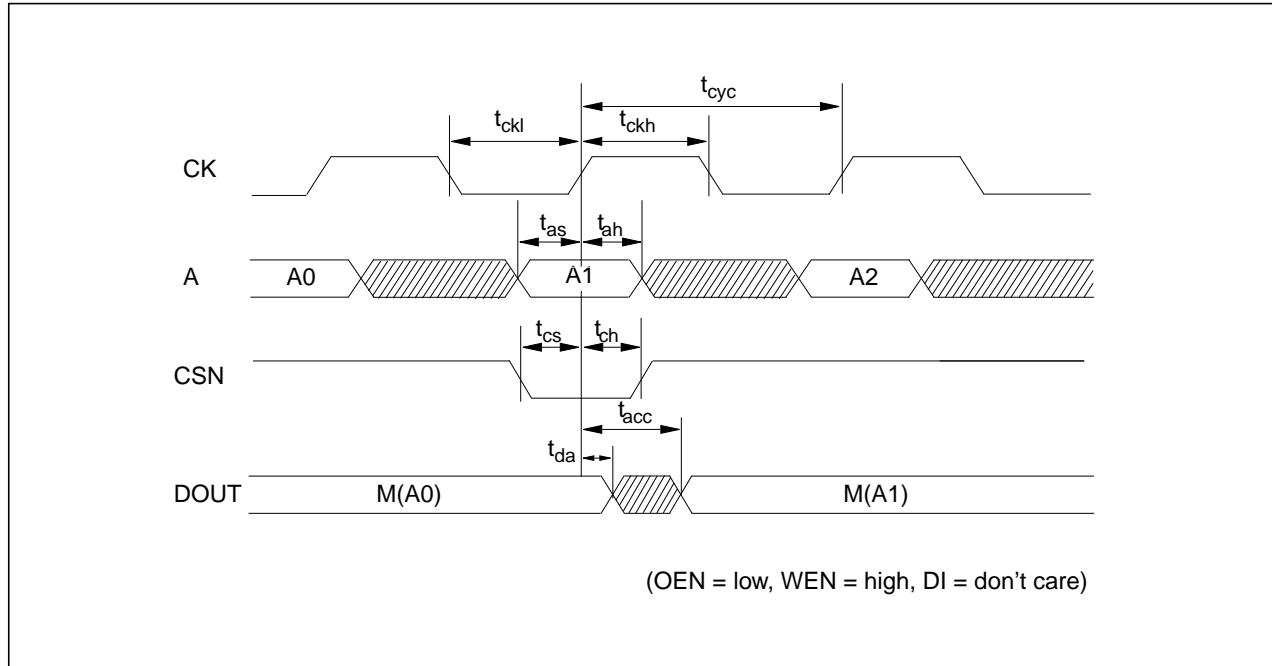




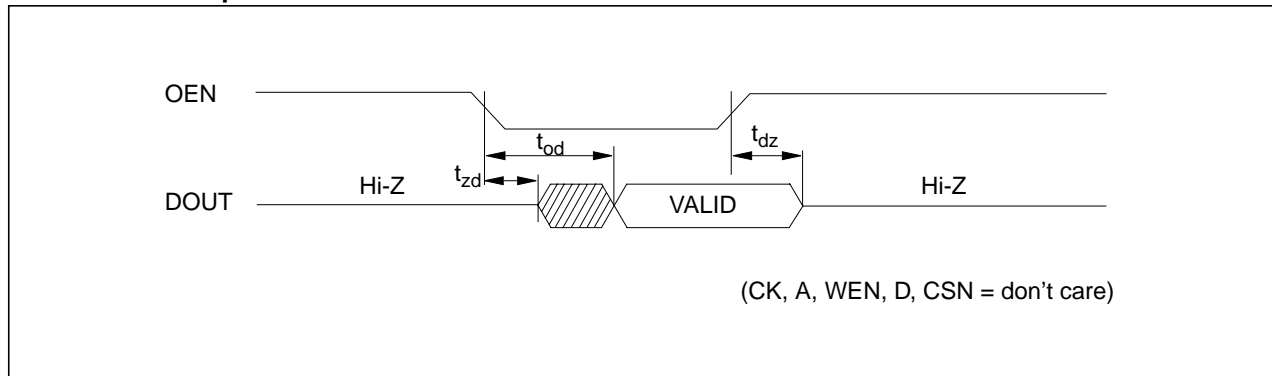
## SPSRAM\_LP

### Low-Power Single-Port Synchronous Static RAM

#### CSN Control



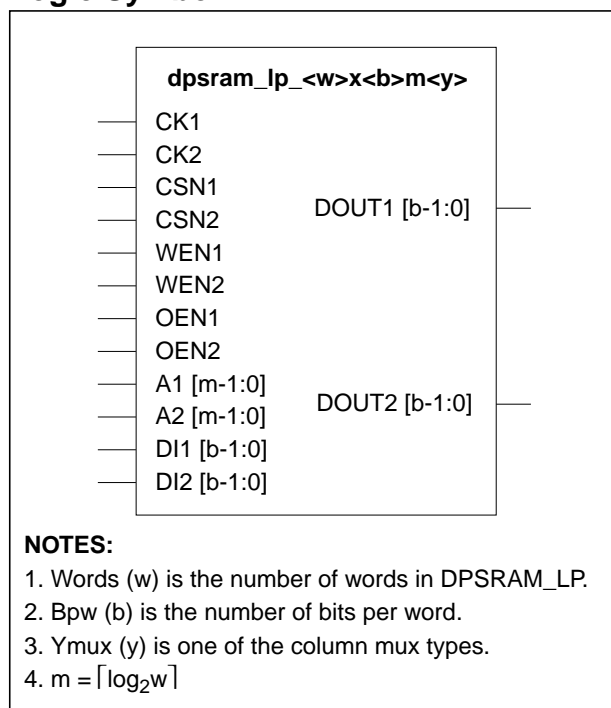
#### OEN Control Output Enable



**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## Logic Symbol



## Features

- Suitable for low-power applications
- Synchronous operation
- Positive-edge clock operation
- Automatic power-down mode available
- Self-controlled circuit available
- Asynchronous tristate output
- Low noise output optimization
- Separated data I/O
- Flexible aspect ratio
- Zero standby current
- Latched inputs and outputs
- Up to 128Kbits capacity
- Up to 8K number of words
- Up to 128 number of bit per word

## Function Description

DPSRAM\_LP is a dual-port synchronous static RAM which is provided as a compiler. DPSRAM\_LP is intended for use in low-power applications. Each port is fully independent. On the rising edge of CK1 (CK), the write cycle is initiated when WEN1 (WEN2) is low and CSN1 (CSN2) is low. The data on DI1[] (DI2[]) is written into the memory location specified on A1[] (A2[]). During the write cycle, DOUT1[] (DOUT2[]) remains stable. On the rising edge of CK1 (CK2), the read cycle is initiated when WEN1 (WEN2) is high and CSN1 (CSN2) is low. The data at DOUT1[] (DOUT2[]) become valid after a delay. While in standby mode that CSN1 (CSN2) is high, A1[] (A2[]) and DI1[] (DI2[]) are disabled, data stored in the memory is retained and DOUT1[] (DOUT2[]) remains stable. When OEN1 (OEN2) is high, DOUT1[] (DOUT2[]) is placed in a high-impedance state.

DPSRAM\_LP Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read Cycle



# DPSRAM\_LP

## Low-Power Dual-Port Synchronous Static RAM

### Parameter Description

DPSRAM\_LP is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and column mux(y).

Parameters		YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	32	64	128	256
	Max	1024	2048	4096	8192
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

### Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [] A2 []	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [] DI2 []	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [] DOUT2 []	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

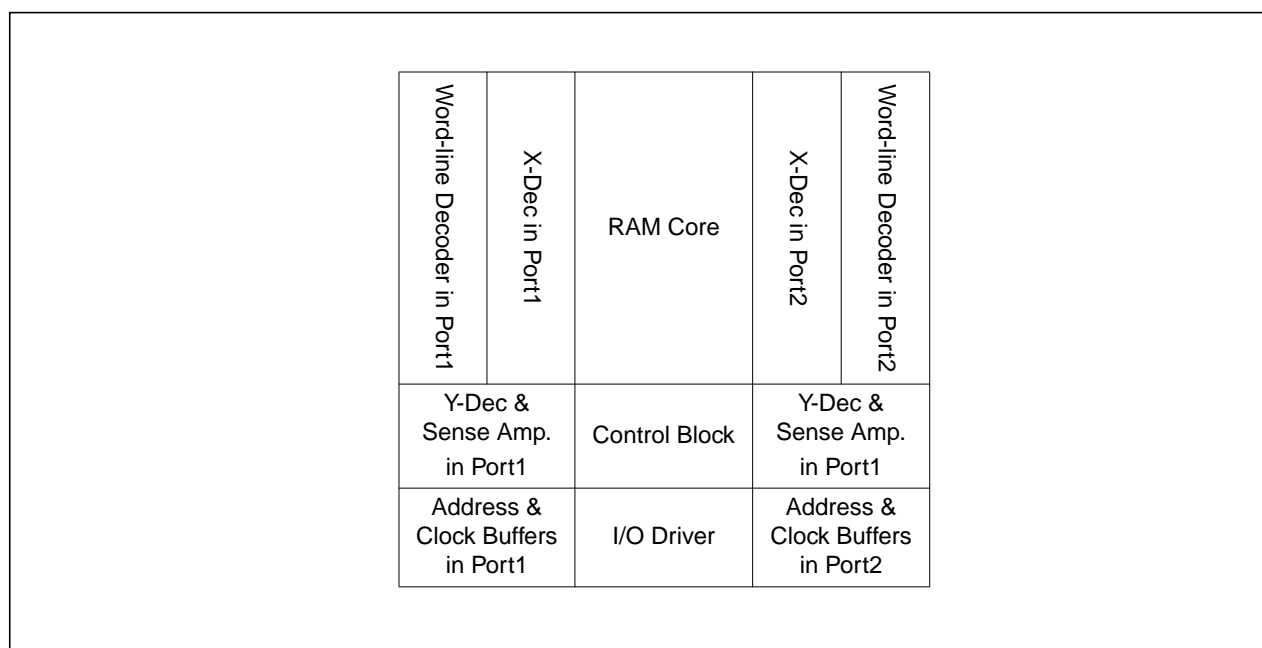
### Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT
5.04	12.00	7.25	4.51	8.02	4.94	9.13



## Block Diagram



## Application Notes

1. **Permitting Over-the-cell routing**  
In chip-level layout, over-the-cell routing in DPSRAM\_LP is permitted for only Metal-5 layer.
2. **Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.**
3. **Power stripe should be tapped from both sides of DPSRAM\_LP.**
4. **Contention mode in same address access**  
In DPSRAM\_LP, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAM\_LP has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions. Power reduction during standby mode.
5. **Power reduction during standby mode**  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## DPSRAM\_LP

### Low-Power Dual-Port Synchronous Static RAM

#### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Clock cycle time	tckl	Clock pulse width low
tckh	Clock pulse width high	tcc	Clock to Clock Setup time
tas	Address setup time	tah	Address hold time
tcs	CSN setup time	tch	CSN hold time
tds	Data-In setup time	tdh	Data-In hold time
twS	WEN setup time	twh	WEN hold time
tacc	Data access time	tda	De-access time
tdz	DOUT drive to high-Z time	tzd	DOUT high-Z to drive time
tod	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## Reference Table

\* For Ymux=4

(Typical process 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	256	512	768	1024
bpw	32	64	96	128
Timing (ns)				
t <sub>cyc</sub>	5.16	6.79	8.59	10.58
t <sub>ckl</sub>	1.43	1.65	1.97	2.39
t <sub>ckh</sub>	2.43	3.29	4.25	5.32
t <sub>cc</sub>	2.17	3.02	3.96	4.99
t <sub>as</sub>	0.60	0.79	1.01	1.26
t <sub>ah</sub>	0.67	0.70	0.71	0.71
t <sub>cs</sub>	1.32	1.65	2.06	2.56
t <sub>ch</sub>	0.35	0.36	0.36	0.36
t <sub>ds</sub>	0.24	0.24	0.24	0.24
t <sub>dh</sub>	0.92	1.14	1.38	1.65
t <sub>ws</sub>	0.85	0.89	0.91	0.90
t <sub>wh</sub>	0.67	0.70	0.71	0.71
t <sub>acc</sub>	3.27	4.32	5.51	6.84
t <sub>da</sub>	2.87	3.93	5.12	6.45
t <sub>dz</sub>	0.80	1.02	1.27	1.54
t <sub>zd</sub>	0.93	1.16	1.41	1.67
t <sub>od</sub>	1.06	1.29	1.54	1.80
Power (μW/MHz)				
Power_read	201.94	407.65	633.31	878.92
Power_write	239.50	537.32	915.91	1375.29
Power_standby	1.25	1.53	1.95	2.52
Area (μm)				
Width	1063.71	2012.43	2961.15	3909.87
Height	524.26	873.70	1223.14	1572.58

## NOTES:

1. In power consumption of DPSRAM\_LP, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## DPSRAM\_LP

### Low-Power Dual-Port Synchronous Static RAM

#### Reference Table

\* For Ymux=8 (Typical process 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	512	1024	1536	2048
bpw	16	32	48	64
Timing (ns)				
t <sub>cyc</sub>	5.13	6.76	8.59	10.64
t <sub>ckl</sub>	1.41	1.64	2.00	2.49
t <sub>ckh</sub>	2.43	3.29	4.25	5.32
t <sub>cc</sub>	2.17	3.02	3.96	4.99
t <sub>as</sub>	0.64	0.88	1.15	1.44
t <sub>ah</sub>	0.67	0.70	0.71	0.71
t <sub>cs</sub>	1.27	1.59	2.04	2.63
t <sub>ch</sub>	0.36	0.36	0.36	0.36
t <sub>ds</sub>	0.24	0.24	0.24	0.24
t <sub>dh</sub>	0.89	1.06	1.25	1.46
t <sub>ws</sub>	0.85	0.89	0.91	0.90
t <sub>wh</sub>	0.67	0.70	0.71	0.71
t <sub>acc</sub>	3.32	4.38	5.58	6.90
t <sub>da</sub>	2.90	3.95	5.15	6.47
t <sub>dz</sub>	0.76	0.94	1.13	1.34
t <sub>zd</sub>	0.89	1.07	1.26	1.46
t <sub>od</sub>	1.02	1.20	1.40	1.60
Power (μW/MHz)				
Power_read	143.73	276.51	419.61	573.02
Power_write	166.62	353.80	584.54	858.84
Power_standby	1.27	1.39	1.51	1.63
Area (μm)				
Width	1063.71	2012.43	2961.15	3909.87
Height	524.26	873.70	1223.14	1572.58

#### NOTES:

1. In power consumption of DPSRAM\_LP, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## Reference Table

\* For Ymux=16

(Typical process 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	1024	2048	3072	4096
bpw	8	16	24	32
<b>Timing (ns)</b>				
t <sub>cyc</sub>	5.18	6.92	8.74	10.62
t <sub>ckl</sub>	1.42	1.61	1.89	2.24
t <sub>ckh</sub>	2.44	3.29	4.25	5.32
t <sub>cc</sub>	2.17	3.02	3.96	5.00
t <sub>as</sub>	0.60	0.80	1.02	1.27
t <sub>ah</sub>	0.67	0.70	0.71	0.71
t <sub>cs</sub>	1.26	1.53	1.89	2.36
t <sub>ch</sub>	0.36	0.36	0.36	0.36
t <sub>ds</sub>	0.24	0.24	0.24	0.24
t <sub>dh</sub>	0.87	1.02	1.19	1.37
t <sub>ws</sub>	0.85	0.89	0.91	0.90
t <sub>wh</sub>	0.67	0.70	0.71	0.71
t <sub>acc</sub>	3.36	4.43	5.62	6.94
t <sub>da</sub>	2.91	3.97	5.16	6.94
t <sub>dz</sub>	0.74	0.89	1.06	1.24
t <sub>zd</sub>	0.87	1.03	1.20	1.36
t <sub>od</sub>	1.00	1.16	1.33	1.51
<b>Power (μW/MHz)</b>				
Power_read	102.73	197.93	298.62	404.79
Power_write	120.48	254.06	412.66	596.28
Power_standby	1.28	1.37	1.49	1.62
<b>Area (μm)</b>				
Width	1063.71	2012.43	2961.15	3909.87
Height	524.26	873.70	1223.14	1572.58

## NOTES:

1. In power consumption of DPSRAM\_LP, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



# DPSRAM\_LP

## Low-Power Dual-Port Synchronous Static RAM

### Reference Table

\* For Ymux=32 (Typical process 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	2048	4096	6144	8192
bpw	4	8	12	16
<b>Timing (ns)</b>				
t <sub>cyc</sub>	5.16	6.91	8.74	10.65
t <sub>ckl</sub>	1.43	1.67	1.93	2.19
t <sub>ckh</sub>	2.44	3.29	4.25	5.32
t <sub>cc</sub>	2.17	3.02	3.96	5.00
t <sub>as</sub>	0.59	0.79	1.01	1.26
t <sub>ah</sub>	0.67	0.70	0.71	0.71
t <sub>cs</sub>	1.27	1.59	1.93	2.28
t <sub>ch</sub>	0.36	0.36	0.36	0.36
t <sub>ds</sub>	0.24	0.24	0.24	0.24
t <sub>dh</sub>	0.86	1.00	1.16	1.33
t <sub>ws</sub>	0.85	0.89	0.91	0.91
t <sub>wh</sub>	0.67	0.70	0.71	0.71
t <sub>acc</sub>	3.43	4.52	5.71	7.03
t <sub>da</sub>	2.94	3.99	5.19	6.51
t <sub>dz</sub>	0.73	0.87	1.03	1.19
t <sub>zd</sub>	0.86	1.01	1.16	1.32
t <sub>od</sub>	0.99	1.14	1.29	1.46
<b>Power (μW/MHz)</b>				
Power_read	88.33	165.78	246.32	329.93
Power_write	103.72	212.70	337.55	478.29
Power_standby	1.28	1.36	1.47	1.60
<b>Area (μm)</b>				
Width	1063.71	2012.43	2961.15	3909.87
Height	524.26	873.70	1223.14	1572.58

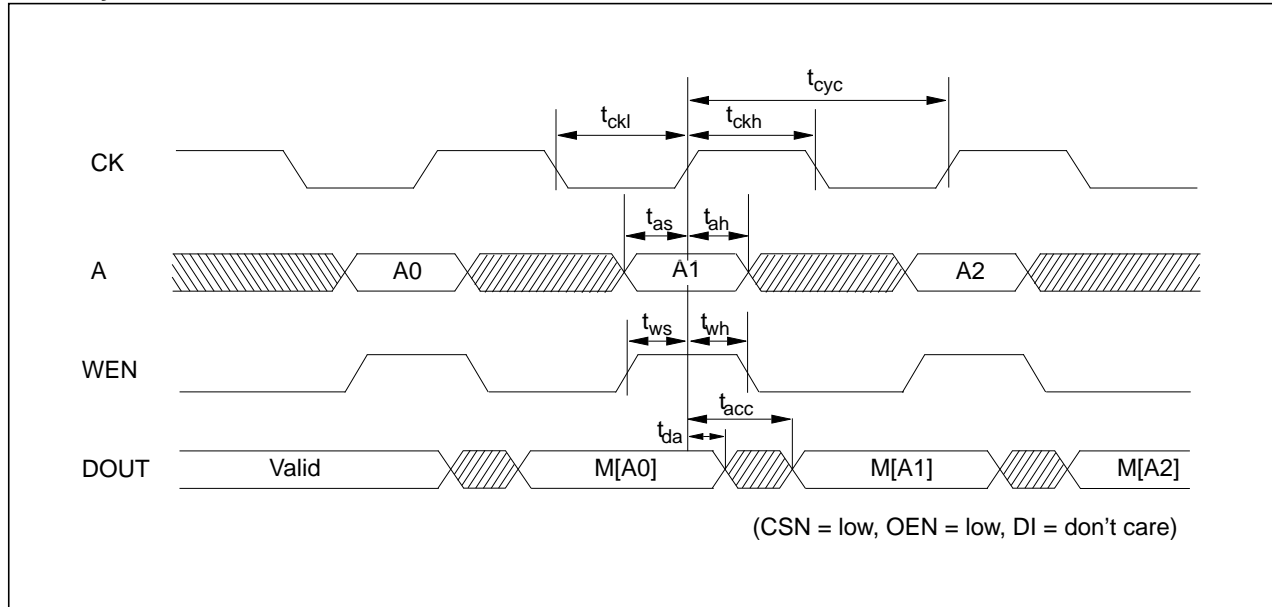
#### NOTES:

1. In power consumption of DPSRAM\_LP, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

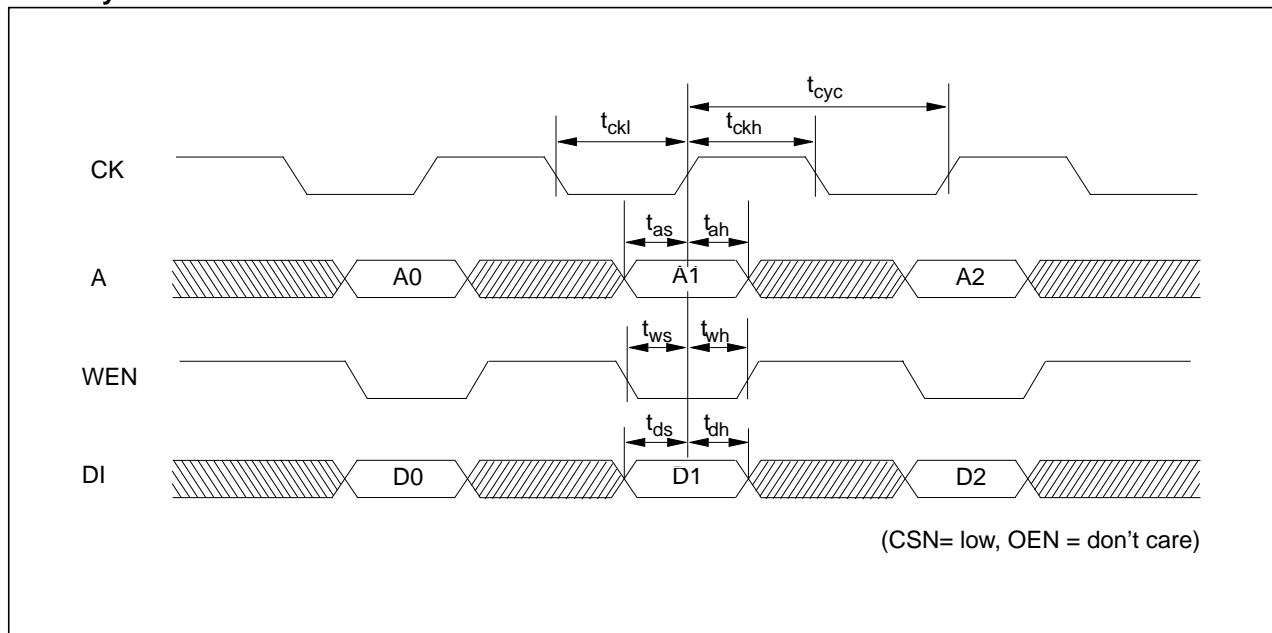


## Timing Diagrams

### Read Cycle



### Write Cycle

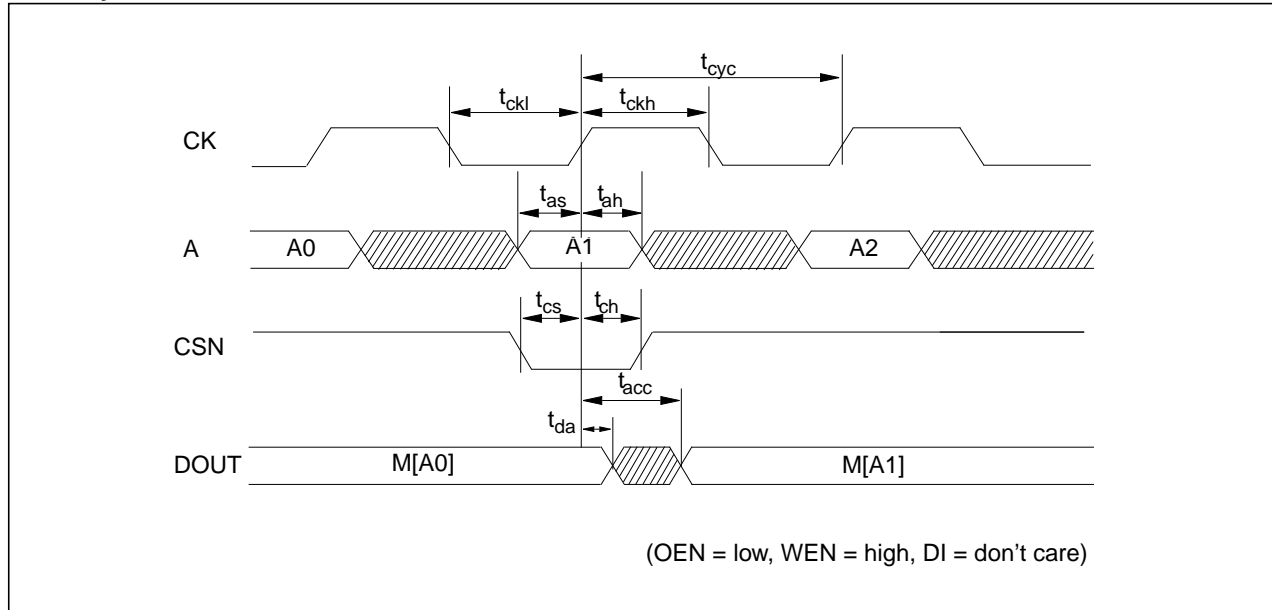




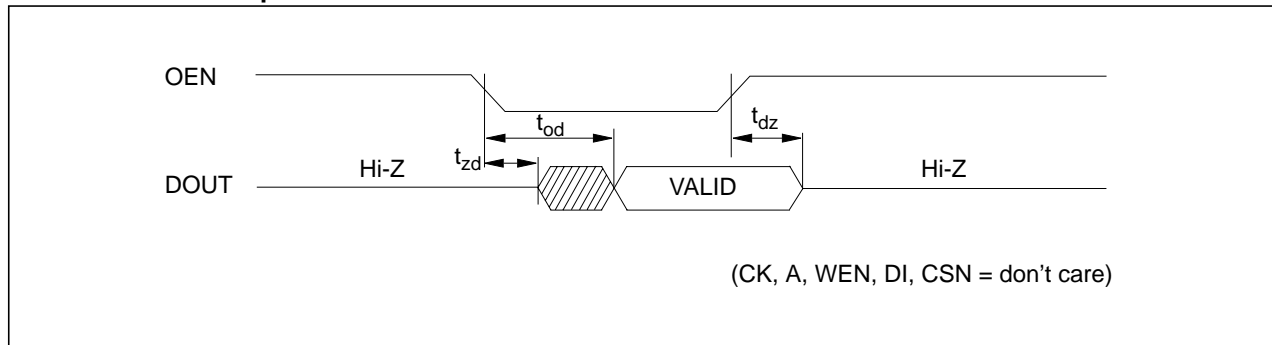
## DPSRAM\_LP

### Low-Power Dual-Port Synchronous Static RAM

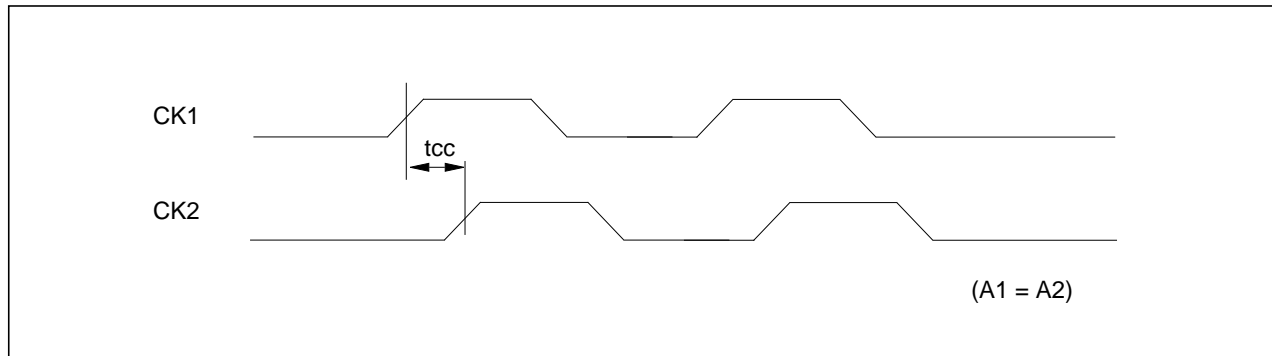
#### Read Cycle with CSN Controlled



#### OEN Controlled Output Enable



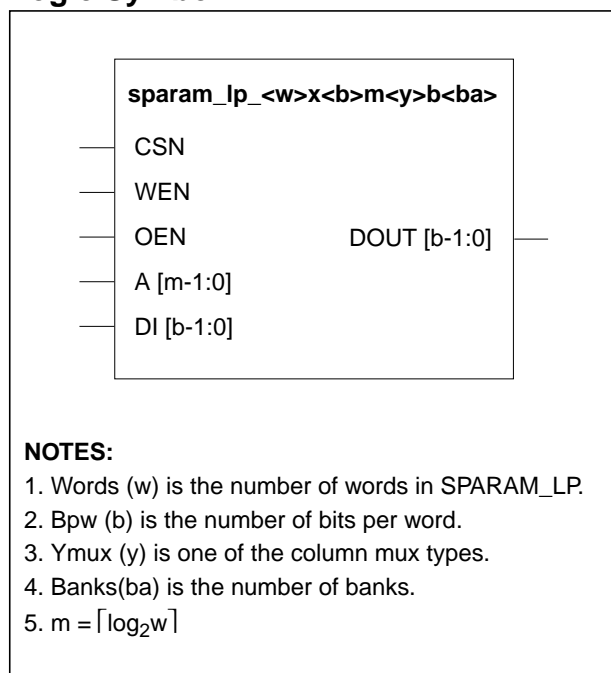
#### Contention Mode



**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## Logic Symbol



## Features

- Suitable for low-power applications
- Standby (power down) mode available
- Separated data I/O
- Asynchronous operation
- Asynchronous tri-state output
- Address transition detectors
- Write enable transition detector
- Chip select transition detector
- Bank select transition detector
- Automatic power-down mode
- Low noise output optimization
- Zero standby current
- Flexible aspect ratio
- Dual bank scheme available
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bit per word

## Function Description

SPARAM\_LP is a single-port asynchronous static RAM which is provided as a compiler. SPARAM\_LP is intended for use in low-power applications. At the falling edge of WEN, the write cycle is initiated. At the rising edge of WEN, the write cycle is ended. During the write cycle, the data on DI[] is written into the memory location specified on A[]. The read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay whenever A[] transition is detected. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

## SPARAM\_LP Function Table

CSN	WEN	OEN	A	DI	DOUT	Comment
X	X	H	X	X	Z	Unconditional tri-state output
H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
L	↓	L	Valid	Valid	DOUT(t-1)	Write cycle starts
L	↑	L	Valid	Valid	MEM(A)	Write cycle ends and read cycle starts
L	L	L	Stable	Valid	DOUT(t-1)	Write cycle
L	H	L	Toggle	X	MEM(A)	Read cycle



# SPARAM\_LP

## Low-Power Single-Port Asynchronous Static RAM

### Parameter Description

SPARAM\_LP is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y) and Number of banks(ba).

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	ba = 1	Min	32	64	128	256
		Max	1024	2048	4096	8192
		Step	16	32	64	128
	ba = 2	Min	64	128	256	512
		Max	2048	4096	8192	16384
		Step	32	64	128	256
Bpw (b)		Min	1	1	1	1
		Max	128	64	32	16
		Step	1	1	1	1

### Pin Descriptions

Name	I/O	Description
CSN	Chip Enable	Chip Select Input. The chip select signal acts as the memory enable signal for selections of multiple blocks. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if low, a read or write access can occur. When CSN falls, an access is initiated.
WEN	Read/Write Enable	Write Enable Input. The write enable signal selects the type of memory access. The high state for a read access and the low state for a write access. Upon the rising edge of WEN, a write access completed and a read access initiated.
OEN	Data Output Enable	Output Enable Input. The output enable signal controls the output drivers from driven to tri-state condition unconditionally.
A [ ]	Address	Address input bus. A[] should be stable when WEN is low. The address selects the location to be accessed. When the address changes, the transition is detected and the internal clock pulse is generated.
DI [ ]	Data Input	Data Input bus. The data input is written to the accessed location when WEN is low.
DOUT [ ]	Data Output	Data Output bus. The data output is data stored in the accessed location during a read access. Data output driver has tri-state logic. When OEN is low, the driver drives a certain value. Otherwise, data output keeps Hi-Z state. During a write access, data on DOUT is predictable.

### Pin Capacitance

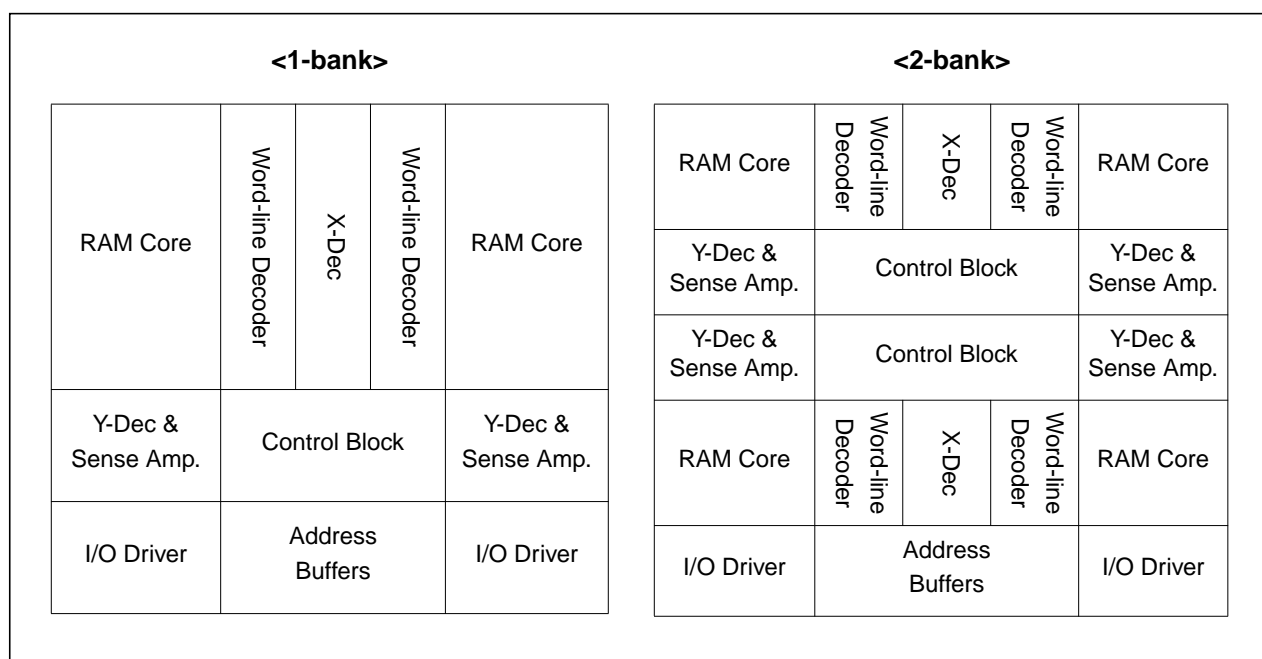
Unit: [SL]

	CSN	WEN	OEN	A	DI/DOUT			
					Ymux = 4	Ymux = 8	Ymux = 16	Ymux = 32
ba = 1	1.87	1.87	1.87	3.91	1.87/7.12	1.87/7.12	1.87/7.12	1.87/7.12
ba = 2	1.87	1.87	1.87	3.91	1.87/7.12	1.87/7.12	1.87/7.12	1.87/7.12



## Block Diagrams

SPARAM\_LP has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPARAM\_LP compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode.



## Application Notes

1. Permitting over-the-cell routing  
In chip-level layout, over-the-cell routing in SPARAM\_LP is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of SPARAM\_LP.
4. Avoiding short transition on the address bus  
In SPARAM\_LP, rather than the write operation which is synchronously performed by WEN signal, the read operation is asynchronously performed whenever the address transition is occurred. In this case, if the short transition on the address, called a skew, is happened, since SPARAM\_LP recognizes the short address transition as the stable address transition and do perform a read operation. At that time, while in the read operation, the data stored in the memory may be corrupted due to the short transition. To prevent such fail, the stable address cycle time (tcyc) is required. The essential requirement to recognize valid address transition is that at least minimum address period should be equal or greater than tacc (access time).
5. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## SPARAM\_LP

### Low-Power Single-Port Asynchronous Static RAM

#### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Address cycle time	tas	Address setup time
tcas	Address setup time for CSN rise	tah	Address hold time
twh	WEN hold time	tcs	CSN setup time
tch	CSN hold time	tds	Data-In setup time
tdh	Data-In hold time	twen	WEN pulse width low
tacc	Data access time for read cycle	twacc	Data access time for WEN rise
tda	De-access time	twda	De-access time for WEN rise
tzd	DOUT high-Z to drive time	tdz	DOUT drive to high-Z time
tod	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## Low-Power Single-Port Asynchronous Static RAM

## Reference Table

\* For Ymux=4

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	256	512	512	1024	768	1536	1024	2048
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.24	4.35	4.68	4.83	5.11	5.32	5.55	5.81
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	4.19	4.29	4.62	4.78	5.06	5.27	5.49	5.75
t <sub>ah</sub>	1.78	1.79	2.19	2.21	2.61	2.63	3.03	3.05
t <sub>wh</sub>	4.19	4.29	4.62	4.78	5.06	5.27	5.49	5.75
t <sub>ds</sub>	0.10	0.09	0.12	0.17	0.11	0.20	0.07	0.17
t <sub>dh</sub>	0.66	0.63	0.73	0.69	0.85	0.74	0.94	0.80
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.19	1.31	1.28	1.46	1.38	1.60	1.47	1.75
t <sub>wen</sub>	2.93	3.10	3.30	3.55	3.67	4.01	4.04	4.47
t <sub>acc</sub>	4.24	4.35	4.68	4.83	5.11	5.32	5.55	5.81
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.24	1.36	1.33	1.51	1.43	1.65	1.52	1.80
t <sub>dz</sub>	0.34	0.35	0.42	0.42	0.49	0.49	0.56	0.56
t <sub>zd</sub>	0.29	0.29	0.37	0.36	0.44	0.44	0.52	0.52
t <sub>od</sub>	0.45	0.45	0.53	0.53	0.61	0.61	0.69	0.69
Power (μW/MHz)								
Power_read	127.68	155.00	237.46	301.07	352.92	469.66	474.07	660.77
Power_write	205.47	230.05	440.97	513.60	751.22	898.01	1136.22	1383.27
Power_standby	17.01	27.91	31.03	53.82	45.17	84.92	59.44	121.20
Area (μm)								
Width	831.84	831.84	1437.28	1437.28	2042.72	2042.72	2648.17	2648.17
Height	529.32	1017.68	853.16	1665.36	1177.00	2313.04	1500.84	2960.72

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



# SPARAM\_LP

## Low-Power Single-Port Asynchronous Static RAM

### Reference Table

\* For Ymux=8 (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.26	4.37	4.70	4.86	5.13	5.35	5.56	5.83
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	4.21	4.32	4.64	4.81	5.08	5.29	5.51	5.78
t <sub>ah</sub>	1.78	1.79	2.19	2.21	2.61	2.63	3.03	3.05
t <sub>wh</sub>	4.21	4.32	4.64	4.81	5.08	5.29	5.51	5.78
t <sub>ds</sub>	0.10	0.18	0.13	0.27	0.12	0.30	0.07	0.28
t <sub>dh</sub>	0.64	0.58	0.73	0.63	0.83	0.69	0.92	0.75
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.21	1.34	1.30	1.49	1.40	1.64	1.49	1.79
t <sub>wen</sub>	2.96	3.16	3.33	3.62	3.70	4.07	4.07	4.53
t <sub>acc</sub>	4.26	4.37	4.70	4.86	5.13	5.35	5.56	5.83
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.26	1.39	1.35	1.54	1.45	1.69	1.54	1.83
t <sub>dz</sub>	0.32	0.32	0.37	0.37	0.42	0.42	0.47	0.47
t <sub>zd</sub>	0.26	0.26	0.31	0.31	0.37	0.37	0.42	0.42
t <sub>od</sub>	0.42	0.42	0.48	0.48	0.53	0.53	0.58	0.58
Power (μW/MHz)								
Power_read	89.72	112.08	154.81	200.04	222.74	299.30	293.53	409.88
Power_write	136.41	153.87	261.39	306.79	423.69	510.31	623.29	764.42
Power_standby	13.54	23.41	23.38	41.44	33.28	62.12	43.24	85.43
Area (μm)								
Width	831.84	831.84	1437.28	1437.28	2042.72	2042.72	2648.17	2648.17
Height	529.32	1017.68	853.16	1665.36	1177.00	2313.04	1500.84	2960.72

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## Low-Power Single-Port Asynchronous Static RAM

## Reference Table

\* For Ymux=16

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.30	4.43	4.73	4.92	5.16	5.40	5.60	5.89
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	4.24	4.38	4.68	4.86	5.11	5.35	5.55	5.83
t <sub>ah</sub>	1.78	1.79	2.20	2.21	2.61	2.63	3.03	3.05
t <sub>wh</sub>	4.24	4.38	4.68	4.86	5.11	5.35	5.55	5.83
t <sub>ds</sub>	0.09	0.12	0.14	0.24	0.14	0.30	0.10	0.30
t <sub>dh</sub>	0.59	0.48	0.68	0.53	0.77	0.59	0.87	0.64
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.25	1.40	1.34	1.55	1.43	1.69	1.53	1.84
t <sub>wen</sub>	3.02	3.28	3.40	3.74	3.77	4.19	4.14	4.65
t <sub>acc</sub>	4.30	4.43	4.73	4.92	5.16	5.40	5.60	5.89
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.30	1.45	1.39	1.60	1.48	1.74	1.58	1.89
t <sub>dz</sub>	0.31	0.31	0.35	0.35	0.38	0.38	0.42	0.42
t <sub>zd</sub>	0.25	0.25	0.29	0.29	0.32	0.32	0.36	0.36
t <sub>od</sub>	0.40	0.40	0.44	0.44	0.48	0.48	0.52	0.52
Power (μW/MHz)								
Power_read	69.37	89.23	112.69	148.76	157.46	213.99	203.68	284.91
Power_write	101.53	117.46	171.73	205.67	260.59	319.18	368.11	457.99
Power_standby	11.60	21.92	19.60	36.39	27.63	52.22	35.70	69.41
Area (μm)								
Width	831.84	831.84	1437.28	1437.28	2042.72	2042.72	2648.17	2648.17
Height	529.32	1017.68	853.16	1665.36	1177.00	2313.04	1500.84	2960.72

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



# SPARAM\_LP

## Low-Power Single-Port Asynchronous Static RAM

### Reference Table

\* For Ymux=32 (Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

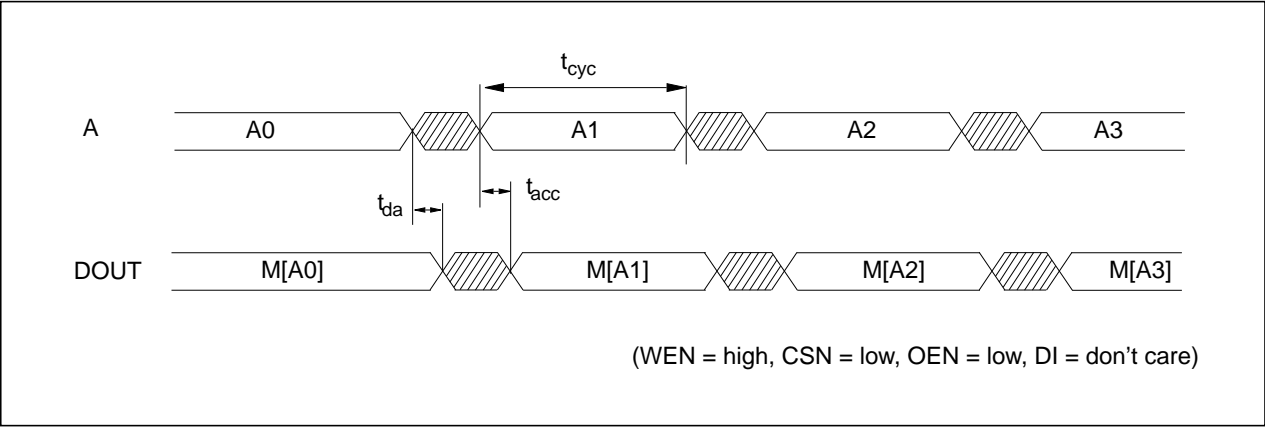
Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	4	4	8	8	12	12	16	16
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.39	4.58	4.81	5.06	5.23	5.53	5.65	6.01
t <sub>as</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>cas</sub>	4.34	4.52	4.76	5.00	5.18	5.47	5.60	5.95
t <sub>ah</sub>	1.77	1.78	2.19	2.21	2.61	2.63	3.03	3.06
t <sub>wh</sub>	4.34	4.52	4.76	5.00	5.18	5.47	5.60	5.95
t <sub>ds</sub>	0.11	0.26	0.18	0.38	0.19	0.48	0.15	0.55
t <sub>dh</sub>	0.49	0.29	0.58	0.34	0.67	0.38	0.77	0.43
t <sub>cs</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>ch</sub>	1.31	1.51	1.40	1.66	1.49	1.81	1.58	4.96
t <sub>wen</sub>	3.16	3.53	3.53	3.98	3.89	4.42	4.25	4.87
t <sub>acc</sub>	4.39	4.58	4.81	5.06	5.23	5.53	5.65	6.01
t <sub>da</sub>	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
t <sub>wda</sub>	0.10	0.10	0.10	0.10	0.10	0.10	0.10	0.10
t <sub>wacc</sub>	1.36	1.57	1.45	1.72	1.54	1.87	1.63	2.01
t <sub>dz</sub>	0.29	0.29	0.34	0.34	0.38	0.38	0.40	0.40
t <sub>zd</sub>	0.23	0.23	0.27	0.27	0.60	0.30	0.34	0.34
t <sub>od</sub>	0.38	0.38	0.44	0.44	0.48	0.48	0.51	0.51
Power (μW/MHz)								
Power_read	57.70	75.79	90.74	121.92	124.49	170.91	158.97	222.74
Power_write	84.02	106.24	127.80	163.74	180.92	233.92	243.37	316.77
Power_standby	11.90	25.70	18.92	38.73	25.95	52.52	32.99	67.00
Area (μm)								
Width	831.84	831.84	1437.28	437.28	2042.72	2042.72	2648.17	2648.17
Height	529.32	1017.68	853.16	1665.36	1177.00	2313.04	1500.84	2960.72

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

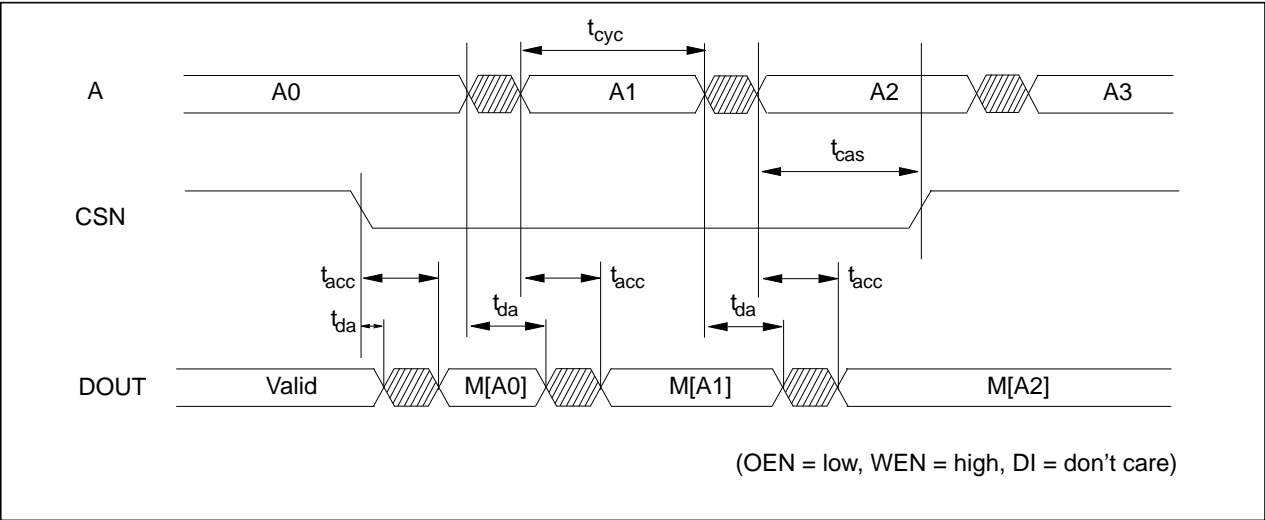


Timing Diagrams

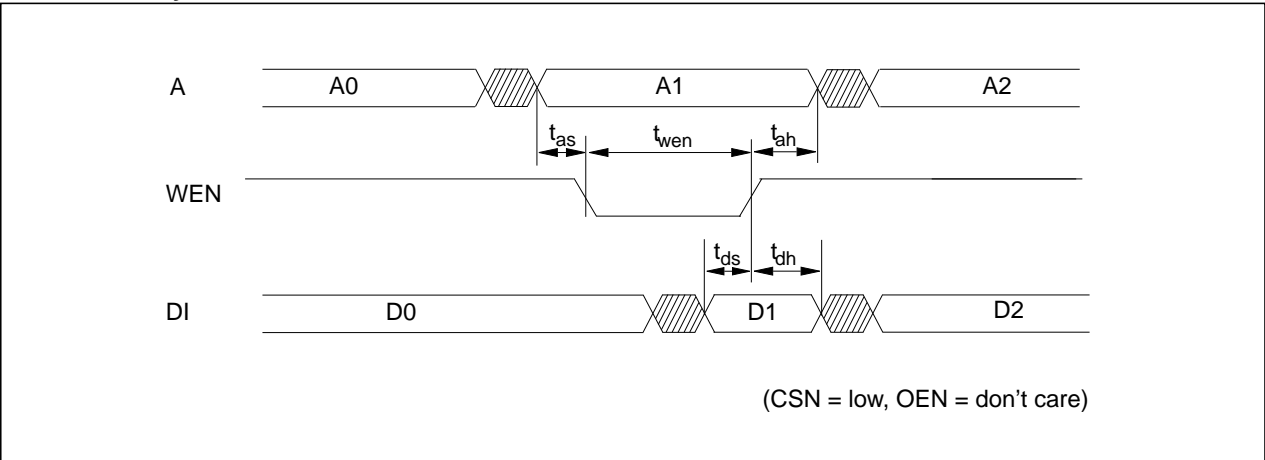
Read Cycle



Read Cycle with CSN-Controlled



Basic Write Cycle

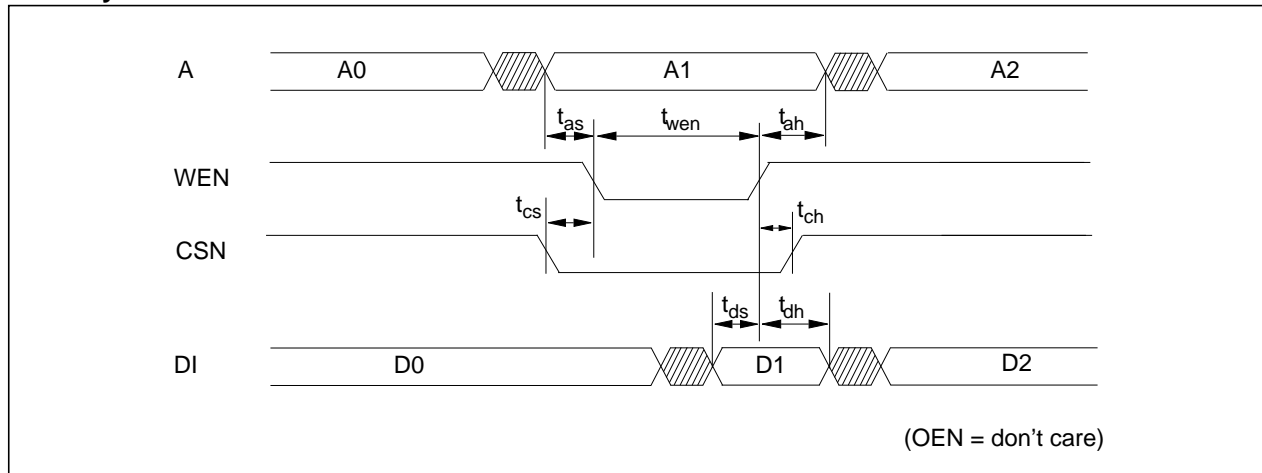




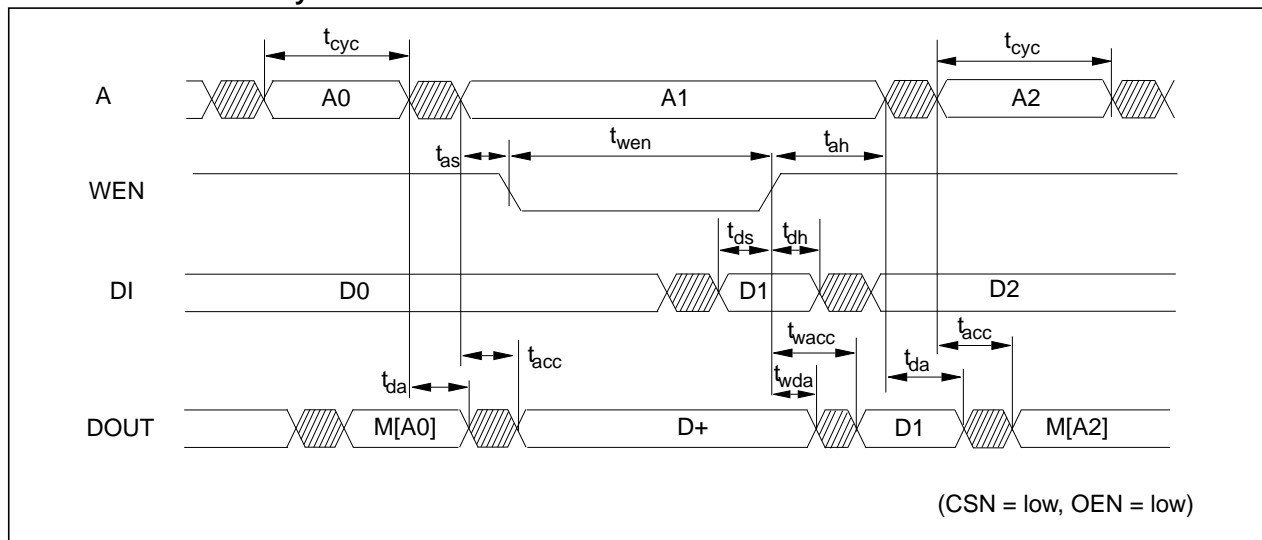
# SPARAM\_LP

## Low-Power Single-Port Asynchronous Static RAM

### Write Cycle with CSN Controlled



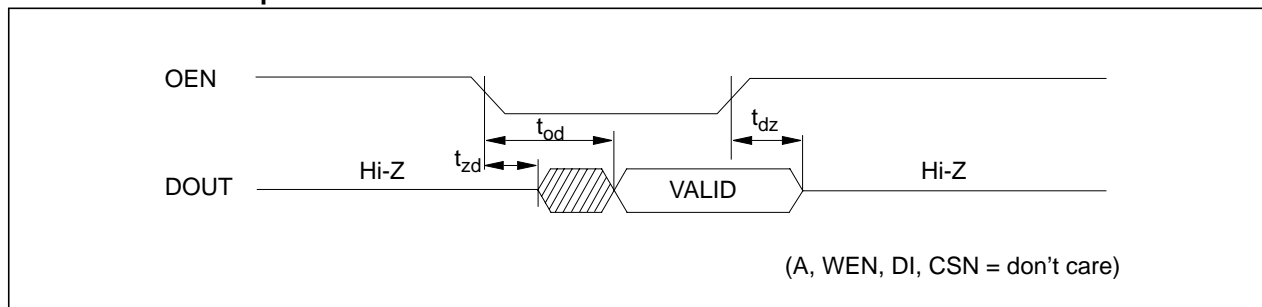
### Read-Modified-Write Cycle



#### NOTES:

1. When the wen hold time after the last address bit transition is satisfied, D+ will toggle in response to a successful read of the initial contents of address A1. When the wen hold time after the last address bit transition is not satisfied, D+ will go to unknown state.
2. Address bits are not allowed to change while WEN is low. If they do change, then the data for one or more addresses in the memory array may be corrupted.

### OEN Controlled Output Enable

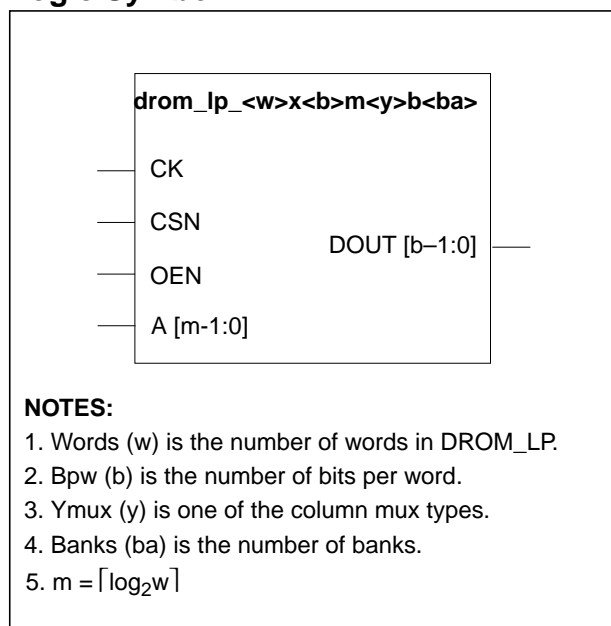


**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## Low-Power Synchronous Diffusion Programmable ROM

### Logic Symbol



### Features

- Suitable for low-power applications
- Diffusion-programmable code available
- Synchronous operation
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down mode available
- Low noise output optimization
- Zero standby current
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

### Function Description

DROM\_LP is a synchronous diffusion programmable ROM which is provided as a compiler. DROM\_LP is intended for use in low-power applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] is disabled and DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

### DROM Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read Cycle

### Parameter Description

DROM\_LP is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y) and Number of banks(ba).



## DROM\_LP

### Low-Power Synchronous Diffusion Programmable ROM

Parameters			YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	ba = 1	Min	64	128	256
		Max	2048	4096	8192
		Step	32	64	128
	ba = 2	Min	128	256	512
		Max	4096	8192	16384
		Step	64	128	256
Bpw (b)		Min	2	2	2
		Max	128	64	32
		Step	1	1	1

### Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

### Pin Capacitance

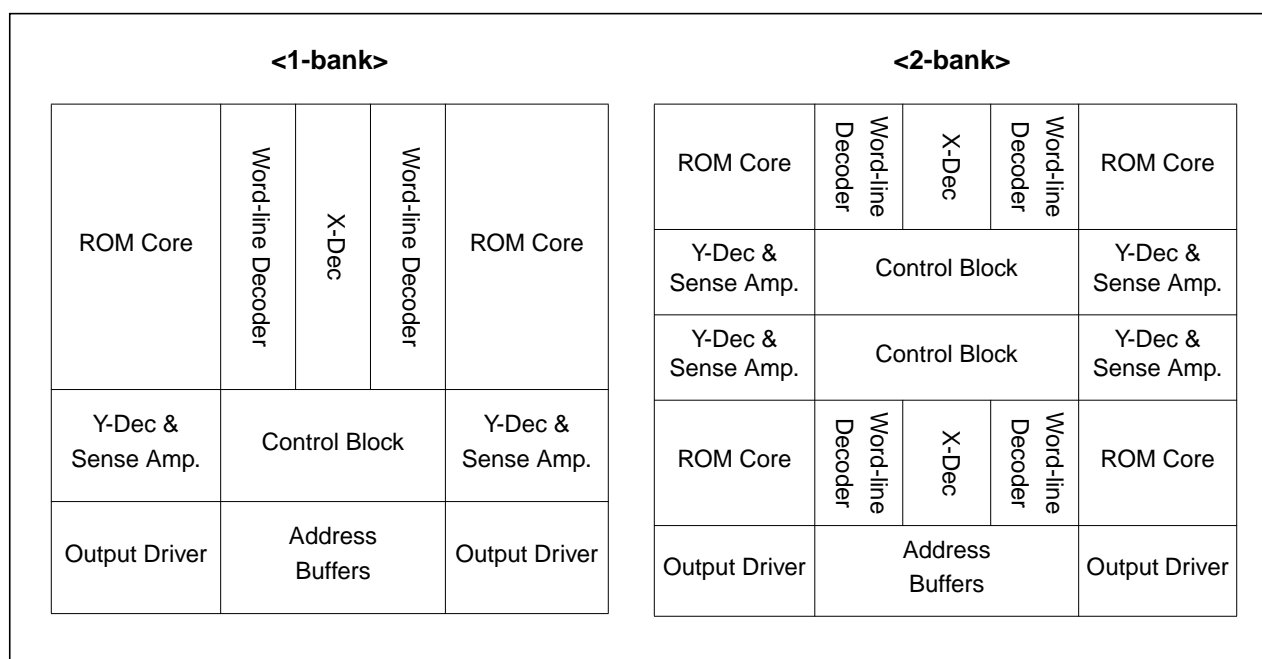
(Unit = SL)

	CK	CSN	OEN	A	DOUT		
					Ymux = 8	Ymux = 16	Ymux = 32
ba = 1	4.581	5.336	3.799	5.623	8.015	8.015	8.015
ba = 2	4.392	4.322	3.050	4.512	8.189	8.189	8.189



## Block Diagrams

DROM\_LP has 2 different physical architectures due to the word depth. For a specific configuration, only one of these architectures is generated from DROM\_LP compiler. Power is consumed by the bank that is selected by the address whereas the other bank will be in idle mode.



## Application Notes

1. Permitting Over-the-cell routing  
In chip-level layout, over-the-cell routing in DROM\_LP is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of DROM\_LP.
4. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## DROM\_LP

### Low-Power Synchronous Diffusion Programmable ROM

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#### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Clock cycle time	tch	CSN hold time from CK rise
tckl	Clock pulse width low	tacc	Data access time
tckh	Clock pulse width high	tda	De-access time
tas	Address setup time	tdz	DOUT drive to high-Z time
tah	Address hold time	tzd	DOUT high-Z to drive time
tcs	CSN setup time	tod	OEN to Valid Output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## Low-Power Synchronous Diffusion Programmable ROM

## Reference Table

\* For Ymux=8

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.79	4.98	6.17	6.39	7.78	8.03	9.64	9.91
t <sub>ckl</sub>	2.02	2.02	2.44	2.44	2.86	2.86	3.26	3.26
t <sub>ckh</sub>	2.11	2.30	2.56	2.78	3.04	3.29	3.54	3.82
t <sub>as</sub>	0.10	1.33	0.10	1.37	0.10	1.41	0.10	1.45
t <sub>ah</sub>	0.69	0.88	0.69	0.91	0.69	0.94	0.69	0.97
t <sub>cs</sub>	0.87	1.23	0.87	1.27	0.87	1.31	0.87	1.35
t <sub>ch</sub>	0.61	0.81	0.61	0.84	0.61	0.87	0.61	0.90
t <sub>acc</sub>	3.37	3.64	3.86	4.17	4.44	4.80	5.11	5.51
t <sub>da</sub>	2.89	3.09	3.47	3.72	4.10	4.37	4.76	5.07
t <sub>dz</sub>	0.67	0.65	0.75	0.74	0.84	0.83	0.92	0.92
t <sub>zd</sub>	0.77	0.76	0.85	0.84	0.93	0.92	1.01	0.99
t <sub>od</sub>	0.90	0.88	0.98	0.97	1.06	1.05	1.14	1.12
Power (μW/MHz)								
Power_read	169.22	179.53	377.62	399.51	641.30	678.26	960.25	1015.80
Power_standby	0.96	4.90	1.07	5.78	1.17	6.64	1.25	7.49
Area (μm)								
Width	511.53	511.53	883.93	883.93	1256.06	1256.06	1627.93	1627.93
Height	214.62	405.22	295.26	566.50	375.90	727.78	456.54	889.06

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## DROM\_LP

### Low-Power Synchronous Diffusion Programmable ROM

#### Reference Table

\* For Ymux=16

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.80	4.99	6.17	6.39	7.78	8.03	9.63	9.91
t <sub>ckl</sub>	2.02	2.02	2.44	2.44	2.86	2.86	3.26	3.26
t <sub>ckh</sub>	2.11	2.31	2.56	2.78	3.04	3.29	3.54	3.82
t <sub>as</sub>	0.10	1.33	0.10	1.37	0.10	1.41	0.10	1.45
t <sub>ah</sub>	0.69	0.88	0.69	0.91	0.69	0.94	0.69	0.97
t <sub>cs</sub>	0.87	1.23	0.87	1.27	0.87	1.31	0.87	1.35
t <sub>ch</sub>	0.61	0.81	0.61	0.84	0.61	0.87	0.61	0.90
t <sub>acc</sub>	3.42	3.71	3.91	4.25	4.48	4.87	5.15	5.58
t <sub>da</sub>	2.90	3.11	3.48	3.73	4.11	4.39	4.77	5.08
t <sub>dz</sub>	0.63	0.63	0.70	0.69	0.76	0.75	0.82	0.81
t <sub>zd</sub>	0.74	0.73	0.80	0.79	0.86	0.84	0.91	0.90
t <sub>od</sub>	0.87	0.86	0.93	0.92	0.99	0.97	1.04	1.03
Power (μW/MHz)								
Power_read	121.24	130.01	156.66	273.76	421.02	438.26	614.32	653.51
Power_standby	0.96	4.89	1.05	5.75	1.14	6.61	1.21	7.46
Area (μm)								
Width	511.24	511.24	883.86	883.86	1256.06	1256.06	1627.86	1627.86
Height	214.62	405.22	295.26	566.50	375.90	727.78	456.54	889.06

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## Low-Power Synchronous Diffusion Programmable ROM

## Reference Table

\* For Ymux=32

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	4.80	4.99	6.17	6.39	7.78	8.03	9.64	9.92
t <sub>ckl</sub>	2.02	2.02	2.44	2.44	2.86	2.86	3.26	3.26
t <sub>ckh</sub>	2.12	2.31	2.56	2.78	3.04	3.29	3.55	3.82
t <sub>as</sub>	0.10	1.33	0.10	1.37	0.10	1.41	0.10	1.45
t <sub>ah</sub>	0.68	0.88	0.68	0.91	0.68	0.94	0.68	0.97
t <sub>cs</sub>	0.87	1.23	0.87	1.27	0.87	1.31	0.87	1.35
t <sub>ch</sub>	0.61	0.81	0.61	0.84	0.61	0.87	0.61	0.90
t <sub>acc</sub>	3.49	3.85	3.98	4.39	4.55	5.01	5.22	5.72
t <sub>da</sub>	2.91	3.13	3.50	3.75	4.12	4.41	4.78	5.10
t <sub>dz</sub>	0.62	0.61	0.67	0.66	0.72	0.71	0.76	0.75
t <sub>zd</sub>	0.73	0.72	0.77	0.76	0.82	0.81	0.86	0.85
t <sub>od</sub>	0.85	0.84	0.90	0.86	0.95	0.93	0.99	0.98
Power (μW/MHz)								
Power_read	97.93	105.95	197.49	212.21	312.62	334.97	443.33	474.24
Power_standby	0.95	4.89	1.04	5.76	1.12	6.63	1.19	7.50
Area (μm)								
Width	510.65	510.65	883.69	883.69	1256.06	1256.06	1627.76	1627.76
Height	214.61	405.22	295.26	566.50	375.90	727.78	456.54	889.06

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

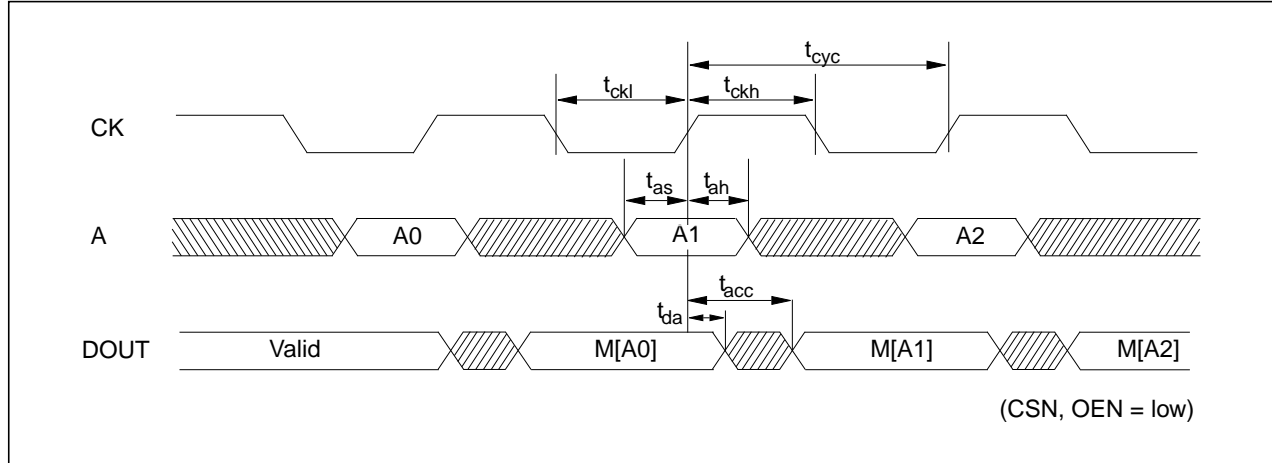


## DROM\_LP

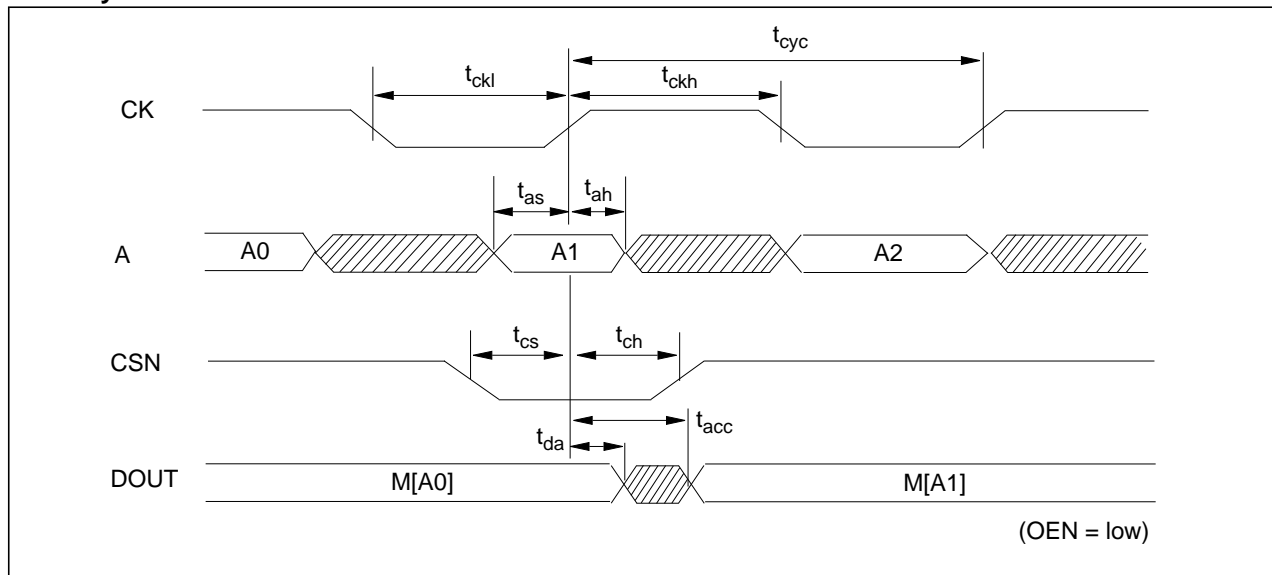
### Low-Power Synchronous Diffusion Programmable ROM

#### Timing Diagrams

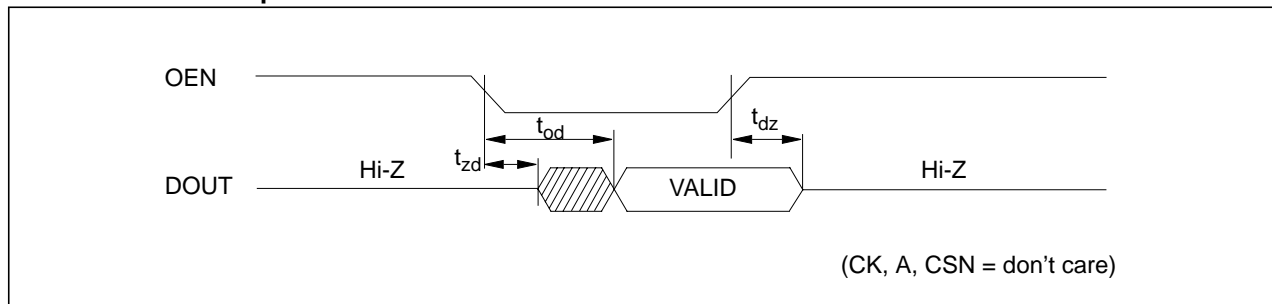
##### Read Cycle



##### Read Cycle with CSN Controlled



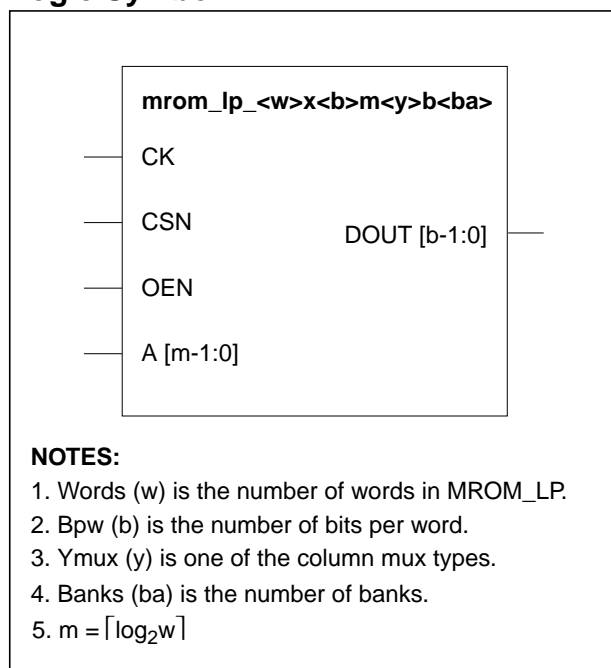
##### OEN Controlled Output Enable



**NOTE:** "don't care" means the condition that these pins are in normal operation mode.



## Logic Symbol



## Features

- Suitable for low-power applications
- Metal-2 programmable code available
- Synchronous operation
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down mode
- Low noise output optimization
- Zero standby current
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

## Function Description

MROM\_LP is a synchronous diffusion programmable ROM which is provided as a compiler. MROM\_LP is intended for use in low-power applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] is disabled and DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

## MROM Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read Cycle



## MROM\_LP

### Low-Power Synchronous Metal Programmable ROM

#### Parameter Description

MROM\_LP is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba).

Parameters			YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	ba = 1	Min	64	128	256
		Max	2048	4096	8192
		Step	32	64	128
	ba = 2	Min	128	256	512
		Max	4096	8192	16384
		Step	64	128	256
Bpw (b)		Min	2	2	2
		Max	128	64	32
		Step	1	1	1

#### Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

#### Pin Capacitance

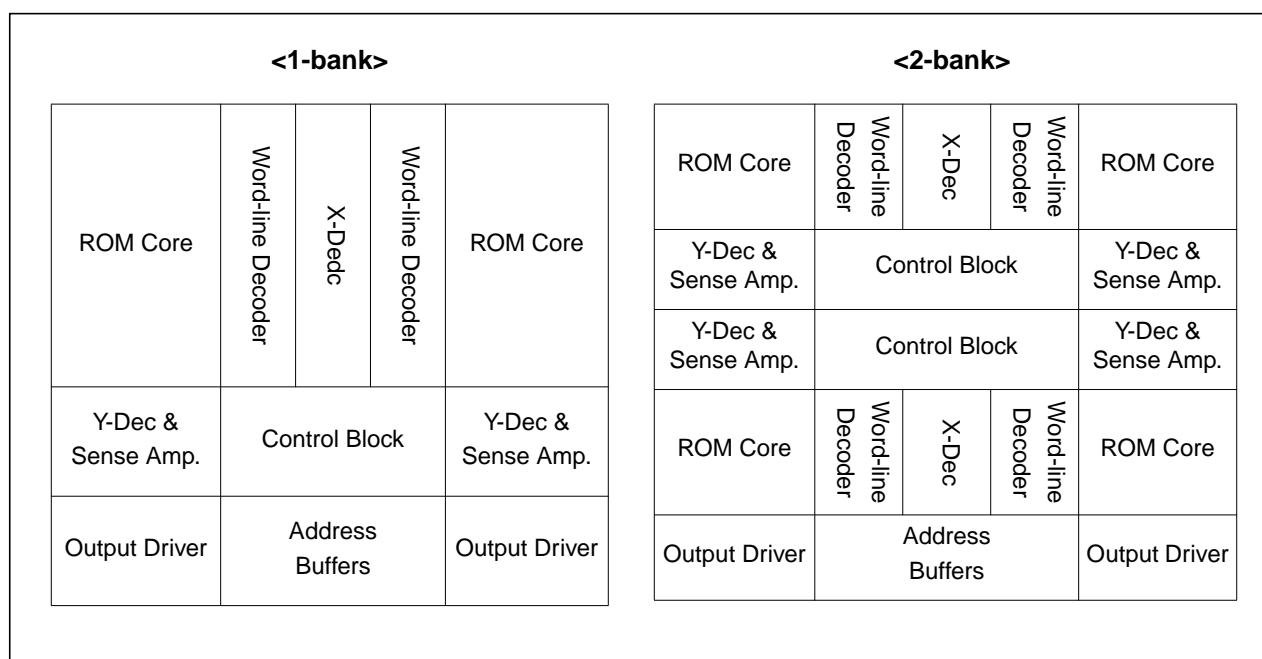
(Unit = SL)

	CK	CSN	OEN	A	DOUT		
					Ymux = 8	Ymux = 16	Ymux = 32
ba = 1	4.346	4.741	3.257	7.865	8.308	8.308	8.308
ba = 2	5.190	5.288	3.405	4.614	8.463	8.463	8.463



## Block Diagrams

MROM\_LP has 2 different physical architectures due to the word depth. For a specific configuration, only one of these architectures is generated from MROM\_LP compiler. Power is consumed by the bank that is selected by the address whereas the other bank will be in idle mode.



## Application Notes

1. Permitting over-the-cell routing  
In chip-level layout, over-the-cell routing in MROM\_LP is permitted for only Metal-5 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of MROM\_LP.
4. Power reduction during standby mode.  
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while standby mode.



## MROM\_LP

### Low-Power Synchronous Metal Programmable ROM

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#### Characteristics

Definition for AC Timing (ns)			
Symbol	Description	Symbol	Description
tcyc	Clock cycle time	tch	CSN hold time from CK rise
tckl	Clock pulse width low	tacc	Data access time
tckh	Clock pulse width high	tda	De-access time
tas	Address setup time	tdz	DOUT drive to high-Z time
tah	Address hold time	tzd	DOUT high-Z to drive time
tcs	CSN setup time	tod	OEN to Valid Output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		



## Low-Power Synchronous Metal Programmable ROM

## Reference Table

\* For Ymux=8

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	512	1024	1024	2048	1536	3072	2048	4096
bpw	32	32	64	64	96	96	128	128
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	5.73	5.95	8.43	8.71	11.31	11.64	14.36	14.74
t <sub>ckl</sub>	2.15	2.15	2.72	2.72	3.24	3.24	3.72	3.72
t <sub>ckh</sub>	2.27	2.49	2.87	3.15	3.53	3.86	4.23	4.62
t <sub>as</sub>	0.10	1.34	0.10	1.41	0.10	1.48	0.10	1.55
t <sub>ah</sub>	0.65	0.87	0.65	0.92	0.65	0.98	0.65	1.03
t <sub>cs</sub>	0.84	1.24	0.84	1.31	0.84	1.38	0.84	1.45
t <sub>ch</sub>	0.58	0.80	0.58	0.86	0.58	0.91	0.58	0.97
t <sub>acc</sub>	3.55	3.84	4.28	4.64	5.12	5.55	6.07	6.57
t <sub>da</sub>	3.11	3.34	3.93	4.22	4.80	5.16	5.73	6.14
t <sub>dz</sub>	0.63	0.63	0.72	0.72	0.81	0.81	0.89	0.90
t <sub>zd</sub>	0.74	0.74	0.82	0.83	0.90	0.91	0.98	0.99
t <sub>od</sub>	0.86	0.87	0.95	0.96	1.03	1.04	1.11	1.12
Power (μW/MHz)								
Power_read	198.36	207.26	475.39	496.65	848.69	885.97	1318.24	1375.22
Power_standby	0.97	5.58	1.07	7.17	1.17	8.77	1.25	10.36
Area (μm)								
Width	484.49	484.49	876.09	876.09	1267.42	1267.42	1658.49	1658.49
Height	275.80	529.46	419.16	816.18	562.52	1102.90	705.88	1389.62

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## MROM\_LP

### Low-Power Synchronous Metal Programmable ROM

#### Reference Table

\* For Ymux=16

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	1024	2048	2048	4096	3072	6144	4096	8192
bpw	16	16	32	32	48	48	64	64
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	5.74	5.96	8.43	8.71	11.31	11.64	14.36	14.75
t <sub>ckl</sub>	2.15	2.15	2.72	2.72	3.24	3.24	3.72	3.72
t <sub>ckh</sub>	2.27	2.49	2.87	3.15	3.53	3.86	4.23	4.62
t <sub>as</sub>	0.10	1.34	0.10	1.41	0.10	1.48	0.10	1.55
t <sub>ah</sub>	0.65	0.87	0.65	0.92	0.65	0.98	0.65	1.03
t <sub>cs</sub>	0.85	1.24	0.85	1.31	0.85	1.38	0.85	1.45
t <sub>ch</sub>	0.58	0.80	0.58	0.86	0.58	0.91	0.58	0.97
t <sub>acc</sub>	3.59	3.91	4.32	4.72	5.16	5.62	6.11	6.64
t <sub>da</sub>	3.12	3.36	3.94	4.24	4.81	5.17	5.74	6.16
t <sub>dz</sub>	0.60	0.60	0.66	0.67	0.72	0.73	0.78	0.79
t <sub>zd</sub>	0.71	0.71	0.77	0.77	0.82	0.83	0.88	0.89
t <sub>od</sub>	0.84	0.84	0.90	0.90	0.95	0.96	1.01	1.01
Power (μW/MHz)								
Power_read	135.73	145.00	307.50	325.72	529.17	558.24	800.72	842.55
Power_standby	0.96	5.57	1.05	7.15	1.13	8.73	1.20	10.30
Area (μm)								
Width	484.20	484.20	876.02	876.02	1267.42	1267.42	1658.42	1658.42
Height	275.80	529.46	419.16	816.18	562.52	1102.90	705.88	1389.62

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.



## Low-Power Synchronous Metal Programmable ROM

## Reference Table

\* For Ymux=32

(Typical process, 2.5V, 25°C, Output load = 10SL, Input slope = 0.2 ns)

Parameters								
words	2048	4096	4096	8192	6144	12288	8192	16384
bpw	8	8	16	16	24	24	32	32
ba	1	2	1	2	1	2	1	2
Timing (ns)								
t <sub>cyc</sub>	5.74	5.96	8.43	8.70	11.30	11.63	14.36	14.74
t <sub>ckl</sub>	2.15	2.15	2.72	2.71	3.24	3.23	3.72	3.71
t <sub>ckh</sub>	2.27	2.49	2.87	3.15	3.53	3.86	4.23	4.62
t <sub>as</sub>	0.10	1.34	0.10	1.41	0.10	1.48	0.10	1.55
t <sub>ah</sub>	0.65	0.87	0.65	0.92	0.65	0.98	0.65	1.04
t <sub>cs</sub>	0.85	1.24	0.85	1.31	0.85	1.38	0.85	1.45
t <sub>ch</sub>	0.58	0.80	0.58	0.86	0.58	0.91	0.58	0.97
t <sub>acc</sub>	3.67	4.05	4.40	4.85	5.24	5.76	6.18	6.77
t <sub>da</sub>	3.13	3.38	3.95	4.26	4.83	5.19	5.76	6.18
t <sub>dz</sub>	0.59	0.59	0.63	0.64	0.68	0.68	0.72	0.73
t <sub>zd</sub>	0.70	0.70	0.74	0.74	0.78	0.79	0.83	0.83
t <sub>od</sub>	0.82	0.83	0.87	0.87	0.91	0.92	0.95	0.96
Power (μW/MHz)								
Power_read	106.53	115.07	226.29	242.14	372.56	396.68	545.33	578.71
Power_standby	0.95	5.57	1.04	7.16	1.12	8.76	1.18	10.37
Area (μm)								
Width	483.61	483.61	875.85	875.85	1267.42	1267.42	1658.32	1658.32
Height	275.80	529.46	419.16	816.18	562.52	1102.90	705.88	1389.62

**NOTE:** Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode.

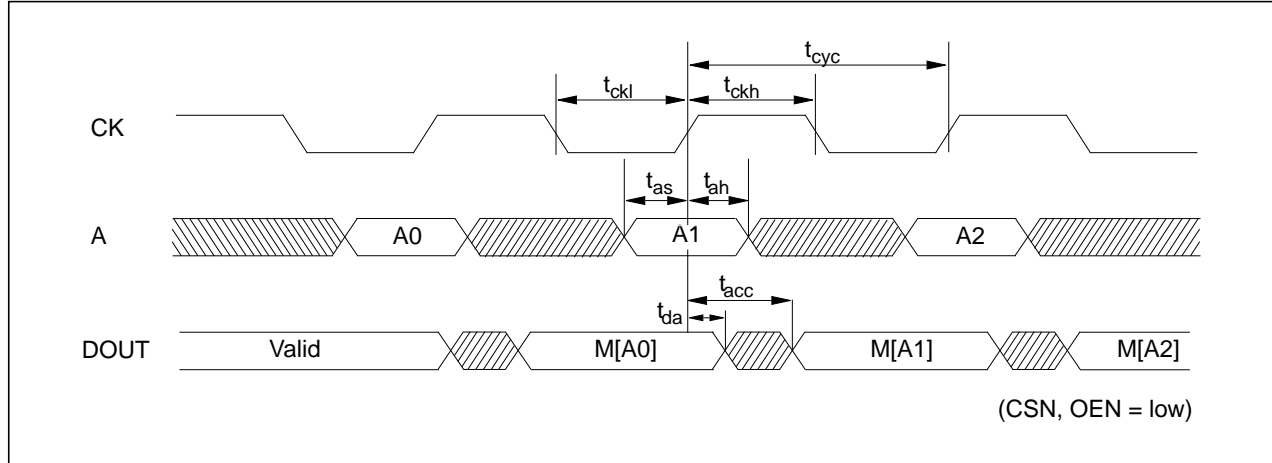


## MROM\_LP

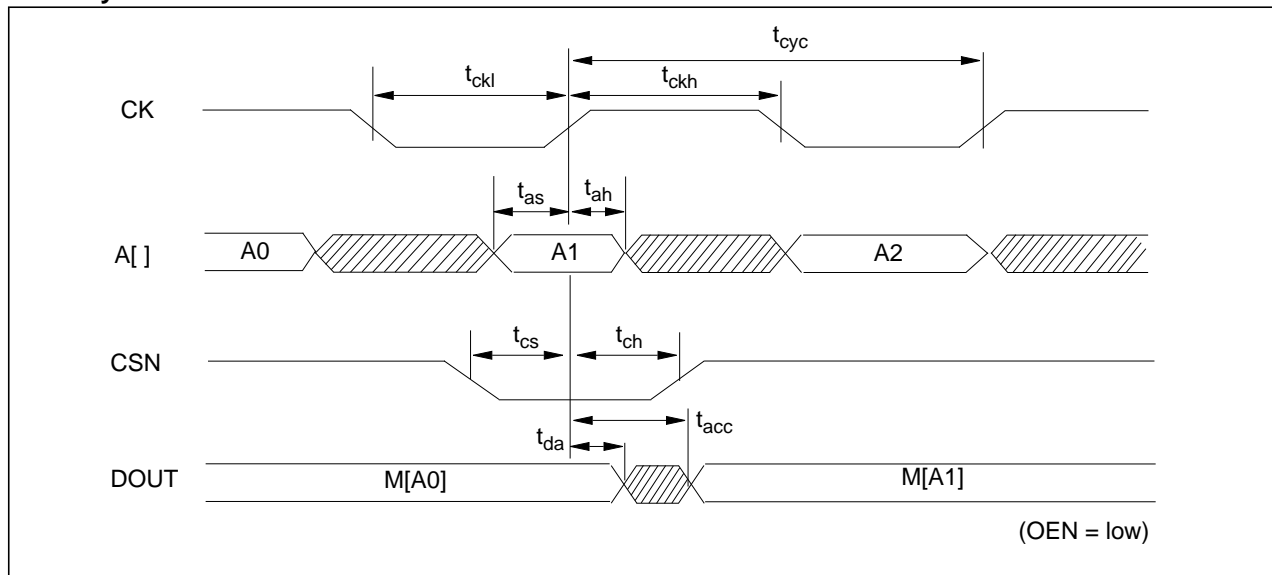
### Low-Power Synchronous Metal Programmable ROM

#### Timing Diagrams

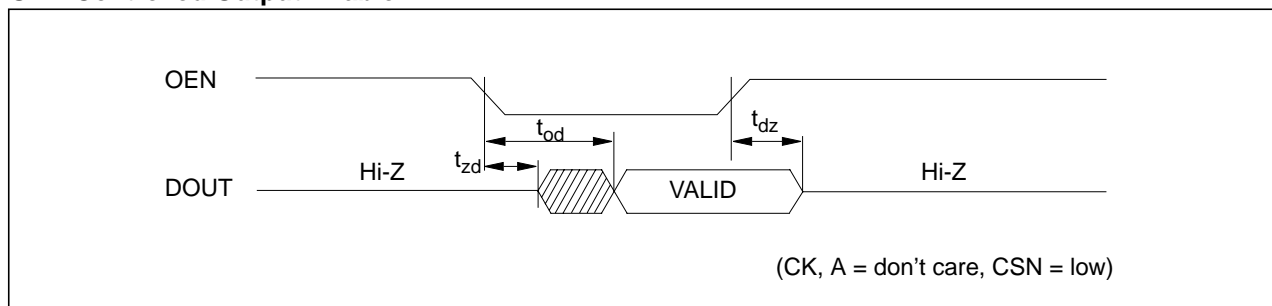
##### Read Cycle



##### Read Cycle with CSN Controlled



##### OEN Controlled Output Enable



**NOTE:** "don't care" means the condition that these pins are in normal operation mode



## COMPILED DATAPATH MACROCELLS

Datapath macrocell is a set of high-level elements that enable more efficient datapath implementation. These macrocells include adder, subtracter, barrel shifter and multiplier elements. Currently, all of these cells can be used anywhere in the design; they are not limited to datapath. Compiled datapath macrocell creates area-optimized and speed-optimized adders, subtracters, ALUs, barrel shifters, booth multipliers and multi-port asynchronous register files based on user specification. It creates logic and layout models for simulation, verification and layout based on the required number of bits, the driving strength, number of multiplier and multiplicand, and so on. We summarized some features of compiled datapath macrocell as follows:

- Dense datapath layout block generation with modularity and topological regularity
- Over-the-cell routing
- Parasitic generation for back-annotation

## DATAPATH MODULE DESIGN FLOW

Today, the implementation of datapath module is one of the most critical and important elements in keeping optimum system performance; especially, digital signal processing (DSP) applications, such as image processing, graphic controlling and CPU-intensive operation, and so on. Since such systems tend to have datapath modules that include the majority of entire design, performance, area and power of these datapath modules are more significant. It means that the datapath module design becomes much more important because these datapath modules effect the overall design performance.

Samsung's datapath module design flow is tightly integrated into netlist-based design flow extracted from Schematic Entry or Synthesis tool. By supporting an easy-to-use ASIC environment and keeping full custom-like density, power and performance, it improves the application-specific integrated circuit (ASIC) designer's productivity.

As one of the most important elements in system performance, optimal datapath module placement is a key point because the datapath design has a topological regular structure and strong modularity. With keeping an optimal datapath module placement, it can maximize density, maximize performance, minimize power requirements in the function of the silicon, and improve design-cycle time.

Fig. 5-3 illustrates the design environment that has been developed to support the datapath design flow and how to fit datapath modules into this flow. This flow is tightly integrated from Verilog, Cadence to Aquarius, Avant!. With the datapath module design flow, it automatically places and routes circuits that have an inherently regular structure. It differs from a standard cell placement and routing tool in that it enables you to map regularity from a logic design into a layout. You can get area-optimized and performance-optimized layouts.



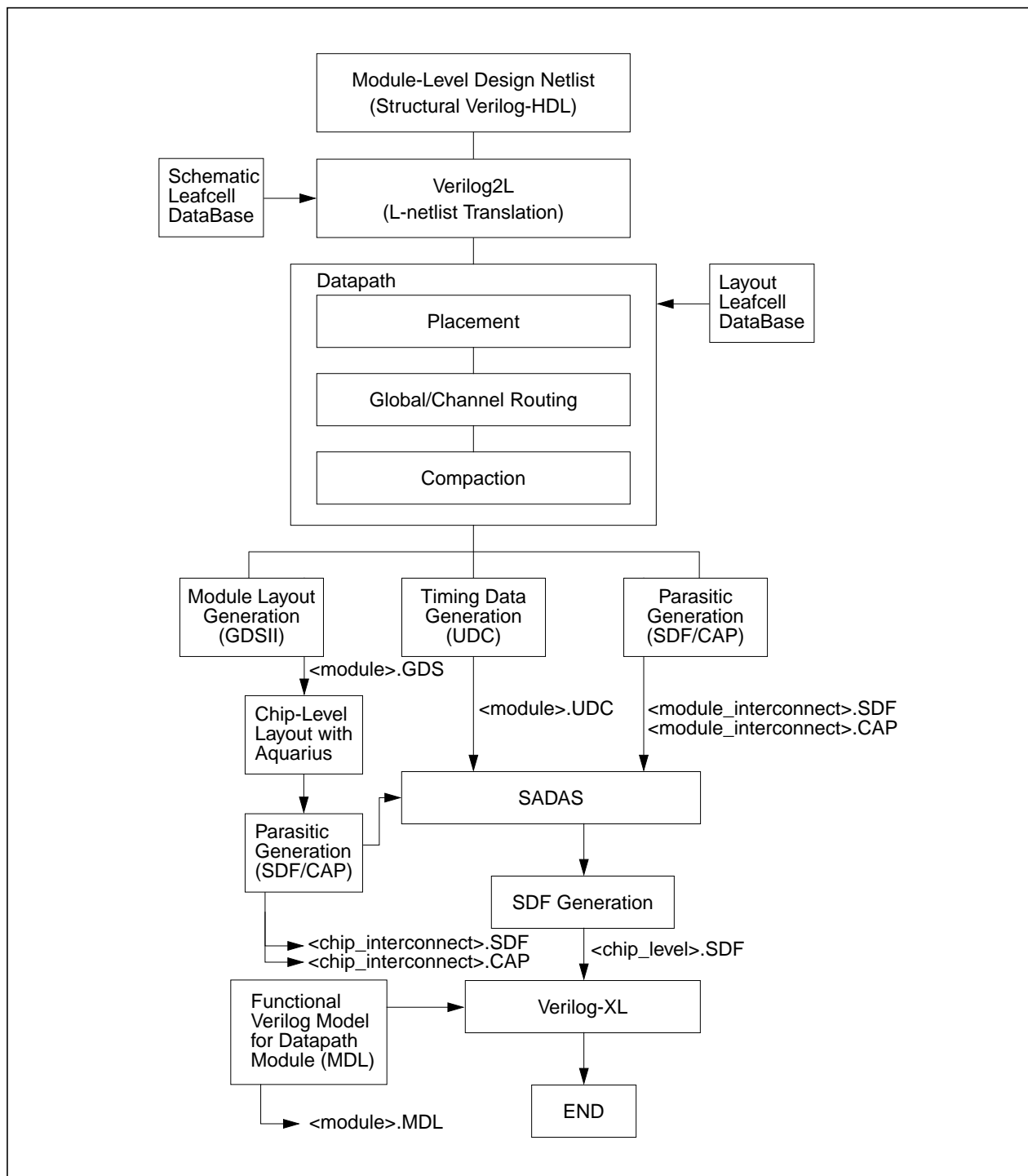


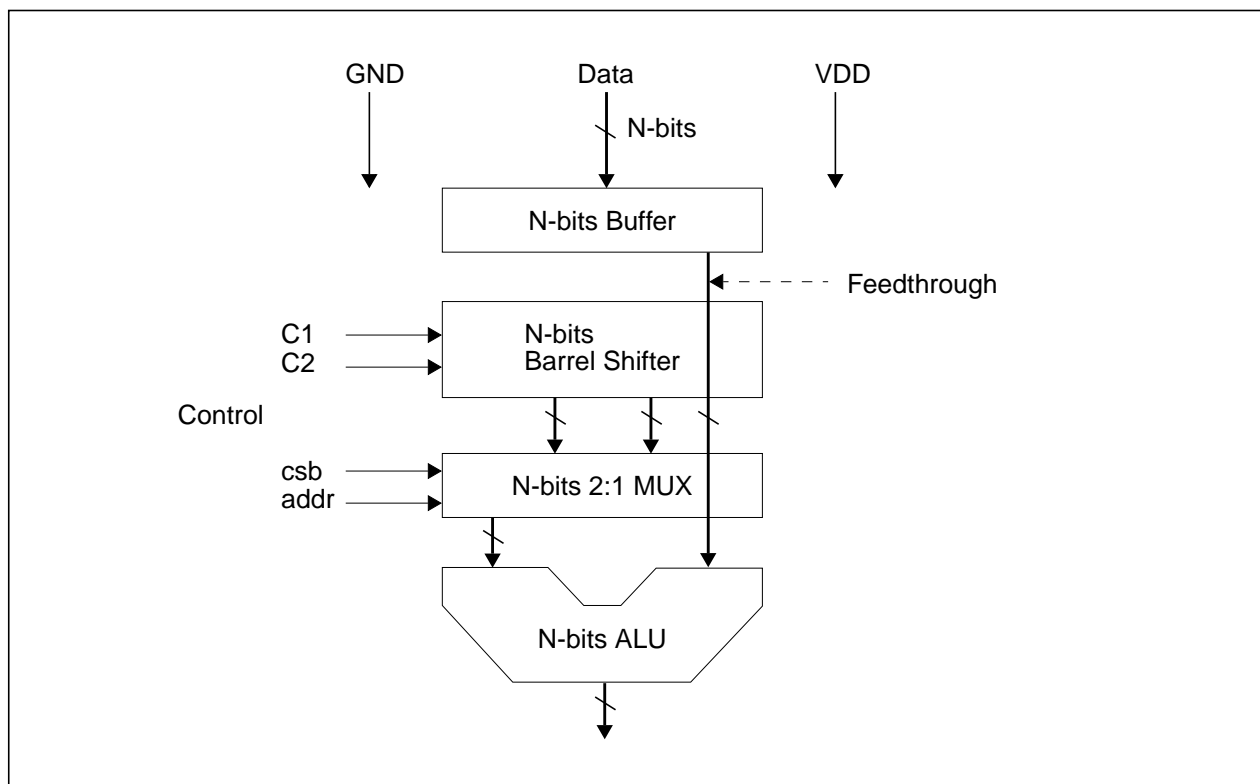
Figure 5-3. Datapath Module Design Flow

**NOTES:**

- Verilog-XL the trademark of Cadence
- Datapath the trademark of Mentor Graphics Co.
- Aquarius the trademark of Avant!
- SADAS the trademark of Samsung



Fig. 5-4 illustrates the typical topology of datapath module design. The datapath layout is a two-dimensional array of rows and columns with routing channels between the rows. The orientation of bits and words with respect to rows and columns defines the datapath layout topology. Feedthrough terminals are the locations on a datapath cell where the datapath router can cross the row without connecting to the cell. Feedthrough terminals can be built into the cell. That is, the cell contains a vertical wire which is not connected to the internal of the cell. Also they can be located where there is sufficient room to route a wire vertically over the cell.



**Figure 5-4. Typical topology of datapath module design**

Currently we provide engineering design services to develop datapath module design with the above flow. For more detailed information regarding the datapath module design, please contact your local representative or headquarter.



## SELECTION GUIDE FOR COMPILED DATAPATH MACROCELLS

Cell Name	Description
ADDER	4-to-64 bit Addition/Subtraction - Ripple-carry/Group-bypass carry scheme - 2's Complement overflow
BS	4-to-64 bit Barrel Shifter - Transmission Gate Multiplexing Scheme - Bi-directional Shift or Rotation - Fill for Vacant bits with Data
MPY	6-to-64 bit Modified Booth Multiplier - 2's Complement Multiplication - Accumulation Scheme - Pipelined Architecture Scheme

### REMARK:

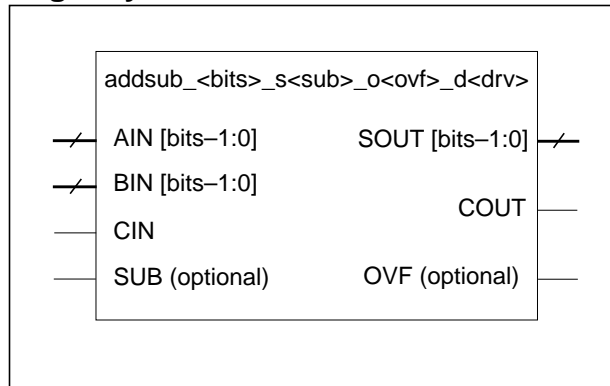
Samsung provides engineering design services to develop additional datapath macrocells. Examples of macrocells that can be developed include:

ADDERSAT	- 4 to 64 bit adder with saturating flag
CMP	- 4 to 64 bit comparator with <, >, <= or >=
DEC/INC	- 4 to 64 bit decrementer / incrementer
ENC	- 4 to 64 bit priority encoder with detection from MSB or LSB
FMPY	- 8 to 64 bit modified Wallace-Tree Multiplier
NORM	- 4 to 64 bit normalizer
ONED/ZEROD	- 4 to 64 bit One detector and Zero detector
PARITY	- 4 to 64 bit odd/even parity generator
PRIMITIVES	- 4 to 64 bit 14 kinds of primitive-level macrocells such as ao/oa, buf/inv, nand/and, nor/or, xor/xnor, tristate-inv/buf, mux, dff, latch etc.

For more detailed information regarding to the above macrocells, contact your local representative or headquarter.



### Logic Symbol



### Features

- Asynchronous operation
- 4 to 64 bit Adder/Subtractor
- High-speed / low-power operation
- 2's complement or unsigned-magnitude operation
- 2's complement overflow flag available
- Sophisticated carry-select and group-bypass scheme
- Two output drive strength available

### Function Description

The ADDER is an  $n$ -bit carry-select adder and subtractor which is provided as a compiler. The ADDER is intended to use in high-speed and low-power applications. It essentially adopts the double carry-select scheme which has hierarchically doubled carry-select groups of bits to allow the high-speed of addition/subtraction operation. And in addition, the inside of each group is designed by a partial group-bypass scheme so as to acquire more high-speed. It performs a 2's complement addition/subtraction or unsigned-magnitude addition. The overflow flag shows the occurrence of overflow while adding two positive or two negative numbers and it should be ignored while doing unsigned-magnitude operations.

### Function Table

Output	Function
SOUT	$AIN + BIN + CIN$ (addition)
	$AIN + \sim BIN + CIN$ (subtraction)
OVF	$(\sim SOUT[bits-1]) \cdot (AIN[bits-1] \cdot BIN[bits-1]) + (SOUT[bits-1]) \cdot (\sim AIN[bits-1]) \cdot (\sim BIN[bits-1])$

### Parameter Description

ADDER is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters.

Parameter Name	Description	Range
bits	Number of bits for the input data bus	4 to 64
sub	0: addition only; 1: addition/subtraction	0/1
ovf	Overflow flag for signed operation	0/1
drv	Output drive strength	1/2



# ADDER

## Adder/Subtractor

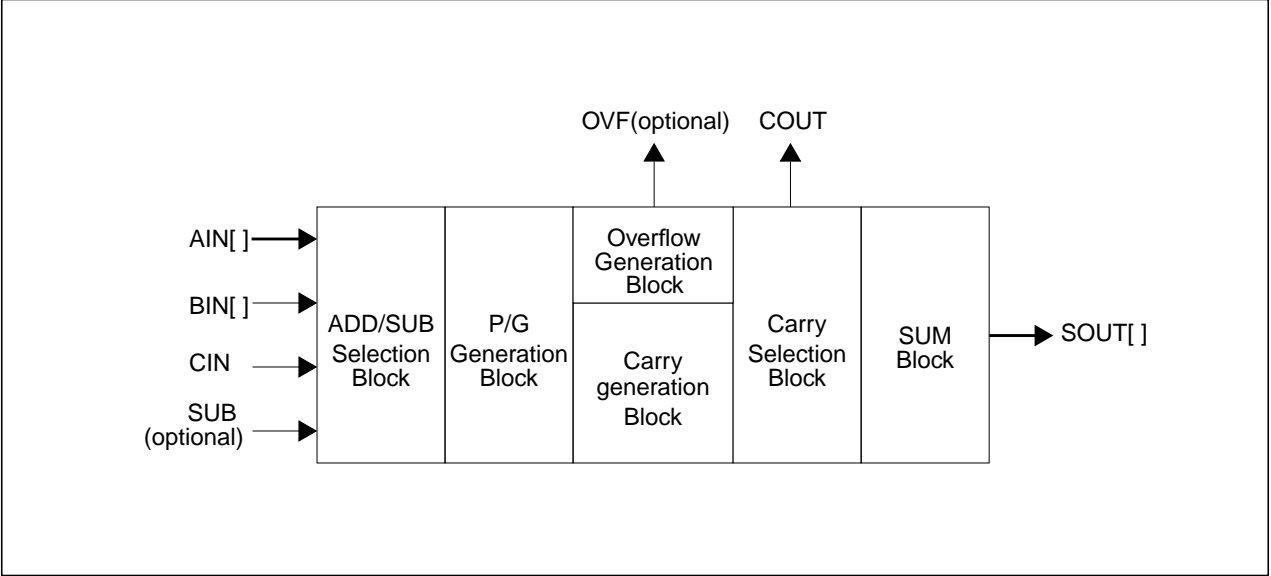
### Pin Description

Name	Type	Description
AIN [ ]	Input	Augend in addition, Minuend in subtraction
BIN [ ]		Addend in addition, Subtrahend in subtraction
CIN		Carry-in in addition/subtraction It must be kept the 'HIGH' state in 2's complement subtraction.
SUB		Addition/subtraction flag (optional when the parameter sub = 1)
SOUT[ ]	output	The result of addition/subtraction
COUT		Carry-out in addition/subtraction
OVF		The overflow/underflow of addition/subtraction (optional when the parameter ovf = 1)

### Pin Capacitance [Unit: pF]

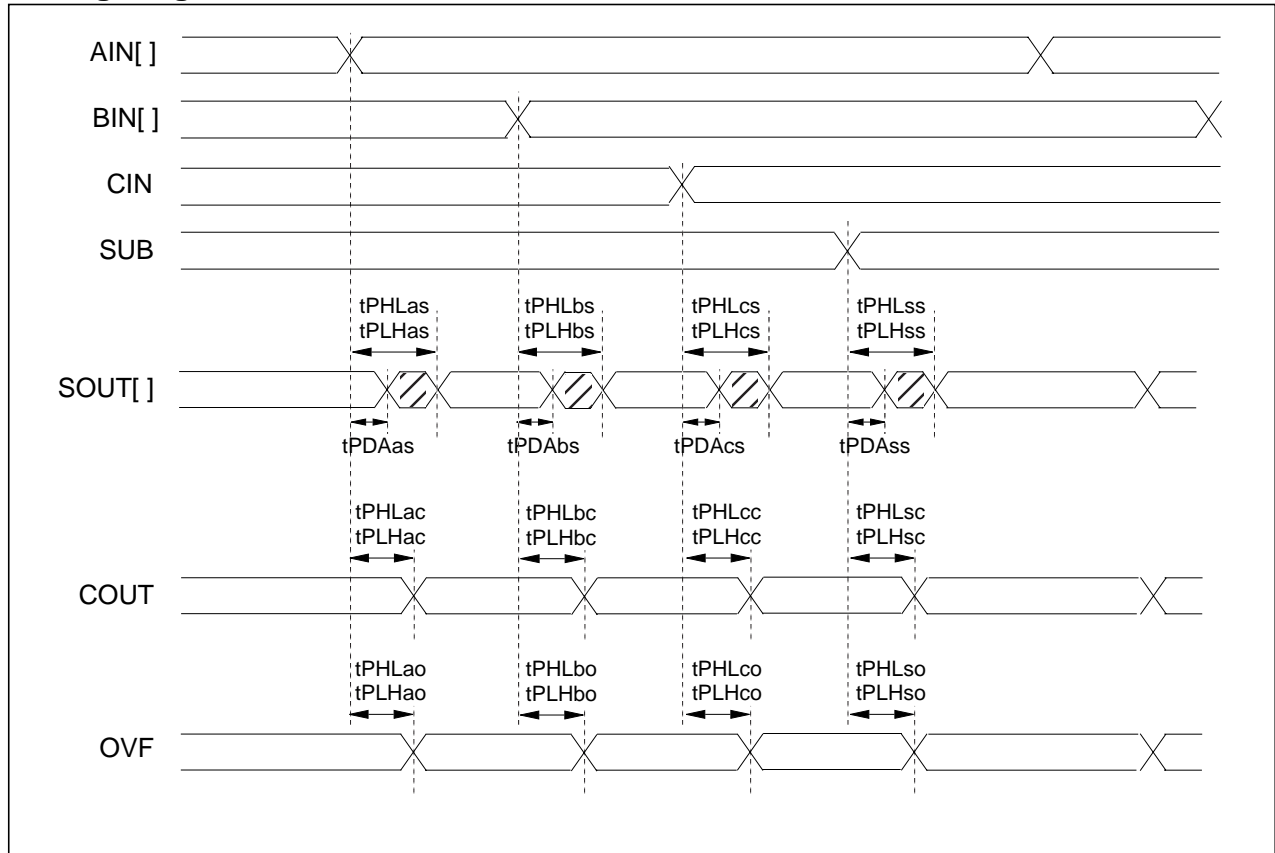
Name	Case	Value
AIN[ ]	all	0.0200
BIN[ ]	sub=0	0.0200
	sub=1	0.0150
CIN	all	0.0349
SUB	sub=1	0.0143 × bits

### Block Diagram





## Timing Diagram



## Timing Type Definition

Timing Type	Definition
$t_{PHLas}/t_{PLHas}$	Propagation delay from AIN[] to SOUT[]
$t_{PHLbs}/t_{PLHbs}$	Propagation delay from BIN[] to SOUT[]
$t_{PHLcs}/t_{PLHcs}$	Propagation delay from CIN to SOUT[]
$t_{PHLss}/t_{PLHss}$	Propagation delay from SUB to SOUT[]
$t_{PHLac}/t_{PLHac}$	Propagation delay from AIN[] to COUT
$t_{PHLbc}/t_{PLHbc}$	Propagation delay from BIN[] to COUT
$t_{PHLcc}/t_{PLHcc}$	Propagation delay from CIN to COUT
$t_{PHLsc}/t_{PLHsc}$	Propagation delay from SUB to COUT
$t_{PHLao}/t_{PLHao}$	Propagation delay from AIN[] to OVF
$t_{PHLbo}/t_{PLHbo}$	Propagation delay from BIN[] to OVF
$t_{PHLco}/t_{PLHco}$	Propagation delay from CIN to OVF
$t_{PHLso}/t_{PLHso}$	Propagation delay from SUB to OVF
$t_{PDAas}$	De-access time from AIN[] to SOUT[]
$t_{PDAbs}$	De-access time from BIN[] to SOUT[]
$t_{PDACS}$	De-access time from CIN to SOUT[]
$t_{PDAss}$	De-access time from SUB to SOUT[]



# ADDER

## Adder/Subtractor

### Characteristic Reference Table

Symbol	Description	Unit	Symbol	Description	Unit
B	Number of Bits	-	S	Input Slope	ns
V <sub>DD</sub>	Power Supply Voltage	V	SL	Standard Load	-
C <sub>L</sub>	Output Load	SL	SA	Input Switching Activity	-

#### 1) Timing Characteristics [Unit: ns]

(Typical process, 25°C, V<sub>DD</sub>=2.5V, C<sub>L</sub>=10, S=0.2)

Type	8		24		36		48		64	
Case: sub=0, ovf=1, drv=1										
tPHLac/tPLHac	0.98	0.90	1.44	1.47	1.72	1.80	1.93	2.06	2.12	2.27
tPHLbc/tPLHbc	0.95	0.90	1.42	1.47	1.69	1.80	1.91	2.05	2.09	2.27
tPHLcc/tPLHcc	0.67	0.77	1.13	1.33	1.41	1.66	1.62	1.92	1.81	2.13
tPHLao/tPLHao	1.08	1.38	1.74	1.96	2.15	2.33	2.49	2.64	2.84	2.97
tPHLbo/tPLHbo	1.09	1.36	1.74	1.94	2.15	2.30	2.49	2.61	2.85	2.94
tPHLco/tPLHco	0.95	1.07	1.60	1.65	2.01	2.02	2.36	2.33	2.71	2.66
tPHLas/tPLHas	1.14	1.29	1.73	1.80	2.09	2.12	2.38	2.37	2.66	2.63
tPHLbs/tPLHbs	1.14	1.26	1.73	1.77	2.09	2.09	2.38	2.35	2.65	2.60
tPHLcs/tPLHcs	1.00	0.98	1.59	1.49	1.95	1.80	2.24	2.06	2.52	2.32
tPDAas	0.35		0.35		0.35		0.35		0.35	
tPDAbs	0.35		0.35		0.35		0.35		0.35	
tPDACS	0.25		0.25		0.25		0.25		0.25	
Case: sub=1, ovf=1, drv=1										
tPHLac/tPLHac	0.98	0.90	1.45	1.48	1.73	1.82	1.73	1.82	2.14	2.30
tPHLbc/tPLHbc	1.27	1.09	1.74	1.66	2.02	2.00	2.02	2.00	2.44	2.48
tPHLcc/tPLHcc	0.67	0.76	1.14	1.34	1.42	1.68	1.42	1.68	1.83	2.16
tPHLsc/tPLHsc	1.01	1.19	1.07	1.89	1.11	2.30	1.11	2.30	1.13	2.88
tPHLao/tPLHao	1.08	1.37	1.78	1.99	2.19	2.37	2.19	2.37	2.80	2.94
tPHLbo/tPLHbo	1.27	1.67	1.96	2.29	2.37	2.66	2.37	2.66	2.98	3.24
tPHLco/tPLHco	0.96	1.06	1.64	1.69	2.05	2.06	2.05	2.06	2.66	2.63
tPHLso/tPLHso	1.54	1.53	1.60	2.35	1.64	2.84	1.64	2.84	1.75	3.58
tPHLas/tPLHas	1.14	1.29	1.76	1.83	2.14	2.16	2.14	2.16	2.69	2.67
tPHLbs/tPLHbs	1.33	1.58	1.95	2.12	2.32	2.45	2.32	2.45	2.88	2.96
tPHLcs/tPLHcs	1.00	0.98	1.63	1.52	2.00	1.85	2.00	1.85	2.56	2.36
tPHLss/tPLHss	1.41	1.32	2.15	2.06	2.59	2.50	2.59	2.50	3.27	3.17
tPDAas	0.35		0.35		0.35		0.35		0.35	
tPDAbs	0.62		0.62		0.62		0.62		0.62	
tPDACS	0.25		0.25		0.25		0.25		0.25	
tPDAss	0.59		0.59		0.59		0.59		0.59	



### Characteristic Reference Table (Cont.)

#### 2) Power Characteristics [Unit: $\mu\text{W}/\text{MHz}$ ]

(Typical process, 25°C,  $V_{DD}=2.5\text{V}$ ,  $C_L=10$ ,  $S=0.2$ ,  $SA=0.5$ )

Case			8	24	36	48	64
sub=0	ovf=0	drv=1	6.46	20.24	30.35	40.27	53.20
		drv=2	7.32	22.55	33.85	45.04	59.80
	ovf=1	drv=1	6.86	20.35	30.47	40.59	54.09
		drv=2	7.65	22.79	34.15	45.51	60.65
sub=1	ovf=0	drv=1	7.44	25.38	38.43	51.12	67.50
		drv=2	8.30	28.26	42.73	56.78	74.87
	ovf=1	drv=1	7.69	25.73	38.89	51.72	68.33
		drv=2	8.59	28.62	43.19	57.38	75.69

#### 3) Size Characteristics [Unit: $\mu\text{m}$ ]

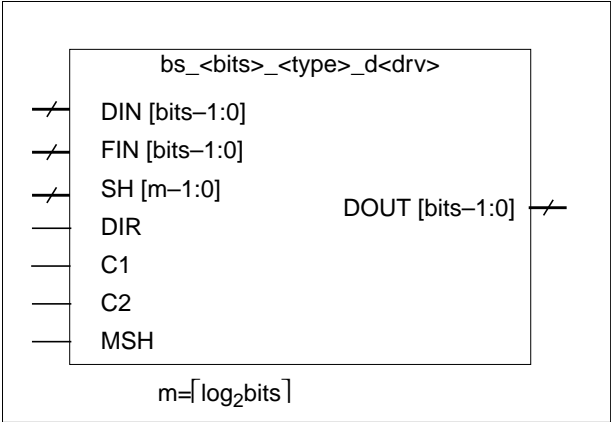
Type	Case	8	24	36	48	64
Width	sub=0 ovf=0	64.79	66.65	67.26	67.22	66.13
	sub=0 ovf=1	66.13	66.75	66.95	66.94	66.58
	sub=1 ovf=0	76.79	78.65	79.26	79.22	78.13
	sub=1 ovf=1	78.13	78.75	78.95	78.94	78.58
Height	all	90.00	266.00	398.00	530.00	706.00



# BS

## Barrel Shifter

### Logic Symbol



### Features

- Asynchronous operation
- 4 to 64 bit Barrel Shifter
- High speed, low power operation
- Transmission gate multiplexing scheme
- Bi-directional shift or rotation
- Fill with zero, MSB, or filler data
- Refresh flag
- Two output drive strength available

### Function Description

The BS is an n-bit barrel shifter which is provided as a compiler. The BS is intended to use in high-speed and low-power applications. It performs a shifting or circular rotation operation and allows both arithmetic and logical shift operations. Also, it can shift and rotate input data in either direction and the direction of the shift can be chosen between MSB (LEFT) and LSB (RIGHT) of the bit string. Logical shifts fill vacant bits with zeros, and arithmetic shifts fill spaces with duplicates of the original MSB. The vacant bits also can be filled with filler data input(FIN). During a right shift, the FIN data fills the vacant bits with data from the LSB of the shift data bus. During a left shift, the shift data bus fills the vacant bits with data from the MSB of the shift data bus (essentially a circular shift).

### Function Table

MSH	DIR	C1	C2	DOUT
0	0	0	0	Shift right and fill with zeros
0	0	0	1	Shift right and fill with MSB of DIN[ ]
0	0	1	0	Shift right and fill with FIN[ ] data
0	0	1	1	Rotate right
0	1	0	0	Shift left and fill with zeros
0	1	0	1	Shift left and fill with MSB
0	1	1	0	Shift left and fill with FIN[ ] data
0	1	1	1	Rotate left
1	X	0	0	All the bits are set to zero
1	X	0	1	All the bits are set to the MSB of DIN[ ]
1	X	1	0	FIN[ ]
1	X	1	1	DIN[ ]

**NOTE:** An 'X' indicates a "don't care" condition.



## Parameter Description

BS is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters.

Parameter Name	Description	Range
bits	Number of bits for the input data bus	4 to 64
type	Direction of shift	BOTH/LEFT/RIGHT
drv	Drive strength	1/2

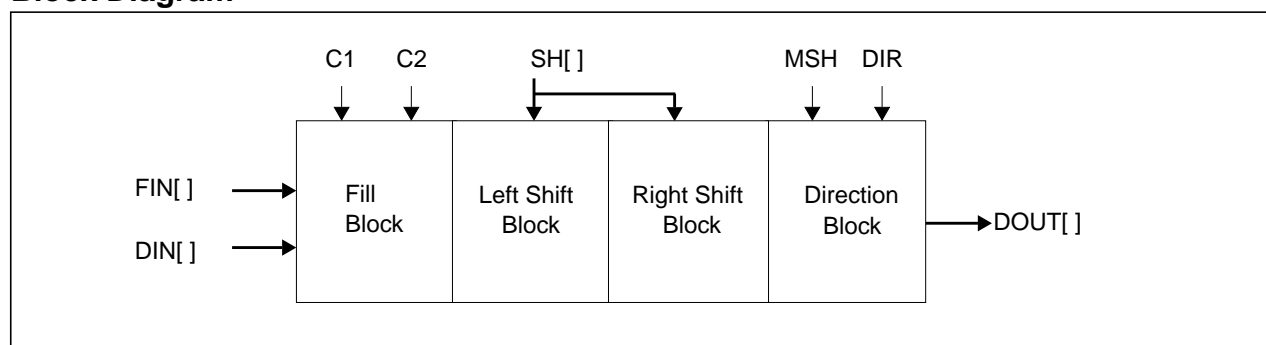
## Pin Description

Name	Type	Description
DIN[ ]	Input	Data input bus
FIN[ ]		Filler data input
DIR		Specify the direction of the shift or rotation (Left/Right) (optional when the parameter type = BOTH)
C1, C2		Specify the filler at the vacant bit (zero/MSB/FIN[ ])
SH[ ]		Shift amount (unsigned-magnitude binary)
MSH		Maximum shift flag. It refreshes all the bits of output data with filler according to C1 and C2.
DOUT[ ]	Output	Data output bus

## Pin Capacitance [Unit: pF]

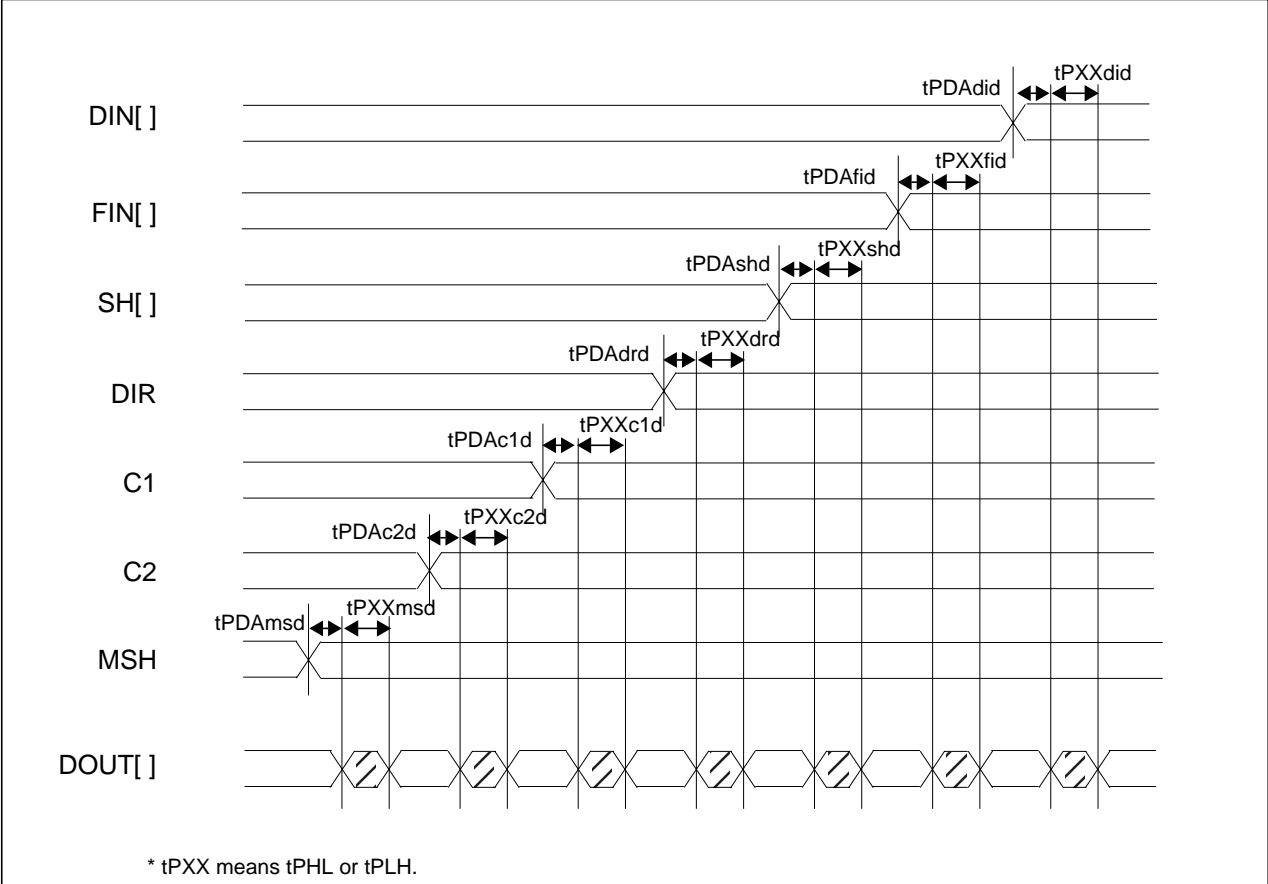
Name	Case	Value
C1	all	0.0155
C2	all	0.0196
FIN[ ]	all	0.0071
MSH	type=BOTH	0.0191
	type=LEFT/RIGHT	0.0263
DIN[ ]	type=BOTH	0.0171
	type=LEFT/RIGHT	0.0157
SH[ ]	type=BOTH	$-0.000003 \cdot \text{bits} \cdot \text{bits} + 0.000017 \cdot \text{bits} + 0.0580$
	type=LEFT/RIGHT	$-0.000002 \cdot \text{bits} \cdot \text{bits} + 0.000009 \cdot \text{bits} + 0.0288$
DIR	type=BOTH	0.0127

## Block Diagram





Timing Diagram



Timing Type Definition

Timing Type	Definition
tPHLdid/tPLHdid	Propagation delay from DIN[ ] to DOUT[ ]
tPHLfid/tPLHfid	Propagation delay from FIN[ ] to DOUT[ ]
tPHLshd/tPLHshd	Propagation delay from SH[ ] to DOUT[ ]
tPHLdrd/tPLHdrd	Propagation delay from DIR to DOUT[ ]
tPHLc1d/tPLHc1d	Propagation delay from C1 to DOUT[ ]
tPHLc2d/tPLHc2d	Propagation delay from C2 to DOUT[ ]
tPHLmsd/tPLHmsd	Propagation delay from MSH to DOUT[ ]
tPDAdid	De-access time from DIN[ ] to DOUT[ ]
tPDAfid	De-access time from FIN[ ] to DOUT[ ]
tPDAshd	De-access time from SH[ ] to DOUT[ ]
tPDAdrd	De-access time from DIR to DOUT[ ]
tPDAc1d	De-access time from C1 to DOUT[ ]
tPDAc2d	De-access time from C2 to DOUT[ ]
tPDAm sd	De-access time from MSH to DOUT[ ]



## Characteristic Reference Tables

Symbol	Description	Unit	Symbol	Description	Unit
B	Number of Bits	-	S	Input Slope	ns
V <sub>DD</sub>	Power Supply Voltage	V	SL	Standard Load	-
C <sub>L</sub>	Output Load	SL	SA	Input Switching Activity	-

## 1) Timing Characteristics [Unit: ns]

(Typical process, 25°C, V<sub>DD</sub>=2.5V, C<sub>L</sub>=10, S=0.2)

Type	8		24		36		48		64	
Case: type=BOTH, drv=1										
tPHLc1d/tPLHc1d	1.55	1.58	1.94	1.96	2.15	2.18	2.29	2.35	2.37	2.49
tPHLc2d/tPLHc2d	1.52	1.56	1.94	2.00	2.18	2.28	2.35	2.52	2.49	2.77
tPHLdid/tPLHdid	1.56	1.48	1.96	1.84	2.19	2.04	2.36	2.17	2.49	2.26
tPHLmsd/tPLHmsd	0.71	0.73	0.82	0.86	0.90	0.96	0.98	1.06	1.08	1.19
tPHLshd/tPLHshd	0.98	0.90	1.13	1.16	1.24	1.36	1.35	1.56	1.51	1.82
tPHLfid/tPLHfid	1.23	1.22	1.52	1.52	1.65	1.66	1.72	1.72	1.71	1.70
tPHLdrd/tPLHdrd	0.62	0.64	0.72	0.77	0.80	0.86	0.87	0.95	0.97	1.08
tPDAc1d	1.12		1.28		1.39		1.50		1.66	
tPDAc2d	1.05		1.14		1.21		1.30		1.43	
tPDAdid	1.05		1.14		1.22		1.32		1.46	
tPDAm sd	0.55		0.66		0.74		0.82		0.93	
tPDAshd	0.76		0.75		0.74		0.73		0.73	
tPD Afid	0.52		0.61		0.68		0.75		0.85	
tPD Adrd	0.74		0.88		0.98		1.08		1.21	
Case: type=LEFT, drv=1										
tPHLc1d/tPLHc1d	1.50	1.52	1.89	1.90	2.10	2.12	2.24	2.27	2.31	2.38
tPHLc2d/tPLHc2d	1.47	1.51	1.87	1.95	2.11	2.22	2.28	2.45	2.43	2.69
tPHLdid/tPLHdid	1.50	1.42	1.90	1.78	2.13	1.97	2.30	2.10	2.42	2.16
tPHLmsd/tPLHmsd	0.50	0.52	0.62	0.66	0.69	0.76	0.76	0.84	0.83	0.93
tPHLshd/tPLHshd	0.96	0.89	1.08	1.10	1.16	1.25	1.24	1.41	1.32	1.61
tPHLfid/tPLHfid	1.18	1.17	1.46	1.46	1.59	1.60	1.66	1.66	1.66	1.64
tPDAc1d	1.09		1.24		1.35		1.46		1.61	
tPDAc2d	1.01		1.10		1.17		1.25		1.37	
tPDAdid	1.01		1.10		1.18		1.27		1.40	
tPDAm sd	0.72		0.70		0.69		0.70		0.71	
tPDAshd	0.43		0.52		0.58		0.63		0.70	
tPD Afid	0.71		0.91		1.02		1.11		1.18	



## Characteristic Reference Table (Cont.)

## 1) Timing Characteristics [Unit: ns]

(Typical process, 25°C,  $V_{DD}=2.5V$ ,  $C_L=10$ ,  $S=0.2$ )

Type	8		24		36		48		64	
Case: type=RIGHT, drv=1										
tPHLc1d/tPLHc1d	1.50	1.53	1.87	1.86	2.07	2.08	2.22	2.28	2.32	2.49
tPHLc2d/tPLHc2d	1.46	1.51	1.83	1.92	2.07	2.20	2.30	2.46	2.56	2.76
tPHLdid/tPLHdid	1.50	1.43	1.89	1.77	2.12	1.96	2.29	2.09	2.45	2.19
tPHLmsd/tPLHmsd	0.49	0.52	0.61	0.66	0.69	0.76	0.75	0.84	0.82	0.92
tPHLshd/tPLHshd	0.96	0.89	1.09	1.10	1.17	1.25	1.23	1.41	1.30	1.62
tPHLfid/tPLHfid	1.19	1.17	1.45	1.46	1.58	1.60	1.65	1.66	1.65	1.64
tPDAc1d	1.09		1.19		1.29		1.43		1.66	
tPDAc2d	1.00		1.09		1.16		1.25		1.39	
tPDAdid	1.00		1.09		1.17		1.27		1.42	
tPDAm sd	0.71		0.69		0.69		0.70		0.73	
tPDAshd	0.43		0.52		0.58		0.64		0.70	
tPD Afid	0.71		0.83		0.93		1.02		1.14	

2) Power Characteristics [Unit:  $\mu W/MHz$ ](Typical process, 25°C,  $V_{DD}=2.5V$ ,  $C_L=10$ ,  $S=0.2$ ,  $SA=0.5$ ,  $drv = 1$ )

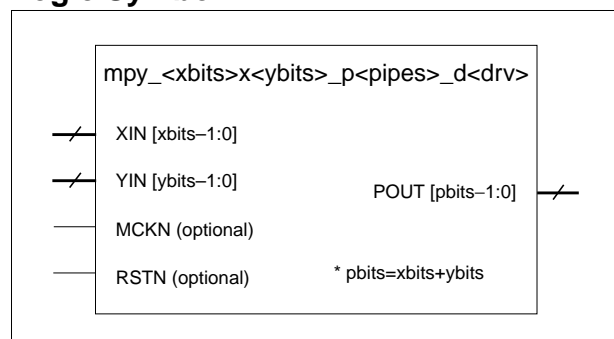
Case	8	24	36	48	64
type=BOTH	9.94	36.69	57.72	79.58	110.01
type=LEFT	6.82	23.31	36.57	50.57	70.42
type=RIGHT	6.80	23.64	36.76	50.30	69.01

3) Size Characteristics [Unit:  $\mu m$ ]

Type	Case	8	24	36	48	64
Width	type=BOTH	114.83	178.33	218.13	251.21	284.88
	type=LEFT	76.37	109.57	131.44	150.71	172.38
	type=RIGHT	76.37	109.57	131.44	150.71	172.38
Height	all	112.00	288.00	420.00	552.00	728.00



## Logic Symbol



## Features

- Asynchronous/Synchronous operation
- 6 to 64 bit multiplication
- High speed/low power operation
- 2's complement signed multiplication
- Modified Booth Algorithm
- 1-stage pipeline insertion available
- Two drive strength available.

## Function Description

The MPY is an NxM multiplier which is provided as a compiler. The MPY is intended to use in high-speed and low-power applications. It adopts the modified booth's multiplication scheme to encode the multiplier bits by partitioning the bits into three bit groups, with one bit shared between groups and performs a signed multiplication operation between two integers. It allows from 6-bit to 64-bit with a configurable size of output buffer and 1-stage pipeline scheme is available to improve the frequency of design.

The partial products are summed up with two adders; the MSB adder and the LSB adder. The MSB adder is a fast group bypass adder. The LSB adder is programmable to insert 1-stage pipeline scheme and is, therefore, the ripple carry adder. The clock to the pipeline controls the internal data change, so that the data is always stable throughout the clock period and there is no hold problem.

## Parameter Description

MPY is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters.

Parameter Name	Description	Range
xbits	Multiplicand (XIN) bits	6 to 64 (even)
ybits	Multiplier (YIN) bits	6 to 64 (even)
pipes	Pipeline stage	0/1
drv	Output drive strength	1/2

**NOTE:** The xbits should be greater than or equal to the ybits ( $x \geq y$ ).



MPY

Modified Booth Multiplier

Pin Description

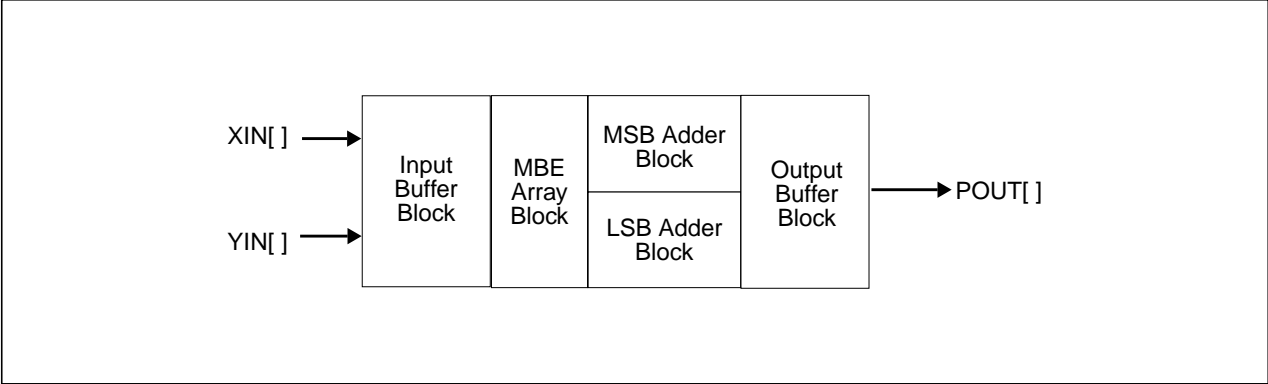
Pin Name	Type	Description
XIN [ ]	Input	Data input bus – Multiplicand
YIN [ ]		Data input bus – Multiplier
MCKN		Clock input to the pipeline register. (optional when the parameter pipes = 1)
RSTN		Reset negative input to the pipeline register. (optional when the parameter pipes = 1).
POUT[ ]	output	Data output bus – Product result

Pin Capacitance [Unit: pF]

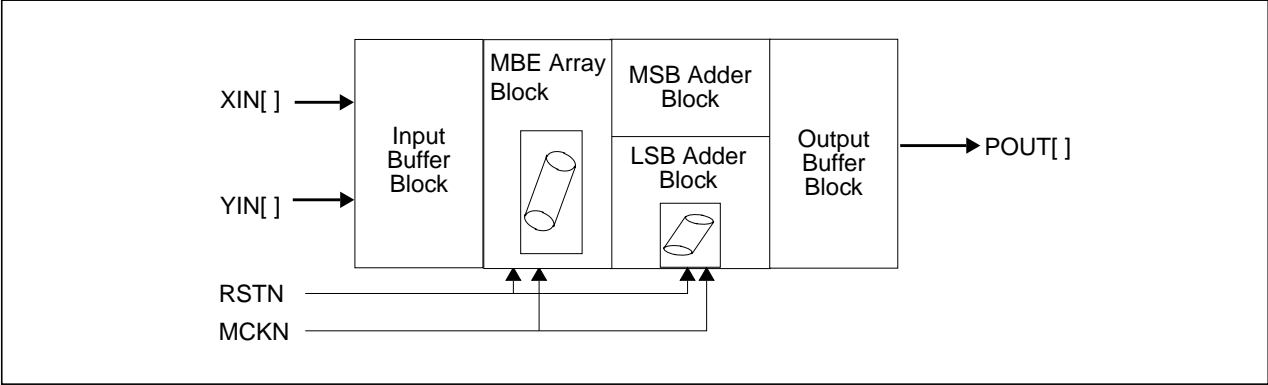
Name	Case	Value
XIN[ ]	all	0.0153
YIN[ ]	all	0.0293
MCKN	pipe=1	0.000018*x_width+0.001406*y_width–0.000003*x_width*y_width+0.021955
RSTN	pipe=1	0.000041*x_width+0.003235*y_width–0.000006*x_width*y_width+0.021454

Block Diagram

<pipes=0>



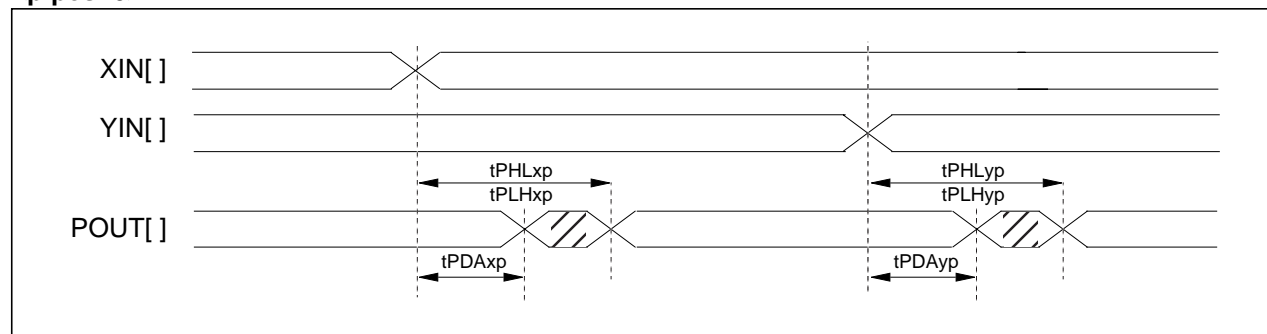
<pipes=1>





## Timing Diagram

&lt;pipes=0&gt;



## Timing Type Definition

Timing Type	Definition
tPHLxp/tPLHxp	Propagation delay from XIN[ ] to POUT[ ]
tPHLyp/tPLHyp	Propagation delay from YIN[ ] to POUT[ ]
tPDAXp	De-access time from XIN[ ] to POUT[ ]
tPDAYp	De-access time from YIN[ ] to POUT[ ]

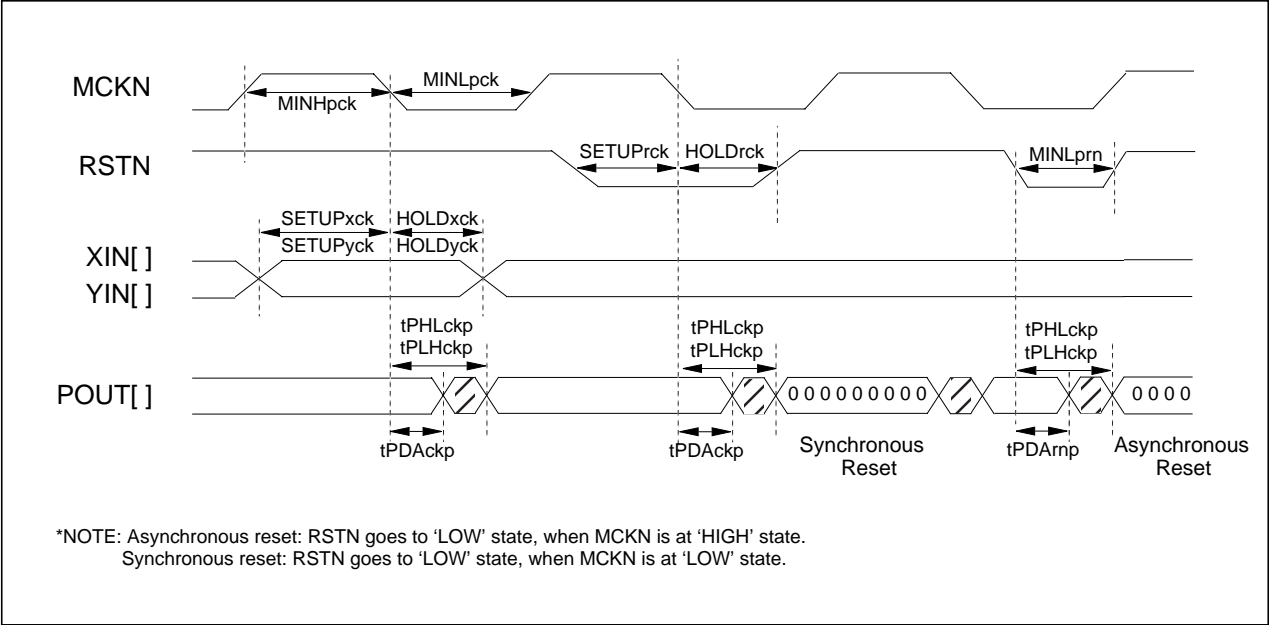


# MPY

## Modified Booth Multiplier

### Timing Diagram (Cont.)

<pipes=1>



### Timing Type Definition

Timing Type	Definition
SETUPxck	Setup time for input XIN[ ] to MCKN
SETUPyck	Setup time for input YIN[ ] to MCKN
SETUPrck	Setup time for input RSTN to MCKN
HOLDxck	Hold time for input XIN[ ] to MCKN
HOLDyck	Hold time for input YIN[ ] to MCKN
HOLDrck	Hold time for input RSTN to MCKN
MINHpck	Minimum Clock Pulse width HIGH
MINLpck	Minimum Clock Pulse width LOW
MINLprn	Minimum Clock Pulse width RSTN
tPHLckp/tPLHckp	Propagation delay from MCKN to POUT[ ]
tPHLrnp/tPLHrnp	Propagation delay from RSTN to POUT[ ]
tPDackp	De-access time from MCKN to POUT[ ]
tPDarnp	De-access time from RSTN to POUT[ ]



## Characteristic Reference Table

Symbol	Description	Unit	Symbol	Description	Unit
B	Number of Bits	-	W	Number of YIN[ ] bits	-
V <sub>DD</sub>	Power Supply Voltage	V	S	Input Slope	ns
C <sub>L</sub>	Output Load	SL	SA	Input Switching Activity	-

## 1) Timing Characteristics [Unit: ns]

(Typical process, 25°C, V<sub>DD</sub>=2.5V, C<sub>L</sub>=10, S=0.2)

Type	8x8	24x24	36x36	48x48	64x64
<i>Case: pipes=0, drv=1</i>					
tPHLxp/tPLHxp	2.72 / 2.68	5.78 / 5.65	8.01 / 7.87	10.17 / 10.10	12.96 / 13.06
tPHLyp/tPLHyp	2.37 / 2.22	4.56 / 4.46	6.20 / 6.13	7.84 / 7.81	10.02 / 10.05
tPDAxp	1.02	1.23	1.43	1.66	2.00
tPDApp	1.97	2.24	2.43	2.63	2.90
<i>Case: pipes=1, drv=1</i>					
HOLDrck	0.00	0.00	0.00	0.00	0.00
HOLDxck	0.00	0.00	0.00	0.00	0.00
HOLDyck	0.00	0.00	0.00	0.00	0.00
MINHpck	0.57	0.71	0.81	0.90	1.04
MINLpck	0.23	0.30	0.35	0.40	0.47
MINLprn	0.67	1.09	1.47	1.91	2.59
SETUPrck	0.67	1.09	1.47	1.91	2.59
SETUPxck	1.66	3.04	4.09	5.13	6.52
SETUPyck	1.88	2.90	3.67	4.43	5.45
tPHLckp	1.83	3.44	4.55	5.58	6.81
tPHLrnp	1.72	2.07	2.32	2.58	2.92
tPLHckp	1.47	3.06	4.19	5.28	6.65
tPLHrnp	0.00	0.00	0.00	0.00	0.00
tPDAckp	0.52	0.57	0.61	0.66	0.71
tPDArnnp	0.61	0.69	0.75	0.81	0.89



# MPY

## Modified Booth Multiplier

### Characteristic Reference Table (Cont.)

#### 2) Power Characteristics [Unit: $\mu\text{W}/\text{MHz}$ ]

(Typical process, 25°C,  $V_{DD}=2.5\text{V}$ ,  $C_L=10$ ,  $S=0.2$ ,  $SA=0.5$ )

Case	8x8	24x24	36x36	48x48	64x64
pipes=0, drv=1	62.32	385.23	1209.05	2531.42	5070.11
pipes=1, drv=1	85.17	328.68	964.13	1987.71	3956.24

#### 3) Size Characteristics [Unit: $\mu\text{m}$ ]

Type	Case	8x8	24x24	36x36	48x48	64x64
Width	pipes=0, drv=1	222.06	475.21	668.62	865.07	1131.74
	pipes=1, drv=1	276.30	531.49	723.89	917.16	1176.21
Height	pipes=0, drv=1	112.00	288.00	420.00	552.00	728.00
	pipes=1, drv=1	123.00	299.00	431.00	563.00	739.00



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**PLL**

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**6**



**Contents**

PLL2013X ..... 6-1



## General Description

The PLL2013X is a Phase-Locked Loop (PLL) Frequency Synthesizer constructed in CMOS on single monolithic structure. The PLL macrofunctions provide frequency multiplication capabilities. The output clock frequency  $F_{out}$  is related to the reference input clock frequency  $F_{in}$  (XTALIN) by the following equation:

$$F_{out} = (m \times F_{in}) / (p \times 2^s)$$

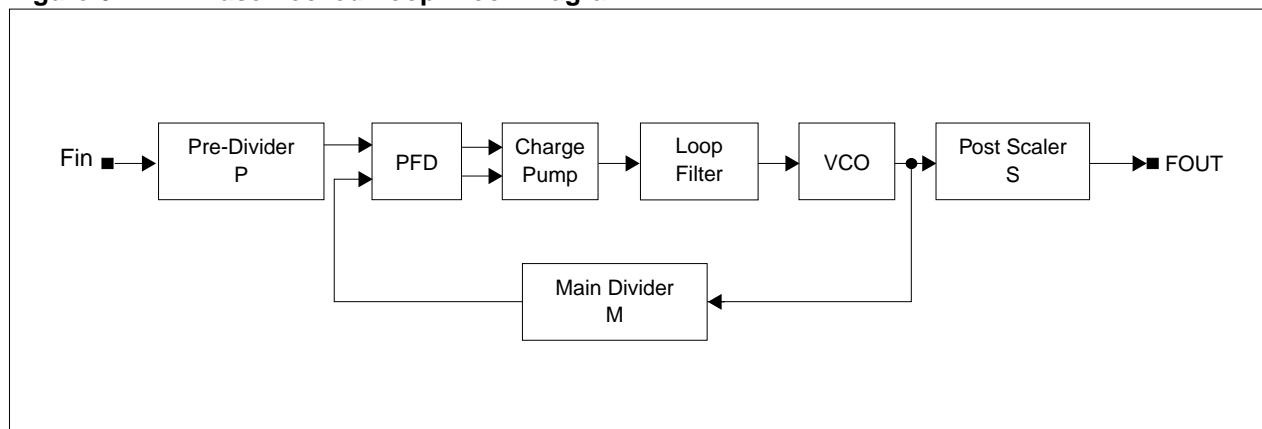
Where,  $F_{out}$  is the output clock frequency.  $F_{in}$  is the reference input clock frequency.  $m$ ,  $p$  and  $s$  are the values for programmable dividers. PLL2013X consists of a Phase/Frequency Detector (PFD), a Charge Pump, an External Loop Filter, a Voltage Controlled Oscillator (VCO), a 6-bit Pre-divider, an 8-bit Main divider and a 2-bit Post Scaler as shown in Figure 6-1

## Features

- 0.25  $\mu$ m CMOS device technology
- 2.5 V single power supply
- Output frequency range: 20-170MHz
- Jitter:  $\pm 150$  ps at 170MHz
- Duty ratio: 45% to 55% (All tuned range)
- Frequency changed by programmable dividers
- Provision for 14.318MHz crystal oscillator buffer (option)
- Lock detector (option)
- Power down mode

## Block Diagram

**Figure 6-1 Phase Locked Loop Block Diagram**



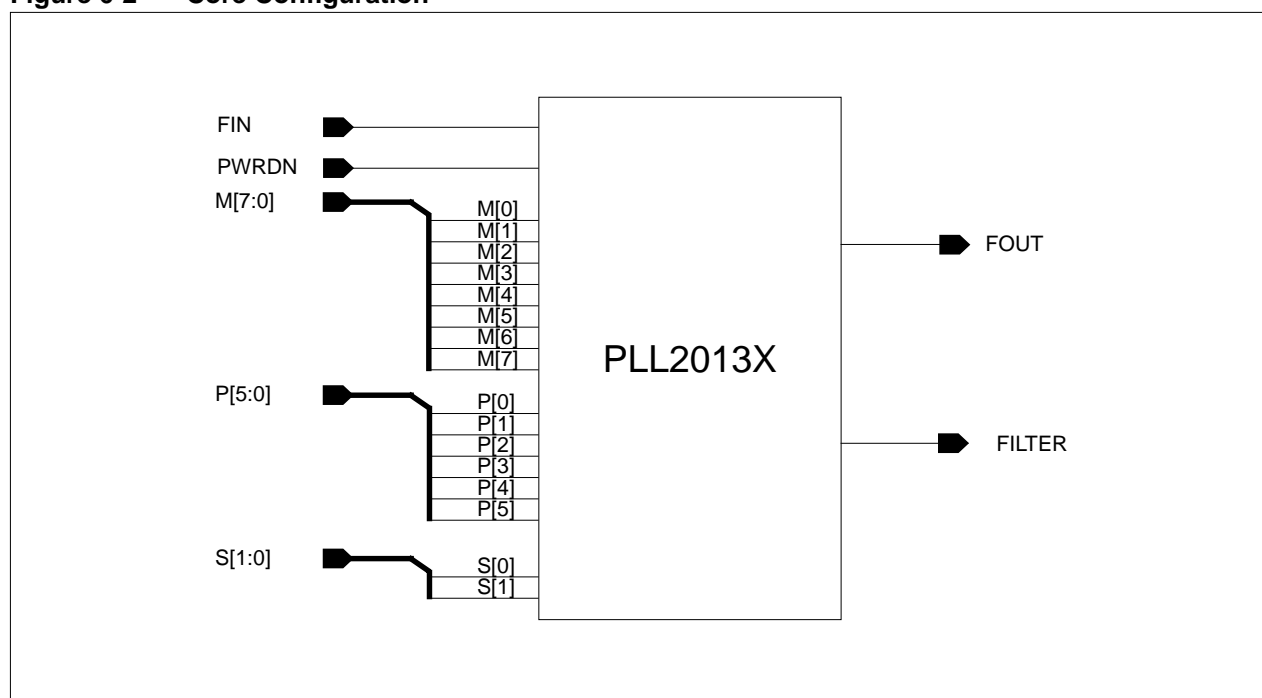
**NOTE:** X-tal oscillator and Lock detector are optional block. If customer concerns about this block - Xtal buffer or lock detector, refer to Optional Block Users Guide (page 6-6).



## Pin Description

Name	I/O Type	I/O Pad	Pin Description
VDD25A2	Digital Power	vdd2t_abb	Digital power supply
VSS25A2	Digital Ground	vss2t_abb	Digital ground
VDD25A1	Analog Power	vdd2t_abb	Analog power supply
VSS25A1	Analog Ground	vss2t_abb	Analog ground
VBBA	Analog sub bias /Digital sub bias	vbb_abb	Analog/Digital sub bias
FIN	Digital Input	picc_abb	Reference frequency input
FILTER	Analog Output	poar50_abb	Pump out is connected to filter. A capacitor is connected between the pin and analog ground.
FOUT	Digital Output	pot8_abb	20MHz~170MHz clock output
PWRDN	Digital Input	picc_abb	FSPLL clock power down. - When PWRDN is High, PLL do not operate. - If PWRDN is not used, it should be tied to VSS.
P[5:0]	Digital Input	picc_abb	The values for 6bit programmable pre-divider.
M[7:0]	Digital Input	picc_abb	The values for 8bit programmable main divider.
S[1:0]	Digital Input	picc_abb	The values for 2bit programmable post scaler.

**Figure 6-2 Core Configuration**





## Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD25A2 - VDD25A1	-0.1		+0.1	V
Oscillator frequency	Fosc		14.318		MHz
External loop filter capacitance	LF		820		pF
Operating temperature	Topr	0		70	°C

**NOTE:** It is strongly recommended that all the supply pins (VDD25A2, VDD25A1) be powered from the same operating supply voltage to avoid power latch-up.

## DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	VDD25A2/VDD25A1	2.375	2.5	2.625	V
Digital input voltage high	V <sub>IH</sub>	2.0			V
Digital input voltage low	V <sub>IL</sub>			0.8	V
Dynamic current	I <sub>dd</sub>			3	mA
Power down current	I <sub>pd</sub>			50	μA

## AC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Crystal frequency	F <sub>XTAL</sub>		14.318		MHz
Input frequency	F <sub>IN</sub>	5		40	MHz
Output clock frequency	F <sub>OUT</sub>	20		170	MHz
Input clock duty cycle	T <sub>ID</sub>	40		60	%
Output clock duty cycle (at 170MHz)	T <sub>OD</sub>	45		55	%
Input glitch pulse width	T <sub>IGP</sub>	1			ns
Locking time	T <sub>LT</sub>			150	μs
Jitter, cycle to cycle	T <sub>JCC</sub>	-150		+150	ps

**NOTE:** It is strongly recommended that input signal is not generated glitch, but if customer cannot help generating glitch, customer must carefully considerate the specification.



## Functional Description

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase.

In this application, it includes the following basic blocks.

- The voltage-controlled oscillator to generate the output frequency
- The divider P divides the reference frequency by p
- The divider M divides the VCO output frequency by m
- The divider S divides the VCO output frequency by s
- The phase frequency detector detects the phase difference between the reference frequency and the output frequency (after division) and controls the charge pump voltage.
- The loop filter removes the high frequency components in charge pump voltage and gives smooth and clean control to VCO

The m, p, s values can be programmed by 16bit digital data from the external source. So the PLL can be locked in the desired frequency.

$$F_{out} = (m \times F_{in}) / (p \times s)$$

where

$$F_{in} = 14.318\text{MHz}, m = M + 8, p = P + 2, s = 2^S$$

**Table 6-1 Digital Data Format**

Main Divider	Pre Divider	Post Scaler
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S1, S0

### NOTES:

1. S[1]-S[0]: Output frequency scaler
2. M[7]-M[0]: VCO frequency divider
3. P[5]-P[0]: Reference frequency input divider

## OUTPUT FREQUENCY EQUATION & TABLE

Frequency equation: 
$$F_{OUT} = \frac{(M+8)}{(P+2) \times 2^S} \times F_{IN}$$

**Table 6-2 Example of Divider Ratio**

M7	M6	M5	M4	M3	M2	M1	M0	M	m(M+8)	S1	S0	2 <sup>S</sup>
0	1	0	1	0	1	0	1	85	93	0	0	1
P5	P4	P3	P2	P1	P0	P	p(P+2)					
1	0	1	0	1	0	42	44					

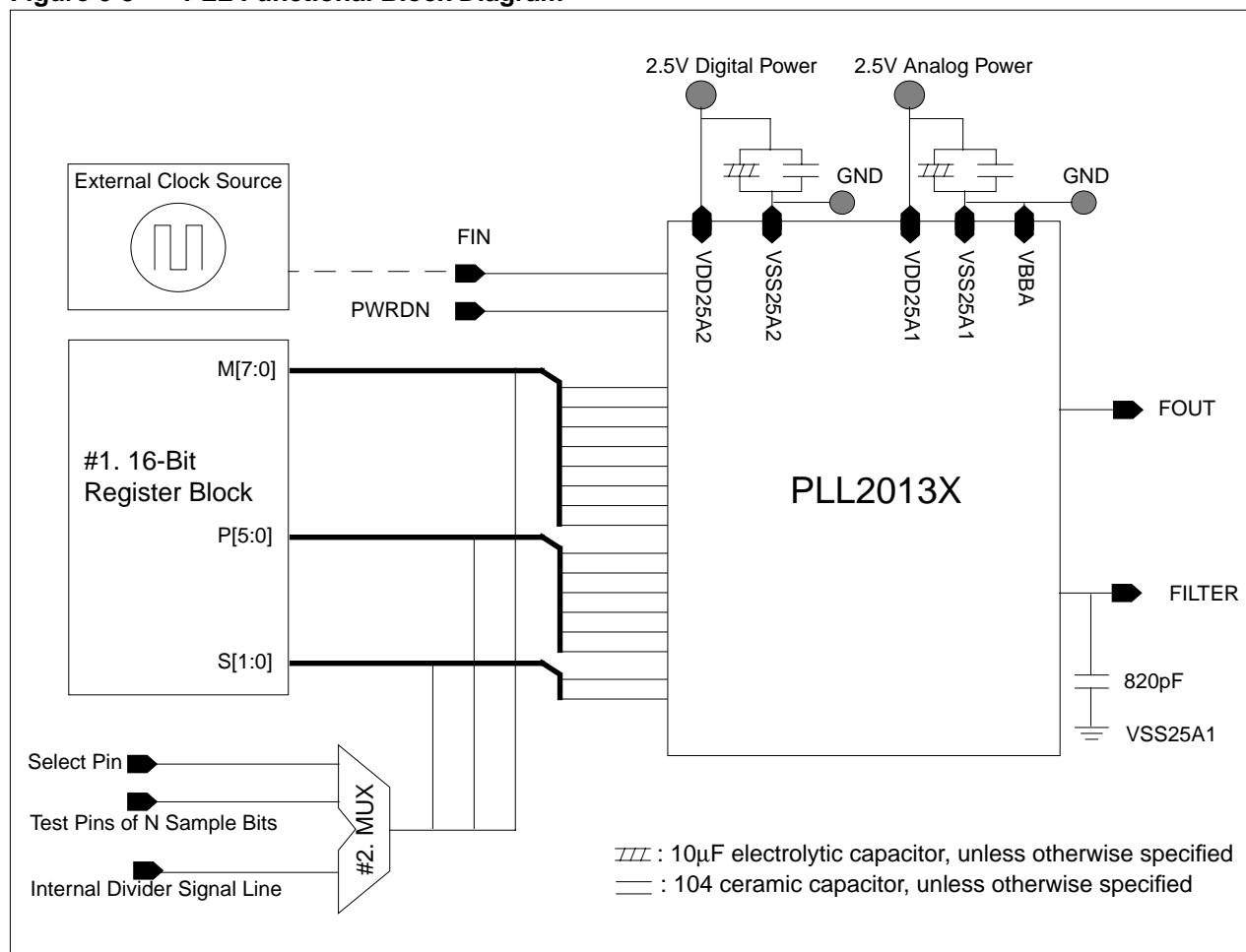


## CORE EVALUATION GUIDE

For the embedded PLL, we must consider the test circuits for the embedded PLL core in multiple applications. Hence the following requirements should be satisfied.

- The FILTER and FOUT pins must be bypassed for external test.
- For PLL test (below 2 examples), it is needed to control the dividers - M[7:0], P[5:0] and S[1:0] - that generate multiple clocks.
  - #1. Registers can be used for easy control of divider values.
  - #2. N sample bits of 16-bit divider pins can be bypassed for test using mux.

**Figure 6-3 PLL Functional Block Diagram**





### Core Layout Guide

The digital power (VDD25A2, VSS25A2) and the analog power (VDD25A1, VSS25A1) must be dedicated to PLL only and separated. If the dedicated VDD25A2 and VSS25A2 is not allowed that of the least power consuming block is shared with the PLL.

The poar50\_abb pad is used as a FILTER pad that contains only ESD production diodes with 500ohm resistors.

The FOUT and FILTER pins must be placed far from the internal signals in order to avoid overlapping signal lines.

The blocks having a large digital switching current must be located away from the PLL core.

The PLL core must be shielded by guardring.

For the FOUT pad, you can use a custom drive buffer or pot8\_abb buffer considering the drive current.

### Optional Block Users Guide

— There are crystal driver cell options for the PLL2013X PLL core

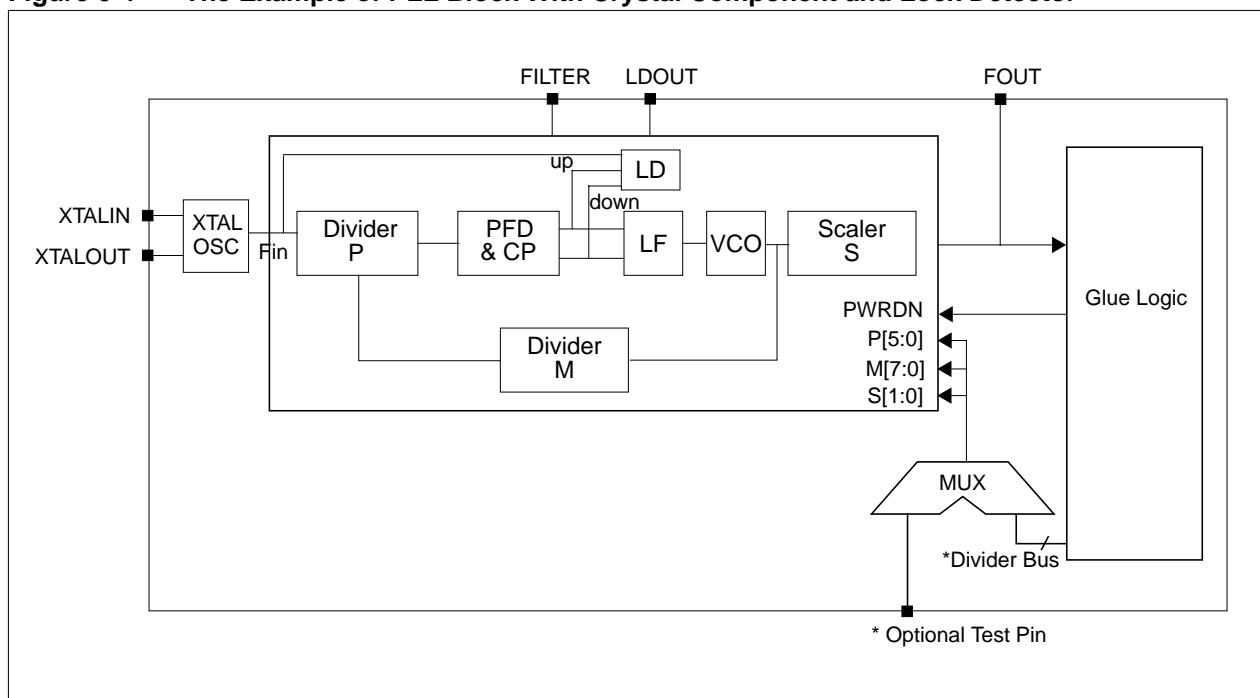
1. If the crystal component not used, an external clock source is applied to the FIN

- If the crystal component not used, an external clock I/O buffer offered from samsung's STD110 library is recommended for use
- When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:
  - Without Xtal-driver: FIN, FILTER, FOUT, VDD25A1, VSS25A1, VDD25A2 and VSS25A2, VBBA.

2. If the crystal componet and the lock detector used, please contact SEC application engineer

- When implementing an embedded PLL block, the following pins must be bypassed externally for testing the PLL locking function:
  - With Xtal-driver: XTALIN, XTALOUT, LDOUT, FILTER, FOUT, VDD25A1, VSS25A1, VDD25A2 and VSS25A2, VBBA

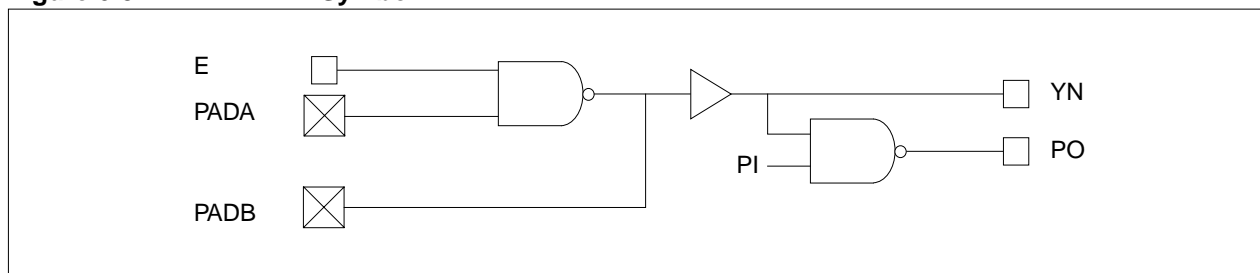
**Figure 6-4 The Example of PLL Block With Crystal Component and Lock Detector**





### XTAL Buffer Cell

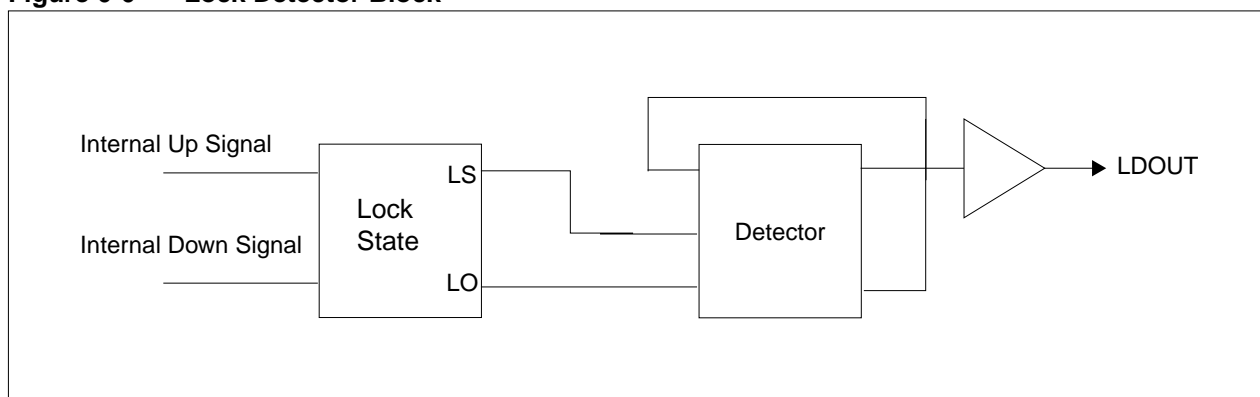
**Figure 6-5 XTAL PAD Symbol**



- A XTAL Buffer cell for PLL is supported STD110 databook of SEC
- The XTAL must be located between PADA and PADB.  
Enable pin (E) must be HIGH in normal operation.
- PI pin must be connected to vdd25a2 and the PO pin floated.

### Lock Detector

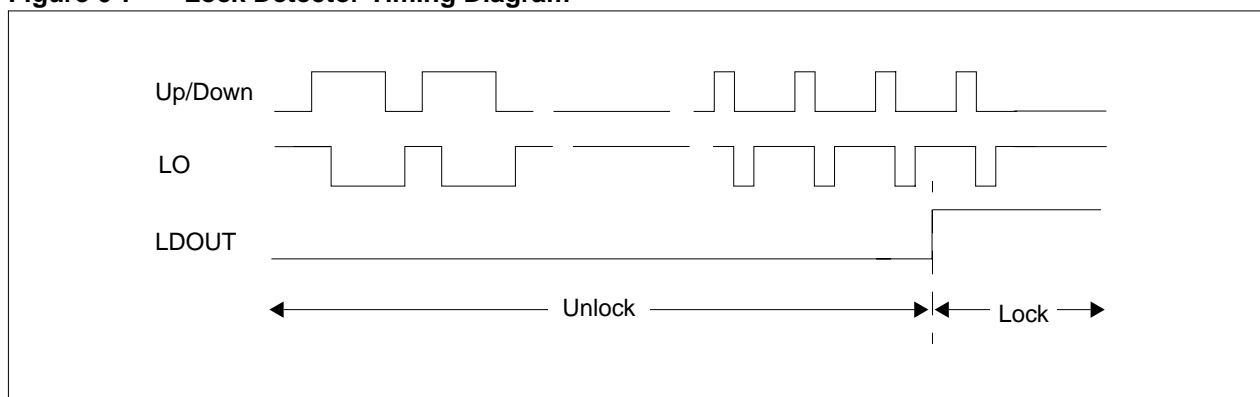
**Figure 6-6 Lock Detector Block**



The built-in lock detector circuit will only work, when it is used in conjunction with PFD block output up/down signal. (refer to Figure 6-6)

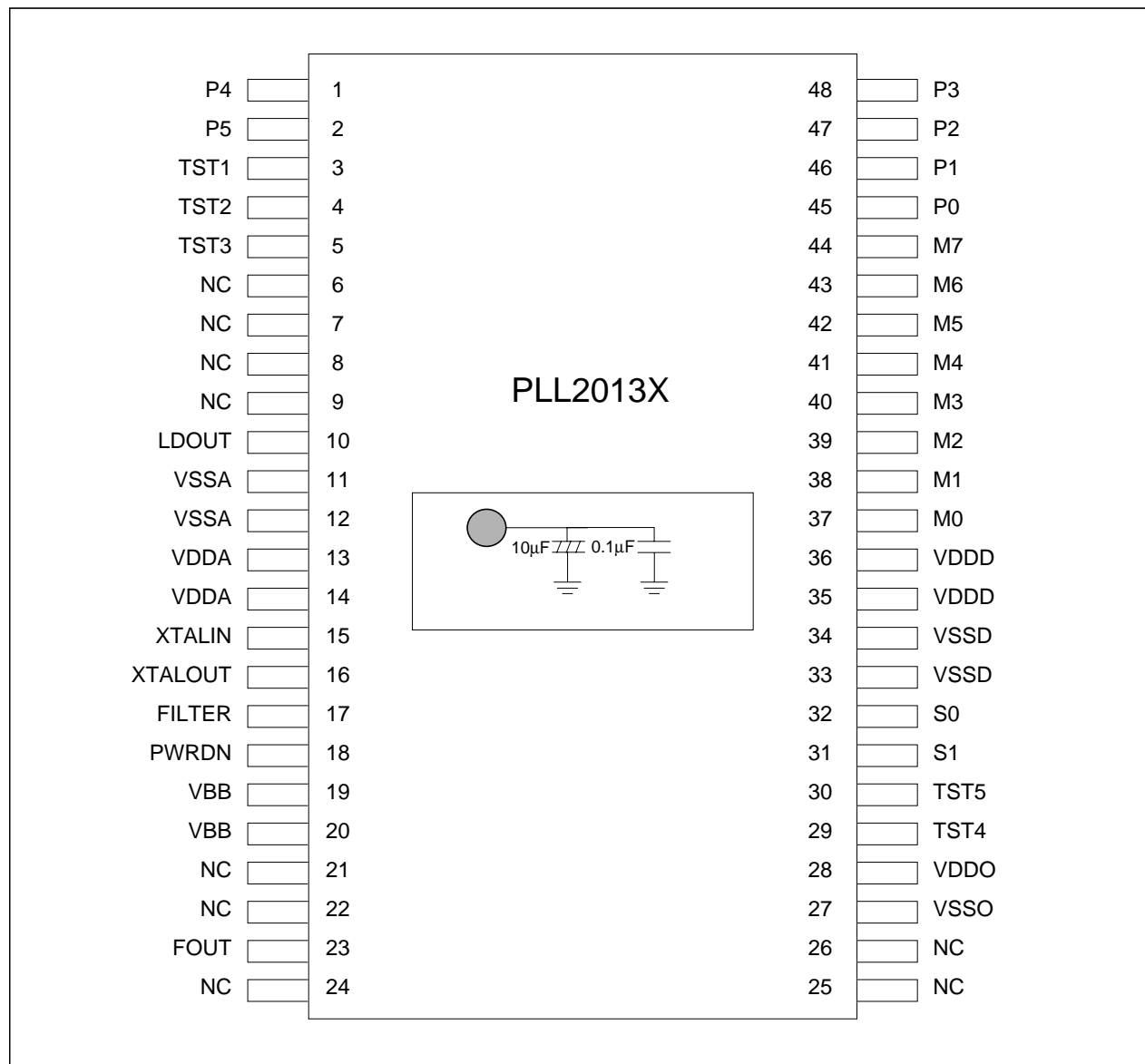
We represent the output of lock detector in the timing diagram. (refer to Figure 6-7)

**Figure 6-7 Lock Detector Timing Diagram**





## PACKAGE CONFIGURATION





**PACKAGE PIN DESCRIPTION**

NAME	PIN No.	I/O TYPE	PIN DESCRIPTION
VDDD	35, 36	DP	Digital power supply
VSSD	33, 34	DG	Digital ground
VBB	19, 20	AB/DB	Analog / digital sub bias
PWRDN	18	DI	FSPLL clock power down. - When PWRDN is high, PLL do not operate. - If PWRDN is not used, it should be tied to VSS.
P[0]~P[5]	45~48, 1, 2	DI	Pre-divider input
VDDA	13, 14	AP	Analog power supply
VSSA	11, 12	AG	Analog ground
XTALIN	15	AI	Crystal external clock input
XTALOUT	16	AO	Xtal buffer output clock
FOUT	23	DO	20MHZ~170MHz clock output
LDOUT	10	DO	Lock detector output
FILTER	17	AO	Pump out is connected to the filter. A 820pF capacitor is connected between the filter pin and analog ground pin
S[0]~S[1]	32, 31	DI	Post scaler input
M[0]~M[7]	37~44	DI	8-bit main divider input
TST1, TST3	3, 5	DI	Test pin, apply to analog vdda
TST2, TST4, TST5	4, 29, 30	DI	Test pin, apply to ground
VDDO	28	PP	I/O pad power
VSSO	27	PG	I/O pad ground

**NOTES:**

1. I/O TYPE PP and PG denote PAD power and PAD ground respectively.
2. XTALIN, XTALOUT, LDOUT is test pin for PLL in SEC.



## Design Considerations

The following design considerations apply:

- Jitter is affected by the power noise, substrate noise, etc.  
It increases when the noise level increases.
- A CMOS-level input reference clock is recommend for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
- The used of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
- The following apply to the noise level, which can be minimized by using good analog power and ground isolation techniques in the system:
  - Use wide PCB traces for POWER (VDD25A2/VSS25A2, VDD25A1/VSS25A1, VBBA) connections to the PLL core. Separate the traces from the chip's VDD25A2/VSS25A2, VDD25A1/VSS25A1 supplies.
  - Use proper VDD25A2/VSS25A2, VDD25A1/VSS25A1 de-coupling.
  - Use good power and ground sources on the board.
  - Use power VBBA for minimize substrate noise.
- The PLL core should be placed as close as possible to the dedicated loop filter and analog power and ground pins.
- It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
- Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction.



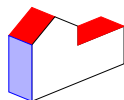
## PLL Specification

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Parameter	Min	Typ	Max	Unit	Remarks
Supply voltage					
Output frequency range					
Input frequency range					
Cycle-to-cycle jitter					
Lock up time					
Dynamic current					
Standby current					
Output clock duty ratio					
Long term jitter					
Output slew rate					

- Do you need XTAL driver buffer in PLL core?
  - If you need it, what is the crystal frequency range?
  - If not, What is the input frequency range?
- Do you need the lock detector?
- Do you need the I/O cell of SEC?
- Do you need the external pin for PLL test?
- What is the main frequency and frequency range?
- How many FSPLLs do you use in your system?
- What is output loading?
- Could you internal/external pin configurations as required?
- Specially requested function list:



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