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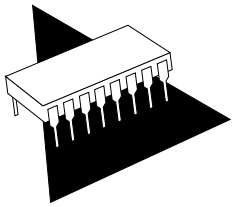
- Chapter 2: DC Electrical Characteristics(Recommended Operating Conditions)
- Chapter 3: Primitive Cells
- Chapter 5: Complied Memories



STDL131

0.18μm 1.8V CMOS Standard Cell Library for Pure Logic Products

STDL131
0.18μm 1.8V CMOS Standard Cell Library
for Pure Logic Products
Data Book

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Introduction

This databook contains information about STDL131 0.18μm 1.8V standard cell library for pure Logic products developed by SEC (Samsung Electronics Corporation).

The “library” basically contains various kinds of primitive and I/O cells and cores which are used for developing ASIC (Application Specific Integrated Circuit). It also includes a design kit helping designers to work in a workstation platform, and all sorts of design environments needed for an automatic chip design.

There are six chapters in this databook:

Chapter 1	Introduction
Chapter 2	Electrical Characteristics
Chapter 3	Primitive Cells
Chapter 4	Input/Output Cells
Chapter 5	Compiled Memories
Chapter 6	PLL
	Appendix

In this databook, each cell is followed by its AC electrical characteristics, and these characteristic values are almost equal when the corresponding cell is operated in a real chip.

The purpose of this databook is to prevent any misuse or misapplication of STDL131 cell library by providing precise information about the cell list, electrical data, directions for use, and matters demanding special attention.

If you want to get more information about digital cores and analog cores that are not included in this databook, access the Samsung ASIC web site(http://www.samsung.com/Products/Semiconductor/ASIC) or contact head office.

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1.1 Library Description

STDL131 is Samsung's next generation Standard Cell library containing standard cells implemented in Samsung's 0.18um, L18L process technology. The focus of Samsung's L18L process is the lowest leakage current. The I_{off} value of that process is 3pA/um at typical conditions. This value is at least 30 to 40 times smaller than that of the generic 0.18um process. Although the L18L process has a little bit poor performance than that of the generic process, it can extremely save the leakage current or standby powers for portable applications. Because the L18L process is based on the generic 0.18um process, L18, it supports the combined process in one chip that is the combination of L18L and L18 process and it also supports all the IP cores and libraries of those process. It is an excellently compensatory method for the poor performance.

The STDL131 library contains diverse application specific digital and analog IP for System-on-Chip (SoC) applications. Samsung provides a full range of cells within the STDL131 library to address the challenges of designing and producing ultra low power as well as high density devices that take advantage of SoC integration. With its reduced power dissipation and high density, STDL131 can help reduce system cost for low leakage corrent applications such as PDA, CDMA and portable applications.

The STDL131 library supports gate counts of up to 16 million gates with 80% usability. Logic and memory densities are respectively 1.8 and 3 times better than STD110.

The STDL131 library also contains fully user configurable complied memories for high density or low power applications. High capacity memory compilers for SoC designs also contain redundant elements for memory repair.

The STDL131 library also supports various of I/O interface voltages and standards. I/O cells that drive 1.8V, 2.5V, and 3.3V are available as are 3.3V and 5V tolerant I/O's. Available I/O standards include LVTTL, LVCMOS, PCI, OSC, ATA, AGP, PECL, SSTL2, GTLp, LVDS, and USB 1.1.

To better support SoC design, a robust collection of digital and analog IP cores are available. Digital cores include the ARM7TDMI, ARM9TDMI, ARM920T, and ARM940T from ARM Ltd., as well as the Teak and TeakLite DSP cores from the DSP Group. Analog cores include ADCs, DACs, CODECs, and PLLs with various bit configurations and frequency ranges. A thick oxide process option allows for high resolution operation of analog cores with a 3.3V power supply.

In addition, the STDL131 library supports communication and data transmission cores such as USB 1.1, IEEE1284, IEEE1394 link controller, UART, PCI controller, PCMCIA controller and 10/100 ethernet MAC.

Samsung's design methodology offers a comprehensive timing driven design flow including automated time budgeting, tight floor plan synthesis integration, powerful timing analysis, and timing driven layout. Our advanced characterization flow provides accurate timing data and robust delay models for L18L, our 0.18um very deep sub-micron process technology. Static verification methods, such as static timing analysis and formal1 equivalence checking, provide an effective verification methodology with a variety of simulators. Samsung's Design-for-Test (DFT) methodology supports full and partial scan chain design, BIST, JTAG boundary scan, and Built-in-Redundancy-Analysis (BIRA) for reparable SRAM. Samsung provides a full set of test ready IP cores with an efficient core test integration methodology.

1.2 Features

- Robust 1.8V standard cell library including processor, DSP, and analog cores.
  - 0.18μm CMOS process technology with optional 6 metal layers.
  - High gate count design of up to 16 million gates with up to 80% utilization for 6 layer metal.
  - Typical 2 input NAND gate delay of 80ps with a fanout of 2.
  - 3pA/um I_{off} value at typical condition.
  - Characterized to industrial (-40˚C to 85˚C) and commercial (0˚C to 70˚C) temperature ranges.
- Robust digital cores
  - Hard macro cells - ARM7TDMI, ARM9TDMI, ARM920T, ARM940T, Teak, and TeakLite.
  - ARM core peripherals - AMBA, DMA controller, SDRAM controller, Interrupt controller, IIC, WDT, RTC.
  - Soft macro cells - USB1.1, IrDA, 16C450 and 16C550 UART, Fast Ether net MAC, P1394a LINK, IEEE1284, PCI controller, PCMCIA controller.
- Ultra Low Voltage (1.8V) and High Resolution (3.3V) Analog Cores
  - Analog core supply voltages (± 5%) -1.8V, 2.5V, and 3.3V.
  - ADC: 10-bit (500K, 30MHz, 1.8V)
  - DAC: 8-bit (2MHz, 50MHz, 1.8V)
  - CODEC: 14-bit Sigma-Delta (8kHz ~ 11kHz, 2.5V)
  - PLL: 1.8V FSPLL (20MHz ~ 150MHz, 20MHz ~ 300MHz and 50MHz ~ 500MHz)
  - Can combine high resolution analog cores with 2.5V or 3.3V supply voltage in STD130 library with STDL130 library. For more information regarding high resolution analog cores, please refer to the STD130 databook.
- Fully User Configurable SRAM and ROM
  - High density or low power memory configurations
  - Single port (1RW, 1R), dual port (2RW), and multi port (1R1W - 2R2W)
  - Zero hold time in synchronous mode
  - Bit-write capability
  - 2 bank architecture
  - Flexible aspect ratio
  - Up to 512K-bit single port SRAM
  - Up to 256K-bit dual port SRAM
  - Up to 512K-bit diffusion or metal 2 programmable ROM
  - Up to 16K-bit multi port register files
  - Up to 64K-bit FIFOs
  - Up to 32K-bit CAM (Content Addressable Memory)
  - Up to 1 megabit reparable SRAM with redundancy.
- Full Compliment of I/O Cells
  - 1.8V/2.5V/3.3V drive and 3.3V/5.0V tolerant I/Os
  - 3 levels (high, medium, and no) of slew rate control
  - Minimum wire bonded pad pitch
  - 70μm single in line I/Os
  - 35μm staggered I/Os
  - Drive capabilities
    - Up to 24mA for drive I/Os
    - Up to 6mA for tolerant I/Os

- Standard Interface IP
  - PCI 2.1 compliant,33/66MHz, 5V tolerant
  - USB 1.1 compliant, full speed/low speed, 3.3V
  - SSTL2 Class-I and II SDRAM interface, up to 200MHz
  - ATA4/UDMA66, 3.3V, 5V tolerant
  - AGP 2.0 compliant, 66MHz @ 1X, 133MHz @ 2X, 266MHz @ 4X
  - PECL, 200MHz single ended, 500MHz differential point-to-point ATM interface
  - HSTL, 300MHz, 1.5V SRAM interface with programmable output impedance control
  - Hot Swap PCI - 1V pre-charge, VIO pre-charge
  - PCI-X, 1.0 compliant, 133MHz, 3.3V
- Fully Integrated CAD software and EDA support
  - Logic synthesis: Synopsys Design compiler
  - Physical synthesis: Synopsys Physical compiler
  - Logic simulation: Cadence Verilog XL, Cadence NC-Verilog, Mentor ModelSim-VHDL, Mentor ModelSim-Verilog, Synopsys VCS.
  - DFT, scan insertion and ATPG: Synopsys TestGen, Synopsys TestCompiler, Synopsys TetraMax, Mentor Fastscan.
  - Static timing analysis: Synopsys PrimeTime
  - RC analysis: Avant! Star-RCXT
  - Power analysis: Synopsys DesignPower, CubicPower (Samsung in-house tool).
  - Formal verification: Synopsys Formality, Avant! Design VERIFYer, Verplex Tuxedo-LEC
  - Fault simulation: Cadence Verifault
  - Delay calculator: CubicDelay (Samsung in-house tool).
  - Floor planner: Avant! PlanerPL, CubicPlan (Samsung in-house tool).
  - Place and Route: Avant! Apollo, Cadence Silicon Ensemble
  - DRC and LVS: Dracula, Hercules, Calibre
- Easy and Accurate Clock Tree Insertion
  - 12 user selectable clock tree cells
  - Accurate pre-layout and post-layout correlation
  - Insertion delay, skew, transition time management
  - Clock tree information file generation
  - Tightly coupled with in-house delay calculator, CubicDelay.

For more information on the CTC flow, refer to "CTS Flow with Clock Tree Cell User Guide for CubicDelay" included in the Samsung Design Kit.

1.3 EDA Support

Samsung provides an effective solution for multi-million gate designs in very deep submicron technology. For large SoC designs, our static timing and verification methodology will reduce design cycle time and reduce ever increasing time-to-market pressure. Our design-for-test (DFT) methodology and service enables all phases of test insertion, test pattern generation, and fault grading resulting in the highest test coverage.

The STDL131 design methodology supports a rich collection of industry standard EDA tools from Cadence, Synopsys, Mentor Graphics, and Avant! on Solaris and HP platforms. Customers may choose from among industry leading EDA tools for design capture, synthesis, simulation, DFT and layout. Several powerful proprietary software tools are seamlessly integrated in our design kits to improve design quality.

The STDL131 design methodology uses a proprietary delay calculator, CubicDelay, for high timing simulation accuracy. Cell delay is calculated based on a matrix of delay parameters for each macrocell and signal interconnection delay is calculated based on RC tree analysis.

1.4 Product Family

STDL131 library includes the following design elements:

- Analog core cells
- Digital core cells
- Internal macrocells
- Compiled memory macrocells
- Input/Output cells

1.4.1 ANALOG CORE CELLS

Introduction to Analog Cores (see Appendix A for a glossary of analog terms)

Samsung is a leading supplier of cell based mixed signal design elements. As a leading supplier of mixed signal elements, Samsung has more analog design experience than other ASIC suppliers. Analog cell development has been and will continue to be a part of the strategic focus of Samsung ASIC. Symbolic representations of analog cells are supplied for design entry by Customers or a Samsung design or technology center and are replaced with the cell physicals during place and route. Samsung design methodology uses the same automatic layout and verification tools for analog cells as for digital cells. Mixed signal designs are processed on the same production line as pure digital designs.

Samsung's analog core family consists of ADCs, DACs, PLLs, and CODECs. A brief description of each follows.

Analog-to-Digital Converter

Analog-to-digital converters, ADCs, provides the link between the analog world and digital systems. An ADC produces a digital output, D, as a function of the analog input, A:

$$D = f(A)$$

While the input can assume an infinite number of values, the output takes on only a finite set of digital values determined by the converter's resolution or output word length. Thus, the ADC must approximate each input level with one of these values. This process is also called quantization.

In digital systems, the input signal amplitude, A, is sampled at discrete time intervals and is then quantized into discrete steps and output as a digital value, D. The sampling time interval is also known as the sampling frequency.

Digital-to-Analog Converter

Digital-to-Analog Converters, or DACs, are the digital value to analog signal conversion circuits. The output can be in the form of a current or a voltage wave form. DACs provide the interface between digital systems and the analog world. DACs are employed in a variety of applications from CRT display systems and voice synthesizers to automatic test systems, digital controlled attenuators, and process control actuators.

Figure 1-1 shows the functional block diagram of a basic DAC. The input to the DAC is a digital value, D, made up of a stream of bits. The output analog current or voltage quantity, A, is related to the input as:

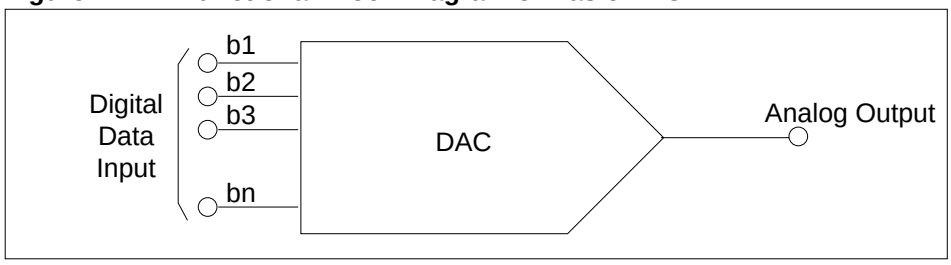
$$A = KV_{REF}\left[\frac{b1}{2^1}+\frac{b2}{2^2}+\ldots+\frac{bn}{2^n}\right]$$

where K is a scale factor, V_{REF} is a reference voltage, n is the resolution expressed as the total number of bits, and b1, b2, …, bn are the bit coefficients. The output exhibits 2^n discrete voltage levels ranging from zero to a maximum value of

$$Vo(max) = V_{REF}\frac{2^n-1}{2^n}$$

with a minimum step change ΔVo given as $\Delta Vo = \frac{V_{REF}}{2^n}$

Figure 1-1. Functional Block Diagram of Basic DAC



Sigma-Delta ADC/DAC

Samsung's L18L process offers high speed and high density, but reduced accuracy and signal range (dynamic range) for analog components. Hence, an exchange of digital complexity and resolution in time for resolution in signal amplitude is needed. A good solution to this trade-off is an over sampling data converter. An over sampling sigma-delta converter is ideal for slow speed (audio band) applications. It's noise shaping (sigma-delta) feature produces a high resolution output with a signal to noise ratio of 90 to 100dB.

In an ADC, an analog signal is converted to a differential signal and then filtered with an anti-aliasing filter. A sigma delta modulator converts the signal into an over sampled noise-shaping 1-bit pulse density modulated (PDM) signal. A digital decimation filter then rejects the out-of-band noise and outputs a 16-bit high resolution digital signal that is down sampled to the sampling rate, Fs. In a DAC, digital data is over sampled by an interpolation filter and is converted to a noise shaped 1-bit PDM signal through a digital sigma-delta modulator. An analog SoC post filter rejects the out-of-band noise. An anti-image filter then rejects the sampling images and outputs a high resolution analog signal.

Phase Locked Loop

Samsung's PLL cores are implemented as an analog function to provide frequency multiplication enabling SoC designers to synchronize chip level clock networks to a common reference signal.

In the past, designers wishing to incorporate a PLL into a digital design had only two options:

1) Use a special mixed signal process, typically an expensive process combing bi-polar and CMOS processing on the same silicon, to implement the analog functions.

2) Use and all digital PLL design requiring very large silicon area so that the PLL could be implemented in a standard CMOS digital process. This type of PLL design usually exhibits poor locking time.

Samsung's PLL cores are analog PLLs implemented on our standard digital CMOS process. Advantages of Samsung's PLL cores are:

* Require only a few off-chip passive components to implement the PLL function.
* No need for an expensive mixed signal (bi-polar and CMOS) process.
* Provide a faster locking time than a full digital implementation.
* Have low jitter characteristics.

Customer Service and Technical Support

Samsung provides full support for our customers needing analog cores. Support is provided through Samsung's worldwide Technology and Design Centers. In addition, Samsung analog design engineers are available to design or customize Samsung analog cores to meet specific customer needs. Since mixed signal design is quite different from digital design in terms of design techniques, layout, and test methodology, Samsung provides a mixed signal technical guide describing all development steps. In addition, each core is fully documented and is delivered with a data sheet. The following is a description of analog core data sheets:

Core Preview

Describes the main features and specifications for a core that is under development. Some specifications, such as the exact pin-out, may not be finalized at the time of publication. The purpose of this document is to provide customers with advanced product planning information.

Preliminary Data Sheet

Completely describes a new core. The preliminary data sheet contains a feature list, applications notes, timing diagrams, theory of operation, core pin information, a test guide, a layout guide, and preliminary AC/DC electrical information. The electrical information is based on worst case simulation data and prototype silicon performance. The purpose of this data sheet is to allow customers to confidently begin active development with the core.

Final Data Sheet

Updated version of the preliminary data sheet reflecting fully characterized silicon performance. Updates include more complete and tighter electrical specifications.

The purpose of this data sheet is to communicate the confirmed performance of the core after full characterization and passing qualification.

1.4.2 STANDARD LOGIC CELLS

Samsung standard cell library is designed to enable designers to achieve the high-integration with best performance in STDL131. In addition, this standard cell library is carefully verified on silicon to ensure much higher manufacturability. Due to this, System-On-Chips (SoC) designed using these standard cells will be obtained much higher yield. Rich standard cells, consisting of about 370 cells, with at least four drive strengths have been optimized specifically for synthesis and place and route tools.

The cells were selected to achieve best performance with synthesis tool and to give designers the elements the need to create high-integration designs. Each cell has been carefully hand-crafted to provide the optimal solution for high-integration applications with best performance.

Each of cells has been very accurately modeled for both timing and power to guarantee timing closure and to eliminate many meaningless iterative design cycles. All models are carefully qualified and tested using the in-house library automation environment. Some of features in STDL131 standard cell library are summarized as follows:

- Complete optimized library with synthesis and place and route tool
- Hand-crafted layouts for the optimal densities for each process
- Low manufacturing cost
- Reducing design time
- Providing more accurate timing and power
- Complete interfaces with all popular EDA tools

STDL131 standard cell library contains a protection diode cell. The protection diode cell is used to avoid the antenna effect. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the antenna effect rule. The protection diode cell can be used in this case to add a diode on the net close to the input gates which do not meet the rule. Also, the protection diode can be added to the input drivers of soft-macro cores. The protection diode cell is composed of forward and reverse diodes. It is not included in this databook.

In addition, STDL131 standard cell library contains several filler cells. During place and route, the filler cells are used to connect power and ground rails across an area including no cells. The filler cells are also used to make sure that gaps do not occur between well or implant layers which may cause some of design rule violations.

1.4.3 COMPILED MEMORY

STDL131 library memories are fully user configurable and provided through compilers. Two different memory types are provided in STDL131 targeted for two different types of applications as follows:

- STDL131HD - compiled memory targeted for high density applications
- STDL131LP - compiled memory targeted for low power applications

Twelve types of STDL131HD high density compiled memories are available as follows:

- Single-port synchronous SRAM with and without bit-write.
- Dual-port synchronous SRAM with and without bit-write.
- Single-port asynchronous SRAM with and without bit-write.
- Single-port synchronous SRAM redundancy.
- Synchronous diffusion programmable and metal 2 programmable ROM.
- Multi-port asynchronous register file.
- Synchronous FIFO (First-in-First-Out) Memory).
- Synchronous CAM (Content Addressable Memory).

Six types of STDL131LP low power compiled memories are available as follows:

- Single-port synchronous SRAM with and without bit-write.
- Dual-port synchronous SRAM with and without bit-write.
- Single-port asynchronous SRAM with and without bit-write.

Synchronous memories are fully synchronous at the rising edge of clock and have zero wait state. They also have optional bit write capability. Address, Data-In, and other control pins have zero hold time. Asynchronous memories have a synchronous write operation and an asynchronous read operation. Multi-port register files have a synchronous write operation at the rising edge of clock and an asynchronous read operation.

Four types of configurations are available for multi port register files. They are 2 port (1 read and 1 write), 3 port (1 read, 2 write or 2 read, 1 write), and 4 port (2 read and 2 write).

The STDL131 library contains two types of speciality memories: FIFO (First-In-First-Out) and CAM (Content Addressable Memory). FIFOs, widely used in communications buffering applications, are fully synchronous at the rising edge of clock. CAMs, widely used as cache tag tables and translation look-up tables, also are fully synchronous at the rising edge of clock.

Memory is becoming much more dominant and larger memory is required for SoC designs. The STDL131 library memory compilers support high capacity memories, from 64Kb to 1Mb with redundancy. These repairable memories use a row redundancy scheme and BIRA (Built-In-Redundancy-Analysis) to help guarantee higher yield. The number of redundant rows varies with memory size.

STDL131 compiled memories provide a power down mode to significantly reduce power during a read or write operation. In addition, a stand-by mode is provided in which memory contents and outputs are stable but power is greatly reduced.

STDL131LP, low power compiled memories, also use a partial array activation architecture and divided word line structure to reduce power even more.

A two bank architecture is provided on STDL131 memories, except dual port synchronous SRAM and specialty memories, to improve performance and reduce power. In this two bank architecture, only one bank is active while the other bank is in stand-by mode.

Flexible memory aspect ratios are provided to facilitate floor planning of an SoC design. In addition, an automated datasheet generator documents memory configuration, timing, aspect ratio and power consumption. Physical abstract data, also called phantoms or black boxes, for Silicon Ensemble and Apollo are generated and provided.

BIST (Built-In Self Test) circuitry is provided for most STDL131 compiled memories. BIST circuits are designed to detect a set of fault types that impact the functionality of the memory. The BIST circuitry is generated by a soft macro based BIST generator. The BIST generator generates both an individual BIST netlist for each memory and a shared BIST netlist for all memories used in a design. However, when several memories are used in a design, it is better to generate a shared BIST netlist to eliminate redundancy in the BIST circuitry over generating BIST circuits for each memory.

1.4.4 INPUT/OUTPUT CELLS

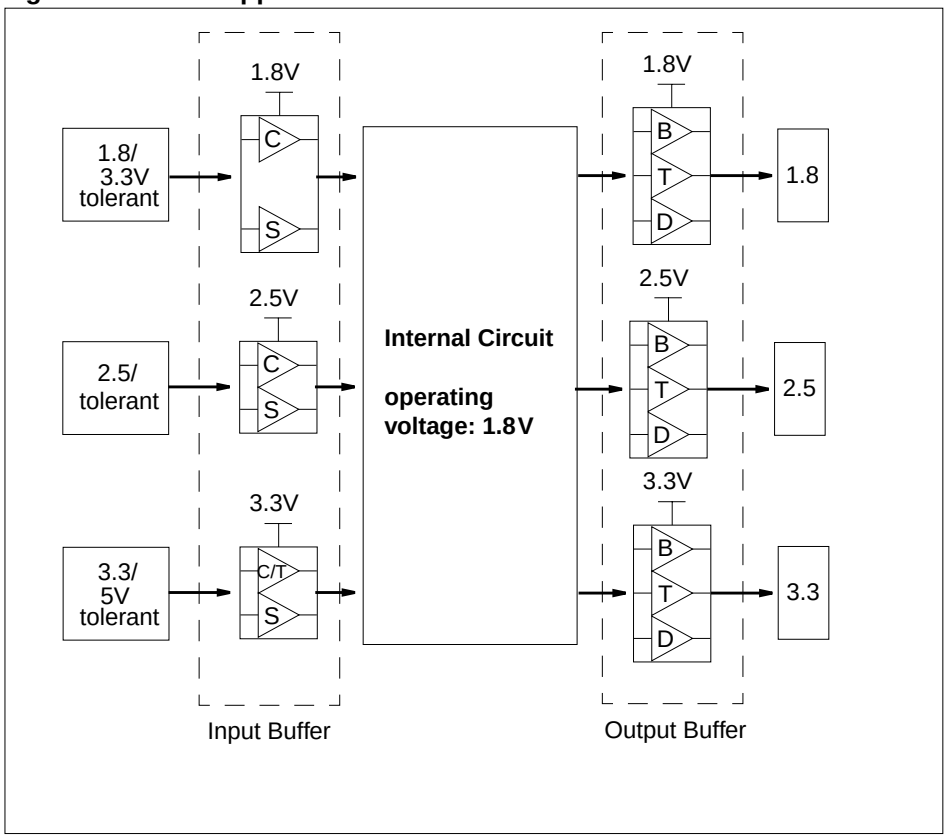
There are about 1000 different I/O cells in the STDL131 library for the designer to choose from. Three types of output buffers and bi-directional buffers (non-inverting, tri-state, and open drain) are available in a range of drive capabilities from 1mA to 24mA for 1.8V, 2.5V, and 3.3V drive outputs, and from 1mA to 6mA for 3.3V and 5V tolerant I/O cells. Three levels of slew rate control are provided for each buffer type except 1mA and 2mA drive buffers, to reduce output power and ground noise and signal ringing, especially for simultaneously switching outputs. All I/O buffers have been fully characterized for ESD protection and latch-up resistance.

Test logic is provided to enable efficient parametric testing on input buffers including LVCMOS and TTL level converters, Schmitt trigger input buffers, clock drivers, and oscillator buffers. 100K ohm pull-down and pull-up resistors are optional features.

1.4.4.1 I/O Applications

To support mixed voltage environments, LVCMOS and Schmitt trigger I/O cells are available at 1.8V, 2.5V, 3.3V interface and 3.3V, 5V tolerant interface. The I/O application diagram is as follows.

Figure 1-2. I/O Applications



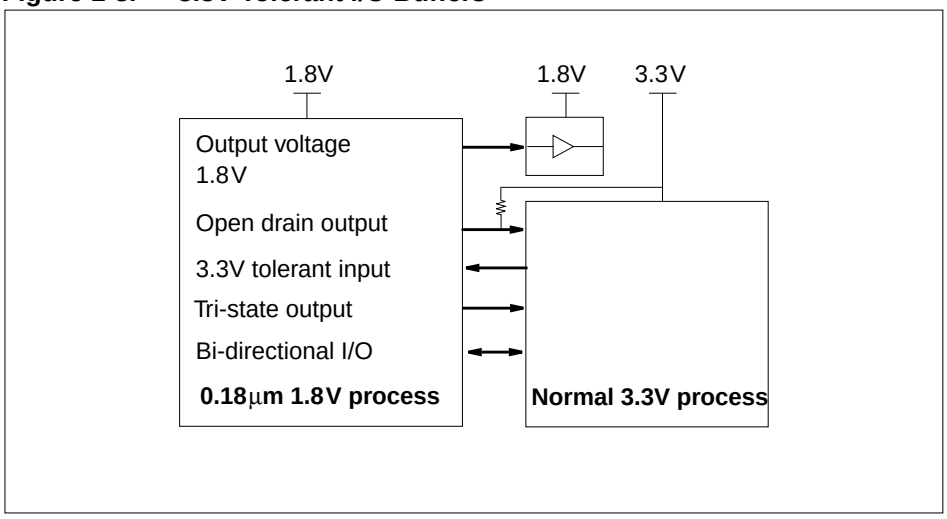
1.4.4.2 I/O Cell Drives Options

To provide flexibility, the designer can choose from various output current drive levels. The choice of current drive level affects propagation delay and noise. Slew rate control helps decrease system noise and output signal overshoot and undershoot caused by the switching of output buffers. The output signal edge slew rates can be slowed down by selecting the high slew rate control cells.

1.4.4.3 3.3V Tolerant I/O Buffers

The STDL131 library is optimized for Samsung's L18L, 0.18µm drawn, process technology. The L18L process technology is optimized for operation at 1.8V. The specified maximum voltage across the thin gate oxide is 1.95V to avoid gate oxide breakdown. A special circuit is available for a 3.6V tolerant LVCMOS driver of up to 6mA. This 3.6V tolerant driver can be used as a normal 1.8V buffer.

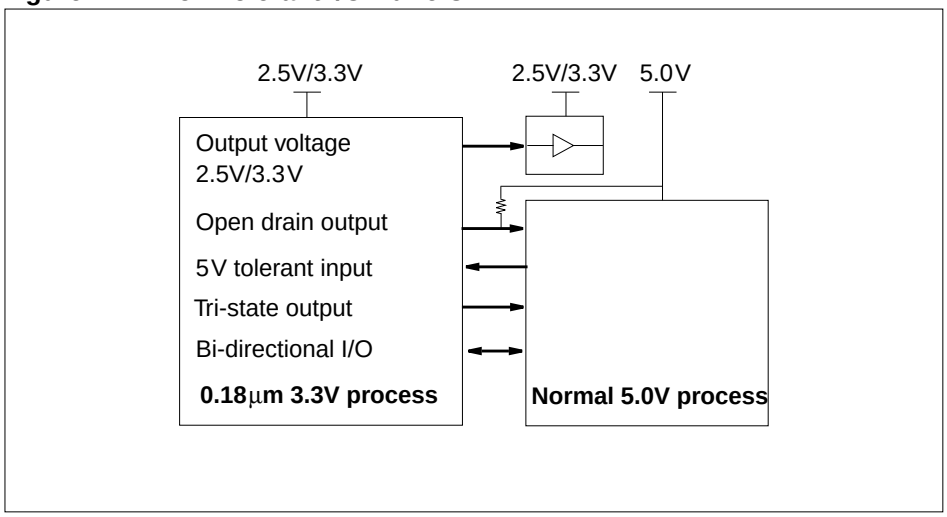
Figure 1-3. 3.3V Tolerant I/O Buffers



1.4.4.4 5V Tolerant I/O Buffers

Samsung's L18L process has a thick gate oxide option that is optimized for 3.3V circuit operation. The specified maximum voltage across the gate oxide of this process option is 5.25V to avoid gate oxide breakdown. A special circuit is available for a 5.25V tolerant LVCMOS driver of up to 6mA. This 5.25V tolerant driver can be used as a normal 2.5V or 3.3V buffer.

Figure 1-4. 5V Tolerant I/O Buffers



1.4.4.5 PCI Buffers

PCI buffers are designed for industry standard PCI high performance 32 or 64 bit local bus applications. The STDL131 library offers input, output, and bi-directional PCI buffers for 33MHz and 66MHz operation compliant with PCI local bus specification 2.2.

1.4.4.6 USB (Universal Serial Bus) Buffers

The STDL131 library offers full speed and low speed USB 1.1 compliant buffers.

1.4.4.7 Other Buffers

The STDL131 library also offers various other I/O buffers including HSTL, SSTL, GTLp, AGP, PECL, and LVDS. For more information about I/O buffers that are not included in this data book, please contact your local Samsung Technology and Design Centers.

1.5 Timings

1.5.1 WIRE LENGTH LOAD

Table 1-1, Table 1-2 and Appendix B show the equivalent standard load matrix for 4, 5, and 6 metal layer interconnect. The equivalent standard load values are a function of the gate count and fanout. These values are based on capacitive loading and are used with wire length estimates which affect propagation delay.

Table 1-1. Equivalent Standard Loads for 4-layer and 5-layer Metal Interconnect

Gate Count	Fanouts										
	1	2	3	4	5	6	7	8	16	32	64
4LM											
5000	0.795	1.635	2.297	3.204	3.840	4.702	5.263	7.047	10.096	17.588	34.192
10000	0.893	2.015	2.840	4.104	4.907	5.976	6.893	8.326	11.992	20.442	40.696
50000	1.224	2.517	3.533	5.909	7.234	8.277	10.830	11.748	14.370	22.346	43.582
100000	1.374	2.799	4.370	6.312	7.549	9.194	12.147	12.744	16.594	24.009	48.909
150000	4.104	6.291	8.021	10.181	11.003	12.494	13.385	14.358	18.222	26.590	51.212
200000	7.429	8.427	9.480	10.929	12.000	13.362	14.297	15.116	19.155	28.159	53.340
300000	8.171	8.952	10.427	12.165	13.326	14.814	15.836	16.726	21.169	31.078	56.183
400000	8.915	10.269	11.297	13.127	14.413	16.045	17.169	18.102	22.883	33.533	59.104
500000	9.944	12.015	12.690	14.722	16.147	17.962	19.210	20.299	24.356	35.700	63.417
600000	10.647	12.681	13.663	15.828	17.344	19.285	20.616	21.822	25.055	36.732	67.431
800000	12.267	15.511	15.875	18.354	20.086	22.314	23.840	25.305	27.076	39.708	75.316
1000000	13.781	16.214	17.944	20.712	22.649	25.145	26.854	28.559	28.954	42.474	78.842
1500000	17.931	21.675	23.578	27.149	29.643	32.879	35.088	37.435	41.425	50.795	95.393
2000000	21.816	26.935	28.858	33.181	36.200	40.127	42.803	45.751	53.533	58.578	106.937
2500000	25.456	32.411	33.799	38.826	42.344	46.911	50.027	53.535	58.472	65.850	123.366
3000000	28.856	35.562	38.419	44.106	48.068	53.251	56.775	60.812	63.080	72.631	138.822
4000000	33.106	39.990	44.076	50.600	55.145	61.094	65.137	69.767	75.133	83.328	158.169
5000000	37.122	48.001	49.423	56.736	61.836	68.503	73.039	76.259	77.242	93.437	166.500
6000000	41.625	52.812	55.417	63.620	69.338	76.812	81.899	87.718	91.773	104.769	196.954
5LM											
5000	0.755	1.553	2.183	3.045	3.647	4.468	5.000	6.694	9.592	16.708	32.482
10000	0.848	1.915	2.698	3.899	4.661	5.677	6.549	7.909	11.391	19.421	38.661
50000	1.163	2.391	3.356	5.614	6.872	7.864	10.289	11.161	13.651	21.228	41.403
100000	1.305	2.659	4.151	5.998	7.171	8.734	11.539	12.106	15.763	22.809	46.464
150000	3.899	5.976	7.620	9.671	10.452	11.870	12.716	13.639	17.311	25.261	48.651
200000	7.057	8.005	9.005	10.381	11.399	12.694	13.582	14.360	18.196	26.751	50.673
300000	7.761	8.505	9.905	11.557	12.659	14.074	15.045	15.889	20.110	29.525	53.374
400000	8.470	9.755	10.732	12.472	13.692	15.242	16.311	17.196	21.740	31.856	56.149
500000	9.446	11.415	12.057	13.986	15.340	17.064	18.250	19.283	23.137	33.915	60.246
600000	10.116	12.047	12.980	15.037	16.476	18.320	19.584	20.732	23.803	34.895	64.059
800000	11.653	14.736	15.082	17.437	19.082	21.198	22.647	24.039	25.722	37.722	71.551
1000000	13.092	15.403	17.047	19.677	21.517	23.887	25.511	27.131	27.507	40.350	74.899
1500000	17.035	20.590	22.399	25.791	28.161	31.236	33.334	35.562	39.354	48.255	90.624
2000000	20.726	25.588	27.415	31.521	34.389	38.122	40.663	43.464	50.856	55.649	101.590
2500000	24.183	30.791	32.108	36.885	40.218	44.564	47.525	50.858	55.549	62.557	117.198
3000000	27.413	33.785	36.498	41.901	45.665	50.588	53.937	57.771	59.927	69.000	131.881
4000000	31.450	37.990	41.872	48.070	52.387	58.039	61.879	66.279	71.377	79.161	150.259
5000000	35.265	45.602	46.952	53.899	58.744	65.078	69.387	74.316	73.379	88.765	158.175
6000000	39.545	50.173	52.645	60.438	65.872	72.972	77.805	83.332	87.185	99.531	187.106
7000000	43.045	60.980	65.492	72.098	76.480	81.466	86.862	96.755	101.602	123.818	246.722
8000000	48.265	68.374	73.437	80.842	85.755	91.350	97.397	108.492	113.482	138.836	251.716

Table 1-2. Equivalent Standard Loads for 6-layer Metal Interconnect

Gate Count	Fanouts										
	1	2	3	4	5	6	7	8	16	32	64
6LM											
5000	0.716	1.472	2.066	2.883	3.456	4.232	4.738	6.342	9.086	15.830	30.773
10000	0.805	1.814	2.557	3.694	4.417	5.377	6.204	7.494	10.793	18.399	36.627
50000	1.102	2.265	3.181	5.318	6.511	7.448	9.748	10.572	12.933	20.112	39.224
100000	1.236	2.519	3.933	5.681	6.795	8.275	10.933	11.470	14.935	21.608	44.017
150000	3.694	5.661	7.218	9.163	9.903	11.244	12.047	12.923	16.399	23.931	46.090
200000	6.687	7.584	8.531	9.836	10.799	12.025	12.868	13.604	17.240	25.344	48.005
300000	7.354	8.057	9.383	10.948	11.994	13.332	14.251	15.053	19.053	27.970	50.564
400000	8.023	9.242	10.167	11.814	12.972	14.440	15.452	16.291	20.596	30.181	53.194
500000	8.950	10.814	11.421	13.250	14.533	16.167	17.289	18.269	21.921	32.129	57.074
600000	9.582	11.413	12.297	14.246	15.610	17.356	18.555	19.639	22.549	33.059	60.688
800000	11.041	13.960	14.287	16.519	18.078	20.082	21.456	22.775	24.370	35.738	67.785
1000000	12.403	14.592	16.149	18.641	20.383	22.631	24.169	25.702	26.059	38.226	70.958
1500000	16.137	19.507	21.220	24.435	26.679	29.592	31.578	33.690	37.283	45.716	85.854
2000000	19.635	24.242	25.972	29.862	32.580	36.116	38.523	41.177	48.181	52.720	96.244
2500000	22.911	29.169	30.419	34.944	38.100	42.220	45.025	48.181	52.625	59.265	111.029
3000000	25.970	32.005	34.576	39.694	43.261	47.927	51.098	54.732	56.773	65.368	124.940
4000000	29.795	35.990	39.669	45.539	49.631	54.984	58.624	62.791	67.620	74.996	142.352
5000000	33.409	43.202	44.480	51.062	55.653	61.653	65.736	68.437	69.517	84.092	149.850
6000000	37.462	47.531	49.875	57.257	62.405	69.131	73.708	78.946	82.596	94.293	177.259
7000000	40.779	57.769	62.045	68.303	72.454	77.179	82.289	91.663	96.253	117.301	233.736
8000000	45.724	64.775	69.570	76.586	81.242	86.541	92.271	102.781	107.509	131.529	238.466

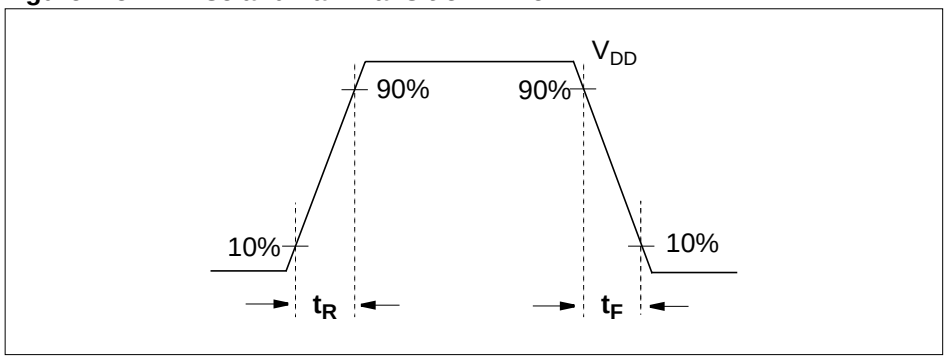
1.5.2 TIMING PARAMETERS

This section defines and discusses AC timing parameters.

1.5.2.1 Rise and Fall Transition Time

Rise time, t_R, and fall time, t_F, are defined as the time that a waveform takes to transition between 10% and 90% of the supply voltage (Figure 1-5).

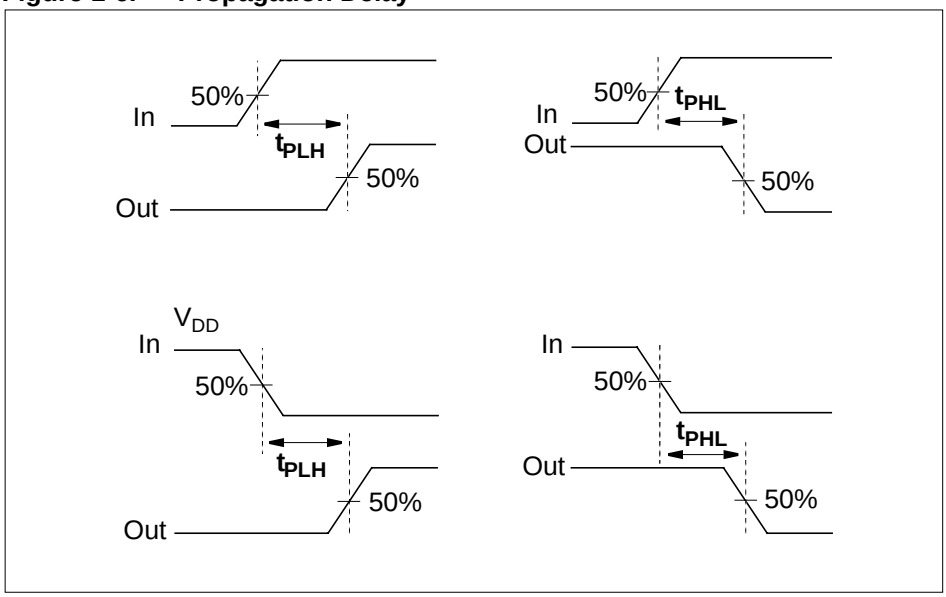
Figure 1-5. Rise and Fall Transition Time



1.5.2.2 Propagation Delay

Propagation delay, t_P, is defined as the time from when the input waveform reaches 50% of the supply voltage to the time that the output waveform reaches 50% of the supply voltage (Figure 1-6).

Figure 1-6. Propagation Delay

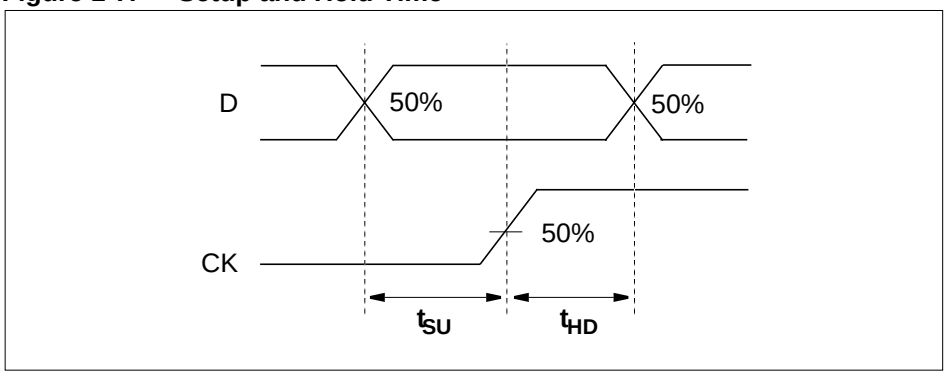


1.5.2.3 Setup and Hold Time

Setup time, t_{SU}, is defined as the minimum time that a data signal must be stable before an active clock transition. Any change to the data signal within this time results in a timing violation, and may result in invalid data being clocked into a circuit (Figure 1-7).

Hold time, t_{HD}, is defined as the minimum time that a data signal must remain valid after an active clock transition. Any change to the data signal within this time results in a timing violation, and may result in invalid data being clocked into a circuit (Figure 1-7).

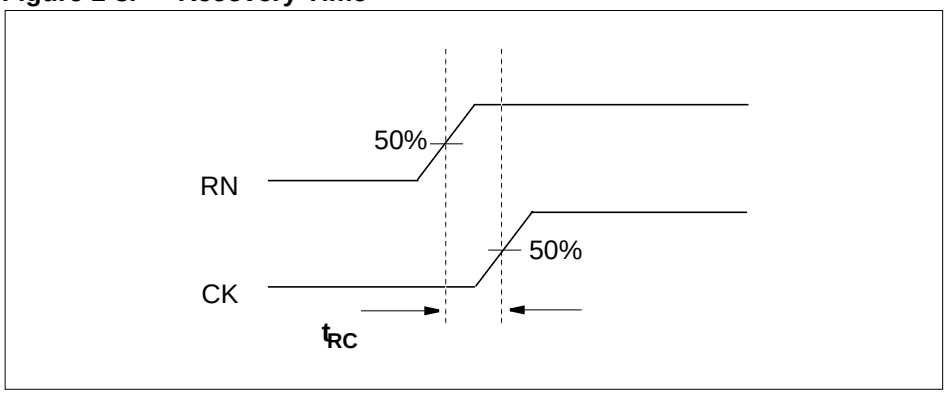
Figure 1-7. Setup and Hold Time



1.5.2.4 Recovery Time

Recovery time, t_{RC}, is defined as the time between the release of an asynchronous control signal from the active state of a circuit to the next active clock edge (Figure 1-8). If an active clock edge occurs too soon after the release of the control signal, a violation occurs that may result in erroneous value being clocked in to the circuit.

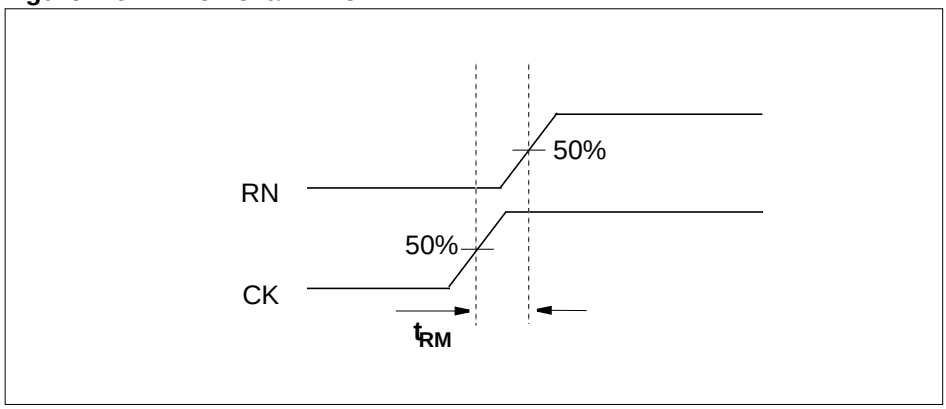
Figure 1-8. Recovery Time



1.5.2.5 Removal Time

Removal time, t_{RM}, is defined as the minimum time between the active clock edge and the release of an asynchronous control signal from the active state (Figure 1-9). If the control signal is released from the active state too soon after an active clock edge, a violation occurs that may result in erroneous value being clocked INTO the circuit.

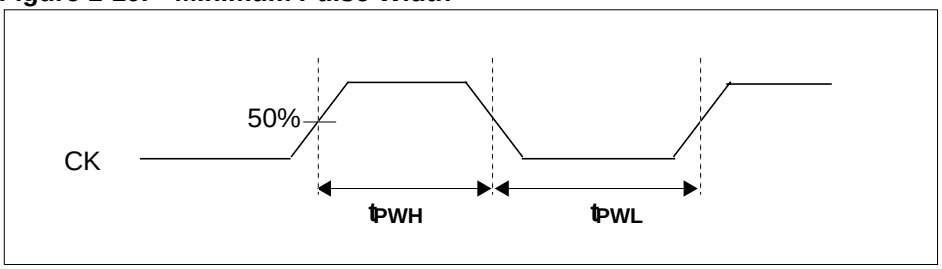
Figure 1-9. Removal Time



1.5.2.6 Minimum Pulse Width

Minimum pulse width, t_{PW}, is defined as the minimum time allowed for the high or low phase of a signal and is measured as the time between the rising and falling edges reaching 50% of the supply voltage (Figure 1-10). A short pulse width results in a timing violation and may result in the signal not being recognized by the circuitry.

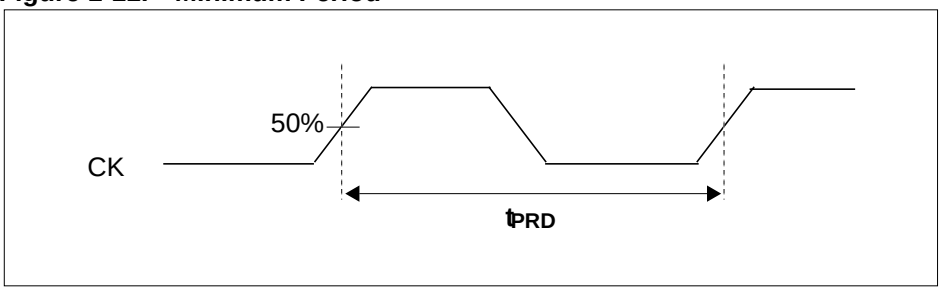
Figure 1-10. Minimum Pulse Width



1.5.2.7 Minimum Period

Minimum period, t_{PRD}, is defined as the minimum allowable time for one complete cycle of a signal (Figure 1-11). A short period results in a timing violation and may result in the signal not being recognized by the circuitry.

Figure 1-11. Minimum Period



1.5.3 BEST AND WORST CASE CONDITIONS

The timing value of best-case (worst-case) can be calculated by using the derating factor derived from the following equations:

$$T_{BC}\ (T_{WC}) = K_P \times K_T \times K_V \times T_{NOM}$$

where,

$T_{BC}\ (T_{WC})$ is a best-case (worst-case) timing.

K_P is the local process derating factor which has different value according to each cell,

K_T is the local temperature derating factor which has different value according to each cell,

K_V is the local voltage derating factor which has different value according to each cell,

T_{NOM} is the nominal timing characterized under typical-process, 25°C and 1.8V power supply.

The best-case (worst-case) timing values may be determined by picking the proper derating values from Table 1-3, Table 1-4 and Table 1-5. Derating factors for conditions between those shown in the tables may be determined by a linear interpolation.

1.5.4 DERATING FACTORS OF STDL131

Cell timing is primarily determined by cell drive capability and loading determined by cell input capacitance and wiring. The following critical variables also affect the timing in a system environment of design:

- Process variation (P)
- Supply voltage (V)
- Junction Temperature (T)

Process variation occurs due to the manufacturing environments and the variation may change the physical characteristics. Its variation affects the electrical characteristics of devices, increasing or decreasing performance and power. On the other hand, to design chips which operate in a wide range of voltage and temperature environments, you have to consider typical-case, worst-case and best-case conditions to compensate for all variations. To yield much more timing accuracy, the cell-specific local derating factor is used in STDL131 standard cells.

For an example, the process, temperature and voltage derating factors for IV cell are as follows in Table 1-3, Table 1-4 and Table 1-5 respectively.

Table 1-3. STDL131 Cell Process Derating Factor (K_P)

Process Factor (K_P)	Slow	Typ	Fast
	1.2227	1.000	0.8833

Table 1-4. STDL131 Cell Temperature Derating Factor (K_T)

Temp. (^oC)	125	85	70	25	0	−40
K_T	1.1186	1.0721	1.0543	1.000	0.9832	0.9500

Table 1-5. STDL131 Cell Voltage Derating Factor (K_V)

Voltage (V)	1.65	1.80	1.95
K_V	1.1303	1.000	0.9340

1.5.5 DELAY MODEL

The STDL131 cell timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout and distributed interconnection wire resistances and capacitances.
- Interconnection wire delay.
- Timing requirement parameters including set up time, hold time, recovery time, skew time, and minimum pulse width.
- Derating factors for junction temperature, power supply voltage, and process variation.

To accomplish accurate timing model, a two dimensional table look-up delay model has been developed. The index variables of this table are input waveform slope and output load capacitance (Figure 1-12). Samsung's SoC design methodology supports an n-dimensional table model, even though a two dimensional model is used.

Figure 1-12. 2-Dimensional Table Delay Model

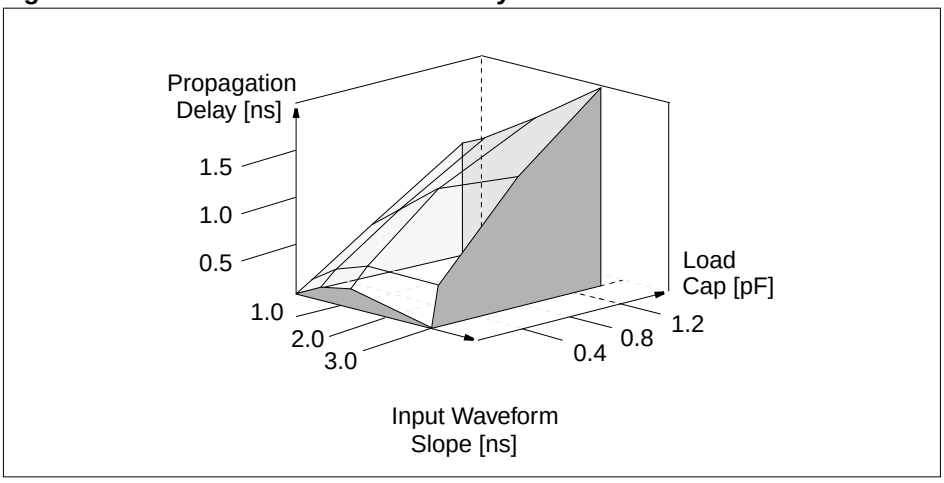


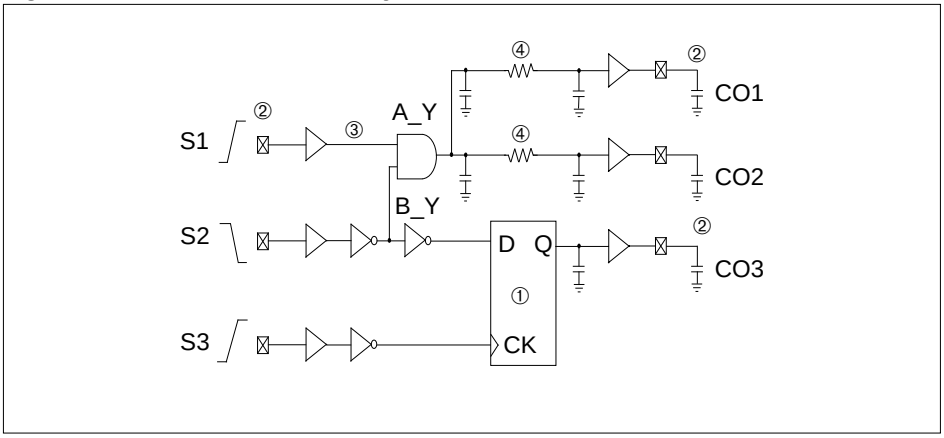
Table 1-6 shows the propagation delay data for a 2-input NAND cell. The data in this table are the high-to-low transition delay times from one of the two input pins to the output pin. The number of points and values of the index variables can differ for each cell.

Table 1-6. Table Delay Model Example

\ CAP[pF] SLOPE[n]	0.008	0.032	0.062	0.124	0.215	0.337
0.019	0.04718	0.08909	0.14084	0.24748	0.40390	0.61356
0.186	0.07759	0.12534	0.17733	0.28437	0.44105	0.65087
0.355	0.09257	0.15618	0.21600	0.32292	0.47948	0.68926
0.693	0.10700	0.19125	0.27178	0.40037	0.55744	0.76677
1.200	0.11522	0.21987	0.32093	0.48507	0.67301	0.88466

Notice that a 5-by-6 table is used. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components, such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a way commonly accepted in the industry. Figure 1-13 summarizes the features of the STDL131 library delay model.

Figure 1-13. Features of Delay Model



① Two dimensional table delay model for output loading and input waveform slope is used. The rise and fall times and delay times of all cell instances are calculated recursively.

② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.

③ Pin to pin delays of cells and interconnection wires are defined.

④ The effect of distributed interconnection wire resistances and capactitances on cell delay is analysed using lumped capacitances.

1.6 Design for Test (DFT) Methodology

Samsung's libraries are designed with DFT in mind. Samsung's DFT methodology includes the ability to include full or partial scan path testing, boundary-scan JTAG for board level testing, Memory BIST, and analog testing. A brief description of the features of Samsung's scan, BIST, and JTAG as well as a more detailed discussion of boundary scan architecture follows.

1.6.1 SCAN DESIGN

- Multiplexed scan flip-flops that minimize area and delay overhead needed to implement scan design.
- Automated design rule checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

1.6.2 BIST (BUILT-IN SELF-TEST)

- Efficient test solution for compiled memory macrocells
- At speed and parallel testing of multiple memories
- Combination with internal scan design and core testing

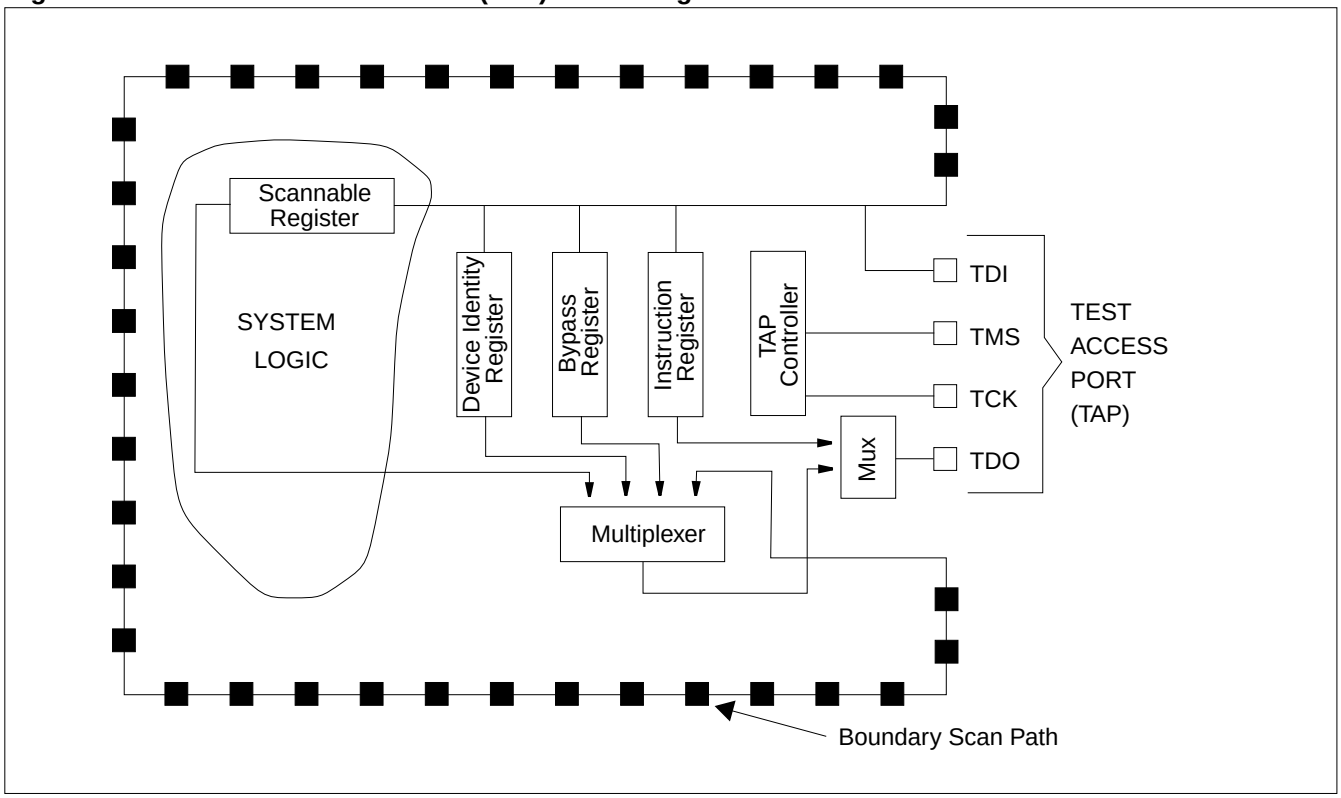
1.6.3 BOUNDARY-SCAN

- IEEE Std 1149.1
- JTAG boundary scan registers implemented with primitive cells
- Boundary -Scan Description Language (BSDL) for board testing
- May be combed with internal scan design and core testing

JTAG Boundary Scan Architecture

Boundary scan architecture contains a TAP (Test Access Port), a TAP controller, an instruction register, and a group of test data registers. The instruction and test data registers are separate shift-register-based paths connected in parallel with a common serial data input and a common serial data output. The common serial data input and output are connected to the TAP, TDI and TDO signals. The TAP controller selects the alternative instruction and test data register paths between TDI and TDO. A schematic view of the top level design of the JTAG test logic architecture is shown in the Figure 1-14.

Figure 1-14. JTAG Test Access Port (TAP) Block Diagram



Functional Block Descriptions

TAP (Test Access Port)

The TAP is a general-purpose port that provides access to many test support functions built into a component including the test logic. It includes three inputs (TCK -Test Clock Signal; TMS -Test Mode Signal; and TDI -Test Data Input) and one output (TDO -Test Data Output) required by the test logic. An optional fourth input (TRSTN -Test Reset) is provided for the asynchronous initialization of the test logic. The values applied at the TMS and TDI pins are sampled on the rising edge of TCK, and the value placed on TDO changes on the falling edge of TCK.

TAP Controller

The TAP controller receives TCK, interprets the signals on TMS, and generates clock and control signals for both instruction and test data registers and for other parts of the test circuit as required.

Instruction Register/Instruction Decoder

Test instructions are shifted into and held by the instruction register. Test instructions include tests to be performed or the test data register addresses to be accessed. A basic 3-bit instruction register and its instruction decoder are provided as macrofunctions in the library.

Test Data Registers

Test data registers include a bypass register, a boundary scan register, a device identification register and other design specific registers. Only the bypass and boundary scan registers are mandatory; the rest are optional.

Test Data Registers Description

Bypass register: The bypass register provides a single-bit serial connection through the circuit when none of the other test data registers are selected. It can be used to allow test data to flow through a given device to the other components in a product without affecting a normal operation.

Boundary scan register: The boundary scan register detects typical production defects in board interconnects, such as opens, and shorts. It also allows access to component inputs and outputs when testing their logic or sample flow-through signals. Special boundary scan register macrocells are provided for this purpose.

Design-specific test data register: These optional registers may be provided to allow access to design-specific test support features in the integrated circuit, such as self-test and scan test.

Device identification register: This is an optional test data register that allows the manufacturer part number and revision to be identified. The 32-bit identification register is partitioned into four fields:

Device version identifier 1st field	The first four bits beginning from MSB	
Device part number	2nd field	16 bits
Manufacturer's JEDEC number	3rd field	11 bits
LSB	4th field	1 bit — tied in High

The ASIC designer is free to fill in the version and part number in any manner as long as all twenty bits are used.
Samsung's JEDEC code: 78 decimal = 1001110

Continuation field (4 bits) = 0000

Contents of device identification register:

XXXX XXXXXXXXXXXXXXX 0000 1001110 1
Users can define these two fields.

1.7 Maximum Fanouts

1.7.1 INTERNAL MACROCELLS

The maximum fanouts for STDL131 primitive cells are tabulated in Table 1-7 and Appendix C. Note that these fanout limitation values are calculated when the rise and fall times of the input signal is 0.186ns. Depending on the rise and fall times, the maximum fanout limitations can be varied case by case.

In the following table the maximum fanout values for all pins of STDL131 internal macrocells are listed.

Table 1-7. Maximum Fanouts of Internal Macrocells
(When input t_R/t_F = 0.186ns, one fanout (SL) = 0.00803pF**)**

Cell Name	Output Pin	Maximum Fanouts
ad2_lp	Y	44
ad2b_lp	Y	44
ad2bd2_lp	Y	88
ad2bd4_lp	Y	178
ad2bd8_lp	Y	356
ad2d2_lp	Y	88
ad2d4_lp	Y	179
ad2d8_lp	Y	351
ad3_lp	Y	44
ad3d2_lp	Y	89
ad3d4_lp	Y	176
ad4_lp	Y	44
ad4d2_lp	Y	88
ad4d4_lp	Y	173
ad5_lp	Y	20
ad5d2_lp	Y	41
ad5d4_lp	Y	179
ao21_lp	Y	19
ao211_lp	Y	12
ao2111_lp	Y	8
ao2111d2_lp	Y	89
ao211d2_lp	Y	24
ao211d4_lp	Y	179
ao21d2_lp	Y	39
ao21d4_lp	Y	177
ao22_lp	Y	19
ao221_lp	Y	11
ao221d2_lp	Y	89
ao221d4_lp	Y	178
ao222_lp	Y	11
ao2222_lp	Y	6
ao2222d2_lp	Y	88
ao2222d4_lp	Y	178
ao222a_lp	Y	16
ao222d2_lp	Y	88
ao222d4_lp	Y	178
ao22a_lp	Y	19
ao22d2_lp	Y	38
ao22d4_lp	Y	179
ao31_lp	Y	18
ao311_lp	Y	10
ao3111_lp	Y	6
ao31d2_lp	Y	37
ao31d4_lp	Y	177
ao32_lp	Y	18
ao321_lp	Y	10
ao322_lp	Y	9
ao32d2_lp	Y	88
ao33_lp	Y	18
ao331_lp	Y	10
ao332_lp	Y	9
busholder_lp	Y	10000
cgln_lp	GCK	43
cglnd2_lp	GCK	87
cglnd4_lp	GCK	176
cglp_lp	GCK	43
cglpd2_lp	GCK	88
cglpd4_lp	GCK	178
dl1d2_lp	Y	89
dl2d2_lp	Y	89
dl5d2_lp	Y	88
dl10d2_lp	Y	89
fa_lp	S	44
	CO	44
fad2_lp	S	89
	CO	88
fd1_lp	Q	43
	QN	43
fd1d2_lp	Q	88
	QN	88
fd1q_lp	Q	43
fd1qd2_lp	Q	88
fd1s_lp	Q	43
	QN	43
fd1sd2_lp	Q	88
	QN	88
fd1sq_lp	Q	43
fd1sqd2_lp	Q	88
fd2_lp	Q	43
	QN	43
fd2d2_lp	Q	89
	QN	88
fd2q_lp	Q	43
fd2qd2_lp	Q	90
fd2s_lp	Q	43
	QN	43
fd2sd2_lp	Q	89
	QN	88
fd2sq_lp	Q	43
fd2sqd2_lp	Q	89
fd3_lp	Q	43
	QN	43
fd3d2_lp	Q	87
	QN	88
fd3q_lp	Q	43
fd3qd2_lp	Q	88
fd3s_lp	Q	43
	QN	43
fd3sd2_lp	Q	88
	QN	88
fd3sq_lp	Q	43
fd3sqd2_lp	Q	88
fd4_lp	Q	44
	QN	43
fd4d2_lp	Q	89
	QN	87

Cell Name	Output Pin	Maximum Fanouts
fd4q_lp	Q	44
fd4qd2_lp	Q	89
fd4s_lp	Q	44
	QN	43
fd4sd2_lp	Q	89
	QN	87
fd4sq_lp	Q	43
fd4sqd2_lp	Q	88
fd5_lp	Q	43
	QN	43
fd5d2_lp	Q	88
	QN	88
fd5s_lp	Q	44
	QN	44
fd5sd2_lp	Q	88
	QN	88
fd6_lp	Q	43
	QN	43
fd6d2_lp	Q	89
	QN	88
fd6s_lp	Q	43
	QN	43
fd6sd2_lp	Q	88
	QN	87
fd7_lp	Q	43
	QN	43
fd7d2_lp	Q	88
	QN	89
fd7s_lp	Q	43
	QN	43
fd7sd2_lp	Q	88
	QN	88
fd8_lp	Q	44
	QN	43
fd8d2_lp	Q	89
	QN	87
fd8s_lp	Q	44
	QN	43
fd8sd2_lp	Q	89
	QN	87
fds2_lp	Q	43
	QN	43
fds2d2_lp	Q	88
	QN	87
fds2s_lp	Q	44
	QN	44
fds2sd2_lp	Q	89
	QN	89
fds3_lp	Q	43
	QN	43
fds3d2_lp	Q	88
	QN	88
fds3s_lp	Q	43
	QN	43
fds3sd2_lp	Q	88
	QN	87
fj2_lp	Q	44
	QN	43
fj2d2_lp	Q	89
	QN	88
fj2s_lp	Q	43
	QN	43
fj2sd2_lp	Q	88
	QN	87

Cell Name	Output Pin	Maximum Fanouts
fj4_lp	Q	43
	QN	44
fj4d2_lp	Q	86
	QN	88
fj4s_lp	Q	44
	QN	43
fj4sd2_lp	Q	89
	QN	87
ft2_lp	Q	44
	QN	43
ft2d2_lp	Q	88
	QN	88
ha_lp	S	44
	CO	44
had2_lp	S	88
	CO	88
iv_lp	Y	44
ivd2_lp	Y	91
ivd3_lp	Y	137
ivd4_lp	Y	184
ivd6_lp	Y	276
ivd8_lp	Y	362
ivd16_lp	Y	722
ivd24_lp	Y	1081
ivt_lp	Y	43
ivtd2_lp	Y	88
ivtd4_lp	Y	178
ivtd8_lp	Y	356
ivtd16_lp	Y	704
ld1_lp	Q	44
	QN	43
ld1d2_lp	Q	88
	QN	88
ld1q_lp	Q	44
ld1qd2_lp	Q	89
ld2_lp	Q	44
	QN	44
ld2d2_lp	Q	87
	QN	88
ld2q_lp	Q	44
ld2qd2_lp	Q	89
ld3_lp	Q	43
	QN	44
ld3d2_lp	Q	87
	QN	89
ld4_lp	Q	43
	QN	44
ld4d2_lp	Q	88
	QN	89
ld5_lp	Q	44
	QN	44
ld5d2_lp	Q	89
	QN	88
ld5q_lp	Q	44
ld5qd2_lp	Q	89
ld6_lp	Q	44
	QN	43
ld6d2_lp	Q	88
	QN	88
ld6q_lp	Q	43
ld6qd2_lp	Q	88
mx2_lp	Y	44
mx2d2_lp	Y	88
mx2d4_lp	Y	178
mx2i_lp	YN	19

Cell Name	Output Pin	Maximum Fanouts
mx2ia_lp	YN	19
mx2id2_lp	YN	39
mx2id2a_lp	YN	39
mx2id4_lp	YN	180
mx2id4a_lp	YN	178
mx4_lp	Y	44
mx4d2_lp	Y	89
mx4d4_lp	Y	175
nd2_lp	Y	43
nd2b_lp	Y	42
nd2bd2_lp	Y	86
nd2bd4_lp	Y	173
nd2bd8_lp	Y	351
nd2d2_lp	Y	88
nd2d4_lp	Y	177
nd2d8_lp	Y	355
nd3_lp	Y	29
nd3b_lp	Y	30
nd3bd2_lp	Y	60
nd3bd4_lp	Y	178
nd3bd8_lp	Y	351
nd3d2_lp	Y	61
nd3d4_lp	Y	179
nd3d8_lp	Y	351
nd4_lp	Y	22
nd4d2_lp	Y	45
nd4d4_lp	Y	177
nd5_lp	Y	43
nd5d2_lp	Y	88
nd5d4_lp	Y	179
nd6_lp	Y	43
nd6d2_lp	Y	88
nd6d4_lp	Y	178
nd8_lp	Y	43
nd8d2_lp	Y	88
nd8d4_lp	Y	178
nid_lp	Y	43
nid16_lp	Y	703
nid2_lp	Y	88
nid3_lp	Y	133
nid4_lp	Y	179
nid6_lp	Y	267
nid8_lp	Y	352
nid24_lp	Y	1051
nit_lp	Y	43
nitd16_lp	Y	701
nitd2_lp	Y	88
nitd4_lp	Y	177
nitd8_lp	Y	356
nr2_lp	Y	20
nr2a_lp	Y	43
nr2b_lp	Y	20
nr2bd2_lp	Y	41
nr2bd4_lp	Y	178
nr2bd8_lp	Y	358
nr2d2_lp	Y	42
nr2d4_lp	Y	177
nr2d8_lp	Y	358
nr3_lp	Y	13
nr3a_lp	Y	26
nr3d2_lp	Y	26
nr3d4_lp	Y	177
nr4_lp	Y	43
nr4d2_lp	Y	88
nr4d4_lp	Y	178

Cell Name	Output Pin	Maximum Fanouts
nr5_lp	Y	43
nr5d2_lp	Y	88
nr5d4_lp	Y	178
nr6_lp	Y	43
nr6d2_lp	Y	88
nr6d4_lp	Y	178
nr8_lp	Y	44
nr8d2_lp	Y	89
nr8d4_lp	Y	177
oa21_lp	Y	20
oa211_lp	Y	20
oa2111_lp	Y	19
oa2111d2_lp	Y	40
oa211d2_lp	Y	40
oa211d4_lp	Y	179
oa21d2_lp	Y	40
oa21d4_lp	Y	179
oa22_lp	Y	18
oa221_lp	Y	18
oa221d2_lp	Y	37
oa221d4_lp	Y	179
oa222_lp	Y	17
oa2222_lp	Y	13
oa2222d2_lp	Y	88
oa2222d4_lp	Y	179
oa222d2_lp	Y	35
oa222d4_lp	Y	180
oa22a_lp	Y	20
oa22d2_lp	Y	38
oa22d2a_lp	Y	40
oa22d4_lp	Y	179
oa22d4a_lp	Y	179
oa31_lp	Y	12
oa311_lp	Y	12
oa3111_lp	Y	11
oa31d2_lp	Y	25
oa31d4_lp	Y	177
oa32_lp	Y	11
oa321_lp	Y	10
oa322_lp	Y	8
oa33_lp	Y	9
or2_lp	Y	43
or2b_lp	Y	43
or2bd2_lp	Y	88
or2bd4_lp	Y	177
or2bd8_lp	Y	356
or2d2_lp	Y	88
or2d4_lp	Y	178
or2d8_lp	Y	351
or3_lp	Y	44
or3d2_lp	Y	89
or3d4_lp	Y	179
or4_lp	Y	43
or4d2_lp	Y	85
or4d4_lp	Y	176
or5_lp	Y	43
or5d2_lp	Y	83
or5d4_lp	Y	177
scg1_lp	Y	30
scg1d2_lp	Y	60
scg2_lp	Y	43
scg2d2_lp	Y	89
scg2d4_lp	Y	178
scg3_lp	Y	30
scg3d2_lp	Y	60

Cell Name	Output Pin	Maximum Fanouts
scg3d4_lp	Y	176
scg4_lp	Y	43
scg4d2_lp	Y	86
scg4d4_lp	Y	169
scg5_lp	Y	43
scg5d2_lp	Y	88
scg5d4_lp	Y	172
scg6_lp	Y	43
scg6d2_lp	Y	88
scg7_lp	Y	43
scg7d2_lp	Y	86
scg8_lp	Y	43
scg8d2_lp	Y	89
scg9_lp	Y	43
scg9d2_lp	Y	89
scg10_lp	Y	43
scg10d2_lp	Y	89
scg11_lp	Y	12
scg11d2_lp	Y	25
scg12_lp	Y	20
scg12d2_lp	Y	41
scg12d4_lp	Y	178
scg13_lp	Y	43
scg13d2_lp	Y	88
scg14_lp	Y	43
scg14d2_lp	Y	85
scg15_lp	Y	29
scg15d2_lp	Y	60
scg16_lp	Y	19
scg16d2_lp	Y	40
scg17_lp	Y	31
scg17d2_lp	Y	85
scg18_lp	Y	30
scg18d2_lp	Y	60
scg19_lp	Y	19
scg19d2_lp	Y	39
scg20_lp	Y	20
scg20d2_lp	Y	41
scg21_lp	Y	13
scg21d2_lp	Y	26
scg22_lp	Y	19
scg22d2_lp	Y	40
xn2_lp	Y	44
xn2d2_lp	Y	88
xn2d4_lp	Y	178
xn3_lp	Y	44
xn3d2_lp	Y	88
xn3d4_lp	Y	174
xo2_lp	Y	44
xo2d2_lp	Y	89
xo2d4_lp	Y	177
xo3_lp	Y	43
xo3d2_lp	Y	87
xo3d4_lp	Y	171

1.7.2 I/O Cells

The maximum fanouts for I/O cells are as follows.

Table 1-8. Maximum Fanouts of I/O Cells

(When input t_R/t_F = 0.186ns, one fanout (SL) = 0.00803pF)

Cell Name	Output Pin	Maximum Fanouts
phic_lp	Y	106
phic_abb_lp	Y	142
phicc_abb_lp	Y	144
phicd_lp	Y	107
phicd_abb_lp	Y	142
phicen_abb_lp	Y	140
phicu_lp	Y	107
phicu_abb_lp	Y	142
phis_lp	Y	107
phis_abb_lp	Y	139
phisd_lp	Y	107
phisd_abb_lp	Y	139
phisu_lp	Y	107
phisu_abb_lp	Y	139
phsckdc2_lp	Y	354
phsckdc4_lp	Y	688
phsckdc6_lp	Y	989
phsckdc8_lp	Y	1248
phsckdcd2_lp	Y	354
phsckdcd4_lp	Y	688
phsckdcd6_lp	Y	989
phsckdcd8_lp	Y	1248
phsckdcu2_lp	Y	354
phsckdcu4_lp	Y	688
phsckdcu6_lp	Y	989
phsckdcu8_lp	Y	1248
phsckds2_lp	Y	354
phsckds4_lp	Y	688
phsckds6_lp	Y	989
phsckds8_lp	Y	1248
phsckdsd2_lp	Y	354
phsckdsd4_lp	Y	688
phsckdsd6_lp	Y	989
phsckdsd8_lp	Y	1248
phsckdsu2_lp	Y	354
phsckdsu4_lp	Y	688
phsckdsu6_lp	Y	989
phsckdsu8_lp	Y	1248
phtic_lp	Y	107
phticd_lp	Y	107
phticu_lp	Y	107
phtis_lp	Y	107
phtisd_lp	Y	107
phtisu_lp	Y	107
phsosck1_lp	YN	86
phsosck17_lp	YN	86
phsosck2_lp	YN	26
phsosck27_lp	YN	26
phsoscm1_lp	YN	33
phsoscm16_lp	YN	33
phsoscm2_lp	YN	275
phsoscm26_lp	YN	276
phsoscm3_lp	YN	331
phsoscm36_lp	YN	336
pic_lp	Y	162
pic_abb_lp	Y	162
picc_abb_lp	Y	164
picd_lp	Y	162
picd_abb_lp	Y	162
picen_abb_lp	Y	156
picu_lp	Y	162
picu_abb_lp	Y	162
pis_lp	Y	159
pis_abb_lp	Y	159
pisd_lp	Y	159
pisd_abb_lp	Y	159
pisu_lp	Y	159
pisu_abb_lp	Y	159
pmic_lp	Y	68
pmic_abb_lp	Y	109
pmicc_abb_lp	Y	110
pmicd_lp	Y	68
pmicd_abb_lp	Y	109
pmicen_abb_lp	Y	106
pmicu_lp	Y	67
pmicu_abb_lp	Y	109
pmis_lp	Y	68
pmis_abb_lp	Y	108
pmisd_lp	Y	67
pmisd_abb_lp	Y	108
pmisu_lp	Y	68
pmisu_abb_lp	Y	108
pmsckdc2_lp	Y	354
pmsckdc4_lp	Y	689
pmsckdc6_lp	Y	991
pmsckdc8_lp	Y	1251
pmsckdcd2_lp	Y	354
pmsckdcd4_lp	Y	689
pmsckdcd6_lp	Y	991
pmsckdcd8_lp	Y	1251
pmsckdcu2_lp	Y	354
pmsckdcu4_lp	Y	689
pmsckdcu6_lp	Y	991
pmsckdcu8_lp	Y	1251
pmsckds2_lp	Y	354
pmsckds4_lp	Y	689
pmsckds6_lp	Y	991
pmsckds8_lp	Y	1251
pmsckdsd2_lp	Y	354
pmsckdsd4_lp	Y	689
pmsckdsd6_lp	Y	991
pmsckdsd8_lp	Y	1251
pmsckdsu2_lp	Y	354
pmsckdsu4_lp	Y	689
pmsckdsu6_lp	Y	991
pmsckdsu8_lp	Y	1251
pmsosck1_lp	YN	87
pmsosck2_lp	YN	26
pmsoscm1_lp	YN	32
pmsoscm2_lp	YN	132
psckdc2_lp	Y	390
psckdc4_lp	Y	759
psckdc6_lp	Y	1096
psckdc8_lp	Y	1392
psckdcd2_lp	Y	390
psckdcd4_lp	Y	759
psckdcd6_lp	Y	1095
psckdcd8_lp	Y	1389
psckdcu2_lp	Y	390
psckdcu4_lp	Y	758
psckdcu6_lp	Y	1095
psckdcu8_lp	Y	1391
psckds2_lp	Y	387
psckds4_lp	Y	736
psckds6_lp	Y	1030

Cell Name	Output Pin	Maximum Fanouts
psckds8_lp	Y	1264
psckdsd2_lp	Y	386
psckdsd4_lp	Y	735
psckdsd6_lp	Y	1027
psckdsd8_lp	Y	1258
psckdsu2_lp	Y	387
psckdsu4_lp	Y	736
psckdsu6_lp	Y	1029
psckdsu8_lp	Y	1261
psosck1_lp	YN	146
psosck2_lp	YN	148
psoscm1_lp	YN	148
psoscm2_lp	YN	148
ptic_lp	Y	160
pticd_lp	Y	160
pticu_lp	Y	160
ptis_lp	Y	156
ptisd_lp	Y	133
ptisu_lp	Y	156

<Condition>

- Library = STDL131
- V_{DD} = 1.8V
- Fanout = 0.00914pF (= input cap for CK pin of FD1_LP)
- Standard Load (SL) = 0.00803pF
- Input slope = 0.186ns
- Maximum output transition time (mott) = 1.2ns
- Maximum frequency ≤ 300MHz
- Net length (μm/fanout): branch net length for each fanout except trunk

Trunk width (μm)	8				In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	2000	5000	2000	5000	
ck2_lp	154	97	52	32	403
ck4_lp	333	258	111	86	806
ck6_lp	505	400	169	134	1210
ck8_lp	668	523	224	175	1612

Trunk width (μm)	0.28		8		In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	2000	5000	2000	5000	
nid_lp	7	-	-	-	43
nid2_lp	25	-	3	-	88
nid3_lp	39	4	11	-	133
nid4_lp	51	9	19	-	179
nid6_lp	70	15	35	15	267
nid8_lp	82	18	50	29	352
nid16_lp	108	23	110	83	703
nid24_lp	119	25	167	132	1051

For high fanout nets including clock net, Samsung strongly recommends using clock tree synthesis.

1.8 PACKAGE CAPABILITY BY PITCH AND LEAD COUNT

See Appendix D for Samsung's package capability as of this writing. The most current package availability and capability can be obtained from your local Samsung Technology and Design Centers.

1.9 Power Dissipation

1.9.1 ESTIMATION OF POWER DISSIPATION IN CMOS CIRCUIT

A primary advantage of CMOS circuits is low power consumption since they draw a very small amount of current under steady state, DC conditions. However, as circuit densities and clock rates increase, the power dissipation in CMOS circuits becomes substantial. Power dissipation in CMOS circuits is affected by various factors such as the number of gates, the switching frequency, and gate output loading.

Circuit operating temperature is an important factor in determining circuit speed and reliability. Circuit power dissipation is a major factor in determining circuit operating temperature. Designers must estimate the power dissipation of a circuit accurately and choose the appropriate package and system operating conditions for the circuit to insure the best performance and reliability.

The following sections describe the components of power dissipation in a CMOS circuit (static and dynamic), and the method of calculating them for the Samsung STDL131 library elements.

1.9.2 STATIC (DC) POWER DISSIPATION

Two types of static or DC current contribute to the total static power dissipation in CMOS circuits - leakage current and input/output current.

Leakage current results from a reverse bias between the well and the substrate region of the CMOS circuit. Since there is no DC current path from power to ground through a CMOS logic gate in steady state, no static current except leakage current flows through the internal circuitry of a CMOS device. The amount of this leakage current is normally on the order of tens of nano amperes and is negligible.

Input/output current flows through I/O buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/pull-down transistor in the input buffers is typically on the order of tens of micro amperes (33µA at 3.3V, 25µA at 2.5V, and 18µA at 1.8V), which is also negligible. Therefore, only the DC current that the output buffers source or sink needs to be counted to estimate total static power dissipation. The DC power dissipation of output and bi-directional buffers is determined by the following formula:

$$P_{DC_OUTPUT}\,[mW] = \left(\sum_{k=1}^{n} (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^{n} ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) / T$$

$$P_{DC_BI}\,[mW] = \left(\sum_{k=1}^{n} (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^{n} ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) \times S_{out} / T$$

where,

n = Number of output and bidirectional buffers

T = Total operation time in output mode

t_H = The sum of logic high state time

t_L = The sum of logic low state time

$t_L + t_H = T$ (assuming that output and bi-directional buffers are not tri-state)

S_{out} is the output mode ratio of bi-directional buffers (typically 0.5)

1.9.3 DYNAMIC (AC) POWER DISSIPATION

When a CMOS logic gate changes state, it draws switching current as a result of charging or discharging a load capacitance, C_L. The power associated with the switching current for a node capacitance, C_L, is

$$C_L \times V_{DD}^2$$

where V_{DD} is the power supply voltage.

In addition to the power dissipated by changing the load capacitance, CMOS circuits consume power due to current flowing from the power supply to ground through the n- and p-channel transistors during switching.

The dynamic power dissipation for an entire chip is difficult to estimate since it depends on the switching activity of the circuit. Samsung has found that switching activity is about 10% on the average and recommends using this number in estimating total dynamic power dissipation.

1.9.4 POWER DISSIPATION IN STDL131

This section describes the equations used to estimate the power dissipation in STDL131. As explained in the previous section, the total power dissipation (P_{TOTAL}) consists of static power dissipation (P_{DC}) and dynamic power dissipation (P_{AC}). Samsung's internal power estimation tool, CubicPower, uses a methodology based on the following equations.

$$P_{TOTAL} = P_{AC} + P_{DC}$$

P_{DC} is negligible in case of CMOS logic in general.

The dynamic power dissipation is caused by four components: input buffers (P_{AC_INPUT}), output buffers (P_{AC_OUTPUT}), bi-directional buffers (P_{AC_BI}), and internal cells ($P_{AC_INTERNAL}$).

$$P_{AC} = P_{AC_INPUT} + P_{AC_OUTPUT} + P_{AC_BI} + P_{AC_INTERNAL}$$

Each term mentioned above is characterized by the following equations:

$$P_{AC_INPUT}\,[mW] = 1.8\times \sum_{i}^{N_1.8V_input}\left(I_{i_eq_p}\times\frac{F_i}{100}\times S_i\right)+2.5\times \sum_{j}^{N_2.5V_input}\left(I_{j_eq_p}\times\frac{F_j}{100}\times S_j\right)$$
$$+3.3\times \sum_{k}^{N_3.3V_input}\left(I_{k_eq_p}\times\frac{F_k}{100}\times S_k\right)+3.24\times \sum_{l}^{N_total_input}(0.001\times S_l\times F_l\times C_{l_inload})$$

$$P_{AC_OUTPUT}\,[mW] = 1.8\times \sum_{i}^{N_1.8V_output}\left(I_{i_eq_p}\times\frac{F_i}{100}\times S_i\right)+2.5\times \sum_{j}^{N_2.5V_output}\left(I_{j_eq_p}\times\frac{F_j}{100}\times S_j\right)+$$
$$3.3\times \sum_{k}^{N_3.3V_output}\left(I_{k_eq_p}\times\frac{F_k}{100}\times S_k\right)+3.24\times \sum_{i}^{N_1.8V_output}(0.001\times S_i\times F_i\times C_{i_outload})+$$
$$6.25\times \sum_{j}^{N_2.5V_output}(0.001\times S_j\times F_j\times C_{j_outload})+10.89\times \sum_{k}^{N_3.3V_output}(0.001\times S_k\times F_k\times C_{k_outload})$$

$$P_{AC_BI}\,[mW] = P_{AC_BI_INPUT}\times(1-S_{out})+P_{AC_BI_OUTPUT}\times S_{out}$$

$$P_{AC_BI_INPUT}\,[mW] = 1.8\times \sum_{i}^{N_1.8V_bi}\left(I_{i_eq_p}\times\frac{F_i}{100}\times S_i\right)+2.5\times \sum_{j}^{N_2.5V_bi}\left(I_{j_eq_p}\times\frac{F_j}{100}\times S_j\right)+$$
$$3.3\times \sum_{k}^{N_3.3V_bi}\left(I_{k_eq_p}\times\frac{F_k}{100}\times S_k\right)+3.24\times \sum_{l}^{N_total_bi}(0.001\times S_l\times F_l\times C_{l_inload})$$

$$P_{AC_BI_OUTPUT}\,[mW] = 1.8\times \sum_{i}^{N_1.8V_bi}\left(I_{i_eq_p}\times\frac{F_i}{100}\times S_i\right)+2.5\times \sum_{j}^{N_2.5V_bi}\left(I_{j_eq_p}\times\frac{F_j}{100}\times S_j\right)+$$
$$3.3\times \sum_{k}^{N_3.3V_bi}\left(I_{k_eq_p}\times\frac{F_k}{100}\times S_k\right)+3.24\times \sum_{i}^{N_1.8V_bi}(0.001\times S_i\times F_i\times C_{i_outload})+$$
$$6.25\times \sum_{j}^{N_2.5V_bi}(0.001\times S_j\times F_j\times C_{j_outload})+10.89\times \sum_{k}^{N_3.3V_bi}(0.001\times S_k\times F_k\times C_{k_outload})$$

$$P_{AC_INTERNAL}\,[mW] = 0.001\times(0.1338\times S+0.0160)\times G\times F+\sum_{i}^{N_macro}(0.001\times P_i\times F_i)$$

where,

N_1.8V_input is the number of 1.8V interface input buffers used,
N_2.5V_input is the number of 2.5V interface input buffers used,
N_3.3V_input is the number of 3.3V interface input buffers used,
N_total_input = N_1.8V_input + N_2.5V_input + N_3.3V_input,
N_1.8V_output is the number of 1.8V interface output buffers used,
N_2.5V_output is the number of 2.5V interface output buffers used,
N_3.3V_output is the number of 3.3V interface output buffers used,
N_1.8V_bi is the number of 1.8V interface bi-directional buffers used,
N_2.5V_bi is the number of 2.5V interface bi-directional buffers used,
N_3.3V_bi is the number of 3.3V interface bi-directional buffer used,
N_total_bi = N_1.8V_bi + N_2.5V_bi + N_3.3V_bi,
N_macro is the number of macro cells used,
G is total gate count of the design,
F is the operating frequency in MHz,
S is the estimated switching activity (typically 0.1 for internal logic and 0.5 for I/O),
S_{out} is the output mode ratio of bi-directional buffers (typically 0.5),
C is the load capacitance in pF,,
P is the characterized power for the i-th hard macro block (μ W/MHz)

1.9.5 TEMPERATURE AND POWER DISSIPATION

The total power dissipation, P_{TOTAL} can be used to find out the device temperature by the following equation:

$$T_J = \theta_{JA} \times P_{TOTAL} + T_A$$

where,

θ_{JA} is the package thermal impedance,

T_J is the junction temperature of the device,

T_A is the ambient temperature.

Thermal impedances of the Samsung packages are given in the following table. The junction temperature, determines the derating factor for the propagation delays and is also used in reliability calculations. Hence, designers can achieve the desired derating factor and reliability targets by choosing appropriate packages and system cooling methods.

Table 1-11. Thermal Impedances of Samsung Plastic Packages

	SOP/TSOP								
Pin Number	**20**	**24**	**28**	**32**	**44**	**50**	**54**	**62**	**66**
θ_{JA}[°C/W]	63	58	41-44	46-56	44-71	39-59	34-56	27-33	34-46

	QFP									
Pin Number	**44**	**48**	**80**	**100**	**120**	**128**	**160**	**208**	**240**	**256**
θ_{JA}[°C/W]	51-62	43-56	43-74	27-61	33-47	43-51	29-51	22-43	28-47	29-42

	TQFP/LQFP							
Pin Number	**32**	**64**	**100**	**144**	**160**	**176**	**208**	**256**
θ_{JA}[°C/W]	68-70	47	37-70	38	35-62	31-34	37-56	30-42

	PBGA			
Pin Number	**272**	**388**	**356 (TEPBGA)**	**452 (TEPBGA)**
θ_{JA}[°C/W]	19-22	16-19	16	14

	SBGA				
Pin Number	**256**	**304**	**352**	**432**	**600**
θ_{JA}[°C/W]	14.1	13.1	11.7	10.2	8.3

1.10 V_{DD}/V_{SS} Rules And Guidelines

Three kinds of power supplies exist in STDL131 providing power to internal and I/O areas:

- Core logic
  – VDD1IH_LP, VDD1IM_LP, VDD1I_LP, VSS3I_LP, VSS2I_LP, VSS1I_LP
- Pre-driver (I/O area)
  – VDD3P_LP, VDD2P_LP, VDD1P_LP, VSS3P_LP, VSS2P_LP, VSS1P_LP
- Output-drive (I/O area)
  – VDD3O_LP, VDD2O_LP, VDD1O_LP, VSS3O_LP, VSS2O_LP, VSS1O_LP

The number of V_{DD} and V_{SS} pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency

1.10.1 BASIC PLACEMENT GUIDELINES

The purpose of these guidelines is to minimize IR drop and noise for reliable device operations.

- Core logic and pre-driver V_{DD}/V_{SS} pads should be evenly distributed on all sides of the chip.
- If you have core block demanding high power (compiled memory, analog), extra power pads should be used to supply that block.
- Power pads for SSO group should be evenly distributed in the SSO group.
- Do not place the quiet signal (analog, reference), analog power (VDDA/VSSA), or bi-directional buffer next to a SSO group.
- Opposite types of power pads (V_{DD}/V_{SS}) should be placed as close together as possible.
- If possible, do not place power pads (V_{DD}/V_{SS}) at the corner of the chip.

1.10.2 VDD1I_LP/VSS1I_LP ALLOCATION GUIDELINES

The purpose of these guidelines is to ensure that the minimum number of core logic power pad pairs are used while meeting the electromigration rules. The number of VDD1I_LP/VSS1I_LP pads required for a specific design is a function of the operating frequency of a chip.

- VDD1I_LP bus width and the number of pads are equal to those of VSS1I
- VDD1I_LP/VSS1I_LP buses and pads should be distributed evenly in the core and on each side of the chip.

The number of VDD1I_LP/VSS1I_LP pad pairs required for a design can be calculated from the following expression:

The number of VDD1I_LP/VSS1I_LP pad pairs =

$$\left\| \left[0.001 \times (0.0743 \times S + 0.0089) \times G \times F + \sum_{i}^{N_macro} (Pi \times Fi) \right] / I_{em} \right\| round-up$$

where,

G = The core (excluding hard macro blocks) size in the gate counts
S = The switching ratio (typically = 0.1)
F = Operating frequency (MHz)
Pi = Characterized current for the i-th hard macro block (mA/MHz)
Fi = Operating frequency for the i-th hard macro block (MHz)
I_{em} = Current limit per V_{DD}/V_{SS} pad pairs based on electromigration rule (40mA)

For reliable device operation and to minimize IR drop, no device should have fewer than 4 VDD1I_LP/VSS1I_LP power pad pairs.

Extra power pad pairs may be needed for high power consuming macro blocks (SRAM, analog blocks, etc.).

1.10.3 VDD1P_LP/VSS1P_LP (VDD2P_LP, 3P_LP/VSS2P_LP, 3P_LP) ALLOCATION GUIDELINES.

These guidelines ensure that adequate input threshold voltage margin is maintained during I/O switching.

The number of VDD1P_LP/VSS1P_LP, VDD2P_LP/VSS2P_LP, VDD3P_LP/VSS3P_LP pads required for a design can be calculated from the following expression:

$$\text{Number_ of_VDD1P_LP/VSS1P_LP (VDD2P_LP, 3P_LP/VSS2P_LP, 3P_L) pairs} = \left\| \frac{I_{eq_p}}{I_{em}} \right\| round-up$$

In the above expression,

I_{eq_p} = ∑(Average current of input/output buffers and bi-direction pre-drivers at maximum operational I/O frequency) [mA] (Refer to Table 1-12, Table 1-13 and Table 1-14)

$$I_{eq_p} = \sum_{i}^{N_input} \left(I_{eq_p_in} \times \frac{F_i}{100} \right) + \sum_{j}^{N_output} \left(I_{j_eq_p_out} \times \frac{F_j}{100} \right) + \sum_{k}^{N_bi} \left[\left(I_{k_eq_p_in} \times \frac{F_k}{100} \right) (1 - S_{out}) + \left(I_{k_eq_p_out} \times \frac{F_k}{100} \right) \times S_{out} \right]$$

where,

N_input is the number of input buffers used,
N_output is the number of output buffers used,
N_bi is the number of bi-directional buffers used,
F is the operating frequency in MHz,
S_{out} is the output mode ratio of bi-directional buffers (typically 0.5),
I_{em} = Current limit per V_{DD}/V_{SS} pad pairs based on electromigration rules. (40mA)

Table 1-12. 1.8V Interface

Input Buffer Type		CMOS			Schmitt Trigger			
Ieq_p_in (mA)	Normal	0.27			0.28			
	Tolerant	0.28			0.29			
Output Pre-Driver Type		**CMOS Driver**			**Tristate**			
		B1–4	**B8–16**	**B20–24**	**T1–4**	**T8–16**	**T20–24**	**Tolerant**
Ieq_p_out (mA)	Normal	0.11	0.36	0.53	0.15	0.41	0.58	0.28
	Slew-rate	0.11	0.35	0.47	0.16	0.41	0.52	0.29

Table 1-13. 2.5V Interface

Input Buffer Type		CMOS			Schmitt Trigger			
Ieq_p_in (mA)	Normal	0.27			0.30			
	Tolerant	0.27			0.32			
Output Pre-Driver Type		**CMOS Driver**			**Tristate**			
		B1–4	**B8–16**	**B20–24**	**T1–4**	**T8–16**	**T20–24**	**Tolerant**
Ieq_p_out (mA)	Normal	0.27	0.60	0.84	0.28	0.67	0.77	0.39
	Slew-rate	0.29	0.55	0.72	0.29	0.61	0.71	0.42

Table 1-14. 3.3V Interface

Input Buffer Type		CMOS			Schmitt Trigger			
Ieq_p_in (mA)	Normal	0.32			0.38			
	Tolerant	0.31			0.34			
Output Pre-Driver Type		**CMOS Driver**			**Tristate**			
		B1–4	**B8–16**	**B20–24**	**T1–4**	**T8–16**	**T20–24**	**Tolerant**
Ieq_p_out (mA)	Normal	0.32	0.57	0.77	0.34	0.59	0.79	0.35
	Slew-rate	0.30	0.57	0.75	0.31	0.58	0.76	0.43

For reliable device operation and minimum IR voltage drop, at least 4 pairs of VDD1P_LP/VSS1P_LP (VDD2P_LP, 3P_LP/VSS2P_LP, 3P_LP) power pads should be used.

1.10.4 VDD1O_LP/VSS1O_LP (VDD2O_LP, 3O_LP/VSS2O_LP, 3O_LP) ALLOCATION GUIDE

SSO (Simultaneous Switching Output) current induced in power and ground wire inductances can cause system failure because of voltage spikes during switching. To calculate the number of output drive power pads, the SSO noise as well as the current limit based on electromigration and taken into consideration. SSO is defined as the number of outputs switching simultaneously in 1ns windows, such as bus type buffers.

NOTE: In case of heavy loads, high frequency, and low package inductance, the number of power pads per SSO block could be determined by the electromigration rule rather than the SSO noise limit. So, the number of power pads per SSO block should be determined as the worst case power pad number determined by SSO noise and electromigration rules.

1) Number of power pads for an SSO block

- Number of power pads for an SSO block under the limit of SSO noise

- Calculating the number of power pad for each SSO group from the following expressions:

$$NVDDO_{each_SSO} = \frac{number_of_SSO}{NBvdd} \times L_{pg} \times \frac{1}{D_{SSO_mode}}$$

$$NVSSO_{each_SSO} = \frac{number_of_SSO}{NBvss} \times L_{pg} \times \frac{1}{D_{SSO_mode}}$$

where,

$NVDDO_{each_sso}$ = Number of VDD1O_LP (VDD2O_LP, 3O_LP) pad required for each SSO group,

$NVSSO_{each_sso}$ = Number of VSS1O_LP (VSS2O_LP, 3O_LP) pad required for each SSO group,

NBvdd = Number of buffers per VDD1O_LP (VDD2O_LP, 3O_LP) power pad with 1nH lead inductance (Refer to Table 1-18),

NBvss = Number of buffers per VSS1O_LP (VSS2O_LP, 3O_LP) ground pas with 1nH lead inductance,

L_{pg} = Package lead frame inductance of power/ground (Refer to 1.8 package capability by pitch and lead count),

$D_{sso_mode} = D_{L_mode} \times D_{P_mode} \times D_{V_mode} \times D_{T_mode} \times D_{C_mode}$ (Refer to Table 1-15, Table 1-16 and Table 1-17)

D_{L_mode} = Lead inductance derating factor

D_{P_mode} = Process derating factor

D_{V_mode} = Voltage derating factor

D_{T_mode} = Temperature derating factor

D_{C_mode} = Cload derating factor (mode is either V_{DD} or V_{SS}.)

Table 1-15. Derating Equation (External 1.8V Interface)

Item	Mode	Equation		Range
		1–8mA	12–24mA	
Package Lead	D_{L_vdd}	0.3214 × Lpg + 0.3571	0.0435 × Lpg + 1.3043	3nH ≤ Lpg ≤ 10nH
		0.1964 × Lpg + 1.6071	0.0435 × Lpg + 1.3043	10nH ≤ Lpg ≤ 15nH
	D_{L_vss}	0.0095 × Lpg + 1.7143	0.0400 × Lpg + 1.2000	3nH ≤ Lpg ≤ 10nH
		0.0381 × Lpg + 1.4286	0.0400 × Lpg + 1.2000	10nH ≤ Lpg ≤ 15nH
Process	D_{P_vdd}	1.0000	1.0000	best
		1.2857	1.1667	typical
		2.8125	1.4167	worst
	D_{P_vss}	1.0000	1.0000	best
		1.3333	1.0400	typical
		3.0476	1.2400	worst
Voltage	D_{V_vdd}	– 2.0833 × voltage + 4.9464	– 1.1594 × voltage + 3.2174	1.65 ≤ voltage ≤ 1.8
		– 1.3095 × voltage + 3.5536	– 0.8696 × voltage + 2.6957	1.8 ≤ voltage ≤ 1.95
	D_{V_vss}	– 2.8571 × voltage + 6.3619	– 0.2067 × voltage + 1.5200	1.65 ≤ voltage ≤ 1.8
		– 1.4603 × voltage + 3.8476	– 0.2067 × voltage + 1.5200	1.8 ≤ voltage ≤ 1.95
Temperature	D_{T_vdd}	0.00071 × temp + 1.0000	0.0035 × temp + 1.0000	– 40 ≤ temp ≤ 25
		0.00032 × temp + 1.0097	0.0008 × temp + 1.0672	25 ≤ temp ≤ 80
	D_{T_vss}	0.0053 × temp + 1.0000	0.0016 × temp + 1.0000	– 40 ≤ temp ≤ 25
		0.0052 × temp + 1.0035	0.0022 × temp + 0.9855	25 ≤ temp ≤ 80
Cload	D_{C_vdd}	0.0379 × cload + 0.6205	0.0261 × cload + 0.7391	10pF ≤ cload ≤ 30pF
		0.0183 × cload + 1.2098	0.0043 × cload + 1.3913	30pF ≤ cload ≤ 50pF
	D_{C_vss}	0.0438 × cload + 0.5619	0.0100 × cload + 0.9000	10pF ≤ cload ≤ 30pF
		0.0109 × cload + 1.5476	0.0020 × cload + 1.1400	30pF ≤ cload ≤ 50pF

Table 1-16. Derating Equation (External 2.5V Interface)

Item	Mode	Equation		Range
		1–8mA	12–24mA	
Package Lead	D_{L_vdd}	0.0123 × Lpg + 1.9753	0.1250 × Lpg + 0.8333	3nH ≤ Lpg ≤ 10nH
		0.0247 × Lpg + 1.8518	0.0833 × Lpg + 1.2500	10nH ≤ Lpg ≤ 15nH
	D_{L_vss}	0.0430 × Lpg + 1.5054	0.0769 × Lpg + 0.7692	3nH ≤ Lpg ≤ 10nH
		0.0323 × Lpg + 1.6129	0.0385 × Lpg + 1.1538	10nH ≤ Lpg ≤ 15nH
Process	D_{P_vdd}	1.0000	1.0000	best
		1.6419	1.2083	typical
		2.0778	1.3750	worst
	D_{P_vss}	1.0000	1.0000	best
		1.1613	1.0000	typical
		1.7742	1.1154	worst
Voltage	D_{V_vdd}	– 1.2962 × voltage + 4.4012	– 0.2083 × voltage + 1.6042	2.3 ≤ voltage ≤ 2.5
		– 0.8025 × voltage + 3.1667	– 0.4167 × voltage + 2.1250	2.5 ≤ voltage ≤ 2.7
	D_{V_vss}	– 1.1828 × voltage + 4.1075	– 0.1923 × voltage + 1.5577	2.3 ≤ voltage ≤ 2.5
		– 0.7527 × voltage + 3.0323	– 0.3846 × voltage + 2.0385	2.5 ≤ voltage ≤ 2.7
Temperature	D_{T_vdd}	0.000988 × temp + 1.0000	0.001667 × temp + 1.0000	– 40 ≤ temp ≤ 25
		0.000455 × temp + 1.0135	0.000758 × temp + 1.0227	25 ≤ temp ≤ 80
	D_{T_vss}	0.00258 × temp + 1.0000	0.00154 × temp + 1.0000	– 40 ≤ temp ≤ 25
		0.00254 × temp + 1.00097	0.00209 × temp + 0.9860	25 ≤ temp ≤ 80
Cload	D_{C_vdd}	0.0370 × cload + 0.6296	0.0125 × cload + 0.8750	10pF ≤ cload ≤ 30pF
		0.0154 × cload + 1.2778	0.0021 × cload + 1.1875	30pF ≤ cload ≤ 50pF
	D_{C_vss}	0.0328 × cload + 0.6720	0.0115 × cload + 0.8846	10pF ≤ cload ≤ 30pF
		0.0199 × cload + 1.0591	0.0019 × cload + 1.1730	30pF ≤ cload ≤ 50pF

Table 1-17. Derating Equation (External 3.3V Interface)

Item	Mode	Equation		Range
		1–8mA	12–24mA	
Package Lead	D_{L_vdd}	0.0320 × Lpg + 1.6800	0.0857 × Lpg + 1.1429	3nH ≤ Lpg ≤ 10nH
		0.0320 × Lpg + 1.6800	0.1143 × Lpg + 0.8571	10nH ≤ Lpg ≤ 15nH
	D_{L_vss}	0.0609 × Lpg + 1.4634	0.0909 × Lpg + 0.9091	3nH ≤ Lpg ≤ 10nH
		0.0244 × Lpg + 1.8293	0.0455 × Lpg + 1.3636	10nH ≤ Lpg ≤ 15nH
Process	D_{P_vdd}	1.0000	1.0000	best
		1.4720	1.2000	typical
		1.7520	1.3428	worst
	D_{P_vss}	1.0000	1.0000	best
		1.1097	1.0000	typical
		1.4390	1.1304	worst
Voltage	D_{V_vdd}	– 0.7200 × voltage + 3.5120	– 0.2857 × voltage + 2.0000	3.0 ≤ voltage ≤ 3.3
		– 0.4533 × voltage + 2.6320	– 0.1905 × voltage + 1.6857	3.3 ≤ voltage ≤ 3.6
	D_{V_vss}	– 0.5285 × voltage + 2.8536	– 0.1515 × voltage + 1.5909	3.0 ≤ voltage ≤ 3.3
		– 0.3658 × voltage + 2.3170	– 0.3030 × voltage +2.0909	3.3 ≤ voltage ≤ 3.6
Temperature	D_{T_vdd}	0.00096 × temp + 1.0000	0.00114 × temp + 1.0000	– 40 ≤ temp ≤ 25
		0.00058 × temp + 1.0095	0.00156 × temp + 0.9896	25 ≤ temp ≤ 80
	D_{T_vss}	0.00146 × temp + 1.0000	0.00364 × temp + 1.0000	– 40 ≤ temp ≤ 25
		0.00155 × temp + 0.9978	0.00165 × temp + 1.0496	25 ≤ temp ≤ 80
Cload	D_{C_vdd}	0.0236 × cload + 0.7640	0.0257 × cload + 0.7429	10pF ≤ cload ≤ 30pF
		0.0264 × cload + 0.6800	0.0043 × cload + 1.3857	30pF ≤ cload ≤ 50pF
	D_{C_vss}	0.0207 × cload + 0.7927	0.01136 × cload + 0.8864	10pF ≤ cload ≤ 30pF
		0.0177 × cload + 0.8841	0.00227 × cload + 1.1591	30pF ≤ cload ≤ 50pF

Table 1-18. NBvdd/NBvss Parameter (Process = best, Volt = 1.95V/2.7V/3.6V, Temp = 0˚C, Llead = 1nH)

Buffer Type	Voltage Type	Normal		Slew-Rate Medium (sm)		Slew-Rate High (sh)	
		NBvdd	NBvss	NBvdd	NBvss	NBvdd	NBvss
pob1 (pot1)_lp	1.8 Interface	261	249	–	–	–	–
pob2 (pot2)_lp		201	174	–	–	–	–
pob4 (pot4)_lp		101	95	123	95	–	–
pob8 (pot8)_lp		37	33	47	41	–	–
pob12 (pot12)_lp		26	25	37	36	57	59
pob16 (pot16)_lp		22	23	29	35	51	57
pob20 (pot20)_lp		20	21	28	34	42	41
pob24 (pot24)_lp		18	20	26	33	39	39
ptot1_lp	3.3V Tolerant for 1.8V Interface	476	423	–	–	–	–
ptot2_lp		340	356	–	–	–	–
ptot4_lp		122	95	164	120	–	–
ptot6_lp		63	52	136	63	–	–
pmob1 (pmot1)_lp	2.5V Interface	239	231	–	–	–	–
pmob2 (pmot2)_lp		163	153	–	–	–	–
pmob4 (pmot4)_lp		73	84	97	98	–	–
pmob8 (pmot8)_lp		34	37	47	43	–	–
pmob12 (pmot12)_lp		25	29	32	31	49	45
pmob16 (pmot16)_lp		22	23	29	29	46	44
pmob20 (pmot20)_lp		21	18	26	27	40	38
pmob24 (pmot24)_lp		20	15	25	26	32	27
pmtot1_lp	5V Tolerant for 2.5V Interface	316	288	–	–	–	–
pmtot2_lp		202	228	–	–	–	–
pmtot4_lp		117	146	118	148	–	–
pmtot6_lp		53	64	59	65	–	–
phob1 (phot1)_lp	3.3V Interface	280	203	–	–	–	–
phob2 (phot2)_lp		200	124	–	–	–	–
phob4 (phot4)_lp		113	74	113	77	–	–
phob8 (phot8)_lp		58	33	69	33	–	–
phob12 (phot12)_lp		41	24	49	25	58	28
phob16 (phot16)_lp		32	21	38	22	47	23
phob20 (phot20)_lp		28	18	33	19	45	22
phob24 (phot24)_lp		26	15	32	18	44	21
phtot1_lp	5V Tolerant for 3.3V Interface	545	274	–	–	–	–
phtot2_lp		338	167	–	–	–	–
phtot4_lp		227	80	254	86	–	–
phtot6_lp		116	48	123	55	–	–

NOTE: pob1_lp means 1mA output driver cell, and pob12_lp means 12mA output driver cell.

- Calculating the number of required power pad for total SSO from the following expression:

  NVDDO1sso = ∑NVDDOeach_sso
  NVSSO1sso = ∑NVSSOeach_sso

When there are SSO blocks which are not switching simultaneously with the others, only maximum value of NVDDO_each_sso/NVSSO_each_sso among the SSO block should be used.

In the above formula,

NVDDOsso = Number of VDD1O_LP (VDD2O_LP, 3O_LP) pad per total SSO buffers
NVSSOsso = Number of VSS1O_LP (VSS2O_LP, 3O_LP) pad per total SSO buffers

- Number of power pads for SSO block limit of electromigration rules:

- Calculating the following expression:

$$NVDDO2_{SSO}/NVSSO2_{SSO} = \frac{I_{eq_o}}{I_{em}}$$

$$I_{eq_o} = \sum_{i}^{N_SSO_output} (0.001 \times C_{i_outload} \times V_i \times F_i \times S_i) + \sum_{j}^{N_SSO_bi} (0.001 \times C_{j_outload} \times V_j \times F_j \times S_j \times S_{j_out})$$

where,

N_SSO_output is the number of simultaneous switching output buffers used,
N_SSO_bi is the number of simultaneous switching bi-directional buffers used,
$C_{outload}$ = Output load capacitance [pF],
V = Operating voltage [V],
F = Maximum I/O operating frequency [MHz],
S = Switching ratio (typically 0.5),
S_{out} = Output mode ratio of bi-directional buffers (typically 0.5),
I_{em} = Current limit per V_{DD}/V_{SS} pad pairs based on electromigration rule. (40mA)

2) Number of power pads for non-SSO block

- Calculating the following expression:

$$NVDDO_{non_SSO}/NVSSO_{non_SSO} = \frac{I_{eq_o}}{I_{em}}$$

$$I_{eq_o} = \sum_{i}^{N_non_SSO_output} (0.001 \times C_{i_outload} \times V_i \times F_i \times S_i) + \sum_{j}^{N_non_SSO_bi} (0.001 \times C_{j_outload} \times V_j \times F_j \times S_j \times S_{j_out})$$

where,

N_non_SSO_output is the number of non-simultaneous switching output buffers used,
N_non_SSO_bi is the number of non-simultaneous switching bi-directional buffers used,
$C_{outload}$ = Output load capacitance [pF],
V = Operating voltage [V],
F = Maximum I/O operating frequency [MHz],
S = Switching ratio (typically 0.5),
S_{out} = Output mode ratio of bi-directional buffers (typically 0.5),
I_{em} = Current limit per V_{DD}/V_{SS} pad pairs based on electromigration rule. (40mA)

3) Total number of power pads for VDD1O_LP/VSS1O_LP (VDD2O_LP, 3O_LP/VSS2O_LP, 3O_LP)

- Calculating the following expressions:

$$\text{Number of VDD1O_LP (VDD2O_LP, 3O_LP)} = \left\| \max(NVDDO1_{SSO}, NVDDO2_{SSO}) + NVDDO_{non_SSO} \right\| \text{ round-up}$$

$$\text{Number of VSS1O_LP (VSS2O_LP, 3O_LP)} = \left\| \max(NVSSO1_{SSO}, NVSSO2_{SSO}) + NVSSO_{non_SSO} \right\| \text{ round-up}$$

When open drain type buffers are used, you can consider using VSS1O_LP (VSS2O_LP, 3O_LP) pads since they have current sink only.

1.11 Crystal Oscillator Consideration

1.11.1 OVERVIEW

The STDL131 library contains a cell commonly referred to as an *on-chip oscillator*. The on-chip oscillator itself is not really an oscillator, but is an amplifier suitable for being used as the feedback amplifier in an oscillator circuit. With proper selection of off-chip components (crystal or ceramic resonator, resistors and capacitors) this oscillator circuit performs better than other types of clock oscillators.

It is very important to select suitable off-chip components for the on-chip oscillator circuitry. It should be noted, however, that Samsung cannot assume responsibility for writing specifications for the off-chip components or for the performance of the finished oscillator design in production since the optimization of the crystal oscillator circuit will be specific to a given application. Samsung does, however, spec and guarantee the performance of the on-chip oscillator cell.

1.11.2 OSCILLATOR DESIGN CONSIDERATIONS

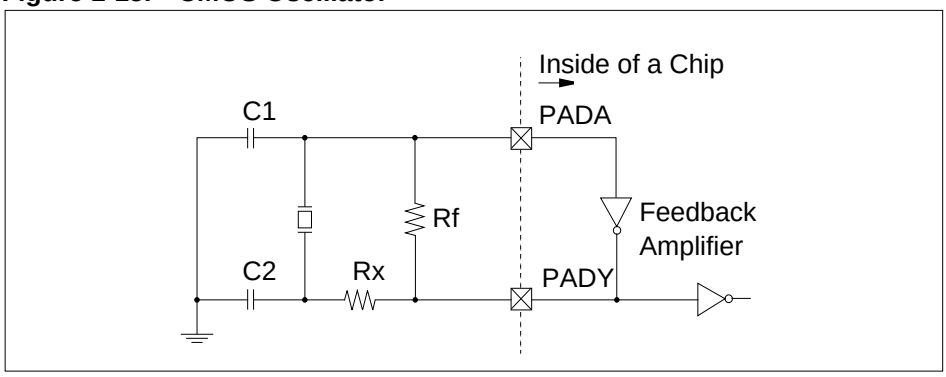
SoC designers have a number of options for clocking the system. A primary decision is whether to use an on-chip oscillator or an external oscillator. If the choice is to use an on-chip oscillator, the designer must then choose the type of oscillator and off-chip component values. These decisions will be based on both economic and technical requirements.The following section discusses some of the factors to be considered.

1.11.2.1 On-Chip Oscillator

In most cases, the on-chip oscillator with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components commonly used for the oscillator circuit are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistors, Rf and Rx, as shown in the figure below.

Figure 1-15. CMOS Oscillator



1.11.2.2 Crystal Specifications

Specifications for an appropriate crystal are not very critical. Any fundamental mode crystal of medium or better quality can be used. Crystal resistance affects start-up time and steady state amplitude but can be compensated by the choice of C1 and C2, however, the lower the crystal resistance, the better. A discussion of external R and C components follows below.

1.11.2.3 Oscillation Frequency

The oscillation frequency is mainly determined by the crystal. The on-chip oscillator has little effect on the frequency.

The influence of the on-chip oscillator on frequency results from its input and output (pin-to-ground) capacitances which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance which parallels the crystal. The input and pin-to-pin capacitances are about 7pF each.

1.11.2.4 C1 and C2 Selection

Optimal values for C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and on application-specific requirements for start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability because of various reset and initialization requirements.

Accuracy of the oscillator frequency is less commonly critical, as when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 15pF (but they don't have to be either).

Increasing the value of these capacitors above 40pF or 50pF improves frequency stability, but also increases the start-up time. If the capacitors are too large (several hundred pF), the oscillator won't start up at all.

1.11.2.5 Rf and Rx Selection

A large Rf (1M ohm) holds the on-chip oscillator (a CMOS inverter) in it linear region allowing it to oscillate. The inverter has a fairly low output resistance which de-stabilizes the oscillator circuit. Rx of several K-ohms is added to the feedback network, as shown in Figure 1-15 to stabilize the oscillator circuit.

At higher oscillator frequencies, a 20pF or 30pF capacitor is sometimes used in place of Rx to compensate for internal propagation delay.

1.11.3 PCB CONSIDERATIONS

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and VSS pins. If possible, use dedicated V_{SS} and V_{DD} pins for the on-chip oscillator.

In addition, surrounding oscillator components with "quiet" traces (V_{DD} and V_{SS}) will alleviate capacitive coupling to signals having fast edges. To minimize inductive coupling, the PCB layout should minimize lead, wire, and trace lengths for oscillator components.

Paths that need to be checked are:
- PADA through the resonator to PADY;
- PADA through C1 to the V_{SS} pin;
- PADY through C2 to the V_{SS} pin.

It is not unusual to find that the ground ends of C1 and C2 connect to the V_{SS} pin through long traces on the board.

1.11.4 TROUBLESHOOTING OSCILLATOR PROBLEMS

The cause of an oscillator problem may be difficult to find once detected. Below are some suggested first things to investigate if an oscillator problem is detected.

There may be significant differences in stray capacitances between the test fixture and the actual application, particularly if the actual application is on a multi-layer board. This may result in an oscillator problem occurring in the test fixture that will not occur on the board, or a problem occurring on the board that cannot be duplicated on the test fixture.

Noise glitches not present in the test fixture but present on the application board may be another cause for an oscillator problem. Capacitive coupling between the oscillator circuitry and other signal should be investigated. Inductive coupling is also possible if there is a lead, trace, or wire with a large current nearby.

Finally, it should not be overlooked that software problems can mimic the symptoms of a slow-starting oscillator or incorrect frequency. Software should also be invigilated.

Electrical Characteristics

2

Contents

DC Electrical Characteristics 2-1

DC ELECTRICAL CHARACTERISTICS

The following tables define the DC electrical characteristics for the standard LVCMOS I/O buffers described in Chapter 4: “Input/Output Cells.” The DC electrical characteristics for oscillator and standard bus interface I/O buffers such as USB and PCI follow the desciptions of those buffer cells in Chapter 4.

V_{DD} = 1.8V± 0.15V, T_A = –40 to 85°C, V_{EXT} = 3.3V ± 0.3V (In case of 3.3V tolerant)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		1.27			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.57	
VT	Switching threshold			$0.5V_{DD}$		V
VT^+	Schmitt trigger, positive-going threshold	CMOS			1.27	V
VT–	Schmitt trigger, negative-going threshold	CMOS	0.57			V
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
	Input buffer with pull-down		5	18	40	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–40	–18	–5	
V_{OH}	High level output voltage					V
	Type B1 to B24	I_{OH} = –1µA	V_{DD} – 0.05			
	Type B1	I_{OH} = –1mA	1.2			
	Type B2	I_{OH} = –2mA				
	Type B4	I_{OH} = –4mA				
	Type B8	I_{OH} = –8mA				
	Type B12	I_{OH} = –12mA				
	Type B16	I_{OH} = –16mA				
	Type B20	I_{OH} = –20mA				
	Type B24	I_{OH} = –24mA				
V_{OL}	Low level output voltage					V
	Type B1 to B24	I_{OL} = 1µA			0.05	
	Type B1	I_{OL} = 1mA			0.45	
	Type B2	I_{OL} = 2mA				
	Type B4	I_{OL} = 4mA				
	Type B8	I_{OL} = 8mA				
	Type B12	I_{OL} = 12mA				
	Type B16	I_{OL} = 16mA				
	Type B20	I_{OL} = 20mA				
	Type B24	I_{OL} = 24mA				
I_{OZ}	Tri-state output leakage current	V_{OUT} =V_{SS} or V_{DD}	–10		10	µA
I_{DD}	Quiescent supply current				100	µA
C_{IN}	Input capacitance	Any input and Bi-directional buffers			4	pF
C_{OUT}	Output capacitance	Any output buffer			4	pF

V_{DD} = 2.5V± 0.2V, T_A = –40 to 85°C, V_{EXT} = 5V ± 0.25V (In case of 5V tolerant)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		1.7			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.7	
VT	Switching threshold			$0.5V_{DD}$		V
VT^+	Schmitt trigger, positive-going threshold	CMOS			1.7	V
VT –	Schmitt trigger, negative-going threshold	CMOS	0.7			V
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
	Input buffer with pull-down		10	25	50	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–50	–25	–10	
V_{OH}	High level output voltage					V
	Type B1 to B24	I_{OH} = –1µA	V_{DD} – 0.05			
	Type B1	I_{OH} = –1mA	1.9			
	Type B2	I_{OH} = –2mA				
	Type B4	I_{OH} = –4mA				
	Type B8	I_{OH} = –8mA				
	Type B12	I_{OH} = –12mA				
	Type B16	I_{OH} = –16mA				
	Type B20	I_{OH} = –20mA				
	Type B24	I_{OH} = –24mA				
V_{OL}	Low level output voltage					V
	Type B1 to B24	I_{OL} = 1µA			0.05	
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA				
	Type B4	I_{OL} = 4mA				
	Type B8	I_{OL} = 8mA				
	Type B12	I_{OL} = 12mA				
	Type B16	I_{OL} = 16mA				
	Type B20	I_{OL} = 20mA				
	Type B24	I_{OL} = 24mA				
I_{OZ}	Tri-state output leakage current	V_{OUT} =V_{SS} or V_{DD}	–10		10	µA
I_{DD}	Quiescent supply current				100	µA
C_{IN}	Input capacitance	Any input and Bi-directional buffers			4	pF
C_{OUT}	Output capacitance	Any output buffer			4	pF

V_{DD} = 3.3V± 0.3V, T_A = –40 to 85°C, V_{EXT} = 5V ± 0.25V (In case of 5V tolerant)

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					V
	LVCMOS interface		2.0			
V_{IL}	Low level input voltage					V
	LVCMOS interface				0.8	
VT	Switching threshold			1.4		V
VT^+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT–	Schmitt trigger, negative-going threshold	CMOS	0.8			V
I_{IH}	High level input current					µA
	Input buffer	$V_{IN} = V_{DD}$	–10		10	
	Input buffer with pull-down		10	33	60	
I_{IL}	Low level input current					µA
	Input buffer	$V_{IN} = V_{SS}$	–10		10	
	Input buffer with pull-up		–60	–33	–10	
V_{OH}	High level output voltage					V
	Type B1 to B24	I_{OH} = –1µA	V_{DD} – 0.05			
	Type B1	I_{OH} = –1mA	2.4			
	Type B2	I_{OH} = –2mA				
	Type B4	I_{OH} = –4mA				
	Type B8	I_{OH} = –8mA				
	Type B12	I_{OH} = –12mA				
	Type B16	I_{OH} = –16mA				
	Type B20	I_{OH} = –20mA				
	Type B24	I_{OH} = –24mA				
V_{OL}	Low level output voltage					V
	Type B1 to B24	I_{OL} = 1µA			0.05	
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA				
	Type B4	I_{OL} = 4mA				
	Type B8	I_{OL} = 8mA				
	Type B12	I_{OL} = 12mA				
	Type B16	I_{OL} = 16mA				
	Type B20	I_{OL} = 20mA				
	Type B24	I_{OL} = 24mA				
I_{OZ}	Tri-state output leakage current	V_{OUT} =V_{SS} or V_{DD}	–10		10	µA
I_{DD}	Quiescent supply current				100	µA
C_{IN}	Input capacitance	Any input and Bi-directional buffers			4	pF
C_{OUT}	Output capacitance	Any output buffer			4	pF

Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
V_{DD}	DC supply voltage	1.8V V_{DD}	2.7	V
		2.5V V_{DD}	3.8	
		3.3V V_{DD}	4.8	
V_{IN}	DC input voltage	1.8V input buffer	2.7	
		2.5V input buffer	3.8	
		3.3V input buffer	4.8	
		1.8V interface/3.3V tolerant input buffer	3.8	
		3.3V interface/5V tolerant input buffer	6.5	
V_{OUT}	DC output voltage	1.8V output buffer	2.7	
		2.5V output buffer	3.8	
		3.3V output buffer	4.8	
		1.8V interface/3.3V tolerant output buffer	3.8	
		3.3V interface/5V tolerant output buffer	6.5	
I_{Latch}	Latch up current	± 200		mA
T_{STG}	Storage temperature	–65 to 150		°C

Recommended Operating Conditions

Symbol	Parameter	Rating			Unit
			Min	Max	
V_{DD}	DC supply voltage for internal (=V_{DDIN})	1.8V V_{DD}	1.65	1.95	V
	DC supply voltage for I/O block (=V_{DDIO})	1.8V V_{DD}	1.65	1.95	
		2.5V V_{DD}	2.3	2.7	
		3.3V V_{DD}	3.0	3.6	
	DC supply voltage for analog core (=V_{DDA})	1.8V V_{DD}	1.8 – 5%	1.8 + 5%	
		2.5V V_{DD}	2.5 – 5%	2.5 + 5%	
		3.3V V_{DD}	3.3 – 5%	3.3 + 5%	
V_{IN}	DC input voltage	1.8V input buffer	–0.1	V_{DDIO}+0.15	
		2.5V input buffer	–0.2	V_{DDIO}+0.2	
		3.3V input buffer	–0.3	V_{DDIO}+0.3	
		1.8V interface/3.3V tolerant input buffer	–0.1	3.6	
		3.3V interface/5V tolerant input buffer	–0.3	5.5	
V_{OUT}	DC output voltage	1.8V output buffer	–0.1	V_{DDIO}+0.15	
		2.5V output buffer	–0.2	V_{DDIO}+0.2	
		3.3V output buffer	–0.3	V_{DDIO}+0.3	
		1.8V interface/3.3V tolerant output buffer	–0.1	3.6	
		3.3V interface/5V tolerant output buffer	–0.3	5.5	
T_A	Commercial temperature range			0 to 70	°C
	Industrial temperature range			–40 to 85	

Internal Macrocells

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OVERVIEW

This chapter contains data sheets for standard logic macrocells; combinational logic cells, flip-flops, latches, bus holder, internal clock drivers, decoders, adders, multiplexers and integrated clock-gating cells. The electrical characteristics of each cell follow each cell's description. A summary table in the following pages list the entire STDL131 standard logic macrocell library by the cell type along with the cell description page number. Moreover, each section begins with a table containing a brief functional description of each cell in that section.

SUMMARY TABLES

Logic Cells

Cell Type	Cell Name	Page
AND Cell	AD2_LP/AD2D2_LP/AD2D4_LP/AD2D8_LP	3-14
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	ND3B_LP/ND3BD2_LP/ND3BD4_LP/ND3BD8_LP	3-32
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	NR4_LP/NR4D2_LP/NR4D4_LP	3-55
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Exclusive-NOR Cell	XN2_LP/XN2D2_LP/XN2D4_LP	3-80
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Cell Type	Cell Name	Page
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	AO22_LP/AO22D2_LP/AO22D4_LP	3-94
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	AO221_LP/AO221D2_LP/AO221D4_LP	3-97
	AO222_LP/AO222D2_LP/AO222D4_LP	3-100
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	AO2222_LP/AO2222D2_LP/AO2222D4_LP	3-105
	AO31_LP/AO31D2_LP/AO31D4_LP	3-109
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Latches

Cell Type	Cell Name	Page
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Bus Holder

Cell Type	Cell Name	Page
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Internal Clock Drivers

Cell Type	Cell Name	Page
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Adders

Cell Type	Cell Name	Page
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Multiplexers

Cell Type	Cell Name	Page
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2 > 1 Inverting Mux	MX2I_LP/MX2ID2_LP/MX2ID4_LP	3-333
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4 > 1 Non-Inverting Mux	MX4_LP/MX4D2_LP/MX4D4_LP	3-338

Integrated Clock-Gating Cells

Cell Type	Cell Name	Page
Integrated Clock-Gating Cells	CGLN_LP/CGLND2_LP/CGLND4_LP	3-343
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Cell Names & Function Descriptions

Cell Name	Function Description
AD2_LP	2-Input AND with 1X Drive
AD2D2_LP	2-Input AND with 2X Drive
AD2D4_LP	2-Input AND with 4X Drive
AD2D8_LP	2-Input AND with 8X Drive
AD2B_LP	2-Input AND with one Inverted Input, 1X Drive
AD2BD2_LP	2-Input AND with one Inverted Input, 2X Drive
AD2BD4_LP	2-Input AND with one Inverted Input, 4X Drive
AD2BD8_LP	2-Input AND with one Inverted Input, 8X Drive
AD3_LP	3-Input AND with 1X Drive
AD3D2_LP	3-Input AND with 2X Drive
AD3D4_LP	3-Input AND with 4X Drive
AD4_LP	4-Input AND with 1X Drive
AD4D2_LP	4-Input AND with 2X Drive
AD4D4_LP	4-Input AND with 4X Drive
AD5_LP	5-Input AND with 1X Drive
AD5D2_LP	5-Input AND with 2X Drive
AD5D4_LP	5-Input AND with 4X Drive
ND2_LP	2-Input NAND with 1X Drive
ND2D2_LP	2-Input NAND with 2X Drive
ND2D4_LP	2-Input NAND with 4X Drive
ND2D8_LP	2-Input NAND with 8X Drive
ND2B_LP	2-Input NAND with one Inverted Input, 1X Drive
ND2BD2_LP	2-Input NAND with one Inverted Input, 2X Drive
ND2BD4_LP	2-Input NAND with one Inverted Input, 4X Drive
ND2BD8_LP	2-Input NAND with one Inverted Input, 8X Drive
ND3_LP	3-Input NAND with 1X Drive
ND3D2_LP	3-Input NAND with 2X Drive
ND3D4_LP	3-Input NAND with 4X Drive
ND3D8_LP	3-Input NAND with 8X Drive
ND3B_LP	3-Input NAND with one Inverted Input, 1X Drive
ND3BD2_LP	3-Input NAND with one Inverted Input, 2X Drive
ND3BD4_LP	3-Input NAND with one Inverted Input, 4X Drive
ND3BD8_LP	3-Input NAND with one Inverted Input, 8X Drive
ND4_LP	4-Input NAND with 1X Drive
ND4D2_LP	4-Input NAND with 2X Drive
ND4D4_LP	4-Input NAND with 4X Drive
ND5_LP	5-Input NAND with 1X Drive
ND5D2_LP	5-Input NAND with 2X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
ND5D4_LP	5-Input NAND with 4X Drive
ND6_LP	6-Input NAND with 1X Drive
ND6D2_LP	6-Input NAND with 2X Drive
ND6D4_LP	6-Input NAND with 4X Drive
ND8_LP	8-Input NAND with 1X Drive
ND8D2_LP	8-Input NAND with 2X Drive
ND8D4_LP	8-Input NAND with 4X Drive
NR2_LP	2-Input NOR with 1X Drive
NR2A_LP	NR2 with 2X P-Transistor, 1X N-Transistor
NR2D2_LP	2-Input NOR with 2X Drive
NR2D4_LP	2-Input NOR with 4X Drive
NR2D8_LP	2-Input NOR with 8X Drive
NR2B_LP	2-Input NOR with one Inverted Input, 1X Drive
NR2BD2_LP	2-Input NOR with one Inverted Input, 2X Drive
NR2BD4_LP	2-Input NOR with one Inverted Input, 4X Drive
NR2BD8_LP	2-Input NOR with one Inverted Input, 8X Drive
NR3_LP	3-Input NOR with 1X Drive
NR3A_LP	3-Input NOR with 2X P-Transistor, 1X N-Transistor
NR3D2_LP	3-Input NOR with 2X Drive
NR3D4_LP	3-Input NOR with 4X Drive
NR4_LP	4-Input NOR with 1X Drive
NR4D2_LP	4-Input NOR with 2X Drive
NR4D4_LP	4-Input NOR with 4X Drive
NR5_LP	5-Input NOR with 1X Drive
NR5D2_LP	5-Input NOR with 2X Drive
NR5D4_LP	5-Input NOR with 4X Drive
NR6_LP	6-Input NOR with 1X Drive
NR6D2_LP	6-Input NOR with 2X Drive
NR6D4_LP	6-Input NOR with 4X Drive
NR8_LP	8-Input NOR with 1X Drive
NR8D2_LP	8-Input NOR with 2X Drive
NR8D4_LP	8-Input NOR with 4X Drive
OR2_LP	2-Input OR with 1X Drive
OR2D2_LP	2-Input OR with 2X Drive
OR2D4_LP	2-Input OR with 4X Drive
OR2D8_LP	2-Input OR with 8X Drive
OR2B_LP	2-Input OR with one Inverted Input, 1X Drive
OR2BD2_LP	2-Input OR with one Inverted Input, 2X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
OR2BD4_LP	2-Input OR with one Inverted Input, 4X Drive
OR2BD8_LP	2-Input OR with one Inverted Input, 8X Drive
OR3_LP	3-Input OR with 1X Drive
OR3D2_LP	3-Input OR with 2X Drive
OR3D4_LP	3-Input OR with 4X Drive
OR4_LP	4-Input OR with 1X Drive
OR4D2_LP	4-Input OR with 2X Drive
OR4D4_LP	4-Input OR with 4X Drive
OR5_LP	5-Input OR with 1X Drive
OR5D2_LP	5-Input OR with 2X Drive
OR5D4_LP	5-Input OR with 4X Drive
XN2_LP	2-Input Exclusive-NOR with 1X Drive
XN2D2_LP	2-Input Exclusive-NOR with 2X Drive
XN2D4_LP	2-Input Exclusive-NOR with 4X Drive
XN3_LP	3-Input Exclusive-NOR with 1X Drive
XN3D2_LP	3-Input Exclusive-NOR with 2X Drive
XN3D4_LP	3-Input Exclusive-NOR with 4X Drive
XO2_LP	2-Input Exclusive-OR with 1X Drive
XO2D2_LP	2-Input Exclusive-OR with 2X Drive
XO2D4_LP	2-Input Exclusive-OR with 4X Drive
XO3_LP	3-Input Exclusive-OR with 1X Drive
XO3D2_LP	3-Input Exclusive-OR with 2X Drive
XO3D4_LP	3-Input Exclusive-OR with 4X Drive
AO21_LP	2-AND into 2-NOR with 1X Drive
AO21D2_LP	2-AND into 2-NOR with 2X Drive
AO21D4_LP	2-AND into 2-NOR with 4X Drive
AO211_LP	2-AND into 3-NOR with 1X Drive
AO211D2_LP	2-AND into 3-NOR with 2X Drive
AO211D4_LP	2-AND into 3-NOR with 4X Drive
AO2111_LP	2-AND into 4-NOR with 1X Drive
AO2111D2_LP	2-AND into 4-NOR with 2X Drive
AO22_LP	Two 2-ANDs into 2-NOR with 1X Drive
AO22D2_LP	Two 2-ANDs into 2-NOR with 2X Drive
AO22D4_LP	Two 2-ANDs into 2-NOR with 4X Drive
AO22A_LP	2-AND and 2-NOR into 2-NOR with 1X Drive
AO221_LP	Two 2-ANDs into 3-NOR with 1X Drive
AO221D2_LP	Two 2-ANDs into 3-NOR with 2X Drive
AO221D4_LP	Two 2-ANDs into 3-NOR with 4X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
AO222_LP	Three 2-ANDs into 3-NOR with 1X Drive
AO222D2_LP	Three 2-ANDs into 3-NOR with 2X Drive
AO222D4_LP	Three 2-ANDs into 3-NOR with 4X Drive
AO222A_LP	Inverting 2-of-3 Majority with 1X Drive
AO2222_LP	Four 2-ANDs into 4-NOR with 1X Drive
AO2222D2_LP	Four 2-ANDs into 4-NOR with 2X Drive
AO2222D4_LP	Four 2-ANDs into 4-NOR with 4X Drive
AO31_LP	3-AND into 2-NOR with 1X Drive
AO31D2_LP	3-AND into 2-NOR with 2X Drive
AO31D4_LP	3-AND into 2-NOR with 4X Drive
AO311_LP	3-AND into 3-NOR with 1X Drive
AO3111_LP	3-AND into 4-NOR with 1X Drive
AO32_LP	3-AND and 2-AND into 2-NOR with 1X Drive
AO32D2_LP	3-AND and 2-AND into 2-NOR with 2X Drive
AO321_LP	3-AND and 2-AND into 3-NOR with 1X Drive
AO322_LP	3-AND and Two 2-ANDs into 3-NOR with 1X Drive
AO33_LP	Two 3-ANDs into 2-NOR with 1X Drive
AO331_LP	Two 3-ANDs into 3-NOR with 1X Drive
AO332_LP	Two 3-ANDs and 2-AND into 3-NOR with 1X Drive
OA21_LP	2-OR into 2-NAND with 1X Drive
OA21D2_LP	2-OR into 2-NAND with 2X Drive
OA21D4_LP	2-OR into 2-NAND with 4X Drive
OA211_LP	2-OR into 3-NAND with 1X Drive
OA211D2_LP	2-OR into 3-NAND with 2X Drive
OA211D4_LP	2-OR into 3-NAND with 4X Drive
OA2111_LP	2-OR into 4-NAND with 1X Drive
OA2111D2_LP	2-OR into 4-NAND with 2X Drive
OA22_LP	Two 2-ORs into 2-NAND with 1X Drive
OA22D2_LP	Two 2-ORs into 2-NAND with 2X Drive
OA22D4_LP	Two 2-ORs into 2-NAND with 4X Drive
OA22A_LP	2-OR and 2-NAND into 2-NAND with 1X Drive
OA22D2A_LP	2-OR and 2-NAND into 2-NAND with 2X Drive
OA22D4A_LP	2-OR and 2-NAND into 2-NAND with 4X Drive
OA221_LP	Two 2-ORs into 3-NAND with 1X Drive
OA221D2_LP	Two 2-ORs into 3-NAND with 2X Drive
OA221D4_LP	Two 2-ORs into 3-NAND with 4X Drive
OA222_LP	Three 2-ORs into 3-NAND with 1X Drive
OA222D2_LP	Three 2-ORs into 3-NAND with 2X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
OA222D4_LP	Three 2-ORs into 3-NAND with 4X Drive
OA2222_LP	Four 2-ORs into 4-NAND with 1X Drive
OA2222D2_LP	Four 2-ORs into 4-NAND with 2X Drive
OA2222D4_LP	Four 2-ORs into 4-NAND with 4X Drive
OA31_LP	3-OR into 2-NAND with 1X Drive
OA31D2_LP	3-OR into 2-NAND with 2X Drive
OA31D4_LP	3-OR into 2-NAND with 4X Drive
OA311_LP	3-OR into 3-NAND with 1X Drive
OA3111_LP	3-OR into 4-NAND with 1X Drive
OA32_LP	3-OR and 2-OR into 2-NAND with 1X Drive
OA321_LP	3-OR and 2-OR into 3-NAND with 1X Drive
OA322_LP	3-OR and Two 2-ORs into 3-NAND with 1X Drive
OA33_LP	Two 3-ORs into 2-NAND with 1X Drive
SCG1_LP	2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 1X Drive
SCG1D2_LP	2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 2X Drive
SCG2_LP	Two 2-ANDs into 2-OR with 1X Drive
SCG2D2_LP	Two 2-ANDs into 2-OR with 2X Drive
SCG2D4_LP	Two 2-ANDs into 2-OR with 4X Drive
SCG3_LP	Two 2-NANDs into 3-NAND with 1X Drive
SCG3D2_LP	Two 2-NANDs into 3-NAND with 2X Drive
SCG3D4_LP	Two 2-NANDs into 3-NAND with 4X Drive
SCG4_LP	Two (two 2-ANDs into 2-NOR)s into 2-NAND with 1X Drive
SCG4D2_LP	Two (two 2-ANDs into 2-NOR)s into 2-NAND with 2X Drive
SCG4D4_LP	Two (two 2-ANDs into 2-NOR)s into 2-NAND with 4X Drive
SCG5_LP	Three 2-ANDs into 3-OR with 1X Drive
SCG5D2_LP	Three 2-ANDs into 3-OR with 2X Drive
SCG5D4_LP	Three 2-ANDs into 3-OR with 4X Drive
SCG6_LP	2-AND into 2-OR with 1X Drive
SCG6D2_LP	2-AND into 2-OR with 2X Drive
SCG7_LP	2-NAND and (2-AND into 2-NOR) into 2-NAND with 1X Drive
SCG7D2_LP	2-NAND and (2-AND into 2-NOR) into 2-NAND with 2X Drive
SCG8_LP	2-AND into 3-OR with 1X Drive
SCG8D2_LP	2-AND into 3-OR with 2X Drive
SCG9_LP	2-OR into 2-AND with 1X Drive
SCG9D2_LP	2-OR into 2-AND with 2X Drive
SCG10_LP	Two 2-ORs into 2-AND with 1X Drive
SCG10D2_LP	Two 2-ORs into 2-AND with 2X Drive
SCG11_LP	Two 2-NORs into 3-NOR with 1X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
SCG11D2_LP	Two 2-NORs into 3-NOR with 2X Drive
SCG12_LP	2-NAND into 2-NOR with 1X Drive
SCG12D2_LP	2-NAND into 2-NOR with 2X Drive
SCG12D4_LP	2-NAND into 2-NOR with 4X Drive
SCG13_LP	2-NOR into 2-NAND with 1X Drive
SCG13D2_LP	2-NOR into 2-NAND with 2X Drive
SCG14_LP	2-NAND into 2-NAND with 1X Drive
SCG14D2_LP	2-NAND into 2-NAND with 2X Drive
SCG15_LP	2-NAND into 3-NAND with 1X Drive
SCG15D2_LP	2-NAND into 3-NAND with 2X Drive
SCG16_LP	2-OR with one inverted input into 2-NAND with 1X Drive
SCG16D2_LP	2-OR with one inverted input into 2-NAND with 2X Drive
SCG17_LP	2-AND into 2-NOR into 2-NAND with 1X Drive
SCG17D2_LP	2-AND into 2-NOR into 2-NAND with 2X Drive
SCG18_LP	2-AND into 2-NOR into 3-NAND with 1X Drive
SCG18D2_LP	2-AND into 2-NOR into 3-NAND with 2X Drive
SCG19_LP	2-AND into 2-AND into 2-NOR with 1X Drive
SCG19D2_LP	2-AND into 2-AND into 2-NOR with 2X Drive
SCG20_LP	2-NOR into 2-NOR with 1X Drive
SCG20D2_LP	2-NOR into 2-NOR with 2X Drive
SCG21_LP	2-NOR into 3-NOR with 1X Drive
SCG21D2_LP	2-NOR into 3-NOR with 2X Drive
SCG22_LP	2-NAND into 2-OR into 2-NAND with 1X Drive
SCG22D2_LP	2-NAND into 2-OR into 2-NAND with 2X Drive
DL1D2_LP	1ns Delay Cell with 2X Drive
DL2D2_LP	2ns Delay Cell with 2X Drive
DL5D2_LP	5ns Delay Cell with 2X Drive
DL10D2_LP	10ns Delay Cell with 2X Drive
IV_LP	Inverter with 1X Drive
IVD2_LP	Inverter with 2X Drive
IVD3_LP	Inverter with 3X Drive
IVD4_LP	Inverter with 4X Drive
IVD6_LP	Inverter with 6X Drive
IVD8_LP	Inverter with 8X Drive
IVD16_LP	Inverter with 16X Drive
IVD24_LP	Inverter with 24X Drive
IVT_LP	Inverting Tri-State Buffer with Enable High, 1X Drive
IVTD2_LP	Inverting Tri-State Buffer with Enable High, 2X Drive

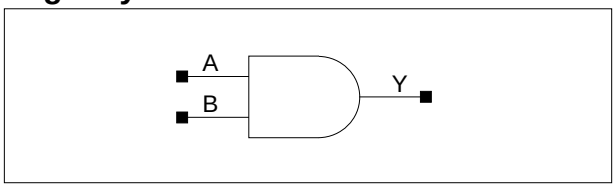
Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
IVTD4_LP	Inverting Tri-State Buffer with Enable High, 4X Drive
IVTD8_LP	Inverting Tri-State Buffer with Enable High, 8X Drive
IVTD16_LP	Inverting Tri-State Buffer with Enable High, 16X Drive
NID_LP	Non-Inverting Buffer with 1X Drive
NID2_LP	Non-Inverting Buffer with 2X Drive
NID3_LP	Non-Inverting Buffer with 3X Drive
NID4_LP	Non-Inverting Buffer with 4X Drive
NID6_LP	Non-Inverting Buffer with 6X Drive
NID8_LP	Non-Inverting Buffer with 8X Drive
NID16_LP	Non-Inverting Buffer with 16X Drive
NID24_LP	Non-Inverting Buffer with 24X Drive
NIT_LP	Non-Inverting Tri-State Buffer with Enable High, 1X Drive
NITD2_LP	Non-Inverting Tri-State Buffer with Enable High, 2X Drive
NITD4_LP	Non-Inverting Tri-State Buffer with Enable High, 4X Drive
NITD8_LP	Non-Inverting Tri-State Buffer with Enable High, 8X Drive
NITD16_LP	Non-Inverting Tri-State Buffer with Enable High, 16X Drive

AD2_LP/AD2D2_LP/AD2D4_LP/AD2D8_LP

2-Input AND with 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)								Gate Count			
AD2_LP		*AD2D2_LP*		*AD2D4_LP*		AD2D8_*LP*		*AD2_LP*	*AD2D2_LP*	*AD2D4_LP*	AD2D8_*LP*
A	B	A	B	A	B	A	B				
0.7	0.7	1.1	1.2	1.1	1.2	2.2	2.3	1.33	1.67	2.33	4.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.051 + 0.025*SL	0.046 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.073	0.040 + 0.017*SL	0.039 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.168	0.140 + 0.014*SL	0.146 + 0.013*SL	0.149 + 0.012*SL
	t_{PHL}	0.169	0.146 + 0.012*SL	0.154 + 0.010*SL	0.158 + 0.010*SL
B to Y	t_R	0.100	0.050 + 0.025*SL	0.045 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.075	0.043 + 0.016*SL	0.040 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.165	0.136 + 0.014*SL	0.143 + 0.013*SL	0.146 + 0.012*SL
	t_{PHL}	0.178	0.154 + 0.012*SL	0.163 + 0.010*SL	0.168 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AD2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.077	0.055 + 0.011*SL	0.048 + 0.013*SL	0.039 + 0.013*SL
	t_F	0.052	0.035 + 0.009*SL	0.036 + 0.008*SL	0.032 + 0.009*SL
	t_{PLH}	0.156	0.139 + 0.009*SL	0.147 + 0.007*SL	0.154 + 0.006*SL
	t_{PHL}	0.155	0.141 + 0.007*SL	0.148 + 0.005*SL	0.156 + 0.005*SL
B to Y	t_R	0.074	0.049 + 0.012*SL	0.048 + 0.013*SL	0.038 + 0.013*SL
	t_F	0.054	0.035 + 0.010*SL	0.040 + 0.008*SL	0.032 + 0.009*SL
	t_{PLH}	0.153	0.136 + 0.008*SL	0.144 + 0.007*SL	0.150 + 0.006*SL
	t_{PHL}	0.164	0.150 + 0.007*SL	0.157 + 0.005*SL	0.165 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD2D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.075	0.061 + 0.007*SL	0.064 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.057	0.047 + 0.005*SL	0.051 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.187	0.176 + 0.006*SL	0.184 + 0.004*SL	0.201 + 0.003*SL
	t_{PHL}	0.183	0.174 + 0.005*SL	0.181 + 0.003*SL	0.199 + 0.002*SL
B to Y	t_R	0.075	0.062 + 0.007*SL	0.064 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.058	0.049 + 0.004*SL	0.050 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.184	0.173 + 0.006*SL	0.180 + 0.004*SL	0.198 + 0.003*SL
	t_{PHL}	0.191	0.182 + 0.005*SL	0.189 + 0.003*SL	0.207 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

AD2D8_LP

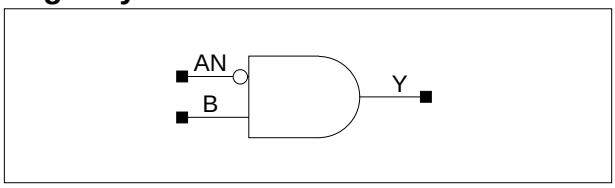
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.057 + 0.005*SL	0.063 + 0.003*SL	0.055 + 0.003*SL
	t_F	0.051	0.045 + 0.003*SL	0.049 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.180	0.174 + 0.003*SL	0.178 + 0.002*SL	0.199 + 0.002*SL
	t_{PHL}	0.177	0.172 + 0.003*SL	0.176 + 0.002*SL	0.196 + 0.001*SL
B to Y	t_R	0.067	0.061 + 0.003*SL	0.062 + 0.003*SL	0.055 + 0.003*SL
	t_F	0.053	0.049 + 0.002*SL	0.050 + 0.002*SL	0.048 + 0.002*SL
	t_{PLH}	0.177	0.170 + 0.003*SL	0.175 + 0.002*SL	0.196 + 0.002*SL
	t_{PHL}	0.185	0.180 + 0.003*SL	0.184 + 0.002*SL	0.205 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

AD2B_LP/AD2BD2_LP/AD2BD4_LP/AD2BD8_LP

2-Input AND with one Inverted Input, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

AN	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

Cell Data

Input Load (SL)								Gate Count			
AD2B_LP		*AD2BD2_LP*		*AD2BD4_LP*		*AD2BD8_LP*		*AD2B_LP*	*AD2BD2_LP*	*AD2BD4_LP*	*AD2BD8_LP*
AN	B	AN	B	AN	B	AN	B				
0.6	0.7	0.8	1.2	0.8	1.2	1.0	2.4	2.00	2.00	2.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD2B_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.101	0.052 + 0.024*SL	0.045 + 0.026*SL	0.036 + 0.027*SL
	t_F	0.072	0.038 + 0.017*SL	0.037 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.237	0.208 + 0.014*SL	0.215 + 0.013*SL	0.218 + 0.012*SL
	t_{PHL}	0.195	0.172 + 0.012*SL	0.180 + 0.010*SL	0.184 + 0.010*SL
B to Y	t_R	0.100	0.051 + 0.025*SL	0.046 + 0.026*SL	0.036 + 0.027*SL
	t_F	0.075	0.043 + 0.016*SL	0.039 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.166	0.137 + 0.014*SL	0.144 + 0.013*SL	0.146 + 0.012*SL
	t_{PHL}	0.177	0.154 + 0.012*SL	0.162 + 0.010*SL	0.166 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD2BD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.074	0.051 + 0.012*SL	0.048 + 0.013*SL	0.039 + 0.013*SL
	t_F	0.054	0.037 + 0.009*SL	0.038 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.236	0.220 + 0.008*SL	0.227 + 0.007*SL	0.234 + 0.006*SL
	t_{PHL}	0.195	0.181 + 0.007*SL	0.188 + 0.005*SL	0.196 + 0.005*SL
B to Y	t_R	0.078	0.056 + 0.011*SL	0.049 + 0.012*SL	0.039 + 0.013*SL
	t_F	0.054	0.035 + 0.010*SL	0.041 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.154	0.137 + 0.009*SL	0.144 + 0.007*SL	0.151 + 0.006*SL
	t_{PHL}	0.164	0.150 + 0.007*SL	0.157 + 0.005*SL	0.166 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AD2BD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.075	0.059 + 0.008*SL	0.066 + 0.006*SL	0.056 + 0.006*SL
	t_F	0.057	0.046 + 0.005*SL	0.051 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.267	0.256 + 0.006*SL	0.264 + 0.004*SL	0.282 + 0.003*SL
	t_{PHL}	0.222	0.213 + 0.005*SL	0.220 + 0.003*SL	0.238 + 0.002*SL
B to Y	t_R	0.075	0.060 + 0.007*SL	0.066 + 0.006*SL	0.056 + 0.006*SL
	t_F	0.058	0.050 + 0.004*SL	0.050 + 0.004*SL	0.050 + 0.004*SL
	t_{PLH}	0.187	0.175 + 0.006*SL	0.183 + 0.004*SL	0.201 + 0.003*SL
	t_{PHL}	0.192	0.182 + 0.005*SL	0.189 + 0.003*SL	0.208 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

AD2BD8_LP

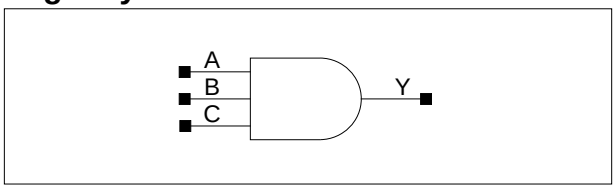
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.068	0.062 + 0.003*SL	0.061 + 0.003*SL	0.055 + 0.003*SL
	t_F	0.051	0.046 + 0.002*SL	0.047 + 0.002*SL	0.048 + 0.002*SL
	t_{PLH}	0.274	0.267 + 0.003*SL	0.272 + 0.002*SL	0.293 + 0.002*SL
	t_{PHL}	0.227	0.221 + 0.003*SL	0.226 + 0.002*SL	0.246 + 0.001*SL
B to Y	t_R	0.068	0.061 + 0.003*SL	0.063 + 0.003*SL	0.056 + 0.003*SL
	t_F	0.054	0.049 + 0.002*SL	0.050 + 0.002*SL	0.048 + 0.002*SL
	t_{PLH}	0.179	0.173 + 0.003*SL	0.178 + 0.002*SL	0.199 + 0.002*SL
	t_{PHL}	0.185	0.179 + 0.003*SL	0.184 + 0.002*SL	0.205 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

AD3_LP/AD3D2_LP/AD3D4_LP

3-Input AND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Data

Input Load (SL)									Gate Count		
AD3_LP			*AD3D2_LP*			*AD3D4_LP*			*AD3_LP*	*AD3D2_LP*	*AD3D4_LP*
A	B	C	A	B	C	A	B	C			
0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.1	1.1	1.67	2.33	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.112	0.063 + 0.025*SL	0.060 + 0.026*SL	0.045 + 0.026*SL
	t_F	0.078	0.046 + 0.016*SL	0.044 + 0.016*SL	0.032 + 0.017*SL
	t_{PLH}	0.201	0.169 + 0.016*SL	0.181 + 0.013*SL	0.188 + 0.012*SL
	t_{PHL}	0.181	0.157 + 0.012*SL	0.167 + 0.010*SL	0.173 + 0.009*SL
B to Y	t_R	0.113	0.064 + 0.025*SL	0.060 + 0.026*SL	0.045 + 0.026*SL
	t_F	0.077	0.044 + 0.017*SL	0.045 + 0.016*SL	0.033 + 0.017*SL
	t_{PLH}	0.204	0.173 + 0.016*SL	0.184 + 0.013*SL	0.191 + 0.012*SL
	t_{PHL}	0.191	0.166 + 0.012*SL	0.177 + 0.010*SL	0.183 + 0.009*SL
C to Y	t_R	0.113	0.064 + 0.025*SL	0.060 + 0.026*SL	0.045 + 0.026*SL
	t_F	0.080	0.048 + 0.016*SL	0.046 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.203	0.172 + 0.016*SL	0.184 + 0.013*SL	0.190 + 0.012*SL
	t_{PHL}	0.200	0.175 + 0.012*SL	0.185 + 0.010*SL	0.193 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AD3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.090	0.063 + 0.013*SL	0.066 + 0.012*SL	0.058 + 0.013*SL
	t_F	0.060	0.043 + 0.009*SL	0.044 + 0.008*SL	0.041 + 0.008*SL
	t_{PLH}	0.205	0.185 + 0.010*SL	0.197 + 0.007*SL	0.213 + 0.006*SL
	t_{PHL}	0.175	0.160 + 0.008*SL	0.168 + 0.006*SL	0.181 + 0.005*SL
B to Y	t_R	0.090	0.063 + 0.013*SL	0.067 + 0.012*SL	0.058 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.046 + 0.008*SL	0.041 + 0.008*SL
	t_{PLH}	0.210	0.189 + 0.010*SL	0.201 + 0.007*SL	0.218 + 0.006*SL
	t_{PHL}	0.185	0.169 + 0.008*SL	0.178 + 0.006*SL	0.191 + 0.005*SL
C to Y	t_R	0.090	0.064 + 0.013*SL	0.067 + 0.012*SL	0.058 + 0.013*SL
	t_F	0.063	0.045 + 0.009*SL	0.048 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.210	0.190 + 0.010*SL	0.201 + 0.007*SL	0.218 + 0.006*SL
	t_{PHL}	0.193	0.177 + 0.008*SL	0.186 + 0.006*SL	0.200 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD3D4_LP

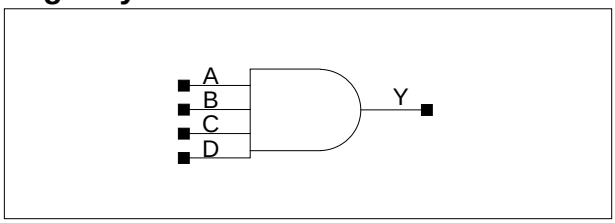
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.090	0.075 + 0.008*SL	0.081 + 0.006*SL	0.082 + 0.006*SL
	t_F	0.063	0.051 + 0.006*SL	0.058 + 0.004*SL	0.059 + 0.004*SL
	t_{PLH}	0.237	0.224 + 0.007*SL	0.233 + 0.004*SL	0.263 + 0.003*SL
	t_{PHL}	0.204	0.194 + 0.005*SL	0.202 + 0.003*SL	0.225 + 0.002*SL
B to Y	t_R	0.090	0.074 + 0.008*SL	0.081 + 0.006*SL	0.082 + 0.006*SL
	t_F	0.065	0.055 + 0.005*SL	0.058 + 0.004*SL	0.059 + 0.004*SL
	t_{PLH}	0.241	0.227 + 0.007*SL	0.237 + 0.004*SL	0.267 + 0.003*SL
	t_{PHL}	0.213	0.203 + 0.005*SL	0.211 + 0.003*SL	0.234 + 0.002*SL
C to Y	t_R	0.091	0.075 + 0.008*SL	0.081 + 0.006*SL	0.082 + 0.006*SL
	t_F	0.066	0.054 + 0.006*SL	0.061 + 0.004*SL	0.061 + 0.004*SL
	t_{PLH}	0.241	0.228 + 0.007*SL	0.238 + 0.004*SL	0.268 + 0.003*SL
	t_{PHL}	0.222	0.211 + 0.005*SL	0.220 + 0.003*SL	0.244 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

AD4_LP/AD4D2_LP/AD4D4_LP

4-Input AND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Data

Input Load (SL)											
AD4_LP				*AD4D2_LP*				*AD4D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
0.8	0.8	0.8	0.8	0.9	0.9	1.0	0.9	0.9	0.9	0.9	0.9

Gate Count		
AD4_LP	*AD4D2_LP*	*AD4D4_LP*
2.00	2.33	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.119	0.069 + 0.025*SL	0.068 + 0.025*SL	0.053 + 0.026*SL
	t_F	0.081	0.045 + 0.018*SL	0.049 + 0.017*SL	0.037 + 0.017*SL
	t_{PLH}	0.208	0.175 + 0.017*SL	0.190 + 0.013*SL	0.201 + 0.012*SL
	t_{PHL}	0.195	0.169 + 0.013*SL	0.180 + 0.010*SL	0.189 + 0.010*SL
B to Y	t_R	0.119	0.069 + 0.025*SL	0.068 + 0.025*SL	0.053 + 0.026*SL
	t_F	0.083	0.048 + 0.017*SL	0.050 + 0.017*SL	0.038 + 0.017*SL
	t_{PLH}	0.219	0.186 + 0.017*SL	0.201 + 0.013*SL	0.212 + 0.012*SL
	t_{PHL}	0.209	0.183 + 0.013*SL	0.195 + 0.010*SL	0.204 + 0.010*SL
C to Y	t_R	0.119	0.069 + 0.025*SL	0.068 + 0.025*SL	0.053 + 0.026*SL
	t_F	0.085	0.053 + 0.016*SL	0.051 + 0.017*SL	0.039 + 0.017*SL
	t_{PLH}	0.225	0.191 + 0.017*SL	0.206 + 0.013*SL	0.218 + 0.012*SL
	t_{PHL}	0.221	0.194 + 0.013*SL	0.207 + 0.010*SL	0.217 + 0.010*SL
D to Y	t_R	0.119	0.069 + 0.025*SL	0.068 + 0.025*SL	0.053 + 0.026*SL
	t_F	0.087	0.053 + 0.017*SL	0.055 + 0.017*SL	0.042 + 0.017*SL
	t_{PLH}	0.229	0.196 + 0.017*SL	0.211 + 0.013*SL	0.222 + 0.012*SL
	t_{PHL}	0.229	0.202 + 0.013*SL	0.215 + 0.010*SL	0.227 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD4D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.097	0.069 + 0.014*SL	0.075 + 0.013*SL	0.073 + 0.013*SL
	t_F	0.065	0.047 + 0.009*SL	0.049 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.221	0.198 + 0.011*SL	0.212 + 0.008*SL	0.235 + 0.006*SL
	t_{PHL}	0.191	0.174 + 0.008*SL	0.184 + 0.006*SL	0.200 + 0.005*SL
B to Y	t_R	0.097	0.067 + 0.015*SL	0.077 + 0.012*SL	0.072 + 0.013*SL
	t_F	0.066	0.046 + 0.010*SL	0.052 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.231	0.209 + 0.011*SL	0.223 + 0.008*SL	0.246 + 0.006*SL
	t_{PHL}	0.203	0.187 + 0.008*SL	0.197 + 0.006*SL	0.213 + 0.005*SL
C to Y	t_R	0.098	0.070 + 0.014*SL	0.075 + 0.013*SL	0.072 + 0.013*SL
	t_F	0.068	0.050 + 0.009*SL	0.054 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.238	0.215 + 0.011*SL	0.229 + 0.008*SL	0.252 + 0.006*SL
	t_{PHL}	0.213	0.196 + 0.008*SL	0.207 + 0.006*SL	0.223 + 0.005*SL
D to Y	t_R	0.097	0.067 + 0.015*SL	0.077 + 0.013*SL	0.072 + 0.013*SL
	t_F	0.070	0.051 + 0.010*SL	0.057 + 0.008*SL	0.052 + 0.008*SL
	t_{PLH}	0.241	0.219 + 0.011*SL	0.233 + 0.008*SL	0.255 + 0.006*SL
	t_{PHL}	0.222	0.205 + 0.009*SL	0.216 + 0.006*SL	0.233 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AD4D4_LP

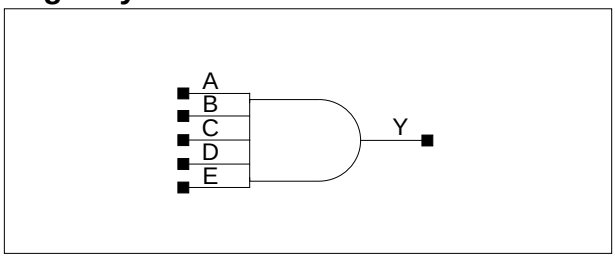
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.086 + 0.008*SL	0.093 + 0.007*SL	0.103 + 0.006*SL
	t_F	0.073	0.062 + 0.006*SL	0.067 + 0.004*SL	0.073 + 0.004*SL
	t_{PLH}	0.269	0.254 + 0.007*SL	0.264 + 0.005*SL	0.303 + 0.003*SL
	t_{PHL}	0.235	0.223 + 0.006*SL	0.233 + 0.004*SL	0.261 + 0.003*SL
B to Y	t_R	0.103	0.085 + 0.009*SL	0.094 + 0.007*SL	0.103 + 0.006*SL
	t_F	0.075	0.062 + 0.006*SL	0.071 + 0.004*SL	0.075 + 0.004*SL
	t_{PLH}	0.279	0.265 + 0.007*SL	0.275 + 0.005*SL	0.314 + 0.003*SL
	t_{PHL}	0.248	0.236 + 0.006*SL	0.245 + 0.004*SL	0.275 + 0.003*SL
C to Y	t_R	0.101	0.084 + 0.008*SL	0.091 + 0.007*SL	0.104 + 0.006*SL
	t_F	0.078	0.066 + 0.006*SL	0.073 + 0.004*SL	0.076 + 0.004*SL
	t_{PLH}	0.286	0.271 + 0.007*SL	0.282 + 0.005*SL	0.320 + 0.003*SL
	t_{PHL}	0.258	0.246 + 0.006*SL	0.256 + 0.004*SL	0.286 + 0.003*SL
D to Y	t_R	0.103	0.086 + 0.009*SL	0.094 + 0.007*SL	0.103 + 0.006*SL
	t_F	0.079	0.066 + 0.006*SL	0.074 + 0.004*SL	0.080 + 0.004*SL
	t_{PLH}	0.289	0.275 + 0.007*SL	0.285 + 0.005*SL	0.323 + 0.003*SL
	t_{PHL}	0.269	0.257 + 0.006*SL	0.266 + 0.004*SL	0.297 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

AD5_LP/AD5D2_LP/AD5D4_LP

5-Input AND with 1X/2X/4XDrive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	1

Cell Data

Input Load (SL)														
AD5_LP					*AD5D2_LP*					*AD5D4_LP*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	0.8	0.9	0.9	1.0	0.9	1.0	1.0	0.8	0.8	0.9	0.8	0.8

Gate Count		
AD5_LP	*AD5D2_LP*	*AD5D4_LP*
3.00	3.33	5.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD5_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.203	0.100 + 0.051*SL	0.094 + 0.053*SL	0.088 + 0.053*SL
	t_F	0.077	0.047 + 0.015*SL	0.046 + 0.015*SL	0.036 + 0.016*SL
	t_{PLH}	0.221	0.167 + 0.027*SL	0.171 + 0.026*SL	0.173 + 0.026*SL
	t_{PHL}	0.184	0.161 + 0.011*SL	0.171 + 0.009*SL	0.178 + 0.009*SL
B to Y	t_R	0.203	0.101 + 0.051*SL	0.095 + 0.053*SL	0.088 + 0.053*SL
	t_F	0.078	0.048 + 0.015*SL	0.047 + 0.015*SL	0.037 + 0.016*SL
	t_{PLH}	0.225	0.171 + 0.027*SL	0.175 + 0.026*SL	0.178 + 0.026*SL
	t_{PHL}	0.198	0.175 + 0.011*SL	0.184 + 0.009*SL	0.192 + 0.009*SL
C to Y	t_R	0.203	0.100 + 0.051*SL	0.095 + 0.053*SL	0.088 + 0.053*SL
	t_F	0.078	0.047 + 0.016*SL	0.050 + 0.015*SL	0.039 + 0.016*SL
	t_{PLH}	0.224	0.170 + 0.027*SL	0.174 + 0.026*SL	0.177 + 0.026*SL
	t_{PHL}	0.209	0.186 + 0.012*SL	0.196 + 0.009*SL	0.205 + 0.009*SL
D to Y	t_R	0.197	0.092 + 0.052*SL	0.090 + 0.053*SL	0.088 + 0.053*SL
	t_F	0.086	0.056 + 0.015*SL	0.055 + 0.015*SL	0.045 + 0.016*SL
	t_{PLH}	0.215	0.162 + 0.026*SL	0.164 + 0.026*SL	0.166 + 0.026*SL
	t_{PHL}	0.182	0.161 + 0.011*SL	0.168 + 0.009*SL	0.173 + 0.009*SL
E to Y	t_R	0.197	0.092 + 0.052*SL	0.090 + 0.053*SL	0.088 + 0.053*SL
	t_F	0.087	0.055 + 0.016*SL	0.057 + 0.015*SL	0.046 + 0.016*SL
	t_{PLH}	0.213	0.161 + 0.026*SL	0.163 + 0.026*SL	0.165 + 0.026*SL
	t_{PHL}	0.196	0.174 + 0.011*SL	0.181 + 0.009*SL	0.186 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD5D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.151	0.100 + 0.025*SL	0.097 + 0.026*SL	0.088 + 0.027*SL
	t_F	0.065	0.048 + 0.009*SL	0.052 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.220	0.191 + 0.015*SL	0.197 + 0.013*SL	0.201 + 0.013*SL
	t_{PHL}	0.189	0.174 + 0.007*SL	0.182 + 0.005*SL	0.196 + 0.004*SL
B to Y	t_R	0.151	0.100 + 0.025*SL	0.098 + 0.026*SL	0.087 + 0.027*SL
	t_F	0.066	0.048 + 0.009*SL	0.054 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.224	0.194 + 0.015*SL	0.201 + 0.013*SL	0.205 + 0.013*SL
	t_{PHL}	0.200	0.186 + 0.007*SL	0.194 + 0.005*SL	0.208 + 0.004*SL
C to Y	t_R	0.151	0.101 + 0.025*SL	0.098 + 0.026*SL	0.087 + 0.027*SL
	t_F	0.068	0.052 + 0.008*SL	0.053 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.223	0.194 + 0.015*SL	0.200 + 0.013*SL	0.204 + 0.013*SL
	t_{PHL}	0.211	0.196 + 0.007*SL	0.204 + 0.005*SL	0.219 + 0.005*SL
D to Y	t_R	0.141	0.088 + 0.026*SL	0.087 + 0.027*SL	0.084 + 0.027*SL
	t_F	0.074	0.058 + 0.008*SL	0.061 + 0.007*SL	0.056 + 0.008*SL
	t_{PLH}	0.218	0.190 + 0.014*SL	0.194 + 0.013*SL	0.197 + 0.013*SL
	t_{PHL}	0.187	0.175 + 0.006*SL	0.180 + 0.005*SL	0.189 + 0.004*SL
E to Y	t_R	0.140	0.088 + 0.026*SL	0.087 + 0.027*SL	0.084 + 0.027*SL
	t_F	0.076	0.060 + 0.008*SL	0.062 + 0.007*SL	0.056 + 0.008*SL
	t_{PLH}	0.216	0.188 + 0.014*SL	0.192 + 0.013*SL	0.195 + 0.013*SL
	t_{PHL}	0.199	0.186 + 0.006*SL	0.192 + 0.005*SL	0.201 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

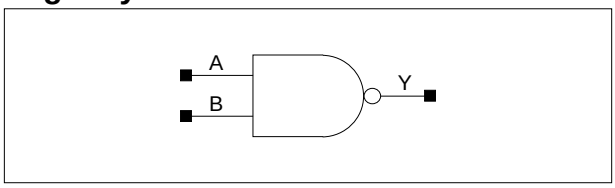
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AD5D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.065	0.053 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.055	0.044 + 0.006*SL	0.050 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.345	0.335 + 0.005*SL	0.341 + 0.003*SL	0.349 + 0.003*SL
	t_{PHL}	0.317	0.308 + 0.005*SL	0.315 + 0.003*SL	0.332 + 0.002*SL
B to Y	t_R	0.065	0.053 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.055	0.045 + 0.005*SL	0.048 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.348	0.339 + 0.005*SL	0.345 + 0.003*SL	0.353 + 0.003*SL
	t_{PHL}	0.333	0.323 + 0.005*SL	0.330 + 0.003*SL	0.347 + 0.002*SL
C to Y	t_R	0.065	0.053 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.056	0.047 + 0.004*SL	0.047 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.349	0.339 + 0.005*SL	0.345 + 0.003*SL	0.353 + 0.003*SL
	t_{PHL}	0.346	0.337 + 0.005*SL	0.343 + 0.003*SL	0.361 + 0.002*SL
D to Y	t_R	0.065	0.054 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.055	0.046 + 0.005*SL	0.048 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.344	0.334 + 0.005*SL	0.340 + 0.003*SL	0.348 + 0.003*SL
	t_{PHL}	0.318	0.309 + 0.005*SL	0.316 + 0.003*SL	0.333 + 0.002*SL
E to Y	t_R	0.063	0.049 + 0.007*SL	0.053 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.056	0.047 + 0.004*SL	0.048 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.342	0.332 + 0.005*SL	0.338 + 0.003*SL	0.347 + 0.003*SL
	t_{PHL}	0.335	0.326 + 0.005*SL	0.333 + 0.003*SL	0.350 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)								Gate Count			
ND2_LP		*ND2D2_LP*		*ND2D4_LP*		*ND2D8_LP*		*ND2_LP*	*ND2D2_LP*	*ND2D4_LP*	*ND2D8_LP*
A	B	A	B	A	B	A	B				
1.1	1.1	2.3	2.2	4.6	4.6	1.1	1.2	1.00	1.67	3.00	4.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.124	0.082 + 0.021*SL	0.065 + 0.025*SL	0.042 + 0.027*SL
	t_F	0.120	0.075 + 0.023*SL	0.065 + 0.025*SL	0.043 + 0.026*SL
	t_{PLH}	0.104	0.076 + 0.014*SL	0.083 + 0.012*SL	0.084 + 0.012*SL
	t_{PHL}	0.095	0.063 + 0.016*SL	0.072 + 0.014*SL	0.073 + 0.014*SL
B to Y	t_R	0.129	0.083 + 0.023*SL	0.073 + 0.025*SL	0.050 + 0.027*SL
	t_F	0.111	0.064 + 0.023*SL	0.056 + 0.025*SL	0.042 + 0.026*SL
	t_{PLH}	0.113	0.086 + 0.013*SL	0.091 + 0.012*SL	0.091 + 0.012*SL
	t_{PHL}	0.092	0.060 + 0.016*SL	0.068 + 0.014*SL	0.070 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

ND2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.080 + 0.010*SL	0.075 + 0.012*SL	0.056 + 0.013*SL
	t_F	0.099	0.076 + 0.011*SL	0.074 + 0.012*SL	0.056 + 0.013*SL
	t_{PLH}	0.090	0.072 + 0.009*SL	0.081 + 0.006*SL	0.084 + 0.006*SL
	t_{PHL}	0.079	0.060 + 0.009*SL	0.069 + 0.007*SL	0.073 + 0.007*SL
B to Y	t_R	0.107	0.086 + 0.010*SL	0.079 + 0.012*SL	0.064 + 0.013*SL
	t_F	0.090	0.067 + 0.011*SL	0.063 + 0.012*SL	0.052 + 0.013*SL
	t_{PLH}	0.100	0.084 + 0.008*SL	0.090 + 0.006*SL	0.091 + 0.006*SL
	t_{PHL}	0.077	0.059 + 0.009*SL	0.066 + 0.007*SL	0.070 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND2D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.090	0.078 + 0.006*SL	0.080 + 0.006*SL	0.057 + 0.006*SL
	t_F	0.087	0.076 + 0.005*SL	0.074 + 0.006*SL	0.057 + 0.006*SL
	t_{PLH}	0.080	0.070 + 0.005*SL	0.077 + 0.003*SL	0.083 + 0.003*SL
	t_{PHL}	0.068	0.058 + 0.005*SL	0.064 + 0.004*SL	0.072 + 0.003*SL
B to Y	t_R	0.095	0.085 + 0.005*SL	0.083 + 0.006*SL	0.065 + 0.006*SL
	t_F	0.077	0.066 + 0.005*SL	0.064 + 0.006*SL	0.052 + 0.007*SL
	t_{PLH}	0.091	0.083 + 0.004*SL	0.087 + 0.003*SL	0.091 + 0.003*SL
	t_{PHL}	0.067	0.058 + 0.005*SL	0.062 + 0.004*SL	0.069 + 0.003*SL

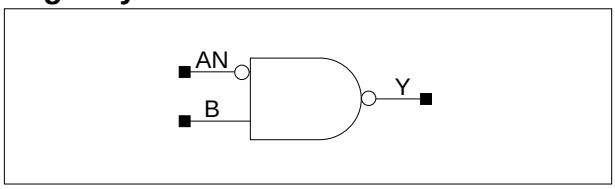
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

ND2D8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.055	0.049 + 0.003*SL	0.050 + 0.003*SL	0.037 + 0.003*SL
	t_F	0.051	0.047 + 0.002*SL	0.047 + 0.002*SL	0.044 + 0.002*SL
	t_{PLH}	0.237	0.232 + 0.003*SL	0.235 + 0.002*SL	0.245 + 0.002*SL
	t_{PHL}	0.246	0.241 + 0.003*SL	0.245 + 0.002*SL	0.263 + 0.001*SL
B to Y	t_R	0.055	0.049 + 0.003*SL	0.050 + 0.003*SL	0.037 + 0.003*SL
	t_F	0.050	0.044 + 0.003*SL	0.048 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.245	0.240 + 0.003*SL	0.244 + 0.002*SL	0.253 + 0.002*SL
	t_{PHL}	0.242	0.237 + 0.003*SL	0.241 + 0.002*SL	0.260 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

Logic Symbol



Truth Table

AN	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

Cell Data

Input Load (SL)								Gate Count			
ND2B_LP		*ND2BD2_LP*		*ND2BD4_LP*		*ND2BD8_LP*		*ND2B_LP*	*ND2BD2_LP*	*ND2BD4_LP*	*ND2BD8_LP*
AN	B	AN	B	AN	B	AN	B				
0.7	1.2	0.9	2.4	1.0	4.7	0.9	1.2	1.33	2.00	3.33	5.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND2B_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.106	0.056 + 0.025*SL	0.051 + 0.026*SL	0.043 + 0.027*SL
	t_F	0.106	0.055 + 0.026*SL	0.052 + 0.026*SL	0.045 + 0.027*SL
	t_{PLH}	0.168	0.141 + 0.013*SL	0.145 + 0.012*SL	0.146 + 0.012*SL
	t_{PHL}	0.174	0.144 + 0.015*SL	0.147 + 0.014*SL	0.149 + 0.014*SL
B to Y	t_R	0.129	0.084 + 0.022*SL	0.073 + 0.025*SL	0.050 + 0.027*SL
	t_F	0.115	0.066 + 0.024*SL	0.060 + 0.026*SL	0.046 + 0.027*SL
	t_{PLH}	0.113	0.086 + 0.014*SL	0.090 + 0.012*SL	0.091 + 0.012*SL
	t_{PHL}	0.094	0.062 + 0.016*SL	0.070 + 0.014*SL	0.072 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND2BD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.085	0.060 + 0.012*SL	0.059 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.082	0.055 + 0.013*SL	0.056 + 0.013*SL	0.050 + 0.013*SL
	t_{PLH}	0.169	0.154 + 0.007*SL	0.158 + 0.006*SL	0.162 + 0.006*SL
	t_{PHL}	0.177	0.160 + 0.008*SL	0.165 + 0.007*SL	0.169 + 0.007*SL
B to Y	t_R	0.105	0.084 + 0.010*SL	0.078 + 0.012*SL	0.061 + 0.013*SL
	t_F	0.089	0.064 + 0.012*SL	0.063 + 0.013*SL	0.053 + 0.013*SL
	t_{PLH}	0.097	0.081 + 0.008*SL	0.087 + 0.006*SL	0.089 + 0.006*SL
	t_{PHL}	0.076	0.058 + 0.009*SL	0.065 + 0.007*SL	0.071 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

ND2BD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.083	0.072 + 0.006*SL	0.071 + 0.006*SL	0.058 + 0.007*SL
	t_F	0.081	0.068 + 0.006*SL	0.068 + 0.006*SL	0.061 + 0.007*SL
	t_{PLH}	0.189	0.180 + 0.005*SL	0.185 + 0.003*SL	0.194 + 0.003*SL
	t_{PHL}	0.201	0.191 + 0.005*SL	0.195 + 0.004*SL	0.206 + 0.003*SL
B to Y	t_R	0.096	0.085 + 0.005*SL	0.083 + 0.006*SL	0.064 + 0.006*SL
	t_F	0.076	0.064 + 0.006*SL	0.063 + 0.006*SL	0.057 + 0.007*SL
	t_{PLH}	0.089	0.080 + 0.004*SL	0.085 + 0.003*SL	0.089 + 0.003*SL
	t_{PHL}	0.067	0.057 + 0.005*SL	0.062 + 0.004*SL	0.072 + 0.004*SL

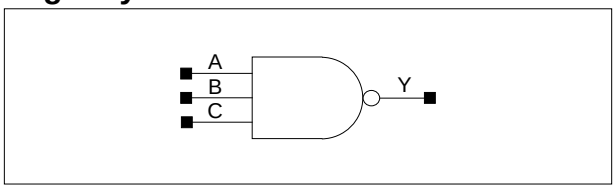
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

ND2BD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.055	0.049 + 0.003*SL	0.049 + 0.003*SL	0.037 + 0.003*SL
	t_F	0.051	0.046 + 0.002*SL	0.047 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.287	0.282 + 0.003*SL	0.285 + 0.002*SL	0.295 + 0.002*SL
	t_{PHL}	0.317	0.311 + 0.003*SL	0.316 + 0.002*SL	0.334 + 0.001*SL
B to Y	t_R	0.055	0.049 + 0.003*SL	0.050 + 0.003*SL	0.037 + 0.003*SL
	t_F	0.051	0.047 + 0.002*SL	0.047 + 0.002*SL	0.045 + 0.002*SL
	t_{PLH}	0.246	0.241 + 0.003*SL	0.244 + 0.002*SL	0.254 + 0.002*SL
	t_{PHL}	0.246	0.240 + 0.003*SL	0.245 + 0.002*SL	0.263 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Data

Input Load (SL)											
ND3_LP			*ND3D2_LP*			*ND3D4_LP*			*ND3D8_LP*		
A	B	C	A	B	C	A	B	C	A	B	C
0.9	1.0	0.9	2.0	2.0	1.9	0.5	0.5	0.5	0.9	1.0	1.0

Gate Count			
ND3_LP	*ND3D2_LP*	*ND3D4_LP*	*ND3D8_LP*
1.33	2.33	3.33	5.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.156	0.091 + 0.032*SL	0.080 + 0.035*SL	0.063 + 0.036*SL
	t_F	0.165	0.098 + 0.034*SL	0.087 + 0.037*SL	0.070 + 0.037*SL
	t_{PLH}	0.127	0.092 + 0.017*SL	0.094 + 0.017*SL	0.095 + 0.017*SL
	t_{PHL}	0.119	0.079 + 0.020*SL	0.081 + 0.019*SL	0.082 + 0.019*SL
B to Y	t_R	0.166	0.101 + 0.032*SL	0.089 + 0.035*SL	0.075 + 0.036*SL
	t_F	0.159	0.090 + 0.035*SL	0.082 + 0.037*SL	0.071 + 0.037*SL
	t_{PLH}	0.138	0.104 + 0.017*SL	0.105 + 0.017*SL	0.106 + 0.017*SL
	t_{PHL}	0.122	0.082 + 0.020*SL	0.085 + 0.019*SL	0.086 + 0.019*SL
C to Y	t_R	0.177	0.112 + 0.033*SL	0.101 + 0.035*SL	0.087 + 0.036*SL
	t_F	0.154	0.083 + 0.036*SL	0.078 + 0.037*SL	0.071 + 0.037*SL
	t_{PLH}	0.147	0.112 + 0.017*SL	0.113 + 0.017*SL	0.115 + 0.017*SL
	t_{PHL}	0.122	0.082 + 0.020*SL	0.085 + 0.019*SL	0.087 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

ND3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.123	0.094 + 0.015*SL	0.085 + 0.017*SL	0.067 + 0.018*SL
	t_F	0.130	0.098 + 0.016*SL	0.091 + 0.017*SL	0.074 + 0.018*SL
	t_{PLH}	0.107	0.088 + 0.010*SL	0.093 + 0.008*SL	0.093 + 0.008*SL
	t_{PHL}	0.095	0.073 + 0.011*SL	0.079 + 0.010*SL	0.079 + 0.009*SL
B to Y	t_R	0.131	0.100 + 0.016*SL	0.094 + 0.017*SL	0.078 + 0.018*SL
	t_F	0.122	0.090 + 0.016*SL	0.084 + 0.018*SL	0.073 + 0.018*SL
	t_{PLH}	0.119	0.101 + 0.009*SL	0.103 + 0.008*SL	0.104 + 0.008*SL
	t_{PHL}	0.098	0.077 + 0.011*SL	0.082 + 0.010*SL	0.083 + 0.010*SL
C to Y	t_R	0.142	0.111 + 0.016*SL	0.105 + 0.017*SL	0.090 + 0.018*SL
	t_F	0.114	0.079 + 0.018*SL	0.078 + 0.018*SL	0.071 + 0.018*SL
	t_{PLH}	0.128	0.111 + 0.009*SL	0.111 + 0.009*SL	0.113 + 0.008*SL
	t_{PHL}	0.099	0.078 + 0.010*SL	0.081 + 0.010*SL	0.083 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND3D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.063	0.050 + 0.006*SL	0.052 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.058	0.048 + 0.005*SL	0.052 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.287	0.277 + 0.005*SL	0.283 + 0.003*SL	0.291 + 0.003*SL
	t_{PHL}	0.283	0.273 + 0.005*SL	0.280 + 0.003*SL	0.298 + 0.002*SL
B to Y	t_R	0.064	0.053 + 0.005*SL	0.050 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.058	0.048 + 0.005*SL	0.052 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.302	0.293 + 0.005*SL	0.298 + 0.003*SL	0.307 + 0.003*SL
	t_{PHL}	0.287	0.277 + 0.005*SL	0.284 + 0.003*SL	0.302 + 0.002*SL
C to Y	t_R	0.065	0.052 + 0.006*SL	0.053 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.058	0.047 + 0.005*SL	0.052 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.316	0.307 + 0.005*SL	0.312 + 0.003*SL	0.321 + 0.003*SL
	t_{PHL}	0.287	0.278 + 0.005*SL	0.285 + 0.003*SL	0.302 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

ND3D8_LP

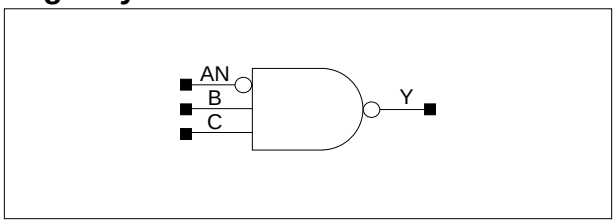
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.056	0.048 + 0.004*SL	0.051 + 0.003*SL	0.038 + 0.003*SL
	t_F	0.052	0.046 + 0.003*SL	0.050 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.269	0.264 + 0.003*SL	0.267 + 0.002*SL	0.277 + 0.002*SL
	t_{PHL}	0.284	0.279 + 0.003*SL	0.283 + 0.002*SL	0.302 + 0.001*SL
B to Y	t_R	0.054	0.048 + 0.003*SL	0.049 + 0.003*SL	0.037 + 0.003*SL
	t_F	0.052	0.046 + 0.003*SL	0.050 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.282	0.276 + 0.003*SL	0.280 + 0.002*SL	0.290 + 0.002*SL
	t_{PHL}	0.288	0.283 + 0.003*SL	0.287 + 0.002*SL	0.306 + 0.001*SL
C to Y	t_R	0.058	0.052 + 0.003*SL	0.051 + 0.003*SL	0.038 + 0.003*SL
	t_F	0.052	0.046 + 0.003*SL	0.050 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.292	0.287 + 0.003*SL	0.291 + 0.002*SL	0.301 + 0.002*SL
	t_{PHL}	0.288	0.283 + 0.003*SL	0.287 + 0.002*SL	0.307 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

ND3B_LP/ND3BD2_LP/ND3BD4_LP/ND3BD8_LP

3-Input NAND with one Inverted Input, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

AN	B	C	Y
0	1	1	0
Other Stares			1

Cell Data

Input Load (SL)											
ND3B_LP			*ND3BD2_LP*			*ND3BD4_LP*			*ND3BD8_LP*		
AN	B	C	AN	B	C	AN	B	C	AN	B	C
0.7	1.0	1.0	1.0	2.0	1.9	0.7	1.0	1.0	0.7	1.0	1.0

Gate Count			
ND3B_LP	*ND3BD2_LP*	*ND3BD4_LP*	*ND3BD8_LP*
2.00	3.00	4.00	5.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND3B_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.146	0.078 + 0.034*SL	0.072 + 0.035*SL	0.069 + 0.036*SL
	t_F	0.156	0.083 + 0.036*SL	0.081 + 0.037*SL	0.077 + 0.037*SL
	t_{PLH}	0.183	0.149 + 0.017*SL	0.151 + 0.017*SL	0.153 + 0.017*SL
	t_{PHL}	0.190	0.151 + 0.020*SL	0.152 + 0.019*SL	0.153 + 0.019*SL
B to Y	t_R	0.169	0.105 + 0.032*SL	0.094 + 0.035*SL	0.079 + 0.036*SL
	t_F	0.164	0.095 + 0.035*SL	0.088 + 0.037*SL	0.077 + 0.037*SL
	t_{PLH}	0.139	0.105 + 0.017*SL	0.106 + 0.017*SL	0.107 + 0.017*SL
	t_{PHL}	0.125	0.085 + 0.020*SL	0.088 + 0.019*SL	0.090 + 0.019*SL
C to Y	t_R	0.180	0.115 + 0.032*SL	0.105 + 0.035*SL	0.091 + 0.036*SL
	t_F	0.160	0.088 + 0.036*SL	0.084 + 0.037*SL	0.077 + 0.037*SL
	t_{PLH}	0.147	0.113 + 0.017*SL	0.114 + 0.017*SL	0.116 + 0.017*SL
	t_{PHL}	0.126	0.086 + 0.020*SL	0.089 + 0.019*SL	0.091 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

ND3BD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.110	0.077 + 0.017*SL	0.074 + 0.018*SL	0.067 + 0.018*SL
	t_F	0.117	0.081 + 0.018*SL	0.080 + 0.018*SL	0.074 + 0.018*SL
	t_{PLH}	0.174	0.156 + 0.009*SL	0.158 + 0.008*SL	0.159 + 0.008*SL
	t_{PHL}	0.179	0.158 + 0.010*SL	0.160 + 0.010*SL	0.162 + 0.009*SL
B to Y	t_R	0.133	0.103 + 0.015*SL	0.096 + 0.017*SL	0.080 + 0.018*SL
	t_F	0.125	0.091 + 0.017*SL	0.088 + 0.018*SL	0.078 + 0.018*SL
	t_{PLH}	0.119	0.102 + 0.009*SL	0.103 + 0.008*SL	0.104 + 0.008*SL
	t_{PHL}	0.101	0.079 + 0.011*SL	0.084 + 0.010*SL	0.086 + 0.010*SL
C to Y	t_R	0.144	0.113 + 0.016*SL	0.107 + 0.017*SL	0.092 + 0.018*SL
	t_F	0.119	0.083 + 0.018*SL	0.082 + 0.018*SL	0.076 + 0.018*SL
	t_{PLH}	0.129	0.112 + 0.009*SL	0.112 + 0.009*SL	0.114 + 0.008*SL
	t_{PHL}	0.102	0.081 + 0.011*SL	0.084 + 0.010*SL	0.086 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND3BD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.061	0.048 + 0.006*SL	0.050 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.056	0.045 + 0.005*SL	0.050 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.307	0.298 + 0.005*SL	0.303 + 0.003*SL	0.311 + 0.003*SL
	t_{PHL}	0.335	0.326 + 0.005*SL	0.332 + 0.003*SL	0.349 + 0.002*SL
B to Y	t_R	0.061	0.048 + 0.006*SL	0.049 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.057	0.049 + 0.004*SL	0.048 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.263	0.254 + 0.005*SL	0.259 + 0.003*SL	0.267 + 0.003*SL
	t_{PHL}	0.270	0.261 + 0.005*SL	0.268 + 0.003*SL	0.285 + 0.002*SL
C to Y	t_R	0.063	0.052 + 0.006*SL	0.049 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.057	0.049 + 0.004*SL	0.049 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.274	0.265 + 0.005*SL	0.270 + 0.003*SL	0.278 + 0.003*SL
	t_{PHL}	0.271	0.262 + 0.005*SL	0.268 + 0.003*SL	0.286 + 0.002*SL

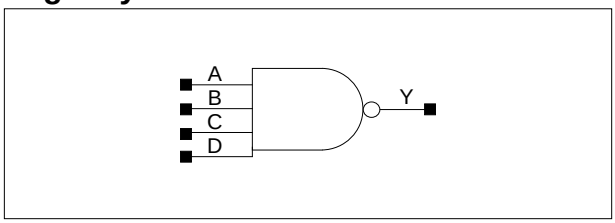
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

ND3BD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.055	0.049 + 0.003*SL	0.050 + 0.003*SL	0.037 + 0.003*SL
	t_F	0.053	0.048 + 0.002*SL	0.049 + 0.002*SL	0.046 + 0.002*SL
	t_{PLH}	0.323	0.318 + 0.003*SL	0.321 + 0.002*SL	0.331 + 0.002*SL
	t_{PHL}	0.352	0.346 + 0.003*SL	0.351 + 0.002*SL	0.370 + 0.001*SL
B to Y	t_R	0.055	0.048 + 0.003*SL	0.049 + 0.003*SL	0.037 + 0.003*SL
	t_F	0.052	0.046 + 0.003*SL	0.050 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.281	0.276 + 0.003*SL	0.279 + 0.002*SL	0.290 + 0.002*SL
	t_{PHL}	0.289	0.284 + 0.003*SL	0.288 + 0.002*SL	0.307 + 0.001*SL
C to Y	t_R	0.058	0.052 + 0.003*SL	0.051 + 0.003*SL	0.038 + 0.003*SL
	t_F	0.052	0.046 + 0.003*SL	0.050 + 0.002*SL	0.047 + 0.002*SL
	t_{PLH}	0.292	0.287 + 0.003*SL	0.290 + 0.002*SL	0.300 + 0.002*SL
	t_{PHL}	0.289	0.283 + 0.003*SL	0.287 + 0.002*SL	0.307 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Data

Input Load (SL)											
ND4_LP				*ND4D2_LP*				*ND4D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
0.8	0.8	0.9	0.8	1.7	1.7	1.7	1.6	0.8	0.8	0.8	0.8
Gate Count											
ND4_LP				*ND4D2_LP*				*ND4D4_LP*			
1.67				3.00				3.33			

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.184	0.102 + 0.041*SL	0.087 + 0.045*SL	0.075 + 0.046*SL
	t_F	0.203	0.115 + 0.044*SL	0.103 + 0.047*SL	0.092 + 0.048*SL
	t_{PLH}	0.143	0.100 + 0.021*SL	0.101 + 0.021*SL	0.102 + 0.021*SL
	t_{PHL}	0.132	0.083 + 0.025*SL	0.083 + 0.024*SL	0.084 + 0.024*SL
B to Y	t_R	0.196	0.113 + 0.042*SL	0.100 + 0.045*SL	0.091 + 0.046*SL
	t_F	0.199	0.108 + 0.046*SL	0.100 + 0.047*SL	0.092 + 0.048*SL
	t_{PLH}	0.156	0.113 + 0.022*SL	0.114 + 0.021*SL	0.116 + 0.021*SL
	t_{PHL}	0.141	0.091 + 0.025*SL	0.093 + 0.024*SL	0.094 + 0.024*SL
C to Y	t_R	0.210	0.126 + 0.042*SL	0.114 + 0.045*SL	0.106 + 0.046*SL
	t_F	0.196	0.103 + 0.046*SL	0.098 + 0.048*SL	0.092 + 0.048*SL
	t_{PLH}	0.168	0.124 + 0.022*SL	0.127 + 0.021*SL	0.129 + 0.021*SL
	t_{PHL}	0.148	0.098 + 0.025*SL	0.100 + 0.024*SL	0.102 + 0.024*SL
D to Y	t_R	0.224	0.138 + 0.043*SL	0.129 + 0.045*SL	0.122 + 0.046*SL
	t_F	0.193	0.100 + 0.047*SL	0.096 + 0.048*SL	0.092 + 0.048*SL
	t_{PLH}	0.177	0.132 + 0.022*SL	0.136 + 0.022*SL	0.140 + 0.021*SL
	t_{PHL}	0.150	0.101 + 0.025*SL	0.102 + 0.024*SL	0.103 + 0.024*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND4D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.144	0.103 + 0.020*SL	0.098 + 0.022*SL	0.080 + 0.023*SL
	t_F	0.161	0.118 + 0.022*SL	0.113 + 0.023*SL	0.096 + 0.024*SL
	t_{PLH}	0.122	0.100 + 0.011*SL	0.101 + 0.011*SL	0.102 + 0.011*SL
	t_{PHL}	0.108	0.082 + 0.013*SL	0.084 + 0.012*SL	0.085 + 0.012*SL
B to Y	t_R	0.157	0.117 + 0.020*SL	0.109 + 0.022*SL	0.095 + 0.023*SL
	t_F	0.157	0.113 + 0.022*SL	0.108 + 0.023*SL	0.098 + 0.024*SL
	t_{PLH}	0.136	0.115 + 0.011*SL	0.115 + 0.011*SL	0.116 + 0.011*SL
	t_{PHL}	0.117	0.091 + 0.013*SL	0.093 + 0.012*SL	0.095 + 0.012*SL
C to Y	t_R	0.171	0.130 + 0.020*SL	0.123 + 0.022*SL	0.110 + 0.023*SL
	t_F	0.152	0.106 + 0.023*SL	0.103 + 0.023*SL	0.097 + 0.024*SL
	t_{PLH}	0.148	0.126 + 0.011*SL	0.127 + 0.011*SL	0.129 + 0.011*SL
	t_{PHL}	0.124	0.099 + 0.013*SL	0.101 + 0.012*SL	0.102 + 0.012*SL
D to Y	t_R	0.184	0.142 + 0.021*SL	0.138 + 0.022*SL	0.125 + 0.023*SL
	t_F	0.149	0.103 + 0.023*SL	0.100 + 0.024*SL	0.096 + 0.024*SL
	t_{PLH}	0.156	0.133 + 0.011*SL	0.135 + 0.011*SL	0.139 + 0.011*SL
	t_{PHL}	0.127	0.101 + 0.013*SL	0.103 + 0.012*SL	0.104 + 0.012*SL

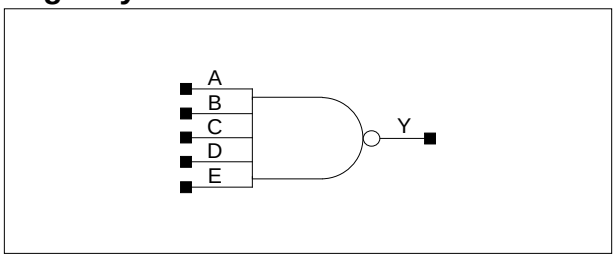
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

ND4D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.060	0.046 + 0.007*SL	0.049 + 0.006*SL	0.035 + 0.007*SL
	t_F	0.058	0.047 + 0.005*SL	0.053 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.270	0.261 + 0.005*SL	0.266 + 0.003*SL	0.273 + 0.003*SL
	t_{PHL}	0.283	0.273 + 0.005*SL	0.280 + 0.003*SL	0.298 + 0.002*SL
B to Y	t_R	0.060	0.046 + 0.007*SL	0.049 + 0.006*SL	0.035 + 0.007*SL
	t_F	0.058	0.049 + 0.005*SL	0.051 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.287	0.278 + 0.005*SL	0.283 + 0.003*SL	0.290 + 0.003*SL
	t_{PHL}	0.291	0.282 + 0.005*SL	0.289 + 0.003*SL	0.307 + 0.002*SL
C to Y	t_R	0.061	0.048 + 0.006*SL	0.048 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.058	0.048 + 0.005*SL	0.053 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.302	0.293 + 0.005*SL	0.298 + 0.003*SL	0.306 + 0.003*SL
	t_{PHL}	0.299	0.289 + 0.005*SL	0.296 + 0.003*SL	0.314 + 0.002*SL
D to Y	t_R	0.063	0.052 + 0.006*SL	0.049 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.058	0.047 + 0.006*SL	0.053 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.315	0.306 + 0.005*SL	0.311 + 0.003*SL	0.318 + 0.003*SL
	t_{PHL}	0.301	0.292 + 0.005*SL	0.299 + 0.003*SL	0.317 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)														
ND5_LP					*ND5D2_LP*					*ND5D4_LP*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.9	0.8	0.8	0.8	0.9	0.8

Gate Count		
ND5_LP	*ND5D2_LP*	*ND5D4_LP*
3.33	3.67	4.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND5_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.089	0.038 + 0.025*SL	0.034 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.085	0.049 + 0.018*SL	0.054 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.248	0.222 + 0.013*SL	0.225 + 0.012*SL	0.226 + 0.012*SL
	t_{PHL}	0.262	0.235 + 0.014*SL	0.248 + 0.010*SL	0.261 + 0.010*SL
B to Y	t_R	0.089	0.038 + 0.025*SL	0.034 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.085	0.049 + 0.018*SL	0.054 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.265	0.239 + 0.013*SL	0.242 + 0.012*SL	0.243 + 0.012*SL
	t_{PHL}	0.266	0.238 + 0.014*SL	0.252 + 0.010*SL	0.265 + 0.010*SL
C to Y	t_R	0.089	0.038 + 0.025*SL	0.035 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.085	0.049 + 0.018*SL	0.054 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.281	0.255 + 0.013*SL	0.258 + 0.012*SL	0.259 + 0.012*SL
	t_{PHL}	0.266	0.239 + 0.014*SL	0.252 + 0.010*SL	0.265 + 0.010*SL
D to Y	t_R	0.091	0.041 + 0.025*SL	0.036 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.084	0.047 + 0.018*SL	0.053 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.239	0.213 + 0.013*SL	0.215 + 0.012*SL	0.217 + 0.012*SL
	t_{PHL}	0.262	0.235 + 0.014*SL	0.248 + 0.010*SL	0.261 + 0.010*SL
E to Y	t_R	0.091	0.041 + 0.025*SL	0.036 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.085	0.051 + 0.017*SL	0.051 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.254	0.228 + 0.013*SL	0.230 + 0.012*SL	0.232 + 0.012*SL
	t_{PHL}	0.261	0.234 + 0.014*SL	0.247 + 0.010*SL	0.260 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND5D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.042 + 0.012*SL	0.041 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.073	0.053 + 0.010*SL	0.059 + 0.008*SL	0.059 + 0.008*SL
	t_{PLH}	0.265	0.249 + 0.008*SL	0.255 + 0.006*SL	0.258 + 0.006*SL
	t_{PHL}	0.272	0.254 + 0.009*SL	0.265 + 0.006*SL	0.285 + 0.005*SL
B to Y	t_R	0.067	0.042 + 0.012*SL	0.041 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.073	0.053 + 0.010*SL	0.059 + 0.008*SL	0.059 + 0.008*SL
	t_{PLH}	0.282	0.266 + 0.008*SL	0.272 + 0.006*SL	0.275 + 0.006*SL
	t_{PHL}	0.276	0.258 + 0.009*SL	0.269 + 0.006*SL	0.289 + 0.005*SL
C to Y	t_R	0.067	0.043 + 0.012*SL	0.041 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.073	0.053 + 0.010*SL	0.059 + 0.008*SL	0.059 + 0.008*SL
	t_{PLH}	0.298	0.282 + 0.008*SL	0.288 + 0.006*SL	0.291 + 0.006*SL
	t_{PHL}	0.277	0.259 + 0.009*SL	0.270 + 0.006*SL	0.290 + 0.005*SL
D to Y	t_R	0.069	0.046 + 0.011*SL	0.042 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.072	0.052 + 0.010*SL	0.058 + 0.008*SL	0.059 + 0.008*SL
	t_{PLH}	0.257	0.241 + 0.008*SL	0.247 + 0.006*SL	0.250 + 0.006*SL
	t_{PHL}	0.272	0.254 + 0.009*SL	0.266 + 0.006*SL	0.285 + 0.005*SL
E to Y	t_R	0.070	0.047 + 0.011*SL	0.042 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.072	0.052 + 0.010*SL	0.059 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.272	0.256 + 0.008*SL	0.262 + 0.006*SL	0.266 + 0.006*SL
	t_{PHL}	0.271	0.253 + 0.009*SL	0.264 + 0.006*SL	0.284 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND5D4_LP

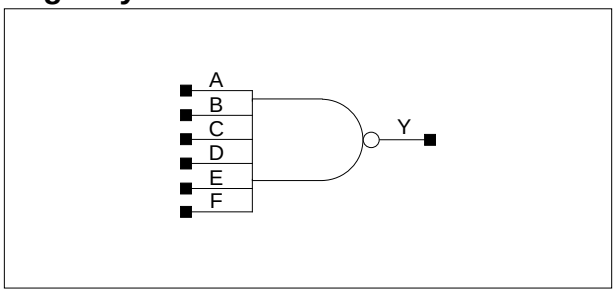
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.076	0.064 + 0.006*SL	0.064 + 0.006*SL	0.053 + 0.006*SL
	t_F	0.084	0.072 + 0.006*SL	0.079 + 0.004*SL	0.089 + 0.004*SL
	t_{PLH}	0.317	0.306 + 0.006*SL	0.313 + 0.004*SL	0.329 + 0.003*SL
	t_{PHL}	0.329	0.316 + 0.006*SL	0.326 + 0.004*SL	0.360 + 0.003*SL
B to Y	t_R	0.077	0.064 + 0.006*SL	0.065 + 0.006*SL	0.053 + 0.006*SL
	t_F	0.085	0.072 + 0.006*SL	0.080 + 0.004*SL	0.089 + 0.004*SL
	t_{PLH}	0.334	0.323 + 0.006*SL	0.331 + 0.004*SL	0.347 + 0.003*SL
	t_{PHL}	0.332	0.320 + 0.006*SL	0.330 + 0.004*SL	0.364 + 0.003*SL
C to Y	t_R	0.077	0.064 + 0.006*SL	0.066 + 0.006*SL	0.053 + 0.006*SL
	t_F	0.084	0.072 + 0.006*SL	0.079 + 0.004*SL	0.089 + 0.004*SL
	t_{PLH}	0.350	0.339 + 0.006*SL	0.347 + 0.004*SL	0.363 + 0.003*SL
	t_{PHL}	0.333	0.321 + 0.006*SL	0.331 + 0.004*SL	0.365 + 0.003*SL
D to Y	t_R	0.077	0.062 + 0.008*SL	0.069 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.086	0.073 + 0.007*SL	0.081 + 0.004*SL	0.089 + 0.004*SL
	t_{PLH}	0.313	0.302 + 0.006*SL	0.310 + 0.004*SL	0.326 + 0.003*SL
	t_{PHL}	0.327	0.314 + 0.006*SL	0.325 + 0.004*SL	0.358 + 0.003*SL
E to Y	t_R	0.077	0.062 + 0.008*SL	0.069 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.085	0.072 + 0.006*SL	0.079 + 0.004*SL	0.090 + 0.004*SL
	t_{PLH}	0.329	0.317 + 0.006*SL	0.326 + 0.004*SL	0.342 + 0.003*SL
	t_{PHL}	0.326	0.314 + 0.006*SL	0.324 + 0.004*SL	0.357 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

ND6_LP/ND6D2_LP/ND6D4_LP

6-Input NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	1	1	1	0
Other States						1

Cell Data

Input Load (SL)																	
ND6_LP						*ND6D2_LP*						*ND6D4_LP*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.8	0.8	0.8	0.8	0.8	0.8	0.7	0.7	0.7	0.7	0.7	0.7	0.6	0.6	0.6	0.6	0.6	0.6

Gate Count		
ND6_LP	*ND6D2_LP*	*ND6D4_LP*
3.67	4.00	4.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.089	0.038 + 0.025*SL	0.034 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.085	0.049 + 0.018*SL	0.054 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.249	0.223 + 0.013*SL	0.225 + 0.012*SL	0.226 + 0.012*SL
	t_{PHL}	0.261	0.234 + 0.014*SL	0.247 + 0.010*SL	0.260 + 0.010*SL
B to Y	t_R	0.089	0.038 + 0.025*SL	0.034 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.085	0.048 + 0.018*SL	0.054 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.266	0.240 + 0.013*SL	0.242 + 0.012*SL	0.243 + 0.012*SL
	t_{PHL}	0.265	0.238 + 0.014*SL	0.251 + 0.010*SL	0.264 + 0.010*SL
C to Y	t_R	0.090	0.040 + 0.025*SL	0.034 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.085	0.049 + 0.018*SL	0.054 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.281	0.255 + 0.013*SL	0.258 + 0.012*SL	0.259 + 0.012*SL
	t_{PHL}	0.266	0.238 + 0.014*SL	0.252 + 0.010*SL	0.265 + 0.010*SL
D to Y	t_R	0.091	0.042 + 0.025*SL	0.036 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.085	0.051 + 0.017*SL	0.052 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.261	0.235 + 0.013*SL	0.237 + 0.012*SL	0.239 + 0.012*SL
	t_{PHL}	0.289	0.262 + 0.014*SL	0.275 + 0.010*SL	0.288 + 0.010*SL
E to Y	t_R	0.092	0.042 + 0.025*SL	0.036 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.085	0.049 + 0.018*SL	0.054 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.279	0.253 + 0.013*SL	0.255 + 0.012*SL	0.257 + 0.012*SL
	t_{PHL}	0.292	0.265 + 0.014*SL	0.279 + 0.010*SL	0.292 + 0.010*SL
F to Y	t_R	0.090	0.041 + 0.025*SL	0.035 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.085	0.051 + 0.017*SL	0.051 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.294	0.268 + 0.013*SL	0.271 + 0.012*SL	0.272 + 0.012*SL
	t_{PHL}	0.294	0.267 + 0.014*SL	0.280 + 0.010*SL	0.293 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND6D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.064	0.040 + 0.012*SL	0.037 + 0.013*SL	0.028 + 0.013*SL
	t_F	0.074	0.053 + 0.010*SL	0.060 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.269	0.255 + 0.007*SL	0.259 + 0.006*SL	0.261 + 0.006*SL
	t_{PHL}	0.272	0.254 + 0.009*SL	0.265 + 0.006*SL	0.286 + 0.005*SL
B to Y	t_R	0.064	0.041 + 0.012*SL	0.037 + 0.013*SL	0.028 + 0.013*SL
	t_F	0.074	0.053 + 0.010*SL	0.060 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.292	0.277 + 0.007*SL	0.281 + 0.006*SL	0.284 + 0.006*SL
	t_{PHL}	0.276	0.258 + 0.009*SL	0.269 + 0.006*SL	0.290 + 0.005*SL
C to Y	t_R	0.064	0.041 + 0.012*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.074	0.054 + 0.010*SL	0.060 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.313	0.298 + 0.008*SL	0.303 + 0.006*SL	0.305 + 0.006*SL
	t_{PHL}	0.277	0.259 + 0.009*SL	0.270 + 0.006*SL	0.291 + 0.005*SL
D to Y	t_R	0.066	0.043 + 0.012*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.074	0.053 + 0.010*SL	0.061 + 0.008*SL	0.060 + 0.008*SL
	t_{PLH}	0.280	0.265 + 0.007*SL	0.269 + 0.006*SL	0.272 + 0.006*SL
	t_{PHL}	0.300	0.281 + 0.009*SL	0.293 + 0.006*SL	0.314 + 0.005*SL
E to Y	t_R	0.066	0.044 + 0.011*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.074	0.054 + 0.010*SL	0.060 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.303	0.288 + 0.007*SL	0.292 + 0.006*SL	0.295 + 0.006*SL
	t_{PHL}	0.305	0.286 + 0.009*SL	0.298 + 0.006*SL	0.319 + 0.005*SL
F to Y	t_R	0.067	0.044 + 0.011*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.073	0.052 + 0.010*SL	0.059 + 0.009*SL	0.061 + 0.008*SL
	t_{PLH}	0.323	0.308 + 0.007*SL	0.313 + 0.006*SL	0.315 + 0.006*SL
	t_{PHL}	0.306	0.287 + 0.009*SL	0.299 + 0.006*SL	0.319 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND6D4_LP

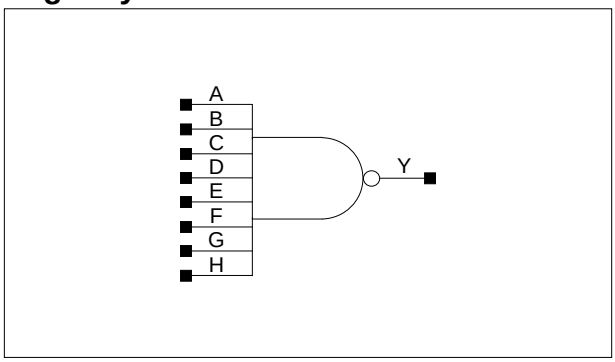
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.065	0.053 + 0.006*SL	0.053 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.086	0.073 + 0.007*SL	0.081 + 0.004*SL	0.092 + 0.004*SL
	t_{PLH}	0.331	0.321 + 0.005*SL	0.327 + 0.003*SL	0.336 + 0.003*SL
	t_{PHL}	0.322	0.310 + 0.006*SL	0.320 + 0.004*SL	0.354 + 0.003*SL
B to Y	t_R	0.066	0.055 + 0.006*SL	0.054 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.087	0.073 + 0.007*SL	0.082 + 0.004*SL	0.090 + 0.004*SL
	t_{PLH}	0.364	0.354 + 0.005*SL	0.360 + 0.003*SL	0.368 + 0.003*SL
	t_{PHL}	0.327	0.314 + 0.006*SL	0.325 + 0.004*SL	0.359 + 0.003*SL
C to Y	t_R	0.067	0.055 + 0.006*SL	0.055 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.087	0.073 + 0.007*SL	0.082 + 0.004*SL	0.090 + 0.004*SL
	t_{PLH}	0.396	0.386 + 0.005*SL	0.392 + 0.003*SL	0.401 + 0.003*SL
	t_{PHL}	0.328	0.315 + 0.006*SL	0.326 + 0.004*SL	0.360 + 0.003*SL
D to Y	t_R	0.065	0.052 + 0.007*SL	0.054 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.086	0.073 + 0.006*SL	0.080 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.337	0.327 + 0.005*SL	0.333 + 0.003*SL	0.341 + 0.003*SL
	t_{PHL}	0.351	0.338 + 0.006*SL	0.348 + 0.004*SL	0.383 + 0.003*SL
E to Y	t_R	0.065	0.054 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.086	0.073 + 0.006*SL	0.080 + 0.005*SL	0.092 + 0.004*SL
	t_{PLH}	0.370	0.361 + 0.005*SL	0.366 + 0.003*SL	0.375 + 0.003*SL
	t_{PHL}	0.356	0.344 + 0.006*SL	0.354 + 0.004*SL	0.388 + 0.003*SL
F to Y	t_R	0.066	0.053 + 0.006*SL	0.055 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.087	0.073 + 0.007*SL	0.082 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.400	0.391 + 0.005*SL	0.397 + 0.003*SL	0.405 + 0.003*SL
	t_{PHL}	0.358	0.345 + 0.006*SL	0.355 + 0.004*SL	0.390 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

ND8_LP/ND8D2_LP/ND8D4_LP

8-Input NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	1	1	1	1	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
ND8_LP								*ND8_LP*
A	B	C	D	E	F	G	H	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	4.33
ND8D2_LP								*ND8D2_LP*
A	B	C	D	E	F	G	H	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	4.67
ND8D4_LP								*ND8D4_LP*
A	B	C	D	E	F	G	H	
0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	5.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.089	0.039 + 0.025*SL	0.034 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.086	0.052 + 0.017*SL	0.052 + 0.017*SL	0.044 + 0.017*SL
	t_{PLH}	0.270	0.244 + 0.013*SL	0.246 + 0.012*SL	0.247 + 0.012*SL
	t_{PHL}	0.282	0.255 + 0.014*SL	0.268 + 0.010*SL	0.281 + 0.010*SL
B to Y	t_R	0.089	0.039 + 0.025*SL	0.034 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.086	0.050 + 0.018*SL	0.055 + 0.017*SL	0.044 + 0.017*SL
	t_{PLH}	0.291	0.265 + 0.013*SL	0.267 + 0.012*SL	0.268 + 0.012*SL
	t_{PHL}	0.291	0.264 + 0.014*SL	0.277 + 0.010*SL	0.291 + 0.010*SL
C to Y	t_R	0.090	0.040 + 0.025*SL	0.035 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.086	0.051 + 0.017*SL	0.054 + 0.017*SL	0.044 + 0.017*SL
	t_{PLH}	0.309	0.283 + 0.013*SL	0.285 + 0.012*SL	0.286 + 0.012*SL
	t_{PHL}	0.297	0.270 + 0.014*SL	0.283 + 0.010*SL	0.297 + 0.010*SL
D to Y	t_R	0.092	0.042 + 0.025*SL	0.037 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.086	0.052 + 0.017*SL	0.053 + 0.017*SL	0.044 + 0.017*SL
	t_{PLH}	0.326	0.300 + 0.013*SL	0.302 + 0.012*SL	0.304 + 0.012*SL
	t_{PHL}	0.301	0.274 + 0.014*SL	0.287 + 0.010*SL	0.301 + 0.010*SL
E to Y	t_R	0.092	0.042 + 0.025*SL	0.037 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.085	0.051 + 0.017*SL	0.052 + 0.017*SL	0.044 + 0.017*SL
	t_{PLH}	0.283	0.257 + 0.013*SL	0.260 + 0.012*SL	0.262 + 0.012*SL
	t_{PHL}	0.309	0.281 + 0.014*SL	0.295 + 0.010*SL	0.308 + 0.010*SL
F to Y	t_R	0.092	0.043 + 0.025*SL	0.037 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.085	0.050 + 0.017*SL	0.052 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.305	0.279 + 0.013*SL	0.282 + 0.012*SL	0.283 + 0.012*SL
	t_{PHL}	0.318	0.291 + 0.014*SL	0.304 + 0.010*SL	0.317 + 0.010*SL
G to Y	t_R	0.093	0.043 + 0.025*SL	0.037 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.086	0.051 + 0.018*SL	0.055 + 0.017*SL	0.044 + 0.017*SL
	t_{PLH}	0.324	0.298 + 0.013*SL	0.301 + 0.012*SL	0.303 + 0.012*SL
	t_{PHL}	0.324	0.297 + 0.014*SL	0.310 + 0.010*SL	0.324 + 0.010*SL
H to Y	t_R	0.092	0.043 + 0.025*SL	0.036 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.085	0.050 + 0.018*SL	0.053 + 0.017*SL	0.043 + 0.017*SL
	t_{PLH}	0.340	0.313 + 0.013*SL	0.316 + 0.012*SL	0.318 + 0.012*SL
	t_{PHL}	0.327	0.300 + 0.014*SL	0.313 + 0.010*SL	0.326 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND8D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.043 + 0.011*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.074	0.054 + 0.010*SL	0.061 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.281	0.266 + 0.007*SL	0.271 + 0.006*SL	0.273 + 0.006*SL
	t_{PHL}	0.297	0.279 + 0.009*SL	0.290 + 0.006*SL	0.311 + 0.005*SL
B to Y	t_R	0.066	0.043 + 0.011*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.074	0.054 + 0.010*SL	0.061 + 0.008*SL	0.060 + 0.008*SL
	t_{PLH}	0.305	0.290 + 0.007*SL	0.294 + 0.006*SL	0.297 + 0.006*SL
	t_{PHL}	0.306	0.288 + 0.009*SL	0.300 + 0.006*SL	0.320 + 0.005*SL
C to Y	t_R	0.067	0.044 + 0.011*SL	0.039 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.075	0.055 + 0.010*SL	0.061 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.326	0.311 + 0.007*SL	0.315 + 0.006*SL	0.318 + 0.006*SL
	t_{PHL}	0.313	0.294 + 0.009*SL	0.306 + 0.006*SL	0.327 + 0.005*SL
D to Y	t_R	0.067	0.045 + 0.011*SL	0.039 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.075	0.055 + 0.010*SL	0.061 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.346	0.331 + 0.008*SL	0.336 + 0.006*SL	0.338 + 0.006*SL
	t_{PHL}	0.317	0.298 + 0.009*SL	0.310 + 0.006*SL	0.331 + 0.005*SL
E to Y	t_R	0.066	0.042 + 0.012*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.074	0.054 + 0.010*SL	0.061 + 0.008*SL	0.060 + 0.008*SL
	t_{PLH}	0.294	0.279 + 0.007*SL	0.283 + 0.006*SL	0.286 + 0.006*SL
	t_{PHL}	0.324	0.306 + 0.009*SL	0.318 + 0.006*SL	0.338 + 0.005*SL
F to Y	t_R	0.065	0.041 + 0.012*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.074	0.053 + 0.010*SL	0.060 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.319	0.304 + 0.007*SL	0.308 + 0.006*SL	0.311 + 0.006*SL
	t_{PHL}	0.334	0.315 + 0.009*SL	0.327 + 0.006*SL	0.348 + 0.005*SL
G to Y	t_R	0.065	0.041 + 0.012*SL	0.039 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.075	0.055 + 0.010*SL	0.061 + 0.008*SL	0.061 + 0.008*SL
	t_{PLH}	0.341	0.326 + 0.008*SL	0.330 + 0.006*SL	0.333 + 0.006*SL
	t_{PHL}	0.340	0.322 + 0.009*SL	0.333 + 0.006*SL	0.354 + 0.005*SL
H to Y	t_R	0.066	0.043 + 0.012*SL	0.039 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.074	0.054 + 0.010*SL	0.061 + 0.008*SL	0.060 + 0.008*SL
	t_{PLH}	0.358	0.343 + 0.008*SL	0.348 + 0.006*SL	0.350 + 0.006*SL
	t_{PHL}	0.343	0.324 + 0.009*SL	0.336 + 0.006*SL	0.357 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

ND8D4_LP

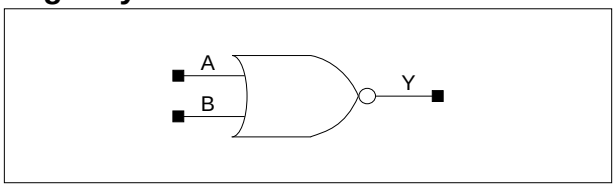
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.055 + 0.006*SL	0.054 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.086	0.074 + 0.006*SL	0.080 + 0.005*SL	0.093 + 0.004*SL
	t_{PLH}	0.342	0.332 + 0.005*SL	0.338 + 0.003*SL	0.347 + 0.003*SL
	t_{PHL}	0.347	0.334 + 0.006*SL	0.344 + 0.004*SL	0.379 + 0.003*SL
B to Y	t_R	0.067	0.054 + 0.006*SL	0.055 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.086	0.074 + 0.006*SL	0.080 + 0.005*SL	0.093 + 0.004*SL
	t_{PLH}	0.376	0.366 + 0.005*SL	0.372 + 0.003*SL	0.381 + 0.003*SL
	t_{PHL}	0.356	0.344 + 0.006*SL	0.354 + 0.004*SL	0.389 + 0.003*SL
C to Y	t_R	0.068	0.056 + 0.006*SL	0.056 + 0.006*SL	0.041 + 0.007*SL
	t_F	0.087	0.073 + 0.007*SL	0.082 + 0.004*SL	0.092 + 0.004*SL
	t_{PLH}	0.406	0.396 + 0.005*SL	0.402 + 0.003*SL	0.411 + 0.003*SL
	t_{PHL}	0.363	0.350 + 0.006*SL	0.360 + 0.004*SL	0.395 + 0.003*SL
D to Y	t_R	0.068	0.056 + 0.006*SL	0.056 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.086	0.073 + 0.006*SL	0.081 + 0.005*SL	0.092 + 0.004*SL
	t_{PLH}	0.436	0.426 + 0.005*SL	0.432 + 0.003*SL	0.441 + 0.003*SL
	t_{PHL}	0.367	0.354 + 0.006*SL	0.364 + 0.004*SL	0.399 + 0.003*SL
E to Y	t_R	0.066	0.054 + 0.006*SL	0.053 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.086	0.074 + 0.006*SL	0.080 + 0.005*SL	0.093 + 0.004*SL
	t_{PLH}	0.352	0.343 + 0.005*SL	0.348 + 0.003*SL	0.357 + 0.003*SL
	t_{PHL}	0.373	0.361 + 0.006*SL	0.371 + 0.004*SL	0.405 + 0.003*SL
F to Y	t_R	0.067	0.055 + 0.006*SL	0.053 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.086	0.074 + 0.006*SL	0.081 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.387	0.378 + 0.005*SL	0.384 + 0.003*SL	0.392 + 0.003*SL
	t_{PHL}	0.382	0.369 + 0.006*SL	0.379 + 0.004*SL	0.414 + 0.003*SL
G to Y	t_R	0.066	0.053 + 0.007*SL	0.056 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.086	0.074 + 0.006*SL	0.080 + 0.005*SL	0.093 + 0.004*SL
	t_{PLH}	0.419	0.409 + 0.005*SL	0.415 + 0.003*SL	0.424 + 0.003*SL
	t_{PHL}	0.390	0.377 + 0.006*SL	0.387 + 0.004*SL	0.422 + 0.003*SL
H to Y	t_R	0.068	0.057 + 0.006*SL	0.056 + 0.006*SL	0.041 + 0.007*SL
	t_F	0.086	0.074 + 0.006*SL	0.081 + 0.005*SL	0.092 + 0.004*SL
	t_{PLH}	0.445	0.435 + 0.005*SL	0.442 + 0.003*SL	0.450 + 0.003*SL
	t_{PHL}	0.393	0.380 + 0.006*SL	0.390 + 0.004*SL	0.425 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

NR2_LP/NR2A_LP/NR2D2_LP/NR2D4_LP/NR2D8_LP

2-Input NOR with 1X/2X P-Tr, 1X N-Tr/2X/4X/8X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Cell Data

Input Load (SL)									
NR2_LP		*NR2A_LP*		*NR2D2_LP*		*NR2D4_LP*		*NR2D8_LP*	
A	B	A	B	A	B	A	B	A	B
1.1	1.1	1.8	1.9	2.2	2.3	0.8	0.8	1.1	1.1
Gate Count									
NR2_LP		*NR2A_LP*		*NR2D2_LP*		*NR2D4_LP*		*NR2D8_LP*	
1.00		1.67		1.67		2.67		4.33	

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.204	0.105 + 0.049*SL	0.092 + 0.052*SL	0.081 + 0.053*SL
	t_F	0.086	0.059 + 0.013*SL	0.054 + 0.015*SL	0.031 + 0.016*SL
	t_{PLH}	0.142	0.091 + 0.026*SL	0.091 + 0.026*SL	0.092 + 0.026*SL
	t_{PHL}	0.073	0.047 + 0.013*SL	0.064 + 0.009*SL	0.067 + 0.009*SL
B to Y	t_R	0.194	0.091 + 0.051*SL	0.086 + 0.053*SL	0.081 + 0.053*SL
	t_F	0.098	0.072 + 0.013*SL	0.065 + 0.015*SL	0.044 + 0.016*SL
	t_{PLH}	0.162	0.110 + 0.026*SL	0.111 + 0.026*SL	0.112 + 0.026*SL
	t_{PHL}	0.086	0.063 + 0.012*SL	0.074 + 0.009*SL	0.076 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NR2A_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.139	0.095 + 0.022*SL	0.083 + 0.025*SL	0.062 + 0.026*SL
	t_F	0.097	0.065 + 0.016*SL	0.056 + 0.018*SL	0.036 + 0.019*SL
	t_{PLH}	0.101	0.072 + 0.015*SL	0.079 + 0.013*SL	0.080 + 0.013*SL
	t_{PHL}	0.094	0.067 + 0.013*SL	0.078 + 0.011*SL	0.080 + 0.011*SL
B to Y	t_R	0.123	0.074 + 0.025*SL	0.069 + 0.026*SL	0.060 + 0.027*SL
	t_F	0.122	0.088 + 0.017*SL	0.082 + 0.019*SL	0.066 + 0.020*SL
	t_{PLH}	0.123	0.096 + 0.014*SL	0.099 + 0.013*SL	0.100 + 0.013*SL
	t_{PHL}	0.121	0.098 + 0.012*SL	0.101 + 0.011*SL	0.105 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.149	0.103 + 0.023*SL	0.094 + 0.025*SL	0.075 + 0.026*SL
	t_F	0.069	0.053 + 0.008*SL	0.057 + 0.007*SL	0.044 + 0.008*SL
	t_{PLH}	0.112	0.085 + 0.014*SL	0.088 + 0.013*SL	0.087 + 0.013*SL
	t_{PHL}	0.057	0.040 + 0.008*SL	0.053 + 0.005*SL	0.065 + 0.004*SL
B to Y	t_R	0.135	0.085 + 0.025*SL	0.081 + 0.026*SL	0.074 + 0.027*SL
	t_F	0.081	0.067 + 0.007*SL	0.067 + 0.007*SL	0.055 + 0.008*SL
	t_{PLH}	0.132	0.105 + 0.013*SL	0.107 + 0.013*SL	0.108 + 0.013*SL
	t_{PHL}	0.071	0.057 + 0.007*SL	0.066 + 0.005*SL	0.074 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NR2D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.063	0.052 + 0.005*SL	0.049 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.055	0.046 + 0.005*SL	0.048 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.278	0.269 + 0.005*SL	0.274 + 0.003*SL	0.282 + 0.003*SL
	t_{PHL}	0.219	0.210 + 0.005*SL	0.217 + 0.003*SL	0.234 + 0.002*SL
B to Y	t_R	0.062	0.048 + 0.007*SL	0.051 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.055	0.045 + 0.005*SL	0.048 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.298	0.289 + 0.005*SL	0.294 + 0.003*SL	0.302 + 0.003*SL
	t_{PHL}	0.235	0.226 + 0.005*SL	0.233 + 0.003*SL	0.250 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

NR2D8_LP

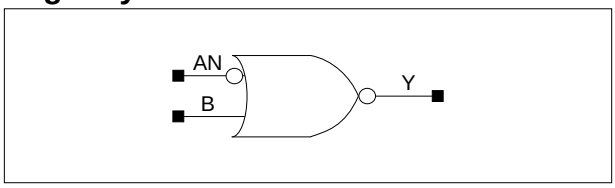
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.060	0.054 + 0.003*SL	0.053 + 0.003*SL	0.039 + 0.003*SL
	t_F	0.050	0.046 + 0.002*SL	0.045 + 0.002*SL	0.044 + 0.002*SL
	t_{PLH}	0.300	0.294 + 0.003*SL	0.298 + 0.002*SL	0.309 + 0.002*SL
	t_{PHL}	0.210	0.205 + 0.003*SL	0.209 + 0.002*SL	0.228 + 0.001*SL
B to Y	t_R	0.060	0.054 + 0.003*SL	0.053 + 0.003*SL	0.039 + 0.003*SL
	t_F	0.049	0.044 + 0.002*SL	0.045 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.321	0.316 + 0.003*SL	0.319 + 0.002*SL	0.330 + 0.002*SL
	t_{PHL}	0.224	0.219 + 0.003*SL	0.223 + 0.002*SL	0.241 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

NR2B_LP/NR2BD2_LP/NR2BD4_LP/NR2BD8_LP

2-Input NOR with one Inverted Input, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

AN	B	Y
0	0	0
0	1	0
1	0	1
1	1	0

Cell Data

Input Load (SL)							
NR2B_LP		*NR2BD2_LP*		*NR2BD4_LP*		*NR2BD8_LP*	
AN	B	AN	B	AN	B	AN	B
0.6	1.2	0.8	2.3	0.5	0.8	0.6	1.1

Gate Count			
NR2B_LP	*NR2BD2_LP*	*NR2BD4_LP*	*NR2BD8_LP*
1.33	2.00	3.33	5.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR2B_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.192	0.087 + 0.053*SL	0.084 + 0.053*SL	0.084 + 0.053*SL
	t_F	0.073	0.041 + 0.016*SL	0.042 + 0.015*SL	0.033 + 0.016*SL
	t_{PLH}	0.183	0.130 + 0.026*SL	0.132 + 0.026*SL	0.135 + 0.026*SL
	t_{PHL}	0.175	0.153 + 0.011*SL	0.161 + 0.009*SL	0.166 + 0.009*SL
B to Y	t_R	0.198	0.095 + 0.051*SL	0.088 + 0.053*SL	0.083 + 0.053*SL
	t_F	0.098	0.073 + 0.013*SL	0.065 + 0.015*SL	0.045 + 0.016*SL
	t_{PLH}	0.166	0.114 + 0.026*SL	0.115 + 0.026*SL	0.116 + 0.026*SL
	t_{PHL}	0.087	0.064 + 0.012*SL	0.075 + 0.009*SL	0.078 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NR2BD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.135	0.083 + 0.026*SL	0.081 + 0.026*SL	0.077 + 0.027*SL
	t_F	0.062	0.048 + 0.007*SL	0.045 + 0.008*SL	0.041 + 0.008*SL
	t_{PLH}	0.174	0.147 + 0.013*SL	0.148 + 0.013*SL	0.150 + 0.013*SL
	t_{PHL}	0.174	0.161 + 0.007*SL	0.168 + 0.005*SL	0.178 + 0.004*SL
B to Y	t_R	0.139	0.089 + 0.025*SL	0.084 + 0.026*SL	0.077 + 0.027*SL
	t_F	0.083	0.069 + 0.007*SL	0.069 + 0.007*SL	0.056 + 0.008*SL
	t_{PLH}	0.136	0.109 + 0.014*SL	0.111 + 0.013*SL	0.112 + 0.013*SL
	t_{PHL}	0.071	0.057 + 0.007*SL	0.066 + 0.005*SL	0.074 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR2BD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.063	0.052 + 0.005*SL	0.049 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.055	0.045 + 0.005*SL	0.049 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.316	0.306 + 0.005*SL	0.312 + 0.003*SL	0.319 + 0.003*SL
	t_{PHL}	0.310	0.301 + 0.005*SL	0.307 + 0.003*SL	0.324 + 0.002*SL
B to Y	t_R	0.061	0.048 + 0.007*SL	0.050 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.054	0.045 + 0.005*SL	0.047 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.299	0.290 + 0.005*SL	0.296 + 0.003*SL	0.303 + 0.003*SL
	t_{PHL}	0.234	0.224 + 0.005*SL	0.231 + 0.003*SL	0.248 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

NR2BD8_LP

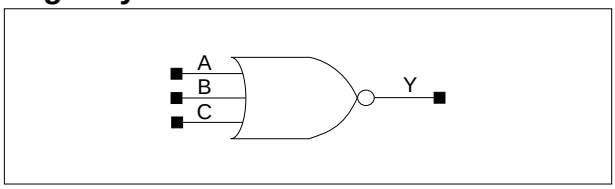
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.060	0.054 + 0.003*SL	0.054 + 0.003*SL	0.040 + 0.003*SL
	t_F	0.049	0.044 + 0.002*SL	0.045 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.341	0.336 + 0.003*SL	0.339 + 0.002*SL	0.350 + 0.002*SL
	t_{PHL}	0.310	0.305 + 0.003*SL	0.309 + 0.002*SL	0.328 + 0.001*SL
B to Y	t_R	0.060	0.054 + 0.003*SL	0.054 + 0.003*SL	0.039 + 0.003*SL
	t_F	0.050	0.046 + 0.002*SL	0.046 + 0.002*SL	0.043 + 0.002*SL
	t_{PLH}	0.324	0.319 + 0.003*SL	0.323 + 0.002*SL	0.333 + 0.002*SL
	t_{PHL}	0.223	0.218 + 0.003*SL	0.222 + 0.002*SL	0.241 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

NR3_LP/NR3A_LP/NR3D2_LP/NR3D4_LP

3-Input NOR with 1X/2X P-Tr, 1X N-Tr/2X/4X/8X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
Other States			0

Cell Data

Input Load (SL)											
NR3_LP			*NR3A_LP*			*NR3D2_LP*			*NR3D4_LP*		
A	B	C	A	B	C	A	B	C	A	B	C
1.0	1.0	1.0	1.7	1.8	1.9	2.0	2.0	2.0	0.9	0.9	0.9

Gate Count			
NR3_LP	*NR3A_LP*	*NR3D2_LP*	*NR3D4_LP*
1.33	2.00	2.33	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.317	0.164 + 0.076*SL	0.151 + 0.080*SL	0.153 + 0.080*SL
	t_F	0.113	0.067 + 0.023*SL	0.056 + 0.026*SL	0.037 + 0.027*SL
	t_{PLH}	0.178	0.100 + 0.039*SL	0.099 + 0.039*SL	0.102 + 0.039*SL
	t_{PHL}	0.106	0.073 + 0.016*SL	0.080 + 0.014*SL	0.082 + 0.014*SL
B to Y	t_R	0.316	0.160 + 0.078*SL	0.155 + 0.079*SL	0.153 + 0.080*SL
	t_F	0.130	0.083 + 0.023*SL	0.074 + 0.026*SL	0.058 + 0.027*SL
	t_{PLH}	0.226	0.147 + 0.039*SL	0.148 + 0.039*SL	0.150 + 0.039*SL
	t_{PHL}	0.124	0.093 + 0.015*SL	0.096 + 0.015*SL	0.100 + 0.014*SL
C to Y	t_R	0.315	0.158 + 0.078*SL	0.154 + 0.079*SL	0.153 + 0.080*SL
	t_F	0.149	0.100 + 0.024*SL	0.094 + 0.026*SL	0.080 + 0.027*SL
	t_{PLH}	0.245	0.167 + 0.039*SL	0.168 + 0.039*SL	0.170 + 0.039*SL
	t_{PHL}	0.131	0.099 + 0.016*SL	0.103 + 0.015*SL	0.111 + 0.015*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NR3A_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.205	0.131 + 0.037*SL	0.120 + 0.040*SL	0.108 + 0.040*SL
	t_F	0.119	0.072 + 0.024*SL	0.060 + 0.027*SL	0.045 + 0.028*SL
	t_{PLH}	0.120	0.081 + 0.019*SL	0.079 + 0.020*SL	0.081 + 0.020*SL
	t_{PHL}	0.119	0.086 + 0.016*SL	0.091 + 0.015*SL	0.095 + 0.015*SL
B to Y	t_R	0.202	0.126 + 0.038*SL	0.119 + 0.040*SL	0.113 + 0.040*SL
	t_F	0.155	0.104 + 0.026*SL	0.098 + 0.027*SL	0.090 + 0.028*SL
	t_{PLH}	0.167	0.127 + 0.020*SL	0.129 + 0.020*SL	0.130 + 0.020*SL
	t_{PHL}	0.157	0.124 + 0.016*SL	0.128 + 0.015*SL	0.134 + 0.015*SL
C to Y	t_R	0.199	0.121 + 0.039*SL	0.117 + 0.040*SL	0.113 + 0.040*SL
	t_F	0.194	0.140 + 0.027*SL	0.138 + 0.027*SL	0.135 + 0.028*SL
	t_{PLH}	0.187	0.147 + 0.020*SL	0.149 + 0.020*SL	0.150 + 0.020*SL
	t_{PHL}	0.177	0.142 + 0.018*SL	0.149 + 0.016*SL	0.162 + 0.015*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.243	0.168 + 0.037*SL	0.160 + 0.039*SL	0.152 + 0.040*SL
	t_F	0.091	0.069 + 0.011*SL	0.064 + 0.012*SL	0.048 + 0.013*SL
	t_{PLH}	0.141	0.104 + 0.019*SL	0.100 + 0.020*SL	0.102 + 0.019*SL
	t_{PHL}	0.089	0.070 + 0.010*SL	0.079 + 0.007*SL	0.081 + 0.007*SL
B to Y	t_R	0.241	0.164 + 0.039*SL	0.161 + 0.039*SL	0.156 + 0.040*SL
	t_F	0.108	0.086 + 0.011*SL	0.081 + 0.012*SL	0.067 + 0.013*SL
	t_{PLH}	0.188	0.149 + 0.020*SL	0.149 + 0.020*SL	0.151 + 0.019*SL
	t_{PHL}	0.109	0.092 + 0.008*SL	0.095 + 0.007*SL	0.099 + 0.007*SL
C to Y	t_R	0.239	0.161 + 0.039*SL	0.159 + 0.040*SL	0.156 + 0.040*SL
	t_F	0.125	0.102 + 0.012*SL	0.097 + 0.013*SL	0.089 + 0.013*SL
	t_{PLH}	0.208	0.169 + 0.020*SL	0.169 + 0.020*SL	0.170 + 0.019*SL
	t_{PHL}	0.116	0.099 + 0.008*SL	0.101 + 0.008*SL	0.108 + 0.007*SL

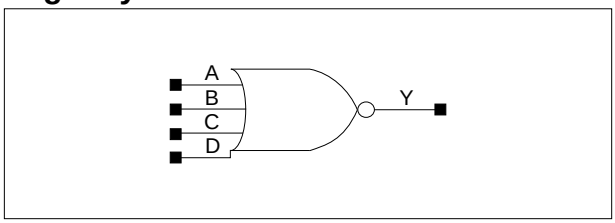
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NR3D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.055 + 0.006*SL	0.055 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.056	0.047 + 0.004*SL	0.048 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.318	0.308 + 0.005*SL	0.315 + 0.003*SL	0.323 + 0.003*SL
	t_{PHL}	0.238	0.228 + 0.005*SL	0.235 + 0.003*SL	0.253 + 0.002*SL
B to Y	t_R	0.067	0.056 + 0.006*SL	0.055 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.056	0.046 + 0.005*SL	0.049 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.369	0.359 + 0.005*SL	0.365 + 0.003*SL	0.373 + 0.003*SL
	t_{PHL}	0.258	0.249 + 0.005*SL	0.256 + 0.003*SL	0.273 + 0.002*SL
C to Y	t_R	0.067	0.056 + 0.006*SL	0.055 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.056	0.045 + 0.006*SL	0.051 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.389	0.379 + 0.005*SL	0.385 + 0.003*SL	0.393 + 0.003*SL
	t_{PHL}	0.269	0.259 + 0.005*SL	0.266 + 0.003*SL	0.284 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	1
Other States				0

Cell Data

Input Load (SL)											
NR4_LP				*NR4D2_LP*				*NR4D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8

Gate Count		
NR4_LP	*NR4D2_LP*	*NR4D4_LP*
3.00	3.33	4.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.104	0.055 + 0.024*SL	0.049 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.071	0.037 + 0.017*SL	0.038 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.291	0.262 + 0.014*SL	0.269 + 0.013*SL	0.272 + 0.012*SL
	t_{PHL}	0.195	0.171 + 0.012*SL	0.179 + 0.010*SL	0.183 + 0.009*SL
B to Y	t_R	0.104	0.055 + 0.024*SL	0.049 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.071	0.038 + 0.017*SL	0.037 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.311	0.282 + 0.014*SL	0.289 + 0.013*SL	0.292 + 0.012*SL
	t_{PHL}	0.209	0.186 + 0.012*SL	0.194 + 0.010*SL	0.198 + 0.009*SL
C to Y	t_R	0.103	0.055 + 0.024*SL	0.049 + 0.026*SL	0.037 + 0.027*SL
	t_F	0.073	0.039 + 0.017*SL	0.039 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.286	0.257 + 0.014*SL	0.265 + 0.013*SL	0.268 + 0.012*SL
	t_{PHL}	0.201	0.178 + 0.012*SL	0.186 + 0.010*SL	0.191 + 0.009*SL
D to Y	t_R	0.102	0.054 + 0.024*SL	0.047 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.074	0.042 + 0.016*SL	0.039 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.306	0.277 + 0.014*SL	0.285 + 0.013*SL	0.288 + 0.012*SL
	t_{PHL}	0.217	0.193 + 0.012*SL	0.201 + 0.010*SL	0.206 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR4D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.073	0.049 + 0.012*SL	0.047 + 0.013*SL	0.037 + 0.013*SL
	t_F	0.059	0.041 + 0.009*SL	0.043 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.268	0.251 + 0.008*SL	0.258 + 0.007*SL	0.264 + 0.006*SL
	t_{PHL}	0.213	0.198 + 0.008*SL	0.207 + 0.006*SL	0.219 + 0.005*SL
B to Y	t_R	0.072	0.047 + 0.013*SL	0.048 + 0.013*SL	0.038 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.045 + 0.008*SL	0.040 + 0.009*SL
	t_{PLH}	0.288	0.271 + 0.008*SL	0.278 + 0.007*SL	0.284 + 0.006*SL
	t_{PHL}	0.229	0.214 + 0.008*SL	0.222 + 0.006*SL	0.234 + 0.005*SL
C to Y	t_R	0.072	0.047 + 0.012*SL	0.046 + 0.013*SL	0.036 + 0.013*SL
	t_F	0.063	0.046 + 0.008*SL	0.047 + 0.008*SL	0.042 + 0.009*SL
	t_{PLH}	0.264	0.247 + 0.008*SL	0.254 + 0.007*SL	0.260 + 0.006*SL
	t_{PHL}	0.224	0.208 + 0.008*SL	0.217 + 0.006*SL	0.230 + 0.005*SL
D to Y	t_R	0.073	0.049 + 0.012*SL	0.046 + 0.013*SL	0.038 + 0.013*SL
	t_F	0.062	0.043 + 0.009*SL	0.047 + 0.008*SL	0.042 + 0.009*SL
	t_{PLH}	0.283	0.267 + 0.008*SL	0.274 + 0.007*SL	0.280 + 0.006*SL
	t_{PHL}	0.240	0.224 + 0.008*SL	0.233 + 0.006*SL	0.246 + 0.005*SL

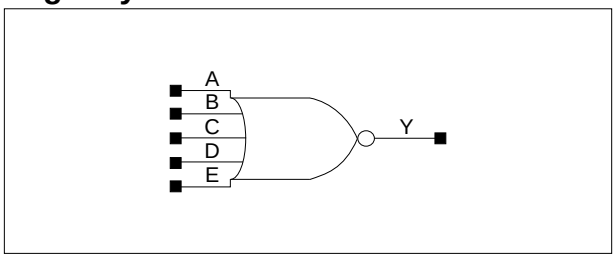
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NR4D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.076	0.063 + 0.007*SL	0.064 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.070	0.059 + 0.005*SL	0.063 + 0.004*SL	0.065 + 0.004*SL
	t_{PLH}	0.303	0.292 + 0.006*SL	0.299 + 0.004*SL	0.316 + 0.003*SL
	t_{PHL}	0.257	0.245 + 0.006*SL	0.255 + 0.003*SL	0.279 + 0.003*SL
B to Y	t_R	0.075	0.061 + 0.007*SL	0.065 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.069	0.057 + 0.006*SL	0.064 + 0.004*SL	0.065 + 0.004*SL
	t_{PLH}	0.323	0.312 + 0.006*SL	0.320 + 0.004*SL	0.337 + 0.003*SL
	t_{PHL}	0.272	0.261 + 0.006*SL	0.270 + 0.003*SL	0.295 + 0.003*SL
C to Y	t_R	0.075	0.062 + 0.007*SL	0.063 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.072	0.060 + 0.006*SL	0.066 + 0.004*SL	0.067 + 0.004*SL
	t_{PLH}	0.296	0.285 + 0.006*SL	0.292 + 0.004*SL	0.310 + 0.003*SL
	t_{PHL}	0.265	0.254 + 0.006*SL	0.263 + 0.003*SL	0.289 + 0.003*SL
D to Y	t_R	0.076	0.062 + 0.007*SL	0.065 + 0.006*SL	0.054 + 0.006*SL
	t_F	0.071	0.058 + 0.006*SL	0.067 + 0.004*SL	0.066 + 0.004*SL
	t_{PLH}	0.316	0.305 + 0.006*SL	0.312 + 0.004*SL	0.330 + 0.003*SL
	t_{PHL}	0.282	0.270 + 0.006*SL	0.280 + 0.003*SL	0.305 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	1
Other States					0

Cell Data

Input Load (SL)														
NR5_LP					*NR5D2_LP*					*NR5D4_LP*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	0.8	0.8	1.0	1.0	1.1	0.8	0.8	1.0	1.0	1.1	0.8	0.8
Gate Count														
NR5_LP					*NR5D2_LP*					*NR5D4_LP*				
3.33					3.67					4.33				

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR5_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.104	0.055 + 0.024*SL	0.049 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.077	0.044 + 0.016*SL	0.042 + 0.017*SL	0.032 + 0.017*SL
	t_{PLH}	0.300	0.272 + 0.014*SL	0.279 + 0.013*SL	0.282 + 0.012*SL
	t_{PHL}	0.224	0.200 + 0.012*SL	0.209 + 0.010*SL	0.215 + 0.009*SL
B to Y	t_R	0.103	0.055 + 0.024*SL	0.048 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.077	0.044 + 0.016*SL	0.043 + 0.017*SL	0.032 + 0.017*SL
	t_{PLH}	0.349	0.320 + 0.014*SL	0.327 + 0.013*SL	0.330 + 0.012*SL
	t_{PHL}	0.245	0.221 + 0.012*SL	0.230 + 0.010*SL	0.236 + 0.009*SL
C to Y	t_R	0.103	0.055 + 0.024*SL	0.048 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.076	0.042 + 0.017*SL	0.044 + 0.017*SL	0.032 + 0.017*SL
	t_{PLH}	0.370	0.341 + 0.014*SL	0.348 + 0.013*SL	0.351 + 0.012*SL
	t_{PHL}	0.256	0.231 + 0.012*SL	0.241 + 0.010*SL	0.247 + 0.009*SL
D to Y	t_R	0.101	0.053 + 0.024*SL	0.046 + 0.026*SL	0.036 + 0.027*SL
	t_F	0.079	0.047 + 0.016*SL	0.044 + 0.017*SL	0.033 + 0.017*SL
	t_{PLH}	0.274	0.245 + 0.014*SL	0.252 + 0.013*SL	0.255 + 0.012*SL
	t_{PHL}	0.215	0.190 + 0.012*SL	0.200 + 0.010*SL	0.206 + 0.010*SL
E to Y	t_R	0.102	0.053 + 0.024*SL	0.047 + 0.026*SL	0.036 + 0.027*SL
	t_F	0.078	0.044 + 0.017*SL	0.044 + 0.017*SL	0.033 + 0.017*SL
	t_{PLH}	0.293	0.264 + 0.014*SL	0.271 + 0.013*SL	0.274 + 0.012*SL
	t_{PHL}	0.230	0.205 + 0.012*SL	0.215 + 0.010*SL	0.222 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR5D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.075	0.052 + 0.012*SL	0.050 + 0.012*SL	0.039 + 0.013*SL
	t_F	0.060	0.041 + 0.009*SL	0.046 + 0.008*SL	0.040 + 0.009*SL
	t_{PLH}	0.295	0.278 + 0.009*SL	0.286 + 0.007*SL	0.292 + 0.006*SL
	t_{PHL}	0.221	0.206 + 0.008*SL	0.215 + 0.006*SL	0.227 + 0.005*SL
B to Y	t_R	0.075	0.050 + 0.013*SL	0.051 + 0.012*SL	0.039 + 0.013*SL
	t_F	0.060	0.041 + 0.009*SL	0.046 + 0.008*SL	0.040 + 0.009*SL
	t_{PLH}	0.344	0.327 + 0.009*SL	0.334 + 0.007*SL	0.341 + 0.006*SL
	t_{PHL}	0.240	0.225 + 0.008*SL	0.234 + 0.006*SL	0.246 + 0.005*SL
C to Y	t_R	0.076	0.052 + 0.012*SL	0.051 + 0.012*SL	0.040 + 0.013*SL
	t_F	0.061	0.042 + 0.009*SL	0.047 + 0.008*SL	0.040 + 0.009*SL
	t_{PLH}	0.365	0.348 + 0.009*SL	0.356 + 0.007*SL	0.362 + 0.006*SL
	t_{PHL}	0.249	0.233 + 0.008*SL	0.242 + 0.006*SL	0.254 + 0.005*SL
D to Y	t_R	0.072	0.047 + 0.012*SL	0.046 + 0.013*SL	0.036 + 0.013*SL
	t_F	0.063	0.046 + 0.008*SL	0.047 + 0.008*SL	0.042 + 0.009*SL
	t_{PLH}	0.263	0.247 + 0.008*SL	0.254 + 0.007*SL	0.260 + 0.006*SL
	t_{PHL}	0.223	0.207 + 0.008*SL	0.216 + 0.006*SL	0.229 + 0.005*SL
E to Y	t_R	0.073	0.049 + 0.012*SL	0.047 + 0.013*SL	0.038 + 0.013*SL
	t_F	0.061	0.044 + 0.009*SL	0.046 + 0.008*SL	0.042 + 0.009*SL
	t_{PLH}	0.283	0.266 + 0.008*SL	0.274 + 0.007*SL	0.280 + 0.006*SL
	t_{PHL}	0.239	0.224 + 0.008*SL	0.233 + 0.006*SL	0.245 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

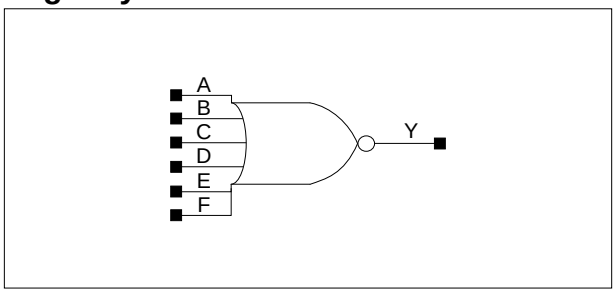
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR5D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.078	0.066 + 0.006*SL	0.067 + 0.006*SL	0.058 + 0.006*SL
	t_F	0.068	0.056 + 0.006*SL	0.064 + 0.004*SL	0.064 + 0.004*SL
	t_{PLH}	0.335	0.324 + 0.006*SL	0.331 + 0.004*SL	0.349 + 0.003*SL
	t_{PHL}	0.264	0.253 + 0.006*SL	0.262 + 0.003*SL	0.287 + 0.003*SL
B to Y	t_R	0.079	0.066 + 0.006*SL	0.067 + 0.006*SL	0.057 + 0.006*SL
	t_F	0.069	0.057 + 0.006*SL	0.064 + 0.004*SL	0.065 + 0.004*SL
	t_{PLH}	0.383	0.372 + 0.006*SL	0.380 + 0.004*SL	0.398 + 0.003*SL
	t_{PHL}	0.283	0.272 + 0.006*SL	0.281 + 0.003*SL	0.306 + 0.003*SL
C to Y	t_R	0.079	0.066 + 0.006*SL	0.067 + 0.006*SL	0.057 + 0.006*SL
	t_F	0.069	0.057 + 0.006*SL	0.065 + 0.004*SL	0.065 + 0.004*SL
	t_{PLH}	0.404	0.393 + 0.006*SL	0.401 + 0.004*SL	0.419 + 0.003*SL
	t_{PHL}	0.292	0.281 + 0.006*SL	0.290 + 0.003*SL	0.315 + 0.003*SL
D to Y	t_R	0.075	0.062 + 0.007*SL	0.063 + 0.006*SL	0.055 + 0.006*SL
	t_F	0.071	0.060 + 0.006*SL	0.066 + 0.004*SL	0.066 + 0.004*SL
	t_{PLH}	0.296	0.285 + 0.006*SL	0.293 + 0.004*SL	0.310 + 0.003*SL
	t_{PHL}	0.265	0.253 + 0.006*SL	0.262 + 0.003*SL	0.289 + 0.003*SL
E to Y	t_R	0.076	0.062 + 0.007*SL	0.065 + 0.006*SL	0.054 + 0.006*SL
	t_F	0.071	0.058 + 0.006*SL	0.067 + 0.004*SL	0.066 + 0.004*SL
	t_{PLH}	0.316	0.305 + 0.006*SL	0.313 + 0.004*SL	0.330 + 0.003*SL
	t_{PHL}	0.281	0.270 + 0.006*SL	0.279 + 0.003*SL	0.305 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
Other States						0

Cell Data

Input Load (SL)																	
NR6_LP						*NR6D2_LP*						*NR6D4_LP*					
A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D	E	F
0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9

Gate Count		
NR6_LP	*NR6D2_LP*	*NR6D4_LP*
3.67	4.00	4.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.096	0.047 + 0.025*SL	0.042 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.073	0.039 + 0.017*SL	0.040 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.281	0.254 + 0.014*SL	0.258 + 0.013*SL	0.261 + 0.012*SL
	t_{PHL}	0.223	0.199 + 0.012*SL	0.208 + 0.010*SL	0.212 + 0.009*SL
B to Y	t_R	0.096	0.047 + 0.025*SL	0.040 + 0.026*SL	0.033 + 0.026*SL
	t_F	0.075	0.042 + 0.016*SL	0.040 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.330	0.302 + 0.014*SL	0.307 + 0.013*SL	0.309 + 0.012*SL
	t_{PHL}	0.243	0.219 + 0.012*SL	0.228 + 0.010*SL	0.233 + 0.009*SL
C to Y	t_R	0.096	0.047 + 0.024*SL	0.040 + 0.026*SL	0.033 + 0.026*SL
	t_F	0.075	0.041 + 0.017*SL	0.041 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.350	0.323 + 0.014*SL	0.328 + 0.013*SL	0.330 + 0.012*SL
	t_{PHL}	0.253	0.229 + 0.012*SL	0.238 + 0.010*SL	0.243 + 0.009*SL
D to Y	t_R	0.095	0.046 + 0.025*SL	0.040 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.076	0.044 + 0.016*SL	0.042 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.280	0.252 + 0.014*SL	0.257 + 0.012*SL	0.259 + 0.012*SL
	t_{PHL}	0.239	0.215 + 0.012*SL	0.224 + 0.010*SL	0.229 + 0.009*SL
E to Y	t_R	0.095	0.045 + 0.025*SL	0.041 + 0.026*SL	0.033 + 0.026*SL
	t_F	0.076	0.043 + 0.017*SL	0.042 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.328	0.301 + 0.014*SL	0.306 + 0.012*SL	0.308 + 0.012*SL
	t_{PHL}	0.258	0.234 + 0.012*SL	0.243 + 0.010*SL	0.249 + 0.009*SL
F to Y	t_R	0.096	0.045 + 0.025*SL	0.042 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.077	0.044 + 0.016*SL	0.042 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.347	0.320 + 0.014*SL	0.325 + 0.012*SL	0.327 + 0.012*SL
	t_{PHL}	0.269	0.245 + 0.012*SL	0.254 + 0.010*SL	0.260 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR6D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.075	0.051 + 0.012*SL	0.049 + 0.012*SL	0.038 + 0.013*SL
	t_F	0.065	0.045 + 0.010*SL	0.051 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.293	0.276 + 0.008*SL	0.283 + 0.007*SL	0.290 + 0.006*SL
	t_{PHL}	0.241	0.225 + 0.008*SL	0.235 + 0.006*SL	0.250 + 0.005*SL
B to Y	t_R	0.074	0.049 + 0.013*SL	0.050 + 0.012*SL	0.039 + 0.013*SL
	t_F	0.065	0.046 + 0.010*SL	0.052 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.341	0.324 + 0.008*SL	0.332 + 0.007*SL	0.338 + 0.006*SL
	t_{PHL}	0.262	0.245 + 0.008*SL	0.255 + 0.006*SL	0.270 + 0.005*SL
C to Y	t_R	0.074	0.049 + 0.013*SL	0.050 + 0.012*SL	0.039 + 0.013*SL
	t_F	0.066	0.047 + 0.009*SL	0.051 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.362	0.345 + 0.008*SL	0.353 + 0.007*SL	0.359 + 0.006*SL
	t_{PHL}	0.273	0.256 + 0.008*SL	0.266 + 0.006*SL	0.281 + 0.005*SL
D to Y	t_R	0.073	0.049 + 0.012*SL	0.047 + 0.013*SL	0.037 + 0.013*SL
	t_F	0.068	0.050 + 0.009*SL	0.055 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.287	0.270 + 0.008*SL	0.277 + 0.007*SL	0.284 + 0.006*SL
	t_{PHL}	0.256	0.239 + 0.008*SL	0.250 + 0.006*SL	0.265 + 0.005*SL
E to Y	t_R	0.074	0.050 + 0.012*SL	0.048 + 0.013*SL	0.038 + 0.013*SL
	t_F	0.069	0.051 + 0.009*SL	0.055 + 0.008*SL	0.049 + 0.008*SL
	t_{PLH}	0.335	0.318 + 0.008*SL	0.325 + 0.007*SL	0.332 + 0.006*SL
	t_{PHL}	0.276	0.259 + 0.008*SL	0.269 + 0.006*SL	0.285 + 0.005*SL
F to Y	t_R	0.073	0.048 + 0.012*SL	0.048 + 0.013*SL	0.038 + 0.013*SL
	t_F	0.069	0.051 + 0.009*SL	0.055 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.354	0.337 + 0.008*SL	0.345 + 0.007*SL	0.351 + 0.006*SL
	t_{PHL}	0.287	0.271 + 0.008*SL	0.281 + 0.006*SL	0.297 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

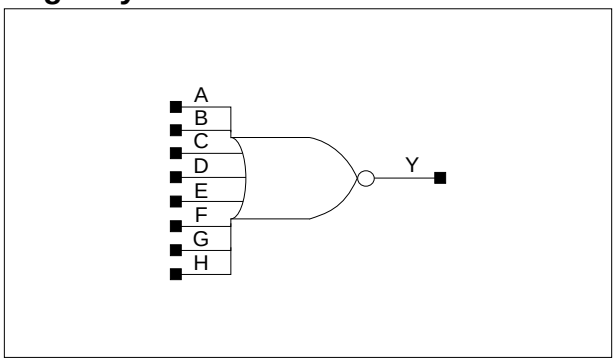
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR6D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.078	0.066 + 0.006*SL	0.066 + 0.006*SL	0.057 + 0.006*SL
	t_F	0.072	0.060 + 0.006*SL	0.067 + 0.004*SL	0.070 + 0.004*SL
	t_{PLH}	0.339	0.327 + 0.006*SL	0.335 + 0.004*SL	0.353 + 0.003*SL
	t_{PHL}	0.280	0.268 + 0.006*SL	0.277 + 0.003*SL	0.304 + 0.003*SL
B to Y	t_R	0.078	0.064 + 0.007*SL	0.068 + 0.006*SL	0.057 + 0.006*SL
	t_F	0.072	0.060 + 0.006*SL	0.068 + 0.004*SL	0.070 + 0.004*SL
	t_{PLH}	0.387	0.376 + 0.006*SL	0.384 + 0.004*SL	0.402 + 0.003*SL
	t_{PHL}	0.300	0.288 + 0.006*SL	0.297 + 0.003*SL	0.324 + 0.003*SL
C to Y	t_R	0.078	0.063 + 0.007*SL	0.068 + 0.006*SL	0.057 + 0.006*SL
	t_F	0.072	0.060 + 0.006*SL	0.068 + 0.004*SL	0.070 + 0.004*SL
	t_{PLH}	0.408	0.397 + 0.006*SL	0.405 + 0.004*SL	0.423 + 0.003*SL
	t_{PHL}	0.311	0.300 + 0.006*SL	0.309 + 0.003*SL	0.336 + 0.003*SL
D to Y	t_R	0.077	0.064 + 0.007*SL	0.066 + 0.006*SL	0.056 + 0.006*SL
	t_F	0.076	0.064 + 0.006*SL	0.071 + 0.004*SL	0.072 + 0.004*SL
	t_{PLH}	0.328	0.316 + 0.006*SL	0.324 + 0.004*SL	0.342 + 0.003*SL
	t_{PHL}	0.291	0.280 + 0.006*SL	0.289 + 0.003*SL	0.317 + 0.003*SL
E to Y	t_R	0.077	0.063 + 0.007*SL	0.066 + 0.006*SL	0.056 + 0.006*SL
	t_F	0.076	0.064 + 0.006*SL	0.071 + 0.004*SL	0.072 + 0.004*SL
	t_{PLH}	0.376	0.365 + 0.006*SL	0.372 + 0.004*SL	0.390 + 0.003*SL
	t_{PHL}	0.311	0.299 + 0.006*SL	0.309 + 0.003*SL	0.336 + 0.003*SL
F to Y	t_R	0.077	0.062 + 0.007*SL	0.067 + 0.006*SL	0.056 + 0.006*SL
	t_F	0.075	0.063 + 0.006*SL	0.071 + 0.004*SL	0.072 + 0.004*SL
	t_{PLH}	0.395	0.384 + 0.006*SL	0.392 + 0.004*SL	0.410 + 0.003*SL
	t_{PHL}	0.323	0.312 + 0.006*SL	0.321 + 0.003*SL	0.349 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
NR8_LP								*NR8_LP*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	1.0	1.0	5.33
NR8D2_LP								*NR8D2_LP*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	1.0	1.0	5.33
NR8D4_LP								*NR8D4_LP*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	0.9	1.0	1.0	6.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.109	0.060 + 0.024*SL	0.055 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.077	0.043 + 0.017*SL	0.045 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.321	0.291 + 0.015*SL	0.300 + 0.013*SL	0.305 + 0.012*SL
	t_{PHL}	0.239	0.214 + 0.012*SL	0.225 + 0.010*SL	0.232 + 0.009*SL
B to Y	t_R	0.108	0.060 + 0.024*SL	0.055 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.078	0.043 + 0.017*SL	0.047 + 0.016*SL	0.034 + 0.017*SL
	t_{PLH}	0.370	0.340 + 0.015*SL	0.349 + 0.013*SL	0.354 + 0.012*SL
	t_{PHL}	0.259	0.234 + 0.012*SL	0.245 + 0.010*SL	0.253 + 0.009*SL
C to Y	t_R	0.108	0.059 + 0.025*SL	0.054 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.078	0.045 + 0.016*SL	0.045 + 0.016*SL	0.035 + 0.017*SL
	t_{PLH}	0.391	0.361 + 0.015*SL	0.370 + 0.013*SL	0.375 + 0.012*SL
	t_{PHL}	0.270	0.245 + 0.013*SL	0.256 + 0.010*SL	0.264 + 0.009*SL
D to Y	t_R	0.108	0.059 + 0.024*SL	0.054 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.080	0.047 + 0.017*SL	0.049 + 0.016*SL	0.036 + 0.017*SL
	t_{PLH}	0.320	0.289 + 0.015*SL	0.299 + 0.013*SL	0.304 + 0.012*SL
	t_{PHL}	0.252	0.227 + 0.013*SL	0.238 + 0.010*SL	0.247 + 0.009*SL
E to Y	t_R	0.109	0.059 + 0.025*SL	0.055 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.080	0.046 + 0.017*SL	0.049 + 0.016*SL	0.036 + 0.017*SL
	t_{PLH}	0.371	0.341 + 0.015*SL	0.351 + 0.013*SL	0.356 + 0.012*SL
	t_{PHL}	0.273	0.248 + 0.013*SL	0.259 + 0.010*SL	0.267 + 0.009*SL
F to Y	t_R	0.109	0.060 + 0.025*SL	0.055 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.081	0.048 + 0.016*SL	0.048 + 0.016*SL	0.036 + 0.017*SL
	t_{PLH}	0.390	0.360 + 0.015*SL	0.370 + 0.013*SL	0.375 + 0.012*SL
	t_{PHL}	0.285	0.259 + 0.013*SL	0.271 + 0.010*SL	0.279 + 0.009*SL
G to Y	t_R	0.107	0.057 + 0.025*SL	0.053 + 0.026*SL	0.041 + 0.026*SL
	t_F	0.082	0.048 + 0.017*SL	0.051 + 0.016*SL	0.038 + 0.017*SL
	t_{PLH}	0.295	0.265 + 0.015*SL	0.275 + 0.013*SL	0.279 + 0.012*SL
	t_{PHL}	0.236	0.211 + 0.013*SL	0.223 + 0.010*SL	0.232 + 0.009*SL
H to Y	t_R	0.106	0.056 + 0.025*SL	0.053 + 0.026*SL	0.041 + 0.026*SL
	t_F	0.083	0.049 + 0.017*SL	0.052 + 0.016*SL	0.038 + 0.017*SL
	t_{PLH}	0.314	0.284 + 0.015*SL	0.293 + 0.013*SL	0.298 + 0.012*SL
	t_{PHL}	0.252	0.226 + 0.013*SL	0.238 + 0.010*SL	0.248 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR8D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.087	0.059 + 0.014*SL	0.064 + 0.012*SL	0.054 + 0.013*SL
	t_F	0.070	0.050 + 0.010*SL	0.057 + 0.008*SL	0.054 + 0.008*SL
	t_{PLH}	0.329	0.310 + 0.010*SL	0.320 + 0.007*SL	0.334 + 0.006*SL
	t_{PHL}	0.259	0.241 + 0.009*SL	0.252 + 0.006*SL	0.271 + 0.005*SL
B to Y	t_R	0.087	0.061 + 0.013*SL	0.064 + 0.012*SL	0.054 + 0.013*SL
	t_F	0.070	0.050 + 0.010*SL	0.057 + 0.008*SL	0.054 + 0.008*SL
	t_{PLH}	0.378	0.359 + 0.010*SL	0.369 + 0.007*SL	0.383 + 0.006*SL
	t_{PHL}	0.279	0.262 + 0.009*SL	0.273 + 0.006*SL	0.291 + 0.005*SL
C to Y	t_R	0.087	0.062 + 0.013*SL	0.064 + 0.012*SL	0.054 + 0.013*SL
	t_F	0.072	0.053 + 0.009*SL	0.058 + 0.008*SL	0.056 + 0.008*SL
	t_{PLH}	0.399	0.380 + 0.010*SL	0.390 + 0.007*SL	0.404 + 0.006*SL
	t_{PHL}	0.291	0.273 + 0.009*SL	0.284 + 0.006*SL	0.303 + 0.005*SL
D to Y	t_R	0.087	0.062 + 0.012*SL	0.062 + 0.012*SL	0.054 + 0.013*SL
	t_F	0.074	0.055 + 0.009*SL	0.060 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.325	0.306 + 0.010*SL	0.317 + 0.007*SL	0.331 + 0.006*SL
	t_{PHL}	0.273	0.255 + 0.009*SL	0.267 + 0.006*SL	0.286 + 0.005*SL
E to Y	t_R	0.087	0.061 + 0.013*SL	0.064 + 0.012*SL	0.054 + 0.013*SL
	t_F	0.074	0.055 + 0.009*SL	0.061 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.377	0.358 + 0.010*SL	0.369 + 0.007*SL	0.383 + 0.006*SL
	t_{PHL}	0.294	0.276 + 0.009*SL	0.288 + 0.006*SL	0.307 + 0.005*SL
F to Y	t_R	0.087	0.062 + 0.013*SL	0.062 + 0.012*SL	0.054 + 0.013*SL
	t_F	0.074	0.055 + 0.010*SL	0.061 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.397	0.377 + 0.010*SL	0.388 + 0.007*SL	0.402 + 0.006*SL
	t_{PHL}	0.306	0.288 + 0.009*SL	0.300 + 0.006*SL	0.319 + 0.005*SL
G to Y	t_R	0.085	0.060 + 0.012*SL	0.060 + 0.012*SL	0.053 + 0.013*SL
	t_F	0.075	0.056 + 0.010*SL	0.063 + 0.008*SL	0.060 + 0.008*SL
	t_{PLH}	0.302	0.282 + 0.010*SL	0.293 + 0.007*SL	0.306 + 0.006*SL
	t_{PHL}	0.256	0.238 + 0.009*SL	0.250 + 0.006*SL	0.270 + 0.005*SL
H to Y	t_R	0.085	0.059 + 0.013*SL	0.061 + 0.012*SL	0.052 + 0.013*SL
	t_F	0.075	0.056 + 0.010*SL	0.062 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.320	0.301 + 0.010*SL	0.311 + 0.007*SL	0.325 + 0.006*SL
	t_{PHL}	0.272	0.254 + 0.009*SL	0.266 + 0.006*SL	0.286 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

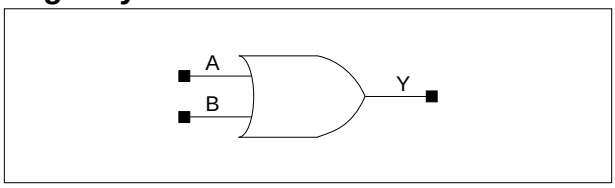
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NR8D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.092	0.078 + 0.007*SL	0.082 + 0.006*SL	0.081 + 0.006*SL
	t_F	0.080	0.069 + 0.006*SL	0.075 + 0.004*SL	0.082 + 0.004*SL
	t_{PLH}	0.384	0.371 + 0.006*SL	0.380 + 0.004*SL	0.408 + 0.003*SL
	t_{PHL}	0.305	0.293 + 0.006*SL	0.303 + 0.004*SL	0.335 + 0.003*SL
B to Y	t_R	0.091	0.076 + 0.008*SL	0.082 + 0.006*SL	0.080 + 0.006*SL
	t_F	0.081	0.069 + 0.006*SL	0.076 + 0.004*SL	0.082 + 0.004*SL
	t_{PLH}	0.432	0.419 + 0.006*SL	0.429 + 0.004*SL	0.457 + 0.003*SL
	t_{PHL}	0.326	0.314 + 0.006*SL	0.324 + 0.004*SL	0.355 + 0.003*SL
C to Y	t_R	0.091	0.075 + 0.008*SL	0.082 + 0.006*SL	0.081 + 0.006*SL
	t_F	0.082	0.069 + 0.006*SL	0.077 + 0.004*SL	0.083 + 0.004*SL
	t_{PLH}	0.453	0.440 + 0.006*SL	0.450 + 0.004*SL	0.478 + 0.003*SL
	t_{PHL}	0.338	0.325 + 0.006*SL	0.336 + 0.004*SL	0.368 + 0.003*SL
D to Y	t_R	0.092	0.077 + 0.007*SL	0.081 + 0.006*SL	0.080 + 0.006*SL
	t_F	0.084	0.071 + 0.006*SL	0.079 + 0.004*SL	0.085 + 0.004*SL
	t_{PLH}	0.376	0.363 + 0.006*SL	0.372 + 0.004*SL	0.400 + 0.003*SL
	t_{PHL}	0.317	0.304 + 0.006*SL	0.315 + 0.004*SL	0.347 + 0.003*SL
E to Y	t_R	0.091	0.076 + 0.008*SL	0.082 + 0.006*SL	0.081 + 0.006*SL
	t_F	0.084	0.072 + 0.006*SL	0.079 + 0.004*SL	0.085 + 0.004*SL
	t_{PLH}	0.428	0.415 + 0.006*SL	0.424 + 0.004*SL	0.453 + 0.003*SL
	t_{PHL}	0.338	0.326 + 0.006*SL	0.336 + 0.004*SL	0.368 + 0.003*SL
F to Y	t_R	0.091	0.075 + 0.008*SL	0.081 + 0.006*SL	0.081 + 0.006*SL
	t_F	0.083	0.071 + 0.006*SL	0.078 + 0.004*SL	0.085 + 0.004*SL
	t_{PLH}	0.447	0.434 + 0.006*SL	0.443 + 0.004*SL	0.472 + 0.003*SL
	t_{PHL}	0.351	0.338 + 0.006*SL	0.348 + 0.004*SL	0.381 + 0.003*SL
G to Y	t_R	0.091	0.076 + 0.007*SL	0.080 + 0.006*SL	0.079 + 0.006*SL
	t_F	0.084	0.073 + 0.006*SL	0.079 + 0.004*SL	0.086 + 0.004*SL
	t_{PLH}	0.349	0.336 + 0.006*SL	0.345 + 0.004*SL	0.373 + 0.003*SL
	t_{PHL}	0.299	0.287 + 0.006*SL	0.297 + 0.004*SL	0.330 + 0.003*SL
H to Y	t_R	0.088	0.073 + 0.008*SL	0.079 + 0.006*SL	0.080 + 0.006*SL
	t_F	0.084	0.073 + 0.006*SL	0.079 + 0.004*SL	0.086 + 0.004*SL
	t_{PLH}	0.368	0.355 + 0.006*SL	0.365 + 0.004*SL	0.393 + 0.003*SL
	t_{PHL}	0.315	0.302 + 0.006*SL	0.312 + 0.004*SL	0.346 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Cell Data

Input Load (SL)								Gate Count			
OR2_LP		*OR2D2_LP*		*OR2D4_LP*		*OR2D8_LP*		*OR2_LP*	*OR2D2_LP*	*OR2D4_LP*	*OR2D8_LP*
A	B	A	B	A	B	A	B				
0.7	0.8	1.1	1.1	1.0	1.1	2.0	2.1	1.33	1.67	2.33	4.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.091	0.041 + 0.025*SL	0.037 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.090	0.055 + 0.018*SL	0.059 + 0.017*SL	0.048 + 0.017*SL
	t_{PLH}	0.145	0.119 + 0.013*SL	0.121 + 0.012*SL	0.123 + 0.012*SL
	t_{PHL}	0.208	0.180 + 0.014*SL	0.194 + 0.010*SL	0.209 + 0.010*SL
B to Y	t_R	0.099	0.054 + 0.022*SL	0.038 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.089	0.055 + 0.017*SL	0.056 + 0.017*SL	0.048 + 0.017*SL
	t_{PLH}	0.161	0.134 + 0.013*SL	0.137 + 0.013*SL	0.139 + 0.012*SL
	t_{PHL}	0.231	0.203 + 0.014*SL	0.217 + 0.010*SL	0.232 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OR2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.065	0.041 + 0.012*SL	0.037 + 0.013*SL	0.028 + 0.013*SL
	t_F	0.072	0.052 + 0.010*SL	0.059 + 0.008*SL	0.058 + 0.008*SL
	t_{PLH}	0.130	0.116 + 0.007*SL	0.119 + 0.006*SL	0.121 + 0.006*SL
	t_{PHL}	0.206	0.187 + 0.009*SL	0.199 + 0.006*SL	0.219 + 0.005*SL
B to Y	t_R	0.068	0.048 + 0.010*SL	0.037 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.071	0.051 + 0.010*SL	0.058 + 0.008*SL	0.059 + 0.008*SL
	t_{PLH}	0.144	0.129 + 0.007*SL	0.133 + 0.006*SL	0.136 + 0.006*SL
	t_{PHL}	0.227	0.210 + 0.009*SL	0.221 + 0.006*SL	0.240 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR2D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.054 + 0.006*SL	0.054 + 0.006*SL	0.041 + 0.007*SL
	t_F	0.085	0.072 + 0.007*SL	0.081 + 0.004*SL	0.089 + 0.004*SL
	t_{PLH}	0.166	0.156 + 0.005*SL	0.162 + 0.003*SL	0.171 + 0.003*SL
	t_{PHL}	0.261	0.248 + 0.006*SL	0.258 + 0.004*SL	0.292 + 0.003*SL
B to Y	t_R	0.065	0.051 + 0.007*SL	0.056 + 0.006*SL	0.042 + 0.007*SL
	t_F	0.085	0.072 + 0.007*SL	0.081 + 0.004*SL	0.089 + 0.004*SL
	t_{PLH}	0.180	0.170 + 0.005*SL	0.176 + 0.003*SL	0.186 + 0.003*SL
	t_{PHL}	0.283	0.270 + 0.006*SL	0.280 + 0.004*SL	0.314 + 0.003*SL

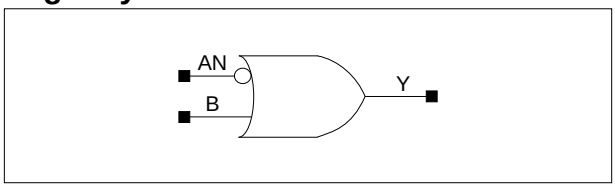
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

OR2D8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.058	0.050 + 0.004*SL	0.054 + 0.003*SL	0.040 + 0.003*SL
	t_F	0.076	0.069 + 0.004*SL	0.075 + 0.002*SL	0.087 + 0.002*SL
	t_{PLH}	0.158	0.152 + 0.003*SL	0.156 + 0.002*SL	0.168 + 0.002*SL
	t_{PHL}	0.249	0.243 + 0.003*SL	0.248 + 0.002*SL	0.285 + 0.001*SL
B to Y	t_R	0.060	0.054 + 0.003*SL	0.053 + 0.003*SL	0.042 + 0.003*SL
	t_F	0.076	0.069 + 0.004*SL	0.075 + 0.002*SL	0.087 + 0.002*SL
	t_{PLH}	0.173	0.167 + 0.003*SL	0.171 + 0.002*SL	0.184 + 0.002*SL
	t_{PHL}	0.272	0.265 + 0.003*SL	0.271 + 0.002*SL	0.307 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

Logic Symbol



Truth Table

AN	B	Y
0	0	1
0	1	1
1	0	0
1	1	1

Cell Data

Input Load (SL)								Gate Count			
OR2B_LP		*OR2BD2_LP*		*OR2BD4_LP*		*OR2BD8_LP*		*OR2B_LP*	*OR2BD2_LP*	*OR2BD4_LP*	*OR2BD8_LP*
AN	B	AN	B	AN	B	AN	B				
0.5	0.8	0.6	1.1	0.6	1.1	0.8	2.3	2.00	2.00	2.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR2B_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.090	0.040 + 0.025*SL	0.035 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.089	0.055 + 0.017*SL	0.057 + 0.016*SL	0.048 + 0.017*SL
	t_{PLH}	0.231	0.204 + 0.013*SL	0.207 + 0.012*SL	0.208 + 0.012*SL
	t_{PHL}	0.244	0.217 + 0.014*SL	0.231 + 0.010*SL	0.247 + 0.009*SL
B to Y	t_R	0.099	0.054 + 0.022*SL	0.038 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.088	0.055 + 0.017*SL	0.056 + 0.016*SL	0.048 + 0.017*SL
	t_{PLH}	0.161	0.134 + 0.013*SL	0.137 + 0.013*SL	0.139 + 0.012*SL
	t_{PHL}	0.230	0.202 + 0.014*SL	0.217 + 0.010*SL	0.232 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OR2BD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.063	0.040 + 0.012*SL	0.035 + 0.013*SL	0.028 + 0.013*SL
	t_F	0.073	0.052 + 0.010*SL	0.059 + 0.008*SL	0.059 + 0.008*SL
	t_{PLH}	0.227	0.212 + 0.007*SL	0.216 + 0.006*SL	0.219 + 0.006*SL
	t_{PHL}	0.248	0.230 + 0.009*SL	0.242 + 0.006*SL	0.262 + 0.005*SL
B to Y	t_R	0.063	0.038 + 0.012*SL	0.036 + 0.013*SL	0.028 + 0.013*SL
	t_F	0.073	0.053 + 0.010*SL	0.060 + 0.008*SL	0.059 + 0.008*SL
	t_{PLH}	0.139	0.125 + 0.007*SL	0.129 + 0.006*SL	0.131 + 0.006*SL
	t_{PHL}	0.230	0.212 + 0.009*SL	0.224 + 0.006*SL	0.244 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR2BD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.060	0.047 + 0.006*SL	0.048 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.087	0.073 + 0.007*SL	0.082 + 0.004*SL	0.090 + 0.004*SL
	t_{PLH}	0.249	0.240 + 0.005*SL	0.245 + 0.003*SL	0.252 + 0.003*SL
	t_{PHL}	0.307	0.294 + 0.006*SL	0.304 + 0.004*SL	0.339 + 0.003*SL
B to Y	t_R	0.062	0.049 + 0.006*SL	0.050 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.086	0.073 + 0.007*SL	0.082 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.159	0.149 + 0.005*SL	0.154 + 0.003*SL	0.162 + 0.003*SL
	t_{PHL}	0.289	0.276 + 0.006*SL	0.286 + 0.004*SL	0.321 + 0.003*SL

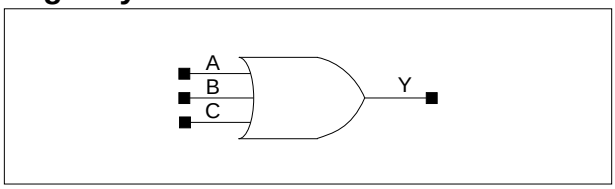
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

OR2BD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
AN to Y	t_R	0.056	0.050 + 0.003*SL	0.049 + 0.003*SL	0.037 + 0.003*SL
	t_F	0.078	0.071 + 0.004*SL	0.076 + 0.002*SL	0.088 + 0.002*SL
	t_{PLH}	0.253	0.248 + 0.003*SL	0.251 + 0.002*SL	0.261 + 0.002*SL
	t_{PHL}	0.316	0.309 + 0.003*SL	0.314 + 0.002*SL	0.352 + 0.001*SL
B to Y	t_R	0.058	0.055 + 0.001*SL	0.049 + 0.003*SL	0.036 + 0.003*SL
	t_F	0.078	0.071 + 0.004*SL	0.076 + 0.002*SL	0.089 + 0.002*SL
	t_{PLH}	0.150	0.145 + 0.003*SL	0.149 + 0.002*SL	0.158 + 0.002*SL
	t_{PHL}	0.278	0.271 + 0.003*SL	0.277 + 0.002*SL	0.314 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
1	x	x	1
x	1	x	1
x	x	1	1

Cell Data

Input Load (SL)									Gate Count		
OR3_LP			*OR3D2_LP*			*OR3D4_LP*			*OR3_LP*	*OR3D2_LP*	*OR3D4_LP*
A	B	C	A	B	C	A	B	C			
0.7	0.7	0.7	1.1	1.1	1.1	1.0	1.0	1.0	1.67	2.33	2.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.098	0.054 + 0.022*SL	0.038 + 0.026*SL	0.032 + 0.026*SL
	t_F	0.111	0.072 + 0.020*SL	0.083 + 0.017*SL	0.083 + 0.017*SL
	t_{PLH}	0.156	0.130 + 0.013*SL	0.133 + 0.012*SL	0.135 + 0.012*SL
	t_{PHL}	0.258	0.224 + 0.017*SL	0.244 + 0.012*SL	0.277 + 0.010*SL
B to Y	t_R	0.094	0.045 + 0.025*SL	0.040 + 0.026*SL	0.033 + 0.026*SL
	t_F	0.111	0.071 + 0.020*SL	0.084 + 0.017*SL	0.083 + 0.017*SL
	t_{PLH}	0.174	0.147 + 0.013*SL	0.151 + 0.012*SL	0.153 + 0.012*SL
	t_{PHL}	0.307	0.274 + 0.017*SL	0.294 + 0.012*SL	0.327 + 0.010*SL
C to Y	t_R	0.100	0.052 + 0.024*SL	0.045 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.111	0.072 + 0.020*SL	0.084 + 0.017*SL	0.083 + 0.017*SL
	t_{PLH}	0.182	0.154 + 0.014*SL	0.159 + 0.013*SL	0.163 + 0.012*SL
	t_{PHL}	0.329	0.295 + 0.017*SL	0.316 + 0.012*SL	0.348 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.043 + 0.012*SL	0.040 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.096	0.073 + 0.012*SL	0.084 + 0.009*SL	0.096 + 0.008*SL
	t_{PLH}	0.141	0.126 + 0.007*SL	0.130 + 0.006*SL	0.133 + 0.006*SL
	t_{PHL}	0.262	0.240 + 0.011*SL	0.254 + 0.007*SL	0.285 + 0.006*SL
B to Y	t_R	0.069	0.045 + 0.012*SL	0.041 + 0.013*SL	0.034 + 0.013*SL
	t_F	0.096	0.074 + 0.011*SL	0.082 + 0.009*SL	0.094 + 0.008*SL
	t_{PLH}	0.156	0.141 + 0.008*SL	0.145 + 0.006*SL	0.149 + 0.006*SL
	t_{PHL}	0.315	0.293 + 0.011*SL	0.307 + 0.007*SL	0.338 + 0.006*SL
C to Y	t_R	0.072	0.048 + 0.012*SL	0.045 + 0.013*SL	0.037 + 0.013*SL
	t_F	0.096	0.072 + 0.012*SL	0.084 + 0.009*SL	0.095 + 0.008*SL
	t_{PLH}	0.163	0.147 + 0.008*SL	0.153 + 0.007*SL	0.157 + 0.006*SL
	t_{PHL}	0.340	0.318 + 0.011*SL	0.332 + 0.007*SL	0.364 + 0.006*SL

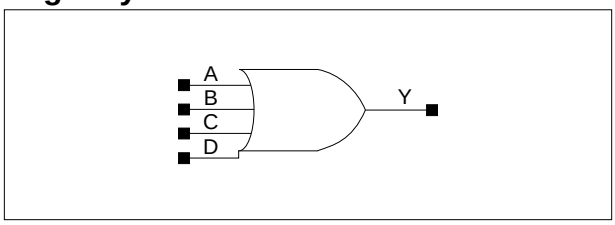
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OR3D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.071	0.057 + 0.007*SL	0.059 + 0.006*SL	0.047 + 0.006*SL
	t_F	0.114	0.101 + 0.007*SL	0.108 + 0.005*SL	0.133 + 0.004*SL
	t_{PLH}	0.184	0.173 + 0.005*SL	0.180 + 0.004*SL	0.192 + 0.003*SL
	t_{PHL}	0.341	0.327 + 0.007*SL	0.337 + 0.005*SL	0.384 + 0.003*SL
B to Y	t_R	0.072	0.058 + 0.007*SL	0.062 + 0.006*SL	0.049 + 0.006*SL
	t_F	0.115	0.101 + 0.007*SL	0.109 + 0.005*SL	0.132 + 0.004*SL
	t_{PLH}	0.202	0.191 + 0.005*SL	0.198 + 0.004*SL	0.212 + 0.003*SL
	t_{PHL}	0.392	0.378 + 0.007*SL	0.389 + 0.005*SL	0.435 + 0.003*SL
C to Y	t_R	0.077	0.065 + 0.006*SL	0.064 + 0.006*SL	0.054 + 0.006*SL
	t_F	0.114	0.099 + 0.007*SL	0.109 + 0.005*SL	0.132 + 0.004*SL
	t_{PLH}	0.213	0.202 + 0.006*SL	0.209 + 0.004*SL	0.225 + 0.003*SL
	t_{PHL}	0.415	0.401 + 0.007*SL	0.411 + 0.005*SL	0.458 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Cell Data

Input Load (SL)											
OR4_LP				*OR4D2_LP*				*OR4D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
0.8	0.8	0.7	0.8	1.0	1.1	1.0	1.0	0.8	0.8	0.8	0.8

Gate Count		
OR4_LP	*OR4D2_LP*	*OR4D4_LP*
2.67	3.00	4.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.053 + 0.025*SL	0.047 + 0.026*SL	0.042 + 0.027*SL
	t_F	0.125	0.074 + 0.026*SL	0.074 + 0.026*SL	0.063 + 0.026*SL
	t_{PLH}	0.153	0.127 + 0.013*SL	0.129 + 0.012*SL	0.131 + 0.012*SL
	t_{PHL}	0.233	0.198 + 0.017*SL	0.209 + 0.014*SL	0.219 + 0.014*SL
B to Y	t_R	0.104	0.054 + 0.025*SL	0.050 + 0.026*SL	0.043 + 0.027*SL
	t_F	0.125	0.075 + 0.025*SL	0.073 + 0.026*SL	0.062 + 0.026*SL
	t_{PLH}	0.168	0.141 + 0.013*SL	0.144 + 0.013*SL	0.146 + 0.012*SL
	t_{PHL}	0.254	0.220 + 0.017*SL	0.231 + 0.014*SL	0.241 + 0.014*SL
C to Y	t_R	0.111	0.060 + 0.025*SL	0.056 + 0.026*SL	0.052 + 0.027*SL
	t_F	0.117	0.066 + 0.026*SL	0.065 + 0.026*SL	0.058 + 0.026*SL
	t_{PLH}	0.160	0.134 + 0.013*SL	0.136 + 0.012*SL	0.138 + 0.012*SL
	t_{PHL}	0.232	0.199 + 0.016*SL	0.208 + 0.014*SL	0.216 + 0.014*SL
D to Y	t_R	0.112	0.061 + 0.026*SL	0.059 + 0.026*SL	0.053 + 0.027*SL
	t_F	0.117	0.066 + 0.026*SL	0.065 + 0.026*SL	0.058 + 0.026*SL
	t_{PLH}	0.176	0.150 + 0.013*SL	0.152 + 0.013*SL	0.154 + 0.012*SL
	t_{PHL}	0.255	0.222 + 0.017*SL	0.230 + 0.014*SL	0.239 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR4D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.081	0.057 + 0.012*SL	0.055 + 0.013*SL	0.046 + 0.013*SL
	t_F	0.102	0.077 + 0.013*SL	0.076 + 0.013*SL	0.074 + 0.013*SL
	t_{PLH}	0.161	0.146 + 0.007*SL	0.150 + 0.006*SL	0.152 + 0.006*SL
	t_{PHL}	0.227	0.207 + 0.010*SL	0.215 + 0.008*SL	0.229 + 0.007*SL
B to Y	t_R	0.085	0.061 + 0.012*SL	0.057 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.102	0.077 + 0.013*SL	0.076 + 0.013*SL	0.074 + 0.013*SL
	t_{PLH}	0.178	0.163 + 0.007*SL	0.167 + 0.006*SL	0.170 + 0.006*SL
	t_{PHL}	0.249	0.229 + 0.010*SL	0.237 + 0.008*SL	0.251 + 0.007*SL
C to Y	t_R	0.090	0.064 + 0.013*SL	0.064 + 0.013*SL	0.056 + 0.013*SL
	t_F	0.093	0.065 + 0.014*SL	0.069 + 0.013*SL	0.065 + 0.013*SL
	t_{PLH}	0.171	0.157 + 0.007*SL	0.159 + 0.006*SL	0.162 + 0.006*SL
	t_{PHL}	0.230	0.211 + 0.009*SL	0.217 + 0.008*SL	0.229 + 0.007*SL
D to Y	t_R	0.092	0.067 + 0.013*SL	0.067 + 0.013*SL	0.058 + 0.013*SL
	t_F	0.093	0.066 + 0.013*SL	0.068 + 0.013*SL	0.066 + 0.013*SL
	t_{PLH}	0.188	0.174 + 0.007*SL	0.177 + 0.006*SL	0.180 + 0.006*SL
	t_{PHL}	0.250	0.232 + 0.009*SL	0.238 + 0.008*SL	0.249 + 0.007*SL

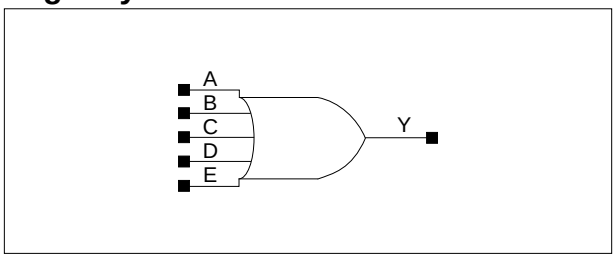
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OR4D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.062	0.051 + 0.006*SL	0.049 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.056	0.047 + 0.004*SL	0.049 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.296	0.286 + 0.005*SL	0.292 + 0.003*SL	0.300 + 0.003*SL
	t_{PHL}	0.355	0.345 + 0.005*SL	0.352 + 0.003*SL	0.370 + 0.002*SL
B to Y	t_R	0.062	0.048 + 0.007*SL	0.051 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.057	0.046 + 0.005*SL	0.050 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.313	0.304 + 0.005*SL	0.309 + 0.003*SL	0.318 + 0.003*SL
	t_{PHL}	0.377	0.367 + 0.005*SL	0.374 + 0.003*SL	0.392 + 0.002*SL
C to Y	t_R	0.062	0.051 + 0.006*SL	0.050 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.056	0.047 + 0.005*SL	0.050 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.305	0.296 + 0.005*SL	0.301 + 0.003*SL	0.310 + 0.003*SL
	t_{PHL}	0.351	0.342 + 0.005*SL	0.349 + 0.003*SL	0.366 + 0.002*SL
D to Y	t_R	0.062	0.048 + 0.007*SL	0.052 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.056	0.046 + 0.005*SL	0.049 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.323	0.313 + 0.005*SL	0.319 + 0.003*SL	0.327 + 0.003*SL
	t_{PHL}	0.372	0.363 + 0.005*SL	0.370 + 0.003*SL	0.387 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Cell Data

Input Load (SL)														
OR5_LP					*OR5D2_LP*					*OR5D4_LP*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.9	0.9	0.9	0.7	0.8	1.0	1.1	1.1	1.0	1.0	0.9	0.9	1.0	0.8	0.8
Gate Count														
OR5_LP					*OR5D2_LP*					*OR5D4_LP*				
3.00					3.33					4.67				

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR5_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.106	0.056 + 0.025*SL	0.050 + 0.026*SL	0.045 + 0.027*SL
	t_F	0.144	0.090 + 0.027*SL	0.097 + 0.025*SL	0.090 + 0.026*SL
	t_{PLH}	0.155	0.129 + 0.013*SL	0.131 + 0.012*SL	0.133 + 0.012*SL
	t_{PHL}	0.271	0.232 + 0.019*SL	0.249 + 0.015*SL	0.272 + 0.014*SL
B to Y	t_R	0.106	0.055 + 0.026*SL	0.052 + 0.026*SL	0.047 + 0.027*SL
	t_F	0.146	0.093 + 0.027*SL	0.098 + 0.025*SL	0.090 + 0.026*SL
	t_{PLH}	0.172	0.146 + 0.013*SL	0.148 + 0.013*SL	0.150 + 0.012*SL
	t_{PHL}	0.323	0.284 + 0.019*SL	0.301 + 0.015*SL	0.324 + 0.014*SL
C to Y	t_R	0.110	0.059 + 0.025*SL	0.055 + 0.026*SL	0.051 + 0.027*SL
	t_F	0.146	0.092 + 0.027*SL	0.097 + 0.025*SL	0.090 + 0.026*SL
	t_{PLH}	0.180	0.153 + 0.014*SL	0.157 + 0.013*SL	0.161 + 0.012*SL
	t_{PHL}	0.345	0.306 + 0.019*SL	0.323 + 0.015*SL	0.346 + 0.014*SL
D to Y	t_R	0.115	0.065 + 0.025*SL	0.059 + 0.026*SL	0.055 + 0.027*SL
	t_F	0.119	0.068 + 0.026*SL	0.067 + 0.026*SL	0.061 + 0.026*SL
	t_{PLH}	0.162	0.136 + 0.013*SL	0.137 + 0.012*SL	0.139 + 0.012*SL
	t_{PHL}	0.233	0.201 + 0.016*SL	0.209 + 0.014*SL	0.217 + 0.014*SL
E to Y	t_R	0.116	0.065 + 0.025*SL	0.061 + 0.026*SL	0.056 + 0.027*SL
	t_F	0.119	0.068 + 0.026*SL	0.067 + 0.026*SL	0.061 + 0.026*SL
	t_{PLH}	0.177	0.151 + 0.013*SL	0.153 + 0.013*SL	0.155 + 0.012*SL
	t_{PHL}	0.256	0.223 + 0.016*SL	0.231 + 0.014*SL	0.240 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR5D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.083	0.060 + 0.011*SL	0.055 + 0.013*SL	0.048 + 0.013*SL
	t_F	0.125	0.097 + 0.014*SL	0.101 + 0.013*SL	0.107 + 0.013*SL
	t_{PLH}	0.163	0.149 + 0.007*SL	0.152 + 0.006*SL	0.155 + 0.006*SL
	t_{PHL}	0.284	0.261 + 0.012*SL	0.272 + 0.009*SL	0.298 + 0.007*SL
B to Y	t_R	0.085	0.060 + 0.012*SL	0.059 + 0.013*SL	0.050 + 0.013*SL
	t_F	0.127	0.098 + 0.015*SL	0.104 + 0.013*SL	0.107 + 0.013*SL
	t_{PLH}	0.181	0.166 + 0.007*SL	0.170 + 0.006*SL	0.174 + 0.006*SL
	t_{PHL}	0.335	0.312 + 0.012*SL	0.322 + 0.009*SL	0.348 + 0.007*SL
C to Y	t_R	0.089	0.066 + 0.012*SL	0.061 + 0.013*SL	0.054 + 0.013*SL
	t_F	0.127	0.098 + 0.015*SL	0.104 + 0.013*SL	0.107 + 0.013*SL
	t_{PLH}	0.191	0.175 + 0.008*SL	0.180 + 0.007*SL	0.185 + 0.006*SL
	t_{PHL}	0.356	0.333 + 0.012*SL	0.344 + 0.009*SL	0.370 + 0.007*SL
D to Y	t_R	0.090	0.065 + 0.013*SL	0.065 + 0.013*SL	0.057 + 0.013*SL
	t_F	0.095	0.066 + 0.014*SL	0.071 + 0.013*SL	0.068 + 0.013*SL
	t_{PLH}	0.171	0.157 + 0.007*SL	0.160 + 0.006*SL	0.162 + 0.006*SL
	t_{PHL}	0.232	0.213 + 0.009*SL	0.219 + 0.008*SL	0.231 + 0.007*SL
E to Y	t_R	0.094	0.070 + 0.012*SL	0.068 + 0.013*SL	0.059 + 0.013*SL
	t_F	0.095	0.066 + 0.014*SL	0.071 + 0.013*SL	0.068 + 0.013*SL
	t_{PLH}	0.189	0.175 + 0.007*SL	0.178 + 0.006*SL	0.181 + 0.006*SL
	t_{PHL}	0.254	0.235 + 0.009*SL	0.241 + 0.008*SL	0.253 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OR5D4_LP

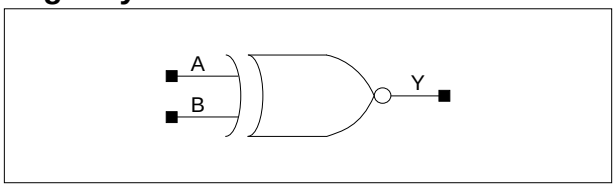
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.062	0.050 + 0.006*SL	0.050 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.056	0.047 + 0.005*SL	0.049 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.298	0.288 + 0.005*SL	0.294 + 0.003*SL	0.302 + 0.003*SL
	t_{PHL}	0.388	0.378 + 0.005*SL	0.385 + 0.003*SL	0.403 + 0.002*SL
B to Y	t_R	0.062	0.048 + 0.007*SL	0.051 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.056	0.046 + 0.005*SL	0.049 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.316	0.307 + 0.005*SL	0.312 + 0.003*SL	0.321 + 0.003*SL
	t_{PHL}	0.438	0.429 + 0.005*SL	0.435 + 0.003*SL	0.453 + 0.002*SL
C to Y	t_R	0.063	0.051 + 0.006*SL	0.049 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.057	0.048 + 0.004*SL	0.049 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.327	0.317 + 0.005*SL	0.323 + 0.003*SL	0.331 + 0.003*SL
	t_{PHL}	0.462	0.452 + 0.005*SL	0.459 + 0.003*SL	0.477 + 0.002*SL
D to Y	t_R	0.062	0.049 + 0.007*SL	0.051 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.056	0.047 + 0.005*SL	0.049 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.306	0.297 + 0.005*SL	0.302 + 0.003*SL	0.311 + 0.003*SL
	t_{PHL}	0.352	0.343 + 0.005*SL	0.350 + 0.003*SL	0.367 + 0.002*SL
E to Y	t_R	0.062	0.049 + 0.007*SL	0.052 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.056	0.047 + 0.005*SL	0.050 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.324	0.314 + 0.005*SL	0.320 + 0.003*SL	0.328 + 0.003*SL
	t_{PHL}	0.374	0.365 + 0.005*SL	0.371 + 0.003*SL	0.389 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

XN2_LP/XN2D2_LP/XN2D4_LP

2-Input Exclusive-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)						Gate Count		
XN2_LP		*XN2D2_LP*		*XN2D4_LP*		*XN2_LP*	*XN2D2_LP*	*XN2D4_LP*
A	B	A	B	A	B			
0.9	1.4	0.9	1.5	0.9	1.5	2.33	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

XN2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.050 + 0.025*SL	0.047 + 0.026*SL	0.036 + 0.026*SL
	t_F	0.109	0.072 + 0.018*SL	0.079 + 0.016*SL	0.069 + 0.017*SL
	t_{PLH}	0.253	0.225 + 0.014*SL	0.231 + 0.013*SL	0.234 + 0.012*SL
	t_{PHL}	0.267	0.235 + 0.016*SL	0.255 + 0.011*SL	0.281 + 0.010*SL
B to Y	t_R	0.100	0.050 + 0.025*SL	0.047 + 0.026*SL	0.036 + 0.026*SL
	t_F	0.104	0.067 + 0.018*SL	0.075 + 0.017*SL	0.068 + 0.017*SL
	t_{PLH}	0.241	0.213 + 0.014*SL	0.219 + 0.013*SL	0.222 + 0.012*SL
	t_{PHL}	0.230	0.198 + 0.016*SL	0.217 + 0.011*SL	0.242 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

XN2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.077	0.052 + 0.013*SL	0.052 + 0.013*SL	0.044 + 0.013*SL
	t_F	0.099	0.076 + 0.011*SL	0.087 + 0.009*SL	0.092 + 0.008*SL
	t_{PLH}	0.265	0.247 + 0.009*SL	0.256 + 0.007*SL	0.264 + 0.006*SL
	t_{PHL}	0.300	0.280 + 0.010*SL	0.293 + 0.006*SL	0.317 + 0.005*SL
B to Y	t_R	0.078	0.054 + 0.012*SL	0.051 + 0.012*SL	0.042 + 0.013*SL
	t_F	0.094	0.072 + 0.011*SL	0.082 + 0.009*SL	0.090 + 0.008*SL
	t_{PLH}	0.259	0.241 + 0.009*SL	0.250 + 0.007*SL	0.258 + 0.006*SL
	t_{PHL}	0.228	0.206 + 0.011*SL	0.222 + 0.007*SL	0.253 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

XN2D4_LP

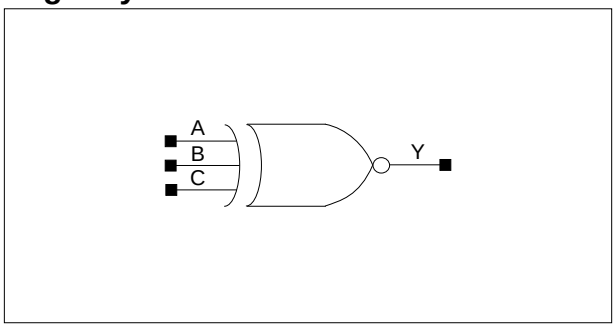
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.080	0.065 + 0.007*SL	0.070 + 0.006*SL	0.061 + 0.006*SL
	t_F	0.117	0.103 + 0.007*SL	0.111 + 0.005*SL	0.135 + 0.004*SL
	t_{PLH}	0.298	0.286 + 0.006*SL	0.295 + 0.004*SL	0.315 + 0.003*SL
	t_{PHL}	0.364	0.351 + 0.007*SL	0.362 + 0.004*SL	0.400 + 0.003*SL
B to Y	t_R	0.081	0.068 + 0.007*SL	0.069 + 0.006*SL	0.061 + 0.006*SL
	t_F	0.116	0.101 + 0.007*SL	0.110 + 0.005*SL	0.132 + 0.004*SL
	t_{PLH}	0.291	0.279 + 0.006*SL	0.287 + 0.004*SL	0.308 + 0.003*SL
	t_{PHL}	0.291	0.278 + 0.007*SL	0.289 + 0.004*SL	0.327 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

XN3_LP/XN3D2_LP/XN3D4_LP

3-Input Exclusive-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Data

Input Load (SL)									Gate Count		
XN3_LP			*XN3D2_LP*			*XN3D4_LP*			*XN3_LP*	*XN3D2_LP*	*XN3D4_LP*
A	B	C	A	B	C	A	B	C			
1.6	0.9	1.5	1.6	0.9	1.5	1.6	0.9	1.5	4.33	4.67	5.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

XN3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.116	0.064 + 0.026*SL	0.065 + 0.026*SL	0.055 + 0.026*SL
	t_F	0.120	0.076 + 0.022*SL	0.091 + 0.018*SL	0.112 + 0.017*SL
	t_{PLH}	0.227	0.195 + 0.016*SL	0.207 + 0.013*SL	0.219 + 0.012*SL
	t_{PHL}	0.238	0.202 + 0.018*SL	0.223 + 0.013*SL	0.266 + 0.010*SL
B to Y	t_R	0.123	0.071 + 0.026*SL	0.072 + 0.025*SL	0.058 + 0.026*SL
	t_F	0.151	0.114 + 0.018*SL	0.122 + 0.016*SL	0.116 + 0.017*SL
	t_{PLH}	0.408	0.380 + 0.014*SL	0.386 + 0.013*SL	0.389 + 0.012*SL
	t_{PHL}	0.454	0.415 + 0.020*SL	0.443 + 0.013*SL	0.486 + 0.010*SL
C to Y	t_R	0.122	0.071 + 0.026*SL	0.072 + 0.025*SL	0.058 + 0.026*SL
	t_F	0.175	0.135 + 0.020*SL	0.148 + 0.017*SL	0.149 + 0.017*SL
	t_{PLH}	0.360	0.328 + 0.016*SL	0.341 + 0.013*SL	0.352 + 0.012*SL
	t_{PHL}	0.423	0.396 + 0.014*SL	0.409 + 0.010*SL	0.423 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

XN3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.088	0.059 + 0.014*SL	0.066 + 0.013*SL	0.062 + 0.013*SL
	t_F	0.121	0.092 + 0.014*SL	0.108 + 0.010*SL	0.136 + 0.009*SL
	t_{PLH}	0.228	0.207 + 0.010*SL	0.219 + 0.008*SL	0.239 + 0.006*SL
	t_{PHL}	0.259	0.231 + 0.014*SL	0.251 + 0.009*SL	0.297 + 0.006*SL
B to Y	t_R	0.093	0.066 + 0.013*SL	0.069 + 0.013*SL	0.069 + 0.013*SL
	t_F	0.142	0.118 + 0.012*SL	0.131 + 0.009*SL	0.143 + 0.008*SL
	t_{PLH}	0.412	0.394 + 0.009*SL	0.403 + 0.007*SL	0.412 + 0.006*SL
	t_{PHL}	0.471	0.443 + 0.014*SL	0.465 + 0.009*SL	0.511 + 0.006*SL
C to Y	t_R	0.093	0.066 + 0.014*SL	0.069 + 0.013*SL	0.069 + 0.013*SL
	t_F	0.168	0.142 + 0.013*SL	0.157 + 0.009*SL	0.177 + 0.008*SL
	t_{PLH}	0.363	0.342 + 0.011*SL	0.354 + 0.008*SL	0.374 + 0.006*SL
	t_{PHL}	0.441	0.422 + 0.010*SL	0.435 + 0.006*SL	0.458 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

XN3D4_LP

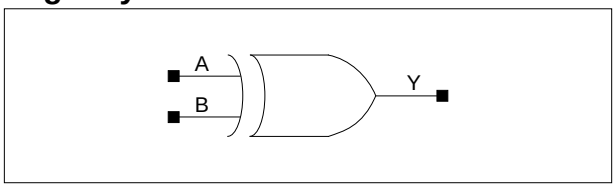
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.093	0.076 + 0.008*SL	0.083 + 0.007*SL	0.089 + 0.006*SL
	t_F	0.174	0.156 + 0.009*SL	0.168 + 0.006*SL	0.211 + 0.004*SL
	t_{PLH}	0.264	0.250 + 0.007*SL	0.260 + 0.004*SL	0.293 + 0.003*SL
	t_{PHL}	0.341	0.321 + 0.010*SL	0.337 + 0.006*SL	0.409 + 0.004*SL
B to Y	t_R	0.094	0.077 + 0.009*SL	0.084 + 0.007*SL	0.094 + 0.006*SL
	t_F	0.166	0.151 + 0.008*SL	0.160 + 0.005*SL	0.193 + 0.004*SL
	t_{PLH}	0.448	0.436 + 0.006*SL	0.444 + 0.004*SL	0.465 + 0.003*SL
	t_{PHL}	0.548	0.530 + 0.009*SL	0.544 + 0.005*SL	0.608 + 0.003*SL
C to Y	t_R	0.094	0.077 + 0.009*SL	0.085 + 0.007*SL	0.094 + 0.006*SL
	t_F	0.200	0.183 + 0.009*SL	0.195 + 0.005*SL	0.233 + 0.004*SL
	t_{PLH}	0.403	0.389 + 0.007*SL	0.399 + 0.004*SL	0.433 + 0.003*SL
	t_{PHL}	0.506	0.493 + 0.007*SL	0.503 + 0.004*SL	0.542 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

XO2_LP/XO2D2_LP/XO2D4_LP

2-Input Exclusive-OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)						Gate Count		
XO2_LP		*XO2D2_LP*		*XO2D4_LP*		*XO2_LP*	*XO2D2_LP*	*XO2D4_LP*
A	B	A	B	A	B			
0.8	1.6	0.9	1.6	1.0	1.7	2.33	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

XO2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.102	0.054 + 0.024*SL	0.047 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.102	0.066 + 0.018*SL	0.072 + 0.017*SL	0.063 + 0.017*SL
	t_{PLH}	0.262	0.234 + 0.014*SL	0.241 + 0.013*SL	0.243 + 0.012*SL
	t_{PHL}	0.301	0.271 + 0.015*SL	0.288 + 0.011*SL	0.307 + 0.010*SL
B to Y	t_R	0.102	0.053 + 0.025*SL	0.049 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.096	0.060 + 0.018*SL	0.065 + 0.017*SL	0.055 + 0.017*SL
	t_{PLH}	0.217	0.188 + 0.015*SL	0.196 + 0.013*SL	0.199 + 0.012*SL
	t_{PHL}	0.254	0.225 + 0.015*SL	0.241 + 0.011*SL	0.261 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

XO2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.087	0.060 + 0.013*SL	0.064 + 0.012*SL	0.054 + 0.013*SL
	t_F	0.092	0.070 + 0.011*SL	0.080 + 0.009*SL	0.085 + 0.008*SL
	t_{PLH}	0.260	0.243 + 0.009*SL	0.251 + 0.007*SL	0.259 + 0.006*SL
	t_{PHL}	0.324	0.305 + 0.010*SL	0.318 + 0.007*SL	0.343 + 0.005*SL
B to Y	t_R	0.087	0.061 + 0.013*SL	0.063 + 0.012*SL	0.053 + 0.013*SL
	t_F	0.086	0.065 + 0.011*SL	0.072 + 0.009*SL	0.081 + 0.008*SL
	t_{PLH}	0.229	0.210 + 0.010*SL	0.221 + 0.007*SL	0.235 + 0.006*SL
	t_{PHL}	0.275	0.256 + 0.010*SL	0.269 + 0.007*SL	0.294 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

XO2D4_LP

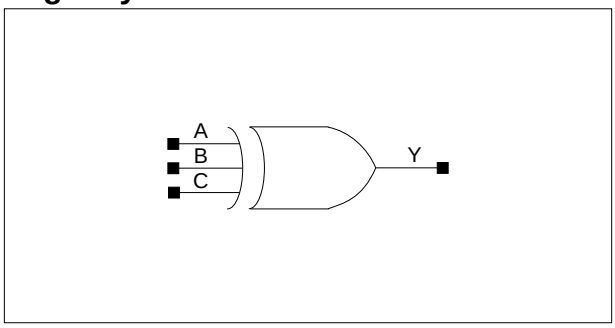
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.089	0.074 + 0.007*SL	0.079 + 0.006*SL	0.076 + 0.006*SL
	t_F	0.101	0.087 + 0.007*SL	0.096 + 0.005*SL	0.115 + 0.004*SL
	t_{PLH}	0.296	0.285 + 0.006*SL	0.293 + 0.004*SL	0.313 + 0.003*SL
	t_{PHL}	0.379	0.365 + 0.007*SL	0.376 + 0.004*SL	0.415 + 0.003*SL
B to Y	t_R	0.088	0.072 + 0.008*SL	0.078 + 0.006*SL	0.076 + 0.006*SL
	t_F	0.100	0.087 + 0.006*SL	0.093 + 0.005*SL	0.113 + 0.004*SL
	t_{PLH}	0.252	0.239 + 0.006*SL	0.248 + 0.004*SL	0.276 + 0.003*SL
	t_{PHL}	0.328	0.315 + 0.007*SL	0.326 + 0.004*SL	0.365 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

XO3_LP/XO3D2_LP/XO3D4_LP

3-Input Exclusive-OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Data

Input Load (SL)									Gate Count		
XO3_LP			*XO3D2_LP*			*XO3D4_LP*			*XO3_LP*	*XO3D2_LP*	*XO3D4_LP*
A	B	C	A	B	C	A	B	C			
1.6	0.8	1.7	1.8	0.8	1.8	1.8	0.8	1.8	4.33	4.33	5.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

XO3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.115	0.061 + 0.027*SL	0.066 + 0.026*SL	0.055 + 0.026*SL
	t_F	0.121	0.077 + 0.022*SL	0.093 + 0.018*SL	0.109 + 0.017*SL
	t_{PLH}	0.246	0.218 + 0.014*SL	0.224 + 0.013*SL	0.227 + 0.012*SL
	t_{PHL}	0.233	0.195 + 0.019*SL	0.219 + 0.013*SL	0.265 + 0.010*SL
B to Y	t_R	0.123	0.071 + 0.026*SL	0.075 + 0.025*SL	0.060 + 0.026*SL
	t_F	0.152	0.111 + 0.020*SL	0.125 + 0.017*SL	0.131 + 0.017*SL
	t_{PLH}	0.441	0.412 + 0.014*SL	0.419 + 0.013*SL	0.423 + 0.012*SL
	t_{PHL}	0.497	0.456 + 0.020*SL	0.485 + 0.013*SL	0.535 + 0.010*SL
C to Y	t_R	0.124	0.071 + 0.026*SL	0.075 + 0.025*SL	0.060 + 0.026*SL
	t_F	0.151	0.112 + 0.020*SL	0.122 + 0.017*SL	0.130 + 0.017*SL
	t_{PLH}	0.358	0.324 + 0.017*SL	0.339 + 0.013*SL	0.351 + 0.012*SL
	t_{PHL}	0.437	0.407 + 0.015*SL	0.424 + 0.011*SL	0.445 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

XO3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.095	0.063 + 0.016*SL	0.075 + 0.013*SL	0.077 + 0.013*SL
	t_F	0.120	0.093 + 0.014*SL	0.107 + 0.010*SL	0.132 + 0.009*SL
	t_{PLH}	0.234	0.216 + 0.009*SL	0.224 + 0.007*SL	0.232 + 0.006*SL
	t_{PHL}	0.259	0.232 + 0.014*SL	0.251 + 0.009*SL	0.294 + 0.006*SL
B to Y	t_R	0.102	0.072 + 0.015*SL	0.081 + 0.013*SL	0.083 + 0.013*SL
	t_F	0.137	0.112 + 0.012*SL	0.124 + 0.009*SL	0.140 + 0.008*SL
	t_{PLH}	0.428	0.410 + 0.009*SL	0.418 + 0.007*SL	0.427 + 0.006*SL
	t_{PHL}	0.505	0.478 + 0.013*SL	0.497 + 0.009*SL	0.540 + 0.006*SL
C to Y	t_R	0.102	0.072 + 0.015*SL	0.082 + 0.013*SL	0.083 + 0.013*SL
	t_F	0.083	0.061 + 0.011*SL	0.072 + 0.008*SL	0.073 + 0.008*SL
	t_{PLH}	0.362	0.340 + 0.011*SL	0.353 + 0.008*SL	0.374 + 0.006*SL
	t_{PHL}	0.439	0.419 + 0.010*SL	0.433 + 0.007*SL	0.457 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

XO3D4_LP

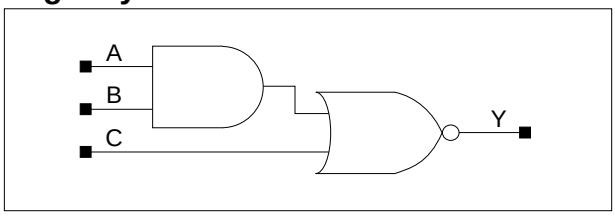
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.105	0.088 + 0.009*SL	0.096 + 0.007*SL	0.111 + 0.006*SL
	t_F	0.158	0.141 + 0.008*SL	0.153 + 0.005*SL	0.186 + 0.004*SL
	t_{PLH}	0.268	0.257 + 0.006*SL	0.265 + 0.004*SL	0.286 + 0.003*SL
	t_{PHL}	0.333	0.315 + 0.009*SL	0.329 + 0.006*SL	0.391 + 0.003*SL
B to Y	t_R	0.107	0.090 + 0.009*SL	0.097 + 0.007*SL	0.114 + 0.006*SL
	t_F	0.154	0.139 + 0.007*SL	0.148 + 0.005*SL	0.178 + 0.004*SL
	t_{PLH}	0.464	0.452 + 0.006*SL	0.461 + 0.004*SL	0.482 + 0.003*SL
	t_{PHL}	0.576	0.559 + 0.008*SL	0.572 + 0.005*SL	0.629 + 0.003*SL
C to Y	t_R	0.108	0.090 + 0.009*SL	0.099 + 0.007*SL	0.114 + 0.006*SL
	t_F	0.097	0.084 + 0.007*SL	0.092 + 0.005*SL	0.105 + 0.004*SL
	t_{PLH}	0.412	0.398 + 0.007*SL	0.408 + 0.005*SL	0.444 + 0.003*SL
	t_{PHL}	0.501	0.487 + 0.007*SL	0.498 + 0.004*SL	0.537 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

AO21_LP/AO21D2_LP/AO21D4_LP

2-AND into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	0	1
x	0	0	1
Other States			0

Cell Data

Input Load (SL)								
AO21_LP			*AO21D2_LP*			*AO21D4_LP*		
A	B	C	A	B	C	A	B	C
1.1	1.1	1.1	2.3	2.2	2.1	0.9	0.9	0.9
Gate Count								
AO21_LP			*AO21D2_LP*			*AO21D4_LP*		
1.33			2.33			3.00		

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO21_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.225	0.125 + 0.050*SL	0.112 + 0.053*SL	0.105 + 0.054*SL
	t_F	0.123	0.078 + 0.023*SL	0.066 + 0.026*SL	0.046 + 0.027*SL
	t_{PLH}	0.149	0.098 + 0.026*SL	0.097 + 0.026*SL	0.099 + 0.026*SL
	t_{PHL}	0.100	0.068 + 0.016*SL	0.076 + 0.014*SL	0.077 + 0.014*SL
B to Y	t_R	0.242	0.141 + 0.051*SL	0.129 + 0.054*SL	0.124 + 0.054*SL
	t_F	0.115	0.066 + 0.024*SL	0.059 + 0.026*SL	0.046 + 0.027*SL
	t_{PLH}	0.166	0.113 + 0.026*SL	0.113 + 0.026*SL	0.115 + 0.026*SL
	t_{PHL}	0.097	0.065 + 0.016*SL	0.072 + 0.014*SL	0.074 + 0.014*SL
C to Y	t_R	0.235	0.129 + 0.053*SL	0.126 + 0.054*SL	0.124 + 0.054*SL
	t_F	0.110	0.081 + 0.015*SL	0.077 + 0.016*SL	0.059 + 0.017*SL
	t_{PLH}	0.205	0.152 + 0.026*SL	0.153 + 0.026*SL	0.155 + 0.026*SL
	t_{PHL}	0.106	0.085 + 0.011*SL	0.090 + 0.009*SL	0.093 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO21D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.179	0.130 + 0.025*SL	0.125 + 0.026*SL	0.109 + 0.027*SL
	t_F	0.101	0.078 + 0.012*SL	0.075 + 0.012*SL	0.060 + 0.013*SL
	t_{PLH}	0.126	0.100 + 0.013*SL	0.099 + 0.013*SL	0.100 + 0.013*SL
	t_{PHL}	0.085	0.067 + 0.009*SL	0.075 + 0.007*SL	0.078 + 0.007*SL
B to Y	t_R	0.196	0.146 + 0.025*SL	0.141 + 0.026*SL	0.127 + 0.027*SL
	t_F	0.093	0.069 + 0.012*SL	0.067 + 0.013*SL	0.056 + 0.013*SL
	t_{PLH}	0.142	0.116 + 0.013*SL	0.116 + 0.013*SL	0.117 + 0.013*SL
	t_{PHL}	0.082	0.065 + 0.009*SL	0.071 + 0.007*SL	0.074 + 0.007*SL
C to Y	t_R	0.188	0.135 + 0.026*SL	0.133 + 0.027*SL	0.129 + 0.027*SL
	t_F	0.099	0.084 + 0.008*SL	0.084 + 0.008*SL	0.073 + 0.008*SL
	t_{PLH}	0.181	0.154 + 0.013*SL	0.155 + 0.013*SL	0.156 + 0.013*SL
	t_{PHL}	0.098	0.086 + 0.006*SL	0.090 + 0.005*SL	0.093 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AO21D4_LP

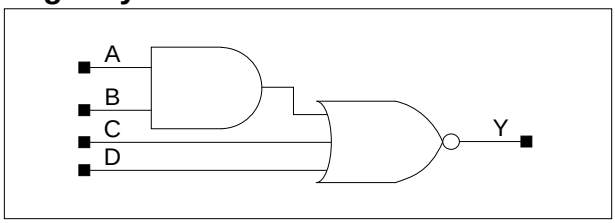
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.062	0.049 + 0.006*SL	0.050 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.055	0.046 + 0.005*SL	0.049 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.287	0.277 + 0.005*SL	0.283 + 0.003*SL	0.290 + 0.003*SL
	t_{PHL}	0.239	0.230 + 0.005*SL	0.236 + 0.003*SL	0.253 + 0.002*SL
B to Y	t_R	0.062	0.050 + 0.006*SL	0.051 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.055	0.045 + 0.005*SL	0.048 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.307	0.297 + 0.005*SL	0.303 + 0.003*SL	0.310 + 0.003*SL
	t_{PHL}	0.235	0.226 + 0.005*SL	0.233 + 0.003*SL	0.250 + 0.002*SL
C to Y	t_R	0.061	0.048 + 0.006*SL	0.049 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.055	0.044 + 0.006*SL	0.050 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.347	0.337 + 0.005*SL	0.343 + 0.003*SL	0.350 + 0.003*SL
	t_{PHL}	0.239	0.229 + 0.005*SL	0.236 + 0.003*SL	0.253 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

AO211_LP/AO211D2_LP/AO211D4_LP

2-AND into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	0	0	1
x	0	0	0	1
Other States				0

Cell Data

Input Load (SL)											
AO211_LP				*AO211D2_LP*				*AO211D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.1	1.0	1.0	2.1	2.2	2.0	1.9	0.9	1.0	0.9	0.9

Gate Count		
AO211_LP	*AO211D2_LP*	*AO211D4_LP*
1.67	3.00	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO211_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.349	0.192 + 0.079*SL	0.182 + 0.081*SL	0.191 + 0.080*SL
	t_F	0.139	0.083 + 0.028*SL	0.071 + 0.031*SL	0.054 + 0.032*SL
	t_{PLH}	0.182	0.104 + 0.039*SL	0.102 + 0.040*SL	0.106 + 0.039*SL
	t_{PHL}	0.115	0.080 + 0.018*SL	0.084 + 0.017*SL	0.085 + 0.017*SL
B to Y	t_R	0.370	0.213 + 0.079*SL	0.204 + 0.081*SL	0.214 + 0.080*SL
	t_F	0.133	0.074 + 0.030*SL	0.066 + 0.032*SL	0.055 + 0.032*SL
	t_{PLH}	0.202	0.123 + 0.039*SL	0.123 + 0.039*SL	0.126 + 0.039*SL
	t_{PHL}	0.112	0.076 + 0.018*SL	0.080 + 0.017*SL	0.082 + 0.017*SL
C to Y	t_R	0.379	0.221 + 0.079*SL	0.216 + 0.080*SL	0.214 + 0.080*SL
	t_F	0.156	0.104 + 0.026*SL	0.098 + 0.028*SL	0.089 + 0.028*SL
	t_{PLH}	0.285	0.205 + 0.040*SL	0.207 + 0.039*SL	0.209 + 0.039*SL
	t_{PHL}	0.152	0.119 + 0.016*SL	0.123 + 0.016*SL	0.127 + 0.015*SL
D to Y	t_R	0.379	0.220 + 0.079*SL	0.216 + 0.080*SL	0.214 + 0.080*SL
	t_F	0.181	0.125 + 0.028*SL	0.123 + 0.029*SL	0.115 + 0.029*SL
	t_{PLH}	0.302	0.223 + 0.040*SL	0.224 + 0.039*SL	0.226 + 0.039*SL
	t_{PHL}	0.166	0.131 + 0.018*SL	0.136 + 0.016*SL	0.144 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO211D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.267	0.190 + 0.039*SL	0.183 + 0.040*SL	0.179 + 0.041*SL
	t_F	0.110	0.085 + 0.013*SL	0.075 + 0.015*SL	0.061 + 0.016*SL
	t_{PLH}	0.142	0.105 + 0.018*SL	0.099 + 0.020*SL	0.101 + 0.020*SL
	t_{PHL}	0.096	0.076 + 0.010*SL	0.082 + 0.008*SL	0.084 + 0.008*SL
B to Y	t_R	0.288	0.210 + 0.039*SL	0.204 + 0.040*SL	0.201 + 0.040*SL
	t_F	0.102	0.073 + 0.014*SL	0.070 + 0.015*SL	0.059 + 0.016*SL
	t_{PLH}	0.160	0.122 + 0.019*SL	0.119 + 0.020*SL	0.121 + 0.020*SL
	t_{PHL}	0.092	0.072 + 0.010*SL	0.078 + 0.009*SL	0.081 + 0.008*SL
C to Y	t_R	0.297	0.219 + 0.039*SL	0.215 + 0.040*SL	0.211 + 0.040*SL
	t_F	0.130	0.105 + 0.013*SL	0.102 + 0.013*SL	0.092 + 0.014*SL
	t_{PLH}	0.243	0.203 + 0.020*SL	0.204 + 0.020*SL	0.206 + 0.020*SL
	t_{PHL}	0.135	0.118 + 0.008*SL	0.120 + 0.008*SL	0.124 + 0.008*SL
D to Y	t_R	0.297	0.219 + 0.039*SL	0.215 + 0.040*SL	0.211 + 0.040*SL
	t_F	0.153	0.126 + 0.014*SL	0.123 + 0.014*SL	0.117 + 0.014*SL
	t_{PLH}	0.261	0.221 + 0.020*SL	0.222 + 0.020*SL	0.224 + 0.020*SL
	t_{PHL}	0.148	0.129 + 0.009*SL	0.132 + 0.008*SL	0.139 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AO211D4_LP

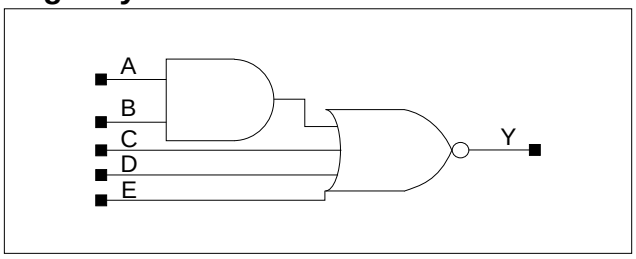
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.056 + 0.006*SL	0.054 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.077	0.065 + 0.006*SL	0.071 + 0.004*SL	0.073 + 0.004*SL
	t_{PLH}	0.313	0.303 + 0.005*SL	0.309 + 0.003*SL	0.317 + 0.003*SL
	t_{PHL}	0.301	0.289 + 0.006*SL	0.299 + 0.003*SL	0.327 + 0.003*SL
B to Y	t_R	0.068	0.056 + 0.006*SL	0.056 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.076	0.064 + 0.006*SL	0.071 + 0.004*SL	0.073 + 0.004*SL
	t_{PLH}	0.339	0.329 + 0.005*SL	0.335 + 0.003*SL	0.343 + 0.003*SL
	t_{PHL}	0.298	0.286 + 0.006*SL	0.295 + 0.003*SL	0.324 + 0.003*SL
C to Y	t_R	0.068	0.056 + 0.006*SL	0.056 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.076	0.063 + 0.006*SL	0.072 + 0.004*SL	0.074 + 0.004*SL
	t_{PLH}	0.423	0.413 + 0.005*SL	0.419 + 0.003*SL	0.427 + 0.003*SL
	t_{PHL}	0.315	0.303 + 0.006*SL	0.312 + 0.003*SL	0.340 + 0.003*SL
D to Y	t_R	0.069	0.057 + 0.006*SL	0.057 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.077	0.065 + 0.006*SL	0.072 + 0.004*SL	0.074 + 0.004*SL
	t_{PLH}	0.441	0.432 + 0.005*SL	0.438 + 0.003*SL	0.446 + 0.003*SL
	t_{PHL}	0.321	0.310 + 0.006*SL	0.319 + 0.003*SL	0.347 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

AO2111_LP/AO2111D2_LP

2-AND into 4-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0
Other states					1

Cell Data

Input Load (SL)										Gate Count	
A02111_LP					*AO2111D2_LP*					*AO2111_LP*	*AO2111D2_LP*
A	B	C	D	E	A	B	C	D	E		
1.0	1.0	0.9	0.9	0.9	1.0	0.9	0.9	0.9	0.9	2.00	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO2111_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.468	0.255 + 0.107*SL	0.249 + 0.108*SL	0.281 + 0.106*SL
	t_F	0.183	0.095 + 0.044*SL	0.084 + 0.046*SL	0.076 + 0.047*SL
	t_{PLH}	0.201	0.100 + 0.051*SL	0.092 + 0.053*SL	0.097 + 0.052*SL
	t_{PHL}	0.150	0.100 + 0.025*SL	0.101 + 0.025*SL	0.104 + 0.024*SL
B to Y	t_R	0.489	0.275 + 0.107*SL	0.270 + 0.108*SL	0.302 + 0.107*SL
	t_F	0.178	0.088 + 0.045*SL	0.082 + 0.047*SL	0.076 + 0.047*SL
	t_{PLH}	0.217	0.114 + 0.052*SL	0.110 + 0.053*SL	0.114 + 0.052*SL
	t_{PHL}	0.146	0.095 + 0.025*SL	0.098 + 0.025*SL	0.101 + 0.024*SL
C to Y	t_R	0.523	0.313 + 0.105*SL	0.308 + 0.106*SL	0.305 + 0.106*SL
	t_F	0.204	0.129 + 0.038*SL	0.124 + 0.039*SL	0.120 + 0.039*SL
	t_{PLH}	0.341	0.235 + 0.053*SL	0.237 + 0.053*SL	0.240 + 0.052*SL
	t_{PHL}	0.194	0.149 + 0.022*SL	0.153 + 0.021*SL	0.159 + 0.021*SL
D to Y	t_R	0.524	0.315 + 0.105*SL	0.309 + 0.106*SL	0.305 + 0.106*SL
	t_F	0.232	0.156 + 0.038*SL	0.153 + 0.039*SL	0.152 + 0.039*SL
	t_{PLH}	0.386	0.280 + 0.053*SL	0.282 + 0.053*SL	0.284 + 0.052*SL
	t_{PHL}	0.212	0.165 + 0.023*SL	0.172 + 0.022*SL	0.181 + 0.021*SL
E to Y	t_R	0.524	0.315 + 0.105*SL	0.308 + 0.106*SL	0.305 + 0.106*SL
	t_F	0.258	0.179 + 0.039*SL	0.180 + 0.039*SL	0.184 + 0.039*SL
	t_{PLH}	0.406	0.299 + 0.053*SL	0.302 + 0.053*SL	0.304 + 0.052*SL
	t_{PHL}	0.222	0.173 + 0.025*SL	0.182 + 0.022*SL	0.198 + 0.021*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO2111D2_LP

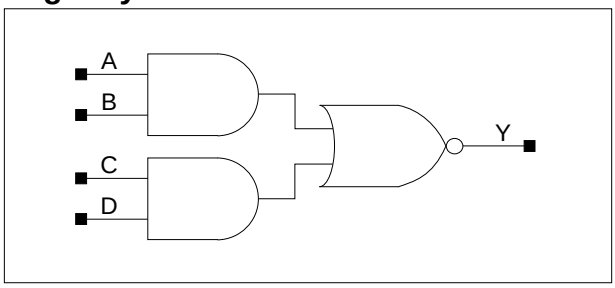
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.070	0.048 + 0.011*SL	0.041 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.065	0.047 + 0.009*SL	0.051 + 0.008*SL	0.044 + 0.009*SL
	t_{PLH}	0.275	0.260 + 0.007*SL	0.265 + 0.006*SL	0.267 + 0.006*SL
	t_{PHL}	0.289	0.273 + 0.008*SL	0.282 + 0.006*SL	0.295 + 0.005*SL
B to Y	t_R	0.070	0.049 + 0.011*SL	0.042 + 0.013*SL	0.032 + 0.013*SL
	t_F	0.064	0.045 + 0.009*SL	0.049 + 0.008*SL	0.044 + 0.009*SL
	t_{PLH}	0.293	0.278 + 0.008*SL	0.283 + 0.006*SL	0.285 + 0.006*SL
	t_{PHL}	0.285	0.269 + 0.008*SL	0.278 + 0.006*SL	0.291 + 0.005*SL
C to Y	t_R	0.069	0.045 + 0.012*SL	0.043 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.066	0.048 + 0.009*SL	0.052 + 0.008*SL	0.045 + 0.009*SL
	t_{PLH}	0.414	0.398 + 0.008*SL	0.403 + 0.006*SL	0.406 + 0.006*SL
	t_{PHL}	0.401	0.385 + 0.008*SL	0.394 + 0.006*SL	0.407 + 0.005*SL
D to Y	t_R	0.071	0.049 + 0.011*SL	0.043 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.067	0.048 + 0.009*SL	0.053 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.460	0.445 + 0.008*SL	0.449 + 0.006*SL	0.452 + 0.006*SL
	t_{PHL}	0.438	0.422 + 0.008*SL	0.431 + 0.006*SL	0.445 + 0.005*SL
E to Y	t_R	0.070	0.048 + 0.011*SL	0.043 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.067	0.048 + 0.009*SL	0.053 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.479	0.464 + 0.008*SL	0.469 + 0.006*SL	0.472 + 0.006*SL
	t_{PHL}	0.463	0.447 + 0.008*SL	0.457 + 0.006*SL	0.471 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AO22_LP/AO22D2_LP/AO22D4_LP

Two 2-ANDs into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

Cell Data

Input Load (SL)											
AO22_LP				*AO22D2_LP*				*AO22D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.1	1.1	1.1	2.2	2.1	2.2	2.1	0.8	0.8	0.9	0.9

Gate Count		
AO22_LP	*AO22D2_LP*	*AO22D4_LP*
2.00	3.00	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO22_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.245	0.143 + 0.051*SL	0.132 + 0.054*SL	0.129 + 0.054*SL
	t_F	0.150	0.097 + 0.027*SL	0.085 + 0.030*SL	0.067 + 0.031*SL
	t_{PLH}	0.162	0.110 + 0.026*SL	0.110 + 0.026*SL	0.113 + 0.026*SL
	t_{PHL}	0.111	0.077 + 0.017*SL	0.081 + 0.016*SL	0.083 + 0.016*SL
B to Y	t_R	0.259	0.156 + 0.051*SL	0.147 + 0.054*SL	0.145 + 0.054*SL
	t_F	0.143	0.087 + 0.028*SL	0.079 + 0.030*SL	0.067 + 0.031*SL
	t_{PLH}	0.176	0.123 + 0.026*SL	0.124 + 0.026*SL	0.126 + 0.026*SL
	t_{PHL}	0.108	0.073 + 0.018*SL	0.078 + 0.016*SL	0.080 + 0.016*SL
C to Y	t_R	0.241	0.135 + 0.053*SL	0.132 + 0.054*SL	0.130 + 0.054*SL
	t_F	0.184	0.126 + 0.029*SL	0.120 + 0.030*SL	0.110 + 0.031*SL
	t_{PLH}	0.218	0.165 + 0.027*SL	0.166 + 0.026*SL	0.168 + 0.026*SL
	t_{PHL}	0.158	0.123 + 0.018*SL	0.127 + 0.016*SL	0.134 + 0.016*SL
D to Y	t_R	0.256	0.150 + 0.053*SL	0.147 + 0.054*SL	0.145 + 0.054*SL
	t_F	0.180	0.121 + 0.029*SL	0.117 + 0.030*SL	0.111 + 0.031*SL
	t_{PLH}	0.232	0.179 + 0.026*SL	0.180 + 0.026*SL	0.182 + 0.026*SL
	t_{PHL}	0.155	0.120 + 0.018*SL	0.125 + 0.016*SL	0.131 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO22D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.195	0.145 + 0.025*SL	0.140 + 0.026*SL	0.127 + 0.027*SL
	t_F	0.123	0.097 + 0.013*SL	0.093 + 0.014*SL	0.077 + 0.015*SL
	t_{PLH}	0.138	0.113 + 0.013*SL	0.111 + 0.013*SL	0.113 + 0.013*SL
	t_{PHL}	0.094	0.074 + 0.010*SL	0.081 + 0.008*SL	0.083 + 0.008*SL
B to Y	t_R	0.209	0.158 + 0.025*SL	0.153 + 0.026*SL	0.142 + 0.027*SL
	t_F	0.116	0.088 + 0.014*SL	0.085 + 0.015*SL	0.074 + 0.015*SL
	t_{PLH}	0.152	0.125 + 0.013*SL	0.125 + 0.013*SL	0.127 + 0.013*SL
	t_{PHL}	0.090	0.071 + 0.010*SL	0.077 + 0.008*SL	0.080 + 0.008*SL
C to Y	t_R	0.188	0.136 + 0.026*SL	0.134 + 0.027*SL	0.130 + 0.027*SL
	t_F	0.152	0.123 + 0.014*SL	0.122 + 0.015*SL	0.112 + 0.015*SL
	t_{PLH}	0.188	0.161 + 0.013*SL	0.162 + 0.013*SL	0.164 + 0.013*SL
	t_{PHL}	0.139	0.121 + 0.009*SL	0.123 + 0.008*SL	0.128 + 0.008*SL
D to Y	t_R	0.203	0.150 + 0.027*SL	0.149 + 0.027*SL	0.146 + 0.027*SL
	t_F	0.148	0.119 + 0.014*SL	0.118 + 0.015*SL	0.112 + 0.015*SL
	t_{PLH}	0.202	0.176 + 0.013*SL	0.176 + 0.013*SL	0.178 + 0.013*SL
	t_{PHL}	0.135	0.117 + 0.009*SL	0.120 + 0.008*SL	0.125 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

AO22D4_LP

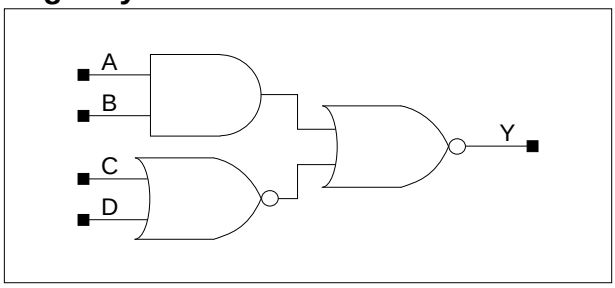
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.064	0.051 + 0.006*SL	0.053 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.057	0.047 + 0.005*SL	0.050 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.317	0.308 + 0.005*SL	0.313 + 0.003*SL	0.321 + 0.003*SL
	t_{PHL}	0.260	0.251 + 0.005*SL	0.257 + 0.003*SL	0.274 + 0.002*SL
B to Y	t_R	0.065	0.052 + 0.006*SL	0.053 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.056	0.046 + 0.005*SL	0.051 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.334	0.325 + 0.005*SL	0.331 + 0.003*SL	0.338 + 0.003*SL
	t_{PHL}	0.256	0.247 + 0.005*SL	0.253 + 0.003*SL	0.271 + 0.002*SL
C to Y	t_R	0.065	0.054 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.057	0.047 + 0.005*SL	0.051 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.365	0.355 + 0.005*SL	0.361 + 0.003*SL	0.369 + 0.003*SL
	t_{PHL}	0.295	0.286 + 0.005*SL	0.293 + 0.003*SL	0.310 + 0.002*SL
D to Y	t_R	0.065	0.054 + 0.006*SL	0.053 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.057	0.046 + 0.005*SL	0.051 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.383	0.373 + 0.005*SL	0.379 + 0.003*SL	0.387 + 0.003*SL
	t_{PHL}	0.292	0.282 + 0.005*SL	0.289 + 0.003*SL	0.306 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

AO22A_LP

2-AND and 2-NOR into 2-NOR with 1X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)				Gate Count
AO22A_LP				*AO22A_LP*
A	B	C	D	
1.1	1.1	0.9	0.9	3.00

Switching Characteristics

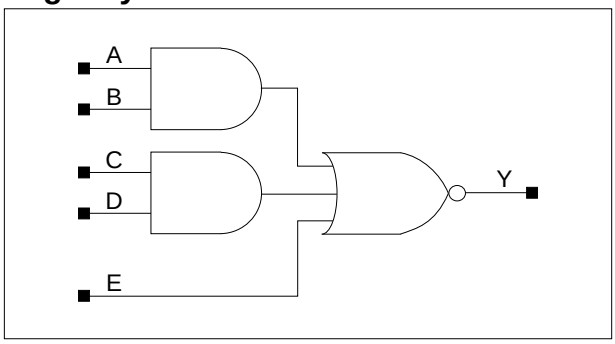
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO22A_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.245	0.143 + 0.051*SL	0.132 + 0.054*SL	0.129 + 0.054*SL
	t_F	0.151	0.097 + 0.027*SL	0.086 + 0.030*SL	0.067 + 0.031*SL
	t_{PLH}	0.162	0.110 + 0.026*SL	0.109 + 0.026*SL	0.112 + 0.026*SL
	t_{PHL}	0.111	0.076 + 0.017*SL	0.081 + 0.016*SL	0.082 + 0.016*SL
B to Y	t_R	0.260	0.157 + 0.051*SL	0.148 + 0.054*SL	0.146 + 0.054*SL
	t_F	0.142	0.086 + 0.028*SL	0.079 + 0.030*SL	0.067 + 0.031*SL
	t_{PLH}	0.176	0.123 + 0.026*SL	0.124 + 0.026*SL	0.127 + 0.026*SL
	t_{PHL}	0.107	0.072 + 0.018*SL	0.078 + 0.016*SL	0.080 + 0.016*SL
C to Y	t_R	0.240	0.134 + 0.053*SL	0.132 + 0.054*SL	0.130 + 0.054*SL
	t_F	0.178	0.117 + 0.031*SL	0.117 + 0.031*SL	0.114 + 0.031*SL
	t_{PLH}	0.252	0.199 + 0.027*SL	0.201 + 0.026*SL	0.203 + 0.026*SL
	t_{PHL}	0.229	0.194 + 0.018*SL	0.198 + 0.017*SL	0.205 + 0.016*SL
D to Y	t_R	0.257	0.150 + 0.053*SL	0.148 + 0.054*SL	0.147 + 0.054*SL
	t_F	0.178	0.117 + 0.030*SL	0.116 + 0.031*SL	0.114 + 0.031*SL
	t_{PLH}	0.266	0.213 + 0.026*SL	0.214 + 0.026*SL	0.216 + 0.026*SL
	t_{PHL}	0.232	0.197 + 0.018*SL	0.201 + 0.017*SL	0.208 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	0
x	x	1	1	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)														
AO221_LP					*AO221D2_LP*					*AO221D4_LP*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.1	1.1	1.1	1.1	1.0	1.0	1.0	1.0	1.0	0.9	1.0	1.0	1.0	1.0	0.9

Gate Count		
AO221_LP	*AO221D2_LP*	*AO221D4_LP*
2.33	3.33	3.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO221_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.393	0.233 + 0.080*SL	0.225 + 0.082*SL	0.244 + 0.081*SL
	t_F	0.159	0.102 + 0.029*SL	0.091 + 0.031*SL	0.075 + 0.032*SL
	t_{PLH}	0.201	0.122 + 0.039*SL	0.120 + 0.040*SL	0.125 + 0.040*SL
	t_{PHL}	0.120	0.084 + 0.018*SL	0.087 + 0.017*SL	0.089 + 0.017*SL
B to Y	t_R	0.413	0.253 + 0.080*SL	0.247 + 0.082*SL	0.265 + 0.081*SL
	t_F	0.153	0.093 + 0.030*SL	0.086 + 0.032*SL	0.075 + 0.032*SL
	t_{PLH}	0.219	0.140 + 0.040*SL	0.140 + 0.040*SL	0.144 + 0.039*SL
	t_{PHL}	0.115	0.080 + 0.018*SL	0.083 + 0.017*SL	0.086 + 0.017*SL
C to Y	t_R	0.414	0.255 + 0.079*SL	0.250 + 0.081*SL	0.247 + 0.081*SL
	t_F	0.196	0.134 + 0.031*SL	0.130 + 0.032*SL	0.121 + 0.032*SL
	t_{PLH}	0.312	0.231 + 0.040*SL	0.234 + 0.040*SL	0.238 + 0.040*SL
	t_{PHL}	0.170	0.133 + 0.018*SL	0.137 + 0.017*SL	0.144 + 0.017*SL
D to Y	t_R	0.435	0.276 + 0.079*SL	0.272 + 0.080*SL	0.269 + 0.081*SL
	t_F	0.192	0.129 + 0.031*SL	0.127 + 0.032*SL	0.122 + 0.032*SL
	t_{PLH}	0.332	0.252 + 0.040*SL	0.254 + 0.040*SL	0.257 + 0.039*SL
	t_{PHL}	0.167	0.130 + 0.018*SL	0.134 + 0.017*SL	0.141 + 0.017*SL
E to Y	t_R	0.435	0.276 + 0.079*SL	0.272 + 0.080*SL	0.269 + 0.081*SL
	t_F	0.232	0.175 + 0.029*SL	0.171 + 0.030*SL	0.167 + 0.030*SL
	t_{PLH}	0.367	0.287 + 0.040*SL	0.289 + 0.040*SL	0.292 + 0.039*SL
	t_{PHL}	0.193	0.155 + 0.019*SL	0.162 + 0.017*SL	0.175 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO221D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.068	0.046 + 0.011*SL	0.039 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.066	0.047 + 0.009*SL	0.052 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.280	0.265 + 0.007*SL	0.269 + 0.006*SL	0.271 + 0.006*SL
	t_{PHL}	0.296	0.280 + 0.008*SL	0.289 + 0.006*SL	0.303 + 0.005*SL
B to Y	t_R	0.068	0.045 + 0.011*SL	0.040 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.066	0.047 + 0.009*SL	0.052 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.295	0.281 + 0.007*SL	0.285 + 0.006*SL	0.287 + 0.006*SL
	t_{PHL}	0.292	0.276 + 0.008*SL	0.285 + 0.006*SL	0.299 + 0.005*SL
C to Y	t_R	0.068	0.045 + 0.011*SL	0.040 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.066	0.047 + 0.009*SL	0.052 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.373	0.359 + 0.007*SL	0.363 + 0.006*SL	0.365 + 0.006*SL
	t_{PHL}	0.361	0.345 + 0.008*SL	0.354 + 0.006*SL	0.368 + 0.005*SL
D to Y	t_R	0.068	0.046 + 0.011*SL	0.040 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.066	0.048 + 0.009*SL	0.052 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.391	0.376 + 0.007*SL	0.381 + 0.006*SL	0.383 + 0.006*SL
	t_{PHL}	0.358	0.342 + 0.008*SL	0.351 + 0.006*SL	0.365 + 0.005*SL
E to Y	t_R	0.067	0.042 + 0.012*SL	0.040 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.068	0.049 + 0.009*SL	0.054 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.428	0.413 + 0.007*SL	0.417 + 0.006*SL	0.420 + 0.006*SL
	t_{PHL}	0.417	0.401 + 0.008*SL	0.410 + 0.006*SL	0.424 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO221D4_LP

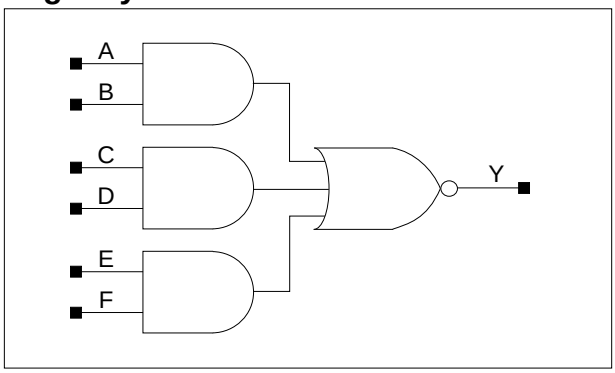
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.056 + 0.006*SL	0.055 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.070	0.058 + 0.006*SL	0.065 + 0.004*SL	0.065 + 0.004*SL
	t_{PLH}	0.315	0.306 + 0.005*SL	0.312 + 0.003*SL	0.320 + 0.003*SL
	t_{PHL}	0.331	0.320 + 0.006*SL	0.329 + 0.003*SL	0.353 + 0.003*SL
B to Y	t_R	0.067	0.056 + 0.005*SL	0.054 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.071	0.060 + 0.005*SL	0.064 + 0.004*SL	0.065 + 0.004*SL
	t_{PLH}	0.332	0.322 + 0.005*SL	0.328 + 0.003*SL	0.336 + 0.003*SL
	t_{PHL}	0.327	0.316 + 0.006*SL	0.325 + 0.003*SL	0.349 + 0.003*SL
C to Y	t_R	0.068	0.056 + 0.006*SL	0.055 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.072	0.061 + 0.005*SL	0.066 + 0.004*SL	0.066 + 0.004*SL
	t_{PLH}	0.409	0.399 + 0.005*SL	0.405 + 0.003*SL	0.413 + 0.003*SL
	t_{PHL}	0.396	0.384 + 0.006*SL	0.394 + 0.003*SL	0.418 + 0.003*SL
D to Y	t_R	0.068	0.057 + 0.006*SL	0.056 + 0.006*SL	0.040 + 0.006*SL
	t_F	0.071	0.059 + 0.006*SL	0.066 + 0.004*SL	0.065 + 0.004*SL
	t_{PLH}	0.427	0.417 + 0.005*SL	0.423 + 0.003*SL	0.432 + 0.003*SL
	t_{PHL}	0.392	0.381 + 0.005*SL	0.390 + 0.003*SL	0.415 + 0.003*SL
E to Y	t_R	0.067	0.054 + 0.007*SL	0.056 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.072	0.062 + 0.005*SL	0.066 + 0.004*SL	0.067 + 0.004*SL
	t_{PLH}	0.464	0.454 + 0.005*SL	0.460 + 0.003*SL	0.468 + 0.003*SL
	t_{PHL}	0.453	0.441 + 0.006*SL	0.450 + 0.003*SL	0.475 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

AO222_LP/AO222D2_LP/AO222D4_LP

Three 2-ANDs into 3-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
Other States						1

Cell Data

Input Load (SL)						Gate Count
AO222_LP						*AO222_LP*
A	B	C	D	E	F	
1.0	1.1	1.0	1.1	1.1	1.1	2.67
AO222D2_LP						*AO222D2_LP*
A	B	C	D	E	F	
0.9	0.9	0.9	0.9	0.9	0.9	3.67
AO222D4_LP						*AO222D4_LP*
A	B	C	D	E	F	
0.9	0.9	0.9	0.9	0.9	0.9	4.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO222_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.421	0.259 + 0.081*SL	0.255 + 0.082*SL	0.274 + 0.081*SL
	t_F	0.180	0.120 + 0.030*SL	0.110 + 0.032*SL	0.094 + 0.033*SL
	t_{PLH}	0.224	0.145 + 0.040*SL	0.145 + 0.040*SL	0.149 + 0.040*SL
	t_{PHL}	0.124	0.088 + 0.018*SL	0.090 + 0.017*SL	0.092 + 0.017*SL
B to Y	t_R	0.441	0.280 + 0.081*SL	0.276 + 0.082*SL	0.295 + 0.081*SL
	t_F	0.174	0.113 + 0.031*SL	0.105 + 0.033*SL	0.094 + 0.033*SL
	t_{PLH}	0.243	0.163 + 0.040*SL	0.164 + 0.040*SL	0.168 + 0.039*SL
	t_{PHL}	0.120	0.084 + 0.018*SL	0.087 + 0.017*SL	0.089 + 0.017*SL
C to Y	t_R	0.442	0.283 + 0.080*SL	0.279 + 0.081*SL	0.276 + 0.081*SL
	t_F	0.217	0.154 + 0.032*SL	0.149 + 0.033*SL	0.141 + 0.033*SL
	t_{PLH}	0.335	0.254 + 0.040*SL	0.256 + 0.040*SL	0.260 + 0.040*SL
	t_{PHL}	0.176	0.138 + 0.019*SL	0.142 + 0.018*SL	0.148 + 0.017*SL
D to Y	t_R	0.462	0.303 + 0.080*SL	0.300 + 0.080*SL	0.298 + 0.081*SL
	t_F	0.214	0.150 + 0.032*SL	0.147 + 0.033*SL	0.142 + 0.033*SL
	t_{PLH}	0.355	0.274 + 0.040*SL	0.277 + 0.040*SL	0.279 + 0.039*SL
	t_{PHL}	0.173	0.135 + 0.019*SL	0.139 + 0.018*SL	0.146 + 0.017*SL
E to Y	t_R	0.441	0.282 + 0.080*SL	0.279 + 0.080*SL	0.276 + 0.081*SL
	t_F	0.252	0.186 + 0.033*SL	0.186 + 0.033*SL	0.184 + 0.033*SL
	t_{PLH}	0.379	0.298 + 0.040*SL	0.301 + 0.040*SL	0.305 + 0.039*SL
	t_{PHL}	0.204	0.163 + 0.020*SL	0.171 + 0.018*SL	0.185 + 0.018*SL
F to Y	t_R	0.463	0.303 + 0.080*SL	0.300 + 0.080*SL	0.298 + 0.081*SL
	t_F	0.252	0.185 + 0.033*SL	0.186 + 0.033*SL	0.184 + 0.033*SL
	t_{PLH}	0.399	0.319 + 0.040*SL	0.322 + 0.040*SL	0.324 + 0.039*SL
	t_{PHL}	0.201	0.160 + 0.020*SL	0.168 + 0.018*SL	0.183 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO222D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.069	0.046 + 0.011*SL	0.041 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.045 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.296	0.281 + 0.008*SL	0.286 + 0.006*SL	0.289 + 0.006*SL
	t_{PHL}	0.305	0.290 + 0.007*SL	0.299 + 0.005*SL	0.308 + 0.005*SL
B to Y	t_R	0.068	0.045 + 0.012*SL	0.041 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.059	0.040 + 0.009*SL	0.045 + 0.008*SL	0.036 + 0.009*SL
	t_{PLH}	0.308	0.293 + 0.008*SL	0.298 + 0.006*SL	0.300 + 0.006*SL
	t_{PHL}	0.301	0.286 + 0.007*SL	0.294 + 0.005*SL	0.305 + 0.005*SL
C to Y	t_R	0.067	0.043 + 0.012*SL	0.041 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.046 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.407	0.392 + 0.008*SL	0.396 + 0.006*SL	0.399 + 0.006*SL
	t_{PHL}	0.401	0.386 + 0.007*SL	0.394 + 0.005*SL	0.404 + 0.005*SL
D to Y	t_R	0.069	0.046 + 0.011*SL	0.041 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.045 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.419	0.404 + 0.008*SL	0.409 + 0.006*SL	0.412 + 0.006*SL
	t_{PHL}	0.398	0.383 + 0.007*SL	0.391 + 0.005*SL	0.402 + 0.005*SL
E to Y	t_R	0.068	0.044 + 0.012*SL	0.041 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.062	0.045 + 0.009*SL	0.047 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.451	0.436 + 0.008*SL	0.441 + 0.006*SL	0.443 + 0.006*SL
	t_{PHL}	0.465	0.449 + 0.008*SL	0.458 + 0.005*SL	0.469 + 0.005*SL
F to Y	t_R	0.069	0.046 + 0.011*SL	0.041 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.061	0.043 + 0.009*SL	0.047 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.464	0.449 + 0.008*SL	0.454 + 0.006*SL	0.457 + 0.006*SL
	t_{PHL}	0.462	0.447 + 0.008*SL	0.455 + 0.005*SL	0.465 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO222D4_LP

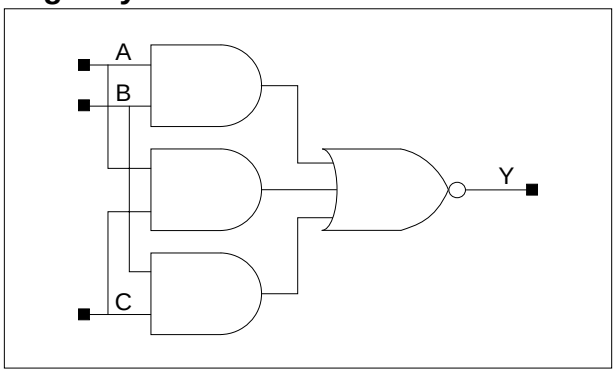
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.069	0.057 + 0.006*SL	0.056 + 0.006*SL	0.041 + 0.007*SL
	t_F	0.063	0.053 + 0.005*SL	0.057 + 0.004*SL	0.055 + 0.004*SL
	t_{PLH}	0.329	0.319 + 0.005*SL	0.325 + 0.003*SL	0.334 + 0.003*SL
	t_{PHL}	0.341	0.331 + 0.005*SL	0.339 + 0.003*SL	0.359 + 0.002*SL
B to Y	t_R	0.068	0.054 + 0.007*SL	0.057 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.064	0.054 + 0.005*SL	0.056 + 0.004*SL	0.055 + 0.004*SL
	t_{PLH}	0.341	0.331 + 0.005*SL	0.337 + 0.003*SL	0.346 + 0.003*SL
	t_{PHL}	0.337	0.327 + 0.005*SL	0.335 + 0.003*SL	0.355 + 0.002*SL
C to Y	t_R	0.069	0.058 + 0.006*SL	0.058 + 0.006*SL	0.041 + 0.007*SL
	t_F	0.063	0.052 + 0.006*SL	0.058 + 0.004*SL	0.055 + 0.004*SL
	t_{PLH}	0.440	0.430 + 0.005*SL	0.436 + 0.003*SL	0.445 + 0.003*SL
	t_{PHL}	0.438	0.427 + 0.005*SL	0.435 + 0.003*SL	0.456 + 0.002*SL
D to Y	t_R	0.069	0.058 + 0.006*SL	0.057 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.064	0.053 + 0.005*SL	0.058 + 0.004*SL	0.055 + 0.004*SL
	t_{PLH}	0.452	0.443 + 0.005*SL	0.449 + 0.003*SL	0.458 + 0.003*SL
	t_{PHL}	0.435	0.425 + 0.005*SL	0.432 + 0.003*SL	0.453 + 0.002*SL
E to Y	t_R	0.068	0.055 + 0.007*SL	0.057 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.065	0.054 + 0.006*SL	0.060 + 0.004*SL	0.056 + 0.004*SL
	t_{PLH}	0.484	0.474 + 0.005*SL	0.481 + 0.003*SL	0.489 + 0.003*SL
	t_{PHL}	0.502	0.492 + 0.005*SL	0.500 + 0.003*SL	0.521 + 0.002*SL
F to Y	t_R	0.069	0.057 + 0.006*SL	0.057 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.066	0.055 + 0.006*SL	0.060 + 0.004*SL	0.057 + 0.004*SL
	t_{PLH}	0.497	0.487 + 0.005*SL	0.494 + 0.003*SL	0.503 + 0.003*SL
	t_{PHL}	0.499	0.489 + 0.005*SL	0.497 + 0.003*SL	0.518 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

AO222A_LP

Inverting 2-of-3 Majority with 1X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Cell Data

Input Load (SL)			Gate Count
AO222A_LP			*AO222A_LP*
A	B	C	
2.0	2.2	2.2	2.33

Switching Characteristics

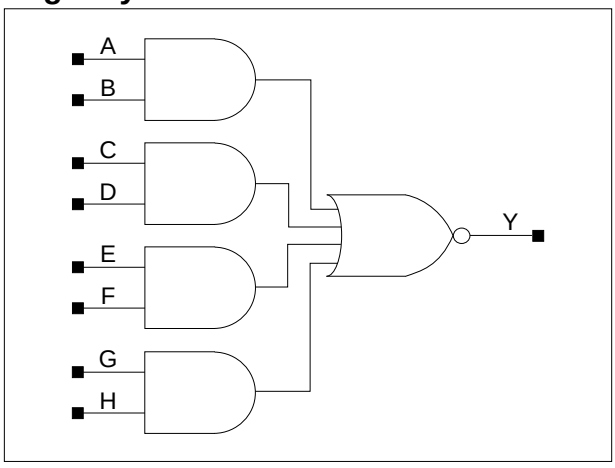
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO222A_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.398	0.295 + 0.051*SL	0.285 + 0.054*SL	0.285 + 0.054*SL
	t_F	0.171	0.121 + 0.025*SL	0.116 + 0.026*SL	0.108 + 0.027*SL
	t_{PLH}	0.206	0.153 + 0.026*SL	0.154 + 0.026*SL	0.157 + 0.026*SL
	t_{PHL}	0.149	0.119 + 0.015*SL	0.121 + 0.014*SL	0.126 + 0.014*SL
B to Y	t_R	0.395	0.290 + 0.052*SL	0.285 + 0.054*SL	0.285 + 0.054*SL
	t_F	0.180	0.128 + 0.026*SL	0.125 + 0.026*SL	0.117 + 0.027*SL
	t_{PLH}	0.221	0.168 + 0.027*SL	0.169 + 0.026*SL	0.173 + 0.026*SL
	t_{PHL}	0.165	0.135 + 0.015*SL	0.138 + 0.014*SL	0.143 + 0.014*SL
C to Y	t_R	0.363	0.259 + 0.052*SL	0.254 + 0.053*SL	0.250 + 0.054*SL
	t_F	0.181	0.130 + 0.026*SL	0.127 + 0.026*SL	0.118 + 0.027*SL
	t_{PLH}	0.235	0.183 + 0.026*SL	0.183 + 0.026*SL	0.185 + 0.026*SL
	t_{PHL}	0.151	0.121 + 0.015*SL	0.124 + 0.014*SL	0.128 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	0
x	x	1	1	x	x	x	x	0
x	x	x	x	1	1	x	x	0
x	x	x	x	x	x	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
AO2222_LP								*AO2222_LP*
A	B	C	D	E	F	G	H	
1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	3.33
AO2222D2_LP								*AO2222D2_LP*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	1.0	1.0	1.0	4.33
AO2222D4_LP								*AO2222D4_LP*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	1.0	1.0	1.0	5.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO2222_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.565	0.344 + 0.111*SL	0.342 + 0.111*SL	0.390 + 0.108*SL
	t_F	0.236	0.150 + 0.043*SL	0.140 + 0.046*SL	0.132 + 0.046*SL
	t_{PLH}	0.233	0.132 + 0.051*SL	0.121 + 0.053*SL	0.126 + 0.053*SL
	t_{PHL}	0.156	0.107 + 0.024*SL	0.108 + 0.024*SL	0.111 + 0.024*SL
B to Y	t_R	0.585	0.364 + 0.110*SL	0.363 + 0.111*SL	0.411 + 0.108*SL
	t_F	0.232	0.144 + 0.044*SL	0.138 + 0.046*SL	0.132 + 0.046*SL
	t_{PLH}	0.250	0.147 + 0.051*SL	0.139 + 0.053*SL	0.143 + 0.053*SL
	t_{PHL}	0.153	0.103 + 0.025*SL	0.105 + 0.024*SL	0.108 + 0.024*SL
C to Y	t_R	0.630	0.417 + 0.107*SL	0.413 + 0.108*SL	0.409 + 0.108*SL
	t_F	0.299	0.209 + 0.045*SL	0.206 + 0.046*SL	0.203 + 0.046*SL
	t_{PLH}	0.398	0.289 + 0.054*SL	0.293 + 0.053*SL	0.297 + 0.053*SL
	t_{PHL}	0.233	0.181 + 0.026*SL	0.186 + 0.025*SL	0.193 + 0.024*SL
D to Y	t_R	0.650	0.437 + 0.107*SL	0.433 + 0.107*SL	0.430 + 0.108*SL
	t_F	0.298	0.208 + 0.045*SL	0.206 + 0.046*SL	0.203 + 0.046*SL
	t_{PLH}	0.417	0.309 + 0.054*SL	0.312 + 0.053*SL	0.316 + 0.053*SL
	t_{PHL}	0.230	0.179 + 0.026*SL	0.183 + 0.025*SL	0.191 + 0.024*SL
E to Y	t_R	0.654	0.443 + 0.106*SL	0.436 + 0.107*SL	0.430 + 0.108*SL
	t_F	0.359	0.267 + 0.046*SL	0.267 + 0.046*SL	0.268 + 0.046*SL
	t_{PLH}	0.511	0.403 + 0.054*SL	0.406 + 0.053*SL	0.411 + 0.053*SL
	t_{PHL}	0.270	0.216 + 0.027*SL	0.224 + 0.025*SL	0.239 + 0.024*SL
F to Y	t_R	0.671	0.460 + 0.106*SL	0.455 + 0.107*SL	0.449 + 0.107*SL
	t_F	0.360	0.268 + 0.046*SL	0.269 + 0.046*SL	0.268 + 0.046*SL
	t_{PLH}	0.528	0.421 + 0.054*SL	0.424 + 0.053*SL	0.427 + 0.053*SL
	t_{PHL}	0.268	0.213 + 0.027*SL	0.221 + 0.025*SL	0.236 + 0.024*SL
G to Y	t_R	0.653	0.442 + 0.106*SL	0.436 + 0.107*SL	0.429 + 0.107*SL
	t_F	0.420	0.324 + 0.048*SL	0.329 + 0.047*SL	0.341 + 0.046*SL
	t_{PLH}	0.562	0.454 + 0.054*SL	0.458 + 0.053*SL	0.462 + 0.053*SL
	t_{PHL}	0.294	0.234 + 0.030*SL	0.247 + 0.026*SL	0.275 + 0.025*SL
H to Y	t_R	0.671	0.460 + 0.106*SL	0.455 + 0.107*SL	0.449 + 0.107*SL
	t_F	0.423	0.327 + 0.048*SL	0.332 + 0.047*SL	0.346 + 0.046*SL
	t_{PLH}	0.580	0.473 + 0.054*SL	0.476 + 0.053*SL	0.479 + 0.053*SL
	t_{PHL}	0.291	0.232 + 0.030*SL	0.244 + 0.026*SL	0.273 + 0.025*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO2222D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.070	0.049 + 0.011*SL	0.042 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.067	0.049 + 0.009*SL	0.053 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.295	0.279 + 0.008*SL	0.284 + 0.006*SL	0.287 + 0.006*SL
	t_{PHL}	0.338	0.321 + 0.008*SL	0.331 + 0.006*SL	0.345 + 0.005*SL
B to Y	t_R	0.069	0.047 + 0.011*SL	0.041 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.066	0.048 + 0.009*SL	0.052 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.309	0.293 + 0.008*SL	0.299 + 0.006*SL	0.301 + 0.006*SL
	t_{PHL}	0.334	0.318 + 0.008*SL	0.327 + 0.006*SL	0.341 + 0.005*SL
C to Y	t_R	0.071	0.048 + 0.011*SL	0.044 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.067	0.049 + 0.009*SL	0.053 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.455	0.440 + 0.008*SL	0.445 + 0.006*SL	0.448 + 0.006*SL
	t_{PHL}	0.441	0.425 + 0.008*SL	0.434 + 0.006*SL	0.448 + 0.005*SL
D to Y	t_R	0.071	0.049 + 0.011*SL	0.043 + 0.012*SL	0.031 + 0.013*SL
	t_F	0.068	0.049 + 0.009*SL	0.054 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.472	0.456 + 0.008*SL	0.462 + 0.006*SL	0.464 + 0.006*SL
	t_{PHL}	0.437	0.421 + 0.008*SL	0.431 + 0.006*SL	0.445 + 0.005*SL
E to Y	t_R	0.072	0.050 + 0.011*SL	0.044 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.068	0.050 + 0.009*SL	0.054 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.566	0.550 + 0.008*SL	0.556 + 0.006*SL	0.558 + 0.006*SL
	t_{PHL}	0.502	0.486 + 0.008*SL	0.496 + 0.006*SL	0.510 + 0.005*SL
F to Y	t_R	0.071	0.047 + 0.012*SL	0.045 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.069	0.051 + 0.009*SL	0.055 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.581	0.566 + 0.008*SL	0.571 + 0.006*SL	0.574 + 0.006*SL
	t_{PHL}	0.499	0.483 + 0.008*SL	0.493 + 0.006*SL	0.507 + 0.005*SL
G to Y	t_R	0.072	0.050 + 0.011*SL	0.044 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.072	0.054 + 0.009*SL	0.058 + 0.008*SL	0.051 + 0.008*SL
	t_{PLH}	0.610	0.594 + 0.008*SL	0.600 + 0.006*SL	0.602 + 0.006*SL
	t_{PHL}	0.544	0.527 + 0.008*SL	0.537 + 0.006*SL	0.552 + 0.005*SL
H to Y	t_R	0.071	0.047 + 0.012*SL	0.045 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.071	0.053 + 0.009*SL	0.057 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.625	0.610 + 0.008*SL	0.615 + 0.006*SL	0.618 + 0.006*SL
	t_{PHL}	0.541	0.524 + 0.008*SL	0.535 + 0.006*SL	0.550 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

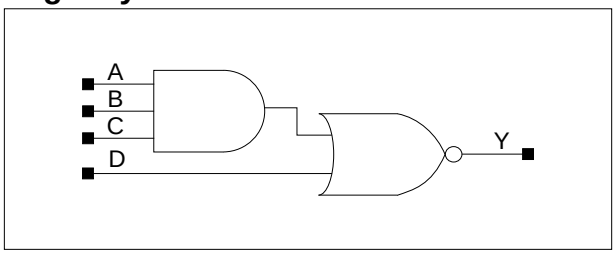
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO2222D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.071	0.060 + 0.005*SL	0.058 + 0.006*SL	0.043 + 0.006*SL
	t_F	0.077	0.065 + 0.006*SL	0.073 + 0.004*SL	0.076 + 0.004*SL
	t_{PLH}	0.332	0.322 + 0.005*SL	0.328 + 0.003*SL	0.338 + 0.003*SL
	t_{PHL}	0.394	0.383 + 0.006*SL	0.392 + 0.003*SL	0.420 + 0.003*SL
B to Y	t_R	0.072	0.060 + 0.006*SL	0.061 + 0.006*SL	0.043 + 0.006*SL
	t_F	0.078	0.066 + 0.006*SL	0.073 + 0.004*SL	0.074 + 0.004*SL
	t_{PLH}	0.346	0.336 + 0.005*SL	0.343 + 0.003*SL	0.352 + 0.003*SL
	t_{PHL}	0.390	0.379 + 0.006*SL	0.388 + 0.003*SL	0.416 + 0.003*SL
C to Y	t_R	0.073	0.062 + 0.005*SL	0.059 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.078	0.066 + 0.006*SL	0.074 + 0.004*SL	0.076 + 0.004*SL
	t_{PLH}	0.494	0.484 + 0.005*SL	0.490 + 0.003*SL	0.500 + 0.003*SL
	t_{PHL}	0.497	0.486 + 0.006*SL	0.495 + 0.003*SL	0.524 + 0.003*SL
D to Y	t_R	0.073	0.062 + 0.006*SL	0.061 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.079	0.067 + 0.006*SL	0.074 + 0.004*SL	0.076 + 0.004*SL
	t_{PLH}	0.510	0.500 + 0.005*SL	0.507 + 0.003*SL	0.517 + 0.003*SL
	t_{PHL}	0.494	0.482 + 0.006*SL	0.492 + 0.003*SL	0.521 + 0.003*SL
E to Y	t_R	0.072	0.058 + 0.007*SL	0.062 + 0.006*SL	0.043 + 0.006*SL
	t_F	0.080	0.067 + 0.006*SL	0.075 + 0.004*SL	0.078 + 0.004*SL
	t_{PLH}	0.604	0.594 + 0.005*SL	0.601 + 0.003*SL	0.610 + 0.003*SL
	t_{PHL}	0.561	0.550 + 0.006*SL	0.559 + 0.004*SL	0.588 + 0.003*SL
F to Y	t_R	0.074	0.062 + 0.006*SL	0.062 + 0.006*SL	0.043 + 0.006*SL
	t_F	0.081	0.069 + 0.006*SL	0.076 + 0.004*SL	0.077 + 0.004*SL
	t_{PLH}	0.620	0.610 + 0.005*SL	0.617 + 0.003*SL	0.627 + 0.003*SL
	t_{PHL}	0.558	0.546 + 0.006*SL	0.556 + 0.004*SL	0.585 + 0.003*SL
G to Y	t_R	0.072	0.059 + 0.007*SL	0.062 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.084	0.071 + 0.006*SL	0.079 + 0.004*SL	0.080 + 0.004*SL
	t_{PLH}	0.648	0.638 + 0.005*SL	0.645 + 0.003*SL	0.655 + 0.003*SL
	t_{PHL}	0.606	0.594 + 0.006*SL	0.603 + 0.004*SL	0.633 + 0.003*SL
H to Y	t_R	0.073	0.062 + 0.006*SL	0.062 + 0.006*SL	0.043 + 0.006*SL
	t_F	0.083	0.071 + 0.006*SL	0.079 + 0.004*SL	0.079 + 0.004*SL
	t_{PLH}	0.664	0.654 + 0.005*SL	0.661 + 0.003*SL	0.671 + 0.003*SL
	t_{PHL}	0.603	0.591 + 0.006*SL	0.601 + 0.004*SL	0.631 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	1	x	0
x	x	x	1	0
Other States				1

Cell Data

Input Load (SL)											
AO31_LP				*AO31D2_LP*				*AO31D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.1	1.1	1.1	2.3	2.3	2.2	2.1	0.9	0.9	0.9	0.8

Gate Count		
AO31_LP	*AO31D2_LP*	*AO31D4_LP*
1.67	3.00	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO31_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.260	0.159 + 0.051*SL	0.148 + 0.053*SL	0.144 + 0.054*SL
	t_F	0.180	0.112 + 0.034*SL	0.102 + 0.037*SL	0.090 + 0.037*SL
	t_{PLH}	0.164	0.112 + 0.026*SL	0.112 + 0.026*SL	0.115 + 0.026*SL
	t_{PHL}	0.135	0.095 + 0.020*SL	0.096 + 0.019*SL	0.098 + 0.019*SL
B to Y	t_R	0.277	0.175 + 0.051*SL	0.165 + 0.054*SL	0.163 + 0.054*SL
	t_F	0.177	0.106 + 0.035*SL	0.099 + 0.037*SL	0.090 + 0.037*SL
	t_{PLH}	0.181	0.128 + 0.026*SL	0.129 + 0.026*SL	0.131 + 0.026*SL
	t_{PHL}	0.137	0.097 + 0.020*SL	0.100 + 0.019*SL	0.102 + 0.019*SL
C to Y	t_R	0.294	0.191 + 0.051*SL	0.183 + 0.054*SL	0.181 + 0.054*SL
	t_F	0.173	0.101 + 0.036*SL	0.097 + 0.037*SL	0.090 + 0.037*SL
	t_{PLH}	0.195	0.142 + 0.027*SL	0.144 + 0.026*SL	0.146 + 0.026*SL
	t_{PHL}	0.137	0.098 + 0.020*SL	0.100 + 0.019*SL	0.102 + 0.019*SL
D to Y	t_R	0.292	0.186 + 0.053*SL	0.183 + 0.054*SL	0.181 + 0.054*SL
	t_F	0.137	0.100 + 0.018*SL	0.099 + 0.019*SL	0.086 + 0.019*SL
	t_{PLH}	0.244	0.191 + 0.027*SL	0.192 + 0.026*SL	0.195 + 0.026*SL
	t_{PHL}	0.134	0.112 + 0.011*SL	0.114 + 0.011*SL	0.117 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO31D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.209	0.160 + 0.025*SL	0.154 + 0.026*SL	0.142 + 0.027*SL
	t_F	0.145	0.111 + 0.017*SL	0.108 + 0.018*SL	0.093 + 0.019*SL
	t_{PLH}	0.138	0.112 + 0.013*SL	0.111 + 0.013*SL	0.113 + 0.013*SL
	t_{PHL}	0.113	0.093 + 0.010*SL	0.095 + 0.010*SL	0.096 + 0.010*SL
B to Y	t_R	0.226	0.176 + 0.025*SL	0.171 + 0.026*SL	0.161 + 0.027*SL
	t_F	0.140	0.104 + 0.018*SL	0.103 + 0.018*SL	0.093 + 0.019*SL
	t_{PLH}	0.155	0.128 + 0.013*SL	0.128 + 0.013*SL	0.130 + 0.013*SL
	t_{PHL}	0.116	0.095 + 0.010*SL	0.098 + 0.010*SL	0.100 + 0.010*SL
C to Y	t_R	0.243	0.193 + 0.025*SL	0.188 + 0.026*SL	0.179 + 0.027*SL
	t_F	0.136	0.101 + 0.018*SL	0.098 + 0.018*SL	0.092 + 0.019*SL
	t_{PLH}	0.168	0.141 + 0.013*SL	0.142 + 0.013*SL	0.145 + 0.013*SL
	t_{PHL}	0.116	0.096 + 0.010*SL	0.098 + 0.010*SL	0.100 + 0.010*SL
D to Y	t_R	0.239	0.186 + 0.027*SL	0.185 + 0.027*SL	0.182 + 0.027*SL
	t_F	0.127	0.110 + 0.008*SL	0.108 + 0.009*SL	0.097 + 0.009*SL
	t_{PLH}	0.220	0.193 + 0.013*SL	0.194 + 0.013*SL	0.196 + 0.013*SL
	t_{PHL}	0.123	0.112 + 0.006*SL	0.113 + 0.005*SL	0.116 + 0.005*SL

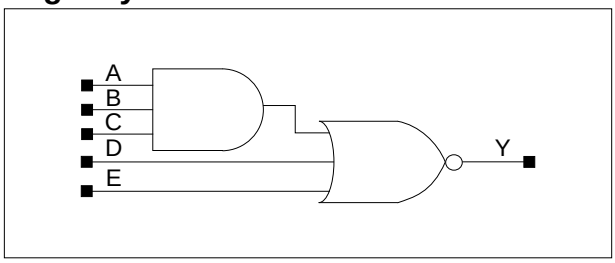
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AO31D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.064	0.052 + 0.006*SL	0.052 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.058	0.048 + 0.005*SL	0.052 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.309	0.300 + 0.005*SL	0.305 + 0.003*SL	0.313 + 0.003*SL
	t_{PHL}	0.296	0.287 + 0.005*SL	0.294 + 0.003*SL	0.312 + 0.002*SL
B to Y	t_R	0.064	0.053 + 0.006*SL	0.051 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.058	0.047 + 0.005*SL	0.052 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.328	0.319 + 0.005*SL	0.324 + 0.003*SL	0.332 + 0.003*SL
	t_{PHL}	0.299	0.290 + 0.005*SL	0.297 + 0.003*SL	0.315 + 0.002*SL
C to Y	t_R	0.065	0.054 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.058	0.047 + 0.005*SL	0.052 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.344	0.335 + 0.005*SL	0.340 + 0.003*SL	0.348 + 0.003*SL
	t_{PHL}	0.299	0.289 + 0.005*SL	0.296 + 0.003*SL	0.314 + 0.002*SL
D to Y	t_R	0.063	0.050 + 0.006*SL	0.052 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.057	0.048 + 0.004*SL	0.048 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.392	0.382 + 0.005*SL	0.388 + 0.003*SL	0.396 + 0.003*SL
	t_{PHL}	0.325	0.316 + 0.005*SL	0.323 + 0.003*SL	0.340 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)					Gate Count
AO311_LP					*AO311_LP*
A	B	C	D	E	
1.1	1.1	1.1	1.0	1.0	2.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO311_LP

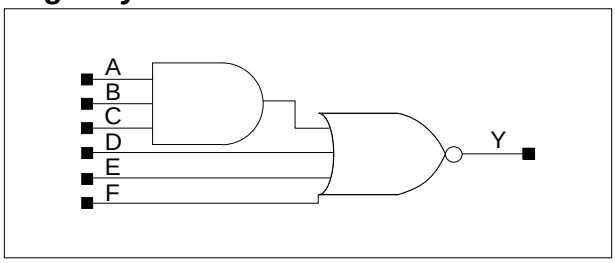
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.422	0.264 + 0.079*SL	0.257 + 0.081*SL	0.272 + 0.080*SL
	t_F	0.188	0.119 + 0.035*SL	0.111 + 0.037*SL	0.101 + 0.037*SL
	t_{PLH}	0.209	0.130 + 0.039*SL	0.130 + 0.039*SL	0.134 + 0.039*SL
	t_{PHL}	0.140	0.102 + 0.019*SL	0.102 + 0.019*SL	0.104 + 0.019*SL
B to Y	t_R	0.452	0.292 + 0.080*SL	0.288 + 0.081*SL	0.303 + 0.080*SL
	t_F	0.185	0.115 + 0.035*SL	0.109 + 0.037*SL	0.101 + 0.037*SL
	t_{PLH}	0.236	0.156 + 0.040*SL	0.157 + 0.039*SL	0.161 + 0.039*SL
	t_{PHL}	0.145	0.105 + 0.020*SL	0.107 + 0.019*SL	0.109 + 0.019*SL
C to Y	t_R	0.480	0.320 + 0.080*SL	0.316 + 0.081*SL	0.330 + 0.080*SL
	t_F	0.182	0.110 + 0.036*SL	0.107 + 0.037*SL	0.101 + 0.037*SL
	t_{PLH}	0.259	0.179 + 0.040*SL	0.181 + 0.039*SL	0.186 + 0.039*SL
	t_{PHL}	0.145	0.106 + 0.020*SL	0.107 + 0.019*SL	0.110 + 0.019*SL
D to Y	t_R	0.495	0.337 + 0.079*SL	0.334 + 0.080*SL	0.332 + 0.080*SL
	t_F	0.248	0.185 + 0.031*SL	0.180 + 0.033*SL	0.173 + 0.033*SL
	t_{PLH}	0.364	0.284 + 0.040*SL	0.286 + 0.039*SL	0.290 + 0.039*SL
	t_{PHL}	0.210	0.171 + 0.019*SL	0.175 + 0.018*SL	0.180 + 0.018*SL
E to Y	t_R	0.495	0.337 + 0.079*SL	0.334 + 0.080*SL	0.332 + 0.080*SL
	t_F	0.274	0.211 + 0.032*SL	0.206 + 0.033*SL	0.201 + 0.033*SL
	t_{PLH}	0.381	0.301 + 0.040*SL	0.303 + 0.039*SL	0.307 + 0.039*SL
	t_{PHL}	0.225	0.186 + 0.019*SL	0.190 + 0.018*SL	0.197 + 0.018*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AO3111_LP

3-AND into 4-NOR with 1X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0
Other States						1

Cell Data

Input Load (SL)						Gate Count
AO3111_LP						*AO3111_LP*
A	B	C	D	E	F	
1.0	1.1	1.0	0.9	0.9	0.9	2.33

Switching Characteristics

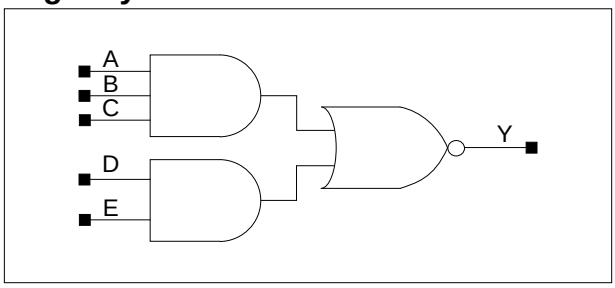
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO3111_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.553	0.337 + 0.108*SL	0.334 + 0.109*SL	0.371 + 0.106*SL
	t_F	0.222	0.132 + 0.045*SL	0.123 + 0.047*SL	0.117 + 0.048*SL
	t_{PLH}	0.228	0.125 + 0.052*SL	0.120 + 0.053*SL	0.126 + 0.052*SL
	t_{PHL}	0.164	0.114 + 0.025*SL	0.116 + 0.025*SL	0.118 + 0.025*SL
B to Y	t_R	0.583	0.366 + 0.108*SL	0.364 + 0.109*SL	0.400 + 0.107*SL
	t_F	0.220	0.128 + 0.046*SL	0.122 + 0.047*SL	0.117 + 0.048*SL
	t_{PLH}	0.253	0.148 + 0.053*SL	0.147 + 0.053*SL	0.152 + 0.052*SL
	t_{PHL}	0.168	0.117 + 0.025*SL	0.119 + 0.025*SL	0.122 + 0.025*SL
C to Y	t_R	0.611	0.395 + 0.108*SL	0.393 + 0.109*SL	0.428 + 0.107*SL
	t_F	0.218	0.125 + 0.047*SL	0.121 + 0.048*SL	0.117 + 0.048*SL
	t_{PLH}	0.276	0.169 + 0.053*SL	0.171 + 0.053*SL	0.176 + 0.052*SL
	t_{PHL}	0.167	0.116 + 0.025*SL	0.118 + 0.025*SL	0.121 + 0.025*SL
D to Y	t_R	0.650	0.440 + 0.105*SL	0.436 + 0.106*SL	0.432 + 0.106*SL
	t_F	0.281	0.201 + 0.040*SL	0.195 + 0.042*SL	0.192 + 0.042*SL
	t_{PLH}	0.426	0.319 + 0.053*SL	0.322 + 0.053*SL	0.325 + 0.052*SL
	t_{PHL}	0.247	0.199 + 0.024*SL	0.202 + 0.023*SL	0.208 + 0.023*SL
E to Y	t_R	0.651	0.441 + 0.105*SL	0.436 + 0.106*SL	0.432 + 0.106*SL
	t_F	0.314	0.232 + 0.041*SL	0.228 + 0.042*SL	0.227 + 0.042*SL
	t_{PLH}	0.470	0.364 + 0.053*SL	0.367 + 0.053*SL	0.370 + 0.052*SL
	t_{PHL}	0.269	0.221 + 0.024*SL	0.225 + 0.023*SL	0.234 + 0.023*SL
F to Y	t_R	0.651	0.441 + 0.105*SL	0.436 + 0.106*SL	0.432 + 0.106*SL
	t_F	0.342	0.258 + 0.042*SL	0.257 + 0.042*SL	0.261 + 0.042*SL
	t_{PLH}	0.489	0.382 + 0.053*SL	0.385 + 0.053*SL	0.388 + 0.052*SL
	t_{PHL}	0.284	0.233 + 0.025*SL	0.240 + 0.024*SL	0.253 + 0.023*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	1	x	x	0
x	x	x	1	1	0
Other States					1

Cell Data

Input Load (SL)										Gate Count	
AO32_LP					AO32D2_*LP*					*AO32_LP*	*AO32D2_LP*
A	B	C	D	E	A	B	C	D	E		
1.1	1.1	1.1	1.1	1.1	0.9	0.8	0.8	0.9	0.8	2.33	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO32_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.283	0.180 + 0.052*SL	0.171 + 0.054*SL	0.171 + 0.054*SL
	t_F	0.226	0.146 + 0.040*SL	0.136 + 0.043*SL	0.128 + 0.043*SL
	t_{PLH}	0.179	0.126 + 0.026*SL	0.127 + 0.026*SL	0.129 + 0.026*SL
	t_{PHL}	0.152	0.106 + 0.023*SL	0.108 + 0.022*SL	0.110 + 0.022*SL
B to Y	t_R	0.297	0.193 + 0.052*SL	0.185 + 0.054*SL	0.186 + 0.054*SL
	t_F	0.223	0.141 + 0.041*SL	0.135 + 0.043*SL	0.128 + 0.043*SL
	t_{PLH}	0.192	0.140 + 0.026*SL	0.141 + 0.026*SL	0.143 + 0.026*SL
	t_{PHL}	0.155	0.109 + 0.023*SL	0.111 + 0.022*SL	0.114 + 0.022*SL
C to Y	t_R	0.312	0.207 + 0.052*SL	0.200 + 0.054*SL	0.201 + 0.054*SL
	t_F	0.221	0.137 + 0.042*SL	0.133 + 0.043*SL	0.128 + 0.043*SL
	t_{PLH}	0.204	0.151 + 0.027*SL	0.153 + 0.026*SL	0.156 + 0.026*SL
	t_{PHL}	0.154	0.108 + 0.023*SL	0.110 + 0.022*SL	0.113 + 0.022*SL
D to Y	t_R	0.298	0.192 + 0.053*SL	0.189 + 0.054*SL	0.186 + 0.054*SL
	t_F	0.234	0.177 + 0.029*SL	0.171 + 0.030*SL	0.160 + 0.031*SL
	t_{PLH}	0.256	0.202 + 0.027*SL	0.204 + 0.026*SL	0.207 + 0.026*SL
	t_{PHL}	0.188	0.154 + 0.017*SL	0.157 + 0.016*SL	0.163 + 0.016*SL
E to Y	t_R	0.313	0.207 + 0.053*SL	0.205 + 0.054*SL	0.202 + 0.054*SL
	t_F	0.231	0.173 + 0.029*SL	0.168 + 0.030*SL	0.160 + 0.031*SL
	t_{PLH}	0.270	0.217 + 0.027*SL	0.219 + 0.026*SL	0.221 + 0.026*SL
	t_{PHL}	0.186	0.151 + 0.017*SL	0.155 + 0.016*SL	0.161 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

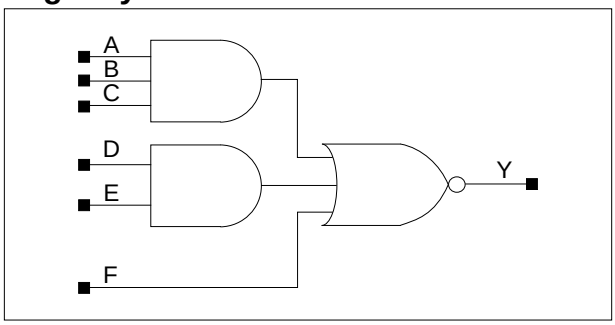
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO32D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.044 + 0.011*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.057	0.040 + 0.009*SL	0.042 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.287	0.273 + 0.007*SL	0.277 + 0.006*SL	0.279 + 0.006*SL
	t_{PHL}	0.319	0.304 + 0.007*SL	0.313 + 0.005*SL	0.321 + 0.005*SL
B to Y	t_R	0.065	0.040 + 0.012*SL	0.038 + 0.013*SL	0.028 + 0.013*SL
	t_F	0.056	0.038 + 0.009*SL	0.042 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.300	0.285 + 0.007*SL	0.289 + 0.006*SL	0.292 + 0.006*SL
	t_{PHL}	0.322	0.308 + 0.007*SL	0.315 + 0.005*SL	0.324 + 0.005*SL
C to Y	t_R	0.067	0.044 + 0.011*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.056	0.039 + 0.009*SL	0.042 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.311	0.296 + 0.007*SL	0.300 + 0.006*SL	0.303 + 0.006*SL
	t_{PHL}	0.322	0.307 + 0.007*SL	0.315 + 0.005*SL	0.324 + 0.005*SL
D to Y	t_R	0.067	0.044 + 0.011*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.057	0.040 + 0.008*SL	0.041 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.363	0.348 + 0.007*SL	0.352 + 0.006*SL	0.355 + 0.006*SL
	t_{PHL}	0.394	0.379 + 0.007*SL	0.387 + 0.005*SL	0.395 + 0.005*SL
E to Y	t_R	0.066	0.043 + 0.012*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.056	0.038 + 0.009*SL	0.041 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.374	0.359 + 0.007*SL	0.363 + 0.006*SL	0.366 + 0.006*SL
	t_{PHL}	0.390	0.376 + 0.007*SL	0.384 + 0.005*SL	0.392 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	x	0
x	x	x	x	x	1	0
Other States						1

Cell Data

Input Load (SL)						Gate Count
AO321_LP						*AO321_LP*
A	B	C	D	E	F	
1.1	1.1	1.1	1.0	1.1	1.0	2.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO321_LP

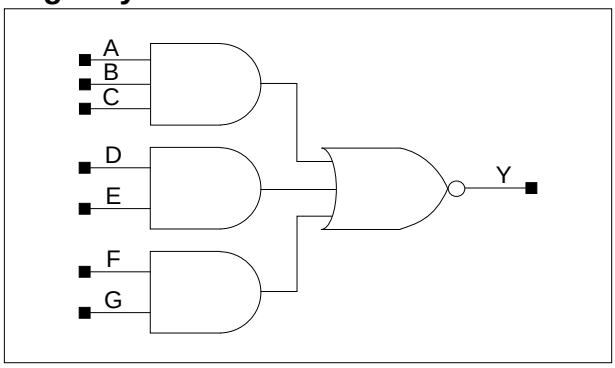
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.454	0.292 + 0.081*SL	0.288 + 0.082*SL	0.309 + 0.081*SL
	t_F	0.205	0.135 + 0.035*SL	0.127 + 0.037*SL	0.117 + 0.037*SL
	t_{PLH}	0.224	0.144 + 0.040*SL	0.144 + 0.040*SL	0.149 + 0.040*SL
	t_{PHL}	0.141	0.102 + 0.019*SL	0.103 + 0.019*SL	0.104 + 0.019*SL
B to Y	t_R	0.483	0.320 + 0.081*SL	0.317 + 0.082*SL	0.337 + 0.081*SL
	t_F	0.202	0.131 + 0.035*SL	0.125 + 0.037*SL	0.117 + 0.037*SL
	t_{PLH}	0.249	0.169 + 0.040*SL	0.170 + 0.040*SL	0.174 + 0.040*SL
	t_{PHL}	0.144	0.105 + 0.020*SL	0.107 + 0.019*SL	0.109 + 0.019*SL
C to Y	t_R	0.512	0.349 + 0.082*SL	0.346 + 0.082*SL	0.366 + 0.081*SL
	t_F	0.198	0.127 + 0.036*SL	0.123 + 0.037*SL	0.117 + 0.037*SL
	t_{PLH}	0.273	0.192 + 0.040*SL	0.194 + 0.040*SL	0.199 + 0.040*SL
	t_{PHL}	0.145	0.105 + 0.020*SL	0.107 + 0.019*SL	0.109 + 0.019*SL
D to Y	t_R	0.515	0.356 + 0.080*SL	0.351 + 0.081*SL	0.348 + 0.081*SL
	t_F	0.271	0.206 + 0.033*SL	0.200 + 0.034*SL	0.191 + 0.035*SL
	t_{PLH}	0.380	0.298 + 0.041*SL	0.301 + 0.040*SL	0.306 + 0.040*SL
	t_{PHL}	0.213	0.174 + 0.019*SL	0.177 + 0.019*SL	0.183 + 0.018*SL
E to Y	t_R	0.536	0.376 + 0.080*SL	0.372 + 0.081*SL	0.370 + 0.081*SL
	t_F	0.269	0.203 + 0.033*SL	0.198 + 0.034*SL	0.192 + 0.035*SL
	t_{PLH}	0.399	0.318 + 0.040*SL	0.321 + 0.040*SL	0.324 + 0.040*SL
	t_{PHL}	0.210	0.171 + 0.019*SL	0.175 + 0.019*SL	0.181 + 0.018*SL
F to Y	t_R	0.536	0.376 + 0.080*SL	0.372 + 0.081*SL	0.369 + 0.081*SL
	t_F	0.282	0.220 + 0.031*SL	0.217 + 0.032*SL	0.216 + 0.032*SL
	t_{PLH}	0.435	0.354 + 0.040*SL	0.356 + 0.040*SL	0.360 + 0.040*SL
	t_{PHL}	0.217	0.178 + 0.020*SL	0.183 + 0.018*SL	0.195 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AO322_LP

3-AND and Two 2-ANDs into 3-NOR with 1X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	x	x	x	x	0
x	x	x	1	1	x	x	0
x	x	x	x	x	1	1	0
Other States							1

Cell Data

Input Load (SL)							Gate Count
AO322_LP							*AO322_LP*
A	B	C	D	E	F	G	
1.1	1.1	1.1	1.0	1.0	1.1	1.1	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO322_LP

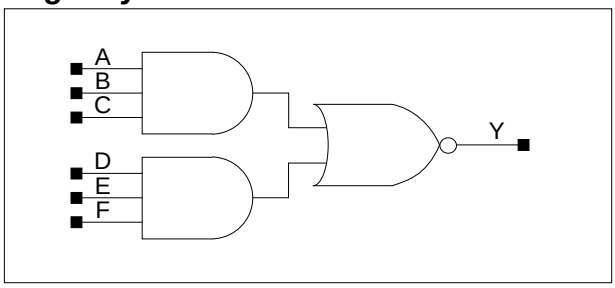
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.484	0.321 + 0.082*SL	0.317 + 0.082*SL	0.339 + 0.081*SL
	t_F	0.223	0.154 + 0.035*SL	0.145 + 0.037*SL	0.135 + 0.037*SL
	t_{PLH}	0.245	0.165 + 0.040*SL	0.165 + 0.040*SL	0.170 + 0.040*SL
	t_{PHL}	0.143	0.105 + 0.019*SL	0.105 + 0.019*SL	0.107 + 0.019*SL
B to Y	t_R	0.513	0.349 + 0.082*SL	0.347 + 0.082*SL	0.368 + 0.081*SL
	t_F	0.219	0.149 + 0.035*SL	0.143 + 0.037*SL	0.135 + 0.037*SL
	t_{PLH}	0.271	0.190 + 0.040*SL	0.192 + 0.040*SL	0.196 + 0.040*SL
	t_{PHL}	0.147	0.108 + 0.020*SL	0.109 + 0.019*SL	0.111 + 0.019*SL
C to Y	t_R	0.541	0.377 + 0.082*SL	0.376 + 0.082*SL	0.397 + 0.081*SL
	t_F	0.216	0.144 + 0.036*SL	0.141 + 0.037*SL	0.135 + 0.037*SL
	t_{PLH}	0.295	0.214 + 0.040*SL	0.216 + 0.040*SL	0.220 + 0.040*SL
	t_{PHL}	0.147	0.108 + 0.020*SL	0.109 + 0.019*SL	0.112 + 0.019*SL
D to Y	t_R	0.547	0.387 + 0.080*SL	0.384 + 0.081*SL	0.381 + 0.081*SL
	t_F	0.280	0.212 + 0.034*SL	0.206 + 0.035*SL	0.203 + 0.036*SL
	t_{PLH}	0.403	0.322 + 0.041*SL	0.325 + 0.040*SL	0.329 + 0.040*SL
	t_{PHL}	0.208	0.168 + 0.020*SL	0.172 + 0.019*SL	0.178 + 0.019*SL
E to Y	t_R	0.566	0.406 + 0.080*SL	0.403 + 0.081*SL	0.401 + 0.081*SL
	t_F	0.279	0.209 + 0.035*SL	0.207 + 0.035*SL	0.203 + 0.036*SL
	t_{PLH}	0.421	0.341 + 0.040*SL	0.343 + 0.040*SL	0.347 + 0.040*SL
	t_{PHL}	0.205	0.165 + 0.020*SL	0.169 + 0.019*SL	0.175 + 0.019*SL
F to Y	t_R	0.547	0.387 + 0.080*SL	0.384 + 0.081*SL	0.381 + 0.081*SL
	t_F	0.333	0.262 + 0.035*SL	0.261 + 0.035*SL	0.260 + 0.036*SL
	t_{PLH}	0.455	0.374 + 0.041*SL	0.376 + 0.040*SL	0.381 + 0.040*SL
	t_{PHL}	0.236	0.193 + 0.021*SL	0.200 + 0.020*SL	0.214 + 0.019*SL
G to Y	t_R	0.567	0.406 + 0.080*SL	0.403 + 0.081*SL	0.401 + 0.081*SL
	t_F	0.333	0.262 + 0.035*SL	0.262 + 0.035*SL	0.261 + 0.036*SL
	t_{PLH}	0.473	0.392 + 0.040*SL	0.395 + 0.040*SL	0.398 + 0.040*SL
	t_{PHL}	0.233	0.190 + 0.022*SL	0.197 + 0.020*SL	0.211 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AO33_LP

Two 3-ANDs into 2-NOR with 1X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
Other States						1

Cell Data

Input Load (SL)						Gate Count
AO33_LP						*AO33_LP*
A	B	C	D	E	F	
1.1	1.1	1.1	1.1	1.1	1.1	2.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO33_LP

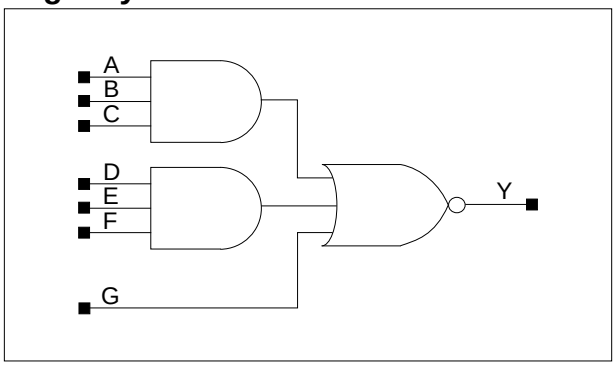
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.299	0.195 + 0.052*SL	0.187 + 0.054*SL	0.189 + 0.054*SL
	t_F	0.227	0.146 + 0.040*SL	0.137 + 0.043*SL	0.128 + 0.043*SL
	t_{PLH}	0.191	0.138 + 0.027*SL	0.140 + 0.026*SL	0.143 + 0.026*SL
	t_{PHL}	0.152	0.106 + 0.023*SL	0.107 + 0.022*SL	0.109 + 0.022*SL
B to Y	t_R	0.314	0.209 + 0.053*SL	0.202 + 0.054*SL	0.205 + 0.054*SL
	t_F	0.246	0.164 + 0.041*SL	0.156 + 0.043*SL	0.149 + 0.043*SL
	t_{PLH}	0.206	0.152 + 0.027*SL	0.154 + 0.026*SL	0.158 + 0.026*SL
	t_{PHL}	0.155	0.109 + 0.023*SL	0.111 + 0.022*SL	0.113 + 0.022*SL
C to Y	t_R	0.328	0.223 + 0.053*SL	0.217 + 0.054*SL	0.219 + 0.054*SL
	t_F	0.221	0.137 + 0.042*SL	0.133 + 0.043*SL	0.128 + 0.043*SL
	t_{PLH}	0.218	0.164 + 0.027*SL	0.166 + 0.026*SL	0.170 + 0.026*SL
	t_{PHL}	0.154	0.108 + 0.023*SL	0.110 + 0.022*SL	0.113 + 0.022*SL
D to Y	t_R	0.300	0.194 + 0.053*SL	0.191 + 0.054*SL	0.188 + 0.054*SL
	t_F	0.329	0.246 + 0.042*SL	0.240 + 0.043*SL	0.235 + 0.043*SL
	t_{PLH}	0.261	0.207 + 0.027*SL	0.209 + 0.026*SL	0.213 + 0.026*SL
	t_{PHL}	0.248	0.200 + 0.024*SL	0.204 + 0.023*SL	0.212 + 0.022*SL
E to Y	t_R	0.316	0.209 + 0.053*SL	0.207 + 0.054*SL	0.204 + 0.054*SL
	t_F	0.329	0.245 + 0.042*SL	0.240 + 0.043*SL	0.235 + 0.043*SL
	t_{PLH}	0.276	0.222 + 0.027*SL	0.224 + 0.026*SL	0.227 + 0.026*SL
	t_{PHL}	0.253	0.206 + 0.024*SL	0.210 + 0.023*SL	0.217 + 0.022*SL
F to Y	t_R	0.331	0.225 + 0.053*SL	0.223 + 0.054*SL	0.221 + 0.054*SL
	t_F	0.328	0.243 + 0.042*SL	0.240 + 0.043*SL	0.235 + 0.043*SL
	t_{PLH}	0.289	0.235 + 0.027*SL	0.238 + 0.026*SL	0.241 + 0.026*SL
	t_{PHL}	0.254	0.206 + 0.024*SL	0.210 + 0.023*SL	0.218 + 0.022*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

AO331_LP

Two 3-ANDs into 3-NOR with 1X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
1	1	1	x	x	x	x	0
x	x	x	1	1	1	x	0
x	x	x	x	x	x	1	0
Other States							1

Cell Data

Input Load (SL)							Gate Count
AO331_LP							*AO331_LP*
A	B	C	D	E	F	G	
1.1	1.1	1.1	1.1	1.1	1.1	1.0	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO331_LP

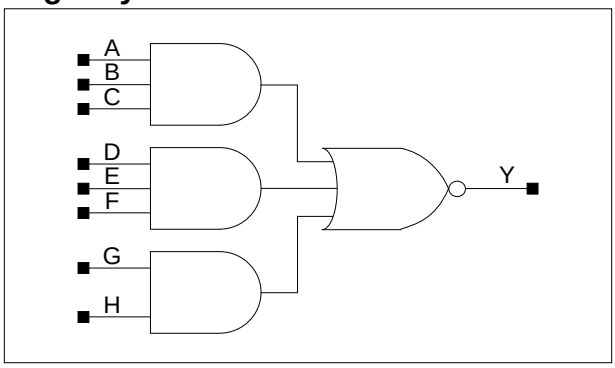
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.480	0.318 + 0.081*SL	0.314 + 0.082*SL	0.338 + 0.081*SL
	t_F	0.233	0.152 + 0.041*SL	0.143 + 0.043*SL	0.134 + 0.043*SL
	t_{PLH}	0.238	0.158 + 0.040*SL	0.159 + 0.040*SL	0.165 + 0.039*SL
	t_{PHL}	0.156	0.111 + 0.023*SL	0.112 + 0.022*SL	0.114 + 0.022*SL
B to Y	t_R	0.504	0.341 + 0.082*SL	0.338 + 0.082*SL	0.362 + 0.081*SL
	t_F	0.230	0.147 + 0.041*SL	0.141 + 0.043*SL	0.134 + 0.043*SL
	t_{PLH}	0.260	0.180 + 0.040*SL	0.181 + 0.040*SL	0.186 + 0.040*SL
	t_{PHL}	0.160	0.114 + 0.023*SL	0.115 + 0.022*SL	0.118 + 0.022*SL
C to Y	t_R	0.527	0.364 + 0.082*SL	0.362 + 0.082*SL	0.385 + 0.081*SL
	t_F	0.227	0.143 + 0.042*SL	0.140 + 0.043*SL	0.134 + 0.043*SL
	t_{PLH}	0.279	0.198 + 0.040*SL	0.200 + 0.040*SL	0.206 + 0.039*SL
	t_{PHL}	0.159	0.114 + 0.023*SL	0.115 + 0.022*SL	0.118 + 0.022*SL
D to Y	t_R	0.514	0.355 + 0.080*SL	0.350 + 0.081*SL	0.345 + 0.081*SL
	t_F	0.341	0.256 + 0.042*SL	0.251 + 0.044*SL	0.246 + 0.044*SL
	t_{PLH}	0.381	0.299 + 0.041*SL	0.302 + 0.040*SL	0.307 + 0.040*SL
	t_{PHL}	0.259	0.211 + 0.024*SL	0.215 + 0.023*SL	0.222 + 0.023*SL
E to Y	t_R	0.537	0.377 + 0.080*SL	0.374 + 0.081*SL	0.370 + 0.081*SL
	t_F	0.341	0.256 + 0.043*SL	0.252 + 0.044*SL	0.246 + 0.044*SL
	t_{PLH}	0.404	0.322 + 0.041*SL	0.325 + 0.040*SL	0.329 + 0.040*SL
	t_{PHL}	0.264	0.215 + 0.024*SL	0.219 + 0.023*SL	0.227 + 0.023*SL
F to Y	t_R	0.558	0.399 + 0.080*SL	0.395 + 0.080*SL	0.391 + 0.081*SL
	t_F	0.341	0.255 + 0.043*SL	0.251 + 0.044*SL	0.246 + 0.044*SL
	t_{PLH}	0.422	0.342 + 0.040*SL	0.345 + 0.040*SL	0.349 + 0.039*SL
	t_{PHL}	0.265	0.216 + 0.024*SL	0.220 + 0.023*SL	0.228 + 0.023*SL
G to Y	t_R	0.558	0.399 + 0.079*SL	0.395 + 0.080*SL	0.391 + 0.081*SL
	t_F	0.310	0.244 + 0.033*SL	0.242 + 0.034*SL	0.243 + 0.034*SL
	t_{PLH}	0.467	0.387 + 0.040*SL	0.390 + 0.040*SL	0.394 + 0.039*SL
	t_{PHL}	0.235	0.192 + 0.021*SL	0.199 + 0.019*SL	0.214 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

AO332_LP

Two 3-ANDs and 2-AND into 3-NOR with 1X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	1	x	x	x	x	x	0
x	x	x	1	1	1	x	x	0
x	x	x	x	x	x	1	1	0
Other States								1

Cell Data

Input Load (SL)								Gate Count
AO332_LP								*AO332_LP*
A	B	C	D	E	F	G	H	
1.1	1.1	1.1	1.1	1.1	1.1	1.0	1.1	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

AO332_LP

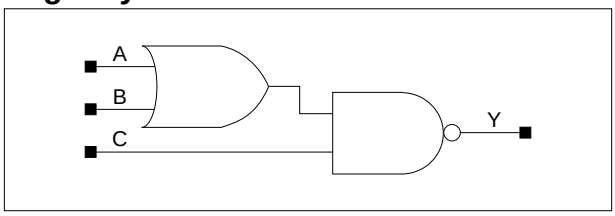
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.493	0.329 + 0.082*SL	0.326 + 0.083*SL	0.351 + 0.081*SL
	t_F	0.255	0.174 + 0.041*SL	0.165 + 0.043*SL	0.157 + 0.043*SL
	t_{PLH}	0.241	0.162 + 0.040*SL	0.161 + 0.040*SL	0.167 + 0.040*SL
	t_{PHL}	0.160	0.115 + 0.022*SL	0.115 + 0.022*SL	0.117 + 0.022*SL
B to Y	t_R	0.517	0.353 + 0.082*SL	0.350 + 0.083*SL	0.375 + 0.081*SL
	t_F	0.252	0.169 + 0.042*SL	0.163 + 0.043*SL	0.157 + 0.043*SL
	t_{PLH}	0.263	0.183 + 0.040*SL	0.184 + 0.040*SL	0.189 + 0.040*SL
	t_{PHL}	0.163	0.118 + 0.023*SL	0.118 + 0.022*SL	0.121 + 0.022*SL
C to Y	t_R	0.540	0.376 + 0.082*SL	0.374 + 0.083*SL	0.398 + 0.081*SL
	t_F	0.272	0.188 + 0.042*SL	0.183 + 0.043*SL	0.178 + 0.043*SL
	t_{PLH}	0.282	0.201 + 0.040*SL	0.203 + 0.040*SL	0.208 + 0.040*SL
	t_{PHL}	0.162	0.117 + 0.023*SL	0.118 + 0.022*SL	0.121 + 0.022*SL
D to Y	t_R	0.546	0.386 + 0.080*SL	0.383 + 0.081*SL	0.379 + 0.081*SL
	t_F	0.351	0.265 + 0.043*SL	0.262 + 0.044*SL	0.259 + 0.044*SL
	t_{PLH}	0.404	0.323 + 0.041*SL	0.326 + 0.040*SL	0.331 + 0.040*SL
	t_{PHL}	0.248	0.199 + 0.024*SL	0.203 + 0.023*SL	0.211 + 0.023*SL
E to Y	t_R	0.569	0.409 + 0.080*SL	0.406 + 0.081*SL	0.402 + 0.081*SL
	t_F	0.351	0.265 + 0.043*SL	0.262 + 0.044*SL	0.259 + 0.044*SL
	t_{PLH}	0.427	0.346 + 0.041*SL	0.348 + 0.040*SL	0.353 + 0.040*SL
	t_{PHL}	0.252	0.203 + 0.025*SL	0.208 + 0.023*SL	0.216 + 0.023*SL
F to Y	t_R	0.590	0.430 + 0.080*SL	0.427 + 0.080*SL	0.424 + 0.081*SL
	t_F	0.351	0.264 + 0.043*SL	0.262 + 0.044*SL	0.259 + 0.044*SL
	t_{PLH}	0.446	0.365 + 0.040*SL	0.368 + 0.040*SL	0.372 + 0.039*SL
	t_{PHL}	0.253	0.204 + 0.025*SL	0.209 + 0.023*SL	0.217 + 0.023*SL
G to Y	t_R	0.574	0.414 + 0.080*SL	0.411 + 0.081*SL	0.407 + 0.081*SL
	t_F	0.354	0.282 + 0.036*SL	0.280 + 0.036*SL	0.282 + 0.036*SL
	t_{PLH}	0.491	0.409 + 0.041*SL	0.413 + 0.040*SL	0.418 + 0.040*SL
	t_{PHL}	0.246	0.201 + 0.022*SL	0.209 + 0.020*SL	0.226 + 0.019*SL
H to Y	t_R	0.590	0.431 + 0.080*SL	0.428 + 0.080*SL	0.424 + 0.081*SL
	t_F	0.354	0.282 + 0.036*SL	0.282 + 0.036*SL	0.282 + 0.036*SL
	t_{PLH}	0.508	0.427 + 0.040*SL	0.430 + 0.040*SL	0.434 + 0.039*SL
	t_{PHL}	0.243	0.199 + 0.022*SL	0.207 + 0.020*SL	0.223 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OA21_LP/OA21D2_LP/OA21D4_LP

2-OR into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	x	1
x	x	0	1
Others States			0

Cell Data

Input Load (SL)								
OA21_LP			*OA21D2_LP*			*OA21D4_LP*		
A	B	C	A	B	C	A	B	C
1.1	1.1	1.1	2.2	2.1	2.2	1.0	0.9	1.0
Gate Count								
OA21_LP			*OA21D2_LP*			*OA21D4_LP*		
1.33			2.33			3.00		

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA21_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.221	0.122 + 0.049*SL	0.109 + 0.053*SL	0.100 + 0.053*SL
	t_F	0.140	0.083 + 0.028*SL	0.071 + 0.031*SL	0.053 + 0.032*SL
	t_{PLH}	0.151	0.099 + 0.026*SL	0.099 + 0.026*SL	0.101 + 0.026*SL
	t_{PHL}	0.112	0.076 + 0.018*SL	0.081 + 0.017*SL	0.083 + 0.017*SL
B to Y	t_R	0.213	0.110 + 0.051*SL	0.103 + 0.053*SL	0.100 + 0.053*SL
	t_F	0.164	0.106 + 0.029*SL	0.095 + 0.032*SL	0.081 + 0.032*SL
	t_{PLH}	0.172	0.120 + 0.026*SL	0.121 + 0.026*SL	0.123 + 0.026*SL
	t_{PHL}	0.133	0.098 + 0.018*SL	0.101 + 0.017*SL	0.104 + 0.017*SL
C to Y	t_R	0.134	0.088 + 0.023*SL	0.079 + 0.025*SL	0.059 + 0.027*SL
	t_F	0.155	0.093 + 0.031*SL	0.089 + 0.032*SL	0.081 + 0.032*SL
	t_{PLH}	0.121	0.095 + 0.013*SL	0.097 + 0.012*SL	0.098 + 0.012*SL
	t_{PHL}	0.138	0.102 + 0.018*SL	0.105 + 0.017*SL	0.110 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA21D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.173	0.125 + 0.024*SL	0.118 + 0.026*SL	0.101 + 0.027*SL
	t_F	0.111	0.085 + 0.013*SL	0.078 + 0.015*SL	0.062 + 0.016*SL
	t_{PLH}	0.125	0.099 + 0.013*SL	0.099 + 0.013*SL	0.100 + 0.013*SL
	t_{PHL}	0.094	0.073 + 0.010*SL	0.080 + 0.008*SL	0.082 + 0.008*SL
B to Y	t_R	0.162	0.112 + 0.025*SL	0.107 + 0.026*SL	0.101 + 0.027*SL
	t_F	0.135	0.107 + 0.014*SL	0.102 + 0.015*SL	0.089 + 0.016*SL
	t_{PLH}	0.146	0.120 + 0.013*SL	0.121 + 0.013*SL	0.122 + 0.013*SL
	t_{PHL}	0.116	0.098 + 0.009*SL	0.100 + 0.009*SL	0.103 + 0.009*SL
C to Y	t_R	0.113	0.093 + 0.010*SL	0.085 + 0.012*SL	0.070 + 0.013*SL
	t_F	0.126	0.095 + 0.015*SL	0.094 + 0.016*SL	0.085 + 0.016*SL
	t_{PLH}	0.107	0.092 + 0.007*SL	0.096 + 0.006*SL	0.097 + 0.006*SL
	t_{PHL}	0.119	0.101 + 0.009*SL	0.103 + 0.009*SL	0.107 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OA21D4_LP

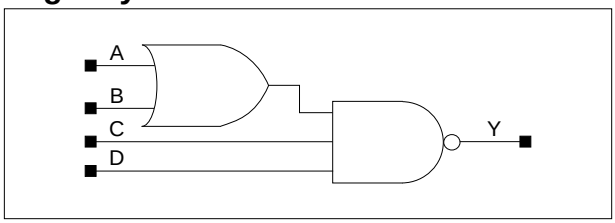
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.053 + 0.007*SL	0.054 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.057	0.048 + 0.004*SL	0.049 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.298	0.289 + 0.005*SL	0.294 + 0.003*SL	0.303 + 0.003*SL
	t_{PHL}	0.245	0.236 + 0.005*SL	0.242 + 0.003*SL	0.259 + 0.002*SL
B to Y	t_R	0.066	0.055 + 0.006*SL	0.052 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.056	0.046 + 0.005*SL	0.050 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.320	0.311 + 0.005*SL	0.316 + 0.003*SL	0.325 + 0.003*SL
	t_{PHL}	0.267	0.258 + 0.005*SL	0.264 + 0.003*SL	0.282 + 0.002*SL
C to Y	t_R	0.066	0.054 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.057	0.046 + 0.005*SL	0.051 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.263	0.253 + 0.005*SL	0.259 + 0.003*SL	0.267 + 0.003*SL
	t_{PHL}	0.270	0.261 + 0.005*SL	0.267 + 0.003*SL	0.284 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

OA211_LP/OA211D2_LP/OA211D4_LP

2-OR into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)											
OA211_LP				*OA211D2_LP*				*OA211D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.1	0.9	0.9	2.3	2.2	1.9	1.8	0.9	0.9	0.9	1.0

Gate Count		
OA211_LP	*OA211D2_LP*	*OA211D4_LP*
1.67	3.00	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA211_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.242	0.143 + 0.050*SL	0.131 + 0.053*SL	0.124 + 0.053*SL
	t_F	0.176	0.107 + 0.034*SL	0.097 + 0.037*SL	0.085 + 0.038*SL
	t_{PLH}	0.163	0.111 + 0.026*SL	0.112 + 0.026*SL	0.114 + 0.026*SL
	t_{PHL}	0.129	0.089 + 0.020*SL	0.091 + 0.019*SL	0.093 + 0.019*SL
B to Y	t_R	0.235	0.131 + 0.052*SL	0.127 + 0.053*SL	0.124 + 0.053*SL
	t_F	0.204	0.134 + 0.035*SL	0.125 + 0.037*SL	0.115 + 0.038*SL
	t_{PLH}	0.183	0.130 + 0.026*SL	0.131 + 0.026*SL	0.134 + 0.026*SL
	t_{PHL}	0.151	0.111 + 0.020*SL	0.113 + 0.020*SL	0.116 + 0.019*SL
C to Y	t_R	0.191	0.122 + 0.034*SL	0.112 + 0.037*SL	0.101 + 0.037*SL
	t_F	0.199	0.127 + 0.036*SL	0.122 + 0.037*SL	0.115 + 0.038*SL
	t_{PLH}	0.157	0.121 + 0.018*SL	0.122 + 0.018*SL	0.124 + 0.017*SL
	t_{PHL}	0.162	0.122 + 0.020*SL	0.124 + 0.020*SL	0.128 + 0.019*SL
D to Y	t_R	0.202	0.132 + 0.035*SL	0.124 + 0.037*SL	0.114 + 0.037*SL
	t_F	0.197	0.123 + 0.037*SL	0.120 + 0.038*SL	0.115 + 0.038*SL
	t_{PLH}	0.166	0.131 + 0.018*SL	0.132 + 0.018*SL	0.134 + 0.017*SL
	t_{PHL}	0.161	0.121 + 0.020*SL	0.123 + 0.020*SL	0.127 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA211D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.193	0.145 + 0.024*SL	0.139 + 0.026*SL	0.125 + 0.027*SL
	t_F	0.141	0.108 + 0.017*SL	0.103 + 0.018*SL	0.089 + 0.019*SL
	t_{PLH}	0.137	0.111 + 0.013*SL	0.111 + 0.013*SL	0.113 + 0.013*SL
	t_{PHL}	0.108	0.088 + 0.010*SL	0.090 + 0.010*SL	0.092 + 0.010*SL
B to Y	t_R	0.184	0.133 + 0.026*SL	0.130 + 0.026*SL	0.125 + 0.027*SL
	t_F	0.170	0.136 + 0.017*SL	0.132 + 0.018*SL	0.119 + 0.019*SL
	t_{PLH}	0.157	0.130 + 0.013*SL	0.131 + 0.013*SL	0.133 + 0.013*SL
	t_{PHL}	0.131	0.111 + 0.010*SL	0.112 + 0.010*SL	0.115 + 0.010*SL
C to Y	t_R	0.158	0.125 + 0.016*SL	0.119 + 0.018*SL	0.106 + 0.019*SL
	t_F	0.163	0.128 + 0.018*SL	0.125 + 0.018*SL	0.118 + 0.019*SL
	t_{PLH}	0.140	0.122 + 0.009*SL	0.123 + 0.009*SL	0.124 + 0.009*SL
	t_{PHL}	0.143	0.122 + 0.010*SL	0.123 + 0.010*SL	0.127 + 0.010*SL
D to Y	t_R	0.169	0.135 + 0.017*SL	0.130 + 0.018*SL	0.118 + 0.019*SL
	t_F	0.160	0.124 + 0.018*SL	0.122 + 0.019*SL	0.118 + 0.019*SL
	t_{PLH}	0.149	0.131 + 0.009*SL	0.132 + 0.009*SL	0.133 + 0.009*SL
	t_{PHL}	0.142	0.121 + 0.010*SL	0.122 + 0.010*SL	0.126 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OA211D4_LP

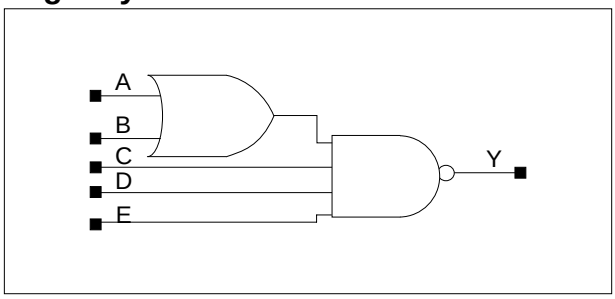
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.068	0.057 + 0.006*SL	0.055 + 0.006*SL	0.041 + 0.006*SL
	t_F	0.058	0.047 + 0.006*SL	0.053 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.326	0.316 + 0.005*SL	0.322 + 0.003*SL	0.331 + 0.003*SL
	t_{PHL}	0.300	0.290 + 0.005*SL	0.297 + 0.003*SL	0.315 + 0.002*SL
B to Y	t_R	0.066	0.053 + 0.007*SL	0.056 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.059	0.050 + 0.005*SL	0.052 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.345	0.335 + 0.005*SL	0.342 + 0.003*SL	0.350 + 0.003*SL
	t_{PHL}	0.326	0.317 + 0.005*SL	0.324 + 0.003*SL	0.341 + 0.002*SL
C to Y	t_R	0.064	0.052 + 0.006*SL	0.053 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.059	0.049 + 0.005*SL	0.052 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.277	0.267 + 0.005*SL	0.273 + 0.003*SL	0.281 + 0.003*SL
	t_{PHL}	0.338	0.329 + 0.005*SL	0.336 + 0.003*SL	0.354 + 0.002*SL
D to Y	t_R	0.065	0.052 + 0.006*SL	0.054 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.059	0.050 + 0.005*SL	0.051 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.283	0.273 + 0.005*SL	0.279 + 0.003*SL	0.288 + 0.003*SL
	t_{PHL}	0.338	0.328 + 0.005*SL	0.335 + 0.003*SL	0.353 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

OA2111_LP/OA2111D2_LP

2-OR into 4-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)										Gate Count	
OA2111_LP					*OA2111D2_LP*					*OA2111_LP*	*OA2111D2_LP*
A	B	C	D	E	A	B	C	D	E		
1.1	1.1	0.9	0.9	0.9	2.2	2.3	1.9	1.9	1.8	2.00	3.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA2111_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.253	0.153 + 0.050*SL	0.142 + 0.053*SL	0.136 + 0.053*SL
	t_F	0.233	0.141 + 0.046*SL	0.133 + 0.048*SL	0.128 + 0.048*SL
	t_{PLH}	0.169	0.117 + 0.026*SL	0.118 + 0.026*SL	0.121 + 0.026*SL
	t_{PHL}	0.153	0.103 + 0.025*SL	0.104 + 0.025*SL	0.106 + 0.025*SL
B to Y	t_R	0.247	0.144 + 0.052*SL	0.139 + 0.053*SL	0.137 + 0.053*SL
	t_F	0.271	0.178 + 0.047*SL	0.170 + 0.048*SL	0.167 + 0.049*SL
	t_{PLH}	0.189	0.137 + 0.026*SL	0.138 + 0.026*SL	0.140 + 0.026*SL
	t_{PHL}	0.183	0.131 + 0.026*SL	0.134 + 0.025*SL	0.137 + 0.025*SL
C to Y	t_R	0.198	0.129 + 0.035*SL	0.120 + 0.037*SL	0.111 + 0.037*SL
	t_F	0.270	0.175 + 0.047*SL	0.171 + 0.048*SL	0.167 + 0.049*SL
	t_{PLH}	0.162	0.126 + 0.018*SL	0.127 + 0.018*SL	0.129 + 0.017*SL
	t_{PHL}	0.203	0.151 + 0.026*SL	0.154 + 0.025*SL	0.158 + 0.025*SL
D to Y	t_R	0.209	0.139 + 0.035*SL	0.131 + 0.037*SL	0.123 + 0.037*SL
	t_F	0.268	0.173 + 0.048*SL	0.169 + 0.049*SL	0.167 + 0.049*SL
	t_{PLH}	0.172	0.135 + 0.018*SL	0.137 + 0.018*SL	0.139 + 0.017*SL
	t_{PHL}	0.209	0.158 + 0.026*SL	0.161 + 0.025*SL	0.165 + 0.025*SL
E to Y	t_R	0.221	0.151 + 0.035*SL	0.143 + 0.037*SL	0.136 + 0.037*SL
	t_F	0.267	0.171 + 0.048*SL	0.169 + 0.049*SL	0.167 + 0.049*SL
	t_{PLH}	0.180	0.143 + 0.018*SL	0.145 + 0.018*SL	0.149 + 0.018*SL
	t_{PHL}	0.211	0.160 + 0.026*SL	0.163 + 0.025*SL	0.167 + 0.025*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA2111D2_LP

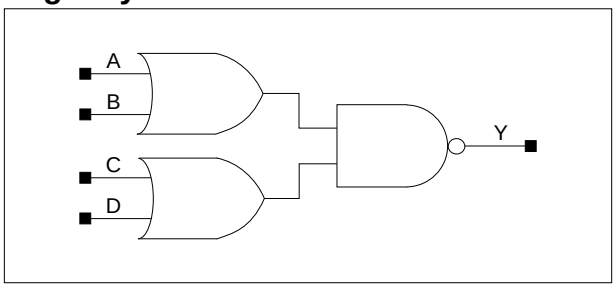
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.203	0.155 + 0.024*SL	0.148 + 0.026*SL	0.136 + 0.027*SL
	t_F	0.188	0.143 + 0.022*SL	0.138 + 0.024*SL	0.127 + 0.024*SL
	t_{PLH}	0.143	0.117 + 0.013*SL	0.117 + 0.013*SL	0.119 + 0.013*SL
	t_{PHL}	0.128	0.103 + 0.012*SL	0.103 + 0.012*SL	0.105 + 0.012*SL
B to Y	t_R	0.195	0.144 + 0.026*SL	0.141 + 0.026*SL	0.136 + 0.027*SL
	t_F	0.222	0.176 + 0.023*SL	0.173 + 0.023*SL	0.164 + 0.024*SL
	t_{PLH}	0.163	0.136 + 0.013*SL	0.137 + 0.013*SL	0.139 + 0.013*SL
	t_{PHL}	0.154	0.129 + 0.013*SL	0.130 + 0.012*SL	0.133 + 0.012*SL
C to Y	t_R	0.165	0.131 + 0.017*SL	0.127 + 0.018*SL	0.114 + 0.019*SL
	t_F	0.219	0.173 + 0.023*SL	0.170 + 0.024*SL	0.165 + 0.024*SL
	t_{PLH}	0.146	0.128 + 0.009*SL	0.129 + 0.009*SL	0.130 + 0.009*SL
	t_{PHL}	0.177	0.151 + 0.013*SL	0.153 + 0.012*SL	0.157 + 0.012*SL
D to Y	t_R	0.175	0.140 + 0.017*SL	0.137 + 0.018*SL	0.126 + 0.019*SL
	t_F	0.218	0.171 + 0.023*SL	0.170 + 0.024*SL	0.165 + 0.024*SL
	t_{PLH}	0.154	0.136 + 0.009*SL	0.137 + 0.009*SL	0.139 + 0.009*SL
	t_{PHL}	0.182	0.156 + 0.013*SL	0.158 + 0.012*SL	0.162 + 0.012*SL
E to Y	t_R	0.187	0.152 + 0.017*SL	0.149 + 0.018*SL	0.138 + 0.019*SL
	t_F	0.217	0.170 + 0.023*SL	0.169 + 0.024*SL	0.165 + 0.024*SL
	t_{PLH}	0.162	0.143 + 0.009*SL	0.144 + 0.009*SL	0.147 + 0.009*SL
	t_{PHL}	0.183	0.158 + 0.013*SL	0.159 + 0.012*SL	0.163 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OA22_LP/OA22D2_LP/OA22D4_LP

Two 2-ORs into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
Other States				0

Cell Data

Input Load (SL)											
OA22_LP				*OA22D2_LP*				*OA22D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.1	1.1	1.1	2.1	2.2	2.1	2.2	1.0	0.9	1.0	1.0

Gate Count		
OA22_LP	*OA22D2_LP*	*OA22D4_LP*
1.67	3.00	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA22_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.298	0.200 + 0.049*SL	0.185 + 0.052*SL	0.173 + 0.053*SL
	t_F	0.166	0.104 + 0.031*SL	0.096 + 0.033*SL	0.085 + 0.034*SL
	t_{PLH}	0.153	0.101 + 0.026*SL	0.101 + 0.026*SL	0.103 + 0.026*SL
	t_{PHL}	0.141	0.105 + 0.018*SL	0.107 + 0.018*SL	0.111 + 0.017*SL
B to Y	t_R	0.289	0.188 + 0.051*SL	0.180 + 0.053*SL	0.173 + 0.053*SL
	t_F	0.189	0.127 + 0.031*SL	0.120 + 0.033*SL	0.111 + 0.033*SL
	t_{PLH}	0.174	0.122 + 0.026*SL	0.122 + 0.026*SL	0.124 + 0.026*SL
	t_{PHL}	0.160	0.123 + 0.019*SL	0.127 + 0.018*SL	0.132 + 0.017*SL
C to Y	t_R	0.254	0.153 + 0.050*SL	0.143 + 0.053*SL	0.139 + 0.053*SL
	t_F	0.160	0.096 + 0.032*SL	0.091 + 0.033*SL	0.085 + 0.033*SL
	t_{PLH}	0.184	0.131 + 0.026*SL	0.133 + 0.026*SL	0.135 + 0.026*SL
	t_{PHL}	0.148	0.111 + 0.019*SL	0.114 + 0.018*SL	0.119 + 0.017*SL
D to Y	t_R	0.248	0.144 + 0.052*SL	0.140 + 0.053*SL	0.139 + 0.053*SL
	t_F	0.184	0.119 + 0.032*SL	0.116 + 0.033*SL	0.111 + 0.033*SL
	t_{PLH}	0.205	0.153 + 0.026*SL	0.155 + 0.026*SL	0.157 + 0.026*SL
	t_{PHL}	0.168	0.131 + 0.019*SL	0.135 + 0.018*SL	0.140 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA22D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.249	0.202 + 0.023*SL	0.193 + 0.025*SL	0.173 + 0.027*SL
	t_F	0.134	0.103 + 0.015*SL	0.100 + 0.016*SL	0.088 + 0.017*SL
	t_{PLH}	0.125	0.099 + 0.013*SL	0.100 + 0.013*SL	0.101 + 0.013*SL
	t_{PHL}	0.122	0.103 + 0.009*SL	0.104 + 0.009*SL	0.109 + 0.009*SL
B to Y	t_R	0.237	0.188 + 0.025*SL	0.182 + 0.026*SL	0.174 + 0.027*SL
	t_F	0.156	0.124 + 0.016*SL	0.124 + 0.016*SL	0.114 + 0.017*SL
	t_{PLH}	0.147	0.121 + 0.013*SL	0.121 + 0.013*SL	0.122 + 0.013*SL
	t_{PHL}	0.141	0.122 + 0.010*SL	0.124 + 0.009*SL	0.128 + 0.009*SL
C to Y	t_R	0.200	0.151 + 0.025*SL	0.145 + 0.026*SL	0.133 + 0.027*SL
	t_F	0.127	0.095 + 0.016*SL	0.093 + 0.016*SL	0.086 + 0.017*SL
	t_{PLH}	0.155	0.129 + 0.013*SL	0.129 + 0.013*SL	0.131 + 0.013*SL
	t_{PHL}	0.127	0.108 + 0.010*SL	0.110 + 0.009*SL	0.115 + 0.009*SL
D to Y	t_R	0.192	0.141 + 0.026*SL	0.138 + 0.026*SL	0.133 + 0.027*SL
	t_F	0.151	0.119 + 0.016*SL	0.118 + 0.016*SL	0.113 + 0.017*SL
	t_{PLH}	0.177	0.150 + 0.013*SL	0.151 + 0.013*SL	0.153 + 0.013*SL
	t_{PHL}	0.147	0.128 + 0.010*SL	0.131 + 0.009*SL	0.136 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OA22D4_LP

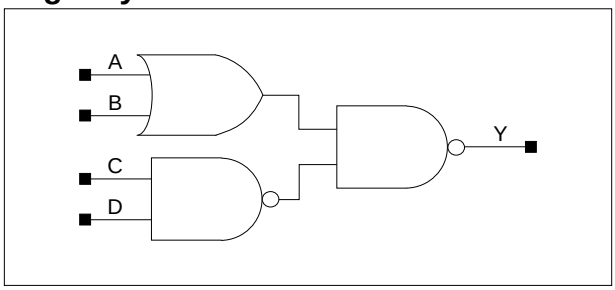
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.071	0.059 + 0.006*SL	0.060 + 0.006*SL	0.043 + 0.006*SL
	t_F	0.056	0.046 + 0.005*SL	0.049 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.321	0.311 + 0.005*SL	0.317 + 0.003*SL	0.327 + 0.003*SL
	t_{PHL}	0.270	0.260 + 0.005*SL	0.267 + 0.003*SL	0.284 + 0.002*SL
B to Y	t_R	0.071	0.059 + 0.006*SL	0.060 + 0.006*SL	0.043 + 0.006*SL
	t_F	0.056	0.046 + 0.005*SL	0.051 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.342	0.332 + 0.005*SL	0.338 + 0.003*SL	0.348 + 0.003*SL
	t_{PHL}	0.291	0.282 + 0.005*SL	0.289 + 0.003*SL	0.305 + 0.002*SL
C to Y	t_R	0.071	0.060 + 0.005*SL	0.058 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.056	0.046 + 0.005*SL	0.050 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.352	0.342 + 0.005*SL	0.348 + 0.003*SL	0.358 + 0.003*SL
	t_{PHL}	0.275	0.266 + 0.005*SL	0.273 + 0.003*SL	0.289 + 0.002*SL
D to Y	t_R	0.071	0.060 + 0.005*SL	0.058 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.057	0.047 + 0.005*SL	0.050 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.373	0.363 + 0.005*SL	0.370 + 0.003*SL	0.379 + 0.003*SL
	t_{PHL}	0.295	0.286 + 0.005*SL	0.292 + 0.003*SL	0.309 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

OA22A_LP/OA22D2A_LP/OA22D4A_LP

2-OR and 2-NAND into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
Other States				0

Cell Data

Input Load (SL)											
OA22A_LP				*OA22D2A_LP*				*OA22D4A_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
1.1	1.1	0.9	1.0	2.2	2.1	0.9	1.0	1.1	1.1	1.0	1.0

Gate Count		
OA22A_LP	*OA22D2A_LP*	*OA22D4A_LP*
2.00	3.00	4.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA22A_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.223	0.124 + 0.050*SL	0.110 + 0.053*SL	0.102 + 0.054*SL
	t_F	0.140	0.084 + 0.028*SL	0.072 + 0.031*SL	0.055 + 0.032*SL
	t_{PLH}	0.152	0.100 + 0.026*SL	0.100 + 0.026*SL	0.102 + 0.026*SL
	t_{PHL}	0.112	0.076 + 0.018*SL	0.081 + 0.017*SL	0.083 + 0.017*SL
B to Y	t_R	0.215	0.111 + 0.052*SL	0.105 + 0.053*SL	0.101 + 0.054*SL
	t_F	0.163	0.106 + 0.029*SL	0.096 + 0.031*SL	0.081 + 0.032*SL
	t_{PLH}	0.173	0.121 + 0.026*SL	0.122 + 0.026*SL	0.123 + 0.026*SL
	t_{PHL}	0.133	0.097 + 0.018*SL	0.100 + 0.017*SL	0.104 + 0.017*SL
C to Y	t_R	0.123	0.072 + 0.025*SL	0.069 + 0.026*SL	0.062 + 0.026*SL
	t_F	0.149	0.086 + 0.032*SL	0.084 + 0.032*SL	0.081 + 0.032*SL
	t_{PLH}	0.180	0.154 + 0.013*SL	0.157 + 0.012*SL	0.159 + 0.012*SL
	t_{PHL}	0.220	0.184 + 0.018*SL	0.188 + 0.017*SL	0.192 + 0.017*SL
D to Y	t_R	0.122	0.072 + 0.025*SL	0.069 + 0.026*SL	0.062 + 0.026*SL
	t_F	0.149	0.086 + 0.031*SL	0.084 + 0.032*SL	0.081 + 0.032*SL
	t_{PLH}	0.177	0.151 + 0.013*SL	0.154 + 0.012*SL	0.156 + 0.012*SL
	t_{PHL}	0.229	0.193 + 0.018*SL	0.197 + 0.017*SL	0.201 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA22D2A_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.172	0.124 + 0.024*SL	0.117 + 0.026*SL	0.100 + 0.027*SL
	t_F	0.112	0.085 + 0.013*SL	0.079 + 0.015*SL	0.063 + 0.016*SL
	t_{PLH}	0.125	0.099 + 0.013*SL	0.099 + 0.013*SL	0.101 + 0.013*SL
	t_{PHL}	0.093	0.073 + 0.010*SL	0.080 + 0.008*SL	0.082 + 0.008*SL
B to Y	t_R	0.162	0.111 + 0.025*SL	0.107 + 0.026*SL	0.100 + 0.027*SL
	t_F	0.134	0.105 + 0.015*SL	0.102 + 0.015*SL	0.089 + 0.016*SL
	t_{PLH}	0.146	0.119 + 0.013*SL	0.120 + 0.013*SL	0.122 + 0.013*SL
	t_{PHL}	0.115	0.097 + 0.009*SL	0.099 + 0.009*SL	0.102 + 0.008*SL
C to Y	t_R	0.107	0.082 + 0.013*SL	0.082 + 0.013*SL	0.074 + 0.013*SL
	t_F	0.122	0.091 + 0.016*SL	0.090 + 0.016*SL	0.086 + 0.016*SL
	t_{PLH}	0.199	0.184 + 0.007*SL	0.188 + 0.006*SL	0.192 + 0.006*SL
	t_{PHL}	0.229	0.210 + 0.009*SL	0.213 + 0.009*SL	0.218 + 0.008*SL
D to Y	t_R	0.107	0.083 + 0.012*SL	0.081 + 0.013*SL	0.073 + 0.013*SL
	t_F	0.123	0.091 + 0.016*SL	0.091 + 0.016*SL	0.086 + 0.016*SL
	t_{PLH}	0.195	0.181 + 0.007*SL	0.184 + 0.007*SL	0.189 + 0.006*SL
	t_{PHL}	0.238	0.219 + 0.010*SL	0.221 + 0.009*SL	0.226 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

OA22D4A_LP

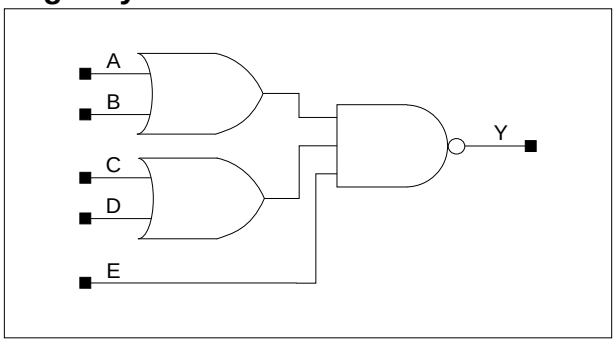
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.065	0.054 + 0.005*SL	0.051 + 0.006*SL	0.040 + 0.007*SL
	t_F	0.056	0.047 + 0.005*SL	0.049 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.284	0.275 + 0.005*SL	0.280 + 0.003*SL	0.288 + 0.003*SL
	t_{PHL}	0.252	0.243 + 0.005*SL	0.249 + 0.003*SL	0.266 + 0.002*SL
B to Y	t_R	0.065	0.053 + 0.006*SL	0.053 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.057	0.047 + 0.005*SL	0.050 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.305	0.296 + 0.005*SL	0.301 + 0.003*SL	0.310 + 0.003*SL
	t_{PHL}	0.277	0.268 + 0.005*SL	0.275 + 0.003*SL	0.291 + 0.002*SL
C to Y	t_R	0.065	0.053 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.056	0.046 + 0.005*SL	0.050 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.314	0.304 + 0.005*SL	0.310 + 0.003*SL	0.318 + 0.003*SL
	t_{PHL}	0.365	0.356 + 0.005*SL	0.362 + 0.003*SL	0.379 + 0.002*SL
D to Y	t_R	0.065	0.053 + 0.006*SL	0.052 + 0.006*SL	0.039 + 0.007*SL
	t_F	0.057	0.048 + 0.004*SL	0.048 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.310	0.301 + 0.005*SL	0.307 + 0.003*SL	0.314 + 0.003*SL
	t_{PHL}	0.375	0.366 + 0.005*SL	0.372 + 0.003*SL	0.389 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

OA221_LP/OA221D2_LP/OA221D4_LP

Two 2-ORs into 3-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)														
OA221_LP					*OA221D2_LP*					*OA221D4_LP*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
1.1	1.1	1.1	1.2	1.0	2.2	2.2	2.3	2.3	2.2	0.9	0.9	0.9	1.0	1.0

Gate Count		
OA221_LP	*OA221D2_LP*	*OA221D4_LP*
2.33	4.33	3.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA221_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.338	0.239 + 0.049*SL	0.226 + 0.053*SL	0.218 + 0.053*SL
	t_F	0.236	0.156 + 0.040*SL	0.150 + 0.042*SL	0.145 + 0.042*SL
	t_{PLH}	0.172	0.120 + 0.026*SL	0.121 + 0.026*SL	0.123 + 0.026*SL
	t_{PHL}	0.178	0.133 + 0.022*SL	0.136 + 0.022*SL	0.140 + 0.021*SL
B to Y	t_R	0.331	0.228 + 0.051*SL	0.222 + 0.053*SL	0.218 + 0.053*SL
	t_F	0.271	0.189 + 0.041*SL	0.184 + 0.042*SL	0.181 + 0.042*SL
	t_{PLH}	0.195	0.143 + 0.026*SL	0.143 + 0.026*SL	0.145 + 0.026*SL
	t_{PHL}	0.207	0.161 + 0.023*SL	0.164 + 0.022*SL	0.169 + 0.022*SL
C to Y	t_R	0.295	0.193 + 0.051*SL	0.185 + 0.053*SL	0.182 + 0.053*SL
	t_F	0.233	0.152 + 0.040*SL	0.149 + 0.041*SL	0.145 + 0.042*SL
	t_{PLH}	0.205	0.152 + 0.026*SL	0.154 + 0.026*SL	0.156 + 0.026*SL
	t_{PHL}	0.193	0.148 + 0.022*SL	0.152 + 0.022*SL	0.157 + 0.021*SL
D to Y	t_R	0.290	0.186 + 0.052*SL	0.183 + 0.053*SL	0.182 + 0.053*SL
	t_F	0.269	0.186 + 0.041*SL	0.184 + 0.042*SL	0.181 + 0.042*SL
	t_{PLH}	0.226	0.174 + 0.026*SL	0.175 + 0.026*SL	0.177 + 0.026*SL
	t_{PHL}	0.222	0.177 + 0.023*SL	0.180 + 0.022*SL	0.186 + 0.022*SL
E to Y	t_R	0.203	0.142 + 0.031*SL	0.135 + 0.033*SL	0.124 + 0.033*SL
	t_F	0.268	0.184 + 0.042*SL	0.183 + 0.042*SL	0.181 + 0.042*SL
	t_{PLH}	0.167	0.135 + 0.016*SL	0.137 + 0.016*SL	0.140 + 0.016*SL
	t_{PHL}	0.226	0.180 + 0.023*SL	0.184 + 0.022*SL	0.189 + 0.022*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA221D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.280	0.233 + 0.024*SL	0.224 + 0.026*SL	0.209 + 0.026*SL
	t_F	0.191	0.152 + 0.020*SL	0.148 + 0.021*SL	0.139 + 0.021*SL
	t_{PLH}	0.143	0.117 + 0.013*SL	0.117 + 0.013*SL	0.118 + 0.013*SL
	t_{PHL}	0.152	0.129 + 0.011*SL	0.131 + 0.011*SL	0.135 + 0.011*SL
B to Y	t_R	0.271	0.221 + 0.025*SL	0.216 + 0.026*SL	0.209 + 0.026*SL
	t_F	0.225	0.184 + 0.020*SL	0.182 + 0.021*SL	0.175 + 0.021*SL
	t_{PLH}	0.164	0.138 + 0.013*SL	0.139 + 0.013*SL	0.140 + 0.013*SL
	t_{PHL}	0.180	0.156 + 0.012*SL	0.158 + 0.011*SL	0.163 + 0.011*SL
C to Y	t_R	0.235	0.185 + 0.025*SL	0.180 + 0.026*SL	0.172 + 0.027*SL
	t_F	0.186	0.146 + 0.020*SL	0.144 + 0.020*SL	0.139 + 0.021*SL
	t_{PLH}	0.175	0.148 + 0.013*SL	0.149 + 0.013*SL	0.151 + 0.013*SL
	t_{PHL}	0.166	0.143 + 0.012*SL	0.145 + 0.011*SL	0.150 + 0.011*SL
D to Y	t_R	0.229	0.177 + 0.026*SL	0.175 + 0.026*SL	0.172 + 0.027*SL
	t_F	0.223	0.181 + 0.021*SL	0.180 + 0.021*SL	0.176 + 0.021*SL
	t_{PLH}	0.196	0.169 + 0.013*SL	0.170 + 0.013*SL	0.172 + 0.013*SL
	t_{PHL}	0.196	0.173 + 0.012*SL	0.175 + 0.011*SL	0.180 + 0.011*SL
E to Y	t_R	0.167	0.138 + 0.015*SL	0.133 + 0.016*SL	0.122 + 0.017*SL
	t_F	0.220	0.178 + 0.021*SL	0.178 + 0.021*SL	0.175 + 0.021*SL
	t_{PLH}	0.148	0.132 + 0.008*SL	0.133 + 0.008*SL	0.135 + 0.008*SL
	t_{PHL}	0.198	0.175 + 0.012*SL	0.176 + 0.011*SL	0.181 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

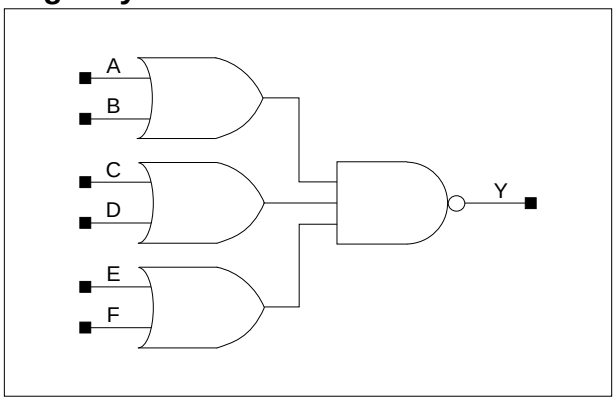
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA221D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.073	0.061 + 0.006*SL	0.061 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.058	0.047 + 0.005*SL	0.052 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.347	0.337 + 0.005*SL	0.344 + 0.003*SL	0.354 + 0.003*SL
	t_{PHL}	0.333	0.323 + 0.005*SL	0.330 + 0.003*SL	0.348 + 0.002*SL
B to Y	t_R	0.072	0.058 + 0.007*SL	0.061 + 0.006*SL	0.043 + 0.007*SL
	t_F	0.059	0.048 + 0.005*SL	0.054 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.367	0.356 + 0.005*SL	0.363 + 0.003*SL	0.374 + 0.003*SL
	t_{PHL}	0.362	0.352 + 0.005*SL	0.359 + 0.003*SL	0.377 + 0.002*SL
C to Y	t_R	0.073	0.062 + 0.006*SL	0.060 + 0.006*SL	0.043 + 0.007*SL
	t_F	0.059	0.048 + 0.005*SL	0.053 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.377	0.367 + 0.005*SL	0.374 + 0.003*SL	0.384 + 0.003*SL
	t_{PHL}	0.345	0.336 + 0.005*SL	0.343 + 0.003*SL	0.360 + 0.002*SL
D to Y	t_R	0.072	0.059 + 0.006*SL	0.061 + 0.006*SL	0.044 + 0.007*SL
	t_F	0.059	0.048 + 0.005*SL	0.052 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.399	0.389 + 0.005*SL	0.396 + 0.003*SL	0.406 + 0.003*SL
	t_{PHL}	0.377	0.368 + 0.005*SL	0.375 + 0.003*SL	0.393 + 0.002*SL
E to Y	t_R	0.068	0.056 + 0.006*SL	0.055 + 0.006*SL	0.041 + 0.007*SL
	t_F	0.060	0.051 + 0.004*SL	0.052 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.300	0.290 + 0.005*SL	0.296 + 0.003*SL	0.305 + 0.003*SL
	t_{PHL}	0.385	0.375 + 0.005*SL	0.382 + 0.003*SL	0.400 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
OA222_LP						*OA222_LP*
A	B	C	D	E	F	
1.1	1.1	1.1	1.1	1.1	1.1	2.67
OA222D2_LP						*OA222D2_LP*
A	B	C	D	E	F	
2.1	2.2	2.1	2.2	2.1	2.2	4.67
OA222D4_LP						*OA222D4_LP*
A	B	C	D	E	F	
0.9	0.9	0.9	0.9	0.9	0.9	4.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA222_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.412	0.313 + 0.049*SL	0.301 + 0.052*SL	0.292 + 0.053*SL
	t_F	0.286	0.198 + 0.044*SL	0.194 + 0.045*SL	0.193 + 0.045*SL
	t_{PLH}	0.171	0.119 + 0.026*SL	0.120 + 0.026*SL	0.122 + 0.026*SL
	t_{PHL}	0.221	0.172 + 0.024*SL	0.176 + 0.023*SL	0.182 + 0.023*SL
B to Y	t_R	0.406	0.303 + 0.051*SL	0.297 + 0.053*SL	0.292 + 0.053*SL
	t_F	0.319	0.231 + 0.044*SL	0.228 + 0.045*SL	0.228 + 0.045*SL
	t_{PLH}	0.193	0.141 + 0.026*SL	0.142 + 0.026*SL	0.144 + 0.026*SL
	t_{PHL}	0.250	0.201 + 0.024*SL	0.205 + 0.023*SL	0.212 + 0.023*SL
C to Y	t_R	0.369	0.269 + 0.050*SL	0.259 + 0.053*SL	0.254 + 0.053*SL
	t_F	0.284	0.195 + 0.044*SL	0.193 + 0.045*SL	0.192 + 0.045*SL
	t_{PLH}	0.205	0.153 + 0.026*SL	0.154 + 0.026*SL	0.157 + 0.026*SL
	t_{PHL}	0.239	0.190 + 0.024*SL	0.194 + 0.023*SL	0.201 + 0.023*SL
D to Y	t_R	0.365	0.262 + 0.052*SL	0.257 + 0.053*SL	0.254 + 0.053*SL
	t_F	0.319	0.231 + 0.044*SL	0.229 + 0.045*SL	0.228 + 0.045*SL
	t_{PLH}	0.228	0.176 + 0.026*SL	0.178 + 0.026*SL	0.180 + 0.026*SL
	t_{PHL}	0.270	0.222 + 0.024*SL	0.225 + 0.023*SL	0.232 + 0.023*SL
E to Y	t_R	0.324	0.221 + 0.051*SL	0.215 + 0.053*SL	0.213 + 0.053*SL
	t_F	0.283	0.194 + 0.044*SL	0.193 + 0.045*SL	0.192 + 0.045*SL
	t_{PLH}	0.231	0.178 + 0.027*SL	0.181 + 0.026*SL	0.185 + 0.026*SL
	t_{PHL}	0.248	0.199 + 0.024*SL	0.203 + 0.023*SL	0.210 + 0.023*SL
F to Y	t_R	0.321	0.216 + 0.052*SL	0.213 + 0.053*SL	0.213 + 0.053*SL
	t_F	0.318	0.229 + 0.044*SL	0.229 + 0.045*SL	0.228 + 0.045*SL
	t_{PLH}	0.253	0.200 + 0.027*SL	0.203 + 0.026*SL	0.206 + 0.026*SL
	t_{PHL}	0.279	0.230 + 0.024*SL	0.234 + 0.023*SL	0.241 + 0.023*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA222D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.344	0.297 + 0.024*SL	0.289 + 0.026*SL	0.273 + 0.026*SL
	t_F	0.232	0.188 + 0.022*SL	0.186 + 0.022*SL	0.181 + 0.023*SL
	t_{PLH}	0.143	0.117 + 0.013*SL	0.117 + 0.013*SL	0.119 + 0.013*SL
	t_{PHL}	0.189	0.164 + 0.012*SL	0.167 + 0.012*SL	0.172 + 0.012*SL
B to Y	t_R	0.335	0.285 + 0.025*SL	0.281 + 0.026*SL	0.274 + 0.026*SL
	t_F	0.263	0.219 + 0.022*SL	0.217 + 0.022*SL	0.214 + 0.022*SL
	t_{PLH}	0.163	0.137 + 0.013*SL	0.137 + 0.013*SL	0.138 + 0.013*SL
	t_{PHL}	0.216	0.192 + 0.012*SL	0.193 + 0.012*SL	0.198 + 0.012*SL
C to Y	t_R	0.305	0.255 + 0.025*SL	0.251 + 0.026*SL	0.239 + 0.027*SL
	t_F	0.231	0.187 + 0.022*SL	0.185 + 0.022*SL	0.182 + 0.023*SL
	t_{PLH}	0.175	0.148 + 0.013*SL	0.149 + 0.013*SL	0.151 + 0.013*SL
	t_{PHL}	0.207	0.182 + 0.013*SL	0.184 + 0.012*SL	0.189 + 0.012*SL
D to Y	t_R	0.299	0.247 + 0.026*SL	0.245 + 0.026*SL	0.240 + 0.027*SL
	t_F	0.262	0.218 + 0.022*SL	0.217 + 0.022*SL	0.215 + 0.022*SL
	t_{PLH}	0.194	0.168 + 0.013*SL	0.169 + 0.013*SL	0.170 + 0.013*SL
	t_{PHL}	0.234	0.209 + 0.012*SL	0.212 + 0.012*SL	0.217 + 0.012*SL
E to Y	t_R	0.263	0.213 + 0.025*SL	0.209 + 0.026*SL	0.202 + 0.027*SL
	t_F	0.227	0.184 + 0.022*SL	0.182 + 0.022*SL	0.181 + 0.022*SL
	t_{PLH}	0.200	0.173 + 0.013*SL	0.175 + 0.013*SL	0.178 + 0.013*SL
	t_{PHL}	0.215	0.190 + 0.012*SL	0.192 + 0.012*SL	0.198 + 0.012*SL
F to Y	t_R	0.259	0.207 + 0.026*SL	0.206 + 0.026*SL	0.203 + 0.027*SL
	t_F	0.261	0.216 + 0.022*SL	0.216 + 0.022*SL	0.215 + 0.022*SL
	t_{PLH}	0.220	0.193 + 0.013*SL	0.195 + 0.013*SL	0.198 + 0.013*SL
	t_{PHL}	0.243	0.218 + 0.012*SL	0.221 + 0.012*SL	0.226 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

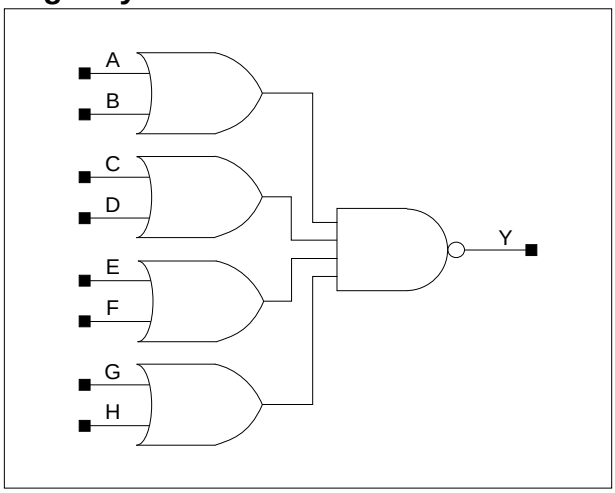
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA222D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.077	0.065 + 0.006*SL	0.066 + 0.006*SL	0.047 + 0.006*SL
	t_F	0.060	0.051 + 0.004*SL	0.052 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.362	0.351 + 0.005*SL	0.359 + 0.003*SL	0.371 + 0.003*SL
	t_{PHL}	0.368	0.359 + 0.005*SL	0.366 + 0.003*SL	0.384 + 0.002*SL
B to Y	t_R	0.077	0.064 + 0.007*SL	0.066 + 0.006*SL	0.048 + 0.006*SL
	t_F	0.060	0.050 + 0.005*SL	0.054 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.384	0.373 + 0.005*SL	0.381 + 0.003*SL	0.392 + 0.003*SL
	t_{PHL}	0.396	0.387 + 0.005*SL	0.394 + 0.003*SL	0.412 + 0.002*SL
C to Y	t_R	0.078	0.067 + 0.005*SL	0.065 + 0.006*SL	0.048 + 0.006*SL
	t_F	0.060	0.049 + 0.005*SL	0.054 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.398	0.388 + 0.005*SL	0.395 + 0.003*SL	0.407 + 0.003*SL
	t_{PHL}	0.387	0.377 + 0.005*SL	0.384 + 0.003*SL	0.402 + 0.002*SL
D to Y	t_R	0.078	0.067 + 0.005*SL	0.065 + 0.006*SL	0.047 + 0.006*SL
	t_F	0.059	0.049 + 0.005*SL	0.053 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.422	0.411 + 0.005*SL	0.419 + 0.003*SL	0.430 + 0.003*SL
	t_{PHL}	0.417	0.407 + 0.005*SL	0.414 + 0.003*SL	0.432 + 0.002*SL
E to Y	t_R	0.077	0.063 + 0.007*SL	0.068 + 0.006*SL	0.049 + 0.006*SL
	t_F	0.059	0.049 + 0.005*SL	0.053 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.427	0.416 + 0.005*SL	0.424 + 0.004*SL	0.436 + 0.003*SL
	t_{PHL}	0.396	0.386 + 0.005*SL	0.393 + 0.003*SL	0.411 + 0.002*SL
F to Y	t_R	0.079	0.067 + 0.006*SL	0.067 + 0.006*SL	0.049 + 0.006*SL
	t_F	0.060	0.049 + 0.005*SL	0.054 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.449	0.438 + 0.005*SL	0.446 + 0.004*SL	0.458 + 0.003*SL
	t_{PHL}	0.426	0.416 + 0.005*SL	0.423 + 0.003*SL	0.441 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
OA2222_LP								*OA2222_LP*
A	B	C	D	E	F	G	H	
1.1	1.1	1.1	1.1	1.1	1.1	1.2	1.1	3.67
OA2222D2_LP								*OA2222D2_LP*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	1.0	1.0	1.0	4.33
OA2222D4_LP								*OA2222D4_LP*
A	B	C	D	E	F	G	H	
0.9	0.9	0.9	0.9	0.9	1.0	1.0	1.0	5.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA2222_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.499	0.399 + 0.050*SL	0.389 + 0.053*SL	0.382 + 0.053*SL
	t_F	0.345	0.245 + 0.050*SL	0.242 + 0.051*SL	0.243 + 0.051*SL
	t_{PLH}	0.186	0.134 + 0.026*SL	0.135 + 0.026*SL	0.136 + 0.026*SL
	t_{PHL}	0.252	0.198 + 0.027*SL	0.201 + 0.026*SL	0.207 + 0.026*SL
B to Y	t_R	0.494	0.391 + 0.052*SL	0.386 + 0.053*SL	0.382 + 0.053*SL
	t_F	0.383	0.283 + 0.050*SL	0.281 + 0.051*SL	0.283 + 0.051*SL
	t_{PLH}	0.207	0.155 + 0.026*SL	0.156 + 0.026*SL	0.157 + 0.026*SL
	t_{PHL}	0.284	0.230 + 0.027*SL	0.233 + 0.026*SL	0.240 + 0.026*SL
C to Y	t_R	0.464	0.362 + 0.051*SL	0.354 + 0.053*SL	0.349 + 0.053*SL
	t_F	0.346	0.246 + 0.050*SL	0.244 + 0.051*SL	0.243 + 0.051*SL
	t_{PLH}	0.221	0.168 + 0.026*SL	0.169 + 0.026*SL	0.172 + 0.026*SL
	t_{PHL}	0.277	0.223 + 0.027*SL	0.227 + 0.026*SL	0.233 + 0.026*SL
D to Y	t_R	0.460	0.357 + 0.052*SL	0.352 + 0.053*SL	0.349 + 0.053*SL
	t_F	0.384	0.284 + 0.050*SL	0.283 + 0.050*SL	0.283 + 0.051*SL
	t_{PLH}	0.242	0.190 + 0.026*SL	0.191 + 0.026*SL	0.193 + 0.026*SL
	t_{PHL}	0.310	0.256 + 0.027*SL	0.259 + 0.026*SL	0.266 + 0.026*SL
E to Y	t_R	0.489	0.387 + 0.051*SL	0.380 + 0.053*SL	0.374 + 0.053*SL
	t_F	0.346	0.245 + 0.050*SL	0.244 + 0.050*SL	0.244 + 0.050*SL
	t_{PLH}	0.248	0.195 + 0.027*SL	0.198 + 0.026*SL	0.202 + 0.026*SL
	t_{PHL}	0.292	0.237 + 0.027*SL	0.241 + 0.026*SL	0.248 + 0.026*SL
F to Y	t_R	0.486	0.383 + 0.051*SL	0.378 + 0.053*SL	0.374 + 0.053*SL
	t_F	0.384	0.283 + 0.050*SL	0.283 + 0.051*SL	0.283 + 0.050*SL
	t_{PLH}	0.269	0.216 + 0.026*SL	0.218 + 0.026*SL	0.221 + 0.026*SL
	t_{PHL}	0.324	0.270 + 0.027*SL	0.274 + 0.026*SL	0.280 + 0.026*SL
G to Y	t_R	0.590	0.488 + 0.051*SL	0.481 + 0.053*SL	0.475 + 0.053*SL
	t_F	0.440	0.326 + 0.057*SL	0.325 + 0.057*SL	0.325 + 0.057*SL
	t_{PLH}	0.274	0.219 + 0.027*SL	0.223 + 0.026*SL	0.230 + 0.026*SL
	t_{PHL}	0.383	0.321 + 0.031*SL	0.325 + 0.030*SL	0.334 + 0.029*SL
H to Y	t_R	0.589	0.486 + 0.052*SL	0.481 + 0.053*SL	0.475 + 0.053*SL
	t_F	0.484	0.369 + 0.057*SL	0.370 + 0.057*SL	0.370 + 0.057*SL
	t_{PLH}	0.295	0.241 + 0.027*SL	0.245 + 0.026*SL	0.251 + 0.026*SL
	t_{PHL}	0.420	0.359 + 0.030*SL	0.363 + 0.030*SL	0.371 + 0.029*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA2222D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.083	0.062 + 0.010*SL	0.055 + 0.012*SL	0.040 + 0.013*SL
	t_F	0.059	0.042 + 0.008*SL	0.043 + 0.008*SL	0.035 + 0.008*SL
	t_{PLH}	0.358	0.341 + 0.009*SL	0.349 + 0.006*SL	0.354 + 0.006*SL
	t_{PHL}	0.369	0.354 + 0.007*SL	0.362 + 0.005*SL	0.371 + 0.005*SL
B to Y	t_R	0.083	0.062 + 0.011*SL	0.056 + 0.012*SL	0.040 + 0.013*SL
	t_F	0.059	0.043 + 0.008*SL	0.043 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.379	0.362 + 0.009*SL	0.370 + 0.006*SL	0.375 + 0.006*SL
	t_{PHL}	0.399	0.385 + 0.007*SL	0.393 + 0.005*SL	0.401 + 0.005*SL
C to Y	t_R	0.084	0.063 + 0.011*SL	0.057 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.058	0.041 + 0.009*SL	0.044 + 0.008*SL	0.035 + 0.009*SL
	t_{PLH}	0.395	0.378 + 0.009*SL	0.387 + 0.006*SL	0.391 + 0.006*SL
	t_{PHL}	0.394	0.380 + 0.007*SL	0.387 + 0.005*SL	0.396 + 0.005*SL
D to Y	t_R	0.084	0.063 + 0.010*SL	0.056 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.059	0.042 + 0.008*SL	0.044 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.416	0.399 + 0.009*SL	0.408 + 0.006*SL	0.412 + 0.006*SL
	t_{PHL}	0.425	0.411 + 0.007*SL	0.419 + 0.005*SL	0.427 + 0.005*SL
E to Y	t_R	0.086	0.065 + 0.010*SL	0.058 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.043 + 0.008*SL	0.035 + 0.009*SL
	t_{PLH}	0.424	0.406 + 0.009*SL	0.415 + 0.006*SL	0.420 + 0.006*SL
	t_{PHL}	0.409	0.395 + 0.007*SL	0.402 + 0.005*SL	0.411 + 0.005*SL
F to Y	t_R	0.085	0.064 + 0.011*SL	0.058 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.058	0.041 + 0.009*SL	0.043 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.443	0.426 + 0.009*SL	0.435 + 0.006*SL	0.439 + 0.006*SL
	t_{PHL}	0.440	0.426 + 0.007*SL	0.433 + 0.005*SL	0.442 + 0.005*SL
G to Y	t_R	0.086	0.065 + 0.011*SL	0.059 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.060	0.045 + 0.008*SL	0.044 + 0.008*SL	0.037 + 0.008*SL
	t_{PLH}	0.447	0.429 + 0.009*SL	0.439 + 0.006*SL	0.443 + 0.006*SL
	t_{PHL}	0.496	0.481 + 0.007*SL	0.489 + 0.005*SL	0.498 + 0.005*SL
H to Y	t_R	0.086	0.066 + 0.010*SL	0.059 + 0.012*SL	0.042 + 0.013*SL
	t_F	0.060	0.043 + 0.009*SL	0.046 + 0.008*SL	0.036 + 0.008*SL
	t_{PLH}	0.467	0.449 + 0.009*SL	0.459 + 0.006*SL	0.463 + 0.006*SL
	t_{PHL}	0.533	0.518 + 0.007*SL	0.526 + 0.005*SL	0.535 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

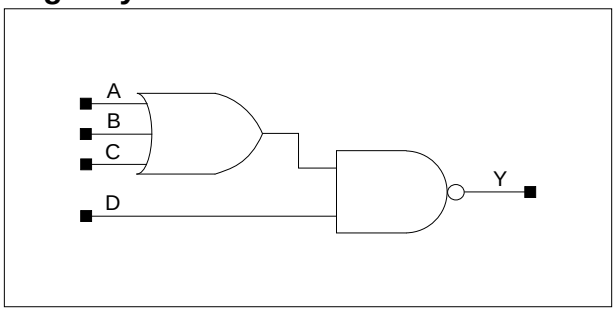
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA2222D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.081	0.069 + 0.006*SL	0.069 + 0.006*SL	0.051 + 0.006*SL
	t_F	0.062	0.053 + 0.005*SL	0.055 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.393	0.382 + 0.006*SL	0.390 + 0.004*SL	0.403 + 0.003*SL
	t_{PHL}	0.408	0.398 + 0.005*SL	0.405 + 0.003*SL	0.424 + 0.002*SL
B to Y	t_R	0.081	0.070 + 0.006*SL	0.069 + 0.006*SL	0.051 + 0.006*SL
	t_F	0.062	0.052 + 0.005*SL	0.057 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.414	0.403 + 0.006*SL	0.411 + 0.004*SL	0.424 + 0.003*SL
	t_{PHL}	0.439	0.429 + 0.005*SL	0.437 + 0.003*SL	0.455 + 0.002*SL
C to Y	t_R	0.081	0.067 + 0.007*SL	0.071 + 0.006*SL	0.052 + 0.006*SL
	t_F	0.062	0.053 + 0.004*SL	0.055 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.431	0.420 + 0.006*SL	0.428 + 0.004*SL	0.441 + 0.003*SL
	t_{PHL}	0.433	0.423 + 0.005*SL	0.430 + 0.003*SL	0.449 + 0.002*SL
D to Y	t_R	0.082	0.070 + 0.006*SL	0.070 + 0.006*SL	0.052 + 0.006*SL
	t_F	0.062	0.051 + 0.005*SL	0.057 + 0.004*SL	0.050 + 0.004*SL
	t_{PLH}	0.452	0.441 + 0.006*SL	0.449 + 0.004*SL	0.462 + 0.003*SL
	t_{PHL}	0.465	0.455 + 0.005*SL	0.463 + 0.003*SL	0.481 + 0.002*SL
E to Y	t_R	0.084	0.072 + 0.006*SL	0.072 + 0.006*SL	0.053 + 0.006*SL
	t_F	0.062	0.053 + 0.005*SL	0.056 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.460	0.449 + 0.006*SL	0.457 + 0.004*SL	0.470 + 0.003*SL
	t_{PHL}	0.449	0.439 + 0.005*SL	0.446 + 0.003*SL	0.465 + 0.002*SL
F to Y	t_R	0.083	0.070 + 0.006*SL	0.071 + 0.006*SL	0.053 + 0.006*SL
	t_F	0.062	0.052 + 0.005*SL	0.056 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.480	0.468 + 0.006*SL	0.477 + 0.004*SL	0.490 + 0.003*SL
	t_{PHL}	0.480	0.470 + 0.005*SL	0.477 + 0.003*SL	0.496 + 0.002*SL
G to Y	t_R	0.084	0.073 + 0.006*SL	0.073 + 0.006*SL	0.053 + 0.006*SL
	t_F	0.063	0.052 + 0.005*SL	0.058 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.484	0.473 + 0.006*SL	0.481 + 0.004*SL	0.495 + 0.003*SL
	t_{PHL}	0.537	0.528 + 0.005*SL	0.535 + 0.003*SL	0.555 + 0.002*SL
H to Y	t_R	0.084	0.073 + 0.006*SL	0.073 + 0.006*SL	0.054 + 0.006*SL
	t_F	0.065	0.056 + 0.005*SL	0.058 + 0.004*SL	0.054 + 0.004*SL
	t_{PLH}	0.504	0.493 + 0.006*SL	0.501 + 0.004*SL	0.515 + 0.003*SL
	t_{PHL}	0.575	0.565 + 0.005*SL	0.573 + 0.003*SL	0.592 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)											
OA31_LP				*OA31D2_LP*				*OA31D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
1.0	1.0	1.0	0.7	2.0	2.0	2.0	1.3	0.9	0.9	0.9	0.9

Gate Count		
OA31_LP	*OA31D2_LP*	*OA31D4_LP*
1.67	3.00	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA31_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.341	0.186 + 0.077*SL	0.175 + 0.080*SL	0.178 + 0.080*SL
	t_F	0.187	0.099 + 0.044*SL	0.088 + 0.047*SL	0.081 + 0.047*SL
	t_{PLH}	0.189	0.110 + 0.039*SL	0.111 + 0.039*SL	0.114 + 0.039*SL
	t_{PHL}	0.151	0.100 + 0.025*SL	0.102 + 0.025*SL	0.105 + 0.025*SL
B to Y	t_R	0.343	0.185 + 0.079*SL	0.180 + 0.080*SL	0.178 + 0.080*SL
	t_F	0.222	0.131 + 0.045*SL	0.124 + 0.047*SL	0.119 + 0.047*SL
	t_{PLH}	0.240	0.161 + 0.040*SL	0.162 + 0.039*SL	0.164 + 0.039*SL
	t_{PHL}	0.183	0.131 + 0.026*SL	0.135 + 0.025*SL	0.139 + 0.025*SL
C to Y	t_R	0.342	0.184 + 0.079*SL	0.180 + 0.080*SL	0.178 + 0.080*SL
	t_F	0.259	0.168 + 0.046*SL	0.163 + 0.047*SL	0.159 + 0.047*SL
	t_{PLH}	0.262	0.183 + 0.040*SL	0.184 + 0.039*SL	0.186 + 0.039*SL
	t_{PHL}	0.201	0.146 + 0.027*SL	0.154 + 0.025*SL	0.165 + 0.025*SL
D to Y	t_R	0.209	0.122 + 0.044*SL	0.110 + 0.047*SL	0.101 + 0.047*SL
	t_F	0.256	0.163 + 0.046*SL	0.161 + 0.047*SL	0.159 + 0.047*SL
	t_{PLH}	0.165	0.120 + 0.022*SL	0.121 + 0.022*SL	0.122 + 0.022*SL
	t_{PHL}	0.204	0.149 + 0.027*SL	0.157 + 0.025*SL	0.169 + 0.025*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA31D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.259	0.183 + 0.038*SL	0.175 + 0.040*SL	0.169 + 0.040*SL
	t_F	0.141	0.098 + 0.022*SL	0.092 + 0.023*SL	0.079 + 0.024*SL
	t_{PLH}	0.149	0.110 + 0.019*SL	0.108 + 0.020*SL	0.111 + 0.020*SL
	t_{PHL}	0.124	0.098 + 0.013*SL	0.100 + 0.013*SL	0.103 + 0.012*SL
B to Y	t_R	0.259	0.181 + 0.039*SL	0.177 + 0.040*SL	0.173 + 0.040*SL
	t_F	0.175	0.131 + 0.022*SL	0.127 + 0.023*SL	0.117 + 0.024*SL
	t_{PLH}	0.197	0.158 + 0.020*SL	0.158 + 0.020*SL	0.160 + 0.020*SL
	t_{PHL}	0.154	0.128 + 0.013*SL	0.130 + 0.013*SL	0.134 + 0.012*SL
C to Y	t_R	0.257	0.179 + 0.039*SL	0.176 + 0.040*SL	0.173 + 0.040*SL
	t_F	0.211	0.166 + 0.023*SL	0.164 + 0.023*SL	0.158 + 0.023*SL
	t_{PLH}	0.223	0.183 + 0.020*SL	0.184 + 0.020*SL	0.185 + 0.020*SL
	t_{PHL}	0.173	0.144 + 0.014*SL	0.149 + 0.013*SL	0.159 + 0.013*SL
D to Y	t_R	0.164	0.122 + 0.021*SL	0.115 + 0.023*SL	0.100 + 0.024*SL
	t_F	0.206	0.159 + 0.023*SL	0.159 + 0.023*SL	0.156 + 0.024*SL
	t_{PLH}	0.142	0.120 + 0.011*SL	0.120 + 0.011*SL	0.121 + 0.011*SL
	t_{PHL}	0.175	0.146 + 0.014*SL	0.151 + 0.013*SL	0.162 + 0.013*SL

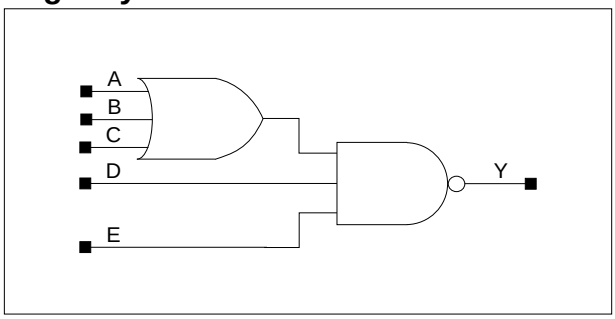
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OA31D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.072	0.060 + 0.006*SL	0.060 + 0.006*SL	0.044 + 0.007*SL
	t_F	0.055	0.046 + 0.005*SL	0.048 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.369	0.359 + 0.005*SL	0.366 + 0.003*SL	0.376 + 0.003*SL
	t_{PHL}	0.256	0.247 + 0.005*SL	0.254 + 0.003*SL	0.271 + 0.002*SL
B to Y	t_R	0.072	0.060 + 0.006*SL	0.059 + 0.006*SL	0.043 + 0.007*SL
	t_F	0.057	0.047 + 0.005*SL	0.050 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.421	0.411 + 0.005*SL	0.418 + 0.003*SL	0.428 + 0.003*SL
	t_{PHL}	0.278	0.269 + 0.005*SL	0.276 + 0.003*SL	0.293 + 0.002*SL
C to Y	t_R	0.072	0.060 + 0.006*SL	0.059 + 0.006*SL	0.043 + 0.007*SL
	t_F	0.057	0.048 + 0.005*SL	0.050 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.442	0.431 + 0.005*SL	0.438 + 0.003*SL	0.449 + 0.003*SL
	t_{PHL}	0.292	0.282 + 0.005*SL	0.289 + 0.003*SL	0.307 + 0.002*SL
D to Y	t_R	0.064	0.051 + 0.006*SL	0.052 + 0.006*SL	0.038 + 0.007*SL
	t_F	0.057	0.046 + 0.006*SL	0.052 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.276	0.266 + 0.005*SL	0.272 + 0.003*SL	0.280 + 0.003*SL
	t_{PHL}	0.297	0.288 + 0.005*SL	0.295 + 0.003*SL	0.312 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)					Gate Count
OA311_LP					*OA311_LP*
A	B	C	D	E	
1.0	1.0	1.1	0.8	0.7	2.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA311_LP

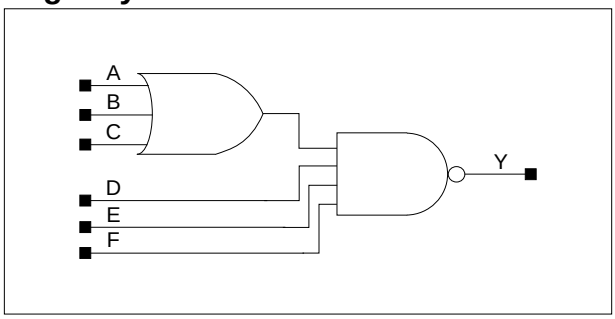
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.370	0.214 + 0.078*SL	0.205 + 0.080*SL	0.208 + 0.080*SL
	t_F	0.223	0.127 + 0.048*SL	0.117 + 0.050*SL	0.112 + 0.050*SL
	t_{PLH}	0.205	0.126 + 0.040*SL	0.127 + 0.039*SL	0.131 + 0.039*SL
	t_{PHL}	0.160	0.107 + 0.026*SL	0.109 + 0.026*SL	0.111 + 0.026*SL
B to Y	t_R	0.371	0.213 + 0.079*SL	0.210 + 0.080*SL	0.208 + 0.080*SL
	t_F	0.260	0.163 + 0.048*SL	0.156 + 0.050*SL	0.153 + 0.050*SL
	t_{PLH}	0.256	0.176 + 0.040*SL	0.178 + 0.039*SL	0.180 + 0.039*SL
	t_{PHL}	0.193	0.139 + 0.027*SL	0.143 + 0.026*SL	0.147 + 0.026*SL
C to Y	t_R	0.371	0.212 + 0.079*SL	0.209 + 0.080*SL	0.209 + 0.080*SL
	t_F	0.301	0.204 + 0.049*SL	0.198 + 0.050*SL	0.196 + 0.050*SL
	t_{PLH}	0.278	0.198 + 0.040*SL	0.200 + 0.039*SL	0.203 + 0.039*SL
	t_{PHL}	0.213	0.157 + 0.028*SL	0.164 + 0.026*SL	0.174 + 0.026*SL
D to Y	t_R	0.228	0.140 + 0.044*SL	0.131 + 0.046*SL	0.125 + 0.047*SL
	t_F	0.298	0.199 + 0.050*SL	0.197 + 0.050*SL	0.195 + 0.050*SL
	t_{PLH}	0.180	0.136 + 0.022*SL	0.137 + 0.022*SL	0.138 + 0.022*SL
	t_{PHL}	0.228	0.171 + 0.028*SL	0.178 + 0.027*SL	0.189 + 0.026*SL
E to Y	t_R	0.242	0.152 + 0.045*SL	0.143 + 0.047*SL	0.138 + 0.047*SL
	t_F	0.297	0.197 + 0.050*SL	0.197 + 0.050*SL	0.195 + 0.050*SL
	t_{PLH}	0.191	0.146 + 0.022*SL	0.147 + 0.022*SL	0.149 + 0.022*SL
	t_{PHL}	0.227	0.170 + 0.028*SL	0.178 + 0.027*SL	0.189 + 0.026*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

OA3111_LP

3-OR into 4-NAND with 1X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
OA3111_LP						*OA3111_LP*
A	B	C	D	E	F	
1.1	1.1	1.2	0.8	0.8	0.8	2.33

Switching Characteristics

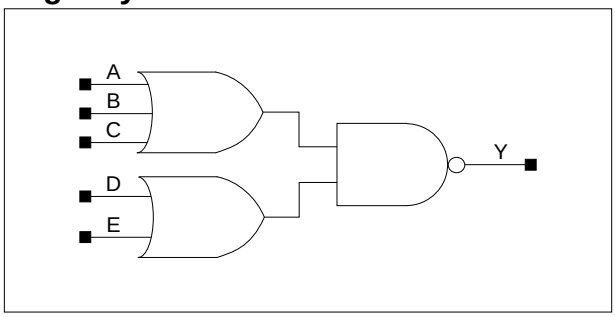
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA3111_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.405	0.248 + 0.079*SL	0.242 + 0.080*SL	0.246 + 0.080*SL
	t_F	0.245	0.152 + 0.046*SL	0.144 + 0.048*SL	0.141 + 0.048*SL
	t_{PLH}	0.225	0.146 + 0.040*SL	0.147 + 0.039*SL	0.152 + 0.039*SL
	t_{PHL}	0.159	0.109 + 0.025*SL	0.110 + 0.025*SL	0.112 + 0.025*SL
B to Y	t_R	0.408	0.249 + 0.079*SL	0.247 + 0.080*SL	0.246 + 0.080*SL
	t_F	0.282	0.188 + 0.047*SL	0.182 + 0.048*SL	0.179 + 0.048*SL
	t_{PLH}	0.275	0.195 + 0.040*SL	0.197 + 0.039*SL	0.201 + 0.039*SL
	t_{PHL}	0.190	0.139 + 0.026*SL	0.142 + 0.025*SL	0.146 + 0.025*SL
C to Y	t_R	0.407	0.248 + 0.079*SL	0.246 + 0.080*SL	0.246 + 0.080*SL
	t_F	0.322	0.228 + 0.047*SL	0.223 + 0.048*SL	0.221 + 0.048*SL
	t_{PLH}	0.298	0.219 + 0.040*SL	0.221 + 0.039*SL	0.224 + 0.039*SL
	t_{PHL}	0.211	0.157 + 0.027*SL	0.163 + 0.025*SL	0.173 + 0.025*SL
D to Y	t_R	0.282	0.182 + 0.050*SL	0.175 + 0.052*SL	0.173 + 0.052*SL
	t_F	0.320	0.226 + 0.047*SL	0.223 + 0.048*SL	0.220 + 0.048*SL
	t_{PLH}	0.215	0.166 + 0.025*SL	0.167 + 0.024*SL	0.169 + 0.024*SL
	t_{PHL}	0.233	0.179 + 0.027*SL	0.185 + 0.025*SL	0.195 + 0.025*SL
E to Y	t_R	0.303	0.200 + 0.051*SL	0.195 + 0.053*SL	0.193 + 0.053*SL
	t_F	0.320	0.225 + 0.048*SL	0.223 + 0.048*SL	0.220 + 0.048*SL
	t_{PLH}	0.232	0.182 + 0.025*SL	0.184 + 0.025*SL	0.186 + 0.025*SL
	t_{PHL}	0.238	0.184 + 0.027*SL	0.190 + 0.025*SL	0.200 + 0.025*SL
F to Y	t_R	0.320	0.217 + 0.052*SL	0.213 + 0.053*SL	0.211 + 0.053*SL
	t_F	0.319	0.223 + 0.048*SL	0.222 + 0.048*SL	0.220 + 0.048*SL
	t_{PLH}	0.246	0.195 + 0.025*SL	0.197 + 0.025*SL	0.201 + 0.025*SL
	t_{PHL}	0.240	0.187 + 0.027*SL	0.193 + 0.025*SL	0.203 + 0.025*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	x	x	1
x	x	x	0	0	1
Other States					0

Cell Data

Input Load (SL)					Gate Count
OA32_LP					*OA32_LP*
A	B	C	D	E	
1.0	1.0	1.0	1.0	1.0	2.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA32_LP

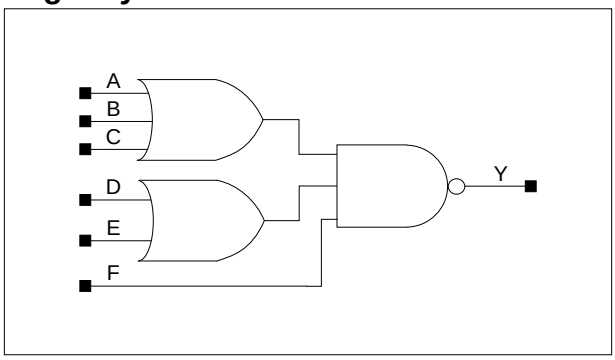
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.487	0.333 + 0.077*SL	0.322 + 0.080*SL	0.324 + 0.080*SL
	t_F	0.244	0.153 + 0.046*SL	0.146 + 0.047*SL	0.143 + 0.047*SL
	t_{PLH}	0.208	0.129 + 0.040*SL	0.130 + 0.039*SL	0.133 + 0.039*SL
	t_{PHL}	0.199	0.147 + 0.026*SL	0.151 + 0.025*SL	0.155 + 0.025*SL
B to Y	t_R	0.489	0.333 + 0.078*SL	0.328 + 0.080*SL	0.324 + 0.080*SL
	t_F	0.280	0.188 + 0.046*SL	0.184 + 0.047*SL	0.182 + 0.047*SL
	t_{PLH}	0.259	0.181 + 0.039*SL	0.182 + 0.039*SL	0.183 + 0.039*SL
	t_{PHL}	0.233	0.180 + 0.026*SL	0.184 + 0.025*SL	0.190 + 0.025*SL
C to Y	t_R	0.488	0.331 + 0.078*SL	0.327 + 0.080*SL	0.324 + 0.080*SL
	t_F	0.318	0.224 + 0.047*SL	0.223 + 0.047*SL	0.223 + 0.047*SL
	t_{PLH}	0.283	0.204 + 0.039*SL	0.205 + 0.039*SL	0.206 + 0.039*SL
	t_{PHL}	0.254	0.200 + 0.027*SL	0.206 + 0.025*SL	0.217 + 0.025*SL
D to Y	t_R	0.279	0.177 + 0.051*SL	0.168 + 0.053*SL	0.164 + 0.053*SL
	t_F	0.282	0.188 + 0.047*SL	0.187 + 0.047*SL	0.187 + 0.047*SL
	t_{PLH}	0.195	0.142 + 0.026*SL	0.143 + 0.026*SL	0.145 + 0.026*SL
	t_{PHL}	0.234	0.179 + 0.028*SL	0.187 + 0.026*SL	0.199 + 0.025*SL
E to Y	t_R	0.274	0.169 + 0.052*SL	0.165 + 0.053*SL	0.164 + 0.053*SL
	t_F	0.316	0.221 + 0.047*SL	0.222 + 0.047*SL	0.222 + 0.047*SL
	t_{PLH}	0.215	0.163 + 0.026*SL	0.164 + 0.026*SL	0.166 + 0.026*SL
	t_{PHL}	0.266	0.212 + 0.027*SL	0.219 + 0.025*SL	0.230 + 0.025*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

OA321_LP

3-OR and 2-OR into 3-NAND with 1X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	0	x	1
x	x	x	x	x	0	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
OA321_LP						*OA321_LP*
A	B	C	D	E	F	
1.0	1.1	1.1	1.0	1.0	0.7	2.67

Switching Characteristics

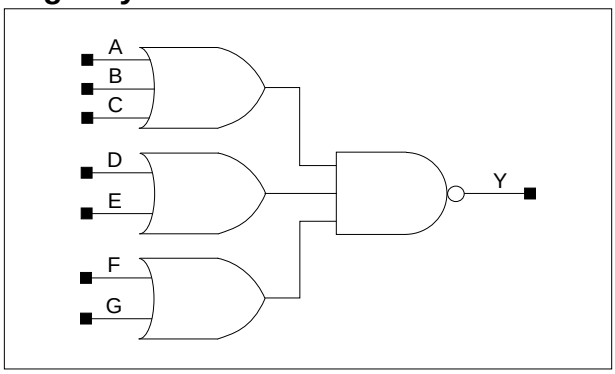
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA321_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.489	0.335 + 0.077*SL	0.326 + 0.080*SL	0.328 + 0.079*SL
	t_F	0.258	0.166 + 0.046*SL	0.160 + 0.047*SL	0.158 + 0.048*SL
	t_{PLH}	0.216	0.137 + 0.039*SL	0.139 + 0.039*SL	0.142 + 0.039*SL
	t_{PHL}	0.190	0.139 + 0.025*SL	0.142 + 0.025*SL	0.147 + 0.024*SL
B to Y	t_R	0.492	0.336 + 0.078*SL	0.331 + 0.079*SL	0.328 + 0.079*SL
	t_F	0.294	0.201 + 0.047*SL	0.197 + 0.048*SL	0.196 + 0.048*SL
	t_{PLH}	0.266	0.187 + 0.040*SL	0.189 + 0.039*SL	0.192 + 0.039*SL
	t_{PHL}	0.222	0.171 + 0.026*SL	0.174 + 0.025*SL	0.180 + 0.024*SL
C to Y	t_R	0.491	0.335 + 0.078*SL	0.331 + 0.079*SL	0.328 + 0.079*SL
	t_F	0.332	0.239 + 0.047*SL	0.237 + 0.047*SL	0.236 + 0.047*SL
	t_{PLH}	0.289	0.210 + 0.040*SL	0.212 + 0.039*SL	0.215 + 0.039*SL
	t_{PHL}	0.244	0.191 + 0.027*SL	0.197 + 0.025*SL	0.207 + 0.024*SL
D to Y	t_R	0.338	0.218 + 0.060*SL	0.211 + 0.062*SL	0.211 + 0.062*SL
	t_F	0.301	0.207 + 0.047*SL	0.204 + 0.047*SL	0.203 + 0.048*SL
	t_{PLH}	0.235	0.175 + 0.030*SL	0.176 + 0.030*SL	0.179 + 0.030*SL
	t_{PHL}	0.237	0.183 + 0.027*SL	0.190 + 0.025*SL	0.201 + 0.025*SL
E to Y	t_R	0.336	0.213 + 0.061*SL	0.211 + 0.062*SL	0.211 + 0.062*SL
	t_F	0.332	0.238 + 0.047*SL	0.237 + 0.047*SL	0.236 + 0.047*SL
	t_{PLH}	0.259	0.198 + 0.030*SL	0.200 + 0.030*SL	0.202 + 0.030*SL
	t_{PHL}	0.266	0.213 + 0.027*SL	0.219 + 0.025*SL	0.230 + 0.024*SL
F to Y	t_R	0.510	0.414 + 0.048*SL	0.402 + 0.051*SL	0.390 + 0.052*SL
	t_F	0.331	0.236 + 0.047*SL	0.236 + 0.047*SL	0.236 + 0.047*SL
	t_{PLH}	0.229	0.179 + 0.025*SL	0.181 + 0.024*SL	0.184 + 0.024*SL
	t_{PHL}	0.269	0.216 + 0.027*SL	0.222 + 0.025*SL	0.233 + 0.024*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Y
0	0	0	x	x	x	x	1
x	x	x	0	0	x	x	1
x	x	x	x	x	0	0	1
Other States							0

Cell Data

Input Load (SL)							Gate Count
OA322_LP							*OA322_LP*
A	B	C	D	E	F	G	
1.0	1.0	1.1	1.1	1.1	1.1	1.1	3.33

OA322_LP

3-OR and Two 2-ORs into 3-NAND with 1X Drive

Switching Characteristics

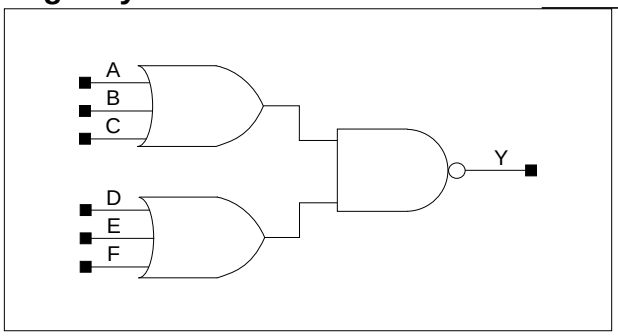
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA322_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.658	0.502 + 0.078*SL	0.495 + 0.080*SL	0.496 + 0.079*SL
	t_F	0.325	0.231 + 0.047*SL	0.229 + 0.048*SL	0.229 + 0.048*SL
	t_{PLH}	0.237	0.158 + 0.040*SL	0.159 + 0.039*SL	0.163 + 0.039*SL
	t_{PHL}	0.246	0.195 + 0.026*SL	0.199 + 0.025*SL	0.205 + 0.024*SL
B to Y	t_R	0.660	0.504 + 0.078*SL	0.500 + 0.079*SL	0.496 + 0.079*SL
	t_F	0.362	0.267 + 0.047*SL	0.266 + 0.048*SL	0.267 + 0.048*SL
	t_{PLH}	0.287	0.208 + 0.040*SL	0.210 + 0.039*SL	0.212 + 0.039*SL
	t_{PHL}	0.280	0.228 + 0.026*SL	0.232 + 0.025*SL	0.239 + 0.024*SL
C to Y	t_R	0.660	0.503 + 0.079*SL	0.500 + 0.079*SL	0.496 + 0.079*SL
	t_F	0.401	0.306 + 0.048*SL	0.307 + 0.047*SL	0.308 + 0.047*SL
	t_{PLH}	0.312	0.233 + 0.039*SL	0.234 + 0.039*SL	0.237 + 0.039*SL
	t_{PHL}	0.304	0.251 + 0.026*SL	0.256 + 0.025*SL	0.267 + 0.024*SL
D to Y	t_R	0.480	0.381 + 0.050*SL	0.371 + 0.052*SL	0.359 + 0.053*SL
	t_F	0.366	0.271 + 0.048*SL	0.271 + 0.048*SL	0.271 + 0.048*SL
	t_{PLH}	0.225	0.172 + 0.026*SL	0.174 + 0.026*SL	0.176 + 0.026*SL
	t_{PHL}	0.296	0.242 + 0.027*SL	0.248 + 0.025*SL	0.259 + 0.025*SL
E to Y	t_R	0.477	0.375 + 0.051*SL	0.369 + 0.052*SL	0.359 + 0.053*SL
	t_F	0.401	0.306 + 0.048*SL	0.307 + 0.047*SL	0.308 + 0.047*SL
	t_{PLH}	0.247	0.195 + 0.026*SL	0.196 + 0.026*SL	0.198 + 0.026*SL
	t_{PHL}	0.328	0.276 + 0.026*SL	0.281 + 0.025*SL	0.292 + 0.024*SL
F to Y	t_R	0.581	0.481 + 0.050*SL	0.472 + 0.052*SL	0.462 + 0.053*SL
	t_F	0.363	0.268 + 0.047*SL	0.269 + 0.047*SL	0.268 + 0.047*SL
	t_{PLH}	0.253	0.200 + 0.026*SL	0.202 + 0.026*SL	0.206 + 0.026*SL
	t_{PHL}	0.305	0.251 + 0.027*SL	0.257 + 0.025*SL	0.269 + 0.024*SL
G to Y	t_R	0.579	0.477 + 0.051*SL	0.471 + 0.052*SL	0.462 + 0.053*SL
	t_F	0.401	0.306 + 0.048*SL	0.307 + 0.047*SL	0.307 + 0.047*SL
	t_{PLH}	0.276	0.224 + 0.026*SL	0.226 + 0.026*SL	0.229 + 0.026*SL
	t_{PHL}	0.340	0.287 + 0.026*SL	0.292 + 0.025*SL	0.303 + 0.024*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	x	x	x	1
x	x	x	0	0	0	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
OA33_LP						*OA33_LP*
A	B	C	D	E	F	
1.0	1.0	1.0	1.0	1.0	1.0	2.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

OA33_LP

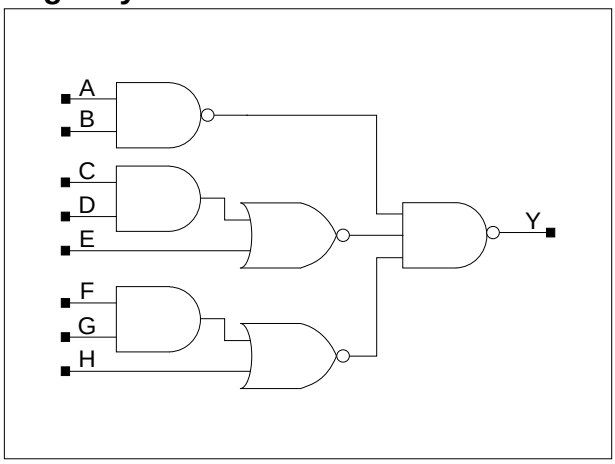
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.471	0.317 + 0.077*SL	0.305 + 0.080*SL	0.307 + 0.080*SL
	t_F	0.246	0.162 + 0.042*SL	0.158 + 0.043*SL	0.157 + 0.043*SL
	t_{PLH}	0.197	0.118 + 0.039*SL	0.119 + 0.039*SL	0.122 + 0.039*SL
	t_{PHL}	0.197	0.147 + 0.025*SL	0.154 + 0.023*SL	0.165 + 0.023*SL
B to Y	t_R	0.473	0.317 + 0.078*SL	0.312 + 0.079*SL	0.308 + 0.080*SL
	t_F	0.281	0.196 + 0.042*SL	0.194 + 0.043*SL	0.194 + 0.043*SL
	t_{PLH}	0.254	0.175 + 0.039*SL	0.176 + 0.039*SL	0.178 + 0.039*SL
	t_{PHL}	0.232	0.182 + 0.025*SL	0.188 + 0.023*SL	0.200 + 0.023*SL
C to Y	t_R	0.473	0.317 + 0.078*SL	0.311 + 0.080*SL	0.308 + 0.080*SL
	t_F	0.316	0.229 + 0.043*SL	0.230 + 0.043*SL	0.231 + 0.043*SL
	t_{PLH}	0.276	0.197 + 0.039*SL	0.199 + 0.039*SL	0.200 + 0.039*SL
	t_{PHL}	0.252	0.201 + 0.026*SL	0.209 + 0.024*SL	0.224 + 0.023*SL
D to Y	t_R	0.412	0.254 + 0.079*SL	0.249 + 0.080*SL	0.254 + 0.080*SL
	t_F	0.248	0.163 + 0.043*SL	0.162 + 0.043*SL	0.161 + 0.043*SL
	t_{PLH}	0.252	0.172 + 0.040*SL	0.174 + 0.039*SL	0.178 + 0.039*SL
	t_{PHL}	0.212	0.161 + 0.025*SL	0.169 + 0.023*SL	0.182 + 0.023*SL
E to Y	t_R	0.415	0.256 + 0.079*SL	0.254 + 0.080*SL	0.254 + 0.080*SL
	t_F	0.282	0.195 + 0.043*SL	0.196 + 0.043*SL	0.196 + 0.043*SL
	t_{PLH}	0.304	0.225 + 0.040*SL	0.227 + 0.039*SL	0.229 + 0.039*SL
	t_{PHL}	0.245	0.195 + 0.025*SL	0.202 + 0.023*SL	0.214 + 0.023*SL
F to Y	t_R	0.414	0.255 + 0.079*SL	0.254 + 0.080*SL	0.254 + 0.080*SL
	t_F	0.315	0.229 + 0.043*SL	0.230 + 0.043*SL	0.231 + 0.043*SL
	t_{PLH}	0.325	0.246 + 0.040*SL	0.248 + 0.039*SL	0.250 + 0.039*SL
	t_{PHL}	0.266	0.214 + 0.026*SL	0.223 + 0.024*SL	0.238 + 0.023*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG1_LP/SCG1D2_LP

2-NAND and two (2-AND into 2-NOR)s into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	1
x	x	1	1	x	x	x	x	1
x	x	x	x	1	x	x	x	1
x	x	x	x	x	1	1	x	1
x	x	x	x	x	x	x	1	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
SCG1_LP								*SCG1_LP*
A	B	C	D	E	F	G	H	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	4.33
SCG1D2_LP								*SCG1D2_LP*
A	B	C	D	E	F	G	H	
0.9	1.0	0.7	0.7	0.7	0.7	0.7	0.7	5.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG1_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.147	0.078 + 0.035*SL	0.074 + 0.036*SL	0.066 + 0.036*SL
	t_F	0.155	0.083 + 0.036*SL	0.079 + 0.037*SL	0.074 + 0.038*SL
	t_{PLH}	0.196	0.161 + 0.018*SL	0.164 + 0.017*SL	0.166 + 0.017*SL
	t_{PHL}	0.207	0.167 + 0.020*SL	0.170 + 0.019*SL	0.171 + 0.019*SL
B to Y	t_R	0.148	0.079 + 0.034*SL	0.074 + 0.036*SL	0.066 + 0.036*SL
	t_F	0.156	0.084 + 0.036*SL	0.079 + 0.037*SL	0.074 + 0.038*SL
	t_{PLH}	0.193	0.157 + 0.018*SL	0.161 + 0.017*SL	0.163 + 0.017*SL
	t_{PHL}	0.217	0.177 + 0.020*SL	0.179 + 0.019*SL	0.181 + 0.019*SL
C to Y	t_R	0.166	0.098 + 0.034*SL	0.092 + 0.035*SL	0.082 + 0.036*SL
	t_F	0.165	0.092 + 0.036*SL	0.090 + 0.037*SL	0.081 + 0.037*SL
	t_{PLH}	0.244	0.208 + 0.018*SL	0.213 + 0.017*SL	0.215 + 0.017*SL
	t_{PHL}	0.262	0.219 + 0.021*SL	0.227 + 0.020*SL	0.232 + 0.019*SL
D to Y	t_R	0.166	0.098 + 0.034*SL	0.092 + 0.035*SL	0.082 + 0.036*SL
	t_F	0.166	0.094 + 0.036*SL	0.090 + 0.037*SL	0.082 + 0.037*SL
	t_{PLH}	0.241	0.204 + 0.018*SL	0.209 + 0.017*SL	0.212 + 0.017*SL
	t_{PHL}	0.274	0.231 + 0.021*SL	0.239 + 0.020*SL	0.244 + 0.019*SL
E to Y	t_R	0.164	0.096 + 0.034*SL	0.089 + 0.036*SL	0.080 + 0.036*SL
	t_F	0.166	0.093 + 0.036*SL	0.090 + 0.037*SL	0.082 + 0.037*SL
	t_{PLH}	0.254	0.218 + 0.018*SL	0.222 + 0.017*SL	0.225 + 0.017*SL
	t_{PHL}	0.314	0.271 + 0.021*SL	0.279 + 0.020*SL	0.285 + 0.019*SL
F to Y	t_R	0.178	0.110 + 0.034*SL	0.103 + 0.036*SL	0.094 + 0.036*SL
	t_F	0.160	0.088 + 0.036*SL	0.085 + 0.037*SL	0.080 + 0.037*SL
	t_{PLH}	0.249	0.212 + 0.018*SL	0.217 + 0.017*SL	0.220 + 0.017*SL
	t_{PHL}	0.260	0.218 + 0.021*SL	0.224 + 0.020*SL	0.229 + 0.019*SL
G to Y	t_R	0.177	0.109 + 0.034*SL	0.103 + 0.036*SL	0.094 + 0.036*SL
	t_F	0.161	0.088 + 0.036*SL	0.085 + 0.037*SL	0.080 + 0.037*SL
	t_{PLH}	0.245	0.209 + 0.018*SL	0.213 + 0.017*SL	0.216 + 0.017*SL
	t_{PHL}	0.272	0.230 + 0.021*SL	0.236 + 0.020*SL	0.241 + 0.019*SL
H to Y	t_R	0.175	0.106 + 0.035*SL	0.102 + 0.036*SL	0.093 + 0.036*SL
	t_F	0.161	0.088 + 0.037*SL	0.086 + 0.037*SL	0.080 + 0.037*SL
	t_{PLH}	0.260	0.224 + 0.018*SL	0.227 + 0.017*SL	0.231 + 0.017*SL
	t_{PHL}	0.312	0.270 + 0.021*SL	0.277 + 0.020*SL	0.282 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

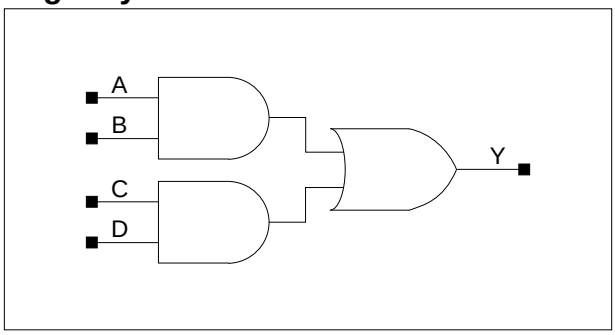
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG1D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.108	0.075 + 0.017*SL	0.071 + 0.018*SL	0.064 + 0.018*SL
	t_F	0.114	0.077 + 0.018*SL	0.076 + 0.018*SL	0.072 + 0.019*SL
	t_{PLH}	0.176	0.157 + 0.010*SL	0.161 + 0.009*SL	0.164 + 0.008*SL
	t_{PHL}	0.194	0.173 + 0.011*SL	0.176 + 0.010*SL	0.179 + 0.010*SL
B to Y	t_R	0.108	0.075 + 0.017*SL	0.071 + 0.018*SL	0.065 + 0.018*SL
	t_F	0.116	0.080 + 0.018*SL	0.079 + 0.018*SL	0.072 + 0.019*SL
	t_{PLH}	0.173	0.153 + 0.010*SL	0.158 + 0.009*SL	0.161 + 0.008*SL
	t_{PHL}	0.204	0.183 + 0.011*SL	0.186 + 0.010*SL	0.189 + 0.010*SL
C to Y	t_R	0.137	0.104 + 0.017*SL	0.102 + 0.017*SL	0.091 + 0.018*SL
	t_F	0.133	0.097 + 0.018*SL	0.096 + 0.018*SL	0.090 + 0.018*SL
	t_{PLH}	0.254	0.233 + 0.010*SL	0.239 + 0.009*SL	0.247 + 0.008*SL
	t_{PHL}	0.277	0.253 + 0.012*SL	0.260 + 0.010*SL	0.272 + 0.010*SL
D to Y	t_R	0.138	0.106 + 0.016*SL	0.102 + 0.017*SL	0.091 + 0.018*SL
	t_F	0.135	0.099 + 0.018*SL	0.098 + 0.018*SL	0.091 + 0.018*SL
	t_{PLH}	0.251	0.230 + 0.010*SL	0.236 + 0.009*SL	0.243 + 0.008*SL
	t_{PHL}	0.290	0.265 + 0.012*SL	0.272 + 0.010*SL	0.284 + 0.010*SL
E to Y	t_R	0.134	0.102 + 0.016*SL	0.098 + 0.017*SL	0.086 + 0.018*SL
	t_F	0.134	0.099 + 0.018*SL	0.098 + 0.018*SL	0.091 + 0.018*SL
	t_{PLH}	0.266	0.246 + 0.010*SL	0.251 + 0.009*SL	0.256 + 0.008*SL
	t_{PHL}	0.330	0.306 + 0.012*SL	0.313 + 0.010*SL	0.325 + 0.010*SL
F to Y	t_R	0.149	0.116 + 0.017*SL	0.114 + 0.017*SL	0.104 + 0.018*SL
	t_F	0.126	0.089 + 0.018*SL	0.089 + 0.018*SL	0.087 + 0.019*SL
	t_{PLH}	0.265	0.245 + 0.010*SL	0.250 + 0.009*SL	0.257 + 0.008*SL
	t_{PHL}	0.280	0.257 + 0.012*SL	0.263 + 0.010*SL	0.273 + 0.010*SL
G to Y	t_R	0.149	0.116 + 0.017*SL	0.115 + 0.017*SL	0.104 + 0.018*SL
	t_F	0.127	0.090 + 0.019*SL	0.091 + 0.018*SL	0.087 + 0.019*SL
	t_{PLH}	0.262	0.242 + 0.010*SL	0.247 + 0.009*SL	0.254 + 0.008*SL
	t_{PHL}	0.292	0.269 + 0.012*SL	0.275 + 0.010*SL	0.286 + 0.010*SL
H to Y	t_R	0.145	0.111 + 0.017*SL	0.110 + 0.017*SL	0.099 + 0.018*SL
	t_F	0.127	0.090 + 0.018*SL	0.091 + 0.018*SL	0.088 + 0.019*SL
	t_{PLH}	0.277	0.257 + 0.010*SL	0.261 + 0.009*SL	0.267 + 0.009*SL
	t_{PHL}	0.333	0.310 + 0.012*SL	0.316 + 0.010*SL	0.327 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	1
x	x	1	1	1
Other States				0

Cell Data

Input Load (SL)											
SCG2_LP				*SCG2D2_LP*				*SCG2D4_LP*			
A	B	C	D	A	B	C	D	A	B	C	D
0.9	0.9	0.9	1.0	1.0	1.1	1.0	1.1	1.0	1.1	1.0	1.1

Gate Count		
SCG2_LP	*SCG2D2_LP*	*SCG2D4_LP*
2.33	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.113	0.065 + 0.024*SL	0.059 + 0.025*SL	0.043 + 0.026*SL
	t_F	0.090	0.053 + 0.018*SL	0.060 + 0.017*SL	0.051 + 0.017*SL
	t_{PLH}	0.209	0.177 + 0.016*SL	0.189 + 0.013*SL	0.196 + 0.012*SL
	t_{PHL}	0.210	0.181 + 0.014*SL	0.196 + 0.011*SL	0.215 + 0.010*SL
B to Y	t_R	0.113	0.064 + 0.024*SL	0.059 + 0.025*SL	0.044 + 0.026*SL
	t_F	0.090	0.054 + 0.018*SL	0.058 + 0.017*SL	0.052 + 0.017*SL
	t_{PLH}	0.204	0.173 + 0.016*SL	0.185 + 0.013*SL	0.191 + 0.012*SL
	t_{PHL}	0.220	0.191 + 0.015*SL	0.206 + 0.011*SL	0.225 + 0.010*SL
C to Y	t_R	0.117	0.068 + 0.024*SL	0.064 + 0.025*SL	0.049 + 0.026*SL
	t_F	0.089	0.053 + 0.018*SL	0.058 + 0.017*SL	0.052 + 0.017*SL
	t_{PLH}	0.279	0.247 + 0.016*SL	0.259 + 0.013*SL	0.267 + 0.012*SL
	t_{PHL}	0.263	0.234 + 0.014*SL	0.249 + 0.011*SL	0.268 + 0.010*SL
D to Y	t_R	0.118	0.069 + 0.024*SL	0.064 + 0.025*SL	0.049 + 0.026*SL
	t_F	0.092	0.055 + 0.018*SL	0.061 + 0.017*SL	0.052 + 0.017*SL
	t_{PLH}	0.275	0.243 + 0.016*SL	0.256 + 0.013*SL	0.263 + 0.012*SL
	t_{PHL}	0.274	0.245 + 0.015*SL	0.260 + 0.011*SL	0.278 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.085	0.058 + 0.013*SL	0.062 + 0.012*SL	0.053 + 0.013*SL
	t_F	0.078	0.057 + 0.010*SL	0.064 + 0.009*SL	0.069 + 0.008*SL
	t_{PLH}	0.195	0.176 + 0.010*SL	0.187 + 0.007*SL	0.201 + 0.006*SL
	t_{PHL}	0.228	0.208 + 0.010*SL	0.221 + 0.007*SL	0.245 + 0.005*SL
B to Y	t_R	0.087	0.062 + 0.013*SL	0.063 + 0.012*SL	0.052 + 0.013*SL
	t_F	0.081	0.060 + 0.010*SL	0.067 + 0.009*SL	0.071 + 0.008*SL
	t_{PLH}	0.191	0.172 + 0.010*SL	0.183 + 0.007*SL	0.197 + 0.006*SL
	t_{PHL}	0.240	0.220 + 0.010*SL	0.233 + 0.007*SL	0.257 + 0.005*SL
C to Y	t_R	0.089	0.063 + 0.013*SL	0.067 + 0.012*SL	0.057 + 0.013*SL
	t_F	0.079	0.058 + 0.010*SL	0.066 + 0.009*SL	0.070 + 0.008*SL
	t_{PLH}	0.251	0.232 + 0.010*SL	0.243 + 0.007*SL	0.256 + 0.006*SL
	t_{PHL}	0.281	0.262 + 0.010*SL	0.274 + 0.007*SL	0.299 + 0.005*SL
D to Y	t_R	0.090	0.065 + 0.013*SL	0.067 + 0.012*SL	0.055 + 0.013*SL
	t_F	0.080	0.059 + 0.011*SL	0.067 + 0.009*SL	0.070 + 0.008*SL
	t_{PLH}	0.248	0.228 + 0.010*SL	0.239 + 0.007*SL	0.253 + 0.006*SL
	t_{PHL}	0.293	0.274 + 0.010*SL	0.286 + 0.007*SL	0.311 + 0.005*SL

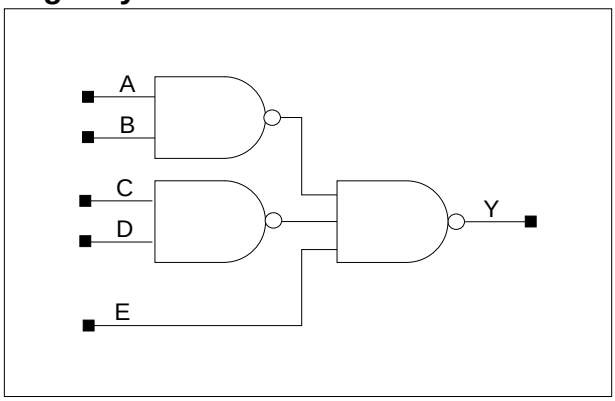
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG2D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.090	0.075 + 0.008*SL	0.081 + 0.006*SL	0.078 + 0.006*SL
	t_F	0.092	0.078 + 0.007*SL	0.087 + 0.005*SL	0.100 + 0.004*SL
	t_{PLH}	0.236	0.223 + 0.007*SL	0.232 + 0.004*SL	0.261 + 0.003*SL
	t_{PHL}	0.286	0.273 + 0.007*SL	0.283 + 0.004*SL	0.321 + 0.003*SL
B to Y	t_R	0.090	0.075 + 0.008*SL	0.081 + 0.006*SL	0.078 + 0.006*SL
	t_F	0.094	0.081 + 0.006*SL	0.087 + 0.005*SL	0.101 + 0.004*SL
	t_{PLH}	0.232	0.219 + 0.007*SL	0.228 + 0.004*SL	0.257 + 0.003*SL
	t_{PHL}	0.297	0.284 + 0.007*SL	0.294 + 0.004*SL	0.332 + 0.003*SL
C to Y	t_R	0.093	0.077 + 0.008*SL	0.083 + 0.006*SL	0.081 + 0.006*SL
	t_F	0.092	0.080 + 0.006*SL	0.085 + 0.005*SL	0.100 + 0.004*SL
	t_{PLH}	0.293	0.280 + 0.007*SL	0.290 + 0.004*SL	0.318 + 0.003*SL
	t_{PHL}	0.340	0.327 + 0.007*SL	0.337 + 0.004*SL	0.374 + 0.003*SL
D to Y	t_R	0.093	0.077 + 0.008*SL	0.083 + 0.006*SL	0.081 + 0.006*SL
	t_F	0.094	0.080 + 0.007*SL	0.089 + 0.005*SL	0.101 + 0.004*SL
	t_{PLH}	0.290	0.277 + 0.006*SL	0.286 + 0.004*SL	0.314 + 0.003*SL
	t_{PHL}	0.350	0.337 + 0.007*SL	0.348 + 0.004*SL	0.386 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	1
x	x	1	1	x	1
x	x	x	x	0	1
Other States					0

Cell Data

Input Load (SL)														
SCG3_LP					*SCG3D2_LP*					*SCG3D4_LP*				
A	B	C	D	E	A	B	C	D	E	A	B	C	D	E
0.8	0.8	0.8	0.8	1.0	1.1	1.1	1.1	1.1	2.0	0.8	0.8	0.8	0.8	1.0

Gate Count		
SCG3_LP	*SCG3D2_LP*	*SCG3D4_LP*
3.00	3.67	4.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.151	0.083 + 0.034*SL	0.077 + 0.036*SL	0.068 + 0.036*SL
	t_F	0.153	0.080 + 0.037*SL	0.077 + 0.038*SL	0.073 + 0.038*SL
	t_{PLH}	0.214	0.178 + 0.018*SL	0.182 + 0.017*SL	0.185 + 0.017*SL
	t_{PHL}	0.193	0.153 + 0.020*SL	0.155 + 0.019*SL	0.156 + 0.019*SL
B to Y	t_R	0.151	0.084 + 0.034*SL	0.076 + 0.036*SL	0.068 + 0.036*SL
	t_F	0.153	0.080 + 0.037*SL	0.077 + 0.038*SL	0.073 + 0.038*SL
	t_{PLH}	0.211	0.174 + 0.018*SL	0.179 + 0.017*SL	0.182 + 0.017*SL
	t_{PHL}	0.199	0.159 + 0.020*SL	0.162 + 0.019*SL	0.163 + 0.019*SL
C to Y	t_R	0.162	0.094 + 0.034*SL	0.088 + 0.036*SL	0.080 + 0.036*SL
	t_F	0.151	0.077 + 0.037*SL	0.075 + 0.038*SL	0.073 + 0.038*SL
	t_{PLH}	0.226	0.190 + 0.018*SL	0.194 + 0.017*SL	0.196 + 0.017*SL
	t_{PHL}	0.202	0.162 + 0.020*SL	0.164 + 0.019*SL	0.166 + 0.019*SL
D to Y	t_R	0.163	0.095 + 0.034*SL	0.088 + 0.036*SL	0.080 + 0.036*SL
	t_F	0.152	0.078 + 0.037*SL	0.076 + 0.038*SL	0.073 + 0.038*SL
	t_{PLH}	0.223	0.187 + 0.018*SL	0.191 + 0.017*SL	0.193 + 0.017*SL
	t_{PHL}	0.209	0.169 + 0.020*SL	0.171 + 0.019*SL	0.173 + 0.019*SL
E to Y	t_R	0.177	0.112 + 0.032*SL	0.101 + 0.035*SL	0.087 + 0.036*SL
	t_F	0.157	0.084 + 0.036*SL	0.080 + 0.037*SL	0.072 + 0.038*SL
	t_{PLH}	0.146	0.112 + 0.017*SL	0.113 + 0.017*SL	0.115 + 0.017*SL
	t_{PHL}	0.125	0.085 + 0.020*SL	0.088 + 0.019*SL	0.090 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.115	0.082 + 0.017*SL	0.078 + 0.017*SL	0.068 + 0.018*SL
	t_F	0.113	0.077 + 0.018*SL	0.075 + 0.019*SL	0.070 + 0.019*SL
	t_{PLH}	0.197	0.177 + 0.010*SL	0.182 + 0.009*SL	0.186 + 0.008*SL
	t_{PHL}	0.182	0.161 + 0.011*SL	0.163 + 0.010*SL	0.166 + 0.010*SL
B to Y	t_R	0.115	0.082 + 0.016*SL	0.078 + 0.017*SL	0.069 + 0.018*SL
	t_F	0.112	0.076 + 0.018*SL	0.074 + 0.019*SL	0.070 + 0.019*SL
	t_{PLH}	0.194	0.174 + 0.010*SL	0.179 + 0.009*SL	0.183 + 0.008*SL
	t_{PHL}	0.189	0.168 + 0.010*SL	0.171 + 0.010*SL	0.173 + 0.010*SL
C to Y	t_R	0.125	0.091 + 0.017*SL	0.090 + 0.017*SL	0.080 + 0.018*SL
	t_F	0.110	0.074 + 0.018*SL	0.072 + 0.019*SL	0.070 + 0.019*SL
	t_{PLH}	0.210	0.191 + 0.010*SL	0.195 + 0.009*SL	0.198 + 0.008*SL
	t_{PHL}	0.191	0.170 + 0.011*SL	0.173 + 0.010*SL	0.176 + 0.010*SL
D to Y	t_R	0.125	0.091 + 0.017*SL	0.089 + 0.017*SL	0.080 + 0.018*SL
	t_F	0.110	0.074 + 0.018*SL	0.072 + 0.019*SL	0.070 + 0.019*SL
	t_{PLH}	0.207	0.188 + 0.010*SL	0.191 + 0.009*SL	0.195 + 0.008*SL
	t_{PHL}	0.198	0.177 + 0.011*SL	0.180 + 0.010*SL	0.183 + 0.010*SL
E to Y	t_R	0.140	0.109 + 0.016*SL	0.103 + 0.017*SL	0.087 + 0.018*SL
	t_F	0.115	0.079 + 0.018*SL	0.077 + 0.018*SL	0.071 + 0.019*SL
	t_{PLH}	0.127	0.109 + 0.009*SL	0.110 + 0.009*SL	0.112 + 0.008*SL
	t_{PHL}	0.102	0.080 + 0.011*SL	0.084 + 0.010*SL	0.087 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG3D4_LP

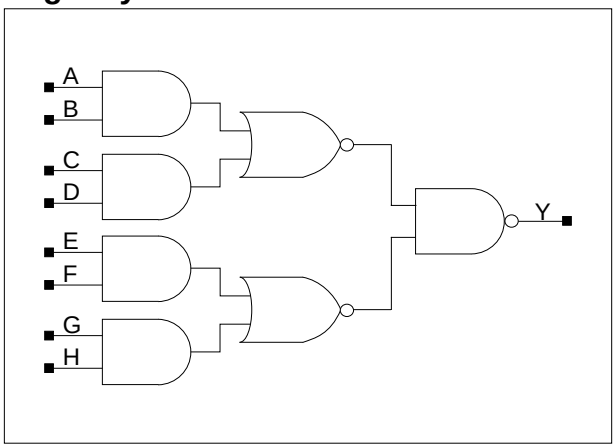
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.061	0.051 + 0.005*SL	0.047 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.057	0.049 + 0.004*SL	0.049 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.338	0.329 + 0.005*SL	0.334 + 0.003*SL	0.342 + 0.003*SL
	t_{PHL}	0.340	0.331 + 0.005*SL	0.338 + 0.003*SL	0.355 + 0.002*SL
B to Y	t_R	0.060	0.046 + 0.007*SL	0.050 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.057	0.046 + 0.006*SL	0.052 + 0.004*SL	0.047 + 0.004*SL
	t_{PLH}	0.335	0.325 + 0.005*SL	0.330 + 0.003*SL	0.338 + 0.003*SL
	t_{PHL}	0.347	0.338 + 0.005*SL	0.344 + 0.003*SL	0.362 + 0.002*SL
C to Y	t_R	0.061	0.049 + 0.006*SL	0.048 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.057	0.046 + 0.005*SL	0.051 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.351	0.342 + 0.005*SL	0.347 + 0.003*SL	0.355 + 0.003*SL
	t_{PHL}	0.350	0.341 + 0.005*SL	0.347 + 0.003*SL	0.365 + 0.002*SL
D to Y	t_R	0.061	0.048 + 0.007*SL	0.049 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.057	0.046 + 0.005*SL	0.052 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.348	0.339 + 0.005*SL	0.344 + 0.003*SL	0.351 + 0.003*SL
	t_{PHL}	0.357	0.348 + 0.005*SL	0.354 + 0.003*SL	0.372 + 0.002*SL
E to Y	t_R	0.062	0.051 + 0.006*SL	0.049 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.057	0.048 + 0.005*SL	0.049 + 0.004*SL	0.048 + 0.004*SL
	t_{PLH}	0.272	0.263 + 0.005*SL	0.268 + 0.003*SL	0.276 + 0.003*SL
	t_{PHL}	0.273	0.263 + 0.005*SL	0.270 + 0.003*SL	0.288 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

SCG4_LP/SCG4D2_LP/SCG4D4_LP

Two (two 2-ANDs into 2-NOR)s into 2-NAND with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
1	1	x	x	x	x	x	x	1
x	x	1	1	x	x	x	x	1
x	x	x	x	1	1	x	x	1
x	x	x	x	x	x	1	1	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
SCG4_LP								*SCG4_LP*
A	B	C	D	E	F	G	H	
0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	3.67
SCG4D2_LP								*SCG4D2_LP*
A	B	C	D	E	F	G	H	
1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	5.00
SCG4D4_LP								*SCG4D4_LP*
A	B	C	D	E	F	G	H	
1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	6.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.124	0.076 + 0.024*SL	0.070 + 0.026*SL	0.056 + 0.026*SL
	t_F	0.134	0.081 + 0.026*SL	0.084 + 0.025*SL	0.071 + 0.026*SL
	t_{PLH}	0.215	0.184 + 0.015*SL	0.194 + 0.013*SL	0.200 + 0.012*SL
	t_{PHL}	0.261	0.225 + 0.018*SL	0.239 + 0.015*SL	0.254 + 0.014*SL
B to Y	t_R	0.123	0.074 + 0.024*SL	0.070 + 0.026*SL	0.055 + 0.026*SL
	t_F	0.135	0.084 + 0.025*SL	0.084 + 0.025*SL	0.073 + 0.026*SL
	t_{PLH}	0.210	0.180 + 0.015*SL	0.190 + 0.013*SL	0.195 + 0.012*SL
	t_{PHL}	0.274	0.237 + 0.018*SL	0.252 + 0.015*SL	0.266 + 0.014*SL
C to Y	t_R	0.126	0.077 + 0.024*SL	0.072 + 0.026*SL	0.059 + 0.026*SL
	t_F	0.134	0.081 + 0.026*SL	0.084 + 0.025*SL	0.072 + 0.026*SL
	t_{PLH}	0.263	0.232 + 0.015*SL	0.242 + 0.013*SL	0.248 + 0.012*SL
	t_{PHL}	0.308	0.271 + 0.018*SL	0.285 + 0.015*SL	0.300 + 0.014*SL
D to Y	t_R	0.127	0.078 + 0.024*SL	0.073 + 0.026*SL	0.059 + 0.026*SL
	t_F	0.135	0.084 + 0.026*SL	0.085 + 0.025*SL	0.073 + 0.026*SL
	t_{PLH}	0.261	0.231 + 0.015*SL	0.241 + 0.013*SL	0.247 + 0.012*SL
	t_{PHL}	0.321	0.284 + 0.018*SL	0.298 + 0.015*SL	0.313 + 0.014*SL
E to Y	t_R	0.131	0.082 + 0.024*SL	0.077 + 0.026*SL	0.064 + 0.026*SL
	t_F	0.122	0.071 + 0.026*SL	0.070 + 0.026*SL	0.063 + 0.026*SL
	t_{PLH}	0.221	0.192 + 0.014*SL	0.199 + 0.013*SL	0.204 + 0.012*SL
	t_{PHL}	0.254	0.221 + 0.017*SL	0.230 + 0.015*SL	0.241 + 0.014*SL
F to Y	t_R	0.131	0.082 + 0.024*SL	0.077 + 0.026*SL	0.064 + 0.026*SL
	t_F	0.123	0.071 + 0.026*SL	0.072 + 0.026*SL	0.063 + 0.026*SL
	t_{PLH}	0.216	0.187 + 0.015*SL	0.195 + 0.013*SL	0.199 + 0.012*SL
	t_{PHL}	0.267	0.233 + 0.017*SL	0.243 + 0.015*SL	0.254 + 0.014*SL
G to Y	t_R	0.137	0.087 + 0.025*SL	0.084 + 0.026*SL	0.070 + 0.026*SL
	t_F	0.122	0.071 + 0.026*SL	0.070 + 0.026*SL	0.063 + 0.026*SL
	t_{PLH}	0.262	0.232 + 0.015*SL	0.241 + 0.013*SL	0.248 + 0.012*SL
	t_{PHL}	0.301	0.267 + 0.017*SL	0.277 + 0.015*SL	0.288 + 0.014*SL
H to Y	t_R	0.137	0.087 + 0.025*SL	0.085 + 0.025*SL	0.070 + 0.026*SL
	t_F	0.123	0.071 + 0.026*SL	0.072 + 0.026*SL	0.063 + 0.026*SL
	t_{PLH}	0.261	0.231 + 0.015*SL	0.240 + 0.013*SL	0.247 + 0.012*SL
	t_{PHL}	0.314	0.280 + 0.017*SL	0.290 + 0.015*SL	0.301 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG4D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.100	0.076 + 0.012*SL	0.074 + 0.012*SL	0.064 + 0.013*SL
	t_F	0.110	0.082 + 0.014*SL	0.087 + 0.013*SL	0.085 + 0.013*SL
	t_{PLH}	0.201	0.183 + 0.009*SL	0.191 + 0.007*SL	0.202 + 0.006*SL
	t_{PHL}	0.257	0.236 + 0.011*SL	0.245 + 0.008*SL	0.265 + 0.007*SL
B to Y	t_R	0.099	0.073 + 0.013*SL	0.076 + 0.012*SL	0.065 + 0.013*SL
	t_F	0.113	0.085 + 0.014*SL	0.089 + 0.013*SL	0.087 + 0.013*SL
	t_{PLH}	0.198	0.181 + 0.009*SL	0.189 + 0.007*SL	0.199 + 0.006*SL
	t_{PHL}	0.273	0.251 + 0.011*SL	0.261 + 0.008*SL	0.281 + 0.007*SL
C to Y	t_R	0.103	0.078 + 0.012*SL	0.078 + 0.012*SL	0.068 + 0.013*SL
	t_F	0.111	0.083 + 0.014*SL	0.087 + 0.013*SL	0.085 + 0.013*SL
	t_{PLH}	0.253	0.236 + 0.009*SL	0.244 + 0.007*SL	0.254 + 0.006*SL
	t_{PHL}	0.313	0.292 + 0.011*SL	0.301 + 0.008*SL	0.321 + 0.007*SL
D to Y	t_R	0.102	0.077 + 0.013*SL	0.079 + 0.012*SL	0.068 + 0.013*SL
	t_F	0.113	0.086 + 0.014*SL	0.089 + 0.013*SL	0.087 + 0.013*SL
	t_{PLH}	0.251	0.234 + 0.009*SL	0.241 + 0.007*SL	0.252 + 0.006*SL
	t_{PHL}	0.327	0.306 + 0.011*SL	0.316 + 0.008*SL	0.335 + 0.007*SL
E to Y	t_R	0.111	0.086 + 0.013*SL	0.087 + 0.012*SL	0.077 + 0.013*SL
	t_F	0.100	0.072 + 0.014*SL	0.076 + 0.013*SL	0.072 + 0.013*SL
	t_{PLH}	0.217	0.200 + 0.009*SL	0.207 + 0.007*SL	0.217 + 0.006*SL
	t_{PHL}	0.263	0.243 + 0.010*SL	0.250 + 0.008*SL	0.264 + 0.007*SL
F to Y	t_R	0.112	0.087 + 0.012*SL	0.087 + 0.012*SL	0.077 + 0.013*SL
	t_F	0.102	0.076 + 0.013*SL	0.077 + 0.013*SL	0.073 + 0.013*SL
	t_{PLH}	0.214	0.197 + 0.008*SL	0.204 + 0.007*SL	0.214 + 0.006*SL
	t_{PHL}	0.276	0.257 + 0.010*SL	0.264 + 0.008*SL	0.278 + 0.007*SL
G to Y	t_R	0.116	0.090 + 0.013*SL	0.092 + 0.012*SL	0.082 + 0.013*SL
	t_F	0.099	0.072 + 0.014*SL	0.076 + 0.013*SL	0.071 + 0.013*SL
	t_{PLH}	0.258	0.241 + 0.009*SL	0.248 + 0.007*SL	0.260 + 0.006*SL
	t_{PHL}	0.308	0.289 + 0.010*SL	0.296 + 0.008*SL	0.310 + 0.007*SL
H to Y	t_R	0.116	0.092 + 0.012*SL	0.091 + 0.012*SL	0.082 + 0.013*SL
	t_F	0.101	0.074 + 0.014*SL	0.078 + 0.013*SL	0.072 + 0.013*SL
	t_{PLH}	0.260	0.242 + 0.009*SL	0.249 + 0.007*SL	0.261 + 0.006*SL
	t_{PHL}	0.327	0.308 + 0.010*SL	0.315 + 0.008*SL	0.329 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG4D4_LP

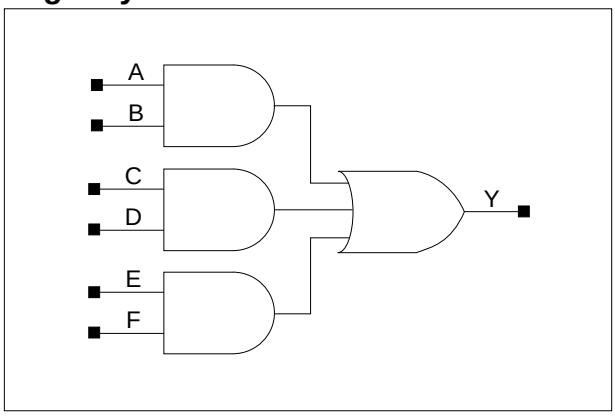
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.103	0.090 + 0.007*SL	0.092 + 0.006*SL	0.086 + 0.006*SL
	t_F	0.123	0.108 + 0.007*SL	0.112 + 0.007*SL	0.117 + 0.006*SL
	t_{PLH}	0.238	0.227 + 0.006*SL	0.233 + 0.004*SL	0.255 + 0.003*SL
	t_{PHL}	0.325	0.312 + 0.007*SL	0.319 + 0.005*SL	0.351 + 0.004*SL
B to Y	t_R	0.105	0.091 + 0.007*SL	0.094 + 0.006*SL	0.086 + 0.006*SL
	t_F	0.125	0.109 + 0.008*SL	0.114 + 0.007*SL	0.119 + 0.006*SL
	t_{PLH}	0.236	0.225 + 0.006*SL	0.231 + 0.004*SL	0.253 + 0.003*SL
	t_{PHL}	0.342	0.328 + 0.007*SL	0.336 + 0.005*SL	0.368 + 0.004*SL
C to Y	t_R	0.107	0.093 + 0.007*SL	0.096 + 0.006*SL	0.088 + 0.006*SL
	t_F	0.121	0.105 + 0.008*SL	0.111 + 0.007*SL	0.117 + 0.006*SL
	t_{PLH}	0.289	0.278 + 0.006*SL	0.284 + 0.004*SL	0.306 + 0.003*SL
	t_{PHL}	0.381	0.368 + 0.007*SL	0.375 + 0.005*SL	0.407 + 0.004*SL
D to Y	t_R	0.107	0.093 + 0.007*SL	0.096 + 0.006*SL	0.089 + 0.006*SL
	t_F	0.125	0.110 + 0.007*SL	0.114 + 0.007*SL	0.120 + 0.006*SL
	t_{PLH}	0.287	0.275 + 0.006*SL	0.282 + 0.004*SL	0.304 + 0.003*SL
	t_{PHL}	0.396	0.382 + 0.007*SL	0.390 + 0.005*SL	0.422 + 0.004*SL
E to Y	t_R	0.117	0.104 + 0.007*SL	0.106 + 0.006*SL	0.099 + 0.006*SL
	t_F	0.111	0.097 + 0.007*SL	0.098 + 0.007*SL	0.100 + 0.006*SL
	t_{PLH}	0.258	0.247 + 0.005*SL	0.253 + 0.004*SL	0.273 + 0.003*SL
	t_{PHL}	0.332	0.319 + 0.006*SL	0.326 + 0.004*SL	0.350 + 0.004*SL
F to Y	t_R	0.116	0.103 + 0.006*SL	0.104 + 0.006*SL	0.099 + 0.006*SL
	t_F	0.112	0.098 + 0.007*SL	0.101 + 0.006*SL	0.101 + 0.006*SL
	t_{PLH}	0.255	0.245 + 0.005*SL	0.250 + 0.004*SL	0.270 + 0.003*SL
	t_{PHL}	0.345	0.333 + 0.006*SL	0.340 + 0.004*SL	0.364 + 0.004*SL
G to Y	t_R	0.121	0.108 + 0.007*SL	0.110 + 0.006*SL	0.104 + 0.006*SL
	t_F	0.110	0.096 + 0.007*SL	0.097 + 0.007*SL	0.099 + 0.006*SL
	t_{PLH}	0.298	0.287 + 0.005*SL	0.293 + 0.004*SL	0.314 + 0.003*SL
	t_{PHL}	0.376	0.364 + 0.006*SL	0.370 + 0.004*SL	0.394 + 0.004*SL
H to Y	t_R	0.121	0.107 + 0.007*SL	0.111 + 0.006*SL	0.105 + 0.006*SL
	t_F	0.112	0.099 + 0.007*SL	0.099 + 0.007*SL	0.101 + 0.006*SL
	t_{PLH}	0.299	0.288 + 0.005*SL	0.294 + 0.004*SL	0.315 + 0.003*SL
	t_{PHL}	0.395	0.383 + 0.006*SL	0.390 + 0.004*SL	0.414 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

SCG5_LP/SCG5D2_LP/SCG5D4_LP

Three 2-ANDs into 3-OR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	1
x	x	1	1	x	x	1
x	x	x	x	1	1	1
Other States						0

Cell Data

Input Load (SL)						Gate Count
SCG5_LP						*SCG5_LP*
A	B	C	D	E	F	
0.8	0.8	0.8	0.8	0.9	0.8	3.00
SCG5D2_LP						*SCG5D2_LP*
A	B	C	D	E	F	
0.9	0.9	0.9	0.9	1.0	0.9	3.67
SCG5D4_LP						*SCG5D4_LP*
A	B	C	D	E	F	
1.0	1.0	1.0	1.0	1.0	1.0	4.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG5_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.129	0.079 + 0.025*SL	0.078 + 0.025*SL	0.059 + 0.026*SL
	t_F	0.119	0.078 + 0.020*SL	0.089 + 0.017*SL	0.098 + 0.017*SL
	t_{PLH}	0.245	0.210 + 0.017*SL	0.227 + 0.013*SL	0.239 + 0.012*SL
	t_{PHL}	0.275	0.240 + 0.018*SL	0.261 + 0.012*SL	0.300 + 0.010*SL
B to Y	t_R	0.129	0.081 + 0.024*SL	0.077 + 0.025*SL	0.059 + 0.026*SL
	t_F	0.121	0.080 + 0.020*SL	0.093 + 0.017*SL	0.099 + 0.017*SL
	t_{PLH}	0.241	0.207 + 0.017*SL	0.223 + 0.013*SL	0.235 + 0.012*SL
	t_{PHL}	0.289	0.254 + 0.018*SL	0.275 + 0.012*SL	0.314 + 0.010*SL
C to Y	t_R	0.133	0.084 + 0.024*SL	0.081 + 0.025*SL	0.062 + 0.026*SL
	t_F	0.121	0.081 + 0.020*SL	0.091 + 0.017*SL	0.099 + 0.017*SL
	t_{PLH}	0.323	0.289 + 0.017*SL	0.305 + 0.013*SL	0.317 + 0.012*SL
	t_{PHL}	0.374	0.339 + 0.018*SL	0.360 + 0.012*SL	0.399 + 0.010*SL
D to Y	t_R	0.133	0.083 + 0.025*SL	0.082 + 0.025*SL	0.062 + 0.026*SL
	t_F	0.122	0.080 + 0.021*SL	0.094 + 0.017*SL	0.100 + 0.017*SL
	t_{PLH}	0.320	0.285 + 0.017*SL	0.302 + 0.013*SL	0.314 + 0.012*SL
	t_{PHL}	0.386	0.351 + 0.018*SL	0.373 + 0.012*SL	0.412 + 0.010*SL
E to Y	t_R	0.140	0.090 + 0.025*SL	0.090 + 0.025*SL	0.075 + 0.026*SL
	t_F	0.121	0.081 + 0.020*SL	0.091 + 0.017*SL	0.099 + 0.017*SL
	t_{PLH}	0.381	0.345 + 0.018*SL	0.363 + 0.014*SL	0.379 + 0.013*SL
	t_{PHL}	0.420	0.385 + 0.018*SL	0.406 + 0.012*SL	0.445 + 0.010*SL
F to Y	t_R	0.140	0.088 + 0.026*SL	0.089 + 0.025*SL	0.076 + 0.026*SL
	t_F	0.122	0.082 + 0.020*SL	0.094 + 0.017*SL	0.100 + 0.017*SL
	t_{PLH}	0.379	0.343 + 0.018*SL	0.361 + 0.014*SL	0.377 + 0.013*SL
	t_{PHL}	0.434	0.398 + 0.018*SL	0.420 + 0.012*SL	0.459 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG5D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.109	0.080 + 0.014*SL	0.089 + 0.012*SL	0.084 + 0.013*SL
	t_F	0.110	0.086 + 0.012*SL	0.097 + 0.010*SL	0.115 + 0.009*SL
	t_{PLH}	0.263	0.240 + 0.012*SL	0.255 + 0.008*SL	0.281 + 0.006*SL
	t_{PHL}	0.304	0.280 + 0.012*SL	0.296 + 0.008*SL	0.333 + 0.006*SL
B to Y	t_R	0.109	0.080 + 0.014*SL	0.088 + 0.012*SL	0.084 + 0.013*SL
	t_F	0.112	0.086 + 0.013*SL	0.099 + 0.010*SL	0.118 + 0.008*SL
	t_{PLH}	0.261	0.238 + 0.012*SL	0.253 + 0.008*SL	0.278 + 0.006*SL
	t_{PHL}	0.319	0.295 + 0.012*SL	0.311 + 0.008*SL	0.349 + 0.006*SL
C to Y	t_R	0.113	0.084 + 0.014*SL	0.092 + 0.012*SL	0.088 + 0.013*SL
	t_F	0.111	0.086 + 0.013*SL	0.099 + 0.010*SL	0.115 + 0.009*SL
	t_{PLH}	0.349	0.325 + 0.012*SL	0.341 + 0.008*SL	0.366 + 0.006*SL
	t_{PHL}	0.412	0.388 + 0.012*SL	0.404 + 0.008*SL	0.441 + 0.006*SL
D to Y	t_R	0.113	0.084 + 0.014*SL	0.092 + 0.012*SL	0.087 + 0.013*SL
	t_F	0.113	0.089 + 0.012*SL	0.100 + 0.010*SL	0.118 + 0.008*SL
	t_{PLH}	0.346	0.322 + 0.012*SL	0.337 + 0.008*SL	0.363 + 0.006*SL
	t_{PHL}	0.424	0.400 + 0.012*SL	0.416 + 0.008*SL	0.454 + 0.006*SL
E to Y	t_R	0.118	0.089 + 0.015*SL	0.098 + 0.012*SL	0.095 + 0.013*SL
	t_F	0.111	0.085 + 0.013*SL	0.098 + 0.010*SL	0.116 + 0.009*SL
	t_{PLH}	0.410	0.385 + 0.012*SL	0.401 + 0.008*SL	0.429 + 0.007*SL
	t_{PHL}	0.459	0.435 + 0.012*SL	0.451 + 0.008*SL	0.488 + 0.006*SL
F to Y	t_R	0.119	0.089 + 0.015*SL	0.097 + 0.013*SL	0.096 + 0.013*SL
	t_F	0.114	0.090 + 0.012*SL	0.099 + 0.010*SL	0.118 + 0.008*SL
	t_{PLH}	0.408	0.383 + 0.012*SL	0.399 + 0.008*SL	0.427 + 0.007*SL
	t_{PHL}	0.472	0.448 + 0.012*SL	0.464 + 0.008*SL	0.501 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG5D4_LP

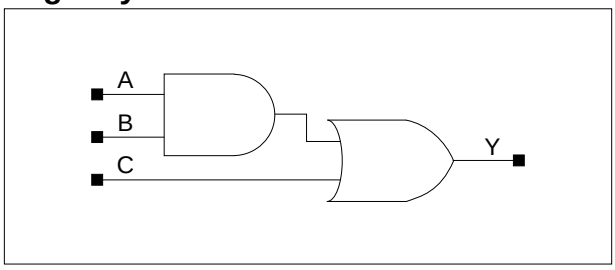
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.111	0.094 + 0.009*SL	0.102 + 0.006*SL	0.110 + 0.006*SL
	t_F	0.123	0.109 + 0.007*SL	0.117 + 0.005*SL	0.146 + 0.004*SL
	t_{PLH}	0.303	0.288 + 0.007*SL	0.299 + 0.005*SL	0.339 + 0.003*SL
	t_{PHL}	0.365	0.350 + 0.008*SL	0.361 + 0.005*SL	0.411 + 0.003*SL
B to Y	t_R	0.109	0.092 + 0.009*SL	0.100 + 0.007*SL	0.111 + 0.006*SL
	t_F	0.124	0.109 + 0.007*SL	0.118 + 0.005*SL	0.147 + 0.004*SL
	t_{PLH}	0.300	0.285 + 0.007*SL	0.296 + 0.005*SL	0.336 + 0.003*SL
	t_{PHL}	0.377	0.362 + 0.008*SL	0.373 + 0.005*SL	0.424 + 0.003*SL
C to Y	t_R	0.114	0.097 + 0.008*SL	0.105 + 0.007*SL	0.115 + 0.006*SL
	t_F	0.122	0.108 + 0.007*SL	0.116 + 0.005*SL	0.145 + 0.004*SL
	t_{PLH}	0.394	0.380 + 0.007*SL	0.391 + 0.005*SL	0.431 + 0.003*SL
	t_{PHL}	0.475	0.460 + 0.008*SL	0.471 + 0.005*SL	0.521 + 0.003*SL
D to Y	t_R	0.115	0.098 + 0.009*SL	0.107 + 0.006*SL	0.115 + 0.006*SL
	t_F	0.126	0.112 + 0.007*SL	0.119 + 0.005*SL	0.148 + 0.004*SL
	t_{PLH}	0.392	0.377 + 0.007*SL	0.388 + 0.005*SL	0.429 + 0.003*SL
	t_{PHL}	0.489	0.473 + 0.008*SL	0.485 + 0.005*SL	0.535 + 0.003*SL
E to Y	t_R	0.120	0.102 + 0.009*SL	0.111 + 0.007*SL	0.122 + 0.006*SL
	t_F	0.122	0.108 + 0.007*SL	0.116 + 0.005*SL	0.144 + 0.004*SL
	t_{PLH}	0.456	0.441 + 0.008*SL	0.452 + 0.005*SL	0.494 + 0.003*SL
	t_{PHL}	0.518	0.503 + 0.008*SL	0.514 + 0.005*SL	0.564 + 0.003*SL
F to Y	t_R	0.120	0.102 + 0.009*SL	0.111 + 0.007*SL	0.121 + 0.006*SL
	t_F	0.126	0.112 + 0.007*SL	0.119 + 0.005*SL	0.148 + 0.004*SL
	t_{PLH}	0.454	0.439 + 0.008*SL	0.450 + 0.005*SL	0.492 + 0.003*SL
	t_{PHL}	0.533	0.517 + 0.008*SL	0.529 + 0.005*SL	0.579 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 31, *Group3 : 31 < SL

SCG6_LP/SCG6D2_LP

2-AND into 2-OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	1
x	x	1	1
Other States			0

Cell Data

Input Load (SL)						Gate Count	
SCG6_LP			*SCG6D2_LP*			*SCG6_LP*	*SCG6D2_LP*
A	B	C	A	B	C		
0.9	0.9	0.9	1.1	1.1	1.1	1.67	2.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.056 + 0.022*SL	0.041 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.090	0.054 + 0.018*SL	0.060 + 0.017*SL	0.050 + 0.017*SL
	t_{PLH}	0.156	0.128 + 0.014*SL	0.134 + 0.013*SL	0.136 + 0.012*SL
	t_{PHL}	0.208	0.180 + 0.014*SL	0.195 + 0.011*SL	0.212 + 0.010*SL
B to Y	t_R	0.102	0.058 + 0.022*SL	0.041 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.093	0.057 + 0.018*SL	0.062 + 0.017*SL	0.052 + 0.017*SL
	t_{PLH}	0.153	0.125 + 0.014*SL	0.131 + 0.013*SL	0.133 + 0.012*SL
	t_{PHL}	0.228	0.199 + 0.015*SL	0.215 + 0.011*SL	0.233 + 0.010*SL
C to Y	t_R	0.091	0.041 + 0.025*SL	0.036 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.092	0.057 + 0.017*SL	0.060 + 0.017*SL	0.052 + 0.017*SL
	t_{PLH}	0.161	0.134 + 0.013*SL	0.137 + 0.013*SL	0.139 + 0.012*SL
	t_{PHL}	0.267	0.237 + 0.015*SL	0.253 + 0.011*SL	0.272 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG6D2_LP

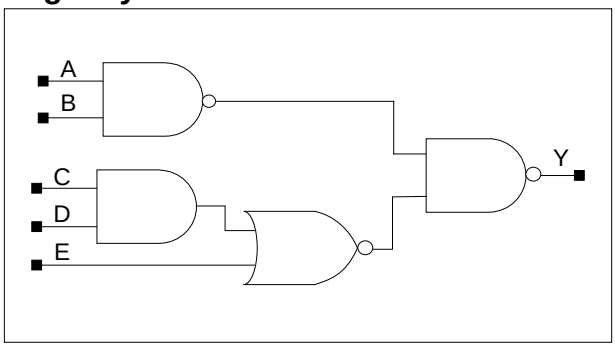
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.075	0.051 + 0.012*SL	0.049 + 0.013*SL	0.039 + 0.013*SL
	t_F	0.076	0.055 + 0.011*SL	0.063 + 0.009*SL	0.065 + 0.008*SL
	t_{PLH}	0.161	0.144 + 0.009*SL	0.151 + 0.007*SL	0.158 + 0.006*SL
	t_{PHL}	0.214	0.195 + 0.009*SL	0.207 + 0.006*SL	0.230 + 0.005*SL
B to Y	t_R	0.073	0.047 + 0.013*SL	0.049 + 0.013*SL	0.039 + 0.013*SL
	t_F	0.078	0.056 + 0.011*SL	0.066 + 0.008*SL	0.068 + 0.008*SL
	t_{PLH}	0.157	0.140 + 0.009*SL	0.148 + 0.007*SL	0.155 + 0.006*SL
	t_{PHL}	0.232	0.213 + 0.010*SL	0.225 + 0.006*SL	0.248 + 0.005*SL
C to Y	t_R	0.066	0.041 + 0.012*SL	0.039 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.078	0.058 + 0.010*SL	0.064 + 0.009*SL	0.067 + 0.008*SL
	t_{PLH}	0.161	0.146 + 0.008*SL	0.151 + 0.006*SL	0.154 + 0.006*SL
	t_{PHL}	0.270	0.251 + 0.010*SL	0.264 + 0.006*SL	0.287 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG7_LP/SCG7D2_LP

2-NAND and (2-AND into 2-NOR) into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
1	1	x	x	x	1
x	x	1	1	x	1
x	x	x	x	1	1
Other States					0

Cell Data

Input Load (SL)										Gate Count	
SCG7_LP					*SCG7D2_LP*					*SCG7_LP*	*SCG7D2_LP*
A	B	C	D	E	A	B	C	D	E		
0.7	0.7	0.7	0.7	0.7	1.0	1.1	1.1	1.1	1.0	3.00	3.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG7_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.108	0.057 + 0.025*SL	0.054 + 0.026*SL	0.045 + 0.027*SL
	t_F	0.108	0.058 + 0.025*SL	0.054 + 0.026*SL	0.047 + 0.026*SL
	t_{PLH}	0.165	0.138 + 0.014*SL	0.142 + 0.013*SL	0.145 + 0.012*SL
	t_{PHL}	0.190	0.159 + 0.015*SL	0.165 + 0.014*SL	0.168 + 0.014*SL
B to Y	t_R	0.108	0.058 + 0.025*SL	0.053 + 0.026*SL	0.045 + 0.027*SL
	t_F	0.109	0.058 + 0.025*SL	0.057 + 0.026*SL	0.048 + 0.026*SL
	t_{PLH}	0.162	0.135 + 0.014*SL	0.139 + 0.013*SL	0.142 + 0.012*SL
	t_{PHL}	0.200	0.170 + 0.015*SL	0.175 + 0.014*SL	0.178 + 0.014*SL
C to Y	t_R	0.123	0.075 + 0.024*SL	0.069 + 0.026*SL	0.058 + 0.027*SL
	t_F	0.117	0.066 + 0.025*SL	0.065 + 0.026*SL	0.057 + 0.026*SL
	t_{PLH}	0.206	0.178 + 0.014*SL	0.184 + 0.013*SL	0.186 + 0.012*SL
	t_{PHL}	0.236	0.203 + 0.016*SL	0.212 + 0.014*SL	0.221 + 0.014*SL
D to Y	t_R	0.123	0.074 + 0.025*SL	0.069 + 0.026*SL	0.057 + 0.027*SL
	t_F	0.119	0.068 + 0.025*SL	0.067 + 0.026*SL	0.057 + 0.026*SL
	t_{PLH}	0.203	0.175 + 0.014*SL	0.181 + 0.013*SL	0.184 + 0.012*SL
	t_{PHL}	0.250	0.217 + 0.017*SL	0.226 + 0.014*SL	0.235 + 0.014*SL
E to Y	t_R	0.122	0.073 + 0.024*SL	0.066 + 0.026*SL	0.057 + 0.027*SL
	t_F	0.118	0.066 + 0.026*SL	0.067 + 0.026*SL	0.057 + 0.026*SL
	t_{PLH}	0.238	0.211 + 0.014*SL	0.215 + 0.013*SL	0.218 + 0.012*SL
	t_{PHL}	0.288	0.255 + 0.017*SL	0.264 + 0.014*SL	0.273 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG7D2_LP

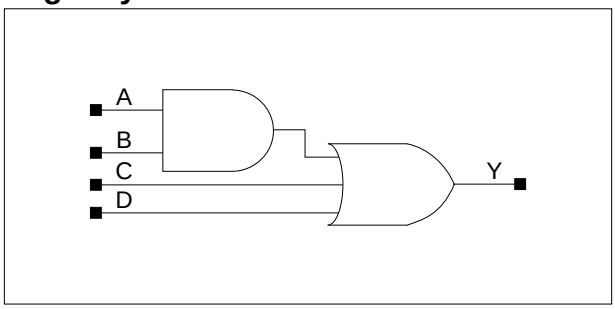
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.088	0.064 + 0.012*SL	0.061 + 0.013*SL	0.053 + 0.013*SL
	t_F	0.086	0.062 + 0.012*SL	0.060 + 0.013*SL	0.054 + 0.013*SL
	t_{PLH}	0.165	0.150 + 0.008*SL	0.155 + 0.007*SL	0.161 + 0.006*SL
	t_{PHL}	0.186	0.169 + 0.009*SL	0.174 + 0.007*SL	0.180 + 0.007*SL
B to Y	t_R	0.087	0.062 + 0.012*SL	0.060 + 0.013*SL	0.052 + 0.013*SL
	t_F	0.086	0.060 + 0.013*SL	0.062 + 0.013*SL	0.053 + 0.013*SL
	t_{PLH}	0.161	0.146 + 0.008*SL	0.151 + 0.007*SL	0.157 + 0.006*SL
	t_{PHL}	0.196	0.179 + 0.009*SL	0.184 + 0.007*SL	0.190 + 0.007*SL
C to Y	t_R	0.102	0.078 + 0.012*SL	0.076 + 0.012*SL	0.066 + 0.013*SL
	t_F	0.096	0.071 + 0.013*SL	0.071 + 0.013*SL	0.066 + 0.013*SL
	t_{PLH}	0.201	0.185 + 0.008*SL	0.190 + 0.007*SL	0.197 + 0.006*SL
	t_{PHL}	0.240	0.221 + 0.009*SL	0.228 + 0.008*SL	0.240 + 0.007*SL
D to Y	t_R	0.101	0.077 + 0.012*SL	0.074 + 0.013*SL	0.066 + 0.013*SL
	t_F	0.097	0.069 + 0.014*SL	0.074 + 0.013*SL	0.068 + 0.013*SL
	t_{PLH}	0.197	0.182 + 0.008*SL	0.187 + 0.007*SL	0.193 + 0.006*SL
	t_{PHL}	0.255	0.236 + 0.010*SL	0.243 + 0.008*SL	0.256 + 0.007*SL
E to Y	t_R	0.100	0.076 + 0.012*SL	0.075 + 0.012*SL	0.063 + 0.013*SL
	t_F	0.098	0.073 + 0.012*SL	0.072 + 0.013*SL	0.068 + 0.013*SL
	t_{PLH}	0.238	0.223 + 0.008*SL	0.228 + 0.007*SL	0.232 + 0.006*SL
	t_{PHL}	0.294	0.275 + 0.010*SL	0.282 + 0.008*SL	0.294 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG8_LP/SCG8D2_LP

2-AND into 3-OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	1
x	x	1	x	1
x	x	x	1	1
	Other States			0

Cell Data

Input Load (SL)								Gate Count	
SCG8_LP				*SCG8D2_LP*				*SCG8_LP*	*SCG8D2_LP*
A	B	C	D	A	B	C	D		
0.9	1.0	0.9	0.9	1.1	1.1	1.1	1.1	2.00	2.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.101	0.052 + 0.025*SL	0.047 + 0.026*SL	0.037 + 0.027*SL
	t_F	0.114	0.073 + 0.020*SL	0.086 + 0.017*SL	0.091 + 0.017*SL
	t_{PLH}	0.171	0.143 + 0.014*SL	0.149 + 0.013*SL	0.151 + 0.012*SL
	t_{PHL}	0.258	0.224 + 0.017*SL	0.245 + 0.012*SL	0.282 + 0.010*SL
B to Y	t_R	0.102	0.053 + 0.025*SL	0.047 + 0.026*SL	0.037 + 0.027*SL
	t_F	0.117	0.076 + 0.021*SL	0.090 + 0.017*SL	0.094 + 0.017*SL
	t_{PLH}	0.168	0.140 + 0.014*SL	0.146 + 0.013*SL	0.148 + 0.012*SL
	t_{PHL}	0.284	0.249 + 0.018*SL	0.271 + 0.012*SL	0.308 + 0.010*SL
C to Y	t_R	0.098	0.049 + 0.025*SL	0.043 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.118	0.076 + 0.021*SL	0.091 + 0.017*SL	0.095 + 0.017*SL
	t_{PLH}	0.182	0.155 + 0.013*SL	0.159 + 0.013*SL	0.161 + 0.012*SL
	t_{PHL}	0.364	0.329 + 0.018*SL	0.351 + 0.012*SL	0.388 + 0.010*SL
D to Y	t_R	0.099	0.050 + 0.025*SL	0.044 + 0.026*SL	0.039 + 0.027*SL
	t_F	0.118	0.076 + 0.021*SL	0.091 + 0.017*SL	0.095 + 0.017*SL
	t_{PLH}	0.191	0.163 + 0.014*SL	0.168 + 0.013*SL	0.171 + 0.012*SL
	t_{PHL}	0.382	0.347 + 0.018*SL	0.369 + 0.012*SL	0.406 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG8D2_LP

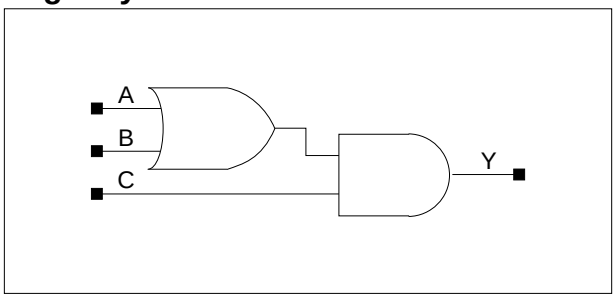
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.075	0.050 + 0.012*SL	0.050 + 0.012*SL	0.040 + 0.013*SL
	t_F	0.099	0.075 + 0.012*SL	0.086 + 0.010*SL	0.103 + 0.008*SL
	t_{PLH}	0.169	0.151 + 0.009*SL	0.160 + 0.007*SL	0.168 + 0.006*SL
	t_{PHL}	0.271	0.248 + 0.012*SL	0.263 + 0.008*SL	0.299 + 0.006*SL
B to Y	t_R	0.076	0.052 + 0.012*SL	0.050 + 0.013*SL	0.041 + 0.013*SL
	t_F	0.103	0.078 + 0.013*SL	0.091 + 0.009*SL	0.107 + 0.008*SL
	t_{PLH}	0.165	0.148 + 0.009*SL	0.156 + 0.007*SL	0.164 + 0.006*SL
	t_{PHL}	0.297	0.273 + 0.012*SL	0.289 + 0.008*SL	0.325 + 0.006*SL
C to Y	t_R	0.071	0.048 + 0.012*SL	0.044 + 0.013*SL	0.034 + 0.013*SL
	t_F	0.104	0.080 + 0.012*SL	0.091 + 0.009*SL	0.107 + 0.008*SL
	t_{PLH}	0.176	0.160 + 0.008*SL	0.166 + 0.006*SL	0.170 + 0.006*SL
	t_{PHL}	0.382	0.359 + 0.012*SL	0.375 + 0.008*SL	0.411 + 0.006*SL
D to Y	t_R	0.073	0.050 + 0.012*SL	0.046 + 0.013*SL	0.037 + 0.013*SL
	t_F	0.103	0.079 + 0.012*SL	0.091 + 0.009*SL	0.107 + 0.008*SL
	t_{PLH}	0.187	0.170 + 0.008*SL	0.177 + 0.007*SL	0.182 + 0.006*SL
	t_{PHL}	0.403	0.379 + 0.012*SL	0.395 + 0.008*SL	0.431 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG9_LP/SCG9D2_LP

2-OR into 2-AND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	x	0
x	x	0	0
Other States			1

Cell Data

Input Load (SL)						Gate Count	
SCG9_LP			*SCG9D2_LP*			*SCG9_LP*	*SCG9D2_LP*
A	B	C	A	B	C		
0.8	0.8	1.0	1.0	1.0	1.1	1.67	2.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG9_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.097	0.047 + 0.025*SL	0.042 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.090	0.054 + 0.018*SL	0.060 + 0.017*SL	0.050 + 0.017*SL
	t_{PLH}	0.161	0.133 + 0.014*SL	0.139 + 0.013*SL	0.141 + 0.012*SL
	t_{PHL}	0.215	0.186 + 0.014*SL	0.202 + 0.011*SL	0.219 + 0.010*SL
B to Y	t_R	0.098	0.049 + 0.025*SL	0.044 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.091	0.054 + 0.018*SL	0.060 + 0.017*SL	0.050 + 0.017*SL
	t_{PLH}	0.180	0.151 + 0.014*SL	0.158 + 0.013*SL	0.161 + 0.012*SL
	t_{PHL}	0.235	0.206 + 0.015*SL	0.222 + 0.011*SL	0.239 + 0.010*SL
C to Y	t_R	0.100	0.051 + 0.025*SL	0.046 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.082	0.048 + 0.017*SL	0.049 + 0.017*SL	0.041 + 0.017*SL
	t_{PLH}	0.172	0.143 + 0.014*SL	0.150 + 0.013*SL	0.153 + 0.012*SL
	t_{PHL}	0.182	0.155 + 0.014*SL	0.169 + 0.010*SL	0.182 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG9D2_LP

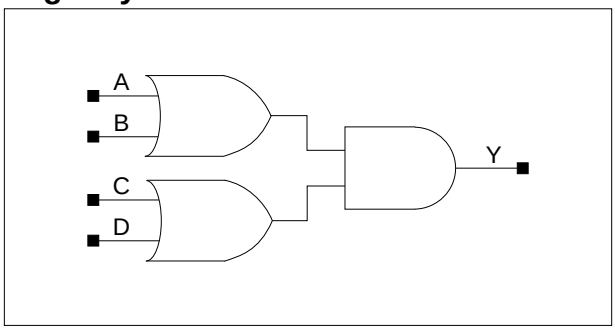
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.075	0.051 + 0.012*SL	0.049 + 0.013*SL	0.040 + 0.013*SL
	t_F	0.078	0.057 + 0.010*SL	0.064 + 0.009*SL	0.067 + 0.008*SL
	t_{PLH}	0.168	0.150 + 0.009*SL	0.158 + 0.007*SL	0.166 + 0.006*SL
	t_{PHL}	0.223	0.204 + 0.010*SL	0.217 + 0.006*SL	0.240 + 0.005*SL
B to Y	t_R	0.079	0.053 + 0.013*SL	0.055 + 0.012*SL	0.044 + 0.013*SL
	t_F	0.078	0.057 + 0.010*SL	0.064 + 0.009*SL	0.067 + 0.008*SL
	t_{PLH}	0.188	0.170 + 0.009*SL	0.178 + 0.007*SL	0.187 + 0.006*SL
	t_{PHL}	0.245	0.225 + 0.010*SL	0.238 + 0.006*SL	0.261 + 0.005*SL
C to Y	t_R	0.078	0.053 + 0.012*SL	0.053 + 0.013*SL	0.043 + 0.013*SL
	t_F	0.064	0.045 + 0.010*SL	0.049 + 0.009*SL	0.052 + 0.008*SL
	t_{PLH}	0.186	0.168 + 0.009*SL	0.176 + 0.007*SL	0.185 + 0.006*SL
	t_{PHL}	0.178	0.161 + 0.008*SL	0.170 + 0.006*SL	0.190 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG10_LP/SCG10D2_LP

Two 2-ORs into 2-AND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
SCG10_LP				*SCG10D2_LP*				*SCG10_LP*	*SCG10D2_LP*
A	B	C	D	A	B	C	D		
0.8	0.8	0.7	0.8	1.1	1.1	1.1	1.1	2.33	2.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG10_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.110	0.062 + 0.024*SL	0.056 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.109	0.066 + 0.022*SL	0.085 + 0.017*SL	0.087 + 0.017*SL
	t_{PLH}	0.223	0.192 + 0.015*SL	0.203 + 0.013*SL	0.208 + 0.012*SL
	t_{PHL}	0.235	0.199 + 0.018*SL	0.224 + 0.012*SL	0.261 + 0.010*SL
B to Y	t_R	0.113	0.065 + 0.024*SL	0.059 + 0.026*SL	0.045 + 0.026*SL
	t_F	0.109	0.066 + 0.022*SL	0.084 + 0.017*SL	0.087 + 0.017*SL
	t_{PLH}	0.246	0.214 + 0.016*SL	0.226 + 0.013*SL	0.232 + 0.012*SL
	t_{PHL}	0.256	0.220 + 0.018*SL	0.244 + 0.012*SL	0.282 + 0.010*SL
C to Y	t_R	0.111	0.063 + 0.024*SL	0.057 + 0.026*SL	0.043 + 0.026*SL
	t_F	0.113	0.069 + 0.022*SL	0.089 + 0.017*SL	0.092 + 0.017*SL
	t_{PLH}	0.230	0.199 + 0.015*SL	0.210 + 0.013*SL	0.216 + 0.012*SL
	t_{PHL}	0.264	0.227 + 0.018*SL	0.253 + 0.012*SL	0.292 + 0.010*SL
D to Y	t_R	0.114	0.065 + 0.024*SL	0.060 + 0.025*SL	0.045 + 0.026*SL
	t_F	0.113	0.069 + 0.022*SL	0.089 + 0.017*SL	0.092 + 0.017*SL
	t_{PLH}	0.254	0.223 + 0.016*SL	0.235 + 0.013*SL	0.241 + 0.012*SL
	t_{PHL}	0.285	0.249 + 0.018*SL	0.274 + 0.012*SL	0.313 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG10D2_LP

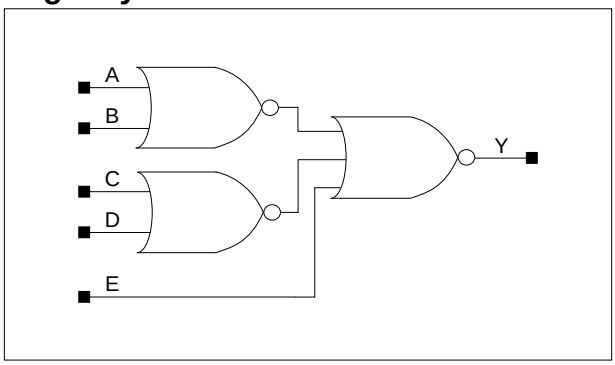
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.083	0.057 + 0.013*SL	0.061 + 0.012*SL	0.050 + 0.013*SL
	t_F	0.086	0.060 + 0.013*SL	0.075 + 0.009*SL	0.094 + 0.008*SL
	t_{PLH}	0.211	0.191 + 0.010*SL	0.202 + 0.007*SL	0.214 + 0.006*SL
	t_{PHL}	0.229	0.207 + 0.011*SL	0.221 + 0.008*SL	0.258 + 0.006*SL
B to Y	t_R	0.085	0.058 + 0.014*SL	0.063 + 0.012*SL	0.051 + 0.013*SL
	t_F	0.087	0.061 + 0.013*SL	0.075 + 0.009*SL	0.094 + 0.008*SL
	t_{PLH}	0.232	0.212 + 0.010*SL	0.223 + 0.007*SL	0.236 + 0.006*SL
	t_{PHL}	0.249	0.227 + 0.011*SL	0.241 + 0.008*SL	0.278 + 0.006*SL
C to Y	t_R	0.085	0.059 + 0.013*SL	0.060 + 0.012*SL	0.050 + 0.013*SL
	t_F	0.091	0.064 + 0.014*SL	0.081 + 0.009*SL	0.099 + 0.008*SL
	t_{PLH}	0.218	0.199 + 0.010*SL	0.209 + 0.007*SL	0.221 + 0.006*SL
	t_{PHL}	0.258	0.235 + 0.012*SL	0.251 + 0.008*SL	0.288 + 0.006*SL
D to Y	t_R	0.087	0.062 + 0.012*SL	0.062 + 0.012*SL	0.052 + 0.013*SL
	t_F	0.091	0.065 + 0.013*SL	0.079 + 0.009*SL	0.099 + 0.008*SL
	t_{PLH}	0.240	0.220 + 0.010*SL	0.231 + 0.007*SL	0.244 + 0.006*SL
	t_{PHL}	0.279	0.255 + 0.012*SL	0.271 + 0.008*SL	0.309 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG11_LP/SCG11D2_LP

Two 2-NORs into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	x	x	x	0
x	x	0	0	x	0
x	x	x	x	1	0
Other States					1

Cell Data

Input Load (SL)										Gate Count	
SCG11_LP					*SCG11D2_LP*					*SCG11_LP*	*SCG11D2_LP*
A	B	C	D	E	A	B	C	D	E		
0.9	0.9	0.9	0.9	1.0	1.2	1.2	1.1	1.1	1.9	3.00	4.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG11_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.301	0.139 + 0.081*SL	0.143 + 0.080*SL	0.147 + 0.080*SL
	t_F	0.119	0.067 + 0.026*SL	0.069 + 0.026*SL	0.055 + 0.027*SL
	t_{PLH}	0.194	0.114 + 0.040*SL	0.117 + 0.039*SL	0.120 + 0.039*SL
	t_{PHL}	0.246	0.209 + 0.019*SL	0.223 + 0.015*SL	0.234 + 0.014*SL
B to Y	t_R	0.301	0.139 + 0.081*SL	0.144 + 0.080*SL	0.147 + 0.080*SL
	t_F	0.119	0.068 + 0.026*SL	0.068 + 0.026*SL	0.055 + 0.026*SL
	t_{PLH}	0.205	0.125 + 0.040*SL	0.128 + 0.039*SL	0.131 + 0.039*SL
	t_{PHL}	0.267	0.229 + 0.019*SL	0.244 + 0.015*SL	0.254 + 0.014*SL
C to Y	t_R	0.309	0.151 + 0.079*SL	0.148 + 0.080*SL	0.147 + 0.080*SL
	t_F	0.139	0.087 + 0.026*SL	0.088 + 0.026*SL	0.076 + 0.027*SL
	t_{PLH}	0.248	0.169 + 0.039*SL	0.171 + 0.039*SL	0.172 + 0.039*SL
	t_{PHL}	0.269	0.233 + 0.018*SL	0.244 + 0.015*SL	0.254 + 0.015*SL
D to Y	t_R	0.309	0.151 + 0.079*SL	0.148 + 0.080*SL	0.147 + 0.080*SL
	t_F	0.140	0.088 + 0.026*SL	0.088 + 0.026*SL	0.076 + 0.027*SL
	t_{PLH}	0.259	0.180 + 0.039*SL	0.182 + 0.039*SL	0.183 + 0.039*SL
	t_{PHL}	0.289	0.254 + 0.018*SL	0.264 + 0.015*SL	0.274 + 0.015*SL
E to Y	t_R	0.310	0.153 + 0.079*SL	0.149 + 0.080*SL	0.147 + 0.080*SL
	t_F	0.149	0.100 + 0.024*SL	0.094 + 0.026*SL	0.080 + 0.027*SL
	t_{PLH}	0.247	0.168 + 0.039*SL	0.169 + 0.039*SL	0.171 + 0.039*SL
	t_{PHL}	0.131	0.098 + 0.016*SL	0.102 + 0.015*SL	0.111 + 0.015*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG11D2_LP

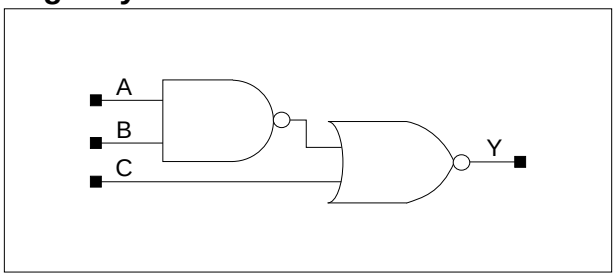
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.229	0.149 + 0.040*SL	0.148 + 0.040*SL	0.154 + 0.040*SL
	t_F	0.101	0.075 + 0.013*SL	0.077 + 0.013*SL	0.073 + 0.013*SL
	t_{PLH}	0.182	0.142 + 0.020*SL	0.143 + 0.020*SL	0.146 + 0.020*SL
	t_{PHL}	0.243	0.222 + 0.011*SL	0.231 + 0.008*SL	0.247 + 0.007*SL
B to Y	t_R	0.229	0.149 + 0.040*SL	0.149 + 0.040*SL	0.155 + 0.040*SL
	t_F	0.101	0.074 + 0.013*SL	0.076 + 0.013*SL	0.073 + 0.013*SL
	t_{PLH}	0.195	0.155 + 0.020*SL	0.156 + 0.020*SL	0.159 + 0.020*SL
	t_{PHL}	0.265	0.244 + 0.011*SL	0.253 + 0.008*SL	0.269 + 0.007*SL
C to Y	t_R	0.238	0.160 + 0.039*SL	0.158 + 0.040*SL	0.156 + 0.040*SL
	t_F	0.121	0.096 + 0.013*SL	0.096 + 0.013*SL	0.092 + 0.013*SL
	t_{PLH}	0.238	0.198 + 0.020*SL	0.199 + 0.020*SL	0.200 + 0.020*SL
	t_{PHL}	0.266	0.246 + 0.010*SL	0.253 + 0.008*SL	0.266 + 0.007*SL
D to Y	t_R	0.239	0.160 + 0.039*SL	0.158 + 0.040*SL	0.156 + 0.040*SL
	t_F	0.121	0.096 + 0.013*SL	0.096 + 0.013*SL	0.092 + 0.013*SL
	t_{PLH}	0.251	0.211 + 0.020*SL	0.212 + 0.020*SL	0.213 + 0.020*SL
	t_{PHL}	0.288	0.268 + 0.010*SL	0.275 + 0.008*SL	0.288 + 0.007*SL
E to Y	t_R	0.240	0.162 + 0.039*SL	0.159 + 0.040*SL	0.156 + 0.040*SL
	t_F	0.127	0.104 + 0.012*SL	0.099 + 0.013*SL	0.090 + 0.013*SL
	t_{PLH}	0.213	0.174 + 0.020*SL	0.174 + 0.020*SL	0.176 + 0.020*SL
	t_{PHL}	0.116	0.099 + 0.008*SL	0.101 + 0.008*SL	0.108 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG12_LP/SCG12D2_LP/SCG12D4_LP

2-NAND into 2-NOR with 1X/2X/4X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	0	1
Other States			0

Cell Data

Input Load (SL)									Gate Count		
SCG12_LP			*SCG12D2_LP*			*SCG12D4_LP*			*SCG12_LP*	*SCG12D2_LP*	*SCG12D4_LP*
A	B	C	A	B	C	A	B	C			
0.8	0.8	1.2	0.8	0.9	2.4	0.6	0.6	0.8	1.67	2.33	3.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG12_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.195	0.091 + 0.052*SL	0.086 + 0.053*SL	0.085 + 0.053*SL
	t_F	0.072	0.041 + 0.016*SL	0.042 + 0.015*SL	0.032 + 0.016*SL
	t_{PLH}	0.185	0.132 + 0.026*SL	0.134 + 0.026*SL	0.137 + 0.026*SL
	t_{PHL}	0.174	0.152 + 0.011*SL	0.160 + 0.009*SL	0.166 + 0.009*SL
B to Y	t_R	0.195	0.091 + 0.052*SL	0.086 + 0.053*SL	0.085 + 0.053*SL
	t_F	0.074	0.042 + 0.016*SL	0.044 + 0.015*SL	0.033 + 0.016*SL
	t_{PLH}	0.184	0.131 + 0.027*SL	0.133 + 0.026*SL	0.136 + 0.026*SL
	t_{PHL}	0.189	0.167 + 0.011*SL	0.175 + 0.009*SL	0.181 + 0.009*SL
C to Y	t_R	0.199	0.096 + 0.051*SL	0.089 + 0.053*SL	0.085 + 0.053*SL
	t_F	0.099	0.073 + 0.013*SL	0.066 + 0.015*SL	0.045 + 0.016*SL
	t_{PLH}	0.166	0.114 + 0.026*SL	0.115 + 0.026*SL	0.117 + 0.026*SL
	t_{PHL}	0.088	0.064 + 0.012*SL	0.075 + 0.009*SL	0.078 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG12D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.138	0.087 + 0.026*SL	0.084 + 0.026*SL	0.078 + 0.027*SL
	t_F	0.066	0.051 + 0.008*SL	0.050 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.177	0.150 + 0.014*SL	0.152 + 0.013*SL	0.155 + 0.013*SL
	t_{PHL}	0.190	0.176 + 0.007*SL	0.184 + 0.005*SL	0.197 + 0.004*SL
B to Y	t_R	0.137	0.086 + 0.026*SL	0.083 + 0.026*SL	0.078 + 0.027*SL
	t_F	0.067	0.049 + 0.009*SL	0.055 + 0.007*SL	0.049 + 0.008*SL
	t_{PLH}	0.175	0.148 + 0.014*SL	0.150 + 0.013*SL	0.152 + 0.013*SL
	t_{PHL}	0.204	0.190 + 0.007*SL	0.198 + 0.005*SL	0.212 + 0.004*SL
C to Y	t_R	0.140	0.090 + 0.025*SL	0.086 + 0.026*SL	0.078 + 0.027*SL
	t_F	0.083	0.069 + 0.007*SL	0.069 + 0.007*SL	0.056 + 0.008*SL
	t_{PLH}	0.137	0.110 + 0.014*SL	0.112 + 0.013*SL	0.114 + 0.013*SL
	t_{PHL}	0.072	0.058 + 0.007*SL	0.066 + 0.005*SL	0.074 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG12D4_LP

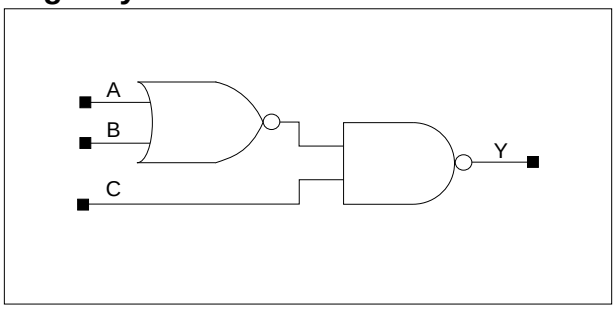
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.061	0.048 + 0.007*SL	0.050 + 0.006*SL	0.037 + 0.007*SL
	t_F	0.056	0.047 + 0.004*SL	0.047 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.327	0.317 + 0.005*SL	0.323 + 0.003*SL	0.330 + 0.003*SL
	t_{PHL}	0.307	0.298 + 0.005*SL	0.304 + 0.003*SL	0.321 + 0.002*SL
B to Y	t_R	0.061	0.048 + 0.007*SL	0.051 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.055	0.045 + 0.005*SL	0.047 + 0.004*SL	0.046 + 0.004*SL
	t_{PLH}	0.325	0.316 + 0.005*SL	0.321 + 0.003*SL	0.328 + 0.003*SL
	t_{PHL}	0.319	0.310 + 0.005*SL	0.317 + 0.003*SL	0.334 + 0.002*SL
C to Y	t_R	0.061	0.048 + 0.007*SL	0.050 + 0.006*SL	0.036 + 0.007*SL
	t_F	0.055	0.046 + 0.005*SL	0.048 + 0.004*SL	0.045 + 0.004*SL
	t_{PLH}	0.296	0.287 + 0.005*SL	0.292 + 0.003*SL	0.300 + 0.003*SL
	t_{PHL}	0.233	0.224 + 0.005*SL	0.230 + 0.003*SL	0.247 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

SCG13_LP/SCG13D2_LP

2-NOR into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	1	0
Other States			1

Cell Data

Input Load (SL)						Gate Count	
SCG13_LP			*SCG13D2_LP*			*SCG13_LP*	*SCG13D2_LP*
A	B	C	A	B	C		
0.7	0.8	1.2	1.0	1.0	2.3	1.67	2.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG13_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.107	0.058 + 0.025*SL	0.053 + 0.026*SL	0.044 + 0.027*SL
	t_F	0.122	0.072 + 0.025*SL	0.070 + 0.026*SL	0.058 + 0.026*SL
	t_{PLH}	0.176	0.150 + 0.013*SL	0.153 + 0.013*SL	0.155 + 0.012*SL
	t_{PHL}	0.220	0.186 + 0.017*SL	0.196 + 0.014*SL	0.204 + 0.014*SL
B to Y	t_R	0.110	0.061 + 0.025*SL	0.055 + 0.026*SL	0.047 + 0.027*SL
	t_F	0.121	0.070 + 0.025*SL	0.069 + 0.026*SL	0.058 + 0.026*SL
	t_{PLH}	0.199	0.172 + 0.014*SL	0.176 + 0.013*SL	0.179 + 0.012*SL
	t_{PHL}	0.241	0.208 + 0.017*SL	0.218 + 0.014*SL	0.225 + 0.014*SL
C to Y	t_R	0.130	0.085 + 0.023*SL	0.074 + 0.025*SL	0.051 + 0.027*SL
	t_F	0.116	0.067 + 0.025*SL	0.061 + 0.026*SL	0.049 + 0.027*SL
	t_{PLH}	0.114	0.087 + 0.013*SL	0.091 + 0.012*SL	0.091 + 0.012*SL
	t_{PHL}	0.096	0.063 + 0.016*SL	0.072 + 0.014*SL	0.075 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG13D2_LP

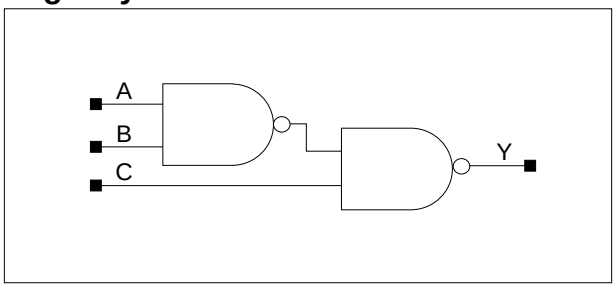
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.087	0.065 + 0.011*SL	0.059 + 0.013*SL	0.051 + 0.013*SL
	t_F	0.102	0.076 + 0.013*SL	0.076 + 0.013*SL	0.072 + 0.013*SL
	t_{PLH}	0.179	0.164 + 0.008*SL	0.168 + 0.006*SL	0.173 + 0.006*SL
	t_{PHL}	0.225	0.205 + 0.010*SL	0.213 + 0.008*SL	0.226 + 0.007*SL
B to Y	t_R	0.090	0.065 + 0.012*SL	0.064 + 0.012*SL	0.053 + 0.013*SL
	t_F	0.101	0.076 + 0.013*SL	0.075 + 0.013*SL	0.072 + 0.013*SL
	t_{PLH}	0.203	0.187 + 0.008*SL	0.192 + 0.007*SL	0.197 + 0.006*SL
	t_{PHL}	0.247	0.227 + 0.010*SL	0.235 + 0.008*SL	0.249 + 0.007*SL
C to Y	t_R	0.106	0.085 + 0.010*SL	0.079 + 0.012*SL	0.062 + 0.013*SL
	t_F	0.090	0.064 + 0.013*SL	0.065 + 0.013*SL	0.056 + 0.013*SL
	t_{PLH}	0.098	0.082 + 0.008*SL	0.088 + 0.006*SL	0.090 + 0.006*SL
	t_{PHL}	0.077	0.059 + 0.009*SL	0.066 + 0.007*SL	0.072 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG14_LP/SCG14D2_LP

2-NAND into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	1	0
x	0	1	0
Other States			1

Cell Data

Input Load (SL)						Gate Count	
SCG14_LP			*SCG14D2_LP*			*SCG14_LP*	*SCG14D2_LP*
A	B	C	A	B	C		
0.7	0.7	1.2	1.0	1.0	2.3	1.67	2.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG14_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.111	0.062 + 0.025*SL	0.057 + 0.026*SL	0.047 + 0.027*SL
	t_F	0.109	0.059 + 0.025*SL	0.055 + 0.026*SL	0.046 + 0.027*SL
	t_{PLH}	0.179	0.151 + 0.014*SL	0.157 + 0.013*SL	0.160 + 0.012*SL
	t_{PHL}	0.187	0.157 + 0.015*SL	0.162 + 0.014*SL	0.164 + 0.014*SL
B to Y	t_R	0.112	0.062 + 0.025*SL	0.058 + 0.026*SL	0.048 + 0.027*SL
	t_F	0.109	0.060 + 0.025*SL	0.054 + 0.026*SL	0.046 + 0.027*SL
	t_{PLH}	0.176	0.148 + 0.014*SL	0.154 + 0.013*SL	0.156 + 0.012*SL
	t_{PHL}	0.197	0.166 + 0.015*SL	0.171 + 0.014*SL	0.174 + 0.014*SL
C to Y	t_R	0.129	0.084 + 0.023*SL	0.074 + 0.025*SL	0.051 + 0.027*SL
	t_F	0.115	0.066 + 0.024*SL	0.060 + 0.026*SL	0.047 + 0.027*SL
	t_{PLH}	0.114	0.087 + 0.013*SL	0.091 + 0.012*SL	0.092 + 0.012*SL
	t_{PHL}	0.095	0.063 + 0.016*SL	0.071 + 0.014*SL	0.074 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG14D2_LP

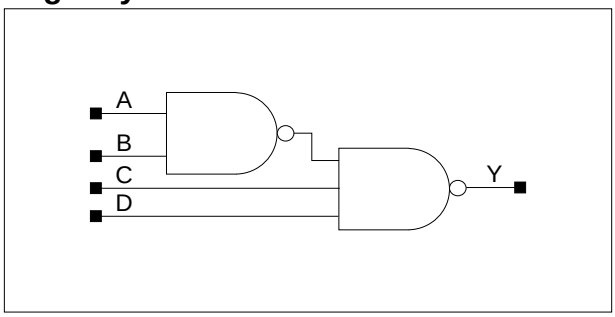
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.089	0.064 + 0.013*SL	0.064 + 0.013*SL	0.054 + 0.013*SL
	t_F	0.087	0.063 + 0.012*SL	0.060 + 0.013*SL	0.053 + 0.013*SL
	t_{PLH}	0.169	0.153 + 0.008*SL	0.158 + 0.007*SL	0.164 + 0.006*SL
	t_{PHL}	0.186	0.169 + 0.009*SL	0.174 + 0.007*SL	0.179 + 0.007*SL
B to Y	t_R	0.089	0.065 + 0.012*SL	0.062 + 0.013*SL	0.054 + 0.013*SL
	t_F	0.087	0.061 + 0.013*SL	0.062 + 0.013*SL	0.053 + 0.013*SL
	t_{PLH}	0.165	0.149 + 0.008*SL	0.155 + 0.007*SL	0.160 + 0.006*SL
	t_{PHL}	0.196	0.179 + 0.009*SL	0.184 + 0.007*SL	0.190 + 0.007*SL
C to Y	t_R	0.106	0.085 + 0.010*SL	0.078 + 0.012*SL	0.062 + 0.013*SL
	t_F	0.089	0.064 + 0.013*SL	0.064 + 0.013*SL	0.054 + 0.013*SL
	t_{PLH}	0.098	0.082 + 0.008*SL	0.088 + 0.006*SL	0.090 + 0.006*SL
	t_{PHL}	0.077	0.059 + 0.009*SL	0.066 + 0.007*SL	0.071 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG15_LP/SCG15D2_LP

2-NAND into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	1	1	0
x	0	1	1	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
SCG15_LP				*SCG15D2_LP*				*SCG15_LP*	*SCG15D2_LP*
A	B	C	D	A	B	C	D		
0.7	0.7	1.0	1.0	0.9	0.9	1.9	1.9	2.00	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG15_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.147	0.079 + 0.034*SL	0.072 + 0.036*SL	0.066 + 0.036*SL
	t_F	0.154	0.081 + 0.036*SL	0.077 + 0.037*SL	0.072 + 0.038*SL
	t_{PLH}	0.194	0.158 + 0.018*SL	0.162 + 0.017*SL	0.164 + 0.017*SL
	t_{PHL}	0.204	0.165 + 0.020*SL	0.167 + 0.019*SL	0.169 + 0.019*SL
B to Y	t_R	0.147	0.079 + 0.034*SL	0.072 + 0.036*SL	0.066 + 0.036*SL
	t_F	0.154	0.081 + 0.036*SL	0.077 + 0.037*SL	0.073 + 0.038*SL
	t_{PLH}	0.191	0.156 + 0.018*SL	0.159 + 0.017*SL	0.161 + 0.017*SL
	t_{PHL}	0.214	0.175 + 0.020*SL	0.177 + 0.019*SL	0.179 + 0.019*SL
C to Y	t_R	0.165	0.101 + 0.032*SL	0.088 + 0.035*SL	0.074 + 0.036*SL
	t_F	0.160	0.089 + 0.035*SL	0.083 + 0.037*SL	0.072 + 0.038*SL
	t_{PLH}	0.137	0.103 + 0.017*SL	0.104 + 0.017*SL	0.105 + 0.017*SL
	t_{PHL}	0.122	0.081 + 0.020*SL	0.085 + 0.019*SL	0.087 + 0.019*SL
D to Y	t_R	0.177	0.112 + 0.033*SL	0.101 + 0.035*SL	0.087 + 0.036*SL
	t_F	0.155	0.083 + 0.036*SL	0.079 + 0.037*SL	0.072 + 0.038*SL
	t_{PLH}	0.147	0.112 + 0.017*SL	0.113 + 0.017*SL	0.115 + 0.017*SL
	t_{PHL}	0.125	0.085 + 0.020*SL	0.088 + 0.019*SL	0.089 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG15D2_LP

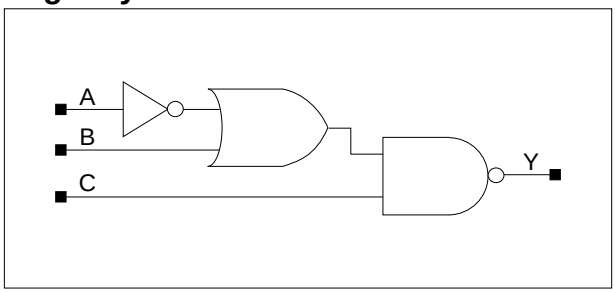
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.111	0.077 + 0.017*SL	0.074 + 0.018*SL	0.066 + 0.018*SL
	t_F	0.115	0.079 + 0.018*SL	0.079 + 0.018*SL	0.071 + 0.019*SL
	t_{PLH}	0.178	0.159 + 0.010*SL	0.163 + 0.009*SL	0.166 + 0.008*SL
	t_{PHL}	0.196	0.175 + 0.011*SL	0.178 + 0.010*SL	0.181 + 0.010*SL
B to Y	t_R	0.110	0.075 + 0.017*SL	0.075 + 0.018*SL	0.066 + 0.018*SL
	t_F	0.117	0.082 + 0.017*SL	0.079 + 0.018*SL	0.072 + 0.019*SL
	t_{PLH}	0.175	0.156 + 0.010*SL	0.160 + 0.009*SL	0.163 + 0.008*SL
	t_{PHL}	0.206	0.185 + 0.011*SL	0.188 + 0.010*SL	0.191 + 0.010*SL
C to Y	t_R	0.129	0.098 + 0.016*SL	0.093 + 0.017*SL	0.075 + 0.018*SL
	t_F	0.120	0.086 + 0.017*SL	0.082 + 0.018*SL	0.073 + 0.019*SL
	t_{PLH}	0.117	0.099 + 0.009*SL	0.101 + 0.009*SL	0.102 + 0.008*SL
	t_{PHL}	0.098	0.076 + 0.011*SL	0.082 + 0.010*SL	0.084 + 0.010*SL
D to Y	t_R	0.140	0.109 + 0.016*SL	0.103 + 0.017*SL	0.087 + 0.018*SL
	t_F	0.113	0.078 + 0.018*SL	0.076 + 0.018*SL	0.071 + 0.019*SL
	t_{PLH}	0.127	0.109 + 0.009*SL	0.110 + 0.009*SL	0.112 + 0.008*SL
	t_{PHL}	0.101	0.079 + 0.011*SL	0.084 + 0.010*SL	0.086 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG16_LP/SCG16D2_LP

2-OR with one Inverted Input into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	1	0
x	1	1	0
Other States			1

Cell Data

Input Load (SL)						Gate Count	
SCG16_LP			*SCG16D2_LP*			*SCG16_LP*	*SCG16D2_LP*
A	B	C	A	B	C		
0.7	1.1	1.1	1.0	2.2	2.1	2.00	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG16_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.227	0.120 + 0.053*SL	0.119 + 0.054*SL	0.119 + 0.054*SL
	t_F	0.140	0.077 + 0.031*SL	0.074 + 0.032*SL	0.069 + 0.032*SL
	t_{PLH}	0.187	0.134 + 0.027*SL	0.136 + 0.026*SL	0.139 + 0.026*SL
	t_{PHL}	0.209	0.174 + 0.018*SL	0.177 + 0.017*SL	0.179 + 0.017*SL
B to Y	t_R	0.232	0.127 + 0.052*SL	0.122 + 0.053*SL	0.119 + 0.054*SL
	t_F	0.172	0.113 + 0.029*SL	0.105 + 0.031*SL	0.090 + 0.032*SL
	t_{PLH}	0.182	0.129 + 0.026*SL	0.130 + 0.026*SL	0.132 + 0.026*SL
	t_{PHL}	0.138	0.103 + 0.018*SL	0.106 + 0.017*SL	0.109 + 0.017*SL
C to Y	t_R	0.142	0.096 + 0.023*SL	0.088 + 0.025*SL	0.068 + 0.027*SL
	t_F	0.164	0.104 + 0.030*SL	0.099 + 0.032*SL	0.090 + 0.032*SL
	t_{PLH}	0.124	0.099 + 0.013*SL	0.100 + 0.012*SL	0.101 + 0.012*SL
	t_{PHL}	0.144	0.108 + 0.018*SL	0.111 + 0.017*SL	0.115 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG16D2_LP

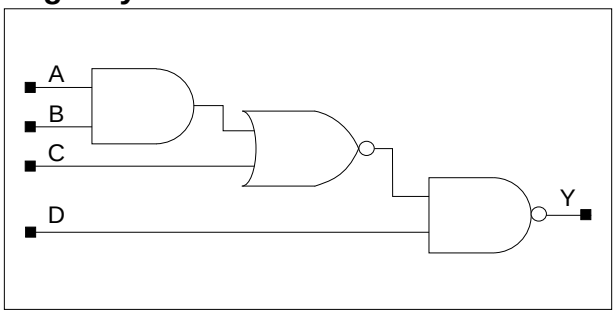
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.168	0.116 + 0.026*SL	0.113 + 0.027*SL	0.113 + 0.027*SL
	t_F	0.109	0.078 + 0.015*SL	0.076 + 0.016*SL	0.070 + 0.016*SL
	t_{PLH}	0.166	0.139 + 0.013*SL	0.141 + 0.013*SL	0.143 + 0.013*SL
	t_{PHL}	0.203	0.184 + 0.010*SL	0.187 + 0.009*SL	0.190 + 0.008*SL
B to Y	t_R	0.174	0.124 + 0.025*SL	0.119 + 0.026*SL	0.113 + 0.027*SL
	t_F	0.139	0.111 + 0.014*SL	0.107 + 0.015*SL	0.094 + 0.016*SL
	t_{PLH}	0.154	0.127 + 0.013*SL	0.128 + 0.013*SL	0.130 + 0.013*SL
	t_{PHL}	0.119	0.101 + 0.009*SL	0.102 + 0.009*SL	0.106 + 0.008*SL
C to Y	t_R	0.119	0.097 + 0.011*SL	0.092 + 0.012*SL	0.075 + 0.013*SL
	t_F	0.131	0.101 + 0.015*SL	0.098 + 0.016*SL	0.091 + 0.016*SL
	t_{PLH}	0.110	0.095 + 0.007*SL	0.099 + 0.006*SL	0.100 + 0.006*SL
	t_{PHL}	0.124	0.106 + 0.009*SL	0.107 + 0.009*SL	0.111 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG17_LP/SCG17D2_LP

2-AND into 2-NOR into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	0	1	0
x	0	0	1	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
SCG17_LP				*SCG17D2_LP*				*SCG17_LP*	*SCG17D2_LP*
A	B	C	D	A	B	C	D		
0.7	0.7	0.6	1.0	1.0	1.0	1.0	2.3	2.00	2.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG17_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.130	0.062 + 0.034*SL	0.057 + 0.036*SL	0.048 + 0.036*SL
	t_F	0.122	0.070 + 0.026*SL	0.071 + 0.026*SL	0.060 + 0.026*SL
	t_{PLH}	0.192	0.156 + 0.018*SL	0.161 + 0.017*SL	0.163 + 0.017*SL
	t_{PHL}	0.233	0.197 + 0.018*SL	0.211 + 0.015*SL	0.224 + 0.014*SL
B to Y	t_R	0.132	0.064 + 0.034*SL	0.057 + 0.036*SL	0.048 + 0.036*SL
	t_F	0.124	0.073 + 0.026*SL	0.074 + 0.025*SL	0.061 + 0.026*SL
	t_{PLH}	0.188	0.151 + 0.018*SL	0.157 + 0.017*SL	0.159 + 0.017*SL
	t_{PHL}	0.251	0.214 + 0.018*SL	0.229 + 0.015*SL	0.243 + 0.014*SL
C to Y	t_R	0.131	0.064 + 0.034*SL	0.056 + 0.036*SL	0.049 + 0.036*SL
	t_F	0.124	0.071 + 0.026*SL	0.075 + 0.025*SL	0.061 + 0.026*SL
	t_{PLH}	0.225	0.189 + 0.018*SL	0.193 + 0.017*SL	0.196 + 0.017*SL
	t_{PHL}	0.289	0.252 + 0.018*SL	0.267 + 0.015*SL	0.281 + 0.014*SL
D to Y	t_R	0.150	0.086 + 0.032*SL	0.072 + 0.035*SL	0.056 + 0.036*SL
	t_F	0.109	0.060 + 0.024*SL	0.054 + 0.026*SL	0.042 + 0.026*SL
	t_{PLH}	0.129	0.094 + 0.017*SL	0.096 + 0.017*SL	0.097 + 0.017*SL
	t_{PHL}	0.089	0.056 + 0.016*SL	0.065 + 0.014*SL	0.069 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

SCG17D2_LP

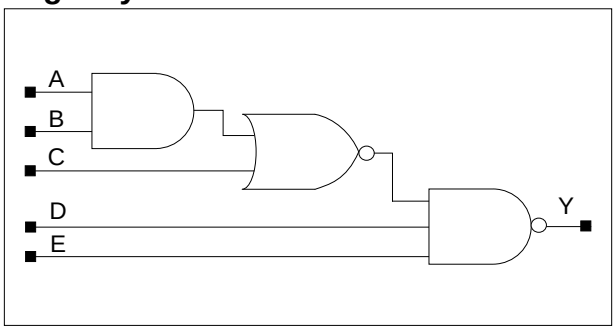
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.097	0.074 + 0.012*SL	0.071 + 0.013*SL	0.062 + 0.013*SL
	t_F	0.106	0.079 + 0.014*SL	0.083 + 0.013*SL	0.079 + 0.013*SL
	t_{PLH}	0.203	0.186 + 0.009*SL	0.193 + 0.007*SL	0.202 + 0.006*SL
	t_{PHL}	0.239	0.218 + 0.010*SL	0.227 + 0.008*SL	0.244 + 0.007*SL
B to Y	t_R	0.098	0.073 + 0.012*SL	0.073 + 0.012*SL	0.062 + 0.013*SL
	t_F	0.109	0.082 + 0.013*SL	0.084 + 0.013*SL	0.080 + 0.013*SL
	t_{PLH}	0.199	0.182 + 0.009*SL	0.189 + 0.007*SL	0.198 + 0.006*SL
	t_{PHL}	0.251	0.230 + 0.010*SL	0.239 + 0.008*SL	0.257 + 0.007*SL
C to Y	t_R	0.096	0.072 + 0.012*SL	0.072 + 0.012*SL	0.059 + 0.013*SL
	t_F	0.108	0.081 + 0.013*SL	0.083 + 0.013*SL	0.081 + 0.013*SL
	t_{PLH}	0.243	0.227 + 0.008*SL	0.233 + 0.007*SL	0.240 + 0.006*SL
	t_{PHL}	0.290	0.269 + 0.010*SL	0.278 + 0.008*SL	0.296 + 0.007*SL
D to Y	t_R	0.106	0.085 + 0.010*SL	0.079 + 0.012*SL	0.062 + 0.013*SL
	t_F	0.090	0.064 + 0.013*SL	0.064 + 0.013*SL	0.056 + 0.013*SL
	t_{PLH}	0.098	0.082 + 0.008*SL	0.088 + 0.006*SL	0.090 + 0.006*SL
	t_{PHL}	0.077	0.059 + 0.009*SL	0.066 + 0.007*SL	0.072 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

SCG18_LP/SCG18D2_LP

2-AND into 2-NOR into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	0	1	1	0
x	0	0	1	1	0
Other States					1

Cell Data

Input Load (SL)										Gate Count	
SCG18_LP					*SCG18D2_LP*					*SCG18_LP*	*SCG18D2_LP*
A	B	C	D	E	A	B	C	D	E		
0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0	1.9	2.0	2.33	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG18_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.157	0.090 + 0.034*SL	0.083 + 0.035*SL	0.072 + 0.036*SL
	t_F	0.169	0.098 + 0.036*SL	0.096 + 0.036*SL	0.085 + 0.037*SL
	t_{PLH}	0.236	0.199 + 0.019*SL	0.205 + 0.017*SL	0.208 + 0.017*SL
	t_{PHL}	0.249	0.206 + 0.021*SL	0.214 + 0.019*SL	0.220 + 0.019*SL
B to Y	t_R	0.158	0.091 + 0.034*SL	0.084 + 0.035*SL	0.072 + 0.036*SL
	t_F	0.171	0.100 + 0.036*SL	0.098 + 0.036*SL	0.086 + 0.037*SL
	t_{PLH}	0.232	0.195 + 0.019*SL	0.201 + 0.017*SL	0.204 + 0.017*SL
	t_{PHL}	0.259	0.216 + 0.022*SL	0.225 + 0.019*SL	0.231 + 0.019*SL
C to Y	t_R	0.152	0.084 + 0.034*SL	0.078 + 0.036*SL	0.070 + 0.036*SL
	t_F	0.171	0.100 + 0.036*SL	0.098 + 0.036*SL	0.086 + 0.037*SL
	t_{PLH}	0.251	0.215 + 0.018*SL	0.218 + 0.017*SL	0.221 + 0.017*SL
	t_{PHL}	0.298	0.255 + 0.022*SL	0.264 + 0.019*SL	0.270 + 0.019*SL
D to Y	t_R	0.167	0.103 + 0.032*SL	0.091 + 0.035*SL	0.076 + 0.036*SL
	t_F	0.161	0.090 + 0.035*SL	0.085 + 0.036*SL	0.075 + 0.037*SL
	t_{PLH}	0.138	0.104 + 0.017*SL	0.105 + 0.017*SL	0.106 + 0.017*SL
	t_{PHL}	0.123	0.083 + 0.020*SL	0.087 + 0.019*SL	0.090 + 0.019*SL
E to Y	t_R	0.179	0.114 + 0.033*SL	0.103 + 0.035*SL	0.089 + 0.036*SL
	t_F	0.156	0.085 + 0.036*SL	0.081 + 0.037*SL	0.075 + 0.037*SL
	t_{PLH}	0.147	0.113 + 0.017*SL	0.114 + 0.017*SL	0.116 + 0.017*SL
	t_{PHL}	0.124	0.084 + 0.020*SL	0.087 + 0.019*SL	0.090 + 0.019*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG18D2_LP

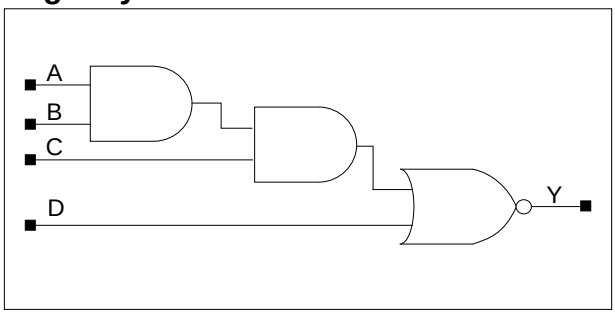
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.120	0.087 + 0.017*SL	0.085 + 0.017*SL	0.074 + 0.018*SL
	t_F	0.130	0.094 + 0.018*SL	0.096 + 0.018*SL	0.089 + 0.018*SL
	t_{PLH}	0.223	0.202 + 0.010*SL	0.208 + 0.009*SL	0.215 + 0.008*SL
	t_{PHL}	0.239	0.215 + 0.012*SL	0.222 + 0.010*SL	0.234 + 0.010*SL
B to Y	t_R	0.121	0.089 + 0.016*SL	0.085 + 0.017*SL	0.073 + 0.018*SL
	t_F	0.132	0.096 + 0.018*SL	0.098 + 0.018*SL	0.091 + 0.018*SL
	t_{PLH}	0.219	0.198 + 0.010*SL	0.204 + 0.009*SL	0.211 + 0.008*SL
	t_{PHL}	0.250	0.226 + 0.012*SL	0.234 + 0.010*SL	0.246 + 0.010*SL
C to Y	t_R	0.115	0.083 + 0.016*SL	0.078 + 0.017*SL	0.067 + 0.018*SL
	t_F	0.132	0.096 + 0.018*SL	0.097 + 0.018*SL	0.091 + 0.018*SL
	t_{PLH}	0.242	0.223 + 0.010*SL	0.227 + 0.009*SL	0.231 + 0.008*SL
	t_{PHL}	0.289	0.265 + 0.012*SL	0.272 + 0.010*SL	0.284 + 0.010*SL
D to Y	t_R	0.128	0.096 + 0.016*SL	0.092 + 0.017*SL	0.074 + 0.018*SL
	t_F	0.120	0.087 + 0.017*SL	0.082 + 0.018*SL	0.073 + 0.018*SL
	t_{PLH}	0.116	0.098 + 0.009*SL	0.100 + 0.008*SL	0.101 + 0.008*SL
	t_{PHL}	0.097	0.075 + 0.011*SL	0.081 + 0.010*SL	0.085 + 0.010*SL
E to Y	t_R	0.139	0.108 + 0.016*SL	0.103 + 0.017*SL	0.086 + 0.018*SL
	t_F	0.113	0.076 + 0.018*SL	0.076 + 0.018*SL	0.072 + 0.018*SL
	t_{PLH}	0.126	0.108 + 0.009*SL	0.109 + 0.009*SL	0.111 + 0.008*SL
	t_{PHL}	0.099	0.077 + 0.011*SL	0.081 + 0.010*SL	0.085 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

SCG19_LP/SCG19D2_LP

2-AND into 2-AND into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	1	x	0
x	x	x	1	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
SCG19_LP				*SCG19D2_LP*				*SCG19_LP*	*SCG19D2_LP*
A	B	C	D	A	B	C	D		
0.5	0.6	1.1	1.1	0.6	0.6	2.2	2.3	2.67	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG19_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.219	0.112 + 0.054*SL	0.112 + 0.054*SL	0.113 + 0.054*SL
	t_F	0.110	0.060 + 0.025*SL	0.055 + 0.026*SL	0.050 + 0.026*SL
	t_{PLH}	0.293	0.240 + 0.027*SL	0.242 + 0.026*SL	0.245 + 0.026*SL
	t_{PHL}	0.224	0.195 + 0.015*SL	0.198 + 0.014*SL	0.200 + 0.014*SL
B to Y	t_R	0.219	0.112 + 0.053*SL	0.112 + 0.054*SL	0.113 + 0.054*SL
	t_F	0.109	0.058 + 0.025*SL	0.055 + 0.026*SL	0.050 + 0.026*SL
	t_{PLH}	0.309	0.256 + 0.027*SL	0.259 + 0.026*SL	0.261 + 0.026*SL
	t_{PHL}	0.223	0.194 + 0.015*SL	0.197 + 0.014*SL	0.199 + 0.014*SL
C to Y	t_R	0.249	0.147 + 0.051*SL	0.136 + 0.054*SL	0.130 + 0.054*SL
	t_F	0.118	0.071 + 0.024*SL	0.063 + 0.026*SL	0.051 + 0.026*SL
	t_{PLH}	0.168	0.115 + 0.026*SL	0.116 + 0.026*SL	0.118 + 0.026*SL
	t_{PHL}	0.098	0.067 + 0.016*SL	0.074 + 0.014*SL	0.077 + 0.014*SL
D to Y	t_R	0.243	0.137 + 0.053*SL	0.133 + 0.054*SL	0.131 + 0.054*SL
	t_F	0.114	0.084 + 0.015*SL	0.079 + 0.016*SL	0.062 + 0.017*SL
	t_{PLH}	0.208	0.155 + 0.026*SL	0.156 + 0.026*SL	0.158 + 0.026*SL
	t_{PHL}	0.109	0.088 + 0.011*SL	0.092 + 0.010*SL	0.095 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG19D2_LP

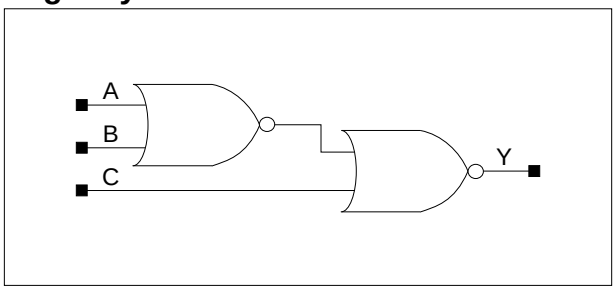
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.161	0.109 + 0.026*SL	0.107 + 0.027*SL	0.106 + 0.027*SL
	t_F	0.086	0.060 + 0.013*SL	0.060 + 0.013*SL	0.055 + 0.013*SL
	t_{PLH}	0.292	0.264 + 0.014*SL	0.266 + 0.013*SL	0.269 + 0.013*SL
	t_{PHL}	0.243	0.227 + 0.008*SL	0.231 + 0.007*SL	0.235 + 0.007*SL
B to Y	t_R	0.161	0.107 + 0.027*SL	0.107 + 0.027*SL	0.106 + 0.027*SL
	t_F	0.088	0.064 + 0.012*SL	0.061 + 0.013*SL	0.055 + 0.013*SL
	t_{PLH}	0.306	0.279 + 0.013*SL	0.280 + 0.013*SL	0.283 + 0.013*SL
	t_{PHL}	0.240	0.223 + 0.008*SL	0.227 + 0.007*SL	0.232 + 0.007*SL
C to Y	t_R	0.193	0.143 + 0.025*SL	0.137 + 0.026*SL	0.123 + 0.027*SL
	t_F	0.093	0.067 + 0.013*SL	0.067 + 0.013*SL	0.058 + 0.013*SL
	t_{PLH}	0.140	0.114 + 0.013*SL	0.114 + 0.013*SL	0.115 + 0.013*SL
	t_{PHL}	0.082	0.064 + 0.009*SL	0.071 + 0.007*SL	0.076 + 0.007*SL
D to Y	t_R	0.184	0.133 + 0.026*SL	0.129 + 0.027*SL	0.124 + 0.027*SL
	t_F	0.095	0.080 + 0.008*SL	0.081 + 0.008*SL	0.071 + 0.008*SL
	t_{PLH}	0.174	0.148 + 0.013*SL	0.149 + 0.013*SL	0.150 + 0.013*SL
	t_{PHL}	0.094	0.082 + 0.006*SL	0.086 + 0.005*SL	0.090 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

SCG20_LP/SCG20D2_LP

2-NOR into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	x	0	1
x	1	0	1
Other States			0

Cell Data

Input Load (SL)						Gate Count	
SCG20_LP			*SCG20D2_LP*			*SCG20_LP*	*SCG20D2_LP*
A	B	C	A	B	C		
0.8	0.8	1.2	1.1	1.1	2.4	1.67	2.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG20_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.192	0.087 + 0.053*SL	0.084 + 0.053*SL	0.084 + 0.053*SL
	t_F	0.088	0.055 + 0.017*SL	0.061 + 0.015*SL	0.052 + 0.016*SL
	t_{PLH}	0.184	0.131 + 0.026*SL	0.133 + 0.026*SL	0.136 + 0.026*SL
	t_{PHL}	0.211	0.184 + 0.013*SL	0.198 + 0.010*SL	0.214 + 0.009*SL
B to Y	t_R	0.193	0.087 + 0.053*SL	0.085 + 0.053*SL	0.085 + 0.053*SL
	t_F	0.088	0.056 + 0.016*SL	0.058 + 0.015*SL	0.051 + 0.016*SL
	t_{PLH}	0.199	0.146 + 0.026*SL	0.148 + 0.026*SL	0.151 + 0.026*SL
	t_{PHL}	0.233	0.206 + 0.013*SL	0.220 + 0.010*SL	0.235 + 0.009*SL
C to Y	t_R	0.198	0.096 + 0.051*SL	0.088 + 0.053*SL	0.084 + 0.053*SL
	t_F	0.099	0.072 + 0.013*SL	0.066 + 0.015*SL	0.045 + 0.016*SL
	t_{PLH}	0.166	0.113 + 0.026*SL	0.114 + 0.026*SL	0.116 + 0.026*SL
	t_{PHL}	0.088	0.065 + 0.012*SL	0.075 + 0.009*SL	0.078 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG20D2_LP

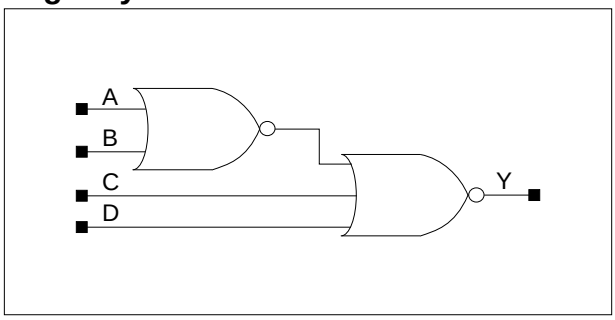
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.133	0.081 + 0.026*SL	0.077 + 0.027*SL	0.076 + 0.027*SL
	t_F	0.076	0.059 + 0.009*SL	0.063 + 0.008*SL	0.065 + 0.008*SL
	t_{PLH}	0.159	0.132 + 0.013*SL	0.133 + 0.013*SL	0.135 + 0.013*SL
	t_{PHL}	0.215	0.198 + 0.008*SL	0.208 + 0.006*SL	0.228 + 0.005*SL
B to Y	t_R	0.133	0.080 + 0.026*SL	0.078 + 0.027*SL	0.076 + 0.027*SL
	t_F	0.076	0.059 + 0.009*SL	0.063 + 0.008*SL	0.065 + 0.008*SL
	t_{PLH}	0.172	0.145 + 0.013*SL	0.147 + 0.013*SL	0.149 + 0.013*SL
	t_{PHL}	0.236	0.219 + 0.008*SL	0.230 + 0.006*SL	0.249 + 0.005*SL
C to Y	t_R	0.139	0.088 + 0.025*SL	0.084 + 0.026*SL	0.076 + 0.027*SL
	t_F	0.082	0.068 + 0.007*SL	0.068 + 0.007*SL	0.056 + 0.008*SL
	t_{PLH}	0.136	0.109 + 0.014*SL	0.111 + 0.013*SL	0.112 + 0.013*SL
	t_{PHL}	0.071	0.057 + 0.007*SL	0.066 + 0.005*SL	0.074 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG21_LP/SCG21D2_LP

2-NOR into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	x	0	0	1
x	1	0	0	1
Other States				0

Cell Data

Input Load (SL)								Gate Count	
SCG21_LP				*SCG21D2_LP*				*SCG21_LP*	*SCG21D2_LP*
A	B	C	D	A	B	C	D		
0.7	0.8	1.0	1.1	1.1	1.1	2.0	2.0	2.00	3.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG21_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.299	0.137 + 0.081*SL	0.140 + 0.080*SL	0.145 + 0.080*SL
	t_F	0.118	0.067 + 0.025*SL	0.066 + 0.026*SL	0.053 + 0.027*SL
	t_{PLH}	0.217	0.137 + 0.040*SL	0.139 + 0.039*SL	0.143 + 0.039*SL
	t_{PHL}	0.237	0.200 + 0.018*SL	0.214 + 0.015*SL	0.224 + 0.014*SL
B to Y	t_R	0.300	0.138 + 0.081*SL	0.141 + 0.080*SL	0.145 + 0.080*SL
	t_F	0.118	0.067 + 0.025*SL	0.065 + 0.026*SL	0.053 + 0.027*SL
	t_{PLH}	0.233	0.153 + 0.040*SL	0.155 + 0.039*SL	0.158 + 0.039*SL
	t_{PHL}	0.259	0.222 + 0.018*SL	0.236 + 0.015*SL	0.246 + 0.014*SL
C to Y	t_R	0.310	0.153 + 0.079*SL	0.147 + 0.080*SL	0.145 + 0.080*SL
	t_F	0.128	0.081 + 0.024*SL	0.073 + 0.026*SL	0.056 + 0.027*SL
	t_{PLH}	0.225	0.146 + 0.040*SL	0.147 + 0.039*SL	0.149 + 0.039*SL
	t_{PHL}	0.122	0.091 + 0.016*SL	0.095 + 0.015*SL	0.098 + 0.015*SL
D to Y	t_R	0.308	0.150 + 0.079*SL	0.146 + 0.080*SL	0.145 + 0.080*SL
	t_F	0.149	0.100 + 0.024*SL	0.093 + 0.026*SL	0.079 + 0.027*SL
	t_{PLH}	0.248	0.169 + 0.039*SL	0.170 + 0.039*SL	0.171 + 0.039*SL
	t_{PHL}	0.131	0.099 + 0.016*SL	0.103 + 0.015*SL	0.112 + 0.015*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG21D2_LP

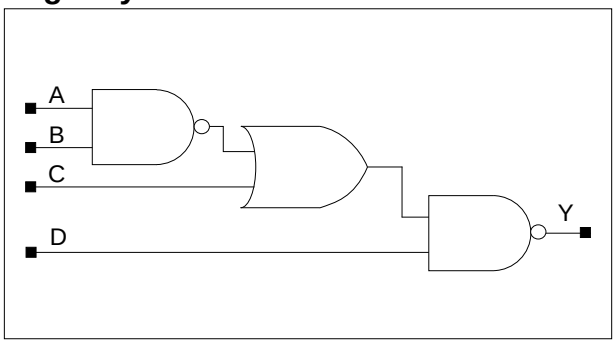
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.204	0.124 + 0.040*SL	0.123 + 0.040*SL	0.129 + 0.040*SL
	t_F	0.092	0.065 + 0.014*SL	0.068 + 0.013*SL	0.063 + 0.013*SL
	t_{PLH}	0.170	0.131 + 0.020*SL	0.130 + 0.020*SL	0.134 + 0.020*SL
	t_{PHL}	0.230	0.208 + 0.011*SL	0.219 + 0.008*SL	0.236 + 0.007*SL
B to Y	t_R	0.204	0.124 + 0.040*SL	0.124 + 0.040*SL	0.130 + 0.040*SL
	t_F	0.091	0.064 + 0.014*SL	0.067 + 0.013*SL	0.063 + 0.013*SL
	t_{PLH}	0.183	0.144 + 0.020*SL	0.144 + 0.020*SL	0.147 + 0.020*SL
	t_{PHL}	0.252	0.230 + 0.011*SL	0.241 + 0.008*SL	0.258 + 0.007*SL
C to Y	t_R	0.217	0.141 + 0.038*SL	0.135 + 0.040*SL	0.131 + 0.040*SL
	t_F	0.101	0.079 + 0.011*SL	0.073 + 0.012*SL	0.060 + 0.013*SL
	t_{PLH}	0.177	0.137 + 0.020*SL	0.138 + 0.020*SL	0.140 + 0.020*SL
	t_{PHL}	0.102	0.084 + 0.009*SL	0.090 + 0.007*SL	0.093 + 0.007*SL
D to Y	t_R	0.215	0.137 + 0.039*SL	0.134 + 0.040*SL	0.131 + 0.040*SL
	t_F	0.120	0.096 + 0.012*SL	0.093 + 0.013*SL	0.083 + 0.013*SL
	t_{PLH}	0.201	0.162 + 0.020*SL	0.163 + 0.020*SL	0.164 + 0.020*SL
	t_{PHL}	0.111	0.094 + 0.009*SL	0.097 + 0.008*SL	0.104 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG22_LP/SCG22D2_LP

2-NAND into 2-OR into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	0	x	1
x	x	x	0	1
Other States				0

Cell Data

Input Load (SL)								Gate Count	
SCG22_LP				*SCG22D2_LP*				*SCG22_LP*	*SCG22D2_LP*
A	B	C	D	A	B	C	D		
0.6	0.6	1.1	1.1	1.1	1.2	2.2	2.2	2.33	3.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

SCG22_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.237	0.133 + 0.052*SL	0.128 + 0.053*SL	0.126 + 0.054*SL
	t_F	0.143	0.082 + 0.031*SL	0.078 + 0.032*SL	0.072 + 0.032*SL
	t_{PLH}	0.233	0.180 + 0.027*SL	0.181 + 0.026*SL	0.184 + 0.026*SL
	t_{PHL}	0.222	0.186 + 0.018*SL	0.190 + 0.017*SL	0.192 + 0.017*SL
B to Y	t_R	0.237	0.132 + 0.052*SL	0.128 + 0.053*SL	0.126 + 0.054*SL
	t_F	0.145	0.084 + 0.030*SL	0.079 + 0.032*SL	0.072 + 0.032*SL
	t_{PLH}	0.230	0.177 + 0.027*SL	0.179 + 0.026*SL	0.182 + 0.026*SL
	t_{PHL}	0.232	0.197 + 0.018*SL	0.201 + 0.017*SL	0.203 + 0.017*SL
C to Y	t_R	0.238	0.134 + 0.052*SL	0.129 + 0.053*SL	0.126 + 0.054*SL
	t_F	0.173	0.116 + 0.029*SL	0.107 + 0.031*SL	0.092 + 0.032*SL
	t_{PLH}	0.186	0.134 + 0.026*SL	0.135 + 0.026*SL	0.137 + 0.026*SL
	t_{PHL}	0.139	0.104 + 0.017*SL	0.106 + 0.017*SL	0.110 + 0.017*SL
D to Y	t_R	0.145	0.098 + 0.023*SL	0.090 + 0.025*SL	0.071 + 0.027*SL
	t_F	0.166	0.106 + 0.030*SL	0.101 + 0.031*SL	0.092 + 0.032*SL
	t_{PLH}	0.126	0.101 + 0.013*SL	0.102 + 0.012*SL	0.103 + 0.012*SL
	t_{PHL}	0.144	0.109 + 0.018*SL	0.112 + 0.017*SL	0.116 + 0.017*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

SCG22D2_LP

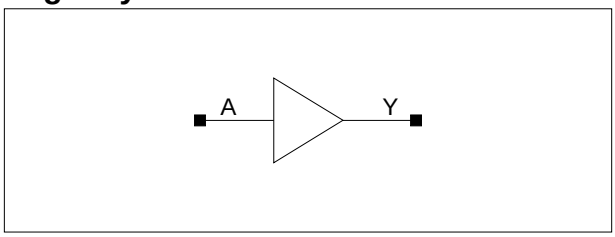
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.175	0.124 + 0.026*SL	0.121 + 0.026*SL	0.116 + 0.027*SL
	t_F	0.105	0.074 + 0.016*SL	0.074 + 0.016*SL	0.068 + 0.016*SL
	t_{PLH}	0.206	0.179 + 0.014*SL	0.181 + 0.013*SL	0.183 + 0.013*SL
	t_{PHL}	0.193	0.175 + 0.009*SL	0.178 + 0.009*SL	0.181 + 0.008*SL
B to Y	t_R	0.176	0.125 + 0.025*SL	0.121 + 0.026*SL	0.116 + 0.027*SL
	t_F	0.107	0.076 + 0.015*SL	0.075 + 0.016*SL	0.069 + 0.016*SL
	t_{PLH}	0.202	0.175 + 0.014*SL	0.176 + 0.013*SL	0.179 + 0.013*SL
	t_{PHL}	0.202	0.183 + 0.009*SL	0.186 + 0.009*SL	0.190 + 0.008*SL
C to Y	t_R	0.176	0.125 + 0.026*SL	0.122 + 0.026*SL	0.116 + 0.027*SL
	t_F	0.138	0.111 + 0.014*SL	0.107 + 0.015*SL	0.092 + 0.016*SL
	t_{PLH}	0.154	0.127 + 0.013*SL	0.129 + 0.013*SL	0.130 + 0.013*SL
	t_{PHL}	0.117	0.099 + 0.009*SL	0.101 + 0.008*SL	0.104 + 0.008*SL
D to Y	t_R	0.118	0.097 + 0.011*SL	0.091 + 0.012*SL	0.075 + 0.013*SL
	t_F	0.130	0.102 + 0.014*SL	0.099 + 0.015*SL	0.090 + 0.016*SL
	t_{PLH}	0.109	0.095 + 0.007*SL	0.099 + 0.006*SL	0.099 + 0.006*SL
	t_{PHL}	0.120	0.102 + 0.009*SL	0.104 + 0.009*SL	0.108 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

DL1D2_LP

1ns Delay Cell with 2X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)	Gate Count
DL1D2_LP	*DL1D2_LP*
A	
0.5	4.00

Switching Characteristics

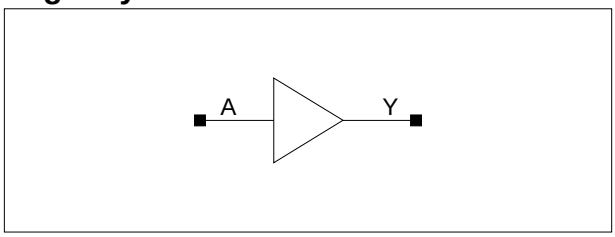
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

DL1D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.042 + 0.012*SL	0.039 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.060	0.038 + 0.011*SL	0.041 + 0.010*SL	0.032 + 0.011*SL
	t_{PLH}	0.907	0.892 + 0.007*SL	0.897 + 0.006*SL	0.900 + 0.006*SL
	t_{PHL}	0.881	0.865 + 0.008*SL	0.872 + 0.006*SL	0.878 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)	Gate Count
DL2D2_LP	*DL2D2_LP*
A	
0.5	4.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

DL2D2_LP

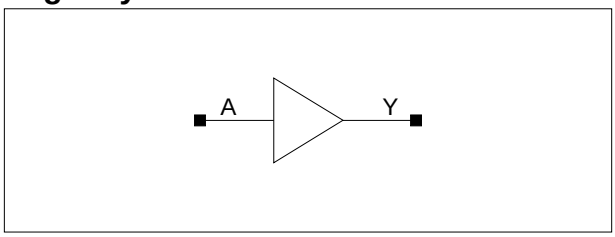
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.043 + 0.012*SL	0.040 + 0.013*SL	0.031 + 0.013*SL
	t_F	0.064	0.043 + 0.011*SL	0.045 + 0.010*SL	0.035 + 0.011*SL
	t_{PLH}	1.889	1.874 + 0.007*SL	1.879 + 0.006*SL	1.882 + 0.006*SL
	t_{PHL}	1.910	1.894 + 0.008*SL	1.901 + 0.006*SL	1.908 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

DL5D2_LP

5ns Delay Cell with 2X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)	Gate Count
DL5D2_LP	*DL5D2_LP*
A	
0.5	6.00

Switching Characteristics

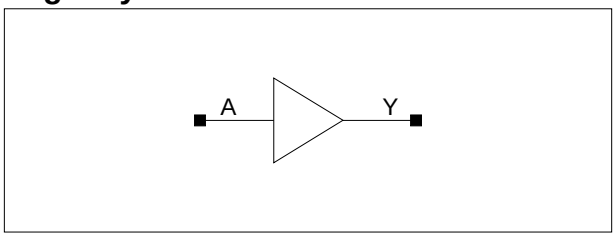
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

DL5D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.068	0.046 + 0.011*SL	0.039 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.066	0.044 + 0.011*SL	0.047 + 0.010*SL	0.034 + 0.011*SL
	t_{PLH}	4.881	4.866 + 0.008*SL	4.871 + 0.006*SL	4.874 + 0.006*SL
	t_{PHL}	4.899	4.882 + 0.009*SL	4.891 + 0.006*SL	4.898 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)	Gate Count
DL10D2_LP	*DL10D2_LP*
A	
0.5	8.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

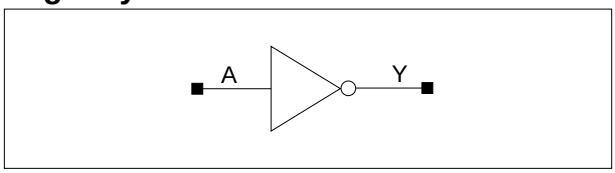
DL10D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.068	0.043 + 0.012*SL	0.042 + 0.012*SL	0.031 + 0.013*SL
	t_F	0.067	0.048 + 0.010*SL	0.048 + 0.010*SL	0.036 + 0.011*SL
	t_{PLH}	9.881	9.866 + 0.008*SL	9.871 + 0.006*SL	9.874 + 0.006*SL
	t_{PHL}	9.771	9.755 + 0.008*SL	9.763 + 0.006*SL	9.771 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

IV_LP/IVD2_LP/IVD3_LP/IVD4_LP/IVD6_LP/IVD8_LP/IVD16_LP/IVD24_LP
Inverter with 1X/2X/3X/4X/6X/8X/16X/24X Drive

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)							
IV_LP	*IVD2_LP*	*IVD3_LP*	*IVD4_LP*	*IVD6_LP*	*IVD8_LP*	*IVD16_LP*	*IVD24_LP*
A	A	A	A	A	A	A	A
1.0	2.0	2.9	3.9	5.9	7.9	16.0	24.4
Gate Count							
IV_LP	*IVD2_LP*	*IVD3_LP*	*IVD4_LP*	*IVD6_LP*	*IVD8_LP*	*IVD16_LP*	*IVD24_LP*
0.67	1.00	1.33	1.67	2.33	3.00	5.67	8.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

IV_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.111	0.069 + 0.021*SL	0.054 + 0.025*SL	0.029 + 0.026*SL
	t_F	0.103	0.062 + 0.021*SL	0.049 + 0.024*SL	0.025 + 0.025*SL
	t_{PLH}	0.094	0.063 + 0.016*SL	0.076 + 0.012*SL	0.076 + 0.012*SL
	t_{PHL}	0.091	0.057 + 0.017*SL	0.069 + 0.014*SL	0.071 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

IVD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.087	0.065 + 0.011*SL	0.062 + 0.012*SL	0.039 + 0.013*SL
	t_F	0.078	0.055 + 0.012*SL	0.058 + 0.011*SL	0.034 + 0.012*SL
	t_{PLH}	0.073	0.052 + 0.010*SL	0.068 + 0.007*SL	0.074 + 0.006*SL
	t_{PHL}	0.068	0.046 + 0.011*SL	0.061 + 0.007*SL	0.067 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

IVD3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.081	0.067 + 0.007*SL	0.065 + 0.008*SL	0.035 + 0.009*SL
	t_F	0.071	0.056 + 0.007*SL	0.056 + 0.008*SL	0.031 + 0.008*SL
	t_{PLH}	0.068	0.052 + 0.008*SL	0.065 + 0.004*SL	0.075 + 0.004*SL
	t_{PHL}	0.063	0.046 + 0.008*SL	0.059 + 0.005*SL	0.069 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

IVD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.074	0.063 + 0.006*SL	0.063 + 0.006*SL	0.040 + 0.006*SL
	t_F	0.066	0.053 + 0.006*SL	0.056 + 0.006*SL	0.036 + 0.006*SL
	t_{PLH}	0.062	0.050 + 0.006*SL	0.061 + 0.004*SL	0.074 + 0.003*SL
	t_{PHL}	0.057	0.044 + 0.007*SL	0.054 + 0.004*SL	0.068 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

IVD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.070	0.062 + 0.004*SL	0.064 + 0.004*SL	0.035 + 0.004*SL
	t_F	0.062	0.052 + 0.005*SL	0.056 + 0.004*SL	0.031 + 0.004*SL
	t_{PLH}	0.058	0.049 + 0.005*SL	0.058 + 0.002*SL	0.074 + 0.002*SL
	t_{PHL}	0.052	0.043 + 0.005*SL	0.051 + 0.003*SL	0.068 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

IVD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.068	0.061 + 0.004*SL	0.065 + 0.003*SL	0.041 + 0.003*SL
	t_F	0.059	0.051 + 0.004*SL	0.056 + 0.003*SL	0.037 + 0.003*SL
	t_{PLH}	0.056	0.049 + 0.004*SL	0.055 + 0.002*SL	0.074 + 0.002*SL
	t_{PHL}	0.050	0.043 + 0.004*SL	0.049 + 0.002*SL	0.067 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

IVD16_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.065	0.060 + 0.002*SL	0.063 + 0.001*SL	0.040 + 0.002*SL
	t_F	0.055	0.051 + 0.002*SL	0.054 + 0.001*SL	0.036 + 0.002*SL
	t_{PLH}	0.052	0.048 + 0.002*SL	0.052 + 0.001*SL	0.074 + 0.001*SL
	t_{PHL}	0.046	0.042 + 0.002*SL	0.046 + 0.001*SL	0.067 + 0.001*SL

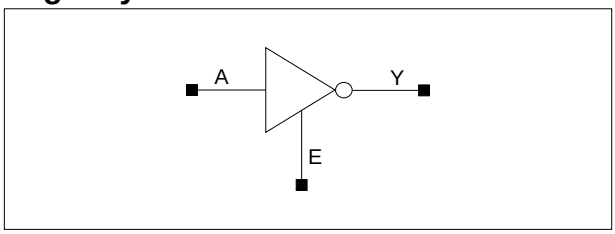
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 117, *Group3 : 117 < SL

IVD24_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.064	0.061 + 0.001*SL	0.063 + 0.001*SL	0.050 + 0.001*SL
	t_F	0.054	0.051 + 0.002*SL	0.054 + 0.001*SL	0.045 + 0.001*SL
	t_{PLH}	0.051	0.048 + 0.001*SL	0.051 + 0.001*SL	0.074 + 0.001*SL
	t_{PHL}	0.045	0.042 + 0.001*SL	0.044 + 0.001*SL	0.067 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 117, *Group3 : 117 < SL

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	1
1	1	0

Cell Data

Input Load (SL)										Output Load (SL)				
IVT_LP		*IVTD2_LP*		*IVTD4_LP*		*IVTD8_LP*		*IVTD16_LP*		*IVT_LP*	*IVTD2_LP*	*IVTD4_LP*	*IVTD8_LP*	*IVTD16_LP*
A	E	A	E	A	E	A	E	A	E	Y	Y	Y	Y	Y
0.8	1.5	0.8	1.6	0.9	1.9	1.1	3.2	1.1	3.2	1.0	1.5	3.0	6.0	11.9

Gate Count				
IVT_LP	*IVTD2_LP*	*IVTD4_LP*	*IVTD8_LP*	*IVTD16_LP*
3.00	3.33	4.00	6.67	9.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

IVT_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.099	0.050 + 0.025*SL	0.045 + 0.026*SL	0.036 + 0.027*SL
	t_F	0.078	0.042 + 0.018*SL	0.046 + 0.017*SL	0.037 + 0.017*SL
	t_{PLH}	0.248	0.220 + 0.014*SL	0.226 + 0.013*SL	0.228 + 0.012*SL
	t_{PHL}	0.252	0.226 + 0.013*SL	0.238 + 0.010*SL	0.248 + 0.010*SL
E to Y	t_R	0.107	0.053 + 0.027*SL	0.050 + 0.028*SL	0.039 + 0.028*SL
	t_F	0.084	0.047 + 0.019*SL	0.052 + 0.017*SL	0.040 + 0.018*SL
	t_{PLH}	0.165	0.137 + 0.014*SL	0.142 + 0.013*SL	0.143 + 0.013*SL
	t_{PHL}	0.200	0.174 + 0.013*SL	0.186 + 0.010*SL	0.196 + 0.010*SL
	t_{PLZ}	0.147	0.147 + 0.000*SL	0.147 + 0.000*SL	0.146 + 0.000*SL
	t_{PHZ}	0.159	0.159 + 0.000*SL	0.159 + 0.000*SL	0.159 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

IVTD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.073	0.048 + 0.013*SL	0.048 + 0.013*SL	0.039 + 0.013*SL
	t_F	0.057	0.038 + 0.010*SL	0.042 + 0.009*SL	0.042 + 0.009*SL
	t_{PLH}	0.250	0.232 + 0.009*SL	0.241 + 0.007*SL	0.248 + 0.006*SL
	t_{PHL}	0.243	0.227 + 0.008*SL	0.236 + 0.006*SL	0.252 + 0.005*SL
E to Y	t_R	0.075	0.048 + 0.013*SL	0.050 + 0.013*SL	0.041 + 0.014*SL
	t_F	0.062	0.042 + 0.010*SL	0.049 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.159	0.142 + 0.009*SL	0.150 + 0.007*SL	0.157 + 0.006*SL
	t_{PHL}	0.190	0.174 + 0.008*SL	0.183 + 0.006*SL	0.198 + 0.005*SL
	t_{PLZ}	0.155	0.155 + 0.000*SL	0.155 + 0.000*SL	0.155 + 0.000*SL
	t_{PHZ}	0.177	0.177 + 0.000*SL	0.177 + 0.000*SL	0.178 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

IVTD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.072	0.058 + 0.007*SL	0.060 + 0.006*SL	0.053 + 0.006*SL
	t_F	0.053	0.041 + 0.006*SL	0.049 + 0.004*SL	0.050 + 0.004*SL
	t_{PLH}	0.268	0.257 + 0.006*SL	0.265 + 0.004*SL	0.283 + 0.003*SL
	t_{PHL}	0.241	0.231 + 0.005*SL	0.238 + 0.003*SL	0.260 + 0.003*SL
E to Y	t_R	0.073	0.060 + 0.007*SL	0.061 + 0.006*SL	0.055 + 0.007*SL
	t_F	0.057	0.044 + 0.006*SL	0.052 + 0.004*SL	0.054 + 0.004*SL
	t_{PLH}	0.175	0.163 + 0.006*SL	0.171 + 0.004*SL	0.188 + 0.003*SL
	t_{PHL}	0.186	0.176 + 0.005*SL	0.184 + 0.003*SL	0.205 + 0.003*SL
	t_{PLZ}	0.166	0.166 + 0.000*SL	0.166 + 0.000*SL	0.166 + 0.000*SL
	t_{PHZ}	0.216	0.215 + 0.000*SL	0.216 + 0.000*SL	0.217 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

IVTD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.063	0.054 + 0.004*SL	0.058 + 0.003*SL	0.051 + 0.003*SL
	t_F	0.047	0.041 + 0.003*SL	0.044 + 0.002*SL	0.048 + 0.002*SL
	t_{PLH}	0.287	0.281 + 0.003*SL	0.286 + 0.002*SL	0.306 + 0.002*SL
	t_{PHL}	0.257	0.251 + 0.003*SL	0.255 + 0.002*SL	0.279 + 0.001*SL
E to Y	t_R	0.064	0.056 + 0.004*SL	0.058 + 0.003*SL	0.052 + 0.003*SL
	t_F	0.049	0.043 + 0.003*SL	0.046 + 0.002*SL	0.051 + 0.002*SL
	t_{PLH}	0.161	0.155 + 0.003*SL	0.160 + 0.002*SL	0.178 + 0.002*SL
	t_{PHL}	0.189	0.183 + 0.003*SL	0.188 + 0.002*SL	0.210 + 0.001*SL
	t_{PLZ}	0.179	0.179 + 0.000*SL	0.179 + 0.000*SL	0.179 + 0.000*SL
	t_{PHZ}	0.203	0.202 + 0.000*SL	0.203 + 0.000*SL	0.204 + 0.000*SL

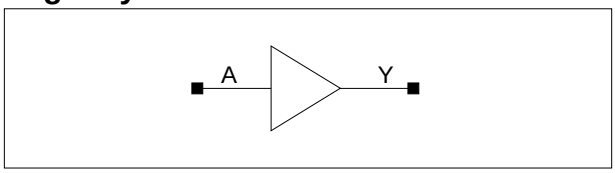
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

IVTD16_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.081	0.078 + 0.002*SL	0.078 + 0.002*SL	0.081 + 0.002*SL
	t_F	0.060	0.057 + 0.001*SL	0.058 + 0.001*SL	0.068 + 0.001*SL
	t_{PLH}	0.336	0.331 + 0.002*SL	0.336 + 0.001*SL	0.378 + 0.001*SL
	t_{PHL}	0.293	0.290 + 0.001*SL	0.292 + 0.001*SL	0.322 + 0.001*SL
E to Y	t_R	0.080	0.076 + 0.002*SL	0.077 + 0.002*SL	0.082 + 0.002*SL
	t_F	0.057	0.054 + 0.002*SL	0.056 + 0.001*SL	0.069 + 0.001*SL
	t_{PLH}	0.210	0.205 + 0.002*SL	0.210 + 0.001*SL	0.250 + 0.001*SL
	t_{PHL}	0.217	0.214 + 0.002*SL	0.217 + 0.001*SL	0.254 + 0.001*SL
	t_{PLZ}	0.203	0.203 + 0.000*SL	0.203 + 0.000*SL	0.203 + 0.000*SL
	t_{PHZ}	0.296	0.295 + 0.000*SL	0.296 + 0.000*SL	0.299 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 117, *Group3 : 117 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)							
NID_LP	*NID2_LP*	*NID3_LP*	*NID4_LP*	*NID6_LP*	*NID8_LP*	*NID16_LP*	*NID24_LP*
A	A	A	A	A	A	A	A
0.8	1.0	1.0	1.0	2.0	2.0	3.9	5.8
Gate Count							
NID_LP	*NID2_LP*	*NID3_LP*	*NID4_LP*	*NID6_LP*	*NID8_LP*	*NID16_LP*	*NID24_LP*
1.00	1.33	1.67	2.00	3.00	3.67	7.00	10.00

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NID_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.091	0.042 + 0.025*SL	0.035 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.075	0.037 + 0.019*SL	0.033 + 0.020*SL	0.025 + 0.020*SL
	t_{PLH}	0.145	0.118 + 0.013*SL	0.121 + 0.012*SL	0.122 + 0.012*SL
	t_{PHL}	0.152	0.127 + 0.012*SL	0.132 + 0.011*SL	0.135 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NID2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.066	0.042 + 0.012*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.055	0.034 + 0.010*SL	0.037 + 0.010*SL	0.028 + 0.010*SL
	t_{PLH}	0.144	0.129 + 0.008*SL	0.134 + 0.006*SL	0.137 + 0.006*SL
	t_{PHL}	0.151	0.136 + 0.007*SL	0.142 + 0.006*SL	0.148 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NID3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.068	0.052 + 0.008*SL	0.050 + 0.008*SL	0.035 + 0.009*SL
	t_F	0.055	0.039 + 0.008*SL	0.045 + 0.006*SL	0.034 + 0.007*SL
	t_{PLH}	0.157	0.145 + 0.006*SL	0.151 + 0.004*SL	0.157 + 0.004*SL
	t_{PHL}	0.164	0.153 + 0.006*SL	0.159 + 0.004*SL	0.169 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

NID4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.067	0.056 + 0.006*SL	0.054 + 0.006*SL	0.043 + 0.007*SL
	t_F	0.056	0.046 + 0.005*SL	0.047 + 0.005*SL	0.043 + 0.005*SL
	t_{PLH}	0.171	0.161 + 0.005*SL	0.168 + 0.003*SL	0.179 + 0.003*SL
	t_{PHL}	0.177	0.167 + 0.005*SL	0.174 + 0.003*SL	0.188 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NID6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.058	0.052 + 0.003*SL	0.047 + 0.004*SL	0.033 + 0.004*SL
	t_F	0.044	0.036 + 0.004*SL	0.039 + 0.003*SL	0.032 + 0.003*SL
	t_{PLH}	0.145	0.138 + 0.003*SL	0.143 + 0.002*SL	0.152 + 0.002*SL
	t_{PHL}	0.152	0.146 + 0.003*SL	0.150 + 0.002*SL	0.163 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

NID8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.061	0.055 + 0.003*SL	0.056 + 0.003*SL	0.042 + 0.003*SL
	t_F	0.051	0.046 + 0.002*SL	0.046 + 0.002*SL	0.042 + 0.002*SL
	t_{PLH}	0.162	0.156 + 0.003*SL	0.160 + 0.002*SL	0.173 + 0.002*SL
	t_{PHL}	0.168	0.163 + 0.003*SL	0.167 + 0.002*SL	0.183 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

NID16_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.058	0.054 + 0.002*SL	0.055 + 0.002*SL	0.041 + 0.002*SL
	t_F	0.049	0.046 + 0.001*SL	0.046 + 0.001*SL	0.041 + 0.001*SL
	t_{PLH}	0.159	0.156 + 0.002*SL	0.158 + 0.001*SL	0.173 + 0.001*SL
	t_{PHL}	0.165	0.163 + 0.001*SL	0.165 + 0.001*SL	0.183 + 0.001*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 117, *Group3 : 117 < SL

NID24_LP

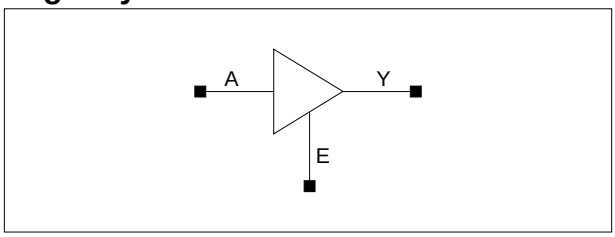
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.057	0.054 + 0.001*SL	0.055 + 0.001*SL	0.046 + 0.001*SL
	t_F	0.048	0.046 + 0.001*SL	0.046 + 0.001*SL	0.045 + 0.001*SL
	t_{PLH}	0.159	0.157 + 0.001*SL	0.158 + 0.001*SL	0.173 + 0.001*SL
	t_{PHL}	0.165	0.163 + 0.001*SL	0.165 + 0.001*SL	0.181 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 117, *Group3 : 117 < SL

NIT_LP/NITD2_LP/NITD4_LP/NITD8_LP/NITD16_LP

Non-Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X/16X Drive

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	0
1	1	1

Cell Data

Input Load (SL)										Output Load (SL)				
NIT_LP		*NITD2_LP*		*NITD4_LP*		*NITD8_LP*		*NITD16_LP*		*NIT_LP*	*NITD2_LP*	*NITD4_LP*	*NITD8_LP*	*NITD16_LP*
A	E	A	E	A	E	A	E	A	E	Y	Y	Y	Y	Y
1.4	1.4	1.7	1.6	2.0	1.8	4.2	3.2	4.2	3.2	1.0	1.5	2.9	6.0	11.8

Gate Count				
NIT_LP	*NITD2_LP*	*NITD4_LP*	*NITD8_LP*	*NITD16_LP*
2.67	3.00	3.67	6.00	8.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NIT_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.098	0.050 + 0.024*SL	0.042 + 0.026*SL	0.034 + 0.026*SL
	t_F	0.077	0.043 + 0.017*SL	0.044 + 0.017*SL	0.035 + 0.017*SL
	t_{PLH}	0.156	0.128 + 0.014*SL	0.134 + 0.012*SL	0.136 + 0.012*SL
	t_{PHL}	0.192	0.166 + 0.013*SL	0.178 + 0.010*SL	0.188 + 0.010*SL
E to Y	t_R	0.105	0.053 + 0.026*SL	0.045 + 0.028*SL	0.036 + 0.028*SL
	t_F	0.084	0.049 + 0.017*SL	0.049 + 0.017*SL	0.038 + 0.018*SL
	t_{PLH}	0.159	0.131 + 0.014*SL	0.136 + 0.013*SL	0.137 + 0.013*SL
	t_{PHL}	0.196	0.169 + 0.013*SL	0.181 + 0.010*SL	0.190 + 0.010*SL
	t_{PLZ}	0.144	0.144 + 0.000*SL	0.144 + 0.000*SL	0.144 + 0.000*SL
	t_{PHZ}	0.151	0.151 + 0.000*SL	0.151 + 0.000*SL	0.152 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NITD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.072	0.047 + 0.013*SL	0.047 + 0.013*SL	0.038 + 0.013*SL
	t_F	0.058	0.037 + 0.010*SL	0.045 + 0.008*SL	0.043 + 0.009*SL
	t_{PLH}	0.153	0.136 + 0.009*SL	0.144 + 0.007*SL	0.151 + 0.006*SL
	t_{PHL}	0.180	0.164 + 0.008*SL	0.173 + 0.006*SL	0.189 + 0.005*SL
E to Y	t_R	0.076	0.050 + 0.013*SL	0.049 + 0.013*SL	0.040 + 0.014*SL
	t_F	0.062	0.041 + 0.010*SL	0.049 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.155	0.138 + 0.008*SL	0.146 + 0.007*SL	0.152 + 0.006*SL
	t_{PHL}	0.189	0.172 + 0.008*SL	0.182 + 0.006*SL	0.196 + 0.005*SL
	t_{PLZ}	0.154	0.153 + 0.000*SL	0.154 + 0.000*SL	0.154 + 0.000*SL
	t_{PHZ}	0.171	0.171 + 0.000*SL	0.171 + 0.000*SL	0.172 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

NITD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.071	0.057 + 0.007*SL	0.060 + 0.006*SL	0.051 + 0.006*SL
	t_F	0.054	0.044 + 0.005*SL	0.047 + 0.004*SL	0.052 + 0.004*SL
	t_{PLH}	0.170	0.158 + 0.006*SL	0.167 + 0.004*SL	0.184 + 0.003*SL
	t_{PHL}	0.187	0.177 + 0.005*SL	0.184 + 0.003*SL	0.206 + 0.003*SL
E to Y	t_R	0.072	0.059 + 0.006*SL	0.060 + 0.006*SL	0.053 + 0.007*SL
	t_F	0.057	0.047 + 0.005*SL	0.050 + 0.004*SL	0.055 + 0.004*SL
	t_{PLH}	0.171	0.160 + 0.006*SL	0.168 + 0.004*SL	0.184 + 0.003*SL
	t_{PHL}	0.188	0.178 + 0.005*SL	0.185 + 0.003*SL	0.207 + 0.003*SL
	t_{PLZ}	0.167	0.167 + 0.000*SL	0.167 + 0.000*SL	0.167 + 0.000*SL
	t_{PHZ}	0.211	0.210 + 0.000*SL	0.211 + 0.000*SL	0.212 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 31, *Group3 : 31 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

NITD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.063	0.056 + 0.003*SL	0.057 + 0.003*SL	0.050 + 0.003*SL
	t_F	0.046	0.039 + 0.003*SL	0.044 + 0.002*SL	0.048 + 0.002*SL
	t_{PLH}	0.157	0.150 + 0.003*SL	0.156 + 0.002*SL	0.175 + 0.002*SL
	t_{PHL}	0.175	0.170 + 0.003*SL	0.174 + 0.002*SL	0.196 + 0.001*SL
E to Y	t_R	0.062	0.055 + 0.003*SL	0.056 + 0.003*SL	0.050 + 0.003*SL
	t_F	0.049	0.044 + 0.003*SL	0.047 + 0.002*SL	0.050 + 0.002*SL
	t_{PLH}	0.161	0.155 + 0.003*SL	0.160 + 0.002*SL	0.178 + 0.002*SL
	t_{PHL}	0.190	0.185 + 0.003*SL	0.189 + 0.002*SL	0.212 + 0.001*SL
	t_{PLZ}	0.181	0.181 + 0.000*SL	0.181 + 0.000*SL	0.181 + 0.000*SL
	t_{PHZ}	0.203	0.203 + 0.000*SL	0.204 + 0.000*SL	0.205 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 58, *Group3 : 58 < SL

NITD16_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.083	0.079 + 0.002*SL	0.081 + 0.002*SL	0.094 + 0.002*SL
	t_F	0.063	0.061 + 0.001*SL	0.061 + 0.001*SL	0.067 + 0.001*SL
	t_{PLH}	0.211	0.207 + 0.002*SL	0.211 + 0.001*SL	0.258 + 0.001*SL
	t_{PHL}	0.212	0.209 + 0.001*SL	0.211 + 0.001*SL	0.239 + 0.001*SL
E to Y	t_R	0.085	0.080 + 0.002*SL	0.083 + 0.002*SL	0.095 + 0.002*SL
	t_F	0.058	0.054 + 0.002*SL	0.058 + 0.001*SL	0.070 + 0.001*SL
	t_{PLH}	0.215	0.211 + 0.002*SL	0.215 + 0.001*SL	0.261 + 0.001*SL
	t_{PHL}	0.217	0.214 + 0.002*SL	0.217 + 0.001*SL	0.254 + 0.001*SL
	t_{PLZ}	0.207	0.207 + 0.000*SL	0.207 + 0.000*SL	0.207 + 0.000*SL
	t_{PHZ}	0.319	0.319 + 0.000*SL	0.320 + 0.000*SL	0.323 + 0.000*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 117, *Group3 : 117 < SL

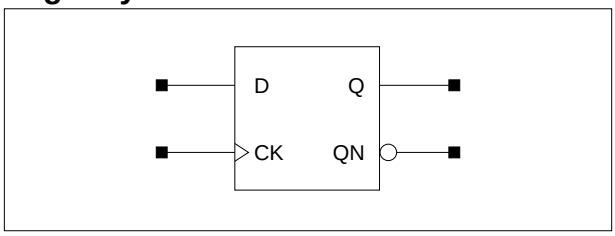
Cell List

Cell Name	Function Description
FD1_LP	D Flip-Flop with 1X Drive
FD1D2_LP	D Flip-Flop with 2X Drive
FD1S_LP	D Flip-Flop with Scan, 1X Drive
FD1SD2_LP	D Flip-Flop with Scan, 2X Drive
FD1SQ_LP	D Flip-Flop with Scan, Q Output Only, 1X Drive
FD1SQD2_LP	D Flip-Flop with Scan, Q Output Only, 2X Drive
FD1Q_LP	D Flip-Flop with Q Output Only, 1X Drive
FD1QD2_LP	D Flip-Flop with Q Output Only, 2X Drive
FD2_LP	D Flip-Flop with Reset, 1X Drive
FD2D2_LP	D Flip-Flop with Reset, 2X Drive
FD2S_LP	D Flip-Flop with Reset, Scan, 1X Drive
FD2SD2_LP	D Flip-Flop with Reset, Scan, 2X Drive
FD2SQ_LP	D Flip-Flop with Reset, Scan, Q Output Only, 1X Drive
FD2SQD2_LP	D Flip-Flop with Reset, Scan, Q Output Only, 2X Drive
FD2Q_LP	D Flip-Flop with Reset, Q Output Only, 1X Drive
FD2QD2_LP	D Flip-Flop with Reset, Q Output Only, 2X Drive
FD3_LP	D Flip-Flop with Set, 1X Drive
FD3D2_LP	D Flip-Flop with Set, 2X Drive
FD3S_LP	D Flip-Flop with Set, Scan, 1X Drive
FD3SD2_LP	D Flip-Flop with Set, Scan, 2X Drive
FD3SQ_LP	D Flip-Flop with Set, Scan, Q Output Only, 1X Drive
FD3SQD2_LP	D Flip-Flop with Set, Scan, Q Output Only, 2X Drive
FD3Q_LP	D Flip-Flop with Set, Q Output Only, 1X Drive
FD3QD2_LP	D Flip-Flop with Set, Q Output Only, 2X Drive
FD4_LP	D Flip-Flop with Reset, Se, 1X Drive
FD4D2_LP	D Flip-Flop with Reset, Set, 2X Drive
FD4S_LP	D Flip-Flop with Reset, Set, Scan, 1X Drive
FD4SD2_LP	D Flip-Flop with Reset, Set, Scan, 2X Drive
FD4SQ_LP	D Flip-Flop with Reset, Set, Scan, Q Output Only, 1X Drive
FD4SQD2_LP	D Flip-Flop with Reset, Set, Scan, Q Output Only, 2X Drive
FD4Q_LP	D Flip-Flop with Reset, Set, Q Output Only, 1X Drive
FD4QD2_LP	D Flip-Flop with Reset, Set, Q Output Only, 2X Drive
FD5_LP	D Flip-Flop with Negative Edge Trigger, 1X Drive
FD5D2_LP	D Flip-Flop with Negative Edge Trigger, 2X Drive
FD5S_LP	D Flip-Flop with Negative Edge Trigger, Scan, 1X Drive
FD5SD2_LP	D Flip-Flop with Negative Edge Trigger, Scan, 2X Drive
FD6_LP	D Flip-Flop with Negative Edge Trigger, Reset, 1X Drive
FD6D2_LP	D Flip-Flop with Negative Edge Trigger, Reset, 2X Drive

Cell List (Continued)

Cell Name	Function Description
FD6S_LP	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 1X Drive
FD6SD2_LP	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 2X Drive
FD7_LP	D Flip-Flop with Negative Edge Trigger, Set, 1X Drive
FD7D2_LP	D Flip-Flop with Negative Edge Trigger, Set, 2X Drive
FD7S_LP	D Flip-Flop with Negative Edge Trigger, Set, Scan, 1X Drive
FD7SD2_LP	D Flip-Flop with Negative Edge Trigger, Set, Scan, 2X Drive
FD8_LP	D Flip-Flop with Negative Edge Trigger, Reset, Set, 1X Drive
FD8D2_LP	D Flip-Flop with Negative Edge Trigger, Reset, Set, 2X Drive
FD8S_LP	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X Drive
FD8SD2_LP	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 2X Drive
FDS2_LP	D Flip-Flop with Synchronous Clear, 1X Drive
FDS2D2_LP	D Flip-Flop with Synchronous Clear, 2X Drive
FDS2S_LP	D Flip-Flop with Synchronous Clear, Scan, 1X Drive
FDS2SD2_LP	D Flip-Flop with Synchronous Clear, Scan, 2X Drive
FDS3_LP	D Flip-Flop with Synchronous Set, 1X Drive
FDS3D2_LP	D Flip-Flop with Synchronous Set, 2X Drive
FDS3S_LP	Flip-Flop with Synchronous Set, Scan, 1X Drive
FDS3SD2_LP	Flip-Flop with Synchronous Set, Scan, 2x Drive
FJ2_LP	JK Flip-Flop with Reset, 1X Drive
FJ2D2_LP	JK Flip-Flop with Reset, 2X Drive
FJ2S_LP	JK Flip-Flop with Reset, Scan, 1X Drive
FJ2SD2_LP	JK Flip-Flop with Reset, Scan, 2X Drive
FJ4_LP	JK Flip-Flop with Reset, Set, 1X Drive
FJ4D2_LP	JK Flip-Flop with Reset, Set, 2X Drive
FJ4S_LP	JK Flip-Flop with Reset, Set, Scan, 1X Drive
FJ4SD2_LP	JK Flip-Flop with Reset, Set, Scan, 2X Drive
FT2_LP	Toggle Flip-Flop with Reset, 1X Drive
FT2D2_LP	Toggle Flip-Flop with Reset, 2X Drive

Logic Symbol



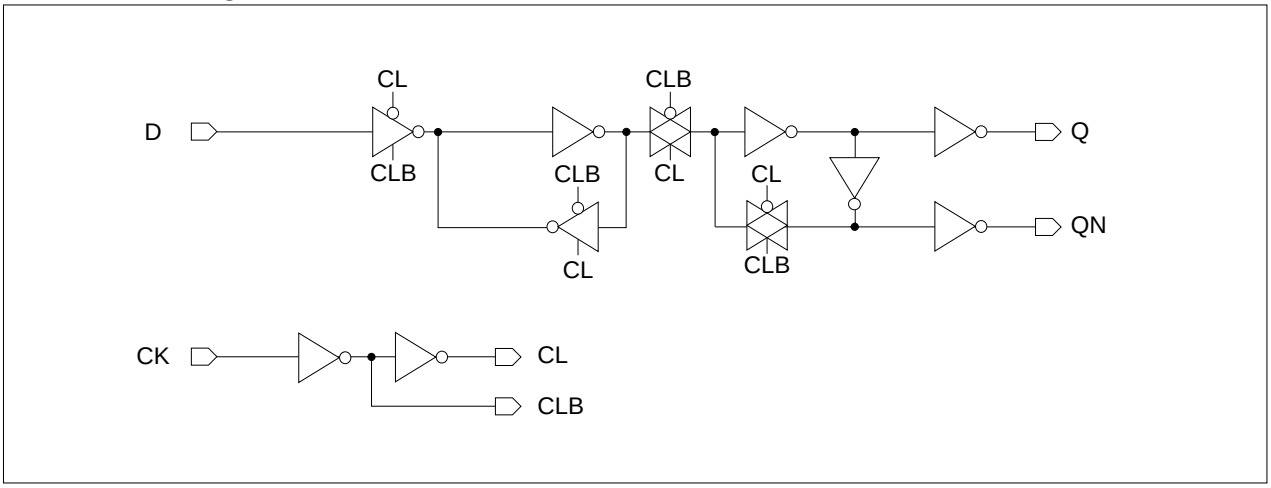
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
FD1_LP		*FD1D2_LP*		*FD1_LP*	*FD1D2_LP*
D	CK	D	CK		
0.7	1.1	0.7	1.1	5.33	5.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1_LP	FD1D2_LP
Input Setup Time (D to CK)	t_{SU}	0.246	0.243
Input Hold Time (D to CK)	t_{HD}	0.089	0.092
Pulse Width Low (CK)	t_{PWL}	0.300	0.301
Pulse Width High (CK)	t_{PWH}	0.254	0.265

FD1_LP/FD1D2_LP

D Flip-Flop with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD1_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.093	0.043 + 0.025*SL	0.039 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.070	0.037 + 0.017*SL	0.035 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.296	0.269 + 0.013*SL	0.272 + 0.013*SL	0.275 + 0.012*SL
	t_{PHL}	0.291	0.268 + 0.012*SL	0.275 + 0.010*SL	0.280 + 0.010*SL
CK to QN	t_R	0.092	0.043 + 0.025*SL	0.037 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.070	0.037 + 0.017*SL	0.035 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.350	0.324 + 0.013*SL	0.326 + 0.012*SL	0.327 + 0.012*SL
	t_{PHL}	0.351	0.329 + 0.011*SL	0.334 + 0.010*SL	0.337 + 0.010*SL

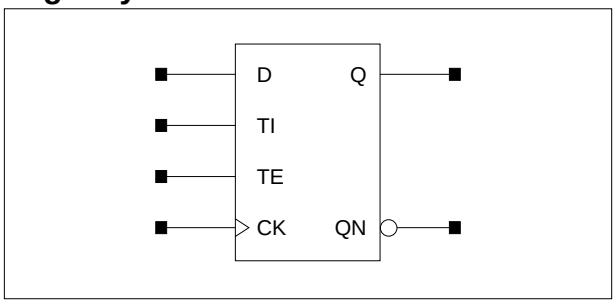
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD1D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.069	0.045 + 0.012*SL	0.042 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.057	0.040 + 0.009*SL	0.041 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.303	0.287 + 0.008*SL	0.293 + 0.007*SL	0.298 + 0.006*SL
	t_{PHL}	0.301	0.286 + 0.008*SL	0.294 + 0.006*SL	0.306 + 0.005*SL
CK to QN	t_R	0.063	0.039 + 0.012*SL	0.036 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.051	0.034 + 0.009*SL	0.035 + 0.008*SL	0.030 + 0.009*SL
	t_{PLH}	0.378	0.363 + 0.007*SL	0.367 + 0.006*SL	0.370 + 0.006*SL
	t_{PHL}	0.377	0.363 + 0.007*SL	0.370 + 0.005*SL	0.378 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



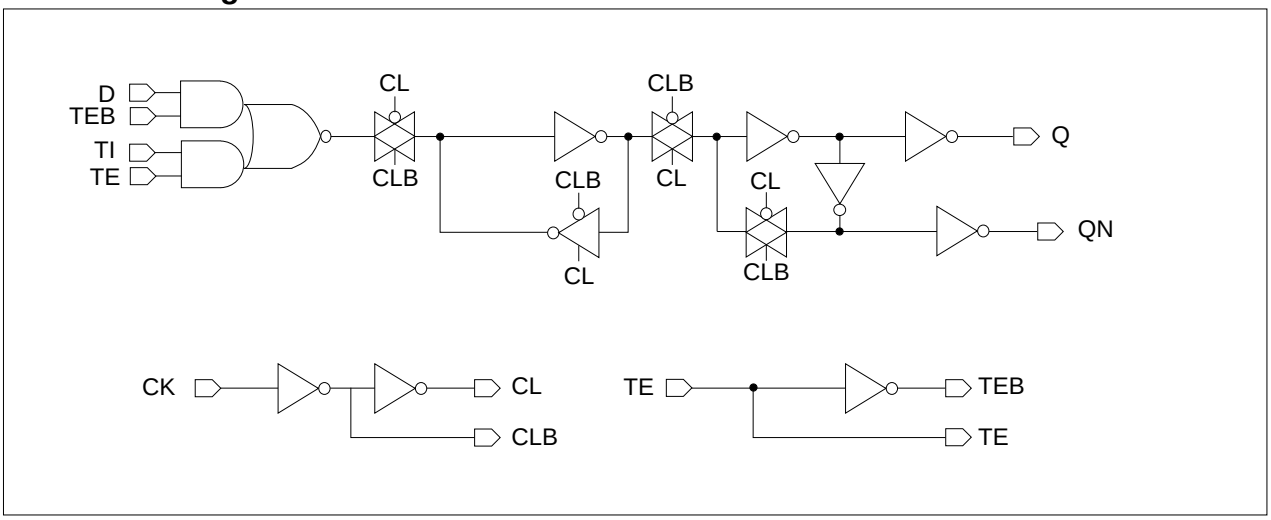
Truth Table

D	TI	TE	CK	Q (n+1)	QN (n+1)
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0
x	x	x	↓	Q(n)	QN(n)

Cell Data

Input Load (SL)								Gate Count	
FD1S_LP				*FD1SD2_LP*				*FD1S_LP*	*FD1SD2_LP*
D	CK	TI	TE	D	CK	TI	TE		
0.6	1.1	0.7	1.6	0.6	1.2	0.7	1.6	7.33	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1S_LP	FD1SD2_LP
Input Setup Time (D to CK)	t_{SU}	0.348	0.348
Input Hold Time (D to CK)	t_{HD}	0.037	0.037
Input Setup Time (TI to CK)	t_{SU}	0.397	0.396
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.382	0.381
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.369	0.369
Pulse Width High (CK)	t_{PWH}	0.257	0.265

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD1S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.094	0.044 + 0.025*SL	0.040 + 0.026*SL	0.034 + 0.027*SL
	t_F	0.072	0.038 + 0.017*SL	0.037 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.301	0.274 + 0.013*SL	0.277 + 0.013*SL	0.280 + 0.012*SL
	t_{PHL}	0.298	0.274 + 0.012*SL	0.282 + 0.010*SL	0.287 + 0.010*SL
CK to QN	t_R	0.089	0.038 + 0.026*SL	0.034 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.069	0.035 + 0.017*SL	0.033 + 0.017*SL	0.025 + 0.018*SL
	t_{PLH}	0.357	0.331 + 0.013*SL	0.333 + 0.012*SL	0.334 + 0.012*SL
	t_{PHL}	0.357	0.334 + 0.011*SL	0.340 + 0.010*SL	0.343 + 0.010*SL

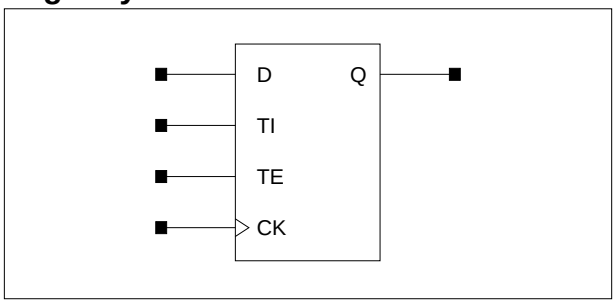
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD1SD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.069	0.046 + 0.012*SL	0.042 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.057	0.039 + 0.009*SL	0.041 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.302	0.286 + 0.008*SL	0.292 + 0.007*SL	0.296 + 0.006*SL
	t_{PHL}	0.302	0.287 + 0.008*SL	0.295 + 0.006*SL	0.307 + 0.005*SL
CK to QN	t_R	0.064	0.040 + 0.012*SL	0.036 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.052	0.034 + 0.009*SL	0.038 + 0.008*SL	0.031 + 0.009*SL
	t_{PLH}	0.379	0.364 + 0.007*SL	0.368 + 0.006*SL	0.370 + 0.006*SL
	t_{PHL}	0.376	0.362 + 0.007*SL	0.369 + 0.005*SL	0.376 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



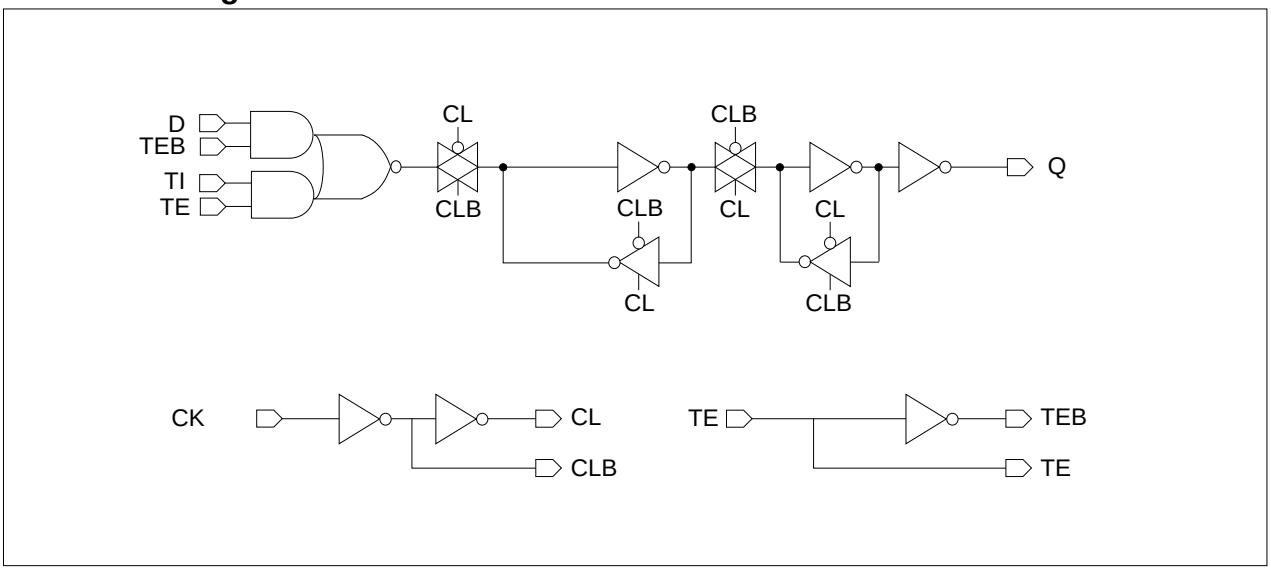
Truth Table

D	TI	TE	CK	Q (n+1)
0	x	0	↑	0
1	x	0	↑	1
x	0	1	↑	0
x	1	1	↑	1
x	x	x	↓	Q(n)

Cell Data

Input Load (SL)								Gate Count	
FD1SQ_LP				*FD1SQD2_LP*				*FD1SQ_LP*	*FD1SQD2_LP*
D	CK	TI	TE	D	CK	TI	TE		
0.6	1.2	0.7	1.6	0.6	1.1	0.7	1.6	6.33	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1SQ_LP	FD1SQD2_LP
Input Setup Time (D to CK)	t_{SU}	0.347	0.348
Input Hold Time (D to CK)	t_{HD}	0.037	0.037
Input Setup Time (TI to CK)	t_{SU}	0.394	0.395
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.380	0.380
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.368	0.369
Pulse Width High (CK)	t_{PWH}	0.242	0.248

FD1SQ_LP/FD1SQD2_LP

D Flip-Flop with Scan, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD1SQ_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.090	0.041 + 0.025*SL	0.034 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.067	0.033 + 0.017*SL	0.032 + 0.017*SL	0.024 + 0.018*SL
	t_{PLH}	0.286	0.260 + 0.013*SL	0.262 + 0.012*SL	0.264 + 0.012*SL
	t_{PHL}	0.282	0.260 + 0.011*SL	0.266 + 0.010*SL	0.268 + 0.010*SL

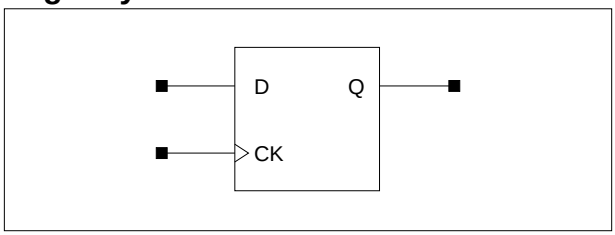
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD1SQD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.066	0.043 + 0.012*SL	0.039 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.052	0.034 + 0.009*SL	0.037 + 0.008*SL	0.030 + 0.009*SL
	t_{PLH}	0.290	0.275 + 0.008*SL	0.280 + 0.006*SL	0.282 + 0.006*SL
	t_{PHL}	0.289	0.275 + 0.007*SL	0.281 + 0.005*SL	0.289 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



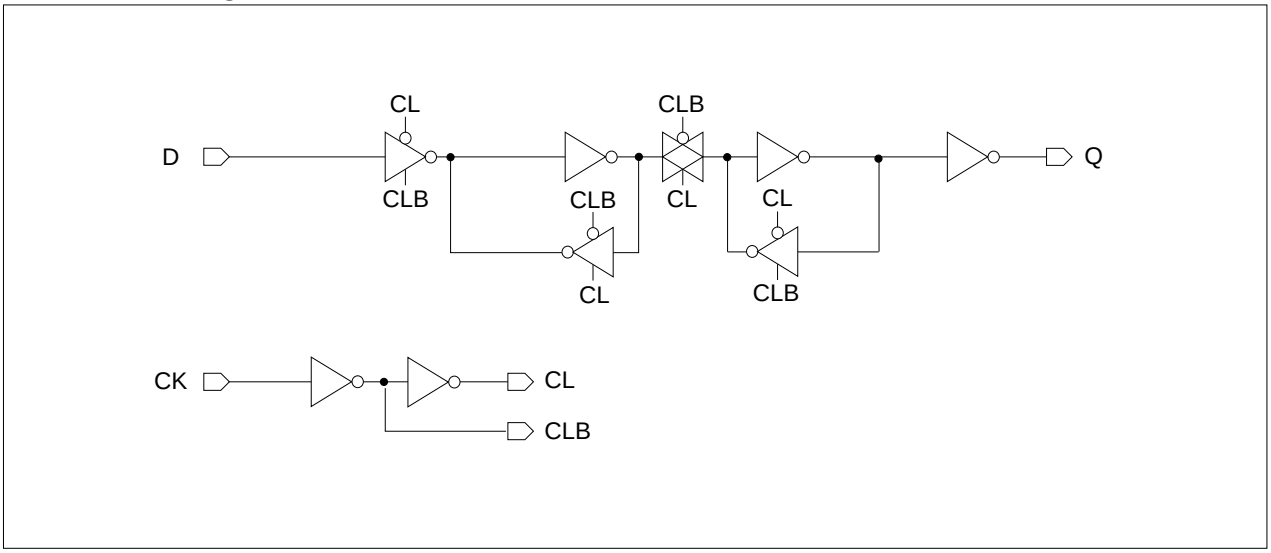
Truth Table

D	CK	Q (n+1)
0	↑	0
1	↑	1
x	↓	Q (n)

Cell Data

Input Load (SL)				Gate Count	
FD1Q_LP		*FD1QD2_LP*		*FD1Q_LP*	*FD1QD2_LP*
D	CK	D	CK		
0.7	1.1	0.7	1.1	4.67	5.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD1Q_LP	FD1QD2_LP
Input Setup Time (D to CK)	t_{SU}	0.243	0.244
Input Hold Time (D to CK)	t_{HD}	0.092	0.090
Pulse Width Low (CK)	t_{PWL}	0.301	0.300
Pulse Width High (CK)	t_{PWH}	0.242	0.247

FD1Q_LP/FD1QD2_LP

D Flip-Flop with Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD1Q_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.092	0.042 + 0.025*SL	0.036 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.066	0.031 + 0.017*SL	0.031 + 0.017*SL	0.024 + 0.018*SL
	t_{PLH}	0.286	0.260 + 0.013*SL	0.262 + 0.012*SL	0.264 + 0.012*SL
	t_{PHL}	0.279	0.257 + 0.011*SL	0.262 + 0.010*SL	0.265 + 0.010*SL

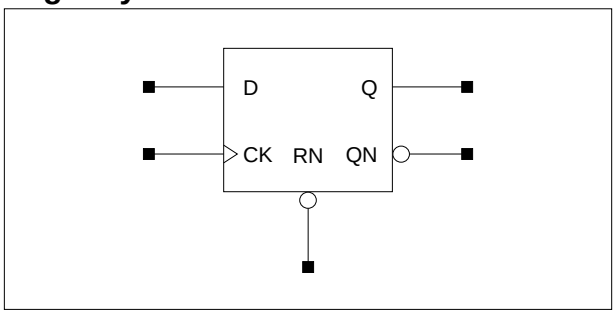
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD1QD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.066	0.043 + 0.012*SL	0.039 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.052	0.033 + 0.009*SL	0.037 + 0.008*SL	0.031 + 0.009*SL
	t_{PLH}	0.289	0.273 + 0.008*SL	0.278 + 0.006*SL	0.281 + 0.006*SL
	t_{PHL}	0.284	0.270 + 0.007*SL	0.277 + 0.005*SL	0.285 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



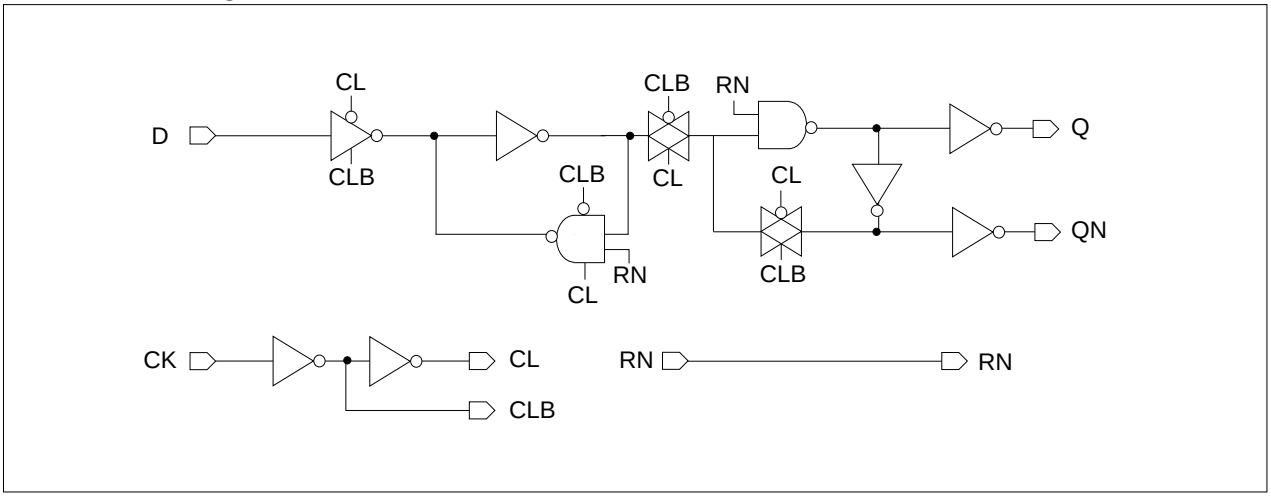
Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD2_LP			*FD2D2_LP*			*FD2_LP*	*FD2D2_LP*
D	CK	RN	D	CK	RN		
0.7	1.2	1.5	0.7	1.2	1.4	5.67	6.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2_LP	FD2D2_LP
Input Setup Time (D to CK)	t_{SU}	0.247	0.244
Input Hold Time (D to CK)	t_{HD}	0.095	0.098
Pulse Width Low (CK)	t_{PWL}	0.299	0.300
Pulse Width High (CK)	t_{PWH}	0.261	0.280
Pulse Width Low (RN)	t_{PWL}	0.279	0.315
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.773	0.778

FD2_LP/FD2D2_LP

D Flip-Flop with Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.104	0.054 + 0.025*SL	0.050 + 0.026*SL	0.040 + 0.026*SL
	t_F	0.075	0.041 + 0.017*SL	0.041 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.326	0.297 + 0.015*SL	0.305 + 0.013*SL	0.310 + 0.012*SL
	t_{PHL}	0.305	0.281 + 0.012*SL	0.290 + 0.010*SL	0.297 + 0.010*SL
RN to Q	t_F	0.077	0.044 + 0.017*SL	0.042 + 0.017*SL	0.035 + 0.017*SL
	t_{PHL}	0.182	0.158 + 0.012*SL	0.167 + 0.010*SL	0.176 + 0.010*SL
CK to QN	t_R	0.090	0.041 + 0.025*SL	0.034 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.070	0.037 + 0.016*SL	0.035 + 0.017*SL	0.025 + 0.018*SL
	t_{PLH}	0.364	0.338 + 0.013*SL	0.341 + 0.012*SL	0.342 + 0.012*SL
	t_{PHL}	0.383	0.360 + 0.011*SL	0.367 + 0.010*SL	0.370 + 0.010*SL
RN to QN	t_R	0.101	0.046 + 0.028*SL	0.051 + 0.026*SL	0.052 + 0.026*SL
	t_{PLH}	0.257	0.227 + 0.015*SL	0.234 + 0.013*SL	0.251 + 0.012*SL

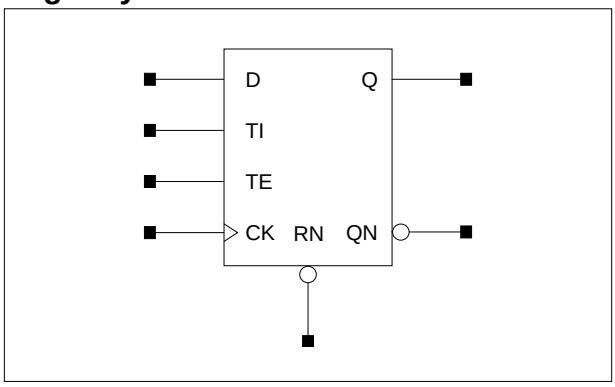
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.082	0.057 + 0.013*SL	0.058 + 0.012*SL	0.049 + 0.013*SL
	t_F	0.062	0.044 + 0.009*SL	0.046 + 0.008*SL	0.045 + 0.009*SL
	t_{PLH}	0.341	0.322 + 0.009*SL	0.332 + 0.007*SL	0.344 + 0.006*SL
	t_{PHL}	0.317	0.301 + 0.008*SL	0.310 + 0.006*SL	0.325 + 0.005*SL
RN to Q	t_F	0.063	0.047 + 0.008*SL	0.046 + 0.009*SL	0.047 + 0.008*SL
	t_{PHL}	0.191	0.175 + 0.008*SL	0.184 + 0.006*SL	0.199 + 0.005*SL
CK to QN	t_R	0.066	0.043 + 0.011*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.056	0.040 + 0.008*SL	0.039 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.397	0.383 + 0.007*SL	0.387 + 0.006*SL	0.389 + 0.006*SL
	t_{PHL}	0.423	0.409 + 0.007*SL	0.416 + 0.005*SL	0.425 + 0.005*SL
RN to QN	t_R	0.072	0.046 + 0.013*SL	0.044 + 0.013*SL	0.048 + 0.013*SL
	t_{PLH}	0.284	0.267 + 0.008*SL	0.272 + 0.007*SL	0.284 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



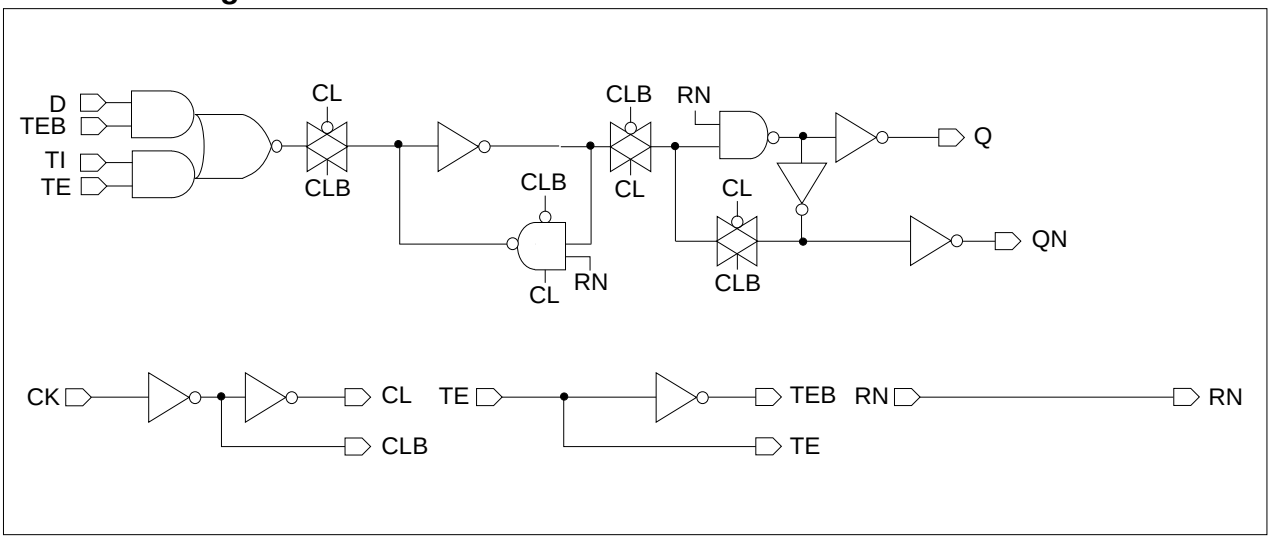
Truth Table

D	TI	TE	CK	RN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1
x	x	x	↓	1	Q(n)	QN(n)

Cell Data

Input Load (SL)										Gate Count	
FD2S_LP					*FD2SD2_LP*					*FD2S_LP*	*FD2SD2_LP*
D	CK	RN	TI	TE	D	CK	RN	TI	TE		
0.7	1.1	1.5	0.7	1.6	0.7	1.2	1.4	0.7	1.7	7.67	8.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2S_LP	FD2SD2_LP
Input Setup Time (D to CK)	t_{SU}	0.345	0.345
Input Hold Time (D to CK)	t_{HD}	0.040	0.044
Input Setup Time (TI to CK)	t_{SU}	0.398	0.398
Input Hold Time (TI to CK)	t_{HD}	0.003	0.004
Input Setup Time (TE to CK)	t_{SU}	0.381	0.379
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.366	0.368
Pulse Width High (CK)	t_{PWH}	0.262	0.279
Pulse Width Low (RN)	t_{PWL}	0.279	0.314
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.783	0.797

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD2S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.103	0.053 + 0.025*SL	0.050 + 0.026*SL	0.040 + 0.026*SL
	t_F	0.075	0.041 + 0.017*SL	0.042 + 0.017*SL	0.032 + 0.017*SL
	t_{PLH}	0.328	0.299 + 0.015*SL	0.307 + 0.013*SL	0.312 + 0.012*SL
	t_{PHL}	0.310	0.285 + 0.012*SL	0.295 + 0.010*SL	0.302 + 0.010*SL
RN to Q	t_F	0.077	0.044 + 0.017*SL	0.042 + 0.017*SL	0.035 + 0.017*SL
	t_{PHL}	0.183	0.158 + 0.012*SL	0.167 + 0.010*SL	0.176 + 0.010*SL
CK to QN	t_R	0.090	0.039 + 0.025*SL	0.035 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.069	0.036 + 0.017*SL	0.034 + 0.017*SL	0.025 + 0.018*SL
	t_{PLH}	0.368	0.342 + 0.013*SL	0.344 + 0.012*SL	0.345 + 0.012*SL
	t_{PHL}	0.384	0.361 + 0.011*SL	0.368 + 0.010*SL	0.371 + 0.010*SL
RN to QN	t_R	0.100	0.045 + 0.028*SL	0.051 + 0.026*SL	0.052 + 0.026*SL
	t_{PLH}	0.257	0.226 + 0.015*SL	0.233 + 0.013*SL	0.251 + 0.012*SL

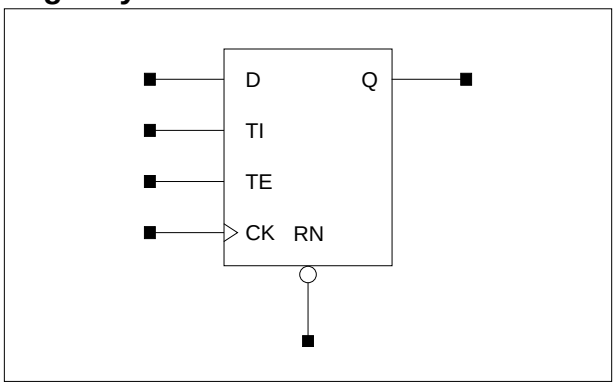
*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

FD2SD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.082	0.056 + 0.013*SL	0.058 + 0.013*SL	0.050 + 0.013*SL
	t_F	0.061	0.042 + 0.009*SL	0.046 + 0.008*SL	0.044 + 0.009*SL
	t_{PLH}	0.341	0.322 + 0.010*SL	0.332 + 0.007*SL	0.344 + 0.006*SL
	t_{PHL}	0.322	0.305 + 0.008*SL	0.315 + 0.006*SL	0.330 + 0.005*SL
RN to Q	t_F	0.064	0.047 + 0.008*SL	0.046 + 0.009*SL	0.047 + 0.008*SL
	t_{PHL}	0.191	0.175 + 0.008*SL	0.184 + 0.006*SL	0.199 + 0.005*SL
CK to QN	t_R	0.065	0.041 + 0.012*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.056	0.040 + 0.008*SL	0.040 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.401	0.387 + 0.007*SL	0.391 + 0.006*SL	0.393 + 0.006*SL
	t_{PHL}	0.423	0.409 + 0.007*SL	0.416 + 0.005*SL	0.424 + 0.005*SL
RN to QN	t_R	0.072	0.046 + 0.013*SL	0.044 + 0.013*SL	0.047 + 0.013*SL
	t_{PLH}	0.283	0.267 + 0.008*SL	0.272 + 0.007*SL	0.283 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Logic Symbol



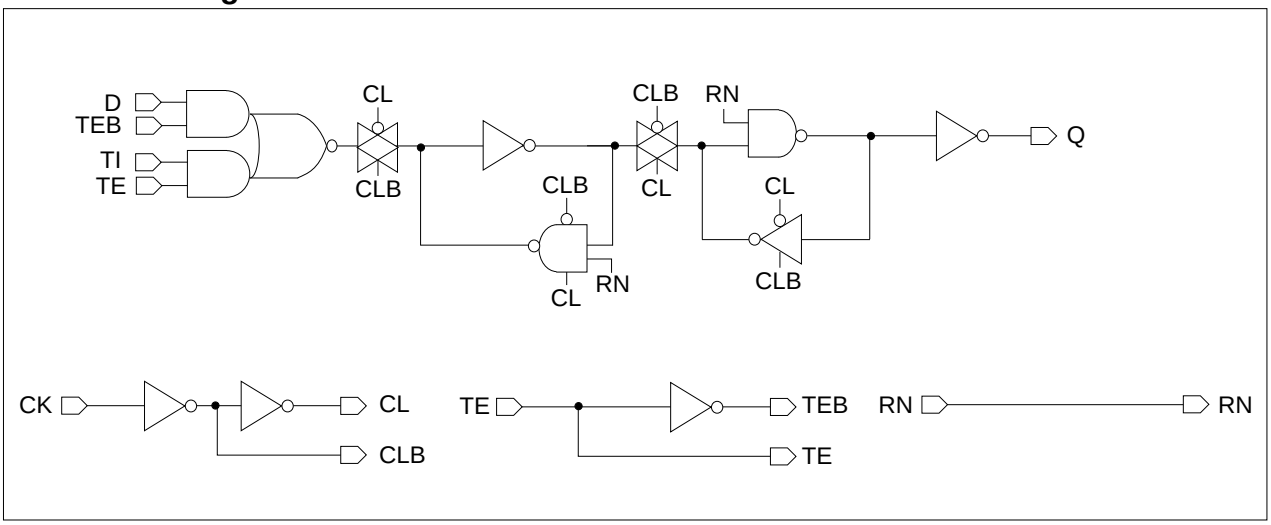
Truth Table

D	TI	TE	CK	RN	Q (n+1)
0	x	0	↑	1	0
1	x	0	↑	1	1
x	0	1	↑	1	0
x	1	1	↑	1	1
x	x	x	x	0	0
x	x	x	↓	1	Q(n)

Cell Data

Input Load (SL)										Gate Count	
FD2SQ_LP					*FD2SQD2_LP*					*FD2SQ_LP*	*FD2SQD2_LP*
D	CK	RN	TI	TE	D	CK	RN	TI	TE		
0.7	1.1	1.4	0.7	1.7	0.7	1.1	1.4	0.7	1.6	7.00	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2SQ_LP	FD2SQD2_LP
Input Setup Time (D to CK)	t_{SU}	0.344	0.344
Input Hold Time (D to CK)	t_{HD}	0.045	0.045
Input Setup Time (TI to CK)	t_{SU}	0.391	0.398
Input Hold Time (TI to CK)	t_{HD}	0.005	0.004
Input Setup Time (TE to CK)	t_{SU}	0.376	0.377
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.366	0.367
Pulse Width High (CK)	t_{PWH}	0.247	0.253
Pulse Width Low (RN)	t_{PWL}	0.293	0.308
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.787	0.789

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD2SQ_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.098	0.049 + 0.024*SL	0.043 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.069	0.035 + 0.017*SL	0.035 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.313	0.285 + 0.014*SL	0.290 + 0.013*SL	0.293 + 0.012*SL
	t_{PHL}	0.297	0.274 + 0.011*SL	0.281 + 0.010*SL	0.285 + 0.010*SL
RN to Q	t_F	0.071	0.036 + 0.017*SL	0.036 + 0.017*SL	0.030 + 0.018*SL
	t_{PHL}	0.168	0.145 + 0.012*SL	0.152 + 0.010*SL	0.157 + 0.010*SL

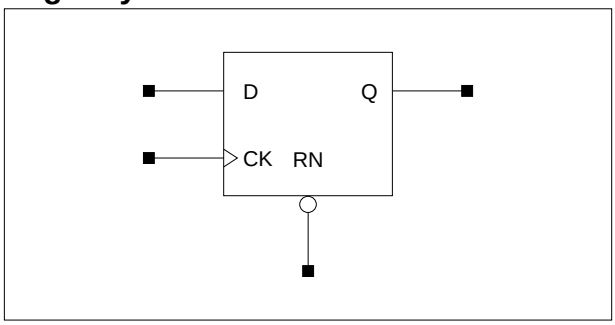
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD2SQD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.077	0.053 + 0.012*SL	0.051 + 0.012*SL	0.040 + 0.013*SL
	t_F	0.055	0.036 + 0.009*SL	0.041 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.319	0.301 + 0.009*SL	0.309 + 0.007*SL	0.317 + 0.006*SL
	t_{PHL}	0.303	0.288 + 0.007*SL	0.296 + 0.005*SL	0.306 + 0.005*SL
RN to Q	t_F	0.058	0.038 + 0.010*SL	0.044 + 0.008*SL	0.037 + 0.009*SL
	t_{PHL}	0.173	0.158 + 0.007*SL	0.166 + 0.005*SL	0.176 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



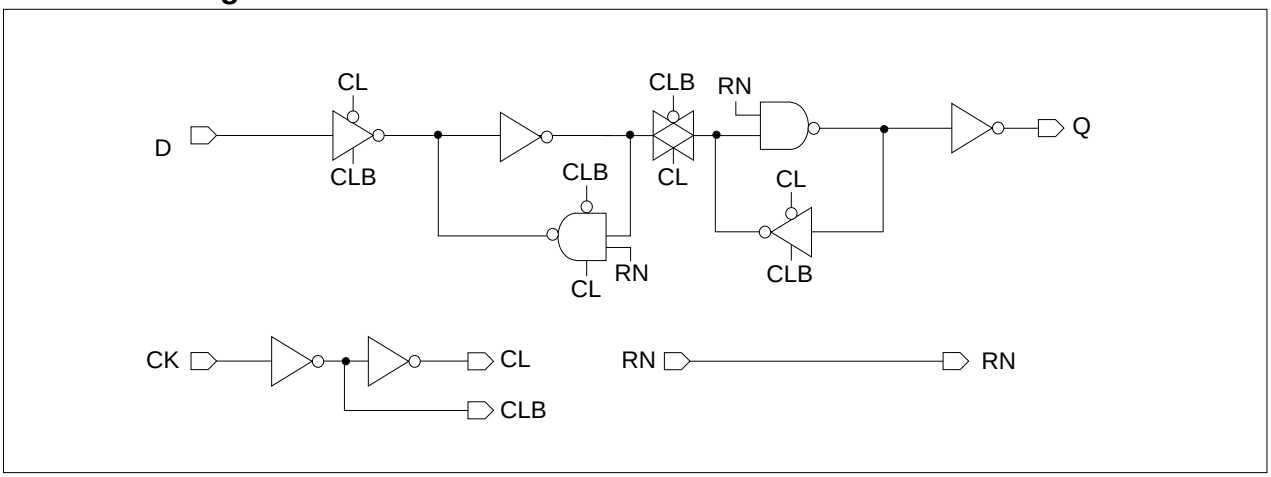
Truth Table

D	CK	RN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	0
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
FD2Q_LP			*FD2QD2_LP*			*FD2Q_LP*	*FD2QD2_LP*
D	CK	RN	D	CK	RN		
0.7	1.2	1.4	0.7	1.2	1.4	5.00	5.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD2Q_LP	FD2QD2_LP
Input Setup Time (D to CK)	t_{SU}	0.247	0.247
Input Hold Time (D to CK)	t_{HD}	0.095	0.095
Pulse Width Low (CK)	t_{PWL}	0.300	0.300
Pulse Width High (CK)	t_{PWH}	0.245	0.251
Pulse Width Low (RN)	t_{PWL}	0.293	0.308
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.778	0.778

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD2Q_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.099	0.049 + 0.025*SL	0.044 + 0.026*SL	0.034 + 0.027*SL
	t_F	0.068	0.034 + 0.017*SL	0.034 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.310	0.282 + 0.014*SL	0.288 + 0.013*SL	0.290 + 0.012*SL
	t_{PHL}	0.290	0.267 + 0.011*SL	0.274 + 0.010*SL	0.277 + 0.010*SL
RN to Q	t_F	0.070	0.036 + 0.017*SL	0.035 + 0.017*SL	0.029 + 0.018*SL
	t_{PHL}	0.167	0.144 + 0.012*SL	0.151 + 0.010*SL	0.155 + 0.010*SL

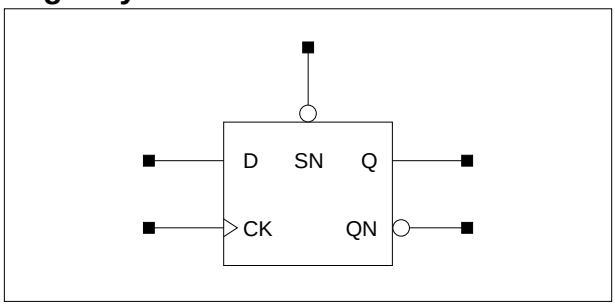
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD2QD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.077	0.053 + 0.012*SL	0.050 + 0.012*SL	0.040 + 0.013*SL
	t_F	0.055	0.036 + 0.009*SL	0.041 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.314	0.297 + 0.009*SL	0.305 + 0.007*SL	0.313 + 0.006*SL
	t_{PHL}	0.295	0.280 + 0.007*SL	0.288 + 0.005*SL	0.298 + 0.005*SL
RN to Q	t_F	0.057	0.038 + 0.009*SL	0.043 + 0.008*SL	0.037 + 0.009*SL
	t_{PHL}	0.172	0.158 + 0.007*SL	0.165 + 0.005*SL	0.175 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



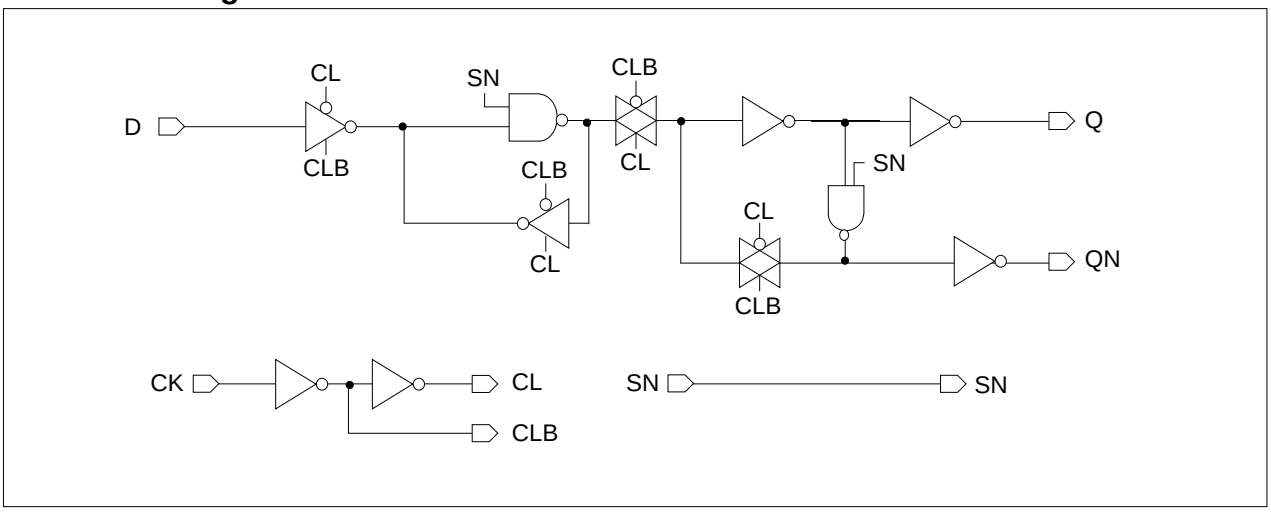
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD3_LP			*FD3D2_LP*			*FD3_LP*	*FD3D2_LP*
D	CK	SN	D	CK	SN		
0.7	1.2	2.0	0.7	1.2	2.2	6.00	7.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3_LP	FD3D2_LP
Input Setup Time (D to CK)	t_{SU}	0.249	0.249
Input Hold Time (D to CK)	t_{HD}	0.085	0.084
Pulse Width Low (CK)	t_{PWL}	0.314	0.315
Pulse Width High (CK)	t_{PWH}	0.259	0.270
Pulse Width Low (SN)	t_{PWL}	0.367	0.392
Recovery Time (SN to CK)	t_{RC}	0.015	0.016
Removal Time (SN to CK)	t_{RM}	0.268	0.267

FD3_LP/FD3D2_LP

D Flip-Flop with Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.093	0.043 + 0.025*SL	0.038 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.071	0.037 + 0.017*SL	0.037 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.301	0.274 + 0.013*SL	0.277 + 0.013*SL	0.280 + 0.012*SL
	t_{PHL}	0.309	0.285 + 0.012*SL	0.293 + 0.010*SL	0.300 + 0.010*SL
SN to Q	t_R	0.109	0.064 + 0.023*SL	0.052 + 0.026*SL	0.034 + 0.027*SL
	t_{PLH}	0.467	0.439 + 0.014*SL	0.446 + 0.012*SL	0.448 + 0.012*SL
CK to QN	t_R	0.099	0.051 + 0.024*SL	0.044 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.071	0.037 + 0.017*SL	0.038 + 0.017*SL	0.027 + 0.018*SL
	t_{PLH}	0.405	0.376 + 0.014*SL	0.383 + 0.013*SL	0.386 + 0.012*SL
	t_{PHL}	0.368	0.345 + 0.012*SL	0.353 + 0.010*SL	0.357 + 0.010*SL
SN to QN	t_F	0.080	0.044 + 0.018*SL	0.046 + 0.018*SL	0.049 + 0.018*SL
	t_{PHL}	0.196	0.169 + 0.013*SL	0.179 + 0.011*SL	0.192 + 0.010*SL

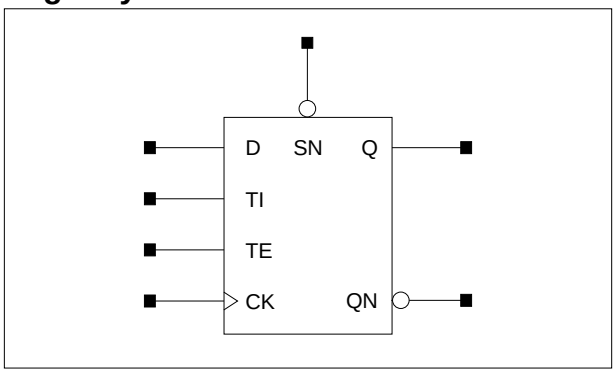
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.069	0.046 + 0.012*SL	0.042 + 0.013*SL	0.034 + 0.013*SL
	t_F	0.059	0.041 + 0.009*SL	0.044 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.304	0.288 + 0.008*SL	0.294 + 0.007*SL	0.298 + 0.006*SL
	t_{PHL}	0.317	0.302 + 0.008*SL	0.310 + 0.006*SL	0.322 + 0.005*SL
SN to Q	t_R	0.087	0.065 + 0.011*SL	0.062 + 0.012*SL	0.044 + 0.013*SL
	t_{PLH}	0.496	0.478 + 0.009*SL	0.488 + 0.007*SL	0.496 + 0.006*SL
CK to QN	t_R	0.076	0.052 + 0.012*SL	0.050 + 0.013*SL	0.040 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.043 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.430	0.412 + 0.009*SL	0.420 + 0.007*SL	0.428 + 0.006*SL
	t_{PHL}	0.395	0.380 + 0.007*SL	0.388 + 0.005*SL	0.399 + 0.005*SL
SN to QN	t_F	0.063	0.043 + 0.010*SL	0.048 + 0.009*SL	0.044 + 0.009*SL
	t_{PHL}	0.192	0.176 + 0.008*SL	0.185 + 0.006*SL	0.197 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



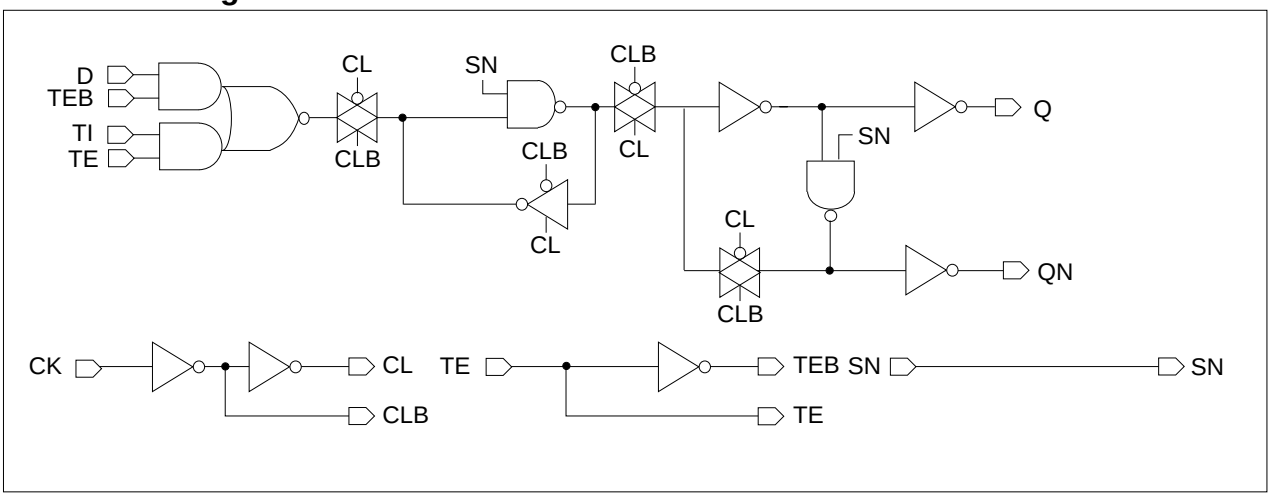
Truth Table

D	TI	TE	CK	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0
x	x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD3S_LP					*FD3SD2_LP*					*FD3S_LP*	*FD3SD2_LP*
D	CK	SN	TI	TE	D	CK	SN	TI	TE		
0.7	1.2	2.0	0.7	1.6	0.7	1.2	2.1	0.7	1.6	8.00	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3S_LP	FD3SD2_LP
Input Setup Time (D to CK)	t_{SU}	0.376	0.375
Input Hold Time (D to CK)	t_{HD}	0.026	0.026
Pulse Width Low (CK)	t_{PWL}	0.392	0.393
Pulse Width High (CK)	t_{PWH}	0.259	0.272
Pulse Width Low (SN)	t_{PWL}	0.365	0.397
Recovery Time (SN to CK)	t_{RC}	0.016	0.016
Removal Time (SN to CK)	t_{RM}	0.268	0.268
Input Setup Time (TI to CK)	t_{SU}	0.421	0.421
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.407	0.406
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD3S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.094	0.044 + 0.025*SL	0.038 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.072	0.038 + 0.017*SL	0.038 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.301	0.274 + 0.013*SL	0.278 + 0.013*SL	0.280 + 0.012*SL
	t_{PHL}	0.309	0.286 + 0.012*SL	0.294 + 0.010*SL	0.300 + 0.010*SL
SN to Q	t_R	0.108	0.063 + 0.023*SL	0.051 + 0.026*SL	0.035 + 0.026*SL
	t_{PLH}	0.465	0.436 + 0.014*SL	0.443 + 0.013*SL	0.445 + 0.012*SL
CK to QN	t_R	0.101	0.053 + 0.024*SL	0.046 + 0.026*SL	0.037 + 0.027*SL
	t_F	0.072	0.037 + 0.017*SL	0.039 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.405	0.377 + 0.014*SL	0.383 + 0.013*SL	0.385 + 0.012*SL
	t_{PHL}	0.369	0.345 + 0.012*SL	0.353 + 0.010*SL	0.357 + 0.010*SL
SN to QN	t_F	0.081	0.046 + 0.018*SL	0.046 + 0.018*SL	0.049 + 0.018*SL
	t_{PHL}	0.195	0.169 + 0.013*SL	0.178 + 0.011*SL	0.190 + 0.010*SL

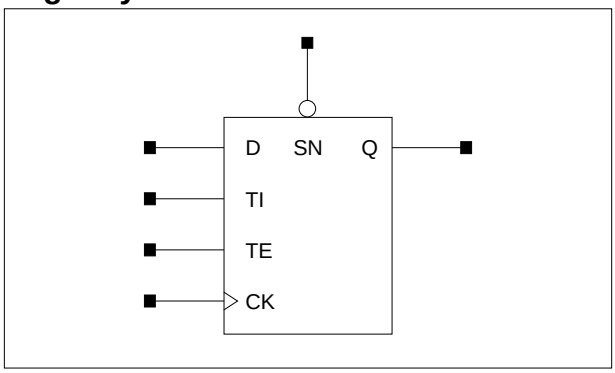
*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

FD3SD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.069	0.046 + 0.012*SL	0.042 + 0.013*SL	0.034 + 0.013*SL
	t_F	0.059	0.041 + 0.009*SL	0.044 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.307	0.290 + 0.008*SL	0.297 + 0.007*SL	0.301 + 0.006*SL
	t_{PHL}	0.320	0.305 + 0.008*SL	0.313 + 0.006*SL	0.324 + 0.005*SL
SN to Q	t_R	0.087	0.062 + 0.012*SL	0.063 + 0.012*SL	0.045 + 0.013*SL
	t_{PLH}	0.502	0.484 + 0.009*SL	0.495 + 0.007*SL	0.502 + 0.006*SL
CK to QN	t_R	0.077	0.053 + 0.012*SL	0.051 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.044 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.434	0.417 + 0.009*SL	0.425 + 0.007*SL	0.433 + 0.006*SL
	t_{PHL}	0.398	0.383 + 0.008*SL	0.392 + 0.005*SL	0.403 + 0.005*SL
SN to QN	t_F	0.064	0.045 + 0.009*SL	0.048 + 0.009*SL	0.045 + 0.009*SL
	t_{PHL}	0.195	0.178 + 0.008*SL	0.188 + 0.006*SL	0.201 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Logic Symbol



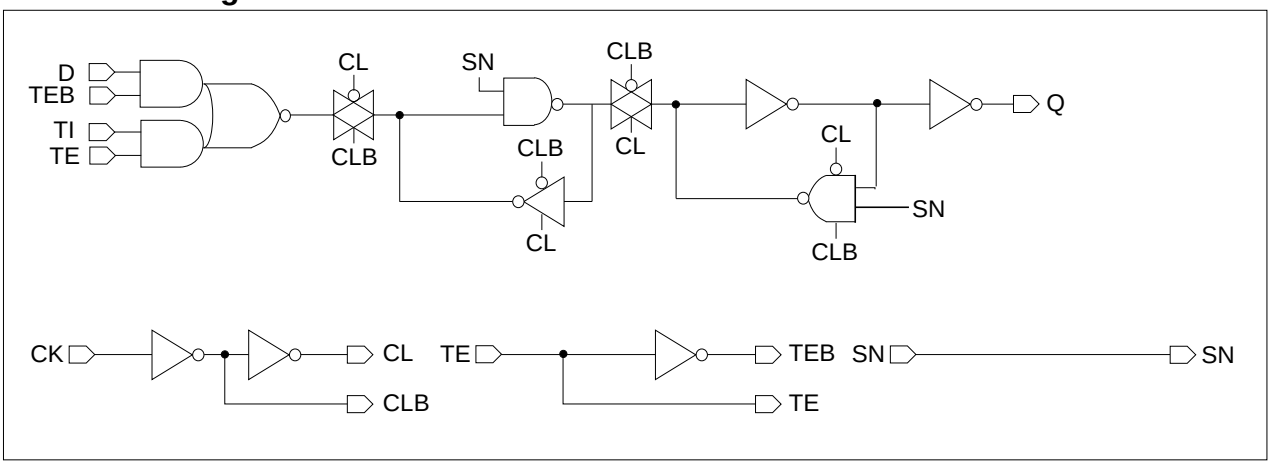
Truth Table

D	TI	TE	CK	SN	Q (n+1)
0	x	0	↑	1	0
1	x	0	↑	1	1
x	0	1	↑	1	0
x	1	1	↑	1	1
x	x	x	x	0	1
x	x	x	↓	1	Q (n)

Cell Data

Input Load (SL)										Gate Count	
FD3SQ_LP					*FD3SQD2_LP*					*FD3SQ_LP*	*FD3SQD2_LP*
D	CK	SN	TI	TE	D	CK	SN	TI	TE		
0.7	2.1	1.3	0.7	1.6	0.7	1.2	1.3	0.7	1.6	7.33	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3SQ_LP	FD3SQD2_LP
Input Setup Time (D to CK)	t_{SU}	0.375	0.375
Input Hold Time (D to CK)	t_{HD}	0.026	0.026
Pulse Width Low (CK)	t_{PWL}	0.391	0.391
Pulse Width High (CK)	t_{PWH}	0.242	0.246
Pulse Width Low (SN)	t_{PWL}	0.838	0.858
Recovery Time (SN to CK)	t_{RC}	0.016	0.016
Removal Time (SN to CK)	t_{RM}	0.268	0.268
Input Setup Time (TI to CK)	t_{SU}	0.422	0.419
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.406	0.405
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD3SQ_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.090	0.040 + 0.025*SL	0.035 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.066	0.032 + 0.017*SL	0.032 + 0.017*SL	0.024 + 0.018*SL
	t_{PLH}	0.285	0.259 + 0.013*SL	0.262 + 0.012*SL	0.263 + 0.012*SL
	t_{PHL}	0.293	0.270 + 0.011*SL	0.276 + 0.010*SL	0.279 + 0.010*SL
SN to Q	t_R	0.116	0.071 + 0.022*SL	0.060 + 0.025*SL	0.038 + 0.026*SL
	t_{PLH}	0.897	0.866 + 0.016*SL	0.879 + 0.013*SL	0.881 + 0.012*SL

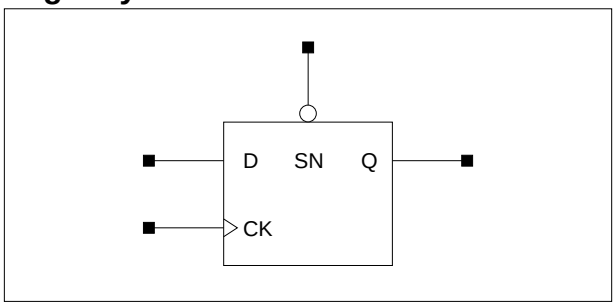
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD3SQD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.067	0.043 + 0.012*SL	0.039 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.053	0.035 + 0.009*SL	0.039 + 0.008*SL	0.031 + 0.009*SL
	t_{PLH}	0.289	0.274 + 0.008*SL	0.279 + 0.006*SL	0.282 + 0.006*SL
	t_{PHL}	0.300	0.286 + 0.007*SL	0.293 + 0.005*SL	0.302 + 0.005*SL
SN to Q	t_R	0.096	0.073 + 0.011*SL	0.072 + 0.012*SL	0.052 + 0.013*SL
	t_{PLH}	0.911	0.890 + 0.011*SL	0.906 + 0.007*SL	0.916 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



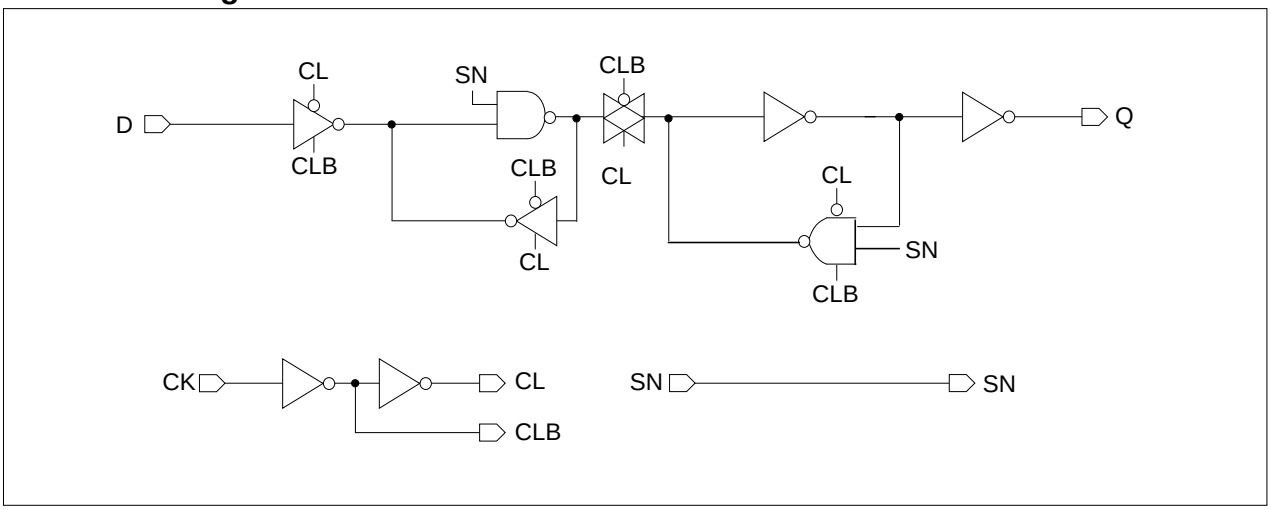
Truth Table

D	CK	SN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	1
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
FD3Q_LP			*FD3QD2_LP*			*FD3Q_LP*	*FD3QD2_LP*
D	CK	SN	D	CK	SN		
0.7	1.2	1.3	0.7	1.2	1.3	5.67	6.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD3Q_LP	FD3QD2_LP
Input Setup Time (D to CK)	t_{SU}	0.248	0.248
Input Hold Time (D to CK)	t_{HD}	0.086	0.087
Pulse Width Low (CK)	t_{PWL}	0.313	0.313
Pulse Width High (CK)	t_{PWH}	0.243	0.248
Pulse Width Low (SN)	t_{PWL}	0.844	0.872
Recovery Time (SN to CK)	t_{RC}	0.015	0.015
Removal Time (SN to CK)	t_{RM}	0.268	0.268

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD3Q_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.093	0.042 + 0.025*SL	0.039 + 0.026*SL	0.034 + 0.027*SL
	t_F	0.070	0.036 + 0.017*SL	0.035 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.288	0.262 + 0.013*SL	0.264 + 0.012*SL	0.266 + 0.012*SL
	t_{PHL}	0.295	0.273 + 0.011*SL	0.279 + 0.010*SL	0.281 + 0.010*SL
SN to Q	t_R	0.119	0.076 + 0.022*SL	0.062 + 0.025*SL	0.041 + 0.026*SL
	t_{PLH}	0.907	0.876 + 0.016*SL	0.888 + 0.013*SL	0.890 + 0.012*SL

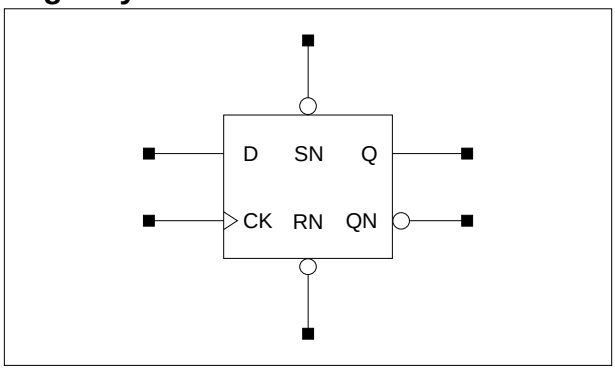
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD3QD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.067	0.044 + 0.011*SL	0.039 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.053	0.035 + 0.009*SL	0.037 + 0.008*SL	0.032 + 0.009*SL
	t_{PLH}	0.290	0.275 + 0.008*SL	0.280 + 0.006*SL	0.283 + 0.006*SL
	t_{PHL}	0.301	0.287 + 0.007*SL	0.294 + 0.005*SL	0.303 + 0.005*SL
SN to Q	t_R	0.096	0.072 + 0.012*SL	0.074 + 0.012*SL	0.052 + 0.013*SL
	t_{PLH}	0.929	0.907 + 0.011*SL	0.924 + 0.007*SL	0.934 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



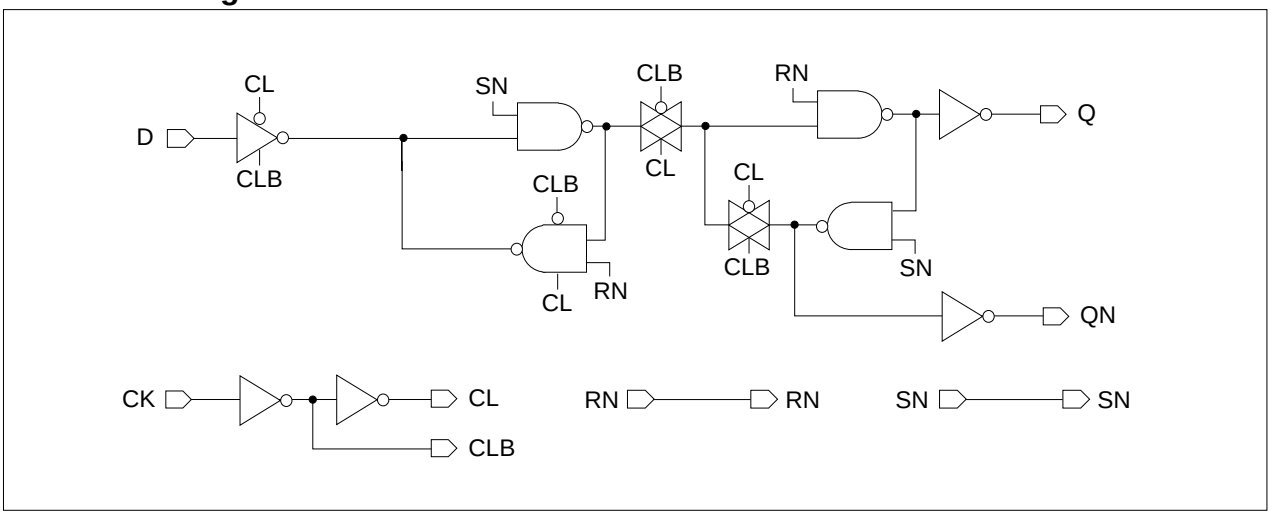
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD4_LP				*FD4D2_LP*				*FD4_LP*	*FD4D2_LP*
D	CK	RN	SN	D	CK	RN	SN		
0.7	1.1	1.6	2.0	0.7	1.1	1.6	2.2	7.00	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4_LP	FD4D2_LP
Input Setup Time (D to CK)	t_{SU}	0.248	0.247
Input Hold Time (D to CK)	t_{HD}	0.090	0.094
Pulse Width Low (CK)	t_{PWL}	0.314	0.314
Pulse Width High (CK)	t_{PWH}	0.271	0.285
Pulse Width Low (RN)	t_{PWL}	0.314	0.314
Pulse Width Low (SN)	t_{PWL}	0.327	0.346
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.816	0.819
Recovery Time (SN to CK)	t_{RC}	0.006	0.002
Removal Time (SN to CK)	t_{RM}	0.293	0.296
Removal Time (SN to RN)	t_{RM}	0.100	0.100
Recovery Time (SN to RN)	t_{RC}	0.180	0.180

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.103	0.054 + 0.024*SL	0.049 + 0.026*SL	0.039 + 0.026*SL
	t_F	0.077	0.042 + 0.017*SL	0.043 + 0.017*SL	0.033 + 0.018*SL
	t_{PLH}	0.336	0.306 + 0.015*SL	0.315 + 0.013*SL	0.320 + 0.012*SL
	t_{PHL}	0.329	0.304 + 0.013*SL	0.314 + 0.010*SL	0.322 + 0.010*SL
RN to Q	t_R	0.102	0.054 + 0.024*SL	0.048 + 0.026*SL	0.036 + 0.026*SL
	t_F	0.077	0.045 + 0.016*SL	0.039 + 0.018*SL	0.036 + 0.018*SL
	t_{PLH}	0.170	0.141 + 0.014*SL	0.149 + 0.012*SL	0.152 + 0.012*SL
	t_{PHL}	0.184	0.159 + 0.012*SL	0.168 + 0.010*SL	0.175 + 0.010*SL
SN to Q	t_R	0.116	0.071 + 0.023*SL	0.062 + 0.025*SL	0.042 + 0.026*SL
	t_{PLH}	0.512	0.481 + 0.016*SL	0.493 + 0.013*SL	0.497 + 0.012*SL
CK to QN	t_R	0.101	0.053 + 0.024*SL	0.046 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.074	0.041 + 0.016*SL	0.039 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.432	0.403 + 0.015*SL	0.411 + 0.013*SL	0.414 + 0.012*SL
	t_{PHL}	0.411	0.386 + 0.012*SL	0.396 + 0.010*SL	0.401 + 0.010*SL
RN to QN	t_R	0.120	0.062 + 0.029*SL	0.072 + 0.026*SL	0.078 + 0.026*SL
	t_{PLH}	0.311	0.275 + 0.018*SL	0.289 + 0.015*SL	0.324 + 0.013*SL
SN to QN	t_R	0.118	0.061 + 0.029*SL	0.070 + 0.026*SL	0.076 + 0.026*SL
	t_F	0.081	0.044 + 0.018*SL	0.046 + 0.018*SL	0.050 + 0.018*SL
	t_{PLH}	0.190	0.155 + 0.018*SL	0.168 + 0.014*SL	0.201 + 0.013*SL
	t_{PHL}	0.201	0.174 + 0.013*SL	0.185 + 0.011*SL	0.197 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD4D2_LP

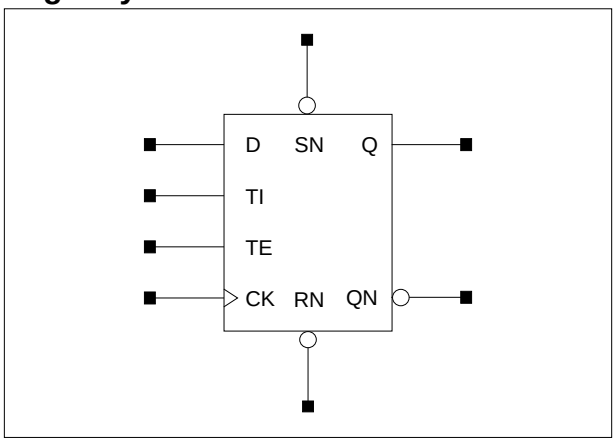
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.082	0.056 + 0.013*SL	0.058 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.062	0.044 + 0.009*SL	0.048 + 0.008*SL	0.045 + 0.009*SL
	t_{PLH}	0.342	0.323 + 0.009*SL	0.333 + 0.007*SL	0.344 + 0.006*SL
	t_{PHL}	0.337	0.321 + 0.008*SL	0.330 + 0.006*SL	0.344 + 0.005*SL
RN to Q	t_R	0.083	0.058 + 0.013*SL	0.058 + 0.012*SL	0.047 + 0.013*SL
	t_F	0.063	0.046 + 0.009*SL	0.046 + 0.009*SL	0.044 + 0.009*SL
	t_{PLH}	0.175	0.157 + 0.009*SL	0.167 + 0.007*SL	0.177 + 0.006*SL
	t_{PHL}	0.189	0.173 + 0.008*SL	0.182 + 0.006*SL	0.195 + 0.005*SL
SN to Q	t_R	0.096	0.072 + 0.012*SL	0.071 + 0.012*SL	0.057 + 0.013*SL
	t_{PLH}	0.538	0.517 + 0.010*SL	0.530 + 0.007*SL	0.544 + 0.006*SL
CK to QN	t_R	0.077	0.052 + 0.013*SL	0.052 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.059	0.041 + 0.009*SL	0.043 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.456	0.438 + 0.009*SL	0.447 + 0.007*SL	0.455 + 0.006*SL
	t_{PHL}	0.443	0.428 + 0.008*SL	0.437 + 0.006*SL	0.449 + 0.005*SL
RN to QN	t_R	0.086	0.058 + 0.014*SL	0.060 + 0.014*SL	0.071 + 0.013*SL
	t_{PLH}	0.324	0.304 + 0.010*SL	0.313 + 0.008*SL	0.334 + 0.007*SL
SN to QN	t_R	0.084	0.055 + 0.015*SL	0.060 + 0.013*SL	0.068 + 0.013*SL
	t_F	0.064	0.045 + 0.009*SL	0.047 + 0.009*SL	0.045 + 0.009*SL
	t_{PLH}	0.174	0.154 + 0.010*SL	0.163 + 0.008*SL	0.184 + 0.007*SL
	t_{PHL}	0.195	0.179 + 0.008*SL	0.188 + 0.006*SL	0.202 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD4S_LP/FD4SD2_LP

D Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Logic Symbol



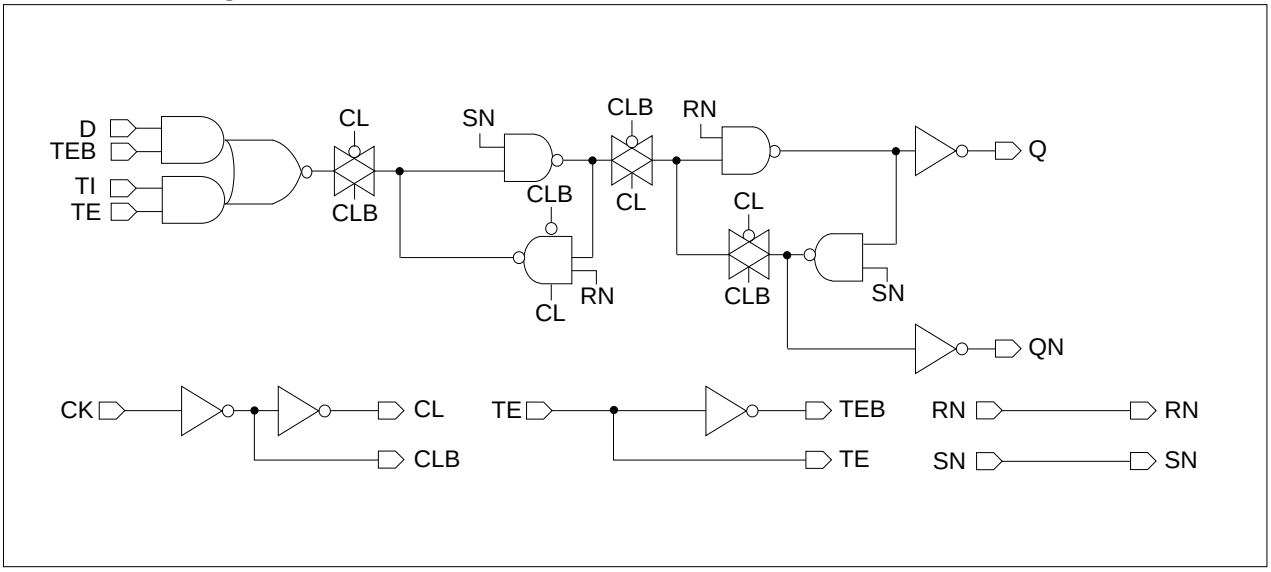
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	1	0	1
1	x	0	↑	1	1	1	0
x	0	1	↑	1	1	0	1
x	1	1	↑	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
FD4S_LP						*FD4SD2_LP*						*FD4S_LP*	*FD4SD2_LP*
D	CK	RN	SN	TI	TE	D	CK	RN	SN	TI	TE		
0.7	1.2	1.6	2.1	0.7	1.6	0.7	1.2	1.6	2.2	0.7	1.6	8.67	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4S_LP	FD4SD2_LP
Input Setup Time (D to CK)	t_{SU}	0.366	0.368
Input Hold Time (D to CK)	t_{HD}	0.038	0.037
Pulse Width Low (CK)	t_{PWL}	0.387	0.392
Pulse Width High (CK)	t_{PWH}	0.268	0.285
Pulse Width Low (RN)	t_{PWL}	0.319	0.347
Pulse Width Low (SN)	t_{PWL}	0.378	0.413
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.821	0.835
Recovery Time (SN to CK)	t_{RC}	0.002	0.000
Removal Time (SN to CK)	t_{RM}	0.295	0.297
Input Setup Time (TI to CK)	t_{SU}	0.413	0.413
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.397	0.397
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000
Recovery Time (SN to RN)	t_{RC}	0.100	0.099
Removal Time (SN to RN)	t_{RM}	0.180	0.181

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD4S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.105	0.056 + 0.025*SL	0.052 + 0.026*SL	0.040 + 0.026*SL
	t_F	0.076	0.043 + 0.016*SL	0.043 + 0.017*SL	0.034 + 0.017*SL
	t_{PLH}	0.336	0.307 + 0.015*SL	0.314 + 0.013*SL	0.320 + 0.012*SL
	t_{PHL}	0.329	0.305 + 0.012*SL	0.314 + 0.010*SL	0.322 + 0.009*SL
RN to Q	t_R	0.104	0.055 + 0.024*SL	0.049 + 0.026*SL	0.038 + 0.027*SL
	t_F	0.076	0.046 + 0.015*SL	0.040 + 0.017*SL	0.036 + 0.017*SL
	t_{PLH}	0.171	0.142 + 0.015*SL	0.150 + 0.013*SL	0.153 + 0.012*SL
	t_{PHL}	0.183	0.159 + 0.012*SL	0.168 + 0.010*SL	0.175 + 0.009*SL
SN to Q	t_R	0.117	0.070 + 0.023*SL	0.062 + 0.025*SL	0.043 + 0.026*SL
	t_{PLH}	0.501	0.470 + 0.015*SL	0.481 + 0.013*SL	0.485 + 0.012*SL
CK to QN	t_R	0.101	0.051 + 0.025*SL	0.047 + 0.026*SL	0.036 + 0.026*SL
	t_F	0.072	0.038 + 0.017*SL	0.038 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.430	0.401 + 0.014*SL	0.408 + 0.013*SL	0.411 + 0.012*SL
	t_{PHL}	0.407	0.383 + 0.012*SL	0.392 + 0.010*SL	0.396 + 0.010*SL
RN to QN	t_R	0.119	0.062 + 0.029*SL	0.072 + 0.026*SL	0.078 + 0.026*SL
	t_{PLH}	0.308	0.272 + 0.018*SL	0.285 + 0.014*SL	0.319 + 0.013*SL
SN to QN	t_R	0.118	0.060 + 0.029*SL	0.071 + 0.026*SL	0.075 + 0.026*SL
	t_F	0.080	0.043 + 0.018*SL	0.046 + 0.018*SL	0.049 + 0.018*SL
	t_{PLH}	0.187	0.152 + 0.018*SL	0.164 + 0.014*SL	0.196 + 0.012*SL
	t_{PHL}	0.196	0.169 + 0.013*SL	0.179 + 0.011*SL	0.191 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD4SD2_LP

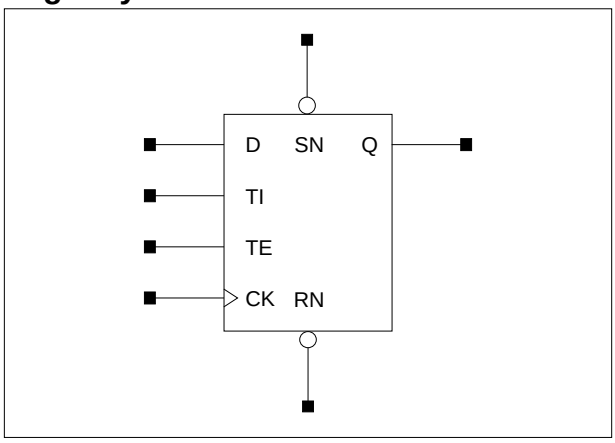
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.082	0.056 + 0.013*SL	0.058 + 0.013*SL	0.050 + 0.013*SL
	t_F	0.064	0.045 + 0.009*SL	0.049 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.345	0.326 + 0.009*SL	0.336 + 0.007*SL	0.348 + 0.006*SL
	t_{PHL}	0.343	0.326 + 0.008*SL	0.336 + 0.006*SL	0.350 + 0.005*SL
RN to Q	t_R	0.083	0.059 + 0.012*SL	0.058 + 0.012*SL	0.047 + 0.013*SL
	t_F	0.064	0.046 + 0.009*SL	0.047 + 0.009*SL	0.045 + 0.009*SL
	t_{PLH}	0.177	0.158 + 0.009*SL	0.168 + 0.007*SL	0.179 + 0.006*SL
	t_{PHL}	0.190	0.174 + 0.008*SL	0.183 + 0.006*SL	0.196 + 0.005*SL
SN to Q	t_R	0.096	0.073 + 0.012*SL	0.072 + 0.012*SL	0.057 + 0.013*SL
	t_{PLH}	0.540	0.519 + 0.010*SL	0.532 + 0.007*SL	0.546 + 0.006*SL
CK to QN	t_R	0.077	0.052 + 0.013*SL	0.053 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.046 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.462	0.444 + 0.009*SL	0.453 + 0.007*SL	0.461 + 0.006*SL
	t_{PHL}	0.447	0.432 + 0.008*SL	0.441 + 0.006*SL	0.453 + 0.005*SL
RN to QN	t_R	0.086	0.058 + 0.014*SL	0.061 + 0.014*SL	0.071 + 0.013*SL
	t_{PLH}	0.326	0.306 + 0.010*SL	0.315 + 0.008*SL	0.336 + 0.007*SL
SN to QN	t_R	0.085	0.056 + 0.014*SL	0.060 + 0.013*SL	0.068 + 0.013*SL
	t_F	0.064	0.046 + 0.009*SL	0.047 + 0.009*SL	0.045 + 0.009*SL
	t_{PLH}	0.175	0.155 + 0.010*SL	0.164 + 0.008*SL	0.185 + 0.007*SL
	t_{PHL}	0.196	0.180 + 0.008*SL	0.189 + 0.006*SL	0.203 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD4SQ_LP/FD4SQD2_LP

D Flip-Flop with Reset, Set, Scan, Q Output Only, 1X/2X Drive

Logic Symbol



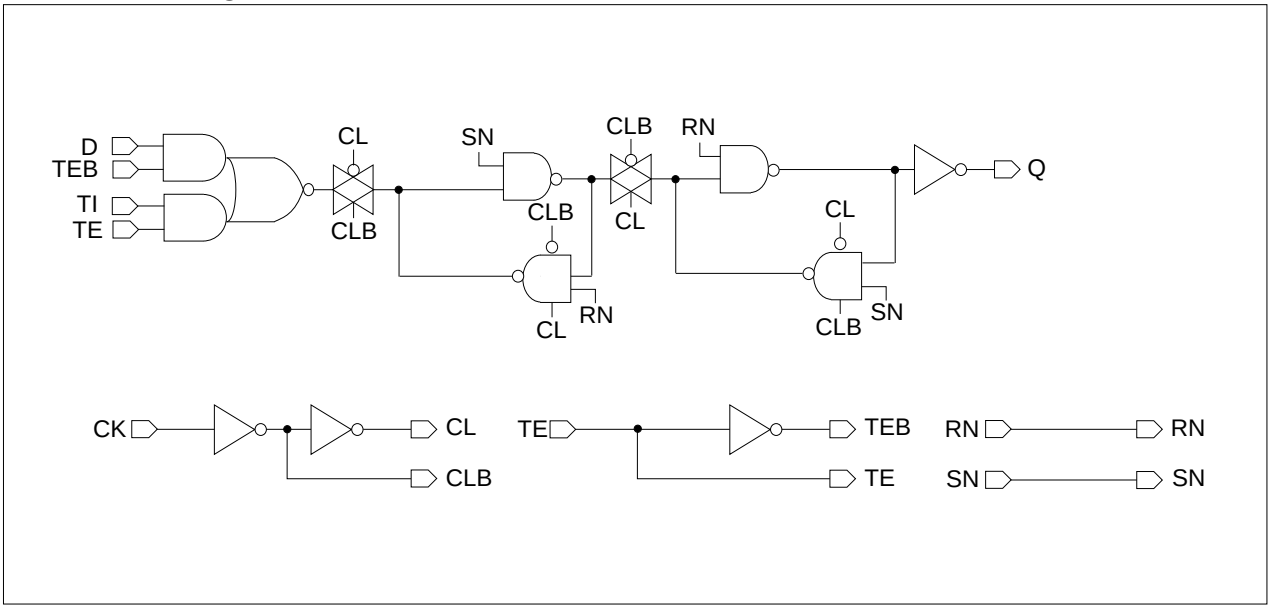
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)
0	x	0	↑	1	1	0
1	x	0	↑	1	1	1
x	0	1	↑	1	1	0
x	1	1	↑	1	1	1
x	x	x	x	1	0	1
x	x	x	x	0	1	0
x	x	x	x	0	0	0
x	x	x	↓	1	1	Q (n)

Cell Data

Input Load (SL)												Gate Count	
FD4SQ_LP						*FD4SQD2_LP*						*FD4SQ_LP*	*FD4SQD2_LP*
D	CK	RN	SN	TI	TE	D	CK	RN	SN	TI	TE		
0.7	1.2	1.5	1.4	0.7	1.6	0.6	1.2	1.5	1.4	0.7	1.6	7.67	8.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4SQ_LP	FD4SQD2_LP
Input Setup Time (D to CK)	t_{SU}	0.365	0.368
Input Hold Time (D to CK)	t_{HD}	0.037	0.037
Pulse Width Low (CK)	t_{PWL}	0.389	0.389
Pulse Width High (CK)	t_{PWH}	0.247	0.252
Pulse Width Low (RN)	t_{PWL}	0.353	0.362
Pulse Width Low (SN)	t_{PWL}	0.845	0.865
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.821	0.824
Recovery Time (SN to CK)	t_{RC}	0.000	0.000
Removal Time (SN to CK)	t_{RM}	0.296	0.296
Input Setup Time (TI to CK)	t_{SU}	0.412	0.414
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.396	0.398
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000
Removal Time (SN to RN)	t_{RM}	0.097	0.098
Recovery Time (SN to RN)	t_{RC}	0.183	0.182

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD4SQ_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.102	0.054 + 0.024*SL	0.047 + 0.026*SL	0.037 + 0.027*SL
	t_F	0.072	0.040 + 0.016*SL	0.039 + 0.017*SL	0.029 + 0.017*SL
	t_{PLH}	0.320	0.292 + 0.014*SL	0.298 + 0.013*SL	0.301 + 0.012*SL
	t_{PHL}	0.313	0.291 + 0.011*SL	0.298 + 0.010*SL	0.302 + 0.009*SL
RN to Q	t_R	0.105	0.059 + 0.023*SL	0.046 + 0.026*SL	0.037 + 0.027*SL
	t_F	0.073	0.040 + 0.016*SL	0.038 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.160	0.132 + 0.014*SL	0.138 + 0.013*SL	0.140 + 0.012*SL
	t_{PHL}	0.170	0.147 + 0.011*SL	0.154 + 0.010*SL	0.158 + 0.009*SL
SN to Q	t_R	0.125	0.080 + 0.023*SL	0.070 + 0.025*SL	0.047 + 0.026*SL
	t_{PLH}	0.928	0.897 + 0.016*SL	0.909 + 0.013*SL	0.913 + 0.012*SL

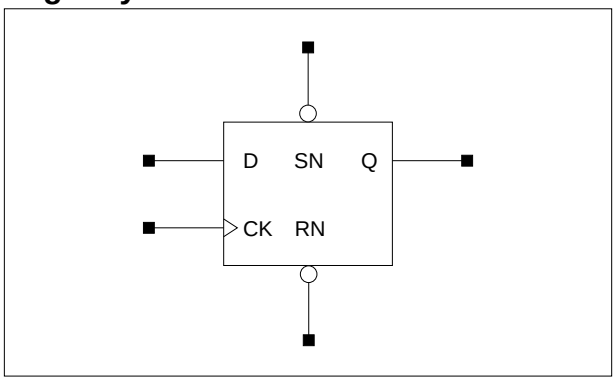
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD4SQD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.078	0.054 + 0.012*SL	0.053 + 0.012*SL	0.042 + 0.013*SL
	t_F	0.057	0.039 + 0.009*SL	0.043 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.323	0.305 + 0.009*SL	0.314 + 0.007*SL	0.321 + 0.006*SL
	t_{PHL}	0.318	0.303 + 0.008*SL	0.311 + 0.005*SL	0.323 + 0.005*SL
RN to Q	t_R	0.076	0.050 + 0.013*SL	0.052 + 0.013*SL	0.041 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.043 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.163	0.145 + 0.009*SL	0.154 + 0.007*SL	0.161 + 0.006*SL
	t_{PHL}	0.175	0.160 + 0.007*SL	0.168 + 0.005*SL	0.178 + 0.005*SL
SN to Q	t_R	0.103	0.077 + 0.013*SL	0.082 + 0.012*SL	0.063 + 0.013*SL
	t_{PLH}	0.942	0.920 + 0.011*SL	0.935 + 0.007*SL	0.949 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



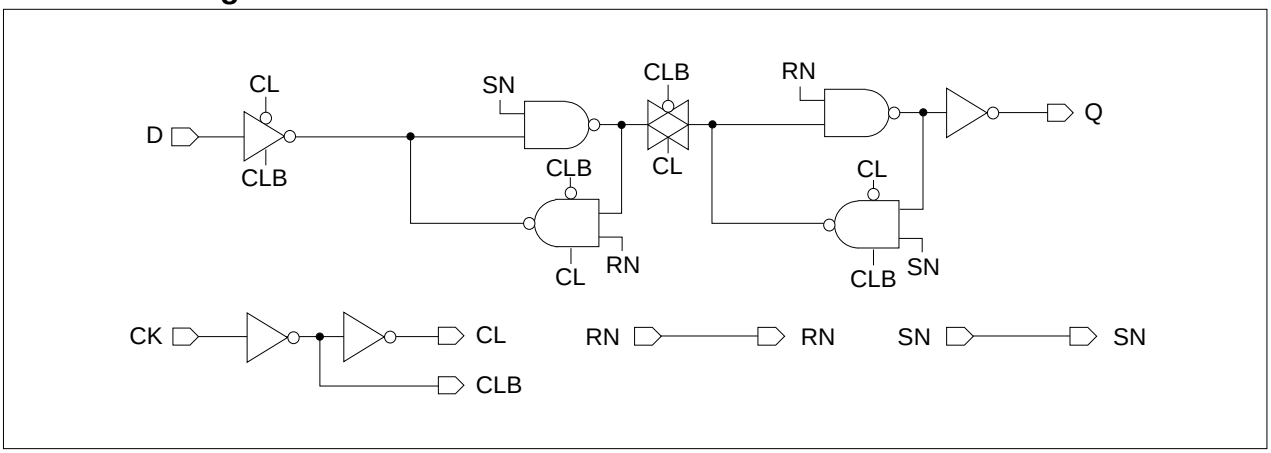
Truth Table

D	CK	RN	SN	Q (n+1)
0	↑	1	1	0
1	↑	1	1	1
x	x	1	0	1
x	x	0	1	0
x	x	0	0	0
x	↓	1	1	Q (n)

Cell Data

Input Load (SL)								Gate Count	
FD4Q_LP				*FD4QD2_LP*				*FD4Q_LP*	*FD4QD2_LP*
D	CK	RN	SN	D	CK	RN	SN		
0.7	1.1	1.5	1.4	0.7	1.1	1.5	1.4	6.00	6.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD4Q_LP	FD4QD2_LP
Input Setup Time (D to CK)	t_{SU}	0.248	0.248
Input Hold Time (D to CK)	t_{HD}	0.091	0.092
Pulse Width Low (CK)	t_{PWL}	0.311	0.312
Pulse Width High (CK)	t_{PWH}	0.246	0.252
Pulse Width Low (RN)	t_{PWL}	0.354	0.366
Pulse Width Low (SN)	t_{PWL}	0.843	0.876
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.811	0.811
Recovery Time (SN to CK)	t_{RC}	0.006	0.006
Removal Time (SN to CK)	t_{RM}	0.293	0.293
Recovery Time (SN to RN)	t_{RC}	0.097	0.100
Removal Time (SN to RN)	t_{RM}	0.183	0.180

FD4Q_LP/FD4QD2_LP

D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD4Q_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.101	0.052 + 0.024*SL	0.047 + 0.026*SL	0.038 + 0.026*SL
	t_F	0.072	0.039 + 0.017*SL	0.039 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.316	0.289 + 0.014*SL	0.294 + 0.012*SL	0.297 + 0.012*SL
	t_{PHL}	0.309	0.286 + 0.011*SL	0.294 + 0.010*SL	0.298 + 0.009*SL
RN to Q	t_R	0.105	0.061 + 0.022*SL	0.046 + 0.026*SL	0.038 + 0.026*SL
	t_F	0.073	0.040 + 0.016*SL	0.039 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.159	0.131 + 0.014*SL	0.137 + 0.012*SL	0.139 + 0.012*SL
	t_{PHL}	0.171	0.148 + 0.011*SL	0.155 + 0.010*SL	0.159 + 0.009*SL
SN to Q	t_R	0.125	0.080 + 0.022*SL	0.071 + 0.025*SL	0.047 + 0.026*SL
	t_{PLH}	0.920	0.887 + 0.016*SL	0.902 + 0.013*SL	0.906 + 0.012*SL

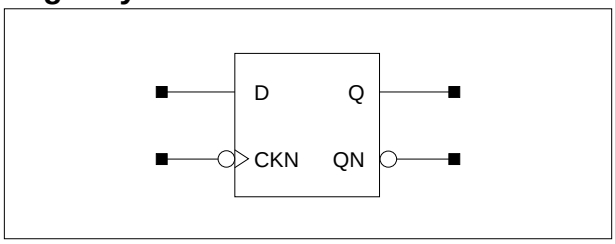
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD4QD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.078	0.054 + 0.012*SL	0.052 + 0.012*SL	0.042 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.044 + 0.008*SL	0.039 + 0.008*SL
	t_{PLH}	0.323	0.306 + 0.009*SL	0.314 + 0.007*SL	0.322 + 0.006*SL
	t_{PHL}	0.317	0.302 + 0.007*SL	0.310 + 0.005*SL	0.322 + 0.005*SL
RN to Q	t_R	0.077	0.053 + 0.012*SL	0.052 + 0.013*SL	0.042 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.044 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.164	0.146 + 0.009*SL	0.154 + 0.007*SL	0.162 + 0.006*SL
	t_{PHL}	0.175	0.161 + 0.007*SL	0.169 + 0.005*SL	0.179 + 0.005*SL
SN to Q	t_R	0.104	0.080 + 0.012*SL	0.081 + 0.012*SL	0.063 + 0.013*SL
	t_{PLH}	0.947	0.925 + 0.011*SL	0.942 + 0.007*SL	0.957 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



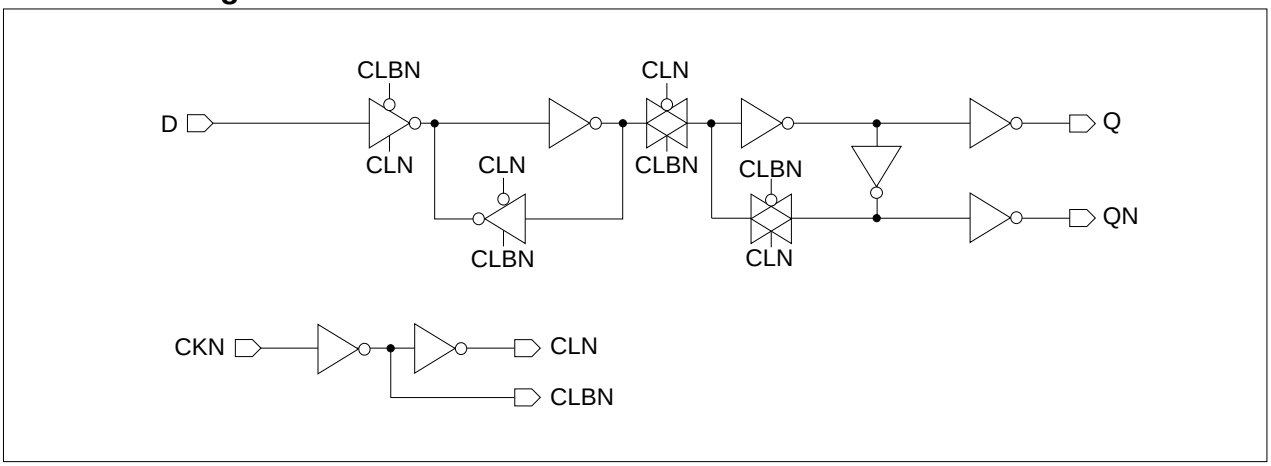
Truth Table

D	CKN	Q (n+1)	QN (n+1)
0	↓	0	1
1	↓	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
FD5_LP		*FD5D2_LP*		*FD5_LP*	*FD5D2_LP*
D	CKN	D	CKN		
0.7	1.2	0.7	1.2	5.33	5.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD5_LP	FD5D2_LP
Input Setup Time (D to CKN)	t_{SU}	0.256	0.255
Input Hold Time (D to CKN)	t_{HD}	0.153	0.155
Pulse Width Low (CKN)	t_{PWL}	0.256	0.268
Pulse Width High (CKN)	t_{PWH}	0.256	0.268

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD5_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.093	0.043 + 0.025*SL	0.039 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.071	0.037 + 0.017*SL	0.035 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.337	0.310 + 0.013*SL	0.313 + 0.013*SL	0.316 + 0.012*SL
	t_{PHL}	0.294	0.271 + 0.012*SL	0.279 + 0.010*SL	0.283 + 0.010*SL
CKN to QN	t_R	0.093	0.042 + 0.025*SL	0.037 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.069	0.035 + 0.017*SL	0.034 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.353	0.327 + 0.013*SL	0.329 + 0.012*SL	0.331 + 0.012*SL
	t_{PHL}	0.392	0.370 + 0.011*SL	0.376 + 0.010*SL	0.378 + 0.010*SL

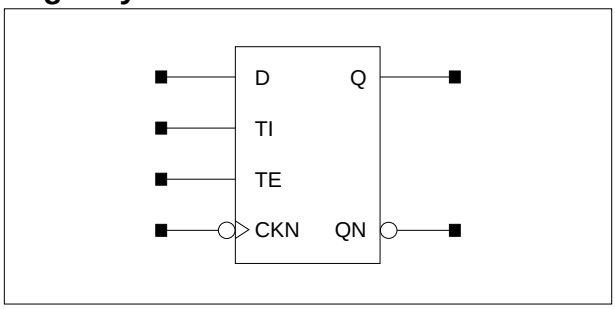
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD5D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.069	0.045 + 0.012*SL	0.042 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.058	0.042 + 0.008*SL	0.040 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.343	0.327 + 0.008*SL	0.333 + 0.007*SL	0.337 + 0.006*SL
	t_{PHL}	0.303	0.288 + 0.008*SL	0.296 + 0.006*SL	0.308 + 0.005*SL
CKN to QN	t_R	0.064	0.040 + 0.012*SL	0.036 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.053	0.036 + 0.008*SL	0.036 + 0.008*SL	0.030 + 0.009*SL
	t_{PLH}	0.380	0.365 + 0.007*SL	0.369 + 0.006*SL	0.371 + 0.006*SL
	t_{PHL}	0.417	0.403 + 0.007*SL	0.410 + 0.005*SL	0.417 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



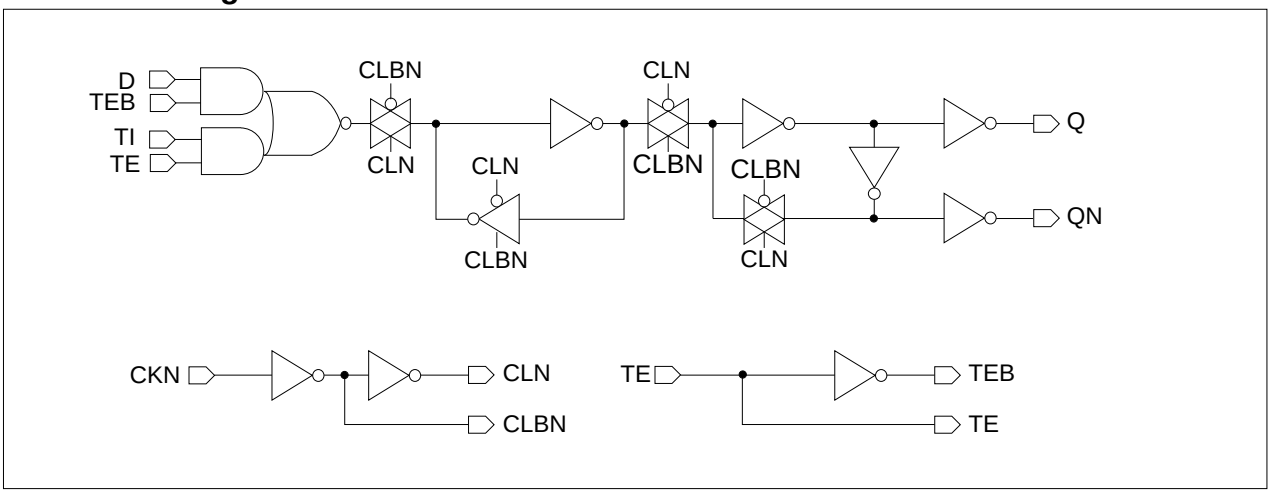
Truth Table

D	TI	TE	CKN	Q (n+1)	QN (n+1)
0	x	0	↓	0	1
1	x	0	↓	1	0
x	0	1	↓	0	1
x	1	1	↓	1	0
x	x	x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD5S_LP				*FD5SD2_LP*				*FD5S_LP*	*FD5SD2_LP*
D	CKN	TI	TE	D	CKN	TI	TE		
0.7	1.1	0.7	1.6	0.7	1.2	0.7	1.6	7.33	7.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD5S_LP	FD5SD2_LP
Input Setup Time (D to CKN)	t_{SU}	0.399	0.397
Input Hold Time (D to CKN)	t_{HD}	0.096	0.096
Pulse Width Low (CKN)	t_{PWL}	0.257	0.269
Pulse Width High (CKN)	t_{PWH}	0.257	0.269
Input Setup Time (TI to CKN)	t_{SU}	0.445	0.441
Input Hold Time (TI to CKN)	t_{HD}	0.084	0.089
Input Setup Time (TE to CKN)	t_{SU}	0.432	0.427
Input Hold Time (TE to CKN)	t_{HD}	0.110	0.115

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD5S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.094	0.043 + 0.025*SL	0.039 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.070	0.036 + 0.017*SL	0.036 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.339	0.313 + 0.013*SL	0.316 + 0.013*SL	0.319 + 0.012*SL
	t_{PHL}	0.296	0.272 + 0.012*SL	0.280 + 0.010*SL	0.285 + 0.010*SL
CKN to QN	t_R	0.093	0.043 + 0.025*SL	0.038 + 0.026*SL	0.034 + 0.027*SL
	t_F	0.071	0.038 + 0.017*SL	0.035 + 0.017*SL	0.027 + 0.018*SL
	t_{PLH}	0.356	0.330 + 0.013*SL	0.332 + 0.012*SL	0.333 + 0.012*SL
	t_{PHL}	0.396	0.374 + 0.011*SL	0.379 + 0.010*SL	0.382 + 0.010*SL

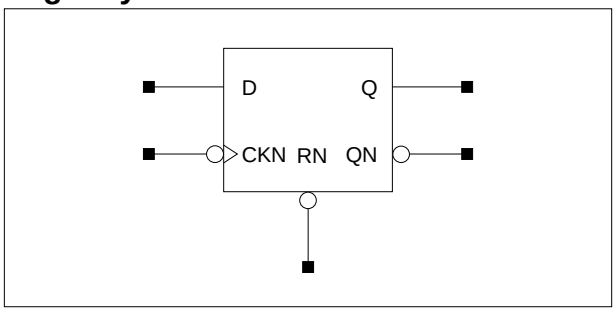
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD5SD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.069	0.045 + 0.012*SL	0.043 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.058	0.041 + 0.008*SL	0.040 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.344	0.329 + 0.008*SL	0.334 + 0.007*SL	0.339 + 0.006*SL
	t_{PHL}	0.305	0.290 + 0.008*SL	0.298 + 0.006*SL	0.310 + 0.005*SL
CKN to QN	t_R	0.063	0.039 + 0.012*SL	0.036 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.052	0.034 + 0.009*SL	0.038 + 0.008*SL	0.031 + 0.009*SL
	t_{PLH}	0.382	0.367 + 0.007*SL	0.371 + 0.006*SL	0.374 + 0.006*SL
	t_{PHL}	0.419	0.405 + 0.007*SL	0.412 + 0.005*SL	0.419 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



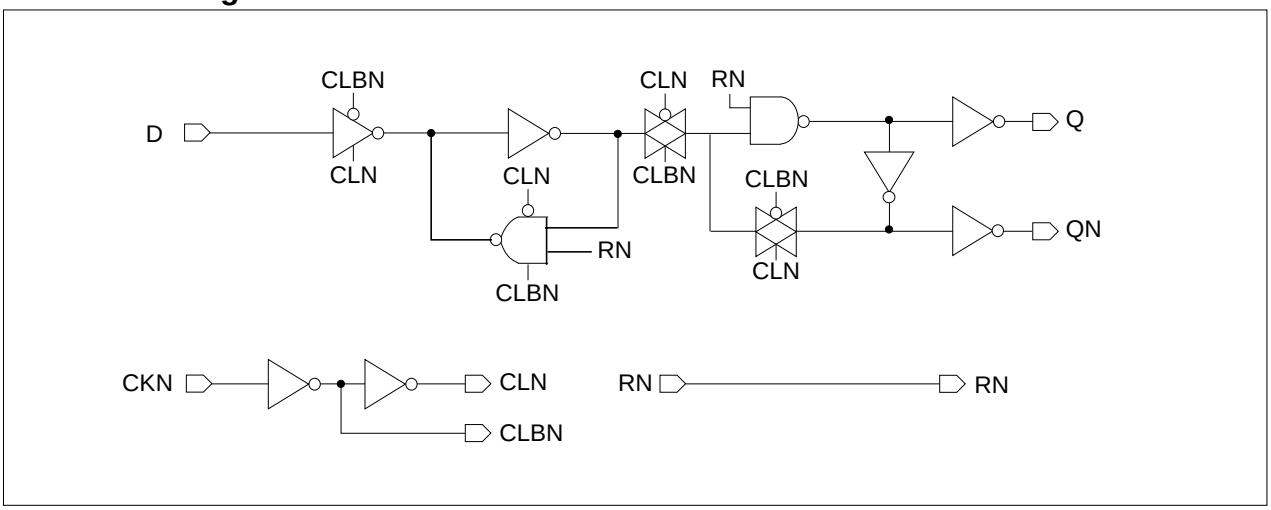
Truth Table

D	CKN	RN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	0	1
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD6_LP			*FD6D2_LP*			*FD6_LP*	*FD6D2_LP*
D	CKN	RN	D	CKN	RN		
0.7	1.2	1.4	0.7	1.2	1.4	5.67	6.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD6_LP	FD6D2_LP
Input Setup Time (D to CKN)	t_{SU}	0.256	0.255
Input Hold Time (D to CKN)	t_{HD}	0.151	0.153
Pulse Width Low (CKN)	t_{PWL}	0.263	0.283
Pulse Width High (CKN)	t_{PWH}	0.263	0.283
Pulse Width Low (RN)	t_{PWL}	0.777	0.775
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.875	0.877

FD6_LP/FD6D2_LP

D Flip-Flop with Negative Edge Trigger, Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.103	0.053 + 0.025*SL	0.049 + 0.026*SL	0.039 + 0.026*SL
	t_F	0.074	0.040 + 0.017*SL	0.041 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.365	0.336 + 0.015*SL	0.344 + 0.013*SL	0.349 + 0.012*SL
	t_{PHL}	0.305	0.280 + 0.012*SL	0.290 + 0.010*SL	0.296 + 0.010*SL
RN to Q	t_F	0.077	0.044 + 0.016*SL	0.041 + 0.017*SL	0.035 + 0.017*SL
	t_{PHL}	0.182	0.157 + 0.012*SL	0.166 + 0.010*SL	0.175 + 0.010*SL
CKN to QN	t_R	0.091	0.040 + 0.025*SL	0.036 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.069	0.035 + 0.017*SL	0.034 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.364	0.338 + 0.013*SL	0.340 + 0.012*SL	0.341 + 0.012*SL
	t_{PHL}	0.422	0.399 + 0.011*SL	0.406 + 0.010*SL	0.409 + 0.010*SL
RN to QN	t_R	0.102	0.046 + 0.028*SL	0.051 + 0.026*SL	0.053 + 0.026*SL
	t_{PLH}	0.257	0.227 + 0.015*SL	0.234 + 0.013*SL	0.251 + 0.012*SL

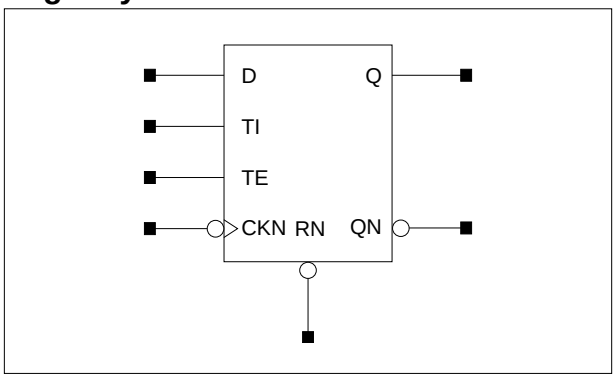
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD6D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.083	0.058 + 0.013*SL	0.057 + 0.013*SL	0.050 + 0.013*SL
	t_F	0.062	0.043 + 0.009*SL	0.046 + 0.008*SL	0.044 + 0.009*SL
	t_{PLH}	0.380	0.361 + 0.010*SL	0.371 + 0.007*SL	0.383 + 0.006*SL
	t_{PHL}	0.317	0.300 + 0.008*SL	0.310 + 0.006*SL	0.325 + 0.005*SL
RN to Q	t_F	0.064	0.047 + 0.008*SL	0.046 + 0.009*SL	0.048 + 0.008*SL
	t_{PHL}	0.192	0.175 + 0.008*SL	0.185 + 0.006*SL	0.199 + 0.005*SL
CKN to QN	t_R	0.066	0.044 + 0.011*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.057	0.040 + 0.008*SL	0.040 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.398	0.383 + 0.007*SL	0.387 + 0.006*SL	0.390 + 0.006*SL
	t_{PHL}	0.463	0.449 + 0.007*SL	0.456 + 0.005*SL	0.464 + 0.005*SL
RN to QN	t_R	0.072	0.046 + 0.013*SL	0.044 + 0.013*SL	0.048 + 0.013*SL
	t_{PLH}	0.285	0.268 + 0.008*SL	0.273 + 0.007*SL	0.285 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



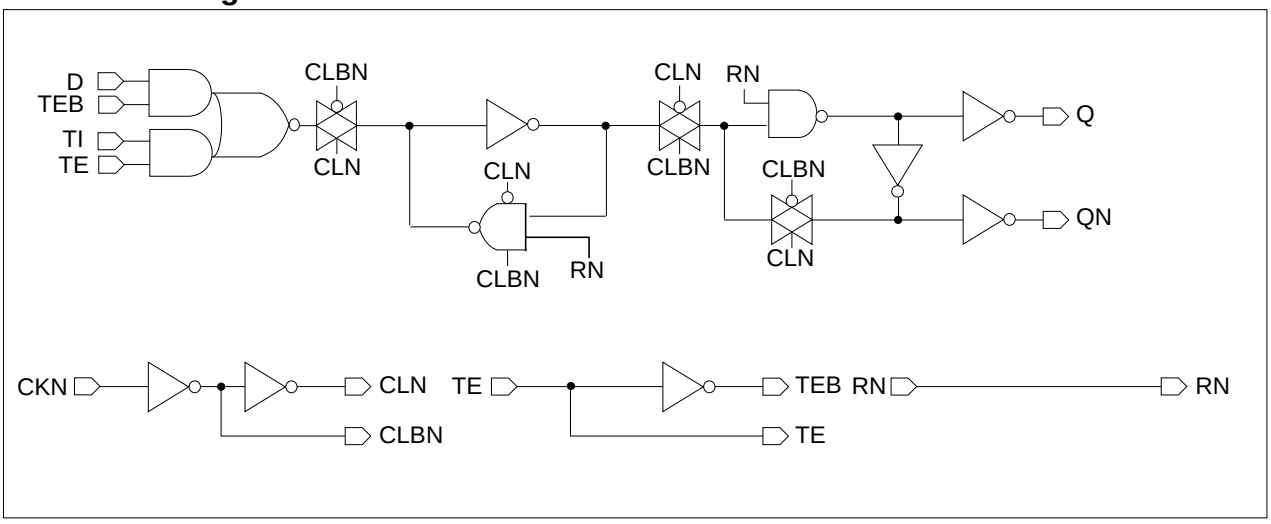
Truth Table

D	TI	TE	CKN	RN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	0	1
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD6S_LP					*FD6SD2_LP*					*FD6S_LP*	*FD6SD2_LP*
D	CKN	RN	TI	TE	D	CKN	RN	TI	TE		
0.7	1.1	1.4	0.7	1.7	0.7	1.1	1.5	0.7	1.7	7.67	8.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD6S_LP	FD6SD2_LP
Input Setup Time (D to CKN)	t_{SU}	0.396	0.397
Input Hold Time (D to CKN)	t_{HD}	0.095	0.096
Pulse Width Low (CKN)	t_{PWL}	0.264	0.283
Pulse Width High (CKN)	t_{PWH}	0.264	0.283
Pulse Width Low (RN)	t_{PWL}	0.779	0.788
Recovery Time (RN to CKN)	t_{RC}	0.000	0.000
Removal Time (RN to CKN)	t_{RM}	0.883	0.894
Input Setup Time (TI to CKN)	t_{SU}	0.444	0.444
Input Hold Time (TI to CKN)	t_{HD}	0.081	0.083
Input Setup Time (TE to CKN)	t_{SU}	0.430	0.429
Input Hold Time (TE to CKN)	t_{HD}	0.107	0.111

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD6S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.103	0.053 + 0.025*SL	0.050 + 0.026*SL	0.040 + 0.026*SL
	t_F	0.074	0.039 + 0.017*SL	0.041 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.369	0.340 + 0.015*SL	0.347 + 0.013*SL	0.353 + 0.012*SL
	t_{PHL}	0.307	0.282 + 0.012*SL	0.292 + 0.010*SL	0.299 + 0.010*SL
RN to Q	t_F	0.077	0.044 + 0.017*SL	0.043 + 0.017*SL	0.035 + 0.017*SL
	t_{PHL}	0.183	0.158 + 0.012*SL	0.167 + 0.010*SL	0.176 + 0.010*SL
CKN to QN	t_R	0.089	0.040 + 0.025*SL	0.033 + 0.026*SL	0.030 + 0.027*SL
	t_F	0.069	0.036 + 0.017*SL	0.034 + 0.017*SL	0.025 + 0.018*SL
	t_{PLH}	0.365	0.339 + 0.013*SL	0.341 + 0.012*SL	0.342 + 0.012*SL
	t_{PHL}	0.425	0.402 + 0.011*SL	0.408 + 0.010*SL	0.411 + 0.010*SL
RN to QN	t_R	0.100	0.045 + 0.028*SL	0.051 + 0.026*SL	0.052 + 0.026*SL
	t_{PLH}	0.256	0.226 + 0.015*SL	0.233 + 0.013*SL	0.251 + 0.012*SL

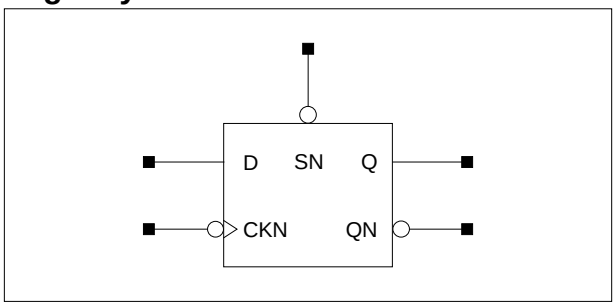
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD6SD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.082	0.056 + 0.013*SL	0.058 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.061	0.042 + 0.009*SL	0.046 + 0.008*SL	0.045 + 0.009*SL
	t_{PLH}	0.383	0.364 + 0.010*SL	0.374 + 0.007*SL	0.386 + 0.006*SL
	t_{PHL}	0.319	0.302 + 0.008*SL	0.312 + 0.006*SL	0.327 + 0.005*SL
RN to Q	t_F	0.064	0.047 + 0.008*SL	0.046 + 0.009*SL	0.047 + 0.008*SL
	t_{PHL}	0.191	0.175 + 0.008*SL	0.185 + 0.006*SL	0.199 + 0.005*SL
CKN to QN	t_R	0.066	0.043 + 0.012*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.056	0.039 + 0.009*SL	0.040 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.399	0.384 + 0.007*SL	0.389 + 0.006*SL	0.391 + 0.006*SL
	t_{PHL}	0.466	0.452 + 0.007*SL	0.459 + 0.005*SL	0.467 + 0.005*SL
RN to QN	t_R	0.071	0.046 + 0.013*SL	0.044 + 0.013*SL	0.047 + 0.013*SL
	t_{PLH}	0.284	0.267 + 0.008*SL	0.273 + 0.007*SL	0.284 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



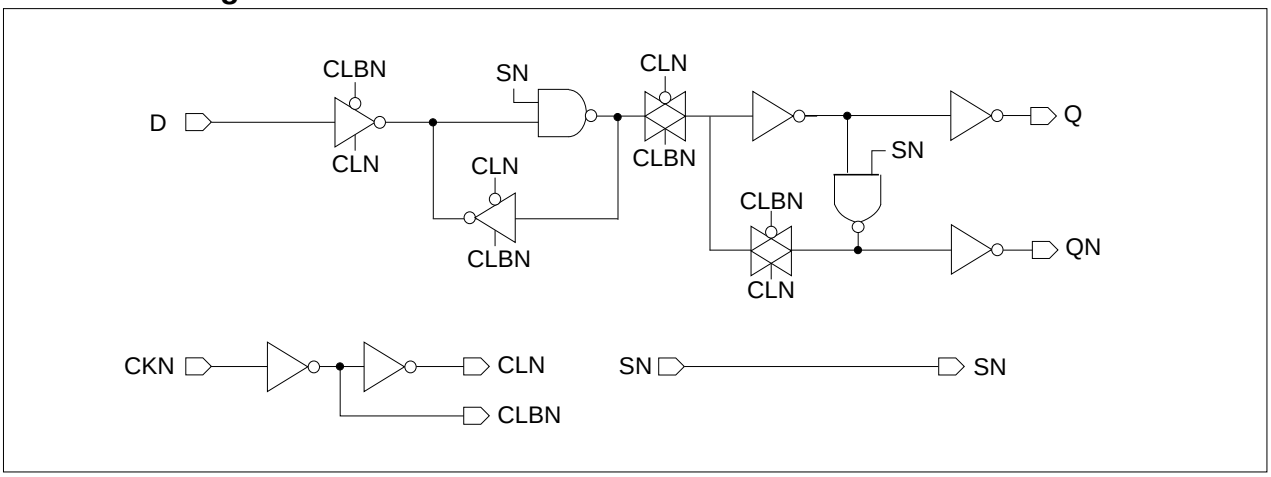
Truth Table

D	CKN	SN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	1	0
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD7_LP			*FD7D2_LP*			*FD7_LP*	*FD7D2_LP*
D	CKN	SN	D	CKN	SN		
0.7	1.2	2.0	0.7	1.2	2.1	6.67	7.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD7_LP	FD7D2_LP
Input Setup Time (D to CKN)	t_{SU}	0.263	0.262
Input Hold Time (D to CKN)	t_{HD}	0.151	0.151
Pulse Width Low (CKN)	t_{PWL}	0.268	0.279
Pulse Width High (CKN)	t_{PWH}	0.268	0.279
Pulse Width Low (SN)	t_{PWL}	0.303	0.302
Recovery Time (SN to CKN)	t_{RC}	0.031	0.030
Removal Time (SN to CKN)	t_{RM}	0.254	0.254

FD7_LP/FD7D2_LP

D Flip-Flop with Negative Edge Trigger, Set, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD7_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.094	0.044 + 0.025*SL	0.039 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.072	0.038 + 0.017*SL	0.037 + 0.017*SL	0.030 + 0.018*SL
	t_{PLH}	0.340	0.313 + 0.013*SL	0.316 + 0.013*SL	0.319 + 0.012*SL
	t_{PHL}	0.311	0.287 + 0.012*SL	0.295 + 0.010*SL	0.301 + 0.010*SL
SN to Q	t_R	0.108	0.062 + 0.023*SL	0.051 + 0.026*SL	0.035 + 0.027*SL
	t_{PLH}	0.470	0.441 + 0.014*SL	0.449 + 0.013*SL	0.451 + 0.012*SL
CKN to QN	t_R	0.105	0.056 + 0.024*SL	0.049 + 0.026*SL	0.039 + 0.027*SL
	t_F	0.075	0.042 + 0.017*SL	0.041 + 0.017*SL	0.031 + 0.018*SL
	t_{PLH}	0.412	0.383 + 0.014*SL	0.390 + 0.013*SL	0.392 + 0.012*SL
	t_{PHL}	0.412	0.388 + 0.012*SL	0.396 + 0.010*SL	0.401 + 0.010*SL
SN to QN	t_F	0.083	0.045 + 0.019*SL	0.049 + 0.018*SL	0.052 + 0.018*SL
	t_{PHL}	0.199	0.173 + 0.013*SL	0.183 + 0.011*SL	0.195 + 0.010*SL

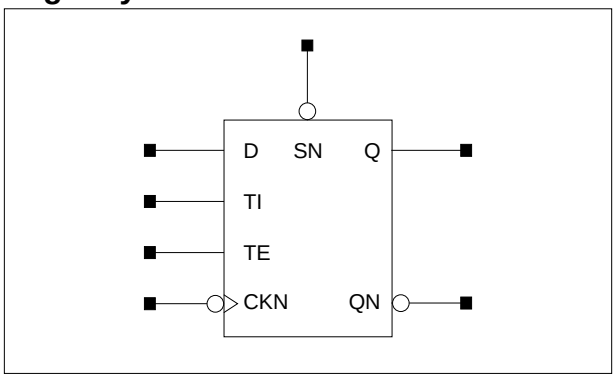
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD7D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.069	0.046 + 0.012*SL	0.042 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.059	0.040 + 0.009*SL	0.044 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.344	0.328 + 0.008*SL	0.334 + 0.006*SL	0.338 + 0.006*SL
	t_{PHL}	0.319	0.303 + 0.008*SL	0.312 + 0.006*SL	0.323 + 0.005*SL
SN to Q	t_R	0.087	0.065 + 0.011*SL	0.062 + 0.012*SL	0.045 + 0.013*SL
	t_{PLH}	0.501	0.482 + 0.009*SL	0.493 + 0.007*SL	0.501 + 0.006*SL
CKN to QN	t_R	0.077	0.052 + 0.012*SL	0.051 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.044 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.434	0.416 + 0.009*SL	0.424 + 0.007*SL	0.432 + 0.006*SL
	t_{PHL}	0.436	0.421 + 0.008*SL	0.429 + 0.005*SL	0.440 + 0.005*SL
SN to QN	t_F	0.064	0.046 + 0.009*SL	0.047 + 0.009*SL	0.045 + 0.009*SL
	t_{PHL}	0.195	0.179 + 0.008*SL	0.188 + 0.006*SL	0.201 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



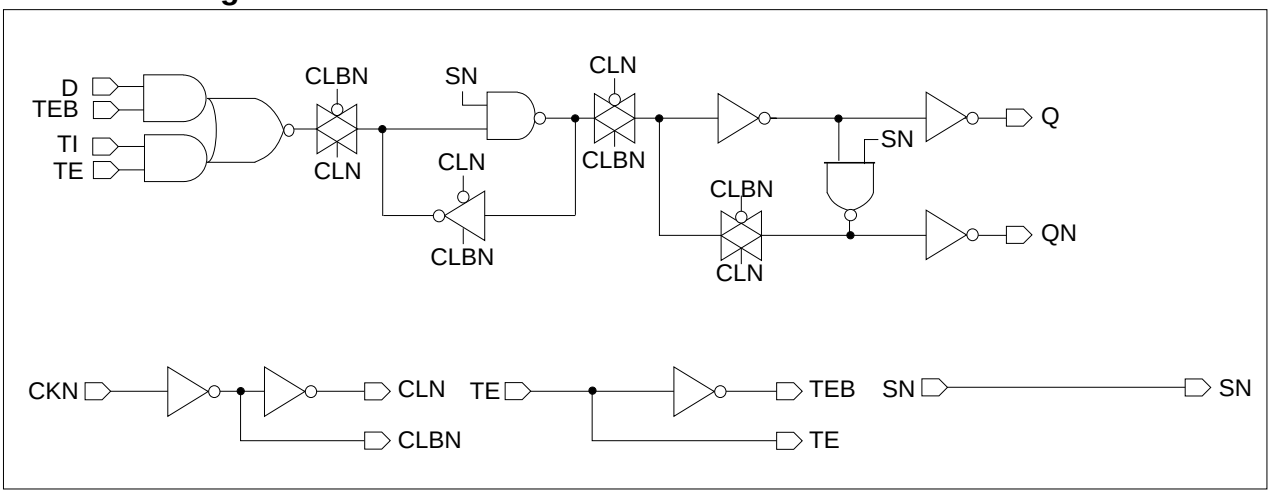
Truth Table

D	TI	TE	CKN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	1	0
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD7S_LP					*FD7SD2_LP*					*FD7S_LP*	*FD7SD2_LP*
D	CKN	SN	TI	TE	D	CKN	SN	TI	TE		
0.7	1.2	2.0	0.7	1.6	0.7	1.2	2.1	0.7	1.6	8.33	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD7S_LP	FD7SD2_LP
Input Setup Time (D to CKN)	t_{SU}	0.413	0.413
Input Hold Time (D to CKN)	t_{HD}	0.095	0.095
Pulse Width Low (CKN)	t_{PWL}	0.267	0.279
Pulse Width High (CKN)	t_{PWH}	0.267	0.279
Pulse Width Low (SN)	t_{PWL}	0.303	0.302
Recovery Time (SN to CKN)	t_{RC}	0.031	0.031
Removal Time (SN to CKN)	t_{RM}	0.254	0.255
Input Setup Time (TI to CKN)	t_{SU}	0.458	0.458
Input Hold Time (TI to CKN)	t_{HD}	0.083	0.081
Input Setup Time (TE to CKN)	t_{SU}	0.443	0.444
Input Hold Time (TE to CKN)	t_{HD}	0.110	0.111

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD7S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.094	0.045 + 0.025*SL	0.039 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.073	0.041 + 0.016*SL	0.038 + 0.017*SL	0.030 + 0.018*SL
	t_{PLH}	0.340	0.313 + 0.013*SL	0.317 + 0.013*SL	0.319 + 0.012*SL
	t_{PHL}	0.311	0.287 + 0.012*SL	0.295 + 0.010*SL	0.301 + 0.010*SL
SN to Q	t_R	0.109	0.064 + 0.023*SL	0.053 + 0.025*SL	0.035 + 0.026*SL
	t_{PLH}	0.469	0.440 + 0.014*SL	0.448 + 0.013*SL	0.449 + 0.012*SL
CKN to QN	t_R	0.102	0.054 + 0.024*SL	0.047 + 0.026*SL	0.037 + 0.027*SL
	t_F	0.073	0.039 + 0.017*SL	0.040 + 0.017*SL	0.030 + 0.018*SL
	t_{PLH}	0.410	0.381 + 0.014*SL	0.388 + 0.013*SL	0.391 + 0.012*SL
	t_{PHL}	0.410	0.387 + 0.012*SL	0.395 + 0.010*SL	0.399 + 0.010*SL
SN to QN	t_F	0.081	0.044 + 0.019*SL	0.048 + 0.018*SL	0.050 + 0.018*SL
	t_{PHL}	0.198	0.172 + 0.013*SL	0.181 + 0.011*SL	0.193 + 0.010*SL

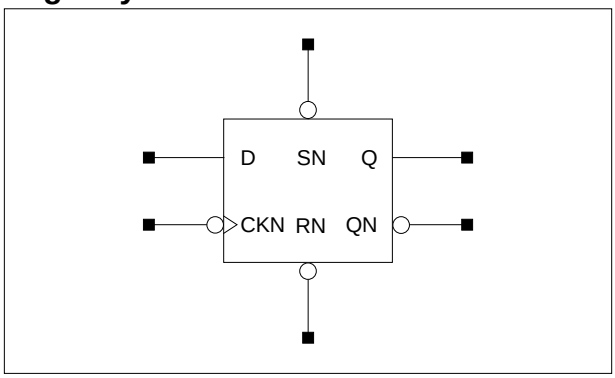
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD7SD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.069	0.046 + 0.012*SL	0.042 + 0.013*SL	0.034 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.044 + 0.008*SL	0.040 + 0.009*SL
	t_{PLH}	0.345	0.329 + 0.008*SL	0.335 + 0.006*SL	0.339 + 0.006*SL
	t_{PHL}	0.320	0.304 + 0.008*SL	0.313 + 0.006*SL	0.324 + 0.005*SL
SN to Q	t_R	0.087	0.063 + 0.012*SL	0.063 + 0.012*SL	0.045 + 0.013*SL
	t_{PLH}	0.502	0.483 + 0.009*SL	0.494 + 0.007*SL	0.502 + 0.006*SL
CKN to QN	t_R	0.076	0.053 + 0.012*SL	0.050 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.043 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.434	0.416 + 0.009*SL	0.425 + 0.007*SL	0.432 + 0.006*SL
	t_{PHL}	0.436	0.421 + 0.008*SL	0.430 + 0.005*SL	0.441 + 0.005*SL
SN to QN	t_F	0.064	0.045 + 0.009*SL	0.047 + 0.009*SL	0.045 + 0.009*SL
	t_{PHL}	0.195	0.178 + 0.008*SL	0.187 + 0.006*SL	0.200 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



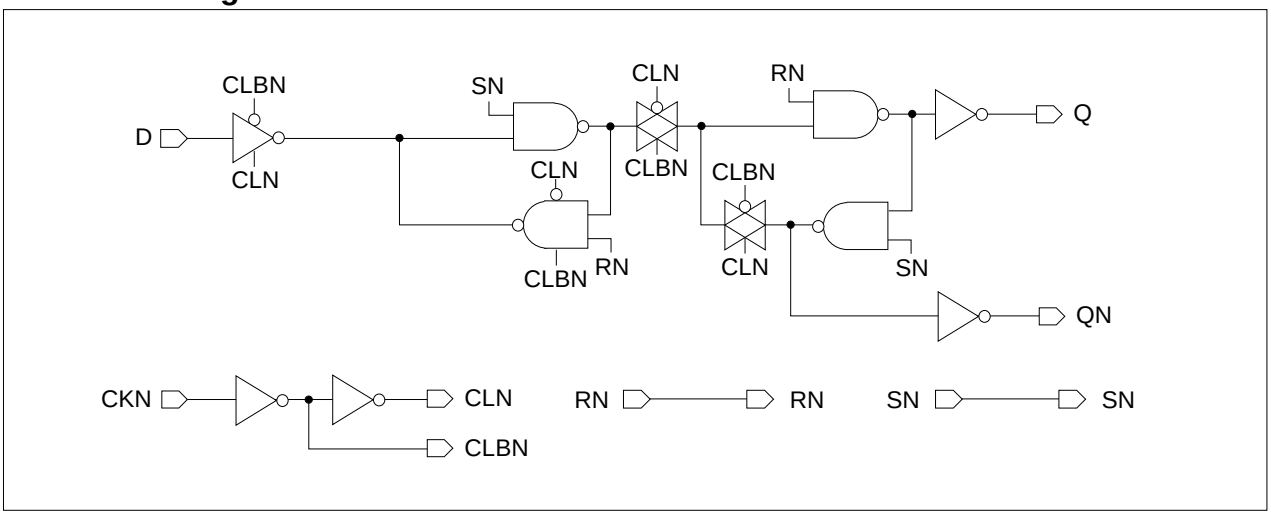
Truth Table

D	CKN	RN	SN	Q (n+1)	QN (n+1)
0	↓	1	1	0	1
1	↓	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD8_LP				*FD8D2_LP*				*FD8_LP*	*FD8D2_LP*
D	CKN	RN	SN	D	CKN	RN	SN		
0.7	1.1	1.5	2.0	0.7	1.2	1.6	2.2	7.00	7.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD8_LP	FD8D2_LP
Input Setup Time (D to CKN)	t_{SU}	0.257	0.257
Input Hold Time (D to CKN)	t_{HD}	0.151	0.154
Pulse Width Low (CKN)	t_{PWL}	0.269	0.289
Pulse Width High (CKN)	t_{PWH}	0.269	0.289
Pulse Width Low (RN)	t_{PWL}	0.814	0.817
Pulse Width Low (SN)	t_{PWL}	0.340	0.339
Recovery Time (RN to CKN)	t_{RC}	0.000	0.000
Removal Time (RN to CKN)	t_{RM}	0.904	0.922
Recovery Time (SN to CKN)	t_{RC}	0.019	0.016
Removal Time (SN to CKN)	t_{RM}	0.288	0.289
Recovery Time (SN to RN)	t_{RC}	0.096	0.099
Removal Time (SN to RN)	t_{RM}	0.184	0.181

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.105	0.056 + 0.025*SL	0.053 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.076	0.043 + 0.017*SL	0.044 + 0.017*SL	0.035 + 0.017*SL
	t_{PLH}	0.373	0.344 + 0.015*SL	0.352 + 0.013*SL	0.358 + 0.012*SL
	t_{PHL}	0.328	0.303 + 0.012*SL	0.313 + 0.010*SL	0.321 + 0.009*SL
RN to Q	t_R	0.104	0.056 + 0.024*SL	0.049 + 0.026*SL	0.039 + 0.026*SL
	t_F	0.077	0.046 + 0.016*SL	0.041 + 0.017*SL	0.037 + 0.017*SL
	t_{PLH}	0.172	0.144 + 0.014*SL	0.151 + 0.012*SL	0.154 + 0.012*SL
	t_{PHL}	0.184	0.160 + 0.012*SL	0.169 + 0.010*SL	0.177 + 0.009*SL
SN to Q	t_R	0.117	0.072 + 0.023*SL	0.063 + 0.025*SL	0.044 + 0.026*SL
	t_{PLH}	0.503	0.472 + 0.015*SL	0.483 + 0.013*SL	0.487 + 0.012*SL
CKN to QN	t_R	0.103	0.055 + 0.024*SL	0.047 + 0.026*SL	0.038 + 0.026*SL
	t_F	0.075	0.041 + 0.017*SL	0.041 + 0.017*SL	0.030 + 0.018*SL
	t_{PLH}	0.429	0.400 + 0.014*SL	0.407 + 0.013*SL	0.410 + 0.012*SL
	t_{PHL}	0.445	0.421 + 0.012*SL	0.430 + 0.010*SL	0.434 + 0.010*SL
RN to QN	t_R	0.122	0.064 + 0.029*SL	0.075 + 0.026*SL	0.080 + 0.026*SL
	t_{PLH}	0.310	0.275 + 0.018*SL	0.287 + 0.014*SL	0.321 + 0.012*SL
SN to QN	t_R	0.121	0.063 + 0.029*SL	0.074 + 0.026*SL	0.078 + 0.026*SL
	t_F	0.081	0.044 + 0.019*SL	0.047 + 0.018*SL	0.050 + 0.018*SL
	t_{PLH}	0.188	0.153 + 0.017*SL	0.166 + 0.014*SL	0.197 + 0.012*SL
	t_{PHL}	0.197	0.171 + 0.013*SL	0.181 + 0.011*SL	0.192 + 0.010*SL

Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD8D2_LP

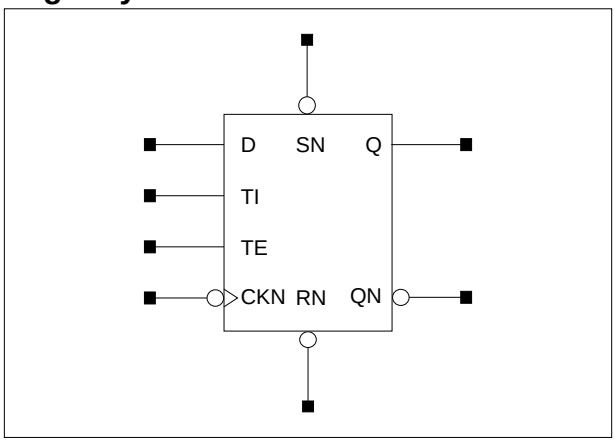
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.082	0.056 + 0.013*SL	0.057 + 0.013*SL	0.050 + 0.013*SL
	t_F	0.063	0.044 + 0.009*SL	0.048 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.385	0.366 + 0.009*SL	0.376 + 0.007*SL	0.387 + 0.006*SL
	t_{PHL}	0.338	0.322 + 0.008*SL	0.331 + 0.006*SL	0.345 + 0.005*SL
RN to Q	t_R	0.083	0.058 + 0.012*SL	0.058 + 0.012*SL	0.047 + 0.013*SL
	t_F	0.064	0.046 + 0.009*SL	0.047 + 0.009*SL	0.045 + 0.009*SL
	t_{PLH}	0.177	0.158 + 0.009*SL	0.168 + 0.007*SL	0.179 + 0.006*SL
	t_{PHL}	0.190	0.174 + 0.008*SL	0.183 + 0.006*SL	0.196 + 0.005*SL
SN to Q	t_R	0.095	0.068 + 0.013*SL	0.074 + 0.012*SL	0.059 + 0.013*SL
	t_{PLH}	0.542	0.521 + 0.010*SL	0.534 + 0.007*SL	0.549 + 0.006*SL
CKN to QN	t_R	0.078	0.054 + 0.012*SL	0.053 + 0.012*SL	0.042 + 0.013*SL
	t_F	0.059	0.041 + 0.009*SL	0.044 + 0.008*SL	0.040 + 0.009*SL
	t_{PLH}	0.459	0.441 + 0.009*SL	0.450 + 0.007*SL	0.458 + 0.006*SL
	t_{PHL}	0.488	0.472 + 0.008*SL	0.481 + 0.006*SL	0.493 + 0.005*SL
RN to QN	t_R	0.087	0.058 + 0.014*SL	0.062 + 0.014*SL	0.071 + 0.013*SL
	t_{PLH}	0.327	0.307 + 0.010*SL	0.316 + 0.008*SL	0.338 + 0.007*SL
SN to QN	t_R	0.086	0.057 + 0.014*SL	0.061 + 0.013*SL	0.069 + 0.013*SL
	t_F	0.065	0.046 + 0.010*SL	0.050 + 0.009*SL	0.047 + 0.009*SL
	t_{PLH}	0.176	0.156 + 0.010*SL	0.165 + 0.008*SL	0.186 + 0.007*SL
	t_{PHL}	0.197	0.180 + 0.008*SL	0.190 + 0.006*SL	0.204 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FD8S_LP/FD8SD2_LP

D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 1X/2X Drive

Logic Symbol



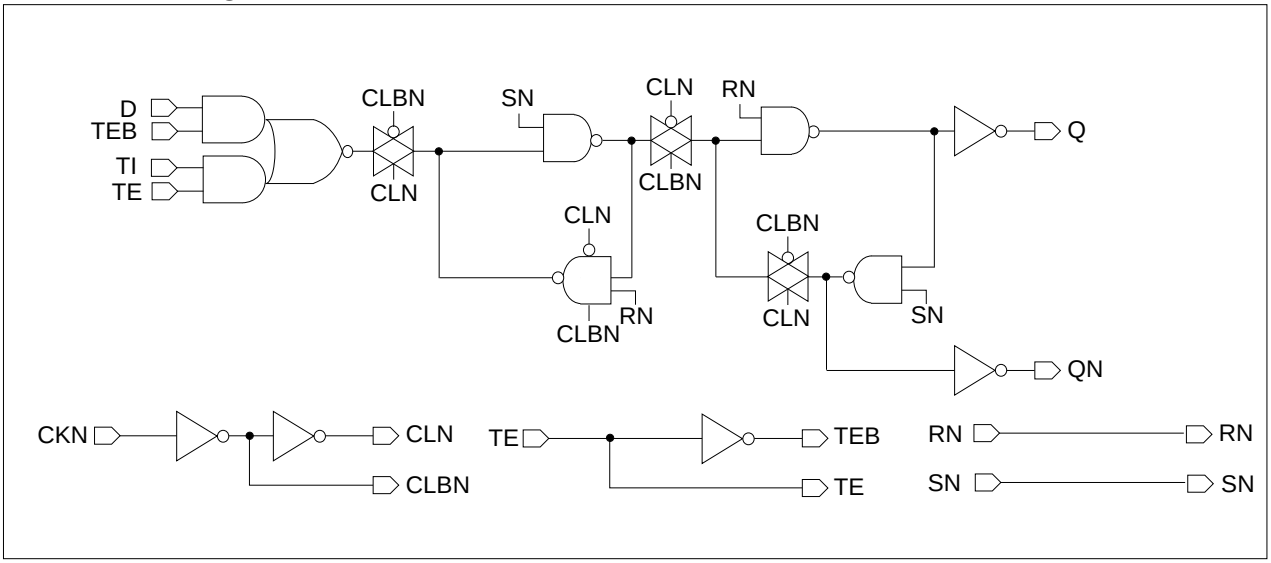
Truth Table

D	TI	TE	CKN	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	1	0	1
1	x	0	↓	1	1	1	0
x	0	1	↓	1	1	0	1
x	1	1	↓	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)												Gate Count	
FD8S_LP						*FD8SD2_LP*						*FD8S_LP*	*FD8SD2_LP*
D	CKN	RN	SN	TI	TE	D	CKN	RN	SN	TI	TE		
0.7	1.2	1.5	2.0	0.7	1.6	0.7	1.2	1.6	2.2	0.7	1.6	9.00	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FD8S_LP	FD8SD2_LP
Input Setup Time (D to CKN)	t_{SU}	0.411	0.412
Input Hold Time (D to CKN)	t_{HD}	0.096	0.096
Pulse Width Low (CKN)	t_{PWL}	0.270	0.289
Pulse Width High (CKN)	t_{PWH}	0.270	0.289
Pulse Width Low (RN)	t_{PWL}	0.816	0.821
Pulse Width Low (SN)	t_{PWL}	0.338	0.339
Recovery Time (RN to CKN)	t_{RC}	0.000	0.000
Removal Time (RN to CKN)	t_{RM}	0.919	0.928
Recovery Time (SN to CKN)	t_{RC}	0.018	0.016
Removal Time (SN to CKN)	t_{RM}	0.288	0.291
Input Setup Time (TI to CKN)	t_{SU}	0.456	0.457
Input Hold Time (TI to CKN)	t_{HD}	0.081	0.084
Input Setup Time (TE to CKN)	t_{SU}	0.441	0.442
Input Hold Time (TE to CKN)	t_{HD}	0.111	0.112
Recovery Time (SN to RN)	t_{RC}	0.098	0.101
Removal Time (SN to RN)	t_{RM}	0.182	0.179

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD8S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.106	0.056 + 0.025*SL	0.052 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.077	0.044 + 0.016*SL	0.043 + 0.017*SL	0.035 + 0.017*SL
	t_{PLH}	0.376	0.347 + 0.015*SL	0.354 + 0.013*SL	0.360 + 0.012*SL
	t_{PHL}	0.329	0.305 + 0.012*SL	0.314 + 0.010*SL	0.323 + 0.009*SL
RN to Q	t_R	0.104	0.056 + 0.024*SL	0.050 + 0.026*SL	0.039 + 0.026*SL
	t_F	0.077	0.046 + 0.016*SL	0.041 + 0.017*SL	0.037 + 0.017*SL
	t_{PLH}	0.172	0.143 + 0.014*SL	0.151 + 0.013*SL	0.154 + 0.012*SL
	t_{PHL}	0.184	0.160 + 0.012*SL	0.169 + 0.010*SL	0.176 + 0.009*SL
SN to Q	t_R	0.117	0.071 + 0.023*SL	0.063 + 0.025*SL	0.044 + 0.026*SL
	t_{PLH}	0.505	0.474 + 0.015*SL	0.485 + 0.013*SL	0.490 + 0.012*SL
CKN to QN	t_R	0.102	0.054 + 0.024*SL	0.047 + 0.026*SL	0.037 + 0.027*SL
	t_F	0.075	0.043 + 0.016*SL	0.040 + 0.017*SL	0.030 + 0.018*SL
	t_{PLH}	0.430	0.402 + 0.014*SL	0.409 + 0.013*SL	0.411 + 0.012*SL
	t_{PHL}	0.447	0.424 + 0.012*SL	0.432 + 0.010*SL	0.436 + 0.010*SL
RN to QN	t_R	0.121	0.064 + 0.029*SL	0.074 + 0.026*SL	0.080 + 0.026*SL
	t_{PLH}	0.309	0.274 + 0.018*SL	0.287 + 0.014*SL	0.321 + 0.013*SL
SN to QN	t_R	0.120	0.063 + 0.029*SL	0.073 + 0.026*SL	0.078 + 0.026*SL
	t_F	0.081	0.044 + 0.018*SL	0.047 + 0.018*SL	0.050 + 0.018*SL
	t_{PLH}	0.188	0.153 + 0.017*SL	0.165 + 0.014*SL	0.197 + 0.012*SL
	t_{PHL}	0.197	0.171 + 0.013*SL	0.181 + 0.011*SL	0.192 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FD8SD2_LP

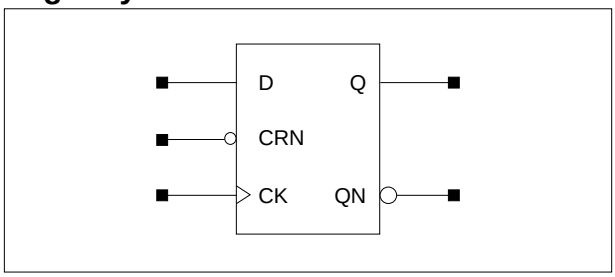
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_R	0.081	0.055 + 0.013*SL	0.058 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.063	0.044 + 0.009*SL	0.048 + 0.008*SL	0.046 + 0.009*SL
	t_{PLH}	0.384	0.365 + 0.009*SL	0.375 + 0.007*SL	0.387 + 0.006*SL
	t_{PHL}	0.338	0.322 + 0.008*SL	0.331 + 0.006*SL	0.345 + 0.005*SL
RN to Q	t_R	0.083	0.058 + 0.012*SL	0.058 + 0.012*SL	0.047 + 0.013*SL
	t_F	0.063	0.046 + 0.009*SL	0.046 + 0.009*SL	0.044 + 0.009*SL
	t_{PLH}	0.176	0.157 + 0.009*SL	0.167 + 0.007*SL	0.178 + 0.006*SL
	t_{PHL}	0.189	0.173 + 0.008*SL	0.182 + 0.006*SL	0.195 + 0.005*SL
SN to Q	t_R	0.096	0.072 + 0.012*SL	0.072 + 0.012*SL	0.057 + 0.013*SL
	t_{PLH}	0.538	0.517 + 0.010*SL	0.530 + 0.007*SL	0.544 + 0.006*SL
CKN to QN	t_R	0.077	0.052 + 0.012*SL	0.052 + 0.012*SL	0.041 + 0.013*SL
	t_F	0.059	0.041 + 0.009*SL	0.043 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.457	0.439 + 0.009*SL	0.448 + 0.007*SL	0.456 + 0.006*SL
	t_{PHL}	0.486	0.470 + 0.008*SL	0.479 + 0.006*SL	0.491 + 0.005*SL
RN to QN	t_R	0.086	0.058 + 0.014*SL	0.060 + 0.014*SL	0.071 + 0.013*SL
	t_{PLH}	0.325	0.304 + 0.010*SL	0.314 + 0.008*SL	0.335 + 0.007*SL
SN to QN	t_R	0.085	0.056 + 0.014*SL	0.059 + 0.014*SL	0.068 + 0.013*SL
	t_F	0.064	0.043 + 0.010*SL	0.049 + 0.009*SL	0.046 + 0.009*SL
	t_{PLH}	0.175	0.155 + 0.010*SL	0.164 + 0.008*SL	0.185 + 0.007*SL
	t_{PHL}	0.196	0.179 + 0.008*SL	0.189 + 0.006*SL	0.202 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FDS2_LP/FDS2D2_LP

D Flip-Flop with Synchronous Clear, 1X/2X Drive

Logic Symbol



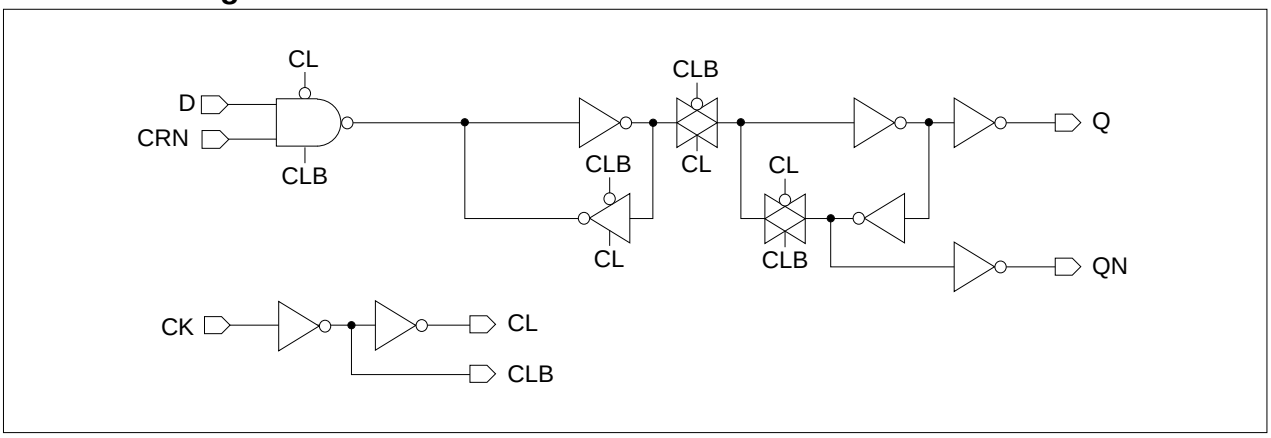
Truth Table

D	CRN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	0	1
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FDS2_LP			*FDS2D2_LP*			*FDS2_LP*	*FDS2D2_LP*
D	CRN	CK	D	CRN	CK		
0.7	0.7	1.1	0.7	0.7	1.1	5.67	6.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS2_LP	FDS2D2_LP
Input Setup Time (D to CK)	t_{SU}	0.308	0.306
Input Hold Time (D to CK)	t_{HD}	0.076	0.079
Pulse Width Low (CK)	t_{PWL}	0.332	0.335
Pulse Width High (CK)	t_{PWH}	0.253	0.266
Input Setup Time (CRN to CK)	t_{SU}	0.309	0.308
Input Hold Time (CRN to CK)	t_{HD}	0.073	0.075

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FDS2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.093	0.043 + 0.025*SL	0.038 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.071	0.037 + 0.017*SL	0.036 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.296	0.269 + 0.013*SL	0.272 + 0.013*SL	0.275 + 0.012*SL
	t_{PHL}	0.291	0.268 + 0.012*SL	0.275 + 0.010*SL	0.280 + 0.010*SL
CK to QN	t_R	0.090	0.040 + 0.025*SL	0.034 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.069	0.036 + 0.016*SL	0.033 + 0.017*SL	0.025 + 0.018*SL
	t_{PLH}	0.348	0.322 + 0.013*SL	0.325 + 0.012*SL	0.326 + 0.012*SL
	t_{PHL}	0.350	0.327 + 0.011*SL	0.333 + 0.010*SL	0.336 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FDS2D2_LP

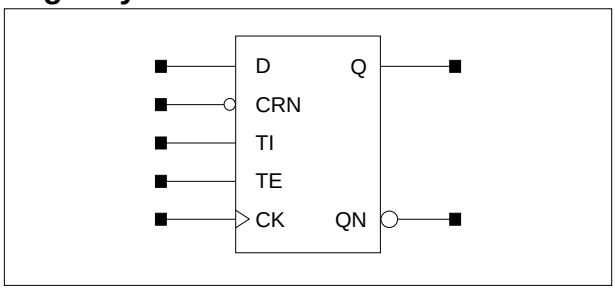
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.069	0.046 + 0.012*SL	0.042 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.058	0.040 + 0.009*SL	0.042 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.305	0.289 + 0.008*SL	0.295 + 0.007*SL	0.299 + 0.006*SL
	t_{PHL}	0.305	0.290 + 0.008*SL	0.298 + 0.006*SL	0.310 + 0.005*SL
CK to QN	t_R	0.064	0.041 + 0.012*SL	0.037 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.052	0.034 + 0.009*SL	0.036 + 0.008*SL	0.029 + 0.009*SL
	t_{PLH}	0.382	0.367 + 0.007*SL	0.371 + 0.006*SL	0.374 + 0.006*SL
	t_{PHL}	0.379	0.365 + 0.007*SL	0.372 + 0.005*SL	0.380 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FDS2S_LP/FDS2SD2_LP

D Flip-Flop with Synchronous Clear, Scan, 1X/2X Drive

Logic Symbol



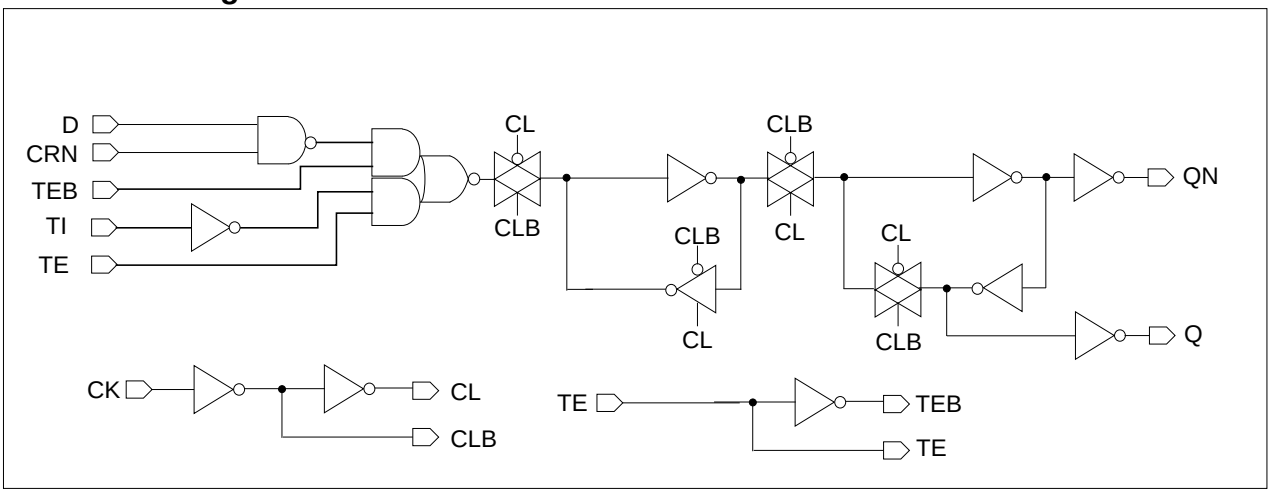
Truth Table

D	CRN	TI	TE	CK	Q (n+1)	QN (n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	0	x	0	↑	0	1
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	x	x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FDS2S_LP					*FDS2SD2_LP*					*FDS2S_LP*	*FDS2SD2_LP*
D	CRN	CK	TI	TE	D	CRN	CK	TI	TE		
0.7	0.7	1.2	0.9	1.7	0.7	0.7	1.2	0.9	1.6	8.33	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS2S_LP	FDS2SD2_LP
Input Setup Time (D to CK)	t_{SU}	0.408	0.410
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (CRN to CK)	t_{SU}	0.406	0.408
Input Hold Time (CRN to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.363	0.365
Pulse Width High (CK)	t_{PWH}	0.255	0.266
Input Setup Time (TI to CK)	t_{SU}	0.447	0.446
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.378	0.379
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FDS2S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.091	0.041 + 0.025*SL	0.035 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.070	0.037 + 0.016*SL	0.034 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.355	0.329 + 0.013*SL	0.331 + 0.012*SL	0.332 + 0.012*SL
	t_{PHL}	0.354	0.331 + 0.011*SL	0.337 + 0.010*SL	0.340 + 0.010*SL
CK to QN	t_R	0.094	0.043 + 0.025*SL	0.039 + 0.026*SL	0.034 + 0.027*SL
	t_F	0.071	0.037 + 0.017*SL	0.037 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.299	0.272 + 0.013*SL	0.276 + 0.013*SL	0.278 + 0.012*SL
	t_{PHL}	0.296	0.273 + 0.012*SL	0.281 + 0.010*SL	0.285 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FDS2SD2_LP

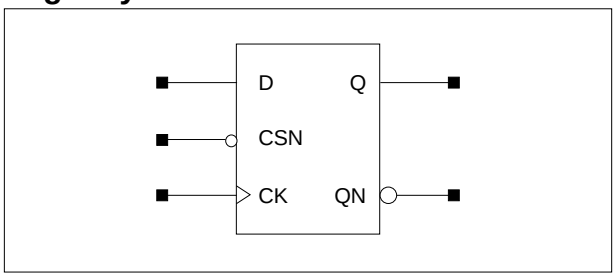
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.064	0.040 + 0.012*SL	0.037 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.053	0.034 + 0.009*SL	0.038 + 0.008*SL	0.031 + 0.009*SL
	t_{PLH}	0.381	0.366 + 0.007*SL	0.370 + 0.006*SL	0.372 + 0.006*SL
	t_{PHL}	0.378	0.364 + 0.007*SL	0.371 + 0.005*SL	0.378 + 0.005*SL
CK to QN	t_R	0.069	0.045 + 0.012*SL	0.043 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.057	0.040 + 0.009*SL	0.041 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.303	0.287 + 0.008*SL	0.293 + 0.007*SL	0.298 + 0.006*SL
	t_{PHL}	0.303	0.288 + 0.008*SL	0.297 + 0.006*SL	0.309 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FDS3_LP/FDS3D2_LP

D Flip-Flop with Synchronous Set, 1X/2X Drive

Logic Symbol



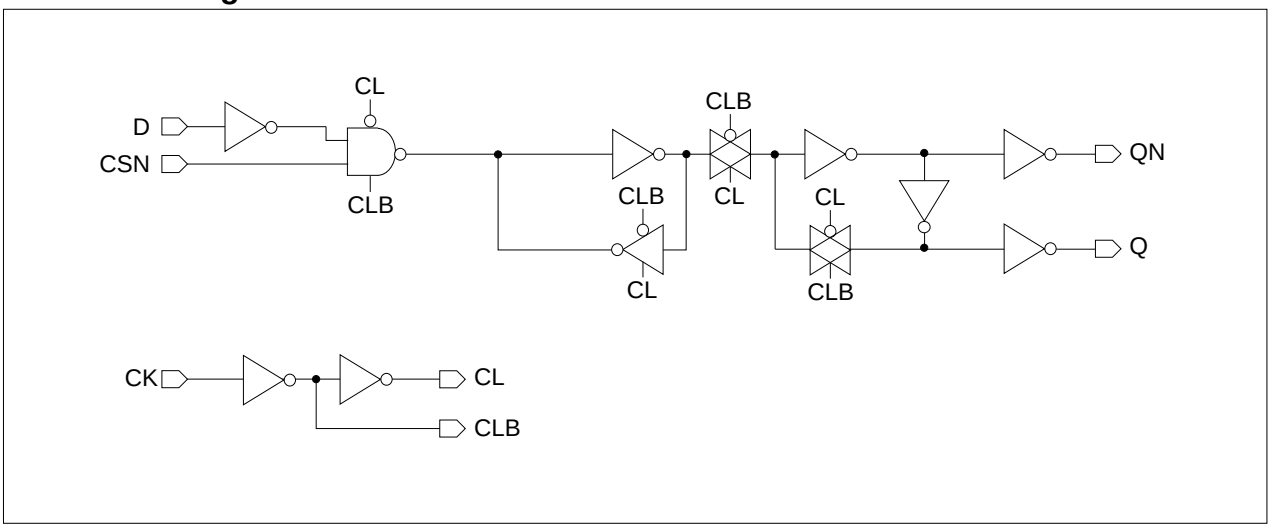
Truth Table

D	CSN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	1	0
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FDS3_LP			*FDS3D2_LP*			*FDS3_LP*	*FDS3D2_LP*
D	CSN	CK	D	CSN	CK		
0.9	0.7	1.1	0.9	0.7	1.2	6.33	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS3_LP	FDS3D2_LP
Input Setup Time (D to CK)	t_{SU}	0.372	0.368
Input Hold Time (D to CK)	t_{HD}	0.054	0.057
Input Setup Time (CSN to CK)	t_{SU}	0.309	0.306
Input Hold Time (CSN to CK)	t_{HD}	0.074	0.077
Pulse Width Low (CK)	t_{PWL}	0.336	0.337
Pulse Width High (CK)	t_{PWH}	0.254	0.266

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FDS3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.090	0.040 + 0.025*SL	0.035 + 0.026*SL	0.031 + 0.027*SL
	t_F	0.069	0.036 + 0.016*SL	0.033 + 0.017*SL	0.024 + 0.018*SL
	t_{PLH}	0.352	0.326 + 0.013*SL	0.328 + 0.012*SL	0.329 + 0.012*SL
	t_{PHL}	0.351	0.329 + 0.011*SL	0.335 + 0.010*SL	0.338 + 0.010*SL
CK to QN	t_R	0.094	0.044 + 0.025*SL	0.039 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.071	0.037 + 0.017*SL	0.037 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.297	0.270 + 0.013*SL	0.274 + 0.013*SL	0.276 + 0.012*SL
	t_{PHL}	0.294	0.270 + 0.012*SL	0.278 + 0.010*SL	0.283 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FDS3D2_LP

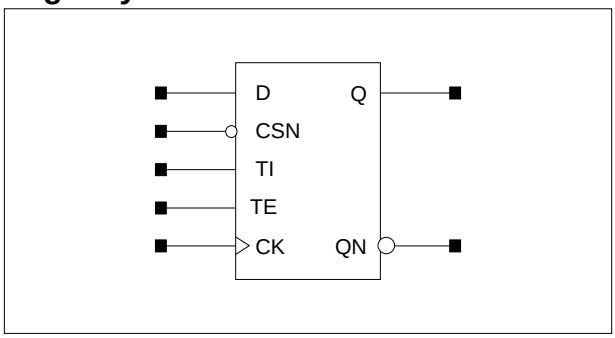
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.064	0.041 + 0.012*SL	0.037 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.052	0.034 + 0.009*SL	0.036 + 0.008*SL	0.029 + 0.009*SL
	t_{PLH}	0.383	0.368 + 0.007*SL	0.372 + 0.006*SL	0.374 + 0.006*SL
	t_{PHL}	0.379	0.366 + 0.007*SL	0.372 + 0.005*SL	0.380 + 0.005*SL
CK to QN	t_R	0.070	0.046 + 0.012*SL	0.042 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.058	0.041 + 0.008*SL	0.041 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.305	0.289 + 0.008*SL	0.295 + 0.007*SL	0.300 + 0.006*SL
	t_{PHL}	0.305	0.290 + 0.008*SL	0.299 + 0.006*SL	0.311 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FDS3S_LP/FDS3SD2_LP

Flip-Flop with Synchronous Set, Scan, 1X/2X Drive

Logic Symbol



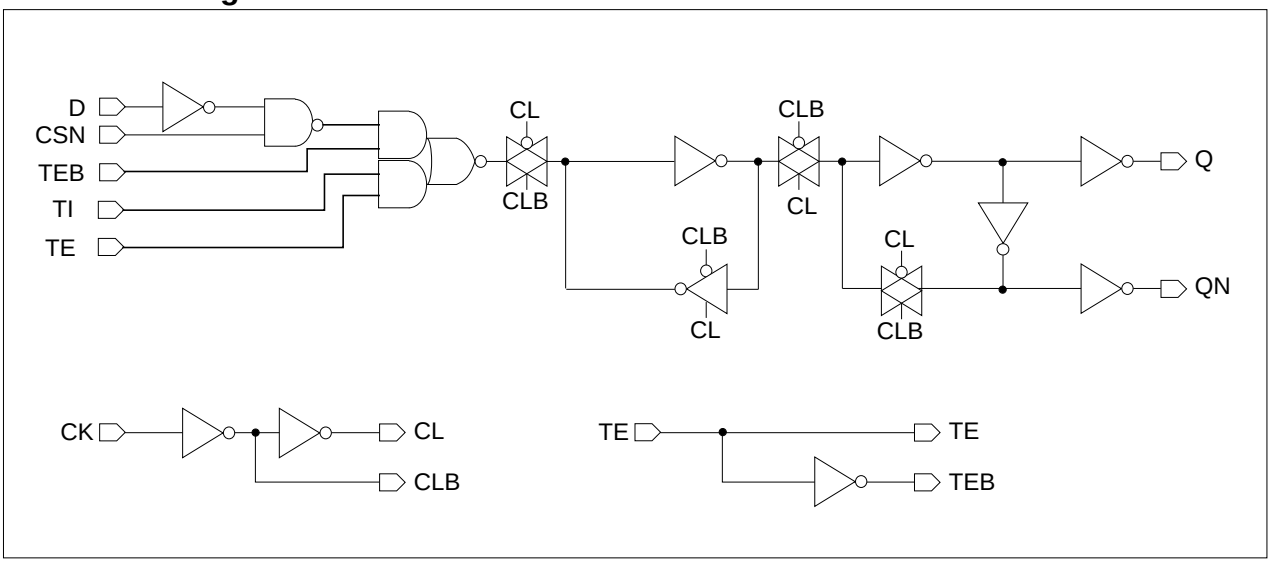
Truth Table

D	CSN	TI	TE	CK	Q(n+1)	QN(n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	0	x	0	↑	1	0
x	x	x	x	↓	Q(n)	QN(n+1)

Cell Data

Input Load (SL)										Gate Count	
FDS3S_LP					*FDS3SD2_LP*					*FDS3S_LP*	*FDS3SD2_LP*
D	CSN	CK	TI	TE	D	CSN	CK	TI	TE		
0.9	0.7	1.2	0.7	1.6	0.9	0.7	1.2	0.7	1.6	8.33	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FDS3S_LP	FDS3SD2_LP
Input Setup Time (D to CK)	t_{SU}	0.467	0.467
Input Hold Time (D to CK)	t_{HD}	0.000	0.000
Input Setup Time (CSN to CK)	t_{SU}	0.406	0.407
Input Hold Time (CSN to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.364	0.367
Pulse Width High (CK)	t_{PWH}	0.255	0.266
Input Setup Time (TI to CK)	t_{SU}	0.392	0.391
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.377	0.377
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FDS3S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.094	0.044 + 0.025*SL	0.038 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.070	0.037 + 0.017*SL	0.035 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.299	0.272 + 0.013*SL	0.276 + 0.013*SL	0.278 + 0.012*SL
	t_{PHL}	0.296	0.273 + 0.012*SL	0.281 + 0.010*SL	0.285 + 0.010*SL
CK to QN	t_R	0.091	0.041 + 0.025*SL	0.035 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.069	0.037 + 0.016*SL	0.034 + 0.017*SL	0.025 + 0.018*SL
	t_{PLH}	0.355	0.328 + 0.013*SL	0.331 + 0.012*SL	0.332 + 0.012*SL
	t_{PHL}	0.354	0.331 + 0.011*SL	0.337 + 0.010*SL	0.340 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FDS3SD2_LP

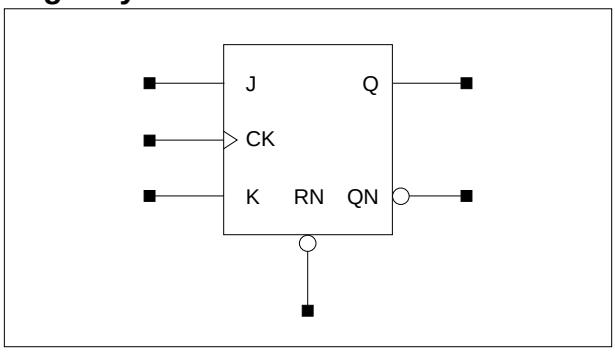
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.070	0.046 + 0.012*SL	0.043 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.058	0.041 + 0.009*SL	0.041 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.305	0.289 + 0.008*SL	0.295 + 0.007*SL	0.300 + 0.006*SL
	t_{PHL}	0.306	0.291 + 0.008*SL	0.299 + 0.006*SL	0.311 + 0.005*SL
CK to QN	t_R	0.064	0.041 + 0.012*SL	0.037 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.053	0.035 + 0.009*SL	0.038 + 0.008*SL	0.030 + 0.009*SL
	t_{PLH}	0.383	0.368 + 0.007*SL	0.372 + 0.006*SL	0.375 + 0.006*SL
	t_{PHL}	0.380	0.366 + 0.007*SL	0.372 + 0.005*SL	0.380 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FJ2_LP/FJ2D2_LP

JK Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



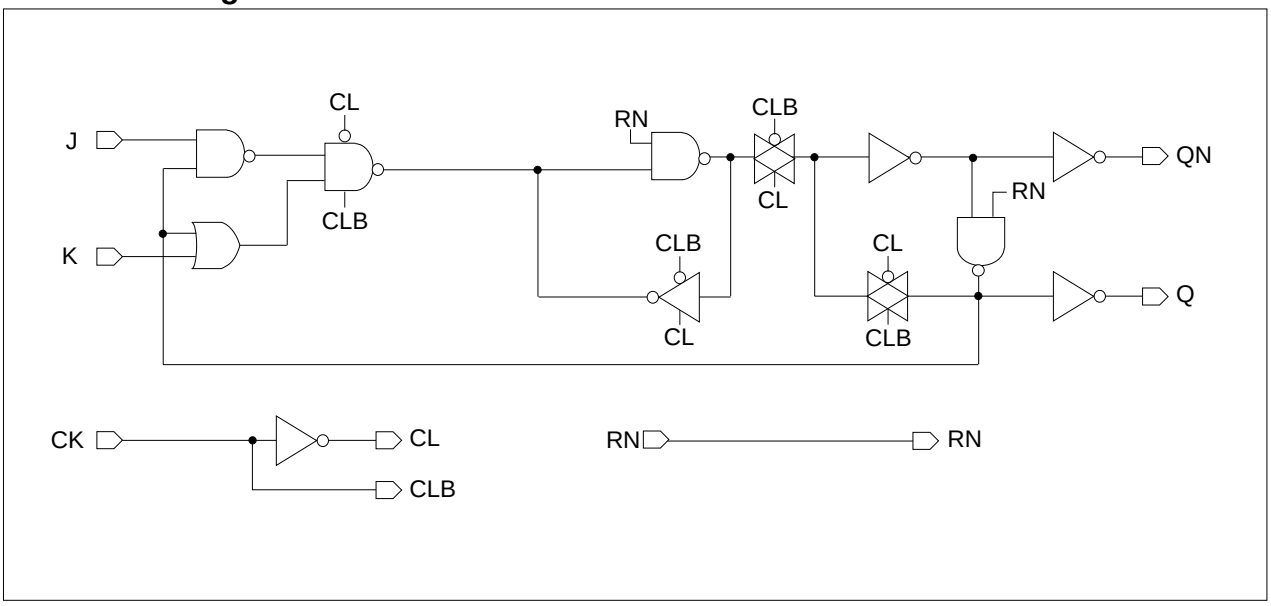
Truth Table

J	CK	K	RN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	0	1	1	0
0	↑	0	1	Q (n)	QN (n)
1	↑	1	1	QN (n)	Q (n)
x	↓	x	1	Q (n)	QN (n)
x	x	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
FJ2_LP				*FJ2D2_LP*				*FJ2_LP*	*FJ2D2_LP*
J	K	CK	RN	J	K	CK	RN		
0.7	0.7	1.2	2.0	0.6	0.7	1.2	2.2	8.33	8.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ2_LP	FJ2D2_LP
Input Setup Time (J to CK)	t_{SU}	0.364	0.363
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.364	0.363
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.379	0.379
Pulse Width High (CK)	t_{PWH}	0.264	0.275
Pulse Width Low (RN)	t_{PWL}	0.393	0.417
Recovery Time (RN to CK)	t_{RC}	0.015	0.016
Removal Time (RN to CK)	t_{RM}	0.268	0.267

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FJ2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.115	0.065 + 0.025*SL	0.063 + 0.025*SL	0.047 + 0.026*SL
	t_F	0.082	0.048 + 0.017*SL	0.048 + 0.017*SL	0.038 + 0.017*SL
	t_{PLH}	0.454	0.422 + 0.016*SL	0.434 + 0.013*SL	0.442 + 0.012*SL
	t_{PHL}	0.404	0.378 + 0.013*SL	0.390 + 0.010*SL	0.400 + 0.010*SL
RN to Q	t_F	0.093	0.057 + 0.018*SL	0.061 + 0.017*SL	0.060 + 0.017*SL
	t_{PHL}	0.234	0.205 + 0.015*SL	0.219 + 0.011*SL	0.238 + 0.010*SL
CK to QN	t_R	0.093	0.044 + 0.025*SL	0.038 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.072	0.040 + 0.016*SL	0.036 + 0.017*SL	0.030 + 0.018*SL
	t_{PLH}	0.303	0.276 + 0.013*SL	0.279 + 0.013*SL	0.282 + 0.012*SL
	t_{PHL}	0.316	0.292 + 0.012*SL	0.300 + 0.010*SL	0.305 + 0.010*SL
RN to QN	t_R	0.110	0.065 + 0.023*SL	0.053 + 0.026*SL	0.036 + 0.027*SL
	t_{PLH}	0.513	0.485 + 0.014*SL	0.492 + 0.012*SL	0.494 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FJ2D2_LP

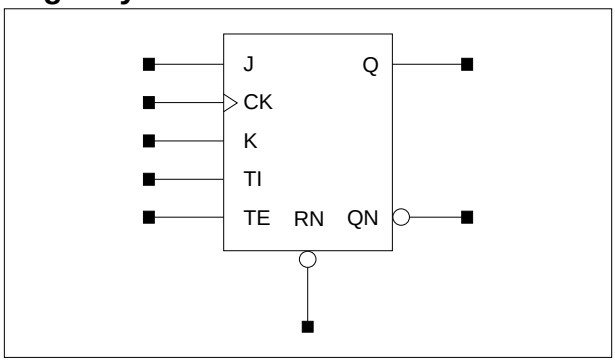
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.084	0.057 + 0.013*SL	0.061 + 0.012*SL	0.052 + 0.013*SL
	t_F	0.063	0.043 + 0.010*SL	0.050 + 0.008*SL	0.046 + 0.008*SL
	t_{PLH}	0.465	0.446 + 0.010*SL	0.457 + 0.007*SL	0.471 + 0.006*SL
	t_{PHL}	0.420	0.404 + 0.008*SL	0.414 + 0.006*SL	0.430 + 0.005*SL
RN to Q	t_F	0.073	0.053 + 0.010*SL	0.058 + 0.009*SL	0.058 + 0.009*SL
	t_{PHL}	0.222	0.203 + 0.009*SL	0.215 + 0.006*SL	0.234 + 0.005*SL
CK to QN	t_R	0.070	0.046 + 0.012*SL	0.043 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.059	0.041 + 0.009*SL	0.044 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.305	0.289 + 0.008*SL	0.295 + 0.006*SL	0.299 + 0.006*SL
	t_{PHL}	0.322	0.307 + 0.008*SL	0.315 + 0.006*SL	0.326 + 0.005*SL
RN to QN	t_R	0.087	0.062 + 0.012*SL	0.064 + 0.012*SL	0.045 + 0.013*SL
	t_{PLH}	0.535	0.516 + 0.009*SL	0.528 + 0.007*SL	0.535 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FJ2S_LP/FJ2SD2_LP

JK Flip-Flop with Reset, Scan, 1X/2X Drive

Logic Symbol



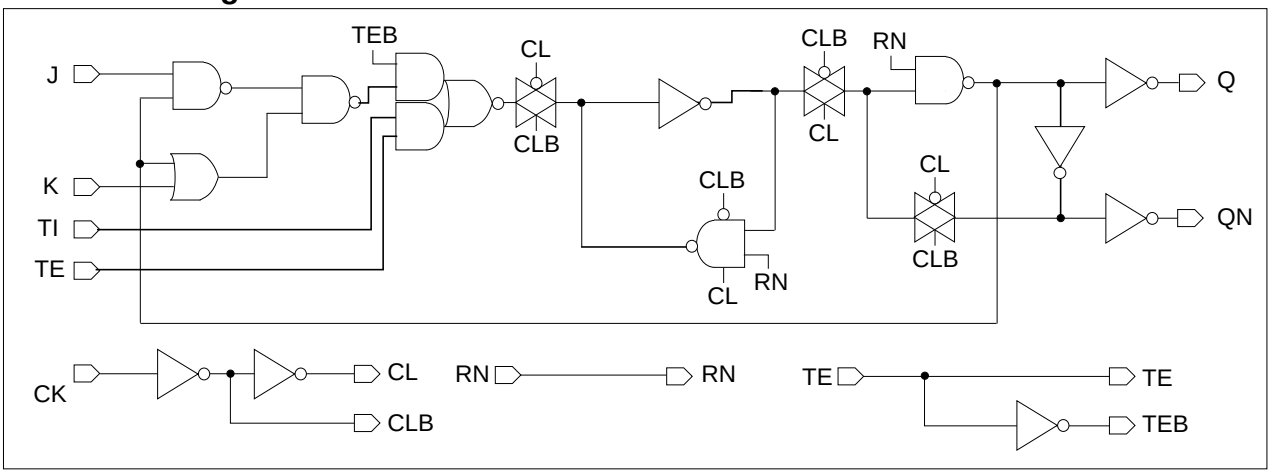
Truth Table

J	CK	K	TI	TE	RN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	0	1
1	↑	0	x	0	1	1	0
0	↑	0	x	0	1	Q (n)	QN (n)
1	↑	1	x	0	1	QN (n)	Q (n)
x	↓	x	x	x	1	Q (n)	QN (n)
x	x	x	x	x	0	0	1
x	↑	x	0	1	1	0	1
x	↑	x	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
FJ2S_LP						*FJ2SD2_LP*						*FJ2S_LP*	*FJ2SD2_LP*
J	K	CK	RN	TI	TE	J	K	CK	RN	TI	TE		
0.7	0.9	1.1	1.5	0.7	1.6	0.7	0.9	1.2	1.5	0.7	1.7	10.00	10.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ2S_LP	FJ2SD2_LP
Input Setup Time (J to CK)	t_{SU}	0.515	0.511
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.515	0.511
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.366	0.368
Pulse Width High (CK)	t_{PWH}	0.275	0.294
Pulse Width Low (RN)	t_{PWL}	0.309	0.347
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.783	0.788
Input Setup Time (TI to CK)	t_{SU}	0.398	0.392
Input Hold Time (TI to CK)	t_{HD}	0.003	0.003
Input Setup Time (TE to CK)	t_{SU}	0.382	0.379
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FJ2S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.115	0.065 + 0.025*SL	0.063 + 0.025*SL	0.048 + 0.026*SL
	t_F	0.082	0.047 + 0.018*SL	0.050 + 0.017*SL	0.040 + 0.017*SL
	t_{PLH}	0.366	0.333 + 0.016*SL	0.347 + 0.013*SL	0.357 + 0.012*SL
	t_{PHL}	0.339	0.312 + 0.014*SL	0.325 + 0.010*SL	0.338 + 0.010*SL
RN to Q	t_F	0.087	0.053 + 0.017*SL	0.055 + 0.017*SL	0.044 + 0.017*SL
	t_{PHL}	0.217	0.189 + 0.014*SL	0.203 + 0.010*SL	0.217 + 0.010*SL
CK to QN	t_R	0.094	0.044 + 0.025*SL	0.040 + 0.026*SL	0.034 + 0.027*SL
	t_F	0.072	0.039 + 0.017*SL	0.037 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.402	0.375 + 0.013*SL	0.378 + 0.012*SL	0.379 + 0.012*SL
	t_{PHL}	0.425	0.403 + 0.011*SL	0.409 + 0.010*SL	0.412 + 0.010*SL
RN to QN	t_R	0.106	0.052 + 0.027*SL	0.056 + 0.026*SL	0.056 + 0.026*SL
	t_{PLH}	0.297	0.267 + 0.015*SL	0.274 + 0.013*SL	0.291 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FJ2SD2_LP

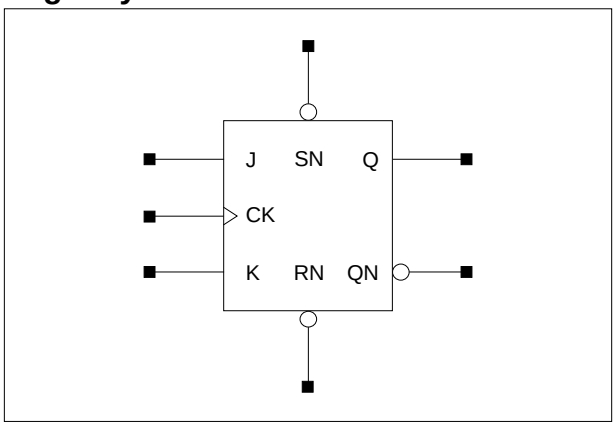
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.093	0.066 + 0.014*SL	0.070 + 0.013*SL	0.065 + 0.013*SL
	t_F	0.070	0.050 + 0.010*SL	0.055 + 0.009*SL	0.058 + 0.008*SL
	t_{PLH}	0.375	0.354 + 0.011*SL	0.366 + 0.007*SL	0.385 + 0.006*SL
	t_{PHL}	0.348	0.330 + 0.009*SL	0.341 + 0.006*SL	0.362 + 0.005*SL
RN to Q	t_F	0.074	0.055 + 0.010*SL	0.060 + 0.008*SL	0.063 + 0.008*SL
	t_{PHL}	0.225	0.206 + 0.009*SL	0.218 + 0.006*SL	0.240 + 0.005*SL
CK to QN	t_R	0.066	0.042 + 0.012*SL	0.039 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.056	0.038 + 0.009*SL	0.040 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.432	0.417 + 0.008*SL	0.422 + 0.006*SL	0.425 + 0.006*SL
	t_{PHL}	0.460	0.446 + 0.007*SL	0.453 + 0.005*SL	0.462 + 0.005*SL
RN to QN	t_R	0.074	0.049 + 0.013*SL	0.046 + 0.013*SL	0.048 + 0.013*SL
	t_{PLH}	0.324	0.307 + 0.009*SL	0.312 + 0.007*SL	0.324 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FJ4_LP/FJ4D2_LP

JK Flip-Flop with Reset, Set, 1X/2X Drive

Logic Symbol5



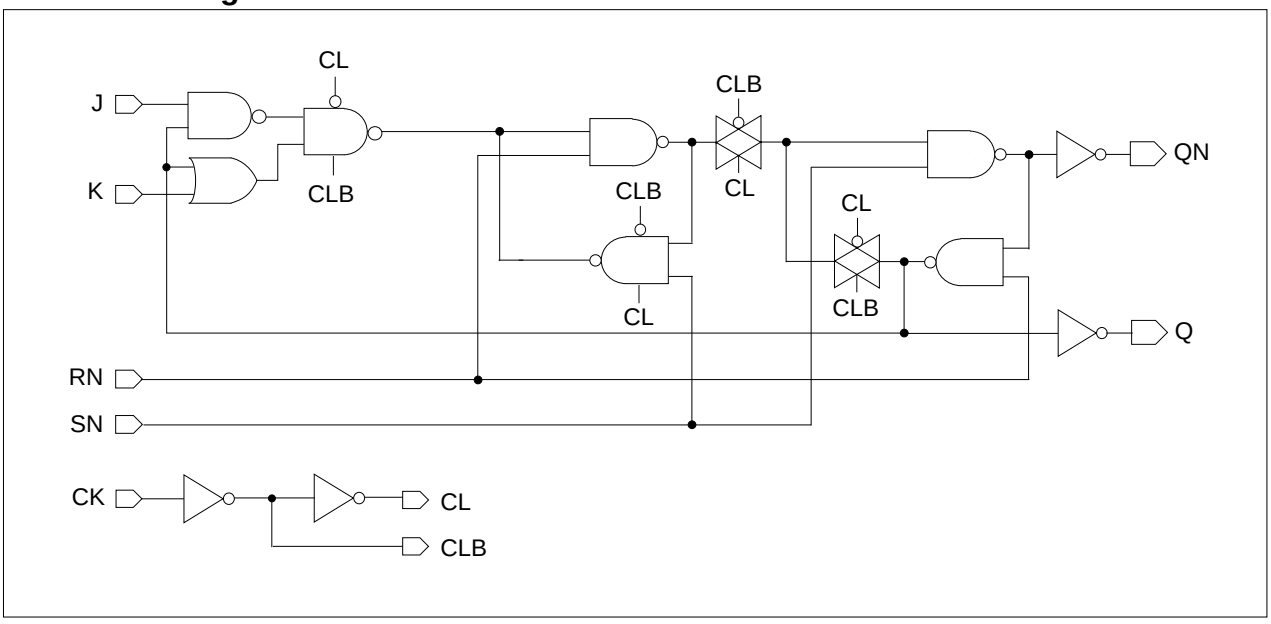
Truth Table

J	CK	K	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	1	0	1
1	↑	0	1	1	1	0
0	↑	0	1	1	Q (n)	QN (n)
1	↑	1	1	1	QN (n)	Q (n)
x	↓	x	1	1	Q (n)	QN (n)
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

Cell Data

Input Load (SL)										Gate Count	
FJ4_LP					*FJ4D2_LP*					*FJ4_LP*	*FJ4D2_LP*
J	K	CK	RN	SN	J	K	CK	RN	SN		
0.6	0.7	1.2	2.1	1.5	0.7	0.7	1.2	2.2	1.5	9.00	9.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ4_LP	FJ4D2_LP
Input Setup Time (J to CK)	t_{SU}	0.366	0.365
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.366	0.365
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.386	0.386
Pulse Width High (CK)	t_{PWH}	0.270	0.287
Pulse Width Low (RN)	t_{PWL}	0.397	0.427
Pulse Width Low (SN)	t_{PWL}	0.346	0.365
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.312	0.304
Recovery Time (SN to CK)	t_{RC}	0.000	0.000
Removal Time (SN to CK)	t_{RM}	0.855	0.846
Recovery Time (SN to RN)	t_{RC}	0.192	0.188
Removal Time (SN to RN)	t_{RM}	0.088	0.092

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FJ4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.116	0.066 + 0.025*SL	0.063 + 0.025*SL	0.048 + 0.026*SL
	t_F	0.084	0.050 + 0.017*SL	0.050 + 0.017*SL	0.039 + 0.017*SL
	t_{PLH}	0.468	0.436 + 0.016*SL	0.449 + 0.013*SL	0.457 + 0.012*SL
	t_{PHL}	0.436	0.410 + 0.013*SL	0.422 + 0.010*SL	0.432 + 0.010*SL
RN to Q	t_R	0.130	0.073 + 0.029*SL	0.083 + 0.026*SL	0.083 + 0.026*SL
	t_F	0.092	0.054 + 0.019*SL	0.060 + 0.017*SL	0.060 + 0.017*SL
	t_{PLH}	0.228	0.191 + 0.018*SL	0.207 + 0.014*SL	0.240 + 0.013*SL
	t_{PHL}	0.233	0.204 + 0.014*SL	0.218 + 0.011*SL	0.235 + 0.010*SL
SN to Q	t_R	0.131	0.074 + 0.029*SL	0.085 + 0.026*SL	0.085 + 0.026*SL
	t_{PLH}	0.347	0.310 + 0.019*SL	0.326 + 0.015*SL	0.361 + 0.013*SL
CK to QN	t_R	0.105	0.055 + 0.025*SL	0.052 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.078	0.045 + 0.016*SL	0.042 + 0.017*SL	0.034 + 0.018*SL
	t_{PLH}	0.332	0.303 + 0.014*SL	0.310 + 0.013*SL	0.316 + 0.012*SL
	t_{PHL}	0.328	0.303 + 0.012*SL	0.312 + 0.010*SL	0.319 + 0.010*SL
RN to QN	t_R	0.118	0.071 + 0.023*SL	0.064 + 0.025*SL	0.045 + 0.026*SL
	t_{PLH}	0.536	0.505 + 0.015*SL	0.516 + 0.013*SL	0.521 + 0.012*SL
SN to QN	t_R	0.104	0.055 + 0.024*SL	0.050 + 0.026*SL	0.039 + 0.026*SL
	t_F	0.078	0.046 + 0.016*SL	0.041 + 0.017*SL	0.036 + 0.018*SL
	t_{PLH}	0.170	0.142 + 0.014*SL	0.149 + 0.012*SL	0.152 + 0.012*SL
	t_{PHL}	0.183	0.159 + 0.012*SL	0.167 + 0.010*SL	0.173 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

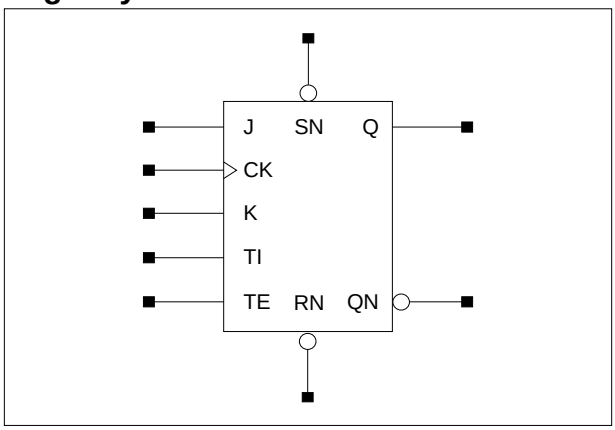
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FJ4D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.085	0.060 + 0.013*SL	0.061 + 0.012*SL	0.053 + 0.013*SL
	t_F	0.065	0.045 + 0.010*SL	0.052 + 0.008*SL	0.050 + 0.008*SL
	t_{PLH}	0.484	0.464 + 0.010*SL	0.476 + 0.007*SL	0.491 + 0.006*SL
	t_{PHL}	0.467	0.450 + 0.009*SL	0.460 + 0.006*SL	0.477 + 0.005*SL
RN to Q	t_R	0.092	0.064 + 0.014*SL	0.066 + 0.013*SL	0.077 + 0.013*SL
	t_F	0.072	0.052 + 0.010*SL	0.058 + 0.009*SL	0.058 + 0.009*SL
	t_{PLH}	0.205	0.183 + 0.011*SL	0.194 + 0.008*SL	0.219 + 0.007*SL
	t_{PHL}	0.223	0.204 + 0.009*SL	0.216 + 0.006*SL	0.236 + 0.005*SL
SN to Q	t_R	0.093	0.063 + 0.015*SL	0.070 + 0.013*SL	0.078 + 0.013*SL
	t_{PLH}	0.355	0.333 + 0.011*SL	0.344 + 0.008*SL	0.369 + 0.007*SL
CK to QN	t_R	0.083	0.059 + 0.012*SL	0.056 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.062	0.044 + 0.009*SL	0.047 + 0.008*SL	0.043 + 0.008*SL
	t_{PLH}	0.339	0.320 + 0.009*SL	0.330 + 0.007*SL	0.341 + 0.006*SL
	t_{PHL}	0.335	0.319 + 0.008*SL	0.328 + 0.006*SL	0.343 + 0.005*SL
RN to QN	t_R	0.096	0.072 + 0.012*SL	0.070 + 0.012*SL	0.058 + 0.013*SL
	t_{PLH}	0.567	0.547 + 0.010*SL	0.559 + 0.007*SL	0.574 + 0.006*SL
SN to QN	t_R	0.083	0.058 + 0.012*SL	0.059 + 0.012*SL	0.047 + 0.013*SL
	t_F	0.062	0.046 + 0.008*SL	0.046 + 0.008*SL	0.042 + 0.009*SL
	t_{PLH}	0.177	0.158 + 0.009*SL	0.168 + 0.007*SL	0.178 + 0.006*SL
	t_{PHL}	0.189	0.173 + 0.008*SL	0.182 + 0.006*SL	0.195 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



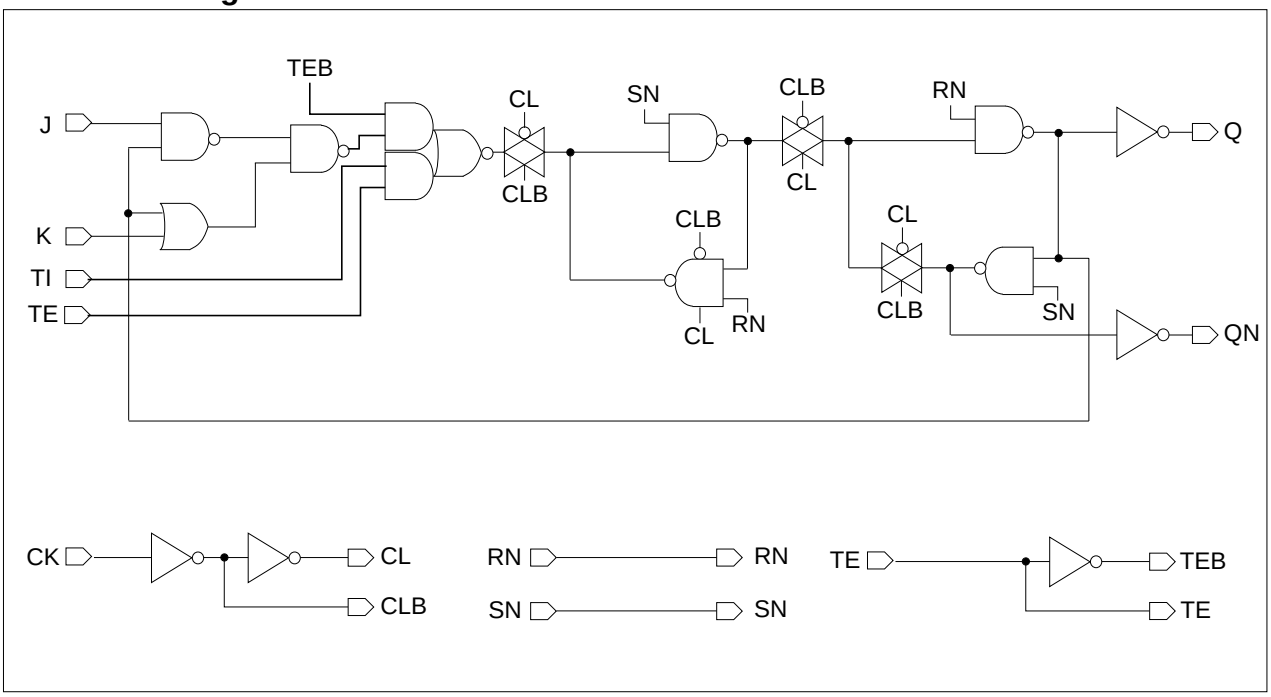
Truth Table

J	CK	K	TI	TE	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	1	0	1
1	↑	0	x	0	1	1	1	0
0	↑	0	x	0	1	1	Q (n)	QN (n)
1	↑	1	x	0	1	1	QN (n)	Q (n)
x	↓	x	x	x	1	1	Q (n)	QN (n)
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0
x	↑	x	0	1	1	1	0	1
x	↑	x	1	1	1	1	1	0

Cell Data

Input Load (SL)														Gate Count	
FJ4S_LP							*FJ4SD2_LP*							*FJ4S_LP*	*FJ4SD2_LP*
J	K	CK	RN	SN	TI	TE	J	K	CK	RN	SN	TI	TE		
0.7	0.9	1.2	1.6	2.1	0.7	1.6	0.7	0.9	1.2	1.5	2.2	0.7	1.6	11.00	11.67

Schematic Diagram



FJ4S_LP/FJ4SD2_LP

JK Flip-Flop with Reset, Set, Scan, 1X/2X Drive

Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FJ4S_LP	FJ4SD2_LP
Input Setup Time (J to CK)	t_{SU}	0.511	0.515
Input Hold Time (J to CK)	t_{HD}	0.000	0.000
Input Setup Time (K to CK)	t_{SU}	0.511	0.515
Input Hold Time (K to CK)	t_{HD}	0.000	0.000
Pulse Width Low (CK)	t_{PWL}	0.391	0.391
Pulse Width High (CK)	t_{PWH}	0.279	0.298
Pulse Width Low (RN)	t_{PWL}	0.343	0.373
Pulse Width Low (SN)	t_{PWL}	0.401	0.430
Recovery Time (RN to CK)	t_{RC}	0.000	0.000
Removal Time (RN to CK)	t_{RM}	0.829	0.827
Recovery Time (SN to CK)	t_{RC}	0.000	0.000
Removal Time (SN to CK)	t_{RM}	0.296	0.296
Input Setup Time (TI to CK)	t_{SU}	0.415	0.415
Input Hold Time (TI to CK)	t_{HD}	0.000	0.000
Input Setup Time (TE to CK)	t_{SU}	0.402	0.402
Input Hold Time (TE to CK)	t_{HD}	0.000	0.000
Recovery Time (SN to RN)	t_{RC}	0.098	0.100
Removal Time (SN to RN)	t_{RM}	0.182	0.180

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FJ4S_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.115	0.065 + 0.025*SL	0.064 + 0.025*SL	0.049 + 0.026*SL
	t_F	0.084	0.048 + 0.018*SL	0.052 + 0.017*SL	0.042 + 0.017*SL
	t_{PLH}	0.368	0.336 + 0.016*SL	0.349 + 0.013*SL	0.360 + 0.012*SL
	t_{PHL}	0.359	0.331 + 0.014*SL	0.345 + 0.010*SL	0.358 + 0.010*SL
RN to Q	t_R	0.112	0.064 + 0.024*SL	0.059 + 0.025*SL	0.043 + 0.026*SL
	t_F	0.085	0.051 + 0.017*SL	0.053 + 0.017*SL	0.045 + 0.017*SL
	t_{PLH}	0.205	0.174 + 0.016*SL	0.186 + 0.013*SL	0.192 + 0.012*SL
	t_{PHL}	0.217	0.189 + 0.014*SL	0.203 + 0.010*SL	0.216 + 0.010*SL
SN to Q	t_R	0.124	0.077 + 0.023*SL	0.072 + 0.025*SL	0.050 + 0.026*SL
	t_{PLH}	0.544	0.511 + 0.017*SL	0.526 + 0.013*SL	0.534 + 0.012*SL
CK to QN	t_R	0.101	0.053 + 0.024*SL	0.046 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.074	0.041 + 0.016*SL	0.039 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.462	0.433 + 0.014*SL	0.441 + 0.013*SL	0.444 + 0.012*SL
	t_{PHL}	0.443	0.419 + 0.012*SL	0.428 + 0.010*SL	0.433 + 0.010*SL
RN to QN	t_R	0.119	0.062 + 0.029*SL	0.072 + 0.026*SL	0.075 + 0.026*SL
	t_{PLH}	0.347	0.311 + 0.018*SL	0.325 + 0.014*SL	0.357 + 0.013*SL
SN to QN	t_R	0.117	0.060 + 0.029*SL	0.070 + 0.026*SL	0.073 + 0.026*SL
	t_F	0.079	0.042 + 0.018*SL	0.045 + 0.018*SL	0.048 + 0.018*SL
	t_{PLH}	0.188	0.153 + 0.017*SL	0.166 + 0.014*SL	0.197 + 0.012*SL
	t_{PHL}	0.196	0.170 + 0.013*SL	0.180 + 0.011*SL	0.190 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FJ4SD2_LP

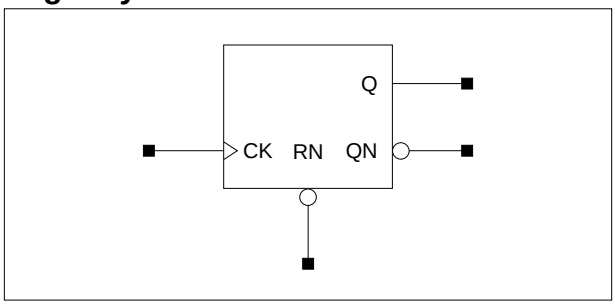
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.091	0.066 + 0.013*SL	0.067 + 0.013*SL	0.062 + 0.013*SL
	t_F	0.069	0.048 + 0.011*SL	0.056 + 0.008*SL	0.056 + 0.008*SL
	t_{PLH}	0.371	0.350 + 0.011*SL	0.362 + 0.007*SL	0.380 + 0.006*SL
	t_{PHL}	0.363	0.345 + 0.009*SL	0.356 + 0.006*SL	0.375 + 0.005*SL
RN to Q	t_R	0.090	0.064 + 0.013*SL	0.065 + 0.012*SL	0.056 + 0.013*SL
	t_F	0.071	0.052 + 0.010*SL	0.057 + 0.008*SL	0.056 + 0.008*SL
	t_{PLH}	0.207	0.187 + 0.010*SL	0.199 + 0.007*SL	0.215 + 0.006*SL
	t_{PHL}	0.218	0.200 + 0.009*SL	0.212 + 0.006*SL	0.232 + 0.005*SL
SN to Q	t_R	0.100	0.073 + 0.013*SL	0.078 + 0.012*SL	0.067 + 0.013*SL
	t_{PLH}	0.573	0.551 + 0.011*SL	0.566 + 0.007*SL	0.585 + 0.006*SL
CK to QN	t_R	0.079	0.054 + 0.012*SL	0.055 + 0.012*SL	0.043 + 0.013*SL
	t_F	0.060	0.041 + 0.010*SL	0.047 + 0.008*SL	0.042 + 0.008*SL
	t_{PLH}	0.489	0.471 + 0.009*SL	0.480 + 0.007*SL	0.488 + 0.006*SL
	t_{PHL}	0.480	0.464 + 0.008*SL	0.473 + 0.006*SL	0.486 + 0.005*SL
RN to QN	t_R	0.087	0.057 + 0.015*SL	0.064 + 0.013*SL	0.071 + 0.013*SL
	t_{PLH}	0.364	0.344 + 0.010*SL	0.353 + 0.008*SL	0.375 + 0.007*SL
SN to QN	t_R	0.086	0.058 + 0.014*SL	0.061 + 0.013*SL	0.069 + 0.013*SL
	t_F	0.064	0.047 + 0.009*SL	0.048 + 0.009*SL	0.045 + 0.009*SL
	t_{PLH}	0.178	0.158 + 0.010*SL	0.167 + 0.008*SL	0.188 + 0.007*SL
	t_{PHL}	0.196	0.179 + 0.008*SL	0.189 + 0.006*SL	0.202 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

FT2_LP/FT2D2_LP

Toggle Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



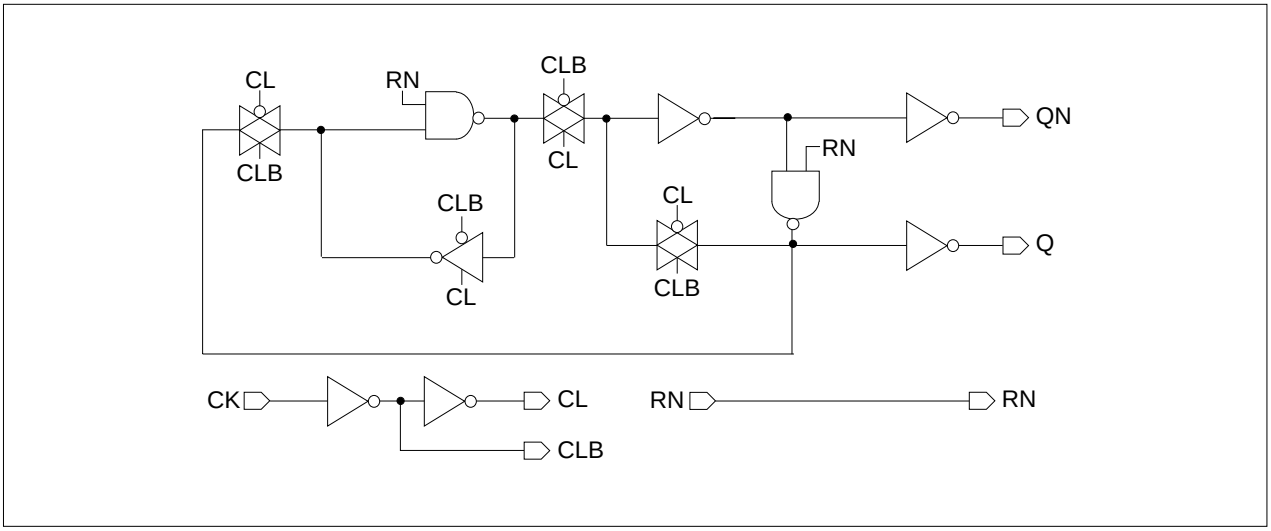
Truth Table

CK	RN	Q (n+1)	QN (n+1)
↑	1	QN (n)	Q (n)
↓	1	Q (n)	QN (n)
x	0	0	1

Cell Data

Input Load (SL)				Gate Count	
FT2_LP		*FT2D2_LP*		*FT2_LP*	*FT2D2_LP*
CK	RN	CK	RN		
1.1	2.1	1.2	2.1	6.67	6.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		FT2_LP	FT2D2_LP
Pulse Width Low (CK)	t_{PWL}	0.266	0.262
Pulse Width High (CK)	t_{PWH}	0.262	0.256
Pulse Width Low (RN)	t_{PWL}	0.406	0.433
Recovery Time (RN to CK)	t_{RC}	0.024	0.024
Removal Time (RN to CK)	t_{RM}	0.261	0.260

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FT2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.110	0.061 + 0.024*SL	0.056 + 0.026*SL	0.043 + 0.026*SL
	t_F	0.080	0.046 + 0.017*SL	0.046 + 0.017*SL	0.035 + 0.017*SL
	t_{PLH}	0.431	0.402 + 0.015*SL	0.410 + 0.013*SL	0.414 + 0.012*SL
	t_{PHL}	0.387	0.362 + 0.012*SL	0.372 + 0.010*SL	0.379 + 0.010*SL
RN to Q	t_F	0.082	0.049 + 0.017*SL	0.047 + 0.017*SL	0.038 + 0.017*SL
	t_{PHL}	0.193	0.168 + 0.013*SL	0.178 + 0.010*SL	0.188 + 0.010*SL
CK to QN	t_R	0.095	0.045 + 0.025*SL	0.040 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.072	0.039 + 0.017*SL	0.037 + 0.017*SL	0.030 + 0.018*SL
	t_{PLH}	0.299	0.273 + 0.013*SL	0.276 + 0.013*SL	0.279 + 0.012*SL
	t_{PHL}	0.310	0.287 + 0.012*SL	0.294 + 0.010*SL	0.301 + 0.010*SL
RN to QN	t_R	0.095	0.046 + 0.025*SL	0.040 + 0.026*SL	0.032 + 0.027*SL
	t_{PLH}	0.316	0.289 + 0.013*SL	0.293 + 0.012*SL	0.294 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

FT2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_R	0.078	0.052 + 0.013*SL	0.055 + 0.012*SL	0.044 + 0.013*SL
	t_F	0.061	0.041 + 0.010*SL	0.047 + 0.008*SL	0.042 + 0.009*SL
	t_{PLH}	0.444	0.426 + 0.009*SL	0.436 + 0.007*SL	0.445 + 0.006*SL
	t_{PHL}	0.407	0.391 + 0.008*SL	0.400 + 0.006*SL	0.414 + 0.005*SL
RN to Q	t_F	0.062	0.044 + 0.009*SL	0.047 + 0.008*SL	0.046 + 0.008*SL
	t_{PHL}	0.188	0.172 + 0.008*SL	0.181 + 0.006*SL	0.197 + 0.005*SL
CK to QN	t_R	0.070	0.048 + 0.011*SL	0.042 + 0.013*SL	0.034 + 0.013*SL
	t_F	0.059	0.041 + 0.009*SL	0.045 + 0.008*SL	0.039 + 0.009*SL
	t_{PLH}	0.303	0.287 + 0.008*SL	0.293 + 0.006*SL	0.297 + 0.006*SL
	t_{PHL}	0.317	0.302 + 0.008*SL	0.310 + 0.006*SL	0.321 + 0.005*SL
RN to QN	t_R	0.071	0.049 + 0.011*SL	0.044 + 0.013*SL	0.033 + 0.013*SL
	t_{PLH}	0.320	0.304 + 0.008*SL	0.310 + 0.006*SL	0.315 + 0.006*SL

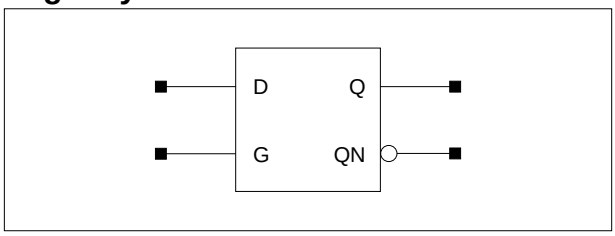
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LATCHES

Cell List

Cell Name	Function Description
LD1_LP	D Latch with Active High, 1X Drive
LD1D2_LP	D Latch with Active High, 2X Drive
LD1Q_LP	D Latch with Active High, Q Output Only, 1X Drive
LD1QD2_LP	D Latch with Active High, Q Output Only, 2X Drive
LD2_LP	D Latch with Active High, Reset, 1X Drive
LD2D2_LP	D Latch with Active High, Reset, 2X Drive
LD2Q_LP	D Latch with Active High, Reset, Q Output Only, 1X Drive
LD2QD2_LP	D Latch with Active High, Reset, Q Output Only, 2X Drive
LD3_LP	D Latch with Active High, Set, 1X Drive
LD3D2_LP	D Latch with Active High, Set, 2X Drive
LD4_LP	D Latch with Active High, Reset, Set, 1X Drive
LD4D2_LP	D Latch with Active High, Reset, Set, 2X Drive
LD5_LP	D Latch with Active Low, 1X Drive
LD5D2_LP	D Latch with Active Low, 2X Drive
LD5Q_LP	D Latch with Active Low, Q Output Only, 1X Drive
LD5QD2_LP	D Latch with Active Low, Q Output Only, 2X Drive
LD6_LP	D Latch with Active Low, Reset, 1X Drive
LD6D2_LP	D Latch with Active Low, Reset, 2X Drive
LD6Q_LP	D Latch with Active Low, Reset, Q Output Only, 1X Drive
LD6QD2_LP	D Latch with Active Low, Reset, Q Output Only, 2X Drive

Logic Symbol



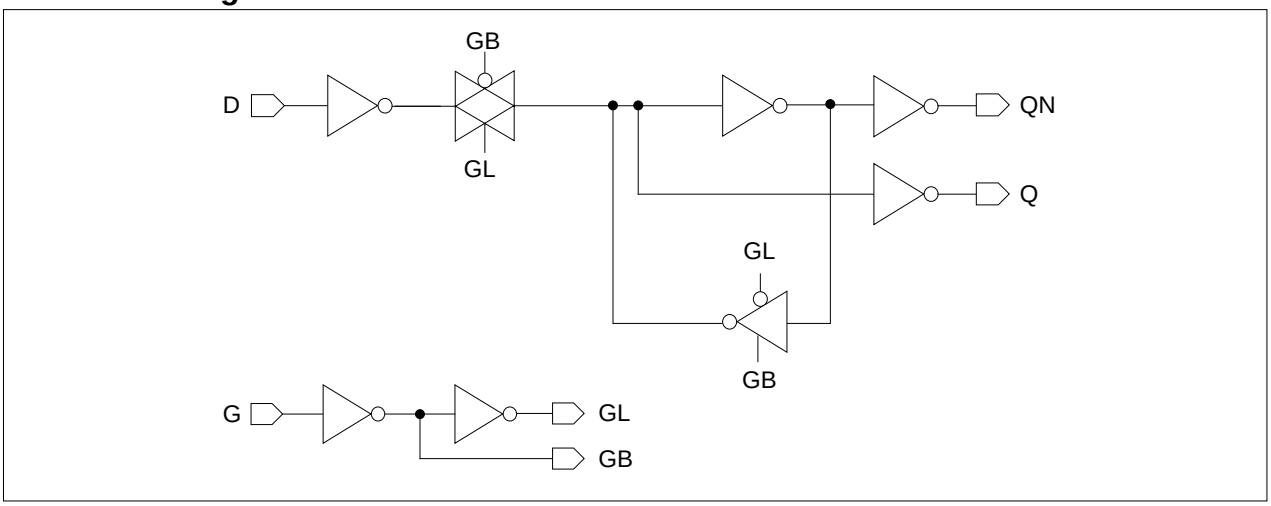
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
LD1_LP		*LD1D2_LP*		*LD1_LP*	*LD1D2_LP*
D	G	D	G		
1.1	1.2	1.2	1.2	4.33	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD1_LP	LD1D2_LP
Input Setup Time (D to G)	t_{SU}	0.249	0.291
Input Hold Time (D to G)	t_{HD}	0.129	0.099
Pulse Width High (G)	t_{PWH}	0.267	0.313

LD1_LP/LD1D2_LP

D Latch with Active High, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD1_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.106	0.057 + 0.025*SL	0.054 + 0.025*SL	0.043 + 0.026*SL
	t_F	0.097	0.061 + 0.018*SL	0.068 + 0.017*SL	0.059 + 0.017*SL
	t_{PLH}	0.200	0.171 + 0.015*SL	0.179 + 0.013*SL	0.185 + 0.012*SL
	t_{PHL}	0.232	0.202 + 0.015*SL	0.219 + 0.011*SL	0.240 + 0.010*SL
G to Q	t_R	0.105	0.056 + 0.025*SL	0.053 + 0.026*SL	0.043 + 0.026*SL
	t_F	0.095	0.057 + 0.019*SL	0.066 + 0.017*SL	0.058 + 0.017*SL
	t_{PLH}	0.236	0.207 + 0.015*SL	0.215 + 0.013*SL	0.221 + 0.012*SL
	t_{PHL}	0.251	0.221 + 0.015*SL	0.238 + 0.011*SL	0.259 + 0.010*SL
D to QN	t_R	0.096	0.047 + 0.024*SL	0.040 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.071	0.037 + 0.017*SL	0.036 + 0.017*SL	0.027 + 0.018*SL
	t_{PLH}	0.299	0.273 + 0.013*SL	0.276 + 0.012*SL	0.277 + 0.012*SL
	t_{PHL}	0.260	0.237 + 0.011*SL	0.244 + 0.010*SL	0.247 + 0.010*SL
G to QN	t_R	0.094	0.045 + 0.025*SL	0.039 + 0.026*SL	0.033 + 0.027*SL
	t_F	0.071	0.038 + 0.017*SL	0.036 + 0.017*SL	0.027 + 0.018*SL
	t_{PLH}	0.318	0.292 + 0.013*SL	0.295 + 0.012*SL	0.296 + 0.012*SL
	t_{PHL}	0.296	0.273 + 0.011*SL	0.279 + 0.010*SL	0.283 + 0.010*SL

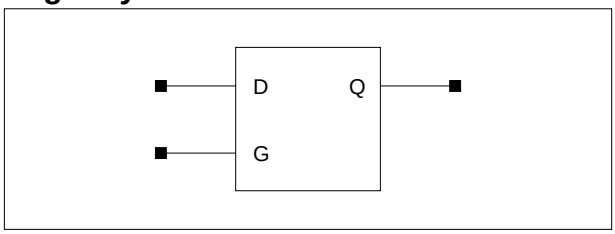
*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

LD1D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.086	0.059 + 0.013*SL	0.062 + 0.013*SL	0.055 + 0.013*SL
	t_F	0.087	0.063 + 0.012*SL	0.074 + 0.009*SL	0.086 + 0.008*SL
	t_{PLH}	0.211	0.191 + 0.010*SL	0.202 + 0.007*SL	0.217 + 0.006*SL
	t_{PHL}	0.248	0.226 + 0.011*SL	0.241 + 0.007*SL	0.272 + 0.005*SL
G to Q	t_R	0.084	0.058 + 0.013*SL	0.060 + 0.013*SL	0.055 + 0.013*SL
	t_F	0.088	0.066 + 0.011*SL	0.073 + 0.009*SL	0.085 + 0.008*SL
	t_{PLH}	0.242	0.222 + 0.010*SL	0.233 + 0.007*SL	0.248 + 0.006*SL
	t_{PHL}	0.266	0.244 + 0.011*SL	0.259 + 0.007*SL	0.290 + 0.005*SL
D to QN	t_R	0.071	0.049 + 0.011*SL	0.044 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.054	0.037 + 0.009*SL	0.038 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.346	0.331 + 0.008*SL	0.336 + 0.006*SL	0.339 + 0.006*SL
	t_{PHL}	0.296	0.282 + 0.007*SL	0.289 + 0.005*SL	0.297 + 0.005*SL
G to QN	t_R	0.071	0.048 + 0.011*SL	0.043 + 0.012*SL	0.031 + 0.013*SL
	t_F	0.054	0.037 + 0.008*SL	0.037 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.365	0.349 + 0.008*SL	0.355 + 0.006*SL	0.358 + 0.006*SL
	t_{PHL}	0.327	0.313 + 0.007*SL	0.320 + 0.005*SL	0.329 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Logic Symbol



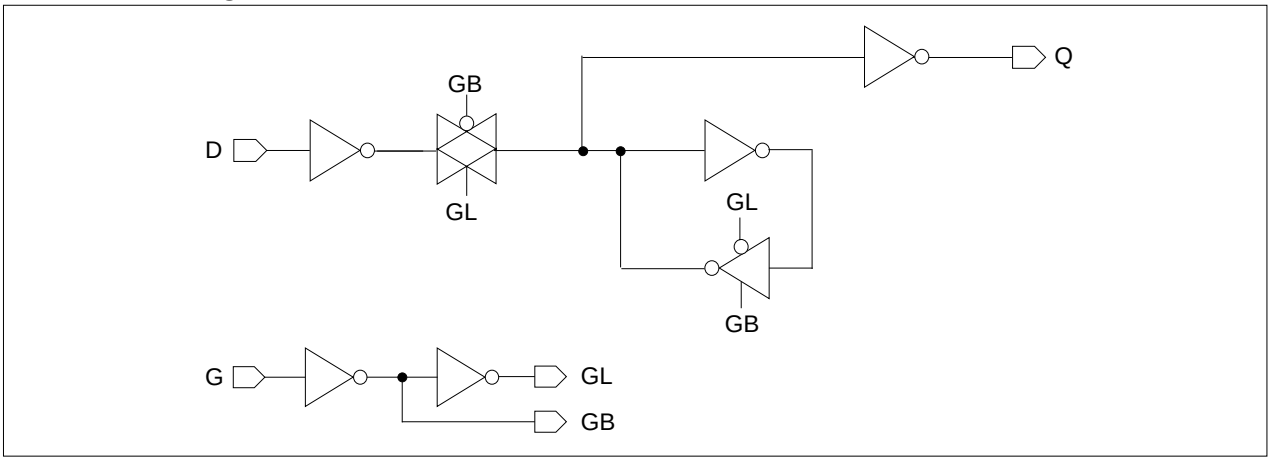
Truth Table

D	G	Q (n+1)
0	1	0
1	1	1
x	0	Q (n)

Cell Data

Input Load (SL)				Gate Count	
LD1Q_LP		*LD1QD2_LP*		*LD1Q_LP*	*LD1QD2_LP*
D	G	D	G		
1.1	1.2	1.1	1.2	3.67	3.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD1Q_LP	LD1QD2_LP
Input Setup Time (D to G)	t_{SU}	0.233	0.257
Input Hold Time (D to G)	t_{HD}	0.134	0.116
Pulse Width High (G)	t_{PWH}	0.245	0.272

LD1Q_LP/LD1QD2_LP

D Latch with Active High, Q Output Only, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD1Q_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.107	0.058 + 0.025*SL	0.054 + 0.026*SL	0.043 + 0.026*SL
	t_F	0.096	0.062 + 0.017*SL	0.065 + 0.017*SL	0.054 + 0.017*SL
	t_{PLH}	0.199	0.170 + 0.015*SL	0.178 + 0.013*SL	0.182 + 0.012*SL
	t_{PHL}	0.229	0.200 + 0.015*SL	0.216 + 0.011*SL	0.233 + 0.010*SL
G to Q	t_R	0.107	0.057 + 0.025*SL	0.054 + 0.026*SL	0.043 + 0.026*SL
	t_F	0.094	0.058 + 0.018*SL	0.064 + 0.017*SL	0.053 + 0.017*SL
	t_{PLH}	0.233	0.204 + 0.015*SL	0.212 + 0.013*SL	0.216 + 0.012*SL
	t_{PHL}	0.245	0.216 + 0.015*SL	0.233 + 0.011*SL	0.250 + 0.010*SL

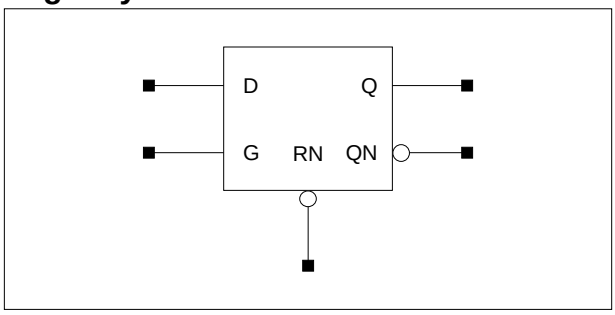
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD1QD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.081	0.055 + 0.013*SL	0.058 + 0.012*SL	0.050 + 0.013*SL
	t_F	0.084	0.061 + 0.011*SL	0.073 + 0.008*SL	0.075 + 0.008*SL
	t_{PLH}	0.200	0.181 + 0.009*SL	0.191 + 0.007*SL	0.204 + 0.006*SL
	t_{PHL}	0.234	0.213 + 0.010*SL	0.227 + 0.007*SL	0.254 + 0.005*SL
G to Q	t_R	0.081	0.055 + 0.013*SL	0.057 + 0.012*SL	0.049 + 0.013*SL
	t_F	0.082	0.059 + 0.012*SL	0.072 + 0.008*SL	0.074 + 0.008*SL
	t_{PLH}	0.234	0.215 + 0.010*SL	0.225 + 0.007*SL	0.238 + 0.006*SL
	t_{PHL}	0.253	0.233 + 0.010*SL	0.247 + 0.007*SL	0.274 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



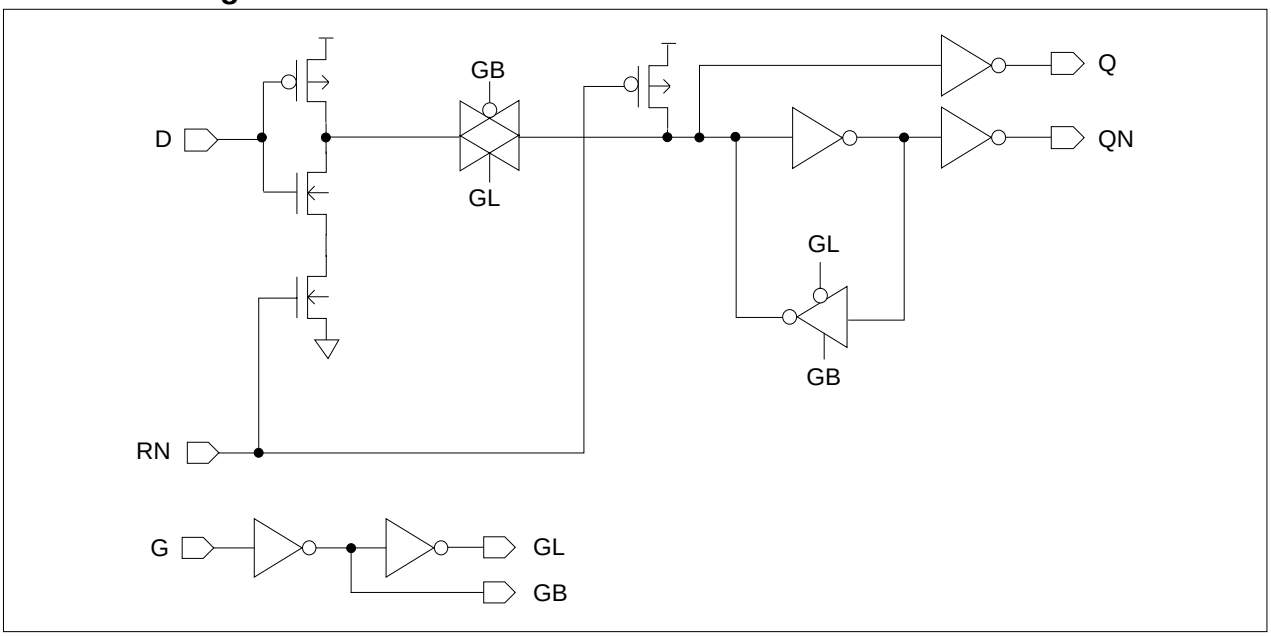
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
LD2_LP			*LD2D2_LP*			*LD2_LP*	*LD2D2_LP*
D	G	RN	D	G	RN		
1.1	1.2	0.7	1.1	1.2	0.8	4.67	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD2_LP	LD2D2_LP
Input Setup Time (D to G)	t_{SU}	0.253	0.296
Input Hold Time (D to G)	t_{HD}	0.080	0.041
Pulse Width High (G)	t_{PWH}	0.274	0.319
Pulse Width Low (RN)	t_{PWL}	0.357	0.352
Recovery Time (RN to G)	t_{RC}	0.196	0.237
Removal Time (RN to G)	t_{RM}	0.089	0.046

LD2_LP/LD2D2_LP

D Latch with Active High, Reset, 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.120	0.068 + 0.026*SL	0.072 + 0.025*SL	0.058 + 0.026*SL
	t_F	0.100	0.062 + 0.019*SL	0.071 + 0.017*SL	0.063 + 0.017*SL
	t_{PLH}	0.254	0.220 + 0.017*SL	0.235 + 0.013*SL	0.250 + 0.012*SL
	t_{PHL}	0.240	0.209 + 0.016*SL	0.227 + 0.011*SL	0.251 + 0.010*SL
G to Q	t_R	0.120	0.068 + 0.026*SL	0.072 + 0.025*SL	0.058 + 0.026*SL
	t_F	0.098	0.061 + 0.019*SL	0.069 + 0.017*SL	0.062 + 0.017*SL
	t_{PLH}	0.266	0.232 + 0.017*SL	0.247 + 0.013*SL	0.262 + 0.012*SL
	t_{PHL}	0.260	0.229 + 0.016*SL	0.247 + 0.011*SL	0.271 + 0.010*SL
RN to Q	t_R	0.121	0.069 + 0.026*SL	0.072 + 0.025*SL	0.058 + 0.026*SL
	t_F	0.121	0.077 + 0.022*SL	0.098 + 0.017*SL	0.105 + 0.017*SL
	t_{PLH}	0.247	0.213 + 0.017*SL	0.229 + 0.013*SL	0.244 + 0.012*SL
	t_{PHL}	0.311	0.273 + 0.019*SL	0.299 + 0.013*SL	0.345 + 0.010*SL
D to QN	t_R	0.098	0.049 + 0.025*SL	0.042 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.074	0.041 + 0.016*SL	0.039 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.307	0.281 + 0.013*SL	0.283 + 0.012*SL	0.285 + 0.012*SL
	t_{PHL}	0.316	0.293 + 0.011*SL	0.300 + 0.010*SL	0.303 + 0.010*SL
G to QN	t_R	0.098	0.049 + 0.025*SL	0.042 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.074	0.041 + 0.016*SL	0.039 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.327	0.301 + 0.013*SL	0.303 + 0.012*SL	0.305 + 0.012*SL
	t_{PHL}	0.328	0.305 + 0.011*SL	0.312 + 0.010*SL	0.315 + 0.010*SL
RN to QN	t_R	0.102	0.054 + 0.024*SL	0.045 + 0.026*SL	0.036 + 0.027*SL
	t_F	0.074	0.040 + 0.017*SL	0.040 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.383	0.356 + 0.013*SL	0.359 + 0.012*SL	0.361 + 0.012*SL
	t_{PHL}	0.310	0.287 + 0.011*SL	0.294 + 0.010*SL	0.297 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD2D2_LP

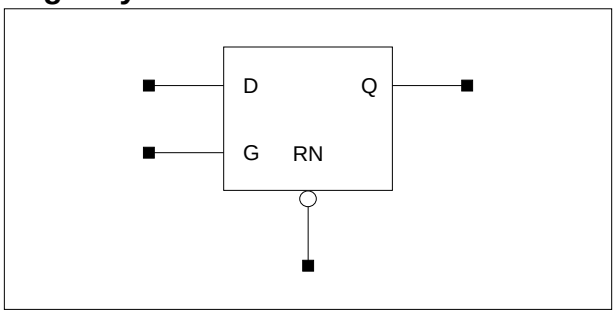
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.100	0.071 + 0.015*SL	0.078 + 0.013*SL	0.081 + 0.013*SL
	t_F	0.091	0.069 + 0.011*SL	0.077 + 0.009*SL	0.090 + 0.008*SL
	t_{PLH}	0.270	0.247 + 0.012*SL	0.261 + 0.008*SL	0.287 + 0.007*SL
	t_{PHL}	0.254	0.232 + 0.011*SL	0.248 + 0.007*SL	0.280 + 0.005*SL
G to Q	t_R	0.101	0.072 + 0.015*SL	0.080 + 0.013*SL	0.081 + 0.013*SL
	t_F	0.089	0.066 + 0.012*SL	0.077 + 0.009*SL	0.090 + 0.008*SL
	t_{PLH}	0.278	0.255 + 0.012*SL	0.270 + 0.008*SL	0.296 + 0.007*SL
	t_{PHL}	0.275	0.252 + 0.011*SL	0.268 + 0.007*SL	0.301 + 0.005*SL
RN to Q	t_R	0.100	0.071 + 0.015*SL	0.078 + 0.013*SL	0.081 + 0.013*SL
	t_F	0.091	0.067 + 0.012*SL	0.077 + 0.009*SL	0.098 + 0.008*SL
	t_{PLH}	0.265	0.242 + 0.012*SL	0.256 + 0.008*SL	0.282 + 0.007*SL
	t_{PHL}	0.278	0.256 + 0.011*SL	0.270 + 0.008*SL	0.306 + 0.006*SL
D to QN	t_R	0.072	0.049 + 0.011*SL	0.045 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.058	0.041 + 0.008*SL	0.042 + 0.008*SL	0.036 + 0.009*SL
	t_{PLH}	0.355	0.339 + 0.008*SL	0.345 + 0.006*SL	0.348 + 0.006*SL
	t_{PHL}	0.366	0.351 + 0.007*SL	0.359 + 0.005*SL	0.369 + 0.005*SL
G to QN	t_R	0.072	0.049 + 0.011*SL	0.044 + 0.012*SL	0.032 + 0.013*SL
	t_F	0.058	0.042 + 0.008*SL	0.042 + 0.008*SL	0.036 + 0.009*SL
	t_{PLH}	0.376	0.360 + 0.008*SL	0.366 + 0.006*SL	0.369 + 0.006*SL
	t_{PHL}	0.374	0.359 + 0.007*SL	0.367 + 0.005*SL	0.377 + 0.005*SL
RN to QN	t_R	0.073	0.051 + 0.011*SL	0.045 + 0.012*SL	0.033 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.046 + 0.008*SL	0.036 + 0.009*SL
	t_{PLH}	0.379	0.363 + 0.008*SL	0.369 + 0.006*SL	0.372 + 0.006*SL
	t_{PHL}	0.360	0.345 + 0.007*SL	0.353 + 0.005*SL	0.363 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD2Q_LP/LD2QD2_LP

D Latch with Active High, Reset, Q Output Only, 1X/2X Drive

Logic Symbol



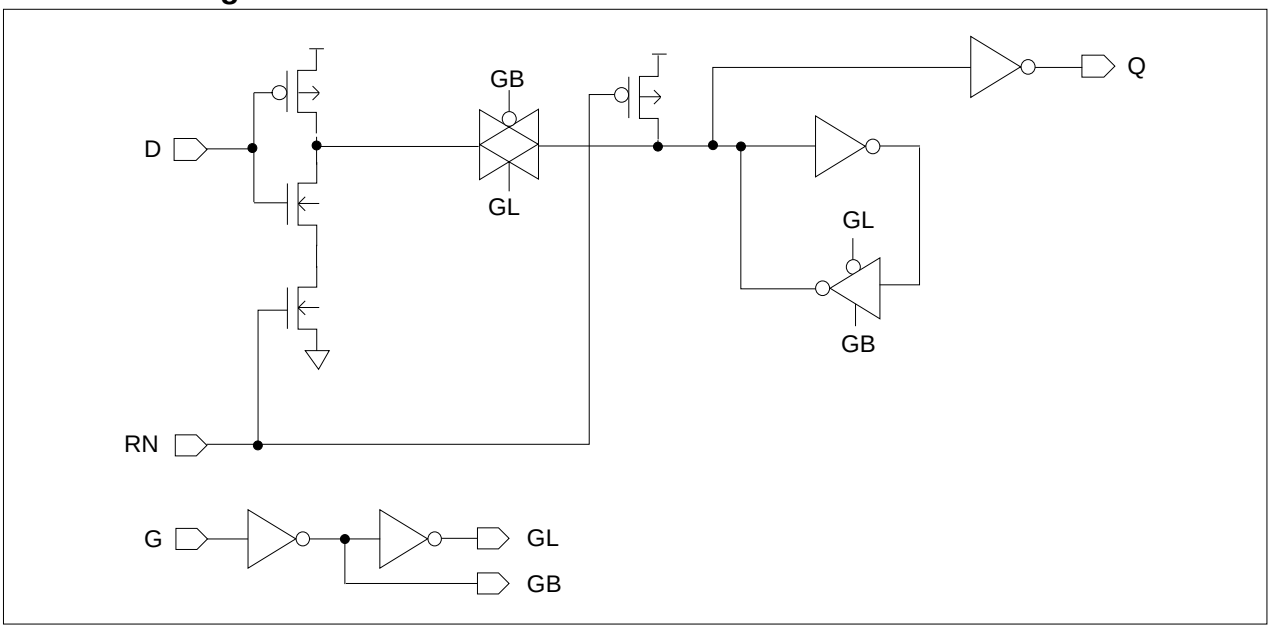
Truth Table

D	G	RN	Q (n+1)
0	1	1	0
1	1	1	1
x	0	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
LD2Q_LP			*LD2QD2_LP*			*LD2Q_LP*	*LD2QD2_LP*
D	G	RN	D	G	RN		
1.1	1.2	0.9	1.1	1.2	0.9	4.00	4.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD2Q_LP	LD2QD2_LP
Input Setup Time (D to G)	t_{SU}	0.237	0.270
Input Hold Time (D to G)	t_{HD}	0.090	0.060
Pulse Width High (G)	t_{PWH}	0.249	0.277
Pulse Width Low (RN)	t_{PWL}	0.317	0.300
Recovery Time (RN to G)	t_{RC}	0.185	0.215
Removal Time (RN to G)	t_{RM}	0.099	0.066

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD2Q_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.122	0.072 + 0.025*SL	0.072 + 0.025*SL	0.057 + 0.026*SL
	t_F	0.100	0.064 + 0.018*SL	0.070 + 0.016*SL	0.058 + 0.017*SL
	t_{PLH}	0.248	0.215 + 0.017*SL	0.229 + 0.013*SL	0.239 + 0.012*SL
	t_{PHL}	0.236	0.206 + 0.015*SL	0.223 + 0.011*SL	0.242 + 0.010*SL
G to Q	t_R	0.122	0.071 + 0.025*SL	0.071 + 0.025*SL	0.056 + 0.026*SL
	t_F	0.099	0.063 + 0.018*SL	0.068 + 0.016*SL	0.058 + 0.017*SL
	t_{PLH}	0.257	0.224 + 0.017*SL	0.238 + 0.013*SL	0.249 + 0.012*SL
	t_{PHL}	0.252	0.222 + 0.015*SL	0.240 + 0.011*SL	0.259 + 0.010*SL
RN to Q	t_R	0.123	0.074 + 0.025*SL	0.071 + 0.025*SL	0.057 + 0.026*SL
	t_F	0.124	0.082 + 0.021*SL	0.098 + 0.017*SL	0.102 + 0.017*SL
	t_{PLH}	0.241	0.207 + 0.017*SL	0.222 + 0.013*SL	0.232 + 0.012*SL
	t_{PHL}	0.308	0.271 + 0.018*SL	0.295 + 0.012*SL	0.338 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD2QD2_LP

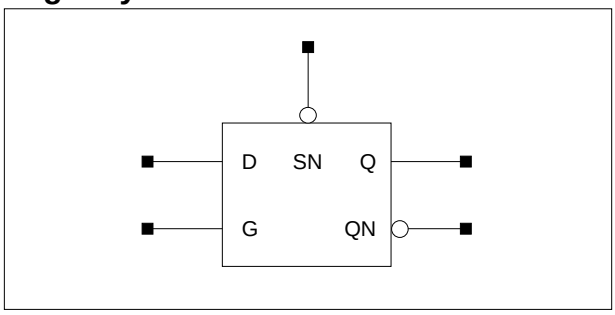
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.099	0.070 + 0.014*SL	0.078 + 0.012*SL	0.075 + 0.013*SL
	t_F	0.088	0.065 + 0.012*SL	0.078 + 0.008*SL	0.082 + 0.008*SL
	t_{PLH}	0.257	0.235 + 0.011*SL	0.248 + 0.008*SL	0.271 + 0.006*SL
	t_{PHL}	0.244	0.223 + 0.011*SL	0.238 + 0.007*SL	0.267 + 0.005*SL
G to Q	t_R	0.098	0.068 + 0.015*SL	0.078 + 0.012*SL	0.074 + 0.013*SL
	t_F	0.087	0.063 + 0.012*SL	0.077 + 0.008*SL	0.080 + 0.008*SL
	t_{PLH}	0.264	0.242 + 0.011*SL	0.255 + 0.008*SL	0.279 + 0.006*SL
	t_{PHL}	0.262	0.241 + 0.011*SL	0.256 + 0.007*SL	0.285 + 0.005*SL
RN to Q	t_R	0.099	0.071 + 0.014*SL	0.078 + 0.012*SL	0.075 + 0.013*SL
	t_F	0.091	0.068 + 0.011*SL	0.077 + 0.009*SL	0.093 + 0.008*SL
	t_{PLH}	0.251	0.229 + 0.011*SL	0.242 + 0.008*SL	0.265 + 0.006*SL
	t_{PHL}	0.269	0.247 + 0.011*SL	0.261 + 0.007*SL	0.295 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD3_LP/LD3D2_LP

D Latch with Active High, Set, 1X/2X Drive

Logic Symbol



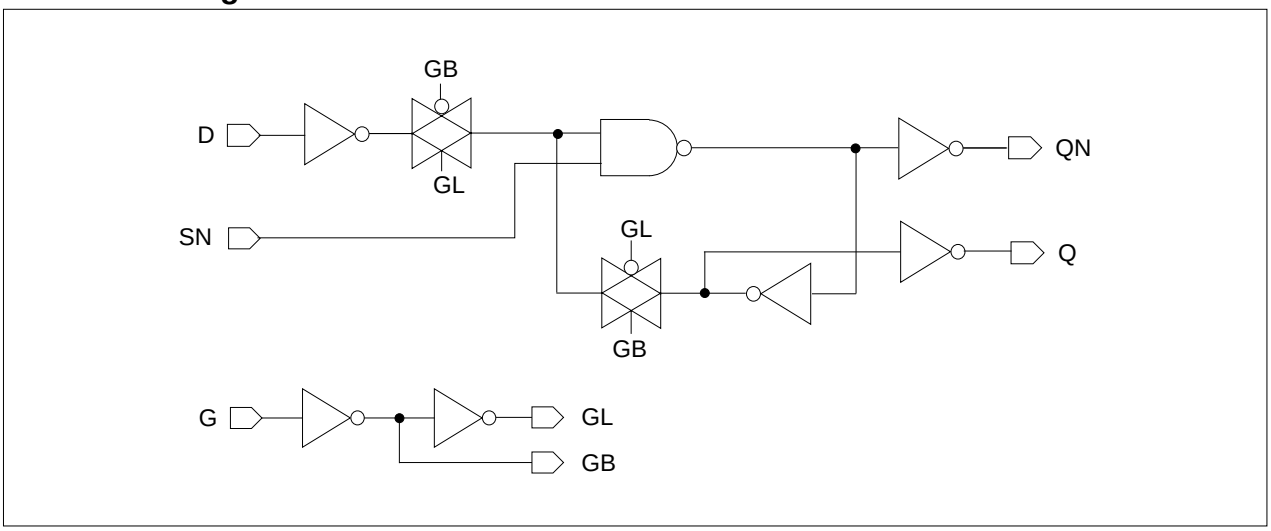
Truth Table

D	G	SN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
LD3_LP			*LD3D2_LP*			*LD3_LP*	*LD3D2_LP*
D	G	SN	D	G	SN		
1.2	1.2	1.1	1.2	1.2	1.1	4.67	5.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD3_LP	LD3D2_LP
Input Setup Time (D to G)	t_{SU}	0.246	0.258
Input Hold Time (D to G)	t_{HD}	0.127	0.110
Pulse Width High (G)	t_{PWH}	0.259	0.274
Pulse Width Low (SN)	t_{PWL}	0.283	0.317
Recovery Time (SN to G)	t_{RC}	0.055	0.085
Removal Time (SN to G)	t_{RM}	0.225	0.195

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.092	0.042 + 0.025*SL	0.036 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.072	0.039 + 0.016*SL	0.036 + 0.017*SL	0.027 + 0.018*SL
	t_{PLH}	0.314	0.288 + 0.013*SL	0.290 + 0.012*SL	0.291 + 0.012*SL
	t_{PHL}	0.362	0.339 + 0.011*SL	0.346 + 0.010*SL	0.349 + 0.010*SL
G to Q	t_R	0.092	0.041 + 0.025*SL	0.038 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.072	0.039 + 0.016*SL	0.036 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.354	0.328 + 0.013*SL	0.330 + 0.012*SL	0.331 + 0.012*SL
	t_{PHL}	0.379	0.357 + 0.011*SL	0.363 + 0.010*SL	0.366 + 0.010*SL
SN to Q	t_R	0.092	0.043 + 0.025*SL	0.035 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.072	0.039 + 0.016*SL	0.036 + 0.017*SL	0.027 + 0.018*SL
	t_{PLH}	0.247	0.220 + 0.013*SL	0.223 + 0.012*SL	0.224 + 0.012*SL
	t_{PHL}	0.231	0.208 + 0.011*SL	0.215 + 0.010*SL	0.218 + 0.010*SL
D to QN	t_R	0.103	0.054 + 0.025*SL	0.050 + 0.026*SL	0.039 + 0.026*SL
	t_F	0.075	0.041 + 0.017*SL	0.041 + 0.017*SL	0.032 + 0.017*SL
	t_{PLH}	0.302	0.273 + 0.015*SL	0.281 + 0.013*SL	0.286 + 0.012*SL
	t_{PHL}	0.252	0.227 + 0.012*SL	0.237 + 0.010*SL	0.244 + 0.010*SL
G to QN	t_R	0.102	0.053 + 0.025*SL	0.050 + 0.026*SL	0.039 + 0.026*SL
	t_F	0.074	0.040 + 0.017*SL	0.041 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.319	0.290 + 0.015*SL	0.298 + 0.013*SL	0.304 + 0.012*SL
	t_{PHL}	0.291	0.267 + 0.012*SL	0.277 + 0.010*SL	0.284 + 0.010*SL
SN to QN	t_R	0.101	0.051 + 0.025*SL	0.049 + 0.026*SL	0.038 + 0.026*SL
	t_F	0.077	0.044 + 0.017*SL	0.043 + 0.017*SL	0.032 + 0.017*SL
	t_{PLH}	0.171	0.141 + 0.015*SL	0.149 + 0.013*SL	0.155 + 0.012*SL
	t_{PHL}	0.184	0.159 + 0.012*SL	0.169 + 0.010*SL	0.176 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD3_LP/LD3D2_LP

D Latch with Active High, Reset, 1X/2X Drive

Switching Characteristics

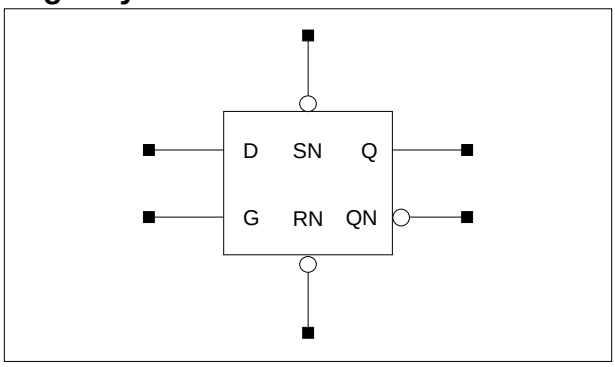
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD3D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.066	0.043 + 0.012*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.056	0.040 + 0.008*SL	0.040 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.343	0.328 + 0.007*SL	0.332 + 0.006*SL	0.335 + 0.006*SL
	t_{PHL}	0.395	0.381 + 0.007*SL	0.389 + 0.005*SL	0.397 + 0.005*SL
G to Q	t_R	0.065	0.042 + 0.012*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.056	0.039 + 0.008*SL	0.040 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.383	0.369 + 0.007*SL	0.373 + 0.006*SL	0.376 + 0.006*SL
	t_{PHL}	0.413	0.398 + 0.007*SL	0.406 + 0.005*SL	0.414 + 0.005*SL
SN to Q	t_R	0.066	0.044 + 0.011*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.055	0.037 + 0.009*SL	0.041 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.275	0.261 + 0.007*SL	0.265 + 0.006*SL	0.268 + 0.006*SL
	t_{PHL}	0.262	0.248 + 0.007*SL	0.255 + 0.005*SL	0.264 + 0.005*SL
D to QN	t_R	0.083	0.057 + 0.013*SL	0.059 + 0.012*SL	0.050 + 0.013*SL
	t_F	0.063	0.044 + 0.009*SL	0.047 + 0.008*SL	0.045 + 0.008*SL
	t_{PLH}	0.312	0.293 + 0.009*SL	0.303 + 0.007*SL	0.315 + 0.006*SL
	t_{PHL}	0.261	0.245 + 0.008*SL	0.254 + 0.006*SL	0.270 + 0.005*SL
G to QN	t_R	0.082	0.056 + 0.013*SL	0.058 + 0.012*SL	0.050 + 0.013*SL
	t_F	0.062	0.044 + 0.009*SL	0.046 + 0.009*SL	0.046 + 0.008*SL
	t_{PLH}	0.329	0.311 + 0.009*SL	0.321 + 0.007*SL	0.333 + 0.006*SL
	t_{PHL}	0.302	0.285 + 0.008*SL	0.295 + 0.006*SL	0.310 + 0.005*SL
SN to QN	t_R	0.081	0.056 + 0.012*SL	0.055 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.064	0.047 + 0.008*SL	0.047 + 0.008*SL	0.047 + 0.008*SL
	t_{PLH}	0.180	0.161 + 0.009*SL	0.171 + 0.007*SL	0.182 + 0.006*SL
	t_{PHL}	0.194	0.177 + 0.008*SL	0.187 + 0.006*SL	0.202 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Logic Symbol



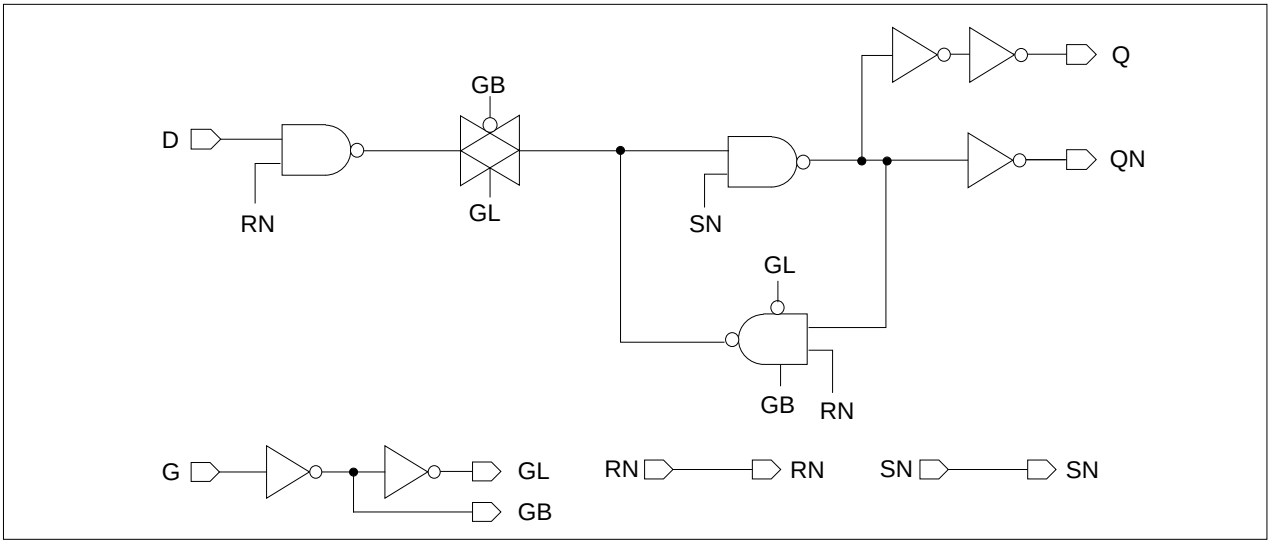
Truth Table

D	G	RN	SN	Q (n+1)	QN (n+1)
0	1	1	1	0	1
1	1	1	1	1	0
x	0	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
LD4_LP				*LD4D2_LP*				*LD4_LP*	*LD4D2_LP*
D	G	SN	RN	D	G	SN	RN		
1.1	1.2	1.1	1.3	1.1	1.2	1.1	1.3	6.00	6.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD4_LP	LD4D2_LP
Input Setup Time (D to G)	t_{SU}	0.270	0.271
Input Hold Time (D to G)	t_{HD}	0.093	0.090
Pulse Width High (G)	t_{PWH}	0.247	0.253
Pulse Width Low (SN)	t_{PWL}	0.366	0.382
Recovery Time (SN to G)	t_{RC}	0.000	0.007
Removal Time (SN to G)	t_{RM}	0.322	0.300
Pulse Width Low (RN)	t_{PWL}	0.883	0.909
Recovery Time (RN to G)	t_{RC}	0.187	0.188
Removal Time (RN to G)	t_{RM}	0.098	0.097
Recovery Time (SN to RN)	t_{RC}	0.053	0.074
Removal Time (SN to RN)	t_{RM}	0.222	0.196

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.092	0.041 + 0.025*SL	0.037 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.071	0.039 + 0.016*SL	0.035 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.372	0.346 + 0.013*SL	0.348 + 0.012*SL	0.349 + 0.012*SL
	t_{PHL}	0.398	0.375 + 0.011*SL	0.381 + 0.010*SL	0.384 + 0.010*SL
G to Q	t_R	0.092	0.042 + 0.025*SL	0.037 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.069	0.036 + 0.017*SL	0.035 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.369	0.343 + 0.013*SL	0.345 + 0.012*SL	0.347 + 0.012*SL
	t_{PHL}	0.386	0.364 + 0.011*SL	0.370 + 0.010*SL	0.373 + 0.010*SL
SN to Q	t_R	0.092	0.042 + 0.025*SL	0.037 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.071	0.036 + 0.018*SL	0.039 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.249	0.223 + 0.013*SL	0.225 + 0.012*SL	0.227 + 0.012*SL
	t_{PHL}	0.233	0.213 + 0.010*SL	0.215 + 0.010*SL	0.218 + 0.010*SL
RN to Q	t_R	0.091	0.042 + 0.025*SL	0.035 + 0.026*SL	0.032 + 0.027*SL
	t_F	0.071	0.038 + 0.016*SL	0.036 + 0.017*SL	0.026 + 0.018*SL
	t_{PLH}	0.368	0.342 + 0.013*SL	0.344 + 0.012*SL	0.346 + 0.012*SL
	t_{PHL}	0.407	0.384 + 0.011*SL	0.391 + 0.010*SL	0.393 + 0.010*SL
D to QN	t_R	0.105	0.056 + 0.024*SL	0.052 + 0.025*SL	0.040 + 0.026*SL
	t_F	0.077	0.042 + 0.017*SL	0.045 + 0.017*SL	0.034 + 0.017*SL
	t_{PLH}	0.340	0.311 + 0.015*SL	0.320 + 0.013*SL	0.326 + 0.012*SL
	t_{PHL}	0.313	0.288 + 0.013*SL	0.299 + 0.010*SL	0.307 + 0.010*SL
G to QN	t_R	0.104	0.055 + 0.025*SL	0.051 + 0.026*SL	0.040 + 0.026*SL
	t_F	0.077	0.042 + 0.018*SL	0.045 + 0.017*SL	0.034 + 0.017*SL
	t_{PLH}	0.329	0.299 + 0.015*SL	0.309 + 0.013*SL	0.315 + 0.012*SL
	t_{PHL}	0.311	0.285 + 0.013*SL	0.296 + 0.010*SL	0.305 + 0.010*SL
SN to QN	t_R	0.103	0.054 + 0.025*SL	0.050 + 0.026*SL	0.039 + 0.026*SL
	t_F	0.078	0.044 + 0.017*SL	0.045 + 0.017*SL	0.034 + 0.017*SL
	t_{PLH}	0.177	0.148 + 0.015*SL	0.156 + 0.013*SL	0.162 + 0.012*SL
	t_{PHL}	0.191	0.166 + 0.013*SL	0.176 + 0.010*SL	0.185 + 0.010*SL
RN to QN	t_R	0.105	0.056 + 0.024*SL	0.052 + 0.026*SL	0.040 + 0.026*SL
	t_F	0.077	0.042 + 0.017*SL	0.044 + 0.017*SL	0.034 + 0.017*SL
	t_{PLH}	0.350	0.320 + 0.015*SL	0.329 + 0.013*SL	0.335 + 0.012*SL
	t_{PHL}	0.310	0.284 + 0.013*SL	0.295 + 0.010*SL	0.304 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD4D2_LP

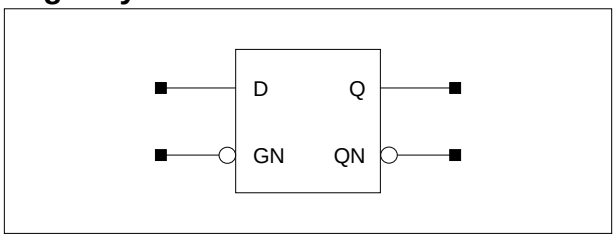
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.065	0.041 + 0.012*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.057	0.041 + 0.008*SL	0.040 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.403	0.388 + 0.007*SL	0.392 + 0.006*SL	0.395 + 0.006*SL
	t_{PHL}	0.433	0.418 + 0.007*SL	0.426 + 0.005*SL	0.435 + 0.005*SL
G to Q	t_R	0.065	0.041 + 0.012*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.055	0.039 + 0.008*SL	0.038 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.401	0.386 + 0.007*SL	0.391 + 0.006*SL	0.393 + 0.006*SL
	t_{PHL}	0.424	0.409 + 0.007*SL	0.417 + 0.005*SL	0.426 + 0.005*SL
SN to Q	t_R	0.066	0.043 + 0.012*SL	0.038 + 0.013*SL	0.030 + 0.013*SL
	t_F	0.055	0.038 + 0.008*SL	0.038 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.280	0.265 + 0.007*SL	0.270 + 0.006*SL	0.272 + 0.006*SL
	t_{PHL}	0.269	0.254 + 0.007*SL	0.262 + 0.005*SL	0.271 + 0.005*SL
RN to Q	t_R	0.066	0.044 + 0.011*SL	0.038 + 0.013*SL	0.029 + 0.013*SL
	t_F	0.057	0.040 + 0.009*SL	0.041 + 0.008*SL	0.034 + 0.009*SL
	t_{PLH}	0.399	0.384 + 0.007*SL	0.388 + 0.006*SL	0.391 + 0.006*SL
	t_{PHL}	0.443	0.428 + 0.007*SL	0.436 + 0.005*SL	0.445 + 0.005*SL
D to QN	t_R	0.084	0.058 + 0.013*SL	0.060 + 0.012*SL	0.051 + 0.013*SL
	t_F	0.064	0.045 + 0.009*SL	0.048 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.346	0.327 + 0.010*SL	0.337 + 0.007*SL	0.351 + 0.006*SL
	t_{PHL}	0.319	0.302 + 0.008*SL	0.312 + 0.006*SL	0.329 + 0.005*SL
G to QN	t_R	0.083	0.058 + 0.013*SL	0.059 + 0.013*SL	0.051 + 0.013*SL
	t_F	0.063	0.045 + 0.009*SL	0.048 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.338	0.318 + 0.010*SL	0.329 + 0.007*SL	0.342 + 0.006*SL
	t_{PHL}	0.318	0.301 + 0.008*SL	0.311 + 0.006*SL	0.328 + 0.005*SL
SN to QN	t_R	0.082	0.056 + 0.013*SL	0.058 + 0.013*SL	0.050 + 0.013*SL
	t_F	0.065	0.047 + 0.009*SL	0.049 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.183	0.164 + 0.010*SL	0.174 + 0.007*SL	0.186 + 0.006*SL
	t_{PHL}	0.197	0.180 + 0.008*SL	0.190 + 0.006*SL	0.207 + 0.005*SL
RN to QN	t_R	0.084	0.059 + 0.013*SL	0.060 + 0.012*SL	0.052 + 0.013*SL
	t_F	0.064	0.045 + 0.009*SL	0.050 + 0.008*SL	0.048 + 0.008*SL
	t_{PLH}	0.357	0.337 + 0.010*SL	0.348 + 0.007*SL	0.361 + 0.006*SL
	t_{PHL}	0.315	0.299 + 0.008*SL	0.309 + 0.006*SL	0.325 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

LD5_LP/LD5D2_LP

D Latch with Active Low, 1X/2X Drive

Logic Symbol



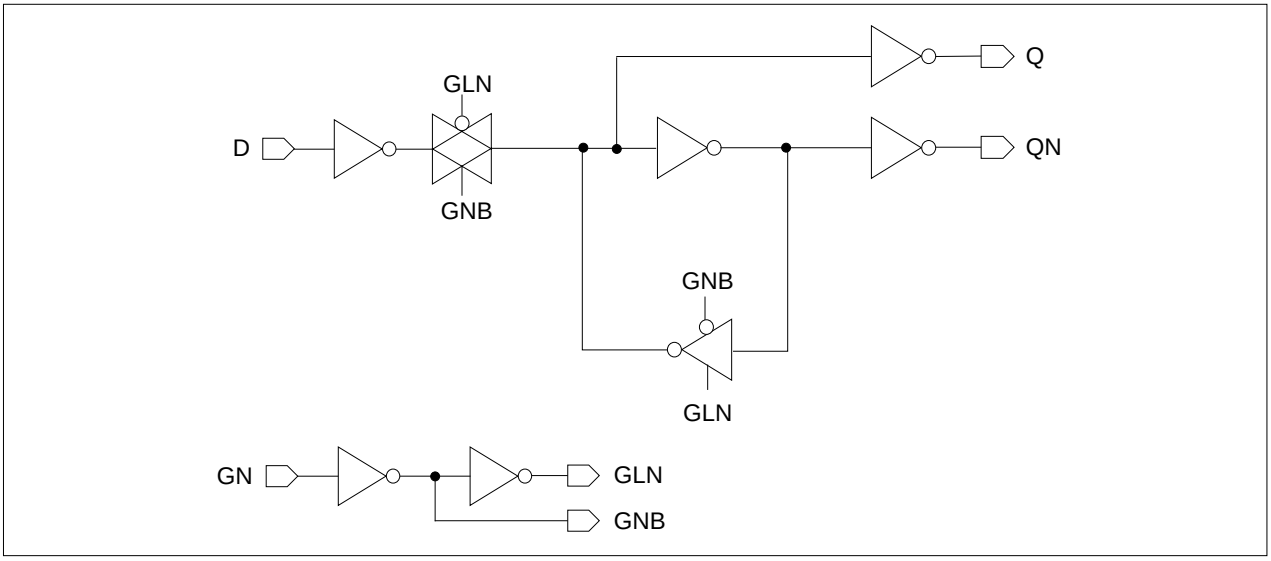
Truth Table

D	GN	Q (n+1)	QN (n+1)
0	0	0	1
1	0	1	0
x	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
LD5_LP		*LD5D2_LP*		*LD5_LP*	*LD5D2_LP*
D	GN	D	GN		
1.1	1.2	1.2	1.2	4.33	4.67

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD5_LP	LD5D2_LP
Input Setup Time (D to GN)	t_{SU}	0.241	0.269
Input Hold Time (D to GN)	t_{HD}	0.055	0.014
Pulse Width Low (GN)	t_{PWL}	0.256	0.299

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD5_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.106	0.056 + 0.025*SL	0.054 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.097	0.060 + 0.018*SL	0.068 + 0.016*SL	0.058 + 0.017*SL
	t_{PLH}	0.200	0.170 + 0.015*SL	0.179 + 0.013*SL	0.185 + 0.012*SL
	t_{PHL}	0.232	0.202 + 0.015*SL	0.219 + 0.011*SL	0.240 + 0.010*SL
GN to Q	t_R	0.105	0.055 + 0.025*SL	0.053 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.095	0.058 + 0.019*SL	0.066 + 0.017*SL	0.057 + 0.017*SL
	t_{PLH}	0.243	0.213 + 0.015*SL	0.222 + 0.013*SL	0.229 + 0.012*SL
	t_{PHL}	0.276	0.246 + 0.015*SL	0.263 + 0.011*SL	0.284 + 0.010*SL
D to QN	t_R	0.098	0.048 + 0.025*SL	0.042 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.072	0.038 + 0.017*SL	0.037 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.298	0.272 + 0.013*SL	0.275 + 0.012*SL	0.276 + 0.012*SL
	t_{PHL}	0.259	0.237 + 0.011*SL	0.243 + 0.010*SL	0.246 + 0.010*SL
GN to QN	t_R	0.097	0.048 + 0.024*SL	0.041 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.072	0.039 + 0.017*SL	0.037 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.343	0.316 + 0.013*SL	0.319 + 0.012*SL	0.320 + 0.012*SL
	t_{PHL}	0.302	0.280 + 0.011*SL	0.286 + 0.010*SL	0.289 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD5D2_LP

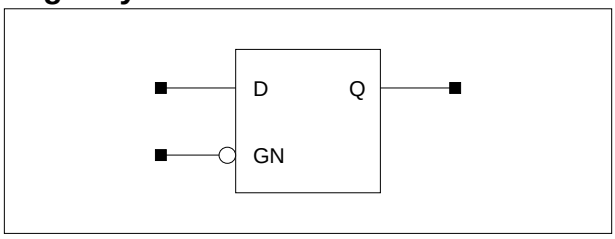
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.086	0.060 + 0.013*SL	0.062 + 0.012*SL	0.055 + 0.013*SL
	t_F	0.087	0.064 + 0.011*SL	0.075 + 0.009*SL	0.085 + 0.008*SL
	t_{PLH}	0.210	0.190 + 0.010*SL	0.201 + 0.007*SL	0.215 + 0.006*SL
	t_{PHL}	0.247	0.226 + 0.011*SL	0.240 + 0.007*SL	0.270 + 0.005*SL
GN to Q	t_R	0.086	0.060 + 0.013*SL	0.062 + 0.012*SL	0.055 + 0.013*SL
	t_F	0.087	0.064 + 0.011*SL	0.074 + 0.009*SL	0.085 + 0.008*SL
	t_{PLH}	0.257	0.238 + 0.010*SL	0.248 + 0.007*SL	0.263 + 0.006*SL
	t_{PHL}	0.294	0.273 + 0.011*SL	0.288 + 0.007*SL	0.318 + 0.005*SL
D to QN	t_R	0.072	0.049 + 0.011*SL	0.044 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.055	0.038 + 0.009*SL	0.039 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.346	0.330 + 0.008*SL	0.336 + 0.006*SL	0.339 + 0.006*SL
	t_{PHL}	0.295	0.281 + 0.007*SL	0.288 + 0.005*SL	0.297 + 0.005*SL
GN to QN	t_R	0.072	0.049 + 0.011*SL	0.044 + 0.013*SL	0.033 + 0.013*SL
	t_F	0.054	0.038 + 0.008*SL	0.038 + 0.008*SL	0.033 + 0.009*SL
	t_{PLH}	0.393	0.377 + 0.008*SL	0.383 + 0.006*SL	0.386 + 0.006*SL
	t_{PHL}	0.343	0.329 + 0.007*SL	0.336 + 0.005*SL	0.344 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD5Q_LP/LD5QD2_LP

D Latch with Active Low, Q Output Only, 1X/2X Drive

Logic Symbol



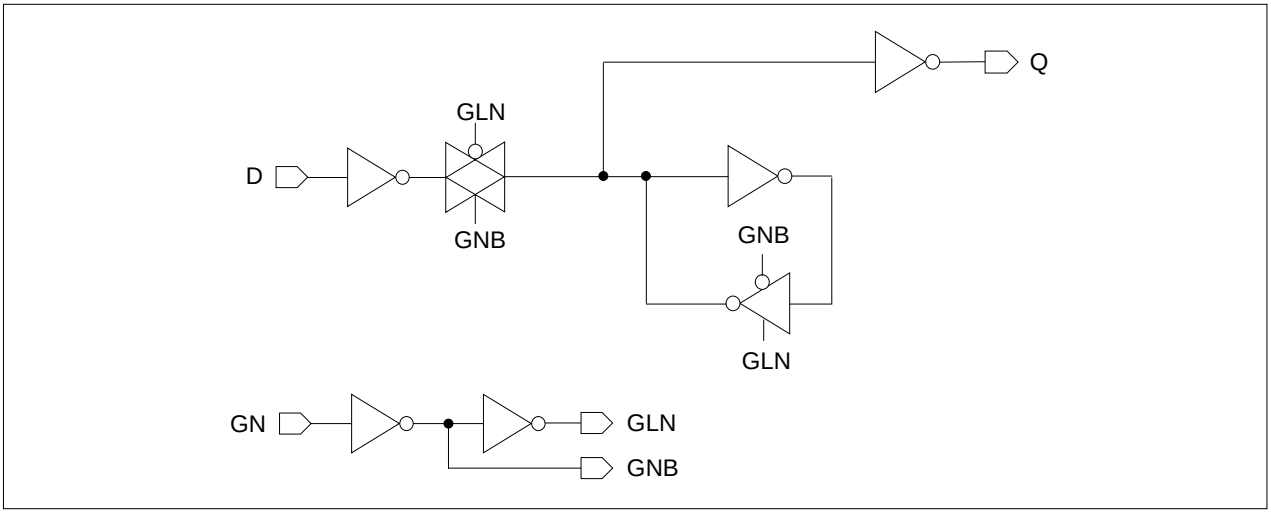
Truth Table

D	GN	Q (n+1)
0	0	0
1	0	1
x	1	Q (n)

Cell Data

Input Load (SL)				Gate Count	
LD5Q_LP		*LD5QD2_LP*		*LD5Q_LP*	*LD5QD2_LP*
D	GN	D	GN		
1.1	1.2	1.1	1.2	3.67	4.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD5Q_LP	LD5QD2_LP
Input Setup Time (D to GN)	t_{SU}	0.234	0.252
Input Hold Time (D to GN)	t_{HD}	0.068	0.044
Pulse Width Low (GN)	t_{PWL}	0.241	0.261

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD5Q_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.107	0.057 + 0.025*SL	0.053 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.096	0.062 + 0.017*SL	0.065 + 0.017*SL	0.054 + 0.017*SL
	t_{PLH}	0.199	0.169 + 0.015*SL	0.178 + 0.013*SL	0.182 + 0.012*SL
	t_{PHL}	0.228	0.199 + 0.015*SL	0.216 + 0.011*SL	0.233 + 0.010*SL
GN to Q	t_R	0.106	0.056 + 0.025*SL	0.053 + 0.026*SL	0.042 + 0.026*SL
	t_F	0.094	0.059 + 0.018*SL	0.064 + 0.017*SL	0.053 + 0.017*SL
	t_{PLH}	0.241	0.211 + 0.015*SL	0.220 + 0.013*SL	0.224 + 0.012*SL
	t_{PHL}	0.272	0.243 + 0.015*SL	0.260 + 0.011*SL	0.277 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD5QD2_LP

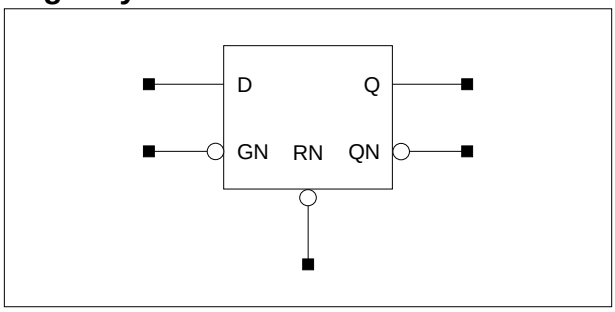
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.083	0.056 + 0.013*SL	0.060 + 0.012*SL	0.050 + 0.013*SL
	t_F	0.084	0.062 + 0.011*SL	0.073 + 0.008*SL	0.075 + 0.008*SL
	t_{PLH}	0.200	0.181 + 0.009*SL	0.191 + 0.007*SL	0.204 + 0.006*SL
	t_{PHL}	0.234	0.214 + 0.010*SL	0.228 + 0.007*SL	0.255 + 0.005*SL
GN to Q	t_R	0.082	0.056 + 0.013*SL	0.059 + 0.012*SL	0.050 + 0.013*SL
	t_F	0.084	0.062 + 0.011*SL	0.072 + 0.008*SL	0.074 + 0.008*SL
	t_{PLH}	0.244	0.225 + 0.009*SL	0.235 + 0.007*SL	0.248 + 0.006*SL
	t_{PHL}	0.278	0.258 + 0.010*SL	0.272 + 0.007*SL	0.298 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD6_LP/LD6D2_LP

D Latch with Active Low, Reset, 1X/2X Drive

Logic Symbol



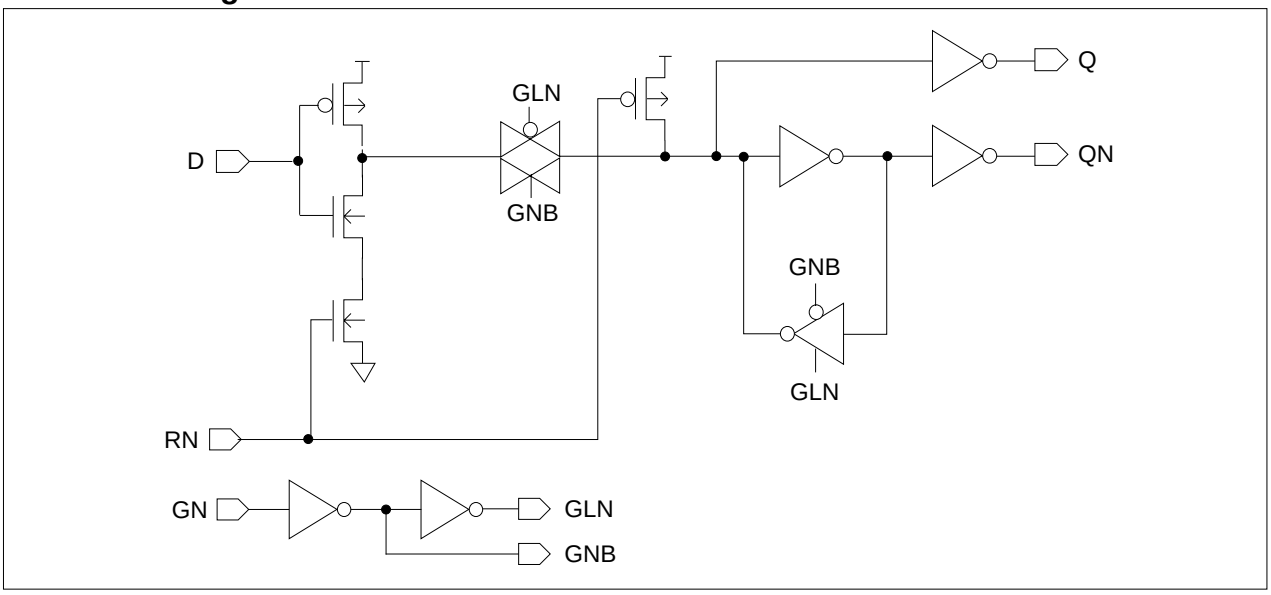
Truth Table

D	GN	RN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
LD6_LP			*LD6D2_LP*			*LD6_LP*	*LD6D2_LP*
D	GN	RN	D	GN	RN		
1.1	1.2	0.7	1.1	1.2	0.8	4.67	5.00

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD6_LP	LD6D2_LP
Input Setup Time (D to GN)	t_{SU}	0.287	0.323
Input Hold Time (D to GN)	t_{HD}	0.047	0.014
Pulse Width Low (GN)	t_{PWL}	0.281	0.328
Pulse Width Low (RN)	t_{PWL}	0.358	0.354
Recovery Time (RN to GN)	t_{RC}	0.282	0.319
Removal Time (RN to GN)	t_{RM}	0.000	0.000

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.121	0.069 + 0.026*SL	0.072 + 0.025*SL	0.058 + 0.026*SL
	t_F	0.100	0.062 + 0.019*SL	0.072 + 0.016*SL	0.063 + 0.017*SL
	t_{PLH}	0.254	0.220 + 0.017*SL	0.235 + 0.013*SL	0.250 + 0.012*SL
	t_{PHL}	0.241	0.210 + 0.016*SL	0.228 + 0.011*SL	0.252 + 0.010*SL
GN to Q	t_R	0.120	0.068 + 0.026*SL	0.072 + 0.025*SL	0.058 + 0.026*SL
	t_F	0.098	0.061 + 0.019*SL	0.070 + 0.017*SL	0.063 + 0.017*SL
	t_{PLH}	0.275	0.241 + 0.017*SL	0.256 + 0.013*SL	0.271 + 0.012*SL
	t_{PHL}	0.285	0.254 + 0.016*SL	0.273 + 0.011*SL	0.297 + 0.010*SL
RN to Q	t_R	0.121	0.070 + 0.026*SL	0.072 + 0.025*SL	0.058 + 0.026*SL
	t_F	0.122	0.077 + 0.022*SL	0.099 + 0.017*SL	0.106 + 0.017*SL
	t_{PLH}	0.248	0.214 + 0.017*SL	0.229 + 0.013*SL	0.244 + 0.012*SL
	t_{PHL}	0.312	0.274 + 0.019*SL	0.300 + 0.013*SL	0.347 + 0.010*SL
D to QN	t_R	0.097	0.048 + 0.024*SL	0.041 + 0.026*SL	0.034 + 0.027*SL
	t_F	0.073	0.040 + 0.017*SL	0.038 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.308	0.281 + 0.013*SL	0.284 + 0.012*SL	0.285 + 0.012*SL
	t_{PHL}	0.315	0.292 + 0.011*SL	0.299 + 0.010*SL	0.303 + 0.010*SL
GN to QN	t_R	0.096	0.047 + 0.025*SL	0.040 + 0.026*SL	0.034 + 0.027*SL
	t_F	0.073	0.039 + 0.017*SL	0.038 + 0.017*SL	0.029 + 0.018*SL
	t_{PLH}	0.352	0.326 + 0.013*SL	0.328 + 0.012*SL	0.330 + 0.012*SL
	t_{PHL}	0.336	0.313 + 0.011*SL	0.320 + 0.010*SL	0.323 + 0.010*SL
RN to QN	t_R	0.099	0.051 + 0.024*SL	0.042 + 0.026*SL	0.035 + 0.027*SL
	t_F	0.073	0.039 + 0.017*SL	0.039 + 0.017*SL	0.028 + 0.018*SL
	t_{PLH}	0.383	0.357 + 0.013*SL	0.360 + 0.012*SL	0.361 + 0.012*SL
	t_{PHL}	0.309	0.286 + 0.012*SL	0.293 + 0.010*SL	0.297 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Switching Characteristics

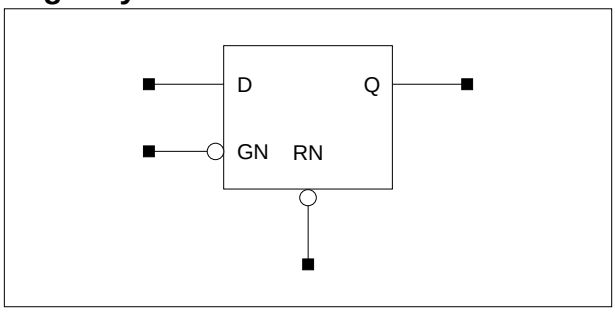
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD6D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.100	0.070 + 0.015*SL	0.078 + 0.013*SL	0.081 + 0.013*SL
	t_F	0.089	0.067 + 0.011*SL	0.076 + 0.009*SL	0.087 + 0.008*SL
	t_{PLH}	0.267	0.244 + 0.012*SL	0.258 + 0.008*SL	0.283 + 0.007*SL
	t_{PHL}	0.251	0.229 + 0.011*SL	0.244 + 0.007*SL	0.275 + 0.005*SL
GN to Q	t_R	0.101	0.074 + 0.014*SL	0.078 + 0.013*SL	0.080 + 0.013*SL
	t_F	0.089	0.067 + 0.011*SL	0.075 + 0.009*SL	0.087 + 0.008*SL
	t_{PLH}	0.294	0.271 + 0.011*SL	0.285 + 0.008*SL	0.310 + 0.007*SL
	t_{PHL}	0.300	0.278 + 0.011*SL	0.294 + 0.007*SL	0.325 + 0.005*SL
RN to Q	t_R	0.101	0.071 + 0.015*SL	0.078 + 0.013*SL	0.081 + 0.013*SL
	t_F	0.090	0.066 + 0.012*SL	0.077 + 0.009*SL	0.096 + 0.008*SL
	t_{PLH}	0.261	0.238 + 0.012*SL	0.252 + 0.008*SL	0.277 + 0.007*SL
	t_{PHL}	0.275	0.253 + 0.011*SL	0.267 + 0.008*SL	0.303 + 0.006*SL
D to QN	t_R	0.073	0.052 + 0.011*SL	0.045 + 0.012*SL	0.034 + 0.013*SL
	t_F	0.060	0.042 + 0.009*SL	0.046 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.358	0.342 + 0.008*SL	0.348 + 0.006*SL	0.351 + 0.006*SL
	t_{PHL}	0.369	0.354 + 0.008*SL	0.362 + 0.005*SL	0.373 + 0.005*SL
GN to QN	t_R	0.073	0.051 + 0.011*SL	0.045 + 0.012*SL	0.033 + 0.013*SL
	t_F	0.060	0.043 + 0.008*SL	0.044 + 0.008*SL	0.037 + 0.009*SL
	t_{PLH}	0.407	0.391 + 0.008*SL	0.398 + 0.006*SL	0.401 + 0.006*SL
	t_{PHL}	0.396	0.381 + 0.008*SL	0.390 + 0.005*SL	0.401 + 0.005*SL
RN to QN	t_R	0.074	0.051 + 0.011*SL	0.047 + 0.012*SL	0.035 + 0.013*SL
	t_F	0.061	0.043 + 0.009*SL	0.047 + 0.008*SL	0.038 + 0.009*SL
	t_{PLH}	0.383	0.367 + 0.008*SL	0.374 + 0.006*SL	0.377 + 0.006*SL
	t_{PHL}	0.363	0.348 + 0.008*SL	0.356 + 0.005*SL	0.367 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 17, *Group3 : 17 < SL

Logic Symbol



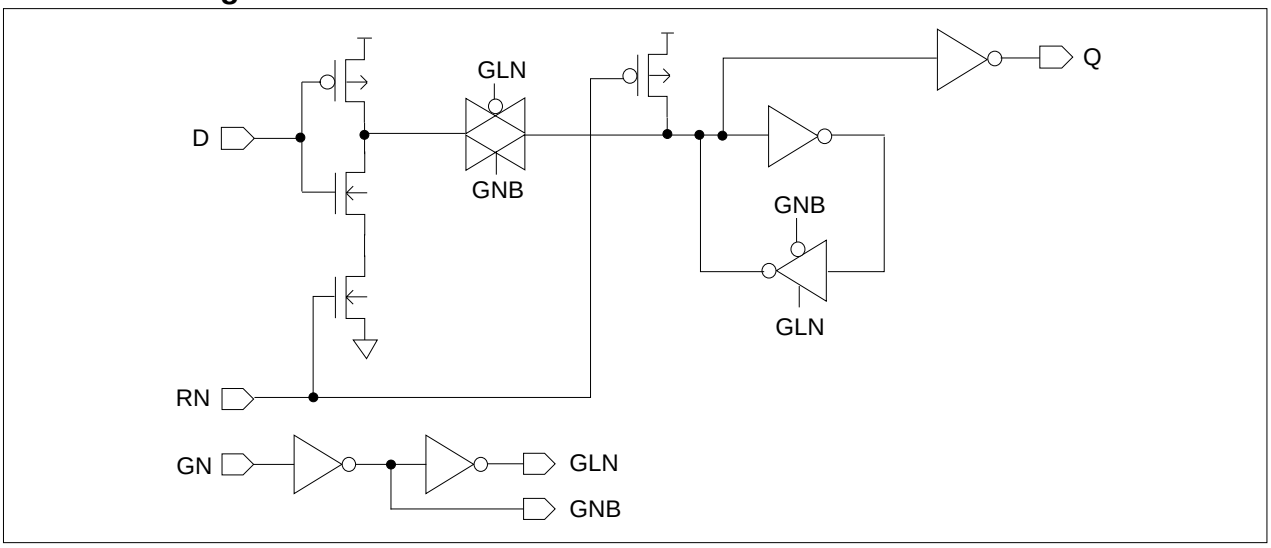
Truth Table

D	GN	RN	Q (n+1)
0	0	1	0
1	0	1	1
x	1	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
LD6Q_LP			*LD6QD2_LP*			*LD6Q_LP*	*LD6QD2_LP*
D	GN	RN	D	GN	RN		
1.1	1.2	0.7	1.1	1.2	0.8	4.00	4.33

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)	
		LD6Q_LP	LD6QD2_LP
Input Setup Time (D to GN)	t_{SU}	0.273	0.301
Input Hold Time (D to GN)	t_{HD}	0.066	0.039
Pulse Width Low (GN)	t_{PWL}	0.262	0.298
Pulse Width Low (RN)	t_{PWL}	0.309	0.302
Recovery Time (RN to GN)	t_{RC}	0.268	0.299
Removal Time (RN to GN)	t_{RM}	0.012	0.000

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

LD6Q_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.117	0.066 + 0.025*SL	0.067 + 0.025*SL	0.052 + 0.026*SL
	t_F	0.097	0.061 + 0.018*SL	0.067 + 0.016*SL	0.056 + 0.017*SL
	t_{PLH}	0.244	0.210 + 0.017*SL	0.225 + 0.013*SL	0.236 + 0.012*SL
	t_{PHL}	0.232	0.202 + 0.015*SL	0.220 + 0.011*SL	0.240 + 0.010*SL
GN to Q	t_R	0.118	0.067 + 0.025*SL	0.066 + 0.025*SL	0.051 + 0.026*SL
	t_F	0.095	0.059 + 0.018*SL	0.065 + 0.017*SL	0.055 + 0.017*SL
	t_{PLH}	0.265	0.231 + 0.017*SL	0.246 + 0.013*SL	0.257 + 0.012*SL
	t_{PHL}	0.277	0.246 + 0.015*SL	0.265 + 0.011*SL	0.285 + 0.010*SL
RN to Q	t_R	0.117	0.067 + 0.025*SL	0.066 + 0.025*SL	0.052 + 0.026*SL
	t_F	0.117	0.074 + 0.021*SL	0.092 + 0.017*SL	0.097 + 0.017*SL
	t_{PLH}	0.237	0.203 + 0.017*SL	0.219 + 0.013*SL	0.230 + 0.012*SL
	t_{PHL}	0.300	0.262 + 0.019*SL	0.288 + 0.012*SL	0.331 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

LD6QD2_LP

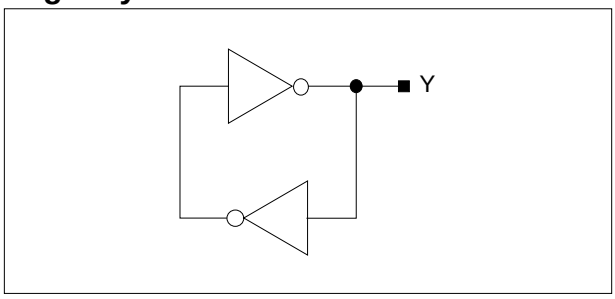
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_R	0.098	0.068 + 0.015*SL	0.077 + 0.013*SL	0.073 + 0.013*SL
	t_F	0.087	0.065 + 0.011*SL	0.075 + 0.009*SL	0.080 + 0.008*SL
	t_{PLH}	0.257	0.235 + 0.011*SL	0.248 + 0.008*SL	0.272 + 0.006*SL
	t_{PHL}	0.242	0.221 + 0.011*SL	0.235 + 0.007*SL	0.265 + 0.005*SL
GN to Q	t_R	0.097	0.068 + 0.015*SL	0.075 + 0.013*SL	0.074 + 0.013*SL
	t_F	0.086	0.061 + 0.012*SL	0.076 + 0.009*SL	0.080 + 0.008*SL
	t_{PLH}	0.283	0.260 + 0.011*SL	0.274 + 0.008*SL	0.298 + 0.006*SL
	t_{PHL}	0.290	0.269 + 0.011*SL	0.284 + 0.007*SL	0.313 + 0.005*SL
RN to Q	t_R	0.098	0.069 + 0.015*SL	0.078 + 0.013*SL	0.074 + 0.013*SL
	t_F	0.089	0.065 + 0.012*SL	0.077 + 0.009*SL	0.090 + 0.008*SL
	t_{PLH}	0.251	0.229 + 0.011*SL	0.242 + 0.008*SL	0.266 + 0.006*SL
	t_{PHL}	0.267	0.245 + 0.011*SL	0.259 + 0.007*SL	0.293 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 17, *Group3 : 17 < SL

Cell List

Cell Name	Function Description
BUSHOLDER	Bus Holder

Logic Symbol



Cell Data

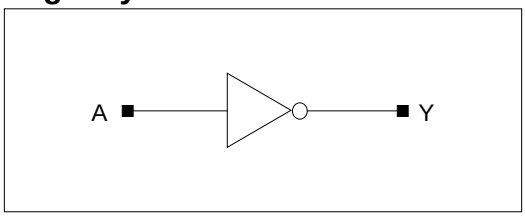
Input Load (SL)	Gate Count
Y	
6.1	1.33

INTERNAL CLOCK DRIVERS

Cell List

Cell Name	Function Description
CK2_LP	Internal Clock Driver CMOS 2mA
CK4_LP	Internal Clock Driver CMOS 4mA
CK6_LP	Internal Clock Driver CMOS 6mA
CK8_LP	Internal Clock Driver CMOS 8mA

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Standard Load (SL)				I/O Slot			
CK2	*CK4*	*CK6*	*CK8*	*CK2*	*CK4*	*CK6*	*CK8*
A	A	A	A				
12.81	12.68	25.81	25.70	1.0	1.0	1.0	1.0

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

CK2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.029 + 0.002*SL	0.027 + 0.002*SL	0.026 + 0.002*SL
	t_F	0.028	0.025 + 0.002*SL	0.023 + 0.002*SL	0.022 + 0.002*SL
	t_{PLH}	0.088	0.087 + 0.001*SL	0.086 + 0.001*SL	0.087 + 0.001*SL
	t_{PHL}	0.088	0.086 + 0.001*SL	0.086 + 0.001*SL	0.087 + 0.001*SL

*Group1 : SL < 275, *Group2 : 275 ≦ SL ≦ 412, *Group3 : 412 < SL

CK4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.036	0.035 + 0.001*SL	0.030 + 0.001*SL	0.029 + 0.001*SL
	t_F	0.031	0.030 + 0.001*SL	0.026 + 0.001*SL	0.024 + 0.001*SL
	t_{PLH}	0.110	0.109 + 0.000*SL	0.109 + 0.000*SL	0.109 + 0.000*SL
	t_{PHL}	0.107	0.106 + 0.000*SL	0.106 + 0.000*SL	0.106 + 0.000*SL

*Group1 : SL < 549, *Group2 : 549 ≦ SL ≦ 823, *Group3 : 823 < SL

CK6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.033	0.031 + 0.001*SL	0.028 + 0.001*SL	0.027 + 0.001*SL
	t_F	0.028	0.026 + 0.001*SL	0.024 + 0.001*SL	0.023 + 0.001*SL
	t_{PLH}	0.099	0.098 + 0.000*SL	0.098 + 0.000*SL	0.098 + 0.000*SL
	t_{PHL}	0.097	0.096 + 0.000*SL	0.097 + 0.000*SL	0.097 + 0.000*SL

*Group1 : SL < 823, *Group2 : 823 ≦ SL ≦ 1235, *Group3 : 1235 < SL

CK8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_R	0.035	0.034 + 0.000*SL	0.030 + 0.000*SL	0.029 + 0.000*SL
	t_F	0.030	0.030 + 0.000*SL	0.026 + 0.000*SL	0.024 + 0.000*SL
	t_{PLH}	0.110	0.109 + 0.000*SL	0.109 + 0.000*SL	0.109 + 0.000*SL
	t_{PHL}	0.106	0.106 + 0.000*SL	0.106 + 0.000*SL	0.106 + 0.000*SL

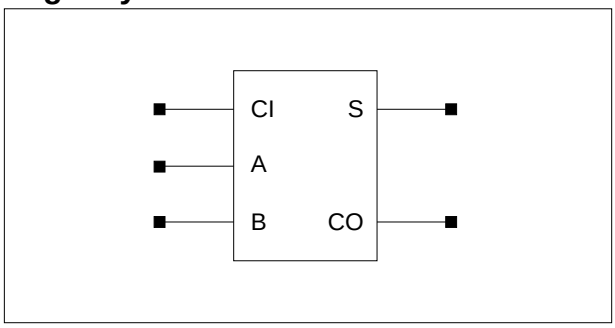
*Group1 : SL < 1096, *Group2 : 1096 ≦ SL ≦ 1644, *Group3 : 1644 < SL

ADDERS

Cell List

Cell Name	Function Description
FA_LP	Full Adder with 1X Drive
FAD2_LP	Full Adder with 2X Drive
HA_LP	Half Adder with 1x Drive
HAD2_LP	Half Adder with 2X Drive

Logic Symbol



Truth Table

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	0	1	1	0
1	0	1	0	1
0	1	0	1	0
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
FA_LP			*FAD2_LP*			*FA_LP*	*FAD2_LP*
CI	A	B	CI	A	B		
1.1	1.1	1.1	1.1	1.1	1.1	7.00	7.67

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FA_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.108	0.060 + 0.024*SL	0.057 + 0.025*SL	0.050 + 0.026*SL
	t_F	0.092	0.056 + 0.018*SL	0.063 + 0.016*SL	0.062 + 0.016*SL
	t_{PLH}	0.386	0.357 + 0.015*SL	0.363 + 0.013*SL	0.367 + 0.012*SL
	t_{PHL}	0.404	0.376 + 0.014*SL	0.386 + 0.011*SL	0.396 + 0.010*SL
B to S	t_R	0.107	0.058 + 0.024*SL	0.056 + 0.025*SL	0.049 + 0.026*SL
	t_F	0.091	0.055 + 0.018*SL	0.061 + 0.016*SL	0.061 + 0.016*SL
	t_{PLH}	0.460	0.431 + 0.015*SL	0.438 + 0.013*SL	0.441 + 0.012*SL
	t_{PHL}	0.463	0.435 + 0.014*SL	0.445 + 0.011*SL	0.455 + 0.010*SL
CI to S	t_R	0.106	0.057 + 0.025*SL	0.055 + 0.025*SL	0.049 + 0.026*SL
	t_F	0.100	0.067 + 0.017*SL	0.070 + 0.016*SL	0.070 + 0.016*SL
	t_{PLH}	0.326	0.297 + 0.014*SL	0.304 + 0.013*SL	0.306 + 0.012*SL
	t_{PHL}	0.316	0.287 + 0.014*SL	0.298 + 0.012*SL	0.309 + 0.010*SL
A to CO	t_R	0.108	0.058 + 0.025*SL	0.057 + 0.025*SL	0.052 + 0.026*SL
	t_F	0.089	0.052 + 0.018*SL	0.056 + 0.017*SL	0.059 + 0.017*SL
	t_{PLH}	0.389	0.358 + 0.015*SL	0.366 + 0.013*SL	0.372 + 0.013*SL
	t_{PHL}	0.403	0.374 + 0.014*SL	0.385 + 0.012*SL	0.395 + 0.010*SL
B to CO	t_R	0.130	0.087 + 0.022*SL	0.078 + 0.024*SL	0.066 + 0.025*SL
	t_F	0.133	0.108 + 0.013*SL	0.104 + 0.014*SL	0.090 + 0.015*SL
	t_{PLH}	0.459	0.428 + 0.015*SL	0.436 + 0.013*SL	0.442 + 0.013*SL
	t_{PHL}	0.467	0.438 + 0.015*SL	0.449 + 0.012*SL	0.459 + 0.011*SL
CI to CO	t_R	0.103	0.053 + 0.025*SL	0.052 + 0.025*SL	0.045 + 0.026*SL
	t_F	0.099	0.063 + 0.018*SL	0.067 + 0.017*SL	0.070 + 0.016*SL
	t_{PLH}	0.223	0.193 + 0.015*SL	0.200 + 0.013*SL	0.204 + 0.013*SL
	t_{PHL}	0.257	0.226 + 0.015*SL	0.240 + 0.012*SL	0.252 + 0.011*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 8, *Group3 : 8 < SL

Switching Characteristics

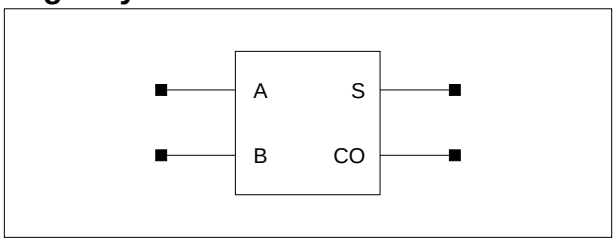
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

FAD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.089	0.064 + 0.013*SL	0.065 + 0.012*SL	0.059 + 0.013*SL
	t_F	0.080	0.059 + 0.010*SL	0.065 + 0.009*SL	0.070 + 0.008*SL
	t_{PLH}	0.396	0.377 + 0.010*SL	0.386 + 0.007*SL	0.398 + 0.006*SL
	t_{PHL}	0.416	0.397 + 0.010*SL	0.408 + 0.007*SL	0.425 + 0.006*SL
B to S	t_R	0.086	0.060 + 0.013*SL	0.064 + 0.012*SL	0.056 + 0.013*SL
	t_F	0.083	0.061 + 0.011*SL	0.071 + 0.009*SL	0.076 + 0.008*SL
	t_{PLH}	0.476	0.457 + 0.010*SL	0.466 + 0.007*SL	0.476 + 0.006*SL
	t_{PHL}	0.480	0.460 + 0.010*SL	0.471 + 0.007*SL	0.490 + 0.006*SL
CI to S	t_R	0.083	0.057 + 0.013*SL	0.061 + 0.012*SL	0.053 + 0.013*SL
	t_F	0.089	0.067 + 0.011*SL	0.077 + 0.008*SL	0.079 + 0.008*SL
	t_{PLH}	0.343	0.324 + 0.009*SL	0.333 + 0.007*SL	0.343 + 0.006*SL
	t_{PHL}	0.336	0.316 + 0.010*SL	0.328 + 0.007*SL	0.347 + 0.006*SL
A to CO	t_R	0.086	0.058 + 0.014*SL	0.062 + 0.013*SL	0.060 + 0.013*SL
	t_F	0.078	0.056 + 0.011*SL	0.063 + 0.009*SL	0.071 + 0.008*SL
	t_{PLH}	0.396	0.376 + 0.010*SL	0.385 + 0.008*SL	0.398 + 0.007*SL
	t_{PHL}	0.415	0.396 + 0.010*SL	0.406 + 0.007*SL	0.424 + 0.006*SL
B to CO	t_R	0.099	0.075 + 0.012*SL	0.075 + 0.012*SL	0.068 + 0.013*SL
	t_F	0.118	0.103 + 0.008*SL	0.106 + 0.007*SL	0.096 + 0.008*SL
	t_{PLH}	0.464	0.444 + 0.010*SL	0.453 + 0.008*SL	0.466 + 0.007*SL
	t_{PHL}	0.476	0.457 + 0.010*SL	0.467 + 0.007*SL	0.485 + 0.006*SL
CI to CO	t_R	0.080	0.054 + 0.013*SL	0.057 + 0.013*SL	0.052 + 0.013*SL
	t_F	0.087	0.067 + 0.010*SL	0.072 + 0.009*SL	0.079 + 0.008*SL
	t_{PLH}	0.225	0.206 + 0.010*SL	0.214 + 0.007*SL	0.225 + 0.006*SL
	t_{PHL}	0.264	0.243 + 0.010*SL	0.256 + 0.007*SL	0.275 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 12, *Group3 : 12 < SL

Logic Symbol



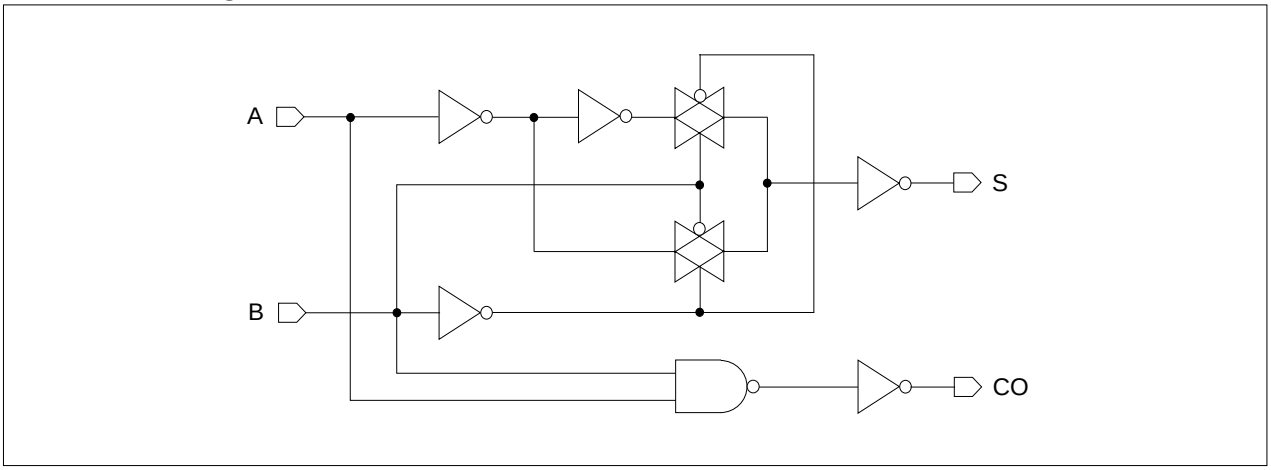
Truth Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Data

Input Load (SL)				Gate Count	
HA_LP		*HAD2_LP*		*HA_LP*	*HAD2_LP*
A	B	A	B		
1.8	2.6	2.2	3.0	4.00	5.00

Schematic Diagram



HA_LP/HAD2_LP

Half Adder with 1X/2X Drive

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

HA_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.114	0.069 + 0.023*SL	0.060 + 0.025*SL	0.055 + 0.026*SL
	t_F	0.102	0.066 + 0.018*SL	0.072 + 0.016*SL	0.068 + 0.017*SL
	t_{PLH}	0.268	0.240 + 0.014*SL	0.245 + 0.013*SL	0.248 + 0.012*SL
	t_{PHL}	0.257	0.228 + 0.014*SL	0.238 + 0.012*SL	0.249 + 0.010*SL
B to S	t_R	0.105	0.056 + 0.024*SL	0.053 + 0.025*SL	0.048 + 0.026*SL
	t_F	0.092	0.055 + 0.018*SL	0.062 + 0.017*SL	0.061 + 0.017*SL
	t_{PLH}	0.216	0.187 + 0.014*SL	0.193 + 0.013*SL	0.197 + 0.012*SL
	t_{PHL}	0.199	0.171 + 0.014*SL	0.182 + 0.011*SL	0.191 + 0.010*SL
A to CO	t_R	0.096	0.047 + 0.025*SL	0.042 + 0.026*SL	0.037 + 0.026*SL
	t_F	0.068	0.035 + 0.017*SL	0.033 + 0.017*SL	0.031 + 0.017*SL
	t_{PLH}	0.154	0.126 + 0.014*SL	0.131 + 0.013*SL	0.133 + 0.013*SL
	t_{PHL}	0.163	0.140 + 0.012*SL	0.145 + 0.010*SL	0.148 + 0.010*SL
B to CO	t_R	0.096	0.045 + 0.025*SL	0.044 + 0.026*SL	0.038 + 0.026*SL
	t_F	0.068	0.033 + 0.017*SL	0.036 + 0.017*SL	0.030 + 0.017*SL
	t_{PLH}	0.157	0.129 + 0.014*SL	0.134 + 0.013*SL	0.136 + 0.013*SL
	t_{PHL}	0.153	0.130 + 0.011*SL	0.136 + 0.010*SL	0.139 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 8, *Group3 : 8 < SL

HAD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_R	0.081	0.055 + 0.013*SL	0.057 + 0.013*SL	0.052 + 0.013*SL
	t_F	0.086	0.065 + 0.011*SL	0.073 + 0.009*SL	0.077 + 0.008*SL
	t_{PLH}	0.269	0.251 + 0.009*SL	0.259 + 0.007*SL	0.268 + 0.006*SL
	t_{PHL}	0.267	0.247 + 0.010*SL	0.259 + 0.007*SL	0.277 + 0.006*SL
B to S	t_R	0.080	0.056 + 0.012*SL	0.055 + 0.013*SL	0.051 + 0.013*SL
	t_F	0.081	0.060 + 0.011*SL	0.067 + 0.009*SL	0.072 + 0.008*SL
	t_{PLH}	0.219	0.200 + 0.009*SL	0.208 + 0.007*SL	0.218 + 0.006*SL
	t_{PHL}	0.211	0.191 + 0.010*SL	0.203 + 0.007*SL	0.221 + 0.006*SL
A to CO	t_R	0.074	0.050 + 0.012*SL	0.048 + 0.013*SL	0.042 + 0.013*SL
	t_F	0.054	0.036 + 0.009*SL	0.039 + 0.008*SL	0.037 + 0.008*SL
	t_{PLH}	0.157	0.140 + 0.009*SL	0.147 + 0.007*SL	0.154 + 0.006*SL
	t_{PHL}	0.166	0.152 + 0.007*SL	0.158 + 0.006*SL	0.166 + 0.005*SL
B to CO	t_R	0.073	0.047 + 0.013*SL	0.048 + 0.013*SL	0.043 + 0.013*SL
	t_F	0.054	0.036 + 0.009*SL	0.040 + 0.008*SL	0.038 + 0.008*SL
	t_{PLH}	0.161	0.144 + 0.009*SL	0.151 + 0.007*SL	0.157 + 0.006*SL
	t_{PHL}	0.158	0.143 + 0.007*SL	0.150 + 0.006*SL	0.158 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 12, *Group3 : 12 < SL

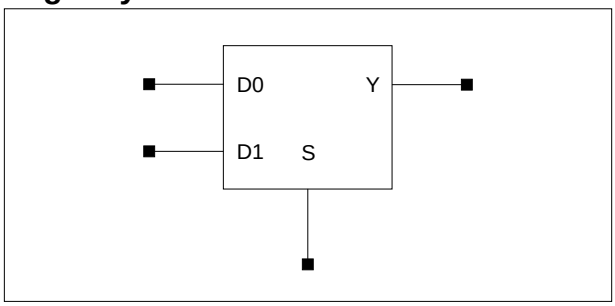
Cell List

Cell Name	Function Description
MX2_LP	2 > 1 Non-Inverting MUX with 1X Drive
MX2D2_LP	2 > 1 Non-Inverting MUX with 2X Drive
MX2D4_LP	2 > 1 Non-Inverting MUX with 4X Drive
MX2I_LP	2 > 1 Inverting MUX with 1X Drive
MX2ID2_LP	2 > 1 Inverting MUX with 2X Drive
MX2ID4_LP	2 > 1 Inverting MUX with 4X Drive
MX2IA_LP	2 > 1 Inverting MUX with Separate S and SN Inputs, 1X Drive
MX2ID2A_LP	2 > 1 Inverting MUX with Separate S and SN Inputs, 2X Drive
MX2ID4A_LP	2 > 1 Inverting MUX with Separate S and SN Inputs, 4X Drive
MX4_LP	4 > 1 Non-Inverting MUX with 1X Drive
MX4D2_LP	4 > 1 Non-Inverting MUX with 2X Drive
MX4D4_LP	4 > 1 Non-Inverting MUX with 4X Drive

MX2_LP/MX2D2_LP/MX2D4_LP

2 > 1 Non-Inverting MUX with 1X/2X/4X Drive

Logic Symbol



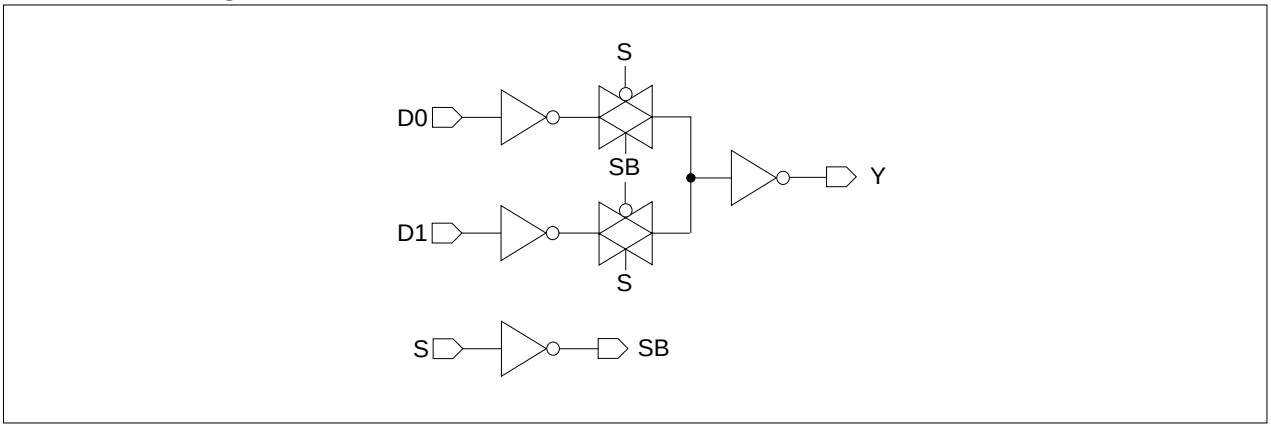
Truth Table

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)								
MX2_LP			*MX2D2_LP*			*MX2D4_LP*		
D0	D1	S	D0	D1	S	D0	D1	S
0.9	0.9	1.6	0.9	0.9	1.6	1.1	1.1	1.7
Gate Count								
MX2_LP			*MX2D2_LP*			*MX2D4_LP*		
2.67			3.00			4.00		

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.104	0.055 + 0.024*SL	0.051 + 0.025*SL	0.047 + 0.026*SL
	t_F	0.096	0.062 + 0.017*SL	0.065 + 0.016*SL	0.065 + 0.016*SL
	t_{PLH}	0.190	0.161 + 0.014*SL	0.167 + 0.013*SL	0.169 + 0.012*SL
	t_{PHL}	0.227	0.199 + 0.014*SL	0.209 + 0.012*SL	0.220 + 0.010*SL
D1 to Y	t_R	0.104	0.056 + 0.024*SL	0.050 + 0.026*SL	0.047 + 0.026*SL
	t_F	0.096	0.062 + 0.017*SL	0.064 + 0.017*SL	0.065 + 0.016*SL
	t_{PLH}	0.190	0.162 + 0.014*SL	0.167 + 0.013*SL	0.170 + 0.012*SL
	t_{PHL}	0.230	0.201 + 0.014*SL	0.212 + 0.012*SL	0.222 + 0.010*SL
S to Y	t_R	0.104	0.055 + 0.025*SL	0.053 + 0.025*SL	0.047 + 0.026*SL
	t_F	0.094	0.060 + 0.017*SL	0.063 + 0.017*SL	0.064 + 0.016*SL
	t_{PLH}	0.212	0.184 + 0.014*SL	0.189 + 0.013*SL	0.191 + 0.012*SL
	t_{PHL}	0.202	0.174 + 0.014*SL	0.184 + 0.011*SL	0.194 + 0.010*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 8, *Group3 : 8 < SL

MX2D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.079	0.055 + 0.012*SL	0.054 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.085	0.064 + 0.011*SL	0.072 + 0.009*SL	0.076 + 0.008*SL
	t_{PLH}	0.192	0.174 + 0.009*SL	0.182 + 0.007*SL	0.191 + 0.006*SL
	t_{PHL}	0.237	0.217 + 0.010*SL	0.228 + 0.007*SL	0.247 + 0.006*SL
D1 to Y	t_R	0.079	0.053 + 0.013*SL	0.055 + 0.013*SL	0.049 + 0.013*SL
	t_F	0.085	0.063 + 0.011*SL	0.073 + 0.009*SL	0.076 + 0.008*SL
	t_{PLH}	0.192	0.174 + 0.009*SL	0.182 + 0.007*SL	0.191 + 0.006*SL
	t_{PHL}	0.239	0.219 + 0.010*SL	0.231 + 0.007*SL	0.249 + 0.006*SL
S to Y	t_R	0.080	0.054 + 0.013*SL	0.056 + 0.012*SL	0.050 + 0.013*SL
	t_F	0.084	0.063 + 0.011*SL	0.071 + 0.009*SL	0.075 + 0.008*SL
	t_{PLH}	0.212	0.194 + 0.009*SL	0.202 + 0.007*SL	0.211 + 0.006*SL
	t_{PHL}	0.215	0.195 + 0.010*SL	0.207 + 0.007*SL	0.225 + 0.006*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 12, *Group3 : 12 < SL

Switching Characteristics

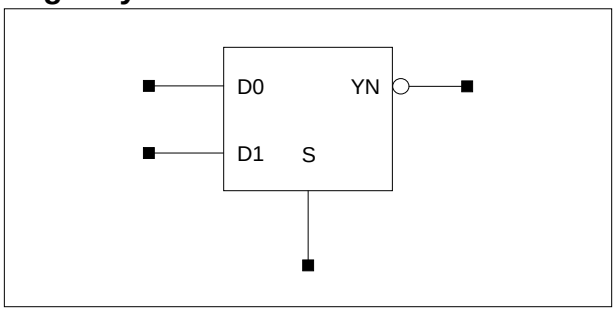
(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX2D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.081	0.067 + 0.007*SL	0.070 + 0.006*SL	0.069 + 0.006*SL
	t_F	0.092	0.079 + 0.007*SL	0.086 + 0.005*SL	0.100 + 0.004*SL
	t_{PLH}	0.222	0.210 + 0.006*SL	0.217 + 0.004*SL	0.236 + 0.003*SL
	t_{PHL}	0.267	0.253 + 0.007*SL	0.263 + 0.005*SL	0.291 + 0.003*SL
D1 to Y	t_R	0.080	0.065 + 0.008*SL	0.070 + 0.006*SL	0.068 + 0.006*SL
	t_F	0.093	0.079 + 0.007*SL	0.088 + 0.005*SL	0.102 + 0.004*SL
	t_{PLH}	0.216	0.204 + 0.006*SL	0.212 + 0.004*SL	0.230 + 0.003*SL
	t_{PHL}	0.265	0.251 + 0.007*SL	0.261 + 0.004*SL	0.290 + 0.003*SL
S to Y	t_R	0.081	0.067 + 0.007*SL	0.070 + 0.006*SL	0.069 + 0.006*SL
	t_F	0.093	0.080 + 0.007*SL	0.088 + 0.005*SL	0.101 + 0.004*SL
	t_{PLH}	0.239	0.227 + 0.006*SL	0.234 + 0.004*SL	0.253 + 0.003*SL
	t_{PHL}	0.252	0.239 + 0.007*SL	0.248 + 0.005*SL	0.277 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≤ SL ≤ 20, *Group3 : 20 < SL

Logic Symbol



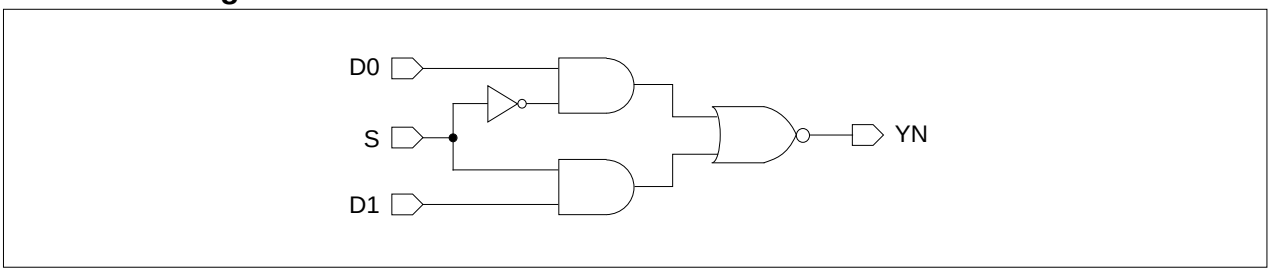
Truth Table

D0	D1	S	YN
0	x	0	1
1	x	0	0
x	0	1	1
x	1	1	0

Cell Data

Input Load (SL)								
MX2I_LP			*MX2ID2_LP*			*MX2ID4_LP*		
D0	D1	S	D0	D1	S	D0	D1	S
1.1	1.2	2.0	2.1	2.1	3.1	0.9	1.0	1.8
Gate Count								
MX2I_LP			*MX2ID2_LP*			*MX2ID4_LP*		
2.33			3.67			4.33		

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX2I_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.244	0.141 + 0.051*SL	0.134 + 0.053*SL	0.126 + 0.054*SL
	t_F	0.150	0.096 + 0.027*SL	0.088 + 0.029*SL	0.079 + 0.030*SL
	t_{PLH}	0.161	0.109 + 0.026*SL	0.109 + 0.026*SL	0.110 + 0.026*SL
	t_{PHL}	0.112	0.077 + 0.017*SL	0.081 + 0.016*SL	0.082 + 0.016*SL
D1 to YN	t_R	0.238	0.132 + 0.053*SL	0.130 + 0.053*SL	0.128 + 0.054*SL
	t_F	0.191	0.134 + 0.029*SL	0.129 + 0.030*SL	0.122 + 0.031*SL
	t_{PLH}	0.211	0.158 + 0.026*SL	0.159 + 0.026*SL	0.160 + 0.026*SL
	t_{PHL}	0.156	0.120 + 0.018*SL	0.123 + 0.017*SL	0.126 + 0.017*SL
S to YN	t_R	0.239	0.133 + 0.053*SL	0.130 + 0.054*SL	0.128 + 0.054*SL
	t_F	0.169	0.109 + 0.030*SL	0.103 + 0.031*SL	0.101 + 0.032*SL
	t_{PLH}	0.197	0.145 + 0.026*SL	0.145 + 0.026*SL	0.146 + 0.026*SL
	t_{PHL}	0.179	0.146 + 0.017*SL	0.147 + 0.016*SL	0.148 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 8, *Group3 : 8 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX2ID2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.196	0.146 + 0.025*SL	0.141 + 0.026*SL	0.130 + 0.027*SL
	t_F	0.127	0.100 + 0.014*SL	0.096 + 0.015*SL	0.085 + 0.016*SL
	t_{PLH}	0.138	0.112 + 0.013*SL	0.111 + 0.013*SL	0.112 + 0.013*SL
	t_{PHL}	0.096	0.077 + 0.010*SL	0.082 + 0.009*SL	0.084 + 0.008*SL
D1 to YN	t_R	0.191	0.138 + 0.026*SL	0.136 + 0.027*SL	0.133 + 0.027*SL
	t_F	0.163	0.136 + 0.014*SL	0.130 + 0.015*SL	0.123 + 0.016*SL
	t_{PLH}	0.185	0.158 + 0.013*SL	0.158 + 0.013*SL	0.160 + 0.013*SL
	t_{PHL}	0.138	0.119 + 0.009*SL	0.121 + 0.009*SL	0.124 + 0.008*SL
S to YN	t_R	0.186	0.132 + 0.027*SL	0.131 + 0.027*SL	0.131 + 0.027*SL
	t_F	0.136	0.105 + 0.015*SL	0.105 + 0.015*SL	0.098 + 0.016*SL
	t_{PLH}	0.189	0.162 + 0.013*SL	0.163 + 0.013*SL	0.164 + 0.013*SL
	t_{PHL}	0.193	0.175 + 0.009*SL	0.177 + 0.009*SL	0.179 + 0.008*SL

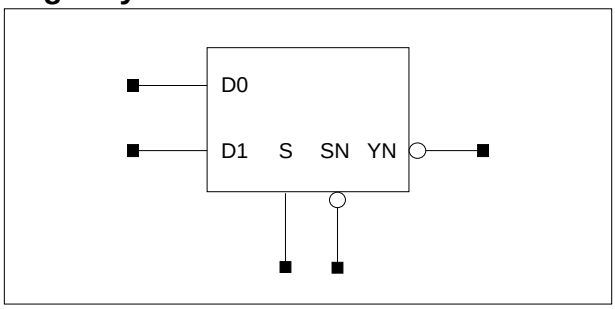
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 12, *Group3 : 12 < SL

MX2ID4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.065	0.052 + 0.006*SL	0.054 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.057	0.046 + 0.005*SL	0.051 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.320	0.310 + 0.005*SL	0.315 + 0.004*SL	0.323 + 0.003*SL
	t_{PHL}	0.265	0.255 + 0.005*SL	0.261 + 0.003*SL	0.275 + 0.003*SL
D1 to YN	t_R	0.065	0.053 + 0.006*SL	0.052 + 0.006*SL	0.043 + 0.006*SL
	t_F	0.058	0.048 + 0.005*SL	0.052 + 0.004*SL	0.052 + 0.004*SL
	t_{PLH}	0.371	0.362 + 0.005*SL	0.367 + 0.004*SL	0.374 + 0.003*SL
	t_{PHL}	0.301	0.292 + 0.005*SL	0.298 + 0.003*SL	0.312 + 0.003*SL
S to YN	t_R	0.065	0.053 + 0.006*SL	0.054 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.057	0.048 + 0.005*SL	0.050 + 0.004*SL	0.051 + 0.004*SL
	t_{PLH}	0.357	0.347 + 0.005*SL	0.353 + 0.004*SL	0.360 + 0.003*SL
	t_{PHL}	0.319	0.310 + 0.005*SL	0.316 + 0.003*SL	0.330 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 20, *Group3 : 20 < SL

Logic Symbol



Truth Table

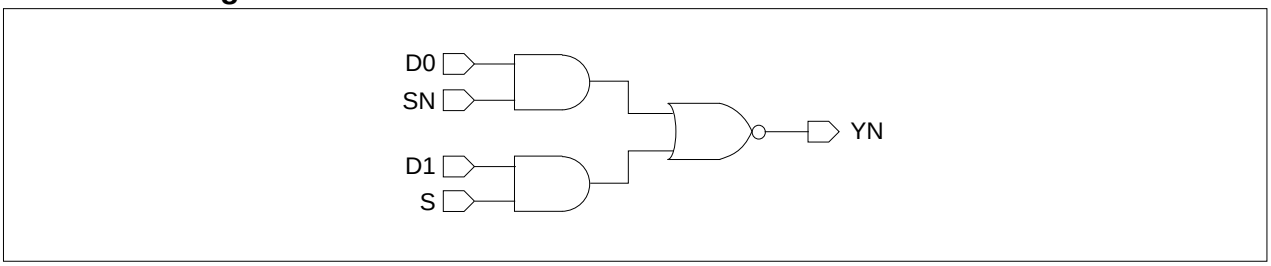
D0	D1	S	SN	YN
0	x	0	1	1
1	x	0	1	0
x	0	1	0	1
x	1	1	0	0

Cell Data

Input Load (SL)											
MX2IA_LP				*MX2ID2A_LP*				*MX2ID4A_LP*			
D0	D1	S	SN	D0	D1	S	SN	D0	D1	S	SN
1.1	1.1	1.1	1.1	2.1	2.1	2.2	2.2	0.9	0.9	0.8	0.9

Gate Count		
MX2IA_LP	*MX2ID2A_LP*	*MX2ID4A_LP*
1.67	3.00	3.67

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX2IA_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.244	0.140 + 0.052*SL	0.133 + 0.054*SL	0.124 + 0.055*SL
	t_F	0.149	0.094 + 0.027*SL	0.086 + 0.029*SL	0.077 + 0.031*SL
	t_{PLH}	0.161	0.107 + 0.027*SL	0.107 + 0.027*SL	0.108 + 0.027*SL
	t_{PHL}	0.111	0.076 + 0.018*SL	0.080 + 0.017*SL	0.081 + 0.016*SL
D1 to YN	t_R	0.241	0.133 + 0.054*SL	0.131 + 0.055*SL	0.129 + 0.055*SL
	t_F	0.180	0.121 + 0.029*SL	0.119 + 0.030*SL	0.114 + 0.031*SL
	t_{PLH}	0.215	0.161 + 0.027*SL	0.162 + 0.027*SL	0.163 + 0.027*SL
	t_{PHL}	0.155	0.120 + 0.018*SL	0.123 + 0.017*SL	0.126 + 0.017*SL
S to YN	t_R	0.256	0.148 + 0.054*SL	0.146 + 0.055*SL	0.144 + 0.055*SL
	t_F	0.177	0.118 + 0.030*SL	0.115 + 0.030*SL	0.113 + 0.031*SL
	t_{PLH}	0.229	0.175 + 0.027*SL	0.176 + 0.027*SL	0.177 + 0.027*SL
	t_{PHL}	0.152	0.117 + 0.018*SL	0.120 + 0.017*SL	0.123 + 0.017*SL
SN to YN	t_R	0.259	0.154 + 0.053*SL	0.147 + 0.054*SL	0.140 + 0.055*SL
	t_F	0.141	0.084 + 0.029*SL	0.078 + 0.030*SL	0.073 + 0.031*SL
	t_{PLH}	0.174	0.121 + 0.027*SL	0.121 + 0.027*SL	0.122 + 0.027*SL
	t_{PHL}	0.108	0.072 + 0.018*SL	0.077 + 0.017*SL	0.078 + 0.016*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 8, *Group3 : 8 < SL

MX2ID2A_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.186	0.135 + 0.025*SL	0.131 + 0.026*SL	0.119 + 0.027*SL
	t_F	0.121	0.094 + 0.014*SL	0.090 + 0.015*SL	0.078 + 0.016*SL
	t_{PLH}	0.132	0.106 + 0.013*SL	0.105 + 0.013*SL	0.106 + 0.013*SL
	t_{PHL}	0.091	0.070 + 0.010*SL	0.077 + 0.009*SL	0.079 + 0.008*SL
D1 to YN	t_R	0.179	0.126 + 0.026*SL	0.123 + 0.027*SL	0.121 + 0.027*SL
	t_F	0.149	0.119 + 0.015*SL	0.119 + 0.015*SL	0.113 + 0.016*SL
	t_{PLH}	0.180	0.153 + 0.014*SL	0.154 + 0.013*SL	0.156 + 0.013*SL
	t_{PHL}	0.136	0.118 + 0.009*SL	0.120 + 0.009*SL	0.123 + 0.009*SL
S to YN	t_R	0.193	0.140 + 0.027*SL	0.138 + 0.027*SL	0.136 + 0.027*SL
	t_F	0.146	0.116 + 0.015*SL	0.114 + 0.015*SL	0.110 + 0.016*SL
	t_{PLH}	0.194	0.167 + 0.014*SL	0.168 + 0.013*SL	0.170 + 0.013*SL
	t_{PHL}	0.133	0.114 + 0.009*SL	0.116 + 0.009*SL	0.121 + 0.009*SL
SN to YN	t_R	0.199	0.147 + 0.026*SL	0.144 + 0.026*SL	0.134 + 0.027*SL
	t_F	0.112	0.083 + 0.015*SL	0.081 + 0.015*SL	0.073 + 0.016*SL
	t_{PLH}	0.145	0.118 + 0.013*SL	0.118 + 0.013*SL	0.119 + 0.013*SL
	t_{PHL}	0.088	0.068 + 0.010*SL	0.073 + 0.009*SL	0.076 + 0.008*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 12, *Group3 : 12 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX2ID4A_LP

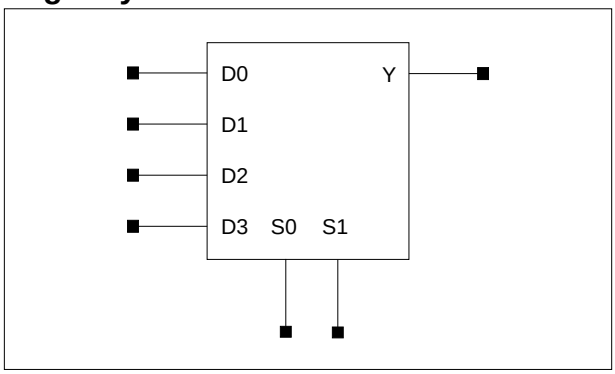
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_R	0.064	0.051 + 0.007*SL	0.053 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.056	0.048 + 0.004*SL	0.048 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.321	0.311 + 0.005*SL	0.316 + 0.004*SL	0.324 + 0.003*SL
	t_{PHL}	0.264	0.255 + 0.005*SL	0.261 + 0.003*SL	0.275 + 0.003*SL
D1 to YN	t_R	0.064	0.053 + 0.006*SL	0.051 + 0.006*SL	0.042 + 0.006*SL
	t_F	0.056	0.046 + 0.005*SL	0.050 + 0.004*SL	0.050 + 0.004*SL
	t_{PLH}	0.368	0.359 + 0.005*SL	0.364 + 0.004*SL	0.371 + 0.003*SL
	t_{PHL}	0.298	0.289 + 0.005*SL	0.295 + 0.003*SL	0.309 + 0.003*SL
S to YN	t_R	0.065	0.053 + 0.006*SL	0.052 + 0.006*SL	0.042 + 0.006*SL
	t_F	0.057	0.048 + 0.005*SL	0.049 + 0.004*SL	0.049 + 0.004*SL
	t_{PLH}	0.389	0.379 + 0.005*SL	0.384 + 0.004*SL	0.392 + 0.003*SL
	t_{PHL}	0.297	0.287 + 0.005*SL	0.293 + 0.003*SL	0.307 + 0.003*SL
SN to YN	t_R	0.064	0.052 + 0.006*SL	0.053 + 0.006*SL	0.044 + 0.006*SL
	t_F	0.056	0.045 + 0.005*SL	0.050 + 0.004*SL	0.050 + 0.004*SL
	t_{PLH}	0.339	0.330 + 0.005*SL	0.335 + 0.004*SL	0.343 + 0.003*SL
	t_{PHL}	0.261	0.251 + 0.005*SL	0.257 + 0.003*SL	0.271 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 20, *Group3 : 20 < SL

MX4_LP/MX4D2_LP/MX4D4_LP

4 > 1 Non-Inverting MUX with 1X/2X/4X Drive

Logic Symbol



Truth Table

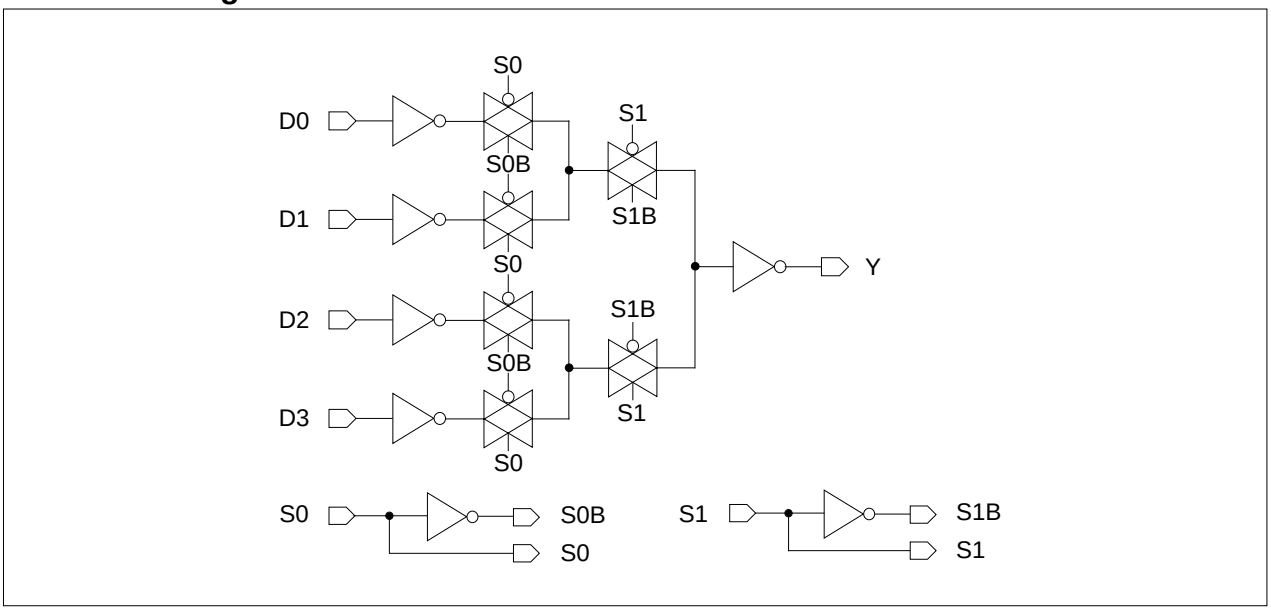
S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)																	
MX4_LP						*MX4D2_LP*						*MX4D4_LP*					
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1
0.9	1.0	0.9	1.0	2.6	1.7	0.9	1.0	0.9	1.0	2.6	1.7	0.9	1.0	0.9	1.0	2.6	1.7

Gate Count		
MX4_LP	*MX4D2_LP*	*MX4D4_LP*
6.33	6.67	7.67

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.122	0.072 + 0.025*SL	0.073 + 0.025*SL	0.069 + 0.025*SL
	t_F	0.139	0.100 + 0.019*SL	0.109 + 0.017*SL	0.114 + 0.016*SL
	t_{PLH}	0.285	0.252 + 0.017*SL	0.262 + 0.014*SL	0.271 + 0.013*SL
	t_{PHL}	0.350	0.313 + 0.019*SL	0.330 + 0.014*SL	0.349 + 0.012*SL
D1 to Y	t_R	0.121	0.071 + 0.025*SL	0.072 + 0.025*SL	0.068 + 0.025*SL
	t_F	0.138	0.100 + 0.019*SL	0.109 + 0.017*SL	0.113 + 0.016*SL
	t_{PLH}	0.280	0.247 + 0.016*SL	0.258 + 0.014*SL	0.266 + 0.013*SL
	t_{PHL}	0.350	0.313 + 0.019*SL	0.330 + 0.014*SL	0.349 + 0.012*SL
D2 to Y	t_R	0.121	0.071 + 0.025*SL	0.071 + 0.025*SL	0.068 + 0.025*SL
	t_F	0.138	0.100 + 0.019*SL	0.108 + 0.017*SL	0.112 + 0.016*SL
	t_{PLH}	0.281	0.248 + 0.016*SL	0.259 + 0.014*SL	0.267 + 0.013*SL
	t_{PHL}	0.351	0.314 + 0.019*SL	0.330 + 0.014*SL	0.349 + 0.012*SL
D3 to Y	t_R	0.121	0.071 + 0.025*SL	0.072 + 0.025*SL	0.067 + 0.025*SL
	t_F	0.138	0.100 + 0.019*SL	0.109 + 0.017*SL	0.111 + 0.016*SL
	t_{PLH}	0.280	0.247 + 0.016*SL	0.258 + 0.014*SL	0.266 + 0.013*SL
	t_{PHL}	0.352	0.315 + 0.019*SL	0.332 + 0.014*SL	0.351 + 0.012*SL
S0 to Y	t_R	0.121	0.071 + 0.025*SL	0.072 + 0.025*SL	0.068 + 0.025*SL
	t_F	0.137	0.099 + 0.019*SL	0.106 + 0.017*SL	0.112 + 0.016*SL
	t_{PLH}	0.313	0.280 + 0.016*SL	0.290 + 0.014*SL	0.298 + 0.013*SL
	t_{PHL}	0.342	0.305 + 0.019*SL	0.322 + 0.014*SL	0.341 + 0.012*SL
S1 to Y	t_R	0.119	0.068 + 0.025*SL	0.069 + 0.025*SL	0.067 + 0.025*SL
	t_F	0.119	0.078 + 0.020*SL	0.087 + 0.018*SL	0.097 + 0.017*SL
	t_{PLH}	0.234	0.201 + 0.016*SL	0.211 + 0.014*SL	0.219 + 0.013*SL
	t_{PHL}	0.231	0.195 + 0.018*SL	0.210 + 0.014*SL	0.227 + 0.012*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 8, *Group3 : 8 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX4D2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.098	0.070 + 0.014*SL	0.077 + 0.013*SL	0.077 + 0.013*SL
	t_F	0.131	0.107 + 0.012*SL	0.118 + 0.009*SL	0.129 + 0.008*SL
	t_{PLH}	0.292	0.270 + 0.011*SL	0.281 + 0.008*SL	0.298 + 0.007*SL
	t_{PHL}	0.367	0.341 + 0.013*SL	0.356 + 0.009*SL	0.384 + 0.007*SL
D1 to Y	t_R	0.097	0.069 + 0.014*SL	0.076 + 0.013*SL	0.075 + 0.013*SL
	t_F	0.131	0.106 + 0.012*SL	0.117 + 0.009*SL	0.129 + 0.008*SL
	t_{PLH}	0.287	0.265 + 0.011*SL	0.276 + 0.008*SL	0.292 + 0.007*SL
	t_{PHL}	0.367	0.341 + 0.013*SL	0.356 + 0.009*SL	0.384 + 0.007*SL
D2 to Y	t_R	0.097	0.068 + 0.014*SL	0.076 + 0.012*SL	0.076 + 0.013*SL
	t_F	0.129	0.105 + 0.012*SL	0.116 + 0.009*SL	0.128 + 0.008*SL
	t_{PLH}	0.288	0.266 + 0.011*SL	0.277 + 0.008*SL	0.294 + 0.007*SL
	t_{PHL}	0.367	0.341 + 0.013*SL	0.357 + 0.009*SL	0.385 + 0.007*SL
D3 to Y	t_R	0.097	0.069 + 0.014*SL	0.076 + 0.012*SL	0.075 + 0.013*SL
	t_F	0.129	0.105 + 0.012*SL	0.116 + 0.009*SL	0.128 + 0.008*SL
	t_{PLH}	0.287	0.265 + 0.011*SL	0.276 + 0.008*SL	0.292 + 0.007*SL
	t_{PHL}	0.369	0.343 + 0.013*SL	0.359 + 0.009*SL	0.386 + 0.007*SL
S0 to Y	t_R	0.099	0.071 + 0.014*SL	0.077 + 0.012*SL	0.076 + 0.013*SL
	t_F	0.130	0.105 + 0.012*SL	0.116 + 0.009*SL	0.129 + 0.008*SL
	t_{PLH}	0.318	0.297 + 0.011*SL	0.308 + 0.008*SL	0.324 + 0.007*SL
	t_{PHL}	0.361	0.335 + 0.013*SL	0.350 + 0.009*SL	0.379 + 0.007*SL
S1 to Y	t_R	0.097	0.068 + 0.014*SL	0.075 + 0.013*SL	0.076 + 0.013*SL
	t_F	0.116	0.091 + 0.013*SL	0.102 + 0.010*SL	0.118 + 0.009*SL
	t_{PLH}	0.238	0.217 + 0.011*SL	0.227 + 0.008*SL	0.244 + 0.007*SL
	t_{PHL}	0.248	0.223 + 0.013*SL	0.238 + 0.009*SL	0.265 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 12, *Group3 : 12 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

MX4D4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_R	0.104	0.087 + 0.008*SL	0.093 + 0.007*SL	0.105 + 0.006*SL
	t_F	0.154	0.139 + 0.008*SL	0.147 + 0.006*SL	0.172 + 0.004*SL
	t_{PLH}	0.339	0.325 + 0.007*SL	0.333 + 0.005*SL	0.360 + 0.004*SL
	t_{PHL}	0.438	0.421 + 0.008*SL	0.431 + 0.006*SL	0.471 + 0.004*SL
D1 to Y	t_R	0.102	0.085 + 0.009*SL	0.092 + 0.007*SL	0.104 + 0.006*SL
	t_F	0.154	0.140 + 0.007*SL	0.146 + 0.006*SL	0.171 + 0.004*SL
	t_{PLH}	0.333	0.319 + 0.007*SL	0.327 + 0.005*SL	0.353 + 0.004*SL
	t_{PHL}	0.437	0.421 + 0.008*SL	0.431 + 0.006*SL	0.470 + 0.004*SL
D2 to Y	t_R	0.104	0.087 + 0.008*SL	0.093 + 0.007*SL	0.104 + 0.006*SL
	t_F	0.152	0.136 + 0.008*SL	0.146 + 0.006*SL	0.170 + 0.004*SL
	t_{PLH}	0.334	0.320 + 0.007*SL	0.328 + 0.005*SL	0.354 + 0.004*SL
	t_{PHL}	0.437	0.421 + 0.008*SL	0.431 + 0.006*SL	0.470 + 0.004*SL
D3 to Y	t_R	0.102	0.085 + 0.009*SL	0.092 + 0.007*SL	0.104 + 0.006*SL
	t_F	0.153	0.137 + 0.008*SL	0.147 + 0.006*SL	0.169 + 0.004*SL
	t_{PLH}	0.333	0.319 + 0.007*SL	0.327 + 0.005*SL	0.353 + 0.004*SL
	t_{PHL}	0.439	0.422 + 0.008*SL	0.433 + 0.006*SL	0.472 + 0.004*SL
S0 to Y	t_R	0.103	0.087 + 0.008*SL	0.092 + 0.007*SL	0.106 + 0.006*SL
	t_F	0.155	0.140 + 0.007*SL	0.147 + 0.006*SL	0.171 + 0.004*SL
	t_{PLH}	0.363	0.349 + 0.007*SL	0.357 + 0.005*SL	0.384 + 0.004*SL
	t_{PHL}	0.434	0.417 + 0.008*SL	0.428 + 0.006*SL	0.467 + 0.004*SL
S1 to Y	t_R	0.103	0.085 + 0.009*SL	0.093 + 0.007*SL	0.105 + 0.006*SL
	t_F	0.150	0.136 + 0.007*SL	0.142 + 0.006*SL	0.166 + 0.004*SL
	t_{PLH}	0.282	0.268 + 0.007*SL	0.276 + 0.005*SL	0.303 + 0.004*SL
	t_{PHL}	0.330	0.313 + 0.009*SL	0.324 + 0.006*SL	0.363 + 0.004*SL

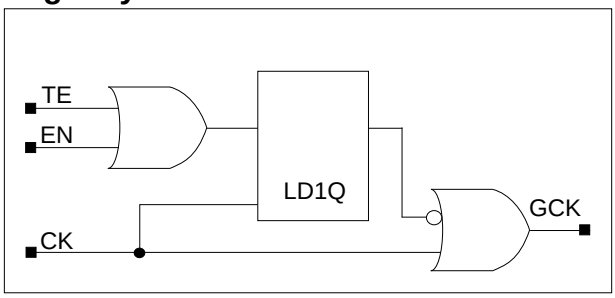
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 20, *Group3 : 20 < SL

INTEGRATED CLOCK-GATING CELLS

Cell List

Cell Name	Function Description
CGLN_LP	Negative edge Triggered Clock-Gating with 1X Drive
CGLND2_LP	Negative edge Triggered Clock-Gating with 2X Drive
CGLND4_LP	Negative edge Triggered Clock-Gating with 4X Drive
CGLP_LP	Positive edge Triggered Clock-Gating with 1X Drive
CGLPD2_LP	Positive edge Triggered Clock-Gating with 2X Drive
CGLPD4_LP	Positive edge Triggered Clock-Gating with 4X Drive

Logic Symbol



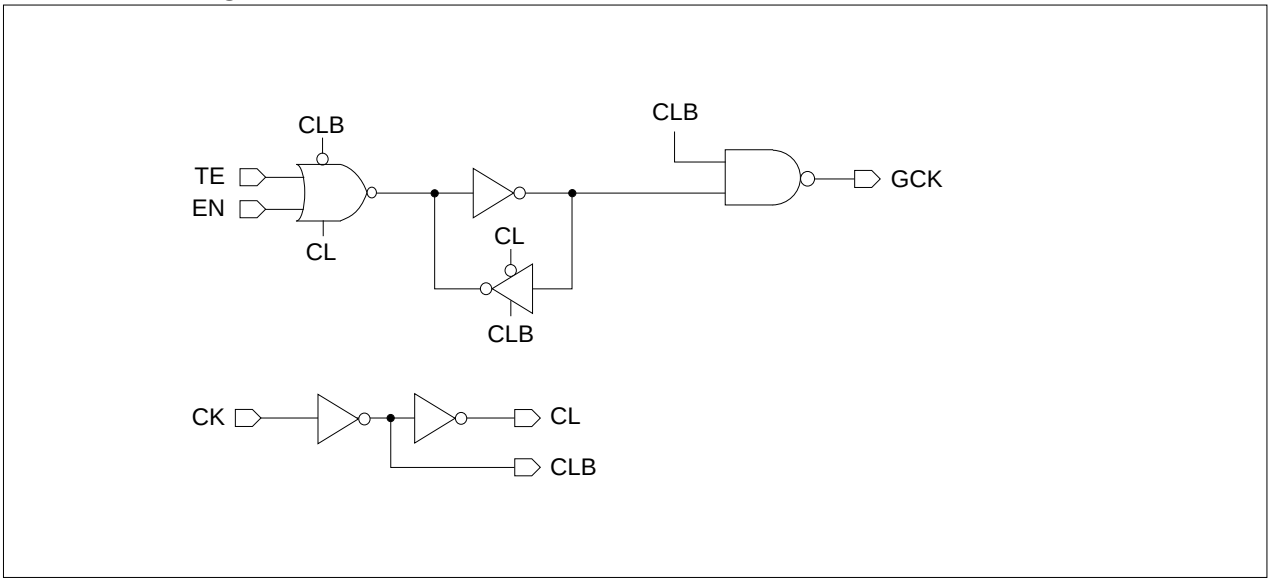
Truth Table

CK	EN	TE	GCK
↓	0	0	1
↓	1	x	0
↓	x	1	0
1	x	x	1

Cell Data

Input Load (SL)								
CGLN_LP			*CGLND2_LP*			*CGLND4_LP*		
EN	CK	TE	EN	CK	TE	EN	CK	TE
1.2	1.0	1.2	1.2	1.0	1.2	1.2	1.0	1.2
Gate Count								
CGLN_LP			*CGLND2_LP*			*CGLND4_LP*		
4.67			5.33			6.67		

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)		
		CGLN_LP	CGLND2_LP	CGLND4_LP
Input Setup Time (EN to CK)	t_{SU}	0.193	0.190	0.182
Input Hold Time (EN to CK)	t_{HD}	0.039	0.055	0.082
Pulse Width High (CK)	t_{PWH}	0.166	0.186	0.218
Input Setup Time (TE to CK)	t_{SU}	0.221	0.218	0.210
Input Hold Time (TE to CK)	t_{HD}	0.027	0.044	0.066

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

CGLN_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.114	0.065 + 0.024*SL	0.059 + 0.026*SL	0.055 + 0.026*SL
	t_F	0.109	0.058 + 0.025*SL	0.058 + 0.025*SL	0.052 + 0.026*SL
	t_{PLH}	0.198	0.170 + 0.014*SL	0.175 + 0.013*SL	0.178 + 0.013*SL
	t_{PHL}	0.185	0.154 + 0.015*SL	0.159 + 0.014*SL	0.162 + 0.014*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 8, *Group3 : 8 < SL

CGLND2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.097	0.074 + 0.012*SL	0.070 + 0.013*SL	0.065 + 0.013*SL
	t_F	0.091	0.065 + 0.013*SL	0.066 + 0.013*SL	0.061 + 0.013*SL
	t_{PLH}	0.206	0.189 + 0.008*SL	0.194 + 0.007*SL	0.202 + 0.006*SL
	t_{PHL}	0.192	0.175 + 0.009*SL	0.180 + 0.008*SL	0.186 + 0.007*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 12, *Group3 : 12 < SL

CGLND4_LP

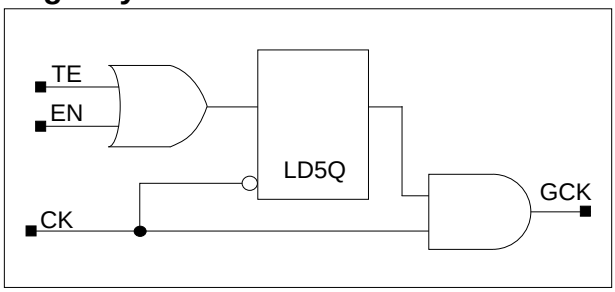
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.097	0.084 + 0.007*SL	0.087 + 0.006*SL	0.081 + 0.006*SL
	t_F	0.090	0.076 + 0.007*SL	0.078 + 0.006*SL	0.076 + 0.006*SL
	t_{PLH}	0.230	0.220 + 0.005*SL	0.225 + 0.004*SL	0.239 + 0.003*SL
	t_{PHL}	0.220	0.210 + 0.005*SL	0.214 + 0.004*SL	0.227 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 20, *Group3 : 20 < SL

CGLP_LP/CGLPD2_LP/CGLPD4_LP

Positive Edge Triggered Clock-Gating with 1X/2X/4X Drive

Logic Symbol



Truth Table

CK	EN	TE	GCK
↑	0	0	0
↑	1	x	1
↑	x	1	1
0	x	x	0

Cell Data

Input Load (SL)								
CGLP_LP			*CGLPD2_LP*			*CGLPD4_LP*		
EN	CK	TE	EN	CK	TE	EN	CK	TE
1.2	0.8	1.1	1.2	0.8	1.1	1.2	0.8	1.1
Gate Count								
CGLP_LP			*CGLPD2_LP*			*CGLPD4_LP*		
5.00			5.33			6.00		

Timing Requirements

(Typical process, 25°C, 1.8V, Unit = ns)

Parameter	Symbol	Value (ns)		
		CGLP_LP	CGLPD2_LP	CGLPD4_LP
Input Setup Time (EN to CK)	t_{SU}	0.141	0.141	0.141
Input Hold Time (EN to CK)	t_{HD}	0.010	0.010	0.010
Pulse Width Low (CK)	t_{PWL}	0.125	0.125	0.125
Input Setup Time (TE to CK)	t_{SU}	0.161	0.161	0.161
Input Hold Time (TE to CK)	t_{HD}	0.010	0.010	0.010

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.19ns, SL: Standard Load)

CGLP_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.098	0.049 + 0.025*SL	0.043 + 0.026*SL	0.041 + 0.026*SL
	t_F	0.070	0.038 + 0.016*SL	0.037 + 0.016*SL	0.033 + 0.017*SL
	t_{PLH}	0.278	0.251 + 0.014*SL	0.255 + 0.013*SL	0.256 + 0.013*SL
	t_{PHL}	0.284	0.261 + 0.011*SL	0.267 + 0.010*SL	0.270 + 0.009*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 8, *Group3 : 8 < SL

CGLPD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.072	0.046 + 0.013*SL	0.048 + 0.013*SL	0.042 + 0.013*SL
	t_F	0.057	0.040 + 0.008*SL	0.041 + 0.008*SL	0.038 + 0.008*SL
	t_{PLH}	0.281	0.264 + 0.009*SL	0.271 + 0.007*SL	0.277 + 0.006*SL
	t_{PHL}	0.291	0.276 + 0.007*SL	0.284 + 0.006*SL	0.292 + 0.005*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 12, *Group3 : 12 < SL

CGLPD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to GCK	t_R	0.097	0.084 + 0.007*SL	0.087 + 0.006*SL	0.081 + 0.006*SL
	t_F	0.090	0.076 + 0.007*SL	0.078 + 0.006*SL	0.076 + 0.006*SL
	t_{PLH}	0.230	0.220 + 0.005*SL	0.225 + 0.004*SL	0.239 + 0.003*SL
	t_{PHL}	0.220	0.210 + 0.005*SL	0.214 + 0.004*SL	0.227 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 20, *Group3 : 20 < SL

Input/Output Cells

4

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OVERVIEW

This chapter describes the Input/Output cells (1.8V/2.5V/ 3.3V drive and 3.3V/5V-tolerant), power/ground and ESD slot cells in the STDL131 library.

The switching characteristics of each cell follow the table of switching characteristics of the cell. The AC characteristics of bi-directional buffers are not included in this data sheet. However, they are the same as the component input and output buffers that make up the bi-directional buffer.

There are many possible combinations of input/output cells, therefore, the naming convention is adopted to help efficiently identify the cell and its characteristics from its name (refer to the naming conventions contained in “Summary Tables” section.)

The “Summary Tables” section shows the list of 1.8V/2.5V/3.3V drive and 3.3V/5V-tolerant I/O cells by category (input, output, bi-directional, etc.). Moreover, each section begins with a table containing a brief functional description of each cell in that section.

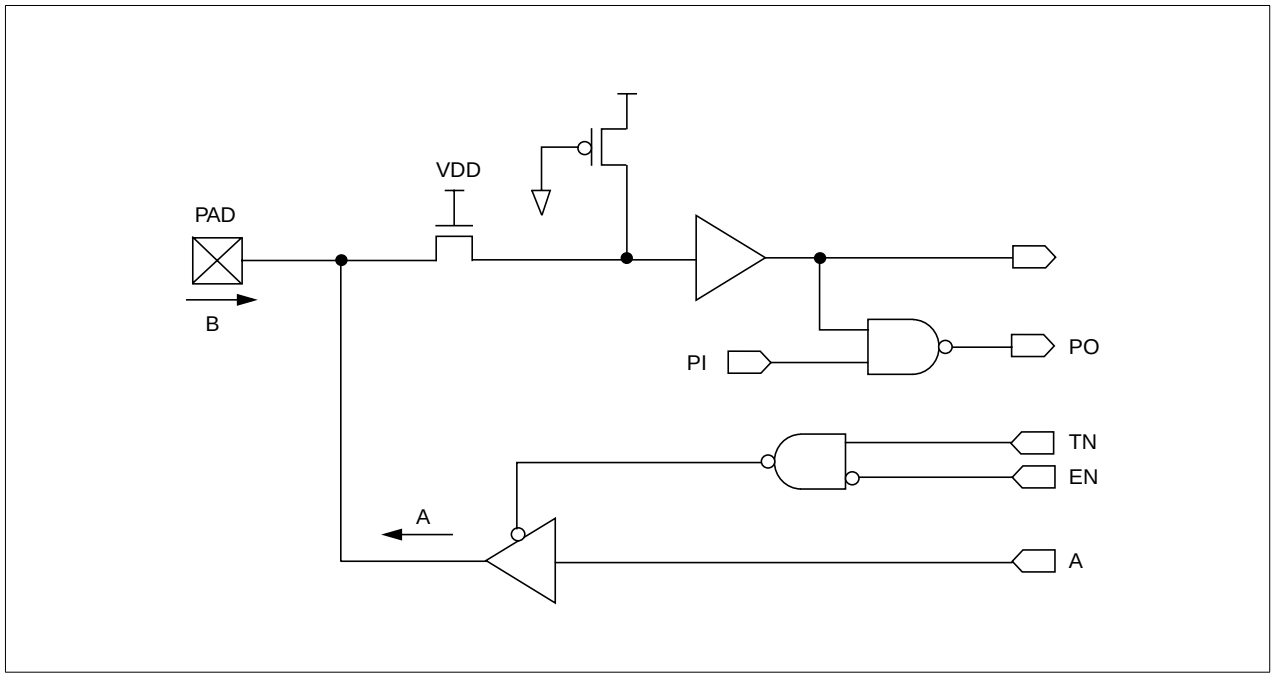


Figure 4-1.

NOTES:

1. As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.
2. When both A and B driving signals do not exist, SEC tolerant IO’s pad voltage goes high state. However, those 3.3V tolerant and 5V tolerant input and bi-directional cells with 100kΩ pull-up resistor have NMOS pass transistor like Figure 4.1. Therefore, pad voltage of 3.3V tolerant IO for 1.8V interface could be 1.0V instead of VDD, and pad voltage of 5V tolerant IO for 3.3V interface could be 1.6V instead of VDD.

SUMMARY TABLES

Input Buffers

Cell Type	Cell Name	Page
CMOS Level	PIC_LP/PICD_LP/PICU_LP PTIC_LP/PTICD_LP/PTICU_LP	4-11
	PMIC_LP/PMICD_LP/PMICU_LP	
	PHIC_LP/PHICD_LP/PHICU_LP PHTIS_LP/PTISD_LP/PTISU_LP	
CMOS Schmitt Trigger Level	PIS_LP/PISD_LP/PISU_LP PTIS_LP/PTISD_LP/PTISU_LP	4-17
	PMIS_LP/PMISD_LP/PMISU_LP	
	PHIS_LP/PHISD_LP/PHISU_LP PHTIS_LP/PHTISD_LP/PMTISU_LP	

<Naming Convention of Input Buffers>

Pvwlab_LP							
v		**w**		**a**		**b**	
None	1.8V interface	None	Normal	C	CMOS level	None	No resistor
M	2.5V interface	T	Tolerant	S	Schmitt trigger level	D	Pull-down resistor
H	3.3V interface					U	Pull-up resistor

Output Buffers

Cell Type	Cell Name	Current Drive (mA)	Page
Normal	POBy_LP	1/2/4/8/12/16/20/24	4-24
	POBySM_LP	4/8/12/16/20/24	
	POBySH_LP	12/16/20/24	
	PMOBy_LP	1/2/4/8/12/16/20/24	
	PMOBySM_LP	4/8/12/16/20/24	
	PMOBySH_LP	12/16/20/24	
	PHOBy_LP	1/2/4/8/12/16/20/24	
	PHOBySM_LP	4/8/12/16/20/24	
	PHOBySH_LP	12/16/20/24	

Cell Type	Cell Name	Current Drive (mA)	Page
Open Drain	PODy_LP	1/2/4/8/12/16/20/24	4-40
	PODySM_LP	4/8/12/16/20/24	
	PODySH_LP	12/16/20/24	
	PMODy_LP	1/2/4/8/12/16/20/24	
	PMODySM_LP	4/8/12/16/20/24	
	PMODySH_LP	12/16/20/24	
	PHODy_LP	1/2/4/8/12/16/20/24	
	PHODySM_LP	4/8/12/16/20/24	
	PHODySH_LP	12/16/20/24	
	PTODy_LP	1/2/4/6	
	PTODySM_LP	4/6	
	PHTODy_LP	1/2/4/6	
	PHTODySM_LP	4/6	
Tri-State	POTy_LP	1/2/4/8/12/16/20/24	4-60
	POTySM_LP	4/8/12/16/20/24	
	POTySH_LP	12/16/20/24	
	PMOTy_LP	1/2/4/8/12/16/20/24	
	PMOTySM_LP	4/8/12/16/20/24	
	PMOTySH_LP	12/16/20/24	
	PHOTy_LP	1/2/4/8/12/16/20/24	
	PHOTySM_LP	4/8/12/16/20/24	
	PHOTySH_LP	12/16/20/24	
	PTOTy_LP	1/2/4/6	
	PTOTySM_LP	4/6	
	PHTOTy_LP	1/2/4/6	
	PHTOTySM_LP	4/6	

<Naming Convention of Output Buffers>

P v O x y z_LP: Normal Output Buffer			
v		**y**	
None	1.8V interface	1	1mA drive
M	2.5V interface	2	2mA drive
H	3.3V interface	4	4mA drive
x		8	8mA drive
B	Normal buffer	12	12mA drive
D	Open drain buffer	16	16mA drive
T	Tri-state buffer	20	20mA drive
z		24	24mA drive

P v O x y z_LP: Normal Output Buffer			
v		**y**	
None	1.8V interface	1	1mA drive
M	2.5V interface	2	2mA drive
H	3.3V interface	4	4mA drive
x		8	8mA drive
B	Normal buffer	12	12mA drive
D	Open drain buffer	16	16mA drive
T	Tri-state buffer	20	20mA drive
None	No slew-rate control		
SM	Medium slew-rate control		
SH	High slew-rate control		
P v T O x y z_LP: Tolerant Output Buffer			
v		**y**	
None	1.8V interface	1	1mA drive
M	2.5V interface	2	2mA drive
H	3.3V interface	4	4mA drive
x		6	6mA drive
D	Open drain buffer		
T	Tri-state buffer		
z			
None	No slew-rate control		
SM	Medium slew-rate control		

Bi-Directional Buffers

Cell Type	Cell Name	Page
Open Drain	PBaDyz_LP/PBaUDyz_LP PTBaDyz_LP/PTBaUDyz_LP	4-95
	PMBaDyz_LP/PMBaUDyz_LP	
	PHBaDyz_LP/PHBaUDyz_LP PHTBaDyz_LP/PHTBaUDyz_LP	
Tri-State	PBaTyz_LP/PBaDTyz_LP/PBaUTyz_LP PTBaTyz_LP/PTBaDTyz_LP/PTBaUTyz_LP	4-95
	PMBaTyz_LP/PMBaDTyz_LP/PMBaUTyz_LP	
	PHBaTyz_LP/PHBaDTyz_LP/PHBaUTyz_LP PHTBaTyz_LP/PHTBaDTyz_LP/PHTBaUTyz_LP	

<Naming Convention of Bi-Directional Buffers>

P w B a b x y z_LP: Normal Bi-Directional Buffer			
w		**y**	
None	1.8V interface	1	1mA drive
M	2.5V interface	2	2mA drive
H	3.3V interface	4	4mA drive
a		8	8mA drive
C	CMOS level	12	12mA drive
S	CMOS Schmitt trigger level	16	16mA drive
b		20	20mA drive
None	No resistor	24	24mA drive
D	Pull-down resistor	**z**	
U	Pull-up resistor	None	No slew-rate control
x		SM	Medium slew-rate control
D	Open drain buffer	SH	High slew-rate control
T	Tri-state buffer		
P w T B a b x y z_LP: Tolerant Bi-Directional Buffer			
w		**x**	
None	1.8V interface	D	Open drain buffer
M	2.5V interface	T	Tri-state buffer
H	3.3V interface	**y**	
a		1	1mA drive
C	CMOS level	2	2mA drive
S	CMOS Schmitt trigger level	4	4mA drive
b		6	6mA drive
None	No resistor		
D	Pull-down resistor		
U	Pull-up resistor		
z			
None	No slew-rate control		
SM	Medium slew-rate control		

Input Clock Drivers with PAD

Cell Type	Cell Name	Cell Name	Page
CMOS Level	PvSCKDCaby_LP	2/4/6/8	4-97
CMOS Schmitt Trigger Level	PvSCKDSaby_LP	2/4/6/8	4-107

<Naming Convention of Input Clock Drivers>

P w T B a b x y z_LP			
a		**y**	
C	CMOS level	2	2mA drive
S	CMOS Schmitt trigger level	4	4mA drive
b		6	6mA drive
None	No resistor	8	8mA drive
D	Pull-down resistor		
U	Pull-up resistor		

Oscillators

Cell Type	Cell Name	Page
3.3V Oscillator	PHSOSCK1_LP/K2_LP/M1_LP/M2_LP/M3_LP	4-119
	PHSOSCK17_LP/K27_LP/M16_LP/M26_LP/M36_LP	4-125
2.5V Oscillator	PMSOSCK1_LP/K2_LP/M1_LP/M2_LP	4-131
1.8V Oscillator	PSOSCK1_LP/K2_LP/M1_LP/M2_LP	4-136

PCI Buffers

Cell Type	Cell Name	Page
5V-tolerant PCI Input	PTIPCI_LP	4-143
5V-tolerant PCI Input	PTOPCI_LP	4-144
5V-tolerant PCI Bi-Directional	PTBPCI_LP	4-146

Power Pads

Descriptions		Cell Name	Supply Voltage	Page
Power for	1.8V Interface Digital I/O	VDD1(I/O/P/IP/OP/T)_LP	1.8V	4-147
	2.5V Interface Digital I/O	VDD1IM_LP	1.8V	
		VDD2(O/P/OP)_LP	2.5V	
	3.3V Interface Digital I/O	VDD1IH_LP	1.8V	
		VDD3(O/P/OP)_LP	3.3V	
	1.8V Interface Analog I/O	VDD1(I/OP/T)_ABB_LP	1.8V	
	2.5V Interface Analog I/O	VDD1IM_ABB_LP	1.8V	
		VDD2(I/OP/T)_ABB_LP	2.5V	
	3.3V Interface Analog I/O	VDD1IH_ABB_LP	1.8V	
		VDD3(I/OP/T)_ABB_LP	3.3V	
Ground for	1.8V Interface Digital I/O	VSS1(I/O/P/IP/OP/T)_LP		
	2.5V Interface Digital I/O	VSS2(I/O/P/IP/OP/T)_LP		
	3.3V Interface Digital I/O	VSS3(I/O/P/IP/OP/T)_LP		
	1.8V Interface Analog I/O	VSS1(I/OP/T)_ABB_LP, VBB1_ABB_LP, VSS1BB_ABB_LP (for Bulk Bias)		4-148
	2.5V Interface Analog I/O	VSS2(I/OP/T)_ABB_LP, VBB2_ABB_LP, VSS2BB_ABB_LP (for Bulk Bias)		
	3.3V Interface Analog I/O	VSS3(I/OP/T)_ABB_LP, VBB3_ABB_LP, VSS3BB_ABB_LP (for Bulk Bias)		

Analog Interface

Cell Type	Cell Name	Page
1.8V Analog Input with Separated Bulk-Bias	PNC_ABB_LP PIA_ABB_LP/PIAR10_ABB_LP/PIAR50_ABB_LP PIC_ABB_LP/PICD_ABB_LP/PICU_ABB_LP/ PICC_ABB_LP/PICEN_ABB_LP PIS_ABB_LP/PISD_ABB_LP/PISU_ABB_LP	4-151
2.5V Analog Input with Separated Bulk-Bias	PMNC_ABB_LP PMIA_ABB_LP/PMIAR10_ABB_LP/PMIAR50_ABB_LP PMIC_ABB_LP/PMICD_ABB_LP/PMICU_ABB_LP/ PMICC_ABB_LP/PMICEN_ABB_LP PMIS_ABB_LP/PMISD_ABB_LP/PMISU_ABB_LP	
3.3V Analog Input with Separated Bulk-Bias	PHNC_ABB_LP PHIA_ABB_LP/PHIAR10_ABB_LP/PHIAR50_ABB_LP PHIC_ABB_LP/PHICD_ABB_LP/PHICU_ABB_LP/ PHICC_ABB_LP/PHICEN_ABB_LP PHIS_ABB_LP/PHISD_ABB_LP/PHISU_ABB_LP	
1.8V Analog Output with Separated Bulk-Bias	POA_ABB_LP/POAR10_ABB_LP/POAR50_ABB_LP POB(1/2/8)_ABB_LP/POT(1/2/4/6/8/10/12/16)_ABB_LP	4-162
1.8V Analog Bi-Directional with Separated Bulk-Bias	PBCT(1/2/4/6)_ABB_LP	
2.5V Analog Output with Separated Bulk-Bias	PMOA_ABB_LP/PMOAR10_ABB_LP/PMOAR50_ABB_LP PMOB(1/2/8)_ABB_LP/PMOT(1/2/4/6/8/10/12/16)_ABB_LP	
2.5V Analog Bi-Directional with Separated Bulk-Bias	PMBCT(1/2/4/6)_ABB_LP	
3.3V Analog Output with Separated Bulk-Bias	PHOA_ABB_LP/PHOAR10_ABB_LP/PHOAR50_ABB_LP PHOB(1/2/8)_ABB_LP/PHOT(1/2/4/6/8/10/12/16)_ABB_LP/ PHOD4SM_ABB_LP	
3.3V Analog Bi-Directional with Separated Bulk-Bias	PHBCT(1/2/4/6)_ABB_LP/PHBSD4SM_ABB_LP	

NOTE: As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.

Slot Cells

Descriptions		Cell Name	Page
ESD Slot Cells for	1.8V Interface I/Os	EV1(I/O/P/OP)_LP, EV1(OP/T)_ABB_LP	4-181
	2.5V Interface I/Os	EV1IM_LP, EV2(O/P/OP)_LP, EV2(OP/T)_ABB_LP	
	3.3V Interface I/Os	EV1IH_LP, EV3(O/P/OP)_LP, EV3(OP/T)_ABB_LP	
Common Slot Cells		EC0C0_LP/EC0C0D_LP EC0CA0_LP/EC0CA0D_LP ECA0CA0_LP/ECA0CA0D_LP ECA0CA0_VBB_LP/ECA0CA0D_VBB_LP	4-182

INPUT BUFFERS

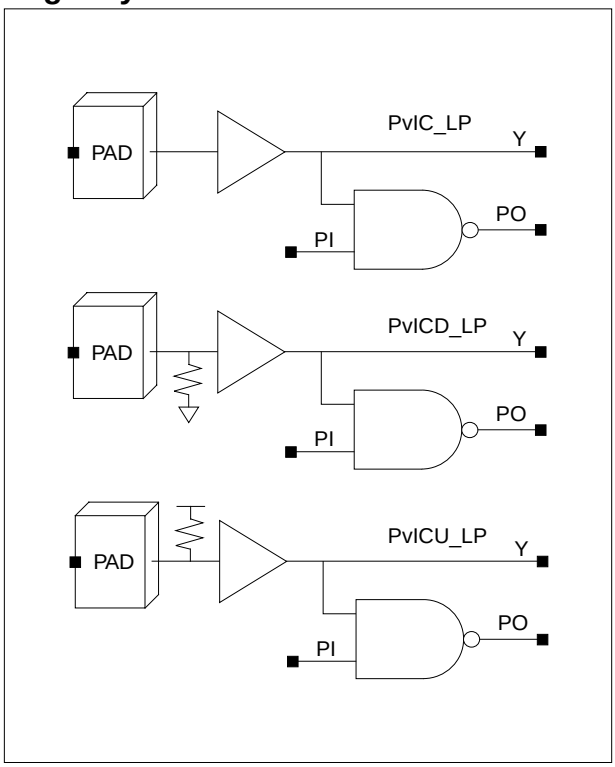
Cell List

Cell Name	Function Description
PIC_LP/PICD_LP/PICU_LP	1.8V Interface CMOS Level Input Buffers
PMIC_LP/PMICD_LP/PMICU_LP	2.5V Interface CMOS Level Input Buffers
PHIC_LP/PHICD_LP/PHICU_LP	3.3V Interface LVCMOS Level Input Buffers
PTIC_LP/PTICD_LP/PTICU_LP	3.3V-tolerant for 1.8V Interface CMOS Level Input Buffers
PHTIC_LP/PHTICD_LP/PHTICU_LP	5V-tolerant for 3.3V Interface LVCMOS Level Input Buffers
PIS_LP/PISD_LP/PISU_LP	1.8V Interface CMOS Schmitt Trigger Level Input Buffers
PMIS_LP/PMISD_LP/PMISU_LP	2.5V Interface CMOS Schmitt Trigger Level Input Buffers
PHIS_LP/PHISD_LP/PHISU_LP	3.3V Interface LVCMOS Schmitt Trigger Level Input Buffers
PTIS_LP/PTISD_LP/PTISU_LP	3.3V-tolerant for 1.8V Interface CMOS Schmitt Trigger Level Input Buffers
PHTIS_LP/PHTISD_LP/PHTISU_LP	5V-tolerant for 3.3V Interface LVCMOS Schmitt Trigger Level Input Buffers

Cell Availability

1.8V Interface		2.5V Interface	3.3V Interface	
1.8V Interface	3.3V-Tolerant		3.3V Interface	5V-Tolerant
PIC_LP PICD_LP PICU_LP	PTIC_LP PTICD_LP PTICU_LP	PMIC_LP PMICD_LP PMICU_LP	PHIC_LP PHICD_LP PHICU_LP	PHTIC_LP PHTICD_LP PHTICU_LP

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PIC_LP/PICD_LP/PICU_LP	3.79
PTIC_LP/PTICD_LP/PTICU_LP	3.79
PMIC_LP/PMICD_LP/PMICU_LP	3.74
PHIC_LP/PHICD_LP/PHICU_LP	3.74
PHTIC_LP/PHTICD_LP/PHTICU_LP	3.74

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PIC_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.120	0.112 + 0.004*SL	0.112 + 0.004*SL	0.110 + 0.004*SL
	t_F	0.106	0.098 + 0.004*SL	0.098 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.388	0.380 + 0.004*SL	0.385 + 0.003*SL	0.402 + 0.002*SL
	t_{PHL}	0.383	0.375 + 0.004*SL	0.379 + 0.003*SL	0.393 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PICD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.119	0.111 + 0.004*SL	0.111 + 0.004*SL	0.109 + 0.004*SL
	t_F	0.107	0.098 + 0.004*SL	0.100 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.412	0.404 + 0.004*SL	0.409 + 0.003*SL	0.426 + 0.002*SL
	t_{PHL}	0.377	0.369 + 0.004*SL	0.373 + 0.003*SL	0.387 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PICU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.110	0.103 + 0.003*SL	0.104 + 0.003*SL	0.101 + 0.003*SL
	t_F	0.092	0.084 + 0.004*SL	0.085 + 0.004*SL	0.082 + 0.004*SL
	t_{PLH}	0.263	0.256 + 0.003*SL	0.260 + 0.002*SL	0.275 + 0.002*SL
	t_{PHL}	0.278	0.271 + 0.003*SL	0.274 + 0.003*SL	0.285 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 28, *Group3 : 28 < SL

NOTE: The delay measure point of CMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PTIC_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.258	0.248 + 0.005*SL	0.252 + 0.004*SL	0.282 + 0.003*SL
	t_F	0.115	0.106 + 0.005*SL	0.108 + 0.004*SL	0.109 + 0.004*SL
	t_{PLH}	1.064	1.053 + 0.005*SL	1.059 + 0.004*SL	1.095 + 0.003*SL
	t_{PHL}	0.657	0.650 + 0.004*SL	0.653 + 0.003*SL	0.666 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PTICD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.258	0.248 + 0.005*SL	0.252 + 0.004*SL	0.281 + 0.003*SL
	t_F	0.117	0.109 + 0.004*SL	0.109 + 0.004*SL	0.111 + 0.004*SL
	t_{PLH}	1.093	1.082 + 0.005*SL	1.088 + 0.004*SL	1.124 + 0.003*SL
	t_{PHL}	0.652	0.645 + 0.004*SL	0.648 + 0.003*SL	0.662 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PTICU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.198	0.189 + 0.005*SL	0.193 + 0.003*SL	0.217 + 0.003*SL
	t_F	0.109	0.100 + 0.005*SL	0.102 + 0.004*SL	0.103 + 0.004*SL
	t_{PLH}	0.864	0.855 + 0.005*SL	0.860 + 0.004*SL	0.893 + 0.002*SL
	t_{PHL}	0.734	0.727 + 0.004*SL	0.730 + 0.003*SL	0.743 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

NOTE: The delay measure point of CMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

Switching Characteristics

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMIC_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.158	0.140 + 0.009*SL	0.139 + 0.009*SL	0.141 + 0.009*SL
	t_F	0.096	0.083 + 0.006*SL	0.084 + 0.006*SL	0.082 + 0.006*SL
	t_{PLH}	0.582	0.568 + 0.007*SL	0.574 + 0.005*SL	0.589 + 0.005*SL
	t_{PHL}	0.720	0.710 + 0.005*SL	0.713 + 0.004*SL	0.725 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PMICD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.158	0.139 + 0.009*SL	0.139 + 0.010*SL	0.141 + 0.009*SL
	t_F	0.096	0.083 + 0.006*SL	0.084 + 0.006*SL	0.082 + 0.006*SL
	t_{PLH}	0.598	0.584 + 0.007*SL	0.590 + 0.005*SL	0.605 + 0.005*SL
	t_{PHL}	0.714	0.704 + 0.005*SL	0.707 + 0.004*SL	0.719 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PMICU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.158	0.140 + 0.009*SL	0.139 + 0.010*SL	0.141 + 0.009*SL
	t_F	0.096	0.083 + 0.006*SL	0.084 + 0.006*SL	0.083 + 0.006*SL
	t_{PLH}	0.573	0.559 + 0.007*SL	0.565 + 0.005*SL	0.580 + 0.005*SL
	t_{PHL}	0.734	0.724 + 0.005*SL	0.728 + 0.004*SL	0.739 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

NOTE: The delay measure point of CMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHIC_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.211	0.199 + 0.006*SL	0.203 + 0.005*SL	0.190 + 0.006*SL
	t_F	0.110	0.097 + 0.006*SL	0.098 + 0.006*SL	0.096 + 0.006*SL
	t_{PLH}	0.436	0.422 + 0.007*SL	0.432 + 0.005*SL	0.471 + 0.003*SL
	t_{PHL}	0.785	0.775 + 0.005*SL	0.778 + 0.004*SL	0.790 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHICD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.211	0.198 + 0.006*SL	0.203 + 0.005*SL	0.191 + 0.006*SL
	t_F	0.110	0.097 + 0.007*SL	0.098 + 0.006*SL	0.096 + 0.006*SL
	t_{PLH}	0.461	0.446 + 0.007*SL	0.457 + 0.005*SL	0.495 + 0.003*SL
	t_{PHL}	0.793	0.783 + 0.005*SL	0.786 + 0.004*SL	0.798 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHICU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.211	0.199 + 0.006*SL	0.203 + 0.005*SL	0.190 + 0.006*SL
	t_F	0.110	0.098 + 0.006*SL	0.098 + 0.006*SL	0.097 + 0.006*SL
	t_{PLH}	0.427	0.412 + 0.007*SL	0.423 + 0.005*SL	0.461 + 0.003*SL
	t_{PHL}	0.800	0.790 + 0.005*SL	0.793 + 0.004*SL	0.805 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

NOTE: The delay measure point of LVCMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

LVCMOS Level Input Buffers

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHTIC_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.211	0.198 + 0.006*SL	0.203 + 0.005*SL	0.190 + 0.006*SL
	t_F	0.110	0.097 + 0.007*SL	0.098 + 0.006*SL	0.097 + 0.006*SL
	t_{PLH}	0.557	0.543 + 0.007*SL	0.553 + 0.005*SL	0.591 + 0.003*SL
	t_{PHL}	0.882	0.872 + 0.005*SL	0.875 + 0.004*SL	0.887 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHTICD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.211	0.198 + 0.006*SL	0.203 + 0.005*SL	0.191 + 0.006*SL
	t_F	0.110	0.097 + 0.006*SL	0.098 + 0.006*SL	0.097 + 0.006*SL
	t_{PLH}	0.585	0.570 + 0.007*SL	0.581 + 0.005*SL	0.619 + 0.003*SL
	t_{PHL}	0.886	0.876 + 0.005*SL	0.879 + 0.004*SL	0.891 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHTICU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.211	0.199 + 0.006*SL	0.203 + 0.005*SL	0.190 + 0.006*SL
	t_F	0.110	0.098 + 0.006*SL	0.098 + 0.006*SL	0.097 + 0.006*SL
	t_{PLH}	0.540	0.525 + 0.007*SL	0.536 + 0.005*SL	0.574 + 0.003*SL
	t_{PHL}	0.961	0.952 + 0.005*SL	0.955 + 0.004*SL	0.967 + 0.004*SL

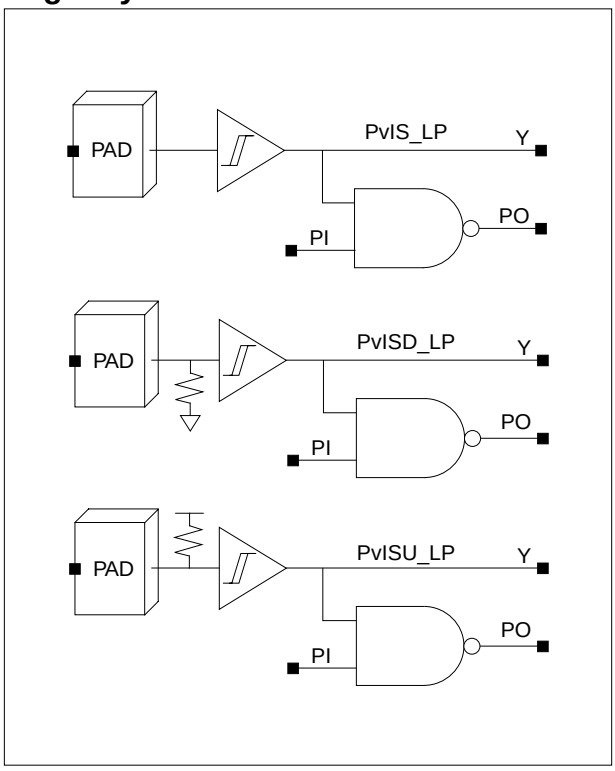
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

NOTE: The delay measure point of LVCMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

Cell Availability

1.8V Interface		2.5V Interface	3.3V Interface	
1.8V Interface	3.3V-Tolerant		3.3V Interface	5V-Tolerant
PIS_LP PISD_LP PISU_LP	PTIS_LP PTISD_LP PTISU_LP	PMIS_LP PMISD_LP PMISU_LP	PHIS_LP PHISD_LP PHISU_LP	PHTIS_LP PHTISD_LP PHTISU_LP

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PIS_LP/PISD_LP/PISU_LP	3.79
PTIS_LP/PTISD_LP/PTISU_LP	3.79
PMIS_LP/PMISD_LP/PMISU_LP	3.74
PHIS_LP/PHISD_LP/PHISU_LP	3.74
PHTIS_LP/PHTISD_LP/PHTISU_LP	3.74

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PIS_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.113	0.103 + 0.005*SL	0.106 + 0.004*SL	0.107 + 0.004*SL
	t_F	0.121	0.112 + 0.005*SL	0.114 + 0.004*SL	0.119 + 0.004*SL
	t_{PLH}	0.653	0.645 + 0.004*SL	0.650 + 0.003*SL	0.667 + 0.002*SL
	t_{PHL}	0.688	0.679 + 0.005*SL	0.684 + 0.003*SL	0.704 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PISD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.115	0.105 + 0.005*SL	0.108 + 0.004*SL	0.109 + 0.004*SL
	t_F	0.124	0.115 + 0.005*SL	0.117 + 0.004*SL	0.121 + 0.004*SL
	t_{PLH}	0.656	0.648 + 0.004*SL	0.652 + 0.003*SL	0.671 + 0.002*SL
	t_{PHL}	0.695	0.686 + 0.005*SL	0.691 + 0.003*SL	0.712 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PISU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.114	0.104 + 0.005*SL	0.106 + 0.004*SL	0.108 + 0.004*SL
	t_F	0.122	0.111 + 0.005*SL	0.115 + 0.004*SL	0.119 + 0.004*SL
	t_{PLH}	0.658	0.650 + 0.004*SL	0.654 + 0.003*SL	0.673 + 0.002*SL
	t_{PHL}	0.703	0.694 + 0.005*SL	0.699 + 0.003*SL	0.720 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PTIS_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.295	0.280 + 0.007*SL	0.286 + 0.006*SL	0.332 + 0.004*SL
	t_F	0.113	0.104 + 0.005*SL	0.106 + 0.004*SL	0.110 + 0.004*SL
	t_{PLH}	2.139	2.124 + 0.008*SL	2.132 + 0.006*SL	2.184 + 0.004*SL
	t_{PHL}	0.835	0.826 + 0.004*SL	0.830 + 0.003*SL	0.850 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PTISD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.295	0.281 + 0.007*SL	0.286 + 0.006*SL	0.332 + 0.004*SL
	t_F	0.115	0.106 + 0.005*SL	0.108 + 0.004*SL	0.112 + 0.004*SL
	t_{PLH}	2.167	2.152 + 0.008*SL	2.160 + 0.006*SL	2.212 + 0.004*SL
	t_{PHL}	0.836	0.827 + 0.004*SL	0.831 + 0.003*SL	0.851 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PTISU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.187	0.174 + 0.006*SL	0.181 + 0.005*SL	0.202 + 0.004*SL
	t_F	0.111	0.101 + 0.005*SL	0.104 + 0.004*SL	0.108 + 0.004*SL
	t_{PLH}	1.154	1.142 + 0.006*SL	1.149 + 0.004*SL	1.187 + 0.003*SL
	t_{PHL}	0.875	0.866 + 0.004*SL	0.871 + 0.003*SL	0.890 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

NOTE: The delay measure point of LVCMOS input buffer is from PAD(VDD/2) to Y(VDD/2).

Switching Characteristics (Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMIS_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.158	0.140 + 0.009*SL	0.139 + 0.009*SL	0.140 + 0.009*SL
	t_F	0.096	0.083 + 0.006*SL	0.084 + 0.006*SL	0.082 + 0.006*SL
	t_{PLH}	0.784	0.770 + 0.007*SL	0.776 + 0.005*SL	0.791 + 0.005*SL
	t_{PHL}	1.141	1.131 + 0.005*SL	1.134 + 0.004*SL	1.146 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PMISD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.158	0.140 + 0.009*SL	0.139 + 0.009*SL	0.141 + 0.009*SL
	t_F	0.096	0.083 + 0.006*SL	0.084 + 0.006*SL	0.082 + 0.006*SL
	t_{PLH}	0.789	0.775 + 0.007*SL	0.781 + 0.005*SL	0.796 + 0.005*SL
	t_{PHL}	1.159	1.149 + 0.005*SL	1.152 + 0.004*SL	1.164 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PMISU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.158	0.140 + 0.009*SL	0.139 + 0.009*SL	0.140 + 0.009*SL
	t_F	0.096	0.083 + 0.006*SL	0.084 + 0.006*SL	0.082 + 0.006*SL
	t_{PLH}	0.787	0.773 + 0.007*SL	0.779 + 0.005*SL	0.794 + 0.005*SL
	t_{PHL}	1.148	1.139 + 0.005*SL	1.142 + 0.004*SL	1.153 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHIS_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.212	0.199 + 0.006*SL	0.203 + 0.005*SL	0.192 + 0.006*SL
	t_F	0.110	0.097 + 0.006*SL	0.098 + 0.006*SL	0.097 + 0.006*SL
	t_{PLH}	0.693	0.678 + 0.007*SL	0.689 + 0.005*SL	0.728 + 0.003*SL
	t_{PHL}	1.127	1.118 + 0.005*SL	1.121 + 0.004*SL	1.133 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHISD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.212	0.200 + 0.006*SL	0.204 + 0.005*SL	0.192 + 0.006*SL
	t_F	0.110	0.098 + 0.006*SL	0.098 + 0.006*SL	0.097 + 0.006*SL
	t_{PLH}	0.706	0.691 + 0.008*SL	0.702 + 0.005*SL	0.740 + 0.003*SL
	t_{PHL}	1.158	1.148 + 0.005*SL	1.151 + 0.004*SL	1.163 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHISU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.212	0.199 + 0.006*SL	0.204 + 0.005*SL	0.191 + 0.006*SL
	t_F	0.110	0.098 + 0.006*SL	0.098 + 0.006*SL	0.097 + 0.006*SL
	t_{PLH}	0.698	0.684 + 0.007*SL	0.694 + 0.005*SL	0.733 + 0.003*SL
	t_{PHL}	1.156	1.147 + 0.005*SL	1.150 + 0.004*SL	1.161 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHTIS_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.210	0.197 + 0.006*SL	0.202 + 0.005*SL	0.190 + 0.006*SL
	t_F	0.110	0.098 + 0.006*SL	0.098 + 0.006*SL	0.096 + 0.006*SL
	t_{PLH}	1.001	0.986 + 0.007*SL	0.997 + 0.005*SL	1.035 + 0.003*SL
	t_{PHL}	1.264	1.254 + 0.005*SL	1.257 + 0.004*SL	1.269 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHTISD_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.210	0.198 + 0.006*SL	0.201 + 0.005*SL	0.190 + 0.006*SL
	t_F	0.110	0.097 + 0.006*SL	0.098 + 0.006*SL	0.097 + 0.006*SL
	t_{PLH}	0.993	0.978 + 0.007*SL	0.989 + 0.005*SL	1.027 + 0.003*SL
	t_{PHL}	1.297	1.287 + 0.005*SL	1.290 + 0.004*SL	1.302 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHTISU_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.211	0.198 + 0.006*SL	0.203 + 0.005*SL	0.190 + 0.006*SL
	t_F	0.110	0.097 + 0.006*SL	0.098 + 0.006*SL	0.096 + 0.006*SL
	t_{PLH}	1.077	1.062 + 0.007*SL	1.072 + 0.005*SL	1.111 + 0.003*SL
	t_{PHL}	1.291	1.281 + 0.005*SL	1.284 + 0.004*SL	1.296 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Cell List

Cell Name	Function Description
POB(1/2/4/8/12/16/20/24)_LP	1.8V CMOS Normal Output Buffers
POB(4/8/12/16/20/24)SM_LP	1.8V CMOS Normal Output Buffers with Medium Slew-Rate
POB(12/16/20/24)SH_LP	1.8V CMOS Normal Output Buffers with High Slew-Rate
PMOB(1/2/4/8/12/16/20/24)_LP	2.5V CMOS Normal Output Buffers
PMOB(4/8/12/16/20/24)SM_LP	2.5V CMOS Normal Output Buffers with Medium Slew-Rate
PMOB(12/16/20/24)SH_LP	2.5V CMOS Normal Output Buffers with High Slew-Rate
PHOB(1/2/4/8/12/16/20/24)_LP	3.3V LVCMOS Normal Output Buffers
PHOB(4/8/12/16/20/24)SM_LP	3.3V LVCMOS Normal Output Buffers with Medium Slew-Rate
PHOB(12/16/20/24)SH_LP	3.3V LVCMOS Normal Output Buffers with High Slew-Rate
POD(1/2/4/8/12/16/20/24)_LP	1.8V CMOS Open Drain Output Buffers
POD(4/8/12/16/20/24)SM_LP	1.8V CMOS Open Drain Output Buffers with Medium Slew-Rate
POD(12/16/20/24)SH_LP	1.8V CMOS Open Drain Output Buffers with High Slew-Rate
PMOD(1/2/4/8/12/16/20/24)_LP	2.5V CMOS Open Drain Output Buffers
PMOD(4/8/12/16/20/24)SM_LP	2.5V CMOS Open Drain Output Buffers with Medium Slew-Rate
PMOD(12/16/20/24)SH_LP	2.5V CMOS Open Drain Output Buffers with High Slew-Rate
PHOD(1/2/4/8/12/16/20/24)_LP	3.3V LVCMOS Open Drain Output Buffers
PHOD(4/8/12/16/20/24)SM_LP	3.3V LVCMOS Open Drain Output Buffers with Medium Slew-Rate
PHOD(12/16/20/24)SH_LP	3.3V LVCMOS Open Drain Output Buffers with High Slew-Rate
POT(1/2/4/8/12/16/20/24)_LP	1.8V CMOS Tri-State Output Buffers
POT(4/8/12/16/20/24)SM_LP	1.8V CMOS Tri-State Output Buffers with Medium Slew-Rate
POT(12/16/20/24)SH_LP	1.8V CMOS Tri-State Output Buffers with High Slew-Rate
PMOT(1/2/4/8/12/16/20/24)_LP	2.5V CMOS Tri-State Output Buffers
PMOT(4/8/12/16/20/24)SM_LP	2.5V CMOS Tri-State Output Buffers with Medium Slew-Rate
PMO(12/16/20/24)SH_LP	2.5V CMOS Tri-State Output Buffers with High Slew-Rate
PHOT(1/2/4/8/12/16/20/24)_LP	3.3V LVCMOS Tri-State Output Buffers
PHOT(4/8/12/16/20/24)SM_LP	3.3V LVCMOS Tri-State Output Buffers with Medium Slew-Rate
PHOT(12/16/20/24)SH_LP	3.3V LVCMOS Tri-State Output Buffers with High Slew-Rate
PTOD(1/2/4/6)_LP	3.3V-Tolerant for 1.8V Interface Open Drain Output Buffers
PTOD(4/6)SM_LP	3.3V-Tolerant for 1.8V Interface Open Drain Output with Medium Slew-Rate
PHTOD(1/2/4/6)_LP	5V-Tolerant for 3.3V Interface Open Drain Output Buffers
PHTOD(4/6)SM_LP	5V-Tolerant for 3.3V Interface Open Drain Output with Medium Slew-Rate
PTOT(1/2/4/6)_LP	3.3V-Tolerant for 1.8V Interface Tri-State Output Buffers
PTOT(4/6)SM_LP	3.3V-Tolerant for 1.8V Interface Tri-State Output with Medium Slew-Rate
PHTOT(1/2/4/6)_LP	5V-Tolerant for 3.3V Interface Tri-State Output Buffers
PHTOT(4/6)SM_LP	5V-Tolerant for 3.3V Interface Tri-State Output with Medium Slew-Rate

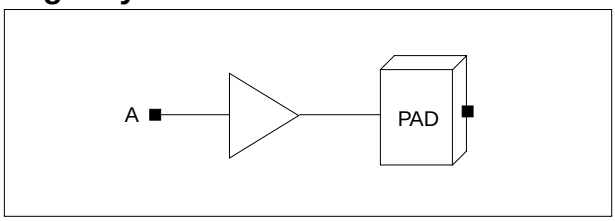
PvOByz_LP

Normal Output Buffers

Cell Availability

1.8V Interface	2.5V Interface	3.3V Interface
POB(1/2/4/8/12/16/20/24)_LP POB(4/8/12/16/20/24)SM_LP POB(12/16/20/24)SH_LP	PMOB(1/2/4/8/12/16/20/24)_LP PMOB(4/8/12/16/20/24)SM_LP PMOB(12/16/20/24)SH_LP	PHOB(1/2/4/8/12/16/20/24)_LP PHOB(4/8/12/16/20/24)SM_LP PHOB(12/16/20/24)SH_LP

Logic Symbol



Truth Table

A	PAD
0	0
1	1

Standard Load (SL)

Cell Name	A
POB(1/2/4)_LP	8.16
POB(8/12/16/20/24)_LP	15.95
POB4SM_LP	21.70
POB(8/12/20/24)SM_LP	27.85
POB12SH_LP	29.05
POB16SH_LP	28.75
POB20SH_LP	26.74
POB24SH_LP	25.81
PMOB(1/2/4/8/12/16/20/24)_LP	6.32
PMOB(4/8/12/16/20/24)SM_LP	6.32
PMOB(12/16/20/24)SH_LP	6.32
PHOB(1/2/4/8/12/16/20/24)_LP	7.50
PHOB(4/8/12/16/20/24)SM_LP	7.50
PHOB(12/16/20/24)SH_LP	7.50

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	20.443	1.560 + 0.378*CL	1.557 + 0.378*CL	1.554 + 0.378*CL
	t_F	23.041	1.821 + 0.424*CL	1.811 + 0.425*CL	1.811 + 0.425*CL
	t_{PLH}	9.823	0.909 + 0.178*CL	0.909 + 0.178*CL	0.909 + 0.178*CL
	t_{PHL}	12.404	1.537 + 0.217*CL	1.538 + 0.217*CL	1.535 + 0.217*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.759	1.082 + 0.254*CL	1.081 + 0.254*CL	1.078 + 0.254*CL
	t_F	12.208	0.976 + 0.225*CL	0.968 + 0.225*CL	0.962 + 0.225*CL
	t_{PLH}	6.850	0.782 + 0.121*CL	0.783 + 0.121*CL	0.782 + 0.121*CL
	t_{PHL}	6.741	0.889 + 0.117*CL	0.890 + 0.117*CL	0.890 + 0.117*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.856	0.564 + 0.126*CL	0.563 + 0.126*CL	0.562 + 0.126*CL
	t_F	6.905	0.572 + 0.127*CL	0.570 + 0.127*CL	0.562 + 0.127*CL
	t_{PLH}	3.495	0.520 + 0.059*CL	0.523 + 0.059*CL	0.524 + 0.059*CL
	t_{PHL}	3.980	0.564 + 0.068*CL	0.566 + 0.068*CL	0.567 + 0.068*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.439	0.292 + 0.063*CL	0.292 + 0.063*CL	0.292 + 0.063*CL
	t_F	3.462	0.295 + 0.063*CL	0.294 + 0.063*CL	0.293 + 0.063*CL
	t_{PLH}	1.877	0.388 + 0.030*CL	0.389 + 0.030*CL	0.391 + 0.030*CL
	t_{PHL}	2.109	0.400 + 0.034*CL	0.402 + 0.034*CL	0.403 + 0.034*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOByz_LP

Normal Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.312	0.226 + 0.042*CL	0.217 + 0.042*CL	0.213 + 0.042*CL
	t_F	2.326	0.229 + 0.042*CL	0.218 + 0.042*CL	0.214 + 0.042*CL
	t_{PLH}	1.427	0.433 + 0.020*CL	0.434 + 0.020*CL	0.436 + 0.020*CL
	t_{PHL}	1.558	0.426 + 0.023*CL	0.423 + 0.023*CL	0.421 + 0.023*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.762	0.219 + 0.031*CL	0.202 + 0.031*CL	0.190 + 0.031*CL
	t_F	1.773	0.236 + 0.031*CL	0.209 + 0.031*CL	0.190 + 0.032*CL
	t_{PLH}	1.246	0.497 + 0.015*CL	0.500 + 0.015*CL	0.502 + 0.015*CL
	t_{PHL}	1.323	0.487 + 0.017*CL	0.478 + 0.017*CL	0.472 + 0.017*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.447	0.235 + 0.024*CL	0.214 + 0.025*CL	0.197 + 0.025*CL
	t_F	1.464	0.274 + 0.024*CL	0.237 + 0.025*CL	0.209 + 0.025*CL
	t_{PLH}	1.171	0.564 + 0.012*CL	0.572 + 0.012*CL	0.575 + 0.012*CL
	t_{PHL}	1.217	0.565 + 0.013*CL	0.551 + 0.013*CL	0.541 + 0.013*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.252	0.261 + 0.020*CL	0.240 + 0.020*CL	0.220 + 0.021*CL
	t_F	1.280	0.333 + 0.019*CL	0.285 + 0.020*CL	0.249 + 0.020*CL
	t_{PLH}	1.147	0.628 + 0.010*CL	0.644 + 0.010*CL	0.651 + 0.010*CL
	t_{PHL}	1.178	0.646 + 0.011*CL	0.635 + 0.011*CL	0.621 + 0.011*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.988	0.791 + 0.124*CL	0.743 + 0.125*CL	0.711 + 0.125*CL
	t_F	6.965	0.672 + 0.126*CL	0.654 + 0.126*CL	0.635 + 0.126*CL
	t_{PLH}	4.341	1.344 + 0.060*CL	1.360 + 0.060*CL	1.369 + 0.059*CL
	t_{PHL}	4.400	0.970 + 0.069*CL	0.983 + 0.068*CL	0.987 + 0.068*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.896	0.908 + 0.060*CL	0.875 + 0.060*CL	0.827 + 0.061*CL
	t_F	3.917	0.908 + 0.060*CL	0.889 + 0.061*CL	0.842 + 0.061*CL
	t_{PLH}	3.542	1.903 + 0.033*CL	1.990 + 0.031*CL	2.044 + 0.030*CL
	t_{PHL}	3.748	1.860 + 0.038*CL	1.964 + 0.036*CL	2.030 + 0.035*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.480	1.427 + 0.041*CL	1.505 + 0.040*CL	1.532 + 0.039*CL
	t_F	3.470	1.344 + 0.043*CL	1.452 + 0.040*CL	1.516 + 0.039*CL
	t_{PLH}	3.829	2.316 + 0.030*CL	2.534 + 0.026*CL	2.715 + 0.023*CL
	t_{PHL}	3.992	2.343 + 0.033*CL	2.545 + 0.029*CL	2.725 + 0.027*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOByz_LP

Normal Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.716	1.167 + 0.031*CL	1.222 + 0.030*CL	1.246 + 0.030*CL
	t_F	2.738	1.072 + 0.033*CL	1.182 + 0.031*CL	1.254 + 0.030*CL
	t_{PLH}	3.607	2.451 + 0.023*CL	2.616 + 0.020*CL	2.754 + 0.018*CL
	t_{PHL}	3.816	2.519 + 0.026*CL	2.680 + 0.023*CL	2.827 + 0.021*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.837	1.435 + 0.028*CL	1.551 + 0.026*CL	1.638 + 0.025*CL
	t_F	2.849	1.330 + 0.030*CL	1.466 + 0.028*CL	1.590 + 0.026*CL
	t_{PLH}	3.897	2.674 + 0.024*CL	2.886 + 0.020*CL	3.074 + 0.018*CL
	t_{PHL}	4.158	2.918 + 0.025*CL	3.053 + 0.022*CL	3.208 + 0.020*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.628	1.444 + 0.024*CL	1.543 + 0.022*CL	1.622 + 0.021*CL
	t_F	2.495	1.179 + 0.026*CL	1.306 + 0.024*CL	1.425 + 0.022*CL
	t_{PLH}	4.180	3.071 + 0.022*CL	3.275 + 0.018*CL	3.455 + 0.016*CL
	t_{PHL}	4.298	3.214 + 0.022*CL	3.340 + 0.019*CL	3.483 + 0.017*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POB12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.447	2.138 + 0.046*CL	2.319 + 0.043*CL	2.451 + 0.041*CL
	t_F	4.666	2.243 + 0.048*CL	2.490 + 0.044*CL	2.671 + 0.041*CL
	t_{PLH}	5.768	3.835 + 0.039*CL	4.154 + 0.032*CL	4.439 + 0.028*CL
	t_{PHL}	6.337	4.040 + 0.046*CL	4.436 + 0.038*CL	4.790 + 0.033*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.415	2.256 + 0.043*CL	2.551 + 0.037*CL	2.789 + 0.034*CL
	t_F	4.854	2.569 + 0.046*CL	2.958 + 0.038*CL	3.260 + 0.034*CL
	t_{PLH}	5.780	3.849 + 0.039*CL	4.193 + 0.032*CL	4.514 + 0.027*CL
	t_{PHL}	6.301	3.861 + 0.049*CL	4.360 + 0.039*CL	4.815 + 0.033*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.988	2.226 + 0.035*CL	2.475 + 0.030*CL	2.677 + 0.028*CL
	t_F	4.163	2.199 + 0.039*CL	2.487 + 0.034*CL	2.737 + 0.030*CL
	t_{PLH}	5.592	3.867 + 0.035*CL	4.202 + 0.028*CL	4.508 + 0.024*CL
	t_{PHL}	6.298	4.274 + 0.040*CL	4.655 + 0.033*CL	5.002 + 0.028*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.865	2.137 + 0.035*CL	2.425 + 0.029*CL	2.663 + 0.026*CL
	t_F	4.135	2.249 + 0.038*CL	2.570 + 0.031*CL	2.845 + 0.028*CL
	t_{PLH}	5.525	3.871 + 0.033*CL	4.192 + 0.027*CL	4.485 + 0.023*CL
	t_{PHL}	6.320	4.315 + 0.040*CL	4.708 + 0.032*CL	5.070 + 0.027*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOByz_LP

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOB1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	26.044	1.406 + 0.493*CL	1.404 + 0.493*CL	1.398 + 0.493*CL
	t_F	22.782	1.225 + 0.431*CL	1.216 + 0.431*CL	1.213 + 0.431*CL
	t_{PLH}	13.018	1.146 + 0.237*CL	1.146 + 0.237*CL	1.149 + 0.237*CL
	t_{PHL}	12.365	1.227 + 0.223*CL	1.227 + 0.223*CL	1.227 + 0.223*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.053	0.741 + 0.246*CL	0.737 + 0.246*CL	0.731 + 0.246*CL
	t_F	12.991	0.714 + 0.246*CL	0.707 + 0.246*CL	0.704 + 0.246*CL
	t_{PLH}	6.857	0.919 + 0.119*CL	0.921 + 0.119*CL	0.920 + 0.119*CL
	t_{PHL}	7.485	0.887 + 0.132*CL	0.886 + 0.132*CL	0.885 + 0.132*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.856	0.564 + 0.126*CL	0.563 + 0.126*CL	0.562 + 0.126*CL
	t_F	6.905	0.572 + 0.127*CL	0.570 + 0.127*CL	0.562 + 0.127*CL
	t_{PLH}	3.495	0.520 + 0.059*CL	0.523 + 0.059*CL	0.524 + 0.059*CL
	t_{PHL}	3.980	0.564 + 0.068*CL	0.566 + 0.068*CL	0.567 + 0.068*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.404	0.424 + 0.060*CL	0.377 + 0.061*CL	0.340 + 0.061*CL
	t_F	3.312	0.321 + 0.060*CL	0.273 + 0.061*CL	0.239 + 0.061*CL
	t_{PLH}	2.745	1.241 + 0.030*CL	1.254 + 0.030*CL	1.260 + 0.030*CL
	t_{PHL}	2.513	0.904 + 0.032*CL	0.885 + 0.033*CL	0.873 + 0.033*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOB12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.288	0.311 + 0.040*CL	0.276 + 0.040*CL	0.248 + 0.041*CL
	t_F	2.273	0.344 + 0.039*CL	0.289 + 0.040*CL	0.245 + 0.040*CL
	t_{PLH}	2.057	1.052 + 0.020*CL	1.062 + 0.020*CL	1.067 + 0.020*CL
	t_{PHL}	2.029	0.992 + 0.021*CL	0.964 + 0.021*CL	0.945 + 0.022*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.828	0.392 + 0.029*CL	0.357 + 0.029*CL	0.321 + 0.030*CL
	t_F	1.841	0.501 + 0.027*CL	0.416 + 0.029*CL	0.356 + 0.029*CL
	t_{PLH}	1.983	1.190 + 0.016*CL	1.225 + 0.015*CL	1.239 + 0.015*CL
	t_{PHL}	1.922	1.164 + 0.015*CL	1.158 + 0.015*CL	1.126 + 0.016*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.597	0.473 + 0.022*CL	0.450 + 0.023*CL	0.417 + 0.023*CL
	t_F	1.659	0.715 + 0.019*CL	0.592 + 0.021*CL	0.507 + 0.022*CL
	t_{PLH}	1.998	1.305 + 0.014*CL	1.364 + 0.013*CL	1.400 + 0.012*CL
	t_{PHL}	1.933	1.290 + 0.013*CL	1.328 + 0.012*CL	1.332 + 0.012*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.477	0.544 + 0.019*CL	0.540 + 0.019*CL	0.516 + 0.019*CL
	t_F	1.619	0.894 + 0.014*CL	0.820 + 0.016*CL	0.696 + 0.018*CL
	t_{PLH}	2.050	1.405 + 0.013*CL	1.483 + 0.011*CL	1.538 + 0.011*CL
	t_{PHL}	1.986	1.411 + 0.011*CL	1.457 + 0.011*CL	1.494 + 0.010*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOByz_LP

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOB4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.909	0.995 + 0.118*CL	0.908 + 0.120*CL	0.820 + 0.121*CL
	t_F	6.764	0.811 + 0.119*CL	0.746 + 0.120*CL	0.679 + 0.121*CL
	t_{PLH}	5.535	2.469 + 0.061*CL	2.537 + 0.060*CL	2.567 + 0.060*CL
	t_{PHL}	5.378	2.004 + 0.067*CL	2.060 + 0.066*CL	2.081 + 0.066*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.352	1.445 + 0.058*CL	1.474 + 0.058*CL	1.447 + 0.058*CL
	t_F	3.928	1.002 + 0.059*CL	1.014 + 0.058*CL	0.985 + 0.059*CL
	t_{PLH}	5.123	3.174 + 0.039*CL	3.396 + 0.035*CL	3.565 + 0.032*CL
	t_{PHL}	4.373	2.423 + 0.039*CL	2.578 + 0.036*CL	2.690 + 0.034*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.254	1.259 + 0.040*CL	1.324 + 0.039*CL	1.342 + 0.038*CL
	t_F	2.979	0.994 + 0.040*CL	1.045 + 0.039*CL	1.054 + 0.039*CL
	t_{PLH}	4.125	2.660 + 0.029*CL	2.861 + 0.025*CL	3.026 + 0.023*CL
	t_{PHL}	3.804	2.332 + 0.029*CL	2.498 + 0.026*CL	2.631 + 0.024*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOB16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.076	1.447 + 0.033*CL	1.561 + 0.030*CL	1.638 + 0.029*CL
	t_F	2.709	1.110 + 0.032*CL	1.212 + 0.030*CL	1.273 + 0.029*CL
	t_{PLH}	4.374	2.988 + 0.028*CL	3.222 + 0.023*CL	3.423 + 0.020*CL
	t_{PHL}	3.936	2.605 + 0.027*CL	2.796 + 0.023*CL	2.961 + 0.021*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.710	1.418 + 0.026*CL	1.516 + 0.024*CL	1.579 + 0.023*CL
	t_F	2.476	1.083 + 0.028*CL	1.211 + 0.025*CL	1.304 + 0.024*CL
	t_{PLH}	4.285	3.077 + 0.024*CL	3.304 + 0.020*CL	3.497 + 0.017*CL
	t_{PHL}	3.906	2.707 + 0.024*CL	2.889 + 0.020*CL	3.053 + 0.018*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.749	1.570 + 0.024*CL	1.692 + 0.021*CL	1.783 + 0.020*CL
	t_F	2.422	1.140 + 0.026*CL	1.287 + 0.023*CL	1.407 + 0.021*CL
	t_{PLH}	4.564	3.346 + 0.024*CL	3.594 + 0.019*CL	3.809 + 0.017*CL
	t_{PHL}	4.106	2.959 + 0.023*CL	3.141 + 0.019*CL	3.312 + 0.017*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOByz_LP

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOB12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.610	2.137 + 0.049*CL	2.434 + 0.044*CL	2.659 + 0.041*CL
	t_F	4.117	1.780 + 0.047*CL	2.034 + 0.042*CL	2.203 + 0.039*CL
	t_{PLH}	5.767	3.612 + 0.043*CL	3.989 + 0.036*CL	4.348 + 0.031*CL
	t_{PHL}	4.934	2.840 + 0.042*CL	3.197 + 0.035*CL	3.510 + 0.031*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.692	2.338 + 0.047*CL	2.776 + 0.038*CL	3.123 + 0.034*CL
	t_F	4.029	1.903 + 0.043*CL	2.260 + 0.035*CL	2.540 + 0.032*CL
	t_{PLH}	5.694	3.453 + 0.045*CL	3.888 + 0.036*CL	4.322 + 0.030*CL
	t_{PHL}	5.141	3.156 + 0.040*CL	3.520 + 0.032*CL	3.866 + 0.028*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.156	2.144 + 0.040*CL	2.430 + 0.035*CL	2.701 + 0.031*CL
	t_F	3.674	1.576 + 0.042*CL	1.970 + 0.034*CL	2.281 + 0.030*CL
	t_{PLH}	5.946	4.088 + 0.037*CL	4.429 + 0.030*CL	4.735 + 0.026*CL
	t_{PHL}	5.132	3.325 + 0.036*CL	3.622 + 0.030*CL	3.914 + 0.026*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.528	1.730 + 0.036*CL	2.018 + 0.030*CL	2.291 + 0.027*CL
	t_F	3.348	1.485 + 0.037*CL	1.796 + 0.031*CL	2.090 + 0.027*CL
	t_{PLH}	4.702	3.120 + 0.032*CL	3.391 + 0.026*CL	3.646 + 0.023*CL
	t_{PHL}	4.346	2.964 + 0.028*CL	3.064 + 0.026*CL	3.239 + 0.023*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOB1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	36.042	2.067 + 0.679*CL	2.066 + 0.680*CL	2.066 + 0.680*CL
	t_F	26.591	1.534 + 0.501*CL	1.529 + 0.501*CL	1.526 + 0.501*CL
	t_{PLH}	17.533	1.568 + 0.319*CL	1.567 + 0.319*CL	1.567 + 0.319*CL
	t_{PHL}	13.360	1.408 + 0.239*CL	1.410 + 0.239*CL	1.410 + 0.239*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	18.642	1.107 + 0.351*CL	1.104 + 0.351*CL	1.101 + 0.351*CL
	t_F	14.643	0.869 + 0.275*CL	0.865 + 0.276*CL	0.862 + 0.276*CL
	t_{PLH}	9.279	0.994 + 0.166*CL	0.994 + 0.166*CL	0.993 + 0.166*CL
	t_{PHL}	7.823	0.963 + 0.137*CL	0.963 + 0.137*CL	0.963 + 0.137*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	9.348	0.584 + 0.175*CL	0.583 + 0.175*CL	0.579 + 0.175*CL
	t_F	8.642	0.523 + 0.162*CL	0.521 + 0.162*CL	0.516 + 0.162*CL
	t_{PLH}	4.974	0.828 + 0.083*CL	0.830 + 0.083*CL	0.831 + 0.083*CL
	t_{PHL}	5.043	0.738 + 0.086*CL	0.738 + 0.086*CL	0.737 + 0.086*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.709	0.343 + 0.087*CL	0.331 + 0.088*CL	0.326 + 0.088*CL
	t_F	4.338	0.281 + 0.081*CL	0.280 + 0.081*CL	0.278 + 0.081*CL
	t_{PLH}	2.950	0.872 + 0.042*CL	0.875 + 0.041*CL	0.878 + 0.041*CL
	t_{PHL}	2.821	0.675 + 0.043*CL	0.673 + 0.043*CL	0.671 + 0.043*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOByz_LP

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOB12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.195	0.333 + 0.057*CL	0.301 + 0.058*CL	0.278 + 0.058*CL
	t_F	2.913	0.248 + 0.053*CL	0.217 + 0.054*CL	0.205 + 0.054*CL
	t_{PLH}	2.387	0.996 + 0.028*CL	1.002 + 0.028*CL	1.005 + 0.028*CL
	t_{PHL}	2.136	0.724 + 0.028*CL	0.713 + 0.028*CL	0.706 + 0.029*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.387	0.234 + 0.043*CL	0.212 + 0.044*CL	0.197 + 0.044*CL
	t_F	2.201	0.226 + 0.040*CL	0.193 + 0.040*CL	0.169 + 0.040*CL
	t_{PLH}	1.899	0.858 + 0.021*CL	0.861 + 0.021*CL	0.862 + 0.021*CL
	t_{PHL}	1.802	0.753 + 0.021*CL	0.740 + 0.021*CL	0.731 + 0.021*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.950	0.257 + 0.034*CL	0.228 + 0.034*CL	0.205 + 0.035*CL
	t_F	1.804	0.267 + 0.031*CL	0.226 + 0.032*CL	0.193 + 0.032*CL
	t_{PLH}	1.765	0.926 + 0.017*CL	0.932 + 0.017*CL	0.935 + 0.017*CL
	t_{PHL}	1.643	0.828 + 0.016*CL	0.807 + 0.017*CL	0.792 + 0.017*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.675	0.290 + 0.028*CL	0.260 + 0.028*CL	0.232 + 0.029*CL
	t_F	1.562	0.330 + 0.025*CL	0.276 + 0.026*CL	0.237 + 0.026*CL
	t_{PLH}	1.702	0.989 + 0.014*CL	1.005 + 0.014*CL	1.011 + 0.014*CL
	t_{PHL}	1.567	0.905 + 0.013*CL	0.886 + 0.014*CL	0.866 + 0.014*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOB4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	9.495	0.873 + 0.172*CL	0.804 + 0.174*CL	0.749 + 0.175*CL
	t_F	8.701	0.636 + 0.161*CL	0.610 + 0.162*CL	0.584 + 0.162*CL
	t_{PLH}	5.929	1.758 + 0.083*CL	1.779 + 0.083*CL	1.787 + 0.083*CL
	t_{PHL}	5.563	1.249 + 0.086*CL	1.256 + 0.086*CL	1.257 + 0.086*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.075	0.886 + 0.084*CL	0.840 + 0.085*CL	0.778 + 0.086*CL
	t_F	4.463	0.497 + 0.079*CL	0.462 + 0.080*CL	0.428 + 0.080*CL
	t_{PLH}	4.111	1.904 + 0.044*CL	1.993 + 0.042*CL	2.038 + 0.042*CL
	t_{PHL}	3.544	1.351 + 0.044*CL	1.379 + 0.043*CL	1.392 + 0.043*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.046	1.292 + 0.055*CL	1.341 + 0.054*CL	1.311 + 0.054*CL
	t_F	3.230	0.643 + 0.052*CL	0.632 + 0.052*CL	0.597 + 0.052*CL
	t_{PLH}	3.812	2.008 + 0.036*CL	2.233 + 0.032*CL	2.388 + 0.030*CL
	t_{PHL}	3.136	1.566 + 0.031*CL	1.646 + 0.030*CL	1.696 + 0.029*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOByz_LP

Normal Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOB16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.372	1.169 + 0.044*CL	1.292 + 0.042*CL	1.342 + 0.041*CL
	t_F	2.745	0.790 + 0.039*CL	0.826 + 0.038*CL	0.822 + 0.038*CL
	t_{PLH}	3.411	1.850 + 0.031*CL	2.086 + 0.027*CL	2.278 + 0.024*CL
	t_{PHL}	3.045	1.710 + 0.027*CL	1.836 + 0.024*CL	1.932 + 0.023*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.827	1.037 + 0.036*CL	1.125 + 0.034*CL	1.175 + 0.033*CL
	t_F	2.317	0.724 + 0.032*CL	0.769 + 0.031*CL	0.781 + 0.031*CL
	t_{PLH}	3.366	2.090 + 0.026*CL	2.259 + 0.022*CL	2.410 + 0.020*CL
	t_{PHL}	2.890	1.758 + 0.023*CL	1.876 + 0.020*CL	1.973 + 0.019*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.687	1.101 + 0.032*CL	1.212 + 0.029*CL	1.294 + 0.028*CL
	t_F	2.078	0.726 + 0.027*CL	0.780 + 0.026*CL	0.806 + 0.026*CL
	t_{PLH}	3.422	2.210 + 0.024*CL	2.387 + 0.021*CL	2.547 + 0.019*CL
	t_{PHL}	2.873	1.865 + 0.020*CL	1.984 + 0.018*CL	2.085 + 0.016*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOB12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.285	1.450 + 0.057*CL	1.516 + 0.055*CL	1.528 + 0.055*CL
	t_F	3.745	1.112 + 0.053*CL	1.167 + 0.052*CL	1.178 + 0.051*CL
	t_{PLH}	4.898	2.988 + 0.038*CL	3.216 + 0.034*CL	3.403 + 0.031*CL
	t_{PHL}	4.179	2.325 + 0.037*CL	2.513 + 0.033*CL	2.664 + 0.031*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.684	1.512 + 0.043*CL	1.601 + 0.042*CL	1.643 + 0.041*CL
	t_F	3.085	1.062 + 0.040*CL	1.134 + 0.039*CL	1.171 + 0.039*CL
	t_{PLH}	4.812	3.170 + 0.033*CL	3.412 + 0.028*CL	3.615 + 0.025*CL
	t_{PHL}	3.978	2.450 + 0.031*CL	2.634 + 0.027*CL	2.790 + 0.025*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.616	1.721 + 0.038*CL	1.860 + 0.035*CL	1.960 + 0.034*CL
	t_F	3.022	1.277 + 0.035*CL	1.389 + 0.033*CL	1.472 + 0.032*CL
	t_{PLH}	5.105	3.485 + 0.032*CL	3.763 + 0.027*CL	4.003 + 0.024*CL
	t_{PHL}	4.227	2.735 + 0.030*CL	2.956 + 0.025*CL	3.151 + 0.023*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.590	1.876 + 0.034*CL	2.039 + 0.031*CL	2.168 + 0.029*CL
	t_F	3.093	1.479 + 0.032*CL	1.634 + 0.029*CL	1.756 + 0.028*CL
	t_{PLH}	5.337	3.734 + 0.032*CL	4.033 + 0.026*CL	4.296 + 0.023*CL
	t_{PHL}	4.413	2.892 + 0.030*CL	3.150 + 0.025*CL	3.380 + 0.022*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

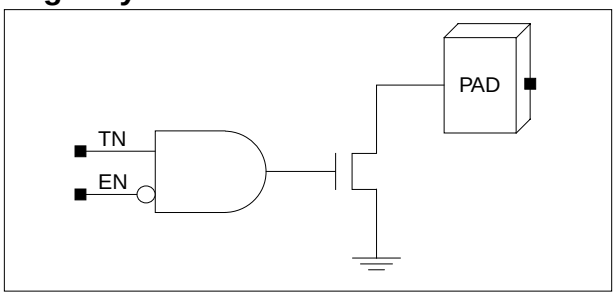
PvODyz_LP

Open Drain Output Buffers

Cell Availability

1.8V Interface	**1.8V Interface**	POD(1/2/4/8/12/16/20/24)_LP
		POD(4/8/12/16/20/24)SM_LP
		POD(12/16/20/24)SH_LP
	3.3V-Tolerant	PTOD(1/2/4/6)_LP
		PTOD(4/6)SM_LP
2.5V Interface	**2.5V Interface**	PMOD(1/2/4/8/12/16/20/24)_LP
		PMOD(4/8/12/16/20/24)SM_LP
		PMOD(12/16/20/24)SH_LP
3.3V Interface	**3.3V Interface**	PHOD(1/2/4/8/12/16/20/24)_LP
		PHOD(4/8/12/16/20/24)SM_LP
		PHOD(12/16/20/24)SH_LP
	5V-Tolerant	PHTOD(1/2/4/6)_LP
		PHTOD(4/6)SM_LP

Logic Symbol



Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

Standard Load (SL)

Cell Name	TN	EN
POD(1/2/4/8/12/16/20/24)_LP	3.82	3.69
POD(4/8/12/16/20/24)SM_LP	3.82	3.69
POD(12/16/20/24)SH_LP	3.82	3.69
PTOD(1/2/4/6)_LP	3.82	3.69
PTOD(4/6)SM_LP	3.82	3.69
PMOD(1/2/4/8/12/16/20/24)_LP	3.74	3.64
PMOD(4/8/12/16/20/24)SM_LP	3.74	3.64
PMOD(12/16/20/24)SH_LP	3.74	3.64
PHOD(1/2/4/8/12/16/20/24)_LP	3.74	3.64
PHOD(4/8/12/16/20/24)SM_LP	3.74	3.64
PHOD(12/16/20/24)SH_LP	3.74	3.64
PHTOD(1/2/4/6)_LP	3.74	3.64
PHTOD(4/6)SM_LP	3.74	3.64

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	23.041	1.821 + 0.424*CL	1.811 + 0.425*CL	1.811 + 0.425*CL
	t_{PHL}	12.578	1.712 + 0.217*CL	1.710 + 0.217*CL	1.713 + 0.217*CL
	t_{PLZ}	0.621	0.621 + 0.000*CL	0.621 + 0.000*CL	0.621 + 0.000*CL
EN to PAD	t_F	23.041	1.821 + 0.424*CL	1.811 + 0.425*CL	1.811 + 0.425*CL
	t_{PHL}	12.643	1.776 + 0.217*CL	1.775 + 0.217*CL	1.778 + 0.217*CL
	t_{PLZ}	0.655	0.654 + 0.000*CL	0.654 + 0.000*CL	0.654 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	12.222	0.988 + 0.225*CL	0.984 + 0.225*CL	0.975 + 0.225*CL
	t_{PHL}	6.916	1.064 + 0.117*CL	1.065 + 0.117*CL	1.065 + 0.117*CL
	t_{PLZ}	0.463	0.463 + 0.000*CL	0.463 + 0.000*CL	0.463 + 0.000*CL
EN to PAD	t_F	12.222	0.988 + 0.225*CL	0.984 + 0.225*CL	0.975 + 0.225*CL
	t_{PHL}	6.981	1.129 + 0.117*CL	1.129 + 0.117*CL	1.128 + 0.117*CL
	t_{PLZ}	0.495	0.495 + 0.000*CL	0.495 + 0.000*CL	0.495 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.905	0.572 + 0.127*CL	0.569 + 0.127*CL	0.566 + 0.127*CL
	t_{PHL}	4.152	0.734 + 0.068*CL	0.737 + 0.068*CL	0.738 + 0.068*CL
	t_{PLZ}	0.382	0.382 + 0.000*CL	0.382 + 0.000*CL	0.382 + 0.000*CL
EN to PAD	t_F	6.905	0.572 + 0.127*CL	0.569 + 0.127*CL	0.566 + 0.127*CL
	t_{PHL}	4.217	0.798 + 0.068*CL	0.802 + 0.068*CL	0.803 + 0.068*CL
	t_{PLZ}	0.416	0.416 + 0.000*CL	0.416 + 0.000*CL	0.416 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.462	0.293 + 0.063*CL	0.293 + 0.063*CL	0.293 + 0.063*CL
	t_{PHL}	2.297	0.584 + 0.034*CL	0.587 + 0.034*CL	0.590 + 0.034*CL
	t_{PLZ}	0.398	0.398 + 0.000*CL	0.398 + 0.000*CL	0.398 + 0.000*CL
EN to PAD	t_F	3.462	0.293 + 0.063*CL	0.293 + 0.063*CL	0.293 + 0.063*CL
	t_{PHL}	2.362	0.649 + 0.034*CL	0.652 + 0.034*CL	0.655 + 0.034*CL
	t_{PLZ}	0.431	0.431 + 0.000*CL	0.431 + 0.000*CL	0.431 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.325	0.220 + 0.042*CL	0.214 + 0.042*CL	0.212 + 0.042*CL
	t_{PHL}	1.738	0.592 + 0.023*CL	0.596 + 0.023*CL	0.599 + 0.023*CL
	t_{PLZ}	0.437	0.437 + 0.000*CL	0.437 + 0.000*CL	0.437 + 0.000*CL
EN to PAD	t_F	2.325	0.220 + 0.042*CL	0.214 + 0.042*CL	0.212 + 0.042*CL
	t_{PHL}	1.802	0.657 + 0.023*CL	0.660 + 0.023*CL	0.664 + 0.023*CL
	t_{PLZ}	0.472	0.472 + 0.000*CL	0.472 + 0.000*CL	0.472 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.765	0.202 + 0.031*CL	0.190 + 0.031*CL	0.182 + 0.032*CL
	t_{PHL}	1.488	0.625 + 0.017*CL	0.629 + 0.017*CL	0.632 + 0.017*CL
	t_{PLZ}	0.480	0.480 + 0.000*CL	0.480 + 0.000*CL	0.480 + 0.000*CL
EN to PAD	t_F	1.765	0.202 + 0.031*CL	0.190 + 0.031*CL	0.182 + 0.032*CL
	t_{PHL}	1.552	0.690 + 0.017*CL	0.694 + 0.017*CL	0.697 + 0.017*CL
	t_{PLZ}	0.514	0.514 + 0.000*CL	0.514 + 0.000*CL	0.514 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.440	0.206 + 0.025*CL	0.192 + 0.025*CL	0.179 + 0.025*CL
	t_{PHL}	1.361	0.665 + 0.014*CL	0.671 + 0.014*CL	0.675 + 0.014*CL
	t_{PLZ}	0.521	0.520 + 0.000*CL	0.520 + 0.000*CL	0.521 + 0.000*CL
EN to PAD	t_F	1.440	0.206 + 0.025*CL	0.191 + 0.025*CL	0.179 + 0.025*CL
	t_{PHL}	1.425	0.729 + 0.014*CL	0.736 + 0.014*CL	0.740 + 0.014*CL
	t_{PLZ}	0.555	0.555 + 0.000*CL	0.555 + 0.000*CL	0.555 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.235	0.221 + 0.020*CL	0.205 + 0.021*CL	0.191 + 0.021*CL
	t_{PHL}	1.294	0.703 + 0.012*CL	0.716 + 0.012*CL	0.722 + 0.011*CL
	t_{PLZ}	0.561	0.561 + 0.000*CL	0.561 + 0.000*CL	0.561 + 0.000*CL
EN to PAD	t_F	1.235	0.221 + 0.020*CL	0.205 + 0.021*CL	0.191 + 0.021*CL
	t_{PHL}	1.359	0.768 + 0.012*CL	0.781 + 0.012*CL	0.787 + 0.011*CL
	t_{PLZ}	0.595	0.595 + 0.000*CL	0.595 + 0.000*CL	0.595 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.966	0.675 + 0.126*CL	0.655 + 0.126*CL	0.639 + 0.126*CL
	t_{PHL}	4.576	1.147 + 0.069*CL	1.159 + 0.068*CL	1.163 + 0.068*CL
	t_{PLZ}	0.522	0.522 + 0.000*CL	0.522 + 0.000*CL	0.522 + 0.000*CL
EN to PAD	t_F	6.966	0.675 + 0.126*CL	0.655 + 0.126*CL	0.639 + 0.126*CL
	t_{PHL}	4.641	1.211 + 0.069*CL	1.224 + 0.068*CL	1.228 + 0.068*CL
	t_{PLZ}	0.556	0.556 + 0.000*CL	0.556 + 0.000*CL	0.556 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.878	0.875 + 0.060*CL	0.847 + 0.061*CL	0.797 + 0.061*CL
	t_{PHL}	3.718	1.845 + 0.037*CL	1.942 + 0.036*CL	2.003 + 0.035*CL
	t_{PLZ}	0.659	0.659 + 0.000*CL	0.659 + 0.000*CL	0.659 + 0.000*CL
EN to PAD	t_F	3.878	0.875 + 0.060*CL	0.847 + 0.061*CL	0.797 + 0.061*CL
	t_{PHL}	3.783	1.909 + 0.037*CL	2.007 + 0.036*CL	2.068 + 0.035*CL
	t_{PLZ}	0.693	0.693 + 0.000*CL	0.693 + 0.000*CL	0.693 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.486	1.427 + 0.041*CL	1.532 + 0.039*CL	1.564 + 0.039*CL
	t_{PHL}	3.883	2.173 + 0.034*CL	2.425 + 0.029*CL	2.627 + 0.026*CL
	t_{PLZ}	0.931	0.931 + 0.000*CL	0.931 + 0.000*CL	0.931 + 0.000*CL
EN to PAD	t_F	3.486	1.427 + 0.041*CL	1.532 + 0.039*CL	1.564 + 0.039*CL
	t_{PHL}	3.948	2.238 + 0.034*CL	2.490 + 0.029*CL	2.691 + 0.026*CL
	t_{PLZ}	0.966	0.965 + 0.000*CL	0.965 + 0.000*CL	0.965 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.686	1.088 + 0.032*CL	1.165 + 0.030*CL	1.208 + 0.030*CL
	t_{PHL}	3.580	2.274 + 0.026*CL	2.451 + 0.023*CL	2.601 + 0.021*CL
	t_{PLZ}	0.931	0.931 + 0.000*CL	0.931 + 0.000*CL	0.931 + 0.000*CL
EN to PAD	t_F	2.686	1.088 + 0.032*CL	1.165 + 0.030*CL	1.208 + 0.030*CL
	t_{PHL}	3.644	2.339 + 0.026*CL	2.515 + 0.023*CL	2.666 + 0.021*CL
	t_{PLZ}	0.965	0.964 + 0.000*CL	0.965 + 0.000*CL	0.965 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.861	1.322 + 0.031*CL	1.498 + 0.027*CL	1.636 + 0.025*CL
	t_{PHL}	3.775	2.357 + 0.028*CL	2.593 + 0.024*CL	2.813 + 0.021*CL
	t_{PLZ}	1.202	1.201 + 0.000*CL	1.202 + 0.000*CL	1.202 + 0.000*CL
EN to PAD	t_F	2.861	1.322 + 0.031*CL	1.498 + 0.027*CL	1.636 + 0.025*CL
	t_{PHL}	3.839	2.422 + 0.028*CL	2.658 + 0.024*CL	2.877 + 0.021*CL
	t_{PLZ}	1.236	1.235 + 0.000*CL	1.236 + 0.000*CL	1.236 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.484	1.237 + 0.025*CL	1.357 + 0.023*CL	1.454 + 0.021*CL
	t_{PHL}	3.841	2.642 + 0.024*CL	2.846 + 0.020*CL	3.030 + 0.017*CL
	t_{PLZ}	1.202	1.201 + 0.000*CL	1.201 + 0.000*CL	1.202 + 0.000*CL
EN to PAD	t_F	2.484	1.237 + 0.025*CL	1.357 + 0.023*CL	1.454 + 0.021*CL
	t_{PHL}	3.906	2.707 + 0.024*CL	2.911 + 0.020*CL	3.094 + 0.017*CL
	t_{PLZ}	1.236	1.235 + 0.000*CL	1.236 + 0.000*CL	1.236 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POD12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	5.032	2.309 + 0.054*CL	2.742 + 0.046*CL	3.056 + 0.042*CL
	t_{PHL}	5.726	3.124 + 0.052*CL	3.624 + 0.042*CL	4.089 + 0.036*CL
	t_{PLZ}	1.131	1.130 + 0.000*CL	1.131 + 0.000*CL	1.131 + 0.000*CL
EN to PAD	t_F	5.032	2.309 + 0.054*CL	2.742 + 0.046*CL	3.056 + 0.042*CL
	t_{PHL}	5.791	3.189 + 0.052*CL	3.689 + 0.042*CL	4.153 + 0.036*CL
	t_{PLZ}	1.165	1.164 + 0.000*CL	1.165 + 0.000*CL	1.165 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.039	2.346 + 0.074*CL	3.418 + 0.052*CL	4.217 + 0.042*CL
	t_{PHL}	5.811	2.496 + 0.066*CL	3.055 + 0.055*CL	3.855 + 0.044*CL
	t_{PLZ}	1.493	1.492 + 0.000*CL	1.492 + 0.000*CL	1.493 + 0.000*CL
EN to PAD	t_F	6.039	2.346 + 0.074*CL	3.418 + 0.052*CL	4.218 + 0.042*CL
	t_{PHL}	5.875	2.560 + 0.066*CL	3.120 + 0.055*CL	3.920 + 0.044*CL
	t_{PLZ}	1.527	1.526 + 0.000*CL	1.527 + 0.000*CL	1.527 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.605	1.870 + 0.035*CL	2.097 + 0.030*CL	2.287 + 0.028*CL
	t_{PHL}	5.423	3.675 + 0.035*CL	3.992 + 0.029*CL	4.283 + 0.025*CL
	t_{PLZ}	1.478	1.477 + 0.000*CL	1.477 + 0.000*CL	1.477 + 0.000*CL
EN to PAD	t_F	3.605	1.870 + 0.035*CL	2.097 + 0.030*CL	2.287 + 0.028*CL
	t_{PHL}	5.488	3.740 + 0.035*CL	4.057 + 0.029*CL	4.347 + 0.025*CL
	t_{PLZ}	1.512	1.511 + 0.000*CL	1.512 + 0.000*CL	1.512 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POD24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.194	1.615 + 0.052*CL	2.132 + 0.041*CL	2.649 + 0.034*CL
	t_{PHL}	5.205	3.146 + 0.041*CL	3.422 + 0.036*CL	3.738 + 0.031*CL
	t_{PLZ}	1.840	1.838 + 0.000*CL	1.840 + 0.000*CL	1.840 + 0.000*CL
EN to PAD	t_F	4.194	1.615 + 0.052*CL	2.132 + 0.041*CL	2.649 + 0.034*CL
	t_{PHL}	5.269	3.211 + 0.041*CL	3.487 + 0.036*CL	3.803 + 0.031*CL
	t_{PLZ}	1.874	1.872 + 0.000*CL	1.873 + 0.000*CL	1.874 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOD1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	24.366	3.196 + 0.423*CL	3.188 + 0.424*CL	3.155 + 0.424*CL
	t_{PHL}	12.396	1.482 + 0.218*CL	1.502 + 0.218*CL	1.505 + 0.218*CL
	t_{PLZ}	0.542	0.542 + 0.000*CL	0.542 + 0.000*CL	0.542 + 0.000*CL
EN to PAD	t_F	24.366	3.196 + 0.423*CL	3.188 + 0.424*CL	3.155 + 0.424*CL
	t_{PHL}	12.461	1.546 + 0.218*CL	1.567 + 0.218*CL	1.573 + 0.218*CL
	t_{PLZ}	0.575	0.575 + 0.000*CL	0.575 + 0.000*CL	0.575 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PTOD2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	12.934	1.661 + 0.225*CL	1.688 + 0.225*CL	1.706 + 0.225*CL
	t_{PHL}	6.708	0.744 + 0.119*CL	0.808 + 0.118*CL	0.863 + 0.117*CL
	t_{PLZ}	0.382	0.382 + 0.000*CL	0.382 + 0.000*CL	0.382 + 0.000*CL
EN to PAD	t_F	12.934	1.661 + 0.225*CL	1.688 + 0.225*CL	1.706 + 0.225*CL
	t_{PHL}	6.773	0.809 + 0.119*CL	0.872 + 0.118*CL	0.927 + 0.117*CL
	t_{PLZ}	0.416	0.416 + 0.000*CL	0.416 + 0.000*CL	0.416 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PTOD4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.452	0.867 + 0.112*CL	0.825 + 0.113*CL	0.819 + 0.113*CL
	t_{PHL}	3.625	0.671 + 0.059*CL	0.673 + 0.059*CL	0.675 + 0.059*CL
	t_{PLZ}	0.465	0.465 + 0.000*CL	0.465 + 0.000*CL	0.465 + 0.000*CL
EN to PAD	t_F	6.452	0.867 + 0.112*CL	0.826 + 0.113*CL	0.819 + 0.113*CL
	t_{PHL}	3.690	0.735 + 0.059*CL	0.738 + 0.059*CL	0.740 + 0.059*CL
	t_{PLZ}	0.499	0.499 + 0.000*CL	0.499 + 0.000*CL	0.499 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PTOD6_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.312	0.629 + 0.074*CL	0.587 + 0.074*CL	0.555 + 0.075*CL
	t_{PHL}	2.680	0.715 + 0.039*CL	0.717 + 0.039*CL	0.720 + 0.039*CL
	t_{PLZ}	0.547	0.547 + 0.000*CL	0.547 + 0.000*CL	0.547 + 0.000*CL
EN to PAD	t_F	4.312	0.629 + 0.074*CL	0.587 + 0.074*CL	0.555 + 0.075*CL
	t_{PHL}	2.745	0.779 + 0.039*CL	0.782 + 0.039*CL	0.784 + 0.039*CL
	t_{PLZ}	0.581	0.581 + 0.000*CL	0.581 + 0.000*CL	0.581 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOD4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.554	1.087 + 0.109*CL	0.993 + 0.111*CL	0.946 + 0.112*CL
	t_{PHL}	4.631	1.644 + 0.060*CL	1.670 + 0.059*CL	1.682 + 0.059*CL
	t_{PLZ}	0.478	0.478 + 0.000*CL	0.478 + 0.000*CL	0.478 + 0.000*CL
EN to PAD	t_F	6.554	1.087 + 0.109*CL	0.993 + 0.111*CL	0.946 + 0.112*CL
	t_{PHL}	4.695	1.709 + 0.060*CL	1.735 + 0.059*CL	1.746 + 0.059*CL
	t_{PLZ}	0.512	0.512 + 0.000*CL	0.512 + 0.000*CL	0.512 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PTOD6SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.589	1.160 + 0.069*CL	1.022 + 0.071*CL	0.898 + 0.073*CL
	t_{PHL}	3.757	1.680 + 0.042*CL	1.752 + 0.040*CL	1.793 + 0.040*CL
	t_{PLZ}	0.904	0.903 + 0.000*CL	0.903 + 0.000*CL	0.904 + 0.000*CL
EN to PAD	t_F	4.589	1.160 + 0.069*CL	1.022 + 0.071*CL	0.898 + 0.073*CL
	t_{PHL}	3.822	1.745 + 0.042*CL	1.817 + 0.040*CL	1.858 + 0.040*CL
	t_{PLZ}	0.938	0.937 + 0.000*CL	0.937 + 0.000*CL	0.937 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOD1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	22.782	1.225 + 0.431*CL	1.216 + 0.431*CL	1.213 + 0.431*CL
	t_{PHL}	12.710	1.572 + 0.223*CL	1.572 + 0.223*CL	1.572 + 0.223*CL
	t_{PLZ}	0.899	0.899 + 0.000*CL	0.899 + 0.000*CL	0.899 + 0.000*CL
EN to PAD	t_F	22.782	1.225 + 0.431*CL	1.216 + 0.431*CL	1.213 + 0.431*CL
	t_{PHL}	12.813	1.674 + 0.223*CL	1.675 + 0.223*CL	1.675 + 0.223*CL
	t_{PLZ}	0.975	0.975 + 0.000*CL	0.975 + 0.000*CL	0.975 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	12.991	0.714 + 0.246*CL	0.707 + 0.246*CL	0.704 + 0.246*CL
	t_{PHL}	7.829	1.229 + 0.132*CL	1.230 + 0.132*CL	1.229 + 0.132*CL
	t_{PLZ}	0.800	0.800 + 0.000*CL	0.799 + 0.000*CL	0.800 + 0.000*CL
EN to PAD	t_F	12.991	0.714 + 0.246*CL	0.707 + 0.246*CL	0.704 + 0.246*CL
	t_{PHL}	7.932	1.332 + 0.132*CL	1.331 + 0.132*CL	1.332 + 0.132*CL
	t_{PLZ}	0.876	0.876 + 0.000*CL	0.876 + 0.000*CL	0.876 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.518	0.385 + 0.123*CL	0.382 + 0.123*CL	0.379 + 0.123*CL
	t_{PHL}	4.410	1.106 + 0.066*CL	1.110 + 0.066*CL	1.111 + 0.066*CL
	t_{PLZ}	0.902	0.902 + 0.000*CL	0.902 + 0.000*CL	0.902 + 0.000*CL
EN to PAD	t_F	6.518	0.385 + 0.123*CL	0.382 + 0.123*CL	0.379 + 0.123*CL
	t_{PHL}	4.513	1.209 + 0.066*CL	1.212 + 0.066*CL	1.213 + 0.066*CL
	t_{PLZ}	0.977	0.977 + 0.000*CL	0.977 + 0.000*CL	0.977 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.299	0.251 + 0.061*CL	0.240 + 0.061*CL	0.232 + 0.061*CL
	t_{PHL}	2.806	1.143 + 0.033*CL	1.151 + 0.033*CL	1.156 + 0.033*CL
	t_{PLZ}	1.104	1.104 + 0.000*CL	1.104 + 0.000*CL	1.104 + 0.000*CL
EN to PAD	t_F	3.299	0.251 + 0.061*CL	0.239 + 0.061*CL	0.232 + 0.061*CL
	t_{PHL}	2.908	1.245 + 0.033*CL	1.253 + 0.033*CL	1.258 + 0.033*CL
	t_{PLZ}	1.179	1.179 + 0.000*CL	1.179 + 0.000*CL	1.179 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOD12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.229	0.217 + 0.040*CL	0.200 + 0.041*CL	0.187 + 0.041*CL
	t_{PHL}	2.275	1.162 + 0.022*CL	1.168 + 0.022*CL	1.173 + 0.022*CL
	t_{PLZ}	1.010	1.010 + 0.000*CL	1.010 + 0.000*CL	1.010 + 0.000*CL
EN to PAD	t_F	2.229	0.217 + 0.040*CL	0.200 + 0.041*CL	0.187 + 0.041*CL
	t_{PHL}	2.378	1.264 + 0.022*CL	1.271 + 0.022*CL	1.276 + 0.022*CL
	t_{PLZ}	1.084	1.084 + 0.000*CL	1.084 + 0.000*CL	1.084 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.727	0.245 + 0.030*CL	0.225 + 0.030*CL	0.206 + 0.030*CL
	t_{PHL}	2.087	1.238 + 0.017*CL	1.252 + 0.017*CL	1.260 + 0.017*CL
	t_{PLZ}	1.109	1.109 + 0.000*CL	1.109 + 0.000*CL	1.109 + 0.000*CL
EN to PAD	t_F	1.727	0.245 + 0.030*CL	0.225 + 0.030*CL	0.206 + 0.030*CL
	t_{PHL}	2.190	1.340 + 0.017*CL	1.355 + 0.017*CL	1.362 + 0.017*CL
	t_{PLZ}	1.183	1.183 + 0.000*CL	1.183 + 0.000*CL	1.184 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.449	0.283 + 0.023*CL	0.266 + 0.024*CL	0.245 + 0.024*CL
	t_{PHL}	2.012	1.305 + 0.014*CL	1.334 + 0.014*CL	1.348 + 0.013*CL
	t_{PLZ}	1.208	1.207 + 0.000*CL	1.208 + 0.000*CL	1.208 + 0.000*CL
EN to PAD	t_F	1.449	0.283 + 0.023*CL	0.266 + 0.024*CL	0.246 + 0.024*CL
	t_{PHL}	2.114	1.408 + 0.014*CL	1.436 + 0.014*CL	1.451 + 0.013*CL
	t_{PLZ}	1.282	1.282 + 0.000*CL	1.282 + 0.000*CL	1.282 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.282	0.320 + 0.019*CL	0.310 + 0.019*CL	0.293 + 0.020*CL
	t_{PHL}	1.988	1.364 + 0.012*CL	1.406 + 0.012*CL	1.431 + 0.011*CL
	t_{PLZ}	1.306	1.306 + 0.000*CL	1.306 + 0.000*CL	1.306 + 0.000*CL
EN to PAD	t_F	1.282	0.319 + 0.019*CL	0.311 + 0.019*CL	0.293 + 0.020*CL
	t_{PHL}	2.091	1.467 + 0.012*CL	1.509 + 0.012*CL	1.534 + 0.011*CL
	t_{PLZ}	1.381	1.380 + 0.000*CL	1.381 + 0.000*CL	1.381 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOD4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.772	0.827 + 0.119*CL	0.758 + 0.120*CL	0.687 + 0.121*CL
	t_{PHL}	5.655	2.280 + 0.067*CL	2.337 + 0.066*CL	2.358 + 0.066*CL
	t_{PLZ}	1.046	1.045 + 0.000*CL	1.045 + 0.000*CL	1.045 + 0.000*CL
EN to PAD	t_F	6.772	0.827 + 0.119*CL	0.758 + 0.120*CL	0.687 + 0.121*CL
	t_{PHL}	5.757	2.382 + 0.067*CL	2.439 + 0.066*CL	2.460 + 0.066*CL
	t_{PLZ}	1.120	1.119 + 0.000*CL	1.120 + 0.000*CL	1.120 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.945	1.031 + 0.058*CL	1.039 + 0.058*CL	1.006 + 0.059*CL
	t_{PHL}	4.654	2.700 + 0.039*CL	2.857 + 0.036*CL	2.970 + 0.034*CL
	t_{PLZ}	1.266	1.265 + 0.000*CL	1.265 + 0.000*CL	1.265 + 0.000*CL
EN to PAD	t_F	3.945	1.031 + 0.058*CL	1.039 + 0.058*CL	1.006 + 0.059*CL
	t_{PHL}	4.756	2.802 + 0.039*CL	2.960 + 0.036*CL	3.073 + 0.034*CL
	t_{PLZ}	1.340	1.339 + 0.000*CL	1.340 + 0.000*CL	1.340 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.000	1.030 + 0.039*CL	1.075 + 0.039*CL	1.079 + 0.038*CL
	t_{PHL}	4.103	2.625 + 0.030*CL	2.794 + 0.026*CL	2.929 + 0.024*CL
	t_{PLZ}	1.410	1.409 + 0.000*CL	1.409 + 0.000*CL	1.410 + 0.000*CL
EN to PAD	t_F	3.000	1.030 + 0.039*CL	1.075 + 0.039*CL	1.080 + 0.038*CL
	t_{PHL}	4.205	2.728 + 0.030*CL	2.897 + 0.026*CL	3.032 + 0.024*CL
	t_{PLZ}	1.484	1.483 + 0.000*CL	1.484 + 0.000*CL	1.484 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOD16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.740	1.168 + 0.031*CL	1.255 + 0.030*CL	1.309 + 0.029*CL
	t_{PHL}	4.229	2.886 + 0.027*CL	3.084 + 0.023*CL	3.253 + 0.021*CL
	t_{PLZ}	1.626	1.626 + 0.000*CL	1.626 + 0.000*CL	1.626 + 0.000*CL
EN to PAD	t_F	2.740	1.168 + 0.031*CL	1.255 + 0.030*CL	1.308 + 0.029*CL
	t_{PHL}	4.332	2.988 + 0.027*CL	3.186 + 0.023*CL	3.355 + 0.021*CL
	t_{PLZ}	1.701	1.700 + 0.000*CL	1.701 + 0.000*CL	1.701 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.523	1.184 + 0.027*CL	1.285 + 0.025*CL	1.359 + 0.024*CL
	t_{PHL}	4.197	2.968 + 0.025*CL	3.168 + 0.021*CL	3.341 + 0.018*CL
	t_{PLZ}	1.641	1.640 + 0.000*CL	1.641 + 0.000*CL	1.641 + 0.000*CL
EN to PAD	t_F	2.523	1.184 + 0.027*CL	1.285 + 0.025*CL	1.359 + 0.024*CL
	t_{PHL}	4.300	3.070 + 0.025*CL	3.270 + 0.021*CL	3.444 + 0.018*CL
	t_{PLZ}	1.716	1.715 + 0.000*CL	1.715 + 0.000*CL	1.716 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.523	1.184 + 0.027*CL	1.285 + 0.025*CL	1.359 + 0.024*CL
	t_{PHL}	4.197	2.968 + 0.025*CL	3.168 + 0.021*CL	3.341 + 0.018*CL
	t_{PLZ}	1.641	1.640 + 0.000*CL	1.641 + 0.000*CL	1.641 + 0.000*CL
EN to PAD	t_F	2.523	1.184 + 0.027*CL	1.285 + 0.025*CL	1.359 + 0.024*CL
	t_{PHL}	4.300	3.070 + 0.025*CL	3.270 + 0.021*CL	3.444 + 0.018*CL
	t_{PLZ}	1.716	1.715 + 0.000*CL	1.715 + 0.000*CL	1.716 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOD12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.173	1.871 + 0.046*CL	2.110 + 0.041*CL	2.268 + 0.039*CL
	t_{PHL}	5.241	3.110 + 0.043*CL	3.488 + 0.035*CL	3.813 + 0.031*CL
	t_{PLZ}	1.715	1.714 + 0.000*CL	1.715 + 0.000*CL	1.715 + 0.000*CL
EN to PAD	t_F	4.173	1.871 + 0.046*CL	2.110 + 0.041*CL	2.268 + 0.039*CL
	t_{PHL}	5.344	3.212 + 0.043*CL	3.591 + 0.035*CL	3.916 + 0.031*CL
	t_{PLZ}	1.790	1.789 + 0.000*CL	1.790 + 0.000*CL	1.789 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.100	1.085 + 0.040*CL	1.154 + 0.039*CL	1.189 + 0.038*CL
	t_{PHL}	4.235	2.706 + 0.031*CL	2.890 + 0.027*CL	3.046 + 0.025*CL
	t_{PLZ}	1.272	1.272 + 0.000*CL	1.272 + 0.000*CL	1.272 + 0.000*CL
EN to PAD	t_F	3.100	1.085 + 0.040*CL	1.154 + 0.039*CL	1.189 + 0.038*CL
	t_{PHL}	4.338	2.809 + 0.031*CL	2.993 + 0.027*CL	3.149 + 0.025*CL
	t_{PLZ}	1.347	1.347 + 0.000*CL	1.347 + 0.000*CL	1.347 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.755	1.721 + 0.041*CL	2.084 + 0.033*CL	2.371 + 0.030*CL
	t_{PHL}	5.373	3.501 + 0.037*CL	3.833 + 0.031*CL	4.145 + 0.027*CL
	t_{PLZ}	2.156	2.155 + 0.000*CL	2.156 + 0.000*CL	2.155 + 0.000*CL
EN to PAD	t_F	3.755	1.721 + 0.041*CL	2.084 + 0.033*CL	2.371 + 0.030*CL
	t_{PHL}	5.476	3.603 + 0.037*CL	3.936 + 0.031*CL	4.248 + 0.027*CL
	t_{PLZ}	2.231	2.230 + 0.000*CL	2.230 + 0.000*CL	2.231 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOD24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.443	1.285 + 0.043*CL	1.799 + 0.033*CL	2.200 + 0.028*CL
	t_{PHL}	4.333	2.574 + 0.035*CL	2.839 + 0.030*CL	3.151 + 0.026*CL
	t_{PLZ}	2.488	2.487 + 0.000*CL	2.488 + 0.000*CL	2.488 + 0.000*CL
EN to PAD	t_F	3.443	1.285 + 0.043*CL	1.799 + 0.033*CL	2.200 + 0.028*CL
	t_{PHL}	4.436	2.677 + 0.035*CL	2.942 + 0.030*CL	3.254 + 0.026*CL
	t_{PLZ}	2.563	2.562 + 0.000*CL	2.562 + 0.000*CL	2.563 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOD1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	26.612	1.552 + 0.501*CL	1.552 + 0.501*CL	1.546 + 0.501*CL
	t_{PHL}	13.674	1.724 + 0.239*CL	1.724 + 0.239*CL	1.724 + 0.239*CL
	t_{PLZ}	1.090	1.090 + 0.000*CL	1.090 + 0.000*CL	1.090 + 0.000*CL
EN to PAD	t_F	26.612	1.552 + 0.501*CL	1.552 + 0.501*CL	1.546 + 0.501*CL
	t_{PHL}	13.777	1.826 + 0.239*CL	1.827 + 0.239*CL	1.827 + 0.239*CL
	t_{PLZ}	1.165	1.165 + 0.000*CL	1.165 + 0.000*CL	1.165 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	14.643	0.869 + 0.275*CL	0.865 + 0.276*CL	0.862 + 0.276*CL
	t_{PHL}	8.144	1.284 + 0.137*CL	1.283 + 0.137*CL	1.284 + 0.137*CL
	t_{PLZ}	0.886	0.886 + 0.000*CL	0.886 + 0.000*CL	0.886 + 0.000*CL
EN to PAD	t_F	14.643	0.869 + 0.275*CL	0.865 + 0.276*CL	0.862 + 0.276*CL
	t_{PHL}	8.247	1.386 + 0.137*CL	1.386 + 0.137*CL	1.387 + 0.137*CL
	t_{PLZ}	0.961	0.961 + 0.000*CL	0.961 + 0.000*CL	0.961 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	8.642	0.523 + 0.162*CL	0.521 + 0.162*CL	0.516 + 0.162*CL
	t_{PHL}	5.362	1.055 + 0.086*CL	1.056 + 0.086*CL	1.056 + 0.086*CL
	t_{PLZ}	0.782	0.782 + 0.000*CL	0.782 + 0.000*CL	0.782 + 0.000*CL
EN to PAD	t_F	8.642	0.523 + 0.162*CL	0.521 + 0.162*CL	0.516 + 0.162*CL
	t_{PHL}	5.464	1.157 + 0.086*CL	1.158 + 0.086*CL	1.158 + 0.086*CL
	t_{PLZ}	0.857	0.857 + 0.000*CL	0.856 + 0.000*CL	0.857 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.338	0.281 + 0.081*CL	0.280 + 0.081*CL	0.279 + 0.081*CL
	t_{PHL}	3.132	0.974 + 0.043*CL	0.977 + 0.043*CL	0.979 + 0.043*CL
	t_{PLZ}	0.888	0.888 + 0.000*CL	0.888 + 0.000*CL	0.888 + 0.000*CL
EN to PAD	t_F	4.338	0.280 + 0.081*CL	0.280 + 0.081*CL	0.278 + 0.081*CL
	t_{PHL}	3.235	1.076 + 0.043*CL	1.080 + 0.043*CL	1.082 + 0.043*CL
	t_{PLZ}	0.963	0.963 + 0.000*CL	0.962 + 0.000*CL	0.963 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOD12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.909	0.213 + 0.054*CL	0.207 + 0.054*CL	0.203 + 0.054*CL
	t_{PHL}	2.428	0.985 + 0.029*CL	0.989 + 0.029*CL	0.992 + 0.029*CL
	t_{PLZ}	0.993	0.993 + 0.000*CL	0.993 + 0.000*CL	0.993 + 0.000*CL
EN to PAD	t_F	2.909	0.213 + 0.054*CL	0.207 + 0.054*CL	0.203 + 0.054*CL
	t_{PHL}	2.531	1.087 + 0.029*CL	1.092 + 0.029*CL	1.095 + 0.029*CL
	t_{PLZ}	1.068	1.068 + 0.000*CL	1.068 + 0.000*CL	1.068 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.190	0.175 + 0.040*CL	0.166 + 0.040*CL	0.160 + 0.041*CL
	t_{PHL}	2.063	0.979 + 0.022*CL	0.983 + 0.022*CL	0.985 + 0.022*CL
	t_{PLZ}	0.894	0.894 + 0.000*CL	0.894 + 0.000*CL	0.894 + 0.000*CL
EN to PAD	t_F	2.190	0.175 + 0.040*CL	0.166 + 0.040*CL	0.160 + 0.041*CL
	t_{PHL}	2.166	1.082 + 0.022*CL	1.086 + 0.022*CL	1.089 + 0.022*CL
	t_{PLZ}	0.969	0.969 + 0.000*CL	0.969 + 0.000*CL	0.969 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.771	0.174 + 0.032*CL	0.160 + 0.032*CL	0.150 + 0.032*CL
	t_{PHL}	1.878	1.009 + 0.017*CL	1.013 + 0.017*CL	1.016 + 0.017*CL
	t_{PLZ}	0.945	0.945 + 0.000*CL	0.945 + 0.000*CL	0.945 + 0.000*CL
EN to PAD	t_F	1.771	0.174 + 0.032*CL	0.161 + 0.032*CL	0.150 + 0.032*CL
	t_{PHL}	1.981	1.111 + 0.017*CL	1.116 + 0.017*CL	1.118 + 0.017*CL
	t_{PLZ}	1.020	1.020 + 0.000*CL	1.020 + 0.000*CL	1.020 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	1.500	0.184 + 0.026*CL	0.168 + 0.027*CL	0.154 + 0.027*CL
	t_{PHL}	1.770	1.040 + 0.015*CL	1.047 + 0.014*CL	1.050 + 0.014*CL
	t_{PLZ}	0.997	0.997 + 0.000*CL	0.997 + 0.000*CL	0.997 + 0.000*CL
EN to PAD	t_F	1.500	0.184 + 0.026*CL	0.168 + 0.027*CL	0.154 + 0.027*CL
	t_{PHL}	1.873	1.143 + 0.015*CL	1.150 + 0.014*CL	1.153 + 0.014*CL
	t_{PLZ}	1.071	1.071 + 0.000*CL	1.071 + 0.000*CL	1.071 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOD4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	8.701	0.638 + 0.161*CL	0.610 + 0.162*CL	0.588 + 0.162*CL
	t_{PHL}	5.814	1.501 + 0.086*CL	1.508 + 0.086*CL	1.509 + 0.086*CL
	t_{PLZ}	0.762	0.762 + 0.000*CL	0.762 + 0.000*CL	0.762 + 0.000*CL
EN to PAD	t_F	8.701	0.638 + 0.161*CL	0.610 + 0.162*CL	0.588 + 0.162*CL
	t_{PHL}	5.917	1.604 + 0.086*CL	1.611 + 0.086*CL	1.610 + 0.086*CL
	t_{PLZ}	0.837	0.837 + 0.000*CL	0.837 + 0.000*CL	0.837 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	4.465	0.504 + 0.079*CL	0.467 + 0.080*CL	0.431 + 0.080*CL
	t_{PHL}	3.793	1.601 + 0.044*CL	1.629 + 0.043*CL	1.642 + 0.043*CL
	t_{PLZ}	0.909	0.908 + 0.000*CL	0.908 + 0.000*CL	0.909 + 0.000*CL
EN to PAD	t_F	4.465	0.504 + 0.079*CL	0.467 + 0.080*CL	0.431 + 0.080*CL
	t_{PHL}	3.896	1.704 + 0.044*CL	1.732 + 0.043*CL	1.744 + 0.043*CL
	t_{PLZ}	0.984	0.984 + 0.000*CL	0.984 + 0.000*CL	0.984 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.242	0.671 + 0.051*CL	0.652 + 0.052*CL	0.612 + 0.052*CL
	t_{PHL}	3.403	1.824 + 0.032*CL	1.909 + 0.030*CL	1.962 + 0.029*CL
	t_{PLZ}	1.086	1.086 + 0.000*CL	1.086 + 0.000*CL	1.086 + 0.000*CL
EN to PAD	t_F	3.242	0.671 + 0.051*CL	0.652 + 0.052*CL	0.612 + 0.052*CL
	t_{PHL}	3.506	1.927 + 0.032*CL	2.012 + 0.030*CL	2.065 + 0.029*CL
	t_{PLZ}	1.161	1.161 + 0.000*CL	1.161 + 0.000*CL	1.161 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOD16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.770	0.849 + 0.038*CL	0.868 + 0.038*CL	0.852 + 0.038*CL
	t_{PHL}	3.313	1.958 + 0.027*CL	2.096 + 0.024*CL	2.199 + 0.023*CL
	t_{PLZ}	1.267	1.267 + 0.000*CL	1.267 + 0.000*CL	1.267 + 0.000*CL
EN to PAD	t_F	2.770	0.848 + 0.038*CL	0.868 + 0.038*CL	0.852 + 0.038*CL
	t_{PHL}	3.416	2.061 + 0.027*CL	2.199 + 0.024*CL	2.301 + 0.023*CL
	t_{PLZ}	1.342	1.342 + 0.000*CL	1.342 + 0.000*CL	1.342 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.336	0.764 + 0.031*CL	0.798 + 0.031*CL	0.804 + 0.031*CL
	t_{PHL}	3.156	2.013 + 0.023*CL	2.138 + 0.020*CL	2.239 + 0.019*CL
	t_{PLZ}	1.262	1.262 + 0.000*CL	1.262 + 0.000*CL	1.262 + 0.000*CL
EN to PAD	t_F	2.336	0.764 + 0.031*CL	0.798 + 0.031*CL	0.804 + 0.031*CL
	t_{PHL}	3.259	2.116 + 0.023*CL	2.241 + 0.020*CL	2.342 + 0.019*CL
	t_{PLZ}	1.337	1.337 + 0.000*CL	1.337 + 0.000*CL	1.337 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	2.336	0.764 + 0.031*CL	0.798 + 0.031*CL	0.804 + 0.031*CL
	t_{PHL}	3.156	2.013 + 0.023*CL	2.138 + 0.020*CL	2.239 + 0.019*CL
	t_{PLZ}	1.262	1.262 + 0.000*CL	1.262 + 0.000*CL	1.262 + 0.000*CL
EN to PAD	t_F	2.336	0.764 + 0.031*CL	0.798 + 0.031*CL	0.804 + 0.031*CL
	t_{PHL}	3.259	2.116 + 0.023*CL	2.241 + 0.020*CL	2.342 + 0.019*CL
	t_{PLZ}	1.337	1.337 + 0.000*CL	1.337 + 0.000*CL	1.337 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOD12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.763	1.142 + 0.052*CL	1.192 + 0.051*CL	1.199 + 0.051*CL
	t_{PHL}	4.428	2.570 + 0.037*CL	2.760 + 0.033*CL	2.913 + 0.031*CL
	t_{PLZ}	1.273	1.272 + 0.000*CL	1.273 + 0.000*CL	1.272 + 0.000*CL
EN to PAD	t_F	3.763	1.142 + 0.052*CL	1.192 + 0.051*CL	1.199 + 0.051*CL
	t_{PHL}	4.531	2.673 + 0.037*CL	2.863 + 0.033*CL	3.016 + 0.031*CL
	t_{PLZ}	1.347	1.347 + 0.000*CL	1.347 + 0.000*CL	1.347 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.100	1.085 + 0.040*CL	1.154 + 0.039*CL	1.189 + 0.038*CL
	t_{PHL}	4.235	2.706 + 0.031*CL	2.890 + 0.027*CL	3.046 + 0.025*CL
	t_{PLZ}	1.272	1.272 + 0.000*CL	1.272 + 0.000*CL	1.272 + 0.000*CL
EN to PAD	t_F	3.100	1.085 + 0.040*CL	1.154 + 0.039*CL	1.189 + 0.038*CL
	t_{PHL}	4.338	2.809 + 0.031*CL	2.993 + 0.027*CL	3.149 + 0.025*CL
	t_{PLZ}	1.347	1.347 + 0.000*CL	1.347 + 0.000*CL	1.347 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.044	1.309 + 0.035*CL	1.418 + 0.033*CL	1.499 + 0.031*CL
	t_{PHL}	4.483	2.988 + 0.030*CL	3.210 + 0.025*CL	3.405 + 0.023*CL
	t_{PLZ}	1.513	1.513 + 0.000*CL	1.513 + 0.000*CL	1.513 + 0.000*CL
EN to PAD	t_F	3.044	1.309 + 0.035*CL	1.418 + 0.033*CL	1.499 + 0.031*CL
	t_{PHL}	4.586	3.090 + 0.030*CL	3.313 + 0.025*CL	3.508 + 0.023*CL
	t_{PLZ}	1.588	1.588 + 0.000*CL	1.588 + 0.000*CL	1.588 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOD24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	3.122	1.518 + 0.032*CL	1.670 + 0.029*CL	1.789 + 0.027*CL
	t_{PHL}	4.667	3.141 + 0.031*CL	3.401 + 0.025*CL	3.633 + 0.022*CL
	t_{PLZ}	1.747	1.747 + 0.000*CL	1.747 + 0.000*CL	1.747 + 0.000*CL
EN to PAD	t_F	3.122	1.518 + 0.032*CL	1.670 + 0.029*CL	1.789 + 0.027*CL
	t_{PHL}	4.770	3.244 + 0.031*CL	3.504 + 0.025*CL	3.735 + 0.022*CL
	t_{PLZ}	1.822	1.822 + 0.000*CL	1.822 + 0.000*CL	1.822 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvODyz_LP

Open Drain Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHTOD1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	28.071	4.173 + 0.478*CL	3.415 + 0.493*CL	3.040 + 0.498*CL
	t_{PHL}	14.822	3.137 + 0.234*CL	3.068 + 0.235*CL	2.909 + 0.237*CL
	t_{PLZ}	0.959	0.959 + 0.000*CL	0.959 + 0.000*CL	0.959 + 0.000*CL
EN to PAD	t_F	28.071	4.173 + 0.478*CL	3.415 + 0.493*CL	3.040 + 0.498*CL
	t_{PHL}	14.925	3.237 + 0.234*CL	3.173 + 0.235*CL	3.008 + 0.237*CL
	t_{PLZ}	1.034	1.034 + 0.000*CL	1.034 + 0.000*CL	1.034 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHTOD2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	15.843	3.513 + 0.247*CL	2.661 + 0.264*CL	2.151 + 0.270*CL
	t_{PHL}	8.623	1.754 + 0.137*CL	1.833 + 0.136*CL	1.855 + 0.136*CL
	t_{PLZ}	0.753	0.753 + 0.000*CL	0.753 + 0.000*CL	0.753 + 0.000*CL
EN to PAD	t_F	15.843	3.513 + 0.247*CL	2.661 + 0.264*CL	2.151 + 0.270*CL
	t_{PHL}	8.726	1.857 + 0.137*CL	1.935 + 0.136*CL	1.958 + 0.136*CL
	t_{PLZ}	0.829	0.829 + 0.000*CL	0.829 + 0.000*CL	0.829 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHTOD4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	8.616	2.928 + 0.114*CL	2.545 + 0.121*CL	1.976 + 0.129*CL
	t_{PHL}	5.267	1.768 + 0.070*CL	1.806 + 0.069*CL	1.844 + 0.069*CL
	t_{PLZ}	0.853	0.853 + 0.000*CL	0.853 + 0.000*CL	0.853 + 0.000*CL
EN to PAD	t_F	8.616	2.928 + 0.114*CL	2.545 + 0.121*CL	1.976 + 0.129*CL
	t_{PHL}	5.370	1.870 + 0.070*CL	1.909 + 0.069*CL	1.946 + 0.069*CL
	t_{PLZ}	0.929	0.929 + 0.000*CL	0.929 + 0.000*CL	0.929 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHTOD6_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.187	2.095 + 0.082*CL	2.217 + 0.079*CL	2.026 + 0.082*CL
	t_{PHL}	4.346	1.979 + 0.047*CL	2.019 + 0.047*CL	2.048 + 0.046*CL
	t_{PLZ}	0.958	0.958 + 0.000*CL	0.958 + 0.000*CL	0.958 + 0.000*CL
EN to PAD	t_F	6.187	2.095 + 0.082*CL	2.217 + 0.079*CL	2.026 + 0.082*CL
	t_{PHL}	4.449	2.082 + 0.047*CL	2.122 + 0.047*CL	2.151 + 0.046*CL
	t_{PLZ}	1.033	1.033 + 0.000*CL	1.033 + 0.000*CL	1.033 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHTOD4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	8.675	3.050 + 0.112*CL	2.638 + 0.121*CL	2.051 + 0.129*CL
	t_{PHL}	5.748	2.227 + 0.070*CL	2.281 + 0.069*CL	2.325 + 0.069*CL
	t_{PLZ}	0.902	0.902 + 0.000*CL	0.902 + 0.000*CL	0.902 + 0.000*CL
EN to PAD	t_F	8.675	3.050 + 0.112*CL	2.638 + 0.121*CL	2.051 + 0.129*CL
	t_{PHL}	5.851	2.330 + 0.070*CL	2.384 + 0.069*CL	2.428 + 0.069*CL
	t_{PLZ}	0.977	0.977 + 0.000*CL	0.977 + 0.000*CL	0.977 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHTOD6SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	6.516	2.660 + 0.077*CL	2.711 + 0.076*CL	2.440 + 0.080*CL
	t_{PHL}	5.198	2.704 + 0.050*CL	2.813 + 0.048*CL	2.888 + 0.047*CL
	t_{PLZ}	1.079	1.079 + 0.000*CL	1.079 + 0.000*CL	1.079 + 0.000*CL
EN to PAD	t_F	6.516	2.660 + 0.077*CL	2.711 + 0.076*CL	2.440 + 0.080*CL
	t_{PHL}	5.301	2.808 + 0.050*CL	2.916 + 0.048*CL	2.990 + 0.047*CL
	t_{PLZ}	1.154	1.154 + 0.000*CL	1.154 + 0.000*CL	1.154 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

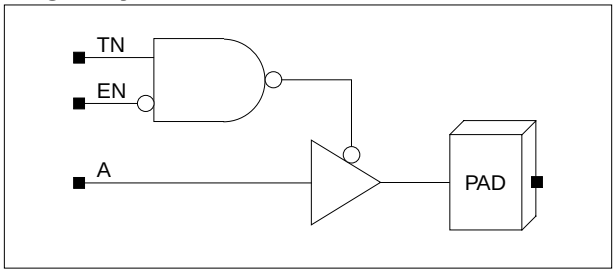
PvOTyz_LP

Tri-State Output Buffers

Cell Availability

1.8V Interface	**1.8V Interface**	POT(1/2/4/8/12/16/20/24)_LP
		POT(4/8/12/16/20/24)SM_LP
		POT(12/16/20/24)SH_LP
	3.3V-Tolerant	PTOT(1/2/4/6)_LP
		PTOT(4/6)SM_LP
2.5V Interface	**2.5V Interface**	PMOT(1/2/4/8/12/16/20/24)_LP
		PMOT(4/8/12/16/20/24)SM_LP
		PMOT(12/16/20/24)SH_LP
3.3V Interface	**3.3V Interface**	PHOT(1/2/4/8/12/16/20/24)_LP
		PHOT(4/8/12/16/20/24)SM_LP
		PHOT(12/16/20/24)SH_LP
	5V-Tolerant	PHTOT(1/2/4/6)_LP
		PHTOT(4/6)SM_LP

Logic Symbol



Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

Standard Load (SL)

Cell Name	TN	EN	A
POT(1/2/4/8/12/16/20/24)_LP	3.80	3.69	3.67
POT(4/8/12/16/20/24)SM_LP	3.80	3.69	3.67
POT(12/16/20/24)SH_LP	3.80	3.69	3.67
PTOT(1/2/4/6)_LP	3.80	3.69	3.67
PTOT(4/6)SM_LP	3.80	3.69	3.67
PMOT(1/2/4/8/12/16/20/24)_LP	3.74	3.64	6.31
PMOT(4/8/12/16/20/24)SM_LP	3.74	3.64	6.31
PMOT(12/16/20/24)SH_LP	3.74	3.64	6.31
PHOT(1/2/4/8/12/16/20/24)_LP	3.74	3.64	7.49
PHOT(4/8/12/16/20/24)SM_LP	3.74	3.64	7.49
PHOT(12/16/20/24)SH_LP	3.74	3.64	7.49
PHTOT(1/2/4/6)_LP	3.74	3.64	7.49
PHTOT(4/6)SM_LP	3.74	3.64	7.49

Switching Characteristics

(Typical process, 25°C,1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	20.443	1.560 + 0.378*CL	1.557 + 0.378*CL	1.554 + 0.378*CL
	t_F	23.041	1.821 + 0.424*CL	1.811 + 0.425*CL	1.811 + 0.425*CL
	t_{PLH}	10.016	1.101 + 0.178*CL	1.102 + 0.178*CL	1.102 + 0.178*CL
	t_{PHL}	12.567	1.701 + 0.217*CL	1.699 + 0.217*CL	1.702 + 0.217*CL
TN to PAD	t_R	20.443	1.560 + 0.378*CL	1.557 + 0.378*CL	1.554 + 0.378*CL
	t_F	23.041	1.821 + 0.424*CL	1.811 + 0.425*CL	1.811 + 0.425*CL
	t_{PLH}	10.066	1.149 + 0.178*CL	1.150 + 0.178*CL	1.150 + 0.178*CL
	t_{PHL}	12.638	1.769 + 0.217*CL	1.772 + 0.217*CL	1.769 + 0.217*CL
	t_{PLZ}	0.670	0.670 + 0.000*CL	0.670 + 0.000*CL	0.670 + 0.000*CL
	t_{PHZ}	0.531	0.531 + 0.000*CL	0.531 + 0.000*CL	0.531 + 0.000*CL
EN to PAD	t_R	20.443	1.560 + 0.378*CL	1.557 + 0.378*CL	1.554 + 0.378*CL
	t_F	23.041	1.821 + 0.424*CL	1.811 + 0.425*CL	1.811 + 0.425*CL
	t_{PLH}	10.131	1.215 + 0.178*CL	1.215 + 0.178*CL	1.215 + 0.178*CL
	t_{PHL}	12.703	1.835 + 0.217*CL	1.837 + 0.217*CL	1.834 + 0.217*CL
	t_{PLZ}	0.704	0.704 + 0.000*CL	0.704 + 0.000*CL	0.704 + 0.000*CL
	t_{PHZ}	0.565	0.565 + 0.000*CL	0.564 + 0.000*CL	0.565 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.759	1.082 + 0.254*CL	1.081 + 0.254*CL	1.078 + 0.254*CL
	t_F	12.208	0.976 + 0.225*CL	0.968 + 0.225*CL	0.962 + 0.225*CL
	t_{PLH}	7.049	0.980 + 0.121*CL	0.981 + 0.121*CL	0.984 + 0.121*CL
	t_{PHL}	6.904	1.052 + 0.117*CL	1.053 + 0.117*CL	1.053 + 0.117*CL
TN to PAD	t_R	13.759	1.082 + 0.254*CL	1.081 + 0.254*CL	1.078 + 0.254*CL
	t_F	12.208	0.976 + 0.225*CL	0.968 + 0.225*CL	0.962 + 0.225*CL
	t_{PLH}	7.099	1.029 + 0.121*CL	1.030 + 0.121*CL	1.032 + 0.121*CL
	t_{PHL}	6.974	1.121 + 0.117*CL	1.122 + 0.117*CL	1.123 + 0.117*CL
	t_{PLZ}	0.511	0.511 + 0.000*CL	0.511 + 0.000*CL	0.511 + 0.000*CL
	t_{PHZ}	0.824	0.824 + 0.000*CL	0.824 + 0.000*CL	0.824 + 0.000*CL
EN to PAD	t_R	13.759	1.082 + 0.254*CL	1.081 + 0.254*CL	1.078 + 0.254*CL
	t_F	12.208	0.976 + 0.225*CL	0.968 + 0.225*CL	0.962 + 0.225*CL
	t_{PLH}	7.165	1.095 + 0.121*CL	1.096 + 0.121*CL	1.097 + 0.121*CL
	t_{PHL}	7.039	1.186 + 0.117*CL	1.187 + 0.117*CL	1.188 + 0.117*CL
	t_{PLZ}	0.545	0.545 + 0.000*CL	0.545 + 0.000*CL	0.545 + 0.000*CL
	t_{PHZ}	0.858	0.858 + 0.000*CL	0.858 + 0.000*CL	0.858 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.856	0.564 + 0.126*CL	0.563 + 0.126*CL	0.562 + 0.126*CL
	t_F	6.905	0.572 + 0.127*CL	0.570 + 0.127*CL	0.562 + 0.127*CL
	t_{PLH}	3.694	0.719 + 0.059*CL	0.721 + 0.059*CL	0.723 + 0.059*CL
	t_{PHL}	4.142	0.727 + 0.068*CL	0.729 + 0.068*CL	0.729 + 0.068*CL
TN to PAD	t_R	6.856	0.564 + 0.126*CL	0.563 + 0.126*CL	0.562 + 0.126*CL
	t_F	6.905	0.572 + 0.127*CL	0.570 + 0.127*CL	0.562 + 0.127*CL
	t_{PLH}	3.744	0.768 + 0.060*CL	0.771 + 0.059*CL	0.773 + 0.059*CL
	t_{PHL}	4.209	0.790 + 0.068*CL	0.794 + 0.068*CL	0.795 + 0.068*CL
	t_{PLZ}	0.428	0.428 + 0.000*CL	0.428 + 0.000*CL	0.428 + 0.000*CL
	t_{PHZ}	0.832	0.832 + 0.000*CL	0.832 + 0.000*CL	0.832 + 0.000*CL
EN to PAD	t_R	6.856	0.564 + 0.126*CL	0.563 + 0.126*CL	0.562 + 0.126*CL
	t_F	6.905	0.572 + 0.127*CL	0.570 + 0.127*CL	0.562 + 0.127*CL
	t_{PLH}	3.810	0.833 + 0.060*CL	0.837 + 0.059*CL	0.838 + 0.059*CL
	t_{PHL}	4.275	0.855 + 0.068*CL	0.860 + 0.068*CL	0.861 + 0.068*CL
	t_{PLZ}	0.463	0.463 + 0.000*CL	0.463 + 0.000*CL	0.463 + 0.000*CL
	t_{PHZ}	0.866	0.866 + 0.000*CL	0.866 + 0.000*CL	0.866 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.439	0.293 + 0.063*CL	0.292 + 0.063*CL	0.292 + 0.063*CL
	t_F	3.462	0.296 + 0.063*CL	0.294 + 0.063*CL	0.293 + 0.063*CL
	t_{PLH}	2.135	0.646 + 0.030*CL	0.648 + 0.030*CL	0.649 + 0.030*CL
	t_{PHL}	2.308	0.603 + 0.034*CL	0.603 + 0.034*CL	0.603 + 0.034*CL
TN to PAD	t_R	3.439	0.293 + 0.063*CL	0.292 + 0.063*CL	0.292 + 0.063*CL
	t_F	3.462	0.293 + 0.063*CL	0.293 + 0.063*CL	0.293 + 0.063*CL
	t_{PLH}	2.186	0.695 + 0.030*CL	0.698 + 0.030*CL	0.699 + 0.030*CL
	t_{PHL}	2.371	0.657 + 0.034*CL	0.661 + 0.034*CL	0.664 + 0.034*CL
	t_{PLZ}	0.460	0.460 + 0.000*CL	0.460 + 0.000*CL	0.460 + 0.000*CL
	t_{PHZ}	0.876	0.876 + 0.000*CL	0.876 + 0.000*CL	0.876 + 0.000*CL
EN to PAD	t_R	3.439	0.293 + 0.063*CL	0.292 + 0.063*CL	0.292 + 0.063*CL
	t_F	3.462	0.293 + 0.063*CL	0.293 + 0.063*CL	0.293 + 0.063*CL
	t_{PLH}	2.251	0.761 + 0.030*CL	0.763 + 0.030*CL	0.765 + 0.030*CL
	t_{PHL}	2.437	0.722 + 0.034*CL	0.727 + 0.034*CL	0.729 + 0.034*CL
	t_{PLZ}	0.495	0.495 + 0.000*CL	0.495 + 0.000*CL	0.495 + 0.000*CL
	t_{PHZ}	0.910	0.910 + 0.000*CL	0.910 + 0.000*CL	0.910 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.312	0.227 + 0.042*CL	0.218 + 0.042*CL	0.213 + 0.042*CL
	t_F	2.327	0.236 + 0.042*CL	0.219 + 0.042*CL	0.215 + 0.042*CL
	t_{PLH}	1.688	0.694 + 0.020*CL	0.696 + 0.020*CL	0.697 + 0.020*CL
	t_{PHL}	1.761	0.634 + 0.023*CL	0.628 + 0.023*CL	0.625 + 0.023*CL
TN to PAD	t_R	2.312	0.228 + 0.042*CL	0.218 + 0.042*CL	0.213 + 0.042*CL
	t_F	2.324	0.218 + 0.042*CL	0.214 + 0.042*CL	0.211 + 0.042*CL
	t_{PLH}	1.739	0.743 + 0.020*CL	0.745 + 0.020*CL	0.747 + 0.020*CL
	t_{PHL}	1.812	0.664 + 0.023*CL	0.669 + 0.023*CL	0.672 + 0.023*CL
	t_{PLZ}	0.503	0.503 + 0.000*CL	0.503 + 0.000*CL	0.503 + 0.000*CL
	t_{PHZ}	1.097	1.096 + 0.000*CL	1.096 + 0.000*CL	1.097 + 0.000*CL
EN to PAD	t_R	2.312	0.228 + 0.042*CL	0.218 + 0.042*CL	0.213 + 0.042*CL
	t_F	2.324	0.218 + 0.042*CL	0.214 + 0.042*CL	0.211 + 0.042*CL
	t_{PLH}	1.804	0.809 + 0.020*CL	0.811 + 0.020*CL	0.813 + 0.020*CL
	t_{PHL}	1.877	0.730 + 0.023*CL	0.734 + 0.023*CL	0.738 + 0.023*CL
	t_{PLZ}	0.537	0.537 + 0.000*CL	0.537 + 0.000*CL	0.537 + 0.000*CL
	t_{PHZ}	1.131	1.130 + 0.000*CL	1.130 + 0.000*CL	1.131 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.762	0.220 + 0.031*CL	0.204 + 0.031*CL	0.192 + 0.031*CL
	t_F	1.777	0.248 + 0.031*CL	0.217 + 0.031*CL	0.194 + 0.031*CL
	t_{PLH}	1.508	0.759 + 0.015*CL	0.762 + 0.015*CL	0.764 + 0.015*CL
	t_{PHL}	1.528	0.698 + 0.017*CL	0.687 + 0.017*CL	0.679 + 0.017*CL
TN to PAD	t_R	1.762	0.221 + 0.031*CL	0.203 + 0.031*CL	0.191 + 0.031*CL
	t_F	1.764	0.198 + 0.031*CL	0.188 + 0.032*CL	0.181 + 0.032*CL
	t_{PLH}	1.558	0.808 + 0.015*CL	0.812 + 0.015*CL	0.814 + 0.015*CL
	t_{PHL}	1.561	0.696 + 0.017*CL	0.701 + 0.017*CL	0.705 + 0.017*CL
	t_{PLZ}	0.544	0.544 + 0.000*CL	0.544 + 0.000*CL	0.544 + 0.000*CL
	t_{PHZ}	1.316	1.316 + 0.000*CL	1.316 + 0.000*CL	1.316 + 0.000*CL
EN to PAD	t_R	1.762	0.221 + 0.031*CL	0.203 + 0.031*CL	0.191 + 0.031*CL
	t_F	1.764	0.198 + 0.031*CL	0.188 + 0.032*CL	0.181 + 0.032*CL
	t_{PLH}	1.624	0.874 + 0.015*CL	0.878 + 0.015*CL	0.880 + 0.015*CL
	t_{PHL}	1.626	0.761 + 0.017*CL	0.766 + 0.017*CL	0.770 + 0.017*CL
	t_{PLZ}	0.578	0.578 + 0.000*CL	0.578 + 0.000*CL	0.578 + 0.000*CL
	t_{PHZ}	1.350	1.350 + 0.000*CL	1.350 + 0.000*CL	1.350 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.448	0.237 + 0.024*CL	0.216 + 0.025*CL	0.199 + 0.025*CL
	t_F	1.470	0.290 + 0.024*CL	0.249 + 0.024*CL	0.219 + 0.025*CL
	t_{PLH}	1.434	0.827 + 0.012*CL	0.835 + 0.012*CL	0.838 + 0.012*CL
	t_{PHL}	1.425	0.780 + 0.013*CL	0.763 + 0.013*CL	0.751 + 0.013*CL
TN to PAD	t_R	1.448	0.237 + 0.024*CL	0.216 + 0.025*CL	0.199 + 0.025*CL
	t_F	1.438	0.201 + 0.025*CL	0.188 + 0.025*CL	0.176 + 0.025*CL
	t_{PLH}	1.484	0.877 + 0.012*CL	0.885 + 0.012*CL	0.889 + 0.012*CL
	t_{PHL}	1.433	0.734 + 0.014*CL	0.742 + 0.014*CL	0.747 + 0.014*CL
	t_{PLZ}	0.585	0.585 + 0.000*CL	0.585 + 0.000*CL	0.585 + 0.000*CL
	t_{PHZ}	1.536	1.534 + 0.000*CL	1.535 + 0.000*CL	1.535 + 0.000*CL
EN to PAD	t_R	1.448	0.237 + 0.024*CL	0.216 + 0.025*CL	0.199 + 0.025*CL
	t_F	1.438	0.201 + 0.025*CL	0.188 + 0.025*CL	0.176 + 0.025*CL
	t_{PLH}	1.550	0.942 + 0.012*CL	0.951 + 0.012*CL	0.954 + 0.012*CL
	t_{PHL}	1.498	0.800 + 0.014*CL	0.808 + 0.014*CL	0.813 + 0.014*CL
	t_{PLZ}	0.620	0.619 + 0.000*CL	0.619 + 0.000*CL	0.620 + 0.000*CL
	t_{PHZ}	1.569	1.569 + 0.000*CL	1.569 + 0.000*CL	1.569 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.254	0.264 + 0.020*CL	0.243 + 0.020*CL	0.222 + 0.020*CL
	t_F	1.289	0.352 + 0.019*CL	0.300 + 0.020*CL	0.261 + 0.020*CL
	t_{PLH}	1.411	0.891 + 0.010*CL	0.907 + 0.010*CL	0.915 + 0.010*CL
	t_{PHL}	1.389	0.861 + 0.011*CL	0.851 + 0.011*CL	0.833 + 0.011*CL
TN to PAD	t_R	1.254	0.263 + 0.020*CL	0.243 + 0.020*CL	0.222 + 0.020*CL
	t_F	1.232	0.214 + 0.020*CL	0.200 + 0.021*CL	0.187 + 0.021*CL
	t_{PLH}	1.462	0.940 + 0.010*CL	0.958 + 0.010*CL	0.965 + 0.010*CL
	t_{PHL}	1.366	0.772 + 0.012*CL	0.786 + 0.012*CL	0.794 + 0.012*CL
	t_{PLZ}	0.626	0.626 + 0.000*CL	0.626 + 0.000*CL	0.626 + 0.000*CL
	t_{PHZ}	1.754	1.753 + 0.000*CL	1.754 + 0.000*CL	1.754 + 0.000*CL
EN to PAD	t_R	1.254	0.263 + 0.020*CL	0.243 + 0.020*CL	0.222 + 0.020*CL
	t_F	1.232	0.214 + 0.020*CL	0.200 + 0.021*CL	0.187 + 0.021*CL
	t_{PLH}	1.527	1.006 + 0.010*CL	1.023 + 0.010*CL	1.030 + 0.010*CL
	t_{PHL}	1.431	0.837 + 0.012*CL	0.851 + 0.012*CL	0.859 + 0.011*CL
	t_{PLZ}	0.660	0.660 + 0.000*CL	0.660 + 0.000*CL	0.660 + 0.000*CL
	t_{PHZ}	1.788	1.787 + 0.000*CL	1.788 + 0.000*CL	1.788 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.989	0.797 + 0.124*CL	0.748 + 0.125*CL	0.708 + 0.125*CL
	t_F	6.965	0.672 + 0.126*CL	0.654 + 0.126*CL	0.635 + 0.126*CL
	t_{PLH}	4.771	1.774 + 0.060*CL	1.791 + 0.060*CL	1.799 + 0.059*CL
	t_{PHL}	4.565	1.140 + 0.068*CL	1.150 + 0.068*CL	1.152 + 0.068*CL
TN to PAD	t_R	6.989	0.797 + 0.124*CL	0.748 + 0.125*CL	0.708 + 0.125*CL
	t_F	6.965	0.672 + 0.126*CL	0.654 + 0.126*CL	0.635 + 0.126*CL
	t_{PLH}	4.820	1.821 + 0.060*CL	1.839 + 0.060*CL	1.848 + 0.060*CL
	t_{PHL}	4.632	1.201 + 0.069*CL	1.215 + 0.068*CL	1.218 + 0.068*CL
	t_{PLZ}	0.570	0.570 + 0.000*CL	0.570 + 0.000*CL	0.570 + 0.000*CL
	t_{PHZ}	1.165	1.164 + 0.000*CL	1.165 + 0.000*CL	1.164 + 0.000*CL
EN to PAD	t_R	6.989	0.797 + 0.124*CL	0.748 + 0.125*CL	0.708 + 0.125*CL
	t_F	6.965	0.672 + 0.126*CL	0.654 + 0.126*CL	0.635 + 0.126*CL
	t_{PLH}	4.886	1.887 + 0.060*CL	1.905 + 0.060*CL	1.913 + 0.060*CL
	t_{PHL}	4.697	1.267 + 0.069*CL	1.280 + 0.068*CL	1.284 + 0.068*CL
	t_{PLZ}	0.604	0.604 + 0.000*CL	0.604 + 0.000*CL	0.604 + 0.000*CL
	t_{PHZ}	1.198	1.198 + 0.000*CL	1.198 + 0.000*CL	1.198 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.901	0.914 + 0.060*CL	0.881 + 0.060*CL	0.833 + 0.061*CL
	t_F	3.917	0.903 + 0.060*CL	0.888 + 0.061*CL	0.842 + 0.061*CL
	t_{PLH}	3.941	2.299 + 0.033*CL	2.388 + 0.031*CL	2.442 + 0.030*CL
	t_{PHL}	3.987	2.105 + 0.038*CL	2.205 + 0.036*CL	2.271 + 0.035*CL
TN to PAD	t_R	3.901	0.914 + 0.060*CL	0.881 + 0.060*CL	0.833 + 0.061*CL
	t_F	3.921	0.918 + 0.060*CL	0.895 + 0.061*CL	0.846 + 0.061*CL
	t_{PLH}	3.991	2.348 + 0.033*CL	2.437 + 0.031*CL	2.491 + 0.030*CL
	t_{PHL}	4.051	2.156 + 0.038*CL	2.264 + 0.036*CL	2.333 + 0.035*CL
	t_{PLZ}	0.742	0.742 + 0.000*CL	0.742 + 0.000*CL	0.742 + 0.000*CL
	t_{PHZ}	2.251	2.250 + 0.000*CL	2.250 + 0.000*CL	2.251 + 0.000*CL
EN to PAD	t_R	3.901	0.914 + 0.060*CL	0.881 + 0.060*CL	0.833 + 0.061*CL
	t_F	3.921	0.918 + 0.060*CL	0.895 + 0.061*CL	0.846 + 0.061*CL
	t_{PLH}	4.056	2.413 + 0.033*CL	2.503 + 0.031*CL	2.557 + 0.030*CL
	t_{PHL}	4.117	2.222 + 0.038*CL	2.329 + 0.036*CL	2.398 + 0.035*CL
	t_{PLZ}	0.776	0.776 + 0.000*CL	0.776 + 0.000*CL	0.776 + 0.000*CL
	t_{PHZ}	2.284	2.284 + 0.000*CL	2.284 + 0.000*CL	2.284 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.488	1.433 + 0.041*CL	1.513 + 0.040*CL	1.541 + 0.039*CL
	t_F	3.463	1.345 + 0.042*CL	1.444 + 0.040*CL	1.503 + 0.040*CL
	t_{PLH}	4.229	2.711 + 0.030*CL	2.932 + 0.026*CL	3.113 + 0.024*CL
	t_{PHL}	4.244	2.618 + 0.033*CL	2.807 + 0.029*CL	2.980 + 0.026*CL
TN to PAD	t_R	3.488	1.434 + 0.041*CL	1.514 + 0.039*CL	1.540 + 0.039*CL
	t_F	3.529	1.443 + 0.042*CL	1.550 + 0.040*CL	1.593 + 0.039*CL
	t_{PLH}	4.279	2.761 + 0.030*CL	2.982 + 0.026*CL	3.164 + 0.024*CL
	t_{PHL}	4.247	2.511 + 0.035*CL	2.763 + 0.030*CL	2.971 + 0.027*CL
	t_{PLZ}	1.015	1.015 + 0.000*CL	1.015 + 0.000*CL	1.015 + 0.000*CL
	t_{PHZ}	3.760	3.759 + 0.000*CL	3.760 + 0.000*CL	3.760 + 0.000*CL
EN to PAD	t_R	3.488	1.434 + 0.041*CL	1.514 + 0.039*CL	1.541 + 0.039*CL
	t_F	3.529	1.443 + 0.042*CL	1.550 + 0.040*CL	1.593 + 0.039*CL
	t_{PLH}	4.345	2.826 + 0.030*CL	3.047 + 0.026*CL	3.230 + 0.024*CL
	t_{PHL}	4.312	2.576 + 0.035*CL	2.829 + 0.030*CL	3.037 + 0.027*CL
	t_{PLZ}	1.049	1.049 + 0.000*CL	1.049 + 0.000*CL	1.049 + 0.000*CL
	t_{PHZ}	3.794	3.793 + 0.000*CL	3.793 + 0.000*CL	3.794 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.720	1.170 + 0.031*CL	1.226 + 0.030*CL	1.250 + 0.030*CL
	t_F	2.730	1.062 + 0.033*CL	1.168 + 0.031*CL	1.242 + 0.030*CL
	t_{PLH}	3.982	2.823 + 0.023*CL	2.989 + 0.020*CL	3.128 + 0.018*CL
	t_{PHL}	4.071	2.787 + 0.026*CL	2.941 + 0.023*CL	3.084 + 0.021*CL
TN to PAD	t_R	2.720	1.169 + 0.031*CL	1.225 + 0.030*CL	1.250 + 0.030*CL
	t_F	2.779	1.170 + 0.032*CL	1.254 + 0.031*CL	1.302 + 0.030*CL
	t_{PLH}	4.033	2.874 + 0.023*CL	3.041 + 0.020*CL	3.179 + 0.018*CL
	t_{PHL}	4.099	2.750 + 0.027*CL	2.941 + 0.023*CL	3.104 + 0.021*CL
	t_{PLZ}	1.241	1.241 + 0.000*CL	1.241 + 0.000*CL	1.242 + 0.000*CL
	t_{PHZ}	3.727	3.725 + 0.000*CL	3.726 + 0.000*CL	3.727 + 0.000*CL
EN to PAD	t_R	2.720	1.169 + 0.031*CL	1.226 + 0.030*CL	1.250 + 0.030*CL
	t_F	2.779	1.170 + 0.032*CL	1.254 + 0.031*CL	1.302 + 0.030*CL
	t_{PLH}	4.098	2.940 + 0.023*CL	3.106 + 0.020*CL	3.245 + 0.018*CL
	t_{PHL}	4.165	2.815 + 0.027*CL	3.006 + 0.023*CL	3.170 + 0.021*CL
	t_{PLZ}	1.275	1.275 + 0.000*CL	1.275 + 0.000*CL	1.275 + 0.000*CL
	t_{PHZ}	3.761	3.759 + 0.000*CL	3.760 + 0.000*CL	3.760 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.841	1.437 + 0.028*CL	1.554 + 0.026*CL	1.642 + 0.025*CL
	t_F	2.846	1.337 + 0.030*CL	1.465 + 0.028*CL	1.589 + 0.026*CL
	t_{PLH}	4.271	3.047 + 0.024*CL	3.259 + 0.020*CL	3.448 + 0.018*CL
	t_{PHL}	4.426	3.209 + 0.024*CL	3.334 + 0.022*CL	3.481 + 0.020*CL
TN to PAD	t_R	2.840	1.435 + 0.028*CL	1.553 + 0.026*CL	1.642 + 0.025*CL
	t_F	2.943	1.419 + 0.030*CL	1.582 + 0.027*CL	1.710 + 0.026*CL
	t_{PLH}	4.324	3.098 + 0.025*CL	3.311 + 0.020*CL	3.499 + 0.018*CL
	t_{PHL}	4.330	2.882 + 0.029*CL	3.129 + 0.024*CL	3.354 + 0.021*CL
	t_{PLZ}	1.602	1.602 + 0.000*CL	1.602 + 0.000*CL	1.602 + 0.000*CL
	t_{PHZ}	5.221	5.219 + 0.000*CL	5.220 + 0.000*CL	5.221 + 0.000*CL
EN to PAD	t_R	2.840	1.435 + 0.028*CL	1.553 + 0.026*CL	1.642 + 0.025*CL
	t_F	2.943	1.419 + 0.030*CL	1.582 + 0.027*CL	1.710 + 0.026*CL
	t_{PLH}	4.389	3.164 + 0.024*CL	3.376 + 0.020*CL	3.565 + 0.018*CL
	t_{PHL}	4.395	2.948 + 0.029*CL	3.195 + 0.024*CL	3.419 + 0.021*CL
	t_{PLZ}	1.636	1.636 + 0.000*CL	1.636 + 0.000*CL	1.636 + 0.000*CL
	t_{PHZ}	5.255	5.253 + 0.000*CL	5.254 + 0.000*CL	5.255 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.631	1.444 + 0.024*CL	1.545 + 0.022*CL	1.624 + 0.021*CL
	t_F	2.487	1.185 + 0.026*CL	1.301 + 0.024*CL	1.416 + 0.022*CL
	t_{PLH}	4.554	3.443 + 0.022*CL	3.647 + 0.018*CL	3.827 + 0.016*CL
	t_{PHL}	4.563	3.505 + 0.021*CL	3.618 + 0.019*CL	3.753 + 0.017*CL
TN to PAD	t_R	2.631	1.442 + 0.024*CL	1.543 + 0.022*CL	1.623 + 0.021*CL
	t_F	2.618	1.353 + 0.025*CL	1.481 + 0.023*CL	1.584 + 0.021*CL
	t_{PLH}	4.607	3.496 + 0.022*CL	3.700 + 0.018*CL	3.880 + 0.016*CL
	t_{PHL}	4.490	3.229 + 0.025*CL	3.452 + 0.021*CL	3.653 + 0.018*CL
	t_{PLZ}	1.602	1.602 + 0.000*CL	1.601 + 0.000*CL	1.602 + 0.000*CL
	t_{PHZ}	5.220	5.216 + 0.000*CL	5.218 + 0.000*CL	5.219 + 0.000*CL
EN to PAD	t_R	2.631	1.442 + 0.024*CL	1.543 + 0.022*CL	1.623 + 0.021*CL
	t_F	2.618	1.353 + 0.025*CL	1.481 + 0.023*CL	1.584 + 0.021*CL
	t_{PLH}	4.672	3.562 + 0.022*CL	3.766 + 0.018*CL	3.946 + 0.016*CL
	t_{PHL}	4.555	3.294 + 0.025*CL	3.518 + 0.021*CL	3.718 + 0.018*CL
	t_{PLZ}	1.636	1.635 + 0.000*CL	1.636 + 0.000*CL	1.636 + 0.000*CL
	t_{PHZ}	5.253	5.250 + 0.000*CL	5.252 + 0.000*CL	5.253 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.452	2.140 + 0.046*CL	2.322 + 0.043*CL	2.456 + 0.041*CL
	t_F	4.667	2.239 + 0.049*CL	2.490 + 0.044*CL	2.673 + 0.041*CL
	t_{PLH}	6.150	4.215 + 0.039*CL	4.534 + 0.032*CL	4.819 + 0.029*CL
	t_{PHL}	6.602	4.305 + 0.046*CL	4.700 + 0.038*CL	5.054 + 0.033*CL
TN to PAD	t_R	4.452	2.140 + 0.046*CL	2.323 + 0.043*CL	2.456 + 0.041*CL
	t_F	4.677	2.270 + 0.048*CL	2.507 + 0.043*CL	2.684 + 0.041*CL
	t_{PLH}	6.201	4.266 + 0.039*CL	4.586 + 0.032*CL	4.871 + 0.029*CL
	t_{PHL}	6.671	4.362 + 0.046*CL	4.764 + 0.038*CL	5.122 + 0.033*CL
	t_{PLZ}	1.461	1.461 + 0.000*CL	1.461 + 0.000*CL	1.461 + 0.000*CL
	t_{PHZ}	4.028	4.027 + 0.000*CL	4.028 + 0.000*CL	4.028 + 0.000*CL
EN to PAD	t_R	4.452	2.140 + 0.046*CL	2.323 + 0.043*CL	2.456 + 0.041*CL
	t_F	4.677	2.269 + 0.048*CL	2.507 + 0.043*CL	2.684 + 0.041*CL
	t_{PLH}	6.267	4.332 + 0.039*CL	4.651 + 0.032*CL	4.936 + 0.029*CL
	t_{PHL}	6.736	4.428 + 0.046*CL	4.830 + 0.038*CL	5.187 + 0.033*CL
	t_{PLZ}	1.495	1.495 + 0.000*CL	1.495 + 0.000*CL	1.495 + 0.000*CL
	t_{PHZ}	4.062	4.061 + 0.000*CL	4.062 + 0.000*CL	4.062 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.420	2.257 + 0.043*CL	2.554 + 0.037*CL	2.793 + 0.034*CL
	t_F	4.856	2.570 + 0.046*CL	2.960 + 0.038*CL	3.262 + 0.034*CL
	t_{PLH}	6.197	4.263 + 0.039*CL	4.607 + 0.032*CL	4.929 + 0.028*CL
	t_{PHL}	6.544	4.102 + 0.049*CL	4.601 + 0.039*CL	5.058 + 0.033*CL
TN to PAD	t_R	4.421	2.257 + 0.043*CL	2.554 + 0.037*CL	2.794 + 0.034*CL
	t_F	4.859	2.575 + 0.046*CL	2.965 + 0.038*CL	3.266 + 0.034*CL
	t_{PLH}	6.248	4.313 + 0.039*CL	4.658 + 0.032*CL	4.980 + 0.028*CL
	t_{PHL}	6.620	4.179 + 0.049*CL	4.678 + 0.039*CL	5.135 + 0.033*CL
	t_{PLZ}	1.577	1.577 + 0.000*CL	1.577 + 0.000*CL	1.577 + 0.000*CL
	t_{PHZ}	2.417	2.416 + 0.000*CL	2.416 + 0.000*CL	2.417 + 0.000*CL
EN to PAD	t_R	4.421	2.257 + 0.043*CL	2.554 + 0.037*CL	2.794 + 0.034*CL
	t_F	4.859	2.575 + 0.046*CL	2.965 + 0.038*CL	3.266 + 0.034*CL
	t_{PLH}	6.313	4.379 + 0.039*CL	4.724 + 0.032*CL	5.045 + 0.028*CL
	t_{PHL}	6.686	4.244 + 0.049*CL	4.744 + 0.039*CL	5.199 + 0.033*CL
	t_{PLZ}	1.611	1.611 + 0.000*CL	1.611 + 0.000*CL	1.611 + 0.000*CL
	t_{PHZ}	2.451	2.450 + 0.000*CL	2.450 + 0.000*CL	2.450 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.993	2.229 + 0.035*CL	2.478 + 0.030*CL	2.682 + 0.028*CL
	t_F	4.165	2.199 + 0.039*CL	2.489 + 0.034*CL	2.739 + 0.030*CL
	t_{PLH}	5.987	4.259 + 0.035*CL	4.594 + 0.028*CL	4.901 + 0.024*CL
	t_{PHL}	6.534	4.509 + 0.041*CL	4.890 + 0.033*CL	5.238 + 0.028*CL
TN to PAD	t_R	3.994	2.230 + 0.035*CL	2.480 + 0.030*CL	2.683 + 0.028*CL
	t_F	4.167	2.201 + 0.039*CL	2.491 + 0.034*CL	2.741 + 0.030*CL
	t_{PLH}	6.039	4.311 + 0.035*CL	4.646 + 0.028*CL	4.954 + 0.024*CL
	t_{PHL}	6.611	4.587 + 0.040*CL	4.967 + 0.033*CL	5.315 + 0.028*CL
	t_{PLZ}	1.273	1.273 + 0.000*CL	1.273 + 0.000*CL	1.273 + 0.000*CL
	t_{PHZ}	3.132	3.131 + 0.000*CL	3.132 + 0.000*CL	3.132 + 0.000*CL
EN to PAD	t_R	3.994	2.230 + 0.035*CL	2.480 + 0.030*CL	2.683 + 0.028*CL
	t_F	4.167	2.201 + 0.039*CL	2.491 + 0.034*CL	2.741 + 0.030*CL
	t_{PLH}	6.104	4.376 + 0.035*CL	4.712 + 0.028*CL	5.019 + 0.024*CL
	t_{PHL}	6.676	4.652 + 0.040*CL	5.033 + 0.033*CL	5.380 + 0.028*CL
	t_{PLZ}	1.307	1.307 + 0.000*CL	1.307 + 0.000*CL	1.307 + 0.000*CL
	t_{PHZ}	3.166	3.165 + 0.000*CL	3.165 + 0.000*CL	3.166 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.868	2.138 + 0.035*CL	2.426 + 0.029*CL	2.665 + 0.026*CL
	t_F	4.135	2.247 + 0.038*CL	2.569 + 0.031*CL	2.844 + 0.028*CL
	t_{PLH}	5.905	4.250 + 0.033*CL	4.570 + 0.027*CL	4.864 + 0.023*CL
	t_{PHL}	6.558	4.552 + 0.040*CL	4.946 + 0.032*CL	5.306 + 0.027*CL
TN to PAD	t_R	3.869	2.136 + 0.035*CL	2.426 + 0.029*CL	2.666 + 0.026*CL
	t_F	4.138	2.251 + 0.038*CL	2.572 + 0.031*CL	2.848 + 0.028*CL
	t_{PLH}	5.958	4.302 + 0.033*CL	4.623 + 0.027*CL	4.917 + 0.023*CL
	t_{PHL}	6.635	4.630 + 0.040*CL	5.024 + 0.032*CL	5.385 + 0.027*CL
	t_{PLZ}	1.541	1.541 + 0.000*CL	1.541 + 0.000*CL	1.542 + 0.000*CL
	t_{PHZ}	3.363	3.362 + 0.000*CL	3.362 + 0.000*CL	3.363 + 0.000*CL
EN to PAD	t_R	3.869	2.136 + 0.035*CL	2.426 + 0.029*CL	2.666 + 0.026*CL
	t_F	4.138	2.251 + 0.038*CL	2.572 + 0.031*CL	2.848 + 0.028*CL
	t_{PLH}	6.023	4.368 + 0.033*CL	4.689 + 0.027*CL	4.982 + 0.023*CL
	t_{PHL}	6.700	4.696 + 0.040*CL	5.089 + 0.032*CL	5.450 + 0.027*CL
	t_{PLZ}	1.575	1.575 + 0.000*CL	1.575 + 0.000*CL	1.575 + 0.000*CL
	t_{PHZ}	3.397	3.395 + 0.000*CL	3.396 + 0.000*CL	3.397 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOT1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	22.581	2.531 + 0.401*CL	2.747 + 0.397*CL	2.927 + 0.394*CL
	t_F	25.239	4.211 + 0.421*CL	4.089 + 0.423*CL	3.984 + 0.424*CL
	t_{PLH}	11.246	2.109 + 0.183*CL	2.198 + 0.181*CL	2.273 + 0.180*CL
	t_{PHL}	13.028	1.839 + 0.224*CL	1.922 + 0.222*CL	2.003 + 0.221*CL
TN to PAD	t_R	22.582	2.532 + 0.401*CL	2.748 + 0.397*CL	2.931 + 0.394*CL
	t_F	25.121	4.161 + 0.419*CL	4.013 + 0.422*CL	3.902 + 0.424*CL
	t_{PLH}	11.298	2.160 + 0.183*CL	2.250 + 0.181*CL	2.322 + 0.180*CL
	t_{PHL}	12.914	1.837 + 0.222*CL	1.886 + 0.221*CL	1.946 + 0.220*CL
	t_{PLZ}	0.591	0.591 + 0.000*CL	0.591 + 0.000*CL	0.591 + 0.000*CL
	t_{PHZ}	1.694	1.694 + 0.000*CL	1.694 + 0.000*CL	1.694 + 0.000*CL
EN to PAD	t_R	22.582	2.532 + 0.401*CL	2.748 + 0.397*CL	2.931 + 0.394*CL
	t_F	25.121	4.161 + 0.419*CL	4.013 + 0.422*CL	3.902 + 0.424*CL
	t_{PLH}	11.364	2.225 + 0.183*CL	2.318 + 0.181*CL	2.387 + 0.180*CL
	t_{PHL}	12.979	1.903 + 0.222*CL	1.949 + 0.221*CL	2.015 + 0.220*CL
	t_{PLZ}	0.625	0.625 + 0.000*CL	0.625 + 0.000*CL	0.625 + 0.000*CL
	t_{PHZ}	1.728	1.728 + 0.000*CL	1.728 + 0.000*CL	1.728 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PTOT2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	15.351	1.761 + 0.272*CL	1.937 + 0.268*CL	2.096 + 0.266*CL
	t_F	13.477	2.314 + 0.223*CL	2.249 + 0.225*CL	2.216 + 0.225*CL
	t_{PLH}	7.997	1.731 + 0.125*CL	1.799 + 0.124*CL	1.865 + 0.123*CL
	t_{PHL}	7.083	0.941 + 0.123*CL	1.054 + 0.121*CL	1.134 + 0.120*CL
TN to PAD	t_R	15.352	1.760 + 0.272*CL	1.940 + 0.268*CL	2.096 + 0.266*CL
	t_F	13.363	2.264 + 0.222*CL	2.177 + 0.224*CL	2.135 + 0.224*CL
	t_{PLH}	8.048	1.780 + 0.125*CL	1.850 + 0.124*CL	1.916 + 0.123*CL
	t_{PHL}	6.984	0.933 + 0.121*CL	1.018 + 0.119*CL	1.085 + 0.118*CL
	t_{PLZ}	0.428	0.428 + 0.000*CL	0.428 + 0.000*CL	0.428 + 0.000*CL
	t_{PHZ}	2.394	2.395 + 0.000*CL	2.394 + 0.000*CL	2.394 + 0.000*CL
EN to PAD	t_R	15.352	1.760 + 0.272*CL	1.940 + 0.268*CL	2.096 + 0.266*CL
	t_F	13.363	2.264 + 0.222*CL	2.177 + 0.224*CL	2.135 + 0.224*CL
	t_{PLH}	8.113	1.846 + 0.125*CL	1.916 + 0.124*CL	1.978 + 0.123*CL
	t_{PHL}	7.049	0.998 + 0.121*CL	1.083 + 0.119*CL	1.152 + 0.118*CL
	t_{PLZ}	0.463	0.463 + 0.000*CL	0.463 + 0.000*CL	0.463 + 0.000*CL
	t_{PHZ}	2.428	2.429 + 0.000*CL	2.428 + 0.000*CL	2.428 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOT4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	7.837	0.896 + 0.139*CL	1.012 + 0.137*CL	1.134 + 0.135*CL
	t_F	6.949	1.530 + 0.108*CL	1.396 + 0.111*CL	1.311 + 0.112*CL
	t_{PLH}	4.286	1.149 + 0.063*CL	1.189 + 0.062*CL	1.234 + 0.061*CL
	t_{PHL}	3.858	0.763 + 0.062*CL	0.800 + 0.061*CL	0.835 + 0.061*CL
TN to PAD	t_R	7.838	0.898 + 0.139*CL	1.013 + 0.136*CL	1.134 + 0.135*CL
	t_F	6.853	1.488 + 0.107*CL	1.337 + 0.110*CL	1.241 + 0.112*CL
	t_{PLH}	4.337	1.198 + 0.063*CL	1.240 + 0.062*CL	1.285 + 0.061*CL
	t_{PHL}	3.801	0.784 + 0.060*CL	0.798 + 0.060*CL	0.818 + 0.060*CL
	t_{PLZ}	0.513	0.513 + 0.000*CL	0.513 + 0.000*CL	0.513 + 0.000*CL
	t_{PHZ}	2.389	2.391 + 0.000*CL	2.389 + 0.000*CL	2.388 + 0.000*CL
EN to PAD	t_R	7.838	0.898 + 0.139*CL	1.013 + 0.136*CL	1.134 + 0.135*CL
	t_F	6.853	1.488 + 0.107*CL	1.337 + 0.110*CL	1.240 + 0.112*CL
	t_{PLH}	4.403	1.264 + 0.063*CL	1.305 + 0.062*CL	1.350 + 0.061*CL
	t_{PHL}	3.866	0.849 + 0.060*CL	0.864 + 0.060*CL	0.883 + 0.060*CL
	t_{PLZ}	0.547	0.547 + 0.000*CL	0.547 + 0.000*CL	0.547 + 0.000*CL
	t_{PHZ}	2.423	2.425 + 0.000*CL	2.423 + 0.000*CL	2.422 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PTOT6_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.502	0.676 + 0.097*CL	0.731 + 0.095*CL	0.803 + 0.094*CL
	t_F	4.700	1.065 + 0.073*CL	0.997 + 0.074*CL	0.928 + 0.075*CL
	t_{PLH}	3.443	1.253 + 0.044*CL	1.276 + 0.043*CL	1.303 + 0.043*CL
	t_{PHL}	2.900	0.825 + 0.042*CL	0.841 + 0.041*CL	0.862 + 0.041*CL
TN to PAD	t_R	5.503	0.677 + 0.097*CL	0.732 + 0.095*CL	0.805 + 0.094*CL
	t_F	4.568	0.967 + 0.072*CL	0.894 + 0.073*CL	0.824 + 0.074*CL
	t_{PLH}	3.495	1.302 + 0.044*CL	1.327 + 0.043*CL	1.355 + 0.043*CL
	t_{PHL}	2.818	0.804 + 0.040*CL	0.811 + 0.040*CL	0.825 + 0.040*CL
	t_{PLZ}	0.595	0.596 + 0.000*CL	0.595 + 0.000*CL	0.595 + 0.000*CL
	t_{PHZ}	3.828	3.843 + 0.000*CL	3.828 + 0.000*CL	3.821 + 0.000*CL
EN to PAD	t_R	5.503	0.677 + 0.097*CL	0.732 + 0.095*CL	0.805 + 0.094*CL
	t_F	4.568	0.968 + 0.072*CL	0.894 + 0.073*CL	0.824 + 0.074*CL
	t_{PLH}	3.560	1.368 + 0.044*CL	1.392 + 0.043*CL	1.420 + 0.043*CL
	t_{PHL}	2.883	0.869 + 0.040*CL	0.876 + 0.040*CL	0.891 + 0.040*CL
	t_{PLZ}	0.629	0.629 + 0.000*CL	0.629 + 0.000*CL	0.629 + 0.000*CL
	t_{PHZ}	3.862	3.877 + 0.000*CL	3.862 + 0.000*CL	3.856 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PTOT4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	8.104	1.346 + 0.135*CL	1.393 + 0.134*CL	1.448 + 0.133*CL
	t_F	7.598	2.488 + 0.102*CL	2.256 + 0.107*CL	2.060 + 0.109*CL
	t_{PLH}	5.561	2.395 + 0.063*CL	2.458 + 0.062*CL	2.510 + 0.061*CL
	t_{PHL}	5.504	2.314 + 0.064*CL	2.392 + 0.062*CL	2.447 + 0.061*CL
TN to PAD	t_R	8.104	1.347 + 0.135*CL	1.393 + 0.134*CL	1.448 + 0.133*CL
	t_F	7.537	2.484 + 0.101*CL	2.235 + 0.106*CL	2.025 + 0.109*CL
	t_{PLH}	5.612	2.444 + 0.063*CL	2.509 + 0.062*CL	2.561 + 0.061*CL
	t_{PHL}	5.472	2.346 + 0.063*CL	2.405 + 0.061*CL	2.451 + 0.061*CL
	t_{PLZ}	0.531	0.531 + 0.000*CL	0.531 + 0.000*CL	0.531 + 0.000*CL
	t_{PHZ}	1.936	1.937 + 0.000*CL	1.936 + 0.000*CL	1.936 + 0.000*CL
EN to PAD	t_R	8.104	1.347 + 0.135*CL	1.393 + 0.134*CL	1.448 + 0.133*CL
	t_F	7.537	2.484 + 0.101*CL	2.235 + 0.106*CL	2.025 + 0.109*CL
	t_{PLH}	5.677	2.510 + 0.063*CL	2.574 + 0.062*CL	2.626 + 0.061*CL
	t_{PHL}	5.538	2.411 + 0.063*CL	2.471 + 0.061*CL	2.516 + 0.061*CL
	t_{PLZ}	0.565	0.565 + 0.000*CL	0.565 + 0.000*CL	0.565 + 0.000*CL
	t_{PHZ}	1.970	1.971 + 0.000*CL	1.970 + 0.000*CL	1.970 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PTOT6SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.516	2.034 + 0.090*CL	2.024 + 0.090*CL	1.997 + 0.090*CL
	t_F	5.440	2.191 + 0.065*CL	2.045 + 0.068*CL	1.841 + 0.071*CL
	t_{PLH}	6.481	4.011 + 0.049*CL	4.189 + 0.046*CL	4.317 + 0.044*CL
	t_{PHL}	4.648	2.377 + 0.045*CL	2.500 + 0.043*CL	2.590 + 0.042*CL
TN to PAD	t_R	6.516	2.033 + 0.090*CL	2.024 + 0.090*CL	1.997 + 0.090*CL
	t_F	5.392	2.214 + 0.064*CL	2.050 + 0.067*CL	1.832 + 0.070*CL
	t_{PLH}	6.533	4.062 + 0.049*CL	4.240 + 0.046*CL	4.369 + 0.044*CL
	t_{PHL}	4.591	2.372 + 0.044*CL	2.484 + 0.042*CL	2.571 + 0.041*CL
	t_{PLZ}	0.954	0.954 + 0.000*CL	0.954 + 0.000*CL	0.954 + 0.000*CL
	t_{PHZ}	2.404	2.410 + 0.000*CL	2.404 + 0.000*CL	2.403 + 0.000*CL
EN to PAD	t_R	6.516	2.033 + 0.090*CL	2.024 + 0.090*CL	1.997 + 0.090*CL
	t_F	5.392	2.214 + 0.064*CL	2.050 + 0.067*CL	1.832 + 0.070*CL
	t_{PLH}	6.598	4.128 + 0.049*CL	4.306 + 0.046*CL	4.434 + 0.044*CL
	t_{PHL}	4.657	2.437 + 0.044*CL	2.549 + 0.042*CL	2.636 + 0.041*CL
	t_{PLZ}	0.988	0.988 + 0.000*CL	0.988 + 0.000*CL	0.988 + 0.000*CL
	t_{PHZ}	2.438	2.444 + 0.000*CL	2.438 + 0.000*CL	2.437 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	26.043	1.408 + 0.493*CL	1.401 + 0.493*CL	1.398 + 0.493*CL
	t_F	22.782	1.225 + 0.431*CL	1.216 + 0.431*CL	1.213 + 0.431*CL
	t_{PLH}	13.279	1.406 + 0.237*CL	1.407 + 0.237*CL	1.410 + 0.237*CL
	t_{PHL}	12.586	1.449 + 0.223*CL	1.448 + 0.223*CL	1.448 + 0.223*CL
TN to PAD	t_R	26.043	1.408 + 0.493*CL	1.401 + 0.493*CL	1.398 + 0.493*CL
	t_F	22.782	1.225 + 0.431*CL	1.216 + 0.431*CL	1.213 + 0.431*CL
	t_{PLH}	13.526	1.653 + 0.237*CL	1.652 + 0.237*CL	1.655 + 0.237*CL
	t_{PHL}	12.804	1.665 + 0.223*CL	1.664 + 0.223*CL	1.667 + 0.223*CL
	t_{PLZ}	1.013	1.013 + 0.000*CL	1.013 + 0.000*CL	1.013 + 0.000*CL
	t_{PHZ}	0.962	0.962 + 0.000*CL	0.962 + 0.000*CL	0.962 + 0.000*CL
EN to PAD	t_R	26.043	1.408 + 0.493*CL	1.401 + 0.493*CL	1.398 + 0.493*CL
	t_F	22.782	1.225 + 0.431*CL	1.216 + 0.431*CL	1.213 + 0.431*CL
	t_{PLH}	13.632	1.759 + 0.237*CL	1.760 + 0.237*CL	1.760 + 0.237*CL
	t_{PHL}	12.910	1.771 + 0.223*CL	1.772 + 0.223*CL	1.772 + 0.223*CL
	t_{PLZ}	1.088	1.088 + 0.000*CL	1.088 + 0.000*CL	1.088 + 0.000*CL
	t_{PHZ}	1.037	1.037 + 0.000*CL	1.037 + 0.000*CL	1.037 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.053	0.741 + 0.246*CL	0.737 + 0.246*CL	0.731 + 0.246*CL
	t_F	12.991	0.713 + 0.246*CL	0.707 + 0.246*CL	0.704 + 0.246*CL
	t_{PLH}	7.122	1.185 + 0.119*CL	1.187 + 0.119*CL	1.186 + 0.119*CL
	t_{PHL}	7.704	1.106 + 0.132*CL	1.105 + 0.132*CL	1.107 + 0.132*CL
TN to PAD	t_R	13.053	0.741 + 0.246*CL	0.737 + 0.246*CL	0.731 + 0.246*CL
	t_F	12.991	0.713 + 0.246*CL	0.707 + 0.246*CL	0.704 + 0.246*CL
	t_{PLH}	7.370	1.430 + 0.119*CL	1.433 + 0.119*CL	1.431 + 0.119*CL
	t_{PHL}	7.920	1.319 + 0.132*CL	1.319 + 0.132*CL	1.321 + 0.132*CL
	t_{PLZ}	0.911	0.911 + 0.000*CL	0.911 + 0.000*CL	0.911 + 0.000*CL
	t_{PHZ}	1.115	1.115 + 0.000*CL	1.115 + 0.000*CL	1.115 + 0.000*CL
EN to PAD	t_R	13.053	0.741 + 0.246*CL	0.737 + 0.246*CL	0.731 + 0.246*CL
	t_F	12.991	0.713 + 0.246*CL	0.707 + 0.246*CL	0.704 + 0.246*CL
	t_{PLH}	7.475	1.537 + 0.119*CL	1.538 + 0.119*CL	1.540 + 0.119*CL
	t_{PHL}	8.026	1.425 + 0.132*CL	1.426 + 0.132*CL	1.426 + 0.132*CL
	t_{PLZ}	0.986	0.986 + 0.000*CL	0.986 + 0.000*CL	0.986 + 0.000*CL
	t_{PHZ}	1.190	1.190 + 0.000*CL	1.190 + 0.000*CL	1.190 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.568	0.423 + 0.123*CL	0.414 + 0.123*CL	0.409 + 0.123*CL
	t_F	6.518	0.386 + 0.123*CL	0.381 + 0.123*CL	0.378 + 0.123*CL
	t_{PLH}	4.194	1.220 + 0.059*CL	1.224 + 0.059*CL	1.226 + 0.059*CL
	t_{PHL}	4.298	1.005 + 0.066*CL	1.003 + 0.066*CL	1.000 + 0.066*CL
TN to PAD	t_R	6.568	0.423 + 0.123*CL	0.414 + 0.123*CL	0.409 + 0.123*CL
	t_F	6.518	0.384 + 0.123*CL	0.381 + 0.123*CL	0.378 + 0.123*CL
	t_{PLH}	4.442	1.465 + 0.060*CL	1.471 + 0.059*CL	1.473 + 0.059*CL
	t_{PHL}	4.506	1.199 + 0.066*CL	1.204 + 0.066*CL	1.206 + 0.066*CL
	t_{PLZ}	1.016	1.016 + 0.000*CL	1.016 + 0.000*CL	1.016 + 0.000*CL
	t_{PHZ}	1.415	1.415 + 0.000*CL	1.415 + 0.000*CL	1.415 + 0.000*CL
EN to PAD	t_R	6.568	0.423 + 0.123*CL	0.414 + 0.123*CL	0.409 + 0.123*CL
	t_F	6.518	0.384 + 0.123*CL	0.381 + 0.123*CL	0.378 + 0.123*CL
	t_{PLH}	4.547	1.572 + 0.060*CL	1.577 + 0.059*CL	1.579 + 0.059*CL
	t_{PHL}	4.611	1.305 + 0.066*CL	1.310 + 0.066*CL	1.311 + 0.066*CL
	t_{PLZ}	1.091	1.091 + 0.000*CL	1.091 + 0.000*CL	1.091 + 0.000*CL
	t_{PHZ}	1.490	1.490 + 0.000*CL	1.490 + 0.000*CL	1.490 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.405	0.426 + 0.060*CL	0.379 + 0.061*CL	0.342 + 0.061*CL
	t_F	3.314	0.330 + 0.060*CL	0.279 + 0.061*CL	0.241 + 0.061*CL
	t_{PLH}	3.019	1.514 + 0.030*CL	1.527 + 0.030*CL	1.533 + 0.030*CL
	t_{PHL}	2.743	1.137 + 0.032*CL	1.117 + 0.033*CL	1.103 + 0.033*CL
TN to PAD	t_R	3.405	0.426 + 0.060*CL	0.379 + 0.061*CL	0.341 + 0.061*CL
	t_F	3.299	0.249 + 0.061*CL	0.238 + 0.061*CL	0.231 + 0.061*CL
	t_{PLH}	3.266	1.760 + 0.030*CL	1.774 + 0.030*CL	1.781 + 0.030*CL
	t_{PHL}	2.902	1.236 + 0.033*CL	1.246 + 0.033*CL	1.251 + 0.033*CL
	t_{PLZ}	1.219	1.219 + 0.000*CL	1.219 + 0.000*CL	1.219 + 0.000*CL
	t_{PHZ}	2.009	2.009 + 0.000*CL	2.009 + 0.000*CL	2.009 + 0.000*CL
EN to PAD	t_R	3.405	0.426 + 0.060*CL	0.379 + 0.061*CL	0.341 + 0.061*CL
	t_F	3.299	0.249 + 0.061*CL	0.238 + 0.061*CL	0.231 + 0.061*CL
	t_{PLH}	3.372	1.867 + 0.030*CL	1.880 + 0.030*CL	1.886 + 0.030*CL
	t_{PHL}	3.008	1.342 + 0.033*CL	1.351 + 0.033*CL	1.357 + 0.033*CL
	t_{PLZ}	1.294	1.294 + 0.000*CL	1.294 + 0.000*CL	1.294 + 0.000*CL
	t_{PHZ}	2.083	2.083 + 0.000*CL	2.083 + 0.000*CL	2.083 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.290	0.316 + 0.039*CL	0.280 + 0.040*CL	0.251 + 0.041*CL
	t_F	2.280	0.361 + 0.038*CL	0.302 + 0.040*CL	0.256 + 0.040*CL
	t_{PLH}	2.376	1.370 + 0.020*CL	1.381 + 0.020*CL	1.385 + 0.020*CL
	t_{PHL}	2.296	1.266 + 0.021*CL	1.235 + 0.021*CL	1.213 + 0.022*CL
TN to PAD	t_R	2.290	0.316 + 0.039*CL	0.280 + 0.040*CL	0.251 + 0.041*CL
	t_F	2.228	0.215 + 0.040*CL	0.198 + 0.041*CL	0.186 + 0.041*CL
	t_{PLH}	2.623	1.616 + 0.020*CL	1.628 + 0.020*CL	1.633 + 0.020*CL
	t_{PHL}	2.415	1.297 + 0.022*CL	1.306 + 0.022*CL	1.313 + 0.022*CL
	t_{PLZ}	1.168	1.168 + 0.000*CL	1.168 + 0.000*CL	1.168 + 0.000*CL
	t_{PHZ}	2.231	2.231 + 0.000*CL	2.231 + 0.000*CL	2.231 + 0.000*CL
EN to PAD	t_R	2.290	0.316 + 0.039*CL	0.280 + 0.040*CL	0.251 + 0.041*CL
	t_F	2.228	0.215 + 0.040*CL	0.198 + 0.041*CL	0.186 + 0.041*CL
	t_{PLH}	2.729	1.722 + 0.020*CL	1.734 + 0.020*CL	1.738 + 0.020*CL
	t_{PHL}	2.521	1.404 + 0.022*CL	1.413 + 0.022*CL	1.419 + 0.022*CL
	t_{PLZ}	1.243	1.243 + 0.000*CL	1.243 + 0.000*CL	1.243 + 0.000*CL
	t_{PHZ}	2.306	2.306 + 0.000*CL	2.306 + 0.000*CL	2.306 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.831	0.398 + 0.029*CL	0.361 + 0.029*CL	0.326 + 0.030*CL
	t_F	1.853	0.522 + 0.027*CL	0.434 + 0.028*CL	0.371 + 0.029*CL
	t_{PLH}	2.302	1.509 + 0.016*CL	1.544 + 0.015*CL	1.560 + 0.015*CL
	t_{PHL}	2.193	1.436 + 0.015*CL	1.433 + 0.015*CL	1.399 + 0.016*CL
TN to PAD	t_R	1.831	0.397 + 0.029*CL	0.361 + 0.029*CL	0.325 + 0.030*CL
	t_F	1.725	0.242 + 0.030*CL	0.222 + 0.030*CL	0.204 + 0.030*CL
	t_{PLH}	2.550	1.756 + 0.016*CL	1.791 + 0.015*CL	1.807 + 0.015*CL
	t_{PHL}	2.227	1.372 + 0.017*CL	1.389 + 0.017*CL	1.398 + 0.017*CL
	t_{PLZ}	1.268	1.268 + 0.000*CL	1.268 + 0.000*CL	1.268 + 0.000*CL
	t_{PHZ}	2.670	2.670 + 0.000*CL	2.670 + 0.000*CL	2.670 + 0.000*CL
EN to PAD	t_R	1.831	0.397 + 0.029*CL	0.361 + 0.029*CL	0.325 + 0.030*CL
	t_F	1.725	0.241 + 0.030*CL	0.222 + 0.030*CL	0.204 + 0.030*CL
	t_{PLH}	2.656	1.862 + 0.016*CL	1.897 + 0.015*CL	1.913 + 0.015*CL
	t_{PHL}	2.332	1.478 + 0.017*CL	1.495 + 0.017*CL	1.503 + 0.017*CL
	t_{PLZ}	1.343	1.343 + 0.000*CL	1.343 + 0.000*CL	1.343 + 0.000*CL
	t_{PHZ}	2.745	2.744 + 0.000*CL	2.745 + 0.000*CL	2.745 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.600	0.479 + 0.022*CL	0.456 + 0.023*CL	0.421 + 0.023*CL
	t_F	1.674	0.739 + 0.019*CL	0.614 + 0.021*CL	0.525 + 0.022*CL
	t_{PLH}	2.318	1.623 + 0.014*CL	1.684 + 0.013*CL	1.720 + 0.012*CL
	t_{PHL}	2.205	1.562 + 0.013*CL	1.601 + 0.012*CL	1.607 + 0.012*CL
TN to PAD	t_R	1.600	0.478 + 0.022*CL	0.455 + 0.023*CL	0.421 + 0.023*CL
	t_F	1.446	0.278 + 0.023*CL	0.262 + 0.024*CL	0.242 + 0.024*CL
	t_{PLH}	2.567	1.871 + 0.014*CL	1.931 + 0.013*CL	1.968 + 0.012*CL
	t_{PHL}	2.150	1.439 + 0.014*CL	1.469 + 0.014*CL	1.485 + 0.013*CL
	t_{PLZ}	1.367	1.367 + 0.000*CL	1.367 + 0.000*CL	1.368 + 0.000*CL
	t_{PHZ}	3.108	3.106 + 0.000*CL	3.107 + 0.000*CL	3.108 + 0.000*CL
EN to PAD	t_R	1.600	0.478 + 0.022*CL	0.455 + 0.023*CL	0.421 + 0.023*CL
	t_F	1.446	0.278 + 0.023*CL	0.262 + 0.024*CL	0.242 + 0.024*CL
	t_{PLH}	2.672	1.977 + 0.014*CL	2.037 + 0.013*CL	2.074 + 0.012*CL
	t_{PHL}	2.256	1.545 + 0.014*CL	1.575 + 0.014*CL	1.591 + 0.013*CL
	t_{PLZ}	1.442	1.442 + 0.000*CL	1.442 + 0.000*CL	1.442 + 0.000*CL
	t_{PHZ}	3.182	3.181 + 0.000*CL	3.182 + 0.000*CL	3.182 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.481	0.550 + 0.019*CL	0.545 + 0.019*CL	0.521 + 0.019*CL
	t_F	1.636	0.917 + 0.014*CL	0.844 + 0.016*CL	0.717 + 0.018*CL
	t_{PLH}	2.370	1.722 + 0.013*CL	1.802 + 0.011*CL	1.858 + 0.011*CL
	t_{PHL}	2.258	1.683 + 0.012*CL	1.730 + 0.011*CL	1.767 + 0.010*CL
TN to PAD	t_R	1.480	0.548 + 0.019*CL	0.544 + 0.019*CL	0.520 + 0.019*CL
	t_F	1.279	0.313 + 0.019*CL	0.305 + 0.019*CL	0.289 + 0.020*CL
	t_{PLH}	2.618	1.970 + 0.013*CL	2.050 + 0.011*CL	2.106 + 0.011*CL
	t_{PHL}	2.125	1.497 + 0.013*CL	1.540 + 0.012*CL	1.567 + 0.011*CL
	t_{PLZ}	1.466	1.466 + 0.000*CL	1.466 + 0.000*CL	1.466 + 0.000*CL
	t_{PHZ}	3.544	3.542 + 0.000*CL	3.543 + 0.000*CL	3.544 + 0.000*CL
EN to PAD	t_R	1.480	0.548 + 0.019*CL	0.544 + 0.019*CL	0.520 + 0.019*CL
	t_F	1.279	0.313 + 0.019*CL	0.305 + 0.019*CL	0.289 + 0.020*CL
	t_{PLH}	2.724	2.076 + 0.013*CL	2.156 + 0.011*CL	2.212 + 0.011*CL
	t_{PHL}	2.231	1.604 + 0.013*CL	1.646 + 0.012*CL	1.673 + 0.011*CL
	t_{PLZ}	1.541	1.541 + 0.000*CL	1.541 + 0.000*CL	1.541 + 0.000*CL
	t_{PHZ}	3.619	3.617 + 0.000*CL	3.618 + 0.000*CL	3.619 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.917	1.007 + 0.118*CL	0.919 + 0.120*CL	0.832 + 0.121*CL
	t_F	6.766	0.814 + 0.119*CL	0.749 + 0.120*CL	0.681 + 0.121*CL
	t_{PLH}	6.113	3.044 + 0.061*CL	3.115 + 0.060*CL	3.146 + 0.060*CL
	t_{PHL}	5.641	2.267 + 0.067*CL	2.323 + 0.066*CL	2.343 + 0.066*CL
TN to PAD	t_R	6.917	1.008 + 0.118*CL	0.919 + 0.120*CL	0.832 + 0.121*CL
	t_F	6.766	0.815 + 0.119*CL	0.750 + 0.120*CL	0.681 + 0.121*CL
	t_{PLH}	6.360	3.289 + 0.061*CL	3.361 + 0.060*CL	3.392 + 0.060*CL
	t_{PHL}	5.858	2.483 + 0.068*CL	2.540 + 0.066*CL	2.561 + 0.066*CL
	t_{PLZ}	1.299	1.299 + 0.000*CL	1.299 + 0.000*CL	1.299 + 0.000*CL
	t_{PHZ}	1.790	1.790 + 0.000*CL	1.790 + 0.000*CL	1.790 + 0.000*CL
EN to PAD	t_R	6.917	1.008 + 0.118*CL	0.919 + 0.120*CL	0.832 + 0.121*CL
	t_F	6.766	0.815 + 0.119*CL	0.750 + 0.120*CL	0.681 + 0.121*CL
	t_{PLH}	6.465	3.396 + 0.061*CL	3.467 + 0.060*CL	3.498 + 0.060*CL
	t_{PHL}	5.964	2.589 + 0.067*CL	2.646 + 0.066*CL	2.667 + 0.066*CL
	t_{PLZ}	1.374	1.374 + 0.000*CL	1.374 + 0.000*CL	1.374 + 0.000*CL
	t_{PHZ}	1.865	1.865 + 0.000*CL	1.865 + 0.000*CL	1.865 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.362	1.453 + 0.058*CL	1.484 + 0.058*CL	1.459 + 0.058*CL
	t_F	3.931	1.002 + 0.059*CL	1.017 + 0.058*CL	0.989 + 0.059*CL
	t_{PLH}	5.701	3.747 + 0.039*CL	3.970 + 0.035*CL	4.141 + 0.032*CL
	t_{PHL}	4.637	2.687 + 0.039*CL	2.842 + 0.036*CL	2.954 + 0.034*CL
TN to PAD	t_R	4.362	1.453 + 0.058*CL	1.484 + 0.058*CL	1.459 + 0.058*CL
	t_F	3.932	1.007 + 0.059*CL	1.019 + 0.058*CL	0.990 + 0.059*CL
	t_{PLH}	5.948	3.993 + 0.039*CL	4.217 + 0.035*CL	4.388 + 0.032*CL
	t_{PHL}	4.855	2.902 + 0.039*CL	3.059 + 0.036*CL	3.171 + 0.034*CL
	t_{PLZ}	1.525	1.525 + 0.000*CL	1.525 + 0.000*CL	1.525 + 0.000*CL
	t_{PHZ}	2.297	2.297 + 0.000*CL	2.297 + 0.000*CL	2.297 + 0.000*CL
EN to PAD	t_R	4.362	1.453 + 0.058*CL	1.484 + 0.058*CL	1.459 + 0.058*CL
	t_F	3.932	1.007 + 0.058*CL	1.019 + 0.058*CL	0.990 + 0.059*CL
	t_{PLH}	6.054	4.099 + 0.039*CL	4.323 + 0.035*CL	4.493 + 0.032*CL
	t_{PHL}	4.961	3.009 + 0.039*CL	3.165 + 0.036*CL	3.277 + 0.034*CL
	t_{PLZ}	1.599	1.599 + 0.000*CL	1.599 + 0.000*CL	1.599 + 0.000*CL
	t_{PHZ}	2.372	2.372 + 0.000*CL	2.372 + 0.000*CL	2.372 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.262	1.265 + 0.040*CL	1.331 + 0.039*CL	1.351 + 0.038*CL
	t_F	2.977	0.977 + 0.040*CL	1.038 + 0.039*CL	1.051 + 0.039*CL
	t_{PLH}	4.637	3.168 + 0.029*CL	3.370 + 0.025*CL	3.536 + 0.023*CL
	t_{PHL}	4.028	2.564 + 0.029*CL	2.725 + 0.026*CL	2.856 + 0.024*CL
TN to PAD	t_R	3.262	1.265 + 0.040*CL	1.331 + 0.039*CL	1.351 + 0.038*CL
	t_F	2.985	1.006 + 0.040*CL	1.053 + 0.039*CL	1.061 + 0.039*CL
	t_{PLH}	4.885	3.414 + 0.029*CL	3.617 + 0.025*CL	3.784 + 0.023*CL
	t_{PHL}	4.241	2.764 + 0.030*CL	2.933 + 0.026*CL	3.067 + 0.024*CL
	t_{PLZ}	1.585	1.585 + 0.000*CL	1.585 + 0.000*CL	1.585 + 0.000*CL
	t_{PHZ}	2.644	2.644 + 0.000*CL	2.644 + 0.000*CL	2.644 + 0.000*CL
EN to PAD	t_R	3.262	1.265 + 0.040*CL	1.331 + 0.039*CL	1.351 + 0.038*CL
	t_F	2.985	1.006 + 0.040*CL	1.053 + 0.039*CL	1.061 + 0.039*CL
	t_{PLH}	4.990	3.521 + 0.029*CL	3.723 + 0.025*CL	3.889 + 0.023*CL
	t_{PHL}	4.347	2.870 + 0.030*CL	3.039 + 0.026*CL	3.173 + 0.024*CL
	t_{PLZ}	1.660	1.660 + 0.000*CL	1.659 + 0.000*CL	1.660 + 0.000*CL
	t_{PHZ}	2.719	2.719 + 0.000*CL	2.719 + 0.000*CL	2.719 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.083	1.450 + 0.033*CL	1.567 + 0.030*CL	1.645 + 0.029*CL
	t_F	2.700	1.077 + 0.032*CL	1.192 + 0.030*CL	1.262 + 0.029*CL
	t_{PLH}	4.885	3.496 + 0.028*CL	3.730 + 0.023*CL	3.932 + 0.020*CL
	t_{PHL}	4.163	2.845 + 0.026*CL	3.029 + 0.023*CL	3.189 + 0.021*CL
TN to PAD	t_R	3.083	1.450 + 0.033*CL	1.566 + 0.030*CL	1.646 + 0.029*CL
	t_F	2.721	1.142 + 0.032*CL	1.231 + 0.030*CL	1.286 + 0.029*CL
	t_{PLH}	5.133	3.743 + 0.028*CL	3.978 + 0.023*CL	4.180 + 0.020*CL
	t_{PHL}	4.369	3.025 + 0.027*CL	3.224 + 0.023*CL	3.392 + 0.021*CL
	t_{PLZ}	1.802	1.802 + 0.000*CL	1.802 + 0.000*CL	1.802 + 0.000*CL
	t_{PHZ}	3.140	3.139 + 0.000*CL	3.140 + 0.000*CL	3.140 + 0.000*CL
EN to PAD	t_R	3.083	1.450 + 0.033*CL	1.566 + 0.030*CL	1.646 + 0.029*CL
	t_F	2.721	1.142 + 0.032*CL	1.231 + 0.030*CL	1.287 + 0.029*CL
	t_{PLH}	5.239	3.850 + 0.028*CL	4.084 + 0.023*CL	4.286 + 0.020*CL
	t_{PHL}	4.475	3.132 + 0.027*CL	3.330 + 0.023*CL	3.499 + 0.021*CL
	t_{PLZ}	1.877	1.877 + 0.000*CL	1.877 + 0.000*CL	1.877 + 0.000*CL
	t_{PHZ}	3.214	3.214 + 0.000*CL	3.214 + 0.000*CL	3.214 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.716	1.421 + 0.026*CL	1.520 + 0.024*CL	1.585 + 0.023*CL
	t_F	2.465	1.062 + 0.028*CL	1.191 + 0.025*CL	1.290 + 0.024*CL
	t_{PLH}	4.732	3.521 + 0.024*CL	3.749 + 0.020*CL	3.942 + 0.017*CL
	t_{PHL}	4.174	2.988 + 0.024*CL	3.163 + 0.020*CL	3.323 + 0.018*CL
TN to PAD	t_R	2.716	1.419 + 0.026*CL	1.520 + 0.024*CL	1.585 + 0.023*CL
	t_F	2.505	1.160 + 0.027*CL	1.262 + 0.025*CL	1.337 + 0.024*CL
	t_{PLH}	4.981	3.770 + 0.024*CL	3.998 + 0.020*CL	4.191 + 0.017*CL
	t_{PHL}	4.368	3.137 + 0.025*CL	3.337 + 0.021*CL	3.512 + 0.018*CL
	t_{PLZ}	1.853	1.852 + 0.000*CL	1.853 + 0.000*CL	1.853 + 0.000*CL
	t_{PHZ}	3.580	3.579 + 0.000*CL	3.580 + 0.000*CL	3.580 + 0.000*CL
EN to PAD	t_R	2.716	1.419 + 0.026*CL	1.520 + 0.024*CL	1.585 + 0.023*CL
	t_F	2.505	1.160 + 0.027*CL	1.262 + 0.025*CL	1.338 + 0.024*CL
	t_{PLH}	5.087	3.877 + 0.024*CL	4.104 + 0.020*CL	4.297 + 0.017*CL
	t_{PHL}	4.473	3.243 + 0.025*CL	3.443 + 0.021*CL	3.618 + 0.018*CL
	t_{PLZ}	1.927	1.927 + 0.000*CL	1.927 + 0.000*CL	1.927 + 0.000*CL
	t_{PHZ}	3.655	3.654 + 0.000*CL	3.654 + 0.000*CL	3.655 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.755	1.572 + 0.024*CL	1.695 + 0.021*CL	1.788 + 0.020*CL
	t_F	2.408	1.119 + 0.026*CL	1.267 + 0.023*CL	1.387 + 0.021*CL
	t_{PLH}	5.011	3.789 + 0.024*CL	4.038 + 0.019*CL	4.253 + 0.017*CL
	t_{PHL}	4.379	3.249 + 0.023*CL	3.421 + 0.019*CL	3.586 + 0.017*CL
TN to PAD	t_R	2.754	1.570 + 0.024*CL	1.694 + 0.021*CL	1.787 + 0.020*CL
	t_F	2.475	1.259 + 0.024*CL	1.378 + 0.022*CL	1.472 + 0.021*CL
	t_{PLH}	5.261	4.039 + 0.024*CL	4.289 + 0.019*CL	4.503 + 0.017*CL
	t_{PHL}	4.554	3.351 + 0.024*CL	3.565 + 0.020*CL	3.754 + 0.017*CL
	t_{PLZ}	2.026	2.026 + 0.000*CL	2.026 + 0.000*CL	2.026 + 0.000*CL
	t_{PHZ}	4.072	4.071 + 0.000*CL	4.072 + 0.000*CL	4.072 + 0.000*CL
EN to PAD	t_R	2.754	1.570 + 0.024*CL	1.693 + 0.021*CL	1.787 + 0.020*CL
	t_F	2.475	1.259 + 0.024*CL	1.378 + 0.022*CL	1.472 + 0.021*CL
	t_{PLH}	5.367	4.146 + 0.024*CL	4.395 + 0.019*CL	4.609 + 0.017*CL
	t_{PHL}	4.659	3.458 + 0.024*CL	3.671 + 0.020*CL	3.859 + 0.017*CL
	t_{PLZ}	2.101	2.101 + 0.000*CL	2.101 + 0.000*CL	2.101 + 0.000*CL
	t_{PHZ}	4.147	4.146 + 0.000*CL	4.147 + 0.000*CL	4.147 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.619	2.142 + 0.050*CL	2.441 + 0.044*CL	2.667 + 0.041*CL
	t_F	4.119	1.773 + 0.047*CL	2.032 + 0.042*CL	2.204 + 0.039*CL
	t_{PLH}	6.158	3.998 + 0.043*CL	4.377 + 0.036*CL	4.737 + 0.031*CL
	t_{PHL}	5.253	3.162 + 0.042*CL	3.517 + 0.035*CL	3.829 + 0.031*CL
TN to PAD	t_R	4.619	2.143 + 0.050*CL	2.441 + 0.044*CL	2.668 + 0.041*CL
	t_F	4.141	1.838 + 0.046*CL	2.073 + 0.041*CL	2.231 + 0.039*CL
	t_{PLH}	6.407	4.246 + 0.043*CL	4.626 + 0.036*CL	4.986 + 0.031*CL
	t_{PHL}	5.459	3.334 + 0.042*CL	3.711 + 0.035*CL	4.033 + 0.031*CL
	t_{PLZ}	1.992	1.992 + 0.000*CL	1.992 + 0.000*CL	1.992 + 0.000*CL
	t_{PHZ}	3.062	3.061 + 0.000*CL	3.062 + 0.000*CL	3.062 + 0.000*CL
EN to PAD	t_R	4.619	2.143 + 0.050*CL	2.441 + 0.044*CL	2.668 + 0.041*CL
	t_F	4.141	1.839 + 0.046*CL	2.073 + 0.041*CL	2.231 + 0.039*CL
	t_{PLH}	6.512	4.352 + 0.043*CL	4.732 + 0.036*CL	5.091 + 0.031*CL
	t_{PHL}	5.564	3.440 + 0.042*CL	3.817 + 0.035*CL	4.138 + 0.031*CL
	t_{PLZ}	2.067	2.067 + 0.000*CL	2.067 + 0.000*CL	2.067 + 0.000*CL
	t_{PHZ}	3.136	3.136 + 0.000*CL	3.136 + 0.000*CL	3.136 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.707	2.348 + 0.047*CL	2.788 + 0.038*CL	3.138 + 0.034*CL
	t_F	3.989	1.871 + 0.042*CL	2.201 + 0.036*CL	2.480 + 0.032*CL
	t_{PLH}	6.236	3.987 + 0.045*CL	4.424 + 0.036*CL	4.861 + 0.030*CL
	t_{PHL}	5.453	3.523 + 0.039*CL	3.856 + 0.032*CL	4.184 + 0.028*CL
TN to PAD	t_R	4.708	2.348 + 0.047*CL	2.789 + 0.038*CL	3.139 + 0.034*CL
	t_F	4.168	2.142 + 0.041*CL	2.487 + 0.034*CL	2.714 + 0.031*CL
	t_{PLH}	6.485	4.234 + 0.045*CL	4.673 + 0.036*CL	5.110 + 0.030*CL
	t_{PHL}	5.548	3.388 + 0.043*CL	3.856 + 0.034*CL	4.258 + 0.028*CL
	t_{PLZ}	2.395	2.395 + 0.000*CL	2.395 + 0.000*CL	2.396 + 0.000*CL
	t_{PHZ}	4.230	4.229 + 0.000*CL	4.230 + 0.000*CL	4.230 + 0.000*CL
EN to PAD	t_R	4.708	2.348 + 0.047*CL	2.789 + 0.038*CL	3.138 + 0.034*CL
	t_F	4.168	2.143 + 0.041*CL	2.486 + 0.034*CL	2.714 + 0.031*CL
	t_{PLH}	6.590	4.341 + 0.045*CL	4.779 + 0.036*CL	5.216 + 0.030*CL
	t_{PHL}	5.653	3.494 + 0.043*CL	3.962 + 0.034*CL	4.363 + 0.028*CL
	t_{PLZ}	2.470	2.470 + 0.000*CL	2.470 + 0.000*CL	2.470 + 0.000*CL
	t_{PHZ}	4.305	4.304 + 0.000*CL	4.305 + 0.000*CL	4.305 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.163	2.146 + 0.040*CL	2.434 + 0.035*CL	2.706 + 0.031*CL
	t_F	3.650	1.536 + 0.042*CL	1.925 + 0.034*CL	2.248 + 0.030*CL
	t_{PLH}	6.492	4.631 + 0.037*CL	4.972 + 0.030*CL	5.279 + 0.026*CL
	t_{PHL}	5.438	3.662 + 0.036*CL	3.941 + 0.030*CL	4.222 + 0.026*CL
TN to PAD	t_R	4.163	2.144 + 0.040*CL	2.433 + 0.035*CL	2.706 + 0.031*CL
	t_F	3.729	1.700 + 0.041*CL	2.059 + 0.033*CL	2.344 + 0.030*CL
	t_{PLH}	6.742	4.880 + 0.037*CL	5.222 + 0.030*CL	5.528 + 0.026*CL
	t_{PHL}	5.602	3.728 + 0.037*CL	4.063 + 0.031*CL	4.375 + 0.027*CL
	t_{PLZ}	2.444	2.444 + 0.000*CL	2.444 + 0.000*CL	2.444 + 0.000*CL
	t_{PHZ}	4.266	4.265 + 0.000*CL	4.266 + 0.000*CL	4.266 + 0.000*CL
EN to PAD	t_R	4.163	2.144 + 0.040*CL	2.433 + 0.035*CL	2.706 + 0.031*CL
	t_F	3.729	1.700 + 0.041*CL	2.059 + 0.033*CL	2.344 + 0.030*CL
	t_{PLH}	6.847	4.987 + 0.037*CL	5.328 + 0.030*CL	5.634 + 0.026*CL
	t_{PHL}	5.707	3.834 + 0.037*CL	4.169 + 0.031*CL	4.481 + 0.027*CL
	t_{PLZ}	2.519	2.518 + 0.000*CL	2.519 + 0.000*CL	2.518 + 0.000*CL
	t_{PHZ}	4.341	4.340 + 0.000*CL	4.340 + 0.000*CL	4.341 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.536	1.743 + 0.036*CL	2.027 + 0.030*CL	2.298 + 0.027*CL
	t_F	3.355	1.520 + 0.037*CL	1.816 + 0.031*CL	2.101 + 0.027*CL
	t_{PLH}	5.085	3.498 + 0.032*CL	3.771 + 0.026*CL	4.028 + 0.023*CL
	t_{PHL}	4.629	3.273 + 0.027*CL	3.365 + 0.025*CL	3.530 + 0.023*CL
TN to PAD	t_R	3.536	1.745 + 0.036*CL	2.028 + 0.030*CL	2.299 + 0.027*CL
	t_F	3.430	1.273 + 0.043*CL	1.789 + 0.033*CL	2.188 + 0.027*CL
	t_{PLH}	5.334	3.744 + 0.032*CL	4.019 + 0.026*CL	4.276 + 0.023*CL
	t_{PHL}	4.477	2.712 + 0.035*CL	2.980 + 0.030*CL	3.294 + 0.026*CL
	t_{PLZ}	2.665	2.665 + 0.000*CL	2.665 + 0.000*CL	2.665 + 0.000*CL
	t_{PHZ}	4.945	4.943 + 0.000*CL	4.944 + 0.000*CL	4.945 + 0.000*CL
EN to PAD	t_R	3.536	1.745 + 0.036*CL	2.028 + 0.030*CL	2.299 + 0.027*CL
	t_F	3.430	1.273 + 0.043*CL	1.789 + 0.033*CL	2.188 + 0.027*CL
	t_{PLH}	5.439	3.850 + 0.032*CL	4.125 + 0.026*CL	4.382 + 0.023*CL
	t_{PHL}	4.582	2.818 + 0.035*CL	3.086 + 0.030*CL	3.400 + 0.026*CL
	t_{PLZ}	2.740	2.740 + 0.000*CL	2.740 + 0.000*CL	2.740 + 0.000*CL
	t_{PHZ}	5.020	5.018 + 0.000*CL	5.019 + 0.000*CL	5.019 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	36.042	2.067 + 0.679*CL	2.066 + 0.680*CL	2.066 + 0.680*CL
	t_F	26.591	1.534 + 0.501*CL	1.529 + 0.501*CL	1.526 + 0.501*CL
	t_{PLH}	17.629	1.664 + 0.319*CL	1.663 + 0.319*CL	1.663 + 0.319*CL
	t_{PHL}	13.550	1.598 + 0.239*CL	1.600 + 0.239*CL	1.600 + 0.239*CL
TN to PAD	t_R	36.041	2.069 + 0.679*CL	2.065 + 0.680*CL	2.062 + 0.680*CL
	t_F	26.590	1.533 + 0.501*CL	1.528 + 0.501*CL	1.525 + 0.501*CL
	t_{PLH}	17.882	1.914 + 0.319*CL	1.914 + 0.319*CL	1.917 + 0.319*CL
	t_{PHL}	13.784	1.833 + 0.239*CL	1.832 + 0.239*CL	1.835 + 0.239*CL
	t_{PLZ}	1.187	1.187 + 0.000*CL	1.187 + 0.000*CL	1.187 + 0.000*CL
	t_{PHZ}	1.018	1.018 + 0.000*CL	1.018 + 0.000*CL	1.018 + 0.000*CL
EN to PAD	t_R	36.041	2.069 + 0.679*CL	2.065 + 0.680*CL	2.062 + 0.680*CL
	t_F	26.590	1.533 + 0.501*CL	1.528 + 0.501*CL	1.525 + 0.501*CL
	t_{PLH}	17.988	2.021 + 0.319*CL	2.022 + 0.319*CL	2.022 + 0.319*CL
	t_{PHL}	13.890	1.939 + 0.239*CL	1.940 + 0.239*CL	1.940 + 0.239*CL
	t_{PLZ}	1.262	1.262 + 0.000*CL	1.262 + 0.000*CL	1.262 + 0.000*CL
	t_{PHZ}	1.093	1.093 + 0.000*CL	1.093 + 0.000*CL	1.093 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	18.642	1.107 + 0.351*CL	1.104 + 0.351*CL	1.101 + 0.351*CL
	t_F	14.643	0.869 + 0.275*CL	0.865 + 0.276*CL	0.862 + 0.276*CL
	t_{PLH}	9.376	1.091 + 0.166*CL	1.091 + 0.166*CL	1.090 + 0.166*CL
	t_{PHL}	8.009	1.149 + 0.137*CL	1.149 + 0.137*CL	1.149 + 0.137*CL
TN to PAD	t_R	18.642	1.107 + 0.351*CL	1.104 + 0.351*CL	1.101 + 0.351*CL
	t_F	14.643	0.869 + 0.275*CL	0.865 + 0.276*CL	0.862 + 0.276*CL
	t_{PLH}	9.629	1.341 + 0.166*CL	1.343 + 0.166*CL	1.343 + 0.166*CL
	t_{PHL}	8.243	1.382 + 0.137*CL	1.382 + 0.137*CL	1.384 + 0.137*CL
	t_{PLZ}	0.983	0.983 + 0.000*CL	0.983 + 0.000*CL	0.983 + 0.000*CL
	t_{PHZ}	0.891	0.891 + 0.000*CL	0.891 + 0.000*CL	0.891 + 0.000*CL
EN to PAD	t_R	18.642	1.107 + 0.351*CL	1.104 + 0.351*CL	1.101 + 0.351*CL
	t_F	14.643	0.869 + 0.275*CL	0.865 + 0.276*CL	0.862 + 0.276*CL
	t_{PLH}	9.735	1.448 + 0.166*CL	1.448 + 0.166*CL	1.449 + 0.166*CL
	t_{PHL}	8.349	1.488 + 0.137*CL	1.488 + 0.137*CL	1.489 + 0.137*CL
	t_{PLZ}	1.058	1.058 + 0.000*CL	1.058 + 0.000*CL	1.058 + 0.000*CL
	t_{PHZ}	0.967	0.967 + 0.000*CL	0.967 + 0.000*CL	0.967 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	9.348	0.584 + 0.175*CL	0.583 + 0.175*CL	0.579 + 0.175*CL
	t_F	8.642	0.523 + 0.162*CL	0.521 + 0.162*CL	0.516 + 0.162*CL
	t_{PLH}	5.066	0.920 + 0.083*CL	0.922 + 0.083*CL	0.923 + 0.083*CL
	t_{PHL}	5.225	0.919 + 0.086*CL	0.920 + 0.086*CL	0.919 + 0.086*CL
TN to PAD	t_R	9.348	0.584 + 0.175*CL	0.583 + 0.175*CL	0.579 + 0.175*CL
	t_F	8.642	0.523 + 0.162*CL	0.521 + 0.162*CL	0.516 + 0.162*CL
	t_{PLH}	5.319	1.172 + 0.083*CL	1.175 + 0.083*CL	1.176 + 0.083*CL
	t_{PHL}	5.459	1.150 + 0.086*CL	1.152 + 0.086*CL	1.152 + 0.086*CL
	t_{PLZ}	0.879	0.879 + 0.000*CL	0.879 + 0.000*CL	0.879 + 0.000*CL
	t_{PHZ}	1.022	1.022 + 0.000*CL	1.022 + 0.000*CL	1.022 + 0.000*CL
EN to PAD	t_R	9.348	0.584 + 0.175*CL	0.583 + 0.175*CL	0.579 + 0.175*CL
	t_F	8.642	0.523 + 0.162*CL	0.521 + 0.162*CL	0.516 + 0.162*CL
	t_{PLH}	5.425	1.278 + 0.083*CL	1.281 + 0.083*CL	1.282 + 0.083*CL
	t_{PHL}	5.564	1.257 + 0.086*CL	1.258 + 0.086*CL	1.258 + 0.086*CL
	t_{PLZ}	0.954	0.954 + 0.000*CL	0.954 + 0.000*CL	0.954 + 0.000*CL
	t_{PHZ}	1.097	1.097 + 0.000*CL	1.097 + 0.000*CL	1.097 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT8_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.709	0.343 + 0.087*CL	0.331 + 0.088*CL	0.327 + 0.088*CL
	t_F	4.338	0.281 + 0.081*CL	0.280 + 0.081*CL	0.278 + 0.081*CL
	t_{PLH}	3.041	0.963 + 0.042*CL	0.967 + 0.041*CL	0.969 + 0.041*CL
	t_{PHL}	3.006	0.857 + 0.043*CL	0.856 + 0.043*CL	0.855 + 0.043*CL
TN to PAD	t_R	4.709	0.343 + 0.087*CL	0.331 + 0.088*CL	0.327 + 0.088*CL
	t_F	4.338	0.280 + 0.081*CL	0.279 + 0.081*CL	0.278 + 0.081*CL
	t_{PLH}	3.294	1.215 + 0.042*CL	1.220 + 0.041*CL	1.222 + 0.041*CL
	t_{PHL}	3.232	1.072 + 0.043*CL	1.077 + 0.043*CL	1.079 + 0.043*CL
	t_{PLZ}	0.985	0.985 + 0.000*CL	0.985 + 0.000*CL	0.985 + 0.000*CL
	t_{PHZ}	1.281	1.281 + 0.000*CL	1.281 + 0.000*CL	1.281 + 0.000*CL
EN to PAD	t_R	4.709	0.343 + 0.087*CL	0.331 + 0.088*CL	0.327 + 0.088*CL
	t_F	4.338	0.280 + 0.081*CL	0.279 + 0.081*CL	0.278 + 0.081*CL
	t_{PLH}	3.400	1.322 + 0.042*CL	1.326 + 0.041*CL	1.328 + 0.041*CL
	t_{PHL}	3.338	1.179 + 0.043*CL	1.183 + 0.043*CL	1.185 + 0.043*CL
	t_{PLZ}	1.060	1.060 + 0.000*CL	1.060 + 0.000*CL	1.060 + 0.000*CL
	t_{PHZ}	1.356	1.356 + 0.000*CL	1.356 + 0.000*CL	1.356 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT12_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.195	0.333 + 0.057*CL	0.300 + 0.058*CL	0.278 + 0.058*CL
	t_F	2.912	0.240 + 0.053*CL	0.213 + 0.054*CL	0.205 + 0.054*CL
	t_{PLH}	2.479	1.088 + 0.028*CL	1.094 + 0.028*CL	1.097 + 0.028*CL
	t_{PHL}	2.321	0.903 + 0.028*CL	0.895 + 0.029*CL	0.890 + 0.029*CL
TN to PAD	t_R	3.195	0.333 + 0.057*CL	0.300 + 0.058*CL	0.278 + 0.058*CL
	t_F	2.909	0.213 + 0.054*CL	0.206 + 0.054*CL	0.203 + 0.054*CL
	t_{PLH}	2.732	1.339 + 0.028*CL	1.346 + 0.028*CL	1.349 + 0.028*CL
	t_{PHL}	2.530	1.083 + 0.029*CL	1.089 + 0.029*CL	1.093 + 0.029*CL
	t_{PLZ}	1.089	1.089 + 0.000*CL	1.089 + 0.000*CL	1.089 + 0.000*CL
	t_{PHZ}	1.539	1.539 + 0.000*CL	1.539 + 0.000*CL	1.539 + 0.000*CL
EN to PAD	t_R	3.195	0.333 + 0.057*CL	0.300 + 0.058*CL	0.278 + 0.058*CL
	t_F	2.909	0.213 + 0.054*CL	0.206 + 0.054*CL	0.203 + 0.054*CL
	t_{PLH}	2.838	1.446 + 0.028*CL	1.452 + 0.028*CL	1.456 + 0.028*CL
	t_{PHL}	2.635	1.190 + 0.029*CL	1.195 + 0.029*CL	1.199 + 0.029*CL
	t_{PLZ}	1.164	1.164 + 0.000*CL	1.164 + 0.000*CL	1.164 + 0.000*CL
	t_{PHZ}	1.614	1.614 + 0.000*CL	1.614 + 0.000*CL	1.614 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT16_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.387	0.232 + 0.043*CL	0.211 + 0.044*CL	0.197 + 0.044*CL
	t_F	2.196	0.210 + 0.040*CL	0.182 + 0.040*CL	0.164 + 0.041*CL
	t_{PLH}	1.954	0.913 + 0.021*CL	0.916 + 0.021*CL	0.917 + 0.021*CL
	t_{PHL}	1.993	0.936 + 0.021*CL	0.927 + 0.021*CL	0.920 + 0.021*CL
TN to PAD	t_R	2.387	0.232 + 0.043*CL	0.211 + 0.044*CL	0.197 + 0.044*CL
	t_F	2.190	0.175 + 0.040*CL	0.166 + 0.040*CL	0.161 + 0.041*CL
	t_{PLH}	2.207	1.164 + 0.021*CL	1.168 + 0.021*CL	1.170 + 0.021*CL
	t_{PHL}	2.197	1.111 + 0.022*CL	1.116 + 0.022*CL	1.120 + 0.022*CL
	t_{PLZ}	1.016	1.016 + 0.000*CL	1.016 + 0.000*CL	1.016 + 0.000*CL
	t_{PHZ}	1.571	1.572 + 0.000*CL	1.571 + 0.000*CL	1.571 + 0.000*CL
EN to PAD	t_R	2.387	0.232 + 0.043*CL	0.211 + 0.044*CL	0.197 + 0.044*CL
	t_F	2.190	0.175 + 0.040*CL	0.166 + 0.040*CL	0.161 + 0.041*CL
	t_{PLH}	2.313	1.271 + 0.021*CL	1.274 + 0.021*CL	1.276 + 0.021*CL
	t_{PHL}	2.303	1.217 + 0.022*CL	1.222 + 0.022*CL	1.226 + 0.022*CL
	t_{PLZ}	1.090	1.090 + 0.000*CL	1.090 + 0.000*CL	1.090 + 0.000*CL
	t_{PHZ}	1.646	1.647 + 0.000*CL	1.646 + 0.000*CL	1.646 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT20_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.949	0.253 + 0.034*CL	0.226 + 0.034*CL	0.204 + 0.035*CL
	t_F	1.794	0.247 + 0.031*CL	0.209 + 0.032*CL	0.180 + 0.032*CL
	t_{PLH}	1.819	0.981 + 0.017*CL	0.987 + 0.017*CL	0.990 + 0.017*CL
	t_{PHL}	1.832	1.006 + 0.017*CL	0.990 + 0.017*CL	0.979 + 0.017*CL
TN to PAD	t_R	1.949	0.254 + 0.034*CL	0.226 + 0.034*CL	0.204 + 0.035*CL
	t_F	1.771	0.174 + 0.032*CL	0.160 + 0.032*CL	0.150 + 0.032*CL
	t_{PLH}	2.072	1.232 + 0.017*CL	1.240 + 0.017*CL	1.242 + 0.017*CL
	t_{PHL}	2.013	1.140 + 0.017*CL	1.146 + 0.017*CL	1.150 + 0.017*CL
	t_{PLZ}	1.068	1.068 + 0.000*CL	1.068 + 0.000*CL	1.068 + 0.000*CL
	t_{PHZ}	1.763	1.763 + 0.000*CL	1.763 + 0.000*CL	1.763 + 0.000*CL
EN to PAD	t_R	1.949	0.254 + 0.034*CL	0.226 + 0.034*CL	0.204 + 0.035*CL
	t_F	1.771	0.174 + 0.032*CL	0.160 + 0.032*CL	0.150 + 0.032*CL
	t_{PLH}	2.178	1.338 + 0.017*CL	1.346 + 0.017*CL	1.348 + 0.017*CL
	t_{PHL}	2.119	1.246 + 0.017*CL	1.252 + 0.017*CL	1.255 + 0.017*CL
	t_{PLZ}	1.143	1.143 + 0.000*CL	1.143 + 0.000*CL	1.143 + 0.000*CL
	t_{PHZ}	1.838	1.838 + 0.000*CL	1.838 + 0.000*CL	1.838 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT24_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.673	0.285 + 0.028*CL	0.257 + 0.028*CL	0.231 + 0.029*CL
	t_F	1.548	0.304 + 0.025*CL	0.255 + 0.026*CL	0.218 + 0.026*CL
	t_{PLH}	1.757	1.044 + 0.014*CL	1.060 + 0.014*CL	1.065 + 0.014*CL
	t_{PHL}	1.753	1.083 + 0.013*CL	1.066 + 0.014*CL	1.049 + 0.014*CL
TN to PAD	t_R	1.673	0.287 + 0.028*CL	0.258 + 0.028*CL	0.231 + 0.029*CL
	t_F	1.500	0.183 + 0.026*CL	0.167 + 0.027*CL	0.153 + 0.027*CL
	t_{PLH}	2.009	1.295 + 0.014*CL	1.312 + 0.014*CL	1.318 + 0.014*CL
	t_{PHL}	1.905	1.170 + 0.015*CL	1.179 + 0.015*CL	1.184 + 0.014*CL
	t_{PLZ}	1.119	1.119 + 0.000*CL	1.119 + 0.000*CL	1.119 + 0.000*CL
	t_{PHZ}	1.955	1.955 + 0.000*CL	1.955 + 0.000*CL	1.954 + 0.000*CL
EN to PAD	t_R	1.673	0.287 + 0.028*CL	0.258 + 0.028*CL	0.231 + 0.029*CL
	t_F	1.500	0.183 + 0.026*CL	0.167 + 0.027*CL	0.153 + 0.027*CL
	t_{PLH}	2.115	1.401 + 0.014*CL	1.418 + 0.014*CL	1.424 + 0.014*CL
	t_{PHL}	2.010	1.277 + 0.015*CL	1.285 + 0.014*CL	1.290 + 0.014*CL
	t_{PLZ}	1.194	1.194 + 0.000*CL	1.194 + 0.000*CL	1.194 + 0.000*CL
	t_{PHZ}	2.030	2.030 + 0.000*CL	2.030 + 0.000*CL	2.029 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	9.496	0.874 + 0.172*CL	0.805 + 0.174*CL	0.749 + 0.175*CL
	t_F	8.701	0.636 + 0.161*CL	0.610 + 0.162*CL	0.584 + 0.162*CL
	t_{PLH}	6.024	1.854 + 0.083*CL	1.875 + 0.083*CL	1.883 + 0.083*CL
	t_{PHL}	5.672	1.358 + 0.086*CL	1.365 + 0.086*CL	1.366 + 0.086*CL
TN to PAD	t_R	9.496	0.874 + 0.172*CL	0.805 + 0.174*CL	0.749 + 0.175*CL
	t_F	8.701	0.636 + 0.161*CL	0.610 + 0.162*CL	0.584 + 0.162*CL
	t_{PLH}	6.277	2.105 + 0.083*CL	2.127 + 0.083*CL	2.134 + 0.083*CL
	t_{PHL}	5.908	1.593 + 0.086*CL	1.600 + 0.086*CL	1.601 + 0.086*CL
	t_{PLZ}	0.848	0.848 + 0.000*CL	0.848 + 0.000*CL	0.848 + 0.000*CL
	t_{PHZ}	1.061	1.061 + 0.000*CL	1.061 + 0.000*CL	1.061 + 0.000*CL
EN to PAD	t_R	9.496	0.874 + 0.172*CL	0.805 + 0.174*CL	0.749 + 0.175*CL
	t_F	8.701	0.636 + 0.161*CL	0.610 + 0.162*CL	0.584 + 0.162*CL
	t_{PLH}	6.383	2.211 + 0.083*CL	2.233 + 0.083*CL	2.240 + 0.083*CL
	t_{PHL}	6.013	1.699 + 0.086*CL	1.706 + 0.086*CL	1.707 + 0.086*CL
	t_{PLZ}	0.922	0.922 + 0.000*CL	0.922 + 0.000*CL	0.922 + 0.000*CL
	t_{PHZ}	1.136	1.136 + 0.000*CL	1.136 + 0.000*CL	1.136 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT8SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	5.077	0.889 + 0.084*CL	0.843 + 0.085*CL	0.780 + 0.086*CL
	t_F	4.463	0.499 + 0.079*CL	0.464 + 0.080*CL	0.429 + 0.080*CL
	t_{PLH}	4.116	1.908 + 0.044*CL	1.998 + 0.042*CL	2.042 + 0.042*CL
	t_{PHL}	3.727	1.535 + 0.044*CL	1.563 + 0.043*CL	1.575 + 0.043*CL
TN to PAD	t_R	5.077	0.889 + 0.084*CL	0.843 + 0.085*CL	0.780 + 0.086*CL
	t_F	4.464	0.499 + 0.079*CL	0.464 + 0.080*CL	0.429 + 0.080*CL
	t_{PLH}	4.369	2.160 + 0.044*CL	2.250 + 0.042*CL	2.296 + 0.042*CL
	t_{PHL}	3.961	1.767 + 0.044*CL	1.796 + 0.043*CL	1.809 + 0.043*CL
	t_{PLZ}	1.061	1.061 + 0.000*CL	1.061 + 0.000*CL	1.061 + 0.000*CL
	t_{PHZ}	1.414	1.414 + 0.000*CL	1.414 + 0.000*CL	1.414 + 0.000*CL
EN to PAD	t_R	5.077	0.890 + 0.084*CL	0.843 + 0.085*CL	0.780 + 0.086*CL
	t_F	4.464	0.499 + 0.079*CL	0.464 + 0.080*CL	0.429 + 0.080*CL
	t_{PLH}	4.475	2.267 + 0.044*CL	2.356 + 0.042*CL	2.402 + 0.042*CL
	t_{PHL}	4.067	1.874 + 0.044*CL	1.902 + 0.043*CL	1.915 + 0.043*CL
	t_{PLZ}	1.136	1.136 + 0.000*CL	1.136 + 0.000*CL	1.136 + 0.000*CL
	t_{PHZ}	1.489	1.489 + 0.000*CL	1.489 + 0.000*CL	1.489 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT12SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.048	1.294 + 0.055*CL	1.343 + 0.054*CL	1.313 + 0.054*CL
	t_F	3.233	0.649 + 0.052*CL	0.637 + 0.052*CL	0.601 + 0.052*CL
	t_{PLH}	3.819	2.015 + 0.036*CL	2.241 + 0.032*CL	2.396 + 0.029*CL
	t_{PHL}	3.337	1.764 + 0.031*CL	1.846 + 0.030*CL	1.896 + 0.029*CL
TN to PAD	t_R	4.048	1.295 + 0.055*CL	1.343 + 0.054*CL	1.314 + 0.054*CL
	t_F	3.236	0.659 + 0.052*CL	0.642 + 0.052*CL	0.604 + 0.052*CL
	t_{PLH}	4.073	2.267 + 0.036*CL	2.494 + 0.032*CL	2.650 + 0.030*CL
	t_{PHL}	3.567	1.987 + 0.032*CL	2.073 + 0.030*CL	2.126 + 0.029*CL
	t_{PLZ}	1.242	1.242 + 0.000*CL	1.242 + 0.000*CL	1.242 + 0.000*CL
	t_{PHZ}	1.895	1.895 + 0.000*CL	1.895 + 0.000*CL	1.894 + 0.000*CL
EN to PAD	t_R	4.048	1.295 + 0.055*CL	1.343 + 0.054*CL	1.314 + 0.054*CL
	t_F	3.236	0.659 + 0.052*CL	0.642 + 0.052*CL	0.604 + 0.052*CL
	t_{PLH}	4.179	2.374 + 0.036*CL	2.600 + 0.032*CL	2.756 + 0.029*CL
	t_{PHL}	3.673	2.094 + 0.032*CL	2.179 + 0.030*CL	2.232 + 0.029*CL
	t_{PLZ}	1.317	1.317 + 0.000*CL	1.317 + 0.000*CL	1.317 + 0.000*CL
	t_{PHZ}	1.970	1.970 + 0.000*CL	1.970 + 0.000*CL	1.969 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT16SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.372	1.167 + 0.044*CL	1.291 + 0.042*CL	1.342 + 0.041*CL
	t_F	2.751	0.801 + 0.039*CL	0.836 + 0.038*CL	0.829 + 0.038*CL
	t_{PLH}	3.415	1.855 + 0.031*CL	2.090 + 0.026*CL	2.281 + 0.024*CL
	t_{PHL}	3.258	1.918 + 0.027*CL	2.046 + 0.024*CL	2.145 + 0.023*CL
TN to PAD	t_R	3.373	1.171 + 0.044*CL	1.293 + 0.042*CL	1.343 + 0.041*CL
	t_F	2.760	0.832 + 0.039*CL	0.853 + 0.038*CL	0.840 + 0.038*CL
	t_{PLH}	3.668	2.105 + 0.031*CL	2.342 + 0.027*CL	2.534 + 0.024*CL
	t_{PHL}	3.483	2.127 + 0.027*CL	2.265 + 0.024*CL	2.368 + 0.023*CL
	t_{PLZ}	1.428	1.428 + 0.000*CL	1.428 + 0.000*CL	1.428 + 0.000*CL
	t_{PHZ}	2.134	2.134 + 0.000*CL	2.134 + 0.000*CL	2.133 + 0.000*CL
EN to PAD	t_R	3.373	1.171 + 0.044*CL	1.293 + 0.042*CL	1.343 + 0.041*CL
	t_F	2.760	0.832 + 0.039*CL	0.853 + 0.038*CL	0.840 + 0.038*CL
	t_{PLH}	3.773	2.211 + 0.031*CL	2.448 + 0.027*CL	2.640 + 0.024*CL
	t_{PHL}	3.589	2.234 + 0.027*CL	2.371 + 0.024*CL	2.474 + 0.023*CL
	t_{PLZ}	1.503	1.503 + 0.000*CL	1.503 + 0.000*CL	1.503 + 0.000*CL
	t_{PHZ}	2.208	2.209 + 0.000*CL	2.208 + 0.000*CL	2.208 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT20SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.828	1.036 + 0.036*CL	1.125 + 0.034*CL	1.176 + 0.033*CL
	t_F	2.321	0.730 + 0.032*CL	0.773 + 0.031*CL	0.786 + 0.031*CL
	t_{PLH}	3.373	2.097 + 0.026*CL	2.266 + 0.022*CL	2.416 + 0.020*CL
	t_{PHL}	3.090	1.954 + 0.023*CL	2.074 + 0.020*CL	2.173 + 0.019*CL
TN to PAD	t_R	2.828	1.036 + 0.036*CL	1.125 + 0.034*CL	1.175 + 0.033*CL
	t_F	2.326	0.749 + 0.032*CL	0.784 + 0.031*CL	0.792 + 0.031*CL
	t_{PLH}	3.628	2.350 + 0.026*CL	2.520 + 0.022*CL	2.671 + 0.020*CL
	t_{PHL}	3.320	2.175 + 0.023*CL	2.301 + 0.020*CL	2.402 + 0.019*CL
	t_{PLZ}	1.418	1.418 + 0.000*CL	1.418 + 0.000*CL	1.418 + 0.000*CL
	t_{PHZ}	2.146	2.146 + 0.000*CL	2.146 + 0.000*CL	2.146 + 0.000*CL
EN to PAD	t_R	2.828	1.036 + 0.036*CL	1.125 + 0.034*CL	1.175 + 0.033*CL
	t_F	2.326	0.749 + 0.032*CL	0.784 + 0.031*CL	0.792 + 0.031*CL
	t_{PLH}	3.733	2.457 + 0.026*CL	2.626 + 0.022*CL	2.777 + 0.020*CL
	t_{PHL}	3.425	2.282 + 0.023*CL	2.407 + 0.020*CL	2.508 + 0.019*CL
	t_{PLZ}	1.493	1.493 + 0.000*CL	1.493 + 0.000*CL	1.493 + 0.000*CL
	t_{PHZ}	2.221	2.221 + 0.000*CL	2.221 + 0.000*CL	2.220 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT24SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.687	1.100 + 0.032*CL	1.212 + 0.030*CL	1.294 + 0.028*CL
	t_F	2.081	0.731 + 0.027*CL	0.785 + 0.026*CL	0.810 + 0.026*CL
	t_{PLH}	3.429	2.217 + 0.024*CL	2.394 + 0.021*CL	2.554 + 0.019*CL
	t_{PHL}	3.072	2.060 + 0.020*CL	2.181 + 0.018*CL	2.284 + 0.016*CL
TN to PAD	t_R	2.687	1.100 + 0.032*CL	1.212 + 0.030*CL	1.294 + 0.028*CL
	t_F	2.091	0.762 + 0.027*CL	0.804 + 0.026*CL	0.822 + 0.026*CL
	t_{PLH}	3.684	2.471 + 0.024*CL	2.648 + 0.021*CL	2.808 + 0.019*CL
	t_{PHL}	3.300	2.272 + 0.021*CL	2.402 + 0.018*CL	2.509 + 0.017*CL
	t_{PLZ}	1.417	1.417 + 0.000*CL	1.417 + 0.000*CL	1.417 + 0.000*CL
	t_{PHZ}	2.397	2.397 + 0.000*CL	2.397 + 0.000*CL	2.397 + 0.000*CL
EN to PAD	t_R	2.687	1.100 + 0.032*CL	1.212 + 0.030*CL	1.294 + 0.028*CL
	t_F	2.091	0.762 + 0.027*CL	0.804 + 0.026*CL	0.822 + 0.026*CL
	t_{PLH}	3.789	2.578 + 0.024*CL	2.754 + 0.021*CL	2.914 + 0.019*CL
	t_{PHL}	3.405	2.379 + 0.021*CL	2.508 + 0.018*CL	2.615 + 0.017*CL
	t_{PLZ}	1.492	1.492 + 0.000*CL	1.492 + 0.000*CL	1.492 + 0.000*CL
	t_{PHZ}	2.472	2.472 + 0.000*CL	2.472 + 0.000*CL	2.471 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT12SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.289	1.453 + 0.057*CL	1.521 + 0.055*CL	1.533 + 0.055*CL
	t_F	3.750	1.117 + 0.053*CL	1.172 + 0.052*CL	1.183 + 0.051*CL
	t_{PLH}	4.838	2.925 + 0.038*CL	3.155 + 0.034*CL	3.342 + 0.031*CL
	t_{PHL}	4.404	2.548 + 0.037*CL	2.737 + 0.033*CL	2.889 + 0.031*CL
TN to PAD	t_R	4.289	1.453 + 0.057*CL	1.520 + 0.055*CL	1.533 + 0.055*CL
	t_F	3.750	1.118 + 0.053*CL	1.173 + 0.052*CL	1.184 + 0.051*CL
	t_{PLH}	5.092	3.179 + 0.038*CL	3.409 + 0.034*CL	3.596 + 0.031*CL
	t_{PHL}	4.640	2.784 + 0.037*CL	2.973 + 0.033*CL	3.125 + 0.031*CL
	t_{PLZ}	1.477	1.477 + 0.000*CL	1.477 + 0.000*CL	1.477 + 0.000*CL
	t_{PHZ}	1.388	1.389 + 0.000*CL	1.388 + 0.000*CL	1.388 + 0.000*CL
EN to PAD	t_R	4.289	1.453 + 0.057*CL	1.520 + 0.055*CL	1.533 + 0.055*CL
	t_F	3.750	1.118 + 0.053*CL	1.173 + 0.052*CL	1.184 + 0.051*CL
	t_{PLH}	5.198	3.285 + 0.038*CL	3.515 + 0.034*CL	3.702 + 0.031*CL
	t_{PHL}	4.745	2.890 + 0.037*CL	3.079 + 0.033*CL	3.231 + 0.031*CL
	t_{PLZ}	1.552	1.552 + 0.000*CL	1.552 + 0.000*CL	1.551 + 0.000*CL
	t_{PHZ}	1.463	1.464 + 0.000*CL	1.463 + 0.000*CL	1.463 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT16SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.686	1.513 + 0.043*CL	1.603 + 0.042*CL	1.645 + 0.041*CL
	t_F	3.088	1.063 + 0.040*CL	1.136 + 0.039*CL	1.174 + 0.039*CL
	t_{PLH}	4.754	3.111 + 0.033*CL	3.353 + 0.028*CL	3.555 + 0.025*CL
	t_{PHL}	4.208	2.679 + 0.031*CL	2.863 + 0.027*CL	3.019 + 0.025*CL
TN to PAD	t_R	3.686	1.512 + 0.043*CL	1.603 + 0.042*CL	1.645 + 0.041*CL
	t_F	3.088	1.063 + 0.041*CL	1.136 + 0.039*CL	1.174 + 0.039*CL
	t_{PLH}	5.008	3.365 + 0.033*CL	3.608 + 0.028*CL	3.810 + 0.025*CL
	t_{PHL}	4.444	2.916 + 0.031*CL	3.099 + 0.027*CL	3.255 + 0.025*CL
	t_{PLZ}	1.476	1.476 + 0.000*CL	1.476 + 0.000*CL	1.476 + 0.000*CL
	t_{PHZ}	1.539	1.539 + 0.000*CL	1.539 + 0.000*CL	1.539 + 0.000*CL
EN to PAD	t_R	3.686	1.512 + 0.043*CL	1.603 + 0.042*CL	1.645 + 0.041*CL
	t_F	3.088	1.063 + 0.041*CL	1.136 + 0.039*CL	1.174 + 0.039*CL
	t_{PLH}	5.114	3.472 + 0.033*CL	3.714 + 0.028*CL	3.915 + 0.025*CL
	t_{PHL}	4.549	3.022 + 0.031*CL	3.206 + 0.027*CL	3.361 + 0.025*CL
	t_{PLZ}	1.551	1.551 + 0.000*CL	1.551 + 0.000*CL	1.551 + 0.000*CL
	t_{PHZ}	1.613	1.614 + 0.000*CL	1.613 + 0.000*CL	1.613 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT20SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.618	1.723 + 0.038*CL	1.862 + 0.035*CL	1.962 + 0.034*CL
	t_F	3.025	1.279 + 0.035*CL	1.392 + 0.033*CL	1.476 + 0.032*CL
	t_{PLH}	5.038	3.418 + 0.032*CL	3.696 + 0.027*CL	3.936 + 0.024*CL
	t_{PHL}	4.462	2.967 + 0.030*CL	3.190 + 0.025*CL	3.384 + 0.023*CL
TN to PAD	t_R	3.618	1.722 + 0.038*CL	1.861 + 0.035*CL	1.962 + 0.034*CL
	t_F	3.025	1.280 + 0.035*CL	1.392 + 0.033*CL	1.476 + 0.032*CL
	t_{PLH}	5.293	3.673 + 0.032*CL	3.951 + 0.027*CL	4.192 + 0.024*CL
	t_{PHL}	4.699	3.206 + 0.030*CL	3.428 + 0.025*CL	3.621 + 0.023*CL
	t_{PLZ}	1.724	1.724 + 0.000*CL	1.724 + 0.000*CL	1.723 + 0.000*CL
	t_{PHZ}	1.708	1.708 + 0.000*CL	1.708 + 0.000*CL	1.707 + 0.000*CL
EN to PAD	t_R	3.618	1.722 + 0.038*CL	1.861 + 0.035*CL	1.962 + 0.034*CL
	t_F	3.026	1.280 + 0.035*CL	1.393 + 0.033*CL	1.476 + 0.032*CL
	t_{PLH}	5.399	3.779 + 0.032*CL	4.057 + 0.027*CL	4.298 + 0.024*CL
	t_{PHL}	4.804	3.313 + 0.030*CL	3.534 + 0.025*CL	3.727 + 0.023*CL
	t_{PLZ}	1.798	1.798 + 0.000*CL	1.798 + 0.000*CL	1.798 + 0.000*CL
	t_{PHZ}	1.783	1.783 + 0.000*CL	1.783 + 0.000*CL	1.782 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT24SH_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.592	1.877 + 0.034*CL	2.040 + 0.031*CL	2.170 + 0.029*CL
	t_F	3.098	1.483 + 0.032*CL	1.638 + 0.029*CL	1.760 + 0.028*CL
	t_{PLH}	5.270	3.667 + 0.032*CL	3.966 + 0.026*CL	4.229 + 0.023*CL
	t_{PHL}	4.648	3.124 + 0.030*CL	3.383 + 0.025*CL	3.614 + 0.022*CL
TN to PAD	t_R	3.591	1.875 + 0.034*CL	2.039 + 0.031*CL	2.169 + 0.029*CL
	t_F	3.099	1.485 + 0.032*CL	1.640 + 0.029*CL	1.762 + 0.028*CL
	t_{PLH}	5.526	3.922 + 0.032*CL	4.222 + 0.026*CL	4.485 + 0.023*CL
	t_{PHL}	4.886	3.364 + 0.030*CL	3.623 + 0.025*CL	3.853 + 0.022*CL
	t_{PLZ}	1.958	1.958 + 0.000*CL	1.958 + 0.000*CL	1.958 + 0.000*CL
	t_{PHZ}	1.871	1.871 + 0.000*CL	1.871 + 0.000*CL	1.871 + 0.000*CL
EN to PAD	t_R	3.591	1.875 + 0.034*CL	2.039 + 0.031*CL	2.169 + 0.029*CL
	t_F	3.099	1.485 + 0.032*CL	1.640 + 0.029*CL	1.762 + 0.028*CL
	t_{PLH}	5.631	4.029 + 0.032*CL	4.328 + 0.026*CL	4.590 + 0.023*CL
	t_{PHL}	4.992	3.471 + 0.030*CL	3.729 + 0.025*CL	3.959 + 0.022*CL
	t_{PLZ}	2.033	2.033 + 0.000*CL	2.033 + 0.000*CL	2.033 + 0.000*CL
	t_{PHZ}	1.946	1.946 + 0.000*CL	1.946 + 0.000*CL	1.946 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHTOT1_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	38.271	3.543 + 0.695*CL	3.765 + 0.690*CL	3.924 + 0.688*CL
	t_F	30.895	7.300 + 0.472*CL	6.525 + 0.487*CL	5.961 + 0.495*CL
	t_{PLH}	19.041	2.901 + 0.323*CL	2.987 + 0.321*CL	3.041 + 0.320*CL
	t_{PHL}	17.517	5.617 + 0.238*CL	5.749 + 0.235*CL	5.626 + 0.237*CL
TN to PAD	t_R	38.271	3.546 + 0.695*CL	3.765 + 0.690*CL	3.927 + 0.688*CL
	t_F	30.850	7.275 + 0.471*CL	6.496 + 0.487*CL	5.935 + 0.495*CL
	t_{PLH}	19.296	3.154 + 0.323*CL	3.242 + 0.321*CL	3.296 + 0.320*CL
	t_{PHL}	17.659	5.799 + 0.237*CL	5.925 + 0.235*CL	5.799 + 0.236*CL
	t_{PLZ}	1.040	1.040 + 0.000*CL	1.040 + 0.000*CL	1.040 + 0.000*CL
	t_{PHZ}	2.291	2.291 + 0.000*CL	2.291 + 0.000*CL	2.291 + 0.000*CL
EN to PAD	t_R	38.271	3.546 + 0.695*CL	3.765 + 0.690*CL	3.927 + 0.688*CL
	t_F	30.850	7.275 + 0.471*CL	6.496 + 0.487*CL	5.935 + 0.495*CL
	t_{PLH}	19.401	3.261 + 0.323*CL	3.345 + 0.321*CL	3.405 + 0.320*CL
	t_{PHL}	17.765	5.905 + 0.237*CL	6.031 + 0.235*CL	5.908 + 0.236*CL
	t_{PLZ}	1.115	1.115 + 0.000*CL	1.115 + 0.000*CL	1.115 + 0.000*CL
	t_{PHZ}	2.366	2.366 + 0.000*CL	2.366 + 0.000*CL	2.366 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHTOT2_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	20.097	1.954 + 0.363*CL	2.151 + 0.359*CL	2.298 + 0.357*CL
	t_F	18.205	5.818 + 0.248*CL	5.233 + 0.259*CL	4.711 + 0.266*CL
	t_{PLH}	10.219	1.773 + 0.169*CL	1.841 + 0.168*CL	1.892 + 0.167*CL
	t_{PHL}	10.425	2.987 + 0.149*CL	3.319 + 0.142*CL	3.580 + 0.139*CL
TN to PAD	t_R	20.097	1.954 + 0.363*CL	2.151 + 0.359*CL	2.298 + 0.357*CL
	t_F	18.143	5.775 + 0.247*CL	5.185 + 0.259*CL	4.663 + 0.266*CL
	t_{PLH}	10.473	2.024 + 0.169*CL	2.095 + 0.168*CL	2.146 + 0.167*CL
	t_{PHL}	10.567	3.163 + 0.148*CL	3.489 + 0.142*CL	3.750 + 0.138*CL
	t_{PLZ}	0.834	0.834 + 0.000*CL	0.834 + 0.000*CL	0.834 + 0.000*CL
	t_{PHZ}	1.871	1.871 + 0.000*CL	1.871 + 0.000*CL	1.871 + 0.000*CL
EN to PAD	t_R	20.097	1.954 + 0.363*CL	2.151 + 0.359*CL	2.298 + 0.357*CL
	t_F	18.143	5.775 + 0.247*CL	5.185 + 0.259*CL	4.663 + 0.266*CL
	t_{PLH}	10.578	2.132 + 0.169*CL	2.198 + 0.168*CL	2.255 + 0.167*CL
	t_{PHL}	10.673	3.269 + 0.148*CL	3.597 + 0.142*CL	3.855 + 0.138*CL
	t_{PLZ}	0.909	0.909 + 0.000*CL	0.909 + 0.000*CL	0.909 + 0.000*CL
	t_{PHZ}	1.946	1.946 + 0.000*CL	1.946 + 0.000*CL	1.946 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PvOTyz_LP

Tri-State Output Buffers

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHTOT4_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	10.349	1.091 + 0.185*CL	1.227 + 0.182*CL	1.359 + 0.181*CL
	t_F	9.944	3.488 + 0.129*CL	3.572 + 0.127*CL	3.383 + 0.130*CL
	t_{PLH}	6.003	1.718 + 0.086*CL	1.762 + 0.085*CL	1.806 + 0.084*CL
	t_{PHL}	5.987	2.057 + 0.079*CL	2.178 + 0.076*CL	2.327 + 0.074*CL
TN to PAD	t_R	10.350	1.090 + 0.185*CL	1.230 + 0.182*CL	1.359 + 0.181*CL
	t_F	9.880	3.443 + 0.129*CL	3.519 + 0.127*CL	3.331 + 0.130*CL
	t_{PLH}	6.256	1.970 + 0.086*CL	2.015 + 0.085*CL	2.059 + 0.084*CL
	t_{PHL}	6.134	2.230 + 0.078*CL	2.345 + 0.076*CL	2.493 + 0.074*CL
	t_{PLZ}	0.931	0.931 + 0.000*CL	0.931 + 0.000*CL	0.931 + 0.000*CL
	t_{PHZ}	2.294	2.295 + 0.000*CL	2.294 + 0.000*CL	2.294 + 0.000*CL
EN to PAD	t_R	10.350	1.090 + 0.185*CL	1.230 + 0.182*CL	1.359 + 0.181*CL
	t_F	9.880	3.443 + 0.129*CL	3.519 + 0.127*CL	3.331 + 0.130*CL
	t_{PLH}	6.362	2.077 + 0.086*CL	2.121 + 0.085*CL	2.166 + 0.084*CL
	t_{PHL}	6.239	2.337 + 0.078*CL	2.450 + 0.076*CL	2.599 + 0.074*CL
	t_{PLZ}	1.006	1.006 + 0.000*CL	1.006 + 0.000*CL	1.006 + 0.000*CL
	t_{PHZ}	2.369	2.370 + 0.000*CL	2.369 + 0.000*CL	2.369 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHTOT6_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	7.077	0.873 + 0.124*CL	0.939 + 0.123*CL	1.029 + 0.122*CL
	t_F	6.939	2.258 + 0.094*CL	2.498 + 0.089*CL	2.619 + 0.087*CL
	t_{PLH}	4.640	1.752 + 0.058*CL	1.787 + 0.057*CL	1.821 + 0.057*CL
	t_{PHL}	4.806	2.175 + 0.053*CL	2.252 + 0.051*CL	2.320 + 0.050*CL
TN to PAD	t_R	7.077	0.873 + 0.124*CL	0.940 + 0.123*CL	1.026 + 0.122*CL
	t_F	6.870	2.214 + 0.093*CL	2.442 + 0.089*CL	2.562 + 0.087*CL
	t_{PLH}	4.893	2.005 + 0.058*CL	2.040 + 0.057*CL	2.075 + 0.057*CL
	t_{PHL}	4.947	2.349 + 0.052*CL	2.411 + 0.051*CL	2.477 + 0.050*CL
	t_{PLZ}	1.036	1.036 + 0.000*CL	1.036 + 0.000*CL	1.036 + 0.000*CL
	t_{PHZ}	2.715	2.717 + 0.000*CL	2.715 + 0.000*CL	2.714 + 0.000*CL
EN to PAD	t_R	7.077	0.873 + 0.124*CL	0.940 + 0.123*CL	1.026 + 0.122*CL
	t_F	6.870	2.214 + 0.093*CL	2.442 + 0.089*CL	2.562 + 0.087*CL
	t_{PLH}	4.999	2.112 + 0.058*CL	2.147 + 0.057*CL	2.181 + 0.057*CL
	t_{PHL}	5.053	2.456 + 0.052*CL	2.517 + 0.051*CL	2.582 + 0.050*CL
	t_{PLZ}	1.111	1.111 + 0.000*CL	1.111 + 0.000*CL	1.111 + 0.000*CL
	t_{PHZ}	2.790	2.792 + 0.000*CL	2.790 + 0.000*CL	2.788 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHTOT4SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	10.450	1.321 + 0.183*CL	1.398 + 0.181*CL	1.479 + 0.180*CL
	t_F	10.122	3.624 + 0.130*CL	3.694 + 0.129*CL	3.541 + 0.131*CL
	t_{PLH}	6.688	2.401 + 0.086*CL	2.449 + 0.085*CL	2.492 + 0.084*CL
	t_{PHL}	6.611	2.604 + 0.080*CL	2.743 + 0.077*CL	2.911 + 0.075*CL
TN to PAD	t_R	10.450	1.322 + 0.183*CL	1.398 + 0.181*CL	1.479 + 0.180*CL
	t_F	10.083	3.610 + 0.129*CL	3.669 + 0.128*CL	3.516 + 0.130*CL
	t_{PLH}	6.941	2.653 + 0.086*CL	2.703 + 0.085*CL	2.746 + 0.084*CL
	t_{PHL}	6.783	2.806 + 0.080*CL	2.936 + 0.077*CL	3.103 + 0.075*CL
	t_{PLZ}	1.049	1.049 + 0.000*CL	1.049 + 0.000*CL	1.049 + 0.000*CL
	t_{PHZ}	1.754	1.754 + 0.000*CL	1.754 + 0.000*CL	1.754 + 0.000*CL
EN to PAD	t_R	10.450	1.322 + 0.183*CL	1.398 + 0.181*CL	1.479 + 0.180*CL
	t_F	10.083	3.610 + 0.129*CL	3.669 + 0.128*CL	3.516 + 0.130*CL
	t_{PLH}	7.047	2.760 + 0.086*CL	2.809 + 0.085*CL	2.852 + 0.084*CL
	t_{PHL}	6.889	2.913 + 0.080*CL	3.043 + 0.077*CL	3.209 + 0.075*CL
	t_{PLZ}	1.124	1.124 + 0.000*CL	1.124 + 0.000*CL	1.124 + 0.000*CL
	t_{PHZ}	1.829	1.829 + 0.000*CL	1.829 + 0.000*CL	1.829 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHTOT6SM_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	7.461	1.513 + 0.119*CL	1.507 + 0.119*CL	1.507 + 0.119*CL
	t_F	7.284	2.827 + 0.089*CL	2.981 + 0.086*CL	3.003 + 0.086*CL
	t_{PLH}	5.714	2.735 + 0.060*CL	2.839 + 0.057*CL	2.900 + 0.057*CL
	t_{PHL}	5.770	3.070 + 0.054*CL	3.170 + 0.052*CL	3.263 + 0.051*CL
TN to PAD	t_R	7.461	1.513 + 0.119*CL	1.508 + 0.119*CL	1.507 + 0.119*CL
	t_F	7.255	2.826 + 0.089*CL	2.973 + 0.086*CL	2.991 + 0.085*CL
	t_{PLH}	5.968	2.988 + 0.060*CL	3.093 + 0.058*CL	3.153 + 0.057*CL
	t_{PHL}	5.941	3.265 + 0.054*CL	3.359 + 0.052*CL	3.450 + 0.050*CL
	t_{PLZ}	1.229	1.229 + 0.000*CL	1.229 + 0.000*CL	1.229 + 0.000*CL
	t_{PHZ}	2.239	2.241 + 0.000*CL	2.239 + 0.000*CL	2.238 + 0.000*CL
EN to PAD	t_R	7.461	1.513 + 0.119*CL	1.508 + 0.119*CL	1.507 + 0.119*CL
	t_F	7.255	2.826 + 0.089*CL	2.973 + 0.086*CL	2.991 + 0.085*CL
	t_{PLH}	6.073	3.094 + 0.060*CL	3.199 + 0.057*CL	3.259 + 0.057*CL
	t_{PHL}	6.047	3.372 + 0.053*CL	3.465 + 0.052*CL	3.555 + 0.050*CL
	t_{PLZ}	1.304	1.304 + 0.000*CL	1.304 + 0.000*CL	1.304 + 0.000*CL
	t_{PHZ}	2.314	2.316 + 0.000*CL	2.314 + 0.000*CL	2.313 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

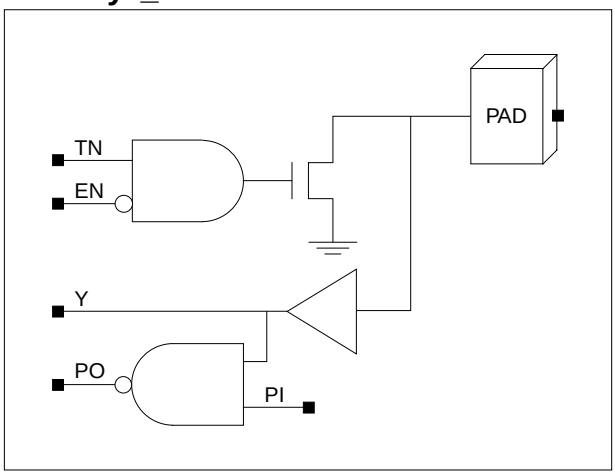
BI-DIRECTIONAL BUFFERS

Cell List

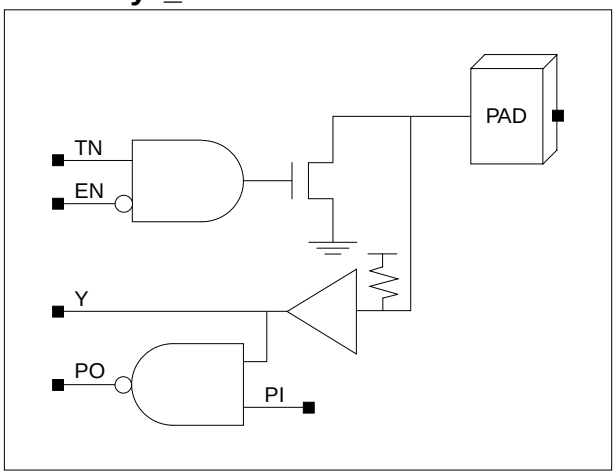
Cell Name	Function Description
PBaDyz_LP	1.8V Open-Drain Bi-Directional Buffers
PBaUDyz_LP	1.8V Open-Drain Bi-Directional Buffers with Pull-Up
PMBaDyz_LP	2.5V Open-Drain Bi-Directional Buffers
PMBaUDyz_LP	2.5V Open-Drain Bi-Directional Buffers with Pull-Up
PHBaDyz_LP	3.3V Open-Drain Bi-Directional Buffers
PHBaUDyz_LP	3.3V Open-Drain Bi-Directional Buffers with Pull-Up
PTBaDyz_LP	1.8V Interface 3.3V-Tolerant Open-Drain Bi-Directional Buffers
PTBaUDyz_LP	1.8V Interface 3.3V-Tolerant Open-Drain Bi-Directional Buffers with Pull-Up
PHTBaDyz_LP	3.3V Interface 5V-Tolerant Open-Drain Bi-Directional Buffers
PHTBaUDyz_LP	3.3V Interface 5V-Tolerant Open-Drain Bi-Directional Buffers with Pull-Up
PBaTyz_LP	1.8V Tri-State Bi-Directional Buffers
PBaDTyz_LP	1.8V Tri-State Bi-Directional Buffers with Pull-Down
PBaUTyz_LP	1.8V Tri-State Bi-Directional Buffers with Pull-Up
PMBaTyz_LP	2.5V Tri-State Bi-Directional Buffers
PMBaDTyz_LP	2.5V Tri-State Bi-Directional Buffers with Pull-Down
PMBaUTyz_LP	2.5V Tri-State Bi-Directional Buffers with Pull-Up
PHBaTyz_LP	3.3V Tri-State Bi-Directional Buffers
PHBaDTyz_LP	3.3V Tri-State Bi-Directional Buffers with Pull-Down
PHBaUTyz_LP	3.3V Tri-State Bi-Directional Buffers with Pull-Up
PTBaTyz_LP	1.8V Interface 3.3V-Tolerant Tri-State Bi-Directional Buffers
PTBaDTyz_LP	1.8V Interface 3.3V-Tolerant Tri-State Bi-Directional Buffers with Pull-Down
PTBaUTyz_LP	1.8V Interface 3.3V-Tolerant Tri-State Bi-Directional Buffers with Pull-Up
PHTBaTyz_LP	3.3V Interface 5V-Tolerant Tri-State Bi-Directional Buffers
PHTBaDTyz_LP	3.3V Interface 5V-Tolerant Tri-State Bi-Directional Buffers with Pull-Down
PHTBaUTyz_LP	3.3V Interface 5V-Tolerant Tri-State Bi-Directional Buffers with Pull-Up

Open Drain Bi-Directional Buffers

PvBaDyz_LP

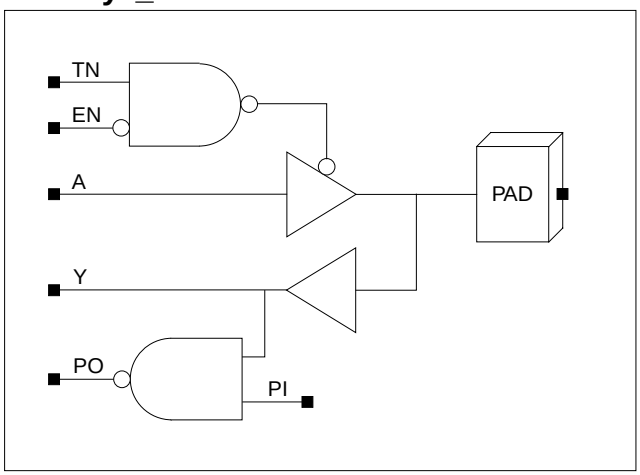


PvBaUDyz_LP

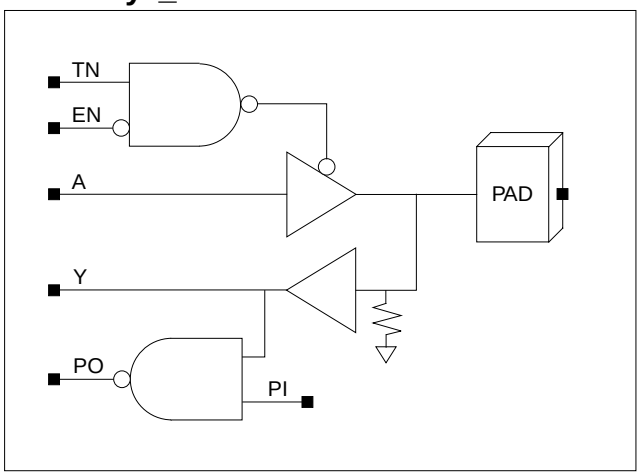


Tri-State Bi-Directional Buffers

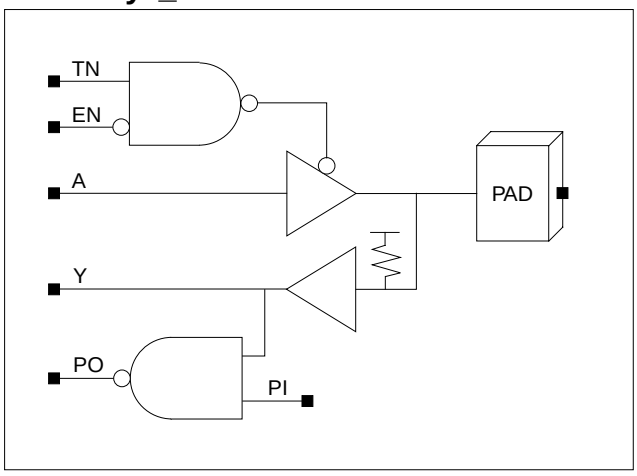
PvBaTyz_LP



PvBaDTyz_LP



PvBaUTyz_LP



INPUT CLOCK DRIVERS

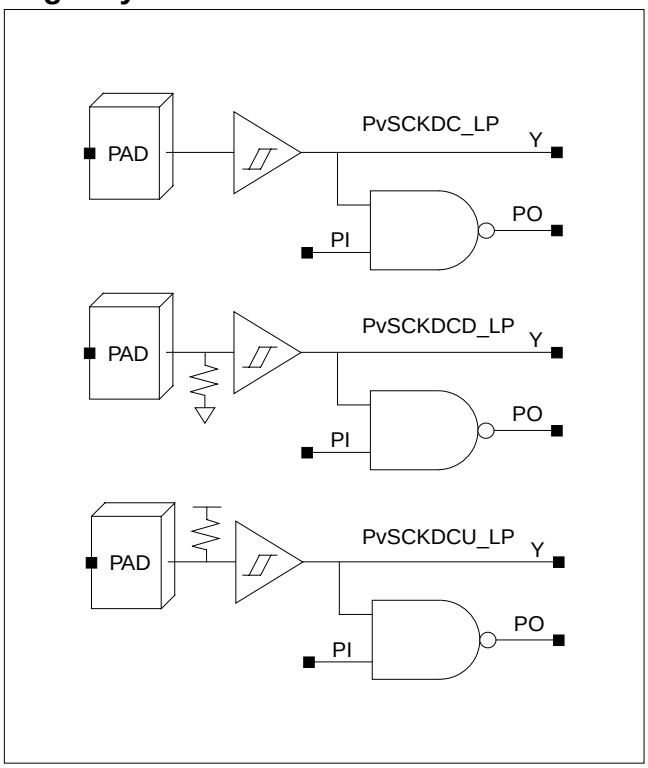
Cell List

Cell Name	Function Description
PSCKDC(2/4/6/8)_LP	1.8V CMOS Level Input Clock Driver
PSCKDCD(2/4/6/8)_LP	1.8V CMOS Level Input Clock Driver with Pull-Down
PSCKDCU(2/4/6/8)_LP	1.8V CMOS Level Input Clock Driver with Pull-Up
PSCKDS(2/4/6/8)_LP	1.8V CMOS Schmitt Trigger Level Input Clock Driver
PSCKDSD(2/4/6/8)_LP	1.8V CMOS Schmitt Trigger Level Input Clock Driver with Pull-Down
PSCKDSU(2/4/6/8)_LP	1.8V CMOS Schmitt Trigger Level Input Clock Driver with Pull-Up
PMSCKDC(2/4/6/8)_LP	2.5V CMOS Level Input Clock Driver
PMSCKDCD(2/4/6/8)_LP	2.5V CMOS Level Input Clock Driver with Pull-Down
PMSCKDCU(2/4/6/8)_LP	2.5V CMOS Level Input Clock Driver with Pull-Up
PMSCKDS(2/4/6/8)_LP	2.5V CMOS Schmitt Trigger Level Input Clock Drive
PMSCKDSD(2/4/6/8)_LP	2.5V CMOS Schmitt Trigger Level Input Clock Drive with Pull-Down
PMSCKDSU(2/4/6/8)_LP	2.5V CMOS Schmitt Trigger Level Input Clock Drive with Pull-Up
PHSCKDC(2/4/6/8)_LP	3.3V LCMOS Level Input Clock Driver
PHSCKDCD(2/4/6/8)_LP	3.3V LCMOS Level Input Clock Driver Pull-Down
PHSCKDCU(2/4/6/8)_LP	3.3V LCMOS Level Input Clock Driver Pull-Up
PHSCKDS(2/4/6/8)_LP	3.3V LCMOS Schmitt Trigger Level Input Clock Driver
PHSCKDSD(2/4/6/8)_LP	3.3V LCMOS Schmitt Trigger Level Input Clock Driver with Pull-Down
PHSCKDSU(2/4/6/8)_LP	3.3V LCMOS Schmitt Trigger Level Input Clock Driver with Pull-Up

Cell Availability

1.8V Interface	2.5V Interface	3.3V Interface
PSCKDC(2/4/6/8)_LP PSCKDCD(2/4/6/8)_LP PSCKDCU(2/4/6/8)_LP	PMSCKDC(2/4/6/8)_LP PMSCKDCD(2/4/6/8)_LP PMSCKDCU(2/4/6/8)_LP	PHSCKDC(2/4/6/8)_LP PHSCKDCD(2/4/6/8)_LP PHSCKDCU(2/4/6/8)_LP

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PSCKDC/PSCKDCD/PSCKDCU(2/4/6/8)_LP	3.79
PMSCKDC/PMSCKDCD/PMSCKDCU(2/4/6/8)_LP	3.74
PHSCKDC/PHSCKDCD/PHSCKDCU(2/4/6/8)_LP	3.74

PvSCKDCby_LP

CMOS Level Input Clock Driver

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PSCKDC2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.135	0.132 + 0.002*SL	0.111 + 0.002*SL	0.095 + 0.002*SL
	t_F	0.106	0.103 + 0.002*SL	0.084 + 0.002*SL	0.072 + 0.002*SL
	t_{PLH}	0.583	0.581 + 0.001*SL	0.589 + 0.001*SL	0.591 + 0.001*SL
	t_{PHL}	0.556	0.554 + 0.001*SL	0.559 + 0.001*SL	0.561 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PSCKDC4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.186	0.184 + 0.001*SL	0.164 + 0.001*SL	0.146 + 0.001*SL
	t_F	0.142	0.141 + 0.001*SL	0.120 + 0.001*SL	0.104 + 0.001*SL
	t_{PLH}	0.785	0.785 + 0.000*SL	0.805 + 0.000*SL	0.813 + 0.000*SL
	t_{PHL}	0.739	0.738 + 0.000*SL	0.751 + 0.000*SL	0.754 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PSCKDC6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.225	0.224 + 0.001*SL	0.214 + 0.001*SL	0.198 + 0.001*SL
	t_F	0.174	0.173 + 0.000*SL	0.154 + 0.001*SL	0.137 + 0.001*SL
	t_{PLH}	0.941	0.940 + 0.000*SL	0.971 + 0.000*SL	0.987 + 0.000*SL
	t_{PHL}	0.878	0.878 + 0.000*SL	0.897 + 0.000*SL	0.904 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PSCKDC8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.265	0.264 + 0.000*SL	0.267 + 0.000*SL	0.255 + 0.000*SL
	t_F	0.205	0.204 + 0.000*SL	0.191 + 0.000*SL	0.174 + 0.000*SL
	t_{PLH}	1.073	1.073 + 0.000*SL	1.114 + 0.000*SL	1.139 + 0.000*SL
	t_{PHL}	0.994	0.993 + 0.000*SL	1.020 + 0.000*SL	1.034 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PSCKDCD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.135	0.132 + 0.002*SL	0.110 + 0.002*SL	0.095 + 0.002*SL
	t_F	0.109	0.106 + 0.002*SL	0.087 + 0.002*SL	0.074 + 0.002*SL
	t_{PLH}	0.606	0.604 + 0.001*SL	0.612 + 0.001*SL	0.614 + 0.001*SL
	t_{PHL}	0.555	0.554 + 0.001*SL	0.558 + 0.001*SL	0.560 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PSCKDCD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.185	0.183 + 0.001*SL	0.163 + 0.001*SL	0.146 + 0.001*SL
	t_F	0.146	0.145 + 0.001*SL	0.122 + 0.001*SL	0.106 + 0.001*SL
	t_{PLH}	0.807	0.806 + 0.000*SL	0.827 + 0.000*SL	0.834 + 0.000*SL
	t_{PHL}	0.743	0.742 + 0.000*SL	0.755 + 0.000*SL	0.759 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PSCKDCD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.225	0.224 + 0.001*SL	0.213 + 0.001*SL	0.199 + 0.001*SL
	t_F	0.178	0.177 + 0.000*SL	0.157 + 0.001*SL	0.140 + 0.001*SL
	t_{PLH}	0.962	0.961 + 0.000*SL	0.993 + 0.000*SL	1.009 + 0.000*SL
	t_{PHL}	0.886	0.885 + 0.000*SL	0.904 + 0.000*SL	0.913 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PSCKDCD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.267	0.266 + 0.000*SL	0.269 + 0.000*SL	0.258 + 0.000*SL
	t_F	0.208	0.207 + 0.000*SL	0.193 + 0.000*SL	0.178 + 0.000*SL
	t_{PLH}	1.095	1.095 + 0.000*SL	1.137 + 0.000*SL	1.162 + 0.000*SL
	t_{PHL}	1.004	1.004 + 0.000*SL	1.030 + 0.000*SL	1.044 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

PvSCKDCby_LP

CMOS Level Input Clock Driver

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PSCKDCU2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.137	0.134 + 0.002*SL	0.113 + 0.002*SL	0.096 + 0.002*SL
	t_F	0.106	0.103 + 0.002*SL	0.085 + 0.002*SL	0.072 + 0.002*SL
	t_{PLH}	0.575	0.573 + 0.001*SL	0.582 + 0.001*SL	0.584 + 0.001*SL
	t_{PHL}	0.573	0.571 + 0.001*SL	0.576 + 0.001*SL	0.577 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PSCKDCU4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.188	0.186 + 0.001*SL	0.167 + 0.001*SL	0.149 + 0.001*SL
	t_F	0.142	0.141 + 0.001*SL	0.120 + 0.001*SL	0.105 + 0.001*SL
	t_{PLH}	0.781	0.780 + 0.000*SL	0.801 + 0.000*SL	0.809 + 0.000*SL
	t_{PHL}	0.756	0.755 + 0.000*SL	0.767 + 0.000*SL	0.771 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PSCKDCU6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.227	0.226 + 0.001*SL	0.216 + 0.001*SL	0.200 + 0.001*SL
	t_F	0.174	0.173 + 0.000*SL	0.154 + 0.001*SL	0.137 + 0.001*SL
	t_{PLH}	0.939	0.938 + 0.000*SL	0.970 + 0.000*SL	0.986 + 0.000*SL
	t_{PHL}	0.895	0.894 + 0.000*SL	0.913 + 0.000*SL	0.922 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PSCKDCU8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.267	0.266 + 0.000*SL	0.268 + 0.000*SL	0.256 + 0.000*SL
	t_F	0.205	0.204 + 0.000*SL	0.192 + 0.000*SL	0.176 + 0.000*SL
	t_{PLH}	1.073	1.073 + 0.000*SL	1.115 + 0.000*SL	1.139 + 0.000*SL
	t_{PHL}	1.011	1.011 + 0.000*SL	1.038 + 0.000*SL	1.051 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMSCKDC2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.121	0.118 + 0.002*SL	0.107 + 0.002*SL	0.100 + 0.002*SL
	t_F	0.129	0.125 + 0.002*SL	0.118 + 0.002*SL	0.111 + 0.002*SL
	t_{PLH}	0.909	0.907 + 0.001*SL	0.912 + 0.001*SL	0.913 + 0.001*SL
	t_{PHL}	0.926	0.924 + 0.001*SL	0.936 + 0.001*SL	0.942 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≤SL ≤ 438, *Group3 : 438 < SL

PMSCKDC4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.182	0.180 + 0.001*SL	0.165 + 0.001*SL	0.152 + 0.001*SL
	t_F	0.202	0.200 + 0.001*SL	0.196 + 0.001*SL	0.186 + 0.001*SL
	t_{PLH}	1.067	1.066 + 0.001*SL	1.083 + 0.000*SL	1.090 + 0.000*SL
	t_{PHL}	1.176	1.175 + 0.001*SL	1.202 + 0.001*SL	1.217 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≤ SL ≤ 875, *Group3 : 875 < SL

PMSCKDC6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.244	0.243 + 0.001*SL	0.232 + 0.001*SL	0.216 + 0.001*SL
	t_F	0.279	0.278 + 0.001*SL	0.277 + 0.001*SL	0.268 + 0.001*SL
	t_{PLH}	1.214	1.213 + 0.000*SL	1.244 + 0.000*SL	1.260 + 0.000*SL
	t_{PHL}	1.416	1.416 + 0.000*SL	1.456 + 0.000*SL	1.481 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≤ SL ≤ 1314, *Group3 : 1314 < SL

PMSCKDC8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.303	0.302 + 0.000*SL	0.298 + 0.000*SL	0.285 + 0.000*SL
	t_F	0.356	0.355 + 0.000*SL	0.359 + 0.000*SL	0.353 + 0.000*SL
	t_{PLH}	1.354	1.353 + 0.000*SL	1.396 + 0.000*SL	1.421 + 0.000*SL
	t_{PHL}	1.650	1.649 + 0.000*SL	1.701 + 0.000*SL	1.735 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≤ SL ≤ 1749, *Group3 : 1749 < SL

PvSCKDCby_LP

CMOS Level Input Clock Driver

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMSCKDCD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.122	0.118 + 0.002*SL	0.107 + 0.002*SL	0.100 + 0.002*SL
	t_F	0.129	0.126 + 0.002*SL	0.118 + 0.002*SL	0.111 + 0.002*SL
	t_{PLH}	0.925	0.923 + 0.001*SL	0.927 + 0.001*SL	0.929 + 0.001*SL
	t_{PHL}	0.923	0.921 + 0.001*SL	0.933 + 0.001*SL	0.939 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≤SL ≤ 438, *Group3 : 438 < SL

PMSCKDCD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.181	0.180 + 0.001*SL	0.165 + 0.001*SL	0.152 + 0.001*SL
	t_F	0.202	0.201 + 0.001*SL	0.195 + 0.001*SL	0.186 + 0.001*SL
	t_{PLH}	1.083	1.082 + 0.001*SL	1.099 + 0.000*SL	1.106 + 0.000*SL
	t_{PHL}	1.173	1.172 + 0.001*SL	1.200 + 0.001*SL	1.214 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≤ SL ≤ 875, *Group3 : 875 < SL

PMSCKDCD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.244	0.243 + 0.001*SL	0.232 + 0.001*SL	0.216 + 0.001*SL
	t_F	0.280	0.279 + 0.001*SL	0.276 + 0.001*SL	0.269 + 0.001*SL
	t_{PLH}	1.230	1.229 + 0.000*SL	1.260 + 0.000*SL	1.276 + 0.000*SL
	t_{PHL}	1.414	1.413 + 0.000*SL	1.453 + 0.000*SL	1.478 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≤ SL ≤ 1314, *Group3 : 1314 < SL

PMSCKDCD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.303	0.302 + 0.000*SL	0.298 + 0.000*SL	0.285 + 0.000*SL
	t_F	0.356	0.355 + 0.000*SL	0.359 + 0.000*SL	0.353 + 0.000*SL
	t_{PLH}	1.369	1.369 + 0.000*SL	1.412 + 0.000*SL	1.437 + 0.000*SL
	t_{PHL}	1.647	1.647 + 0.000*SL	1.698 + 0.000*SL	1.732 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≤ SL ≤ 1749, *Group3 : 1749 < SL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMSCKDCU2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.121	0.118 + 0.002*SL	0.107 + 0.002*SL	0.099 + 0.002*SL
	t_F	0.129	0.126 + 0.002*SL	0.119 + 0.002*SL	0.111 + 0.002*SL
	t_{PLH}	0.901	0.899 + 0.001*SL	0.903 + 0.001*SL	0.905 + 0.001*SL
	t_{PHL}	0.940	0.938 + 0.001*SL	0.951 + 0.001*SL	0.956 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≤SL ≤ 438, *Group3 : 438 < SL

PMSCKDCU4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.181	0.180 + 0.001*SL	0.165 + 0.001*SL	0.152 + 0.001*SL
	t_F	0.203	0.201 + 0.001*SL	0.195 + 0.001*SL	0.186 + 0.001*SL
	t_{PLH}	1.059	1.058 + 0.001*SL	1.075 + 0.000*SL	1.082 + 0.000*SL
	t_{PHL}	1.191	1.190 + 0.001*SL	1.217 + 0.001*SL	1.232 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≤ SL ≤ 875, *Group3 : 875 < SL

PMSCKDCU6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.244	0.243 + 0.001*SL	0.232 + 0.001*SL	0.216 + 0.001*SL
	t_F	0.280	0.279 + 0.001*SL	0.277 + 0.001*SL	0.269 + 0.001*SL
	t_{PLH}	1.206	1.205 + 0.000*SL	1.236 + 0.000*SL	1.251 + 0.000*SL
	t_{PHL}	1.431	1.430 + 0.000*SL	1.470 + 0.000*SL	1.495 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≤ SL ≤ 1314, *Group3 : 1314 < SL

PMSCKDCU8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.303	0.302 + 0.000*SL	0.298 + 0.000*SL	0.285 + 0.000*SL
	t_F	0.356	0.355 + 0.000*SL	0.359 + 0.000*SL	0.353 + 0.000*SL
	t_{PLH}	1.345	1.345 + 0.000*SL	1.388 + 0.000*SL	1.413 + 0.000*SL
	t_{PHL}	1.665	1.664 + 0.000*SL	1.716 + 0.000*SL	1.749 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≤ SL ≤ 1749, *Group3 : 1749 < SL

PvSCKDCby_LP

CMOS Level Input Clock Driver

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHSCKDC2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.125	0.121 + 0.002*SL	0.110 + 0.002*SL	0.102 + 0.002*SL
	t_F	0.105	0.102 + 0.002*SL	0.095 + 0.002*SL	0.088 + 0.002*SL
	t_{PLH}	0.667	0.665 + 0.001*SL	0.670 + 0.001*SL	0.671 + 0.001*SL
	t_{PHL}	1.012	1.010 + 0.001*SL	1.017 + 0.001*SL	1.021 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PHSCKDC4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.184	0.183 + 0.001*SL	0.168 + 0.001*SL	0.155 + 0.001*SL
	t_F	0.150	0.148 + 0.001*SL	0.141 + 0.001*SL	0.132 + 0.001*SL
	t_{PLH}	0.826	0.825 + 0.001*SL	0.842 + 0.000*SL	0.850 + 0.000*SL
	t_{PHL}	1.187	1.186 + 0.001*SL	1.202 + 0.000*SL	1.210 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PHSCKDC6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.247	0.246 + 0.001*SL	0.235 + 0.001*SL	0.219 + 0.001*SL
	t_F	0.200	0.199 + 0.001*SL	0.194 + 0.001*SL	0.185 + 0.001*SL
	t_{PLH}	0.973	0.972 + 0.000*SL	1.003 + 0.000*SL	1.019 + 0.000*SL
	t_{PHL}	1.352	1.351 + 0.000*SL	1.379 + 0.000*SL	1.393 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PHSCKDC8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.306	0.305 + 0.000*SL	0.302 + 0.000*SL	0.288 + 0.000*SL
	t_F	0.252	0.251 + 0.000*SL	0.249 + 0.000*SL	0.239 + 0.000*SL
	t_{PLH}	1.112	1.111 + 0.000*SL	1.155 + 0.000*SL	1.181 + 0.000*SL
	t_{PHL}	1.513	1.513 + 0.000*SL	1.548 + 0.000*SL	1.570 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHSCKDCD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.125	0.121 + 0.002*SL	0.110 + 0.002*SL	0.102 + 0.002*SL
	t_F	0.104	0.101 + 0.002*SL	0.094 + 0.002*SL	0.089 + 0.002*SL
	t_{PLH}	0.691	0.689 + 0.001*SL	0.695 + 0.001*SL	0.697 + 0.001*SL
	t_{PHL}	1.021	1.019 + 0.001*SL	1.027 + 0.001*SL	1.030 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PHSCKDCD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.185	0.183 + 0.001*SL	0.168 + 0.001*SL	0.155 + 0.001*SL
	t_F	0.150	0.149 + 0.001*SL	0.141 + 0.001*SL	0.132 + 0.001*SL
	t_{PLH}	0.850	0.849 + 0.001*SL	0.867 + 0.000*SL	0.874 + 0.000*SL
	t_{PHL}	1.195	1.194 + 0.001*SL	1.212 + 0.000*SL	1.220 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PHSCKDCD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.247	0.246 + 0.001*SL	0.235 + 0.001*SL	0.220 + 0.001*SL
	t_F	0.200	0.199 + 0.001*SL	0.194 + 0.001*SL	0.184 + 0.001*SL
	t_{PLH}	0.997	0.996 + 0.000*SL	1.028 + 0.000*SL	1.044 + 0.000*SL
	t_{PHL}	1.361	1.360 + 0.000*SL	1.387 + 0.000*SL	1.403 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PHSCKDCD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.306	0.305 + 0.000*SL	0.302 + 0.000*SL	0.288 + 0.000*SL
	t_F	0.253	0.252 + 0.000*SL	0.249 + 0.000*SL	0.240 + 0.000*SL
	t_{PLH}	1.136	1.136 + 0.000*SL	1.180 + 0.000*SL	1.205 + 0.000*SL
	t_{PHL}	1.522	1.522 + 0.000*SL	1.558 + 0.000*SL	1.580 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

PvSCKDCby_LP

CMOS Level Input Clock Driver

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHSCKDCU2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.125	0.121 + 0.002*SL	0.109 + 0.002*SL	0.101 + 0.002*SL
	t_F	0.104	0.101 + 0.002*SL	0.095 + 0.002*SL	0.088 + 0.002*SL
	t_{PLH}	0.657	0.656 + 0.001*SL	0.661 + 0.001*SL	0.663 + 0.001*SL
	t_{PHL}	1.027	1.025 + 0.001*SL	1.033 + 0.001*SL	1.036 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PHSCKDCU4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.185	0.183 + 0.001*SL	0.168 + 0.001*SL	0.155 + 0.001*SL
	t_F	0.150	0.148 + 0.001*SL	0.141 + 0.001*SL	0.132 + 0.001*SL
	t_{PLH}	0.816	0.815 + 0.001*SL	0.833 + 0.000*SL	0.840 + 0.000*SL
	t_{PHL}	1.201	1.200 + 0.001*SL	1.218 + 0.000*SL	1.226 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PHSCKDCU6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.247	0.246 + 0.001*SL	0.235 + 0.001*SL	0.220 + 0.001*SL
	t_F	0.200	0.199 + 0.001*SL	0.194 + 0.001*SL	0.185 + 0.001*SL
	t_{PLH}	0.963	0.963 + 0.000*SL	0.994 + 0.000*SL	1.010 + 0.000*SL
	t_{PHL}	1.367	1.366 + 0.000*SL	1.393 + 0.000*SL	1.408 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PHSCKDCU8_LP

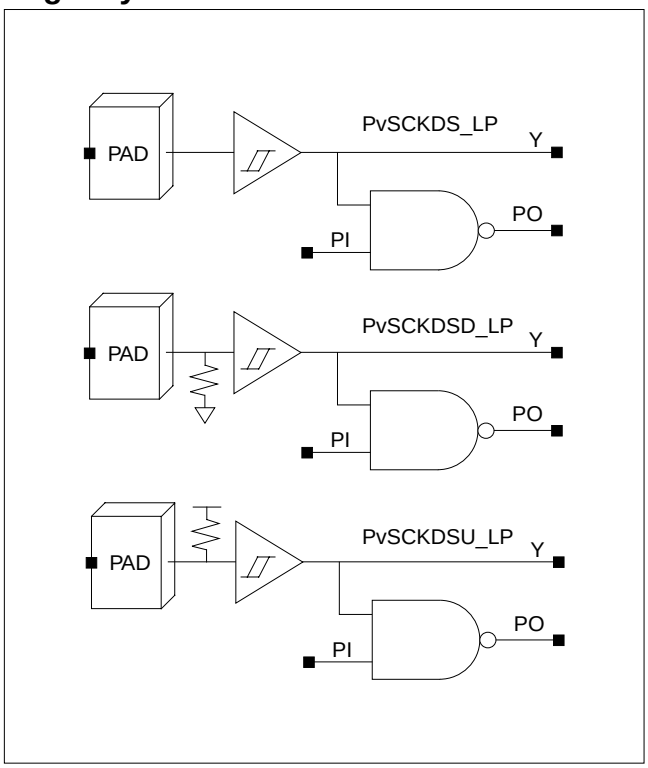
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.307	0.306 + 0.000*SL	0.302 + 0.000*SL	0.287 + 0.000*SL
	t_F	0.252	0.251 + 0.000*SL	0.249 + 0.000*SL	0.240 + 0.000*SL
	t_{PLH}	1.102	1.102 + 0.000*SL	1.146 + 0.000*SL	1.171 + 0.000*SL
	t_{PHL}	1.528	1.528 + 0.000*SL	1.563 + 0.000*SL	1.585 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

Cell Availability

1.8V Interface	2.5V Interface	3.3V Interface
PSCKDS(2/4/6/8)_LP PSCKDSD(2/4/6/8)_LP PSCKDSU(2/4/6/8)_LP	PMSCKDS(2/4/6/8)_LP PMSCKDSD(2/4/6/8)_LP PMSCKDSU(2/4/6/8)_LP	PHSCKDS(2/4/6/8)_LP PHSCKDSD(2/4/6/8)_LP PHSCKDSU(2/4/6/8)_LP

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PSCKDS/PSCKDSD/PSCKDSU(2/4/6/8)_LP	3.79
PMSCKSC/PMSCKDSD/PMSCKDSU(2/4/6/8)_LP	3.74
PHSCKDS/PHSCKDSD/PHSCKDSU(2/4/6/8)_LP	3.74

PvSCKDSby_LP

CMOS Schmitt Trigger Level Input Clock Driver

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PSCKDS2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.139	0.135 + 0.002*SL	0.121 + 0.002*SL	0.107 + 0.002*SL
	t_F	0.153	0.150 + 0.002*SL	0.136 + 0.002*SL	0.123 + 0.002*SL
	t_{PLH}	0.854	0.853 + 0.001*SL	0.866 + 0.001*SL	0.871 + 0.001*SL
	t_{PHL}	0.926	0.925 + 0.001*SL	0.943 + 0.001*SL	0.951 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PSCKDS4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.200	0.199 + 0.001*SL	0.193 + 0.001*SL	0.182 + 0.001*SL
	t_F	0.227	0.226 + 0.001*SL	0.221 + 0.001*SL	0.209 + 0.001*SL
	t_{PLH}	1.065	1.064 + 0.000*SL	1.094 + 0.000*SL	1.110 + 0.000*SL
	t_{PHL}	1.178	1.177 + 0.001*SL	1.211 + 0.000*SL	1.231 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PSCKDS6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.264	0.263 + 0.001*SL	0.271 + 0.001*SL	0.265 + 0.001*SL
	t_F	0.309	0.308 + 0.001*SL	0.316 + 0.001*SL	0.308 + 0.001*SL
	t_{PLH}	1.243	1.242 + 0.000*SL	1.287 + 0.000*SL	1.314 + 0.000*SL
	t_{PHL}	1.407	1.406 + 0.000*SL	1.454 + 0.000*SL	1.484 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PSCKDS8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.324	0.323 + 0.000*SL	0.345 + 0.000*SL	0.346 + 0.000*SL
	t_F	0.388	0.387 + 0.000*SL	0.408 + 0.000*SL	0.406 + 0.000*SL
	t_{PLH}	1.411	1.410 + 0.000*SL	1.466 + 0.000*SL	1.503 + 0.000*SL
	t_{PHL}	1.627	1.626 + 0.000*SL	1.686 + 0.000*SL	1.726 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PSCKDSD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.141	0.138 + 0.002*SL	0.122 + 0.002*SL	0.109 + 0.002*SL
	t_F	0.156	0.153 + 0.002*SL	0.139 + 0.002*SL	0.126 + 0.002*SL
	t_{PLH}	0.858	0.856 + 0.001*SL	0.870 + 0.001*SL	0.875 + 0.001*SL
	t_{PHL}	0.938	0.936 + 0.001*SL	0.955 + 0.001*SL	0.963 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PSCKDSD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.203	0.201 + 0.001*SL	0.196 + 0.001*SL	0.184 + 0.001*SL
	t_F	0.230	0.228 + 0.001*SL	0.223 + 0.001*SL	0.213 + 0.001*SL
	t_{PLH}	1.069	1.068 + 0.000*SL	1.099 + 0.000*SL	1.115 + 0.000*SL
	t_{PHL}	1.195	1.193 + 0.001*SL	1.228 + 0.000*SL	1.248 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PSCKDSD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.267	0.266 + 0.001*SL	0.275 + 0.001*SL	0.269 + 0.001*SL
	t_F	0.312	0.311 + 0.001*SL	0.319 + 0.001*SL	0.311 + 0.001*SL
	t_{PLH}	1.248	1.247 + 0.000*SL	1.292 + 0.000*SL	1.320 + 0.000*SL
	t_{PHL}	1.426	1.425 + 0.000*SL	1.473 + 0.000*SL	1.504 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PSCKDSD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.327	0.327 + 0.000*SL	0.349 + 0.000*SL	0.351 + 0.000*SL
	t_F	0.390	0.389 + 0.000*SL	0.410 + 0.000*SL	0.408 + 0.000*SL
	t_{PLH}	1.417	1.416 + 0.000*SL	1.472 + 0.000*SL	1.511 + 0.000*SL
	t_{PHL}	1.648	1.647 + 0.000*SL	1.708 + 0.000*SL	1.748 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

PvSCKDSby_LP

CMOS Schmitt Trigger Level Input Clock Driver

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PSCKDSU2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.141	0.138 + 0.002*SL	0.122 + 0.002*SL	0.109 + 0.002*SL
	t_F	0.154	0.151 + 0.002*SL	0.138 + 0.002*SL	0.124 + 0.002*SL
	t_{PLH}	0.862	0.860 + 0.001*SL	0.874 + 0.001*SL	0.879 + 0.001*SL
	t_{PHL}	0.941	0.939 + 0.001*SL	0.958 + 0.001*SL	0.966 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PSCKDSU4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.201	0.200 + 0.001*SL	0.194 + 0.001*SL	0.182 + 0.001*SL
	t_F	0.230	0.229 + 0.001*SL	0.224 + 0.001*SL	0.213 + 0.001*SL
	t_{PLH}	1.074	1.073 + 0.000*SL	1.104 + 0.000*SL	1.120 + 0.000*SL
	t_{PHL}	1.194	1.193 + 0.001*SL	1.227 + 0.000*SL	1.248 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PSCKDSU6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.265	0.264 + 0.001*SL	0.272 + 0.001*SL	0.265 + 0.001*SL
	t_F	0.314	0.313 + 0.001*SL	0.321 + 0.001*SL	0.313 + 0.001*SL
	t_{PLH}	1.254	1.253 + 0.000*SL	1.298 + 0.000*SL	1.326 + 0.000*SL
	t_{PHL}	1.426	1.425 + 0.000*SL	1.474 + 0.000*SL	1.505 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PSCKDSU8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.325	0.324 + 0.000*SL	0.345 + 0.000*SL	0.346 + 0.000*SL
	t_F	0.394	0.393 + 0.000*SL	0.413 + 0.000*SL	0.413 + 0.000*SL
	t_{PLH}	1.422	1.422 + 0.000*SL	1.478 + 0.000*SL	1.515 + 0.000*SL
	t_{PHL}	1.650	1.649 + 0.000*SL	1.710 + 0.000*SL	1.750 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMSCKDS2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.121	0.117 + 0.002*SL	0.107 + 0.002*SL	0.099 + 0.002*SL
	t_F	0.129	0.126 + 0.002*SL	0.118 + 0.002*SL	0.111 + 0.002*SL
	t_{PLH}	1.087	1.085 + 0.001*SL	1.089 + 0.001*SL	1.091 + 0.001*SL
	t_{PHL}	1.347	1.345 + 0.001*SL	1.357 + 0.001*SL	1.362 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PMSCKDS4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.181	0.179 + 0.001*SL	0.165 + 0.001*SL	0.152 + 0.001*SL
	t_F	0.202	0.200 + 0.001*SL	0.195 + 0.001*SL	0.186 + 0.001*SL
	t_{PLH}	1.245	1.244 + 0.001*SL	1.261 + 0.000*SL	1.268 + 0.000*SL
	t_{PHL}	1.597	1.596 + 0.001*SL	1.623 + 0.001*SL	1.637 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PMSCKDS6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.244	0.243 + 0.001*SL	0.231 + 0.001*SL	0.216 + 0.001*SL
	t_F	0.280	0.279 + 0.001*SL	0.277 + 0.001*SL	0.269 + 0.001*SL
	t_{PLH}	1.392	1.391 + 0.000*SL	1.422 + 0.000*SL	1.437 + 0.000*SL
	t_{PHL}	1.837	1.836 + 0.000*SL	1.876 + 0.000*SL	1.901 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PMSCKDS8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.304	0.303 + 0.000*SL	0.299 + 0.000*SL	0.283 + 0.000*SL
	t_F	0.356	0.356 + 0.000*SL	0.359 + 0.000*SL	0.352 + 0.000*SL
	t_{PLH}	1.531	1.530 + 0.000*SL	1.574 + 0.000*SL	1.598 + 0.000*SL
	t_{PHL}	2.071	2.070 + 0.000*SL	2.122 + 0.000*SL	2.155 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

PvSCKDSby_LP

CMOS Schmitt Trigger Level Input Clock Driver

Switching Characteristics (Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMSCKDSD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.121	0.117 + 0.002*SL	0.107 + 0.002*SL	0.100 + 0.002*SL
	t_F	0.129	0.126 + 0.002*SL	0.118 + 0.002*SL	0.111 + 0.002*SL
	t_{PLH}	1.092	1.090 + 0.001*SL	1.095 + 0.001*SL	1.097 + 0.001*SL
	t_{PHL}	1.367	1.365 + 0.001*SL	1.377 + 0.001*SL	1.382 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PMSCKDSD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.181	0.180 + 0.001*SL	0.165 + 0.001*SL	0.152 + 0.001*SL
	t_F	0.202	0.200 + 0.001*SL	0.195 + 0.001*SL	0.186 + 0.001*SL
	t_{PLH}	1.251	1.250 + 0.001*SL	1.267 + 0.000*SL	1.273 + 0.000*SL
	t_{PHL}	1.617	1.616 + 0.001*SL	1.643 + 0.001*SL	1.657 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PMSCKDSD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.244	0.243 + 0.001*SL	0.232 + 0.001*SL	0.216 + 0.001*SL
	t_F	0.280	0.279 + 0.001*SL	0.277 + 0.001*SL	0.269 + 0.001*SL
	t_{PLH}	1.398	1.397 + 0.000*SL	1.428 + 0.000*SL	1.443 + 0.000*SL
	t_{PHL}	1.857	1.856 + 0.000*SL	1.897 + 0.000*SL	1.922 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PMSCKDSD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.303	0.302 + 0.000*SL	0.298 + 0.000*SL	0.285 + 0.000*SL
	t_F	0.356	0.356 + 0.000*SL	0.359 + 0.000*SL	0.352 + 0.000*SL
	t_{PLH}	1.537	1.536 + 0.000*SL	1.579 + 0.000*SL	1.604 + 0.000*SL
	t_{PHL}	2.091	2.090 + 0.000*SL	2.141 + 0.000*SL	2.176 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMSCKDSU2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.121	0.118 + 0.002*SL	0.107 + 0.002*SL	0.100 + 0.002*SL
	t_F	0.129	0.126 + 0.002*SL	0.119 + 0.002*SL	0.111 + 0.002*SL
	t_{PLH}	1.091	1.089 + 0.001*SL	1.094 + 0.001*SL	1.096 + 0.001*SL
	t_{PHL}	1.355	1.353 + 0.001*SL	1.365 + 0.001*SL	1.370 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PMSCKDSU4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.181	0.179 + 0.001*SL	0.165 + 0.001*SL	0.152 + 0.001*SL
	t_F	0.202	0.201 + 0.001*SL	0.195 + 0.001*SL	0.186 + 0.001*SL
	t_{PLH}	1.250	1.249 + 0.001*SL	1.266 + 0.000*SL	1.272 + 0.000*SL
	t_{PHL}	1.605	1.604 + 0.001*SL	1.631 + 0.001*SL	1.646 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PMSCKDSU6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.244	0.242 + 0.001*SL	0.232 + 0.001*SL	0.216 + 0.001*SL
	t_F	0.280	0.279 + 0.001*SL	0.276 + 0.001*SL	0.269 + 0.001*SL
	t_{PLH}	1.397	1.396 + 0.000*SL	1.427 + 0.000*SL	1.442 + 0.000*SL
	t_{PHL}	1.845	1.844 + 0.000*SL	1.884 + 0.000*SL	1.910 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PMSCKDSU8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.303	0.303 + 0.000*SL	0.299 + 0.000*SL	0.284 + 0.000*SL
	t_F	0.356	0.355 + 0.000*SL	0.359 + 0.000*SL	0.352 + 0.000*SL
	t_{PLH}	1.536	1.535 + 0.000*SL	1.578 + 0.000*SL	1.603 + 0.000*SL
	t_{PHL}	2.079	2.078 + 0.000*SL	2.130 + 0.000*SL	2.164 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

PvSCKDSby_LP

CMOS Schmitt Trigger Level Input Clock Driver

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHSCKDS2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.125	0.121 + 0.002*SL	0.109 + 0.002*SL	0.101 + 0.002*SL
	t_F	0.105	0.101 + 0.002*SL	0.094 + 0.002*SL	0.088 + 0.002*SL
	t_{PLH}	0.919	0.917 + 0.001*SL	0.922 + 0.001*SL	0.923 + 0.001*SL
	t_{PHL}	1.368	1.366 + 0.001*SL	1.373 + 0.001*SL	1.377 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PHSCKDS4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.185	0.183 + 0.001*SL	0.168 + 0.001*SL	0.155 + 0.001*SL
	t_F	0.150	0.148 + 0.001*SL	0.141 + 0.001*SL	0.132 + 0.001*SL
	t_{PLH}	1.078	1.077 + 0.001*SL	1.095 + 0.000*SL	1.101 + 0.000*SL
	t_{PHL}	1.542	1.541 + 0.001*SL	1.558 + 0.000*SL	1.566 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PHSCKDS6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.247	0.246 + 0.001*SL	0.235 + 0.001*SL	0.219 + 0.001*SL
	t_F	0.201	0.200 + 0.001*SL	0.194 + 0.001*SL	0.184 + 0.001*SL
	t_{PLH}	1.225	1.224 + 0.000*SL	1.255 + 0.000*SL	1.271 + 0.000*SL
	t_{PHL}	1.708	1.707 + 0.000*SL	1.734 + 0.000*SL	1.749 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PHSCKDS8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.306	0.306 + 0.000*SL	0.302 + 0.000*SL	0.287 + 0.000*SL
	t_F	0.252	0.251 + 0.000*SL	0.249 + 0.000*SL	0.239 + 0.000*SL
	t_{PLH}	1.364	1.363 + 0.000*SL	1.407 + 0.000*SL	1.433 + 0.000*SL
	t_{PHL}	1.869	1.868 + 0.000*SL	1.904 + 0.000*SL	1.926 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

Switching Characteristics

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHSCKDSD2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.124	0.120 + 0.002*SL	0.110 + 0.002*SL	0.102 + 0.002*SL
	t_F	0.104	0.101 + 0.002*SL	0.094 + 0.002*SL	0.088 + 0.002*SL
	t_{PLH}	0.932	0.930 + 0.001*SL	0.935 + 0.001*SL	0.937 + 0.001*SL
	t_{PHL}	1.398	1.396 + 0.001*SL	1.404 + 0.001*SL	1.406 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PHSCKDSD4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.185	0.183 + 0.001*SL	0.168 + 0.001*SL	0.155 + 0.001*SL
	t_F	0.150	0.148 + 0.001*SL	0.141 + 0.001*SL	0.132 + 0.001*SL
	t_{PLH}	1.091	1.090 + 0.001*SL	1.108 + 0.000*SL	1.115 + 0.000*SL
	t_{PHL}	1.572	1.571 + 0.001*SL	1.588 + 0.000*SL	1.596 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PHSCKDSD6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.247	0.246 + 0.001*SL	0.235 + 0.001*SL	0.219 + 0.001*SL
	t_F	0.200	0.199 + 0.001*SL	0.194 + 0.001*SL	0.185 + 0.001*SL
	t_{PLH}	1.238	1.237 + 0.000*SL	1.269 + 0.000*SL	1.285 + 0.000*SL
	t_{PHL}	1.738	1.737 + 0.000*SL	1.764 + 0.000*SL	1.779 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PHSCKDSD8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.306	0.305 + 0.000*SL	0.302 + 0.000*SL	0.288 + 0.000*SL
	t_F	0.252	0.252 + 0.000*SL	0.249 + 0.000*SL	0.240 + 0.000*SL
	t_{PLH}	1.377	1.377 + 0.000*SL	1.421 + 0.000*SL	1.446 + 0.000*SL
	t_{PHL}	1.899	1.898 + 0.000*SL	1.934 + 0.000*SL	1.956 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

PvSCKDSby_LP

CMOS Schmitt Trigger Level Input Clock Driver

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHSCKDSU2_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.125	0.121 + 0.002*SL	0.109 + 0.002*SL	0.102 + 0.002*SL
	t_F	0.104	0.101 + 0.002*SL	0.095 + 0.002*SL	0.088 + 0.002*SL
	t_{PLH}	0.926	0.924 + 0.001*SL	0.929 + 0.001*SL	0.930 + 0.001*SL
	t_{PHL}	1.396	1.394 + 0.001*SL	1.402 + 0.001*SL	1.404 + 0.001*SL

*Group1 : SL < 292, *Group2 : 292 ≦SL ≦ 438, *Group3 : 438 < SL

PHSCKDSU4_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.185	0.183 + 0.001*SL	0.168 + 0.001*SL	0.155 + 0.001*SL
	t_F	0.150	0.148 + 0.001*SL	0.141 + 0.001*SL	0.132 + 0.001*SL
	t_{PLH}	1.084	1.083 + 0.001*SL	1.101 + 0.000*SL	1.108 + 0.000*SL
	t_{PHL}	1.570	1.569 + 0.001*SL	1.586 + 0.000*SL	1.594 + 0.000*SL

*Group1 : SL < 584, *Group2 : 584 ≦ SL ≦ 875, *Group3 : 875 < SL

PHSCKDSU6_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.248	0.246 + 0.001*SL	0.235 + 0.001*SL	0.219 + 0.001*SL
	t_F	0.200	0.199 + 0.001*SL	0.194 + 0.001*SL	0.185 + 0.001*SL
	t_{PLH}	1.232	1.231 + 0.000*SL	1.262 + 0.000*SL	1.278 + 0.000*SL
	t_{PHL}	1.736	1.735 + 0.000*SL	1.762 + 0.000*SL	1.777 + 0.000*SL

*Group1 : SL < 876, *Group2 : 876 ≦ SL ≦ 1314, *Group3 : 1314 < SL

PHSCKDSU8_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.306	0.305 + 0.000*SL	0.302 + 0.000*SL	0.288 + 0.000*SL
	t_F	0.252	0.251 + 0.000*SL	0.249 + 0.000*SL	0.239 + 0.000*SL
	t_{PLH}	1.371	1.370 + 0.000*SL	1.414 + 0.000*SL	1.439 + 0.000*SL
	t_{PHL}	1.897	1.896 + 0.000*SL	1.932 + 0.000*SL	1.954 + 0.000*SL

*Group1 : SL < 1166, *Group2 : 1166 ≦ SL ≦ 1749, *Group3 : 1749 < SL

DC Electrical Chracteristic

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Vih	High level input voltage		0.8×Vdd		Vdd	V
Vil	Low level input voltage		Vss		0.2×Vdd	V
Iih	High level input current	Vin=Vdd	–10		10	µA
Iil	Low level input current	Vin=Vss	–10		10	µA
Cin	Input capacitance				7	pF
Cout	Output capacitance				7	pF

OSCILLATORS

Cell List

Cell Name	Function Description
PHSOSCK1_LP	Oscillator Cell with Enable (~ 100kHz)
PHSOSCK2_LP	Oscillator Cell with Enable (100K ~ 1MHz)
PHSOSCK17_LP	Oscillator Cell with Enable and Feedback Resistor 10MΩ (~ 100kHz)
PHSOSCK27_LP	Oscillator Cell with Enable and Feedback Resistor 10MΩ (100K ~ 1MHz)
PHSOSCM1_LP	Oscillator Cell with Enable (1M ~ 10MHz)
PHSOSCM2_LP	Oscillator Cell with Enable (10M ~ 40MHz)
PHSOSCM3_LP	Oscillator Cell with Enable (40M ~ 100MHz)
PHSOSCM16_LP	Oscillator Cell with Enable and Feedback Resistor 1MΩ (1M ~ 10MHz)
PHSOSCM26_LP	Oscillator Cell with Enable and Feedback Resistor 1MΩ (10M ~ 40MHz)
PHSOSCM36_LP	Oscillator Cell with Enable and Feedback Resistor 1MΩ (40M ~ 100MHz)

NOTE: Use I/O 3.3V and Core 1.8V

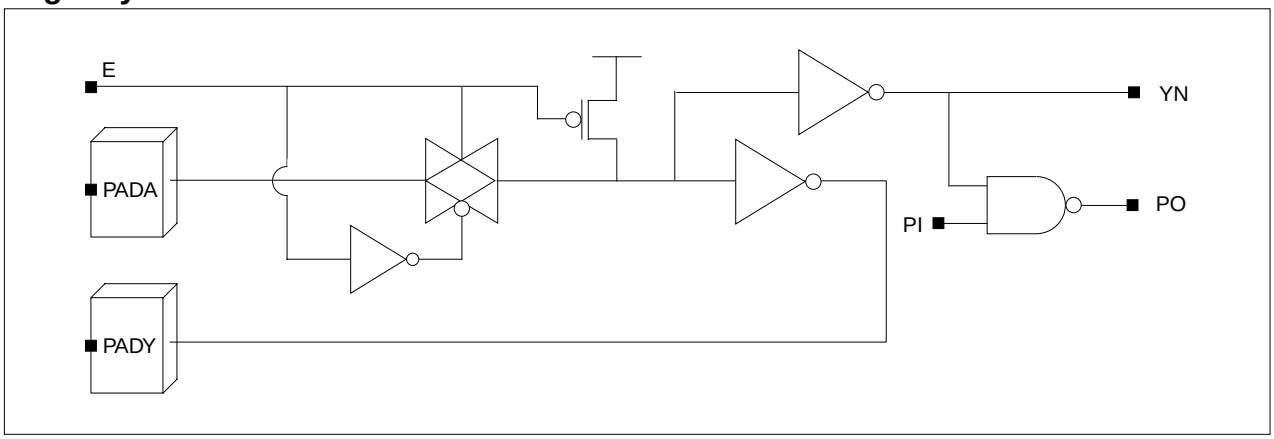
Cell Name	Function Description
PMSOSCK1_LP	Oscillator Cell with Enable (~ 100kHz)
PMSOSCK2_LP	Oscillator Cell with Enable (100K ~ 1MHz)
PMSOSCM1_LP	Oscillator Cell with Enable (1M ~ 10MHz)
PMSOSCM2_LP	Oscillator Cell with Enable (10M ~ 40MHz)

NOTE: Use I/O 2.5V and Core 1.8V

Cell Name	Function Description
PSOSCK1_LP	Oscillator Cell with Enable (~ 100kHz)
PSOSCK2_LP	Oscillator Cell with Enable (100K ~ 1MHz)
PSOSCM1_LP	Oscillator Cell with Enable (1M ~ 10MHz)
PSOSCM2_LP	Oscillator Cell with Enable (10M ~ 40MHz)

NOTE: Use I/O 1.8V and Core 1.8V

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)	
PHSOSCK1_LP/K2_LP	*PHSOSCM1_LP/M2_LP/M3_LP*
E	E
3.77	3.77
I/O Sizes	
PHSOSCK1_LP/K2_LP	*PHSOSCM1_LP/M2_LP/M3_LP*
2 I/O Slots	2 I/O Slots

Switching Characteristics

PHSOSCK1_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	1770.700	155.200 + 32.310*CL	155.700 + 32.300*CL	155.700 + 32.300*CL
	t_F	1392.600	139.025 + 25.071*CL	139.000 + 25.072*CL	138.700 + 25.076*CL
	t_{PLH}	869.350	100.925 + 15.369*CL	100.850 + 15.370*CL	101.000 + 15.368*CL
	t_{PHL}	680.190	53.565 + 12.533*CL	53.550 + 12.533*CL	53.640 + 12.532*CL
E to PADY	t_R	1770.700	155.200 + 32.310*CL	155.700 + 32.300*CL	155.700 + 32.300*CL
	t_F	1392.600	139.000 + 25.072*CL	139.000 + 25.072*CL	138.700 + 25.076*CL
	t_{PLH}	869.580	101.155 + 15.369*CL	101.140 + 15.369*CL	101.200 + 15.368*CL
	t_{PHL}	679.850	53.225 + 12.533*CL	53.210 + 12.533*CL	53.180 + 12.533*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.160	0.144 + 0.008*SL	0.145 + 0.007*SL	0.145 + 0.007*SL
	t_F	0.117	0.103 + 0.008*SL	0.105 + 0.006*SL	0.105 + 0.006*SL
	t_{PLH}	35.654	35.640 + 0.007*SL	35.641 + 0.006*SL	35.644 + 0.005*SL
	t_{PHL}	38.671	37.910 + 0.687*SL	38.660 + 0.006*SL	38.662 + 0.005*SL
E to YN	t_R	0.159	0.145 + 0.007*SL	0.145 + 0.007*SL	0.145 + 0.007*SL
	t_F	0.117	0.104 + 0.007*SL	0.103 + 0.007*SL	0.106 + 0.006*SL
	t_{PLH}	35.673	35.661 + 0.006*SL	35.660 + 0.007*SL	35.664 + 0.005*SL
	t_{PHL}	37.822	37.809 + 0.007*SL	37.811 + 0.006*SL	37.812 + 0.005*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 4, *Group3 : 4 < SL

Switching Characteristics

PHSOSCK2_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	227.450	19.150 + 4.166*CL	19.190 + 4.165*CL	19.160 + 4.166*CL
	t_F	238.400	24.000 + 4.288*CL	23.940 + 4.289*CL	23.940 + 4.289*CL
	t_{PLH}	98.324	12.107 + 1.724*CL	12.112 + 1.724*CL	12.070 + 1.725*CL
	t_{PHL}	110.410	9.195 + 2.024*CL	9.190 + 2.024*CL	9.190 + 2.024*CL
E to PADY	t_R	227.450	19.175 + 4.165*CL	19.170 + 4.166*CL	19.200 + 4.165*CL
	t_F	238.400	23.975 + 4.289*CL	23.940 + 4.289*CL	23.940 + 4.289*CL
	t_{PLH}	98.421	12.206 + 1.724*CL	12.203 + 1.724*CL	12.170 + 1.725*CL
	t_{PHL}	110.300	9.090 + 2.024*CL	9.080 + 2.024*CL	9.080 + 2.024*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°2C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.148	0.144 + 0.002*SL	0.145 + 0.002*SL	0.145 + 0.002*SL
	t_F	0.107	0.103 + 0.002*SL	0.105 + 0.002*SL	0.105 + 0.002*SL
	t_{PLH}	6.369	6.365 + 0.002*SL	6.366 + 0.002*SL	6.369 + 0.001*SL
	t_{PHL}	6.006	6.003 + 0.002*SL	6.003 + 0.001*SL	6.006 + 0.001*SL
E to YN	t_R	0.148	0.145 + 0.002*SL	0.145 + 0.002*SL	0.146 + 0.002*SL
	t_F	0.106	0.103 + 0.002*SL	0.103 + 0.002*SL	0.106 + 0.001*SL
	t_{PLH}	6.052	6.049 + 0.002*SL	6.049 + 0.002*SL	6.053 + 0.001*SL
	t_{PHL}	5.629	5.626 + 0.002*SL	5.626 + 0.001*SL	5.629 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PHSOSCM1_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	21.273	1.203 + 0.401*CL	1.181 + 0.402*CL	1.250 + 0.401*CL
	t_F	23.779	1.329 + 0.449*CL	1.429 + 0.447*CL	1.414 + 0.447*CL
	t_{PLH}	10.847	1.349 + 0.190*CL	1.397 + 0.189*CL	1.370 + 0.189*CL
	t_{PHL}	13.376	1.446 + 0.239*CL	1.428 + 0.239*CL	1.419 + 0.239*CL
E to PADY	t_R	21.323	1.298 + 0.400*CL	1.277 + 0.401*CL	1.277 + 0.401*CL
	t_F	23.778	1.321 + 0.449*CL	1.436 + 0.447*CL	1.418 + 0.447*CL
	t_{PLH}	10.950	1.511 + 0.189*CL	1.466 + 0.190*CL	1.481 + 0.189*CL
	t_{PHL}	13.514	1.559 + 0.239*CL	1.554 + 0.239*CL	1.551 + 0.239*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.141	0.137 + 0.002*SL	0.138 + 0.002*SL	0.137 + 0.002*SL
	t_F	0.107	0.104 + 0.002*SL	0.104 + 0.002*SL	0.107 + 0.001*SL
	t_{PLH}	1.686	1.682 + 0.002*SL	1.683 + 0.001*SL	1.686 + 0.001*SL
	t_{PHL}	1.102	1.099 + 0.002*SL	1.099 + 0.001*SL	1.103 + 0.001*SL
E to YN	t_R	0.141	0.137 + 0.002*SL	0.138 + 0.002*SL	0.137 + 0.002*SL
	t_F	0.107	0.104 + 0.002*SL	0.103 + 0.002*SL	0.106 + 0.002*SL
	t_{PLH}	2.123	2.120 + 0.002*SL	2.121 + 0.001*SL	2.123 + 0.001*SL
	t_{PHL}	1.464	1.461 + 0.002*SL	1.461 + 0.001*SL	1.464 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PHSOSCM2_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	5.755	0.611 + 0.103*CL	0.871 + 0.098*CL	0.814 + 0.098*CL
	t_F	6.257	0.753 + 0.110*CL	0.782 + 0.109*CL	0.172 + 0.118*CL
	t_{PLH}	3.645	1.291 + 0.047*CL	1.247 + 0.048*CL	1.272 + 0.048*CL
	t_{PHL}	4.234	1.256 + 0.060*CL	1.226 + 0.060*CL	1.196 + 0.061*CL
E to PADY	t_R	5.511	1.017 + 0.090*CL	0.369 + 0.103*CL	0.598 + 0.100*CL
	t_F	6.185	0.427 + 0.115*CL	0.557 + 0.113*CL	0.213 + 0.117*CL
	t_{PLH}	3.824	1.408 + 0.048*CL	1.400 + 0.048*CL	1.419 + 0.048*CL
	t_{PHL}	4.524	1.482 + 0.061*CL	1.482 + 0.061*CL	1.470 + 0.061*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.142	0.140 + 0.001*SL	0.140 + 0.001*SL	0.141 + 0.001*SL
	t_F	0.099	0.098 + 0.001*SL	0.097 + 0.001*SL	0.099 + 0.001*SL
	t_{PLH}	1.747	1.745 + 0.001*SL	1.745 + 0.001*SL	1.746 + 0.001*SL
	t_{PHL}	1.307	1.305 + 0.001*SL	1.306 + 0.001*SL	1.306 + 0.001*SL
E to YN	t_R	0.141	0.140 + 0.001*SL	0.140 + 0.001*SL	0.141 + 0.001*SL
	t_F	0.099	0.098 + 0.001*SL	0.098 + 0.001*SL	0.097 + 0.001*SL
	t_{PLH}	2.133	2.132 + 0.001*SL	2.132 + 0.001*SL	2.133 + 0.001*SL
	t_{PHL}	1.721	1.720 + 0.001*SL	1.720 + 0.001*SL	1.721 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PHSOSCM3_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	2.825	0.802 + 0.040*CL	0.728 + 0.042*CL	1.984 + 0.025*CL
	t_F	2.961	0.982 + 0.040*CL	0.885 + 0.042*CL	0.802 + 0.043*CL
	t_{PLH}	2.697	1.647 + 0.021*CL	1.713 + 0.020*CL	1.757 + 0.019*CL
	t_{PHL}	2.943	1.692 + 0.025*CL	1.746 + 0.024*CL	1.756 + 0.024*CL
E to PADY	t_R	2.625	0.613 + 0.040*CL	0.886 + 0.035*CL	-0.045 + 0.047*CL
	t_F	2.807	0.727 + 0.042*CL	0.578 + 0.045*CL	0.759 + 0.042*CL
	t_{PLH}	2.969	1.910 + 0.021*CL	1.967 + 0.020*CL	2.007 + 0.019*CL
	t_{PHL}	3.597	2.322 + 0.026*CL	2.373 + 0.024*CL	2.394 + 0.024*CL

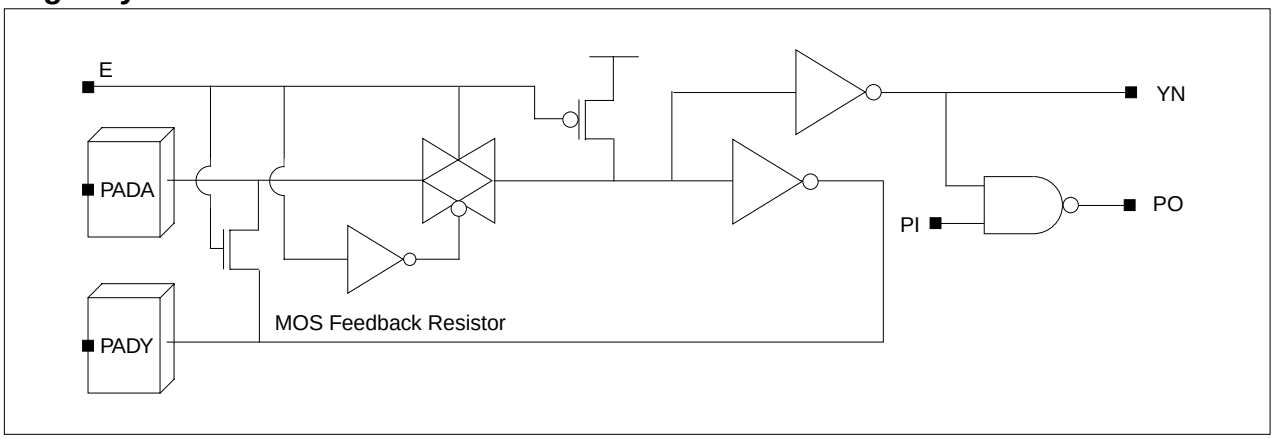
*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.142	0.140 + 0.001*SL	0.140 + 0.001*SL	0.142 + 0.001*SL
	t_F	0.099	0.097 + 0.001*SL	0.097 + 0.001*SL	0.098 + 0.001*SL
	t_{PLH}	2.213	2.211 + 0.001*SL	2.211 + 0.001*SL	2.212 + 0.001*SL
	t_{PHL}	1.871	1.870 + 0.001*SL	1.870 + 0.001*SL	1.871 + 0.001*SL
E to YN	t_R	0.142	0.140 + 0.001*SL	0.141 + 0.001*SL	0.141 + 0.001*SL
	t_F	0.098	0.097 + 0.001*SL	0.097 + 0.001*SL	0.096 + 0.001*SL
	t_{PLH}	2.530	2.529 + 0.001*SL	2.529 + 0.001*SL	2.530 + 0.001*SL
	t_{PHL}	2.519	2.518 + 0.001*SL	2.518 + 0.001*SL	2.519 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)	
PHSOSCK17_LP/K27_LP	*PHSOSCM16_LP/M26_LP/M36_LP*
E	E
3.77	3.77
I/O Sizes	
PHSOSCK17_LP/K27_LP	*PHSOSCM16_LP/M26_LP/M36_LP*
2 I/O Slots	2 I/O Slots

Switching Characteristics

PHSOSCK17_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	1816.000	162.750 + 33.065*CL	163.800 + 33.044*CL	164.100 + 33.040*CL
	t_F	1411.500	144.325 + 25.343*CL	144.700 + 25.336*CL	145.000 + 25.332*CL
	t_{PLH}	871.310	102.060 + 15.385*CL	101.930 + 15.388*CL	101.900 + 15.388*CL
	t_{PHL}	673.950	53.050 + 12.418*CL	52.850 + 12.422*CL	52.700 + 12.424*CL
E to PADY	t_R	1817.600	163.600 + 33.080*CL	165.400 + 33.044*CL	166.300 + 33.032*CL
	t_F	1392.700	139.125 + 25.072*CL	138.900 + 25.076*CL	139.200 + 25.072*CL
	t_{PLH}	876.320	100.370 + 15.519*CL	100.360 + 15.519*CL	100.600 + 15.516*CL
	t_{PHL}	673.910	54.385 + 12.390*CL	54.430 + 12.390*CL	54.400 + 12.390*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.160	0.145 + 0.008*SL	0.145 + 0.007*SL	0.147 + 0.007*SL
	t_F	0.117	0.103 + 0.007*SL	0.103 + 0.007*SL	0.106 + 0.006*SL
	t_{PLH}	35.819	35.805 + 0.007*SL	35.806 + 0.006*SL	35.809 + 0.005*SL
	t_{PHL}	38.796	38.171 + 0.564*SL	38.785 + 0.006*SL	38.788 + 0.005*SL
E to YN	t_R	0.160	0.146 + 0.006*SL	0.144 + 0.008*SL	0.147 + 0.007*SL
	t_F	0.117	0.103 + 0.007*SL	0.105 + 0.006*SL	0.105 + 0.006*SL
	t_{PLH}	36.543	36.529 + 0.007*SL	36.530 + 0.006*SL	36.532 + 0.006*SL
	t_{PHL}	38.477	38.464 + 0.007*SL	38.466 + 0.006*SL	38.469 + 0.005*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 4, *Group3 : 4 < SL

Switching Characteristics

PHSOSCK27_LP

(Typical process, 25°C,1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	228.430	19.530 + 4.178*CL	19.550 + 4.178*CL	19.520 + 4.178*CL
	t_F	239.240	24.365 + 4.298*CL	24.320 + 4.298*CL	24.350 + 4.298*CL
	t_{PLH}	98.650	12.387 + 1.725*CL	12.390 + 1.725*CL	12.390 + 1.725*CL
	t_{PHL}	110.530	9.430 + 2.022*CL	9.410 + 2.022*CL	9.410 + 2.022*CL
E to PADY	t_R	228.310	19.360 + 4.179*CL	19.290 + 4.180*CL	19.320 + 4.180*CL
	t_F	238.410	23.985 + 4.289*CL	23.950 + 4.289*CL	23.950 + 4.289*CL
	t_{PLH}	99.199	12.939 + 1.725*CL	12.917 + 1.726*CL	12.890 + 1.726*CL
	t_{PHL}	110.900	9.815 + 2.022*CL	9.800 + 2.022*CL	9.800 + 2.022*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.148	0.144 + 0.002*SL	0.145 + 0.002*SL	0.145 + 0.002*SL
	t_F	0.106	0.103 + 0.002*SL	0.103 + 0.002*SL	0.106 + 0.001*SL
	t_{PLH}	6.450	6.447 + 0.002*SL	6.447 + 0.002*SL	6.451 + 0.001*SL
	t_{PHL}	6.061	6.058 + 0.002*SL	6.058 + 0.001*SL	6.061 + 0.001*SL
E to YN	t_R	0.148	0.144 + 0.002*SL	0.146 + 0.002*SL	0.145 + 0.002*SL
	t_F	0.106	0.104 + 0.001*SL	0.102 + 0.002*SL	0.106 + 0.001*SL
	t_{PLH}	6.735	6.732 + 0.002*SL	6.733 + 0.002*SL	6.736 + 0.001*SL
	t_{PHL}	6.249	6.246 + 0.002*SL	6.247 + 0.001*SL	6.249 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PHSOSCM16_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	21.410	1.292 + 0.402*CL	1.354 + 0.401*CL	1.234 + 0.403*CL
	t_F	23.850	1.280 + 0.451*CL	1.456 + 0.448*CL	1.426 + 0.448*CL
	t_{PLH}	10.931	1.460 + 0.189*CL	1.463 + 0.189*CL	1.445 + 0.190*CL
	t_{PHL}	13.430	1.501 + 0.239*CL	1.484 + 0.239*CL	1.478 + 0.239*CL
E to PADY	t_R	21.415	1.365 + 0.401*CL	1.303 + 0.402*CL	1.330 + 0.402*CL
	t_F	23.777	1.307 + 0.449*CL	1.437 + 0.447*CL	1.416 + 0.447*CL
	t_{PLH}	11.167	1.696 + 0.189*CL	1.677 + 0.190*CL	1.677 + 0.190*CL
	t_{PHL}	13.752	1.805 + 0.239*CL	1.800 + 0.239*CL	1.800 + 0.239*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.141	0.137 + 0.002*SL	0.138 + 0.002*SL	0.136 + 0.002*SL
	t_F	0.107	0.105 + 0.001*SL	0.103 + 0.002*SL	0.107 + 0.001*SL
	t_{PLH}	1.724	1.721 + 0.002*SL	1.721 + 0.001*SL	1.724 + 0.001*SL
	t_{PHL}	1.139	1.136 + 0.002*SL	1.136 + 0.001*SL	1.139 + 0.001*SL
E to YN	t_R	0.141	0.137 + 0.002*SL	0.138 + 0.002*SL	0.137 + 0.002*SL
	t_F	0.108	0.104 + 0.002*SL	0.105 + 0.002*SL	0.106 + 0.002*SL
	t_{PLH}	2.284	2.281 + 0.002*SL	2.282 + 0.001*SL	2.284 + 0.001*SL
	t_{PHL}	1.691	1.688 + 0.002*SL	1.689 + 0.001*SL	1.691 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PHSOSCM26_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	5.794	0.757 + 0.101*CL	1.247 + 0.091*CL	0.229 + 0.105*CL
	t_F	6.268	0.768 + 0.110*CL	0.621 + 0.113*CL	0.539 + 0.114*CL
	t_{PLH}	3.691	1.321 + 0.047*CL	1.313 + 0.048*CL	1.275 + 0.048*CL
	t_{PHL}	4.268	1.287 + 0.060*CL	1.255 + 0.060*CL	1.234 + 0.061*CL
E to PADY	t_R	5.620	0.312 + 0.106*CL	0.581 + 0.101*CL	0.839 + 0.097*CL
	t_F	6.182	0.421 + 0.115*CL	0.385 + 0.116*CL	0.733 + 0.111*CL
	t_{PLH}	4.045	1.623 + 0.048*CL	1.626 + 0.048*CL	1.680 + 0.048*CL
	t_{PHL}	4.751	1.708 + 0.061*CL	1.707 + 0.061*CL	1.706 + 0.061*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.142	0.140 + 0.001*SL	0.140 + 0.001*SL	0.141 + 0.001*SL
	t_F	0.099	0.098 + 0.001*SL	0.098 + 0.001*SL	0.098 + 0.001*SL
	t_{PLH}	1.763	1.761 + 0.001*SL	1.762 + 0.001*SL	1.763 + 0.001*SL
	t_{PHL}	1.323	1.321 + 0.001*SL	1.322 + 0.001*SL	1.322 + 0.001*SL
E to YN	t_R	0.142	0.140 + 0.001*SL	0.140 + 0.001*SL	0.142 + 0.001*SL
	t_F	0.099	0.098 + 0.001*SL	0.098 + 0.001*SL	0.097 + 0.001*SL
	t_{PLH}	2.332	2.330 + 0.001*SL	2.330 + 0.001*SL	2.331 + 0.001*SL
	t_{PHL}	1.945	1.944 + 0.001*SL	1.944 + 0.001*SL	1.945 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PHSOSCM36_LP

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	2.813	1.050 + 0.035*CL	0.983 + 0.037*CL	0.904 + 0.038*CL
	t_F	2.977	0.990 + 0.040*CL	0.919 + 0.041*CL	0.747 + 0.043*CL
	t_{PLH}	2.726	1.666 + 0.021*CL	1.738 + 0.020*CL	1.782 + 0.019*CL
	t_{PHL}	2.967	1.721 + 0.025*CL	1.766 + 0.024*CL	1.778 + 0.024*CL
E to PADY	t_R	2.627	0.675 + 0.039*CL	0.642 + 0.040*CL	0.536 + 0.041*CL
	t_F	2.819	0.735 + 0.042*CL	0.657 + 0.043*CL	0.520 + 0.045*CL
	t_{PLH}	3.179	2.112 + 0.021*CL	2.174 + 0.020*CL	2.220 + 0.019*CL
	t_{PHL}	3.825	2.546 + 0.026*CL	2.601 + 0.024*CL	2.618 + 0.024*CL

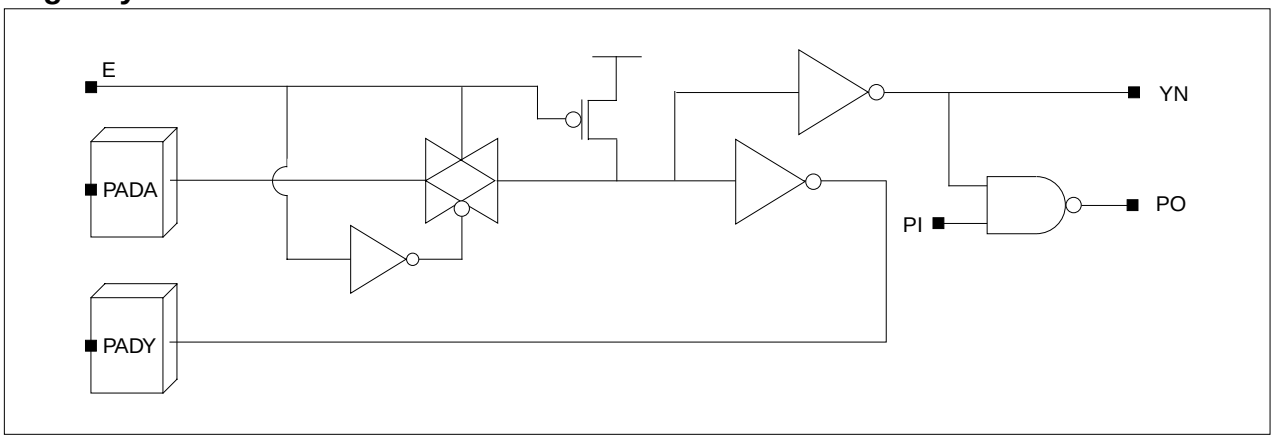
*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 3.3V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.141	0.140 + 0.001*SL	0.140 + 0.001*SL	0.140 + 0.001*SL
	t_F	0.098	0.097 + 0.001*SL	0.097 + 0.001*SL	0.097 + 0.001*SL
	t_{PLH}	2.224	2.222 + 0.001*SL	2.223 + 0.001*SL	2.224 + 0.001*SL
	t_{PHL}	1.886	1.885 + 0.001*SL	1.885 + 0.001*SL	1.886 + 0.001*SL
E to YN	t_R	0.141	0.140 + 0.001*SL	0.140 + 0.001*SL	0.141 + 0.001*SL
	t_F	0.098	0.097 + 0.001*SL	0.096 + 0.001*SL	0.098 + 0.001*SL
	t_{PLH}	2.728	2.726 + 0.001*SL	2.727 + 0.001*SL	2.728 + 0.001*SL
	t_{PHL}	2.747	2.746 + 0.001*SL	2.746 + 0.001*SL	2.747 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)		I/O Sizes	
PMSOSCK1_LP/K2_LP	*PMSOSCM1_LP/M2_LP*	*PMSOSCK1_LP/K2_LP*	*PMSOSCM1_LP/M2_LP*
E	E		
3.77	3.77	2 I/O Slots	2 I/O Slots

Switching Characteristics

PMSOSCK1_LP

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	1688.400	144.400 + 30.880*CL	144.800 + 30.872*CL	144.800 + 30.872*CL
	t_F	1064.800	103.375 + 19.228*CL	103.600 + 19.224*CL	103.300 + 19.228*CL
	t_{PLH}	859.380	100.455 + 15.179*CL	100.540 + 15.177*CL	100.300 + 15.180*CL
	t_{PHL}	534.510	39.535 + 9.899*CL	39.550 + 9.899*CL	39.460 + 9.900*CL
E to PADY	t_R	1688.400	144.650 + 30.875*CL	144.800 + 30.872*CL	144.800 + 30.872*CL
	t_F	1064.800	103.375 + 19.228*CL	103.600 + 19.224*CL	103.300 + 19.228*CL
	t_{PLH}	859.400	100.475 + 15.178*CL	100.400 + 15.180*CL	100.700 + 15.176*CL
	t_{PHL}	534.000	39.025 + 9.899*CL	39.040 + 9.899*CL	38.920 + 9.901*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.140	0.138 + 0.001*SL	0.138 + 0.001*SL	0.139 + 0.001*SL
	t_F	0.100	0.099 + 0.001*SL	0.099 + 0.001*SL	0.098 + 0.001*SL
	t_{PLH}	12.216	12.214 + 0.001*SL	12.215 + 0.001*SL	12.216 + 0.001*SL
	t_{PHL}	12.189	12.187 + 0.001*SL	12.187 + 0.001*SL	12.188 + 0.001*SL
E to YN	t_R	0.139	0.137 + 0.001*SL	0.138 + 0.001*SL	0.138 + 0.001*SL
	t_F	0.100	0.098 + 0.001*SL	0.098 + 0.001*SL	0.100 + 0.001*SL
	t_{PLH}	12.099	12.097 + 0.001*SL	12.097 + 0.001*SL	12.097 + 0.001*SL
	t_{PHL}	11.779	11.777 + 0.001*SL	11.777 + 0.001*SL	11.778 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PMSOSCK2_LP

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	211.590	17.215 + 3.888*CL	17.250 + 3.887*CL	17.220 + 3.887*CL
	t_F	209.890	20.715 + 3.783*CL	20.670 + 3.784*CL	20.700 + 3.784*CL
	t_{PLH}	92.941	11.556 + 1.628*CL	11.543 + 1.628*CL	11.570 + 1.628*CL
	t_{PHL}	96.079	7.637 + 1.769*CL	7.617 + 1.769*CL	7.650 + 1.769*CL
E to PADY	t_R	211.590	17.215 + 3.888*CL	17.250 + 3.887*CL	17.220 + 3.887*CL
	t_F	209.890	20.715 + 3.783*CL	20.690 + 3.784*CL	20.660 + 3.784*CL
	t_{PLH}	92.837	11.454 + 1.628*CL	11.451 + 1.628*CL	11.430 + 1.628*CL
	t_{PHL}	95.658	7.215 + 1.769*CL	7.214 + 1.769*CL	7.190 + 1.769*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.139	0.137 + 0.001*SL	0.138 + 0.001*SL	0.138 + 0.001*SL
	t_F	0.100	0.098 + 0.001*SL	0.098 + 0.001*SL	0.100 + 0.001*SL
	t_{PLH}	7.436	7.434 + 0.001*SL	7.435 + 0.001*SL	7.436 + 0.001*SL
	t_{PHL}	6.542	6.541 + 0.001*SL	6.541 + 0.001*SL	6.542 + 0.001*SL
E to YN	t_R	0.140	0.138 + 0.001*SL	0.137 + 0.001*SL	0.140 + 0.001*SL
	t_F	0.100	0.099 + 0.001*SL	0.099 + 0.001*SL	0.098 + 0.001*SL
	t_{PLH}	7.382	7.380 + 0.001*SL	7.381 + 0.001*SL	7.382 + 0.001*SL
	t_{PHL}	5.982	5.981 + 0.001*SL	5.981 + 0.001*SL	5.982 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PMSOSCM1_LP

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	13.538	0.899 + 0.253*CL	0.460 + 0.262*CL	0.541 + 0.260*CL
	t_F	14.851	0.533 + 0.286*CL	0.697 + 0.283*CL	0.598 + 0.284*CL
	t_{PLH}	7.666	1.421 + 0.125*CL	1.381 + 0.126*CL	1.406 + 0.125*CL
	t_{PHL}	9.070	1.430 + 0.153*CL	1.427 + 0.153*CL	1.425 + 0.153*CL
E to PADY	t_R	13.611	0.682 + 0.259*CL	0.659 + 0.259*CL	0.566 + 0.260*CL
	t_F	14.845	0.446 + 0.288*CL	0.731 + 0.282*CL	0.548 + 0.285*CL
	t_{PLH}	7.698	1.391 + 0.126*CL	1.423 + 0.126*CL	1.431 + 0.125*CL
	t_{PHL}	8.960	1.304 + 0.153*CL	1.312 + 0.153*CL	1.309 + 0.153*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.146	0.145 + 0.001*SL	0.145 + 0.001*SL	0.146 + 0.001*SL
	t_F	0.099	0.097 + 0.001*SL	0.098 + 0.001*SL	0.097 + 0.001*SL
	t_{PLH}	2.193	2.191 + 0.001*SL	2.192 + 0.001*SL	2.193 + 0.001*SL
	t_{PHL}	1.657	1.655 + 0.001*SL	1.656 + 0.001*SL	1.657 + 0.001*SL
E to YN	t_R	0.146	0.144 + 0.001*SL	0.144 + 0.001*SL	0.146 + 0.001*SL
	t_F	0.099	0.097 + 0.001*SL	0.098 + 0.001*SL	0.097 + 0.001*SL
	t_{PLH}	2.349	2.348 + 0.001*SL	2.348 + 0.001*SL	2.349 + 0.001*SL
	t_{PHL}	1.642	1.641 + 0.001*SL	1.641 + 0.001*SL	1.642 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PMSOSCM2_LP

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	4.188	0.517 + 0.073*CL	1.241 + 0.059*CL	1.031 + 0.062*CL
	t_F	4.102	0.782 + 0.066*CL	0.828 + 0.065*CL	0.640 + 0.068*CL
	t_{PLH}	3.689	2.030 + 0.033*CL	2.088 + 0.032*CL	2.140 + 0.031*CL
	t_{PHL}	4.014	2.118 + 0.038*CL	2.150 + 0.037*CL	2.162 + 0.037*CL
E to PADY	t_R	4.106	0.584 + 0.070*CL	1.404 + 0.054*CL	0.403 + 0.067*CL
	t_F	3.996	0.759 + 0.065*CL	0.584 + 0.068*CL	0.341 + 0.071*CL
	t_{PLH}	3.829	2.153 + 0.034*CL	2.223 + 0.032*CL	2.257 + 0.032*CL
	t_{PHL}	4.332	2.431 + 0.038*CL	2.462 + 0.037*CL	2.476 + 0.037*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, 2.5V, t_R/t_F = 3.00ns, SL: Standard Load)

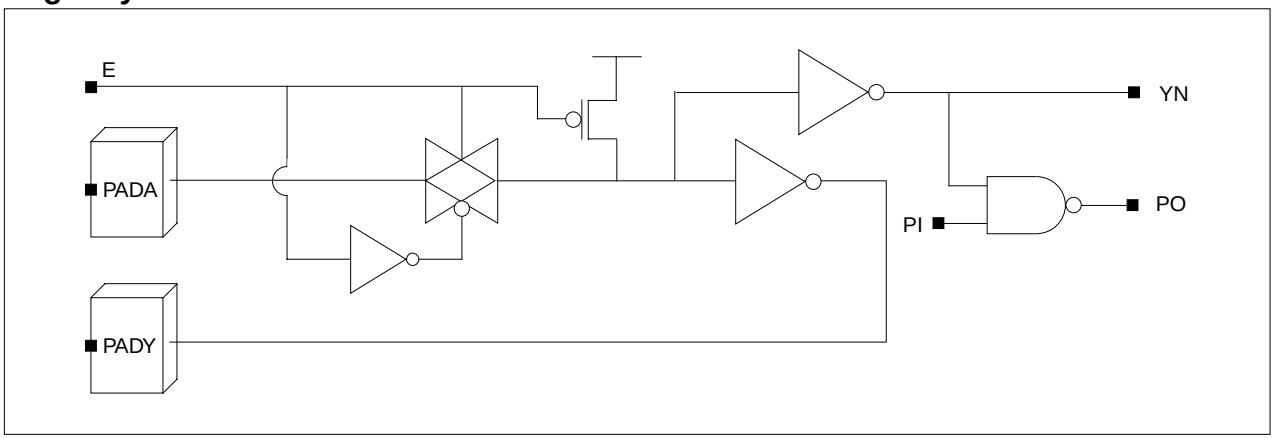
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.146	0.145 + 0.001*SL	0.144 + 0.001*SL	0.146 + 0.001*SL
	t_F	0.099	0.097 + 0.001*SL	0.098 + 0.001*SL	0.096 + 0.001*SL
	t_{PLH}	2.676	2.674 + 0.001*SL	2.674 + 0.001*SL	2.675 + 0.001*SL
	t_{PHL}	2.236	2.235 + 0.001*SL	2.235 + 0.001*SL	2.236 + 0.001*SL
E to YN	t_R	0.146	0.144 + 0.001*SL	0.145 + 0.001*SL	0.145 + 0.001*SL
	t_F	0.098	0.097 + 0.001*SL	0.097 + 0.001*SL	0.098 + 0.001*SL
	t_{PLH}	2.809	2.808 + 0.001*SL	2.808 + 0.001*SL	2.809 + 0.001*SL
	t_{PHL}	2.541	2.540 + 0.001*SL	2.540 + 0.001*SL	2.540 + 0.001*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

PSOSCK1_LP/K2_LP/M1_LP/M2_LP

Oscillator Cell with Enable

Logic Symbol



Truth Table

E	PADA	PADY	YN	PI	PO
0	0	0	0	0	1
0	0	0	0	1	1
0	1	0	0	0	1
0	1	0	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1

Cell Data

Input Load (SL)		I/O Sizes	
PSOSCK1_LP/K2_LP	*PSOSCM1_LP/M2_LP*	*PSOSCK1_LP/K2_LP*	*PSOSCM1_LP/M2_LP*
E	E		
3.75	3.75	2 I/O Slots	2 I/O Slots

Switching Characteristics

PSOSCK1_LP

(Typical process, 25°C, 1.8V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	1163.100	146.575 + 20.330*CL	147.500 + 20.312*CL	147.200 + 20.316*CL
	t_F	1473.200	214.150 + 25.181*CL	212.600 + 25.212*CL	212.000 + 25.220*CL
	t_{PLH}	617.920	111.595 + 10.126*CL	111.980 + 10.119*CL	112.160 + 10.116*CL
	t_{PHL}	707.440	78.740 + 12.574*CL	78.720 + 12.574*CL	78.900 + 12.572*CL
E to PADY	t_R	1163.100	146.575 + 20.330*CL	147.500 + 20.312*CL	147.200 + 20.316*CL
	t_F	1473.100	212.975 + 25.202*CL	212.300 + 25.216*CL	212.000 + 25.220*CL
	t_{PLH}	617.830	111.505 + 10.127*CL	111.890 + 10.119*CL	112.100 + 10.116*CL
	t_{PHL}	703.930	75.255 + 12.573*CL	75.190 + 12.575*CL	75.400 + 12.572*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.107	0.101 + 0.003*SL	0.103 + 0.003*SL	0.102 + 0.003*SL
	t_F	0.101	0.091 + 0.005*SL	0.095 + 0.004*SL	0.083 + 0.005*SL
	t_{PLH}	119.063	119.057 + 0.003*SL	119.062 + 0.002*SL	119.056 + 0.002*SL
	t_{PHL}	127.263	127.257 + 0.003*SL	127.255 + 0.003*SL	127.262 + 0.003*SL
E to YN	t_R	0.107	0.101 + 0.003*SL	0.102 + 0.003*SL	0.101 + 0.003*SL
	t_F	0.101	0.091 + 0.005*SL	0.093 + 0.004*SL	0.088 + 0.005*SL
	t_{PLH}	118.970	118.970 + 0.000*SL	118.959 + 0.003*SL	118.966 + 0.002*SL
	t_{PHL}	120.223	120.217 + 0.003*SL	120.215 + 0.003*SL	120.229 + 0.002*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PSOSCK2_LP

(Typical process, 25°C, 1.8V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	149.960	17.500 + 2.649*CL	17.620 + 2.647*CL	17.740 + 2.645*CL
	t_F	203.440	29.890 + 3.471*CL	29.840 + 3.472*CL	29.900 + 3.471*CL
	t_{PLH}	63.334	12.544 + 1.016*CL	12.872 + 1.009*CL	13.100 + 1.006*CL
	t_{PHL}	91.876	11.876 + 1.600*CL	11.888 + 1.600*CL	11.900 + 1.600*CL
E to PADY	t_R	149.960	17.500 + 2.649*CL	17.620 + 2.647*CL	17.710 + 2.646*CL
	t_F	203.270	29.570 + 3.474*CL	29.590 + 3.474*CL	29.530 + 3.474*CL
	t_{PLH}	62.976	12.186 + 1.016*CL	12.510 + 1.009*CL	12.756 + 1.006*CL
	t_{PHL}	90.441	10.466 + 1.600*CL	10.443 + 1.600*CL	10.470 + 1.600*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.099	0.093 + 0.003*SL	0.094 + 0.003*SL	0.094 + 0.003*SL
	t_F	0.087	0.078 + 0.005*SL	0.079 + 0.004*SL	0.077 + 0.005*SL
	t_{PLH}	29.663	29.657 + 0.003*SL	29.660 + 0.002*SL	29.668 + 0.002*SL
	t_{PHL}	31.635	31.628 + 0.003*SL	31.631 + 0.003*SL	31.634 + 0.003*SL
E to YN	t_R	0.098	0.092 + 0.003*SL	0.093 + 0.003*SL	0.094 + 0.003*SL
	t_F	0.088	0.079 + 0.004*SL	0.079 + 0.004*SL	0.076 + 0.005*SL
	t_{PLH}	29.586	29.581 + 0.003*SL	29.583 + 0.002*SL	29.591 + 0.002*SL
	t_{PHL}	28.671	28.665 + 0.003*SL	28.666 + 0.003*SL	28.669 + 0.003*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Switching Characteristics

PSOSCM1_LP

(Typical process, 25°C, 1.8V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	13.238	1.316 + 0.238*CL	1.212 + 0.241*CL	1.020 + 0.243*CL
	t_F	19.329	1.699 + 0.353*CL	1.579 + 0.355*CL	1.570 + 0.355*CL
	t_{PLH}	7.565	1.789 + 0.116*CL	1.806 + 0.115*CL	1.817 + 0.115*CL
	t_{PHL}	11.527	1.961 + 0.191*CL	1.961 + 0.191*CL	1.961 + 0.191*CL
E to PADY	t_R	13.246	1.269 + 0.240*CL	1.264 + 0.240*CL	0.970 + 0.244*CL
	t_F	19.314	1.714 + 0.352*CL	1.554 + 0.355*CL	1.542 + 0.355*CL
	t_{PLH}	7.337	1.559 + 0.116*CL	1.583 + 0.115*CL	1.574 + 0.115*CL
	t_{PHL}	11.265	1.694 + 0.191*CL	1.699 + 0.191*CL	1.702 + 0.191*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 2.5V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.098	0.093 + 0.003*SL	0.092 + 0.003*SL	0.092 + 0.003*SL
	t_F	0.091	0.082 + 0.005*SL	0.083 + 0.004*SL	0.081 + 0.004*SL
	t_{PLH}	1.371	1.365 + 0.003*SL	1.367 + 0.002*SL	1.376 + 0.002*SL
	t_{PHL}	1.384	1.377 + 0.003*SL	1.379 + 0.003*SL	1.383 + 0.003*SL
E to YN	t_R	0.094	0.089 + 0.003*SL	0.088 + 0.003*SL	0.087 + 0.003*SL
	t_F	0.086	0.077 + 0.005*SL	0.078 + 0.004*SL	0.076 + 0.005*SL
	t_{PLH}	1.355	1.349 + 0.003*SL	1.352 + 0.002*SL	1.359 + 0.002*SL
	t_{PHL}	1.229	1.222 + 0.003*SL	1.224 + 0.003*SL	1.228 + 0.003*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

PSOSCK1_LP/K2_LP/M1_LP/M2_LP

Oscillator Cell with Enable

Switching Characteristics

PSOSCM2_LP

(Typical process, 25°C, 1.8V, t_R/t_F = 3.00ns, CL: Capacitive Load)

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_R	3.718	1.320 + 0.048*CL	0.417 + 0.066*CL	1.741 + 0.048*CL
	t_F	5.129	0.611 + 0.090*CL	0.900 + 0.085*CL	0.296 + 0.093*CL
	t_{PLH}	3.599	2.058 + 0.031*CL	2.117 + 0.030*CL	2.144 + 0.029*CL
	t_{PHL}	4.409	2.010 + 0.048*CL	2.015 + 0.048*CL	2.023 + 0.048*CL
E to PADY	t_R	3.666	1.129 + 0.051*CL	0.335 + 0.067*CL	1.654 + 0.049*CL
	t_F	5.107	0.370 + 0.095*CL	0.698 + 0.088*CL	1.016 + 0.084*CL
	t_{PLH}	3.140	1.600 + 0.031*CL	1.657 + 0.030*CL	1.689 + 0.029*CL
	t_{PHL}	3.999	1.600 + 0.048*CL	1.609 + 0.048*CL	1.600 + 0.048*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

(Typical process, 25°C, 1.8V, t_R/t_F = 3.00ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_R	0.079	0.074 + 0.003*SL	0.074 + 0.003*SL	0.072 + 0.003*SL
	t_F	0.084	0.075 + 0.004*SL	0.074 + 0.005*SL	0.074 + 0.005*SL
	t_{PLH}	1.609	1.604 + 0.002*SL	1.606 + 0.002*SL	1.611 + 0.002*SL
	t_{PHL}	1.675	1.669 + 0.003*SL	1.670 + 0.003*SL	1.673 + 0.003*SL
E to YN	t_R	0.073	0.068 + 0.003*SL	0.068 + 0.003*SL	0.067 + 0.003*SL
	t_F	0.079	0.071 + 0.004*SL	0.070 + 0.005*SL	0.070 + 0.005*SL
	t_{PLH}	1.235	1.231 + 0.002*SL	1.232 + 0.002*SL	1.237 + 0.002*SL
	t_{PHL}	1.366	1.360 + 0.003*SL	1.361 + 0.003*SL	1.364 + 0.003*SL

*Group1 : SL < 5, *Group2 : 5 ≦ SL ≦ 16, *Group3 : 16 < SL

Overview

PCI buffers are designed for PCI local bus application which is intended for high-performance 32-bit or 64-bit bus architecture.

Samsung supports PCI input, output and bi-directional buffers for 3.3V and 5V signaling environment.

Features

— Low-power, high performance CMOS technology
— Input, output, and bi-directional PCI buffers
— Operating at up to 66MHz, including 33MHz
— Electrically compliant interface in 3.3V and 5V bus environments

Description

These PCI buffers are designed for 3.3V and 5V environments. These buffers are compliant with PCI local bus specification rev2.1. The PCI buffers for 66MHz can be available in 33MHz interface, but require more power pads due to their fast and noisy characteristics. The 5V tolerant PCI buffers can be used for 33MHz, 5V environment. These tolerant PCI buffers require 5V power for bulk of PMOS driver for 5V environment or 3.3V power for 3.3V environment. The 5V tolerant PCI drivers support 5V environment while EN5V is low. Although tolerant PCI buffers support 5V environment, they do not drive 5V.

NOTE: If you want to use PCI buffers, please contact Samsung.

Cell List

3.3V Signaling PCI I/Os

Cell Name	Description	Operating Frequency	VIO(note2) Voltage	Operating Voltage
PTBPCI3_LP	Bi-direction	Up to 66MHz at 3.3V signaling(note1)	3.3V	3.3V
PTOPCI3_LP	Driver	Up to 66MHz at 3.3V signaling		
PTIPCI3_LP	Receiver	Up to 66MHz at 3.3V signaling		

5V Signaling PCI I/Os

Cell Name	Description	Operating Frequency	VIO(note2) Voltage	Operating Voltage
PTBPCI5_LP	Bi-direction	Up to 33MHz at 5V signaling(note1)	5V	3.3V
PTOPCI5_LP	Driver	Up to 33MHz at 5V signaling		
PTIPCI5_LP	Receiver	Up to 33MHz at 5V signaling		

NOTE1: 3.3V signaling conditions: EN5V=high, VIO=3.3V, In this case 5V tolerant is not supported.
5V signaling conditions: EN5V=low, VIO=5V, and 5V tolerant is supported.
NOTE2: In 3.3V signaling, the voltage of VIO is 3.3V, which is provided through the VDD5O_PCI_LP power cell.
In 5V signaling, the voltage of VIO is 5V, which is provided through the VDD5O_PCI_LP power cell.

PCI BUFFERS

Power Cell Name	Description
VDD1IH_PCI_LP	1.8V Power cell for internal core and PCI I/Os
VDD3OP_PCI_LP	3.3V Power cell for PCI I/Os
VDD5O_PCI_LP	VIO(3.3V or 5V) Power cell for PCI I/Os(note2)
VSS3I_PCI_LP	Gnd Power cell for internal core; not used for PCI I/Os
VSS3OP_PCI_LP	Gnd Power cell for PCI I/Os

Option (note3)

Cell Name	Description
VDET_L131PCI_LP	3.3V or 5V voltage detector

NOTE3: Voltage detector circuit will automatically set the EN5V pin either high or low according to VIO voltage level.

Electrical Characteristics

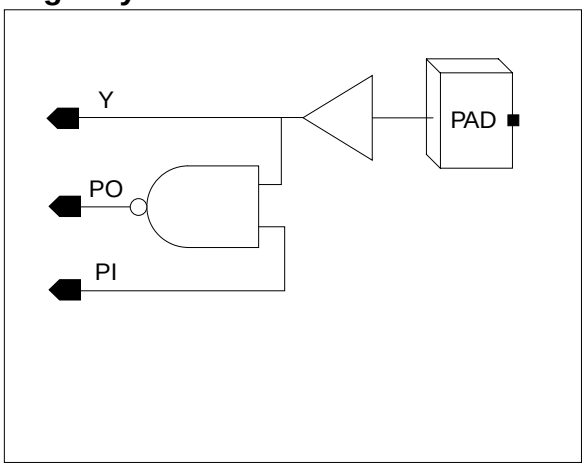
DC Characteristics

Symbol	Parameter	3.3V Signaling			5V Signaling			Unit
		Condition	Min	Max	Condition	Min	Max	
V_{CC}	Supply voltage		3.0	3.6		3.0	3.6	V
VIO	VIO voltage		V_{CC}			4.75	5.25	V
V_{ih}	Input high voltage		$0.47V_{CC}$	V_{CC}+0.5		1.9	VIO+0.5	V
V_{il}	Input low voltage		–0.5	$0.33V_{CC}$		–0.5	0.9	V
I_i	Input leakage current	$0 < V_{IN} < V_{CC}$	–10	10	$0 < V_{IN} < VIO$	–70	70	µA
V_{oh}	Output high voltage	I_{OUT} = –500µA	$0.9V_{CC}$	–	I_{OUT} = –2mA	2.4	–	V
V_{ol}	Output low voltage	I_{OUT} = 1500µA	–	$0.1V_{CC}$	I_{OUT} = 6mA	–	0.55	V

AC Characteristics

Symbol	Parameter	3.3V Signaling (66MHz)			5V Signaling (33MHz)			Unit
		Condition	Min	Max	Condition	Min	Max	
$I_{oh\ (AC)}$	Switching current high	$V_{OUT} = 0.3V_{CC}$	$–12V_{CC}$		V_{OUT} = 1.4V	–44		mA
		$V_{OUT} = 0.7V_{CC}$		$–32V_{CC}$	V_{OUT} = 2.4V	–2.33		
		$V_{OUT} = 0.9V_{CC}$	$–1.71V_{CC}$		V_{OUT} = 3.0V		–142	
$I_{ol\ (AC)}$	Switching current low	$V_{OUT} = 0.6V_{CC}$	$16V_{CC}$		V_{OUT} = 2.2V	95		mA
		$V_{OUT} = 0.1V_{CC}$	$2.67V_{CC}$		V_{OUT} = 0.55V	23.9		
		$V_{OUT} = 0.18V_{CC}$		$38V_{CC}$	V_{OUT} = 0.71V		206	
I_{cl}	Low clamp current	$–3 < V_{IN} \leq –1$	$–25 + (V_{IN}+1)/0.015$		$–5 < V_{IN} \leq –1$	$–25 + (V_{IN}+1)/0.015$		mA
I_{ch}	High clamp current	$V_{CC}+1 \leq V_{IN} < V_{CC}+4$	$25+(V_{IN}–V_{CC}–1)/0.015$					mA
T_r	Output rise time	$0.3V_{CC}$ to $0.6V_{CC}$	1.0	4.0	0.4V to 2.4V	1.0	5.0	V/ns
T_f	Output fall time	$0.6V_{CC}$ to $0.3V_{CC}$	1.0	4.0	2.4V to 0.4V	1.0	5.0	V/ns

Logic Symbol



Truth Table

Input Truth Table			
PAD	**PI**	**Y**	**PO**
1	1	1	0
0	x	0	1
1	0	1	1

Switching Characteristics

(Typical process, 25°C, 1.8V, 3.3V t_R/t_F = 3.00ns, SL: Standard Load)

PTIPCI3_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.263	0.243 + 0.010*SL	0.243 + 0.010*SL	0.242 + 0.010*SL
	t_F	0.107	0.099 + 0.004*SL	0.099 + 0.004*SL	0.110 + 0.003*SL
	t_{PLH}	0.685	0.676 + 0.005*SL	0.676 + 0.004*SL	0.683 + 0.004*SL
	t_{PHL}	0.539	0.529 + 0.006*SL	0.531 + 0.004*SL	0.551 + 0.003*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 15, *Group3 : 15 < SL

PTIPCI5_LP

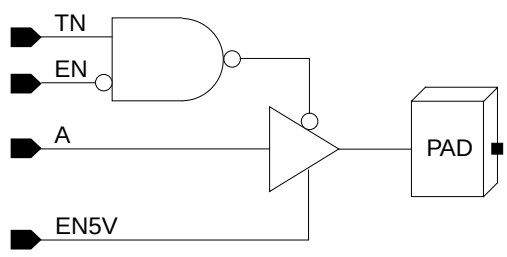
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.254	0.235 + 0.009*SL	0.235 + 0.009*SL	0.236 + 0.009*SL
	t_F	0.092	0.084 + 0.004*SL	0.085 + 0.004*SL	0.091 + 0.003*SL
	t_{PLH}	0.548	0.541 + 0.004*SL	0.541 + 0.004*SL	0.548 + 0.003*SL
	t_{PHL}	0.554	0.546 + 0.005*SL	0.547 + 0.003*SL	0.564 + 0.002*SL

*Group1 : SL < 1, *Group2 : 1 ≦ SL ≦ 15, *Group3 : 15 < SL

PTOPCI_LP

5V-tolerant PCI Output Buffers

Logic Symbol



NOTE:
EN5V=Low: Enable the 5V signaling
EN5V=High: Enable the 3.3V signaling

Truth Table

Output Truth Table			
A	**EN**	**TN**	**PAD**
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	HI-Z

Switching Characteristics

(Typical process, 25°C, 1.8V, 3.3V t_R/t_F = 0.17ns, CL: Capacitive Load)

PTOPCI3_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.436	0.433 + 0.023*CL	0.624 + 0.016*CL	0.714 + 0.014*CL
	t_F	1.519	0.447 + 0.020*CL	0.351 + 0.023*CL	0.284 + 0.025*CL
	t_{PLH}	2.032	1.038 + 0.022*CL	1.233 + 0.016*CL	1.384 + 0.013*CL
	t_{PHL}	2.844	1.307 + 0.032*CL	1.420 + 0.028*CL	1.494 + 0.027*CL
TN to PAD	t_R	1.436	0.435 + 0.023*CL	0.626 + 0.016*CL	0.715 + 0.014*CL
	t_F	1.501	0.375 + 0.022*CL	0.301 + 0.024*CL	0.253 + 0.025*CL
	t_{PLH}	2.208	1.212 + 0.023*CL	1.408 + 0.016*CL	1.560 + 0.013*CL
	t_{PHL}	2.959	1.381 + 0.033*CL	1.523 + 0.029*CL	1.603 + 0.027*CL
	t_{PLZ}	0.779	0.779 + 0.000*CL	0.779 + 0.000*CL	0.779 + 0.000*CL
	t_{PHZ}	0.947	0.946 + 0.000*CL	0.946 + 0.000*CL	0.947 + 0.000*CL
EN to PAD	t_R	1.436	0.435 + 0.023*CL	0.626 + 0.016*CL	0.715 + 0.014*CL
	t_F	1.501	0.375 + 0.022*CL	0.301 + 0.024*CL	0.253 + 0.025*CL
	t_{PLH}	2.279	1.283 + 0.023*CL	1.480 + 0.016*CL	1.631 + 0.013*CL
	t_{PHL}	3.030	1.453 + 0.033*CL	1.595 + 0.029*CL	1.674 + 0.027*CL
	t_{PLZ}	0.783	0.783 + 0.000*CL	0.783 + 0.000*CL	0.783 + 0.000*CL
	t_{PHZ}	0.951	0.949 + 0.000*CL	0.949 + 0.000*CL	0.950 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

Switching Characteristics (Typical process, 25°C, 1.8V, 3.3V t_R/t_F = 0.17ns, CL: Capacitive Load)

PTOPCI5_LP

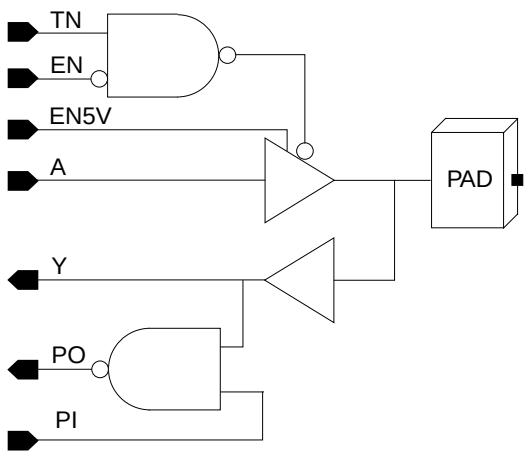
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.243	0.460 + 0.017*CL	0.584 + 0.013*CL	0.632 + 0.012*CL
	t_F	0.978	0.380 + 0.011*CL	0.331 + 0.013*CL	0.281 + 0.014*CL
	t_{PLH}	2.064	1.249 + 0.018*CL	1.400 + 0.013*CL	1.513 + 0.011*CL
	t_{PHL}	2.378	1.267 + 0.024*CL	1.417 + 0.019*CL	1.523 + 0.017*CL
TN to PAD	t_R	1.252	0.515 + 0.016*CL	0.619 + 0.013*CL	0.650 + 0.012*CL
	t_F	0.965	0.340 + 0.012*CL	0.294 + 0.013*CL	0.261 + 0.014*CL
	t_{PLH}	2.234	1.373 + 0.020*CL	1.557 + 0.014*CL	1.679 + 0.011*CL
	t_{PHL}	2.497	1.298 + 0.027*CL	1.502 + 0.020*CL	1.627 + 0.017*CL
	t_{PLZ}	0.783	0.783 + 0.000*CL	0.783 + 0.000*CL	0.783 + 0.000*CL
	t_{PHZ}	0.950	0.947 + 0.000*CL	0.948 + 0.000*CL	0.949 + 0.000*CL
EN to PAD	t_R	1.252	0.515 + 0.016*CL	0.619 + 0.013*CL	0.650 + 0.012*CL
	t_F	0.965	0.340 + 0.012*CL	0.294 + 0.013*CL	0.261 + 0.014*CL
	t_{PLH}	2.305	1.445 + 0.020*CL	1.628 + 0.014*CL	1.751 + 0.011*CL
	t_{PHL}	2.568	1.370 + 0.027*CL	1.574 + 0.020*CL	1.698 + 0.017*CL
	t_{PLZ}	0.787	0.787 + 0.000*CL	0.787 + 0.000*CL	0.787 + 0.000*CL
	t_{PHZ}	0.953	0.951 + 0.000*CL	0.951 + 0.000*CL	0.952 + 0.000*CL

*Group1 : CL < 30, *Group2 : 30 ≦ CL ≦ 50, *Group3 : 50 < CL

PTBPCI_LP

5V-Tolerant PCI Bidirectional Buffer

Logic Symbol



NOTE:
EN5V=Low: Enable the 5V signaling
EN5V=High: Enable the 3.3V signaling

Truth Table

Input Truth Table

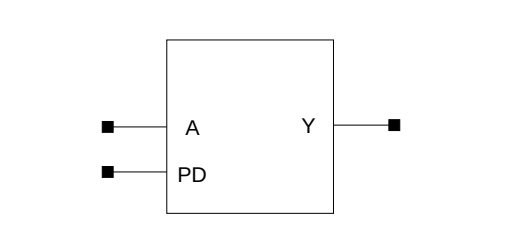
PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

Option:

Logic Symbol



Truth Table

Input		Output
A	PD	Y
3.3V	↗	1
5V	↗	0
X	0	Last Y
X	1	Last Y

Cell Data

Cell Name	Detecting Voltage
vdet_l131pci_lp	3.3V, 5V

Cell List

Cell Type		Cell Name	Supply Voltage	Description
Power	1.8V Interface Digital I/O	VDD1I_LP	1.8V	1.8V Internal
		VDD1P_LP	1.8V	1.8V Pre-Driver
		VDD1O_LP	1.8V	1.8V Output-Driver
		VDD1IP_LP	1.8V	1.8V Internal and Pre-Driver
		VDD1OP_LP	1.8V	1.8V Output-Driver and Pre-Driver
		VDD1T_LP	1.8V	1.8V Total
	2.5V Interface Digital I/O	VDD1IM_LP	1.8V	1.8V Internal for 2.5V Interface I/O
		VDD2P_LP	2.5V	2.5V Pre-Driver
		VDD2O_LP	2.5V	2.5V Output-Driver
		VDD2OP_LP	2.5V	2.5V Output-Driver and Pre-Driver
	3.3V Interface Digital I/O	VDD1IH_LP	1.8V	1.8V Internal for 3.3V Interface I/O
		VDD3P_LP	3.3V	3.3V Pre-Driver
		VDD3O_LP	3.3V	3.3V Output-Driver
		VDD3OP_LP	3.3V	3.3V Output-Driver and Pre-Driver
Ground	1.8V Interface Digital I/O	VSS1I_LP		Internal GND for 1.8V Interface I/O
		VSS1P_LP		Pre-Driver GND for 1.8V Interface I/O
		VSS1O_LP		Output-Driver GND for 1.8V Interface I/O
		VSS1IP_LP		Internal and Pre-Driver GND for 1.8V Interface I/O
		VSS1OP_LP		Output-Driver and Pre-Driver GND for 1.8V Interface I/O
		VSS1T_LP		Total GND for 1.8V Interface I/O
	2.5V Interface Digital I/O	VSS2I_LP		Internal GND for 2.5V Interface I/O
		VSS2P_LP		Pre-Driver GND for 2.5V Interface I/O
		VSS2O_LP		Output-Driver GND for 2.5V Interface I/O
		VSS2IP_LP		Internal and Pre-Driver GND for 2.5V Interface I/O
		VSS2OP_LP		Output-Driver and Pre-Driver GND for 2.5V Interface I/O
		VSS2T_LP		Total GND for 2.5V Interface I/O
	3.3V Interface Digital I/O	VSS3I_LP		Internal GND for 3.3V Interface I/O
		VSS3P_LP		Pre-Driver GND for 3.3V Interface I/O
		VSS3O_LP		Output-Driver GND for 3.3V Interface I/O
		VSS3IP_LP		Internal and Pre-Driver GND for 3.3V Interface I/O
		VSS3OP_LP		Output-Driver and Pre-Driver GND for 3.3V Interface I/O
		VSS3T_LP		Total GND for 3.3V Interface I/O

Cell List (Continued)

Cell Type		Cell Name	Supply Voltage	Description
Power	1.8V Interface Analog I/O	VDD1I_ABB_LP	1.8V	1.8V Internal
		VDD1OP_ABB_LP	1.8V	1.8V Output-Driver and Pre-Driver
		VDD1T_ABB_LP	1.8V	1.8V Total
	2.5V Interface Analog I/O	VDD1IM_ABB_LP	1.8V	1.8V Internal for 2.5V Interface I/O
		VDD2I_ABB_LP	2.5V	2.5V Internal
		VDD2OP_ABB_LP	2.5V	2.5V Output-Driver and Pre-Driver
		VDD2T_ABB_LP	2.5V	2.5V Total
	3.3V Interface Analog I/O	VDD1IH_ABB_LP	1.8V	1.8V Internal for 3.3V Interface I/O
		VDD3I_ABB_LP	3.3V	3.3V Internal
		VDD3OP_ABB_LP	3.3V	3.3V Output-Driver and Pre-Driver
		VDD3T_ABB_LP	3.3V	3.3V Total
Ground	1.8V Interface Analog I/O	VSS1I_ABB_LP		Internal GND for 1.8V Interface I/O
		VSS1OP_ABB_LP		Output-Driver and Pre-Driver GND for 1.8V Interface I/O
		VSS1T_ABB_LP		Total GND for 1.8V Interface I/O
		VBB1_ABB_LP		Bulk-Bias GND for 1.8V Interface I/O
		VSS1BB_ABB_LP		Ground with VBB Ring Connected GND for 1.8V Interface I/O
	2.5V Interface Analog I/O	VSS2I_ABB_LP		Internal GND for 2.5V Interface I/O
		VSS2OP_ABB_LP		Output-Driver and Pre-Driver GND for 2.5V Interface I/O
		VSS2T_ABB_LP		Total GND for 2.5V Interface I/O
		VBB2_ABB_LP		Bulk-Bias GND for 2.5V Interface I/O
		VSS2BB_ABB_LP		Ground with VBB Ring Connected GND for 2.5V Interface I/O
	3.3V Interface Analog I/O	VSS3I_ABB_LP		Internal GND for 3.3V Interface I/O
		VSS3OP_ABB_LP		Output-Driver and Pre-Driver GND for 3.3V Interface I/O
		VSS3T_ABB_LP		Total GND for 3.3V Interface I/O
		VBB3_ABB_LP		Bulk-Bias GND for 3.3V Interface I/O
		VSS3BB_ABB_LP		Ground with VBB Ring Connected GND for 3.3V Interface I/O

Analog Input

Cell Name	Function Description
PIA_ABB_LP	Analog Normal Input Pad for 1.8V Interface with Separate Bulk Bias
PIAR10_ABB_LP	Analog Normal Input Pad for 1.8V Interface with Resistor 10ohm and Separate Bulk Bias
PIAR50_ABB_LP	Analog Normal Input Pad for 1.8V Interface with Resistor 50ohm and Separate Bulk Bias
PNC_ABB_LP	Analog No Connection Pad for 1.8V Interface with Separate Bulk Bias
PIC_ABB_LP	Analog CMOS Level Input Buffer for 1.8V Interface with Separate Bulk-Bias
PICC_ABB_LP	Analog CMOS Level Input Buffer for 1.8V Interface with Separate Bulk-Bias and without Nand-Tree
PICD_ABB_LP	Analog CMOS Level Input Buffer for 1.8V Interface with Pull-Down and Separate Bulk-Bias
PICEN_ABB_LP	Analog CMOS Level Input Buffer for 1.8V Interface with Enable Port and Separate Bulk-Bias
PICU_ABB_LP	Analog CMOS Level Input Buffer for 1.8V Interface with Pull-Up and Separate Bulk-Bias
PIS_ABB_LP	Analog CMOS Schmitt Trigger Level Input Buffer for 1.8V Interface with Separate Bulk Bias
PISD_ABB_LP	Analog CMOS Schmitt Trigger Level Input Buffer for 1.8V Interface with Pull-Down and Separate Bulk Bias
PISU_ABB_LP	Analog CMOS Schmitt Trigger Level Input Buffer for 1.8V Interface with Pull-Up and Separate Bulk Bias
PMIA_ABB_LP	Analog Normal Input Pad for 2.5V Interface with Separate Bulk Bias
PMIAR10_ABB_LP	Analog Normal Input Pad for 2.5V Interface with Resistor 10ohm and Separate Bulk Bias
PMIAR50_ABB_LP	Analog Normal Input Pad for 2.5V Interface with Resistor 50ohm and Separate Bulk Bias
PMNC_ABB_LP	Analog No Connection Pad for 2.5V Interface with Separate Bulk Bias
PMIC_ABB_LP	Analog CMOS Level Input Buffer for 2.5V Interface with Separate Bulk Bias
PMICC_ABB_LP	Analog CMOS Level Input Buffer for 2.5V Interface with Separate Bulk Bias and without Nand-Tree
PMICD_ABB_LP	Analog CMOS Level Input Buffer for 2.5V Interface with Pull-Down and Separate Bulk Bias
PMICEN_ABB_LP	Analog CMOS Level Input Buffer for 2.5V Interface with Enable Port and Separate Bulk Bias
PMICU_ABB_LP	Analog CMOS Level Input Buffer for 2.5V Interface with Pull-Up and Separate Bulk Bias
PMIS_ABB_LP	Analog CMOS Schmitt Trigger Level Input Buffer for 2.5V Interface with Separate Bulk Bias
PMISD_ABB_LP	Analog CMOS Schmitt Trigger Level Input Buffer for 2.5V Interface with Pull-Down and Separate Bulk Bias
PMISU_ABB_LP	Analog CMOS Schmitt Trigger Level Input Buffer for 2.5V Interface with Pull-Up and Separate Bulk Bias
PHIA_ABB_LP	Analog Normal Input Pad for 3.3V Interface with Separate Bulk Bias
PHIAR10_ABB_LP	Analog Normal Input Pad for 3.3V Interface with Resistor 10ohm and Separate Bulk Bias
PHIAR50_ABB_LP	Analog Normal Input Pad for 3.3V Interface with Resistor 50ohm and Separate Bulk Bias
PHNC_ABB_LP	Analog No Connection Pad for 3.3V Interface with Separate Bulk Bias
PHIC_ABB_LP	Analog LVCMOS Level Input Buffer for 3.3V Interface with Separate Bulk-Bias
PHICC_ABB_LP	Analog LVCMOS Level Input Buffer for 3.3V Interface with Separate Bulk-Bias and without Nand-Tree
PHICD_ABB_LP	Analog LVCMOS Level Input Buffer for 3.3V Interface with Pull-Down and Separate Bulk-Bias
PHICEN_ABB_LP	Analog LVCMOS Level Input Buffer for 3.3V Interface with Enable Port and Separate Bulk-Bias
PHICU_ABB_LP	Analog LVCMOS Level Input Buffer for 3.3V Interface with Pull-Up and Separate Bulk-Biasa
PHIS_ABB_LP	Analog LVCMOS Schmitt Trigger Level Input Buffer for 3.3V Interface with Separated Bulk Bias
PHISD_ABB_LP	Analog LVCMOS Schmitt Trigger Level Input Buffer for 3.3V Interface with Pull-Down and Separate Bulk Bias
PHISU_ABB_LP	Analog LVCMOS Schmitt Trigger Level Input Buffer for 3.3V Interface with Pull-Up and Separate Bulk Bias

NOTE: As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.

ANALOG INTERFACE

Analog Output

Cell Name	Function Description
POA_ABB_LP	Analog Normal Output Pad for 1.8V Interface with Separate Bulk Bias
POAR10_ABB_LP	Analog Normal Output Pad for 1.8V Interface with Resistor 10ohm and Separate Bulk Bias
POAR50_ABB_LP	Analog Normal Output Pad for 1.8V Interface with Resistor 50ohm and Separate Bulk Bias
POB1/2/8_ABB_LP	Analog Normal Output Buffer for 1.8V Interface with Separate Bulk Bias, 1/2/8mA Drive
POT1/2/4/6/8/10/12/16_ABB_LP	Analog Tri-State Output Buffer for 1.8V Interface with Separate Bulk Bias, 1/2/4/6/8/10/12/16mA Drive
PMOA_ABB_LP	Analog Normal Output Pad for 2.5V Interface with Separate Bulk Bias
PMOAR10_ABB_LP	Analog Normal Output Pad for 2.5V Interface with Resistor 10ohm and Separate Bulk Bias
PMOAR50_ABB_LP	Analog Normal Output Pad for 2.5V Interface with Resistor 50ohm and Separate Bulk Bias
PMOB1/2/8_ABB_LP	Analog Normal Output Buffer for 2.5V Interface with Separate Bulk Bias, 1/2/8mA Drive
PMOT1/2/4/6/8/10/12/16_ABB_LP	Analog Tri-State Output Buffer for 2.5V Interface with Separate Bulk Bias, 1/2/4/6/8/10/12/16mA Drive
PHOA_ABB_LP	Analog Normal Output Pad for 3.3V Interface with Separate Bulk Bias
PHOAR10_ABB_LP	Analog Normal Output Pad for 3.3V Interface with Resistor 10ohm and Separate Bulk Bias
PHOAR50_ABB_LP	Analog Normal Output Pad for 3.3V Interface with Resistor 50ohm and Separate Bulk Bias
PHOB1/2/8_ABB_LP	Analog Normal Output Buffer for 3.3V Interface with Separate Bulk Bias, 1/2/8mA Drive
PHOT1/2/4/6/8/10/12/16_ABB_LP	Analog Tri-State Output Buffer for 3.3V Interface with Separate Bulk Bias, 1/2/4/6/8/10/12/16mA Drive
PHOD4SM_ABB_LP	Analog Open-Drain Output Buffer for 3.3V Interface with Separated Bulk Bias, 4mA Drive

Analog Bi-Direction

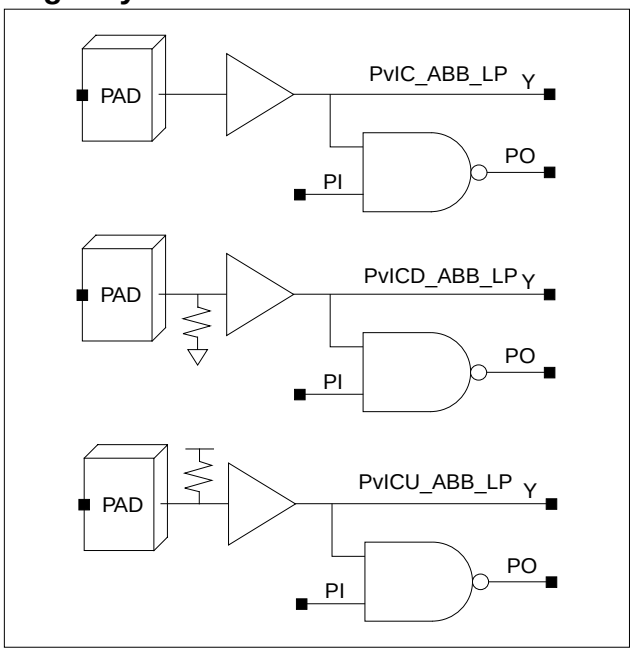
Cell Name	Function Description
PBCT1/2/4/6_ABB_LP	Analog Bi-Directional Buffer for 1.8V Interface with CMOS Level Input, Tri-State Output Pad with Separate Bulk Bias, 1/2/4/6mA Drive
PMBCT1/2/4/6_ABB_LP	Analog Bi-Directional Buffer for 2.5V Interface with CMOS Level Input, Tri-State Output Pad with Separate Bulk Bias, 1/2/4/6mA Drive
PHBCT1/2/4/6_ABB_LP	Analog Bi-Directional Buffer for 3.3V Interface with CMOS Level Input, Tri-State Output Pad with Separate Bulk Bias, 1/2/4/6mA Drive
PHBSD4SM_ABB_LP	Analog Bi-Directional Buffer for 3.3V Interface with CMOS Schmitt Trigger Lever Input, Open-Drain Output Pad with Separated Bulk Bias, 4mA Drive

NOTE: As to analog IO cells in the library, the voltage level of the input/output signal is the same as the IO power supply voltage level, no level shifter inside.

Cell Availability

1.8V Only	2.5V Interface	3.3V Interface
PIC_ABB_LP PICD_ABB_LP PICU_ABB_LP	PMIC_ABB_LP PMICD_ABB_LP PMICU_ABB_LP	PHIC_ABB_LP PHICD_ABB_LP PHICU_ABB_LP

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PIC_ABB_LP/PICD_ABB_LP/PICU_ABB_LP	3.79
PMIC_ABB_LP/PMICD_ABB_LP/PMICU_ABB_LP	2.13
PHIC_ABB_LP/PHICD_ABB_LP/PHICU_ABB_LP	2.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PIC_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.120	0.112 + 0.004*SL	0.112 + 0.004*SL	0.110 + 0.004*SL
	t_F	0.106	0.098 + 0.004*SL	0.098 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.388	0.380 + 0.004*SL	0.385 + 0.003*SL	0.402 + 0.002*SL
	t_{PHL}	0.383	0.375 + 0.004*SL	0.379 + 0.003*SL	0.393 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PICD_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.119	0.111 + 0.004*SL	0.111 + 0.004*SL	0.109 + 0.004*SL
	t_F	0.107	0.098 + 0.004*SL	0.100 + 0.004*SL	0.091 + 0.004*SL
	t_{PLH}	0.412	0.404 + 0.004*SL	0.409 + 0.003*SL	0.426 + 0.002*SL
	t_{PHL}	0.377	0.369 + 0.004*SL	0.373 + 0.003*SL	0.387 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PICU_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.120	0.111 + 0.004*SL	0.114 + 0.004*SL	0.109 + 0.004*SL
	t_F	0.105	0.097 + 0.004*SL	0.098 + 0.004*SL	0.090 + 0.004*SL
	t_{PLH}	0.378	0.370 + 0.004*SL	0.374 + 0.003*SL	0.392 + 0.002*SL
	t_{PHL}	0.400	0.391 + 0.004*SL	0.396 + 0.003*SL	0.410 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMIC_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.142	0.128 + 0.007*SL	0.133 + 0.006*SL	0.127 + 0.006*SL
	t_F	0.122	0.109 + 0.006*SL	0.112 + 0.006*SL	0.111 + 0.006*SL
	t_{PLH}	0.428	0.417 + 0.006*SL	0.424 + 0.004*SL	0.446 + 0.003*SL
	t_{PHL}	0.453	0.442 + 0.006*SL	0.448 + 0.004*SL	0.470 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PMICD_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.141	0.128 + 0.007*SL	0.132 + 0.006*SL	0.126 + 0.006*SL
	t_F	0.124	0.110 + 0.007*SL	0.115 + 0.005*SL	0.113 + 0.006*SL
	t_{PLH}	0.444	0.433 + 0.006*SL	0.440 + 0.004*SL	0.462 + 0.003*SL
	t_{PHL}	0.450	0.438 + 0.006*SL	0.444 + 0.004*SL	0.467 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PMICU_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.143	0.130 + 0.006*SL	0.133 + 0.006*SL	0.127 + 0.006*SL
	t_F	0.121	0.108 + 0.007*SL	0.113 + 0.005*SL	0.110 + 0.006*SL
	t_{PLH}	0.420	0.409 + 0.006*SL	0.416 + 0.004*SL	0.438 + 0.003*SL
	t_{PHL}	0.468	0.456 + 0.006*SL	0.463 + 0.004*SL	0.484 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHIC_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.118	0.108 + 0.005*SL	0.110 + 0.004*SL	0.104 + 0.005*SL
	t_F	0.109	0.099 + 0.005*SL	0.100 + 0.005*SL	0.102 + 0.005*SL
	t_{PLH}	0.174	0.166 + 0.004*SL	0.171 + 0.003*SL	0.185 + 0.002*SL
	t_{PHL}	0.495	0.486 + 0.004*SL	0.490 + 0.003*SL	0.506 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHICD_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.116	0.106 + 0.005*SL	0.109 + 0.004*SL	0.102 + 0.005*SL
	t_F	0.112	0.101 + 0.005*SL	0.104 + 0.005*SL	0.103 + 0.005*SL
	t_{PLH}	0.198	0.190 + 0.004*SL	0.194 + 0.003*SL	0.208 + 0.002*SL
	t_{PHL}	0.504	0.495 + 0.004*SL	0.499 + 0.003*SL	0.516 + 0.003*SL

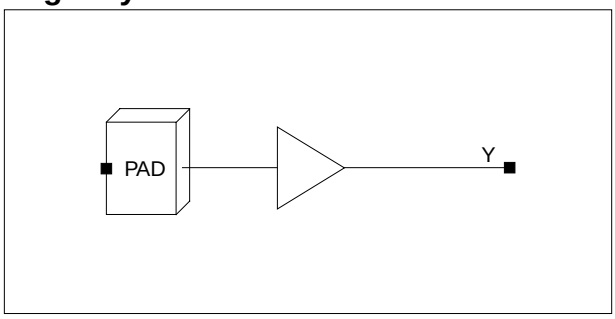
*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHICU_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.120	0.110 + 0.005*SL	0.112 + 0.004*SL	0.106 + 0.005*SL
	t_F	0.110	0.100 + 0.005*SL	0.101 + 0.005*SL	0.102 + 0.005*SL
	t_{PLH}	0.165	0.157 + 0.004*SL	0.162 + 0.003*SL	0.176 + 0.002*SL
	t_{PHL}	0.510	0.501 + 0.004*SL	0.505 + 0.003*SL	0.521 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Logic Symbol



Truth Table

PAD	Y
0	0
1	1

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PICC_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.105	0.096 + 0.005*SL	0.099 + 0.004*SL	0.092 + 0.004*SL
	t_F	0.091	0.082 + 0.005*SL	0.085 + 0.004*SL	0.076 + 0.004*SL
	t_{PLH}	0.373	0.363 + 0.005*SL	0.370 + 0.003*SL	0.393 + 0.002*SL
	t_{PHL}	0.370	0.361 + 0.005*SL	0.367 + 0.003*SL	0.385 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMICC_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.130	0.115 + 0.007*SL	0.122 + 0.006*SL	0.114 + 0.006*SL
	t_F	0.110	0.096 + 0.007*SL	0.102 + 0.006*SL	0.100 + 0.006*SL
	t_{PLH}	0.419	0.407 + 0.006*SL	0.415 + 0.004*SL	0.440 + 0.003*SL
	t_{PHL}	0.444	0.432 + 0.006*SL	0.439 + 0.004*SL	0.464 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

(Typical process, 25°C, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHICC_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.109	0.099 + 0.005*SL	0.101 + 0.004*SL	0.094 + 0.005*SL
	t_F	0.099	0.089 + 0.005*SL	0.090 + 0.005*SL	0.091 + 0.005*SL
	t_{PLH}	0.167	0.158 + 0.004*SL	0.164 + 0.003*SL	0.180 + 0.002*SL
	t_{PHL}	0.486	0.477 + 0.005*SL	0.482 + 0.004*SL	0.501 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

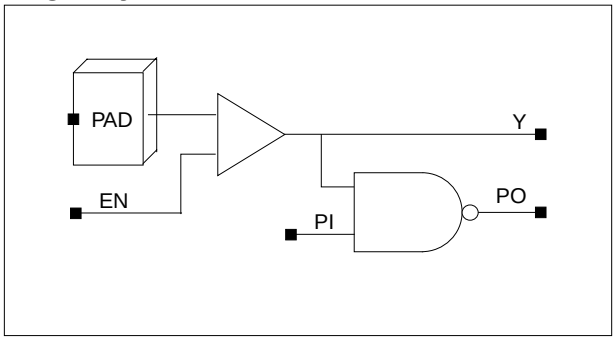
PICEN_ABB_LP/PMICEN_ABB_LP/PHICEN_ABB_LP

Analog CMOS Level Input Buffers with Enable Port and Separate Bulk-Bias

Cell Availability

1.8V Only	2.5V Interface	3.3V Interface
PICEN_ABB_LP	PMICEN_ABB_LP	PHICEN_ABB_LP

Logic Symbol



Truth Table

PAD	PI	EN	Y	PO
1	1	1	1	0
0	x	1	0	1
1	0	1	1	1
x	x	0	0	1

Standard Load (SL)

Cell Name	PI	EN
PICEN_ABB_LP	3.79	3.80
PMICEN_ABB_LP	2.13	2.46
PHICEN_ABB_LP	2.33	2.40

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PICEN_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.118	0.108 + 0.005*SL	0.111 + 0.004*SL	0.107 + 0.004*SL
	t_F	0.109	0.101 + 0.004*SL	0.102 + 0.004*SL	0.098 + 0.004*SL
	t_{PLH}	0.318	0.310 + 0.004*SL	0.315 + 0.003*SL	0.332 + 0.002*SL
	t_{PHL}	0.451	0.443 + 0.004*SL	0.447 + 0.003*SL	0.465 + 0.002*SL
EN to Y	t_R	0.081	0.072 + 0.004*SL	0.072 + 0.004*SL	0.073 + 0.004*SL
	t_F	0.072	0.064 + 0.004*SL	0.063 + 0.004*SL	0.062 + 0.004*SL
	t_{PLH}	0.177	0.171 + 0.003*SL	0.173 + 0.003*SL	0.182 + 0.002*SL
	t_{PHL}	0.200	0.193 + 0.003*SL	0.196 + 0.003*SL	0.204 + 0.002*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMICEN_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.163	0.147 + 0.008*SL	0.155 + 0.006*SL	0.162 + 0.006*SL
	t_F	0.137	0.122 + 0.007*SL	0.128 + 0.006*SL	0.133 + 0.006*SL
	t_{PLH}	0.541	0.529 + 0.006*SL	0.536 + 0.005*SL	0.566 + 0.003*SL
	t_{PHL}	0.539	0.526 + 0.006*SL	0.533 + 0.005*SL	0.561 + 0.004*SL
EN to Y	t_R	0.130	0.116 + 0.007*SL	0.119 + 0.006*SL	0.128 + 0.006*SL
	t_F	0.101	0.088 + 0.006*SL	0.090 + 0.006*SL	0.094 + 0.006*SL
	t_{PLH}	0.293	0.282 + 0.006*SL	0.288 + 0.004*SL	0.313 + 0.003*SL
	t_{PHL}	0.289	0.278 + 0.006*SL	0.284 + 0.004*SL	0.304 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

(Typical process, 25°C, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHICEN_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.138	0.128 + 0.005*SL	0.131 + 0.004*SL	0.130 + 0.004*SL
	t_F	0.133	0.122 + 0.006*SL	0.125 + 0.005*SL	0.129 + 0.005*SL
	t_{PLH}	0.273	0.265 + 0.004*SL	0.270 + 0.003*SL	0.288 + 0.002*SL
	t_{PHL}	0.577	0.568 + 0.005*SL	0.572 + 0.004*SL	0.593 + 0.003*SL
EN to Y	t_R	0.088	0.078 + 0.005*SL	0.080 + 0.005*SL	0.082 + 0.005*SL
	t_F	0.103	0.092 + 0.006*SL	0.094 + 0.005*SL	0.100 + 0.005*SL
	t_{PLH}	0.167	0.160 + 0.004*SL	0.163 + 0.003*SL	0.175 + 0.002*SL
	t_{PHL}	0.292	0.283 + 0.005*SL	0.287 + 0.004*SL	0.305 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

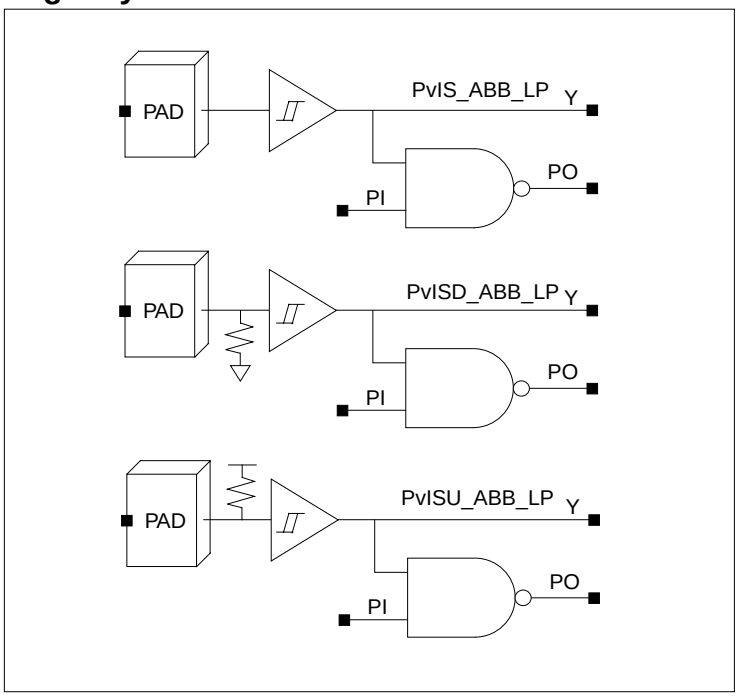
PvIS_ABB_LP/PvISD_ABB_LP/PvISU_ABB_LP

Analog CMOS Schmitt Trigger Level Input Buffer with Separate Bulk-Bias

Cell Availability

1.8V Only	2.5V Interface	3.3V Interface
PIS_ABB_LP PISD_ABB_LP PISU_ABB_LP	PMIS_ABB_LP PMISD_ABB_LP PMISU_ABB_LP	PHIS_ABB_LP PHISD_ABB_LP PHISU_ABB_LP

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Standard Load (SL)

Cell Name	PI
PIS_ABB_LP/PISD_ABB_LP/PISU_ABB_LP	3.79
PMIS_ABB_LP/PMISD_ABB_LP/PMISU_ABB_LP	2.13
PHIS_ABB_LP/PHISD_ABB_LP/PHISU_ABB_LP	2.33

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 1.50ns, SL: Standard Load)

PIS_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.113	0.103 + 0.005*SL	0.106 + 0.004*SL	0.107 + 0.004*SL
	t_F	0.121	0.112 + 0.005*SL	0.114 + 0.004*SL	0.119 + 0.004*SL
	t_{PLH}	0.653	0.645 + 0.004*SL	0.650 + 0.003*SL	0.667 + 0.002*SL
	t_{PHL}	0.688	0.679 + 0.005*SL	0.684 + 0.003*SL	0.704 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PISD_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.115	0.105 + 0.005*SL	0.108 + 0.004*SL	0.109 + 0.004*SL
	t_F	0.124	0.115 + 0.005*SL	0.117 + 0.004*SL	0.121 + 0.004*SL
	t_{PLH}	0.656	0.648 + 0.004*SL	0.652 + 0.003*SL	0.671 + 0.002*SL
	t_{PHL}	0.695	0.686 + 0.005*SL	0.691 + 0.003*SL	0.712 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PISU_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.114	0.104 + 0.005*SL	0.106 + 0.004*SL	0.108 + 0.004*SL
	t_F	0.122	0.111 + 0.005*SL	0.115 + 0.004*SL	0.119 + 0.004*SL
	t_{PLH}	0.658	0.650 + 0.004*SL	0.654 + 0.003*SL	0.673 + 0.002*SL
	t_{PHL}	0.703	0.694 + 0.005*SL	0.699 + 0.003*SL	0.720 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 1.50ns, SL: Standard Load)

PMIS_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.111	0.099 + 0.006*SL	0.099 + 0.006*SL	0.096 + 0.006*SL
	t_F	0.120	0.104 + 0.008*SL	0.111 + 0.006*SL	0.125 + 0.006*SL
	t_{PLH}	0.600	0.590 + 0.005*SL	0.595 + 0.004*SL	0.610 + 0.003*SL
	t_{PHL}	0.862	0.850 + 0.006*SL	0.856 + 0.005*SL	0.885 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PMISD_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.111	0.097 + 0.007*SL	0.100 + 0.006*SL	0.097 + 0.006*SL
	t_F	0.121	0.105 + 0.008*SL	0.112 + 0.006*SL	0.126 + 0.006*SL
	t_{PLH}	0.606	0.596 + 0.005*SL	0.601 + 0.004*SL	0.616 + 0.003*SL
	t_{PHL}	0.883	0.870 + 0.006*SL	0.876 + 0.005*SL	0.905 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PMISU_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.110	0.096 + 0.007*SL	0.099 + 0.006*SL	0.096 + 0.006*SL
	t_F	0.121	0.106 + 0.008*SL	0.112 + 0.006*SL	0.125 + 0.006*SL
	t_{PLH}	0.605	0.595 + 0.005*SL	0.599 + 0.004*SL	0.614 + 0.003*SL
	t_{PHL}	0.870	0.857 + 0.006*SL	0.863 + 0.005*SL	0.892 + 0.004*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 1.50ns, SL: Standard Load)

PHIS_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.088	0.079 + 0.005*SL	0.079 + 0.005*SL	0.077 + 0.005*SL
	t_F	0.106	0.094 + 0.006*SL	0.097 + 0.005*SL	0.106 + 0.005*SL
	t_{PLH}	0.411	0.404 + 0.003*SL	0.407 + 0.003*SL	0.416 + 0.002*SL
	t_{PHL}	0.832	0.822 + 0.005*SL	0.826 + 0.004*SL	0.845 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHISD_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.093	0.083 + 0.005*SL	0.085 + 0.005*SL	0.080 + 0.005*SL
	t_F	0.106	0.095 + 0.005*SL	0.096 + 0.005*SL	0.105 + 0.005*SL
	t_{PLH}	0.426	0.419 + 0.004*SL	0.422 + 0.003*SL	0.433 + 0.002*SL
	t_{PHL}	0.865	0.856 + 0.005*SL	0.860 + 0.004*SL	0.879 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

PHISU_ABB_LP

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_R	0.099	0.089 + 0.005*SL	0.091 + 0.005*SL	0.089 + 0.005*SL
	t_F	0.106	0.095 + 0.006*SL	0.098 + 0.005*SL	0.106 + 0.005*SL
	t_{PLH}	0.422	0.414 + 0.004*SL	0.418 + 0.003*SL	0.430 + 0.002*SL
	t_{PHL}	0.862	0.852 + 0.005*SL	0.856 + 0.004*SL	0.876 + 0.003*SL

*Group1 : SL < 4, *Group2 : 4 ≦ SL ≦ 27, *Group3 : 27 < SL

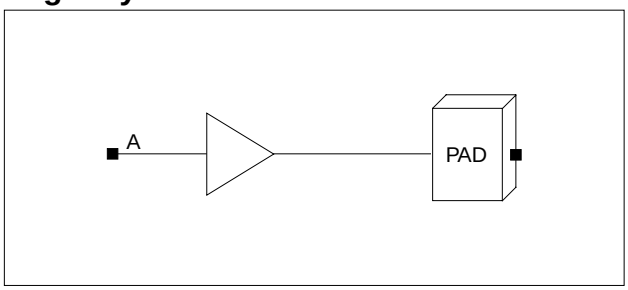
PvOByz_ABB_LP

Analog Normal Output Buffers with Separate Bulk-Bias

Cell Availability

1.8V Only	2.5V Interface	3.3V Interface
POB(1/2/8)_ABB_LP	PMOB(1/2/8)_ABB_LP	PHOB(1/2/8)_ABB_LP

Logic Symbol



Truth Table

A	PAD
0	0
1	1

Standard Load (SL)

Cell Name	A
POB(1/2/8)_ABB_LP	15.95
PMOB(1/2/8)_ABB_LP	10.47
PHOB(1/2/8)_ABB_LP	12.09

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load{pf})

POB1_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	20.215	1.333 + 0.378*CL	1.329 + 0.378*CL	1.326 + 0.378*CL
	t_F	22.775	1.555 + 0.424*CL	1.547 + 0.425*CL	1.541 + 0.425*CL
	t_{PLH}	9.705	0.791 + 0.178*CL	0.790 + 0.178*CL	0.791 + 0.178*CL
	t_{PHL}	12.279	1.412 + 0.217*CL	1.413 + 0.217*CL	1.410 + 0.217*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB2_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.606	0.929 + 0.254*CL	0.928 + 0.254*CL	0.925 + 0.254*CL
	t_F	12.068	0.834 + 0.225*CL	0.830 + 0.225*CL	0.821 + 0.225*CL
	t_{PLH}	6.770	0.701 + 0.121*CL	0.702 + 0.121*CL	0.703 + 0.121*CL
	t_{PHL}	6.674	0.821 + 0.117*CL	0.823 + 0.117*CL	0.822 + 0.117*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POB8_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.401	0.254 + 0.063*CL	0.254 + 0.063*CL	0.254 + 0.063*CL
	t_F	3.423	0.255 + 0.063*CL	0.254 + 0.063*CL	0.253 + 0.063*CL
	t_{PLH}	1.857	0.368 + 0.030*CL	0.370 + 0.030*CL	0.371 + 0.030*CL
	t_{PHL}	2.089	0.381 + 0.034*CL	0.382 + 0.034*CL	0.383 + 0.034*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics (Typical process, 25°C, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load{pf})

PMOB1_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	25.865	1.230 + 0.493*CL	1.223 + 0.493*CL	1.223 + 0.493*CL
	t_F	22.620	1.062 + 0.431*CL	1.054 + 0.431*CL	1.051 + 0.431*CL
	t_{PLH}	12.658	0.787 + 0.237*CL	0.786 + 0.237*CL	0.786 + 0.237*CL
	t_{PHL}	11.996	0.857 + 0.223*CL	0.858 + 0.223*CL	0.858 + 0.223*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB2_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	12.964	0.653 + 0.246*CL	0.648 + 0.246*CL	0.642 + 0.246*CL
	t_F	12.899	0.622 + 0.246*CL	0.615 + 0.246*CL	0.612 + 0.246*CL
	t_{PLH}	6.538	0.601 + 0.119*CL	0.602 + 0.119*CL	0.603 + 0.119*CL
	t_{PHL}	7.150	0.551 + 0.132*CL	0.551 + 0.132*CL	0.549 + 0.132*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOB8_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.382	0.402 + 0.060*CL	0.355 + 0.061*CL	0.318 + 0.061*CL
	t_F	3.289	0.299 + 0.060*CL	0.250 + 0.061*CL	0.217 + 0.061*CL
	t_{PLH}	2.460	0.955 + 0.030*CL	0.968 + 0.030*CL	0.975 + 0.030*CL
	t_{PHL}	2.210	0.601 + 0.032*CL	0.582 + 0.033*CL	0.570 + 0.033*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load{pf})

PHOB1_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	35.745	1.770 + 0.679*CL	1.769 + 0.680*CL	1.769 + 0.680*CL
	t_F	26.361	1.304 + 0.501*CL	1.299 + 0.501*CL	1.296 + 0.501*CL
	t_{PLH}	17.077	1.112 + 0.319*CL	1.111 + 0.319*CL	1.111 + 0.319*CL
	t_{PHL}	12.968	1.017 + 0.239*CL	1.018 + 0.239*CL	1.018 + 0.239*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB2_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	18.489	0.954 + 0.351*CL	0.951 + 0.351*CL	0.948 + 0.351*CL
	t_F	14.517	0.744 + 0.275*CL	0.739 + 0.276*CL	0.736 + 0.276*CL
	t_{PLH}	8.904	0.618 + 0.166*CL	0.619 + 0.166*CL	0.617 + 0.166*CL
	t_{PHL}	7.473	0.612 + 0.137*CL	0.612 + 0.137*CL	0.613 + 0.137*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOB8_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.671	0.305 + 0.087*CL	0.293 + 0.088*CL	0.288 + 0.088*CL
	t_F	4.301	0.245 + 0.081*CL	0.243 + 0.081*CL	0.241 + 0.081*CL
	t_{PLH}	2.622	0.544 + 0.042*CL	0.548 + 0.041*CL	0.550 + 0.041*CL
	t_{PHL}	2.511	0.365 + 0.043*CL	0.363 + 0.043*CL	0.360 + 0.043*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

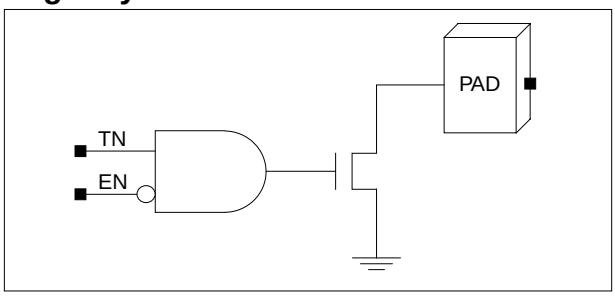
PvODyz_ABB_LP

Analog Open Drain Output Buffers with Separate Bulk-Bias

Cell Availability

3.3V Interface	PHOD4SM_ABB_LP

Logic Symbol



Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

Standard Load (SL)

Cell Name	TN	EN
PHOD4SM_ABB_LP	2.47	2.97

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOD4SM_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_F	8.628	0.565 + 0.161*CL	0.537 + 0.162*CL	0.514 + 0.162*CL
	t_{PHL}	5.367	1.053 + 0.086*CL	1.061 + 0.086*CL	1.062 + 0.086*CL
	t_{PLZ}	0.407	0.407 + 0.000*CL	0.407 + 0.000*CL	0.407 + 0.000*CL
EN to PAD	t_F	8.628	0.565 + 0.161*CL	0.537 + 0.162*CL	0.514 + 0.162*CL
	t_{PHL}	5.430	1.116 + 0.086*CL	1.124 + 0.086*CL	1.125 + 0.086*CL
	t_{PLZ}	0.431	0.431 + 0.000*CL	0.431 + 0.000*CL	0.431 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

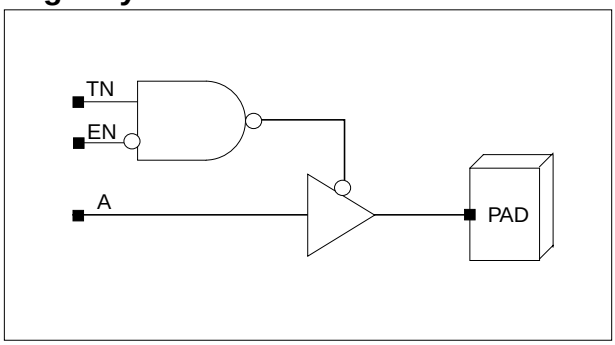
PvOTyz_ABB_LP

Analog Tri-state Output Buffers with Separate Bulk-Bias

Cell Availability

1.8V Only	2.5V Interface	3.3V Interface
POT(1/2/4/6/8/10/12/16)_ABB_LP	PMOT(1/2/4/6/8/10/12/16)_ABB_LP	PHOT(1/2/4/6/8/10/12/16)_ABB_LP

Logic Symbol



Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi - z
0	x	x	Hi - z

Standard Load (SL)

Cell Name	TN	EN	A
POT(1/2/4/6/8/10/12/16)_ABB_LP	3.80	3.69	3.67
PMOT(1/2/4/6/8/10/12/16)_ABB_LP	2.14	2.80	2.74
PHOT(1/2/4/6/8/10/12/16)_ABB_LP	2.37	2.98	2.69

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT1_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	20.215	1.333 + 0.378*CL	1.329 + 0.378*CL	1.326 + 0.378*CL
	t_F	22.775	1.555 + 0.424*CL	1.547 + 0.425*CL	1.541 + 0.425*CL
	t_{PLH}	9.897	0.983 + 0.178*CL	0.984 + 0.178*CL	0.983 + 0.178*CL
	t_{PHL}	12.442	1.575 + 0.217*CL	1.574 + 0.217*CL	1.577 + 0.217*CL
TN to PAD	t_R	20.215	1.333 + 0.378*CL	1.329 + 0.378*CL	1.329 + 0.378*CL
	t_F	22.775	1.555 + 0.424*CL	1.547 + 0.425*CL	1.541 + 0.425*CL
	t_{PLH}	9.948	1.030 + 0.178*CL	1.032 + 0.178*CL	1.035 + 0.178*CL
	t_{PHL}	12.512	1.645 + 0.217*CL	1.644 + 0.217*CL	1.647 + 0.217*CL
	t_{PLZ}	0.670	0.670 + 0.000*CL	0.670 + 0.000*CL	0.670 + 0.000*CL
	t_{PHZ}	0.531	0.531 + 0.000*CL	0.531 + 0.000*CL	0.531 + 0.000*CL
EN to PAD	t_R	20.215	1.333 + 0.378*CL	1.329 + 0.378*CL	1.329 + 0.378*CL
	t_F	22.775	1.555 + 0.424*CL	1.547 + 0.425*CL	1.541 + 0.425*CL
	t_{PLH}	10.013	1.096 + 0.178*CL	1.097 + 0.178*CL	1.097 + 0.178*CL
	t_{PHL}	12.578	1.710 + 0.217*CL	1.712 + 0.217*CL	1.709 + 0.217*CL
	t_{PLZ}	0.704	0.704 + 0.000*CL	0.704 + 0.000*CL	0.704 + 0.000*CL
	t_{PHZ}	0.565	0.565 + 0.000*CL	0.564 + 0.000*CL	0.565 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT2_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	13.606	0.929 + 0.254*CL	0.928 + 0.254*CL	0.925 + 0.254*CL
	t_F	12.068	0.834 + 0.225*CL	0.830 + 0.225*CL	0.821 + 0.225*CL
	t_{PLH}	6.968	0.900 + 0.121*CL	0.901 + 0.121*CL	0.900 + 0.121*CL
	t_{PHL}	6.837	0.985 + 0.117*CL	0.985 + 0.117*CL	0.984 + 0.117*CL
TN to PAD	t_R	13.606	0.929 + 0.254*CL	0.928 + 0.254*CL	0.925 + 0.254*CL
	t_F	12.068	0.834 + 0.225*CL	0.830 + 0.225*CL	0.821 + 0.225*CL
	t_{PLH}	7.019	0.948 + 0.121*CL	0.951 + 0.121*CL	0.951 + 0.121*CL
	t_{PHL}	6.906	1.053 + 0.117*CL	1.054 + 0.117*CL	1.054 + 0.117*CL
	t_{PLZ}	0.511	0.511 + 0.000*CL	0.511 + 0.000*CL	0.511 + 0.000*CL
	t_{PHZ}	0.824	0.824 + 0.000*CL	0.824 + 0.000*CL	0.824 + 0.000*CL
EN to PAD	t_R	13.606	0.929 + 0.254*CL	0.928 + 0.254*CL	0.925 + 0.254*CL
	t_F	12.068	0.834 + 0.225*CL	0.830 + 0.225*CL	0.821 + 0.225*CL
	t_{PLH}	7.084	1.014 + 0.121*CL	1.017 + 0.121*CL	1.016 + 0.121*CL
	t_{PHL}	6.971	1.119 + 0.117*CL	1.120 + 0.117*CL	1.120 + 0.117*CL
	t_{PLZ}	0.545	0.545 + 0.000*CL	0.545 + 0.000*CL	0.545 + 0.000*CL
	t_{PHZ}	0.858	0.858 + 0.000*CL	0.858 + 0.000*CL	0.858 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics (Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT4_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.780	0.488 + 0.126*CL	0.488 + 0.126*CL	0.485 + 0.126*CL
	t_F	6.826	0.493 + 0.127*CL	0.491 + 0.127*CL	0.487 + 0.127*CL
	t_{PLH}	3.655	0.680 + 0.059*CL	0.682 + 0.059*CL	0.683 + 0.059*CL
	t_{PHL}	4.103	0.688 + 0.068*CL	0.690 + 0.068*CL	0.690 + 0.068*CL
TN to PAD	t_R	6.780	0.488 + 0.126*CL	0.488 + 0.126*CL	0.485 + 0.126*CL
	t_F	6.826	0.493 + 0.127*CL	0.491 + 0.127*CL	0.487 + 0.127*CL
	t_{PLH}	3.705	0.728 + 0.060*CL	0.732 + 0.059*CL	0.733 + 0.059*CL
	t_{PHL}	4.170	0.750 + 0.068*CL	0.755 + 0.068*CL	0.756 + 0.068*CL
	t_{PLZ}	0.428	0.428 + 0.000*CL	0.428 + 0.000*CL	0.428 + 0.000*CL
	t_{PHZ}	0.832	0.832 + 0.000*CL	0.832 + 0.000*CL	0.832 + 0.000*CL
EN to PAD	t_R	6.780	0.488 + 0.126*CL	0.488 + 0.126*CL	0.485 + 0.126*CL
	t_F	6.826	0.493 + 0.127*CL	0.490 + 0.127*CL	0.487 + 0.127*CL
	t_{PLH}	3.770	0.794 + 0.060*CL	0.797 + 0.059*CL	0.799 + 0.059*CL
	t_{PHL}	4.235	0.816 + 0.068*CL	0.820 + 0.068*CL	0.822 + 0.068*CL
	t_{PLZ}	0.463	0.463 + 0.000*CL	0.463 + 0.000*CL	0.463 + 0.000*CL
	t_{PHZ}	0.866	0.866 + 0.000*CL	0.866 + 0.000*CL	0.866 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT6_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.723	0.370 + 0.087*CL	0.361 + 0.087*CL	0.358 + 0.087*CL
	t_F	4.392	0.364 + 0.081*CL	0.351 + 0.081*CL	0.343 + 0.081*CL
	t_{PLH}	2.908	0.833 + 0.042*CL	0.837 + 0.041*CL	0.839 + 0.041*CL
	t_{PHL}	2.989	0.837 + 0.043*CL	0.836 + 0.043*CL	0.835 + 0.043*CL
TN to PAD	t_R	4.723	0.370 + 0.087*CL	0.361 + 0.087*CL	0.358 + 0.087*CL
	t_F	4.391	0.359 + 0.081*CL	0.349 + 0.081*CL	0.342 + 0.081*CL
	t_{PLH}	2.959	0.882 + 0.042*CL	0.886 + 0.041*CL	0.889 + 0.041*CL
	t_{PHL}	3.045	0.875 + 0.043*CL	0.884 + 0.043*CL	0.889 + 0.043*CL
	t_{PLZ}	0.594	0.593 + 0.000*CL	0.593 + 0.000*CL	0.593 + 0.000*CL
	t_{PHZ}	1.411	1.411 + 0.000*CL	1.411 + 0.000*CL	1.411 + 0.000*CL
EN to PAD	t_R	4.723	0.370 + 0.087*CL	0.361 + 0.087*CL	0.358 + 0.087*CL
	t_F	4.391	0.359 + 0.081*CL	0.349 + 0.081*CL	0.342 + 0.081*CL
	t_{PLH}	3.024	0.948 + 0.042*CL	0.952 + 0.041*CL	0.954 + 0.041*CL
	t_{PHL}	3.111	0.941 + 0.043*CL	0.950 + 0.043*CL	0.954 + 0.043*CL
	t_{PLZ}	0.627	0.627 + 0.000*CL	0.627 + 0.000*CL	0.627 + 0.000*CL
	t_{PHZ}	1.445	1.445 + 0.000*CL	1.445 + 0.000*CL	1.445 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT8_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.401	0.255 + 0.063*CL	0.254 + 0.063*CL	0.254 + 0.063*CL
	t_F	3.423	0.256 + 0.063*CL	0.255 + 0.063*CL	0.254 + 0.063*CL
	t_{PLH}	2.115	0.627 + 0.030*CL	0.628 + 0.030*CL	0.629 + 0.030*CL
	t_{PHL}	2.289	0.583 + 0.034*CL	0.583 + 0.034*CL	0.583 + 0.034*CL
TN to PAD	t_R	3.401	0.255 + 0.063*CL	0.254 + 0.063*CL	0.254 + 0.063*CL
	t_F	3.422	0.253 + 0.063*CL	0.253 + 0.063*CL	0.253 + 0.063*CL
	t_{PLH}	2.166	0.675 + 0.030*CL	0.678 + 0.030*CL	0.679 + 0.030*CL
	t_{PHL}	2.352	0.637 + 0.034*CL	0.641 + 0.034*CL	0.644 + 0.034*CL
	t_{PLZ}	0.460	0.460 + 0.000*CL	0.460 + 0.000*CL	0.460 + 0.000*CL
	t_{PHZ}	0.876	0.876 + 0.000*CL	0.876 + 0.000*CL	0.876 + 0.000*CL
EN to PAD	t_R	3.401	0.255 + 0.063*CL	0.254 + 0.063*CL	0.254 + 0.063*CL
	t_F	3.423	0.253 + 0.063*CL	0.254 + 0.063*CL	0.253 + 0.063*CL
	t_{PLH}	2.231	0.741 + 0.030*CL	0.743 + 0.030*CL	0.745 + 0.030*CL
	t_{PHL}	2.417	0.702 + 0.034*CL	0.707 + 0.034*CL	0.710 + 0.034*CL
	t_{PLZ}	0.495	0.495 + 0.000*CL	0.495 + 0.000*CL	0.495 + 0.000*CL
	t_{PHZ}	0.910	0.910 + 0.000*CL	0.910 + 0.000*CL	0.910 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT10_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.561	0.209 + 0.047*CL	0.203 + 0.047*CL	0.201 + 0.047*CL
	t_F	2.689	0.231 + 0.049*CL	0.222 + 0.049*CL	0.217 + 0.049*CL
	t_{PLH}	1.778	0.660 + 0.022*CL	0.662 + 0.022*CL	0.663 + 0.022*CL
	t_{PHL}	1.990	0.670 + 0.026*CL	0.669 + 0.026*CL	0.669 + 0.026*CL
TN to PAD	t_R	2.561	0.209 + 0.047*CL	0.203 + 0.047*CL	0.200 + 0.047*CL
	t_F	2.688	0.227 + 0.049*CL	0.220 + 0.049*CL	0.216 + 0.049*CL
	t_{PLH}	1.829	0.709 + 0.022*CL	0.712 + 0.022*CL	0.714 + 0.022*CL
	t_{PHL}	2.051	0.719 + 0.027*CL	0.725 + 0.027*CL	0.728 + 0.026*CL
	t_{PLZ}	0.543	0.543 + 0.000*CL	0.543 + 0.000*CL	0.543 + 0.000*CL
	t_{PHZ}	1.023	1.023 + 0.000*CL	1.023 + 0.000*CL	1.023 + 0.000*CL
EN to PAD	t_R	2.561	0.209 + 0.047*CL	0.203 + 0.047*CL	0.200 + 0.047*CL
	t_F	2.688	0.227 + 0.049*CL	0.220 + 0.049*CL	0.216 + 0.049*CL
	t_{PLH}	1.894	0.775 + 0.022*CL	0.777 + 0.022*CL	0.779 + 0.022*CL
	t_{PHL}	2.116	0.785 + 0.027*CL	0.790 + 0.027*CL	0.794 + 0.026*CL
	t_{PLZ}	0.577	0.577 + 0.000*CL	0.577 + 0.000*CL	0.577 + 0.000*CL
	t_{PHZ}	1.057	1.056 + 0.000*CL	1.057 + 0.000*CL	1.057 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics (Typical process, 25°C, 1.8V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

POT12_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.287	0.203 + 0.042*CL	0.193 + 0.042*CL	0.188 + 0.042*CL
	t_F	2.301	0.211 + 0.042*CL	0.193 + 0.042*CL	0.188 + 0.042*CL
	t_{PLH}	1.675	0.681 + 0.020*CL	0.682 + 0.020*CL	0.684 + 0.020*CL
	t_{PHL}	1.748	0.621 + 0.023*CL	0.615 + 0.023*CL	0.612 + 0.023*CL
TN to PAD	t_R	2.287	0.203 + 0.042*CL	0.193 + 0.042*CL	0.188 + 0.042*CL
	t_F	2.298	0.192 + 0.042*CL	0.187 + 0.042*CL	0.185 + 0.042*CL
	t_{PLH}	1.726	0.729 + 0.020*CL	0.732 + 0.020*CL	0.734 + 0.020*CL
	t_{PHL}	1.799	0.651 + 0.023*CL	0.655 + 0.023*CL	0.660 + 0.023*CL
	t_{PLZ}	0.503	0.503 + 0.000*CL	0.503 + 0.000*CL	0.503 + 0.000*CL
	t_{PHZ}	1.097	1.096 + 0.000*CL	1.096 + 0.000*CL	1.097 + 0.000*CL
EN to PAD	t_R	2.287	0.203 + 0.042*CL	0.193 + 0.042*CL	0.188 + 0.042*CL
	t_F	2.298	0.192 + 0.042*CL	0.187 + 0.042*CL	0.185 + 0.042*CL
	t_{PLH}	1.791	0.795 + 0.020*CL	0.798 + 0.020*CL	0.799 + 0.020*CL
	t_{PHL}	1.864	0.716 + 0.023*CL	0.721 + 0.023*CL	0.725 + 0.023*CL
	t_{PLZ}	0.537	0.537 + 0.000*CL	0.537 + 0.000*CL	0.537 + 0.000*CL
	t_{PHZ}	1.131	1.130 + 0.000*CL	1.130 + 0.000*CL	1.131 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

POT16_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.744	0.203 + 0.031*CL	0.185 + 0.031*CL	0.173 + 0.031*CL
	t_F	1.758	0.230 + 0.031*CL	0.199 + 0.031*CL	0.175 + 0.031*CL
	t_{PLH}	1.498	0.749 + 0.015*CL	0.752 + 0.015*CL	0.754 + 0.015*CL
	t_{PHL}	1.518	0.689 + 0.017*CL	0.678 + 0.017*CL	0.670 + 0.017*CL
TN to PAD	t_R	1.744	0.203 + 0.031*CL	0.185 + 0.031*CL	0.172 + 0.031*CL
	t_F	1.744	0.179 + 0.031*CL	0.169 + 0.032*CL	0.161 + 0.032*CL
	t_{PLH}	1.549	0.798 + 0.015*CL	0.802 + 0.015*CL	0.804 + 0.015*CL
	t_{PHL}	1.551	0.686 + 0.017*CL	0.691 + 0.017*CL	0.695 + 0.017*CL
	t_{PLZ}	0.544	0.544 + 0.000*CL	0.544 + 0.000*CL	0.544 + 0.000*CL
	t_{PHZ}	1.316	1.316 + 0.000*CL	1.316 + 0.000*CL	1.316 + 0.000*CL
EN to PAD	t_R	1.744	0.203 + 0.031*CL	0.185 + 0.031*CL	0.172 + 0.031*CL
	t_F	1.744	0.179 + 0.031*CL	0.169 + 0.032*CL	0.161 + 0.032*CL
	t_{PLH}	1.614	0.864 + 0.015*CL	0.868 + 0.015*CL	0.870 + 0.015*CL
	t_{PHL}	1.616	0.751 + 0.017*CL	0.756 + 0.017*CL	0.760 + 0.017*CL
	t_{PLZ}	0.578	0.578 + 0.000*CL	0.578 + 0.000*CL	0.578 + 0.000*CL
	t_{PHZ}	1.350	1.350 + 0.000*CL	1.350 + 0.000*CL	1.350 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT1_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	25.865	1.230 + 0.493*CL	1.223 + 0.493*CL	1.223 + 0.493*CL
	t_F	22.620	1.062 + 0.431*CL	1.054 + 0.431*CL	1.051 + 0.431*CL
	t_{PLH}	12.996	1.125 + 0.237*CL	1.124 + 0.237*CL	1.124 + 0.237*CL
	t_{PHL}	12.272	1.135 + 0.223*CL	1.134 + 0.223*CL	1.134 + 0.223*CL
TN to PAD	t_R	25.865	1.228 + 0.493*CL	1.223 + 0.493*CL	1.223 + 0.493*CL
	t_F	22.620	1.062 + 0.431*CL	1.054 + 0.431*CL	1.051 + 0.431*CL
	t_{PLH}	13.099	1.225 + 0.237*CL	1.227 + 0.237*CL	1.227 + 0.237*CL
	t_{PHL}	12.391	1.252 + 0.223*CL	1.253 + 0.223*CL	1.253 + 0.223*CL
	t_{PLZ}	0.757	0.757 + 0.000*CL	0.757 + 0.000*CL	0.757 + 0.000*CL
	t_{PHZ}	0.720	0.720 + 0.000*CL	0.720 + 0.000*CL	0.720 + 0.000*CL
EN to PAD	t_R	25.865	1.228 + 0.493*CL	1.223 + 0.493*CL	1.223 + 0.493*CL
	t_F	22.620	1.062 + 0.431*CL	1.054 + 0.431*CL	1.051 + 0.431*CL
	t_{PLH}	13.168	1.295 + 0.237*CL	1.296 + 0.237*CL	1.296 + 0.237*CL
	t_{PHL}	12.460	1.321 + 0.223*CL	1.322 + 0.223*CL	1.322 + 0.223*CL
	t_{PLZ}	0.787	0.787 + 0.000*CL	0.787 + 0.000*CL	0.787 + 0.000*CL
	t_{PHZ}	0.749	0.749 + 0.000*CL	0.749 + 0.000*CL	0.749 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT2_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	12.964	0.652 + 0.246*CL	0.648 + 0.246*CL	0.642 + 0.246*CL
	t_F	12.899	0.622 + 0.246*CL	0.615 + 0.246*CL	0.612 + 0.246*CL
	t_{PLH}	6.887	0.950 + 0.119*CL	0.951 + 0.119*CL	0.952 + 0.119*CL
	t_{PHL}	7.421	0.823 + 0.132*CL	0.822 + 0.132*CL	0.824 + 0.132*CL
TN to PAD	t_R	12.964	0.652 + 0.246*CL	0.648 + 0.246*CL	0.642 + 0.246*CL
	t_F	12.899	0.622 + 0.246*CL	0.615 + 0.246*CL	0.612 + 0.246*CL
	t_{PLH}	6.989	1.050 + 0.119*CL	1.053 + 0.119*CL	1.054 + 0.119*CL
	t_{PHL}	7.538	0.937 + 0.132*CL	0.939 + 0.132*CL	0.938 + 0.132*CL
	t_{PLZ}	0.655	0.655 + 0.000*CL	0.655 + 0.000*CL	0.655 + 0.000*CL
	t_{PHZ}	0.872	0.872 + 0.000*CL	0.872 + 0.000*CL	0.872 + 0.000*CL
EN to PAD	t_R	12.964	0.652 + 0.246*CL	0.648 + 0.246*CL	0.642 + 0.246*CL
	t_F	12.899	0.622 + 0.246*CL	0.615 + 0.246*CL	0.612 + 0.246*CL
	t_{PLH}	7.059	1.120 + 0.119*CL	1.122 + 0.119*CL	1.123 + 0.119*CL
	t_{PHL}	7.607	1.006 + 0.132*CL	1.008 + 0.132*CL	1.007 + 0.132*CL
	t_{PLZ}	0.685	0.685 + 0.000*CL	0.685 + 0.000*CL	0.685 + 0.000*CL
	t_{PHZ}	0.901	0.901 + 0.000*CL	0.901 + 0.000*CL	0.901 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics (Typical process, 25°C, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT4_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.523	0.379 + 0.123*CL	0.370 + 0.123*CL	0.366 + 0.123*CL
	t_F	6.472	0.340 + 0.123*CL	0.336 + 0.123*CL	0.332 + 0.123*CL
	t_{PLH}	3.983	1.008 + 0.059*CL	1.013 + 0.059*CL	1.015 + 0.059*CL
	t_{PHL}	4.037	0.746 + 0.066*CL	0.742 + 0.066*CL	0.739 + 0.066*CL
TN to PAD	t_R	6.523	0.379 + 0.123*CL	0.370 + 0.123*CL	0.366 + 0.123*CL
	t_F	6.472	0.338 + 0.123*CL	0.336 + 0.123*CL	0.332 + 0.123*CL
	t_{PLH}	4.085	1.109 + 0.060*CL	1.114 + 0.059*CL	1.117 + 0.059*CL
	t_{PHL}	4.146	0.840 + 0.066*CL	0.845 + 0.066*CL	0.846 + 0.066*CL
	t_{PLZ}	0.760	0.760 + 0.000*CL	0.760 + 0.000*CL	0.760 + 0.000*CL
	t_{PHZ}	1.173	1.173 + 0.000*CL	1.173 + 0.000*CL	1.173 + 0.000*CL
EN to PAD	t_R	6.523	0.378 + 0.123*CL	0.370 + 0.123*CL	0.366 + 0.123*CL
	t_F	6.472	0.338 + 0.123*CL	0.336 + 0.123*CL	0.332 + 0.123*CL
	t_{PLH}	4.154	1.179 + 0.060*CL	1.184 + 0.059*CL	1.186 + 0.059*CL
	t_{PHL}	4.215	0.909 + 0.066*CL	0.914 + 0.066*CL	0.915 + 0.066*CL
	t_{PLZ}	0.789	0.789 + 0.000*CL	0.789 + 0.000*CL	0.790 + 0.000*CL
	t_{PHZ}	1.201	1.201 + 0.000*CL	1.201 + 0.000*CL	1.201 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT6_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.403	0.353 + 0.081*CL	0.320 + 0.082*CL	0.300 + 0.082*CL
	t_F	4.337	0.274 + 0.081*CL	0.251 + 0.082*CL	0.246 + 0.082*CL
	t_{PLH}	3.143	1.154 + 0.040*CL	1.160 + 0.040*CL	1.164 + 0.040*CL
	t_{PHL}	2.972	0.795 + 0.044*CL	0.785 + 0.044*CL	0.777 + 0.044*CL
TN to PAD	t_R	4.403	0.352 + 0.081*CL	0.320 + 0.082*CL	0.300 + 0.082*CL
	t_F	4.336	0.253 + 0.082*CL	0.248 + 0.082*CL	0.245 + 0.082*CL
	t_{PLH}	3.246	1.255 + 0.040*CL	1.262 + 0.040*CL	1.266 + 0.040*CL
	t_{PHL}	3.062	0.850 + 0.044*CL	0.858 + 0.044*CL	0.862 + 0.044*CL
	t_{PLZ}	0.862	0.862 + 0.000*CL	0.862 + 0.000*CL	0.862 + 0.000*CL
	t_{PHZ}	1.470	1.470 + 0.000*CL	1.470 + 0.000*CL	1.470 + 0.000*CL
EN to PAD	t_R	4.403	0.353 + 0.081*CL	0.320 + 0.082*CL	0.300 + 0.082*CL
	t_F	4.336	0.253 + 0.082*CL	0.248 + 0.082*CL	0.245 + 0.082*CL
	t_{PLH}	3.315	1.324 + 0.040*CL	1.332 + 0.040*CL	1.335 + 0.040*CL
	t_{PHL}	3.131	0.920 + 0.044*CL	0.927 + 0.044*CL	0.931 + 0.044*CL
	t_{PLZ}	0.891	0.891 + 0.000*CL	0.891 + 0.000*CL	0.891 + 0.000*CL
	t_{PHZ}	1.499	1.499 + 0.000*CL	1.499 + 0.000*CL	1.499 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT8_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.383	0.406 + 0.060*CL	0.358 + 0.061*CL	0.320 + 0.061*CL
	t_F	3.292	0.308 + 0.060*CL	0.257 + 0.061*CL	0.219 + 0.061*CL
	t_{PLH}	2.819	1.314 + 0.030*CL	1.327 + 0.030*CL	1.334 + 0.030*CL
	t_{PHL}	2.494	0.889 + 0.032*CL	0.869 + 0.033*CL	0.855 + 0.033*CL
TN to PAD	t_R	3.383	0.405 + 0.060*CL	0.358 + 0.061*CL	0.320 + 0.061*CL
	t_F	3.276	0.227 + 0.061*CL	0.215 + 0.061*CL	0.208 + 0.061*CL
	t_{PLH}	2.922	1.415 + 0.030*CL	1.430 + 0.030*CL	1.436 + 0.030*CL
	t_{PHL}	2.554	0.888 + 0.033*CL	0.897 + 0.033*CL	0.903 + 0.033*CL
	t_{PLZ}	0.963	0.963 + 0.000*CL	0.963 + 0.000*CL	0.963 + 0.000*CL
	t_{PHZ}	1.766	1.766 + 0.000*CL	1.766 + 0.000*CL	1.766 + 0.000*CL
EN to PAD	t_R	3.383	0.405 + 0.060*CL	0.358 + 0.061*CL	0.320 + 0.061*CL
	t_F	3.276	0.227 + 0.061*CL	0.215 + 0.061*CL	0.208 + 0.061*CL
	t_{PLH}	2.991	1.485 + 0.030*CL	1.499 + 0.030*CL	1.505 + 0.030*CL
	t_{PHL}	2.623	0.957 + 0.033*CL	0.967 + 0.033*CL	0.973 + 0.033*CL
	t_{PLZ}	0.992	0.992 + 0.000*CL	0.992 + 0.000*CL	0.992 + 0.000*CL
	t_{PHZ}	1.795	1.795 + 0.000*CL	1.795 + 0.000*CL	1.795 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT10_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.814	0.487 + 0.047*CL	0.434 + 0.048*CL	0.387 + 0.048*CL
	t_F	2.698	0.378 + 0.046*CL	0.314 + 0.048*CL	0.263 + 0.048*CL
	t_{PLH}	2.698	1.462 + 0.025*CL	1.496 + 0.024*CL	1.509 + 0.024*CL
	t_{PHL}	2.258	1.010 + 0.025*CL	0.978 + 0.026*CL	0.955 + 0.026*CL
TN to PAD	t_R	2.814	0.486 + 0.047*CL	0.434 + 0.048*CL	0.387 + 0.048*CL
	t_F	2.649	0.228 + 0.048*CL	0.211 + 0.049*CL	0.199 + 0.049*CL
	t_{PLH}	2.801	1.564 + 0.025*CL	1.598 + 0.024*CL	1.612 + 0.024*CL
	t_{PHL}	2.276	0.936 + 0.027*CL	0.947 + 0.027*CL	0.954 + 0.026*CL
	t_{PLZ}	1.063	1.063 + 0.000*CL	1.063 + 0.000*CL	1.063 + 0.000*CL
	t_{PHZ}	2.061	2.060 + 0.000*CL	2.061 + 0.000*CL	2.061 + 0.000*CL
EN to PAD	t_R	2.814	0.486 + 0.047*CL	0.434 + 0.048*CL	0.387 + 0.048*CL
	t_F	2.649	0.228 + 0.048*CL	0.211 + 0.049*CL	0.199 + 0.049*CL
	t_{PLH}	2.870	1.634 + 0.025*CL	1.667 + 0.024*CL	1.681 + 0.024*CL
	t_{PHL}	2.345	1.005 + 0.027*CL	1.016 + 0.027*CL	1.024 + 0.026*CL
	t_{PLZ}	1.093	1.093 + 0.000*CL	1.093 + 0.000*CL	1.093 + 0.000*CL
	t_{PHZ}	2.089	2.089 + 0.000*CL	2.089 + 0.000*CL	2.089 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 2.5V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PMOT12_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.276	0.303 + 0.039*CL	0.266 + 0.040*CL	0.237 + 0.041*CL
	t_F	2.265	0.348 + 0.038*CL	0.288 + 0.040*CL	0.241 + 0.040*CL
	t_{PLH}	2.180	1.174 + 0.020*CL	1.185 + 0.020*CL	1.189 + 0.020*CL
	t_{PHL}	2.051	1.022 + 0.021*CL	0.990 + 0.021*CL	0.968 + 0.022*CL
TN to PAD	t_R	2.275	0.303 + 0.039*CL	0.266 + 0.040*CL	0.237 + 0.041*CL
	t_F	2.213	0.200 + 0.040*CL	0.183 + 0.041*CL	0.171 + 0.041*CL
	t_{PLH}	2.283	1.275 + 0.020*CL	1.288 + 0.020*CL	1.292 + 0.020*CL
	t_{PHL}	2.071	0.953 + 0.022*CL	0.962 + 0.022*CL	0.968 + 0.022*CL
	t_{PLZ}	0.912	0.912 + 0.000*CL	0.912 + 0.000*CL	0.912 + 0.000*CL
	t_{PHZ}	1.989	1.989 + 0.000*CL	1.989 + 0.000*CL	1.989 + 0.000*CL
EN to PAD	t_R	2.275	0.303 + 0.039*CL	0.266 + 0.040*CL	0.237 + 0.041*CL
	t_F	2.213	0.200 + 0.040*CL	0.183 + 0.041*CL	0.171 + 0.041*CL
	t_{PLH}	2.352	1.345 + 0.020*CL	1.357 + 0.020*CL	1.361 + 0.020*CL
	t_{PHL}	2.140	1.023 + 0.022*CL	1.032 + 0.022*CL	1.037 + 0.022*CL
	t_{PLZ}	0.941	0.941 + 0.000*CL	0.941 + 0.000*CL	0.941 + 0.000*CL
	t_{PHZ}	2.018	2.017 + 0.000*CL	2.018 + 0.000*CL	2.018 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PMOT16_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	1.820	0.389 + 0.029*CL	0.352 + 0.029*CL	0.316 + 0.030*CL
	t_F	1.843	0.514 + 0.027*CL	0.424 + 0.028*CL	0.361 + 0.029*CL
	t_{PLH}	2.109	1.314 + 0.016*CL	1.350 + 0.015*CL	1.366 + 0.015*CL
	t_{PHL}	1.950	1.193 + 0.015*CL	1.190 + 0.015*CL	1.156 + 0.016*CL
TN to PAD	t_R	1.820	0.388 + 0.029*CL	0.351 + 0.029*CL	0.315 + 0.030*CL
	t_F	1.714	0.231 + 0.030*CL	0.211 + 0.030*CL	0.192 + 0.030*CL
	t_{PLH}	2.212	1.416 + 0.016*CL	1.453 + 0.015*CL	1.469 + 0.015*CL
	t_{PHL}	1.884	1.030 + 0.017*CL	1.046 + 0.017*CL	1.055 + 0.017*CL
	t_{PLZ}	1.012	1.012 + 0.000*CL	1.012 + 0.000*CL	1.012 + 0.000*CL
	t_{PHZ}	2.428	2.428 + 0.000*CL	2.428 + 0.000*CL	2.428 + 0.000*CL
EN to PAD	t_R	1.820	0.387 + 0.029*CL	0.351 + 0.029*CL	0.315 + 0.030*CL
	t_F	1.714	0.231 + 0.030*CL	0.211 + 0.030*CL	0.193 + 0.030*CL
	t_{PLH}	2.281	1.486 + 0.016*CL	1.522 + 0.015*CL	1.538 + 0.015*CL
	t_{PHL}	1.953	1.099 + 0.017*CL	1.116 + 0.017*CL	1.124 + 0.017*CL
	t_{PLZ}	1.042	1.041 + 0.000*CL	1.042 + 0.000*CL	1.042 + 0.000*CL
	t_{PHZ}	2.457	2.456 + 0.000*CL	2.457 + 0.000*CL	2.457 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT1_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	35.745	1.770 + 0.679*CL	1.769 + 0.680*CL	1.769 + 0.680*CL
	t_F	26.361	1.304 + 0.501*CL	1.299 + 0.501*CL	1.296 + 0.501*CL
	t_{PLH}	17.279	1.314 + 0.319*CL	1.313 + 0.319*CL	1.313 + 0.319*CL
	t_{PHL}	13.222	1.271 + 0.239*CL	1.272 + 0.239*CL	1.272 + 0.239*CL
TN to PAD	t_R	35.744	1.772 + 0.679*CL	1.768 + 0.680*CL	1.768 + 0.680*CL
	t_F	26.360	1.303 + 0.501*CL	1.298 + 0.501*CL	1.295 + 0.501*CL
	t_{PLH}	17.349	1.379 + 0.319*CL	1.383 + 0.319*CL	1.383 + 0.319*CL
	t_{PHL}	13.305	1.355 + 0.239*CL	1.353 + 0.239*CL	1.356 + 0.239*CL
	t_{PLZ}	0.845	0.845 + 0.000*CL	0.845 + 0.000*CL	0.845 + 0.000*CL
	t_{PHZ}	0.677	0.677 + 0.000*CL	0.677 + 0.000*CL	0.677 + 0.000*CL
EN to PAD	t_R	35.744	1.772 + 0.679*CL	1.768 + 0.680*CL	1.768 + 0.680*CL
	t_F	26.360	1.303 + 0.501*CL	1.298 + 0.501*CL	1.295 + 0.501*CL
	t_{PLH}	17.412	1.445 + 0.319*CL	1.444 + 0.319*CL	1.447 + 0.319*CL
	t_{PHL}	13.369	1.417 + 0.239*CL	1.419 + 0.239*CL	1.419 + 0.239*CL
	t_{PLZ}	0.868	0.868 + 0.000*CL	0.868 + 0.000*CL	0.868 + 0.000*CL
	t_{PHZ}	0.700	0.700 + 0.000*CL	0.700 + 0.000*CL	0.700 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT2_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	18.489	0.954 + 0.351*CL	0.951 + 0.351*CL	0.948 + 0.351*CL
	t_F	14.517	0.744 + 0.275*CL	0.739 + 0.276*CL	0.736 + 0.276*CL
	t_{PLH}	9.101	0.816 + 0.166*CL	0.816 + 0.166*CL	0.815 + 0.166*CL
	t_{PHL}	7.723	0.863 + 0.137*CL	0.864 + 0.137*CL	0.860 + 0.137*CL
TN to PAD	t_R	18.489	0.954 + 0.351*CL	0.951 + 0.351*CL	0.948 + 0.351*CL
	t_F	14.517	0.744 + 0.275*CL	0.739 + 0.276*CL	0.736 + 0.276*CL
	t_{PLH}	9.170	0.883 + 0.166*CL	0.884 + 0.166*CL	0.884 + 0.166*CL
	t_{PHL}	7.806	0.945 + 0.137*CL	0.945 + 0.137*CL	0.947 + 0.137*CL
	t_{PLZ}	0.641	0.641 + 0.000*CL	0.641 + 0.000*CL	0.641 + 0.000*CL
	t_{PHZ}	0.550	0.550 + 0.000*CL	0.550 + 0.000*CL	0.550 + 0.000*CL
EN to PAD	t_R	18.489	0.954 + 0.351*CL	0.951 + 0.351*CL	0.948 + 0.351*CL
	t_F	14.517	0.743 + 0.275*CL	0.739 + 0.276*CL	0.736 + 0.276*CL
	t_{PLH}	9.234	0.947 + 0.166*CL	0.947 + 0.166*CL	0.948 + 0.166*CL
	t_{PHL}	7.870	1.009 + 0.137*CL	1.009 + 0.137*CL	1.010 + 0.137*CL
	t_{PLZ}	0.664	0.664 + 0.000*CL	0.664 + 0.000*CL	0.664 + 0.000*CL
	t_{PHZ}	0.574	0.574 + 0.000*CL	0.574 + 0.000*CL	0.574 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT4_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	9.272	0.507 + 0.175*CL	0.505 + 0.175*CL	0.506 + 0.175*CL
	t_F	8.568	0.449 + 0.162*CL	0.447 + 0.162*CL	0.442 + 0.162*CL
	t_{PLH}	4.831	0.686 + 0.083*CL	0.688 + 0.083*CL	0.688 + 0.083*CL
	t_{PHL}	4.961	0.655 + 0.086*CL	0.655 + 0.086*CL	0.655 + 0.086*CL
TN to PAD	t_R	9.272	0.507 + 0.175*CL	0.505 + 0.175*CL	0.506 + 0.175*CL
	t_F	8.568	0.449 + 0.162*CL	0.447 + 0.162*CL	0.442 + 0.162*CL
	t_{PLH}	4.901	0.754 + 0.083*CL	0.757 + 0.083*CL	0.758 + 0.083*CL
	t_{PHL}	5.043	0.735 + 0.086*CL	0.737 + 0.086*CL	0.737 + 0.086*CL
	t_{PLZ}	0.536	0.536 + 0.000*CL	0.536 + 0.000*CL	0.536 + 0.000*CL
	t_{PHZ}	0.681	0.681 + 0.000*CL	0.681 + 0.000*CL	0.681 + 0.000*CL
EN to PAD	t_R	9.272	0.507 + 0.175*CL	0.505 + 0.175*CL	0.506 + 0.175*CL
	t_F	8.568	0.449 + 0.162*CL	0.447 + 0.162*CL	0.442 + 0.162*CL
	t_{PLH}	4.965	0.818 + 0.083*CL	0.821 + 0.083*CL	0.822 + 0.083*CL
	t_{PHL}	5.106	0.799 + 0.086*CL	0.800 + 0.086*CL	0.800 + 0.086*CL
	t_{PLZ}	0.560	0.560 + 0.000*CL	0.560 + 0.000*CL	0.560 + 0.000*CL
	t_{PHZ}	0.704	0.704 + 0.000*CL	0.704 + 0.000*CL	0.704 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT6_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	6.196	0.356 + 0.117*CL	0.354 + 0.117*CL	0.351 + 0.117*CL
	t_F	5.401	0.302 + 0.102*CL	0.300 + 0.102*CL	0.296 + 0.102*CL
	t_{PLH}	3.469	0.704 + 0.055*CL	0.706 + 0.055*CL	0.707 + 0.055*CL
	t_{PHL}	3.334	0.685 + 0.053*CL	0.688 + 0.053*CL	0.689 + 0.053*CL
TN to PAD	t_R	6.196	0.357 + 0.117*CL	0.354 + 0.117*CL	0.351 + 0.117*CL
	t_F	5.401	0.303 + 0.102*CL	0.300 + 0.102*CL	0.296 + 0.102*CL
	t_{PLH}	3.538	0.770 + 0.055*CL	0.774 + 0.055*CL	0.775 + 0.055*CL
	t_{PHL}	3.415	0.765 + 0.053*CL	0.768 + 0.053*CL	0.770 + 0.053*CL
	t_{PLZ}	0.745	0.745 + 0.000*CL	0.745 + 0.000*CL	0.745 + 0.000*CL
	t_{PHZ}	0.810	0.810 + 0.000*CL	0.810 + 0.000*CL	0.810 + 0.000*CL
EN to PAD	t_R	6.196	0.357 + 0.117*CL	0.354 + 0.117*CL	0.351 + 0.117*CL
	t_F	5.401	0.302 + 0.102*CL	0.300 + 0.102*CL	0.296 + 0.102*CL
	t_{PLH}	3.602	0.833 + 0.055*CL	0.837 + 0.055*CL	0.839 + 0.055*CL
	t_{PHL}	3.478	0.828 + 0.053*CL	0.832 + 0.053*CL	0.833 + 0.053*CL
	t_{PLZ}	0.769	0.769 + 0.000*CL	0.769 + 0.000*CL	0.769 + 0.000*CL
	t_{PHZ}	0.833	0.833 + 0.000*CL	0.833 + 0.000*CL	0.833 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT8_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	4.671	0.305 + 0.087*CL	0.293 + 0.088*CL	0.288 + 0.088*CL
	t_F	4.301	0.245 + 0.081*CL	0.243 + 0.081*CL	0.241 + 0.081*CL
	t_{PLH}	2.827	0.749 + 0.042*CL	0.753 + 0.041*CL	0.755 + 0.041*CL
	t_{PHL}	2.760	0.610 + 0.043*CL	0.610 + 0.043*CL	0.608 + 0.043*CL
TN to PAD	t_R	4.671	0.305 + 0.087*CL	0.293 + 0.088*CL	0.288 + 0.088*CL
	t_F	4.301	0.243 + 0.081*CL	0.243 + 0.081*CL	0.241 + 0.081*CL
	t_{PLH}	2.897	0.817 + 0.042*CL	0.822 + 0.041*CL	0.825 + 0.041*CL
	t_{PHL}	2.834	0.675 + 0.043*CL	0.679 + 0.043*CL	0.682 + 0.043*CL
	t_{PLZ}	0.643	0.643 + 0.000*CL	0.643 + 0.000*CL	0.643 + 0.000*CL
	t_{PHZ}	0.940	0.940 + 0.000*CL	0.940 + 0.000*CL	0.940 + 0.000*CL
EN to PAD	t_R	4.671	0.305 + 0.087*CL	0.293 + 0.088*CL	0.288 + 0.088*CL
	t_F	4.301	0.243 + 0.081*CL	0.243 + 0.081*CL	0.241 + 0.081*CL
	t_{PLH}	2.960	0.881 + 0.042*CL	0.886 + 0.041*CL	0.889 + 0.041*CL
	t_{PHL}	2.898	0.738 + 0.043*CL	0.742 + 0.043*CL	0.745 + 0.043*CL
	t_{PLZ}	0.666	0.666 + 0.000*CL	0.666 + 0.000*CL	0.666 + 0.000*CL
	t_{PHZ}	0.963	0.963 + 0.000*CL	0.963 + 0.000*CL	0.963 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT10_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.760	0.291 + 0.069*CL	0.268 + 0.070*CL	0.254 + 0.070*CL
	t_F	3.338	0.221 + 0.062*CL	0.211 + 0.063*CL	0.205 + 0.063*CL
	t_{PLH}	2.479	0.816 + 0.033*CL	0.819 + 0.033*CL	0.822 + 0.033*CL
	t_{PHL}	2.338	0.701 + 0.033*CL	0.701 + 0.033*CL	0.701 + 0.033*CL
TN to PAD	t_R	3.760	0.292 + 0.069*CL	0.268 + 0.070*CL	0.255 + 0.070*CL
	t_F	3.338	0.220 + 0.062*CL	0.210 + 0.063*CL	0.205 + 0.063*CL
	t_{PLH}	2.547	0.880 + 0.033*CL	0.886 + 0.033*CL	0.889 + 0.033*CL
	t_{PHL}	2.412	0.763 + 0.033*CL	0.769 + 0.033*CL	0.772 + 0.033*CL
	t_{PLZ}	0.849	0.849 + 0.000*CL	0.849 + 0.000*CL	0.849 + 0.000*CL
	t_{PHZ}	1.069	1.069 + 0.000*CL	1.069 + 0.000*CL	1.069 + 0.000*CL
EN to PAD	t_R	3.760	0.292 + 0.069*CL	0.268 + 0.070*CL	0.255 + 0.070*CL
	t_F	3.338	0.220 + 0.062*CL	0.210 + 0.063*CL	0.205 + 0.063*CL
	t_{PLH}	2.611	0.944 + 0.033*CL	0.949 + 0.033*CL	0.953 + 0.033*CL
	t_{PHL}	2.475	0.826 + 0.033*CL	0.832 + 0.033*CL	0.836 + 0.033*CL
	t_{PLZ}	0.873	0.873 + 0.000*CL	0.873 + 0.000*CL	0.873 + 0.000*CL
	t_{PHZ}	1.092	1.092 + 0.000*CL	1.092 + 0.000*CL	1.092 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Switching Characteristics (Typical process, 25°C, 3.3V, t_R/t_F = 0.20ns, CL: Capacitive Load[pf])

PHOT12_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	3.169	0.309 + 0.057*CL	0.276 + 0.058*CL	0.253 + 0.058*CL
	t_F	2.887	0.216 + 0.053*CL	0.189 + 0.054*CL	0.180 + 0.054*CL
	t_{PLH}	2.272	0.880 + 0.028*CL	0.886 + 0.028*CL	0.890 + 0.028*CL
	t_{PHL}	2.080	0.663 + 0.028*CL	0.655 + 0.029*CL	0.649 + 0.029*CL
TN to PAD	t_R	3.169	0.309 + 0.057*CL	0.276 + 0.058*CL	0.253 + 0.058*CL
	t_F	2.884	0.188 + 0.054*CL	0.182 + 0.054*CL	0.178 + 0.054*CL
	t_{PLH}	2.341	0.949 + 0.028*CL	0.955 + 0.028*CL	0.959 + 0.028*CL
	t_{PHL}	2.138	0.691 + 0.029*CL	0.698 + 0.029*CL	0.701 + 0.029*CL
	t_{PLZ}	0.747	0.747 + 0.000*CL	0.747 + 0.000*CL	0.747 + 0.000*CL
	t_{PHZ}	1.198	1.198 + 0.000*CL	1.198 + 0.000*CL	1.198 + 0.000*CL
EN to PAD	t_R	3.169	0.309 + 0.057*CL	0.276 + 0.058*CL	0.253 + 0.058*CL
	t_F	2.884	0.188 + 0.054*CL	0.182 + 0.054*CL	0.178 + 0.054*CL
	t_{PLH}	2.405	1.013 + 0.028*CL	1.019 + 0.028*CL	1.023 + 0.028*CL
	t_{PHL}	2.201	0.755 + 0.029*CL	0.761 + 0.029*CL	0.765 + 0.029*CL
	t_{PLZ}	0.771	0.771 + 0.000*CL	0.771 + 0.000*CL	0.771 + 0.000*CL
	t_{PHZ}	1.221	1.222 + 0.000*CL	1.221 + 0.000*CL	1.221 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

PHOT16_ABB_LP

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_R	2.368	0.214 + 0.043*CL	0.192 + 0.044*CL	0.177 + 0.044*CL
	t_F	2.178	0.193 + 0.040*CL	0.164 + 0.040*CL	0.146 + 0.041*CL
	t_{PLH}	1.749	0.709 + 0.021*CL	0.711 + 0.021*CL	0.713 + 0.021*CL
	t_{PHL}	1.755	0.699 + 0.021*CL	0.689 + 0.021*CL	0.683 + 0.021*CL
TN to PAD	t_R	2.368	0.214 + 0.043*CL	0.192 + 0.044*CL	0.178 + 0.044*CL
	t_F	2.172	0.157 + 0.040*CL	0.147 + 0.040*CL	0.142 + 0.041*CL
	t_{PLH}	1.820	0.778 + 0.021*CL	0.781 + 0.021*CL	0.784 + 0.021*CL
	t_{PHL}	1.808	0.722 + 0.022*CL	0.727 + 0.022*CL	0.731 + 0.022*CL
	t_{PLZ}	0.673	0.673 + 0.000*CL	0.673 + 0.000*CL	0.673 + 0.000*CL
	t_{PHZ}	1.230	1.231 + 0.000*CL	1.230 + 0.000*CL	1.230 + 0.000*CL
EN to PAD	t_R	2.368	0.214 + 0.043*CL	0.192 + 0.044*CL	0.178 + 0.044*CL
	t_F	2.172	0.157 + 0.040*CL	0.147 + 0.040*CL	0.142 + 0.041*CL
	t_{PLH}	1.884	0.842 + 0.021*CL	0.846 + 0.021*CL	0.847 + 0.021*CL
	t_{PHL}	1.872	0.786 + 0.022*CL	0.791 + 0.022*CL	0.794 + 0.022*CL
	t_{PLZ}	0.697	0.697 + 0.000*CL	0.697 + 0.000*CL	0.697 + 0.000*CL
	t_{PHZ}	1.254	1.254 + 0.000*CL	1.254 + 0.000*CL	1.254 + 0.000*CL

*Group1 : CL < 50, *Group2 : 50 ≦ CL ≦ 75, *Group3 : 75 < CL

Cell List

Cell Name	Function Description
EV1I_LP	1.8V Internal ESD Protection
EV1P_LP	1.8V Pre-Driver ESD Protection
EV1O_LP	1.8V Output-Driver ESD Protection
EV1OP_LP	1.8V Output-Drive and Pre-Driver ESD Protection
EV1OP_ABB_LP	1.8V Output-Drive and Pre-Driver ESD Protection with Separate Bulk-Bias
EV1T_ABB_LP	1.8V Total ESD Protection with Separate Bulk-Bias
EV1IM_LP	1.8V Internal for 2.5V Interface ESD Protection
EV2P_LP	2.5V Pre-Driver ESD Protection
EV2O_LP	2.5V Output-Driver ESD Protection
EV2OP_LP	2.5V Output-Driver and Pre-Driver ESD Protection
EV2OP_ABB_LP	2.5V Output-Driver and Pre-Driver ESD Protection with Separate Bulk-Bias
EV2T_ABB_LP	2.5V Total ESD Protection with Separate Bulk-Bias
EV1IH_LP	1.8V Internal for 3.3V Interface ESD Protection
EV3P_LP	3.3V Pre-Driver ESD Protection
EV3O_LP	3.3V Output-Driver ESD Protection
EV3OP_LP	3.3V Output-Driver and Pre-Driver ESD Protection
EV3OP_ABB_LP	3.3V Output-Driver and Pre-Driver ESD Protection with Separate Bulk-Bias
EV3T_ABB_LP	3.3V Total ESD Protection with Separate Bulk-Bias

Common Slot Cells

Cell List

Cell Name	Function Description
EC0C0_LP	Metal Ring Separator between Different Digital Blocks
EC0C0D_LP	Metal Ring Separator between Different Digital Blocks for Noise Critical Design
EC0CA0_LP	Metal Ring Separator between Digital to Analog
EC0CA0D_LP	Metal Ring Separator between Digital to Analog for Noise Critical Design
ECA0CA0_LP	Metal Ring Separator between Different to Analog Blocks
ECA0CA0D_LP	Metal Ring Separator between Different to Analog Blocks for Noise Critical Design
ECA0CA0_VBB_LP	Metal Ring Separator between Different Analog Blocks with VBB Ring Connected
ECA0CA0D_VBB_LP	Metal Ring Separator between Different Analog Blocks for Noise Critical Design with VBB Ring Connected

Compiled Memory

5

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OVERVIEW

This section is an overview of the STDL131 compiled memory. In STDL131 compiled memories provide application-specific memory solution high-density and low-power application. That is, two different compiled memory libraries are available in STDL131: STDL131-HD(High-Density) and STDL131-LP(Low-Power).

The high-density compiled memories are suitable for high integration application. The low-power compiled memories are suitable for portable applications. Each of these memory types may be customized to satisfy the specific circuit requirements. Each memory uses state-of-the-art design architecture techniques. The final memory block is implemented as stand-alone, pitch-matched and customized leafcells. The compiled memory is fully generated by a user-configurable compiler, called memory compiler.
The user defines the memory related specifications such as word depth, bit per word, and column mux type. The compiler then produces any or all of the following items:

— Complete functional model for simulation
— Tabular model for timing and power characteristics
— Automatic generated datasheet including all information for specific memory configuration
— Full GDS and schematic netlist for layout verification
— Phantom cell to use in chip-level floor planning and layout

Additional information about memory compilers can be obtained from your local Samsung Technology Center or Samsung's worldwide headquarters.

COMPILED MEMORY NAMING CONVENTION

In this chapter, we describe the naming convention of memory. The memory name, Figure 5-1 consists of the following convention.

'memory_name':= [memory_code]_[appl_code]_[procs_code]_[opt_code]_[config_code]

Figure 5-1. Compiled Memory Naming Convention

The first string, 'memory_code', means the name of memory type. In STDL131 compiled memory, the available memory types are as follows:

- SPSRAM : Single-Port Synchronous SRAM
- SPSRAMBW : Single-Port Synchronous SRAM with Bit-Write
- SPSRAMR : Single-Port Synchronous SRAM with Redundancy
- DPSRAM : Dual-Port Synchronous SRAM
- DPSRAMBW : Dual-Port Synchronous SRAM with Bit-Write
- DROM : Synchronous Diffusion-Programmable ROM
- MROM : Synchronous Metal2-Programmable ROM
- ARFRAM : Multi-Port Asynchronous Register File
- FIFO : Synchronous First-In First-Out Memory
- CAM : Synchronous Content Addressable Memory

The second string, 'appl_code', means the specific application to suitably support the compiled memory and the application code is one of HD(High-Density) and LP(Low-Power). The third string, 'procs_code', represents the process and the process code is one of Generic process and L Low-Power process(L). In case of Generic process, you don't have to specify 'procs_code'. If there is no process code, it means that the memory is developed under Generic process. If the process code is set to L, it means that the memory is under Low-power process. The fourth string, 'opt_code', represents the number of read and write ports for multi-port memory and the option code is composed of the following convention:

'opt_code' = <n>r<m>w

Currently this field is only used for ARFRAM, where n is the total number of read ports (1~2) and m is the total number of write ports (1~2). The last string, 'config_code', represents the configuration of the memory to be specified. This configuration code is composed of the following convention:

'config_code' = <WORD> x <BPW> m <YMUX> b <BANK>

Where, WORD is the word depth, BPW is bit per word, YMUX is the available column mux type and BANK is the number of bank used. For example, 'spsram_hdl_1024x32m16b2' refers to a High-Density single-port synchronous SRAM with 1024 words, 32 bits, 16 column mux and 2 bank under Generic process. Second, 'arfram_hdl_1r2w_32x32m2' refers to a High-Density three-port (1 read/2 write) asynchronous register file with 32 word, 32 bits and 2 column mux under Generic process. 'spsram_lpl_1024x32m16' refers to a Low-Power single-port synchronous SRAM with 1024 words, 32 bits 16 column mux under Low-power process.

CHARACTERISTICS FOR TIMING AND POWER

STDL131 compiled memories are fully optimized for 1.8V ± 0.15V supply voltage. Compiled memory in this section has been characterized using typical-process at 25 degree and 1.8V supply. The worst-case and best-case parameters can be found by using the derating factor calculated from the following equation:

$$t_{WC}(t_{BC}) = K_{P_local} * K_{V_local} * K_{T_local} * t_{NOM}$$

Where,

t_{WC} is a worst-case propagation delay

t_{BC} is a best-case propagation delay

t_{NOM} is a typical-case propagation delay characterized under typical-process, 25 degree and 1.8V supply

K_{P_local} is a local process derating factor corresponding to each memory type.

K_{V_local} is a local voltage derating factor corresponding to each memory type.

K_{T_local} is a local temperature derating factor that varies by memory type.

Note that K_{P_local}, K_{V_local} and K_{T_local} are only used in compiled memories.

A two-dimensional timing characteristics table look-up model has been adopted to yield more accuracy. Based on the combination of input slopes and output loads, the propagation delay is measured from the input crossing 50% VDD to the output crossing 50% VDD. The timing values reported in the tables are also taken from the same voltage level as the switching characteristics with 0.2ns for input slope and 10SL (Standard Load) for output load.

The power consumption for read and write modes is measured for on input slope of 0.2ns, an output load of 10SL and an input switching activity factor of 0.5. The total power consumption can be calculated by the following equation:

$$P_{total} = ((SA_{read} * P_{read}) + (SA_{write} * P_{write})) * f_{MAX}$$

Where,

P_{total} is the total power consumption in microwatts

P_{read} is the read power consumption in microwatts per MHz

P_{write} is the write power consumption in microwatts per MHz

SA_{read} is the read access ratio on every cycle

SA_{write} is the write access ratio on every cycle

f_{MAX} is the RAM clock frequency in MHz.

The value of SA_{read} or SA_{write} is between 0 and 1. However, the sum of SA_{read} and SA_{write} must be less than or equal to 1.

The power values reported in the tables are also taken from 50% switching activity, SA=0.5. For compiled memory, the read power consumption, the write power consumption and the standby power consumption are available. The standby power consumption is measured on the condition that CSN (Chip Select Negative) disabled and for other signals in their normal operating mode except that OEN (Output Enable Negative) is held low. If any of the signals are not active during standby mode, the standby power is near zero and only static leakage power consumed. In dual-port memories, the power consumption is measured with only one port active and the other port isolated.

BUILT-IN SELF TEST AND BUILT-IN REDUNDANCY-ANALYSIS

Samsung provides engineering design services to support Built-In Self-Test (BIST) and Built-In Redundancy Analysis (BIRA) for compiled memories.

BIST is the recommended test solution for compiled memories. Samsung BIST circuits are designed to detect a complete range of fault types such as stuck-at faults, transition faults, coupling faults, and address macrocells of the same or different types exist together in a circuit, Samsung supports the BIST for all to the memories as a single architecture.

BIRA design services is also provided to test redundancy RAMs with testers. BIRA tests a SRAM and generates fail information after redundancy analysis. The fail information gathered by logic tester is automatically processed and transferred to the laser repair machine. For multiple redundancy RAMs, Samsung BIRA architecture has an integration module to supp ort parallel testing, minimum test pin usage, and optimize logic tester interface.

For more detailed information regarding to the BIST and BIRA, please contact your local Samsung Technology Center or Samsung’s worldwide headquarters.

SELECTION GUIDE FOR COMPILED MEMORY

High-Density Compiled Memory

High-Density	Description
SPSRAM_HDL	- High-Density Single-port Synchronous Static RAM - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Dual bank available - Flexible aspect ratio (Ymux = 4, 8, 16, 32)
SPSRAMBW_HDL	- High-Density Single-port Synchronous Static RAM - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Dual bank available - Flexible aspect ratio(ymux = 4, 8, 16, 32)
SPSRAMR_HDL	- High-Density Single-port Synchronous Static RAM with Redundancy - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Row-only redundancy available - Failure analysis by BIRA and laser repair - Flexible aspect ratio(ymux = 8, 16, 32)
DPSRAM_HDL	- High-Density Dual-port Synchronous Static RAM - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio(ymux = 4, 8, 16, 32)
DPSRAMBW_HDL	- High-Density Dual-port Synchronous Static RAM - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio(ymux = 4, 8, 16, 32)
DROM_HDL	- High-Density Synchronous Diffusion programmable ROM - Diffusion programmable coded - Duty-free clock operation - Zero hold time for address and other control pins - Dual bank available - Flexible aspect ratio(ymux = 8, 16, 32)
MROM_HDL	- High-Density Synchronous Metal-2 programmable ROM - Metal-2 programmable coded - Duty-free clock operation - Zero hold time for address and other control pins - Dual bank available - Flexible aspect ratio(ymux = 8, 16, 32)

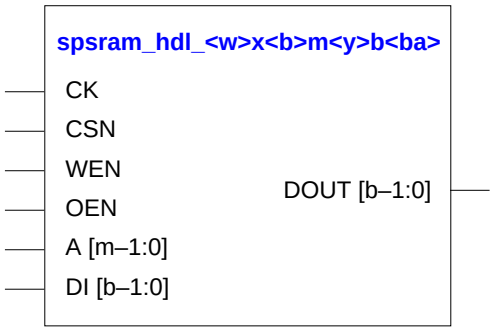
High-Density	Description
ARFRAM_HDL	- High-Density Multi-port Asynchronous Register File - Synchronous write operation / Asynchronous read operation - 1-to-2 write ports / 1-to-2 read ports - Flexible aspect ratio(ymux = 2, 4, 8)
FIFO_HDL	- High-Density Synchronous First-In First-Out Memory - Duty-free clock operation - Reset and Re-transmit operation available - Flexible aspect ratio(ymux = 2, 4, 8, 16)
CAM_HDL	- High-Density Synchronous Binary Content Addressable Memory - Duty-free clock operation - Single cycle compare operation - Built-in priority address encoder available - Global hit/miss handling

Low-Power Compiled Memory

Low-Power	Description
SPSRAM_LPL	- Low-Power Single-port Synchronous Static RAM - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio(ymux = 4, 8, 16, 32)
SPSRAMBW_LPL	- Low-Power Single-port Synchronous Static RAM - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio(ymux = 4, 8, 16, 32)
DPSRAM_LPL	- Low-Power Dual-port Synchronous Static RAM - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio(ymux = 2, 4, 8, 16)
DPSRAMBW_LPL	- Low-Power Dual-port Synchronous Static RAM - Bit-write feature available - Duty-free clock operation - Zero hold time for address, data-in and other control pins - Flexible aspect ratio(ymux = 2, 4, 8, 16)

NOTE

Logic Symbol



NOTES:
1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down
- Near zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512Kbits capacity
- Up to 32K number of words
- Up to 128 number of bits per word

Function Description

SPSRAM_HDL is a single-port synchronous static RAM which is provided as a compiler. SPSRAM_HDL is intended for use in high-density applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data on DI[] is written into the memory location specified on A[]. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAM_HDL Function Table

CK	CSN	WEN	OEN	A	DI	DOUT	COMMENT
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

Parameter Description

SPSRAM_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	ba = 1	Min	32	64	128	256
		Max	2048	4096	8192	16384
		Step	16	32	64	128
	ba = 2	Min	64	128	256	512
		Max	4096	8192	16384	32768
		Step	32	64	128	256
Bpw (b)		Min	1	1	1	1
		Max	128	64	32	16
		Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

Unit: [SL]

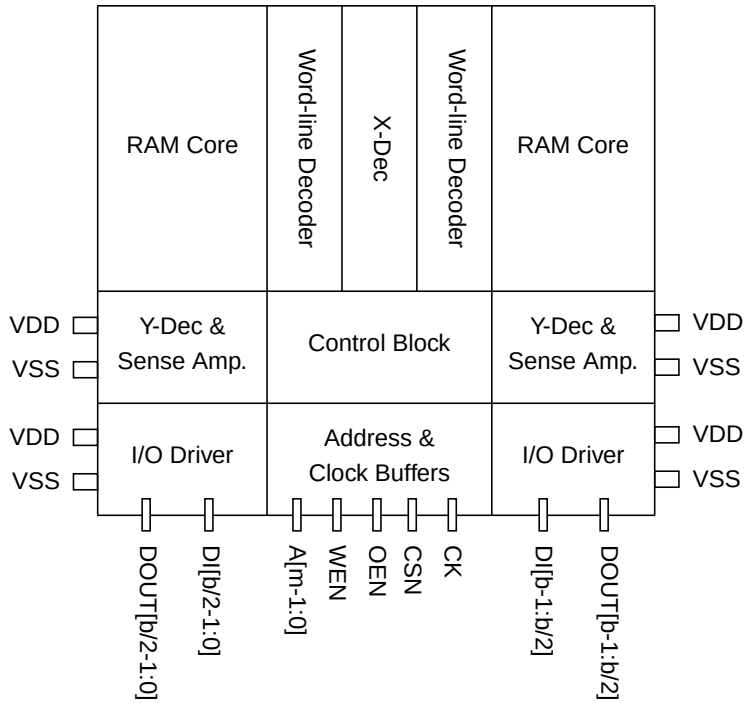
CK	CSN	WEN	OEN	A	DI	DOUT
7.03	4.14	2.89	2.89	2.89	2.89	10.42

NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

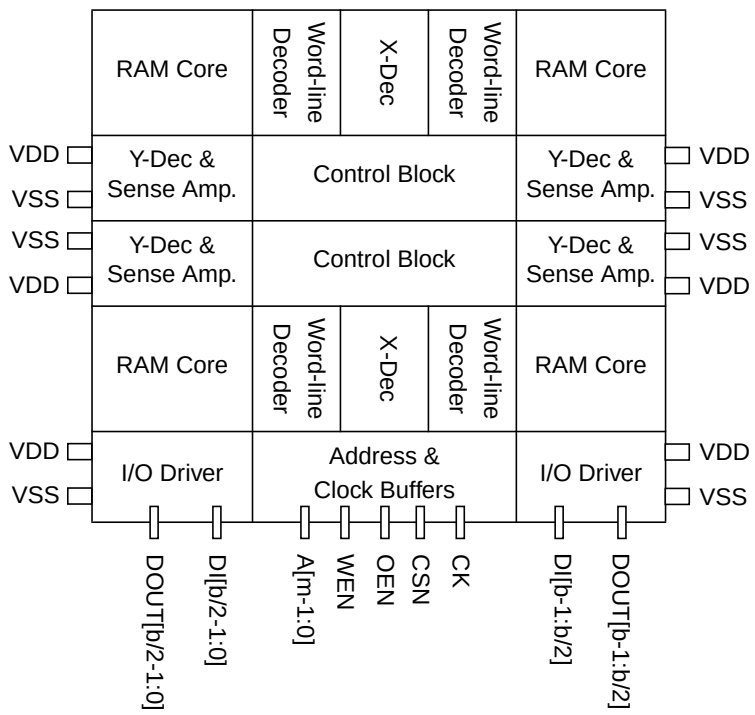
Block Diagrams

SPSRAM_HDL has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPSRAM_HDL compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the middle-edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>



<2-bank architecture >



Application Notes

1. Permitting over-the-cell routing.
   In chip-level layout, over-the-cell routing in SPSRAM_HDL is permitted only for Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAM_HDL.

4. Power reduction during standby mode.
   The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**256**	**256**	**512**	**512**	**768**	**768**
bpw	**32**	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.76	2.76	2.82	2.81	2.92	2.89	3.11	2.97
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.53	0.58	0.54	0.58	0.55	0.58	0.56	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.18	0.18	0.17	0.17	0.15	0.16	0.14	0.15
t_{dh}	0.17	0.17	0.19	0.19	0.20	0.20	0.22	0.22
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.39	0.38
t_{wh}	0.23	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{acc}	2.38	2.39	2.44	2.44	2.55	2.52	2.74	2.60
t_{da}	1.82	1.80	1.88	1.85	1.99	1.92	2.17	1.98
t_{dz}	0.21	0.21	0.22	0.22	0.24	0.24	0.25	0.25
t_{zd}	0.22	0.23	0.25	0.25	0.27	0.27	0.28	0.29
t_{od}	0.77	0.77	0.80	0.80	0.82	0.82	0.85	0.85
Power (µW/MHz)								
Power_read	142.92	157.33	201.95	218.13	266.87	283.21	333.79	353.99
Power_write	147.51	160.94	213.72	225.75	295.29	299.35	387.45	381.82
Power_standby	43.36	50.90	59.78	69.38	76.54	88.80	92.47	107.68
Area (µm)								
Width	337.28	337.28	456.04	456.04	574.80	574.80	693.56	693.56
Height	274.90	393.82	351.70	470.62	505.30	624.22	658.90	777.82

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.31	3.05	3.64	3.27	3.68	3.50	4.01
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.57	0.59	0.58	0.59	0.59	0.59	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.13	0.14	0.12	0.13	0.11	0.11	0.11
t_{dh}	0.24	0.24	0.26	0.26	0.28	0.28	0.28
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.35
t_{wh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{acc}	2.94	2.68	3.28	2.90	3.31	3.13	3.64
t_{da}	2.36	2.05	2.69	2.24	2.72	2.45	2.85
t_{dz}	0.26	0.26	0.27	0.27	0.29	0.29	0.29
t_{zd}	0.30	0.30	0.32	0.32	0.33	0.33	0.33
t_{od}	0.88	0.88	0.90	0.90	0.93	0.93	0.93
Power (µW/MHz)							
Power_read	400.77	423.79	487.08	500.41	554.10	579.97	637.90
Power_write	486.61	466.56	627.73	574.55	773.90	692.54	847.50
Power_standby	109.16	128.13	125.99	150.32	142.60	173.15	187.80
Area (µm)							
Width	812.32	812.32	931.08	931.08	1049.84	1049.84	1049.84
Height	812.50	931.42	1119.70	1238.62	1426.90	1545.82	2774.62

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**512**	**512**	**1024**	**1024**	**1536**	**1536**
bpw	**16**	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.76	2.77	2.82	2.82	2.93	2.89	3.12	2.97
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.53	0.58	0.54	0.58	0.55	0.58	0.56	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.19	0.19	0.18	0.18	0.17	0.17	0.16	0.16
t_{dh}	0.16	0.16	0.17	0.17	0.18	0.18	0.20	0.20
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.39	0.38
t_{wh}	0.23	0.23	0.22	0.22	0.22	0.22	0.22	0.22
t_{acc}	2.39	2.40	2.45	2.44	2.55	2.52	2.74	2.60
t_{da}	1.83	1.81	1.89	1.85	1.99	1.92	2.17	1.98
t_{dz}	0.20	0.20	0.21	0.21	0.22	0.22	0.23	0.23
t_{zd}	0.21	0.21	0.23	0.23	0.24	0.24	0.25	0.25
t_{od}	0.75	0.75	0.77	0.77	0.79	0.79	0.81	0.81
Power (µW/MHz)								
Power_read	115.89	128.12	161.52	174.14	213.41	224.08	267.64	280.42
Power_write	121.97	135.55	172.91	186.19	234.13	242.76	302.94	307.23
Power_standby	28.42	35.49	37.37	46.13	46.68	57.38	55.09	68.02
Area (µm)								
Width	337.28	337.28	456.04	456.04	574.80	574.80	693.56	693.56
Height	210.60	300.76	287.40	377.56	441.00	531.16	594.60	684.76

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.32	3.05	3.64	3.27	3.69	3.50	4.01
t_{ckl}	0.78	0.78	0.78	0.78	0.79	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.57	0.59	0.58	0.59	0.59	0.59	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.16	0.16	0.15	0.15	0.14	0.14	0.14
t_{dh}	0.21	0.21	0.22	0.22	0.24	0.24	0.24
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.35
t_{wh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{acc}	2.94	2.67	3.27	2.90	3.31	3.13	3.64
t_{da}	2.37	2.04	2.69	2.24	2.72	2.45	2.85
t_{dz}	0.24	0.24	0.25	0.25	0.25	0.25	0.25
t_{zd}	0.26	0.27	0.28	0.28	0.29	0.29	0.29
t_{od}	0.83	0.83	0.84	0.84	0.86	0.86	0.86
Power (µW/MHz)							
Power_read	320.61	334.59	392.94	394.03	447.00	455.58	503.90
Power_write	373.67	370.59	472.29	447.52	566.60	530.31	623.00
Power_standby	64.35	79.89	73.53	92.67	82.77	105.83	113.90
Area (µm)							
Width	812.32	812.32	931.08	931.08	1049.84	1049.84	1049.84
Height	748.20	838.36	1055.40	1145.56	1362.60	1452.76	2681.56

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**1024**	**1024**	**2048**	**2048**	**3072**	**3072**
bpw	**8**	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.78	2.81	2.84	2.85	2.95	2.93	3.14	3.01
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.53	0.58	0.54	0.58	0.55	0.58	0.56	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.19	0.20	0.19	0.19	0.18	0.18	0.17	0.17
t_{dh}	0.16	0.16	0.17	0.16	0.17	0.17	0.19	0.18
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.38	0.38
t_{wh}	0.23	0.23	0.22	0.22	0.22	0.22	0.23	0.22
t_{acc}	2.41	2.43	2.47	2.48	2.57	2.56	2.76	2.64
t_{da}	1.83	1.81	1.89	1.85	1.99	1.92	2.17	1.98
t_{dz}	0.19	0.19	0.20	0.20	0.21	0.21	0.22	0.22
t_{zd}	0.21	0.21	0.22	0.22	0.22	0.23	0.24	0.24
t_{od}	0.75	0.75	0.76	0.76	0.77	0.77	0.79	0.79
Power (µW/MHz)								
Power_read	87.90	100.11	119.43	132.00	157.04	167.59	197.52	209.08
Power_write	90.00	103.74	123.54	137.73	164.68	176.19	211.42	221.12
Power_standby	22.05	28.83	27.82	36.06	33.94	43.73	39.02	50.43
Area (µm)								
Width	337.28	337.28	456.04	456.04	574.80	574.78	693.56	693.56
Height	210.60	300.76	287.40	377.56	441.00	531.16	594.60	684.76

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.34	3.09	3.67	3.30	3.70	3.54	4.04
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.42	0.41	0.41	0.41	0.41
t_{as}	0.56	0.59	0.57	0.59	0.59	0.59	0.59
t_{ah}	0.23	0.23	0.24	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.16	0.17	0.15	0.16	0.16	0.16	0.16
t_{dh}	0.20	0.19	0.22	0.20	0.21	0.21	0.21
t_{ws}	0.38	0.38	0.37	0.38	0.39	0.38	0.35
t_{wh}	0.23	0.22	0.23	0.22	0.22	0.22	0.22
t_{acc}	2.96	2.71	3.29	2.93	3.33	3.17	3.67
t_{da}	2.37	2.04	2.69	2.24	2.72	2.45	2.85
t_{dz}	0.22	0.22	0.23	0.23	0.24	0.24	0.24
t_{zd}	0.24	0.25	0.25	0.25	0.26	0.26	0.26
t_{od}	0.80	0.80	0.81	0.81	0.83	0.83	0.83
Power (µW/MHz)							
Power_read	236.66	248.58	294.99	292.89	334.10	339.11	382.90
Power_write	258.62	264.40	325.95	316.89	384.20	373.19	434.40
Power_standby	45.15	58.64	51.23	67.22	54.47	75.94	80.95
Area (µm)							
Width	812.32	812.32	931.08	931.08	1049.84	1049.84	1049.84
Height	748.20	838.36	1055.40	1145.56	1362.60	1452.76	2681.56

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**1024**	**1024**	**2048**	**2048**	**4096**	**4096**	**6144**	**6144**
bpw	**4**	**4**	**6**	**6**	**8**	**8**	**10**	**10**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.82	2.88	2.88	2.92	3.00	3.00	3.17	3.07
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.53	0.58	0.54	0.58	0.55	0.58	0.56	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.20	0.20	0.19	0.19	0.18	0.18	0.18	0.18
t_{dh}	0.15	0.15	0.16	0.16	0.17	0.17	0.18	0.18
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.39	0.38
t_{wh}	0.23	0.23	0.22	0.22	0.22	0.22	0.22	0.22
t_{acc}	2.45	2.50	2.51	2.55	2.62	2.63	2.80	2.71
t_{da}	1.83	1.81	1.89	1.85	1.99	1.92	2.17	1.98
t_{dz}	0.19	0.19	0.20	0.20	0.20	0.20	0.21	0.21
t_{zd}	0.20	0.20	0.21	0.21	0.22	0.22	0.23	0.23
t_{od}	0.74	0.74	0.75	0.75	0.76	0.76	0.78	0.78
Power (µW/MHz)								
Power_read	73.89	85.99	98.33	110.74	128.92	139.15	162.33	173.07
Power_write	73.64	87.51	98.14	112.86	128.81	141.89	163.90	176.34
Power_standby	18.35	24.98	22.28	30.23	26.55	35.84	29.50	39.89
Area (µm)								
Width	337.28	337.28	456.04	456.04	574.80	574.80	693.56	693.56
Height	210.60	300.76	287.40	377.56	441.00	531.16	594.60	684.76

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

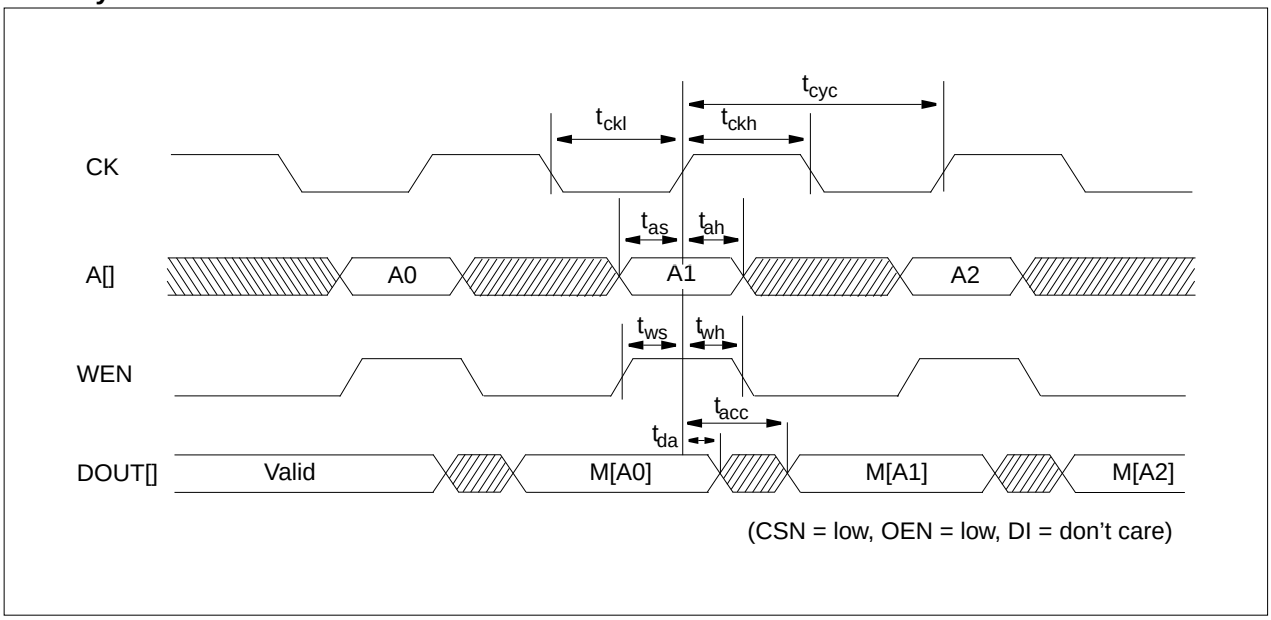
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**8192**	**8192**	**12288**	**12288**	**16384**	**16384**	**32768**
bpw	**12**	**12**	**14**	**14**	**16**	**16**	**16**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.37	3.15	3.71	3.37	3.74	3.60	4.11
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.57	0.59	0.58	0.59	0.59	0.59	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.17	0.17	0.17	0.17	0.16	0.16	0.16
t_{dh}	0.19	0.19	0.20	0.19	0.20	0.20	0.20
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.35
t_{wh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{acc}	3.00	2.78	3.33	3.00	3.37	3.24	3.74
t_{da}	2.37	2.04	2.69	2.24	2.72	2.45	2.85
t_{dz}	0.22	0.22	0.22	0.22	0.23	0.23	0.23
t_{zd}	0.24	0.24	0.24	0.24	0.25	0.25	0.25
t_{od}	0.79	0.79	0.80	0.80	0.81	0.81	0.81
Power (µW/MHz)							
Power_read	194.55	205.42	246.16	242.31	278.50	280.88	321.80
Power_write	199.19	209.62	251.06	249.72	291.20	292.51	337.50
Power_standby	33.10	46.14	38.26	52.54	42.62	58.96	62.26
Area (µm)							
Width	812.32	812.32	931.08	931.08	1049.84	1049.84	1049.84
Height	748.20	838.36	1055.40	1145.56	1362.60	1452.76	2681.56

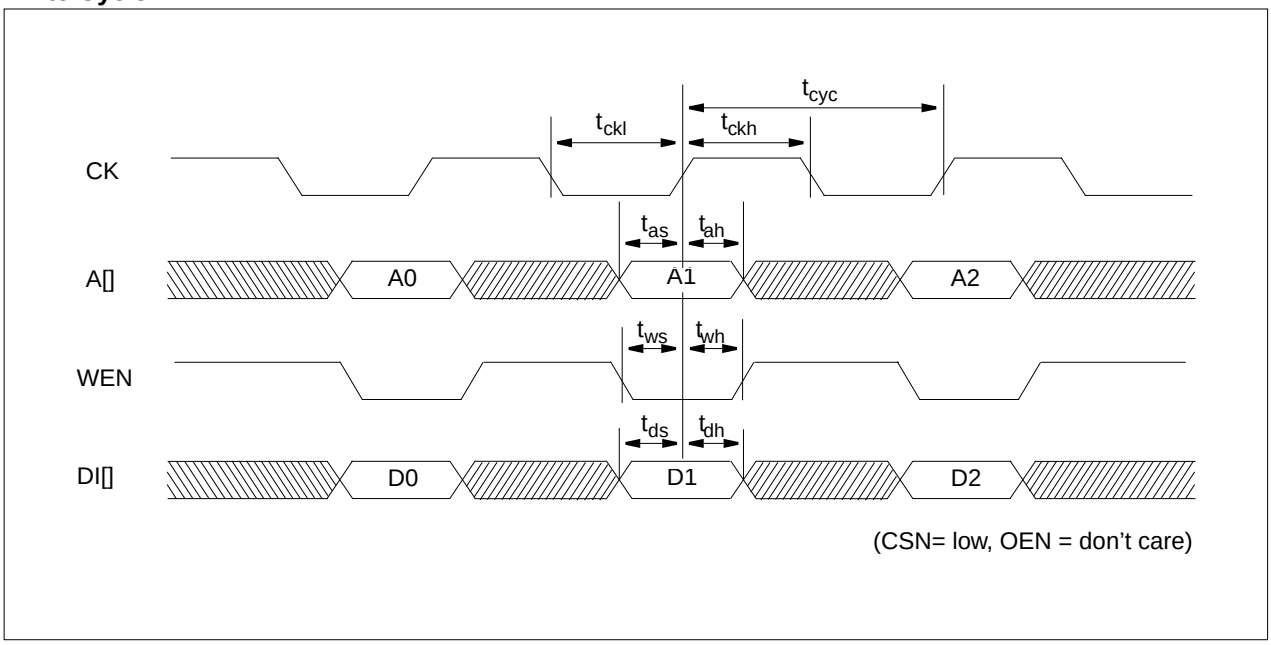
NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Timing Diagrams

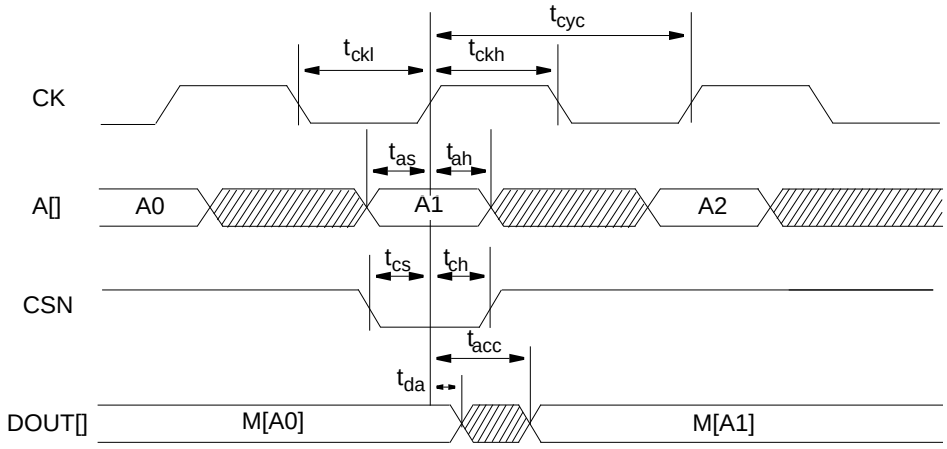
Read Cycle



Write Cycle

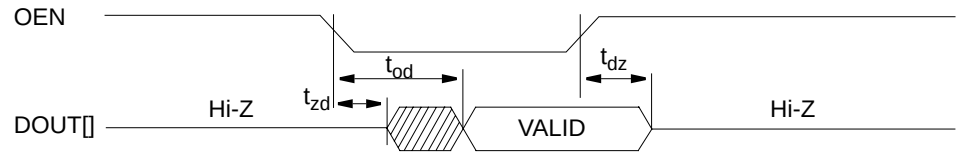


Read Cycle with CSN Controlled



(OEN = low, WEN = high, DI = don't care)

OEN Controlled Output Enable



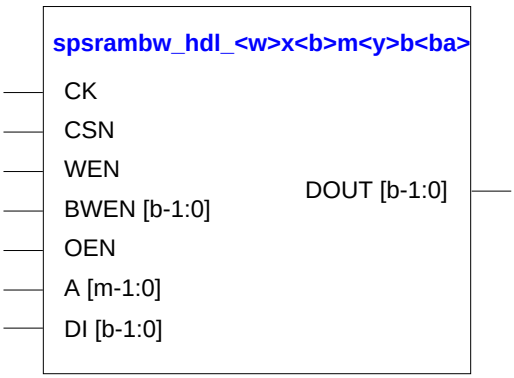
(CK, A, WEN, DI, CSN = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

SPSRAMBW_HDL

High-Density Single-port Synchronous Static RAM with Bit-Write

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Bit-Write capability
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tristate output
- Latched inputs and outputs
- Automatic power-down
- Near zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512Kbits capacity
- Up to 32K number of words
- Up to128 number of bit per word

Function Description

SPSRAMBW_HDL is a single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMBW_HDL is intended for use in high-density applications. Basically, its functionality is exactly same as SPSRAM_HDL except a bit-write operation which is controlled by BWEN[], named bit-write enable signal bus. Each bit of BWEN[] enables or disables the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data bits in DI[], which their corresponding bit(s) in BWEN[] are low, are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM_HDL. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAMBW_HDL Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read Cycle

Parameter Description

SPSRAMBW_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba)

Parameters			Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux =(y) 32
Words (w)	ba = 1	Min	32	64	128	256
		Max	2048	4096	8192	16384
		Step	16	32	64	128
	ba = 2	Min	64	128	256	512
		Max	4096	8192	16384	32768
		Step	32	64	128	256
Bpw (b)		Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
BWEN[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A[]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI[]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT[]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

Unit: [SL]

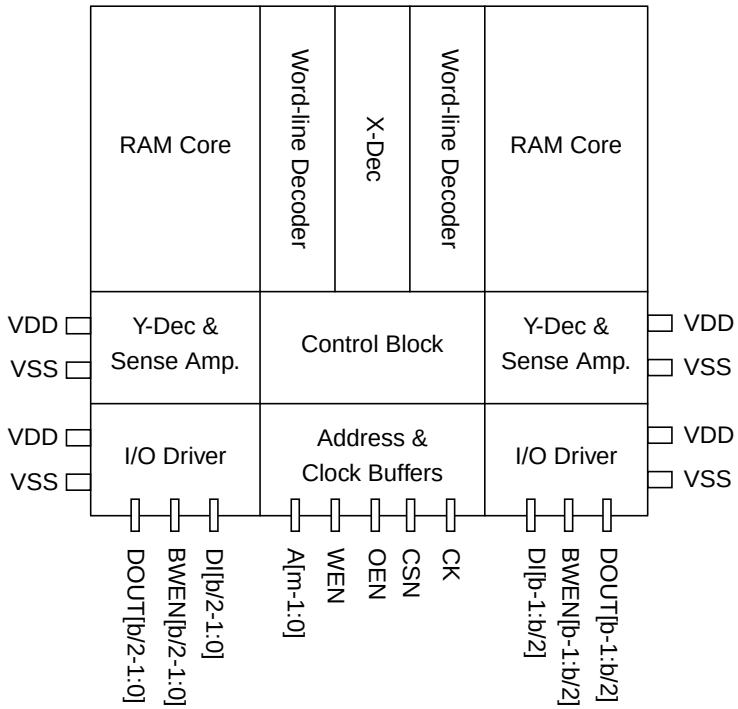
CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
7.03	4.14	2.89	2.89	2.89	2.89	2.89	10.42

NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

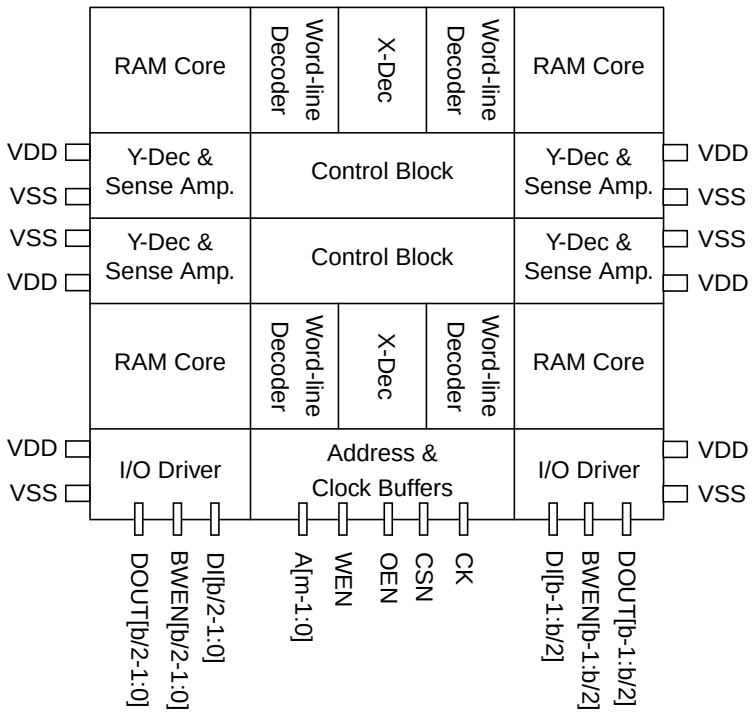
Block Diagrams

SPSRAMBW_HDL has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPSRAMBW_HDL compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the middle-edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>



<2-bank architecture >



Application Notes

1. Permitting Over-the-cell routing
In chip-level layout, over-the-cell routing in SPSRAMBW_HDL is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAMBW_HDL.

4. A byte-write or word-write operation with SPSRAMBW_HDL.
Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPSRAM_HDL. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

5. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{bws}	BWEN setup time
t_{bwh}	BWEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**128**	**128**	**256**	**256**	**512**	**512**	**768**	**768**
bpw	**32**	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.76	2.76	2.82	2.81	2.92	2.89	3.11	2.97
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.53	0.58	0.54	0.58	0.55	0.58	0.56	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.18	0.18	0.17	0.17	0.15	0.16	0.14	0.15
t_{dh}	0.17	0.17	0.19	0.19	0.20	0.20	0.22	0.22
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.39	0.38
t_{wh}	0.23	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{bws}	0.18	0.18	0.17	0.17	0.15	0.17	0.14	0.17
t_{bwh}	0.15	0.15	0.17	0.17	0.19	0.19	0.20	0.20
t_{acc}	2.38	2.39	2.44	2.44	2.55	2.52	2.74	2.60
t_{da}	1.82	1.80	1.88	1.85	1.99	1.92	2.17	1.98
t_{dz}	0.21	0.21	0.22	0.22	0.24	0.24	0.25	0.25
t_{zd}	0.22	0.23	0.25	0.25	0.27	0.27	0.28	0.29
t_{od}	0.77	0.77	0.80	0.80	0.82	0.82	0.85	0.85
Power (µW/MHz)								
Power_read	149.56	163.93	212.12	228.26	280.56	296.88	350.76	371.13
Power_write	154.13	167.93	223.87	235.91	308.95	313.05	404.47	398.99
Power_standby	49.98	57.51	69.92	79.53	90.21	102.49	109.47	124.82
Area (µm)								
Width	337.28	337.28	456.04	456.04	574.80	574.80	693.56	693.56
Height	274.90	393.82	351.70	470.62	505.30	624.22	658.90	777.82

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.31	3.05	3.64	3.27	3.68	3.50	4.01
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.57	0.59	0.58	0.59	0.59	0.59	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.13	0.14	0.12	0.13	0.11	0.11	0.11
t_{dh}	0.24	0.24	0.26	0.26	0.28	0.28	0.28
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.35
t_{wh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{bws}	0.13	0.17	0.12	0.18	0.11	0.19	0.25
t_{bwh}	0.22	0.22	0.24	0.24	0.26	0.26	0.26
t_{acc}	2.94	2.68	3.28	2.90	3.31	3.13	3.64
t_{da}	2.36	2.05	2.69	2.24	2.72	2.45	2.85
t_{dz}	0.26	0.26	0.27	0.27	0.29	0.29	0.29
t_{zd}	0.30	0.30	0.32	0.32	0.33	0.33	0.33
t_{od}	0.88	0.88	0.90	0.90	0.93	0.93	0.93
Power (µW/MHz)							
Power_read	421.34	444.55	511.18	524.83	581.85	608.05	666.40
Power_write	507.19	487.37	651.81	598.99	801.67	720.66	876.01
Power_standby	129.75	148.89	150.10	174.75	170.32	201.31	216.24
Area (µm)							
Width	812.32	812.32	931.08	931.08	1049.84	1049.84	1049.84
Height	812.50	931.42	1119.70	1238.62	1426.90	1545.82	2774.62

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**256**	**256**	**512**	**512**	**1024**	**1024**	**1536**	**1536**
bpw	**16**	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.76	2.77	2.82	2.82	2.93	2.89	3.12	2.97
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.53	0.58	0.54	0.58	0.55	0.58	0.56	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.19	0.19	0.18	0.18	0.17	0.17	0.16	0.16
t_{dh}	0.16	0.16	0.17	0.17	0.18	0.18	0.20	0.20
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.39	0.38
t_{wh}	0.23	0.23	0.22	0.22	0.22	0.22	0.22	0.22
t_{bws}	0.19	0.19	0.17	0.18	0.15	0.18	0.15	0.19
t_{bwh}	0.14	0.14	0.15	0.15	0.17	0.17	0.18	0.18
t_{acc}	2.39	2.40	2.45	2.44	2.55	2.52	2.74	2.60
t_{da}	1.83	1.81	1.89	1.85	1.99	1.92	2.17	1.98
t_{dz}	0.20	0.20	0.21	0.21	0.22	0.22	0.23	0.23
t_{zd}	0.21	0.21	0.23	0.23	0.24	0.24	0.25	0.25
t_{od}	0.75	0.75	0.77	0.77	0.79	0.79	0.81	0.81
Power (µW/MHz)								
Power_read	118.96	131.20	166.33	178.98	219.97	230.70	275.80	288.66
Power_write	125.05	138.65	177.76	191.07	240.76	249.42	311.14	315.46
Power_standby	31.50	38.58	42.22	50.99	53.29	64.02	63.28	76.29
Area (µm)								
Width	337.28	337.28	456.04	456.04	574.80	574.80	693.56	693.56
Height	210.60	300.76	287.40	377.56	441.00	531.16	594.60	684.76

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.32	3.05	3.64	3.27	3.69	3.50	4.01
t_{ckl}	0.78	0.78	0.78	0.78	0.79	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.57	0.59	0.58	0.59	0.59	0.59	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.16	0.16	0.15	0.15	0.14	0.14	0.14
t_{dh}	0.21	0.21	0.22	0.22	0.24	0.24	0.24
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.35
t_{wh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{bws}	0.14	0.19	0.13	0.21	0.12	0.22	0.27
t_{bwh}	0.19	0.19	0.20	0.20	0.22	0.22	0.22
t_{acc}	2.94	2.67	3.27	2.90	3.31	3.13	3.64
t_{da}	2.37	2.04	2.69	2.24	2.72	2.45	2.85
t_{dz}	0.24	0.24	0.25	0.25	0.25	0.25	0.25
t_{zd}	0.26	0.27	0.28	0.28	0.29	0.29	0.29
t_{od}	0.83	0.83	0.84	0.84	0.86	0.86	0.86
Power (µW/MHz)							
Power_read	330.59	344.67	404.75	406.02	460.58	469.51	517.89
Power_write	383.70	380.68	484.13	459.49	580.26	544.15	637.04
Power_standby	74.34	90.02	85.37	104.67	96.38	119.71	127.91
Area (µm)							
Width	812.32	812.32	931.08	931.08	1049.84	1049.84	1049.84
Height	748.20	838.36	1055.40	1145.56	1362.60	1452.76	2681.56

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**512**	**512**	**1024**	**1024**	**2048**	**2048**	**3072**	**3072**
bpw	**8**	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.78	2.81	2.84	2.85	2.95	2.93	3.14	3.01
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.53	0.58	0.54	0.58	0.55	0.58	0.56	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.19	0.20	0.19	0.19	0.18	0.18	0.17	0.17
t_{dh}	0.16	0.16	0.17	0.16	0.17	0.17	0.19	0.18
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.38	0.38
t_{wh}	0.23	0.23	0.22	0.22	0.22	0.22	0.23	0.22
t_{bws}	0.20	0.21	0.18	0.20	0.16	0.20	0.16	0.21
t_{bwh}	0.14	0.14	0.15	0.15	0.16	0.16	0.17	0.17
t_{acc}	2.41	2.43	2.47	2.48	2.57	2.56	2.76	2.64
t_{da}	1.83	1.81	1.89	1.85	1.99	1.92	2.17	1.98
t_{dz}	0.19	0.19	0.20	0.20	0.21	0.21	0.22	0.22
t_{zd}	0.21	0.21	0.22	0.22	0.22	0.23	0.24	0.24
t_{od}	0.75	0.75	0.76	0.76	0.77	0.77	0.79	0.79
Power (µW/MHz)								
Power_read	89.21	101.43	121.62	134.21	160.11	170.70	201.29	212.89
Power_write	91.32	105.08	125.75	139.96	167.80	179.30	215.24	224.97
Power_standby	23.37	30.17	30.03	38.28	37.03	46.84	42.82	54.27
Area (µm)								
Width	337.28	337.28	456.04	456.04	574.80	574.78	693.56	693.56
Height	210.60	300.76	287.40	377.56	441.00	531.16	594.60	684.76

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.34	3.09	3.67	3.30	3.70	3.54	4.04
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.42	0.41	0.41	0.41	0.41
t_{as}	0.56	0.59	0.57	0.59	0.59	0.59	0.59
t_{ah}	0.23	0.23	0.24	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.16	0.17	0.15	0.16	0.16	0.16	0.16
t_{dh}	0.20	0.19	0.22	0.20	0.21	0.21	0.21
t_{ws}	0.38	0.38	0.37	0.38	0.39	0.38	0.35
t_{wh}	0.23	0.22	0.23	0.22	0.22	0.22	0.22
t_{bws}	0.15	0.21	0.15	0.22	0.14	0.24	0.30
t_{bwh}	0.18	0.18	0.19	0.19	0.20	0.20	0.20
t_{acc}	2.96	2.71	3.29	2.93	3.33	3.17	3.67
t_{da}	2.37	2.04	2.69	2.24	2.72	2.45	2.85
t_{dz}	0.22	0.22	0.23	0.23	0.24	0.24	0.24
t_{zd}	0.24	0.25	0.25	0.25	0.26	0.26	0.26
t_{od}	0.80	0.80	0.81	0.81	0.83	0.83	0.83
Power (µW/MHz)							
Power_read	241.37	253.35	300.65	298.65	340.70	345.86	389.65
Power_write	263.34	269.22	331.64	322.68	390.77	379.97	441.17
Power_standby	49.88	63.43	56.91	72.98	64.07	82.67	87.74
Area (µm)							
Width	812.32	812.32	931.08	931.08	1049.84	1049.84	1049.84
Height	748.20	838.36	1055.40	1145.56	1362.60	1452.76	2681.56

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**1024**	**1024**	**2048**	**2048**	**4096**	**4096**	**6144**	**6144**
bpw	**4**	**4**	**6**	**6**	**8**	**8**	**10**	**10**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	2.82	2.88	2.88	2.92	3.00	3.00	3.17	3.07
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.53	0.58	0.54	0.58	0.55	0.58	0.56	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.20	0.20	0.19	0.19	0.18	0.18	0.18	0.18
t_{dh}	0.15	0.15	0.16	0.16	0.17	0.17	0.18	0.18
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.39	0.38
t_{wh}	0.23	0.23	0.22	0.22	0.22	0.22	0.22	0.22
t_{bws}	0.21	0.24	0.20	0.23	0.18	0.23	0.18	0.23
t_{bwh}	0.13	0.13	0.14	0.14	0.15	0.15	0.16	0.16
t_{acc}	2.45	2.50	2.51	2.55	2.62	2.63	2.80	2.71
t_{da}	1.83	1.81	1.89	1.85	1.99	1.92	2.17	1.98
t_{dz}	0.19	0.19	0.20	0.20	0.20	0.20	0.21	0.21
t_{zd}	0.20	0.20	0.21	0.21	0.22	0.22	0.23	0.23
t_{od}	0.74	0.74	0.75	0.75	0.76	0.76	0.78	0.78
Power (µW/MHz)								
Power_read	74.32	86.46	99.19	111.66	130.21	140.50	163.91	174.70
Power_write	74.08	87.95	99.02	113.74	130.12	143.22	165.47	177.90
Power_standby	18.79	25.42	23.16	31.12	27.89	37.19	31.08	41.49
Area (µm)								
Width	337.28	337.28	456.04	456.04	574.80	574.80	693.56	693.56
Height	210.60	300.76	287.40	377.56	441.00	531.16	594.60	684.76

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

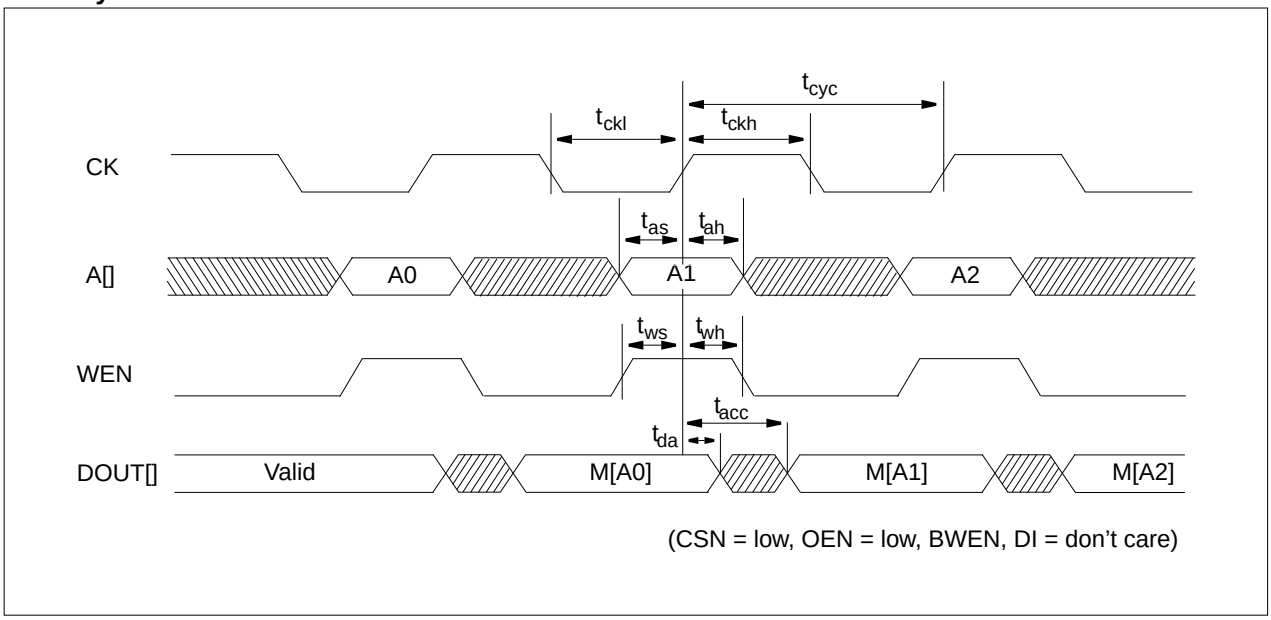
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**8192**	**8192**	**12288**	**12288**	**16384**	**16384**	**32768**
bpw	**12**	**12**	**14**	**14**	**16**	**16**	**16**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.37	3.15	3.71	3.37	3.74	3.60	4.11
t_{ckl}	0.78	0.78	0.78	0.78	0.78	0.78	0.78
t_{ckh}	0.41	0.41	0.41	0.41	0.41	0.41	0.41
t_{as}	0.57	0.59	0.58	0.59	0.59	0.59	0.59
t_{ah}	0.23	0.23	0.23	0.23	0.23	0.23	0.23
t_{cs}	0.44	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.17	0.17	0.17	0.17	0.16	0.16	0.16
t_{dh}	0.19	0.19	0.20	0.19	0.20	0.20	0.20
t_{ws}	0.39	0.38	0.39	0.38	0.39	0.38	0.35
t_{wh}	0.22	0.22	0.22	0.22	0.22	0.22	0.22
t_{bws}	0.17	0.24	0.17	0.25	0.16	0.26	0.31
t_{bwh}	0.17	0.17	0.19	0.18	0.20	0.18	0.18
t_{acc}	3.00	2.78	3.33	3.00	3.37	3.24	3.74
t_{da}	2.37	2.04	2.69	2.24	2.72	2.45	2.85
t_{dz}	0.22	0.22	0.22	0.22	0.23	0.23	0.23
t_{zd}	0.24	0.24	0.24	0.24	0.25	0.25	0.25
t_{od}	0.79	0.79	0.80	0.80	0.81	0.81	0.81
Power (µW/MHz)							
Power_read	196.64	207.56	248.73	244.94	281.66	284.00	324.94
Power_write	201.29	211.70	253.62	252.35	294.27	295.71	340.72
Power_standby	35.98	48.26	2.662	2.681	45.73	62.11	65.44
Area (µm)							
Width	812.32	812.32	931.08	931.08	1049.84	1049.84	1049.84
Height	748.20	838.36	1055.40	1145.56	1362.60	1452.76	2681.56

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

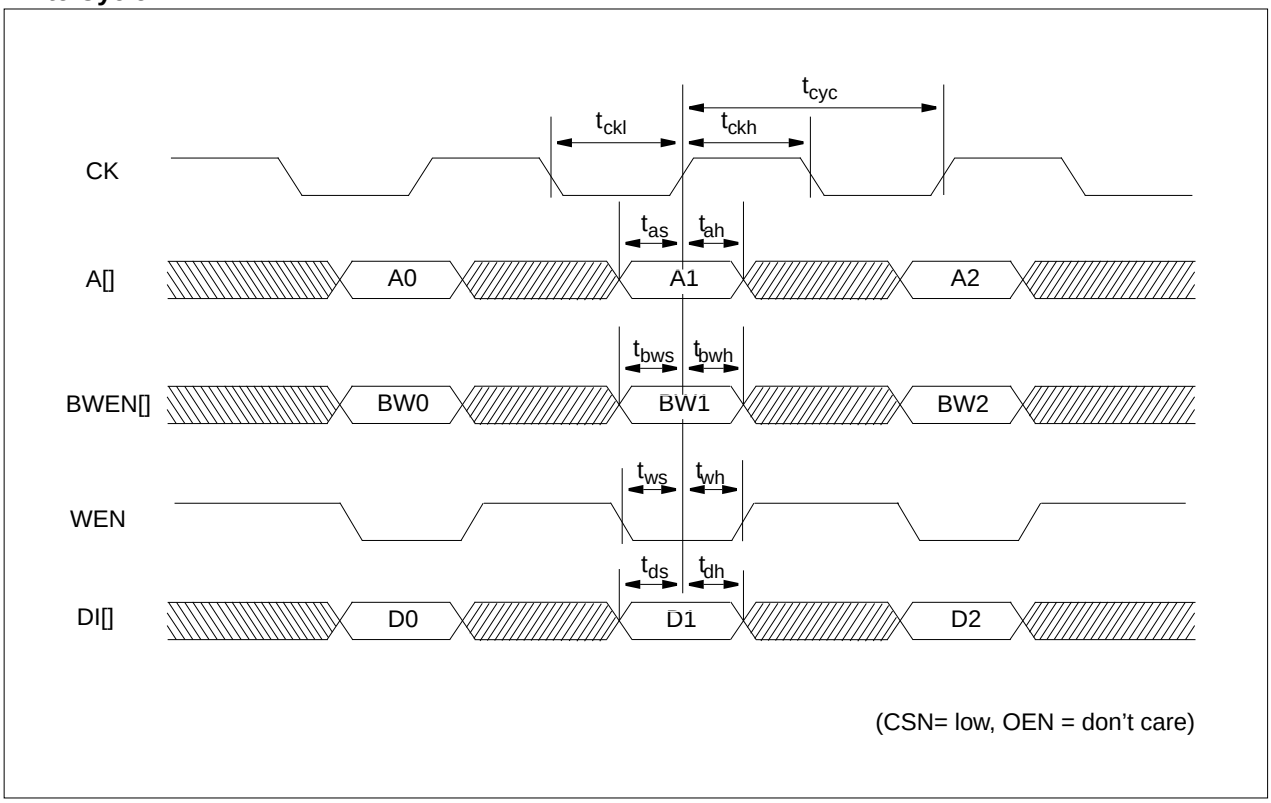
Timing Diagrams

Read Cycle



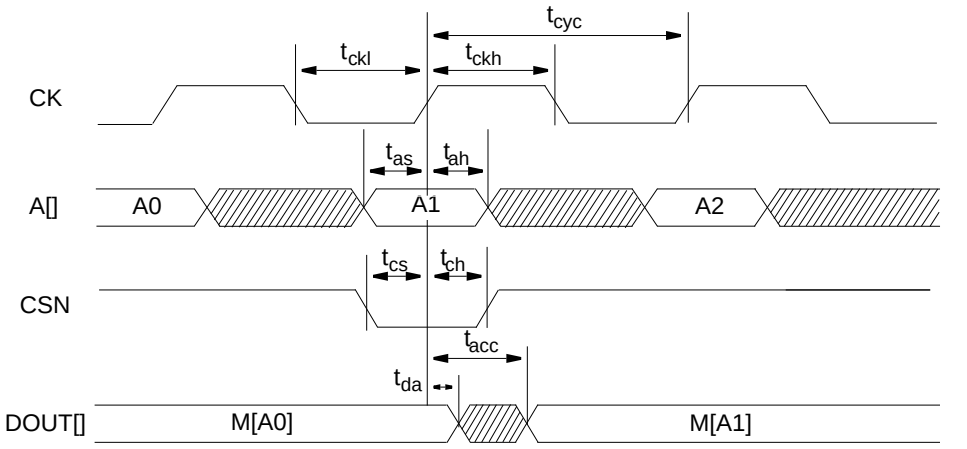
(CSN = low, OEN = low, BWEN, DI = don't care)

Write Cycle



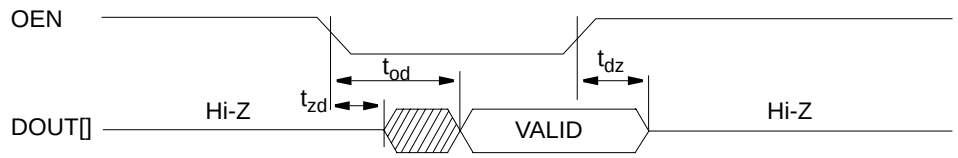
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



(OEN = low, WEN = high, BWEN, DI = don't care)

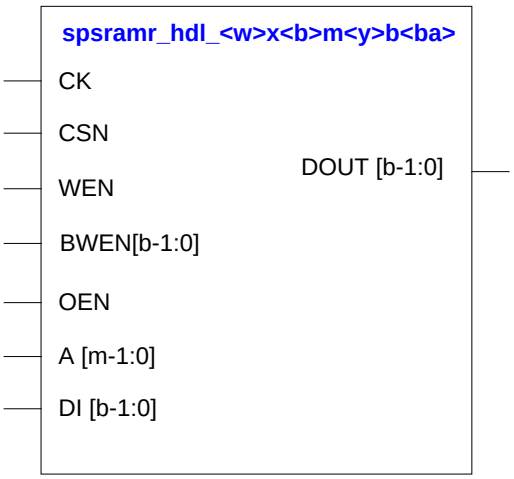
OEN-Controlled Output Enable



(CSN, CK, A, WEN, BWEN, DI = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bit per word.
3. Ymux (y) is one of the column mux types.
4. Banks(ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-capacity application
- Heuristic row-redundancy available
- Bit-write capability
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Near zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Dual-bank scheme available
- 64Kbits ~ 1Mbits capacity
- 2K ~ 32K number of words
- 8 ~ 128 number of bits per word

Function Description

SPSRAMR_HDL is a repairable single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMR_HDL is intended for use in high-capacity applications. Basically, its functionality is exactly same as SPSRAMBW_HDL. Each bit of BWEN[] enables or disable the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data bytes or bits in DI[], which their corresponding bit(s) in BWEN[] are low, are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM_HDL. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAMR_HDL Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L/H	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

SPSRAMR_HDL

Single-Port Synchronous Static RAM with Redundancy

Parameter Description

SPSRAMR_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	ba = 1	Min	2048	4096	8192
		Max	4096	8192	16384
		Step	64	128	256
	ba = 2	Min	4096	8192	16384
		Max	8192	16384	32768
		Step	128	256	512
Bpw (b)		Min	32	16	8
		Max	128	64	32
		Step	1	1	1

Pin Descriptions

Name	Type	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN[]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A[]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI[]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT[]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

(Unit = SL)

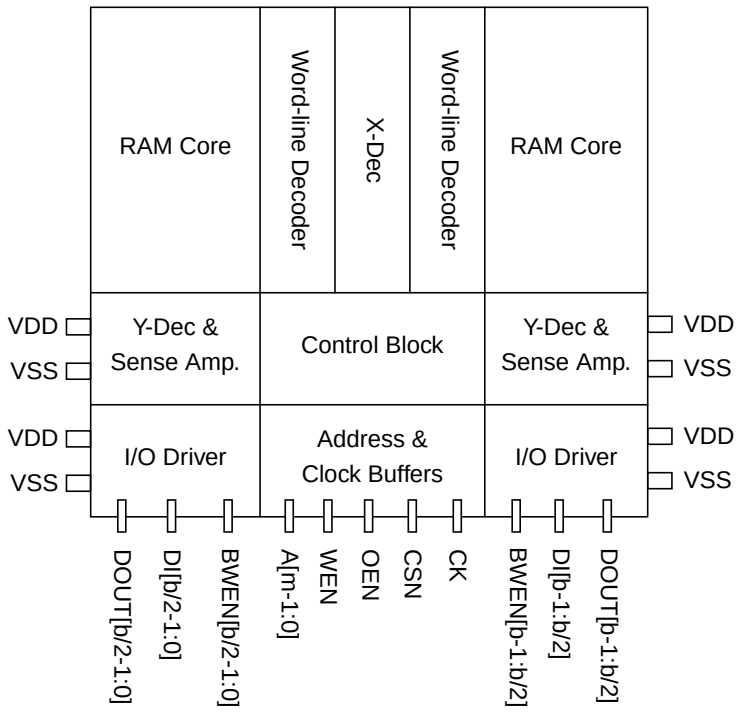
CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
8.1054	1.8946	1.9699	2.1706	3.1744	2.0452	2.1205	5.7591

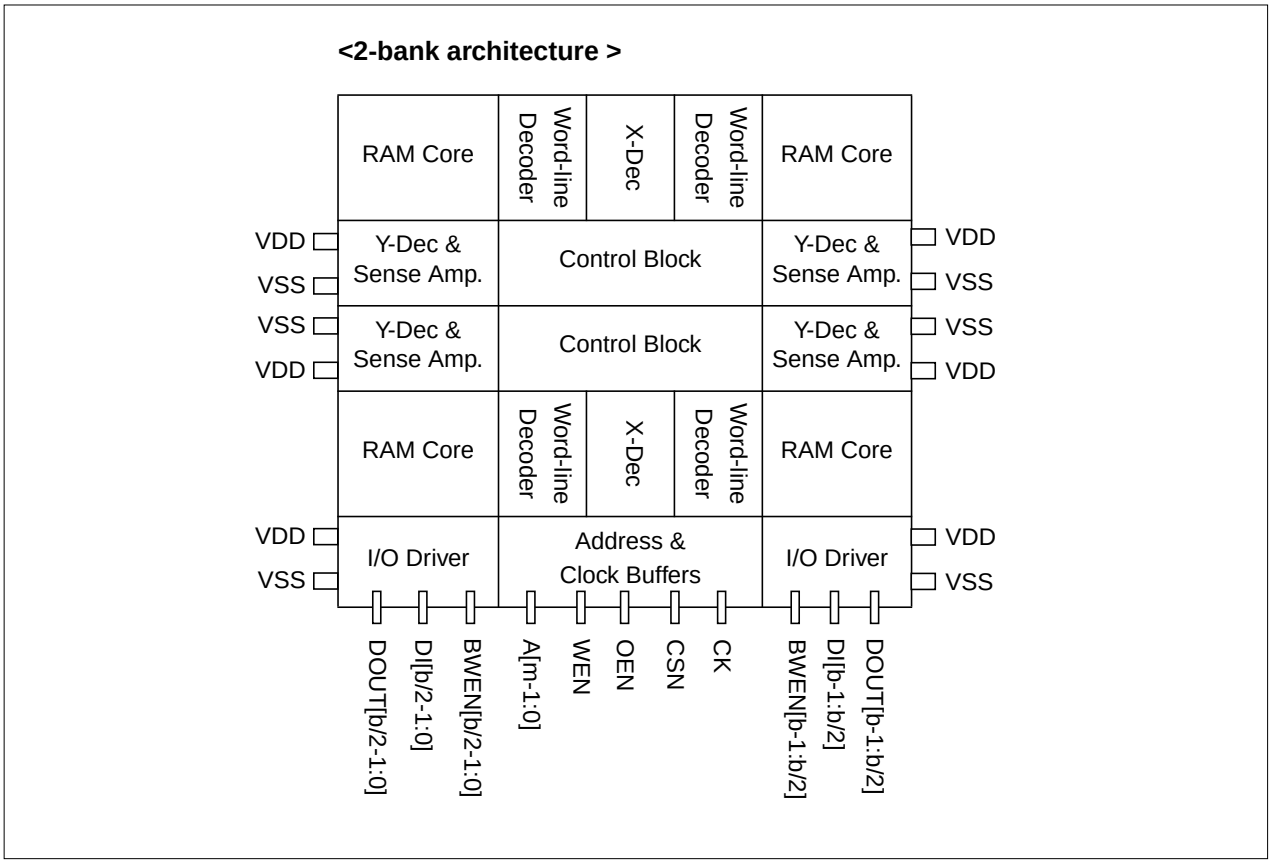
NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank

Block Diagrams

SPSRAMR_HDL has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from SPSRAMR_HDL compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the power ports are located on the middle-edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the power ports are located on the top-edge, the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>





Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in SPSRAMR_HDL is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAMR_HDL.

4. A byte-write or word-write operation with SPSRAMR_HDL. Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPSRAM_HDL. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

5. Power reduction during standby mode. The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep all signals stable while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{bws}	BWEN setup time
t_{bwh}	BWEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations.		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**2048**	**4096**	**2048**	**4096**	**04096**	**8192**	**4096**	**8192**
bpw	**32**	**32**	**64**	**64**	**64**	**64**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	3.78	3.96	3.84	4.02	4.17	4.53	4.31	4.65
t_{ckl}	0.58	0.53	0.56	0.53	0.55	0.53	0.57	0.53
t_{ckh}	0.82	0.82	0.82	0.82	0.82	0.82	0.82	0.83
t_{as}	0.42	0.42	0.42	0.43	0.42	0.42	0.42	0.41
t_{ah}	0.17	0.17	0.17	0.17	0.17	0.17	0.17	0.18
t_{cs}	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.22	0.21	0.16	0.17	0.17	0.16	0.08	0.06
t_{dh}	0.23	0.23	0.32	0.31	0.31	0.32	0.49	0.50
t_{ws}	0.31	0.35	0.32	0.35	0.32	0.39	0.31	0.39
t_{wh}	0.24	0.24	0.22	0.22	0.24	0.20	0.24	0.25
t_{bws}	0.26	0.26	0.21	0.21	0.22	0.21	0.13	0.11
t_{bwh}	0.25	0.25	0.34	0.34	0.34	0.36	0.53	0.52
t_{acc}	3.31	3.48	3.38	3.54	3.70	4.01	3.84	4.13
t_{da}	2.97	3.03	2.99	3.05	3.31	3.44	3.37	3.50
t_{dz}	0.27	0.27	0.31	0.31	0.31	0.31	0.38	0.38
t_{zd}	0.37	0.37	0.41	0.41	0.41	0.41	0.48	0.48
t_{od}	0.56	0.56	0.65	0.64	0.63	0.63	0.82	0.82
Power (µW/MHz)								
Power_read	103.40	146.19	175.32	243.91	182.66	255.72	333.53	460.87
Power_write	178.52	231.23	329.56	418.60	435.23	549.83	844.90	1054.60
Power_standby	57.77	92.59	107.23	173.57	107.14	210.35	205.93	408.42
Area (µm)								
Width	627.88	627.88	1117.16	1117.16	1117.16	1117.16	2095.72	2095.72
Height	772.90	1494.16	779.30	1506.96	1400.10	2748.56	1425.70	2799.70

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**4096**	**8192**	**4096**	**8192**	**8192**	**16384**	**8192**	**16384**
bpw	**16**	**16**	**32**	**32**	**32**	**32**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	3.81	3.99	3.87	4.05	4.22	4.56	4.35	4.70
t_{ckl}	0.53	0.53	0.53	0.53	0.53	0.53	0.53	0.53
t_{ckh}	0.82	0.81	0.82	0.82	0.82	0.82	0.82	0.82
t_{as}	0.43	0.42	0.43	0.42	0.42	0.42	0.42	0.43
t_{ah}	0.17	0.16	0.17	0.16	0.17	0.17	0.17	0.17
t_{cs}	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.23	0.22	0.19	0.18	0.19	0.18	0.11	0.11
t_{dh}	0.21	0.21	0.29	0.28	0.29	0.29	0.43	0.43
t_{ws}	0.32	0.36	0.32	0.36	0.32	0.39	0.32	0.40
t_{wh}	0.17	0.24	0.17	0.22	0.22	0.22	0.17	0.17
t_{bws}	0.27	0.27	0.23	0.23	0.23	0.22	0.15	0.15
t_{bwh}	0.24	0.24	0.31	0.31	0.32	0.32	0.47	0.47
t_{acc}	3.33	3.52	3.39	3.58	3.71	4.05	3.84	4.16
t_{da}	2.95	3.04	2.99	3.07	3.31	3.44	3.38	3.50
t_{dz}	0.26	0.26	0.29	0.29	0.29	0.29	0.36	0.36
t_{zd}	0.36	0.36	0.39	0.39	0.39	0.39	0.46	0.46
t_{od}	0.54	0.54	0.61	0.61	0.62	0.62	0.77	0.77
Power (µW/MHz)								
Power_read	125.20	212.71	219.73	377.71	224.43	386.05	417.48	722.38
Power_write	178.76	286.51	329.06	527.94	383.05	596.11	738.40	1144.70
Power_standby	40.03	66.11	71.73	120.35	71.76	138.97	135.30	265.79
Area (µm)								
Width	627.88	627.88	1117.16	1117.16	1117.16	1117.16	2095.72	2095.72
Height	772.90	1494.16	779.30	1506.96	1400.10	2748.56	1425.70	2799.70

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode.

Reference Table

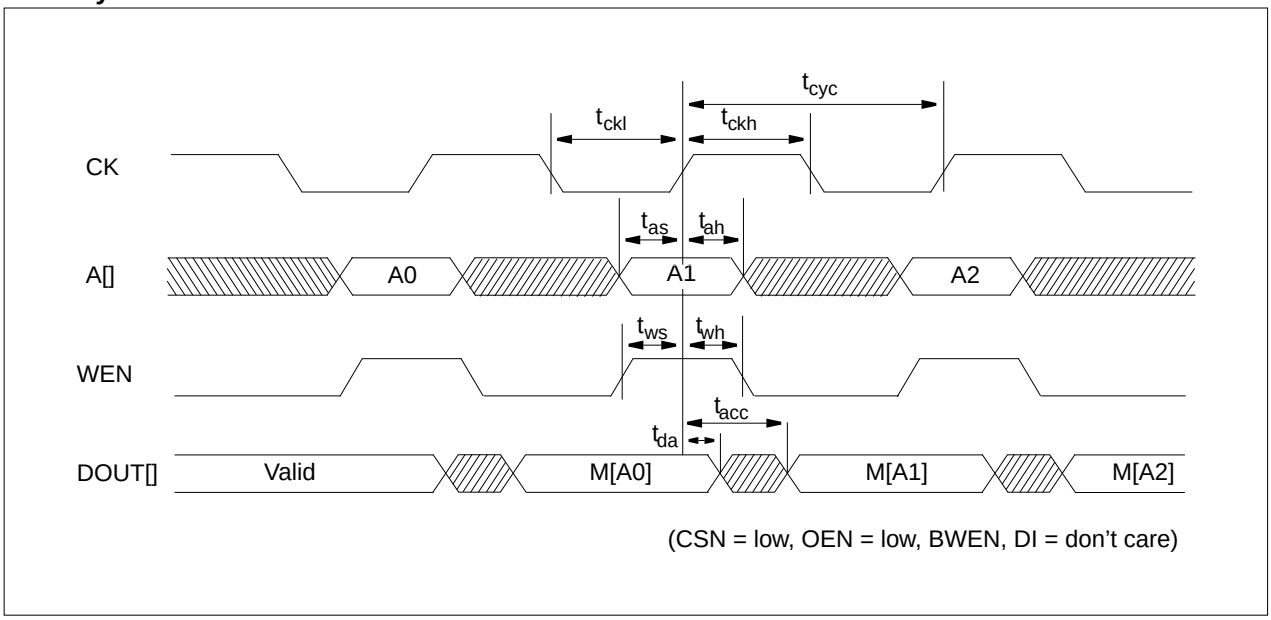
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters								
words	**8192**	**16384**	**8192**	**16384**	**16384**	**32768**	**16384**	**32768**
bpw	**8**	**8**	**16**	**16**	**16**	**16**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)								
t_{cyc}	3.85	4.05	3.91	4.11	4.26	4.63	4.38	4.78
t_{ckl}	0.53	0.53	0.53	0.53	0.53	0.54	0.53	0.56
t_{ckh}	0.82	0.82	0.82	0.82	0.82	0.82	0.82	0.83
t_{as}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{ah}	0.17	0.17	0.17	0.17	0.17	0.17	0.17	0.18
t_{cs}	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.24	0.22	0.20	0.19	0.20	0.19	0.13	0.11
t_{dh}	0.21	0.21	0.27	0.27	0.27	0.27	0.40	0.41
t_{ws}	0.32	0.35	0.32	0.35	0.32	0.39	0.31	0.38
t_{wh}	0.24	0.24	0.22	0.24	0.19	0.20	0.24	0.25
t_{bws}	0.27	0.27	0.24	0.24	0.24	0.24	0.17	0.16
t_{bwh}	0.23	0.25	0.29	0.31	0.30	0.30	0.42	0.43
t_{acc}	3.37	3.60	3.44	3.65	3.75	4.12	3.88	4.25
t_{da}	2.95	3.03	2.99	3.06	3.30	3.45	3.37	3.52
t_{dz}	0.26	0.26	0.29	0.29	0.29	0.29	0.35	0.35
t_{zd}	0.36	0.36	0.39	0.39	0.39	0.39	0.44	0.44
t_{od}	0.53	0.53	0.60	0.60	0.60	0.60	0.73	0.75
Power (µW/MHz)								
Power_read	114.10	201.15	197.72	355.38	201.03	362.82	370.96	676.33
Power_write	146.88	249.94	264.42	454.06	292.76	491.06	556.70	933.86
Power_standby	30.83	52.14	53.32	92.63	53.32	102.15	98.34	192.12
Area (µm)								
Width	627.88	627.88	1117.16	1117.16	1117.16	1117.16	2095.72	2095.72
Height	772.90	1494.16	779.30	1506.96	1400.10	2748.56	1425.70	2799.70

NOTE: Standby power is measured on condition that other signals are in normal operation while CSN is in disable mode.

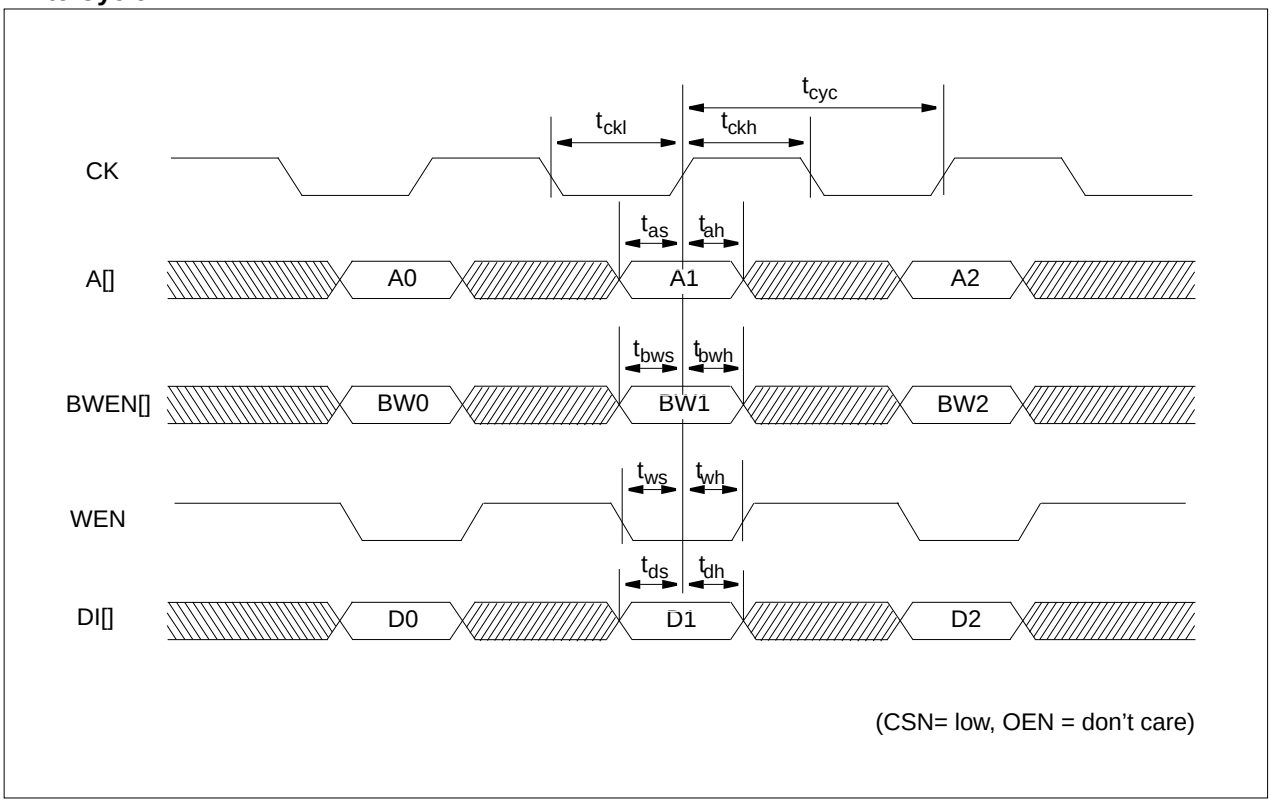
Timing Diagrams

Read Cycle



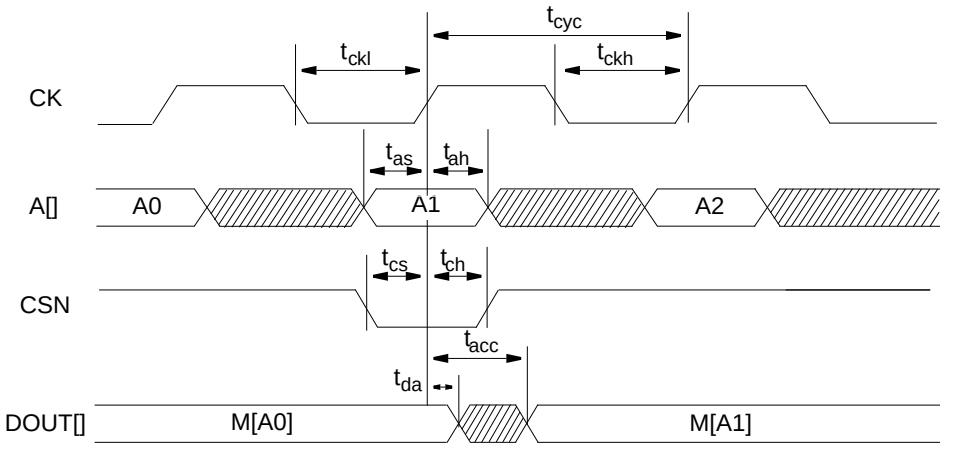
(CSN = low, OEN = low, BWEN, DI = don't care)

Write Cycle



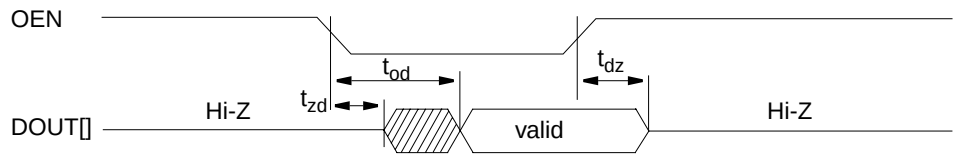
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



(OEN = low, WEN = high, BWEN, DI = don't care)

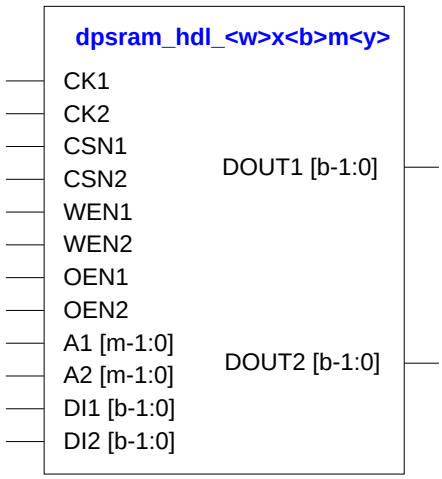
OEN-Controlled Output Enable



(CSN, CK, A, WEN, BWEN, DI = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DPSRAM_HDL is a dual-port synchronous static RAM which is provided as a compiler. DPSRAM_HDL is intended for use in high-density applications. Each port is fully independent. On the rising edge of CK1(CK2), the write cycle is initiated when WEN1 (WEN2) is low and CSN1 (CSN2) is low. The data on DI1[] (DI2[]) is written into the memory location specified on A1[](A2[]). During the write cycle, DOUT1[] (DOUT2[]) remains stable. On the rising edge of CK, the read cycle is initiated when WEN1 (WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[] (DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[](A2[]) and DI1[] (DI2[]) are disabled, data stored in the memory is retained and DOUT1[] (DOUT2[]) remains stable. When OEN1 (OEN2) is high, DOUT1[] (DOUT2[]) is placed in a high-impedance state.

DPSRAM_HDL Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

DPSRAM_HDL

High-Density Dual-Port Synchronous Static RAM

Parameter Description

DPSRAM_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	32	64	128	256
	Max	2048	4096	8192	16384
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [ ] A2 [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [ ] DI2 [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [ ] DOUT2 [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

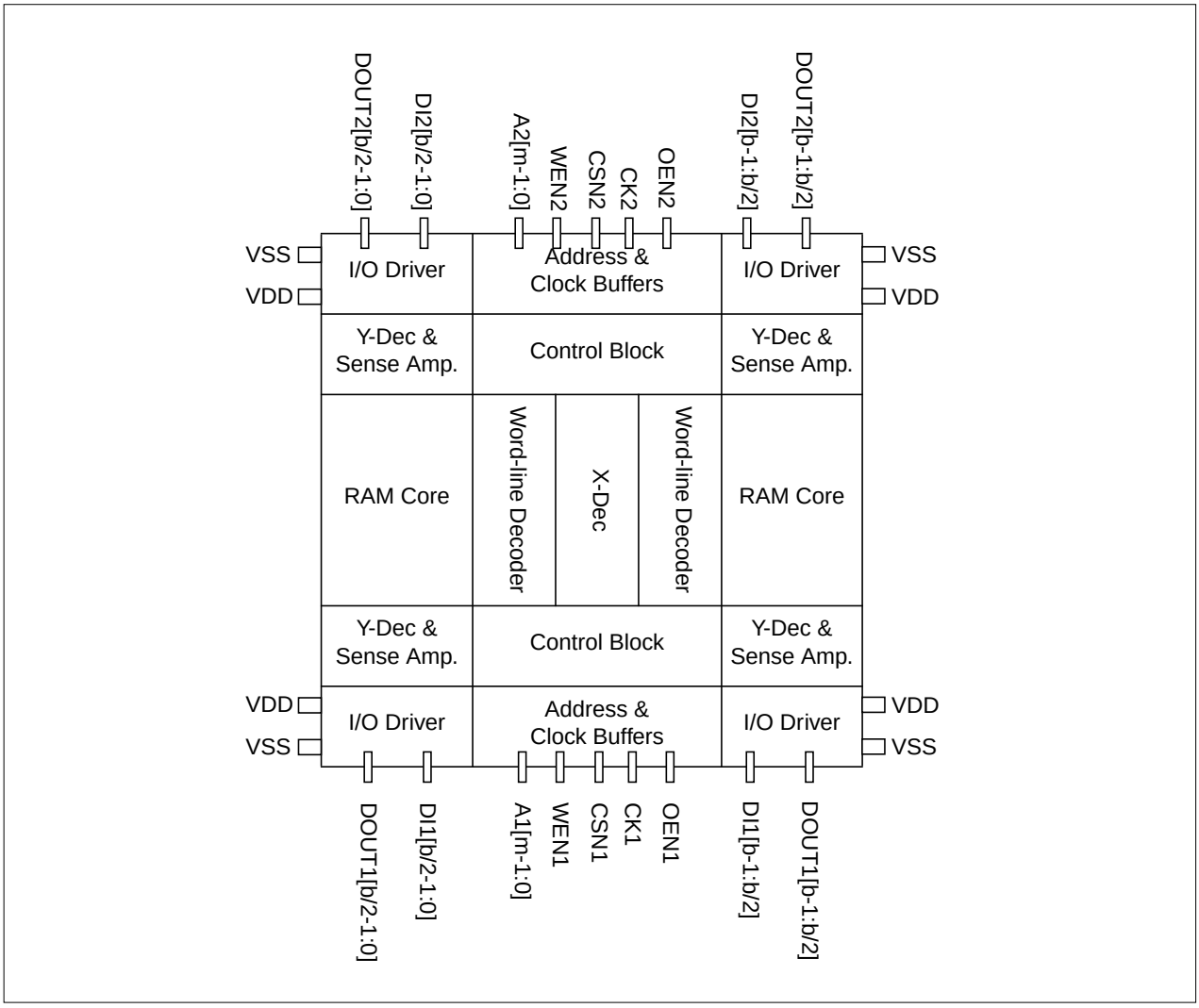
(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT
20.39	2.95	2.95	7.11	2.95	3.35	21.78

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagram

DPSRAM_HDL supports only 1-bank architecture. The power ports are located on the top edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAM_HDL has two symmetrical ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



Application Notes

1. Permitting over-the-cell routing
In chip-level layout, over-the-cell routing in DPSRAM_HDL is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAM_HDL.

4. Contention mode in same address access
In DPSRAM_HDL, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAM_HDL has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

5. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock-to-clock setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

DPSRAM_HDL

High-Density Dual-Port Synchronous Static RAM

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**128**	**256**	**512**	**768**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**	**80**	**96**	**112**	**128**
Timing (ns)								
t_{cyc}	2.60	2.67	2.78	2.97	3.11	3.27	3.58	3.63
t_{ckl}	0.99	0.95	0.92	0.88	0.88	0.85	0.81	0.78
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{cc}	0.93	1.00	1.10	1.28	1.40	1.58	1.90	1.99
t_{as}	0.51	0.51	0.51	0.52	0.51	0.50	0.48	0.45
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.81	0.77	0.73	0.70	0.69	0.66	0.63	0.60
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.45	0.46	0.46	0.46	0.47	0.47	0.48
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.32	2.39	2.51	2.69	2.83	2.99	3.30	3.35
t_{da}	2.19	2.25	2.35	2.53	2.64	2.78	3.05	3.08
t_{dz}	0.48	0.52	0.56	0.59	0.59	0.62	0.66	0.69
t_{zd}	0.59	0.61	0.64	0.66	0.68	0.71	0.75	0.79
t_{od}	0.72	0.76	0.79	0.83	0.84	0.87	0.90	0.93
Power (µW/MHz)								
Power_read	85.12	143.24	204.85	274.26	354.25	430.52	526.29	604.69
Power_write	91.14	158.37	232.43	322.29	425.64	530.99	679.63	826.61
Power_standby	30.47	47.91	66.63	87.95	110.35	131.36	157.27	183.05
Area (µm)								
Width	551.56	897.16	1242.76	1588.36	2011.96	2357.56	2703.16	3048.76
Height	196.56	220.16	267.36	361.76	454.04	548.30	738.82	927.60

NOTES:

1. In power consumption of DPSRAM_HDL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**256**	**512**	**1024**	**1536**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**	**40**	**48**	**56**	**64**
Timing (ns)								
t_{cyc}	2.62	2.69	2.81	2.99	3.13	3.30	3.60	3.65
t_{ckl}	0.99	0.95	0.92	0.88	0.88	0.85	0.52	0.79
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{cc}	0.93	1.00	1.10	1.28	1.40	1.58	1.90	1.99
t_{as}	0.51	0.51	0.51	0.52	0.51	0.50	0.48	0.45
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.56	0.56	0.56	0.57	0.56	0.56	0.56	0.56
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.81	0.77	0.74	0.70	0.70	0.67	0.64	0.61
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.45	0.46	0.46	0.46	0.47	0.47	0.48
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.34	2.42	2.53	2.71	2.85	3.02	3.32	3.37
t_{da}	2.21	2.27	2.37	2.55	2.66	2.80	3.07	3.10
t_{dz}	0.48	0.52	0.55	0.59	0.59	0.62	0.65	0.68
t_{zd}	0.59	0.61	0.64	0.66	0.67	0.71	0.74	0.78
t_{od}	0.72	0.76	0.79	0.82	0.83	0.87	0.90	0.93
Power (µW/MHz)								
Power_read	78.94	130.90	186.34	249.50	322.74	390.88	478.87	549.35
Power_write	77.66	130.73	189.00	259.15	341.26	421.80	533.41	635.85
Power_standby	25.85	38.65	52.75	69.44	88.26	104.91	126.45	148.04
Area (µm)								
Width	551.56	897.16	1242.76	1588.36	2011.96	2357.56	2703.16	3048.76
Height	196.56	220.16	267.36	361.76	454.04	548.30	738.82	927.60

NOTES:

1. In power consumption of DPSRAM_HDL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DPSRAM_HDL

High-Density Dual-Port Synchronous Static RAM

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**512**	**1024**	**2048**	**3072**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**	**20**	**24**	**28**	**32**
Timing (ns)								
t_{cyc}	2.66	2.74	2.85	3.03	3.17	3.34	3.64	3.69
t_{ckl}	0.99	0.95	0.92	0.89	0.88	0.85	0.82	0.79
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{cc}	0.93	1.00	1.10	1.28	1.40	1.58	1.90	1.99
t_{as}	0.51	0.51	0.51	0.52	0.51	0.50	0.48	0.45
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.81	0.77	0.74	0.70	0.70	0.67	0.64	0.61
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.45	0.46	0.46	0.46	0.47	0.47	0.48
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.38	2.46	2.57	2.75	2.89	3.06	3.36	3.41
t_{da}	2.25	2.32	2.41	2.59	2.70	2.84	3.11	3.14
t_{dz}	0.48	0.52	0.55	0.59	0.59	0.62	0.65	0.68
t_{zd}	0.59	0.62	0.64	0.66	0.67	0.71	0.74	0.78
t_{od}	0.72	0.75	0.79	0.82	0.83	0.86	0.89	0.92
Power (µW/MHz)								
Power_read	76.55	124.80	176.52	235.95	306.04	370.88	455.52	522.06
Power_write	71.82	116.86	166.27	225.58	296.70	364.14	457.15	536.50
Power_standby	23.63	33.56	44.78	64.01	74.97	88.83	107.67	126.50
Area (µm)								
Width	551.56	897.16	1242.76	1588.36	2011.96	2357.56	2703.16	3048.76
Height	196.56	220.16	267.36	361.76	454.04	548.30	738.82	927.60

NOTES:

1. In power consumption of DPSRAM_HDL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

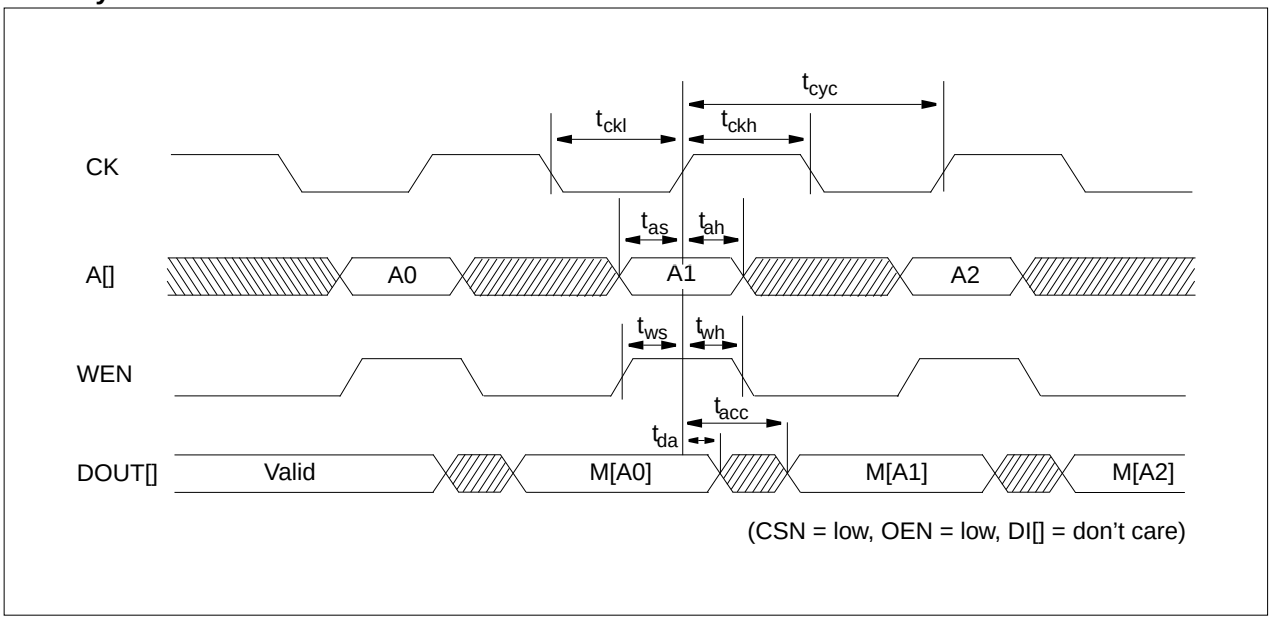
Parameters								
words	**512**	**1024**	**2048**	**4096**	**6144**	**8192**	**12288**	**16384**
bpw	**2**	**4**	**6**	**8**	**10**	**12**	**14**	**16**
Timing (ns)								
t_{cyc}	2.74	2.81	2.92	3.11	3.25	3.42	3.72	3.77
t_{ckl}	0.99	0.96	0.92	0.89	0.88	0.86	0.84	0.82
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{cc}	0.92	0.99	1.10	1.28	1.41	1.58	1.90	1.99
t_{as}	0.51	0.51	0.51	0.52	0.51	0.50	0.48	0.45
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.81	0.77	0.74	0.70	0.69	0.68	0.66	0.64
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.45	0.46	0.46	0.46	0.47	0.48	0.48
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.45	2.53	2.64	2.83	2.97	3.14	3.44	3.49
t_{da}	2.33	2.39	2.49	2.66	2.77	2.91	3.18	3.21
t_{dz}	0.48	0.52	0.55	0.59	0.60	0.62	0.65	0.68
t_{zd}	0.60	0.62	0.64	0.66	0.66	0.70	0.74	0.78
t_{od}	0.72	0.75	0.79	0.82	0.84	0.87	0.89	0.92
Power (µW/MHz)								
Power_read	76.14	122.30	171.91	229.17	298.21	361.04	443.86	508.62
Power_write	70.22	110.68	155.18	208.77	274.68	335.43	418.81	486.29
Power_standby	22.75	31.11	40.76	53.00	68.33	80.78	98.25	115.73
Area (µm)								
Width	551.56	897.16	1242.76	1588.36	2011.96	2357.56	2703.16	3048.76
Height	196.56	220.16	267.36	361.76	454.04	548.30	738.82	927.60

NOTES:

1. In power consumption of DPSRAM_HDL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

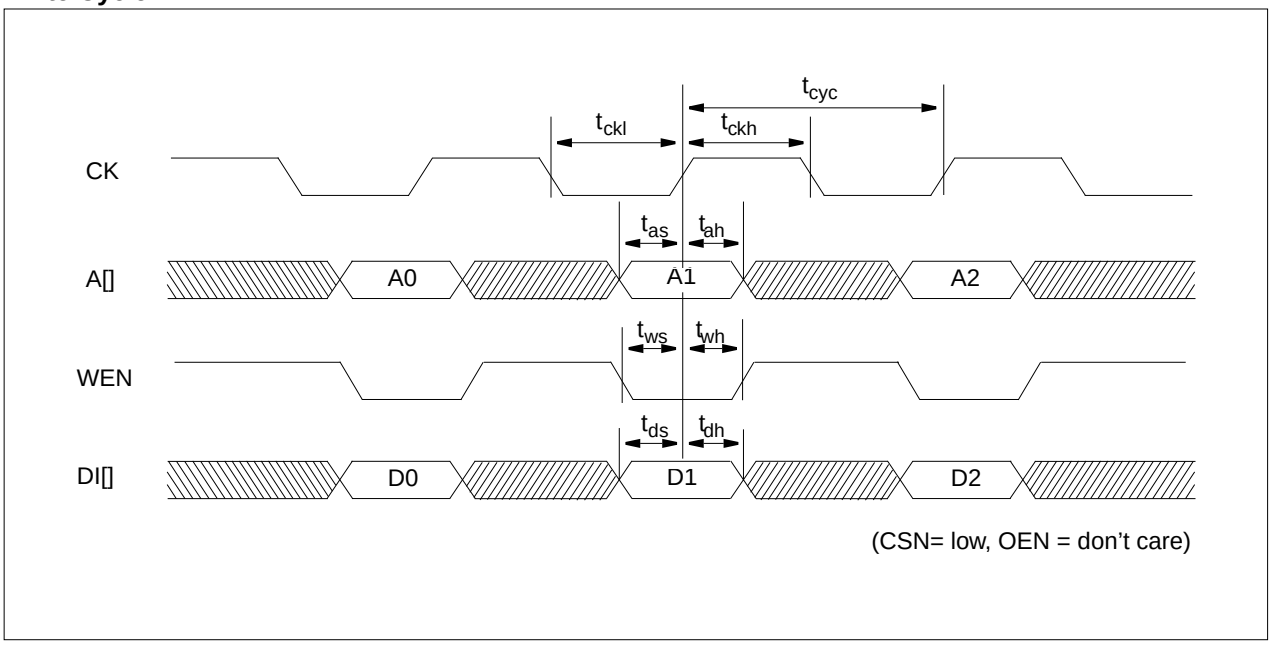
Timing Diagrams

Read Cycle



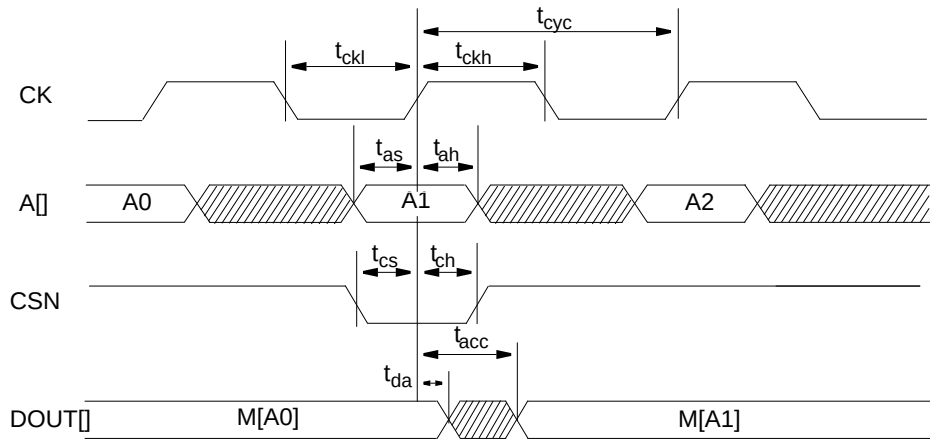
(CSN = low, OEN = low, DI[] = don't care)

Write Cycle



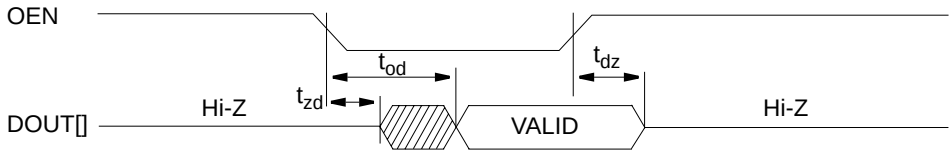
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



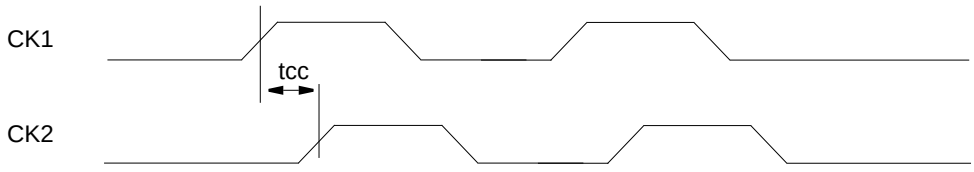
(OEN = low, WEN = high, DI[] = don't care)

OEN-Controlled Output Enable



(CSN, CK, A[], WEN, DI[] = don't care)

Contention Mode



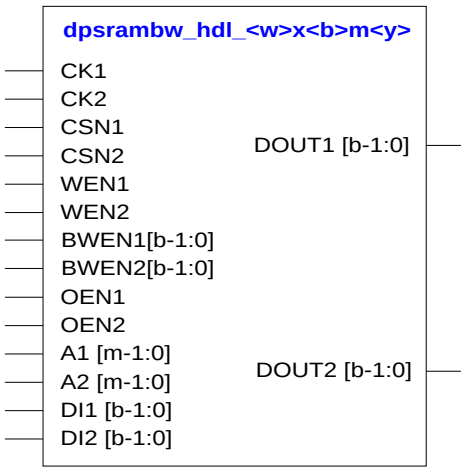
(A1[] = A2[])

NOTE: "don't care" means the condition that these pins are in normal operation mode.

DPSRAMBW_HDL

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Logic Symbol



NOTES:

1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DPSRAMBW_HDL is a dual-port synchronous static RAM with bit-write capability which is provided as a compiler. DPSRAMBW_HDL is intended for use in high-density applications. Each port is fully independent. Basically, its functionality is exactly same as DPSRAM_HDL except a bit-write operation which is controlled by BWEN1[](BWEN2[]), named bit-write enable signal bus. Each bit of BWEN1[](BWEN2[]) enables or disable the write operation of its corresponding bit in DI1[](DI2[]). On the rising edge of CK1(CK2), the write cycle is initiated when WEN1(WEN2) is low and CSN1(CSN2) is low. The data bits in DI1[](DI2[]), which their corresponding bit(s) in BWEN1[](BWEN2[]) are low, are written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEN2[]) are high, any data in DI1[](DI2[]) are not written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEM2[]) are low, the data in DI1[](DI2[]) are written into the memory location specified on A1[](A2[]), which is exactly same as the write operation in DPSRAMBW_HDL. During the write cycle, DOUT1[](DOUT2[]) remains stable. On the rising edge of CK1(CK2), the read cycle is initiated when WEN1(WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[](DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[](A2[]) and DI1[](DI2[]) are disabled, data stored in the memory is retained and DOUT1[](DOUT2[]) remains stable. When OEN1(OEN2) is high, DOUT1[](DOUT2[]) is placed in a high-impedance state.

DPSRAMBW_HDL Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	BWEN1 BWEN2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	All L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	All H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

Parameter Description

DPSRAMBW_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	32	64	128	256
	Max	2048	4096	8192	16384
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are presented at DOUT.
BWEN1[ ] BWEN2[ ]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [ ] A2 [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [ ] DI2 [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [ ] DOUT2 [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT
20.39	2.95	2.95	7.11	2.95	3.35	3.35	21.78

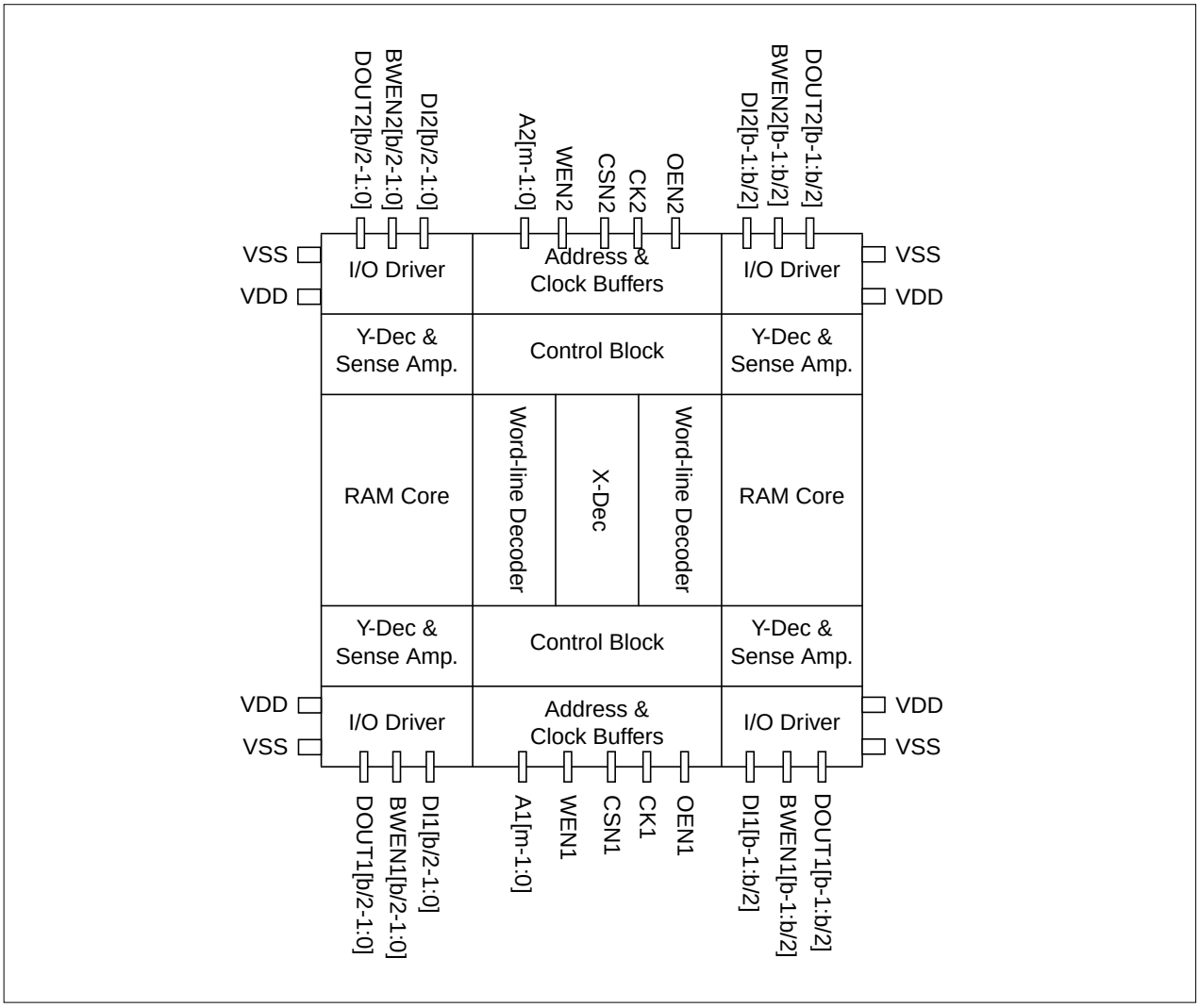
NOTE: Each pin's capacitance is exactly same regardless of available mux types.

DPSRAMBW_HDL

High-Density Dual-Port Synchronous Static RAM Bit-Write

Block Diagram

DPSRAMBW_HDL supports only 1-bank architecture. The power ports are located on the top edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAMBW_HDL has two symmetrical ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



Application Notes

1. Permitting over-the-cell routing
In chip-level layout, over-the-cell routing in DPSRAMBW_HDL is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAMBW_HDL.

4. Contention mode in same address access
In DPSRAMBW_HDL, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAMBW_HDL has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

5. A byte-write or word-write operation with DPSRAMBW_HDL
Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as DPSRAM_HDL. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

6. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

DPSRAMBW_HDL

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock-to-clock setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{bws}	BWEN setup time	t_{bwh}	BWEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (µW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations.		
Definition for Area (µm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**128**	**256**	**512**	**768**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**	**80**	**96**	**112**	**128**
Timing (ns)								
t_{cyc}	2.60	2.67	2.78	2.97	3.11	3.27	3.58	3.63
t_{ckl}	0.99	0.95	0.92	0.88	0.88	0.85	0.81	0.78
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{cc}	0.93	1.00	1.10	1.28	1.40	1.58	1.90	1.99
t_{as}	0.51	0.51	0.51	0.52	0.51	0.50	0.48	0.45
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.81	0.77	0.73	0.70	0.69	0.66	0.63	0.60
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.45	0.46	0.46	0.46	0.47	0.47	0.48
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.77	0.74	0.70	0.66	0.66	0.63	0.59	0.56
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.32	2.39	2.51	2.69	2.83	2.99	3.30	3.35
t_{da}	2.19	2.25	2.35	2.53	2.64	2.78	3.05	3.08
t_{dz}	0.48	0.52	0.56	0.59	0.59	0.62	0.66	0.69
t_{zd}	0.59	0.61	0.64	0.66	0.68	0.71	0.75	0.79
t_{od}	0.72	0.76	0.79	0.83	0.84	0.87	0.90	0.93
Power (µW/MHz)								
Power_read	89.07	151.14	216.71	290.07	373.98	454.24	553.97	636.24
Power_write	95.09	166.27	244.29	338.10	445.38	554.71	707.31	858.16
Power_standby	34.42	55.81	78.49	103.76	130.08	155.07	184.95	214.60
Area (µm)								
Width	551.56	897.16	1242.76	1588.36	2011.96	2357.56	2703.16	3048.76
Height	196.56	220.16	267.36	361.76	454.04	548.30	738.82	927.60

NOTES:

1. In power consumption of DPSRAMBW_HDL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DPSRAMBW_HDL

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**256**	**512**	**1024**	**1536**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**	**40**	**48**	**56**	**64**
Timing (ns)								
t_{cyc}	2.62	2.69	2.81	2.99	3.13	3.30	3.60	3.65
t_{ckl}	0.99	0.95	0.92	0.88	0.88	0.85	0.52	0.79
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{cc}	0.93	1.00	1.10	1.28	1.40	1.58	1.90	1.99
t_{as}	0.51	0.51	0.51	0.52	0.51	0.50	0.48	0.45
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.56	0.56	0.56	0.57	0.56	0.56	0.56	0.56
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.81	0.77	0.74	0.70	0.70	0.67	0.64	0.61
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.45	0.46	0.46	0.46	0.47	0.47	0.48
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.78	0.74	0.70	0.66	0.66	0.63	0.60	0.57
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.34	2.42	2.53	2.71	2.85	3.02	3.32	3.37
t_{da}	2.21	2.27	2.37	2.55	2.66	2.80	3.07	3.10
t_{dz}	0.48	0.52	0.55	0.59	0.59	0.62	0.65	0.68
t_{zd}	0.59	0.61	0.64	0.66	0.67	0.71	0.74	0.78
t_{od}	0.72	0.76	0.79	0.82	0.83	0.87	0.90	0.93
Power (µW/MHz)								
Power_read	80.92	134.86	192.27	257.42	332.62	402.73	492.70	565.13
Power_write	79.63	134.68	194.93	267.07	351.14	433.65	547.23	651.63
Power_standby	27.82	42.60	58.68	77.35	98.14	116.76	140.27	163.82
Area (µm)								
Width	551.56	897.16	1242.76	1588.36	2011.96	2357.56	2703.16	3048.76
Height	196.56	220.16	267.36	361.76	454.04	548.30	738.82	927.60

NOTES:

1. In power consumption of DPSRAMBW_HDL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**512**	**1024**	**2048**	**3072**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**	**20**	**24**	**28**	**32**
Timing (ns)								
t_{cyc}	2.66	2.74	2.85	3.03	3.17	3.34	3.64	3.69
t_{ckl}	0.99	0.95	0.92	0.89	0.88	0.85	0.82	0.79
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{cc}	0.93	1.00	1.10	1.28	1.40	1.58	1.90	1.99
t_{as}	0.51	0.51	0.51	0.52	0.51	0.50	0.48	0.45
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.81	0.77	0.74	0.70	0.70	0.67	0.64	0.61
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.45	0.46	0.46	0.46	0.47	0.47	0.48
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.78	0.74	0.70	0.67	0.66	0.63	0.60	0.57
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.38	2.46	2.57	2.75	2.89	3.06	3.36	3.41
t_{da}	2.25	2.32	2.41	2.59	2.70	2.84	3.11	3.14
t_{dz}	0.48	0.52	0.55	0.59	0.59	0.62	0.65	0.68
t_{zd}	0.59	0.62	0.64	0.66	0.67	0.71	0.74	0.78
t_{od}	0.72	0.75	0.79	0.82	0.83	0.86	0.89	0.92
Power (µW/MHz)								
Power_read	77.53	126.78	179.48	239.90	310.98	376.81	462.42	529.95
Power_write	72.81	118.83	169.23	229.53	301.65	370.06	464.05	544.39
Power_standby	24.62	35.53	47.74	62.54	79.91	94.75	114.57	134.39
Area (µm)								
Width	551.56	897.16	1242.76	1588.36	2011.96	2357.56	2703.16	3048.76
Height	196.56	220.16	267.36	361.76	454.04	548.30	738.82	927.60

NOTES:

1. In power consumption of DPSRAMBW_HDL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

DPSRAMBW_HDL

High-Density Dual-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

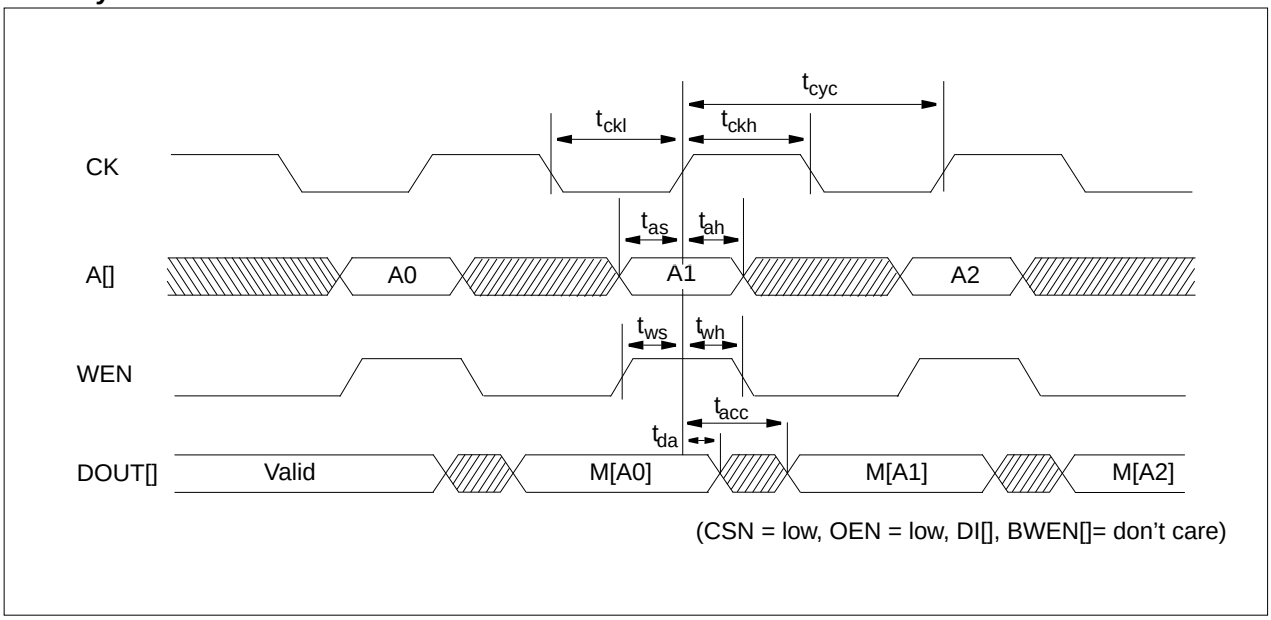
Parameters								
words	**512**	**1024**	**2048**	**4096**	**6144**	**8192**	**12288**	**16384**
bpw	**2**	**4**	**6**	**8**	**10**	**12**	**14**	**16**
Timing (ns)								
t_{cyc}	2.74	2.81	2.92	3.11	3.25	3.42	3.72	3.77
t_{ckl}	0.99	0.96	0.92	0.89	0.88	0.86	0.84	0.82
t_{ckh}	0.42	0.42	0.42	0.42	0.42	0.42	0.42	0.42
t_{cc}	0.92	0.99	1.10	1.28	1.41	1.58	1.90	1.99
t_{as}	0.51	0.51	0.51	0.52	0.51	0.50	0.48	0.45
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.81	0.77	0.74	0.70	0.69	0.68	0.66	0.64
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.44	0.45	0.46	0.46	0.46	0.47	0.48	0.48
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.78	0.74	0.70	0.67	0.66	0.63	0.60	0.57
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.45	2.53	2.64	2.83	2.97	3.14	3.44	3.49
t_{da}	2.33	2.39	2.49	2.66	2.77	2.91	3.18	3.21
t_{dz}	0.48	0.52	0.55	0.59	0.60	0.62	0.65	0.68
t_{zd}	0.60	0.62	0.64	0.66	0.66	0.70	0.74	0.78
t_{od}	0.72	0.75	0.79	0.82	0.84	0.87	0.89	0.92
Power (µW/MHz)								
Power_read	76.63	123.28	173.38	231.14	300.68	364.00	447.32	512.56
Power_write	70.72	11.67.	156.66	210.75	277.15	338.40	422.26	490.22
Power_standby	23.25	32.10	42.24	54.98	70.80	83.75	101.71	119.67
Area (µm)								
Width	551.56	897.16	1242.76	1588.36	2011.96	2357.56	2703.16	3048.76
Height	196.56	220.16	267.36	361.76	454.04	548.30	738.82	927.60

NOTES:

1. In power consumption of DPSRAMBW_HDL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

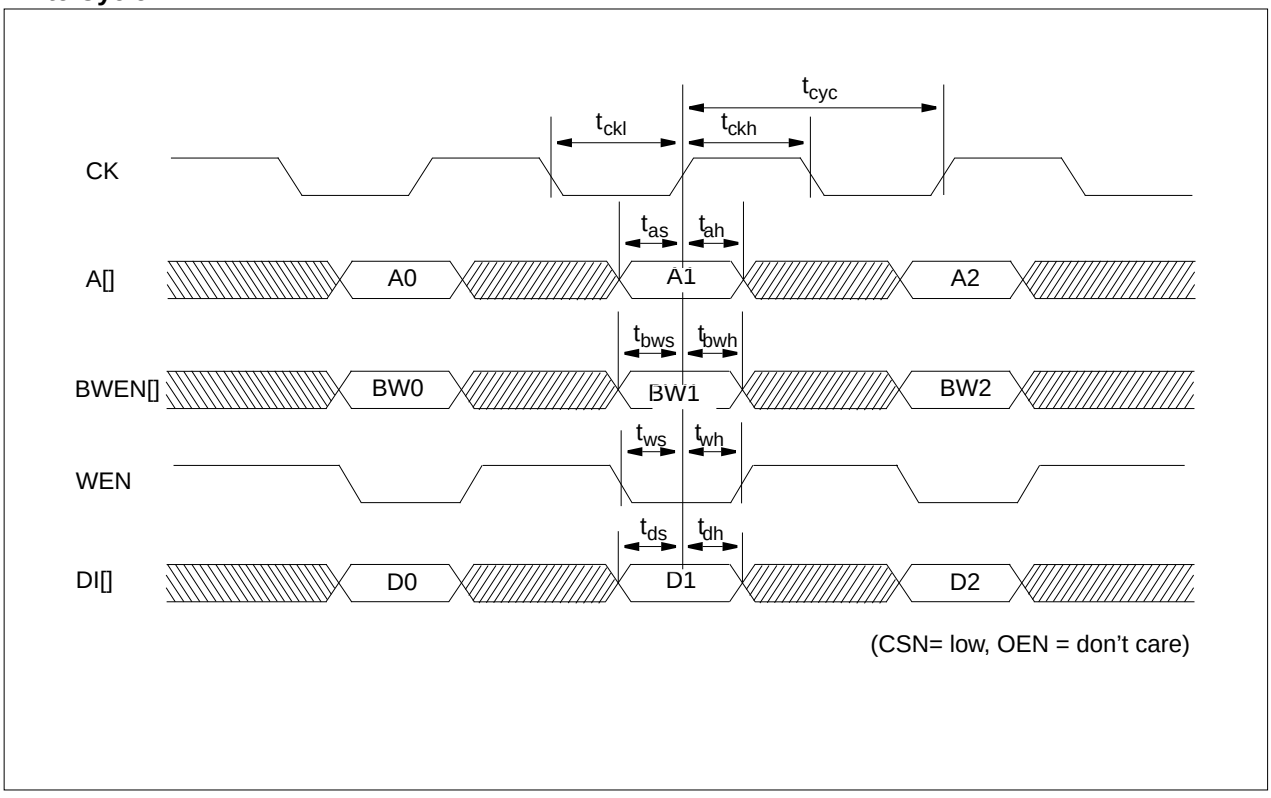
Timing Diagrams

Read Cycle



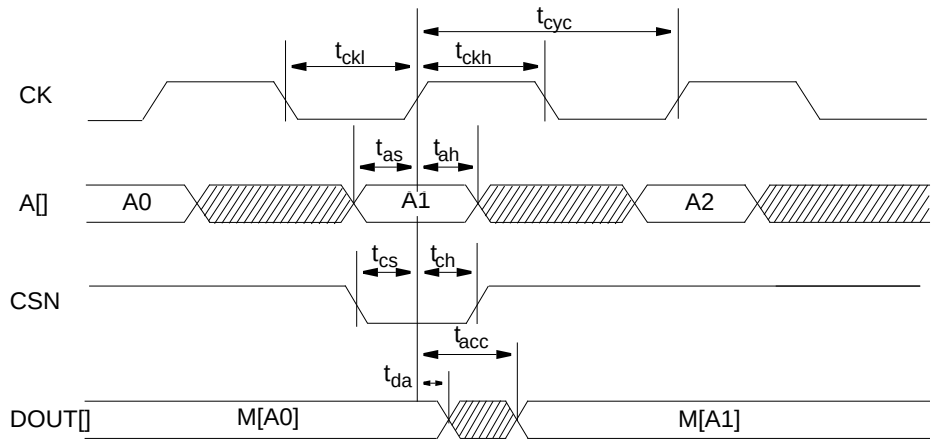
(CSN = low, OEN = low, DI[], BWEN[]= don't care)

Write Cycle



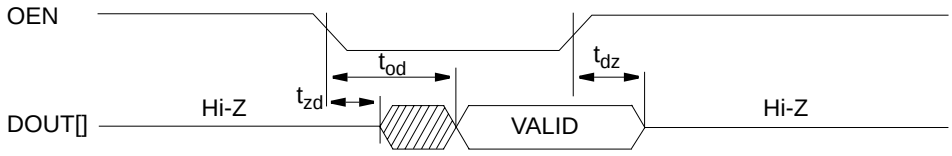
(CSN= low, OEN = don't care)

Read Cycle with CSN-Controlled



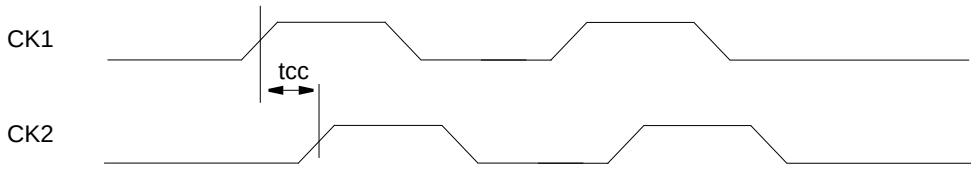
(OEN = low, WEN = high, DI[], BWEN[] = don't care)

OEN-Controlled Output Enable



(CSN, CK, A[], WEN, DI[], BWEN[] = don't care)

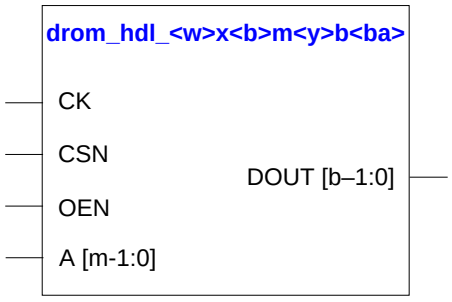
Contention Mode



(A1[] = A2[])

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Banks (ba) is the number of banks.
5. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density applications
- Low-average power operation
- Diffusion-programmable code available
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down mode available
- Low noise output optimization
- Zero standby current
- Zero hold time
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DROM_HDL is a synchronous diffusion programmable ROM which is provided as a compiler. DROM_HDL is intended for use in high-density applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

DROM_HDL Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read cycle

DROM_HDL

High-Density Synchronous Diffusion Programmable ROM

Parameter Description

DROM_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b) and Column mux(y) and Number of banks(ba).

Parameters			Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	ba = 1	Min	64	128	256
		Max	2048	4096	8192
		Step	32	64	128
	ba = 2	Min	128	256	512
		Max	4096	8192	16384
		Step	64	128	256
Bpw (b)		Min	2	2	2
		Max	128	64	32
		Step	1	1	1

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

Pin Capacitance

(Unit = SL)

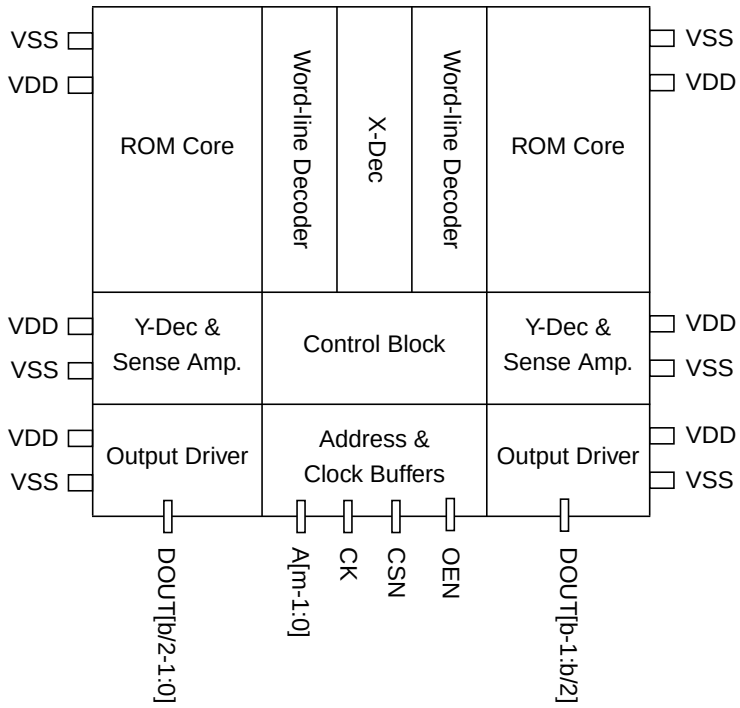
	CK	CSN	OEN	A	DOUT
ba = 1	4.16	1.60	1.71	1.73	6.86
ba = 2	2.70	1.60	1.71	1.73	6.86

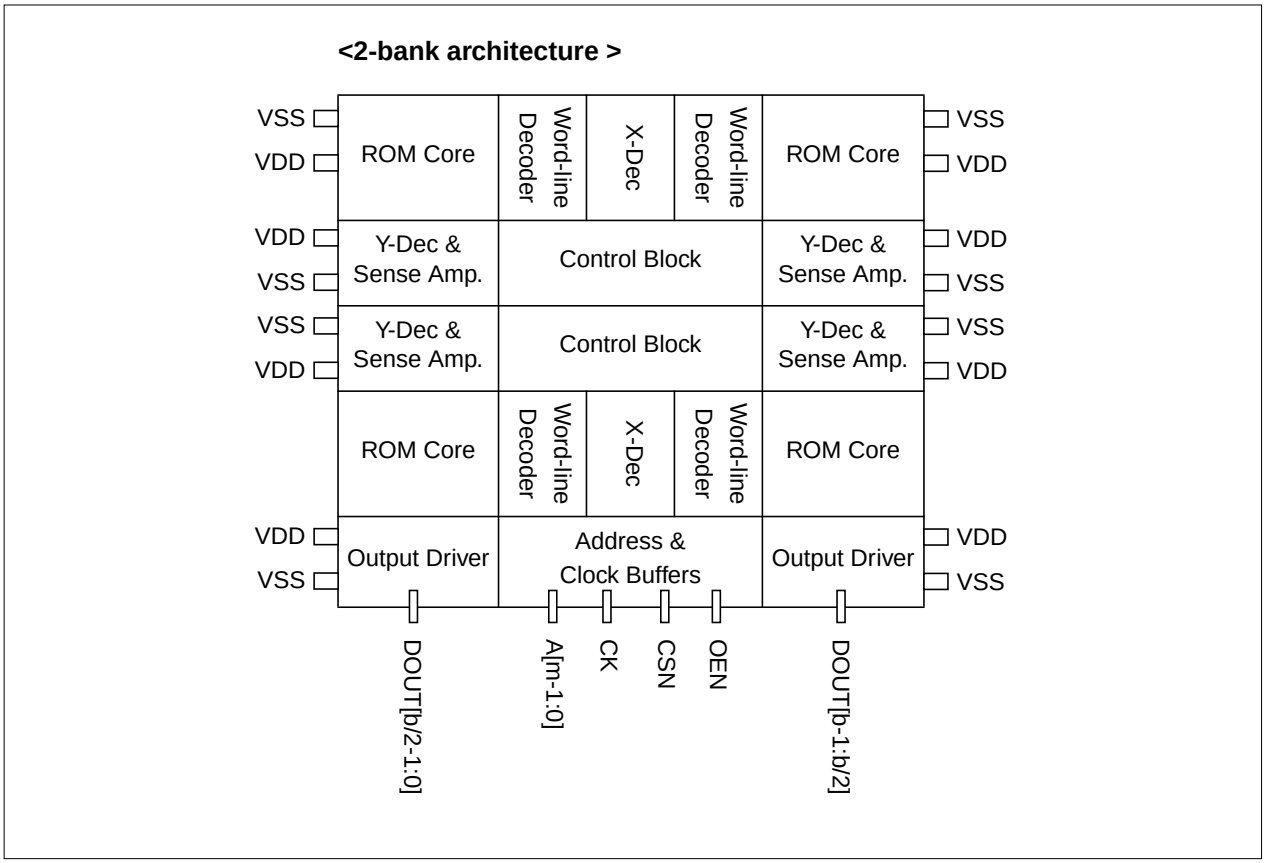
NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

Block Diagrams

DROM_HDL has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from DROM_HDL compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the multi power ports are located on the top edge, the middle edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the multi power ports are located on the top-edge, the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>





Application Notes

1. Permitting over-the-cell routing
In chip-level layout, over-the-cell routing in DROM_HDL is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DROM_HDL.

4. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ch}	CSN hold time from CK rise
t_{ckl}	Clock pulse width low	t_{acc}	Data access time
t_{ckh}	Clock pulse width high	t_{da}	De-access time
t_{as}	Address setup time	t_{dz}	DOUT drive to high-Z time
t_{ah}	Address hold time	t_{zd}	DOUT high-Z to drive time
t_{cs}	CSN setup time	t_{od}	OEN to valid output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**64**	**128**	**128**	**256**	**256**	**512**	**512**
bpw	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	3.21	3.28	3.51	3.35	3.58	3.44	3.67
t_{ckl}	0.82	0.82	0.92	0.82	0.93	0.82	0.95
t_{ckh}	1.20	1.20	1.35	1.20	1.36	1.20	1.38
t_{as}	0.34	0.34	0.92	0.34	0.93	0.33	0.95
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.82	0.82	0.92	0.82	0.93	0.82	0.95
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.33	2.41	2.61	2.50	2.70	2.61	2.82
t_{da}	1.95	2.04	2.19	2.14	2.29	2.28	2.42
t_{dz}	0.49	0.54	0.54	0.58	0.58	0.64	0.64
t_{zd}	0.64	0.68	0.68	0.71	0.71	0.75	0.75
t_{od}	0.73	0.77	0.77	0.80	0.80	0.85	0.85
Power (µW/MHz)							
Power_read	101.98	135.12	176.13	178.45	216.91	245.95	273.96
Power_standby	19.49	21.59	58.17	24.69	62.77	29.72	69.70
Area (µm)							
Width	426.10	581.87	579.88	739.63	735.65	901.36	893.41
Height	166.72	173.92	318.72	188.32	333.12	217.12	361.92

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.59	3.79	3.76	3.93	3.93	4.07	4.39
t_{ckl}	0.82	0.98	0.82	1.01	0.82	1.04	1.17
t_{ckh}	1.20	1.41	1.20	1.44	1.20	1.48	1.60
t_{as}	0.31	0.98	0.29	1.01	0.28	1.04	1.17
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.82	0.98	0.82	1.01	0.82	1.04	1.17
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.77	2.98	2.98	3.15	3.20	3.33	3.70
t_{da}	2.45	2.60	2.64	2.77	2.85	2.95	3.26
t_{dz}	0.69	0.69	0.74	0.74	0.79	0.79	0.79
t_{zd}	0.80	0.80	0.84	0.84	0.88	0.88	0.88
t_{od}	0.89	0.89	0.93	0.93	0.97	0.97	0.97
Power (µW/MHz)							
Power_read	327.04	358.32	416.20	433.12	514.88	514.90	632.48
Power_standby	34.63	81.31	42.62	89.00	50.62	96.68	130.85
Area (µm)							
Width	1059.78	1055.14	1215.88	1211.24	1371.98	1367.34	1371.98
Height	274.72	419.52	332.32	477.12	389.92	534.72	765.12

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**128**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	3.21	3.28	3.51	3.35	3.58	3.44	3.67
t_{ckl}	0.82	0.82	0.92	0.82	0.93	0.82	0.95
t_{ckh}	1.20	1.20	1.35	1.20	1.36	1.20	1.38
t_{as}	0.34	0.34	0.92	0.34	0.93	0.33	0.95
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.81	0.82	0.92	0.82	0.93	0.82	0.95
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.37	2.45	2.67	2.53	2.76	2.64	2.89
t_{da}	1.96	2.04	2.20	2.14	2.30	2.28	2.43
t_{dz}	0.45	0.48	0.48	0.51	0.51	0.54	0.54
t_{zd}	0.61	0.63	0.63	0.66	0.66	0.69	0.69
t_{od}	0.70	0.72	0.72	0.75	0.75	0.78	0.78
Power (µW/MHz)							
Power_read	78.08	100.06	139.99	127.58	167.41	168.80	204.62
Power_standby	18.50	20.10	55.17	22.67	58.77	27.21	64.70
Area (µm)							
Width	426.10	581.87	579.88	739.63	735.65	901.36	893.41
Height	166.72	173.92	318.72	188.32	333.12	217.12	361.92

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.59	3.79	3.76	3.93	3.93	4.07	4.39
t_{ckl}	0.82	0.98	0.82	1.01	0.82	1.04	1.17
t_{ckh}	1.20	1.41	1.20	1.44	1.20	1.48	1.60
t_{as}	0.31	0.98	0.29	1.01	0.28	1.04	1.17
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.82	0.98	0.82	1.01	0.82	1.04	1.17
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.81	3.04	3.02	3.22	3.24	3.40	3.77
t_{da}	2.46	2.61	2.65	2.79	2.85	2.97	3.28
t_{dz}	0.58	0.58	0.61	0.61	0.64	0.64	0.64
t_{zd}	0.71	0.71	0.74	0.74	0.77	0.77	0.77
t_{od}	0.80	0.80	0.83	0.83	0.86	0.86	0.86
Power (µW/MHz)							
Power_read	217.66	258.28	272.39	305.33	332.24	356.14	435.64
Power_standby	31.64	75.34	39.17	82.02	46.69	88.71	122.89
Area (µm)							
Width	1059.78	1055.14	1215.88	1211.24	1371.98	1367.34	1371.98
Height	274.72	419.52	332.32	477.12	389.92	534.72	765.12

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**256**	**512**	**512**	**1024**	**1024**	**2048**	**2048**
bpw	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	3.21	3.28	3.52	3.35	3.58	3.44	3.67
t_{ckl}	0.82	0.82	0.92	0.82	0.93	0.82	0.95
t_{ckh}	1.20	1.20	1.35	1.20	1.36	1.20	1.38
t_{as}	0.34	0.34	0.92	0.34	0.93	0.33	0.95
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.82	0.82	0.92	0.82	0.93	0.82	0.95
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.44	2.52	2.80	2.60	2.89	2.71	3.01
t_{da}	1.97	2.06	2.22	2.16	2.32	2.30	2.45
t_{dz}	0.43	0.45	0.45	0.47	0.47	0.50	0.50
t_{zd}	0.59	0.61	0.61	0.63	0.63	0.65	0.65
t_{od}	0.68	0.70	0.70	0.72	0.72	0.74	0.74
Power (µW/MHz)							
Power_read	66.37	82.45	122.23	102.17	142.87	130.41	170.21
Power_standby	18.00	19.35	53.66	21.67	56.78	25.95	62.23
Area (µm)							
Width	426.10	581.87	579.88	739.63	735.65	901.36	893.41
Height	166.72	173.92	318.72	188.32	333.12	217.12	361.92

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

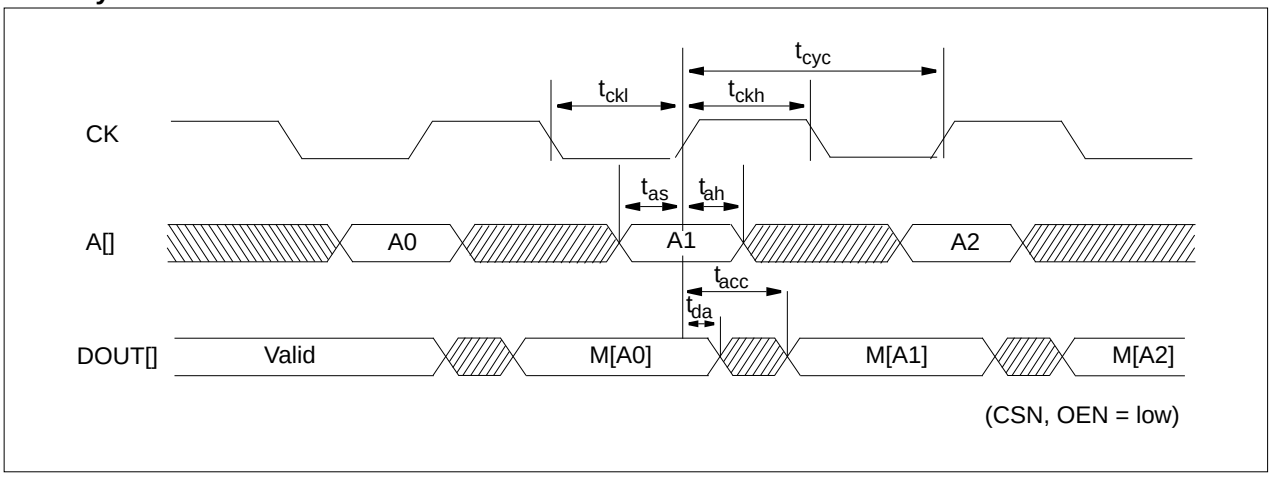
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.59	3.79	3.76	3.93	3.93	4.07	4.39
t_{ckl}	0.82	0.98	0.82	1.01	0.82	1.04	1.17
t_{ckh}	1.20	1.41	1.20	1.44	1.20	1.48	1.60
t_{as}	0.31	0.98	0.29	1.01	0.28	1.04	1.17
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.82	0.98	0.82	1.01	0.82	1.04	1.17
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.88	3.17	3.10	3.35	3.32	3.54	3.91
t_{da}	2.47	2.63	2.67	2.81	2.87	2.99	3.30
t_{dz}	0.52	0.52	0.54	0.54	0.57	0.57	0.57
t_{zd}	0.67	0.67	0.69	0.69	0.71	0.71	0.71
t_{od}	0.76	0.76	0.78	0.78	0.80	0.80	0.80
Power (µW/MHz)							
Power_read	163.23	208.92	200.70	242.00	241.11	277.10	337.56
Power_standby	30.16	72.37	37.40	78.55	44.64	84.74	118.90
Area (µm)							
Width	1059.78	1055.14	1215.88	1211.24	1371.98	1367.34	1371.98
Height	274.72	419.52	332.32	477.12	389.92	534.72	765.12

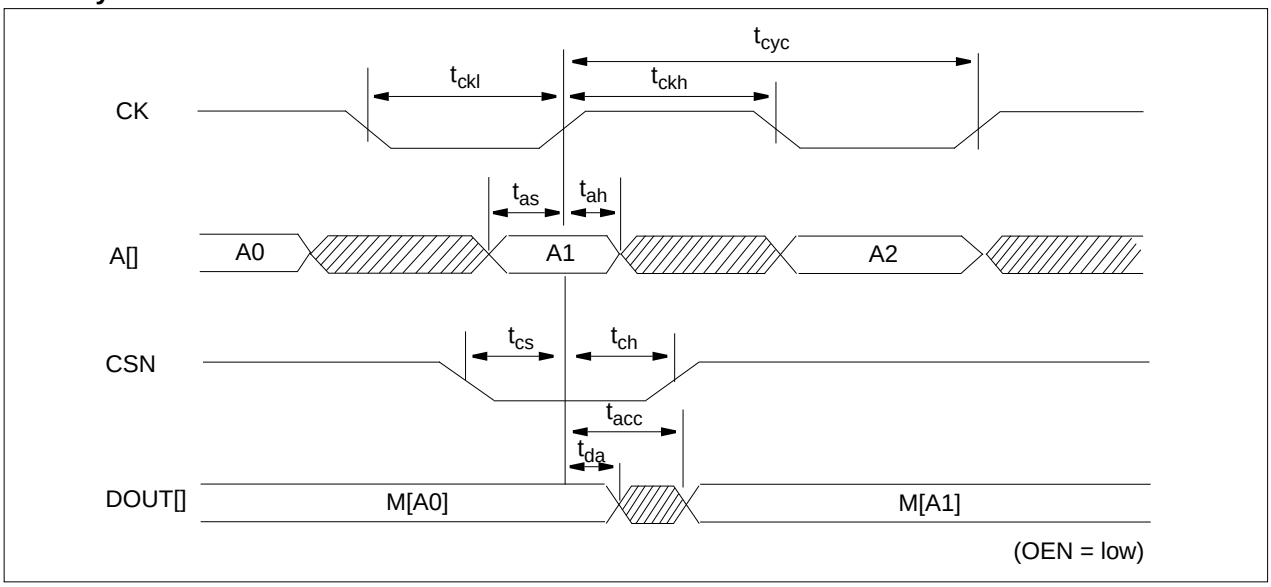
NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Timing Diagrams

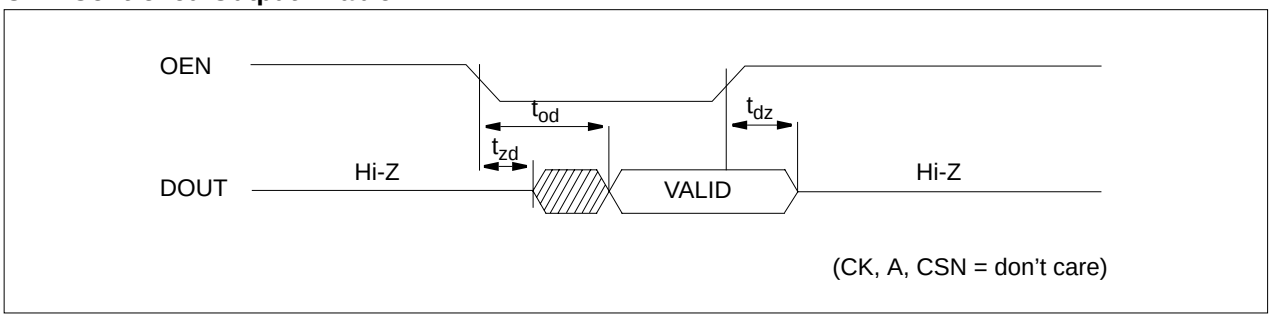
Read Cycle



Read Cycle with CSN Controlled

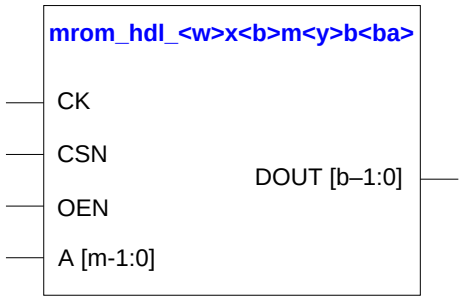


OEN-Controlled Output Enable



NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words (w) is the number of words.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil$

Features

- Suitable for high-density applications
- Low-average power operation
- Metal2-programmable code available
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output
- Latched inputs and outputs
- Automatic power-down mode available
- Low noise output optimization
- Zero standby current
- Zero hold time
- Flexible aspect ratio
- Dual-bank scheme available
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

MROM_HDL is a synchronous metal-2 programmable ROM which is provided as a compiler. MROM_HDL is intended for use in high-density applications. The read cycle is initiated at the rising edge of CK. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, DOUT[] remains stable. When OEN is high, DOUT is placed in a high-impedance state.

MROM_HDL Function Table

CK	CSN	OEN	A	DOUT	Comment
X	X	H	X	Z	Unconditional tri-state output
X	H	L	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	Valid	MEM(A)	Read cycle

MROM_HDL

High-Density Synchronous Metal-2 Programmable ROM

Parameter Description

MROM_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bits per word(b), Column mux(y) and Number of banks(ba).

Parameters			Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	ba = 1	Min	64	128	256
		Max	2048	4096	8192
		Step	32	64	128
	ba = 2	Min	128	256	512
		Max	4096	8192	16384
		Step	64	128	256
Bpw (b)		Min	2	2	2
		Max	128	64	32
		Step	1	1	1

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN and A[] are latched into the ROM on the rising edge of CK. If CSN is low on the rising edge of CK, the ROM is in read mode.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the ROM on the rising edge of CK. When CSN is low, the ROM is enabled for reading. When CSN is high, the ROM goes to the standby mode and is disabled for reading. DOUT remains previous data output.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the ROM on the rising edge of CK.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the ROM is in read mode.

Pin Capacitance

(Unit = SL)

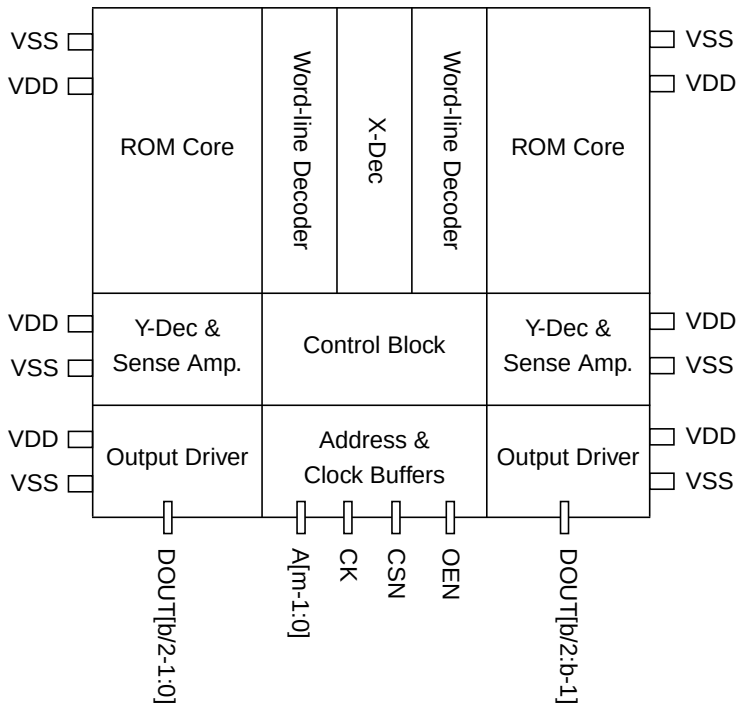
	CK	CSN	OEN	A	DOUT
ba = 1	3.97	1.18	1.32	1.18	5.25
ba = 2	2.17	1.18	1.32	1.18	5.25

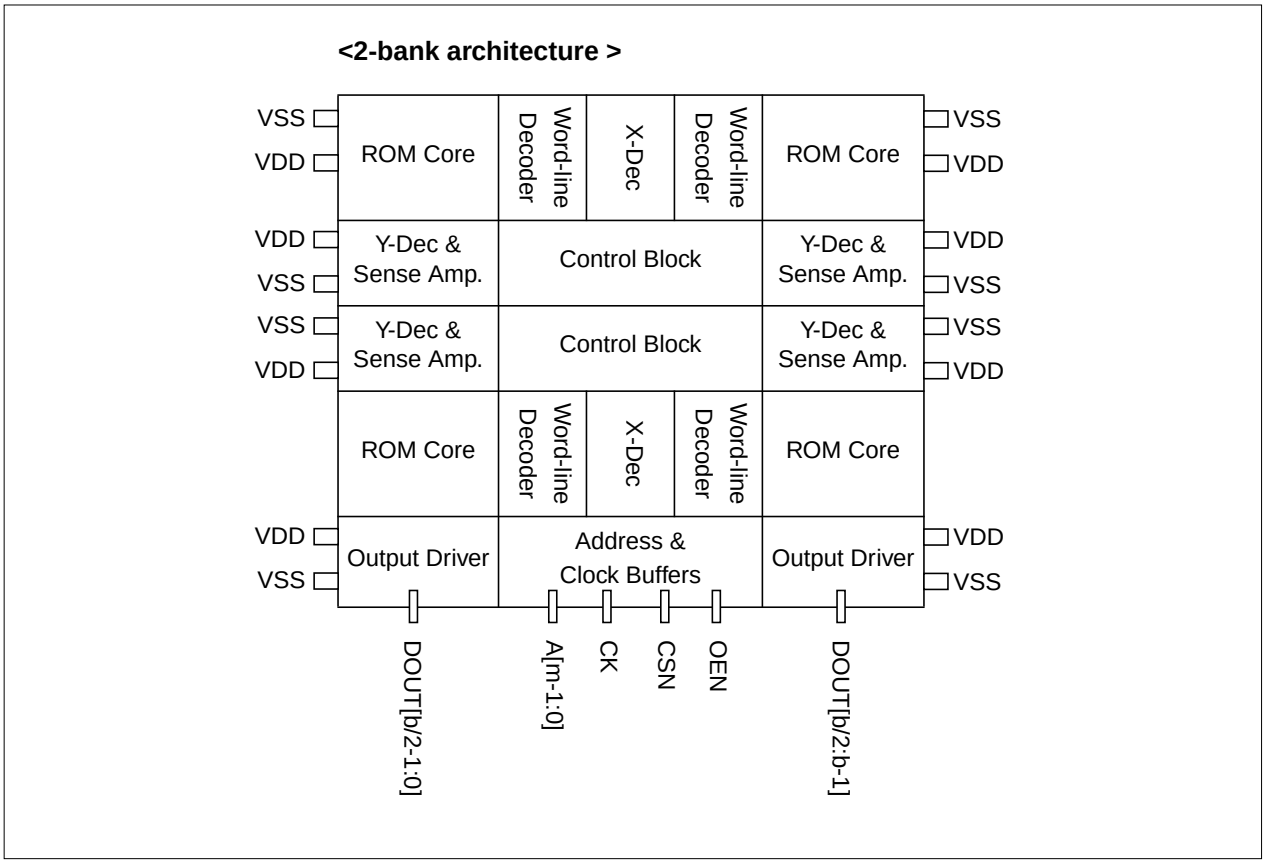
NOTE: Each pin's capacitance is exactly same regardless of available mux types for same bank.

Block Diagrams

MROM_HDL has 2 different physical architectures due to the word depth. Optionally, one of these architectures is generated from MROM_HDL compiler. In dual-bank, the bank selected by the address is only activated while the other bank is in idle mode. In 1-bank architecture, the multi power ports are located on the top-edge, the middle edge and the bottom edge of both right- and left-sides of the memory. In 2-bank architecture, the multi power ports are located on the top-edge, the middle-edge and the bottom-edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory regardless of architecture.

<1-bank architecture>





Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in MROM_HDL is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of MROM_HDL.

4. Power reduction duting standby mode. The standby power is measured on the condition that only CSN is in disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are actived while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ch}	CSN hold time from CK rise
t_{ckl}	Clock pulse width low	t_{acc}	Data access time
t_{ckh}	Clock pulse width high	t_{da}	De-access time
t_{as}	Address setup time	t_{dz}	DOUT drive to high-Z time
t_{ah}	Address hold time	t_{zd}	DOUT high-Z to drive time
t_{cs}	CSN setup time	t_{od}	OEN to valid data output
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operations		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**64**	**128**	**128**	**256**	**256**	**512**	**512**
bpw	**32**	**48**	**48**	**64**	**64**	**80**	**80**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	3.36	3.48	3.60	3.60	3.72	3.75	3.86
t_{ckl}	0.93	0.93	0.91	0.93	0.92	0.93	0.93
t_{ckh}	1.15	1.15	1.30	1.15	1.31	1.15	1.32
t_{as}	0.45	0.45	0.91	0.44	0.92	0.41	0.93
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.93	0.93	0.91	0.93	0.92	0.93	0.93
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.50	2.64	2.85	2.77	2.98	2.89	3.13
t_{da}	2.05	2.21	2.35	2.37	2.50	2.58	2.69
t_{dz}	0.51	0.57	0.57	0.63	0.62	0.68	0.68
t_{zd}	0.65	0.69	0.69	0.74	0.74	0.79	0.79
t_{od}	0.74	0.79	0.79	0.84	0.84	0.88	0.88
Power (µW/MHz)							
Power_read	106.08	148.89	189.67	206.78	240.68	297.72	310.48
Power_standby	22.14	24.48	63.95	27.64	68.94	32.48	75.89
Area (µm)							
Width	427.44	602.19	600.20	783.05	779.07	965.59	957.64
Height	166.70	178.98	320.12	206.54	346.68	259.66	399.80

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**1024**	**1024**	**1536**	**1536**	**2048**	**2048**	**4096**
bpw	**96**	**96**	**112**	**112**	**128**	**128**	**128**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.95	4.05	4.19	4.23	4.42	4.42	4.69
t_{ckl}	0.93	0.94	0.93	0.96	0.93	0.98	1.05
t_{ckh}	1.15	1.33	1.15	1.35	1.15	1.37	1.43
t_{as}	0.36	0.94	0.35	0.96	0.34	0.98	1.05
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.93	0.94	0.93	0.96	0.93	0.98	1.05
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.16	3.31	3.45	3.55	3.73	3.77	4.13
t_{da}	2.83	2.94	3.12	3.17	3.40	3.40	3.70
t_{dz}	0.74	0.74	0.80	0.80	0.86	0.86	0.86
t_{zd}	0.83	0.83	0.88	0.88	0.93	0.93	0.93
t_{od}	0.93	0.93	0.98	0.98	1.02	1.02	1.02
Power (µW/MHz)							
Power_read	417.74	422.50	554.87	523.81	713.46	636.78	832.10
Power_standby	36.84	86.83	43.65	94.06	50.47	101.27	128.01
Area (µm)86.83							
Width	1140.37	1135.73	1312.82	1308.18	1485.28	1480.64	1485.28
Height	365.90	506.04	472.14	612.28	578.38	718.52	1143.48

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**128**	**256**	**256**	**512**	**512**	**1024**	**1024**
bpw	**16**	**24**	**24**	**32**	**32**	**40**	**40**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	3.36	3.48	3.60	3.60	3.72	3.75	3.86
t_{ckl}	0.93	0.93	0.91	0.94	0.92	0.94	0.93
t_{ckh}	1.15	1.15	1.30	1.15	1.31	1.15	1.32
t_{as}	0.45	0.45	0.91	0.44	0.92	0.41	0.93
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.93	0.93	0.91	0.94	0.92	0.94	0.93
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.53	2.68	2.91	2.80	3.04	2.92	3.20
t_{da}	2.05	2.21	2.36	2.38	2.51	2.59	2.70
t_{dz}	0.46	0.50	0.50	0.54	0.54	0.58	0.58
t_{zd}	0.61	0.64	0.64	0.68	0.68	0.71	0.71
t_{od}	0.71	0.74	0.74	0.77	0.77	0.80	0.80
Power (µW/MHz)							
Power_read	82.74	110.90	151.91	148.02	187.02	203.27	232.30
Power_standby	21.11	22.92	60.86	25.58	64.81	29.89	70.79
Area (µm)							
Width	427.44	602.55	600.56	783.05	779.07	965.34	957.39
Height	166.70	179.98	320.12	206.54	346.68	259.66	399.80

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**2048**	**2048**	**3072**	**3072**	**4096**	**4096**	**8192**
bpw	**48**	**48**	**56**	**56**	**64**	**64**	**64**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.95	4.05	4.19	4.23	4.42	4.42	4.69
t_{ckl}	0.93	0.94	0.93	0.96	0.93	0.98	1.05
t_{ckh}	1.15	1.33	1.15	1.35	1.15	1.37	1.43
t_{as}	0.36	0.94	0.35	0.96	0.34	0.98	1.05
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.93	0.94	0.93	0.96	0.93	0.98	1.05
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.19	3.37	3.48	3.62	3.77	3.84	4.19
t_{da}	2.84	2.95	3.13	3.18	3.41	3.42	3.71
t_{dz}	0.61	0.61	0.65	0.65	0.69	0.69	0.69
t_{zd}	0.74	0.74	0.77	0.77	0.80	0.80	0.80
t_{od}	0.83	0.83	0.86	0.86	0.89	0.89	0.89
Power (µW/MHz)							
Power_read	274.20	300.98	351.83	362.76	438.43	430.58	540.03
Power_standby	33.76	80.76	40.07	86.91	46.38	93.06	119.79
Area (µm)							
Width	1140.20	1135.56	1312.74	1308.10	1485.28	1480.64	1485.28
Height	365.90	506.04	472.14	612.28	578.38	718.52	1143.48

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**256**	**512**	**512**	**1024**	**1024**	**2048**	**2048**
bpw	**8**	**12**	**12**	**16**	**16**	**20**	**20**
ba	**1**	**1**	**2**	**1**	**2**	**1**	**2**
Timing (ns)							
t_{cyc}	3.36	3.48	3.60	3.60	3.72	3.75	3.86
t_{ckl}	0.93	0.94	0.92	0.94	0.92	0.93	0.93
t_{ckh}	1.15	1.15	1.30	1.15	1.31	1.15	1.31
t_{as}	0.45	0.45	0.92	0.44	0.92	0.41	0.93
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.93	0.94	0.92	0.94	0.92	0.93	0.93
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	2.59	2.74	3.02	2.86	3.16	2.98	3.31
t_{da}	2.06	2.22	2.38	2.39	2.53	2.60	2.72
t_{dz}	0.44	0.47	0.47	0.49	0.50	0.52	0.52
t_{zd}	0.60	0.62	0.62	0.64	0.64	0.66	0.66
t_{od}	0.69	0.71	0.71	0.73	0.73	0.76	0.76
Power (µW/MHz)							
Power_read	71.12	92.24	133.37	118.76	159.84	156.07	192.78
Power_standby	20.59	22.15	59.30	24.55	62.75	28.61	68.21
Area (µm)							
Width	427.44	603.46	601.47	783.05	779.07	964.80	956.85
Height	166.70	179.98	320.12	206.54	346.68	259.66	399.80

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

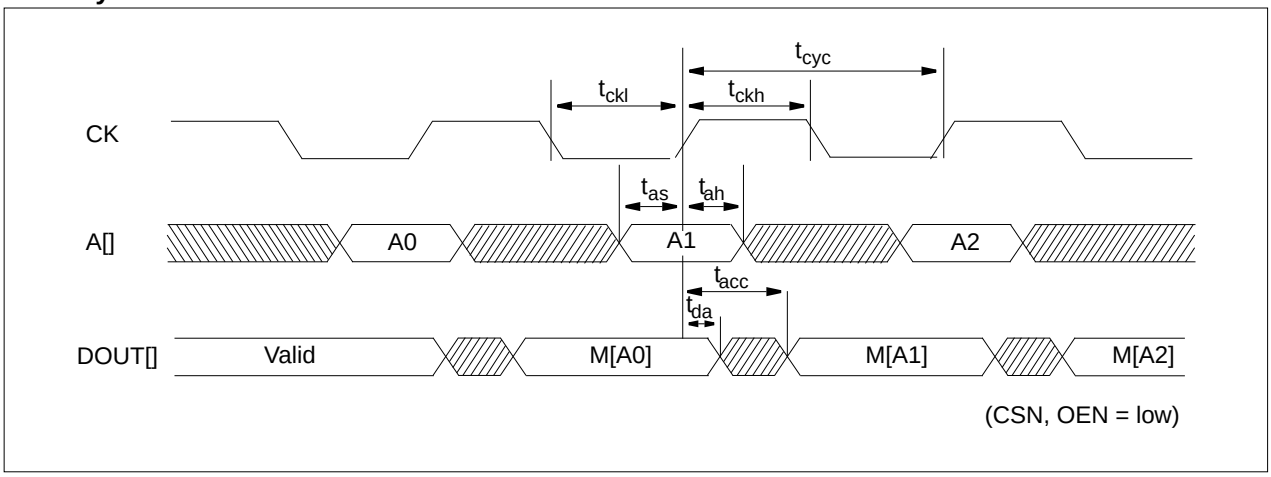
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters							
words	**4096**	**4096**	**6144**	**6144**	**8192**	**8192**	**16384**
bpw	**24**	**24**	**28**	**28**	**32**	**32**	**32**
ba	**1**	**2**	**1**	**2**	**1**	**2**	**2**
Timing (ns)							
t_{cyc}	3.95	4.05	4.18	4.23	4.42	4.42	4.69
t_{ckl}	0.93	0.94	0.93	0.96	0.93	0.98	1.05
t_{ckh}	1.15	1.33	1.15	1.35	1.15	1.37	1.43
t_{as}	0.36	0.94	0.35	0.96	0.34	0.98	1.05
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.93	0.94	0.93	0.96	0.93	0.98	1.05
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.26	3.49	3.55	3.74	3.84	3.97	4.32
t_{da}	2.85	2.96	3.14	3.19	3.42	3.43	3.73
t_{dz}	0.55	0.55	0.57	0.57	0.60	0.60	0.60
t_{zd}	0.68	0.68	0.71	0.71	0.73	0.73	0.73
t_{od}	0.78	0.78	0.80	0.80	0.82	0.82	0.83
Power (µW/MHz)							
Power_read	202.26	240.42	253.23	282.41	309.17	327.62	402.51
Power_standby	32.22	77.66	38.26	83.30	44.32	88.95	115.65
Area (µm)							
Width	1139.84	1135.20	1312.56	1307.92	1485.28	1480.64	1485.28
Height	365.90	506.04	472.14	612.28	578.38	718.52	1143.48

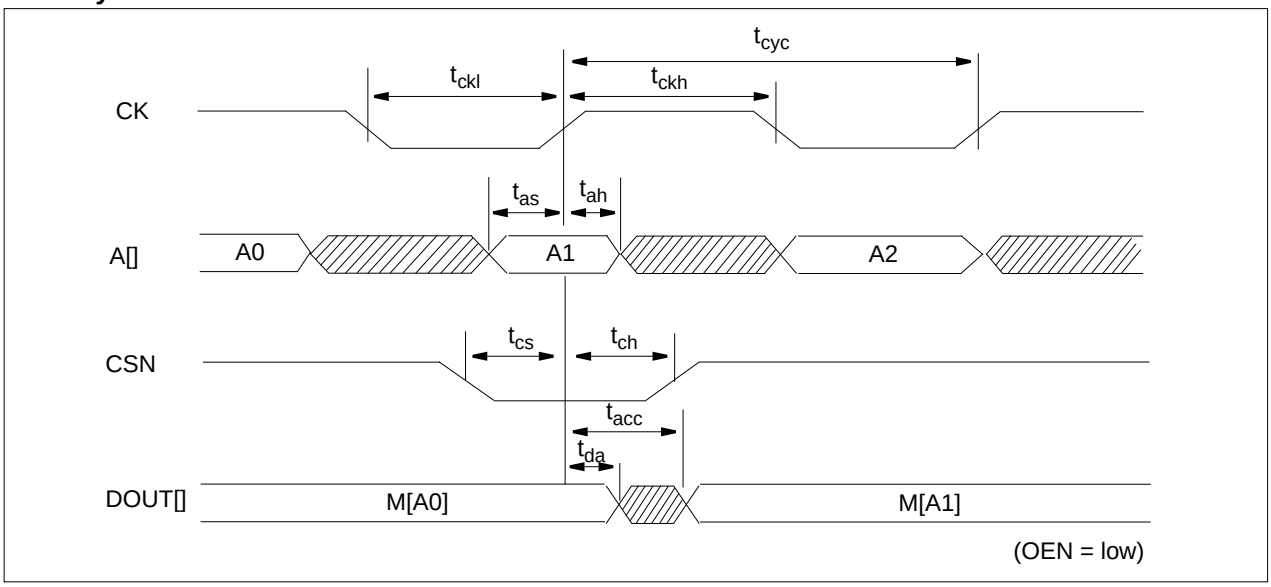
NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Timing Diagrams

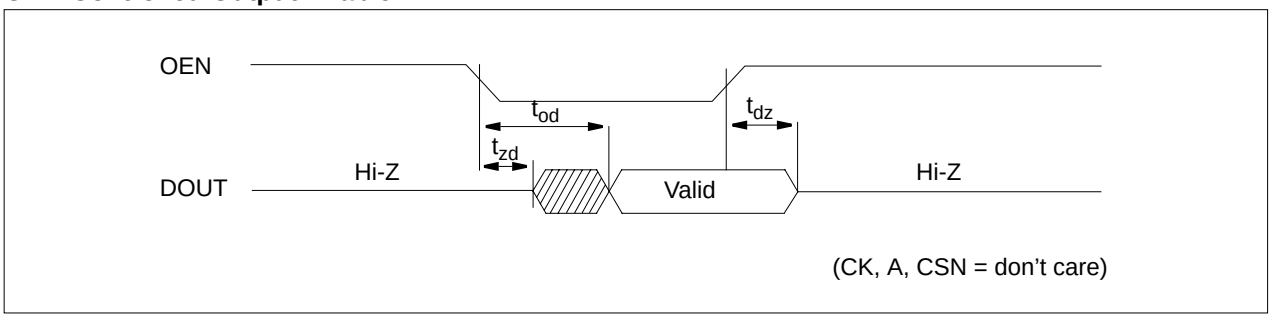
Read Cycle



Read Cycle with CSN Controlled

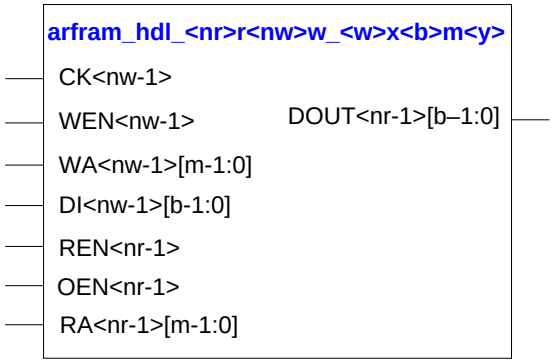


OEN-Controlled Output Enable



NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. Writes(nw) is the number of write ports(1-to-2).
5. Reads(nr) is the number of read ports(1-to-2).
6. m = $\lceil \log_2 w \rceil$

Features

- High-density application
- Suitable for high-speed application
- Synchronous write operation
- Asynchronous read operation
- Fully independent port
- Latched input and output
- Separated data I/O
- Flexible aspect ratio
- Asynchronous tristate output
- Zero standby current
- Configurable 1-to-2 read ports
- Configurable 1-to-2 write ports
- Up to 16Kbits capacity
- Up to 1024K number of words
- Up to 64 number of bits per word

Function Description

ARFRAM_HDL is a multi-port asynchronous register file which is provided as a compiler. ARFRAM_HDL is intended for use in high-density applications. It allows maximum 4 ports with configurable 1-to-2 read ports and 1-to-2 write ports. All read and write ports are fully independent. On the rising edge of CK, the write cycle is initiated when WEN is low. While CK is high, the data at DI[] is written into the memory location specified on WA[]. At the falling edge of CK, the write cycle is terminated. If WEN is high, WA[] and DI[] are disabled . It is called “write standby mode”. When REN and OEN are low, the data stored in the memory location specified on RA[] becomes valid through DOUT[] after a delay. If REN is high, RA[] is disabled and DOUT[] remains in the previous data output. It is called “read standby mode”. When OEN is high, DOUT[] is placed in a high-impedance state regardless of REN.

ARFRAM_HDL Function Table

CK	WEN	WA	DI	RA	REN	OEN	DOUT	Comment
X	H	X	X	X	X	X	X	Write standby mode
↑	L	Valid	Valid	X	X	X	X	Write cycle starts
↓	L	X	X	X	X	X	X	Write cycle ends
X	X	X	X	X	X	H	Z	Unconditional tri-state output
X	X	X	X	X	H	L	DOUT(t-1)	Read standby mode
X	X	X	X	Toggle	L	L	MEM(RA)	Read cycle
X	X	X	X	Valid	↓	L	MEM(RA)	Read cycle with REN-controlled

ARFRAM_HDL

High-Density Multi-Port Asynchronous Register File

Parameter Description

ARFRAM_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y), Number of read ports(nr) and Number of write ports(nw).

Parameters		Ymux(y) = 2	Ymux(y) = 4	Ymux(y) = 8
Words (w)	Min	4	8	16
	Max	256	512	1024
	Step	2	4	8
Bpw (b)	Min	1	1	1
	Max	64	32	16
	Step	1	1	1
Write ports(nw)		1, 2		
Read ports(nr)		1, 2		

Pin Descriptions

Name	I/O	Description
CK<nw-1>	Write Clock	Write clock input on each write port. WEN, WA[] and DI[] are latched into the RAM on the rising edge of CK. If WEN is low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in write standby mode. At the falling edge of CK, the write-operation completes and the RAM is in a precharge state.
WEN<nw-1>	Write Enable	Write enable input on each write port. WEN is latched into the RAM on the rising edge of CK. When WEN is low, the write mode is enabled. When WEN is high, it prevents the write-operation. It is called “write standby mode”.
WA<nw-1> [ ]	Write Address	Write address bus on each write port. It specifies the location in which the data will be written in the write-operation. WA[] is latched at the rising edge of CK.
DI<nw-1> [ ]	Data Input	Data input bus on each write port. It contains data values to be written into the memory during the write-cycle. DI[] is latched at the rising edge of CK.
REN<nr-1>	Read Enable	Read enable input on each read port. When REN is low, read is enabled. When REN is high, read is disabled and DOUT[] remains in the previous state. It is called “read standby mode”
OEN<nr-1>	Data Output Enable	Output enable input on each read port. The low state enables output drivers and the high state disables output to go to the Hi-Z state.
RA<nr-1> [ ]	Read Address	Read address bus on each read port. It specifies the location to be read in the read-operation.
DOUT<nr-1> [ ]	Data Output	Data output bus on each read port. When REN and OEN are low, it presents the data word stored in the location specified by RA[]. When REN is high and OEN is low, DOUT[] remains in the previous state. When OEN is high, DOUT[] is in the high-impedance state regardless of REN.

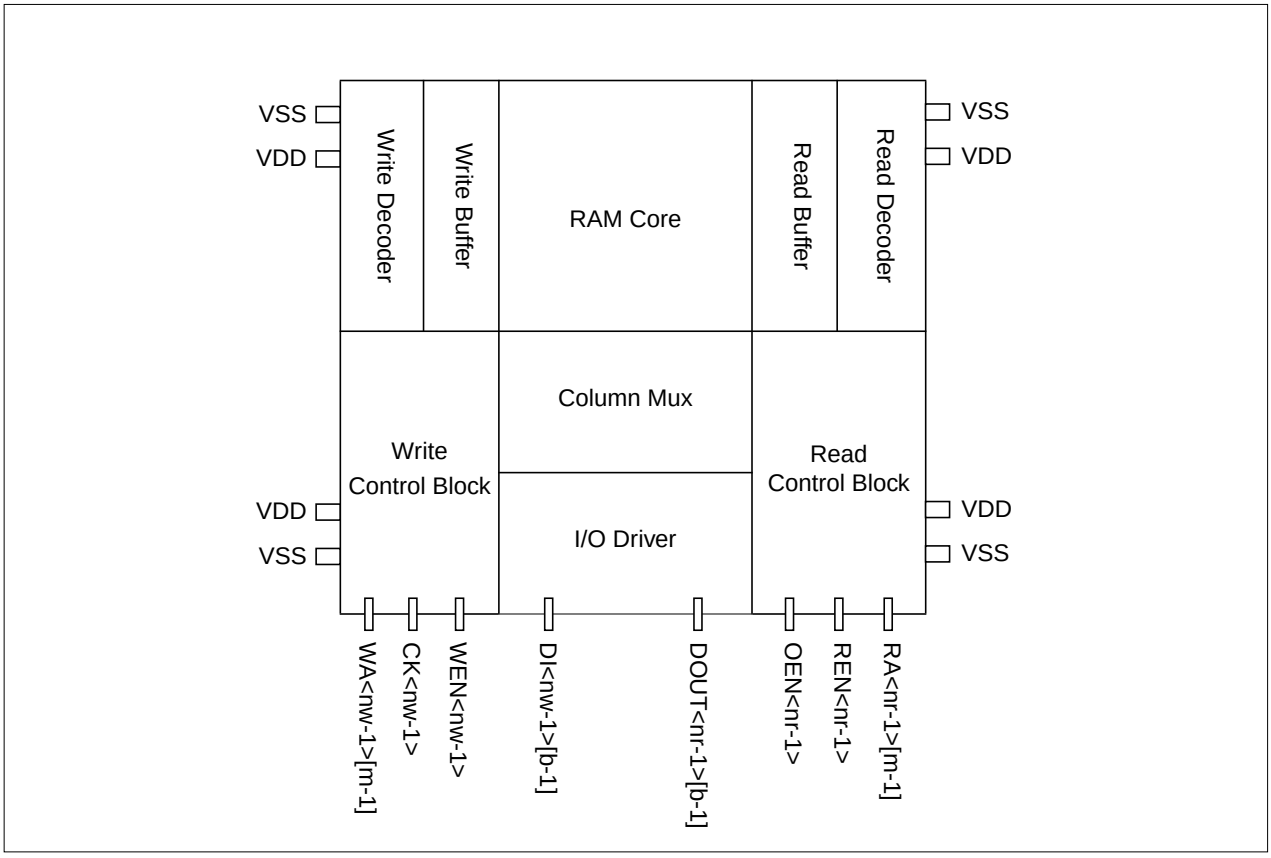
Pin Capacitance

(Unit = SL)

CK	WEN	DI	REN	OEN	WA	RA	DOUT
2.00	6.98	3.39	5.66	2.41	2.00	3.50	19.70

Block Diagrams

ARFRAM_HDL supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



Application Notes

1. Permitting over-the-cell routing.
In ARFRAM_HDL, the over-the-cell routing is permitted for Metal-4 or upper layers. Namely, while doing layout on the chip-level, any signals to be routed can be crossed over the area of register file generated by ARFRAM_HDL compiler.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of ARFRAM_HDL.

4. Contention mode under same addresses(RA[]=WA[] or WA0[] = WA1[]).
In ARFRAM_HDL, simultaneous operations by both ports on the same address(RA[]=WA[] or WA0[] = WA1[]) such as read/write,write/read, write/write operation, cause a contention problem. Simultaneous operations are defined as the state in which both ports are enabled and both address buses are equal. ARFRAM_HDL has no scheme preventing the contention mode. Due to the simultaneous operations, silicon will behave unpredictably. A write operation cannot completes and data appearing at outputs may not be valid.
Please refer to the timing diagrams if you want to avoid the contention mode between both ports.

5. Keeping the stable address cycle time in read mode.
In ARFRAM_HDL, rather than the write operation which is synchronously performed by CK signal, the read operation is asynchronously performed whenever the address transition occures. So, in read mode if the another transition on the address occures after first transition within access time, read operation cannot completes. At that time, while in the read operation, the data stored in the memory may be corrupted due to the short transition. To prevent such fail, the stable read address cycle time (trcyc) is required. The essential requirement to recognize valid read address transition is that at least minimum address period should be equal or greater than tacc (access time).

6. Power reduction during standby mode.
ARFRAM_HDL provides two types of standby modes – the write standby mode and the read standby mode. While in the write standby mode, WA[] and DI[] except CK are blocked even though the transitions of those signals occure. While in the read standby mode, RA[] is blocked even though its transition occures. So, you can reduce the power consumption in ARFRAM_HDL by properly using two standby modes in your design.

Characteristics

Definition for AC Timing (ns)	
Symbol	**Description**
t_{wcyc}	Miminum write clock cycle time for write cycle
t_{ckl}	Mimimum CK pulse width low to guarantee write cycle
t_{ckh}	Mimimum CK pulse width high to guarantee write cycle
t_{was}	Write Address Setup time from WA[] to CK rise
t_{wah}	Write Address Hold time from CK rise to WA[]
t_{ws}	WEN Setup time from WEN fall to CK rise
t_{wh}	WEN Hold time from CK rise to WEN rise
t_{ds}	Data-in Setup time from DI[] to CK rise
t_{dh}	Data-in Hold time from CK rise to DI[]
t_{wwc}	Write-Write contention time from one CK to the other CK
t_{wda}	De-access time from CK rise to DOUT
t_{wacc}	Data Access time from CK fall
t_{rcyc}	Miminum RA[] Cycle time for read cycle
t_{acc}	Data ACCess time for read cycle
t_{ras}	Read Address Setup time from RA[] to REN rise
t_{rah}	Read Address Hold time from REN rise to RA[]
t_{da}	De-Access time from RA to DOUT
t_{zd}	DOUT high-Z to Drive time
t_{dz}	DOUT Drive to high-Z time
t_{od}	OEN to valid output time
Definition for Power Consumption (µW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_w_standby	The write standby power consumption while WEN is high and other signals are in normal operations.
Power_r_standby	The read standby power consumption while REN is high, OEN is low and other signals are in normal operations.
Definition for Area (µm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

Reference Table

*** For Ymux=2(nr=1, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**32**	**64**	**128**	**256**
bpw	**8**	**16**	**32**	**64**
Timing (ns)				
t_{wcyc}	1.39	1.53	1.81	2.54
t_{ckl}	1.08	1.06	1.03	1.08
t_{ckh}	0.26	0.29	0.38	0.69
t_{was}	0.75	0.72	0.65	0.62
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	0.15	1.13	1.10	1.15
t_{wh}	0.42	0.42	0.41	0.41
t_{ds}	0.84	0.80	0.73	0.71
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.94	2.19	2.38	2.71
t_{wacc}	1.99	2.22	2.38	2.84
t_{rcyc}	2.19	2.43	2.65	3.39
t_{acc}	2.19	2.43	2.65	3.39
t_{ras}	0.44	0.44	0.44	0.43
t_{rah}	0.14	0.15	0.16	0.18
t_{da}	0.93	0.99	1.11	1.31
t_{zd}	0.32	0.34	0.37	0.41
t_{dz}	0.28	0.30	0.35	0.39
t_{od}	0.62	0.65	0.71	0.84
Power (µW/MHz)				
Power_read	13.12	26.28	72.25	156.47
Power_write	22.32	43.46	93.98	262.00
Power_w_standby	1.51	2.25	3.70	6.51
Power_r_standby	0.10	0.12	0.25	0.36
Area (µm)				
Width	174.54	256.82	408.58	708.18
Height	216.88	297.20	472.80	824.00

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=4(nr=1, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**64**	**128**	**256**	**512**
bpw	**4**	**8**	**16**	**32**
Timing (ns)				
t_{wcyc}	1.40	1.53	1.79	2.46
t_{ckl}	1.09	1.08	1.06	1.06
t_{ckh}	0.26	0.28	0.38	0.67
t_{was}	0.77	0.74	0.70	0.64
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.16	1.15	1.12	1.12
t_{wh}	0.42	0.42	0.41	0.41
t_{ds}	0.85	0.82	0.78	0.72
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.96	2.21	2.40	2.72
t_{wacc}	2.02	2.24	2.40	2.86
t_{rcyc}	2.20	2.44	2.66	3.41
t_{acc}	2.20	2.44	2.66	3.41
t_{ras}	0.44	0.44	0.44	0.43
t_{rah}	0.14	0.15	0.16	0.17
t_{da}	0.93	0.97	1.06	1.22
t_{zd}	0.31	0.33	0.36	0.38
t_{dz}	0.27	0.29	0.32	0.36
t_{od}	0.61	0.63	0.67	0.76
Power (µW/MHz)				
Power_read	11.53	22.69	63.29	139.75
Power_write	23.13	42.45	89.56	235.72
Power_w_standby	1.92	2.33	3.07	4.52
Power_r_standby	0.10	0.13	0.25	0.36
Area (µm)				
Width	174.54	256.82	408.58	708.18
Height	216.88	297.20	472.80	824.00

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=8(nr=1, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**128**	**256**	**512**	**1024**
bpw	**2**	**4**	**8**	**16**
Timing (ns)				
t_{wcyc}	1.44	1.55	1.80	2.43
t_{ckl}	1.10	1.09	1.08	1.07
t_{ckh}	0.27	0.27	0.36	0.64
t_{was}	0.78	0.76	0.73	0.68
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.16	1.15	1.14	1.14
t_{wh}	0.42	0.42	0.43	0.41
t_{ds}	0.86	0.84	0.81	0.76
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	2.01	2.26	2.44	2.77
t_{wacc}	2.06	2.28	2.44	2.90
t_{rcyc}	2.23	2.47	2.69	3.45
t_{acc}	2.23	2.47	2.69	3.45
t_{ras}	0.44	0.44	0.44	0.43
t_{rah}	0.14	0.15	0.16	0.17
t_{da}	0.94	0.98	1.06	1.19
t_{zd}	0.30	0.32	0.33	0.38
t_{dz}	0.27	0.28	0.31	0.34
t_{od}	0.60	0.62	0.65	0.73
Power (µW/MHz)				
Power_read	10.93	20.97	59.50	130.82
Power_write	24.73	42.90	87.22	221.55
Power_w_standby	2.49	2.74	3.14	3.94
Power_r_standby	0.11	0.13	0.24	0.35
Area (µm)				
Width	174.54	256.82	408.58	708.18
Height	216.88	297.20	472.80	824.00

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=2(nr=1, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**32**	**64**	**128**	**256**
bpw	**8**	**16**	**32**	**64**
Timing (ns)				
t_{wcyc}	1.51	1.73	2.16	3.36
t_{ckl}	0.61	0.60	0.63	1.30
t_{ckh}	0.26	0.30	0.46	0.95
t_{was}	0.92	0.88	0.81	0.77
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.35	1.33	1.30	1.36
t_{wh}	0.27	0.27	0.27	0.27
t_{ds}	1.01	0.97	0.90	0.86
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.26	0.30	0.46	0.95
t_{wda}	2.08	2.44	2.66	3.00
t_{wacc}	2.01	2.29	2.55	3.13
t_{rcyc}	2.19	2.43	2.65	3.39
t_{acc}	2.19	2.43	2.65	3.39
t_{ras}	0.44	0.44	0.44	0.43
t_{rah}	0.14	0.15	0.16	0.18
t_{da}	0.93	0.99	1.11	1.31
t_{zd}	0.32	0.34	0.37	0.41
t_{dz}	0.28	0.30	0.35	0.39
t_{od}	0.62	0.65	0.71	0.84
Power (µW/MHz)				
Power_read	13.12	26.28	72.25	156.47
Power_write	22.61	47.55	108.79	327.22
Power_w_standby	1.23	2.01	3.57	6.91
Power_r_standby	0.10	0.12	0.25	0.36
Area (µm)				
Width	261.44	392.38	627.22	1088.62
Height	208.86	291.74	469.42	824.78

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=4(nr=1, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**64**	**128**	**256**	**512**
bpw	**4**	**8**	**16**	**32**
Timing (ns)				
t_{wcyc}	1.53	1.74	2.17	3.36
t_{ckl}	0.62	0.61	0.63	1.30
t_{ckh}	0.26	0.30	0.46	0.95
t_{was}	0.94	0.91	0.87	0.79
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.36	1.35	1.33	1.34
t_{wh}	0.27	0.27	0.27	0.27
t_{ds}	1.03	0.27	0.96	0.88
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.26	0.30	0.46	0.95
t_{wda}	2.14	2.51	2.73	3.08
t_{wacc}	2.07	2.35	2.61	3.19
t_{rcyc}	2.20	2.44	2.66	3.41
t_{acc}	2.20	2.44	2.66	3.41
t_{ras}	0.44	0.44	0.44	0.43
t_{rah}	0.14	0.15	0.16	0.17
t_{da}	0.93	0.97	1.06	1.22
t_{zd}	0.31	0.33	0.36	0.38
t_{dz}	0.27	0.29	0.32	0.36
t_{od}	0.61	0.63	0.67	0.82
Power (µW/MHz)				
Power_read	11.53	22.69	63.29	139.75
Power_write	23.68	47.39	105.72	326.95
Power_w_standby	1.31	1.80	2.67	4.63
Power_r_standby	0.10	0.13	0.25	0.36
Area (µm)				
Width	261.44	392.38	627.22	1088.62
Height	208.86	291.74	469.42	824.78

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=8(nr=1, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**128**	**256**	**512**	**1024**
bpw	**2**	**4**	**8**	**16**
Timing (ns)				
t_{wcyc}	1.58	1.75	2.18	3.37
t_{ckl}	0.63	0.63	0.63	1.30
t_{ckh}	0.30	0.30	0.44	0.93
t_{was}	0.95	0.93	0.89	0.84
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.36	1.36	1.34	1.34
t_{wh}	0.27	0.27	0.27	0.27
t_{ds}	1.04	1.02	0.98	0.93
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.30	0.30	0.44	0.93
t_{wda}	2.26	2.64	2.88	3.23
t_{wacc}	2.19	2.48	2.73	3.32
t_{rcyc}	2.23	2.47	2.69	3.45
t_{acc}	2.23	2.47	2.69	3.45
t_{ras}	0.44	0.44	0.44	0.43
t_{rah}	0.14	0.15	0.16	0.17
t_{da}	0.94	0.98	1.06	1.19
t_{zd}	0.30	0.32	0.33	0.38
t_{dz}	0.27	0.28	0.31	0.34
t_{od}	0.60	0.62	0.65	0.73
Power (µW/MHz)				
Power_read	10.93	20.97	59.50	130.82
Power_write	25.29	46.33	105.59	323.34
Power_w_standby	1.64	1.80	2.40	3.51
Power_r_standby	0.11	0.13	0.24	0.35
Area (µm)				
Width	261.44	392.38	627.22	1088.62
Height	208.86	291.74	469.42	824.78

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=2(nr=2, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**32**	**64**	**128**	**256**
bpw	**8**	**16**	**32**	**64**
Timing (ns)				
t_{wcyc}	1.39	1.53	1.81	2.54
t_{ckl}	1.08	1.06	1.03	1.08
t_{ckh}	0.26	0.29	0.38	0.69
t_{was}	0.75	0.72	0.65	0.62
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.15	1.13	1.10	1.15
t_{wh}	0.42	0.42	0.41	0.41
t_{ds}	0.84	0.80	0.73	0.71
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.94	2.19	2.38	2.71
t_{wacc}	1.99	2.22	2.38	2.84
t_{rcyc}	2.20	2.53	2.81	3.73
t_{acc}	2.20	2.53	2.81	3.73
t_{ras}	0.39	0.39	0.39	0.38
t_{rah}	0.12	0.14	0.15	0.16
t_{da}	0.90	0.97	1.09	1.27
t_{zd}	0.30	0.33	0.38	0.41
t_{dz}	0.28	0.31	0.37	0.40
t_{od}	0.54	0.59	0.69	0.93
Power (µW/MHz)				
Power_read	13.79	24.90	90.12	192.69
Power_write	22.32	43.46	93.98	262.00
Power_w_standby	1.51	2.25	3.70	6.51
Power_r_standby	0.16	0.27	0.53	0.98
Area (µm)				
Width	252.61	377.28	597.42	1028.76
Height	227.48	310.36	504.38	892.42

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=4(nr=2, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**64**	**128**	**256**	**512**
bpw	**4**	**8**	**16**	**32**
Timing (ns)				
t_{wcyc}	1.40	1.53	1.79	2.46
t_{ckl}	1.09	1.08	1.06	1.06
t_{ckh}	0.26	0.28	0.38	0.67
t_{was}	0.77	0.74	0.70	0.64
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.16	1.15	1.12	1.12
t_{wh}	0.42	0.42	0.41	0.41
t_{ds}	0.85	0.82	0.78	0.72
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	1.96	2.21	2.40	2.72
t_{wacc}	2.02	2.24	2.40	2.76
t_{rcyc}	2.25	2.58	2.86	3.79
t_{acc}	2.25	2.58	2.86	3.79
t_{ras}	0.39	0.39	0.39	0.38
t_{rah}	0.12	0.14	0.15	0.16
t_{da}	0.91	0.96	1.06	1.20
t_{zd}	0.29	0.31	0.35	0.38
t_{dz}	0.26	0.28	0.33	0.36
t_{od}	0.53	0.56	0.62	0.78
Power (μW/MHz)				
Power_read	12.35	24.06	78.28	164.28
Power_write	23.13	42.45	89.56	235.72
Power_w_standby	1.92	2.33	3.07	4.52
Power_r_standby	0.18	0.30	0.55	0.99
Area (μm)				
Width	252.61	377.28	597.42	1028.76
Height	227.48	310.36	504.38	892.42

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=8(nr=2, nw=1)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**128**	**256**	**512**	**1024**
bpw	**2**	**4**	**8**	**16**
Timing (ns)				
t_{wcyc}	1.44	1.55	1.80	2.43
t_{ckl}	1.10	1.09	1.08	1.07
t_{ckh}	0.27	0.27	0.36	0.64
t_{was}	0.78	0.76	0.73	0.68
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.16	0.15	1.14	1.14
t_{wh}	0.42	0.42	0.43	0.41
t_{ds}	0.86	0.84	0.81	0.76
t_{dh}	0.01	0.01	0.01	0.01
t_{wda}	2.01	2.26	2.44	2.77
t_{wacc}	2.06	2.28	2.44	2.90
t_{rcyc}	2.35	2.68	2.97	3.90
t_{acc}	2.35	2.68	2.97	3.90
t_{ras}	0.39	0.39	0.39	0.38
t_{rah}	0.13	0.14	0.15	0.16
t_{da}	0.95	1.00	1.07	1.18
t_{zd}	0.28	0.31	0.33	0.36
t_{dz}	0.25	0.27	0.30	0.34
t_{od}	0.52	0.55	0.59	0.70
Power (μW/MHz)				
Power_read	11.78	23.09	69.03	148.65
Power_write	24.73	42.90	87.22	221.55
Power_w_standby	2.49	2.74	3.14	3.94
Power_r_standby	0.19	0.33	0.59	1.05
Area (μm)				
Width	252.61	377.28	597.42	1028.76
Height	227.48	310.36	504.38	892.42

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=2(nr=2, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**32**	**64**	**128**	**256**
bpw	**8**	**16**	**32**	**64**
Timing (ns)				
t_{wcyc}	1.51	1.73	2.16	3.36
t_{ckl}	0.61	0.60	0.63	1.30
t_{ckh}	0.26	0.30	0.46	0.95
t_{was}	0.92	0.88	0.81	0.77
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.35	1.33	1.30	1.36
t_{wh}	0.27	0.27	0.27	0.27
t_{ds}	1.01	0.97	0.90	0.86
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.26	0.30	0.46	0.95
t_{wda}	2.08	2.44	2.66	3.00
t_{wacc}	2.01	2.29	2.55	3.13
t_{rcyc}	2.20	2.53	2.81	3.73
t_{acc}	2.20	2.53	2.81	3.73
t_{ras}	0.39	0.39	0.39	0.38
t_{rah}	0.12	0.14	0.15	0.16
t_{da}	0.90	0.97	1.09	1.27
t_{zd}	0.30	0.33	0.38	0.41
t_{dz}	0.28	0.31	0.37	0.40
t_{od}	0.54	0.59	0.69	0.93
Power (µW/MHz)				
Power_read	13.79	24.90	90.12	192.69
Power_write	22.61	47.55	108.79	327.22
Power_w_standby	1.23	2.01	3.57	6.91
Power_r_standby	0.16	0.27	0.53	0.98
Area (µm)				
Width	314.59	468.34	736.90	1262.10
Height	229.56	312.44	498.64	871.04

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

*** For Ymux=4(nr=2, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**64**	**128**	**256**	**512**
bpw	**4**	**8**	**16**	**32**
Timing (ns)				
t_{wcyc}	1.53	1.74	2.27	3.36
t_{ckl}	0.62	0.61	0.63	1.30
t_{ckh}	0.26	0.30	0.46	0.95
t_{was}	0.94	0.91	0.87	0.79
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.36	1.35	1.33	1.34
t_{wh}	0.27	0.27	0.27	0.27
t_{ds}	1.03	1.00	0.96	0.88
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.26	0.30	0.46	0.95
t_{wda}	2.14	2.51	2.73	3.08
t_{wacc}	2.07	2.35	2.61	3.19
t_{rcyc}	2.25	2.58	2.86	3.79
t_{acc}	2.25	2.58	2.86	3.79
t_{ras}	0.39	0.39	0.39	0.38
t_{rah}	0.12	0.14	0.15	0.16
t_{da}	0.91	0.96	1.06	1.20
t_{zd}	0.29	0.31	0.35	0.38
t_{dz}	0.26	0.28	0.33	0.36
t_{od}	0.53	0.56	0.62	0.78
Power (µW/MHz)				
Power_read	12.35	24.06	78.28	164.28
Power_write	23.68	47.39	105.72	326.95
Power_w_standby	1.31	1.80	2.67	4.63
Power_r_standby	0.18	0.30	0.55	0.99
Area (µm)				
Width	314.59	468.34	736.90	1262.10
Height	229.56	312.44	498.64	871.04

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

Reference Table

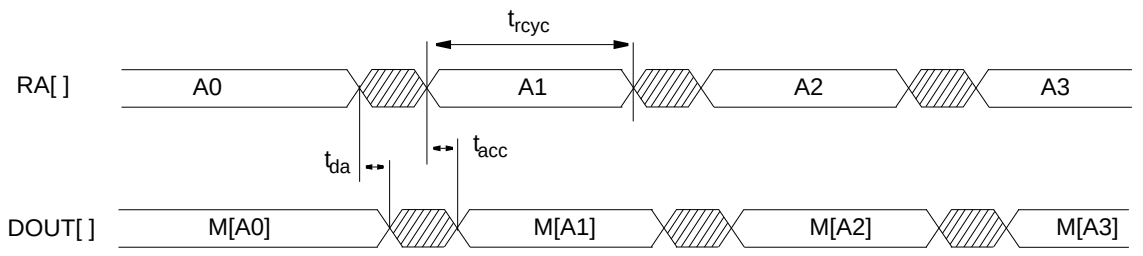
*** For Ymux=8(nr=2, nw=2)** (Typical process, 1.8V, 25°C, Output load=10SL, Input slope=0.2 ns, SA=0.5)

Parameters				
words	**128**	**256**	**512**	**1024**
bpw	**2**	**4**	**8**	**16**
Timing (ns)				
t_{wcyc}	1.58	1.75	2.18	3.37
t_{ckl}	0.63	0.63	0.63	1.30
t_{ckh}	0.30	0.30	0.44	0.93
t_{was}	0.95	0.93	0.89	0.84
t_{wah}	0.01	0.01	0.01	0.01
t_{ws}	1.36	1.36	1.34	1.34
t_{wh}	0.27	0.27	0.27	0.27
t_{ds}	1.04	1.02	0.98	0.93
t_{dh}	0.01	0.01	0.01	0.01
t_{wwc}	0.30	0.30	0.44	0.93
t_{wda}	2.26	2.64	2.88	3.23
t_{wacc}	2.19	2.48	2.73	3.32
t_{rcyc}	2.35	2.68	2.97	3.90
t_{acc}	2.35	2.68	2.97	3.90
t_{ras}	0.39	0.39	0.39	0.38
t_{rah}	0.13	0.14	0.15	0.16
t_{da}	0.95	1.00	1.07	1.18
t_{zd}	0.28	0.31	0.33	0.36
t_{dz}	0.25	0.27	0.30	0.34
t_{od}	0.52	0.55	0.59	0.70
Power (µW/MHz)				
Power_read	11.78	23.09	69.03	148.65
Power_write	25.29	46.33	105.59	323.34
Power_w_standby	1.64	1.80	2.40	3.51
Power_r_standby	0.19	0.33	0.59	1.05
Area (µm)				
Width	314.59	468.34	736.90	1262.10
Height	229.56	312.44	498.64	871.04

NOTE: SL is a standard load and SA is an input switching activity ratio during a clock.

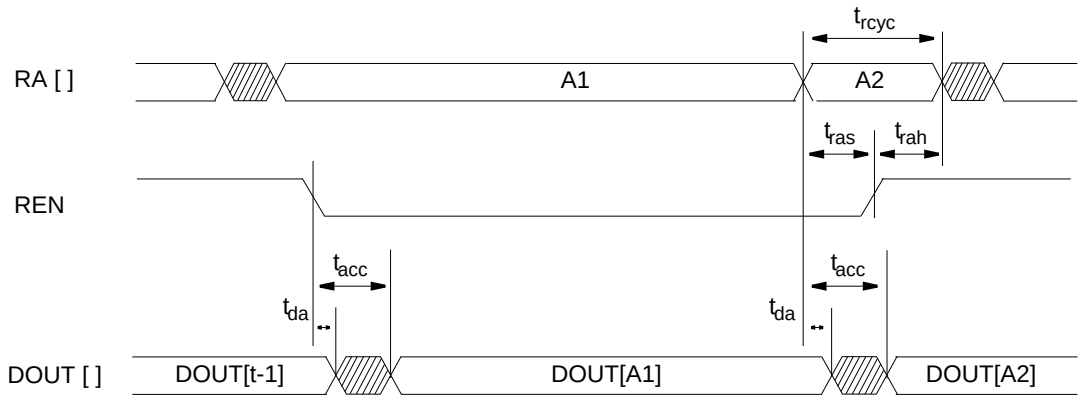
Timing Diagrams

Read Cycle



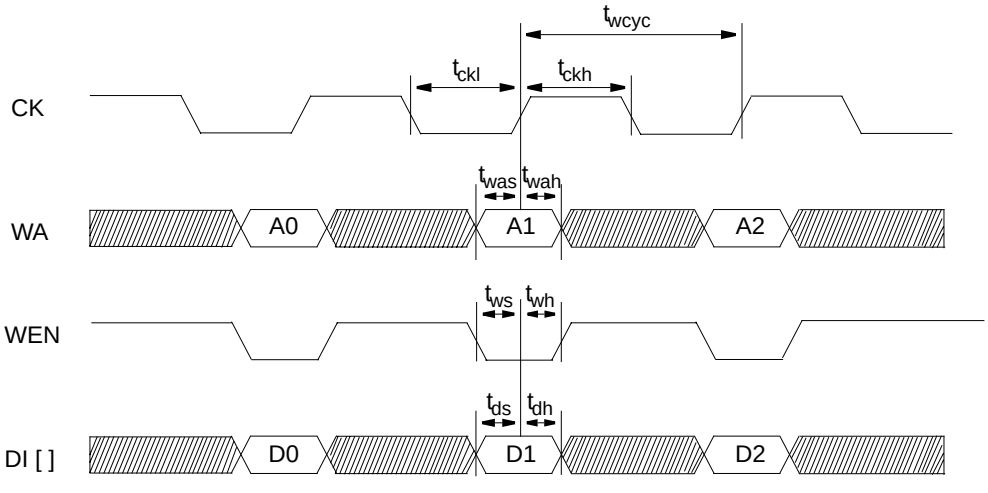
(OEN = low, REN= low, CK, WEN, DI[ ], WA[ ]= don't care)

Read Cycle with REN-Controlled



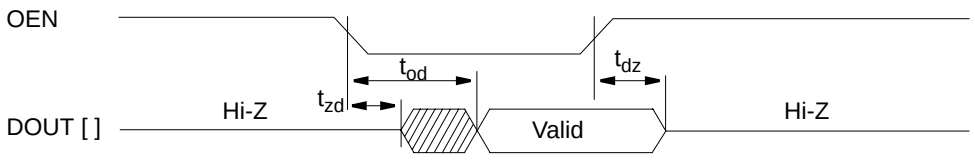
(OEN = low, CK, WEN, DI[ ], WA[ ] = don't care)

Write Cycle



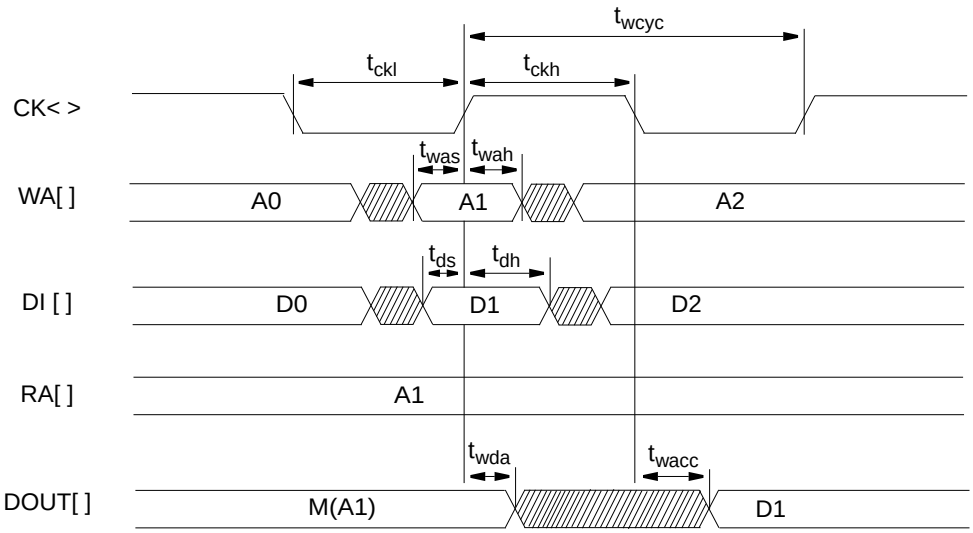
(REN, OEN, RA[ ] = don't care)

OEN Controlled Output Enable



(CK, REN, WEN, DI[ ], WA[ ], RA[ ] = don't care)

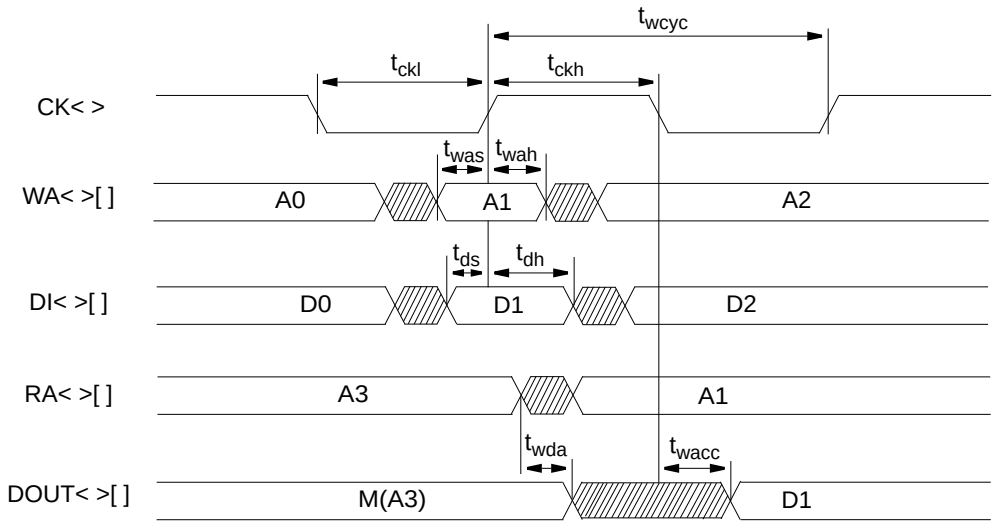
Read-Write Contention



(WA[ ] = RA[ ]; WEN, REN, OEN = low)

NOTE: If CK rise while WA[] is same as RA[], it is a read-write contention. While CK is high, DOUT[] is UNKNOWN and write data is valid. After twacc from the falling edge of CK, the read data (D1) is valid.

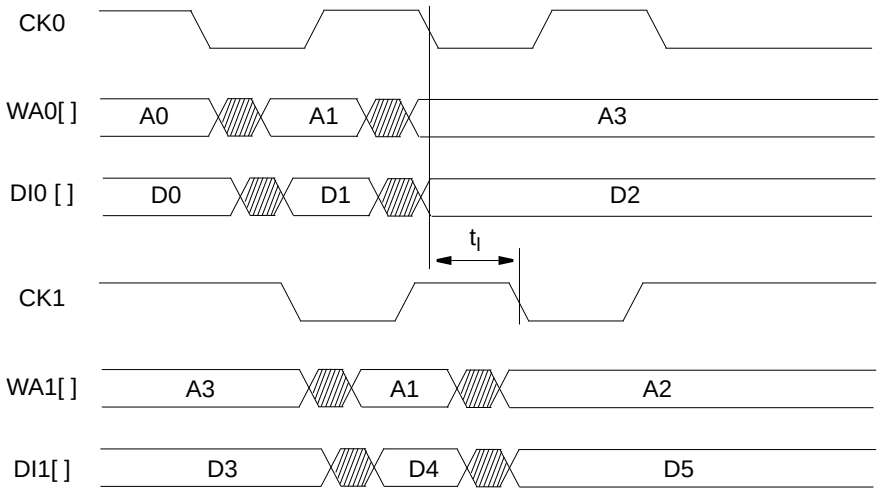
Write-Read Contention



(WA[ ] = RA[ ]; WEN, REN, OEN = low)

NOTE: While CK is high, if read access begins by RA<>[] which is same as WA<>[] latched at the rising edge of CK, it is Write-Read Contention. The read data is invalid whereas the write is still valid. After twacc from the falling edge of CK, DOUT[] is valid.

Write-Write Contention

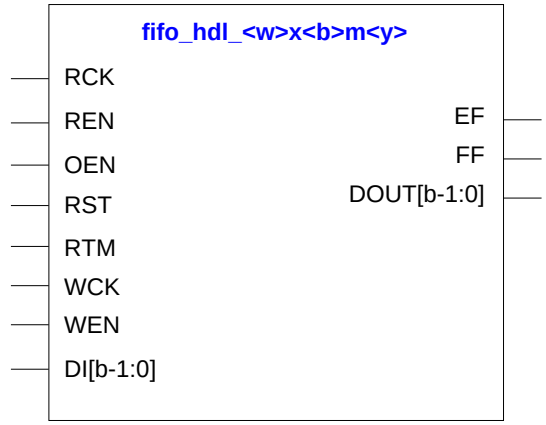


(WA0[ ] = WA1[ ]; WEN0, WEN1 = low, OEN, REN, RA[ ] = don't care)

NOTES:

1. If addresses latched at the rising edge of CK are same and t1 is smaller than or equal to twwc, it is Write-Write Contention. The data stored at current address will be unpredictable.
2. "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:
1. Words(w) is the number of words in FIFO_HDL
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.

Features

- Suitable for high-density applications
- Over-read and over-write protection capability
- Retransmit capability
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched full and empty status flag output
- Automatic power-down
- Flexible aspect ratio
- Up to 64Kbits capacity
- Up to 8K number of words
- Up to 64 number of bits per word

Function Description

FIFO_HDL is a synchronous first-in first-out buffer memory which is provided as a compiler. FIFO_HDL is intended for use in high-density applications. After valid reset, on the rising of WCK, the write cycle is initiated when WEN is low, RST is high and FF is low. The data on DI[] is written into the memory location specified by the write pointer. During normal write operation, the rising edge of WCK will reset EF if it is set. At the last available memory location, write operation will set FF. DI[] and WEN must satisfy the setup and hold requirements with respect to the rising edge of WCK.

On the rising edge of RCK, the read cycle is initiated when REN is low, RST is high, RTM is high and EF is low. The data located in the memory specified by the read pointer comes in DOUT[] after some delay. During normal read operation, the rising edge of RCK will reset FF if it is set. At the last available memory location with available data, read operation will set EF. A valid DOUT[] will be possibly in some specified time after the rising edge of RCK, under that OEN is low. And the output data will remain unchanged until the next read, reset, or retransmit mode come in. REN must satisfy the setup and hold requirements with respect to the rising edge of RCK. When OEN is high, DOUT[] is placed in a high-impedance state.

In reset mode, a reset is globally initiated at the falling edge of RST. The reset operation will set EF and reset FF and make the data output zero.The reset operation will initiate the read pointer and the write pointer as 0. After reset operation, the status of EF will make RCK inoperable. The valid write input signal will become operable as RST is high. The read input signal will remain inoperable until EF is reset by the first valid write.

In retransmit mode, a retransmit is initiated at the falling edge of RTM only if the total number of writes after a reset operation is less than the word size of the memory in FIFO_HDL and more than 0 (0 < total number of write < W-1). The retransmit operation will initiate the read pointer as 0 to allow the retransmission of data, make DOUT[] zero and make EF reset if it is set. The valid read input signal will become operable as RTM is high.

FIFO_HDL

High-Density Synchronous First-In First-Out Memory

FIFO_HDL Function Table

RST	WEN	WCK	REN	RCK	RTM	OEN	EF	FF	DI	DOUT	Comment
↓	X	X	X	X	X	X	↑	↓	X	L	Reset mode
H	X	X	X	X	↓	X	↓	X	X	L	Retransmit mode
H	X	X	L	↑	H	L	L	↓	X	DOUT(t)	Read mode
H	L	↑	X	X	X	X	↓	L	Valid	DOUT(t-1)	Write mode
H	X	X	L	↑	H	L	↑	L	X	DOUT(t)	Read and empty mode
H	L	↑	X	X	X	X	L	↑	Valid	DOUT(t-1)	Write and full mode
H	X	X	H	↑	H	L	X	X	X	DOUT(t-1)	(Note 1)
H	X	X	L	↑	H	L	H	X	X	DOUT(t-1)	(Note 2)
X	X	X	X	X	X	H	X	X	X	Hi-Z	(Note 3)
H	H	↑	X	X	X	X	X	X	Valid	DOUT(t-1)	(Note 4)
H	L	↑	X	X	X	X	X	H	Valid	DOUT(t-1)	(Note 5)

NOTES:

1. Read is blocked when REN is high and the read port is in disable mode.
2. Read is blocked when EF is high (overread protection).
3. Under that OEN is high, DOUT[] goes to tri-state output mode.
4. Write is blocked when WEN is high and the write port is in disable mode.
5. Write is blocked when FF is high (overwrite protection).

Parameter Description

FIFO_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 2	Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16
Words (w)	Min	16	32	64	128
	Max	1024	2048	4096	8192
	Step	w ≤ 128:16	w ≤ 256:32	w ≤ 512:64	w ≤ 1024:128
		w > 128:128	w > 256:256	w > 512:512	w > 1024:1024
Bpw (b)	Min	2	2	2	2
	Max	64	32	16	8
	Step	1	1	1	1

Pin Descriptions

Name	I/O	Description
RCK	Read Clock	Read Clock input. Upon the rising edge of RCK, it begins a read operation when REN is low, RST is high, RTM is high and EF is low.
REN	Read Enable	Read Enable input. When REN is low, the read access occurs properly. Conversely when REN is high, no read access can occur and the read port of the FIFO_HDL goes to power down mode. REN is latched at the rising edge of RCK.
OEN	Data Output Enable	Output Enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
RST	Reset	Reset input. Upon the falling edge of RST, the reset mode is initiated. With reset operation, the read and write pointer goes to their initial position. Reset operation sets EF and resets FF and makes DOUT[] zero.
RTM	Retransmit	Retransmit input. Upon the falling edge of RTM, the retransmit mode is initiated, provided that RST is high. With retransmit operation the read pointer goes to its initial position. Retransmit operation makes DOUT[] zero.
WCK	Write Clock	Write Clock input. Upon the rising edge of WCK, it begins a write operation when WE is low, RST is high and FF is low.
WEN	Write Enable	Write Enable input. When WEN is low, a write access occurs properly. Conversely when WEN is high, no write access can occur and the write port of the FIFO_HDL goes to power down mode. WEN is latched at the rising edge of WCK.
DI	Data In	Data input bus. DI[] is latched on the rising edge of WCK. Data input is written into the addressed location in write mode.
EF	Empty Flag	Empty Flag. If the memory has no data to be read, EF goes high. Valid reset makes EF high and valid retransmit makes it low.
FF	Full Flag	Full Flag. If the memory has no vacancy to write data, FF goes high. Valid reset makes FF low.
DOUT	Data Output	Data output bus. Data output is valid after the rising edge of RCK while the FIFO_HDL is in read mode when OEN is low. Conversely when OEN is high, DOUT[] goes to high-impedance state. By reset or retransmit operation. DOUT[] goes to 0.

Pin Capacitance

(Unit = SL)

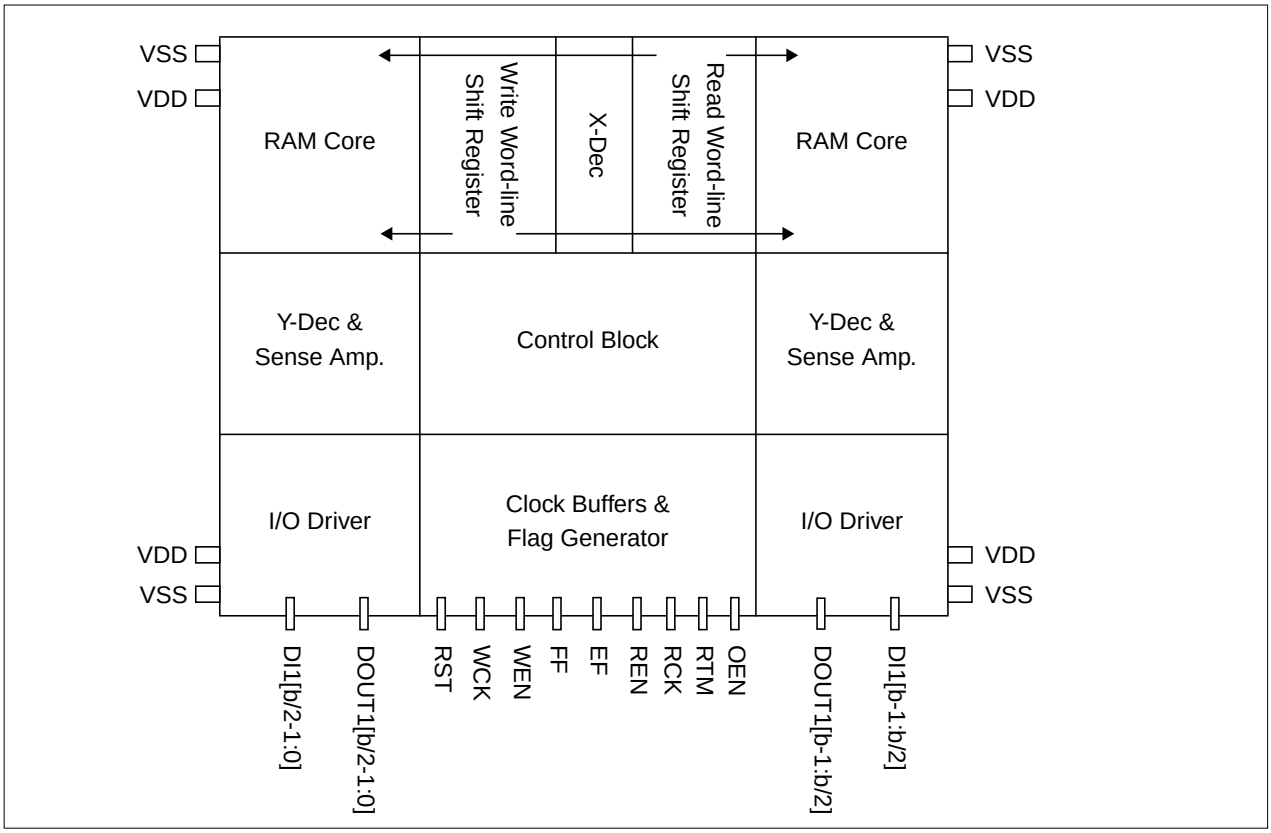
RST	RTM	WCK	RCK	OEN	WEN	REN	DI	DOUT
4.4040	1.9072	10.8532	5.8971	3.3375	2.2459	2.2961	1.5684	4.2033

FIFO_HDL

High-Density Synchronous First-In First-Out Memory

Block Diagrams

FIFO_HDL supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports are placed at the bottom side of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in FIFO_HDL is permitted for Metal-5 layer and Metal-6 layer.
2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.
3. Power stripe should be tapped from both sides of FIFO_HDL.
4. FIFO_HDL must be reset before any operation performed. The reset operation initiates the read pointer and the write pointer as 0.
5. FIFO_HDL should be reset again before resuming normal operation if abnormal operation is performed. Abnormal operations are invalid retransmit attemption, and read/write operation causing the timing requirement violations.
6. The retransmit operation initiates the read pointer as 0.
7. The retransmit is useful only when the total number of writes after a reset is less than the total word capacity of the FIFO_HDL and more than 0.
8. Outputs are not changed until first valid read after a reset or retransmit.

Characteristics

Definition for AC Timing (ns)		
Symbol	**Description**	**Unit**
t_{rst}	Min RST pulse width low	ns
t_{rtm}	Min RTM pulse width low	ns
t_{rcyc}	Read clock cycle time	ns
t_{rckh}	Read clock pulse width high	ns
t_{rckl}	Read clock pulse width low	ns
t_{wcyc}	Write clock cycle time	ns
t_{wckh}	Write clock pulse width high	ns
t_{wckl}	Write clock pulse width low	ns
t_{rs}	REN setup to RCK rising	ns
t_{rh}	REN hold from RCK rising	ns
t_{ws}	WEN setup to WCK rising	ns
t_{wh}	WEN hold from WCK rising	ns
t_{wrcs}	WCK setup to RCK rising	ns
t_{rwcs}	RCK setup to WCK rising	ns
t_{ds}	DI setup to WCK rising	ns
t_{dh}	DI hold from WCK rising	ns
t_{rstw}	RST setup to WCK rising	ns
t_{rtmr}	RTM setup to RCK rising	ns
t_{rste}	Delay from RST falling to EF rising	ns
t_{rstf}	Delay from RST falling to FF falling	ns
t_{rstd}	Delay from RST falling to DOUT zero	ns
t_{rstda}	Output hold time from RST falling to DOUT	ns
t_{rtme}	Delay from RTM falling to EF falling	ns
t_{rtmd}	Delay from RTM falling to DOUT zero	ns
t_{rtmda}	Output hold time from RTM falling to DOUT	ns
t_{we}	Delay from WCK rising to EF falling	ns
t_{wf}	Delay from WCK rising to FF rising	ns
t_{rf}	Delay from RCK rising to FF falling	ns
t_{re}	Delay from RCK rising to EF rising	ns
t_{acc}	Data access time	ns
t_{da}	De-access time	ns
t_{dz}	DOUT drive to high-Z time	ns
t_{zd}	DOUT high-Z to drive time	ns
t_{od}	OEN to valid output time	ns
Definition for Power Consumption (μW/MHz)		
Power_read	The dynamic average power consumption while in a read cycle	uW/MHZ
Power_write	The dynamic average power consumption while in a write cycle	uW/MHZ
Power_w_standby	The write standby power consumption while WEN is high	uW/MHZ
Power_r_standby	The read standby power consumption while REN is high	uW/MHZ
Definition for Area (μm)		
Width	The physical width in X-direction	um
Height	The physical height in Y-direction	um

FIFO_HDL

High-Density Synchronous First-In First-Out Memory

Reference Table

*** For Ymux=2** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters				
words	**64**	**128**	**384**	**1024**
bpw	**16**	**32**	**48**	**64**
Timing (ns)				
t_{rst}	4.59	4.59	4.60	5.32
t_{rtm}	4.49	4.49	4.50	5.22
t_{rcyc}	2.98	3.01	3.05	3.63
t_{rckl}	0.73	0.73	0.73	0.73
t_{rckh}	0.40	0.40	0.40	0.40
t_{wcyc}	2.57	2.62	2.69	3.30
t_{wckl}	0.83	0.86	0.90	0.93
t_{wckh}	0.67	0.71	0.75	0.80
t_{rs}	0.88	0.88	0.88	0.88
t_{rh}	0.01	0.01	0.01	0.01
t_{ws}	0.90	0.90	0.90	0.90
t_{wh}	0.01	0.01	0.01	0.01
t_{ds}	0.97	0.93	0.90	0.86
t_{dh}	0.01	0.01	0.01	0.01
t_{rstw}	0.50	0.50	0.50	0.50
t_{rtmr}	0.52	0.52	0.52	0.52
t_{wrcs}	1.30	1.30	1.30	1.30
t_{rwcs}	1.42	1.41	1.42	1.93
t_{rstd}	3.38	3.41	3.45	4.20
t_{rstda}	0.64	0.66	0.68	0.70
t_{rste}	4.54	4.54	4.55	5.27
t_{rstf}	4.54	4.54	4.55	5.27
t_{rtmd}	3.39	3.42	3.45	4.20
t_{rtmda}	0.65	0.67	0.69	0.71
t_{rtme}	4.11	4.11	4.11	4.84
t_{we}	0.90	0.90	0.90	0.90
t_{wf}	1.94	1.94	1.95	1.95
t_{re}	1.87	1.87	1.87	1.87
t_{rf}	0.98	0.98	0.98	0.98
t_{acc}	2.45	2.48	2.53	3.10
t_{da}	1.96	2.00	2.02	2.59
t_{dz}	0.31	0.33	0.35	0.37
t_{zd}	0.38	0.40	0.42	0.44
t_{od}	0.66	0.69	0.72	0.75
Power (µW/MHz)				
Power_read	57.84	94.57	130.89	181.44
Power_write	56.62	93.78	140.01	223.35
Power_w_standby	2.77	5.11	7.29	9.52
Power_r_standby	0.66	0.73	0.74	0.78
Area (µm)				
Width	463.54	636.34	809.14	981.94
Height	244.08	290.16	478.68	949.98

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters				
words	**128**	**256**	**768**	**2048**
bpw	**8**	**16**	**24**	**32**
Timing (ns)				
t_{rst}	4.59	4.59	4.61	5.32
t_{rtm}	4.49	4.49	4.61	5.22
t_{rcyc}	3.00	3.03	3.08	3.65
t_{rckl}	0.73	0.73	0.73	0.73
t_{rckh}	0.40	0.40	0.40	0.40
t_{wcyc}	2.57	2.62	2.69	3.30
t_{wckl}	0.82	0.85	0.87	0.89
t_{wckh}	0.67	0.70	0.72	0.75
t_{rs}	0.88	0.88	0.88	0.88
t_{rh}	0.01	0.01	0.01	0.01
t_{ws}	0.90	0.90	0.90	0.90
t_{wh}	0.01	0.01	0.01	0.01
t_{ds}	0.98	0.95	0.93	0.90
t_{dh}	0.01	0.01	0.01	0.01
t_{rstw}	0.50	0.50	0.50	0.50
t_{rtmr}	0.52	0.52	0.52	0.52
t_{wrcs}	1.30	1.30	1.30	1.30
t_{rwcs}	1.41	1.41	1.42	1.93
t_{rstd}	3.44	3.46	3.49	4.23
t_{rstda}	0.63	0.65	0.66	0.68
t_{rste}	4.54	4.54	4.56	5.27
t_{rstf}	4.54	4.54	4.56	5.27
t_{rtmd}	3.45	3.47	3.49	4.23
t_{rtmda}	0.64	0.66	0.67	0.69
t_{rtme}	4.11	4.11	4.12	4.84
t_{we}	0.90	0.90	0.90	0.90
t_{wf}	1.94	1.94	1.94	1.95
t_{re}	1.87	1.87	1.86	1.87
t_{rf}	0.98	0.98	0.98	0.98
t_{acc}	2.47	2.50	2.55	3.12
t_{da}	1.96	2.00	2.02	2.59
t_{dz}	0.30	0.32	0.33	0.34
t_{zd}	0.38	0.39	0.41	0.42
t_{od}	0.65	0.67	0.69	0.71
Power (µW/MHz)				
Power_read	53.38	86.40	119.91	165.92
Power_write	50.40	82.12	123.10	200.95
Power_w_standby	1.65	2.84	3.96	5.07
Power_r_standby	0.64	0.66	0.68	0.70
Area (µm)				
Width	463.54	636.34	809.14	981.94
Height	244.08	290.16	478.68	949.98

FIFO_HDL

High-Density Synchronous First-In First-Out Memory

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	**256**	**512**	**1536**	**4096**
bpw	**4**	**8**	**12**	**16**
Timing (ns)				
t_{rst}	4.59	4.59	4.60	5.32
t_{rtm}	4.49	4.49	4.50	5.22
t_{rcyc}	2.98	3.07	3.11	3.69
t_{rckl}	0.73	0.73	0.73	0.73
t_{rckh}	0.40	0.40	0.40	0.40
t_{wcyc}	2.56	2.62	2.69	3.30
t_{wckl}	0.81	0.83	0.85	0.87
t_{wckh}	0.68	0.70	0.72	0.74
t_{rs}	0.88	0.88	0.88	0.88
t_{rh}	0.01	0.01	0.01	0.01
t_{ws}	0.90	0.90	0.90	0.90
t_{wh}	0.01	0.01	0.01	0.01
t_{ds}	0.99	0.97	0.95	0.93
t_{dh}	0.01	0.01	0.01	0.01
t_{rstw}	0.50	0.50	0.50	0.50
t_{rtmr}	0.52	0.52	0.52	0.52
t_{wrcs}	1.30	1.30	1.30	1.30
t_{rwcs}	1.41	1.41	1.42	1.93
t_{rstd}	3.57	3.59	3.61	4.35
t_{rstda}	0.63	0.64	0.65	0.67
t_{rste}	4.54	4.54	4.55	5.27
t_{rstf}	4.54	4.54	4.55	5.27
t_{rtmd}	3.58	3.60	3.61	4.35
t_{rtmda}	0.64	0.65	0.67	0.68
t_{rtme}	4.11	4.11	4.11	4.84
t_{we}	0.90	0.90	0.90	0.90
t_{wf}	1.94	1.94	1.95	1.95
t_{re}	1.87	1.87	1.87	1.87
t_{rf}	0.98	0.98	0.98	0.98
t_{acc}	2.50	2.54	2.58	3.15
t_{da}	1.97	2.00	2.02	2.59
t_{dz}	0.30	0.31	0.32	0.33
t_{zd}	0.38	0.39	0.40	0.41
t_{od}	0.64	0.66	0.68	0.70
Power (µW/MHz)				
Power_read	51.17	82.31	113.23	158.30
Power_write	47.22	76.34	114.46	189.66
Power_w_standby	1.07	1.73	2.30	2.84
Power_r_standby	0.63	0.64	0.66	0.66
Area (µm)				
Width	463.54	636.34	809.14	981.94
Height	244.08	290.16	478.68	949.98

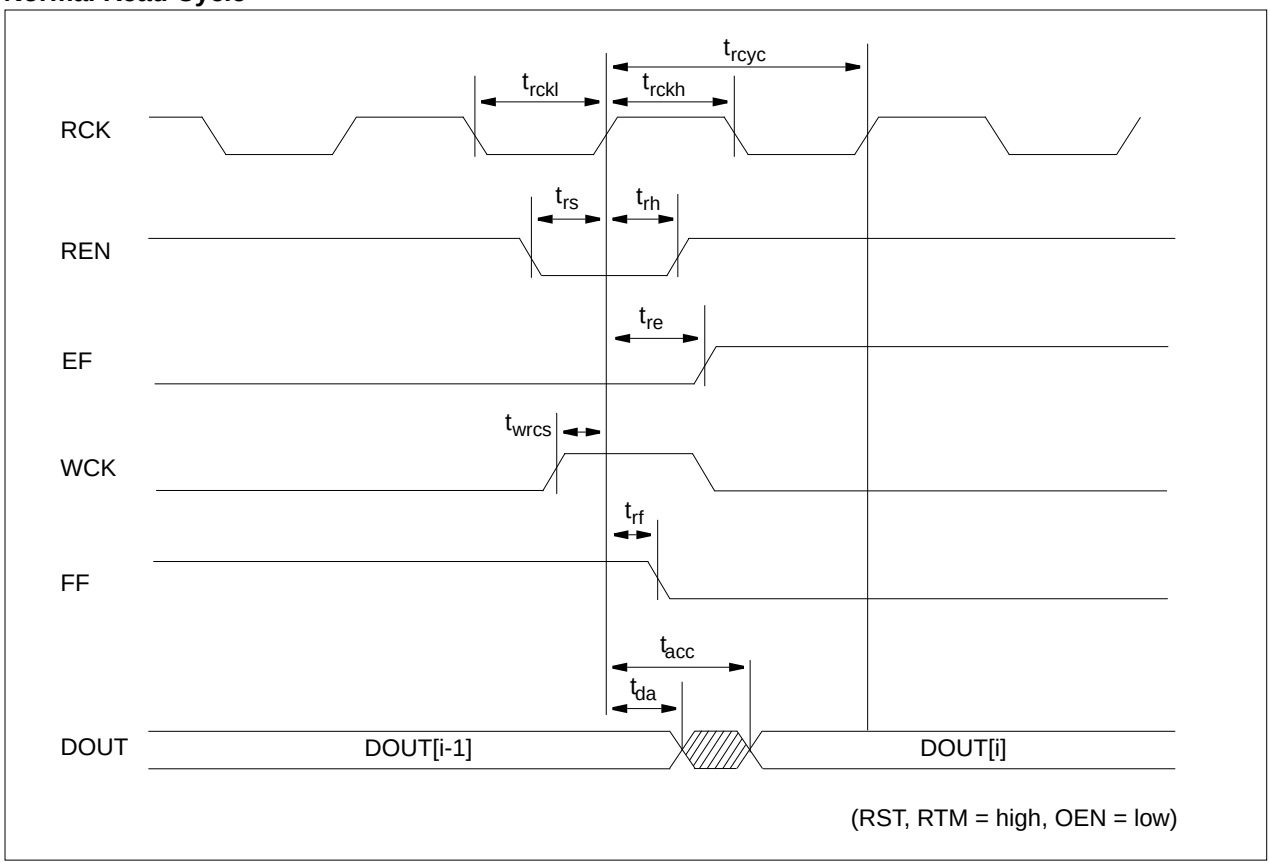
Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters				
words	**512**	**1024**	**3072**	**8192**
bpw	**2**	**4**	**6**	**8**
Timing (ns)				
t_{rst}	4.59	4.59	4.60	5.32
t_{rtm}	4.49	4.49	4.50	5.22
t_{rcyc}	3.11	3.14	3.19	3.76
t_{rckl}	0.73	0.73	0.73	0.73
t_{rckh}	0.40	0.40	0.40	0.40
t_{wcyc}	2.56	2.62	2.69	3.30
t_{wckl}	0.81	0.83	0.84	0.86
t_{wckh}	0.70	0.72	0.73	0.75
t_{rs}	0.88	0.88	0.88	0.88
t_{rh}	0.01	0.01	0.01	0.01
t_{ws}	0.90	0.90	0.90	0.90
t_{wh}	0.01	0.01	0.01	0.01
t_{ds}	0.99	0.97	0.95	0.84
t_{dh}	0.01	0.01	0.01	0.01
t_{rstw}	0.50	0.50	0.50	0.50
t_{rtmr}	0.52	0.52	0.52	0.52
t_{wrcs}	1.30	1.30	1.30	1.30
t_{rwcs}	1.40	1.41	1.42	1.93
t_{rstd}	3.82	3.83	3.85	4.59
t_{rstda}	0.63	0.64	0.65	0.66
t_{rste}	4.54	4.54	4.55	5.27
t_{rstf}	4.54	4.54	4.55	5.27
t_{rtmd}	3.82	3.84	3.86	4.59
t_{rtmda}	0.64	0.65	0.66	0.67
t_{rtme}	4.11	4.11	4.11	4.84
t_{we}	0.90	0.90	0.90	0.90
t_{wf}	1.94	1.94	1.95	1.95
t_{re}	1.87	1.87	1.87	1.87
t_{rf}	0.98	0.98	0.98	0.98
t_{acc}	2.57	2.60	2.64	3.22
t_{da}	1.97	2.00	2.02	2.59
t_{dz}	0.29	0.31	0.32	0.33
t_{zd}	0.38	0.39	0.40	0.41
t_{od}	0.64	0.66	0.67	0.69
Power (µW/MHz)				
Power_read	50.01	80.36	110.31	154.37
Power_write	45.11	73.41	110.14	184.08
Power_w_standby	0.61	1.20	1.45	1.71
Power_r_standby	0.61	0.65	0.63	0.61
Area (µm)				
Width	463.54	636.34	809.14	981.94
Height	244.08	290.16	478.68	949.98

Timing Diagrams

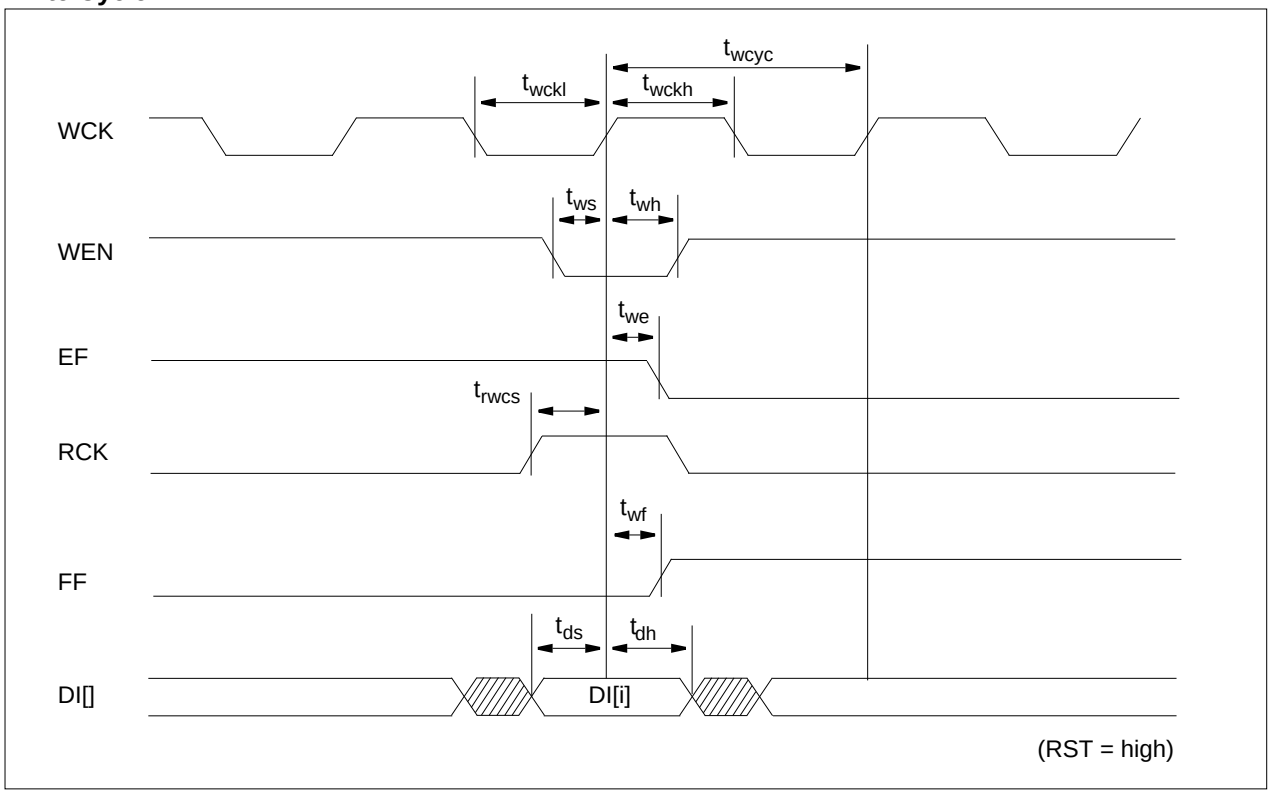
Normal Read Cycle



NOTES:

1. Read cycle is blocked during empty state (over-read protected)
2. Twrcs is the timing related between first write on empty state and first subsequent read. If it is not satisfied, DOUT[i] will be unpredictable.
3. Tre is the timing related the read and empty mode.

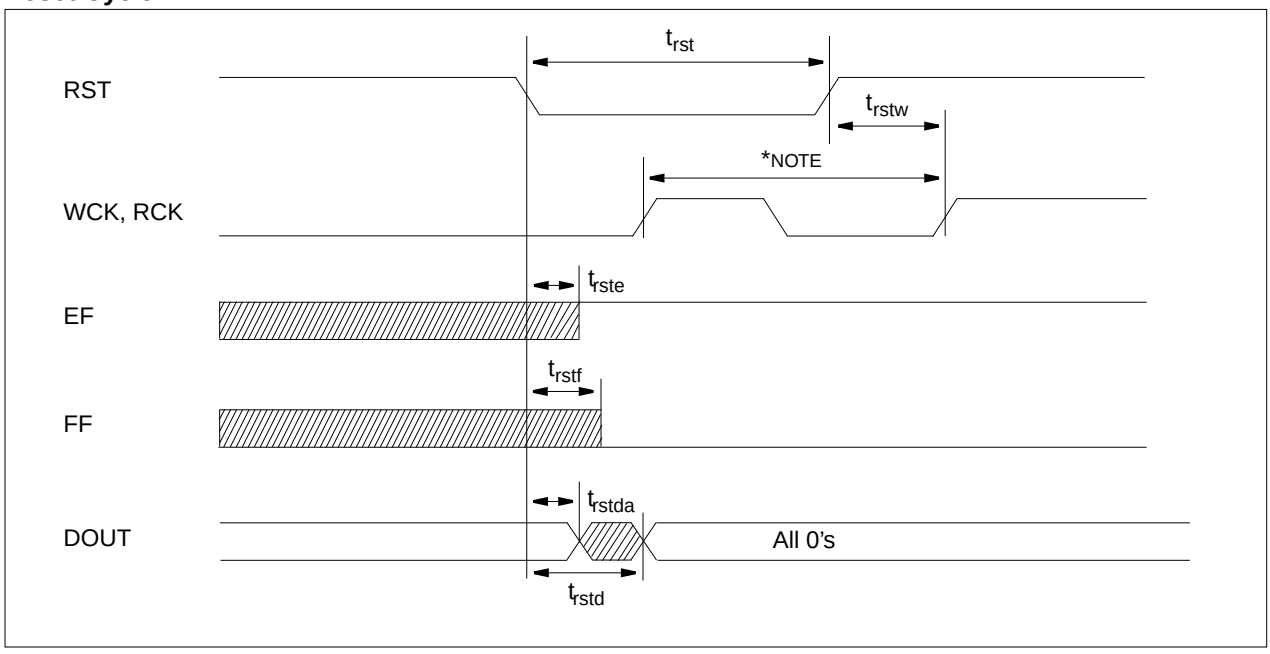
Write Cycle



NOTES:

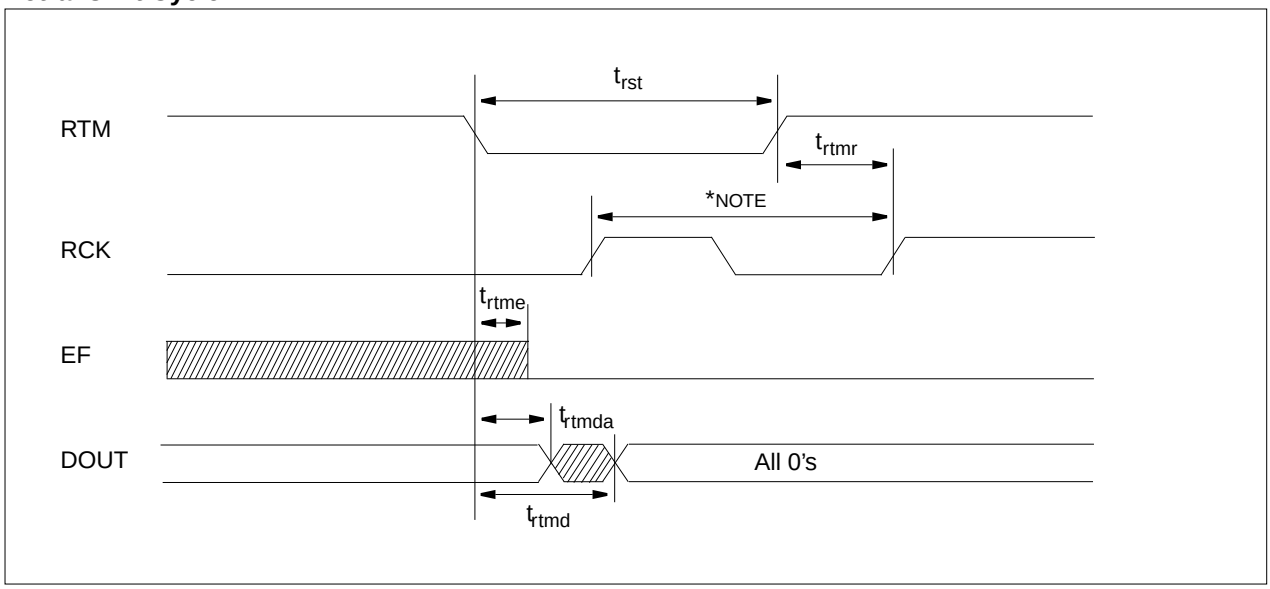
1. Write cycle is blocked during full state (over-write protected)
2. Trwcs is the timing related between first read on full state and first subsequent write. If it is not satisfied, DOUT[i] (not shown) will be unpredictable.
3. Twf is the timing related the write and full mode.

Reset Cycle



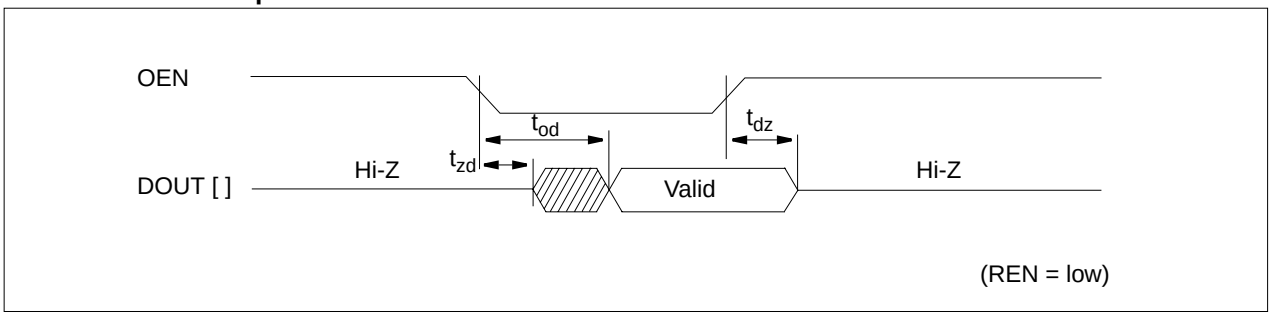
NOTE: Read cycle and write cycle are blocked when RST is low.

Retransmit Cycle

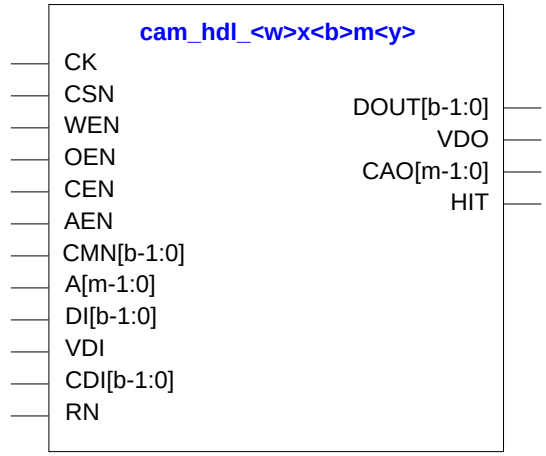


NOTE: Read cycle is blocked when RTM is low.

OEN Controlled Output Enable



Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for high-density application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Single cycle compare operation
- Low noise output optimization
- Global hit/miss
- Built-in priority address encoder
- Asynchronous reset control for all the valid-bits
- Up to 32Kbits capacity
- Up to 512 number of words
- Up to 64 number of bit per word

Function Description

CAM_HDL is a single-port synchronous binary CAM which is provided as a compiler. CAM_HDL is intended for use in high-density applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low and CEN and RN are high. The data on DI[] is written to the addressed CAM location and VDI overwrites the valid bit associated with CAM entry with the state selected by A[], and DOUT[], VDO, CAO[] and HIT remains stable during a normal write access cycle. On the rising edge of CK, the read cycle begins when WEN is high and CSN is low and CEN and RN are high. The data at DOUT[] become valid after a delay and VDO,during a normal read access cycle, reads back the valid bit associated with the A[] selected by CAM entry. On the rising edge of CK, the compare cycle starts when CSN and CEN are low and RN are high, All valid data entries in the CAM are simultaneously searched for the match pattern (CDI[]) defined by mask pattern(CMN[]). CDI[] bits are considered as matched bits at all times, if the corresponding bits of the applied CMN[] are in low states. Each CAM entry can be excluded from the compare function by setting the associated valid bit to a low state by the use of VDI. If one or more entries match with the masked CMN[] pattern, HIT will be asserted and CAO[] will contain the lowest one of all matched addresses by the built-in priority address encoder. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[], VDO, CAO[] and HIT remains stable. When OEN is high, DOUT[] and VDO are placed in a high-impedance state. When AEN is high, CAO[] is placed in a high-impedance state. On the falling edge of RN, all the valid-bits are invalidated and setted to low states, therefore all the entries are excluded from CAM match function so no match can occur. A low state of RN inhibits all access, same as when CSN is in a high state.

CAM_HDL

High-Density Single-Port Synchronous Binary CAM

CAM_HDL Function Table

CK	CSN	RN	WEN	AEN	OEN	A	DI/ VDI	CDI	CMN	CEN	DOUT/ VDO	HIT	CAO	Comment
X	X	L	X	L	L	X	X	X	X	X	X	X	X	Reset
X	H	H	X	L	L	X	X	X	X	X	UNCH	UNCH	UNCH	Idle
X	X	X	X	H	H	X	X	X	X	X	Z	UNCH	Z	Tri-state
↑	L	H	L	L	L	Valid	Valid	X	X	H	UNCH	UNCH	UNCH	Write
↑	L	H	H	L	L	Valid	X	X	X	H	Data-out	UNCH	UNCH	Read
↑	L	H	X	L	L	X	X	Valid	Valid	L	UNCH	1	Lowest of all matched addresses	Matched compare cycle
↑	L	H	X	L	L	X	X	Valid	Valid	L	UNCH	0	0	Missed compare cycle

NOTES:

1. DOUT and VDO are high impedance when OEN is high.
2. CAO is high impedance when AEN is high.
3. HIT is 1 if matched or 0 if not.
4. Match pattern is defined by CDI, bit-wise enabled by CMN.

Parameter Description

CAM_HDL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w) and Number of bit per word(b) and column mux(y).

Parameters	Min	Max	Step	Note
Address Inputs(m)	3	8	1	Words(w) is limited to one (8, 16, 32, 64, 128, 256, 512)
Words (w)	8	512	Note	
Bpw (b)	2	64	1	
Mux(y)	1	1	-	
Capacity	16	32K	-	

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[], DI[], CDI[], CMN[], VDI and CEN are latched into the CAM on the rising edge of CK. If CSN and WEN are low and CEN and RN are high on the rising edge of CK, the CAM is in write mode. If CSN is low and WEN is high and CEN and RN are high on the rising edge of CK, the CAM is in read mode. If CSN and CEN are low and RN is high on the rising edge of CK, the CAM is in compare mode.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the CAM on the rising edge of CK. When CSN is low and RN is high, the CAM is enabled for reading, writing or comparing, depending on the state of WEN and CEN. When CSN is high and RN is high, the CAM goes to the standby mode and is disabled for reading or writing or comparing. DOUT[], VDO, HIT and CAO[] remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the CAM on the rising edge of CK depending on the state of CEN. When CSN and WEN is low and CEN and RN are high, data are written to the addressed location and DOUT[], VDO, HIT and CAO[] remains stable. When CSN is low and WEN is high and CEN and RN are high, data from the addressed word are present at DOUT[] and VDO, whereas HIT and CAO[] remains stable.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of any input. When OEN is high, DOUT[] and VDO are disabled and go to high-impedance state.
CEN	Compare Enable	Compare enable input. The compare enable is latched into the CAM on the rising edge of CK. When CSN and CEN is low and RN is high, the CAM match function is activated. When CSN is low and CEN and RN are high, only read-write accesses are permitted.
AEN	Address Output Enable	Address output enable input. The address output enable is asynchronously operated regardless of any input. When AEN is high, CAO[] is disabled and goes to high-impedance state.
CMN [ ]	Compare Mask Input	Compare mask input bus. CMN[] defines the pattern which enables the CDI[] pattern to be used for the CAM match function. If the CMN[] bit is low, the corresponding CDI[] bit will be interpreted as a wild card.
A [ ]	Address	Address input bus. The address is latched into the CAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
VDI	Valid Bit Input	Valid Bit Input. VDI overwrites the valid bit associated with the CAM entry with the state selected by A[], during a normal write access cycle. Valid Bit Input are latched on the rising edge of CK.
CDI [ ]	Compare Data Input	Compare Data input bus. Compare-data are latched on the rising edge of CK and define the data pattern to be matched with the CAM entries, in conjunction to CMN[].
RN	Reset Enable	Reset Enable. RN, if low, invalidates all the CAM entries by setting all the valid-bits, one per entry,to low states,therefore all the entries are excluded from CAM match function so no match can occur. A low state of RN inhibits all access, same as when CSN is in a high state.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the CAM is in read mode. Data output remains previous data output while the CAM is in write mode and compare mode.
VDO	Valid Bit Output	Valid bit output. VDO, during a normal read access cycle, reads back the valid bit associated with the A[] selected by CAM entry.
CAO [ ]	Address Output	Address output bus. CAO[] presents the address of the matched entry, in a single match case. In a multiple-match case, CAO[] is the lowest one of all matched addresses by the built-in priority address encoder.
HIT	Match Output	Match Output. HIT indicates one or more CAM entries matched the masked CDI[], if high.

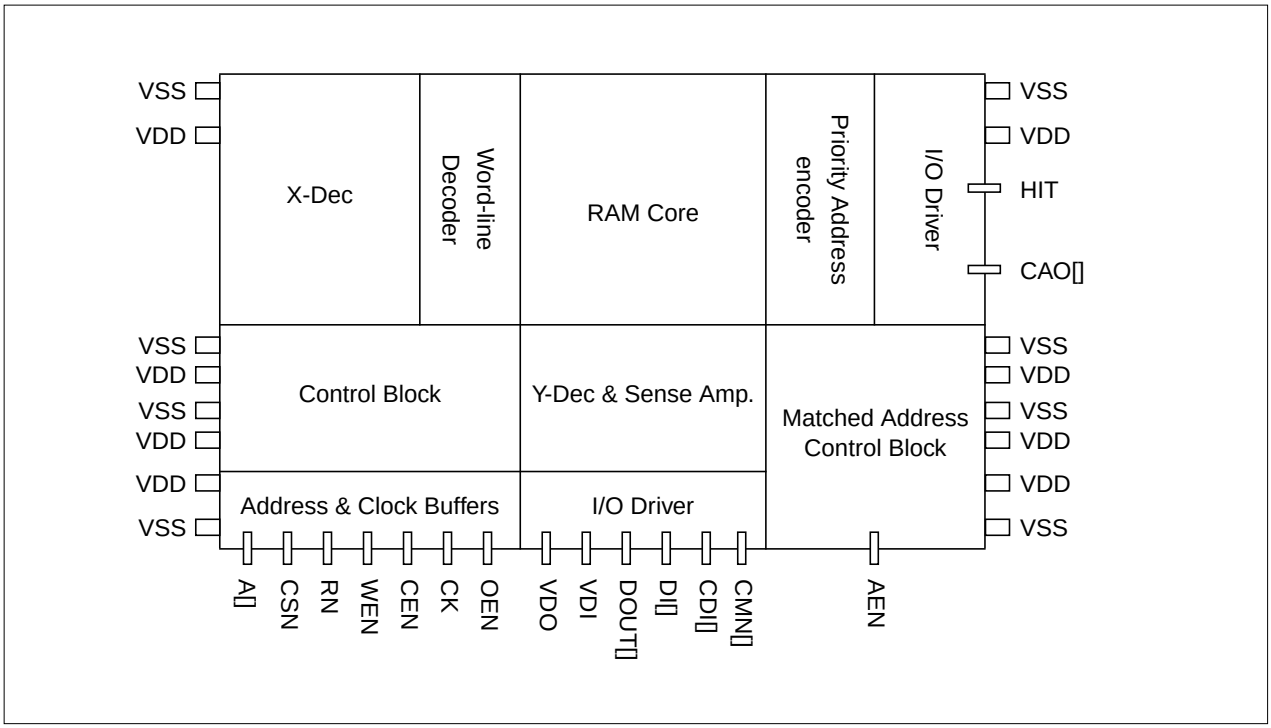
Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	CEN	AEN	CMN	A
2.7794	0.4577	0.9217	0.4577	0.9217	0.9898	0.9217	0.9217
DI	**VDI**	**CDI**	**RN**	**DOUT**	**CDO**	**CAO**	
0.9217	0.9217	0.9217	0.4577	10.8488	10.8488	10.8488	

Block Diagrams

CAM_HDL supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. All signal ports except HIT and CAO are located on the bottom of the memory. HIT and CAO are located on the right-edge of the memory.



Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in CAM_HDL is permitted only for Metal-5 layer or upper layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of CAM_HDL.

4. Power reduction during standby mode. The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{da}	De-access time
t_{ckl}	Clock pulse width low	t_{vdacc}	Validity data access time
t_{ckh}	Clock pulse width high	t_{vdda}	Validity data de-access time
t_{as}	Address setup time	t_{caacc}	Matched address access time
t_{ah}	Address hold time	t_{cada}	Matched address de-access time
t_{cs}	CSN setup time	t_{htacc}	Global Hit/Miss access time
t_{ch}	CSN hold time	t_{htda}	Global Hit/Miss de-access time
t_{ds}	Data-In setup time	t_{dz}	DOUT drive to high-Z time
t_{dh}	Data-In hold time	t_{zd}	DOUT high-Z to drive time
t_{ws}	WEN setup time	t_{od}	OEN to valid output time
t_{wh}	WEN hold time	t_{vddz}	VDO drive to high-Z time
t_{ces}	CEN setup time	t_{vdzd}	VDO high-Z to drive time
t_{ceh}	CEN hold time	t_{vdod}	OEN to valid output time for VDO
t_{cms}	CMN setup time	t_{cadz}	CAO drive to high-Z time
t_{cmh}	CMN hold time	t_{cazd}	CAO high-Z to drive time
t_{vds}	VDI setup time	t_{caod}	AEN to valid output time for CAO
t_{vdh}	VDI hold time	t_{rn}	Min RN pulse width low
t_{cds}	CDI setup time	t_{rns}	RN setup time
t_{cdh}	CDI hold time	t_{rnh}	RN hold time
t_{acc}	Data access time		

Definition for Power Consumption (μW/MHz)	
Power_read	The dynamic average power consumption while in a read cycle
Power_write	The dynamic average power consumption while in a write cycle
Power_compare	The dynamic average power consumption while in a compare cycle
Power_reset	The dynamic average power consumption while in a reset mode
Power_standby	The standby power consumption while CSN and RN are high, OEN and AEN are low and other signals are in normal operations

Definition for Area (μm)	
Width	The physical width in X-direction
Height	The physical height in Y-direction

Reference Table

*** For Ymux=1** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parametersy						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**8**	**8**	**8**	**8**	**8**	**8**
Timing (ns)						
t_{cyc}	4.10	4.15	4.25	5.39	6.69	8.21
t_{ckl}	1.03	1.05	1.07	1.09	1.10	1.12
t_{ckh}	1.10	1.10	1.10	1.10	1.10	1.10
t_{as}	0.35	0.35	0.35	0.35	0.35	0.35
t_{ah}	0.34	0.37	0.40	0.44	0.47	0.50
t_{cs}	1.03	1.05	1.07	1.09	1.10	1.12
t_{ch}	0.69	0.69	0.69	0.69	0.69	0.69
t_{ces}	0.55	0.57	0.59	0.61	0.62	0.64
t_{ceh}	0.69	0.69	0.69	0.69	0.69	0.69
t_{cms}	0.34	0.34	0.34	0.34	0.34	0.34
t_{cmh}	0.41	0.41	0.41	0.41	0.41	0.41
t_{ds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{dh}	0.45	0.45	0.45	0.45	0.45	0.45
t_{vds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{vdh}	0.45	0.45	0.45	0.45	0.45	0.45
t_{cds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{cdh}	0.41	0.41	0.41	0.41	0.41	0.41
t_{ws}	0.28	0.28	0.28	0.28	0.28	0.28
t_{wh}	0.34	0.37	0.40	0.44	0.47	0.50
t_{acc}	2.02	2.07	2.16	2.32	2.63	3.26
t_{da}	1.77	1.82	1.91	2.07	2.38	3.01
t_{dz}	0.48	0.48	0.48	0.48	0.48	0.48
t_{zd}	0.61	0.61	0.61	0.61	0.61	0.61
t_{od}	0.69	0.69	0.69	0.69	0.69	0.69
t_{vdacc}	2.02	2.07	2.16	2.32	2.63	3.26
t_{vdda}	1.77	1.82	1.91	2.07	2.38	3.01
t_{vddz}	0.48	0.48	0.48	0.48	0.48	0.48
t_{vdzd}	0.61	0.61	0.61	0.61	0.61	0.61
t_{vdod}	0.69	0.69	0.69	0.69	0.69	0.69
t_{caacc}	3.22	3.36	3.74	4.43	5.46	6.69
t_{cada}	2.09	2.16	2.29	2.84	3.51	4.35
t_{cadz}	0.42	0.45	0.48	0.55	0.68	0.96
t_{cazd}	0.60	0.62	0.65	0.71	0.83	1.09
t_{caod}	0.68	0.70	0.73	0.79	0.90	1.16
t_{htacc}	2.90	3.12	3.40	4.11	4.94	5.92
t_{htda}	2.09	2.16	2.29	2.84	3.51	4.35
t_{rn}	3.30	3.35	3.45	4.59	5.89	7.41
t_{rns}	1.03	1.05	1.07	1.09	1.10	1.12
t_{rnh}	3.30	3.35	3.45	4.09	5.89	7.41
Power (µW/MHz)						
Power_read	20.36	22.92	26.45	32.57	45.09	72.44
Power_write	18.96	22.13	27.87	39.33	63.17	108.83
Power_compare	68.00	78.54	94.38	125.18	180.78	283.36
Power_standby	0.46	0.50	0.59	0.66	0.79	1.08
Power_reset	1.25	2.02	3.50	6.79	14.83	36.56
Area (µm)						
Width	210.48	232.12	253.76	275.40	297.06	318.70
Height	382.08	455.04	600.96	892.80	1476.48	2643.84

Reference Table

*** For Ymux=1** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**16**	**16**	**16**	**16**	**16**	**16**
Timing (ns)						
t_{cyc}	4.41	4.46	4.56	5.69	7.01	8.56
t_{ckl}	1.03	1.05	1.07	1.09	1.10	1.12
t_{ckh}	1.10	1.10	1.10	1.10	1.10	1.10
t_{as}	0.35	0.35	0.35	0.35	0.35	0.35
t_{ah}	0.34	0.37	0.40	0.44	0.47	0.50
t_{cs}	1.03	1.05	1.07	1.09	1.10	1.12
t_{ch}	0.69	0.69	0.69	0.69	0.69	0.69
t_{ces}	0.55	0.57	0.59	0.61	0.62	0.64
t_{ceh}	0.69	0.69	0.69	0.69	0.69	0.69
t_{cms}	0.34	0.34	0.34	0.34	0.34	0.34
t_{cmh}	0.45	0.45	0.45	0.45	0.45	0.45
t_{ds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{dh}	0.49	0.49	0.49	0.49	0.49	0.49
t_{vds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{vdh}	0.49	0.49	0.49	0.49	0.49	0.49
t_{cds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{cdh}	0.45	0.45	0.45	0.45	0.45	0.45
t_{ws}	0.28	0.28	0.28	0.28	0.28	0.28
t_{wh}	0.34	0.37	0.40	0.44	0.47	0.50
t_{acc}	2.10	2.15	2.24	2.41	2.72	3.35
t_{da}	1.85	1.90	1.99	2.16	2.47	3.10
t_{dz}	0.53	0.53	0.53	0.53	0.53	0.53
t_{zd}	0.65	0.65	0.65	0.65	0.65	0.65
t_{od}	0.73	0.73	0.73	0.73	0.73	0.73
t_{vdacc}	2.10	2.15	2.24	2.41	2.72	3.35
t_{vdda}	1.85	1.90	1.99	2.16	2.47	3.10
t_{vddz}	0.53	0.53	0.53	0.53	0.53	0.53
t_{vdzd}	0.65	0.65	0.65	0.65	0.65	0.65
t_{vdod}	0.73	0.73	0.73	0.73	0.73	0.73
t_{caacc}	3.44	3.57	3.96	4.64	5.68	6.94
t_{cada}	2.30	2.37	2.51	3.06	3.74	4.63
t_{cadz}	0.43	0.45	0.48	0.55	0.68	0.96
t_{cazd}	0.60	0.62	0.65	0.71	0.83	1.09
t_{caod}	0.68	0.70	0.73	0.79	0.90	1.17
t_{htacc}	3.11	3.33	3.62	4.32	5.16	6.18
t_{htda}	2.30	2.37	2.51	3.06	3.74	4.63
t_{rn}	3.61	3.66	3.76	4.89	6.21	7.76
t_{rns}	1.03	1.05	1.07	1.09	1.10	1.12
t_{rnh}	3.61	3.66	3.76	4.89	6.21	7.76
Power (µW/MHz)						
Power_read	28.68	31.93	35.93	42.70	56.11	85.40
Power_write	26.05	30.39	38.43	54.50	88.27	151.22
Power_compare	104.19	117.94	140.05	183.33	263.20	410.25
Power_standby	0.58	0.61	0.75	0.83	1.01	1.42
Power_reset	1.25	2.04	3.51	6.85	14.87	36.67
Area (µm)						
Width	255.44	277.08	298.72	320.36	342.02	363.66
Height	382.08	455.04	600.96	892.80	1476.48	2643.84

Reference Table

*** For Ymux=1** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**32**	**32**	**32**	**32**	**32**	**32**
Timing (ns)						
t_{cyc}	4.94	4.99	5.10	6.24	7.57	9.18
t_{ckl}	1.03	1.05	1.07	1.09	1.10	1.12
t_{ckh}	1.10	1.10	1.10	1.10	1.10	1.10
t_{as}	0.35	0.35	0.35	0.35	0.35	0.35
t_{ah}	0.34	0.37	0.40	0.44	0.47	0.50
t_{cs}	1.03	1.05	1.07	1.09	1.10	1.12
t_{ch}	0.69	0.69	0.69	0.69	0.69	0.69
t_{ces}	0.55	0.57	0.59	0.61	0.62	0.64
t_{ceh}	0.69	0.69	0.69	0.69	0.69	0.69
t_{cms}	0.34	0.34	0.34	0.34	0.34	0.34
t_{cmh}	0.53	0.53	0.53	0.53	0.53	0.53
t_{ds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{dh}	0.57	0.57	0.57	0.57	0.57	0.57
t_{vds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{vdh}	0.57	0.57	0.57	0.57	0.57	0.57
t_{cds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{cdh}	0.53	0.53	0.53	0.53	0.53	0.53
t_{ws}	0.28	0.28	0.28	0.28	0.28	0.28
t_{wh}	0.34	0.37	0.40	0.44	0.47	0.50
t_{acc}	2.24	2.29	2.39	2.56	2.28	3.51
t_{da}	1.99	2.04	2.14	2.31	2.63	3.26
t_{dz}	0.62	0.62	0.62	0.62	0.62	0.62
t_{zd}	0.73	0.73	0.73	0.73	0.73	0.73
t_{od}	0.81	0.81	0.81	0.81	0.81	0.81
t_{vdacc}	2.24	2.29	2.39	2.56	2.88	3.51
t_{vdda}	1.99	2.04	2.14	2.31	2.63	3.26
t_{vddz}	0.62	0.62	0.62	0.62	0.62	0.62
t_{vdzd}	0.73	0.73	0.73	0.73	0.73	0.73
t_{vdod}	0.81	0.81	0.81	0.81	0.81	0.81
t_{caacc}	3.80	3.93	4.33	5.02	6.08	7.37
t_{cada}	2.65	2.73	2.87	3.42	4.13	5.05
t_{cadz}	0.43	0.45	0.48	0.55	0.68	0.96
t_{cazd}	0.60	0.62	0.65	0.71	0.83	1.09
t_{caod}	0.68	0.70	0.73	0.79	0.90	1.16
t_{htacc}	3.47	3.69	4.00	4.70	5.55	6.61
t_{htda}	2.65	2.73	2.87	3.42	4.13	5.05
t_{rn}	4.14	4.19	4.30	5.44	6.77	8.38
t_{rns}	1.03	1.05	1.07	1.09	1.10	1.12
t_{rnh}	4.14	4.19	4.30	5.44	6.77	8.38
Power (µW/MHz)						
Power_read	45.34	50.06	55.14	62.83	78.54	112.32
Power_write	40.34	46.85	59.49	84.80	138.41	236.40
Power_compare	176.44	196.41	231.07	299.13	427.57	663.65
Power_standby	0.82	0.90	0.96	1.15	1.51	2.18
Power_reset	1.26	2.05	3.54	6.90	14.97	36.87
Area (µm)						
Width	345.36	367.00	388.64	410.28	431.94	453.58
Height	382.08	455.04	600.96	892.80	1476.48	2643.84

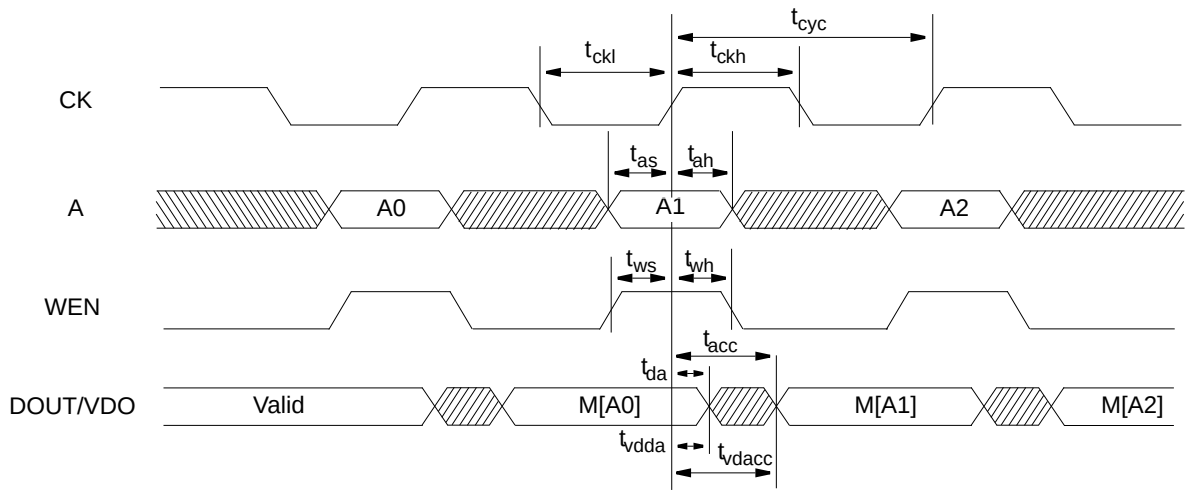
Reference Table

*** For Ymux=1** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA = 0.5)

Parameters						
words	**16**	**32**	**64**	**128**	**256**	**512**
bpw	**64**	**64**	**64**	**64**	**64**	**64**
Timing (ns)						
t_{cyc}	5.92	5.98	6.11	7.25	8.65	10.35
t_{ckl}	1.03	1.05	1.07	1.09	1.10	1.12
t_{ckh}	1.10	1.10	1.10	1.10	1.10	1.10
t_{as}	0.35	0.35	0.35	0.35	0.35	0.35
t_{ah}	0.34	0.37	0.40	0.44	0.47	0.50
t_{cs}	1.03	1.05	1.07	1.09	1.10	1.12
t_{ch}	0.69	0.69	0.69	0.69	0.69	0.69
t_{ces}	0.55	0.57	0.59	0.61	0.63	0.65
t_{ceh}	0.69	0.69	0.69	0.69	0.69	0.69
t_{cms}	0.34	0.34	0.34	0.34	0.34	0.34
t_{cmh}	0.68	0.68	0.68	0.68	0.68	0.68
t_{ds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{dh}	0.72	0.72	0.72	0.72	0.72	0.72
t_{vds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{vdh}	0.72	0.72	0.72	0.72	0.72	0.72
t_{cds}	0.34	0.34	0.34	0.34	0.34	0.34
t_{cdh}	0.68	0.68	0.68	0.68	0.68	0.68
t_{ws}	0.28	0.28	0.28	0.28	0.28	0.28
t_{wh}	0.34	0.37	0.40	0.44	0.47	0.50
t_{acc}	2.50	2.56	2.66	2.85	3.18	3.83
t_{da}	2.25	2.31	2.41	2.60	2.93	3.58
t_{dz}	0.80	0.80	0.80	0.80	0.80	0.80
t_{zd}	0.87	0.87	0.87	0.87	0.87	0.87
t_{od}	0.94	0.94	0.94	0.94	0.94	0.94
t_{vdacc}	2.50	2.56	2.66	2.85	3.18	3.83
t_{vdda}	2.25	2.31	2.41	2.60	2.93	3.58
t_{vddz}	0.80	0.80	0.80	0.80	0.80	0.80
t_{vdzd}	0.87	0.87	0.87	0.87	0.87	0.87
t_{vdod}	0.94	0.94	0.94	0.94	0.94	0.94
t_{caacc}	4.43	4.58	4.98	5.68	6.79	8.21
t_{cada}	3.28	3.36	3.53	4.09	4.84	5.89
t_{cadz}	0.43	0.45	0.48	0.55	0.68	0.96
t_{cazd}	0.60	0.62	0.65	0.71	0.83	1.09
t_{caod}	0.68	0.70	0.73	0.79	0.90	1.16
t_{htacc}	4.11	4.34	4.65	5.39	6.27	7.45
t_{htda}	3.28	3.36	3.53	4.09	4.84	5.89
t_{rn}	5.12	5.18	5.31	6.45	7.85	9.55
t_{rns}	1.03	1.05	1.07	1.09	1.10	1.12
t_{rnh}	5.12	5.18	5.31	6.45	7.85	9.55
Power (µW/MHz)						
Power_read	79.34	86.71	94.31	104.44	124.72	167.22
Power_write	89.60	80.93	102.71	146.63	239.39	408.82
Power_compare	326.04	356.24	414.41	531.58	757.32	1167.60
Power_standby	1.34	1.38	1.66	1.89	2.49	3.71
Power_reset	1.28	2.08	3.60	6.94	15.24	37.28
Area (µm)						
Width	525.20	546.84	568.48	590.12	611.78	633.42
Height	382.08	455.04	600.96	892.80	1476.48	2643.84

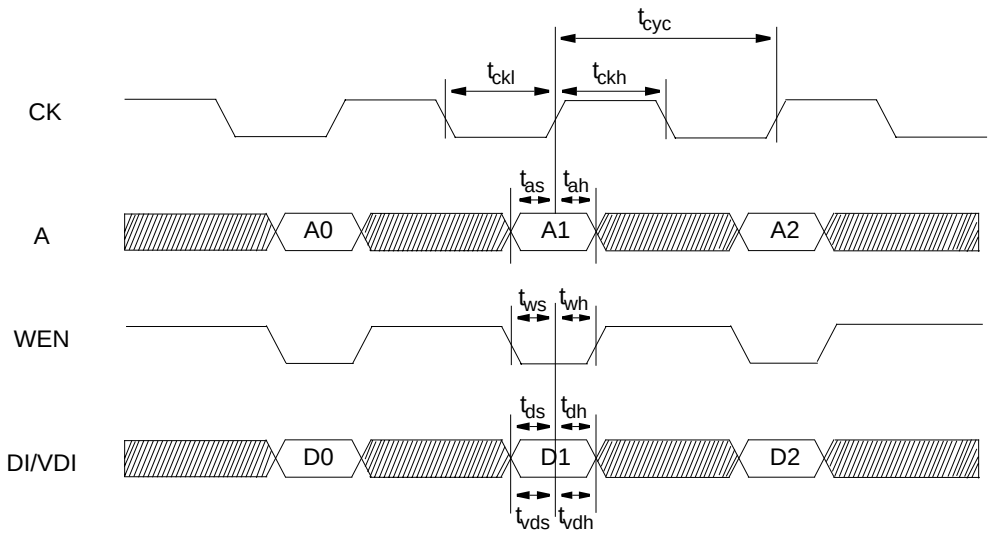
Timing Diagrams

Read Cycle



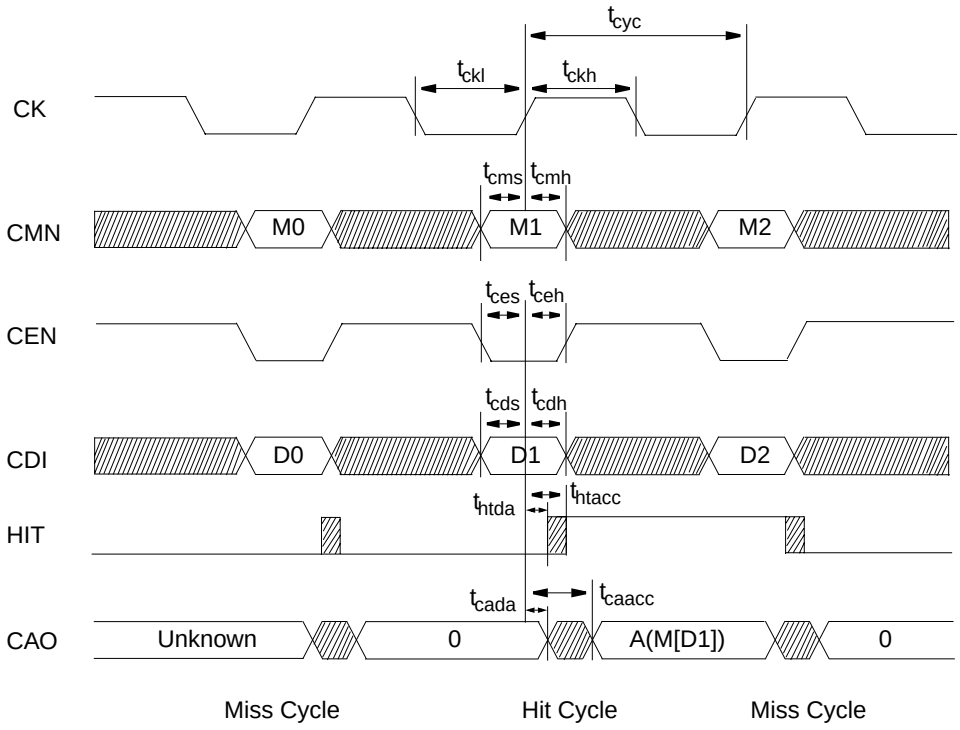
(RN=high, CSN=low, OEN=low, CEN=high, AEN, DI, VDI, CDI, CMN= don't care)

Write Cycle



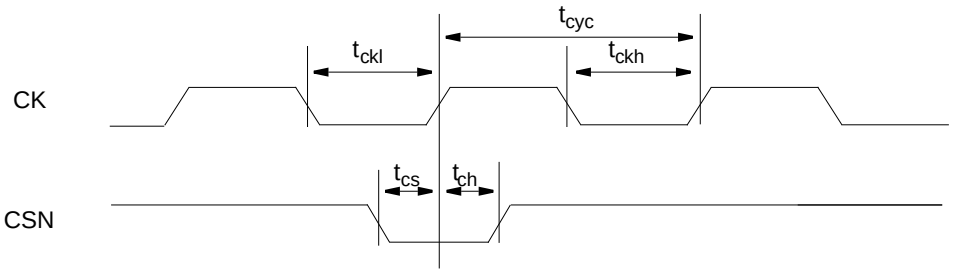
(RN = high, CSN = low, CEN = high, OEN, AEN, CDI, CMN = don't care)

Compare Cycle



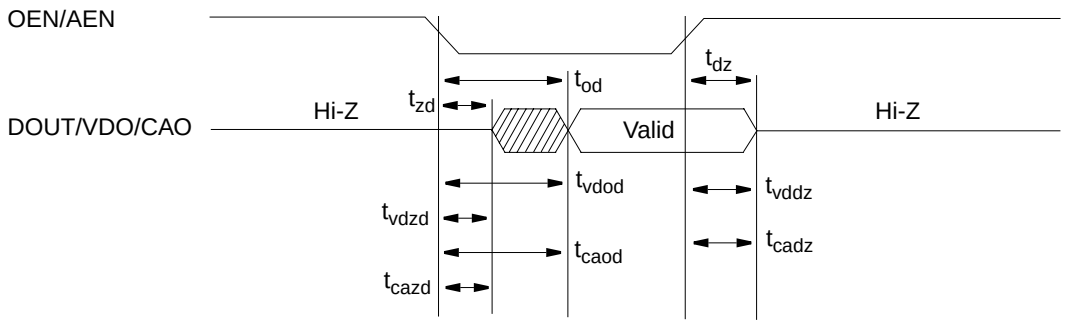
(RE = high, CSN = low, A, WEN, OEN, AEN = don't care)

CSN Controlled



(RN, WEN, OEN CEN, AEN, A, DI, VDI, CDI, CMN = valid)

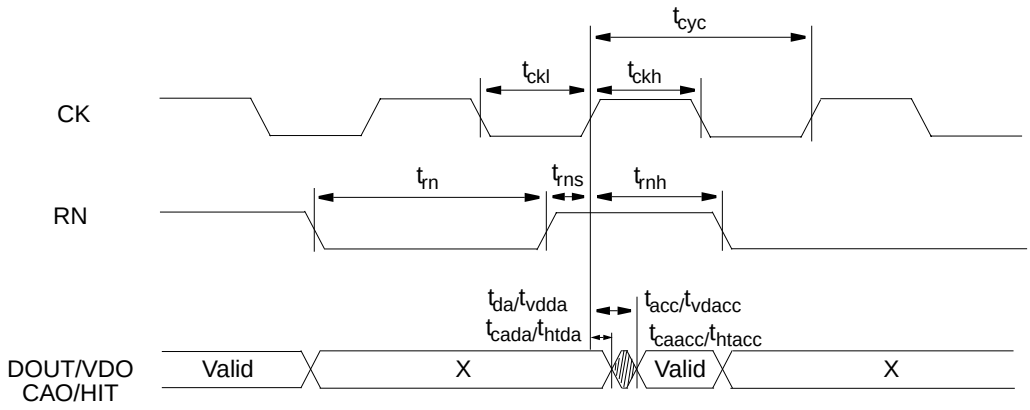
OEN/AEN Controlled Output Enable



(RN, CK, CSN, WEN, CEN, AEN, CMN, A, DI, VDI, CDI = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

RN Controlled Reset Mode

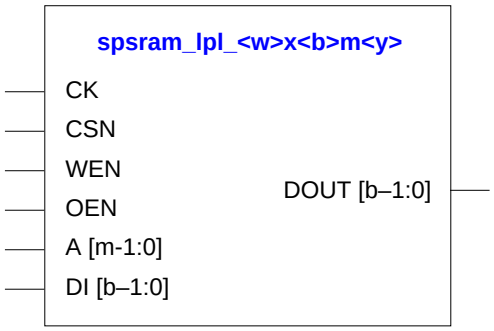


(OEN, CSN, WEN, CEN, AEN, CMN, A, DI, VDI, CDI = valid)

SPSRAM_LPL

Low-Power Single-Port Synchronous Static RAM

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for Low-Power application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 256 number of bits per word

Function Description

SPSRAM_LPL is a single-port synchronous static RAM which is provided as a compiler. SPSRAM_LPL is intended for use in Low-Power applications. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data on DI[] is written into the memory location specified on A[]. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAM_LPL Function Table

CK	CSN	WEN	OEN	A	DI	DOUT	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

Parameter Description

SPSRAM_LPL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b), Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	64	128	256	512
	Max	4096	8192	16384	32768
	Step	32	64	128	256
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

Unit: [SL]

CK	CSN	WEN	OEN	A	DI	DOUT
7.56	2.18	2.70	3.73	2.70	2.95	6.59

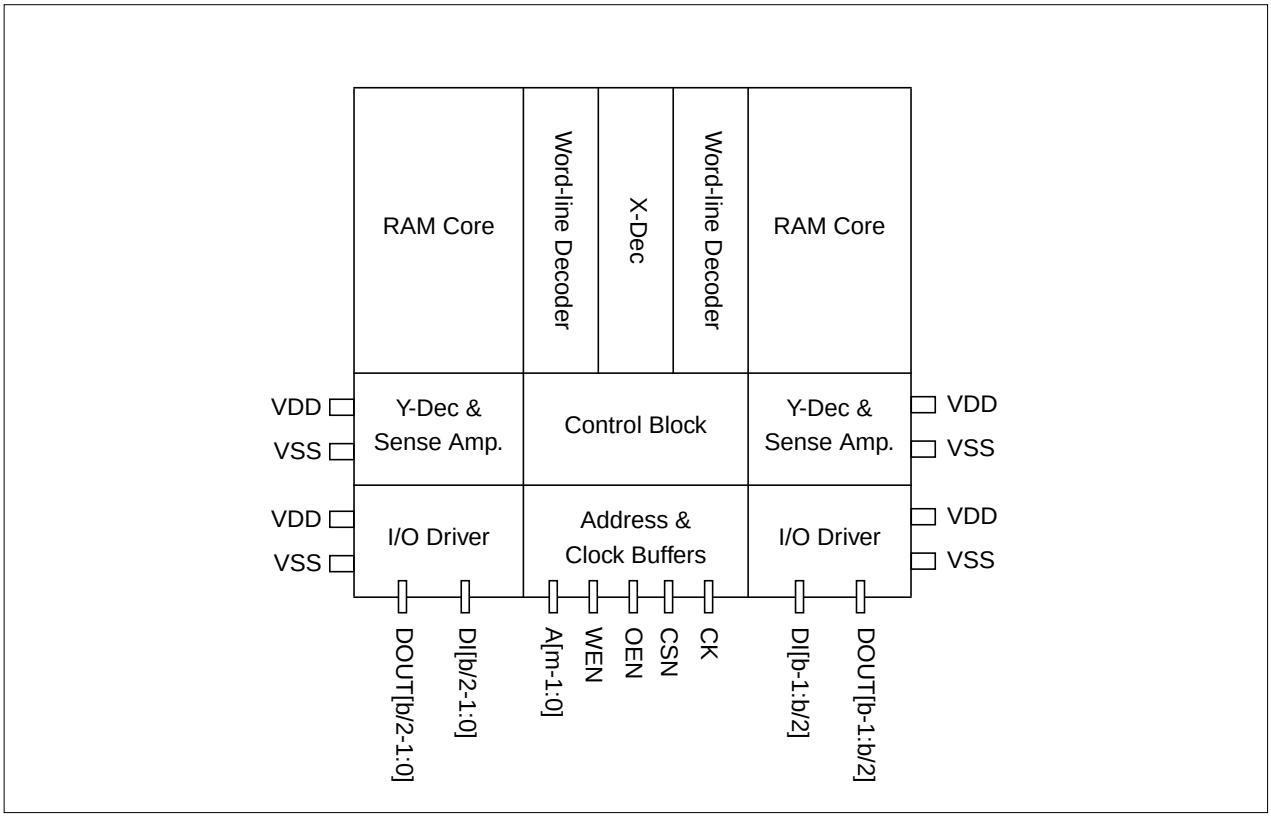
NOTE: Each pin's capacitance is exactly same regardless of available mux types.

SPSRAM_LPL

Low-Power Single-Port Synchronous Static RAM

Block Diagrams

SPSRAM_LPL supports only 1-bank architecture. The power ports are located on the middle-edge and the bottom edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



Application Notes

1. Permitting Over-the-cell routing.
In chip-level layout, over-the-cell routing in SPSRAM_LPL is permitted only for Metal-5 and Metal-6 layers. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAM_LPL.

4. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{acc}	Data access time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operation		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

SPSRAM_LPL

Low-Power Single-Port Synchronous Static RAM

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**128**	**256**	**512**	**1024**	**2048**	**3072**	**4096**
bpw	**16**	**32**	**48**	**64**	**80**	**96**	**112**	**128**
Timing (ns)								
t_{cyc}	3.56	3.58	3.60	3.64	3.68	4.16	4.66	5.34
t_{ckl}	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
t_{ckh}	1.15	1.15	1.15	1.15	1.15	1.15	1.15	1.15
t_{as}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.53	0.51	0.50	0.48	0.46	0.45	0.43	0.41
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.46	3.48	3.50	3.54	3.58	4.06	4.56	5.26
t_{da}	3.10	3.12	3.14	3.16	3.19	3.67	4.17	4.87
t_{dz}	0.65	0.67	0.70	0.72	0.75	0.77	0.79	0.82
t_{zd}	0.75	0.77	0.80	0.82	0.85	0.87	0.89	0.92
t_{od}	0.85	0.87	0.90	0.92	0.95	0.97	0.99	1.02
Power (µW/MHz)								
Power_read	41.81	56.69	73.96	96.82	132.41	168.35	201.82	233.59
Power_write	51.75	73.42	97.06	125.30	163.97	205.76	244.72	289.53
Power_standby	2.70	4.66	6.64	8.66	10.76	12.92	15.71	22.23
Area (µm)								
Width	219.89	338.46	457.02	575.58	694.15	812.71	931.28	1049.84
Height	207.04	248.51	331.44	497.32	829.06	1504.82	2180.58	2856.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**256**	**512**	**1024**	**2048**	**4096**	**6144**	**8192**
bpw	**8**	**16**	**24**	**32**	**40**	**48**	**56**	**64**
Timing (ns)								
t_{cyc}	3.61	3.62	3.64	3.66	3.69	4.17	4.68	5.36
t_{ckl}	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
t_{ckh}	1.15	1.15	1.15	1.15	1.15	1.15	1.15	1.15
t_{as}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.53	0.52	0.51	0.50	0.48	0.47	0.46	0.44
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.51	3.52	3.54	3.56	3.59	4.07	4.58	5.26
t_{da}	3.11	3.13	3.14	3.16	3.19	3.68	4.18	4.87
t_{dz}	0.64	0.66	0.68	0.69	0.71	0.73	0.74	0.76
t_{zd}	0.74	0.76	0.78	0.79	0.81	0.83	0.84	0.86
t_{od}	0.84	0.86	0.88	0.89	0.91	0.93	0.94	0.96
Power (µW/MHz)								
Power_read	41.21	55.53	72.27	94.66	129.92	164.69	195.65	225.76
Power_write	50.03	67.86	87.75	112.44	148.11	185.25	219.89	265.01
Power_standby	1.77	2.76	3.77	4.84	6.02	6.99	8.33	13.37
Area (µm)								
Width	219.71	338.30	456.89	575.48	694.07	812.66	931.25	1049.84
Height	207.04	248.51	331.44	497.32	829.06	1504.82	2180.58	2856.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

SPSRAM_LPL

Low-Power Single-Port Synchronous Static RAM

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**12288**	**16384**
bpw	**4**	**8**	**12**	**16**	**20**	**24**	**28**	**32**
Timing (ns)								
t_{cyc}	3.64	3.66	3.68	3.70	3.73	4.20	4.71	5.39
t_{ckl}	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
t_{ckh}	1.15	1.15	1.15	1.15	1.15	1.15	1.15	1.15
t_{as}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.53	0.52	0.51	0.50	0.49	0.48	0.48	0.46
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.54	3.56	3.57	3.60	3.62	4.11	4.61	5.30
t_{da}	3.14	3.16	3.18	3.21	3.24	3.71	4.22	4.91
t_{dz}	0.64	0.65	0.67	0.68	0.69	0.70	0.72	0.73
t_{zd}	0.74	0.75	0.77	0.78	0.79	0.80	0.82	0.83
t_{od}	0.84	0.85	0.87	0.88	0.89	0.90	0.92	0.93
Power (µW/MHz)								
Power_read	41.05	55.03	71.47	93.64	128.85	162.32	193.02	222.07
Power_write	48.51	64.49	82.51	105.29	138.92	174.79	205.90	251.95
Power_standby	1.24	1.76	2.28	2.82	3.41	4.27	5.22	8.83
Area (µm)								
Width	219.32	337.97	456.61	575.26	693.90	812.55	931.19	1049.84
Height	207.04	248.51	331.44	497.32	829.06	1504.82	2180.58	2856.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

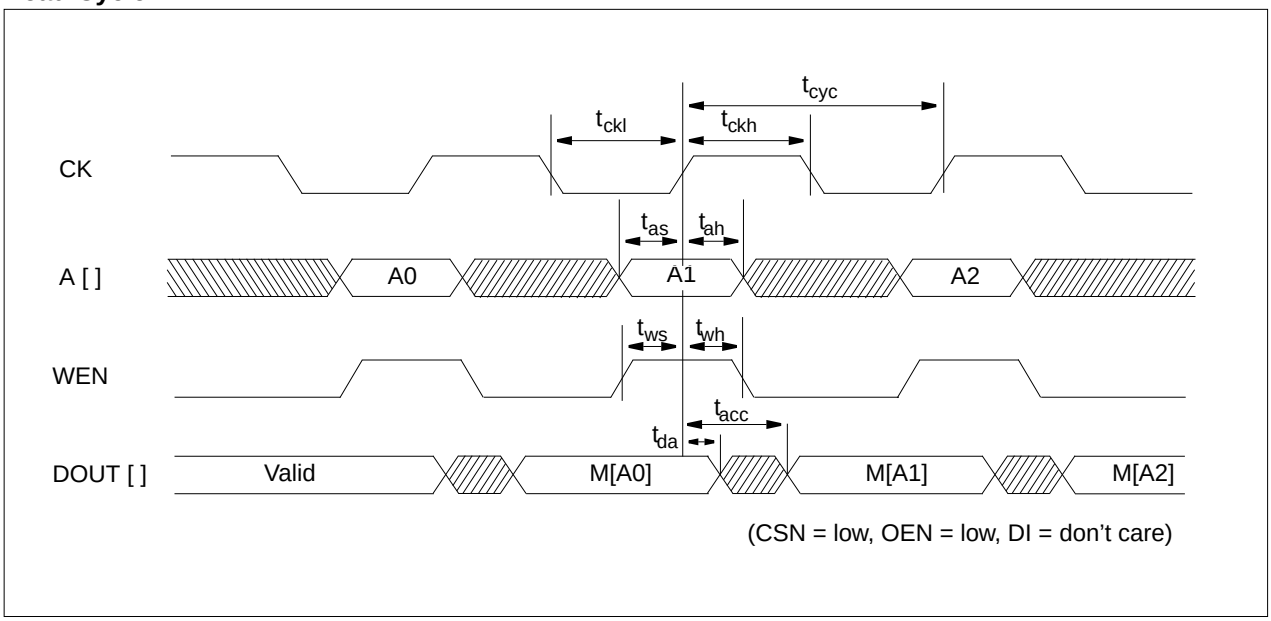
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**24576**	**32768**
bpw	**2**	**4**	**6**	**8**	**10**	**12**	**14**	**16**
Timing (ns)								
t_{cyc}	3.69	3.71	3.73	3.76	3.79	4.26	4.77	5.45
t_{ckl}	1.10	1.09	1.09	1.09	1.09	1.09	1.09	1.09
t_{ckh}	1.15	1.15	1.15	1.15	1.15	1.15	1.15	1.15
t_{as}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.51	0.50	0.48	0.47	0.45	0.44	0.42	0.41
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.59	3.61	3.63	3.66	3.69	4.16	4.67	5.35
t_{da}	3.19	3.21	3.23	3.25	3.29	3.77	4.28	4.98
t_{dz}	0.66	0.68	0.71	0.73	0.75	0.77	0.80	0.82
t_{zd}	0.76	0.78	0.81	0.83	0.85	0.87	0.90	0.92
t_{od}	0.86	0.88	0.91	0.93	0.95	0.97	1.00	1.02
Power (µW/MHz)								
Power_read	41.19	54.99	71.27	93.28	128.38	161.44	191.46	220.11
Power_write	48.41	63.64	80.90	102.90	135.73	169.20	201.68	246.47
Power_standby	0.99	1.28	1.58	1.91	2.29	2.68	3.21	7.04
Area (µm)								
Width	218.52	337.28	456.04	574.80	693.56	812.32	931.08	1049.84
Height	207.04	248.51	331.44	497.32	829.06	1504.82	2180.58	2856.34

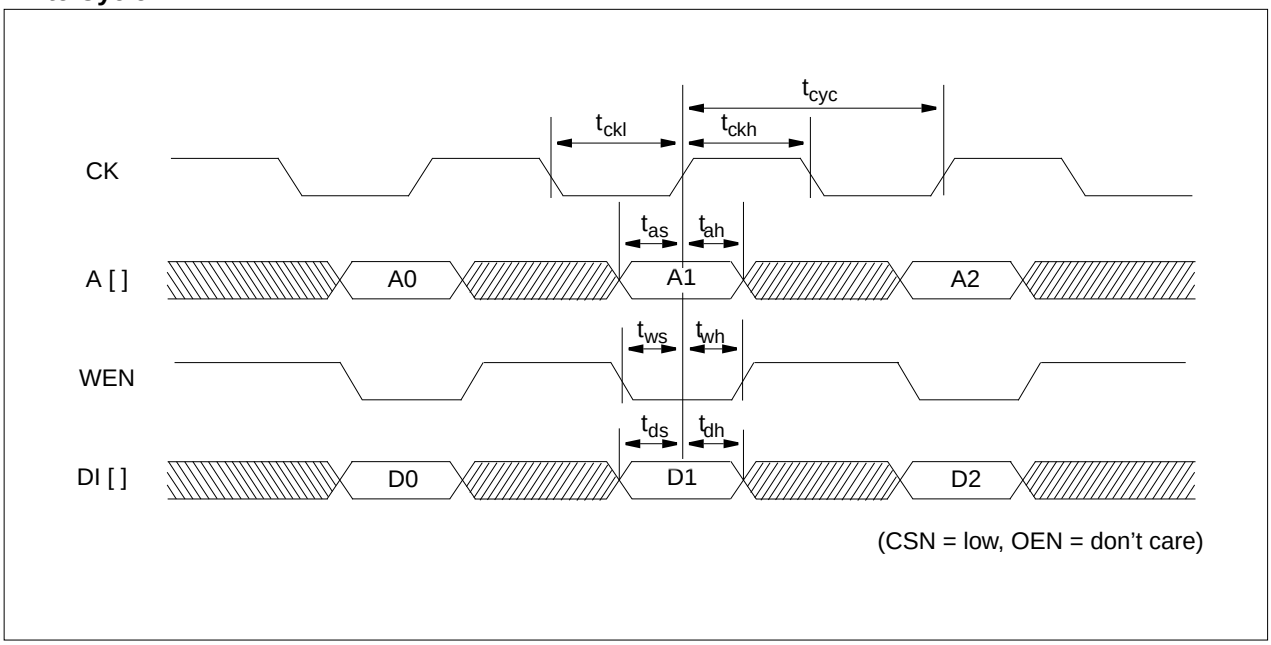
NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Timing Diagrams

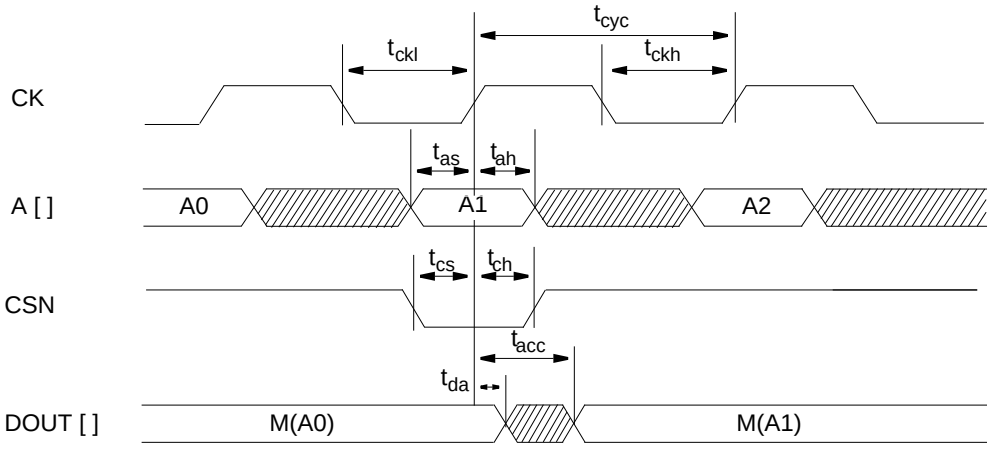
Read Cycle



Write Cycle

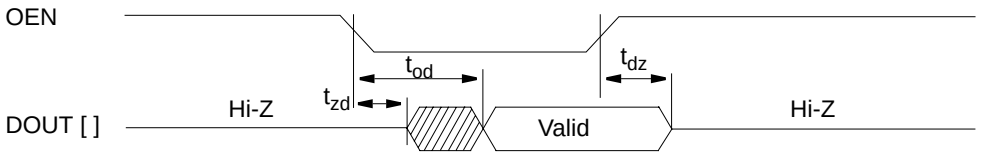


Read Cycle with CSN Controlled



(OEN = low, WEN = high, DI = don't care)

OEN Controlled Output Enable



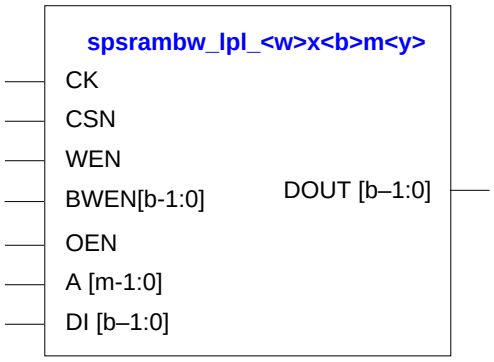
(CK, A, WEN, DI, CSN = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

SPSRAMBW_LPL

Low-Power Single-Port Synchronous Static RAM with Bit-Write

Logic Symbol



NOTES:

1. Words(w) is the number of words.
2. Bpw(b) is the number of bits per word.
3. Ymux(y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for Low-Power application
- Bit-write capability
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state output control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimization
- Flexible aspect ratio
- Up to 512Kbits capacity
- Up to 16K number of words
- Up to 256 number of bits per word

Function Description

SPSRAMBW_LPL is a single-port synchronous static RAM with bit-write capability which is provided as a compiler. SPSRAMBW_LPL is intended for use in Low-Power applications. Basically, its functionality is exactly same as SPSRAM_LPL except a bit-write operation which is controlled by BWEN[], named bit-write enable signal bus. Each bit of BWEN[] enables or disable the write operation of its corresponding bit in DI[]. On the rising edge of CK, the write cycle is initiated when WEN is low and CSN is low. The data bytes or bits in DI[], which their corresponding bit(s) in BWEN[] are low, are written into the memory location specified on A[]. When all bits of BWEN[] are high, any data in DI[] are not written into the memory location specified on A[]. When all bits of BWEN[] are low, the data in DI[] are written into the memory location specified on A[], which is exactly same as the write operation in SPSRAM_LPL. During the write cycle, DOUT[] remains stable. On the rising edge of CK, the read cycle is initiated when WEN is high and CSN is low. The data at DOUT[] become valid after a delay. While in standby mode that CSN is high, A[] and DI[] are disabled, data stored in the memory is retained and DOUT[] remains stable. When OEN is high, DOUT[] is placed in a high-impedance state.

SPSRAMBW_LPL Function Table

CK	CSN	WEN	OEN	A	BWEN	DI	DOUT	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

Parameter Description

SPSRAMBW_LPL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16	Ymux(y) = 32
Words (w)	Min	64	128	256	512
	Max	4096	8192	16384	32768
	Step	32	64	128	256
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN [ ]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other input. When OEN is high, DOUT is disabled and goes to high-impedance state.
A [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

SPSRAMBW_LPL

Low-Power Single-Port Synchronous Static RAM with Bit-Write

Pin Capacitance

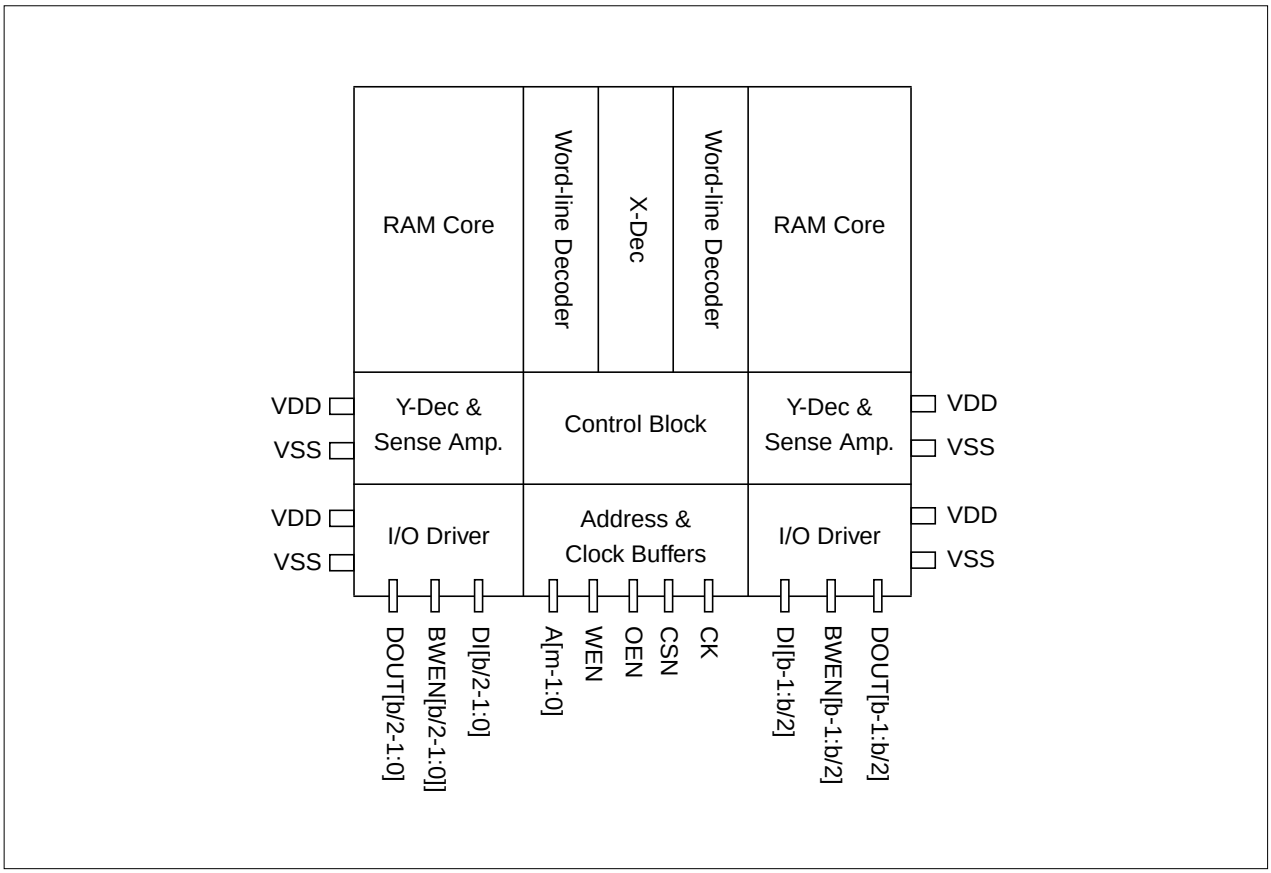
Unit: [SL]

CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
7.56	2.18	2.70	2.95	3.73	2.70	2.95	6.59

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagrams

SPSRAMBW_LPL supports only 1-bank architecture. The power ports are located on the middle-edge and the bottom edge of both right- and left-sides of the memory. All signal ports are only located on the bottom sides of the memory.



Application Notes

1. Permitting Over-the-cell routing.
In chip-level layout, over-the-cell routing in SPSRAMBW_LPL is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of SPSRAMBW_LPL.

4. A byte-write or word-write operation with SPSRAMBW_LPL.
Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as SPSRAM_LPL. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

5. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckh}	Clock pulse width high
t_{ckl}	Clock pulse width low	t_{as}	Address setup time
t_{ah}	Address hold time	t_{cs}	CSN setup time
t_{ch}	CSN hold time	t_{ds}	Data-In setup time
t_{dh}	Data-In hold time	t_{ws}	WEN setup time
t_{wh}	WEN hold time	t_{acc}	Data access time
t_{bwh}	BWEN hold time	t_{bws}	BWEN setup time
t_{da}	De-access time	t_{dz}	DOUT drive to high-Z time
t_{zd}	DOUT high-Z to drive time	t_{od}	OEN to valid output time
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operation		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**128**	**256**	**512**	**1024**	**2048**	**3072**	**4096**
bpw	**16**	**32**	**48**	**64**	**80**	**96**	**112**	**128**
Timing (ns)								
t_{cyc}	3.56	3.58	3.60	3.64	3.68	4.16	4.66	5.34
t_{ckl}	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
t_{ckh}	1.15	1.15	1.15	1.15	1.15	1.15	1.15	1.15
t_{as}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.53	0.51	0.50	0.48	0.46	0.45	0.43	0.41
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.48	0.46	0.45	0.43	0.41	0.40	0.38	0.36
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.46	3.48	3.50	3.54	3.58	4.06	4.56	5.26
t_{da}	3.10	3.12	3.14	3.16	3.19	3.67	4.17	4.87
t_{dz}	0.65	0.67	0.70	0.72	0.75	0.77	0.79	0.82
t_{zd}	0.75	0.77	0.80	0.82	0.85	0.87	0.89	0.92
t_{od}	0.85	0.87	0.90	0.92	0.95	0.97	0.99	1.02
Power (µW/MHz)								
Power_read	41.81	56.69	73.96	96.82	132.41	168.35	201.82	233.59
Power_write	53.48	76.69	102.41	132.44	172.92	216.54	257.26	303.94
Power_standby	4.40	8.20	11.98	15.80	19.70	23.70	28.25	36.64
Area (µm)								
Width	219.89	338.46	457.02	575.58	694.15	812.71	931.28	1049.84
Height	207.04	248.51	331.44	497.32	829.06	1504.82	2180.58	2856.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

SPSRAMBW_LPL

Low-Power Single-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**256**	**512**	**1024**	**2048**	**4096**	**6144**	**8192**
bpw	**8**	**16**	**24**	**32**	**40**	**48**	**56**	**64**
Timing (ns)								
t_{cyc}	3.61	3.62	3.64	3.66	3.69	4.17	4.68	5.36
t_{ckl}	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
t_{ckh}	1.15	1.15	1.15	1.15	1.15	1.15	1.15	1.15
t_{as}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.53	0.52	0.51	0.50	0.48	0.47	0.46	0.44
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.48	0.47	0.46	0.45	0.43	0.42	0.41	0.39
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.51	3.52	3.54	3.56	3.59	4.07	4.58	5.26
t_{da}	3.11	3.13	3.14	3.16	3.19	3.68	4.18	4.87
t_{dz}	0.64	0.66	0.68	0.69	0.71	0.73	0.74	0.76
t_{zd}	0.74	0.76	0.78	0.79	0.81	0.83	0.84	0.86
t_{od}	0.84	0.86	0.88	0.89	0.91	0.93	0.94	0.96
Power (µW/MHz)								
Power_read	41.21	55.53	72.27	94.66	129.92	164.69	195.65	225.76
Power_write	50.87	69.61	90.42	116.02	152.59	190.62	226.15	272.27
Power_standby	2.61	4.51	6.44	8.41	10.50	12.36	14.59	20.63
Area (µm)								
Width	219.71	338.30	456.89	575.48	694.07	812.66	931.25	1049.84
Height	207.04	248.51	331.44	497.32	829.06	1504.82	2180.58	2856.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**12288**	**16384**
bpw	**4**	**8**	**12**	**16**	**20**	**24**	**28**	**32**
Timing (ns)								
t_{cyc}	3.64	3.66	3.68	3.70	3.73	4.20	4.71	5.39
t_{ckl}	1.09	1.09	1.09	1.09	1.09	1.09	1.09	1.09
t_{ckh}	1.15	1.15	1.15	1.15	1.15	1.15	1.15	1.15
t_{as}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.53	0.52	0.51	0.50	0.49	0.48	0.48	0.46
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.48	0.47	0.46	0.45	0.44	0.43	0.43	0.41
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.54	3.56	3.57	3.60	3.62	4.11	4.61	5.30
t_{da}	3.14	3.16	3.18	3.21	3.24	3.71	4.22	4.91
t_{dz}	0.64	0.65	0.67	0.68	0.69	0.70	0.72	0.73
t_{zd}	0.74	0.75	0.77	0.78	0.79	0.80	0.82	0.83
t_{od}	0.84	0.85	0.87	0.88	0.89	0.90	0.92	0.93
Power (µW/MHz)								
Power_read	41.05	55.03	71.47	93.64	128.85	162.32	193.02	222.07
Power_write	48.90	65.34	83.82	107.06	141.15	177.49	209.06	255.59
Power_standby	1.63	2.61	3.59	4.60	5.64	6.97	8.38	12.46
Area (µm)								
Width	219.32	337.97	456.61	575.26	693.90	812.55	931.19	1049.84
Height	207.04	248.51	331.44	497.32	829.06	1504.82	2180.58	2856.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

SPSRAMBW_LPL

Low-Power Single-Port Synchronous Static RAM with Bit-Write

Reference Table

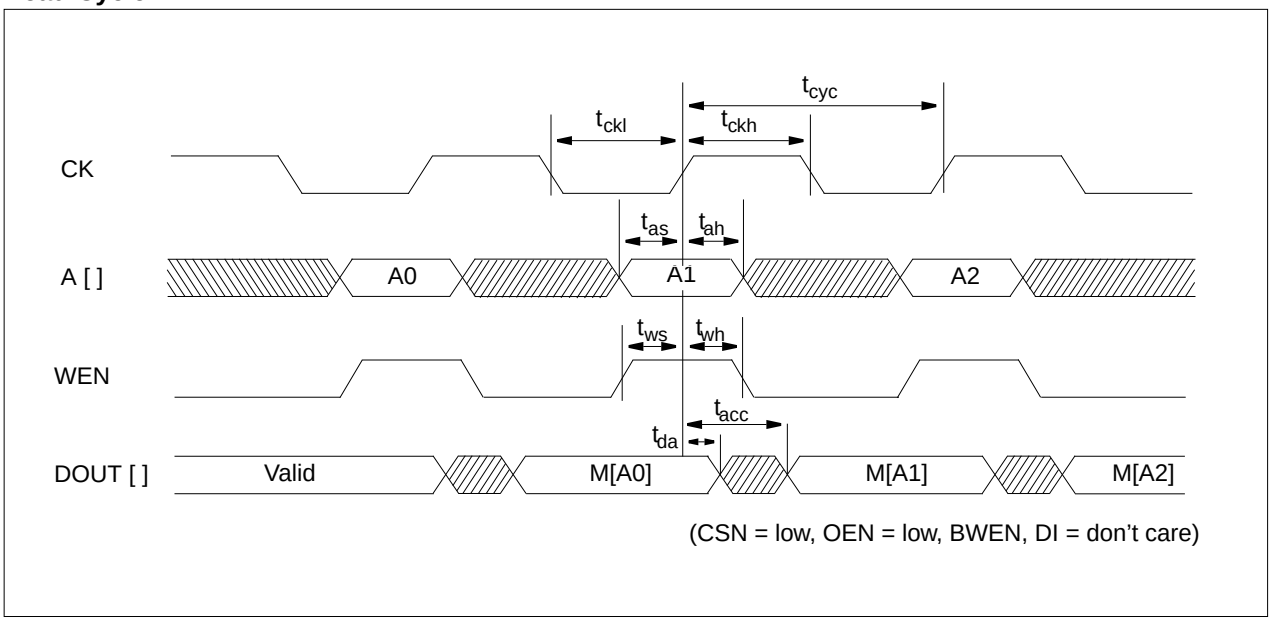
*** For Ymux=32** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**24576**	**32768**
bpw	**2**	**4**	**6**	**8**	**10**	**12**	**14**	**16**
Timing (ns)								
t_{cyc}	3.69	3.71	3.73	3.76	3.79	4.26	4.77	5.45
t_{ckl}	1.10	1.09	1.09	1.09	1.09	1.09	1.09	1.09
t_{ckh}	1.15	1.15	1.15	1.15	1.15	1.15	1.15	1.15
t_{as}	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.51	0.50	0.48	0.47	0.45	0.44	0.42	0.41
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.57	0.57	0.57	0.57	0.57	0.57	0.57	0.57
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.46	0.45	0.43	0.42	0.40	0.39	0.37	0.36
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.59	3.61	3.63	3.66	3.69	4.16	4.67	5.35
t_{da}	3.19	3.21	3.23	3.25	3.29	3.77	4.28	4.98
t_{dz}	0.66	0.68	0.71	0.73	0.75	0.77	0.80	0.82
t_{zd}	0.76	0.78	0.81	0.83	0.85	0.87	0.90	0.92
t_{od}	0.86	0.88	0.91	0.93	0.95	0.97	1.00	1.02
Power (µW/MHz)								
Power_read	41.19	54.99	71.27	93.28	128.38	161.44	191.46	220.11
Power_write	48.58	64.04	81.54	103.78	136.84	170.55	203.28	248.30
Power_standby	1.15	1.68	2.22	2.78	3.40	4.03	4.80	8.87
Area (µm)								
Width	218.52	337.28	456.04	574.80	693.56	812.32	931.08	1049.84
Height	207.04	248.51	331.44	497.32	829.06	1504.82	2180.58	2856.34

NOTE: Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is low.

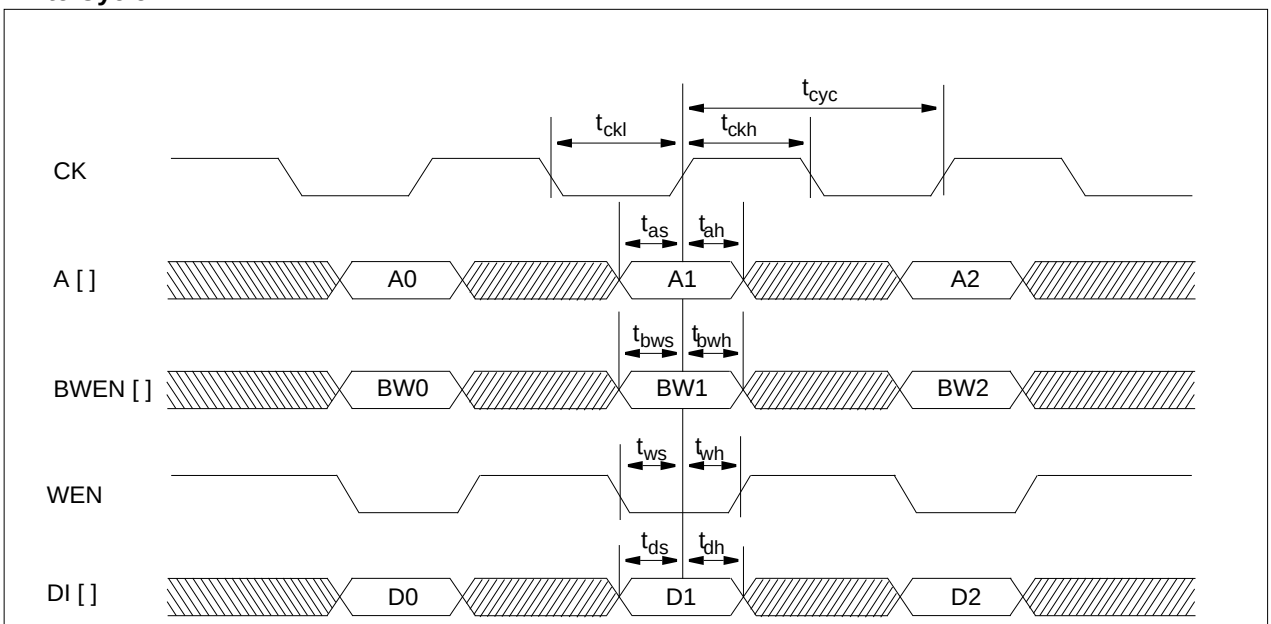
Timing Diagram

Read Cycle



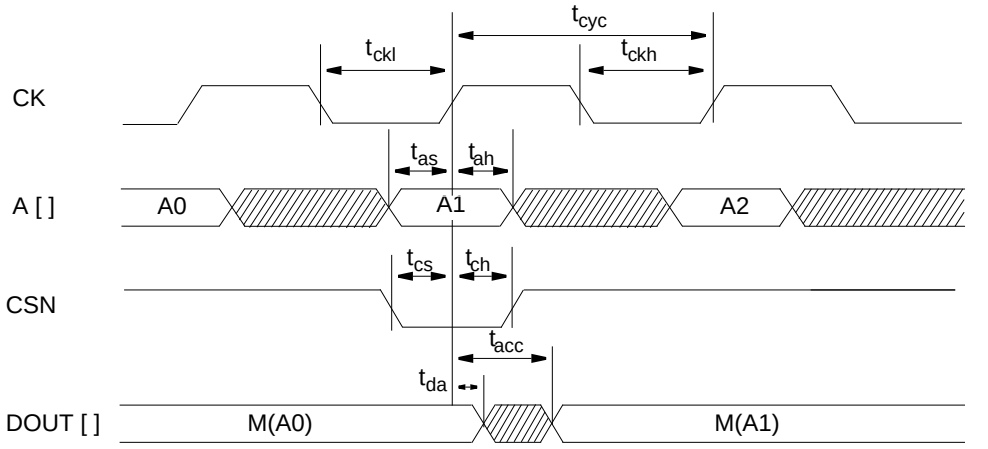
(CSN = low, OEN = low, BWEN, DI = don't care)

Write Cycle



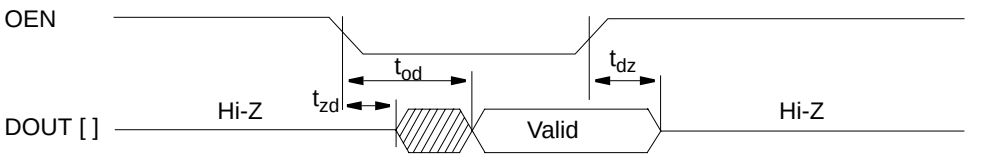
(CSN = low, OEN = don't care)

Read Cycle with CSN Controlled



(OEN = low, WEN = high, BWEN, DI = don't care)

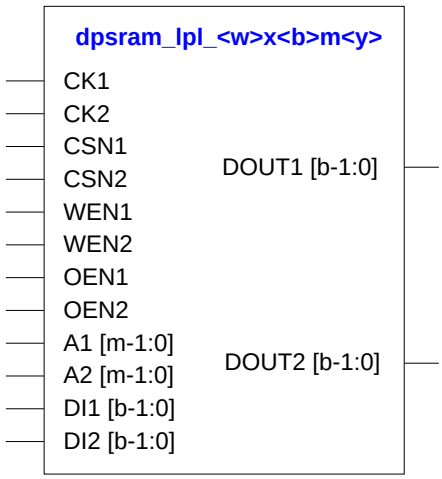
OEN Controlled Output Enable



(CK, A, WEN, BWEN, DI, CSN = don't care)

NOTE: "don't care" means the condition that these pins are in normal operation mode.

Logic Symbol



NOTES:

1. Words (w) is the number of words..
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for low-power application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state ouput control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimizatioin
- Flexible aspect ratio
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bit per word

Function Description

DPSRAM_LPL is a dual-port synchronous static RAM which is provided as a compiler. DPSRAM_LPL is intended for use in low-power applications. Each port is fully independent. On the rising edge of CK1 (CK2), the write cycle is initiated when WEN1 (WEN2) is low and CSN1 (CSN2) is low. The data on DI1[] (DI2[]) is written into the memory location specified on A1[](A2[]). During the write cycle, DOUT1[] (DOUT2[]) remains stable. On the rising edge of CK1 (CK2), the read cycle is initiated when WEN1 (WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[] (DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[] (A2[]) and DI1[] (DI2[]) are disabled, data stored in the memory is retained and DOUT1[] (DOUT2[]) remains stable. When OEN1 (OEN2) is high, DOUT1[] (DOUT2[]) is placed in a high-impedance state.

DPSRAM_LPL Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	Valid	DOUT(t-1)	Write cycle
↑	L	H	L	Valid	X	MEM(A)	Read cycle

DPSRAM_LPL

Low-Power Dual-Port Synchronous Static RAM

Parameter Description

DPSRAM_LPL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 2	Ymux(y) = 4	Ymux(Y) = 8	Ymux(y) = 16
Words (w)	Min	32	64	128	256
	Max	2048	4096	8192	16384
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [ ] A2 [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [ ] DI2 [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [ ] DOUT2 [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

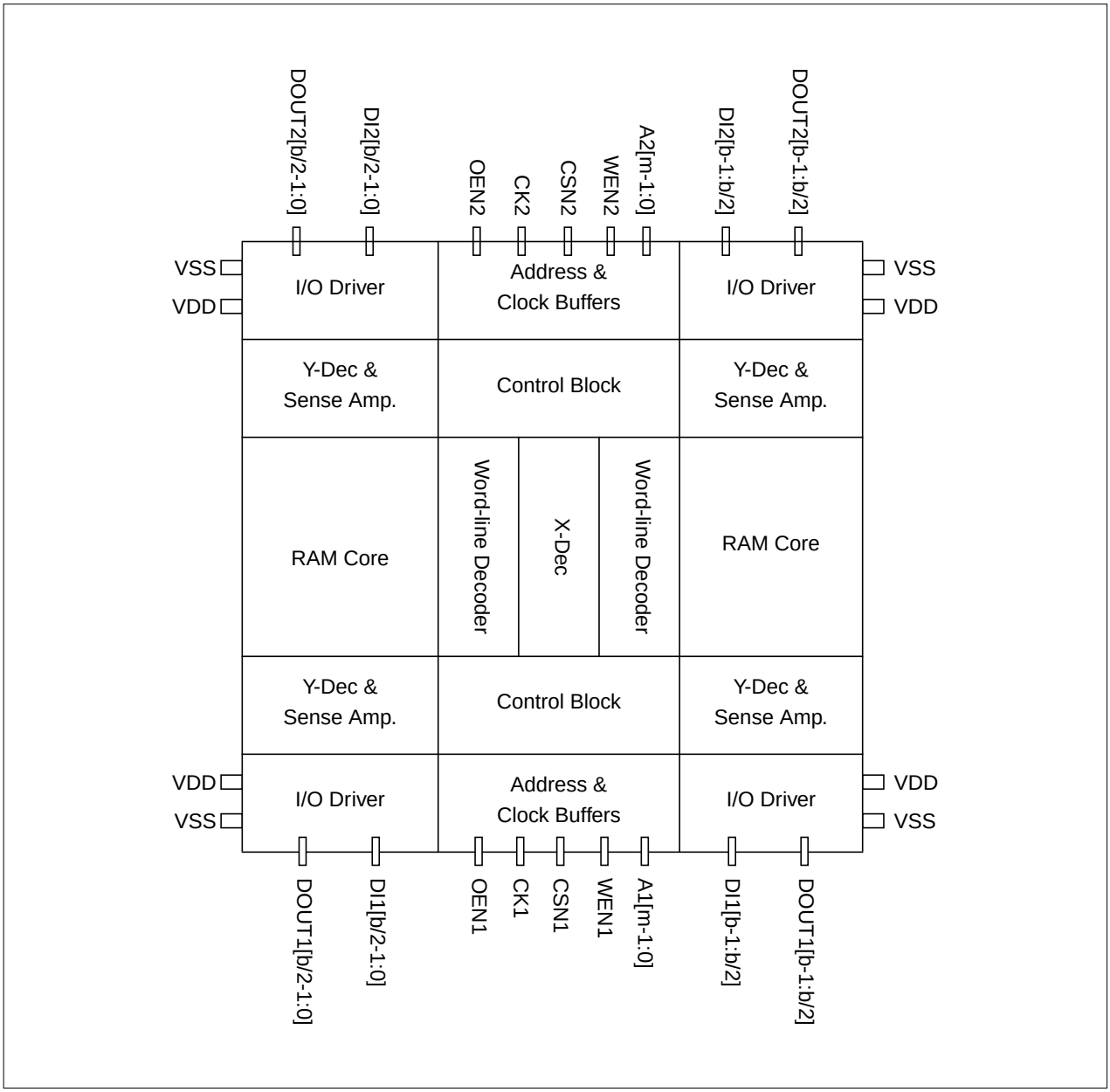
(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT
9.24	2.38	2.34	3.18	2.34	2.34	3.91

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagram

DPSRAM_LPL supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAM_LPL has two symmetrical ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



DPSRAM_LPL

Low-Power Dual-Port Synchronous Static RAM

Application Notes

1. Permitting Over-the-cell routing. In chip-level layout, over-the-cell routing in DPSRAM_LPL is permitted for only Metal-5 and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAM_LPL.

4. Contention mode in same address access.
In DPSRAM_LPL, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAM_LPL has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

5. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock to Clock Setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (μW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operation		
Definition for Area (μm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

DPSRAM_LPL

Low-Power Dual-Port Synchronous Static RAM

Reference Table

*** For Ymux=2** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**32**	**64**	**128**	**256**	**512**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**	**80**	**96**	**112**	**128**
Timing (ns)								
t_{cyc}	4.12	4.15	4.18	4.21	4.24	4.65	5.06	5.46
t_{ckl}	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36
t_{ckh}	1.31	1.31	1.31	1.31	1.31	1.31	1.31	1.31
t_{cc}	2.32	2.34	2.36	2.38	2.40	2.81	3.24	3.68
t_{as}	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.36	0.35	0.36	0.33	0.32	0.30	0.29	0.28
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.63	0.63	0.63	0.63	0.63	0.63	0.63	0.63
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.70	3.73	3.76	3.79	3.82	4.22	4.63	5.04
t_{da}	3.58	3.60	3.62	3.64	3.67	4.07	4.47	4.86
t_{dz}	0.49	0.52	0.55	0.57	0.60	0.62	0.65	0.68
t_{zd}	0.56	0.59	0.61	0.64	0.66	0.68	0.71	0.73
t_{od}	0.65	0.67	0.70	0.72	0.74	0.77	0.79	0.81
Power (µW/MHz)								
Power_read	52.43	79.57	108.20	140.28	180.16	224.46	266.46	310.13
Power_write	51.51	77.56	106.89	144.01	199.11	275.18	362.62	459.49
Power_standby	3.06	5.11	7.17	9.26	11.39	13.72	15.89	18.24
Area (µm)								
Width	377.24	550.04	722.84	895.64	1068.44	1241.24	1414.04	1586.84
Height	221.56	252.01	312.90	434.70	678.28	1174.60	1670.92	2167.24

NOTES:

1. In power consumption of DPSRAM_LPL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is tied to low.

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**128**	**256**	**512**	**1024**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**	**40**	**48**	**56**	**64**
Timing (ns)								
t_{cyc}	4.11	4.13	4.15	4.17	4.19	4.59	4.98	5.38
t_{ckl}	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36
t_{ckh}	1.31	1.31	1.31	1.31	1.31	1.31	1.31	1.31
t_{cc}	2.32	2.34	2.36	2.38	2.40	2.81	3.24	3.68
t_{as}	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.37	0.36	0.35	0.34	0.33	0.32	0.31	0.30
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.63	0.63	0.63	0.63	0.63	0.63	0.63	0.63
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.68	3.70	3.72	3.74	3.76	4.16	4.56	4.95
t_{da}	3.57	3.58	3.60	3.61	3.63	4.02	4.42	4.81
t_{dz}	0.49	0.50	0.52	0.54	0.56	0.58	0.60	0.62
t_{zd}	0.56	0.58	0.59	0.61	0.63	0.65	0.67	0.68
t_{od}	0.64	0.66	0.68	0.70	0.71	0.73	0.75	0.77
Power (µW/MHz)								
Power_read	41.76	58.30	76.58	98.92	130.48	161.97	190.09	218.81
Power_write	41.50	57.17	75.37	99.53	137.46	186.21	243.22	304.83
Power_standby	2.03	3.06	4.10	5.17	6.29	7.56	8.53	9.69
Area (µm)								
Width	377.24	550.04	722.84	895.64	1068.44	1241.24	1414.04	1586.84
Height	221.56	252.01	312.90	434.70	678.28	1174.60	1670.92	2167.24

NOTES:

1. In power consumption of DPSRAM_LPL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is tied to low.

DPSRAM_LPL

Low-Power Dual-Port Synchronous Static RAM

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**256**	**512**	**1024**	**2048**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**	**20**	**24**	**28**	**32**
Timing (ns)								
t_{cyc}	4.13	4.15	4.17	4.19	4.21	4.60	5.00	5.39
t_{ckl}	1.36	1.36	1.36	1.36	1.35	1.36	1.36	1.36
t_{ckh}	1.31	1.31	1.31	1.31	1.31	1.31	1.31	1.31
t_{cc}	2.32	2.34	2.36	2.38	2.40	2.81	3.24	3.68
t_{as}	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.37	0.37	0.37
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.36	0.35	0.34	0.33	0.32	0.31	0.30	0.29
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.63	0.63	0.63	0.63	0.63	0.63	0.63	0.63
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.71	3.72	3.74	3.77	3.79	4.18	4.57	4.97
t_{da}	3.59	3.60	3.62	3.63	3.65	4.04	4.43	4.82
t_{dz}	0.49	0.51	0.53	0.54	0.56	0.58	0.60	0.62
t_{zd}	0.56	0.58	0.60	0.62	0.63	0.65	0.67	0.69
t_{od}	0.64	0.66	0.68	0.70	0.72	0.73	0.75	0.77
Power (µW/MHz)								
Power_read	37.56	50.09	64.41	82.89	110.84	137.67	160.72	184.28
Power_write	41.25	53.89	68.49	87.64	117.24	151.29	191.08	232.44
Power_standby	1.53	2.05	2.58	3.14	3.75	4.46	5.01	5.64
Area (µm)								
Width	377.24	550.04	722.84	895.64	1068.44	1241.24	1414.04	1586.84
Height	221.56	252.01	312.90	434.70	678.28	1174.60	1670.92	2167.24

NOTES:

1. In power consumption of DPSRAM_LPL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is tied to low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

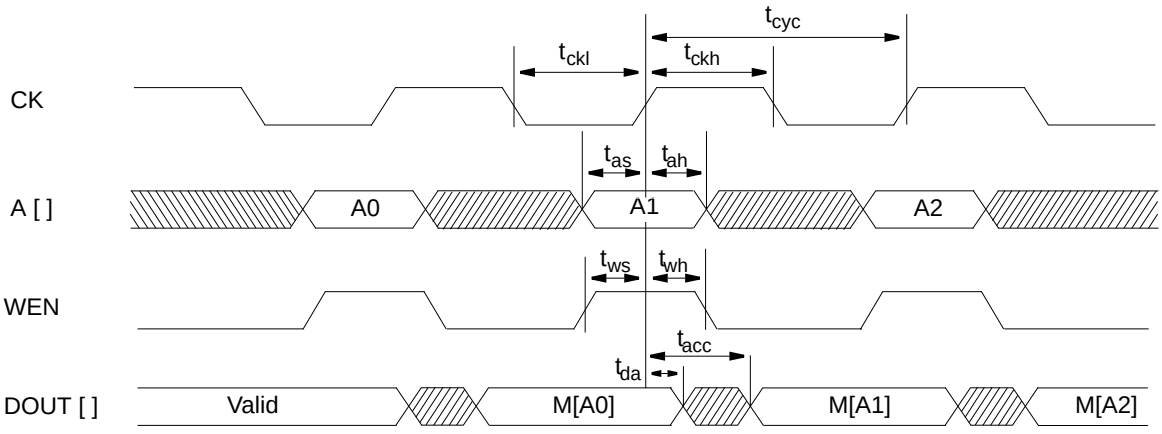
Parameters								
words	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**12288**	**16384**
bpw	**2**	**4**	**6**	**8**	**10**	**12**	**14**	**16**
Timing (ns)								
t_{cyc}	4.18	4.20	4.22	4.24	4.26	4.65	5.04	5.44
t_{ckl}	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36
t_{ckh}	1.31	1.31	1.31	1.31	1.31	1.31	1.30	1.30
t_{cc}	2.32	2.34	2.36	2.38	2.40	2.81	3.24	3.68
t_{as}	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.37	0.37	0.37
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.35	0.34	0.32	0.31	0.30	0.29	0.27	0.26
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.63	0.63	0.63	0.63	0.63	0.64	0.64	0.64
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.75	3.77	3.79	3.81	3.83	4.22	4.62	5.01
t_{da}	3.62	3.64	3.65	3.67	3.69	4.07	4.46	4.85
t_{dz}	0.49	0.52	0.55	0.57	0.60	0.62	0.65	0.67
t_{zd}	0.57	0.59	0.62	0.64	0.67	0.69	0.72	0.74
t_{od}	0.65	0.68	0.70	0.73	0.75	0.77	0.80	0.82
Power (µW/MHz)								
Power_read	36.03	47.05	59.88	76.92	103.55	128.50	149.58	171.04
Power_write	40.01	51.12	63.86	80.41	105.65	132.20	163.28	194.20
Power_standby	1.27	1.54	1.82	2.12	2.48	2.94	20	3.52
Area (µm)								
Width	377.24	550.04	722.84	895.64	1068.44	1241.24	1414.04	1586.84
Height	221.56	252.01	312.90	434.70	678.28	1174.60	1670.92	2167.24

NOTES:

1. In power consumption of DPSRAM_LPL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is tied to low.

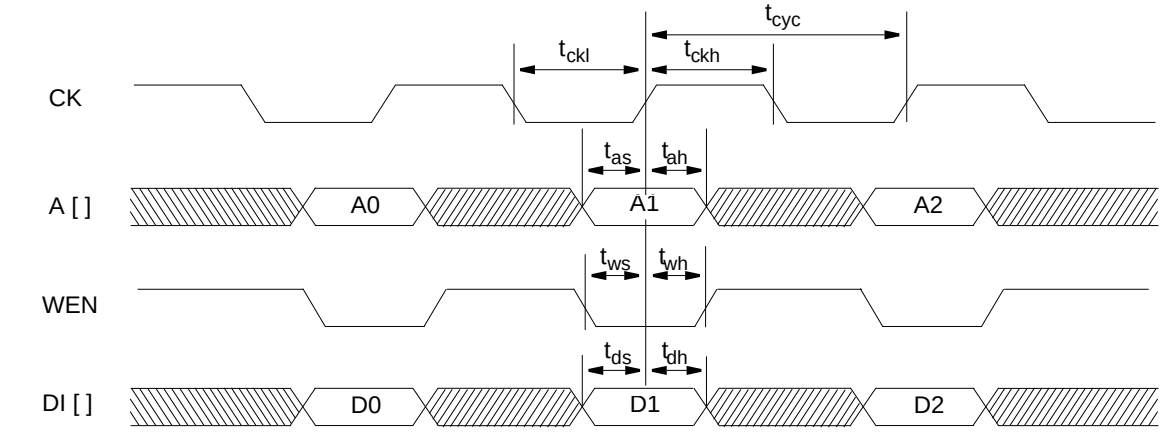
Timing Diagrams

Read Cycle



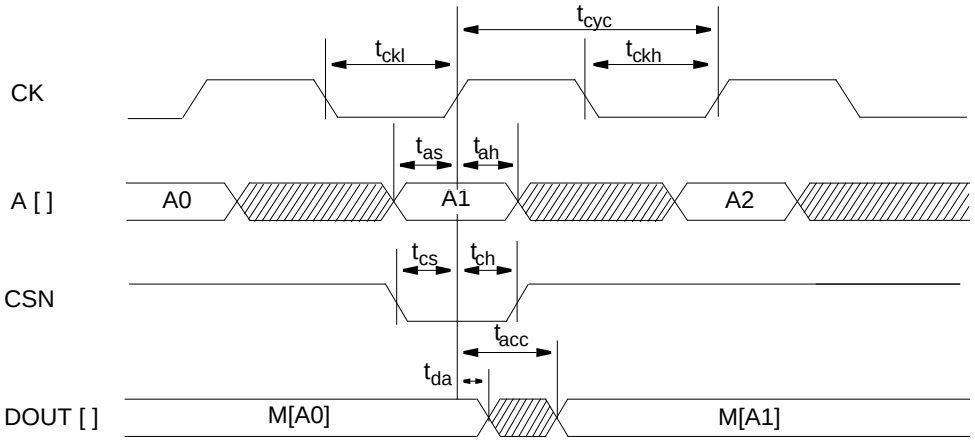
(CSN = low, OEN = low, DI[ ] = don't care)

Write Cycle



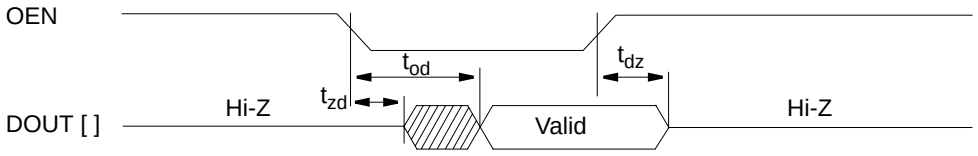
(CSN= low, OEN = don't care)

Read Cycle with CSN Controlled



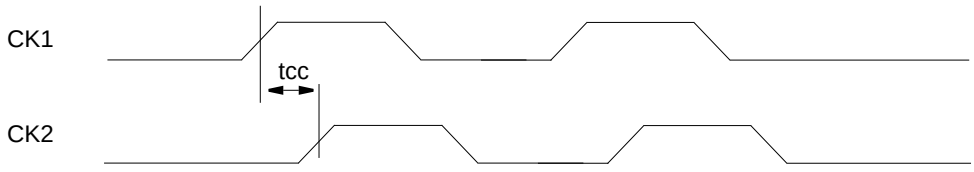
(OEN = low, WEN = high, DI[ ]= don't care)

OEN Controlled Output Enable



(CSN = low, CK, A[ ], WEN, DI[ ] = don't care)

Contention Mode



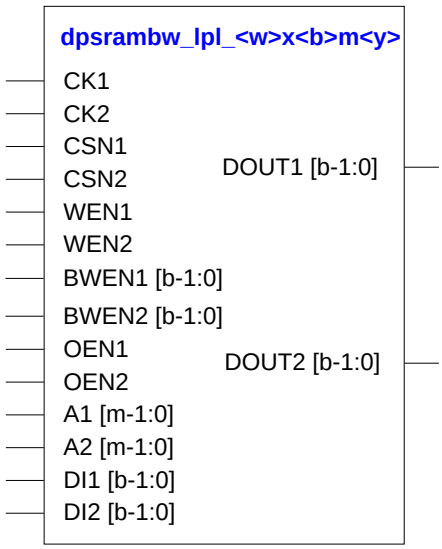
(A1[ ] = A2[ ])

NOTE: "don't care" means the condition that these pins are in normal operation mode.

DPSRAMBW_LPL

Low-Power Dual-Port Synchronous Static RAM with Bit-Write

Logic Symbol



NOTES:

1. Words (w) is the number of words..
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the column mux types.
4. m = $\lceil \log_2 w \rceil$

Features

- Suitable for Low-Power application
- Separated data I/O
- Synchronous operation
- Duty-free clock cycle
- Asynchronous tri-state ouput control
- Latched inputs and outputs
- Automatic power-down
- Zero standby current
- Zero hold time
- Low noise output optimizatioin
- Flexible aspect ratio
- Up to 256Kbits capacity
- Up to 16K number of words
- Up to 128 number of bit per word

Function Description

DPSRAMBW_LPL is a dual-port synchronous static RAM with bit-write capability which is provided as a compiler. DPSRAMBW_LPL is intended for use in Low-Power applications. Each port is fully independent. Basically, its functionality is exactly same as DPSRAM_HDL except a bit-write operation which is controlled by BWEN1[](BWEN2[]), named bit-write enable signal bus. Each bit of BWEN1[](BWEN2[]) enables or disable the write operation of its corresponding bit in DI1[](DI2[]). On the rising edge of CK1(CK2), the write cycle is initiated when WEN1(WEN2) is low and CSN1(CSN2) is low. The data bits in DI1[](DI2[]), which their corresponding bit(s) in BWEN1[](BWEN2[]) are low, are written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEN2[]) are high, any data in DI1[](DI2[]) are not written into the memory location specified on A1[](A2[]). When all bits of BWEN1[](BWEM2[]) are low, the data in DI1[](DI2[]) are written into the memory location specified on A1[](A2[]), which is exactly same as the write operation in DPSRAM_LPL. During the write cycle, DOUT1[](DOUT2[]) remains stable. On the rising edge of CK1(CK2), the read cycle is initiated when WEN1(WEN2) is high and CSN1(CSN2) is low. The data at DOUT1[](DOUT2[]) become valid after a delay. While in standby mode that CSN1(CSN2) is high, A1[](A2[]) and DI1[](DI2[]) are disabled, data stored in the memory is retained and DOUT1[](DOUT2[]) remains stable. When OEN1(OEN2) is high, DOUT1[](DOUT2[]) is placed in a high-impedance state.

DPSRAMBW_LPL Function Table

CK1 CK2	CSN1 CSN2	WEN1 WEN2	OEN1 OEN2	A1 A2	BWEN1 BWEN2	DI1 DI2	DOUT1 DOUT2	Comment
X	X	X	H	X	X	X	Z	Unconditional tri-state output
X	H	X	L	X	X	X	DOUT(t-1)	De-selected (standby mode)
↑	L	L	L	Valid	all L	Valid	DOUT(t-1)	Word-write cycle
↑	L	L	L	Valid	L	Valid	DOUT(t-1)	Bit-write cycle
↑	L	L	L	Valid	all H	Valid	DOUT(t-1)	No operation
↑	L	H	L	Valid	X	X	MEM(A)	Read cycle

Parameter Description

DPSRAMBW_LPL is the compiler that automatically generates symbol, netlist, timing model, power model and layout according to the following parameters; Number of words(w), Number of bit per word(b) and Column mux(y).

Parameters		Ymux(y) = 2	Ymux(y) = 4	Ymux(y) = 8	Ymux(y) = 16
Words (w)	Min	32	64	128	256
	Max	2048	4096	8192	16384
	Step	16	32	64	128
Bpw (b)	Min	1	1	1	1
	Max	128	64	32	16
	Step	1	1	1	1

DPSRAMBW_LPL

Low-Power Dual-Port Synchronous Static RAM with Bit-Write

Pin Descriptions

Name	Type	Description
CK1 CK2	Clock	Clock input. CSN, WEN, A[] and DI[] are latched into the RAM on the rising edge of CK. If CSN and WEN are low on the rising edge of CK, the RAM is in write mode. If WEN is high on the rising edge of CK, the RAM is in read mode. Upon the falling edge of CK, the RAM is in a precharge state.
CSN1 CSN2	Chip Enable	Chip Enable input. The chip enable is active-low and is latched into the RAM on the rising edge of CK. When CSN is low, the RAM is enabled for reading or writing, depending on the state of WEN. When CSN is high, the RAM goes to the standby mode and is disabled for reading or writing. DOUT remains previous data output.
WEN1 WEN2	Read/Write Enable	Read or write enable input. The read/write enable is latched into the RAM on the rising edge of CK. When WEN is low, data are written to the addressed location and DOUT remains stable. When WEN is high, data from the addressed word are present at DOUT.
BWEN1 [ ] BWEN2 [ ]	Bit-Write Enable	Bit-write enable input bus. The bit-write enable is latched into the RAM on the rising edge of CK. Each bit of BWEN[] enables/disables the write operation of corresponding data bit. BWEN[i] corresponds to DI[i] in bit-write. If WEN and BWEN[0] are low and BWEN[1] is high, DI[0] is written into the memory location specified on A[], but DI[1] is not written.
OEN1 OEN2	Data Output Enable	Data output enable input. The data output enable is asynchronously operated regardless of the state of other inputs. When OEN is high, DOUT is disabled and goes to high-impedance state.
A1 [ ] A2 [ ]	Address	Address input bus. The address is latched into the RAM on the rising edge of CK.
DI1 [ ] DI2 [ ]	Data Input	Data input bus. Data are latched on the rising edge of CK. Data input is written into the addressed location in write mode.
DOUT1 [ ] DOUT2 [ ]	Data Output	Data output bus. Data output is valid after the rising edge of CK while the RAM is in read mode. Data output remains previous data output while the RAM is in write mode.

Pin Capacitance

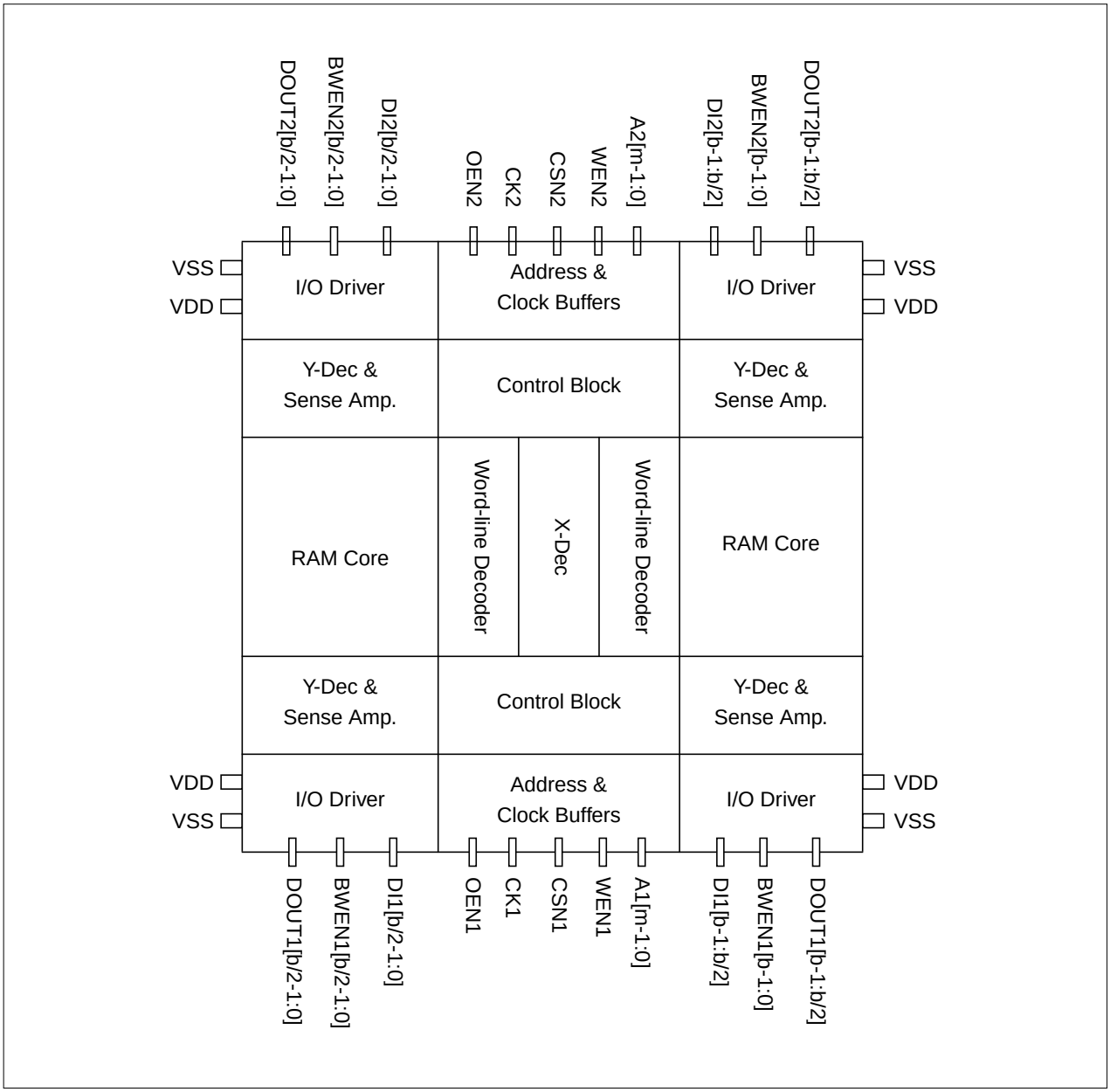
(Unit = SL)

CK	CSN	WEN	BWEN	OEN	A	DI	DOUT
9.24	2.38	2.34	2.40	3.18	2.34	2.34	3.91

NOTE: Each pin's capacitance is exactly same regardless of available mux types.

Block Diagram

DPSRAMBW_LPL supports only 1-bank architecture. The power ports are located on the top-edge and the bottom edge of both right- and left-sides of the memory. However, DPSRAMBW_LPL has two symmetrical ports located on opposite edges of memory. Port1 is located on the bottom of the memory while Port2 is located on the top of the memory.



DPSRAMBW_LPL

Low-Power Dual-Port Synchronous Static RAM with Bit-Write

Application Notes

1. Permitting Over-the-cell routing.
In chip-level layout, over-the-cell routing in DPSRAMBW_LPL is permitted for only Metal-5 layer and Metal-6 layers.

2. Incoming power bus should be adjusted to guarantee NOT more than 10% voltage drop at typical-case current levels.

3. Power stripe should be tapped from both sides of DPSRAMBW_LPL.

4. Contention mode in same address access.
In DPSRAMBW_LPL, simultaneous operation by both ports on the same memory address, as write/write, write/read or read/write operation, causes a contention problem. Simultaneous operation is defined as a state in which both ports are enabled, both address buses are equal at the rising edge of CK. DPSRAMBW_LPL has no scheme preventing the contention. Due to simultaneous operation, silicon will behave unpredictably. A write operation cannot end and data appearing at outputs may not be valid. Please refer to the timing diagrams if you want to avoid the contention mode between both ports. In write/write operation, the data stored at the current address will be unpredictable. In write/read or read/write operation, the read port is invalid while the write port is still valid. If you want to avoid the contention mode, you have to give the value greater than tcc (clock-to-clock setup time). However, simultaneous read/read is allowable without any restrictions.

5. A byte-write or word-write operation with DPSRAMBW_LPL.
Refer to the function table. In byte-write operation, the number of BWEN[] signal bus should be divided by a byte (8) and eight BWEN signals should be tied to a connection wire. In this case, DI[] bus is controlled by a byte-wired BWEN signal instead of each BWEN bit. In word-write operation, the functionality is exactly same as DPSRAM_LPL. If all of BWEN[] signal is tied to low state, DI[] bus is only controlled by WEN.

6. Power reduction during standby mode.
The standby power is measured on the condition that only CSN is disable mode and other signals are in operation mode except that OEN is tied to low. If any of signals are activated while in standby mode, the power will be consumed because the input switching activities are occurred by the signal transition. Therefore, to reduce unnecessary power consumption, you should keep stable for all signals while in standby mode.

Characteristics

Definition for AC Timing (ns)			
Symbol	**Description**	**Symbol**	**Description**
t_{cyc}	Clock cycle time	t_{ckl}	Clock pulse width low
t_{ckh}	Clock pulse width high	t_{cc}	Clock to Clock Setup time
t_{as}	Address setup time	t_{ah}	Address hold time
t_{cs}	CSN setup time	t_{ch}	CSN hold time
t_{ds}	Data-In setup time	t_{dh}	Data-In hold time
t_{ws}	WEN setup time	t_{wh}	WEN hold time
t_{bws}	BWEN setup time	t_{bwh}	BWEN hold time
t_{acc}	Data access time	t_{da}	De-access time
t_{dz}	DOUT drive to high-Z time	t_{zd}	DOUT high-Z to drive time
t_{od}	OEN to valid output time		
Definition for Power Consumption (µW/MHz)			
Power_read	The dynamic average power consumption while in a read cycle		
Power_write	The dynamic average power consumption while in a write cycle		
Power_standby	The standby power consumption while CSN is high, OEN is low and other signals are in normal operation		
Definition for Area (µm)			
Width	The physical width in X-direction		
Height	The physical height in Y-direction		

DPSRAMBW_LPL

Low-Power Dual-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=2** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**32**	**64**	**128**	**256**	**512**	**1024**	**1536**	**2048**
bpw	**16**	**32**	**48**	**64**	**80**	**96**	**112**	**128**
Timing (ns)								
t_{cyc}	4.12	4.15	4.18	4.21	4.24	4.65	5.06	5.46
t_{ckl}	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36
t_{ckh}	1.31	1.31	1.31	1.31	1.31	1.31	1.31	1.31
t_{cc}	2.32	2.34	2.36	2.38	2.40	2.81	3.24	3.68
t_{as}	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.36	0.35	0.34	0.33	0.32	0.30	0.29	0.28
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.63	0.63	0.63	0.63	0.63	0.63	0.63	0.63
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.36	0.35	0.34	0.33	0.32	0.30	0.29	0.28
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.70	3.73	3.76	3.79	3.82	4.22	4.63	5.04
t_{da}	3.58	3.60	3.62	3.64	3.67	4.07	4.47	4.86
t_{dz}	0.49	0.52	0.55	0.57	0.60	0.62	0.65	0.68
t_{zd}	0.56	0.59	0.61	0.64	0.66	0.68	0.71	0.73
t_{od}	0.65	0.67	0.70	0.72	0.74	0.77	0.79	0.81
Power (µW/MHz)								
Power_read	52.43	79.57	108.20	140.28	180.16	224.46	266.46	310.13
Power_write	53.52	81.54	112.86	151.97	209.05	287.07	376.50	475.35
Power_standby	5.06	9.10	13.15	17.22	21.33	25.62	29.77	34.09
Area (µm)								
Width	377.24	550.04	722.84	895.64	1068.44	1241.24	1414.04	1586.84
Height	221.56	252.01	312.90	434.70	678.28	1174.60	1670.92	2167.24

NOTES:

1. In power consumption of DPSRAMBW_LPL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is tied to low.

Reference Table

*** For Ymux=4** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**64**	**128**	**256**	**512**	**1024**	**2048**	**3072**	**4096**
bpw	**8**	**16**	**24**	**32**	**40**	**48**	**56**	**64**
Timing (ns)								
t_{cyc}	4.11	4.13	4.15	4.17	4.19	4.59	4.98	5.38
t_{ckl}	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36
t_{ckh}	1.31	1.31	1.31	1.31	1.31	1.31	1.31	1.31
t_{cc}	2.32	2.34	2.36	2.38	2.40	2.81	3.24	3.68
t_{as}	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.37	0.36	0.35	0.34	0.33	0.32	0.31	0.30
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.63	0.63	0.63	0.63	0.63	0.63	0.63	0.63
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.37	0.36	0.35	0.34	0.33	0.32	0.31	0.30
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.68	3.70	3.72	3.74	3.76	4.16	4.56	4.95
t_{da}	3.57	3.58	3.60	3.61	3.63	4.02	4.42	4.81
t_{dz}	0.49	0.50	0.52	0.54	0.56	0.58	0.60	0.62
t_{zd}	0.56	0.58	0.59	0.61	0.63	0.65	0.67	0.68
t_{od}	0.64	0.66	0.68	0.70	0.71	0.73	0.75	0.77
Power (µW/MHz)								
Power_read	41.76	58.30	76.58	98.92	130.48	161.97	190.09	218.81
Power_write	42.52	59.17	78.36	103.52	142.43	192.17	250.17	312.77
Power_standby	3.04	5.06	7.09	9.15	11.27	13.52	15.48	17.63
Area (µm)								
Width	377.24	550.04	722.84	895.64	1068.44	1241.24	1414.04	1586.84
Height	221.56	252.01	312.90	434.70	678.28	1174.60	1670.92	2167.24

NOTES:

1. In power consumption of DPSRAMBW_LPL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is tied to low.

DPSRAMBW_LPL

Low-Power Dual-Port Synchronous Static RAM with Bit-Write

Reference Table

*** For Ymux=8** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

Parameters								
words	**128**	**256**	**512**	**1024**	**2048**	**4096**	**6144**	**8192**
bpw	**4**	**8**	**12**	**16**	**20**	**24**	**28**	**32**
Timing (ns)								
t_{cyc}	4.13	4.15	4.17	4.19	4.21	4.60	5.00	5.39
t_{ckl}	1.36	1.36	1.36	1.36	1.35	1.36	1.36	1.36
t_{ckh}	1.31	1.31	1.31	1.31	1.31	1.31	1.31	1.31
t_{cc}	2.32	2.34	2.36	2.38	2.40	2.81	3.24	3.68
t_{as}	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.37	0.37	0.37
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.36	0.35	0.34	0.33	0.32	0.31	0.30	0.29
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.63	0.63	0.63	0.63	0.63	0.63	0.63	0.63
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.36	0.35	0.34	0.33	0.32	0.31	0.30	0.29
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.71	3.72	3.74	3.77	3.79	4.18	4.57	4.97
t_{da}	3.59	3.60	3.62	3.63	3.65	4.04	4.43	4.82
t_{dz}	0.49	0.51	0.53	0.54	0.56	0.58	0.60	0.62
t_{zd}	0.56	0.58	0.60	0.62	0.63	0.65	0.67	0.69
t_{od}	0.64	0.66	0.68	0.70	0.72	0.73	0.75	0.77
Power (μW/MHz)								
Power_read	37.56	50.09	64.71	82.89	110.84	137.67	160.72	184.28
Power_write	41.76	54.91	70.00	89.64	119.74	154.28	194.57	236.43
Power_standby	2.05	3.06	4.09	5.15	6.25	7.45	8.50	9.62
Area (μm)								
Width	377.24	550.04	722.84	895.64	1068.44	1241.24	1414.04	1586.84
Height	221.56	252.01	312.90	434.70	678.28	1174.60	1670.92	2167.24

NOTES:

1. In power consumption of DPSRAMBW_LPL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is tied to low.

Reference Table

*** For Ymux=16** (Typical process, 1.8V, 25°C, Output load = 10SL, Input slope = 0.2 ns, SA=0.5)

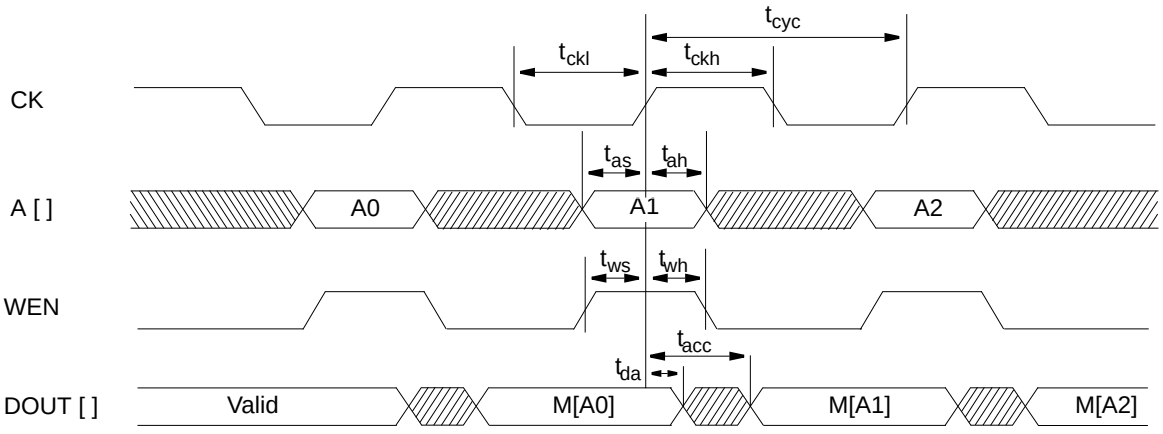
Parameters								
words	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**12288**	**16384**
bpw	**2**	**4**	**6**	**8**	**10**	**12**	**14**	**16**
Timing (ns)								
t_{cyc}	4.18	4.20	4.22	4.24	4.26	4.65	5.04	5.44
t_{ckl}	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36
t_{ckh}	1.31	1.31	1.31	1.31	1.31	1.31	1.30	1.30
t_{cc}	2.32	2.34	2.36	2.38	2.40	2.81	3.24	3.68
t_{as}	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
t_{ah}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{cs}	0.36	0.36	0.36	0.36	0.36	0.37	0.37	0.37
t_{ch}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ds}	0.35	0.34	0.32	0.31	0.30	0.29	0.27	0.26
t_{dh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{ws}	0.63	0.63	0.63	0.63	0.63	0.64	0.64	0.64
t_{wh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{bws}	0.35	0.34	0.32	0.31	0.30	0.29	0.27	0.26
t_{bwh}	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
t_{acc}	3.75	3.77	3.79	3.81	3.83	4.22	4.62	5.01
t_{da}	3.62	3.64	3.65	3.67	3.69	4.07	4.46	4.85
t_{dz}	0.49	0.52	0.55	0.57	0.60	0.62	0.65	0.67
t_{zd}	0.57	0.59	0.62	0.64	0.67	0.69	0.72	0.74
t_{od}	0.65	0.68	0.70	0.73	0.75	0.77	0.80	0.82
Power (µW/MHz)								
Power_read	36.03	47.05	59.88	76.92	103.55	128.50	149.58	171.04
Power_write	40.28	51.64	64.63	81.43	106.90	133.71	165.05	196.21
Power_standby	1.54	2.06	2.58	3.13	3.74	4.45	4.95	5.53
Area (µm)								
Width	377.24	550.04	722.84	895.64	1068.44	1241.24	1414.04	1586.84
Height	221.56	252.01	312.90	434.70	678.28	1174.60	1670.92	2167.24

NOTES:

1. In power consumption of DPSRAMBW_LPL, only one port is measured and the other port is isolated.
2. Standby power is measured on the condition that other signals are in normal operation while CSN is in disable mode and OEN is tied to low.

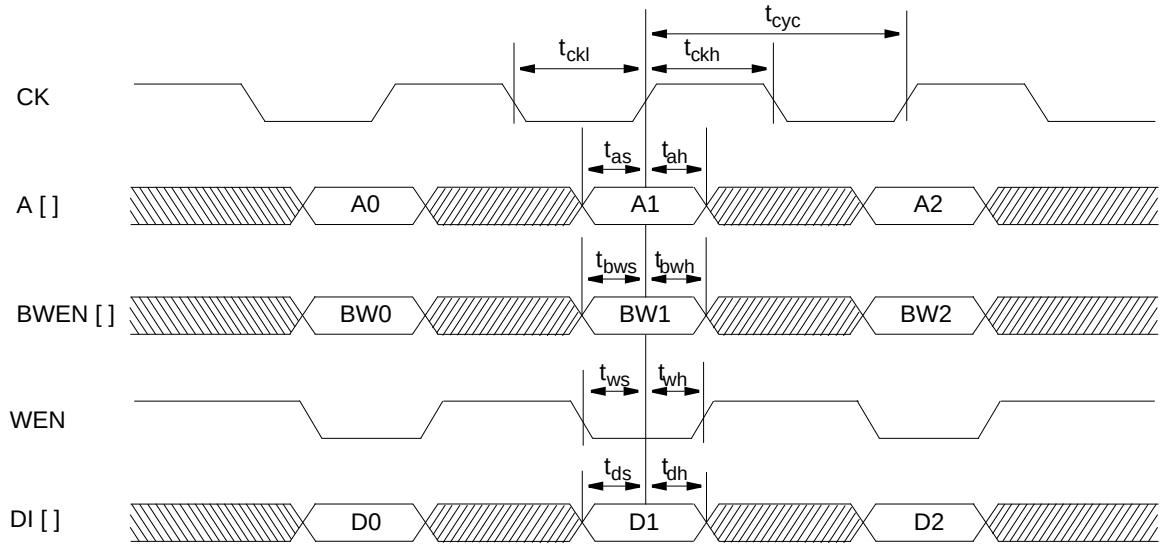
Timing Diagrams

Read Cycle



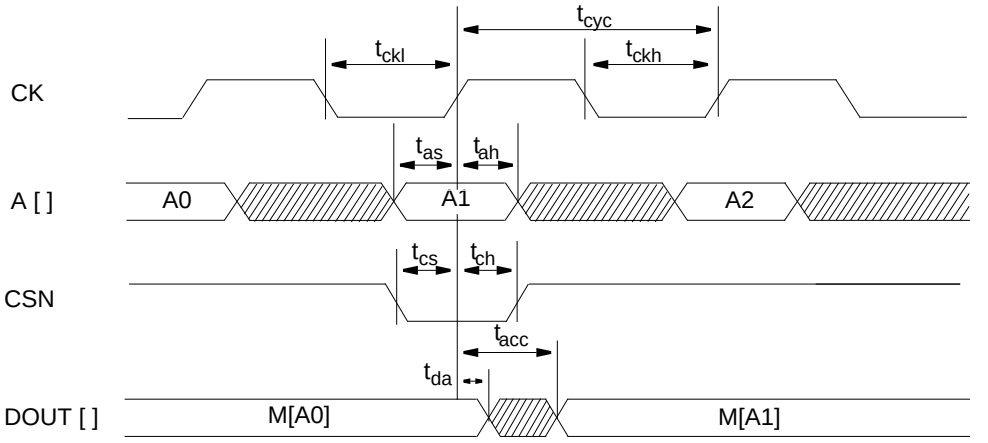
(CSN = low, OEN = low, DI[ ], BWEN[ ]= don't care)

Write Cycle



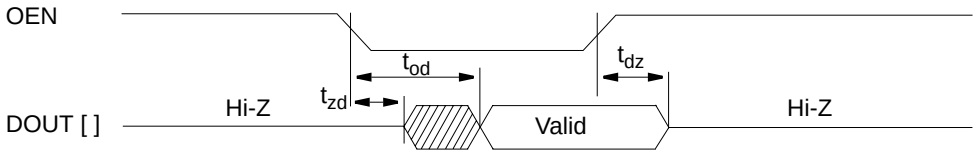
(CSN = low, OEN = don't care)

Read Cycle with CSN Controlled



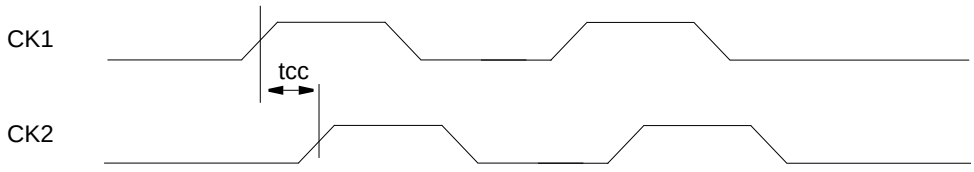
(OEN = low, WEN = high, DI[ ], BWEN[ ] = don't care)

OEN Controlled Output Enable



(CSN = low, CK, A[ ], WEN, DI[ ], BWEN[ ] = don't care)

Contention Mode



(A1[ ] = A2[ ])

NOTE: "don't care" means the condition that these pins are in normal operation mode.

PLL

6

Contents

PLL2099X 6-1

GENERAL DESCRIPTION

The pll299x is a Phase-Locked Loop (PLL) frequency synthesizer constructed in CMOS on single monolithic structure. The PLL macro-functions provide frequency multiplication capabilities. The output clock frequency FOUT is related to the input clock frequency FIN by the following equation:

$$\mathbf{FOUT = (m \times FIN) / (p \times 2^S)}$$

Where, FOUT is the output clock frequency. FIN is the input clock frequency. m, p and s are the values for programmable dividers. pll2099x consists of a Phase/Frequency Detector(PFD), a Charge Pump, an Internal Loop Filter, a Voltage Controlled Oscillator(VCO), a 6-bit Pre-divider, an 8-bit Main divider and 2-bit Post Scaler as shown in Functional Block Diagram.

FEATURES

- 0.18um CMOS device technology
- 1.8V single power supply
- Output frequency range: 20 ~ 300 MHz
- Jitter ±120ps at 300MHz
- Duty ratio 45% to 55% (All tuned range)
- Frequency changed by programmable divider
- Power down mode

NOTES

1. Don't set the P or M as zero, that is 000000 / 00000000
2. The proper range of P and M : $1 \le P \le 62$, $1 \le M \le 248$
3. The P and M must be selected considering stability of PLL and VCO output frequency range
4. Please consult with SEC application engineer to select the proper P, M and S values

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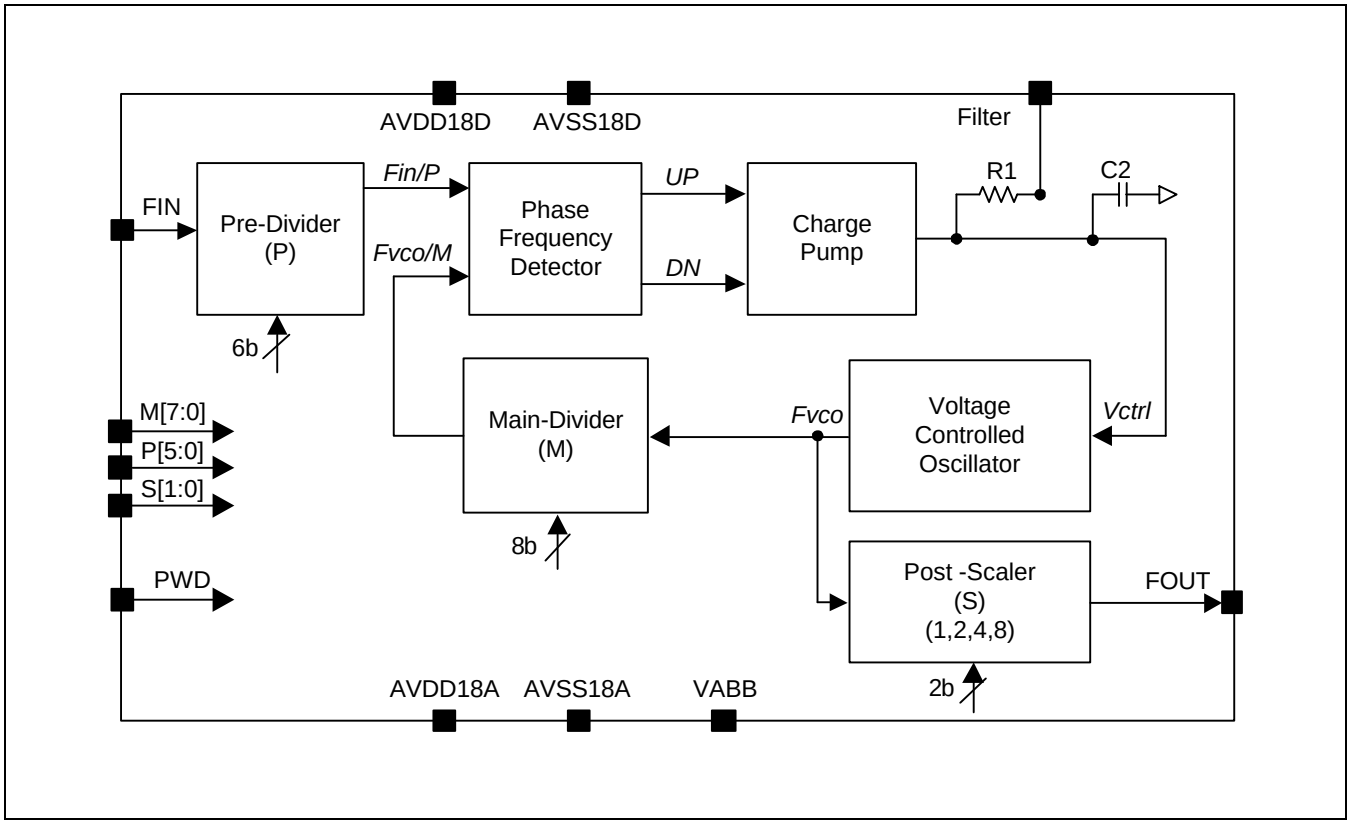
FUNCTIONAL BLOCK DIAGRAM



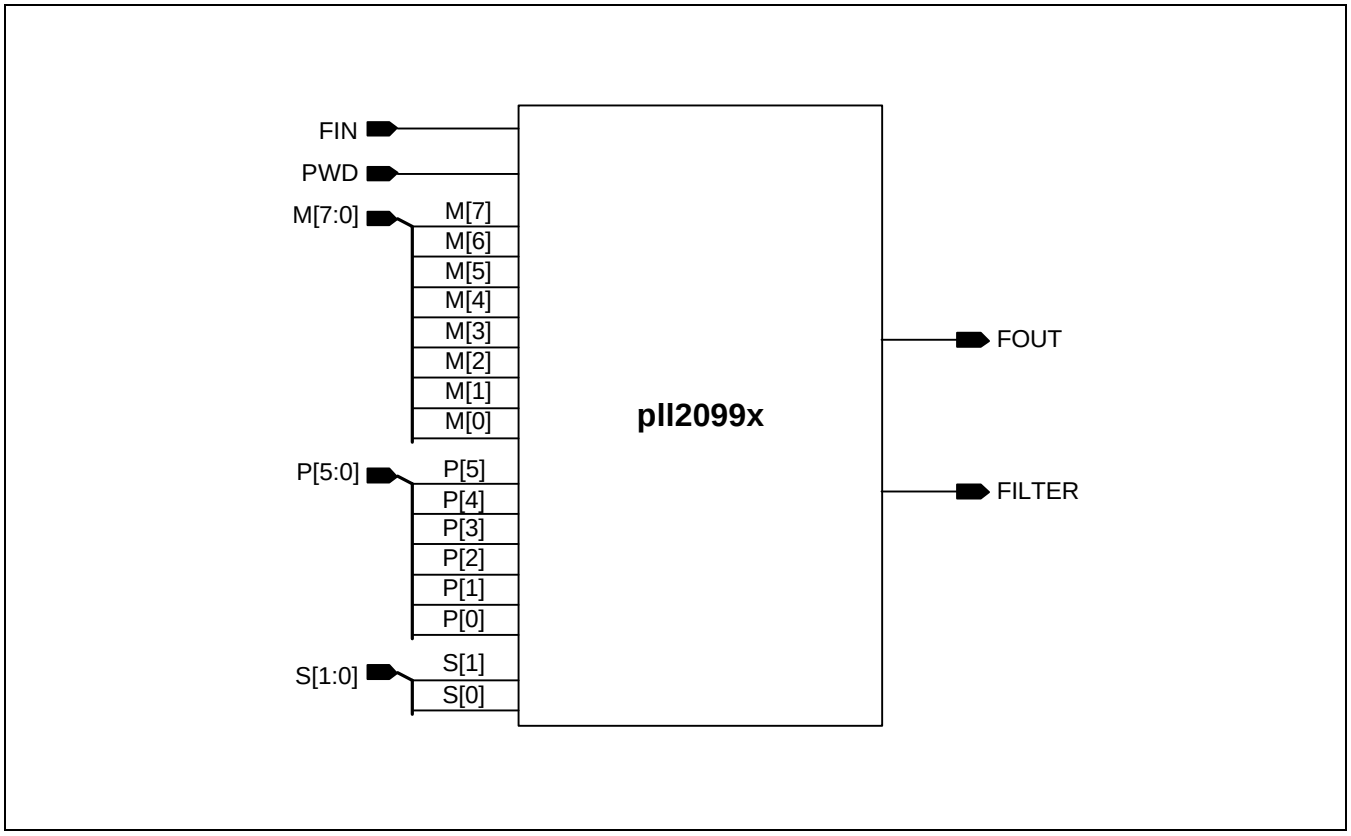
CORE PIN DESCRIPTION

Pin Name	I/O Type	Pin Description
AVDD18D	DP	Digital power supply
AVSS18D	DG	Digital ground
AVDD18A	AP	Analog power supply
AVSS18A	AG	Analog ground
VABB	AB/DB	Bulk ground
FIN	DI	Reference frequency input
FILTER	AO	Pump out is connected to filter A capacitor is connected between the pin and analog ground
FOUT	DO	20MHz ~ 300MHz clock output
PWD	DI	FSPLL clock power down. - When PWD is High, PLL do not operate. - If customer don't use this pin, apply it to AVSS18D
P[5:0]	DI	The values for 6-bit programmable pre-divider.
M[7:0]	DI	The values for 8-bit programmable main divider.
S[1:0]	DI	The values for 2-bit programmable post scaler.

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bi-direction
— DB: Digital Bi-direction
— AP: Analog Power
— AG: Analog Ground
— DP: Digital Power
— DG: Digital Ground
— BD: Bi-directional Port

CORE CONFIGURATION



RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage differential	AVDD18D-AVDD18A	–0.1		+0.1	V
External loop filter capacitance	LF		320		pF
Operating temperature	Topr	–40		85	°C

NOTE: It is strongly recommended that all the supply pins (AVDD18D, AVDD18A) be powered to the same supply voltage to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	AVDD18D/AVDD18A	1.65	1.8	1.95	V
Digital input voltage high	V_{IH}	0.7VDD			V
Digital input voltage low	V_{IL}			0.3VDD	V
Dynamic current	I_{dd}			3	mA
Power down current	I_{pd}			40	uA

AC ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Min	Typ	Max	Unit
Input frequency		F_{IN}	4		40	MHz
Output clock frequency		F_{OUT}	20		300	MHz
VCO output frequency		F_{VCO}	160		400	MHz
Input clock duty cycle		T_{ID}	40		60	%
Output clock duty cycle (at 300MHz)		T_{OD}	45		55	%
Input glitch pulse width		T_{IGP}			1	ns
Locking time		T_{LT}			150	us
Cycle to cycle jitter	20 ~ 100MHz	T_{JCC}	–300		+300	ps
	100 ~ 200MHz		–200		+200	
	200 ~ 300MHz		–120		+120	

NOTE: It is strongly recommended that input signal is not generated glitch, but if consumer cannot help generating glitch, Consumer must carefully considerate the specification.

FUNCTIONAL DESCRIPTION

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase. The pll2099x can provide frequency multiplication capabilities, but does not guarantee phase synchronization between FIN and FOUT.

In this application, it includes the following basic blocks.

- The voltage-controlled oscillator (VCO) generates VCO output frequency (Fvco) with loop filter DC voltage.
- The divider P divides the input frequency by p.
- The Main-divider divides the Fvco by m.
- The Post-divider divides the Fvco by s and generates FOUT.
- The phase frequency detector detects the phase difference between the reference frequency (=FIN/p) and the feedback frequency (=Fvco/m) and controls the loop filter DC voltage.
- The loop filter removes high frequency components and generates stable DC control voltage for VCO.

The m, p, s values can be programmed by **16-bit digital data** from the external source. So the PLL can be locked in the desired frequency.

Fout = m × Fin / p × s **(**m=M+8 , p=P+2, s=2^S)

Digital data format:

Main Divider	Pre Divider	Post Scaler
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S1, S0

NOTE: S[1] - S[0]: Output Frequency Scaler
M[7] - M[0] : VCO Frequency Divider
P[5] - P[0] : Input Frequency Divider

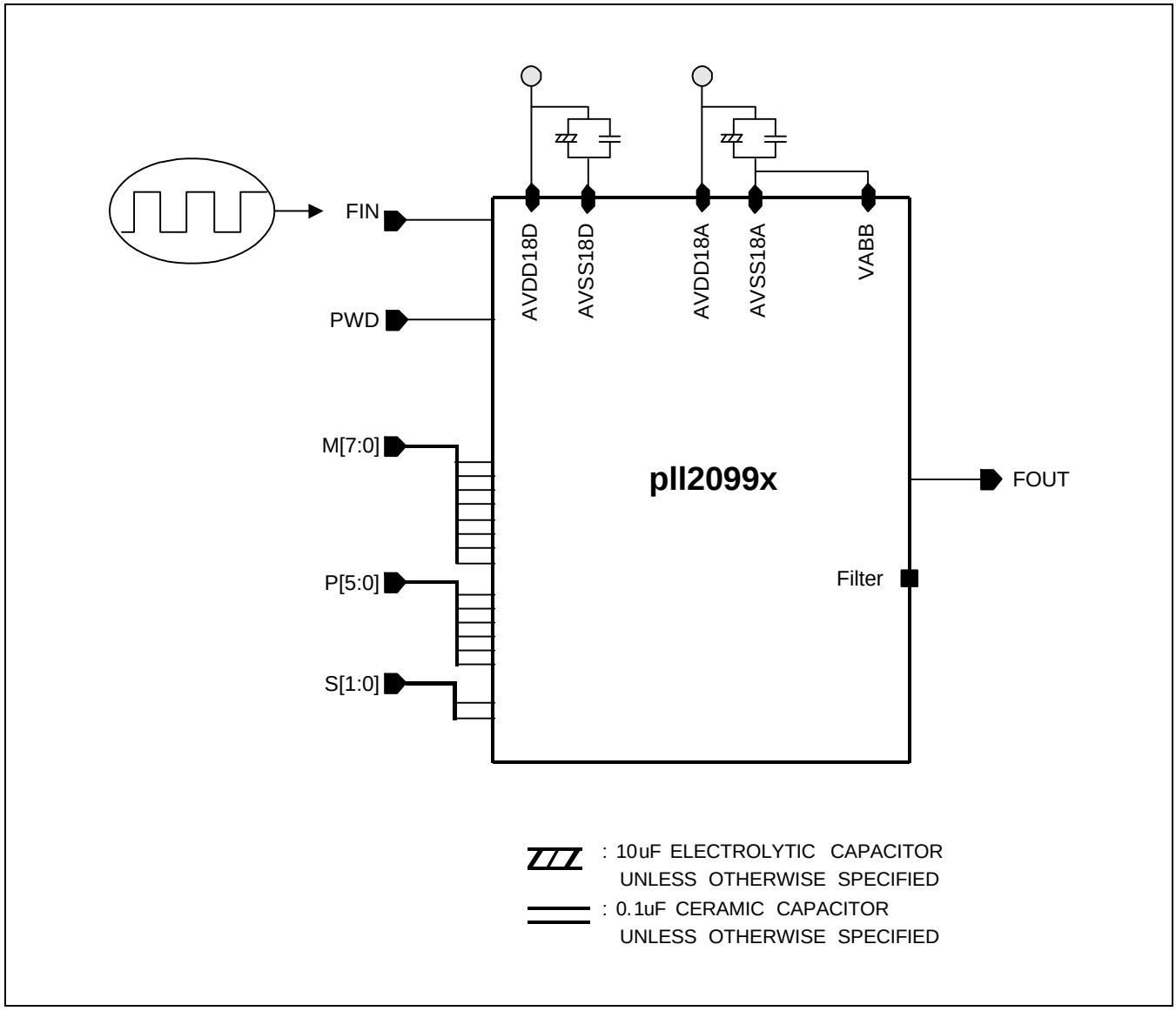
NOTE

Please contact SEC application engineer to confirm the proper selection of M, P, S values.

CORE EVALUATION GUIDE

1. The FOUT should be bypassed for external test.
2. The pll2099x doesn't contains loop filter (capacitor), so the FILTER is necessarily to be connected to external pin.
3. You can generate various output frequencies by changing M/P/S setting. There are two methods of controlling divider values
   - — Method 1: 16-bit register can be used for easy control of divider values.
   - — Method 2: P, M and S ports are bypassed to the external pin, and you can control each pin directly.

It is undesirable to connect P[5:0], M[7:0] and S[1:0] to the internal power or ground directly



CORE LAYOUT GUIDE

- The digital power(AVDD18D, AVSS18D) and the analog power(AVDD18A, AVSS18A) must be dedicated to PLL only and separated. If the dedicated AVDD18D and AVSS18D are not allowed, that of the least power consuming block is shared with the PLL.
- The FOUT and FILTER pins must be placed far from the internal signals in order to avoid overlapping signal lines.
- The blocks having a large digital switching current must be located away from the PLL core.
- The PLL core must be shielded by guard ring
- For the FOUT pad, you can use a custom drive buffer or pot8_lp buffer considering the drive current.

DESIGN CONSIDERATIONS

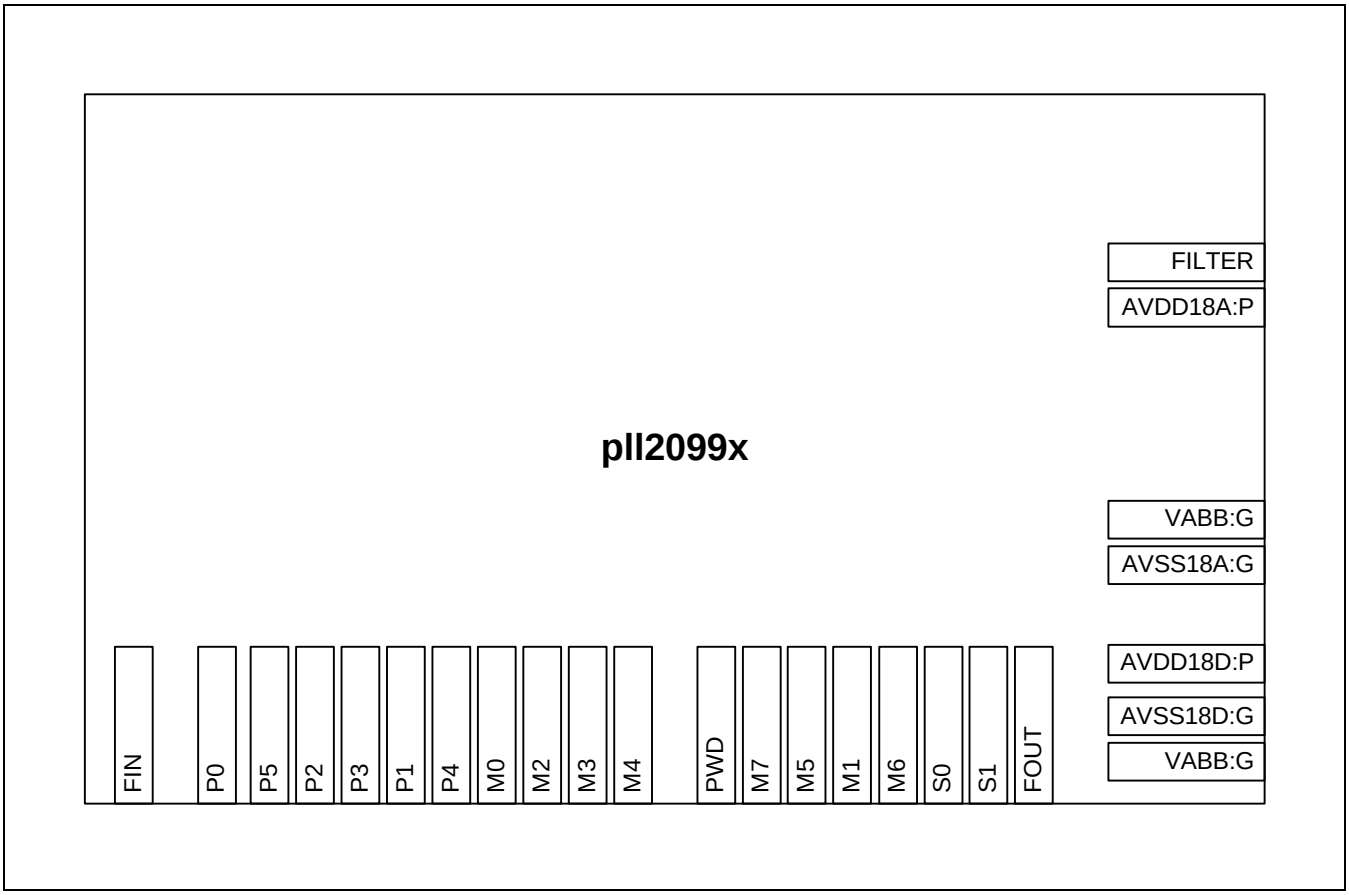
The following design considerations apply

- Jitter is affected by the power noise, substrate noise...etc. It increases when the noise level increases.
- A CMOS-level input reference clock is recommend for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
- The use of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
- The PLL core should be placed as close as possible to the dedicated loop filter and analog power and ground pins.
- It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
- Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction.

PHANTOM CELL INFORMATION

Pins of the core can be assigned externally(Package Pins) or internally(Internal Ports) depending on design methods.

- The term "External" implies that the pins should be assigned externally like power pins.
- The term "Internal/External" implies that these pins are user dependent.



PIN LAYOUT GUIDE

Pin Name	Pin Usage	Pin Layout Guide
AVDD18D	External	Use dedicated power/ground pins for PLL Power cuts are required to provide on-chip isolation => between dedicated PLL power/ground and all other power/ground Use good power and ground source on board
AVSS18D	External	
AVDD18A	External	
AVSS18A	External	
VABB	External	
FIN	External	Do not place noisy, high frequency and high power consuming circuitry pads near the FIN. Use proper low jitters reference clock
FOUT	External/Internal	Do not place noisy, high frequency and high power consuming circuitry pads near the FOUT. Internal routing path should be short. This will minimize loading effect. FOUT signals should not be crossed by any signals and should not run next to digital signals. This will minimize capacitive coupling between the two signals.
FILTER	External	Do not place noisy, high frequency and high power consuming circuitry pads near the FILTER. Ground shielding is needed for internal routing path. FILTER routing path should not be crossed by any signals and should not run next to digital signals. External loop filter pin should be placed between analog power and ground to avoid stray coupling outside the chip and magnetic coupling via bond wires. Closely placed Loop Filter components.
PWD	Internal/External	
M[7]~M[0]	Internal/External	
P[5]~P[0]	Internal/External	
S[1]~S[0]	Internal/External	

FEEDBACK REQUEST

Thank you for having an interest in our products. Please fill out this form, especially the items which you want to request.

Parameter		Customer	SEC	Unit
Process			0.18um CMOS	
Supply voltage (VDD)			1.8 ± 0.15	V
Input frequency (FIN)			4 ~ 40	MHz
Output frequency (FOUT)			20 ~ 300	MHz
Cycle to cycle jitter (TJCC)	20M ~ 100M		± 300	psec (pk-pk)
	100M ~ 200M		± 200	
	200M ~ 300M		± 120	
Period jitter (TJP)	20M ~ 100M		± 300	psec (pk-pk)
	100M ~ 200M		± 200	
	200M ~ 300M		± 120	
Output duty ratio (TOD)			45 ~ 55	%
Lock up time (TLT)			150	usec
Dynamic current			< 3m	A
Stand by current			< 40u	A
Filter capacitor			External	–

1. How many PLLs are embedded in your system?
2. Do you need synchronization between input clock and output clock?
3. Do you need another spec of jitter?

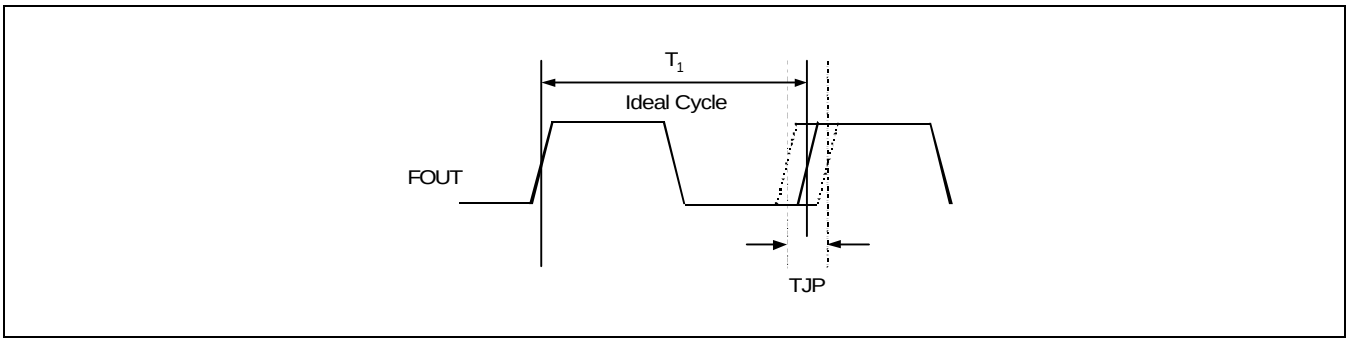
Parameter	Customer	Unit
Long-term Jitter (TJLT)		psec (pk-pk)
Tracking Jitter (TJT)		psec (pk-pk)

If you have another special request, please describe below.

JITTER DEFINITION

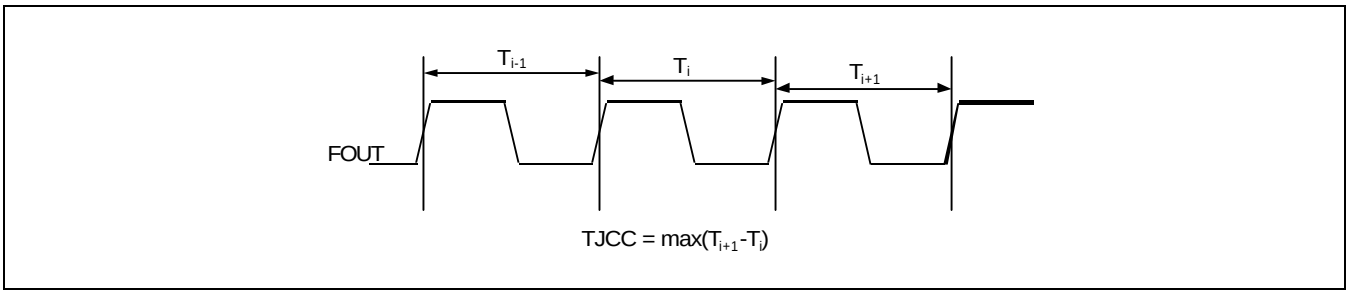
Period Jitter

Period jitter is the maximum deviation of output clock's transition from its ideal position.



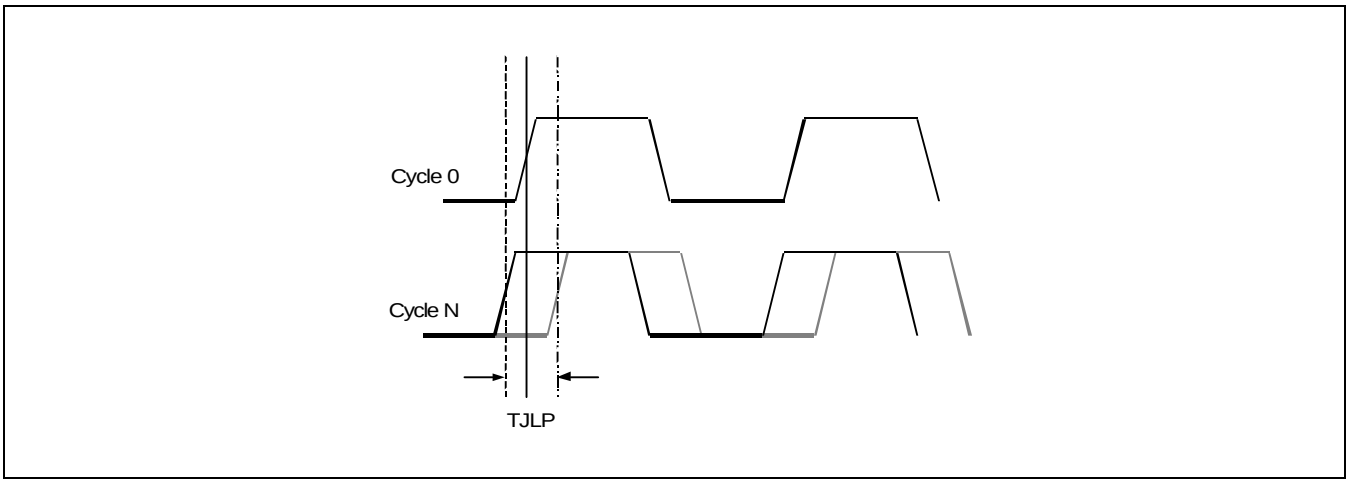
Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the maximum deviation of output clock's transition from its corresponding position of the previous cycle.



Long-Term Jitter

Long-term jitter is the maximum deviation of output clock's transition from its ideal position, after many cycles. The term "many" depends on the application and the frequency.



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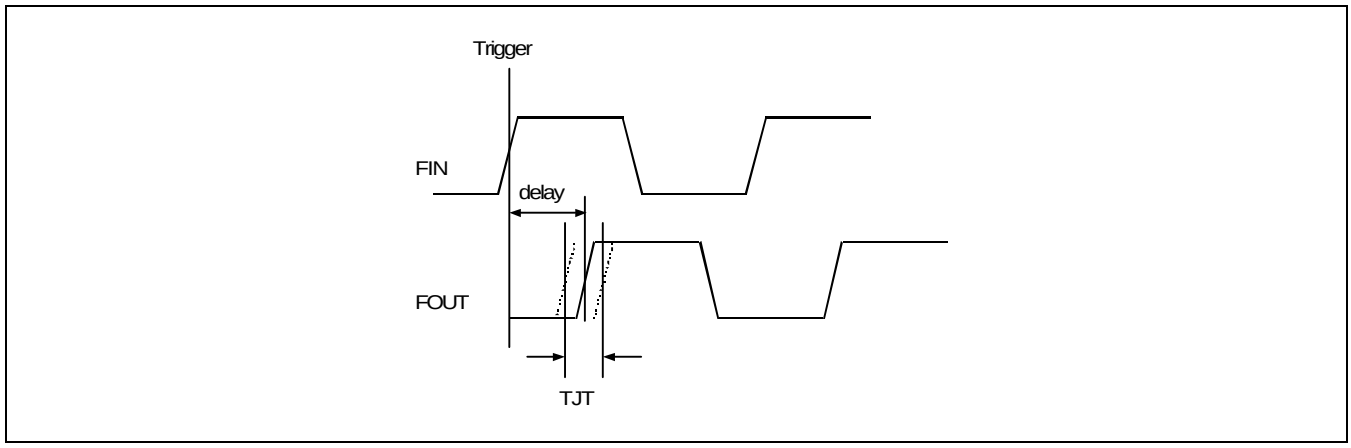
Tracking Jitter

Tracking jitter is the maximum deviation of output clock(FOUT)'s transition from input clock (FIN) position



Appendix A

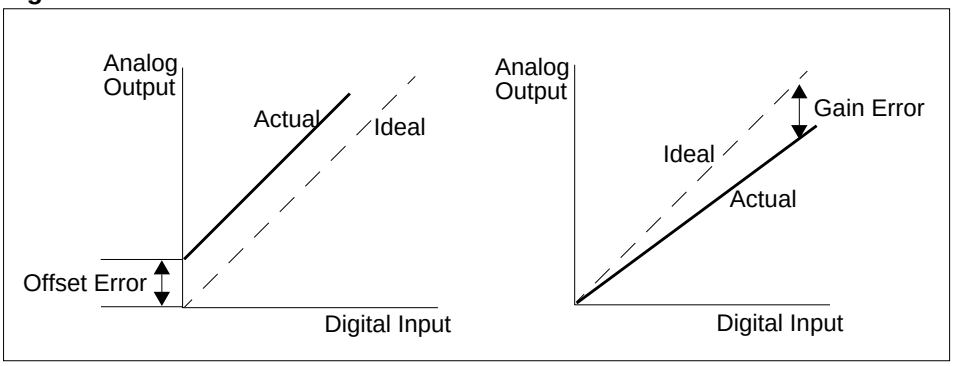
glossary of analog terms

Digital-to-Analog Converter

1. Resolution - An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have resolution of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span.

2. Accuracy - Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Source of error include gain error, offset error, linearity errors and noise. Error is usually commensurate with resolution, less than $2^{-(n+1)}$, or 1/2 LSB of full scale.

Figure 1-1. Error of D/A Converter



3. LSB (Least-Significant Bit) - In a system in which a numerical magnitude is represented by a series of binary digits, the LSB is that bit that carries the smallest value or weight. It represents the smallest analog change that can be resolved by an n-bit converter.

$$\text{LSB (Analog Value)} = FSR/2^n$$

FSR = Full-Scale Range, n = number of bits

4. MSB (Most-Significant Bit) - The binary digit with the largest numerical weighting. Normally, the MSB of a digital word has a weighting of 1/2 the full range.

5. Compliance-Voltage Range - For a current output DAC, the maximum range of(output) terminal voltage for which the device will provide the specified current-output characteristics.

6. Glitch - A glitch is a switching transient appearing in the output during a code transition. Its value is expressed as a product of voltage (V*ns) or current (mA*ns) and time duration or charge transferred.

7. Harmonic Distortion (and Total Harmonic Distortion) - The DAC is driven by the digitized representation of sine wave. The ratio of the RMS sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second through fifth.

$$THD = 20\log\frac{(V2^2+V3^2+V4^2+V5^2)^{1/2}}{V1}$$

V1: RMS amplitude of the fundamental

8. Signal-to-Noise Ratio (SNR) - This signal to noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half

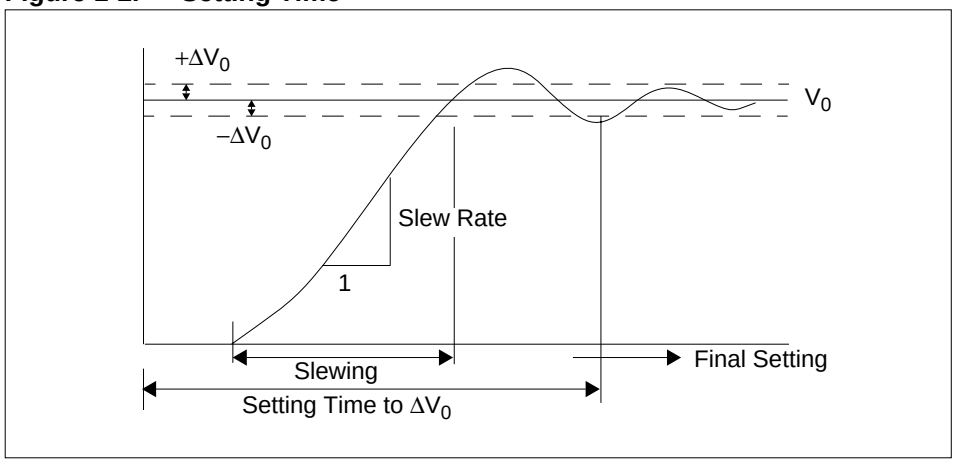
the sampling frequency, this signal to noise ratio must be specified and should ideally follows the theoretical formula;

$$S/N_{max} = 6.02N + 1.76dB$$

9. Slew Rate - Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration such as limited current to charge of capacitor. Amplifiers with slew rate of a few V/μs are common and moderate in cost. Slew rates greater than about 75 V/μs are usually seen only in more sophisticated (and expensive) devices The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

10. Settling Time - The time required, following a prescribed data change from the 50% point of the login input change, for the output of a DAC to reach and to remain within a given fraction (usually ±1/2lsb) of the final value. Typical prescribed changes are full scale, 1MSB and 1LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

Figure 1-2. Setting Time



11. Power-Supply Sensitivity -The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (of fractions of 1LSB) for a 1% dc change in the power supply. Power supply sensitivity may also expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed 1/2LSB for 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

12. ILE (integral Linearity Error) - Linearity error of a converter, expressed in %, ppm of full-scale range or multiples of 1LSB, is a deviation of the analog values in a plot of the measured conversion relationship from a straight line. The straight line can be either a "best straight line" determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviation of the actual transfer characteristics from this straight line; or it can be a straight line passing through the endpoints of the transfer characteristic endpoints of the transfer characteristic after they have been calibrated (sometimes referred to as "endpoint" linearity). Endpoint linearity error is similar to relative accuracy error. For multiplying D/A converters, the analog linearity error, at a specified digital code, is defined in the same way as for multipliers, by deviation from a "best straight line" through the plot of the analog output-input response.

13. DLE (Differential Linearity Error) - Any two adjacent digital codes should result in measured output values that are exactly 1LSB apart (2-n of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called differential linearity error expressed in multiplies of 1LSB. It is an important specification because a differential linearity error greater than 1LSB can lead to non-monotonic response in a D/A converter and missed codes in an A/D converter.

14. Monotonic - A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a differential nonlinearity specification since differential nonlinearity less than 1LSB is a sufficient condition for monotonic behaviour.

2. Analog-to-Digital Converter

1. ILE (Integral Linearity Error: INL) - Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB before the first code transition. "Full scale" is defined as a level 1 1/2LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

2. DLE (Differential Linearity Error: DNL) - An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes are guaranteed.

3. Offset Error - The first transition should occur at a level 1/2LSB above "zero". Offset is defined as the deviation of the actual first code transition from that point.

4. Gain Error - The first code transition should occur for an analog value 1/2LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

5. Pipeline Delay (Latency) - The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

6. Effective Number of Bits (ENOB) - This is a measure of a device's dynamic performance and may be obtained from the SNDR or from a sine wave curve test fit according to the following expression:

ENOB = SNDR - 1.76/6.02

ENOB = N-log2[RMS error (actual) / RMS error (ideal)]

7. Analog Bandwidth - The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

8. Aperture Delay - The delay between the sampling clock and the instant the analog input signal is sampled.

9. Aperture Jitter - The sample to sample variation in aperture delay.

10. Bit Error Rate (BER) - The number of spurious code errors produced for any given input sine wave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sine wave.

11. Signal to Noise Ratio - This signal to noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half the sampling frequency, this signal to noise ratio must be specified and should ideally follow the theoretical formula;

$$S/N_{max} = 6.02N + 1.76dB$$

3. Phase Locked Loop

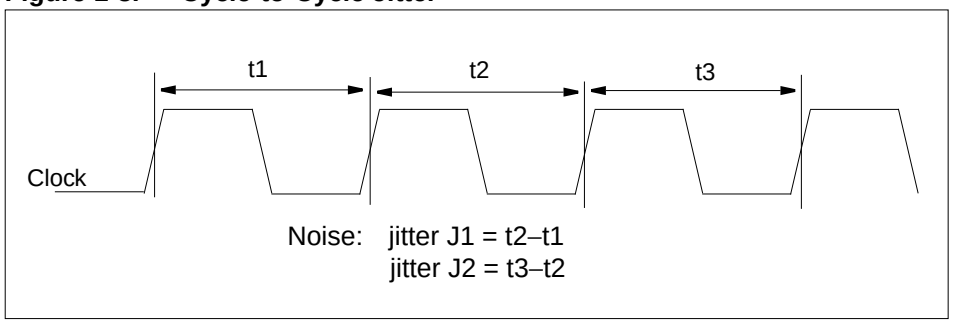
1. Lock Time - The time it takes the PLL to lock onto the system clock. Fast or slow lock time may be controlled by the loop filter characteristics. The loop filter characteristics are controlled by varying the R and C components. (Remember that R and C define the damping-factor as well)

2. Phase Error - The phase difference between the feedback clock signal and the system signal clock.

3. Clock Jitter - The deviations in a clock's output transitions from their ideal positions define the clock jitter. Jitter is sometimes specified as an absolute value in nanoseconds. All jitter measurement are made at a specified voltage.

1) Cycle-to-Cycle Jitter: The change in a clock's output transition from its corresponding position in the previous cycle. This kind of jitter is the most difficult to measure and usually requires a time-interval analyzer

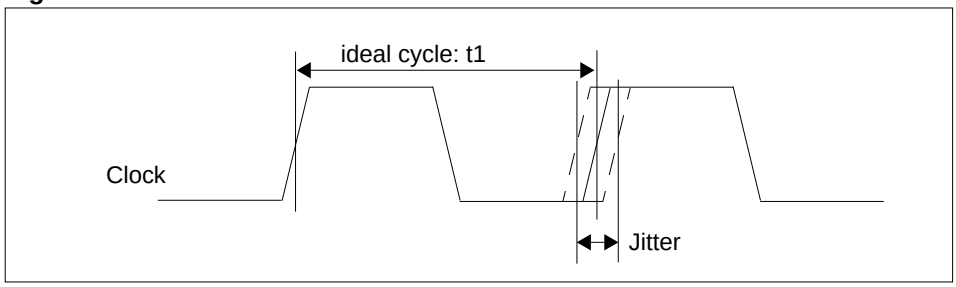
Figure 1-3. Cycle-to-Cycle Jitter



: The maximum of such values over multiple cycles (J1,J2...) is the max. cycle-to-cycle jitter.

2) Period Jitter: Period jitter measures the maximum change in a clock's output transition from its ideal position. You can use period-jitter measurements to calculate timing margins in systems.

Figure 1-4. Period Jitter



3) Long-term Jitter: Long-term jitter measures the maximum change in a clock's output transition from its ideal position over many cycles. How many cycles depends on the application and the frequency. A classic example of system affected by long-term jitter is a graphics card driving a CRT

4) Power Down Mode: PLL state in which the quiescent current is lowered to a very low level to conserve power.

5) Synthesize clock: a system clock may run at a relatively low rate compared to system components. A CPU, for example, may require an internal clock that is several times faster than the system I/O bus clock. Designers can use PLL

Appendix B

equivalent standard loads for 4-layer, 5-layer and 6-layer metal interconnect

Equivalent Standard loads for 4-layer, 5-layer and 6-layer Metal Interconnect

Gates Count	Fanouts										
	1	2	3	4	5	6	7	8	16	32	64
4LM											
5000	0.795	1.635	2.297	3.204	3.840	4.702	5.263	7.047	10.096	17.588	34.192
10000	0.893	2.015	2.840	4.104	4.907	5.976	6.893	8.326	11.992	20.442	40.696
50000	1.224	2.517	3.533	5.909	7.234	8.277	10.830	11.748	14.370	22.346	43.582
100000	1.374	2.799	4.370	6.312	7.549	9.194	12.147	12.744	16.594	24.009	48.909
150000	4.104	6.291	8.021	10.181	11.003	12.494	13.385	14.358	18.222	26.590	51.212
200000	7.429	8.427	9.480	10.929	12.000	13.362	14.297	15.116	19.155	28.159	53.340
300000	8.171	8.952	10.427	12.165	13.326	14.814	15.836	16.726	21.169	31.078	56.183
400000	8.915	10.269	11.297	13.127	14.413	16.045	17.169	18.102	22.883	33.533	59.104
500000	9.944	12.015	12.690	14.722	16.147	17.962	19.210	20.299	24.356	35.700	63.417
600000	10.647	12.681	13.663	15.828	17.344	19.285	20.616	21.822	25.055	36.732	67.431
800000	12.267	15.511	15.875	18.354	20.086	22.314	23.840	25.305	27.076	39.708	75.316
1000000	13.781	16.214	17.944	20.712	22.649	25.145	26.854	28.559	28.954	42.474	78.842
1500000	17.931	21.675	23.578	27.149	29.643	32.879	35.088	37.435	41.425	50.795	95.393
2000000	21.816	26.935	28.858	33.181	36.200	40.127	42.803	45.751	53.533	58.578	106.937
2500000	25.456	32.411	33.799	38.826	42.344	46.911	50.027	53.535	58.472	65.850	123.366
3000000	28.856	35.562	38.419	44.106	48.068	53.251	56.775	60.812	63.080	72.631	138.822
4000000	33.106	39.990	44.076	50.600	55.145	61.094	65.137	69.767	75.133	83.328	158.169
5000000	37.122	48.001	49.423	56.736	61.836	68.503	73.039	76.259	77.242	93.437	166.500
6000000	41.625	52.812	55.417	63.620	69.338	76.812	81.899	87.718	91.773	104.769	196.954
5LM											
5000	0.755	1.553	2.183	3.045	3.647	4.468	5.000	6.694	9.592	16.708	32.482
10000	0.848	1.915	2.698	3.899	4.661	5.677	6.549	7.909	11.391	19.421	38.661
50000	1.163	2.391	3.356	5.614	6.872	7.864	10.289	11.161	13.651	21.228	41.403
100000	1.305	2.659	4.151	5.998	7.171	8.734	11.539	12.106	15.763	22.809	46.464
150000	3.899	5.976	7.620	9.671	10.452	11.870	12.716	13.639	17.311	25.261	48.651
200000	7.057	8.005	9.005	10.381	11.399	12.694	13.582	14.360	18.196	26.751	50.673
300000	7.761	8.505	9.905	11.557	12.659	14.074	15.045	15.889	20.110	29.525	53.374
400000	8.470	9.755	10.732	12.472	13.692	15.242	16.311	17.196	21.740	31.856	56.149
500000	9.446	11.415	12.057	13.986	15.340	17.064	18.250	19.283	23.137	33.915	60.246
600000	10.116	12.047	12.980	15.037	16.476	18.320	19.584	20.732	23.803	34.895	64.059
800000	11.653	14.736	15.082	17.437	19.082	21.198	22.647	24.039	25.722	37.722	71.551
1000000	13.092	15.403	17.047	19.677	21.517	23.887	25.511	27.131	27.507	40.350	74.899
1500000	17.035	20.590	22.399	25.791	28.161	31.236	33.334	35.562	39.354	48.255	90.624
2000000	20.726	25.588	27.415	31.521	34.389	38.122	40.663	43.464	50.856	55.649	101.590
2500000	24.183	30.791	32.108	36.885	40.218	44.564	47.525	50.858	55.549	62.557	117.198
3000000	27.413	33.785	36.498	41.901	45.665	50.588	53.937	57.771	59.927	69.000	131.881
4000000	31.450	37.990	41.872	48.070	52.387	58.039	61.879	66.279	71.377	79.161	150.259
5000000	35.265	45.602	46.952	53.899	58.744	65.078	69.387	74.316	73.379	88.765	158.175
6000000	39.545	50.173	52.645	60.438	65.872	72.972	77.805	83.332	87.185	99.531	187.106
7000000	43.045	60.980	65.492	72.098	76.480	81.466	86.862	96.755	101.602	123.818	246.722
8000000	48.265	68.374	73.437	80.842	85.755	91.350	97.397	108.492	113.482	138.836	251.716

Equivalent Standard loads for 4-layer, 5-layer and 6-layer Metal Interconnect

Gates Count	Fanouts										
	1	2	3	4	5	6	7	8	16	32	64
6LM											
5000	0.716	1.472	2.066	2.883	3.456	4.232	4.738	6.342	9.086	15.830	30.773
10000	0.805	1.814	2.557	3.694	4.417	5.377	6.204	7.494	10.793	18.399	36.627
50000	1.102	2.265	3.181	5.318	6.511	7.448	9.748	10.572	12.933	20.112	39.224
100000	1.236	2.519	3.933	5.681	6.795	8.275	10.933	11.470	14.935	21.608	44.017
150000	3.694	5.661	7.218	9.163	9.903	11.244	12.047	12.923	16.399	23.931	46.090
200000	6.687	7.584	8.531	9.836	10.799	12.025	12.868	13.604	17.240	25.344	48.005
300000	7.354	8.057	9.383	10.948	11.994	13.332	14.251	15.053	19.053	27.970	50.564
400000	8.023	9.242	10.167	11.814	12.972	14.440	15.452	16.291	20.596	30.181	53.194
500000	8.950	10.814	11.421	13.250	14.533	16.167	17.289	18.269	21.921	32.129	57.074
600000	9.582	11.413	12.297	14.246	15.610	17.356	18.555	19.639	22.549	33.059	60.688
800000	11.041	13.960	14.287	16.519	18.078	20.082	21.456	22.775	24.370	35.738	67.785
1000000	12.403	14.592	16.149	18.641	20.383	22.631	24.169	25.702	26.059	38.226	70.958
1500000	16.137	19.507	21.220	24.435	26.679	29.592	31.578	33.690	37.283	45.716	85.854
2000000	19.635	24.242	25.972	29.862	32.580	36.116	38.523	41.177	48.181	52.720	96.244
2500000	22.911	29.169	30.419	34.944	38.100	42.220	45.025	48.181	52.625	59.265	111.029
3000000	25.970	32.005	34.576	39.694	43.261	47.927	51.098	54.732	56.773	65.368	124.940
4000000	29.795	35.990	39.669	45.539	49.631	54.984	58.624	62.791	67.620	74.996	142.352
5000000	33.409	43.202	44.480	51.062	55.653	61.653	65.736	68.437	69.517	84.092	149.850
6000000	37.462	47.531	49.875	57.257	62.405	69.131	73.708	78.946	82.596	94.293	177.259
7000000	40.779	57.769	62.045	68.303	72.454	77.179	82.289	91.663	96.253	117.301	233.736
8000000	45.724	64.775	69.570	76.586	81.242	86.541	92.271	102.781	107.509	131.529	238.466

Appendix C

Maximum Fanout

Maximum Fanouts of Internal Macrocells

(When input t_R/t_F = 0.186ns, one fanout (SL) = 0.00803pF)

Cell Name	Output Pin	Maximum Fanouts
ad2_lp	Y	44
ad2b_lp	Y	44
ad2bd2_lp	Y	88
ad2bd4_lp	Y	178
ad2bd8_lp	Y	356
ad2d2_lp	Y	88
ad2d4_lp	Y	179
ad2d8_lp	Y	351
ad3_lp	Y	44
ad3d2_lp	Y	89
ad3d4_lp	Y	176
ad4_lp	Y	44
ad4d2_lp	Y	88
ad4d4_lp	Y	173
ad5_lp	Y	20
ad5d2_lp	Y	41
ad5d4_lp	Y	179
ao21_lp	Y	19
ao211_lp	Y	12
ao2111_lp	Y	8
ao2111d2_lp	Y	89
ao211d2_lp	Y	24
ao211d4_lp	Y	179
ao21d2_lp	Y	39
ao21d4_lp	Y	177
ao22_lp	Y	19
ao221_lp	Y	11
ao221d2_lp	Y	89
ao221d4_lp	Y	178
ao222_lp	Y	11
ao2222_lp	Y	6
ao2222d2_lp	Y	88
ao2222d4_lp	Y	178
ao222a_lp	Y	16
ao222d2_lp	Y	88
ao222d4_lp	Y	178
ao22a_lp	Y	19
ao22d2_lp	Y	38
ao22d4_lp	Y	179
ao31_lp	Y	18
ao311_lp	Y	10
ao3111_lp	Y	6
ao31d2_lp	Y	37
ao31d4_lp	Y	177
ao32_lp	Y	18
ao321_lp	Y	10
ao322_lp	Y	9
ao32d2_lp	Y	88
ao33_lp	Y	18
ao331_lp	Y	10
ao332_lp	Y	9
busholder_lp	Y	10000
cgln_lp	GCK	43
cglnd2_lp	GCK	87
cglnd4_lp	GCK	176
cglp_lp	GCK	43
cglpd2_lp	GCK	88
cglpd4_lp	GCK	178
dl1d2_lp	Y	89
dl2d2_lp	Y	89
dl5d2_lp	Y	88
dl10d2_lp	Y	89
fa_lp	S	44
	CO	44
fad2_lp	S	89
	CO	88
fd1_lp	Q	43
	QN	43
fd1d2_lp	Q	88
	QN	88
fd1q_lp	Q	43
fd1qd2_lp	Q	88
fd1s_lp	Q	43
	QN	43
fd1sd2_lp	Q	88
	QN	88
fd1sq_lp	Q	43
fd1sqd2_lp	Q	88
fd2_lp	Q	43
	QN	43
fd2d2_lp	Q	89
	QN	88
fd2q_lp	Q	43
fd2qd2_lp	Q	90
fd2s_lp	Q	43
	QN	43
fd2sd2_lp	Q	89
	QN	88
fd2sq_lp	Q	43
fd2sqd2_lp	Q	89
fd3_lp	Q	43
	QN	43
fd3d2_lp	Q	87
	QN	88
fd3q_lp	Q	43
fd3qd2_lp	Q	88
fd3s_lp	Q	43
	QN	43
fd3sd2_lp	Q	88
	QN	88
fd3sq_lp	Q	43
fd3sqd2_lp	Q	88
fd4_lp	Q	44
	QN	43
fd4d2_lp	Q	89
	QN	87
fd4q_lp	Q	44
fd4qd2_lp	Q	89
fd4s_lp	Q	44
	QN	43
fd4sd2_lp	Q	89
	QN	87
fd4sq_lp	Q	43
fd4sqd2_lp	Q	88
fd5_lp	Q	43
	QN	43
fd5d2_lp	Q	88
	QN	88
fd5s_lp	Q	44
	QN	44
fd5sd2_lp	Q	88
	QN	88
fd6_lp	Q	43
	QN	43
fd6d2_lp	Q	89
	QN	88

Cell Name	Output Pin	Maximum Fanouts
fd6s_lp	Q	43
	QN	43
fd6sd2_lp	Q	88
	QN	87
fd7_lp	Q	43
	QN	43
fd7d2_lp	Q	88
	QN	89
fd7s_lp	Q	43
	QN	43
fd7sd2_lp	Q	88
	QN	88
fd8_lp	Q	44
	QN	43
fd8d2_lp	Q	89
	QN	87
fd8s_lp	Q	44
	QN	43
fd8sd2_lp	Q	89
	QN	87
fds2_lp	Q	43
	QN	43
fds2d2_lp	Q	88
	QN	87
fds2s_lp	Q	44
	QN	44
fds2sd2_lp	Q	89
	QN	89
fds3_lp	Q	43
	QN	43
fds3d2_lp	Q	88
	QN	88
fds3s_lp	Q	43
	QN	43
fds3sd2_lp	Q	88
	QN	87
fj2_lp	Q	44
	QN	43
fj2d2_lp	Q	89
	QN	88
fj2s_lp	Q	43
	QN	43
fj2sd2_lp	Q	88
	QN	87
fj4_lp	Q	43
	QN	44
fj4d2_lp	Q	86
	QN	88
fj4s_lp	Q	44
	QN	43
fj4sd2_lp	Q	89
	QN	87
ft2_lp	Q	44
	QN	43
ft2d2_lp	Q	88
	QN	88
ha_lp	S	44
	CO	44
had2_lp	S	88
	CO	88
iv_lp	Y	44
ivd2_lp	Y	91
ivd3_lp	Y	137
ivd4_lp	Y	184
ivd6_lp	Y	276

Cell Name	Output Pin	Maximum Fanouts
ivd8_lp	Y	362
ivd16_lp	Y	722
ivd24_lp	Y	1081
ivt_lp	Y	43
ivtd2_lp	Y	88
ivtd4_lp	Y	178
ivtd8_lp	Y	356
ivtd16_lp	Y	704
ld1_lp	Q	44
	QN	43
ld1d2_lp	Q	88
	QN	88
ld1q_lp	Q	44
ld1qd2_lp	Q	89
ld2_lp	Q	44
	QN	44
ld2d2_lp	Q	87
	QN	88
ld2q_lp	Q	44
ld2qd2_lp	Q	89
ld3_lp	Q	43
	QN	44
ld3d2_lp	Q	87
	QN	89
ld4_lp	Q	43
	QN	44
ld4d2_lp	Q	88
	QN	89
ld5_lp	Q	44
	QN	44
ld5d2_lp	Q	89
	QN	88
ld5q_lp	Q	44
ld5qd2_lp	Q	89
ld6_lp	Q	44
	QN	43
ld6d2_lp	Q	88
	QN	88
ld6q_lp	Q	43
ld6qd2_lp	Q	88
mx2_lp	Y	44
mx2d2_lp	Y	88
mx2d4_lp	Y	178
mx2i_lp	YN	19
mx2ia_lp	YN	19
mx2id2_lp	YN	39
mx2id2a_lp	YN	39
mx2id4_lp	YN	180
mx2id4a_lp	YN	178
mx4_lp	Y	44
mx4d2_lp	Y	89
mx4d4_lp	Y	175
nd2_lp	Y	43
nd2b_lp	Y	42
nd2bd2_lp	Y	86
nd2bd4_lp	Y	173
nd2bd8_lp	Y	351
nd2d2_lp	Y	88
nd2d4_lp	Y	177
nd2d8_lp	Y	355
nd3_lp	Y	29
nd3b_lp	Y	30
nd3bd2_lp	Y	60
nd3bd4_lp	Y	178
nd3bd8_lp	Y	351

Cell Name	Output Pin	Maximum Fanouts
nd3d2_lp	Y	61
nd3d4_lp	Y	179
nd3d8_lp	Y	351
nd4_lp	Y	22
nd4d2_lp	Y	45
nd4d4_lp	Y	177
nd5_lp	Y	43
nd5d2_lp	Y	88
nd5d4_lp	Y	179
nd6_lp	Y	43
nd6d2_lp	Y	88
nd6d4_lp	Y	178
nd8_lp	Y	43
nd8d2_lp	Y	88
nd8d4_lp	Y	178
nid_lp	Y	43
nid16_lp	Y	703
nid2_lp	Y	88
nid3_lp	Y	133
nid4_lp	Y	179
nid6_lp	Y	267
nid8_lp	Y	352
nid24_lp	Y	1051
nit_lp	Y	43
nitd16_lp	Y	701
nitd2_lp	Y	88
nitd4_lp	Y	177
nitd8_lp	Y	356
nr2_lp	Y	20
nr2a_lp	Y	43
nr2b_lp	Y	20
nr2bd2_lp	Y	41
nr2bd4_lp	Y	178
nr2bd8_lp	Y	358
nr2d2_lp	Y	42
nr2d4_lp	Y	177
nr2d8_lp	Y	358
nr3_lp	Y	13
nr3a_lp	Y	26
nr3d2_lp	Y	26
nr3d4_lp	Y	177
nr4_lp	Y	43
nr4d2_lp	Y	88
nr4d4_lp	Y	178
nr5_lp	Y	43
nr5d2_lp	Y	88
nr5d4_lp	Y	178
nr6_lp	Y	43
nr6d2_lp	Y	88
nr6d4_lp	Y	178
nr8_lp	Y	44
nr8d2_lp	Y	89
nr8d4_lp	Y	177
oa21_lp	Y	20
oa211_lp	Y	20
oa2111_lp	Y	19
oa2111d2_lp	Y	40
oa211d2_lp	Y	40
oa211d4_lp	Y	179
oa21d2_lp	Y	40
oa21d4_lp	Y	179
oa22_lp	Y	18
oa221_lp	Y	18
oa221d2_lp	Y	37
oa221d4_lp	Y	179

Cell Name	Output Pin	Maximum Fanouts
oa222_lp	Y	17
oa2222_lp	Y	13
oa2222d2_lp	Y	88
oa2222d4_lp	Y	179
oa222d2_lp	Y	35
oa222d4_lp	Y	180
oa22a_lp	Y	20
oa22d2_lp	Y	38
oa22d2a_lp	Y	40
oa22d4_lp	Y	179
oa22d4a_lp	Y	179
oa31_lp	Y	12
oa311_lp	Y	12
oa3111_lp	Y	11
oa31d2_lp	Y	25
oa31d4_lp	Y	177
oa32_lp	Y	11
oa321_lp	Y	10
oa322_lp	Y	8
oa33_lp	Y	9
or2_lp	Y	43
or2b_lp	Y	43
or2bd2_lp	Y	88
or2bd4_lp	Y	177
or2bd8_lp	Y	356
or2d2_lp	Y	88
or2d4_lp	Y	178
or2d8_lp	Y	351
or3_lp	Y	44
or3d2_lp	Y	89
or3d4_lp	Y	179
or4_lp	Y	43
or4d2_lp	Y	85
or4d4_lp	Y	176
or5_lp	Y	43
or5d2_lp	Y	83
or5d4_lp	Y	177
scg1_lp	Y	30
scg1d2_lp	Y	60
scg2_lp	Y	43
scg2d2_lp	Y	89
scg2d4_lp	Y	178
scg3_lp	Y	30
scg3d2_lp	Y	60
scg3d4_lp	Y	176
scg4_lp	Y	43
scg4d2_lp	Y	86
scg4d4_lp	Y	169
scg5_lp	Y	43
scg5d2_lp	Y	88
scg5d4_lp	Y	172
scg6_lp	Y	43
scg6d2_lp	Y	88
scg7_lp	Y	43
scg7d2_lp	Y	86
scg8_lp	Y	43
scg8d2_lp	Y	89
scg9_lp	Y	43
scg9d2_lp	Y	89
scg10_lp	Y	43
scg10d2_lp	Y	89
scg11_lp	Y	12
scg11d2_lp	Y	25
scg12_lp	Y	20
scg12d2_lp	Y	41

Cell Name	Output Pin	Maximum Fanouts
scg12d4_lp	Y	178
scg13_lp	Y	43
scg13d2_lp	Y	88
scg14_lp	Y	43
scg14d2_lp	Y	85
scg15_lp	Y	29
scg15d2_lp	Y	60
scg16_lp	Y	19
scg16d2_lp	Y	40
scg17_lp	Y	31
scg17d2_lp	Y	85
scg18_lp	Y	30
scg18d2_lp	Y	60
scg19_lp	Y	19
scg19d2_lp	Y	39
scg20_lp	Y	20
scg20d2_lp	Y	41
scg21_lp	Y	13
scg21d2_lp	Y	26
scg22_lp	Y	19
scg22d2_lp	Y	40
xn2_lp	Y	44
xn2d2_lp	Y	88
xn2d4_lp	Y	178
xn3_lp	Y	44
xn3d2_lp	Y	88
xn3d4_lp	Y	174
xo2_lp	Y	44
xo2d2_lp	Y	89
xo2d4_lp	Y	177
xo3_lp	Y	43
xo3d2_lp	Y	87
xo3d4_lp	Y	171

Maximum Fanouts of I/O Cells

(When input t_R/t_F = 0.186ns, one fanout (SL) = 0.00803pF)

Cell Name	Output Pin	Maximum Fanouts
phic_lp	Y	106
phic_abb_lp	Y	142
phicc_abb_lp	Y	144
phicd_lp	Y	107
phicd_abb_lp	Y	142
phicen_abb_lp	Y	140
phicu_lp	Y	107
phicu_abb_lp	Y	142
phis_lp	Y	107
phis_abb_lp	Y	139
phisd_lp	Y	107
phisd_abb_lp	Y	139
phisu_lp	Y	107
phisu_abb_lp	Y	139
phsckdc2_lp	Y	354
phsckdc4_lp	Y	688
phsckdc6_lp	Y	989
phsckdc8_lp	Y	1248
phsckdcd2_lp	Y	354
phsckdcd4_lp	Y	688
phsckdcd6_lp	Y	989
phsckdcd8_lp	Y	1248
phsckdcu2_lp	Y	354
phsckdcu4_lp	Y	688
phsckdcu6_lp	Y	989
phsckdcu8_lp	Y	1248
phsckds2_lp	Y	354
phsckds4_lp	Y	688
phsckds6_lp	Y	989
phsckds8_lp	Y	1248
phsckdsd2_lp	Y	354
phsckdsd4_lp	Y	688
phsckdsd6_lp	Y	989
phsckdsd8_lp	Y	1248
phsckdsu2_lp	Y	354
phsckdsu4_lp	Y	688
phsckdsu6_lp	Y	989
phsckdsu8_lp	Y	1248
phtic_lp	Y	107
phticd_lp	Y	107
phticu_lp	Y	107
phtis_lp	Y	107
phtisd_lp	Y	107
phtisu_lp	Y	107
phsosck1_lp	YN	86
phsosck17_lp	YN	86
phsosck2_lp	YN	26
phsosck27_lp	YN	26
phsoscm1_lp	YN	33
phsoscm16_lp	YN	33
phsoscm2_lp	YN	275
phsoscm26_lp	YN	276
phsoscm3_lp	YN	331
phsoscm36_lp	YN	336
pic_lp	Y	162
pic_abb_lp	Y	162
picc_abb_lp	Y	164
picd_lp	Y	162
picd_abb_lp	Y	162
picen_abb_lp	Y	156
picu_lp	Y	162
picu_abb_lp	Y	162
pis_lp	Y	159
pis_abb_lp	Y	159
pisd_lp	Y	159
pisd_abb_lp	Y	159
pisu_lp	Y	159
pisu_abb_lp	Y	159
pmic_lp	Y	68
pmic_abb_lp	Y	109
pmicc_abb_lp	Y	110
pmicd_lp	Y	68
pmicd_abb_lp	Y	109
pmicen_abb_lp	Y	106
pmicu_lp	Y	67
pmicu_abb_lp	Y	109
pmis_lp	Y	68
pmis_abb_lp	Y	108
pmisd_lp	Y	67
pmisd_abb_lp	Y	108
pmisu_lp	Y	68
pmisu_abb_lp	Y	108
pmsckdc2_lp	Y	354
pmsckdc4_lp	Y	689
pmsckdc6_lp	Y	991
pmsckdc8_lp	Y	1251
pmsckdcd2_lp	Y	354
pmsckdcd4_lp	Y	689
pmsckdcd6_lp	Y	991
pmsckdcd8_lp	Y	1251
pmsckdcu2_lp	Y	354
pmsckdcu4_lp	Y	689
pmsckdcu6_lp	Y	991
pmsckdcu8_lp	Y	1251
pmsckds2_lp	Y	354
pmsckds4_lp	Y	689
pmsckds6_lp	Y	991
pmsckds8_lp	Y	1251
pmsckdsd2_lp	Y	354
pmsckdsd4_lp	Y	689
pmsckdsd6_lp	Y	991
pmsckdsd8_lp	Y	1251
pmsckdsu2_lp	Y	354
pmsckdsu4_lp	Y	689
pmsckdsu6_lp	Y	991
pmsckdsu8_lp	Y	1251
pmsosck1_lp	YN	87
pmsosck2_lp	YN	26
pmsoscm1_lp	YN	32
pmsoscm2_lp	YN	132
psckdc2_lp	Y	390
psckdc4_lp	Y	759
psckdc6_lp	Y	1096
psckdc8_lp	Y	1392
psckdcd2_lp	Y	390
psckdcd4_lp	Y	759
psckdcd6_lp	Y	1095
psckdcd8_lp	Y	1389
psckdcu2_lp	Y	390
psckdcu4_lp	Y	758
psckdcu6_lp	Y	1095
psckdcu8_lp	Y	1391
psckds2_lp	Y	387
psckds4_lp	Y	736
psckds6_lp	Y	1030
psckds8_lp	Y	1264
psckdsd2_lp	Y	386
psckdsd4_lp	Y	735
psckdsd6_lp	Y	1027
psckdsd8_lp	Y	1258
psckdsu2_lp	Y	387
psckdsu4_lp	Y	736

Cell Name	Output Pin	Maximum Fanouts
psckdsu6_lp	Y	1029
psckdsu8_lp	Y	1261
psosck1_lp	YN	146
psosck2_lp	YN	148
psoscm1_lp	YN	148
psoscm2_lp	YN	148
ptic_lp	Y	160
pticd_lp	Y	160
pticu_lp	Y	160
ptis_lp	Y	156
ptisd_lp	Y	133
ptisu_lp	Y	156

Maximum Fanouts for CK and NID Cells

<Condition>

- Library = STDL131
- V_{DD} = 1.8V
- Fanout = 0.00914pF (= input cap for CK pin of FD1_LP)
- Standard Load (SL) = 0.00803pF
- Input slope = 0.186ns
- Maximum output transition time (mott) = 1.2ns
- Maximum frequency ≤ 300MHz
- Net length (μm/fanout): branch net length for each fanout except trunk

Trunk width (μm)	8				In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	2000	5000	2000	5000	
ck2_lp	154	97	52	32	403
ck4_lp	333	258	111	86	806
ck6_lp	505	400	169	134	1210
ck8_lp	668	523	224	175	1612

Trunk width (μm)	0.28		8		In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	2000	5000	2000	5000	
nid_lp	7	-	-	-	43
nid2_lp	25	-	3	-	88
nid3_lp	39	4	11	-	133
nid4_lp	51	9	19	-	179
nid6_lp	70	15	35	15	267
nid8_lp	82	18	50	29	352
nid16_lp	108	23	110	83	703
nid24_lp	119	25	167	132	1051

For high fanout nets including clock net, Samsung strongly recommends using clock tree synthesis.

Appendix D

Package Capabilities

Package

The most current package availability and capability can be obtained from your local Samsung Technology and Design Centers.

■ In-house ❑ Sub-contractor

LQFP												
Package	**Pitch**	**Lead Inductance**	**Lead Count**									
			32	48	64	80	100	128	144	160	176	208	256
0707 mm	0.8		■										
	0.5	< 3nH		■									
1010 mm	0.5	< 5nH			■								
1212 mm	0.5	< 5nH				■							
1420 mm	0.5	< 12nH						■					
1414 mm	0.8	< 6nH			■								
	0.5	< 6nH					■						
	0.4	v						■					
2020 mm	0.4								■				
2024 mm	0.5									■	■		
2828 mm	0.5	< 17nH										■	
	0.4	< 17nH											■
TQFP													
1212 mm	0.5	< 5nH				■							
1414 mm	0.5	< 5nH					■						
1420 mm	0.065	< 10nH					■						

PQFP (PQ2 Thermally Enhanced)									
Package	**Pitch**	**Lead Count**							
		100	120	128	144	160	208	240	304
1420 mm	0.65	❑							
	0.5			❑					
2828 mm	0.8		❑	❑					
	0.65				❑	❑			
	0.5						❑		
3232 mm	0.5							❑	
4040 mm	0.5								❑
QFP (with Heat Spreader)									
1420 mm	0.65	■							
	0.5								
2828 mm	0.8		❑	■					
	0.65				❑	❑			
	0.5						❑		
3232 mm	0.5							❑	
4040 mm	0.5								❑

■ In-house ❑ Sub-contractor

PLCC									
Package	Pitch	Lead Inductance	Lead Count						
			18	28	32	44	52	68	84
7.37 x 12.35 mm	1.27		■						
11.53 x 11.53 mm				■					
11.44 x 13.98 mm					■				
16.61 x 16.61 mm		< 5nH				■			
19.10 x 19.10 mm							■		
24.23 x 24.23 mm								■	
29.31 x 29.31 mm		< 13nH							■

SOP								
Package	Pitch	Lead Count						
		32	48	64(56)	68	69	100	256
8.34 x 20.30 mm	1.27	■						
TSOP1								
1014 mm	0.4		■					
PLCC								
24.33 x 24.23mm	1.27				■			
QFP								
1420 mm	0.65						■	
FBGA								
0909 mm	0.75			■				
0911 mm	0.8					■		
1717 mm	1.00							■

SBGA									
Package	Pitch	Lead Inductance		Lead Count					
		Lp/g	Lsig	256	304	352	540	648	696
2727 mm	1.27	< 3nH	< 7nH	❑					
3131 mm		< 3nH	< 8nH		❑				
3535 mm		< 3nH	< 8nH			❑			
42.5 x 47.5 mm		< 3nH	<9nH				❑		
4545 mm		< 3nH	<9nH					❑	
47.5 x 47.5 mm									❑

Package Parameter Guide for PBGAs and FBGAs

Lead Inductance							
Package Type	**Stack-Up (layer)**	**PCB Size (mm x mm)**	**L_p/g (nH)**	**L_wire (nH)**	**L_total (nH)**	**T (mm)**	**L_sig (nH)**
PBGA	2L	23 x 23	< 3.5	1.5	< 4.5	5	< 7
	2L	27 x 27	< 4	1.5	< 5.5	6	< 7.5
	2L	31 x 31	< 4.1	1.5	< 5.6	7	< 8.5
	2L	35 x 35	< 4.5	1.5	< 6	8	< 10
	4L	23 x 23	< 1.3	1.5	< 2.8	5	< 3.5
	4L	27 x 27	< 1.5	1.5	< 3	6	< 4
	4L	31 x 31	< 1.6	1.5	< 3.1	7	< 4.5
	4L	35 x 35	< 1.7	1.5	< 3.2	8	< 5.5
FBGA	2L	06 x 06	< 2	1.5	< 3.5	2	< 2.5
	2L	08 x 08	< 2	1.5	< 3.5	2	< 3.5
	2L	09 x 09	< 2	1.5	< 3.5	2	< 4.5
	2L	10 x 10	< 2	1.5	< 3.5	2	< 4.5
	2L	12 x 12	< 2	1.5	< 3.5	2	< 5
	2L	13 x 13	< 2	1.5	< 3.5	2	< 6
	2L	14 x 14	< 2	1.5	< 3.5	2	< 6
	2L	16 x 16	< 2	1.5	< 3.5	2	< 7
	2L	17 x 17	< 2	1.5	< 3.5	2	< 8
	2L	18 x 18	< 2	1.5	< 3.5	2	< 8

NOTES: Condition to use above package parameter guide;

1. Above data are estimated calculations with below assumptions.
2. Center balls are all ground balls for PBGA ball map design.
3. For a ball map design, the power/ground ball pair should be arranged next to each other and located on the center closed inside row and column.
4. Distance between power/ground bonding pad and ball must be less than listed above T[mm] column distance.
5. The bonding wire length between power/ground ball and PCB bonding pad should be less than 2mm.
6. L_total = L_p/g + L_wire; L_p/g: Total inductance of power/ground pad L_sig: Signal line inductance.
7. Contact IPT development P/T for ball map design request form in special case, other than above 1) ~ 6) notes. Special guide will be provided.

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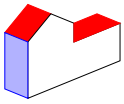

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