



# LC74735NW

## On-Screen Display Controller

### Overview

The LC74735NW is an on-screen display CMOS IC that displays characters and patterns on a TV screen.

For QVGA display, the LC74735NW supports the use of both a  $12 \times 18$  dot character font and a  $12 \times 18$  dot graphics font with 16 colors with a total of 512 characters and glyphs.

For WVGA display, the LC74735NW supports the use of both a  $24 \times 32$  dot character font and a  $12 \times 16$  dot graphics font with 16 colors with a total of 512 characters and glyphs.

The LC74735NW can also implement extremely varied displays by the use of an external ROM.

The LC74735NW supports both QVGA ( $480 \times 234$ ) and WVGA ( $800 \times 480$ ).

### Features

- Screen structure

- Main:

- QVGA mode: 40 characters  $\times$  13 lines (up to 520 characters) on a QVGA panel

- WVGA mode: 33 characters  $\times$  15 lines (up to 495 characters) on a WVGA panel

- Wallpaper display screen: Permanent repetition of a  $2 \times 2$  (horizontal  $\times$  vertical) character pattern

- Character structure

- QVGA mode:

- 12 dots (horizontal)  $\times$  18 dots (vertical): Character display

- 12 dots (horizontal)  $\times$  18 dots (vertical): Graphic glyph display

- WVGA mode:

- 24 dots (horizontal)  $\times$  32 dots (vertical): Character display

12 dots (horizontal)  $\times$  16 dots (vertical): Graphic glyph display (1 pixel:  $2 \times 2$  dots)

- Character display clock:

About 9 MHz — QVGA with an LC oscillator

33.2 MHz (maximum: 40 MHz) WVGA with an external clock signal input

\*: The ROM image is known when QVGA or WVGA mode is specified.

- Number of characters: 512 (internal)

Up to 2048 characters when an external 16-bit 4M ROM is used.

- Character sizes: Four horizontal sizes (1 $\times$ , 2 $\times$ , 3 $\times$ , and 4 $\times$ )

Four vertical sizes (1 $\times$ , 2 $\times$ , 3 $\times$ , and 4 $\times$ )  
(The character size is specified in line units.)

- Display start positions: 512 positions in the horizontal direction and 256 positions in the vertical direction.

	QVGA mode	WVGA mode
Setting units: Horizontal:	1 dot	2 dots (In screen units)
Vertical:	1 dot	2 dots (In screen units)

- Display functions

- Blinking specification (in character units)

Period: 1/64, 1/32, and 1/16 of the vertical sync signal (in screen units)

Duty: Fixed at 50%

- Box (raised or recessed) display

Raised/recessed specification (in character units)

Left: Off/on specification (in character units)

Right: Off/on specification (in character units)

Top: Off/on specification (in character units)

Bottom: Off/on specification (in character units)

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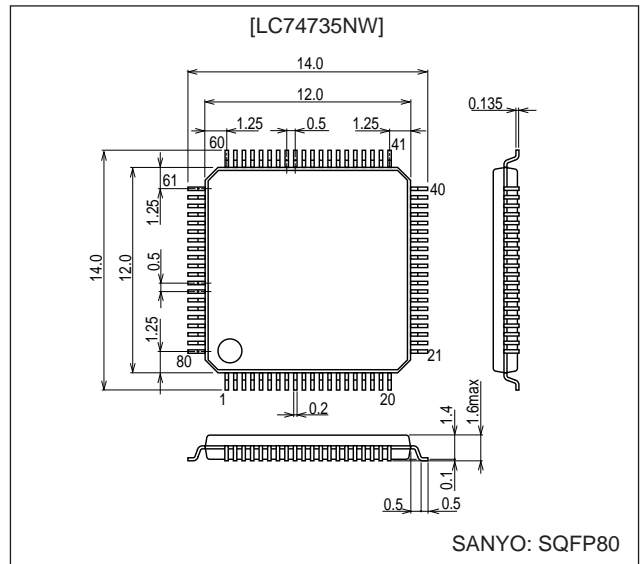
O1003TN (OT) No. 7545-1/52

- Border specification (in line units): Only valid with glyphs from the character font.
- Color specification
  - Character
    - Character color (in character units): 1 of 16 colors can be specified.
    - Character background color (in character units): 1 of 16 colors can be specified.
    - Border color (in line units): 1 of 16 colors can be specified.
- Graphic
  - 16 types can be specified by ROM data
- Box color (line units) : 1/16 colors
- Background color (screen units) : 1/16 colors
- Color table (palette)
  - Sixteen colors can be selected from a set of 512 colors (One of which is specified to be transparent.)
  - Number of color tables: 2. This allows up to 32 colors to be displayed at the same time.
- Wallpaper screen (Graphics glyphs only)
  - Wallpaper display: Repeated display under the main screen (2 characters horizontally by 2 characters vertically).
  - Sprite character display: Displayed above the main screen (2 characters horizontally by 2 characters vertically)
- Output
  - QVGA
    - Analog RGB output
    - BLK (OSD display period signal)
  - WVGA
    - Digital RGB output (3 bits per color)
    - BLK (OSD display period signal)
- Package: SQFP80
- Voltage: 3.3 V

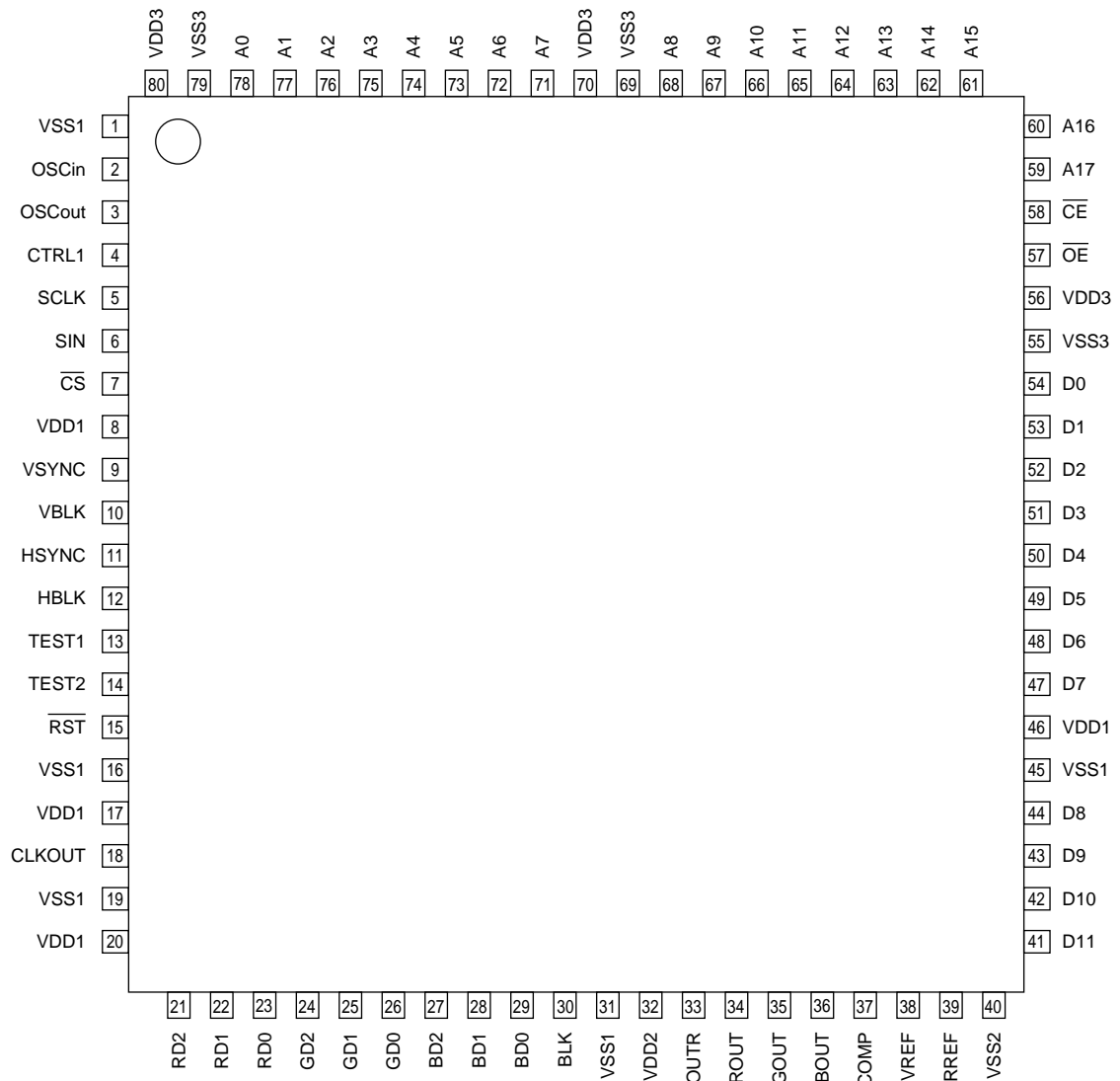
## Package Dimensions

unit: mm

### 3220-SQFP80



# Pin Assignments



Top view

# LC74735NW

## Pin Functions

Pin No.	Symbol	Type	Functional description
1	V <sub>SS1</sub>	Ground	Connect a ground to this pin. (Digital system ground)
2	OSCin	LC oscillator	Connect to the character output dot clock generator oscillator coil and capacitor. May also be used for external clock input.
3	OSCOut		
4	CTRL1	OSCin oscillator input control	Switches between external clock input mode and LC oscillator mode. Low: LC oscillator, high: external clock input MORE+
5	SCLK	Clock input	Clock input for the serial data input system MORE+ (This input has hysteresis characteristics.)
6	SIN	Data input	Serial data input MORE+ (This input has hysteresis characteristics.)
7	$\overline{\text{CS}}$	Enable input	Enable input for the serial data input system. Serial data input is enabled when this pin is set low. MORE+ (This input has hysteresis characteristics.)
8	V <sub>DD1</sub>	Power supply (+3.3 V)	Digital system power supply: +3.3 V
9	VSYNC	Vertical sync signal input	Vertical sync signal input MORE+ (This input has hysteresis characteristics.)
10	VBLK	Vertical blanking signal input	Vertical blanking signal input MORE+ (This input has hysteresis characteristics.)
11	HSYNC	Horizontal sync signal input	Horizontal sync signal input MORE+ (This input has hysteresis characteristics.)
12	HBLK	Horizontal blanking signal input	Horizontal blanking signal input MORE+ (This input has hysteresis characteristics.)
13	TEST1	Test mode control 1	Test mode control 1 Low: normal operation, high: test mode MORE+
14	TEST2	Test mode control 2	Test mode control 2 Low: normal operation, high: test mode (scan mode) MORE+
15	$\overline{\text{RST}}$	Reset input	System reset input MORE+ (This input has hysteresis characteristics.)
16	V <sub>SS1</sub>	Ground	Connect a ground to this pin. (Digital system ground)
17	V <sub>DD1</sub>	Power supply (+3.3 V)	Power supply: (+3.3 V: Digital system)
18	CLKOUT	Clock output	Clock output
19	V <sub>SS1</sub>	Ground	Connect a ground to this pin. (Digital system ground)
20	V <sub>DD1</sub>	Power supply (+3.3 V)	Power supply: (+3.3 V: Digital system)
21	RD2	Rout output: bit 2	Rout output This is a 3-bit digital output with values from 000 to 111.
22	RD1	Rout output: bit 1	
23	RD0	Rout output: bit 0	
24	GD2	Gout output: bit 2	Gout output This is a 3-bit digital output with values from 000 to 111.
25	GD1	Gout output: bit 1	
26	GD0	Gout output: bit 0	
27	BD2	Bout output: bit 2	Bout output This is a 3-bit digital output with values from 000 to 111.
28	BD1	Bout output: bit 1	
29	BD0	Bout output: bit 0	
30	BLK	Blanking signal output	This signal indicates the OSD display period.
31	V <sub>SS1</sub>	Ground	Connect a ground to this pin. (Digital system ground)
32	V <sub>DD2</sub>	Power supply (+3.3 V)	Power supply: (+3.3 V: D/A converter)
33	OUTR	Outr output: analog	Output. Connect a resistor R <sub>o</sub> (68 Ω) to this pin.
34	Rout	Rout output: analog	D/A converter (3 bits) output. Connect a resistor R <sub>o</sub> to this pin.
35	Gout	Gout output: analog	D/A converter (3 bits) output. Connect a resistor R <sub>o</sub> to this pin.
36	Bout	Bout output: analog	D/A converter (3 bits) output. Connect a resistor R <sub>o</sub> to this pin.
37	CCOMP	Phase correction capacitor connection	Capacitor connection: 1.5 μF
38	CVREF	Reference voltage output	Capacitor connection: 0.1 μF
39	RREF	Reference resistor connection	Connect a reference register to this pin.
40	V <sub>SS2</sub>	Ground	Connect a ground to this pin. (D/A converter ground)

Continued on next page.

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Continued from preceding page.

Pin No.	Symbol	Type	Functional description
41	D11	Data input 11	ROM data input 11. MORE+
42	D10	Data input 10	ROM data input 10. MORE+
43	D9	Data input 9	ROM data input 9. MORE+
44	D8	Data input 8	ROM data input 8. MORE+
45	V <sub>SS1</sub>	Ground	Connect a ground to this pin. (Digital system ground)
46	V <sub>DD1</sub>	Power supply (+3.3 V)	Power supply: (+3.3 V: Digital system)
47	D7	Data input 7	ROM data input 7. MORE+
48	D6	Data input 6	ROM data input 6. MORE+
49	D5	Data input 5	ROM data input 5. MORE+
50	D4	Data input 4	ROM data input 4. MORE+
51	D3	Data input 3	ROM data input 3. MORE+
52	D2	Data input 2	ROM data input 2. MORE+
53	D1	Data input 1	ROM data input 1. MORE+
54	D0	Data input 0	ROM data input 0. MORE+
55	V <sub>SS3</sub>	Ground	Connect a ground to this pin. (External ROM output system ground)
56	V <sub>DD3</sub>	Power supply (+3.3 or +5.5 V)	Power supply (External ROM output system power supply)
57	$\overline{OE}$	Output enable	ROM output enable output. This is an active low output.
58	$\overline{CE}$	Chip enable	ROM chip enable output. This is an active low output.
59	A17	Address output 17	ROM address output 17
60	A16	Address output 16	ROM address output 16
61	A15	Address output 15	ROM address output 15
62	A14	Address output 14	ROM address output 14
63	A13	Address output 13	ROM address output 13
64	A12	Address output 12	ROM address output 12
65	A11	Address output 11	ROM address output 11
66	A10	Address output 10	ROM address output 10
67	A9	Address output 9	ROM address output 9
68	A8	Address output 8	ROM address output 8
69	V <sub>SS3</sub>	Ground	Connect a ground to this pin. (External ROM output system ground)
70	V <sub>DD3</sub>	Power supply (+3.3 or +5.5 V)	Power supply (External ROM output system power supply)
71	A7	Address output 7	ROM address output 7
72	A6	Address output 6	ROM address output 6
73	A5	Address output 5	ROM address output 5
74	A4	Address output 4	ROM address output 4
75	A3	Address output 3	ROM address output 3
76	A2	Address output 2	ROM address output 2
77	A1	Address output 1	ROM address output 1
78	A0	Address output 0	ROM address output 0
79	V <sub>SS3</sub>	Ground	Connect a ground to this pin. (External ROM output system ground)
80	V <sub>DD3</sub>	Power supply (+3.3 or +5.5 V)	Power supply (External ROM output system power supply)

## Specifications

### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD1}$	$V_{DD1}, V_{DD2}$	$V_{SS} - 0.3$ to $V_{SS} + 4.6$	V
	$V_{DD3}$	$V_{DD3}$	$V_{SS} - 0.3$ to $V_{SS} + 6.0$	V
Input voltage	$V_{IN}$	All input pins	$V_{SS} - 0.3$ to $V_{DD1} + 0.3$	V
Output voltage	$V_{OUT1}$	RD2 to 0, GD2 to 0, BD2 to 0, and BLK outputs	$V_{SS} - 0.3$ to $V_{DD1} + 0.3$	V
	$V_{OUT2}$	A0 to A17, $\overline{CE}$ , $\overline{OE}$ outputs	$V_{SS} - 0.3$ to $V_{DD1} + 0.3$	V
Maximum power dissipation	$P_{dmax}$		230	mW
Operating temperature	$T_{opg}$		$-30$ to $+70$	$^\circ\text{C}$
Storage temperature	$T_{stg}$		$-40$ to $+125$	$^\circ\text{C}$

### Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD1}$	$V_{DD1}, V_{DD2}$	3.0	3.3	3.6	V
	$V_{DD3}$	$V_{DD3}$	3.0	3.3	5.5	V
Input high-level voltage	$V_{IH1}$	CTRL1, TEST1, TEST2	$0.7 V_{DD1}$	—	5.5	V
	$V_{IH2}$	SCLK, SIN, $\overline{CS}$ , VSYNC, HSYNC, $\overline{RST}$	$0.8 V_{DD1}$	—	5.5	V
	$V_{IH3}$	D0 to D11	$0.7 V_{DD1}$	—	5.5	V
Input low-level voltage	$V_{IL1}$	CTRL1, TEST1, TEST2	$V_{SS} - 0.3$	—	$0.3 V_{DD1}$	V
	$V_{IL2}$	SCLK, SIN, $\overline{CS}$ , VSYNC, HSYNC, $\overline{RST}$	$V_{SS} - 0.3$	—	$0.2 V_{DD1}$	V
	$V_{IL3}$	D0 to D11	$V_{SS} - 0.3$	—	$0.3 V_{DD1}$	V
Oscillator frequency	$F_{OSC1}$	OSCI <sub>n</sub> and OSCOUT oscillator pins (LC oscillator)	—	10	—	MHz
External clock input	$F_{OSC2}$	OSCI <sub>n</sub> , $V_{DD1} = 3.3\text{ V}$	—	33	40	MHz
	$V_{IN1}$	$V_{DD1} = 3.3\text{ V}$ , CTRL1 = high	0.5	—	3.3	V <sub>p-p</sub>
D/A converter (3 bit, 3 ch) When maximum output voltage = 0.7 V	$V_{refda}$	Reference voltage	—	1.1	—	V
	$R_{fda}$	Output load resistance ROUT, GOUT, and BOUT	120	—	225	$\Omega$
	$R_{fbda}$	Output load resistance OUTR	40	—	75	$\Omega$
	$R_{ref}$	Reference load resistance, RREF	1232	—	2310	$\Omega$

# LC74735NW

**Electrical Characteristics at Ta = –30 to +70°C, V<sub>DD</sub> = 3.3 V unless otherwise specified.**

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Output high-level voltage	V <sub>OH1</sub>	RD2 to 0, GD2 to 0, BD2 to 0, and BLK outputs	V <sub>DD1</sub> = 3.0 V I <sub>OH1</sub> = –8 mA	V <sub>DD1</sub> – 0.8	—	—	V
	V <sub>OH2</sub>	A0 to 17, $\overline{\text{CE}}$ , and $\overline{\text{OE}}$	V <sub>DD3</sub> = 3.0 V I <sub>OH2</sub> = –8 mA	V <sub>DD3</sub> – 0.8	—	—	V
	V <sub>OH3</sub>	A0 to 17, $\overline{\text{CE}}$ , and $\overline{\text{OE}}$	V <sub>DD3</sub> = 4.5 V I <sub>OH3</sub> = –8 mA	V <sub>DD3</sub> – 0.8	—	—	V
Output low-level voltage	V <sub>OL1</sub>	RD2 to 0, GD2 to 0, BD2 to 0, and BLK outputs	V <sub>DD1</sub> = 3.0 V I <sub>OL1</sub> = 8 mA	—	—	0.4	V
	V <sub>OL2</sub>	A0 to 17, $\overline{\text{CE}}$ , and $\overline{\text{OE}}$	V <sub>DD3</sub> = 3.0 V I <sub>OL2</sub> = 8 mA	—	—	0.4	V
	V <sub>OL3</sub>	A0 to 17, $\overline{\text{CE}}$ , and $\overline{\text{OE}}$	V <sub>DD3</sub> = 4.5 V I <sub>OL3</sub> = 8 mA	—	—	0.4	V
Input current	I <sub>IH1</sub>	CTRL1, TEST1, TEST2, SCLK, SIN, $\overline{\text{CS}}$ , VSYNC, HSYNC, $\overline{\text{RST}}$	V <sub>IN</sub> = V <sub>DD1</sub>	—	—	10	μA
	I <sub>IH2</sub>	D0 to 11	V <sub>IN</sub> = V <sub>DD3</sub>	—	—	10	μA
	I <sub>IL1</sub>	CTRL1, TEST1, TEST2, SCLK, SIN, $\overline{\text{CS}}$ , VSYNC, HSYNC	V <sub>IN</sub> = V <sub>SS</sub>	–10	—	—	μA
	I <sub>IL2</sub>	D0 to 11	V <sub>IN</sub> = V <sub>SS</sub>	–10	—	—	μA
Operating current drain	I <sub>DD1</sub>	V <sub>DD1</sub>	All outputs open OSCin: 40 MHz	—	—	37	mA
	I <sub>DD2</sub>	V <sub>DD2</sub>	D/A on	—	—	22	mA
	I <sub>DD3</sub>	V <sub>DD3</sub>		—	—	20	mA
D/A converter	CLK	Clock frequency		—	—	20	MHz
	V <sub>max</sub>	Maximum output voltage	V <sub>DD2</sub> = 3.3 V	0.25	—	1.5	V
	V <sub>min</sub>	Minimum output voltage	V <sub>DD2</sub> = 3.3 V	—	0	—	V

## Timing Characteristics

OSD Write (See figure 1.) at  $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{DD1} = 3.3 \pm 0.3 \text{ V}$ 

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_w(\text{sclk})$	SCLK	200	—	—	ns
	$t_w(\text{cs})$	$\overline{\text{CS}}$ (The period $\overline{\text{CS}}$ is high)	1	—	—	$\mu\text{s}$
Data setup time	$t_{su}(\text{cs})$	$\overline{\text{CS}}$	200	—	—	ns
	$t_{su}(\text{sin})$	SIN	200	—	—	ns
Data hold time	$t_h(\text{cs})$	$\overline{\text{CS}}$	2	—	—	$\mu\text{s}$
	$t_h(\text{sin})$	SIN	200	—	—	ns
One word write time	$t_{\text{word}}$	The time to write 8 bits of data	4.2	—	—	$\mu\text{s}$
	$t_{wt}$	RAM data write time	1	—	—	$\mu\text{s}$

## Supplementary Materials

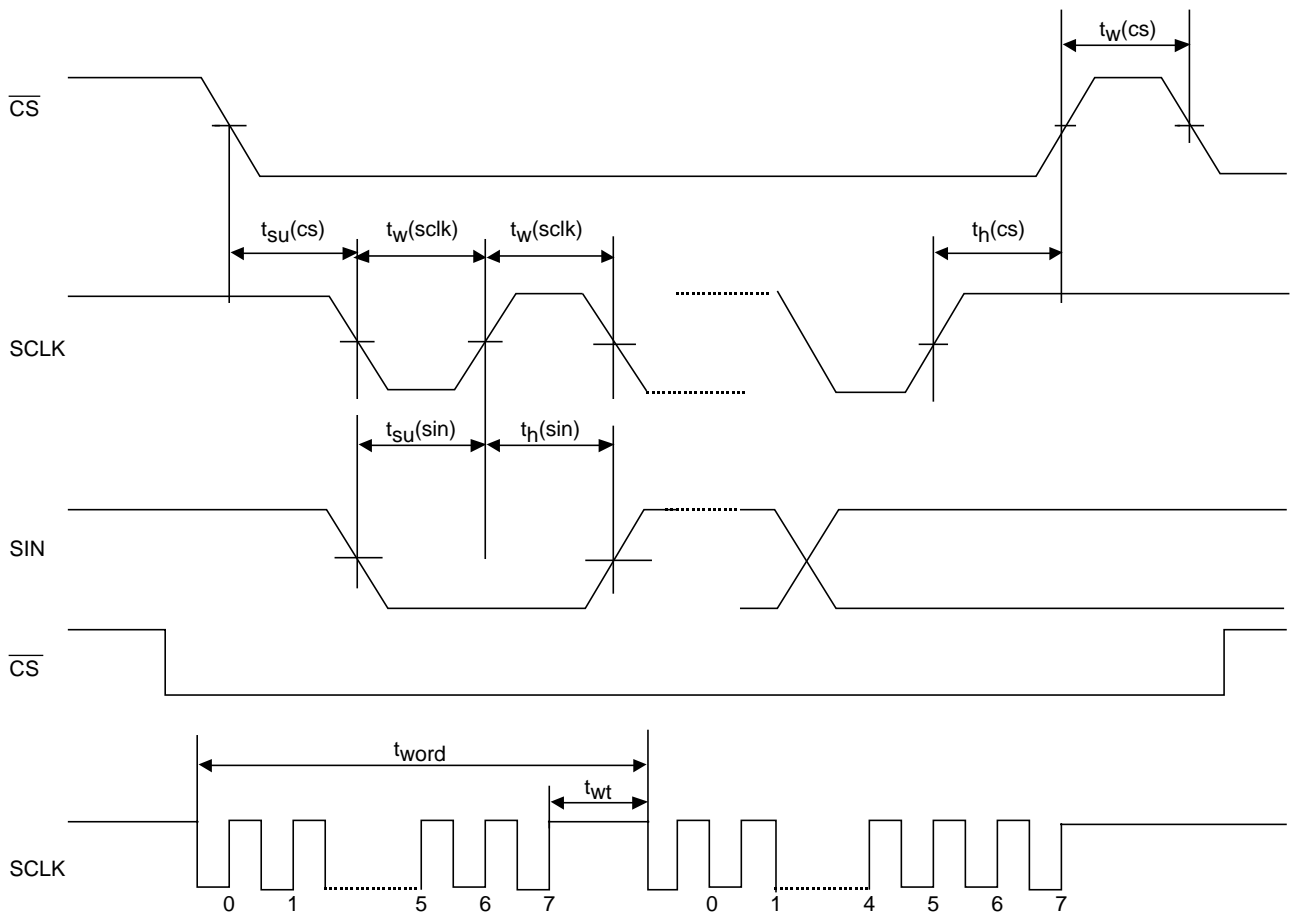
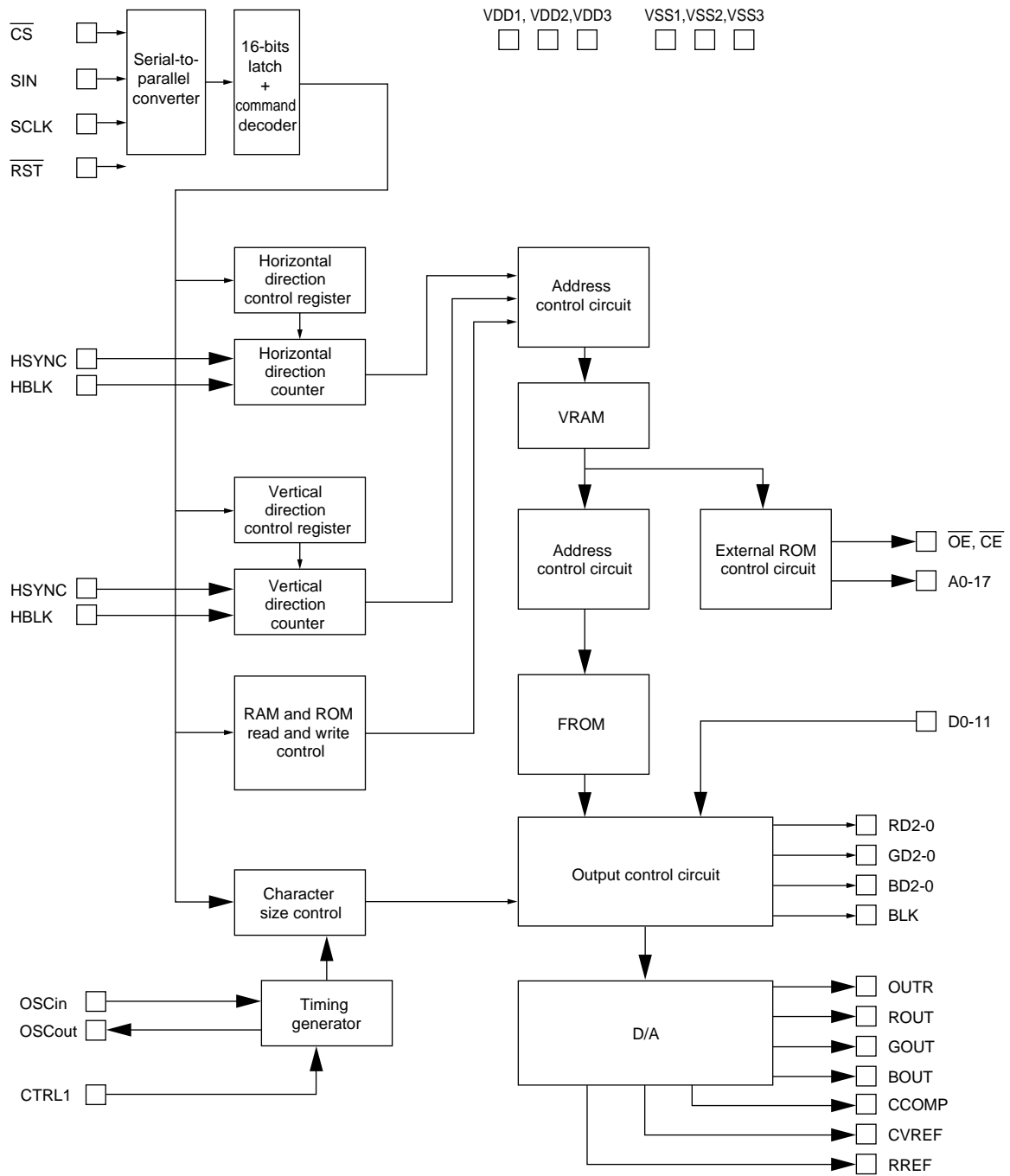


Figure 1 OSD Serial Data Input Timing



# System Block Diagram



## Display Control Commands

The display control commands have serial input format that consists of 8-bit units transmitted LSB first. A command consists of a command identification code in the first byte and data in the second and following bytes. Both a first byte and a second byte (16 bits) must be transmitted for each command. Commands 10, 11, and 71 set the IC to continuous write mode. (Continuous write mode is cleared by setting the  $\overline{\text{CS}}$  pin high.)

## Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Command00 (Write address) Main	1	0	0	0	0	0	V3	V2	V1	V0	H5	H4	H3	H2	H1	H0
Command01 (Write address) Sub (Wallpaper)	1	0	0	0	0	1	0	0	0	SV0	0	0	0	0	0	SH0
Command 10 (Character write) Main	1	0	0	1	0	0	RM2	RM1(1)	0	0	at	BXS	BXL	BXR	BXU	BXD
								(2)	CB3	CB2	CB1	CB0	CC3	CC2	CC1	CC0
								(3)	0	0	CT0	I/E	M/G	C10	C9	C8
								(4)	C7	C6	C5	C4	C3	C2	C1	C0
Command 11 (Character write) Sub (Wallpaper)	1	0	0	1	0	1	RM2	RM1(1)	0	0	0	0	0	0	0	0
								(2)	0	0	0	0	0	0	0	0
								(3)	0	0	CT0	I/E	M/G	C10	C9	C8
								(4)	C7	C6	C5	C4	C3	C2	C1	C0
Command20 (System control)	1	0	1	0	0	0	0	0	TSTMD2	TSTMD1	Q/W2	Q/W1	SYSRST	CTERS	SRMERS	MRMERS
Command21 (Display control)	1	0	1	0	0	0	0	1	LCSOFF	BK1	BK0	SBG1	SBG0	DSPBG	DSPGS	DSPGM
Command22 (I/O polarity control 1)	1	0	1	0	0	0	1	0	BLD1	BLO0	BLOP	BLO1	BLO0	CKP	VIP	HIP
Command23 (Screen background color)	1	0	1	0	0	0	1	1	0	0	BGCT1	BGCT0	BGC3	BGC2	BGC1	BGC0
Command24 (I/O polarity control 2)	1	0	1	0	0	1	0	0	DSPMD1	DSPMD0	DASEL	VLKON	HBLKON	CKOP	VBP	HBP
Command25 (Output control)	1	0	1	0	0	1	0	1	CEHSL	TOKSL	VIPSL	OTM2	OTM1	OTM0	QRM1	QRM0
Command30 (Vertical display start position: main)	1	0	1	1	0	0	0	0	VPM7	VPM6	VPM5	VPM4	VPM3	VPM2	VPM1	VPM0
Command31 (Horizontal display start position: main)	1	0	1	1	0	0	1	HPM8	HPM7	HPM6	HPM5	HPM4	HPM3	HPM2	HPM1	HPM0
Command32 (Vertical display start position: sub)	1	0	1	1	0	1	0	0	VPS7	VPS6	VPS5	VPS4	VPS3	VPS2	VPS1	VPS0
Command33 (Horizontal display start position: sub)	1	0	1	1	0	1	1	HPS8	HPS7	HPS6	HPS5	HPS4	HPS3	HPS2	HPS1	HPS0
Command34 (Vertical display start position: screen)	1	0	1	1	1	0	0	0	VPG7	VPG6	VPG5	VPG4	VPG3	VPG2	VPG1	VPG0
Command35 (Horizontal display start position: screen)	1	0	1	1	1	0	1	HPG8	HPG7	HPG6	HPG5	HPG4	HPG3	HPG2	HPG1	HPG0
Command40 (Character size control)	1	1	0	0	0	0	0	0	0	0	0	0	SZV1	SZV0	SZH1	SZH0
Command41 (Character size control: line setting U)	1	1	0	0	0	1	0	0	LSZ7	LSZ6	LSZ5	LSZ4	LSZ3	LSZ2	LSZ1	LSZ0
Command42 (Character size control: line setting D)	1	1	0	0	1	0	0	0	LSZ15	LSZ14	LSZ13	LSZ12	LSZ11	LSZ10	LSZ9	LSZ8
Command50 (Box control U)	1	1	0	1	0	0	0	0	BXUW	BXLW	0	BXUCT0	BXUC3	BXUC2	BXUC1	BXUC0
Command51 (Box control D)	1	1	0	1	0	1	0	0	BXDW	BXRW	0	BXDCT0	BXDC3	BXDC2	BXDC1	BXDC0
Command52 (Box control: line setting U)	1	1	0	1	1	0	0	0	LBX7	LBX6	LBX5	LBX4	LBX3	LBX2	LBX1	LBX0
Command53 (Box control: line setting D)	1	1	0	1	1	1	0	0	LBX15	LBX14	LBX13	LBX12	LBX11	LBX10	LBX9	LBX8
Command60 (Border control)	1	1	1	0	0	0	BLK1	BLK0	0	0	0	EGCT0	EGC3	EGC2	EGC1	EGC0
Command61 (Border control: line setting U)	1	1	1	0	0	1	0	0	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
Command62 (Border control: line setting D)	1	1	1	0	1	0	0	0	LFC15	LFC14	LFC13	LFC12	LFC11	LFC10	LFC9	LFC8
Command70 (Write address) Color table	1	1	1	1	0	0	0	0	0	0	0	CTN1	CTA3	CTA2	CTA1	CTA0
Command71 (Data write) Color table	1	1	1	1	0	1	0	RMB(1)	0	0	0	0	TCK	TB2	TB1	TB0
								(2)	0	0	TG2	TG1	TG0	TR2	TR1	TR0

**Command 00 (Main screen write address set command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 0 identification code Main screen write address setting	
6	—	0		
5	—	0		
4	—	0		
3	—	0	Sub-identification code: 0	
2	—	0		
1	V3 <MSB>	0		
		1		
0	V2	0		
		1		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	V1	0	Main screen memory line address (0 to E, hexadecimal)	
		1		
6	V0 <LSB>	0	QVGA mode: 13 lines	
		1	WVGA mode: 15 lines	
5	H5 <MSB>	0	Main screen memory character position address (00 to 27, hexadecimal) QVGA mode: 40 characters WVGA mode: 33 characters	
		1		
4	H4	0		
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0 <LSB>	0		
		1		

**Command 01 (Subscreen write address set command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 0 identification code Subscreen memory write address setting	
6	—	0		
5	—	0		
4	—	0		
3	—	0	Sub-identification code: 1	
2	—	1		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	V0	0	Subscreen memory line address (0 to 1, hexadecimal) 2 lines	
		1		
5	—	0		
4	—	0		
3	—	0		
2	—	0		
1	—	0		
0	H0 <LSB>	0	Subscreen memory character address (0 to 1, hexadecimal) 2 characters	
		1		

**Command 10 (Main screen display character data write setting command)**

## • First byte

DA0 to 7	Register	Content				Notes																				
		State	Function																							
7	—	1	Command 1 identification code Display character data write setting			When this command has been issued, the IC remains in display character data write mode until the CS pin is set high.																				
6	—	0																								
5	—	0																								
4	—	1																								
3	—	0	Sub-identification code 0																							
2	—	0																								
1	RM2	0	<table><tr><td>RM2</td><td>RM1</td><td colspan="2">Mode</td></tr><tr><td>0</td><td>0</td><td>(1)(2)(3)(4)</td><td>End</td></tr><tr><td>0</td><td>1</td><td>(1)(2)(3)(4)</td><td>Continuous</td></tr><tr><td>1</td><td>0</td><td>(3)(4)</td><td>Continuous</td></tr><tr><td>1</td><td>1</td><td>(2)(3)(4)</td><td>Continuous</td></tr></table>			RM2	RM1	Mode		0	0	(1)(2)(3)(4)	End	0	1	(1)(2)(3)(4)	Continuous	1	0	(3)(4)	Continuous	1	1	(2)(3)(4)	Continuous	Continuous write mode selection
		RM2				RM1	Mode																			
0	0	(1)(2)(3)(4)				End																				
0	1	(1)(2)(3)(4)				Continuous																				
1	0	(3)(4)				Continuous																				
1	1	(2)(3)(4)				Continuous																				
1	1																									
0	RM1	0																								
		1																								

## • Second byte (1)

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	—	0		
5	at	0	Blinking off	Blinking specification
		1	Blinking on	
4	BXS	0	Raised	Box specification: raised/recessed
		1	Recessed	
3	BXL	0	None	Box specification: left side
		1	Box displayed	
2	BXR	0	None	Box specification: right side
		1	Box displayed	
1	BXU	0	None	Box specification: upper
		1	Box displayed	
0	BXD	0	None	Box specification: lower
		1	Box displayed	

## • Second byte (2)

DA0 to 7	Register	Content		Notes
		State	Function	
7	CB3 [MSB]	0	Character background color specification 0000 to 1111, or 0 to F (hexadecimal)	Character background color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
6	CB2	0		
		1		
5	CB1	0		
		1		
4	CB0 [LSB]	0		
		1		
3	CC3 [MSB]	0	Character color specification 0000 to 1111, or 0 to F (hexadecimal)	Character color specification When a character glyph is specified, 1 of 16 colors may be selected.
		1		
2	CC2	0		
		1		
1	CC1	0		
		1		
0	CC0 <LSB>	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the RST pin.

## LC74735NW

### • Second byte (3)

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	—	0		
5	CT0	0	Color table number 1	Color table selection
		1	Color table number 2	
4	I/E	0	Internal ROM	ROM selection
		1	External ROM	
3	M/G	0	Character	Character/graphic specification
		1	Graphic	
2	C10 [MSB]	0		Character code specification
		1		
1	C9	0		
		1		
0	C8	0		
		1		

### • Second byte (4)

DA0 to 7	Register	Content		Notes
		State	Function	
7	C7	0	Character code Internal ROM: 512 characters 000 to 1FF (hexadecimal) 0 to 511  External ROM: 2048 characters 000 to 7FF (hexadecimal) 0 to 2047  * Transparent character specification I/E = 0 (Internal ROM) M/G = 0 (Character) Code = 1FF (hexadecimal)	Character code specification
		1		
6	C6	0		
		1		
5	C5	0		
		1		
4	C4	0		
		1		
3	C3	0		
		1		
2	C2	0		
		1		
1	C1	0		
		1		
0	C0 [LSB]	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 11 (Subscreen display character data write setting command)**

## • First byte

DA0 to 7	Register	Content				Notes																				
		State	Function																							
7	—	1	Command 1 identification code Display character data write setting			When this command has been issued, the IC remains in display character data write mode until the CS pin is set high.																				
6	—	0																								
5	—	0																								
4	—	1																								
3	—	0	Sub-identification code 1																							
2	—	1																								
1	RM2	0	<table><tr><td>RM2</td><td>RM1</td><td colspan="2">Mode</td></tr><tr><td>0</td><td>0</td><td>[1][2][3][4]</td><td>End</td></tr><tr><td>0</td><td>1</td><td>[1][2][3][4]</td><td>Continuous</td></tr><tr><td>1</td><td>0</td><td>[3][4]</td><td>Continuous</td></tr><tr><td>1</td><td>1</td><td>[2][3][4]</td><td>Continuous</td></tr></table>			RM2	RM1	Mode		0	0	[1][2][3][4]	End	0	1	[1][2][3][4]	Continuous	1	0	[3][4]	Continuous	1	1	[2][3][4]	Continuous	Continuous write mode selection
		RM2				RM1	Mode																			
0	0	[1][2][3][4]				End																				
0	1	[1][2][3][4]				Continuous																				
1	0	[3][4]				Continuous																				
1	1	[2][3][4]				Continuous																				
1	1																									
0	RM1	0																								
		1																								
		0																								
		1																								

## • Second byte (1)

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	—	0		
5		0		
4		0		
3		0		
2		0		
1		0		
0		0		

## • Second byte (2)

DA0 to 7	Register	Content		Notes
		State	Function	
7		0		
6		0		
5		0		
4		0		
3		0		
2		0		
1		0		
0		0		

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

• Second byte (3)

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	—	0		
5	CT0	0	Color table number 1	Color table selection
		1	Color table number 2	
4	I/E	0	Internal ROM	ROM selection
		1	External ROM	
3	M/G	0	Only when transparent is selected	Graphic only
		1	Graphic only	
2	C10 [MSB]	0		Character code specification
		1		
1	C9	0		
		1		
0	C8	0		
		1		

• Second byte (4)

DA0 to 7	Register	Content		Notes
		State	Function	
7	C7	0	Character code Internal ROM: 512 characters 000 to 1FF (hexadecimal) 0 to 511  External ROM: 2048 characters 000 to 7FF (hexadecimal) 0 to 2047  * Transparent character specification I/E = 0 (Internal ROM) M/G = 0 (Character) Code = 1FF (hexadecimal)	Character code specification
		1		
6	C6	0		
		1		
5	C5	0		
		1		
4	C4	0		
		1		
3	C3	0		
		1		
2	C2	0		
		1		
1	C1	0		
		1		
0	C0 [LSB]	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.



**Command 20 (System control setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code System control settings	
6	—	0		
5		1		
4		0		
3		0	Sub-identification code 0	
2		0		
1		0		
0		0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	TSTMD2	0	Normal operation	Do not use test mode. This bit must always be set to 0.
		1	Test mode 2	
6	TSTMD1	0	Normal operation	Do not use test mode. This bit must always be set to 0.
		1	Test mode 1	
5	Q/W2	0	Normal mode	Normal / Independent
		1	Independent mode    Specified by COM24.	
4	Q/W1	0	QVGA mode    D/A converter on, 40 characters × 13 lines	QVGA / WVGA
		1	WVGA mode    D/A converter off, 33 characters × 15 lines	
3	SYSRST	0		The registers are reset when the $\overline{CS}$ pin is low. The reset state is cleared when the $\overline{CS}$ pin goes high.
		1	Reset all registers (All bits set to 0.)	
2	CTERS	0		Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		1	Erase the color table. (Sets all values to 00.)	
1	SRMERS	0		Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		1	Erase main RAM. (Sets all values to 00.) Wallpaper	
0	MRMERS	0		Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		1	Erase sub-RAM. (Sets all values to 00.) Main screen	

**Command 21 (Display control setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code Display control	
6	—	0		
5	—	1		
4	—	0		
3	—	0	Extended command 1 identification code	
2	—	0		
1	—	0		
0	—	1		

## • Second byte

DA0 to 7	Register	Content				Notes														
		State	Function																	
7	LCSOFF	0	Enables stopping the LC oscillator			LC oscillator on/off control														
		1	Disables stopping the LC oscillator			Valid when the display is off.														
6	BK1	0	<table><tr><th>BK1</th><th>BK0</th><th>Blinking period</th></tr><tr><td>0</td><td>0</td><td>1/16</td></tr><tr><td>0</td><td>1</td><td>1/32</td></tr><tr><td>1</td><td>0</td><td>1/64</td></tr></table>			BK1	BK0	Blinking period	0	0	1/16	0	1	1/32	1	0	1/64	Blinking period Specified for screen units.		
		BK1				BK0	Blinking period													
0	0	1/16																		
0	1	1/32																		
1	0	1/64																		
1																				
5	BK0	0																		
		1																		
4	SBG1	0	Display after the main screen			Subscreen display specification														
		1	Display before the main screen																	
3	SBG0	0	Iterated display (wallpaper)			Subscreen display specification														
		1	Horizontal 2-character x vertical 2-character display (sprite)																	
2	DSPBG	0	Display off			Screen background color														
		1	Display on																	
1	DSPGS	0	Display off			Subscreen (wallpaper)														
		1	Display on																	
0	DSPGM	0	Display off			Main screen														
		1	Display on																	

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 22 (I/O polarity control setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code I/O polarity control 1	
6	—	0		
5	—	1		
4	—	0		
3	—	0	Extended command 2 identification code	
2	—	0		
1	—	1		
0	—	0		

## • Second byte

DA0 to 7	Register	Content				Notes
		State	Function			
7	BLD1	0	BLD1	BLD0	BLY output delay	BLK output delay setting In dot clock units
6	BLD0	1	0	0	±0	
		0	0	1	+1	
		1	0	0	+2	
		1	1	1	+3	
5	BLOP	0	BLK output: positive polarity			BLK output polarity selection
		1	BLK output: negative polarity			
4	BLO1	0	BLO1	BLO0	BLK output	BLK output control
		1	0	0	Text + character background + wallpaper + screen background	
		0	0	1	Text + character background + wallpaper	
		1	0	0	Text + character background	
3	BLO0	0	1	1	Text	
2	CKP	0	Clock input: positive polarity			Clock input polarity selection
		1	Clock input: negative polarity			
1	VIP	0	VSYNC input: negative polarity			VSYNC input polarity selection
		1	VSYNC input: positive polarity			
0	HIP	0	HSYNC input: negative polarity			HSYNC input polarity selection
		1	HSYNC input: positive polarity			

\*: This register is set to the all bits zero state when the IC is reset by the RST pin.

**Command 23 (Screen background color setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code	
6	—	0		
5	—	1		
4	—	0	Screen background color	
3	—	0		
2	—	0	Extended command 3 identification code	
1		1		
0		1		

## • Second byte

DA0 to 7	Register	Content			Notes													
		State	Function															
7	—	0																
6	—	0																
5	BGCT1	0	<table><tr><td>T1</td><td>T0</td><td>Color table setting</td></tr><tr><td>0</td><td>0</td><td>Color table No. 2</td></tr><tr><td>0</td><td>1</td><td>Invalid setting</td></tr><tr><td>1</td><td>X</td><td>Color table No. 1</td></tr></table>		T1	T0	Color table setting	0	0	Color table No. 2	0	1	Invalid setting	1	X	Color table No. 1	Screen background color Color table setting	
		T1	T0	Color table setting														
0	0	Color table No. 2																
0	1	Invalid setting																
1	X	Color table No. 1																
1																		
4	BGCT0	0																
		1																
3	BGC3	0	Screen background color 0000 to 1111 0 to F (hexadecimal)		Screen background color Selects 1 of 16 values.													
		1																
2	BGC2	0																
		1																
1	BGC1	0																
		1																
0	BGC0	0																
		1																

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 24 (I/O polarity control setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code I/O polarity control 2	
6	—	0		
5	—	1		
4	—	0		
3	—	0	Extended command 4 identification code	
2	—	1		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content				Notes														
		State	Function																	
7	DSPMD1	0	<table><tr><th>MD1</th><th>MD0</th><th>Main screen display area</th></tr><tr><td>0</td><td>0</td><td>40 characters × 13 lines</td></tr><tr><td>0</td><td>1</td><td>33 characters × 15 lines</td></tr><tr><td>1</td><td>0</td><td>40 characters × 16 lines</td></tr></table>			MD1	MD0	Main screen display area	0	0	40 characters × 13 lines	0	1	33 characters × 15 lines	1	0	40 characters × 16 lines	Main screen display area selection Only valid in independent mode. COM20 to COM2 *: In WVGA mode: fixed 33-character × 15-line display		
		MD1				MD0	Main screen display area													
0	0	40 characters × 13 lines																		
0	1	33 characters × 15 lines																		
1	0	40 characters × 16 lines																		
1																				
6	DSPMD0	0	<table><tr><th>MD1</th><th>MD0</th><th>Main screen display area</th></tr><tr><td>0</td><td>1</td><td>33 characters × 15 lines</td></tr><tr><td>1</td><td>0</td><td>40 characters × 16 lines</td></tr></table>			MD1	MD0	Main screen display area	0	1	33 characters × 15 lines	1	0	40 characters × 16 lines	Main screen display area selection Only valid in independent mode. COM20 to COM2 *: In WVGA mode: fixed 33-character × 15-line display					
		MD1				MD0	Main screen display area													
0	1	33 characters × 15 lines																		
1	0	40 characters × 16 lines																		
1																				
5	D/ASEL	0	On			D/A converter used/unused selection Only valid in independent mode. COM20 to COM2														
		1	Off																	
4	VBLKON	0	Disabled			VBLK input selection														
		1	Enabled																	
3	HBLKON	0	Disabled			HBLK input selection														
		1	Enabled																	
2	CKOP	0	Clock output positive polarity			Clock output polarity selection														
		1	Clock output negative polarity																	
1	VBP	0	VBLK input negative polarity			VBLK input polarity selection														
		1	VBLK input positive polarity																	
0	HBP	0	HBLK input negative polarity			HBLK input polarity selection														
		1	HBLK input positive polarity																	

\*: This register is set to the all bits zero state when the IC is reset by the RST pin.

**Command 25 (Output control 3 setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code Output control	
6	—	0		
5	—	1		
4	—	0		
3	—	0	Extended command 5 identification code	
2	—	1		
1	—	0		
0	—	1		

## • Second byte

DA0 to 7	Register	Content		Notes																				
		State	Function																					
7	CEHSL	0	Normal operation	$\overline{\text{CE}}$ pin																				
		1	$\overline{\text{CE}}$ pin held fixed at the high level																					
6	TOKSL	0	Normal mode	Transmissive mode specification																				
		1	Transmissive mode The color specified at address 0 in color table No. 1 is displayed in the transmissive state.																					
5	VIPSL	0	Falling edge detection	Selects the detection polarity for the VSYNC signal.																				
		1	Rising edge detection																					
4	OTMD2	0	Output off state (always low)	CLKOUT pin (pin 18) Output control																				
		1	Normal output																					
3	OTMD1	0	<table><tr><th>OTMD2</th><th>OTMD1</th><th>OTMD0</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Normal</td></tr><tr><td>0</td><td>0</td><td>1</td><td>RGB No. 1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>RGB No. 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>High-impedance state</td></tr></table>	OTMD2	OTMD1	OTMD0	Output	0	0	0	Normal	0	0	1	RGB No. 1	0	1	0	RGB No. 2	0	1	1	High-impedance state	A0 to 17 output selection
OTMD2	OTMD1	OTMD0		Output																				
0	0	0		Normal																				
0	0	1		RGB No. 1																				
0	1	0		RGB No. 2																				
0	1	1	High-impedance state																					
	1																							
2	OTMD0	0																						
		1																						
1	QRM1	0	<table><tr><th>QRM1</th><th>QRM0</th><th>ROM selection</th></tr><tr><td>0</td><td>0</td><td>ROM1</td></tr><tr><td>0</td><td>1</td><td>ROM2</td></tr><tr><td>1</td><td>0</td><td>ROM3</td></tr><tr><td>1</td><td>1</td><td>ROM4</td></tr></table>	QRM1	QRM0	ROM selection	0	0	ROM1	0	1	ROM2	1	0	ROM3	1	1	ROM4	ROM selection when character output is specified in QVGA mode					
QRM1	QRM0	ROM selection																						
0	0	ROM1																						
0	1	ROM2																						
1	0	ROM3																						
1	1	ROM4																						
	1																							
0	QRM0	0																						
		1																						

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

## • When RGB No. 1 or RGB No. 2 is selected:

The A17 to 9 output is set to the RD2 to BD0 three-value output. (Supported by connecting external resistors.)

\* It will not be possible to use external ROM in this case. (Only internal ROM can be used.)

No. 1: RGB = 000 = Black only. Here the output will go to the high-impedance state giving the middle level due to the external resistor.

For areas other than the display area, the output will be at the low level.

No. 2: When any individual color is zero, the output will go to the high-impedance state giving the middle level due to the external resistor.

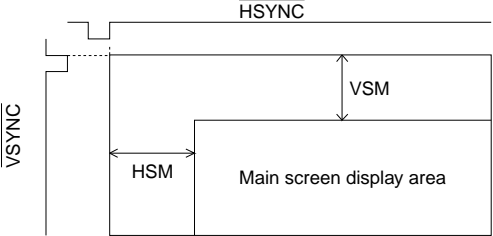
For areas other than the display area, the output will be at the low level.

**Command 30 (Main screen: vertical display start position setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 3 identification code Main screen: vertical display start position setting	
6	—	0		
5	—	1		
4	—	1		
3	—	0	Extended command 0 identification code	
2	—	0		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	VPM7 (MSB)	0	<p>The vertical display start position, VSM, is given by:</p> $VSM = 1H \times \left( \sum_{n=0}^7 2^n VPMn \right)$ 	<p>Main screen</p> <p>The vertical display start position is specified by the 8 bits VPM7 to 0.</p> <p>The weight of the LSB is 1H in QVGA mode, and the weight of the LSB is 2H in WVGA mode</p> <p>This setting applies in screen units.</p>
6	VPM6	0		
		1		
5	VPM5	0		
		1		
4	VPM4	0		
		1		
3	VPM3	0		
		1		
2	VPM2	0		
		1		
1	VPM1	0		
		1		
0	VPM0 (LSB)	0		
		1		

**Command 31 (Main screen: horizontal display start position setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 3 identification code Main screen: horizontal display start position setting	
6	—	0		
5	—	1		
4	—	1		
3	—	0	Extended command 1 identification code	
2	—	0		
1	—	1		
0	HPM8 (MSB)	0		
		1		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HPM7	0	The horizontal display start position, HSM, is given by: $\text{HSM} = 1\text{Tc} \times \left( \sum_{n=0}^8 2^n \text{HPM}n \right) + \alpha$ $\alpha = 57 \text{ Tc}$ Tc: The input clock frequency in operating mode.  • Setting disable range QVGA : 00 to 07 HEX WVGA : 00 to 07 HEX	Main screen The horizontal display start position is specified by the 9 bits HPM8:0. The weight of the LSB is 1TC in QVGA mode, and the weight of the LSB is 2TC in WVGA mode  This setting applies in screen units.
		1		
6	HPM6	0		
		1		
5	HPM5	0		
		1		
4	HPM4	0		
		1		
3	HPM3	0		
		1		
2	HPM2	0		
		1		
1	HPM1	0		
		1		
0	HPM0 (LSB)	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

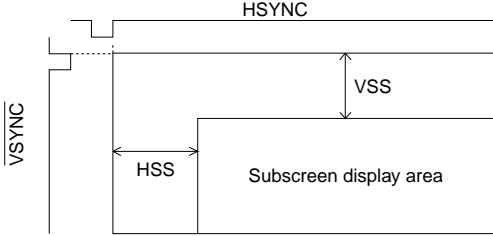


**Command 32 (Subscreen: vertical display start position setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 3 identification code Subscreen: vertical display start position setting	
6	—	0		
5	—	1		
4	—	1		
3	—	0	Extended command 2 identification code	
2	—	1		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	VPS7 (MSB)	0	<p>The vertical display start position, VSS, is given by:</p> $VSS = 1H \times \left( \sum_{n=0}^7 2^n VPS_n \right)$  <p>Subscreen (wallpaper) The vertical display start position is specified by the 8 bits VPS7 to 0. The weight of the LSB is 1H in QVGA mode, and the weight of the LSB is 2H in WVGA mode  This setting applies in screen units.</p>	
6	VPS6	0		
		1		
5	VPS5	0		
		1		
4	VPS4	0		
		1		
3	VPS3	0		
		1		
2	VPS2	0		
		1		
1	VPS1	0		
		1		
0	VPS0 (LSB)	0		
		1		

**Command 33 (Subscreen: horizontal display start position setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 3 identification code Subscreen: horizontal display start position setting	
6	—	0		
5	—	1		
4	—	1		
3	—	0	Extended command 3 identification code	
2	—	1		
1	—	1		
0	HPS8 (MSB)	0		
		1		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HPS7	0	The horizontal display start position, HSS, is given by: $HSS = 1Tc \times \left( \sum_{n=0}^8 HPSn \right) + \alpha$ $\alpha = 14 Tc$ Tc: The input clock frequency in operating mode.  • Setting disable range QVGA : 00 to 2F HEX WVGA : 00 to 17 HEX	Subscreen (wallpaper) The horizontal display start position is specified by the 9 bits HPS8 to 0. The weight of the LSB is 1TC in QVGA mode, and the weight of the LSB is 2TC in WVGA mode  This setting applies in screen units.
		1		
6	HPS6	0		
		1		
5	HPS5	0		
		1		
4	HPS4	0		
		1		
3	HPS3	0		
		1		
2	HPS2	0		
		1		
1	HPS1	0		
		1		
0	HPS0 (LSB)	0		
		1		

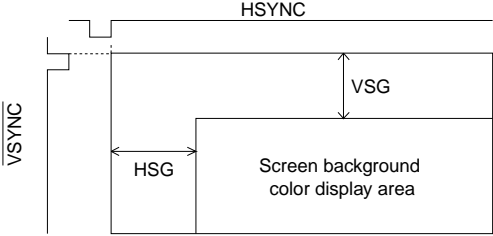
\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{RST}$  pin.

**Command 34 (Screen background color: vertical display start position setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 3 identification code Screen background color: vertical display start position setting	
6	—	0		
5	—	1		
4	—	1		
3	—	1	Extended command 4 identification code	
2	—	0		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	VPG7 (MSB)	0	<p>The vertical display start position, VSG, is given by:</p> $VSG = 1H \times \left( \sum_{n=0}^7 2^n VPG_n \right)$ 	<p>Screen background color</p> <p>The vertical display start position is specified by the 8 bits VPG7 to 0.</p> <p>The weight of the LSB is 1H in QVGA mode, and the weight of the LSB is 2H in WVGA mode</p> <p>This setting applies in screen units.</p>
6	VPG6	0		
		1		
5	VPG5	0		
		1		
4	VPG4	0		
		1		
3	VPG3	0		
		1		
2	VPG2	0		
		1		
1	VPG1	0		
		1		
0	VPG0 (LSB)	0		
		1		

**Command 35 (Screen background color: horizontal display start position setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 3 identification code	
6	—	0		
5	—	1		
4	—	1		
3	—	1	Screen background color: horizontal display start position setting	
2	—	0		
1	—	1		
0	—	0		
0	HPS8 (MSB)	0	Extended command 5 identification code	
		1		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	HPG7	0	<p>The horizontal display start position, HSG, is given by:</p> $\text{HSG} = 1\text{Tc} \times \left( \sum_{n=0}^8 2^n \text{HPG}_n \right)$ <p>Tc: The input clock frequency in operating mode.</p>	<p>Screen background color</p> <p>The horizontal display start position is specified by the 9 bits HPG8 to 0.</p> <p>The weight of the LSB is 1TC in QVGA mode, and the weight of the LSB is 2TC in WVGA mode</p> <p>This setting applies in screen units.</p>
		1		
6	HPG6	0		
		1		
5	HPG5	0		
		1		
4	HPG4	0		
		1		
3	HPG3	0		
		1		
2	HPG2	0		
		1		
1	HPG1	0		
		1		
0	HPG0 (LSB)	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 40 (Character size control setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 4 identification code Display character data write settings	
6	—	1		
5	—	0		
4	—	0		
3	—	0	Extended command 0 identification code	
2	—	0		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content				Notes																
		State	Function																			
7	—	0																				
6	—	0																				
5	—	0																				
4	—	0																				
3	SZV1	0	<table><tr><th>SZV1</th><th>SZV0</th><th>Character size</th></tr><tr><td>0</td><td>0</td><td>1×</td></tr><tr><td>0</td><td>1</td><td>2×</td></tr><tr><td>1</td><td>0</td><td>3×</td></tr><tr><td>1</td><td>1</td><td>4×</td></tr></table>			SZV1	SZV0	Character size	0	0	1×	0	1	2×	1	0	3×	1	1	4×	Specifies the character size in the vertical direction. This setting applies in line units.	
		SZV1				SZV0	Character size															
0	0	1×																				
0	1	2×																				
1	0	3×																				
1	1	4×																				
1																						
2	SZV0	0																				
		1																				
1	SZH1	0	<table><tr><th>SZH1</th><th>SZH0</th><th>Character size</th></tr><tr><td>0</td><td>0</td><td>1×</td></tr><tr><td>0</td><td>1</td><td>2×</td></tr><tr><td>1</td><td>0</td><td>3×</td></tr><tr><td>1</td><td>1</td><td>4×</td></tr></table>			SZH1	SZH0	Character size	0	0	1×	0	1	2×	1	0	3×	1	1	4×	Specifies the character size in the horizontal direction. This setting applies in line units.	
		SZH1				SZH0	Character size															
0	0	1×																				
0	1	2×																				
1	0	3×																				
1	1	4×																				
1																						
0	SZH0	0																				
		1																				

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 41 (Character size line U control setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 4 identification code Character size line U control	
6	—	1		
5	—	0		
4	—	0		
3	—	0	Extended command 1 identification code	
2	—	1		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LSZ7	0	Do not set for line 8.	Character size line setting control Upper lines
		1	Set for line 8.	
6	LSZ6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LSZ5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LSZ4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LSZ3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LSZ2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LSZ1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LSZ0	0	Do not set for line 1.	
		1	Set for line 1.	

**Command 42 (Character size line D control setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 4 identification code Character size line D control	
6	—	1		
5	—	0		
4	—	0		
3	—	1	Extended command 2 identification code	
2	—	0		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LSZ15	0	Do not set for line 16.	Character size line setting control Lower lines
		1	Set for line 16.	
6	LSZ14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LSZ13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LSZ12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LSZ11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LSZ10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LSZ9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LSZ8	0	Do not set for line 9.	
		1	Set for line 9.	

**Command 50 (Box control: U setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 5 identification code Box control U settings	
6	—	1		
5	—	0		
4	—	1	Extended command 0 identification code	
3	—	0		
2	—	0		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	BXUW	0	Box display: upper side is 1 dot.	Box display: upper side Dot width. This setting applies in line units.
		1	Box display: upper side is 2 dots.	
6	BXLW	0	Box display: left side is 1 dot.	Box display: left side Dot width. This setting applies in line units.
		1	Box display: left side is 2 dots.	
5	—	0		
4	BXUCT0	0	Color table No. 1	Box display: upper side Color table specification This setting applies in line units.
		1	Color table No. 2	
3	BXUC3	0	Box display: upper side color specification 0000 to 1111 0 to F (hexadecimal)	Box display: upper side Color specification This setting applies in line units.
		1		
2	BXUC2	0		
		1		
1	BXUC1	0		
		1		
0	BXUC0	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.



**Command 51 (Box control: D setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 5 identification code	
6	—	1		
5	—	0		
4	—	1	Box control D settings	
3	—	0		
2	—	1		
1	—	0	Extended command 1 identification code	
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	BXDW	0	Box display: lower side is 1 dot.	Box display: lower side Dot width. This setting applies in line units.
		1	Box display: lower side is 2 dots.	
6	BXRW	0	Box display: right side is 1 dot.	Box display: right side Dot width. This setting applies in line units.
		1	Box display: right side is 2 dots.	
5	—	0		
4	BXDCT0	0	Color table No. 1	Box display: lower side Color table specification This setting applies in line units.
		1	Color table No. 2	
3	BXDC3	0	Box display: lower side color specification 0000 to 1111 0 to F (hexadecimal)	Box display: lower side Color specification This setting applies in line units.
		1		
2	BXDC2	0		
		1		
1	BXDC1	0		
		1		
0	BXDC0	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 52 (Box control: U line setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 5 identification code Box control U line setting	
6	—	1		
5	—	0		
4	—	1	Extended command 2 identification code	
3	—	1		
2	—	0		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LBX7	0	Do not set for line 8.	Box control line setting control Upper lines
		1	Set for line 8.	
6	LBX6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LBX5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LBX4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LBX3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LBX2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LBX1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LBX0	0	Do not set for line 1.	
		1	Set for line 1.	

**Command 53 (Box control: D line control setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 4 identification code Box control D line setting	
6	—	1		
5	—	0		
4	—	0		
3	—	1	Extended command 3 identification code	
2	—	1		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LBX15	0	Do not set for line 16.	Box control line setting control Lower lines
		1	Set for line 16.	
6	LBX14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LBX13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LBX12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LBX11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LBX10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LBX9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LBX8	0	Do not set for line 9.	
		1	Set for line 9.	

**Command 60 (Border control setting command)**

## • First byte

DA0 to 7	Register	Content				Notes
		State	Function			
7	—	1	Command 6 identification code Border control setting			
6	—	1				
5	—	1				
4	—	0				
3	—	0	Extended command 0 identification code			
2	—	0				
1	BLK1	0	BLK1	BLK0	Border mode specification	Border mode specification This setting applies in line units.
		1	0	0	Normal display	
0	BLK0	0	0	1	Border	
		1	1	0	Shadow 1 (lower side)	
		1	1	1	Shadow 2 (lower and right sides)	

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	—	0		
5	—	0		
4	EGCT0	0	Color table No. 1	Border display Color table specification This setting applies in line units.
		1	Color table No. 2	
3	EGC3	0	Border display: color specification 0000 to 1111 0 to F (hexadecimal)	Border display color specification This setting applies in line units.
		1		
2	EGC2	0		
		1		
1	EGC1	0		
		1		
0	EGC0	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the RST pin.

**Command 61 (Border control U line setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 6 identification code Border control U line setting	
6	—	1		
5	—	1		
4	—	0	Extended command 1 identification code	
3	—	0		
2	—	1		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LFC7	0	Do not set for line 8.	Border control line settings control Upper lines
		1	Set for line 8.	
6	LFC6	0	Do not set for line 7.	
		1	Set for line 7.	
5	LFC5	0	Do not set for line 6.	
		1	Set for line 6.	
4	LFC4	0	Do not set for line 5.	
		1	Set for line 5.	
3	LFC3	0	Do not set for line 4.	
		1	Set for line 4.	
2	LFC2	0	Do not set for line 3.	
		1	Set for line 3.	
1	LFC1	0	Do not set for line 2.	
		1	Set for line 2.	
0	LFC0	0	Do not set for line 1.	
		1	Set for line 1.	

**Command 62 (Border control D line setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 6 identification code Border control D line setting	
6	—	1		
5	—	1		
4	—	0	Extended command 2 identification code	
3	—	1		
2	—	0		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	LFC15	0	Do not set for line 16.	Border control line settings control Lower lines
		1	Set for line 16.	
6	LFC14	0	Do not set for line 15.	
		1	Set for line 15.	
5	LFC13	0	Do not set for line 14.	
		1	Set for line 14.	
4	LFC12	0	Do not set for line 13.	
		1	Set for line 13.	
3	LFC11	0	Do not set for line 12.	
		1	Set for line 12.	
2	LFC10	0	Do not set for line 11.	
		1	Set for line 11.	
1	LFC9	0	Do not set for line 10.	
		1	Set for line 10.	
0	LFC8	0	Do not set for line 9.	
		1	Set for line 9.	

**Command 70 (Color table write address setting command)**

## • First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 7 identification code Color table write address setting	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Sub-identifier code 0	
2	—	0		
1	—	0		
0	—	0		

## • Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—			
6	—			
5	—			
4	CTN1	0	Color table No. 1 selected	Color table selection No. 1 or No. 2
		1	Color table No. 2 selected	
3	CTA3 <MSB>	0	Color table address 0 to 15 0 to F (hexadecimal) 16 values	Addresses of the color tables
		1		
2	CTA2	0		
		1		
1	CTA1	0		
		1		
0	CTA0 <LSB>	0		
		1		

**Command 71 (Color table data write setting command)**

## • First byte

DA0 to 7	Register	Content		Notes	
		State	Function		
7	—	1	Command 7 identification code Display character data write setting	When this command has been issued, the IC remains in display character data write mode until the $\overline{CS}$ pin is set high.	
6	—	1			
5	—	1			
4	—	1			
3	—	0	Sub-identifier code 1		
2	—	1			
1	—	0			
0	RM3	0	RM3	Mode	Continuous write mode selection
			0	[1][2]	
		1	1	[1][2]	

## • Second byte (1)

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	—	0		
5	—	0		
4	—	0		
3	TOK	0	Color	
		1	Transparent (BLK output: low)	
2	TB2	0	Color table B output 000 to 111 0 to 7 (hexadecimal)	Color table setting B
		1		
1	TB1	0		
		1		
0	TB0	0		
		1		

## • Second byte (2)

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	—	0		
5	TG2	0	Color table G output 000 to 111 0 to 7 (hexadecimal)	Color table setting G
		1		
4	TG1	0		
		1		
3	TG0	0	Color table R output 000 to 111 0 to 7 (hexadecimal)	Color table setting R
		1		
2	TR2	0		
		1		
1	TR1	0		
		1		
0	TR0	0		
		1		

\*: This register is set to the all bits zero state when the IC is reset by the  $\overline{\text{RST}}$  pin.

When transparent is selected, the BLK output is set to the low level. (Transparent state)

The RGB outputs are values from the color table.

The transparent specification is best for color table 1, address 0000.

Since the data is set to all zeros by a RAM clear operation,  
the RGB output will be 000 (black) and the BLK output will be 1.

Transparent is specified by setting the TOK bit to 1. (The BLK output will go to the low level.)



## Display Structure

The display screen consists of a 40-character  $\times$  15-line grid.

QVGA mode ( $12 \times 18$  dot characters)

40-character  $\times$  13-line QVGA panel ( $480 \times 234$ )

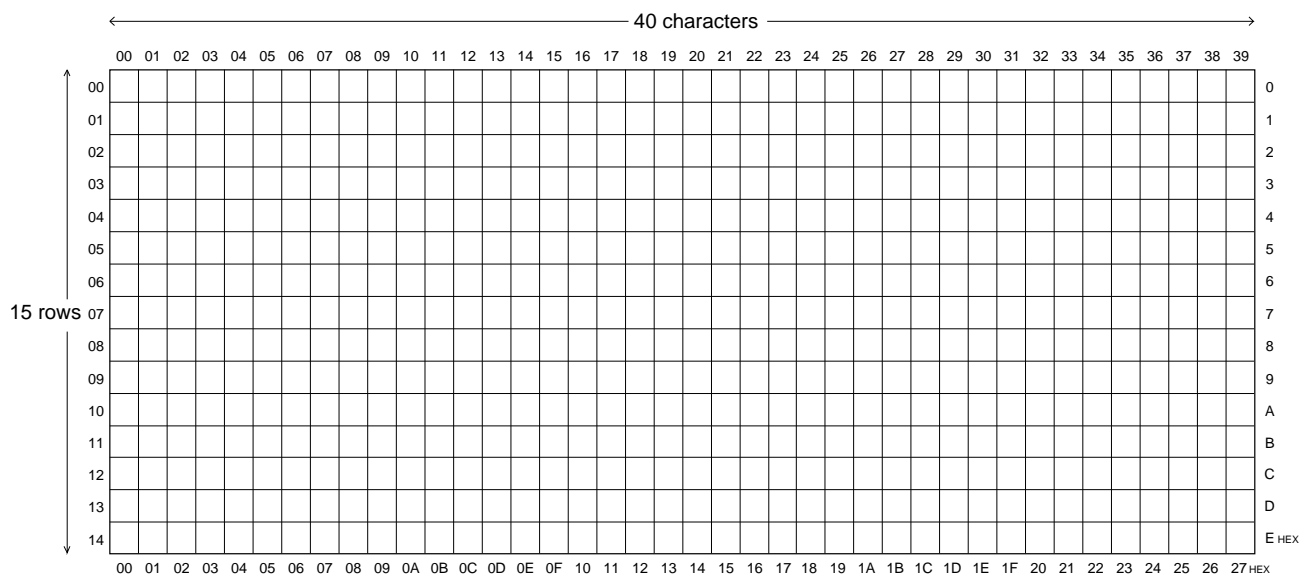
WVGA mode ( $12 \times 16$  dot characters)

33-character  $\times$  15-line WVGA panel ( $800 \times 480$ )

Up to a maximum of 600 characters can be displayed.

If the character size is increased, the number of characters that can be displayed will decrease to be fewer than 600 characters.

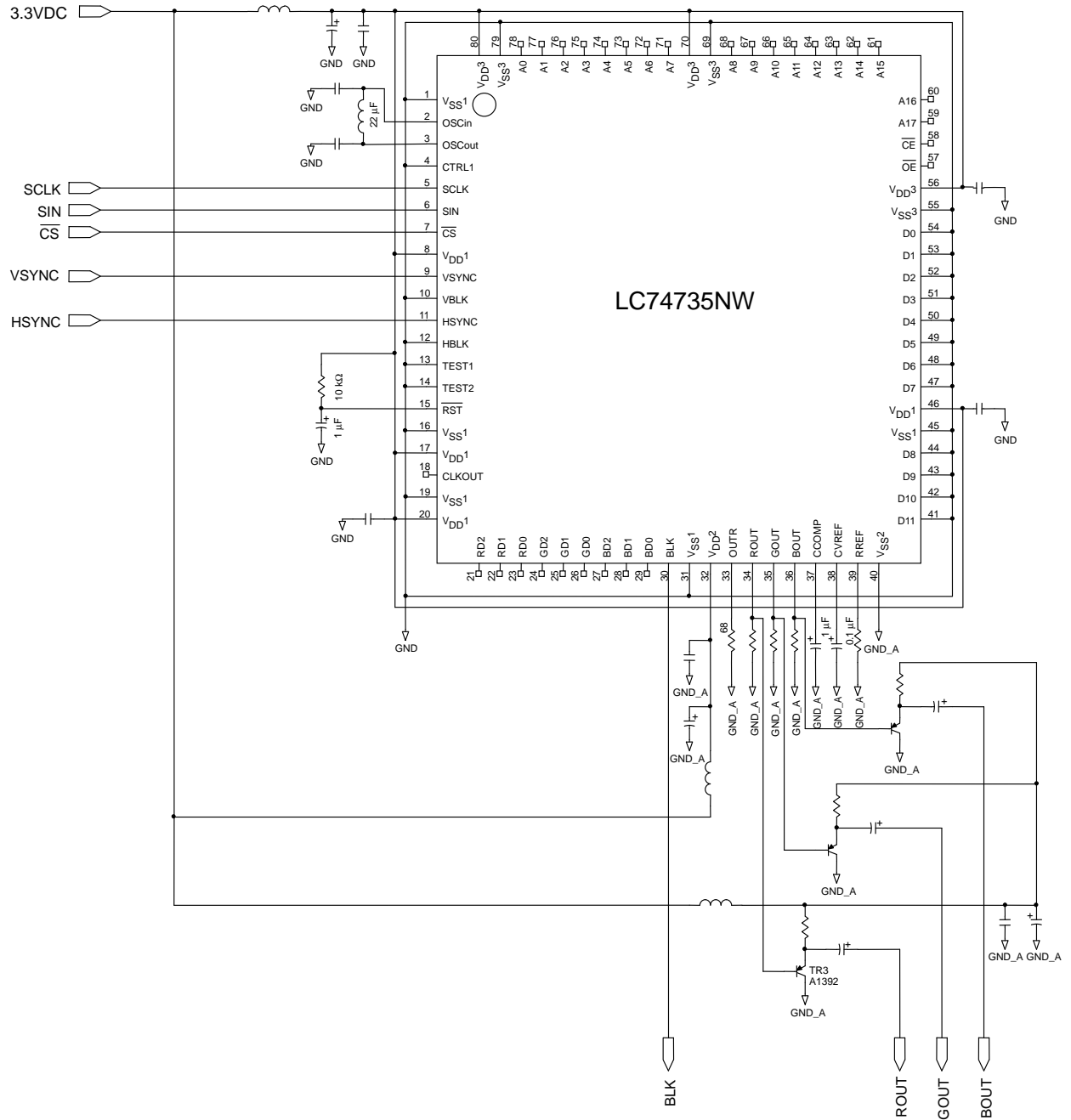
Display memory is addressed by specifying a line address (0 to 14 (decimal) and a character position address (0 to 39 (decimal)).



**Display Structure (Display memory address)**

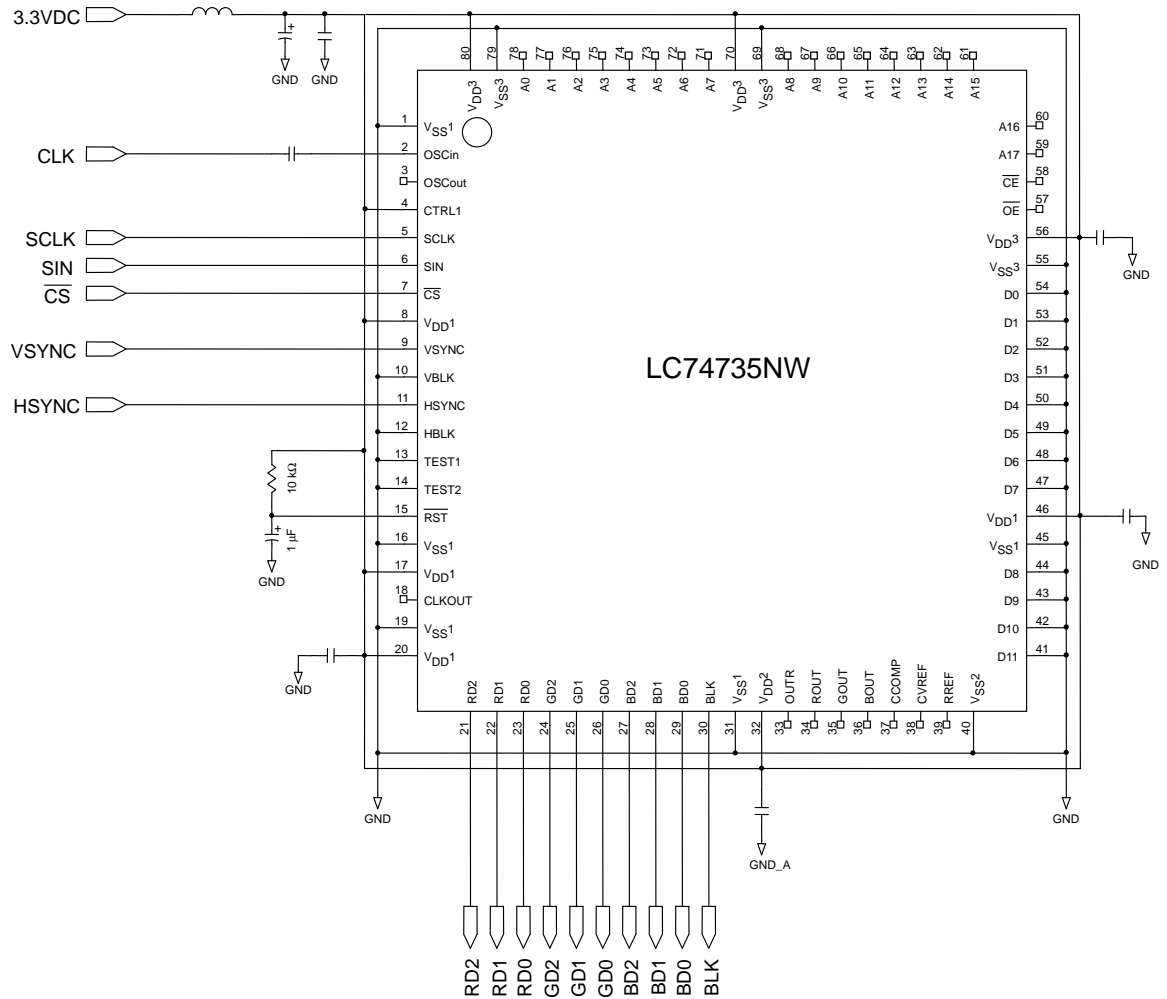
# Sample Application Circuits

- QVGA mode (analog output)



## LC74735NW

- WVGA mode (digital output)



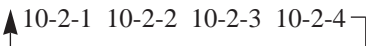
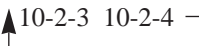
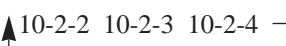
## Operational Description

### Command transfer method

#### Overview

- Commands are transferred in 8-bit units, LSB first.  
Always send a first byte and a second byte (16 bits).
- Command 10 (Main RAM write)  
Command 11 (Wallpaper write)  
Command 71 (Color table write)  
When these commands specify continuous mode (RM2, 1 RM3), the IC is locked in continuous write mode.  
(Continuous write mode is cleared by setting the CS  $\overline{\text{pin}}$  high.)

#### Writing Data to VRAM

- Write start address specification  
Use command 00 to set the write start address.  
V3:0: Vertical direction, H5:0: Horizontal direction
- Data write  
Continuous write mode differs depending on the write mode specification. (RM1, RM2)
  - 1 Normal (RM2 = 0, RM1 = 0: initial state) \*Continuous mode not used\*  
-- COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 command wait state --
  - 2 Write continuous (RM2 = 0, RM1 = 1): Mode 2  
COM10-1 
  - 3 Write continuous (RM2 = 1, RM1 = 0): Mode 3  
COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 
  - 4 Write continuous (RM2 = 1, RM1 = 1): Mode 4  
COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 

\*: In modes 2, 3, and 4, the IC remains locked in continuous write mode until the  $\overline{\text{CS}}$  pin is set high.

- The write address is automatically incremented.
- The write address is retained unless the IC is reset or a new write address is issued.

## Color Table write

- Write start address specification

Use command 70 to set the color table write start address.

CTN1: Color table specification (No.1, No.2), CTA3 to 0: Address specification

No.1				No.2					
		R	G	B			R	G	B
Address	0000	XXX	XXX	XXX		0000	XXX	XXX	XXX
	0001					0001			
	0010					0010			
	1110					1110			
	1111					1111			

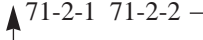
- Data write

Continuous write mode differs depending on the write mode specification. (RM3)

- 1 Normal (RM3 = 0: initial state) \*Continuous mode not used\*

-- COM71-1 71-2-1 71-2-2 command wait state ---

- 2 Write continuous (RM3 = 1) mode

COM71-1 

\*: In mode 2, the IC remains locked in continuous write mode until the  $\overline{\text{CS}}$  pin is set high.

- The write address is automatically incremented.
- The write address is retained unless the IC is reset or a new write address is issued.

**Display format**

## Color Specification Related Items

- When a character is specified

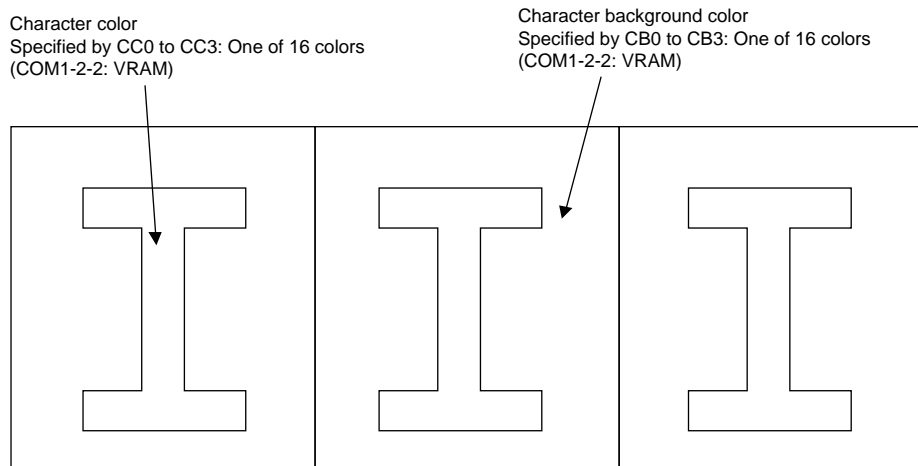
Specify color with the character color (character area) and character background color (outside the character area)

Character color: One of 16 colors

Character background color: One of 16 colors

Color tables: Table No. 1 or No. 2 specified by CT1 to CT0. (COM1-2-3: VRAM)

→ One of 32 types



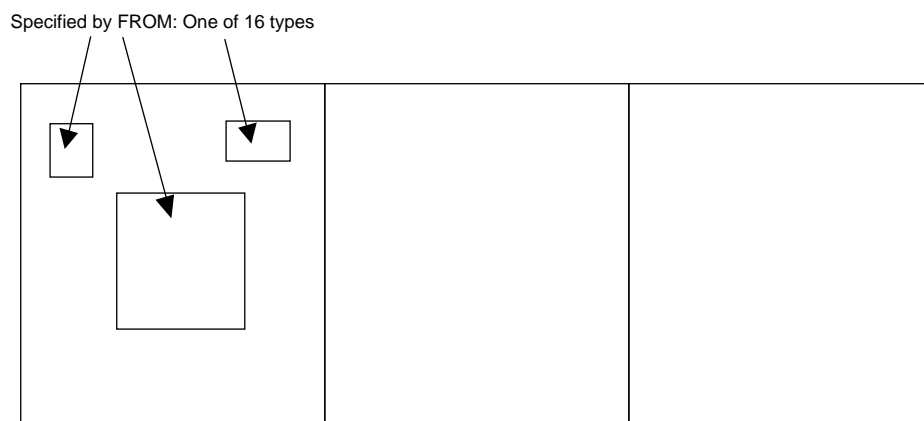
- When a graphic is specified

Specify color is in dot units ( $12 \times 18$  or  $12 \times 16$ )

One of 16 colors (FROM)

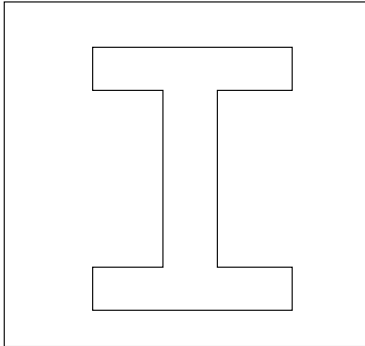
Color tables: Table No. 1 or No. 2 specified by CT1 to CT0. (COM1-2-3: VRAM)

→ One of 32 types



## Display Control Related Items

- Blinking: In character units  
Normal at1 = 0 (COM1-2-1: VRAM)

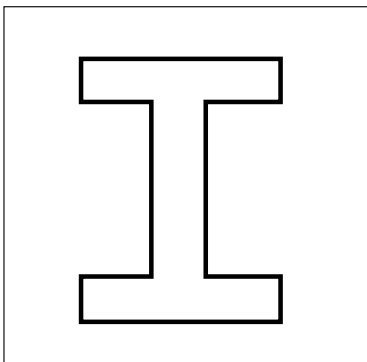


Blinking at1 = 1

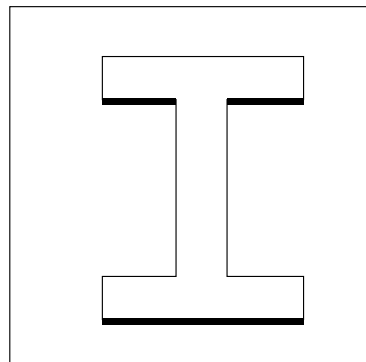
Display alternates between normal and transparent with the blinking period. (COM21-2: BK1, 0)

- Border display: Only valid for font specified characters  
Border color: One of 16 colors (COM60-2 EGC3 to 0)  
Color table specification (COM60-2 EGCT0)  
→ One of 32 types  
Border mode control (COM60-1 BLK1, 0)

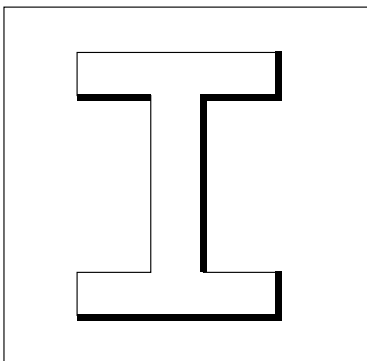
Border



Shadow 1: lower

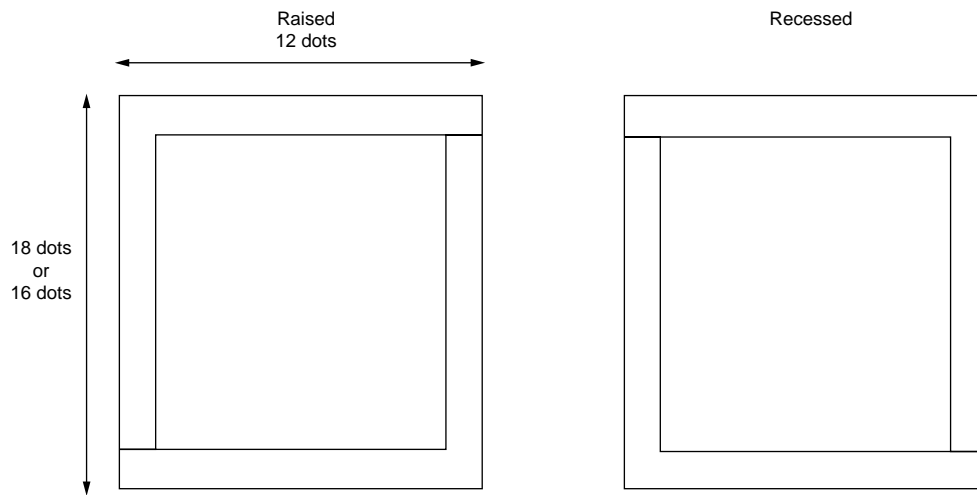


Shadow 2: lower + right



- Character size: Specified in line units  
The character size is specified as 1x to 4x independently for the vertical and horizontal directions.  
(COM40-2)

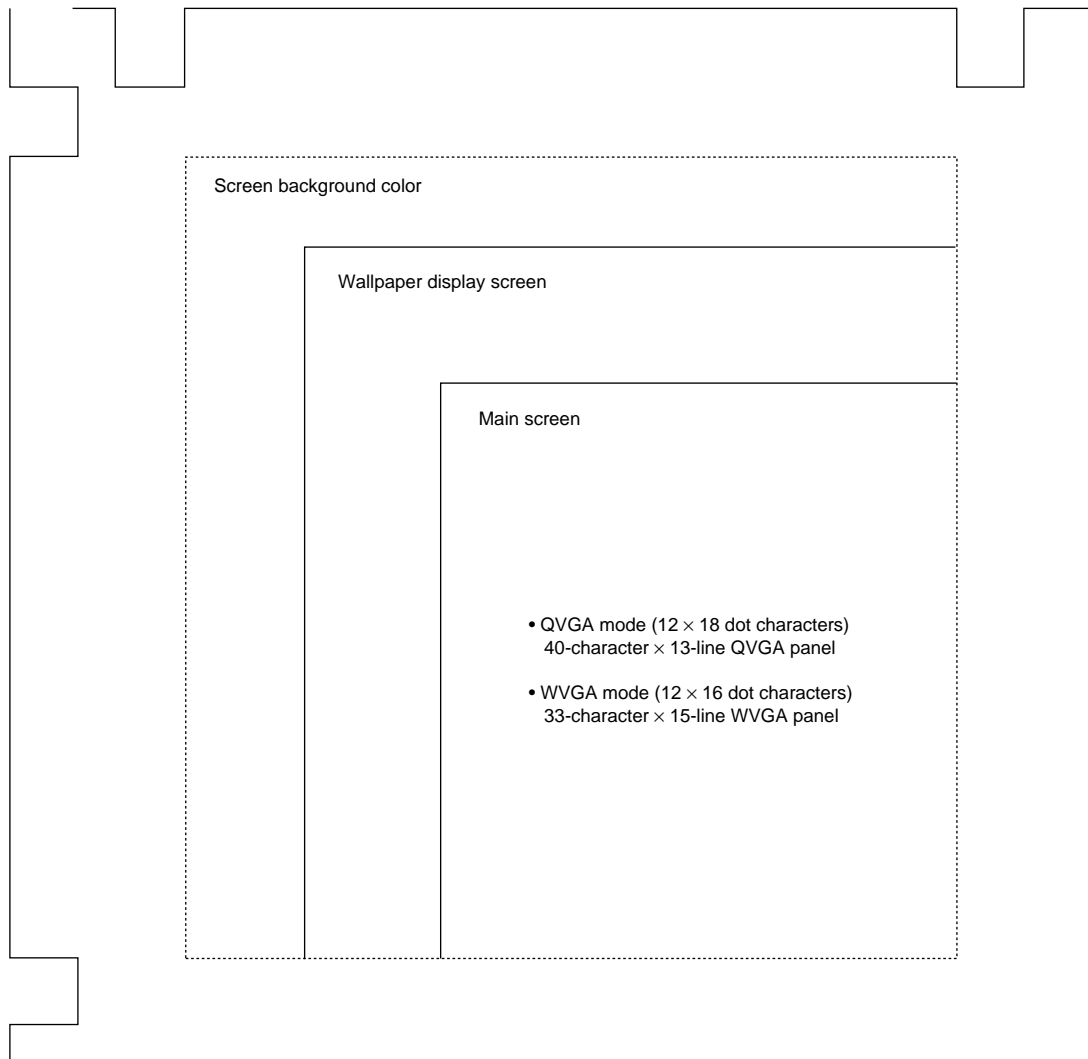
## Box Display (raised/recessed)



- Raised/recessed specification: In character units (COM10-2-1 BXS)
- Left side - displayed/undisplayed specification: in character units (COM10-2-1 BXL)
- Right side - displayed/undisplayed specification: in character units (COM10-2-1 BXR)
- Upper side - displayed/undisplayed specification: in character units (COM10-2-1 BXU)
- Lower side - displayed/undisplayed specification: in character units (COM10-2-1 BXD)
- Color specification: In line units
  - COM50 (Upper side)
  - COM51 (Lower side)
    - BXUC3:0: One of 16 colors
    - BXDC3:0: One of 16 colors
- Color table specification
  - BXUCT0
  - BXDCT0
  - ' One of 32 types
- Dot width specification: 1 or 2 dots
  - Each of left, right, upper, and lower can be specified independently. (BXLW BXRW BXUW BXDW)



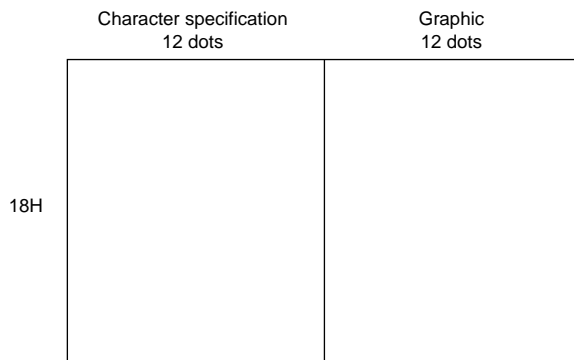
## Screen Structure



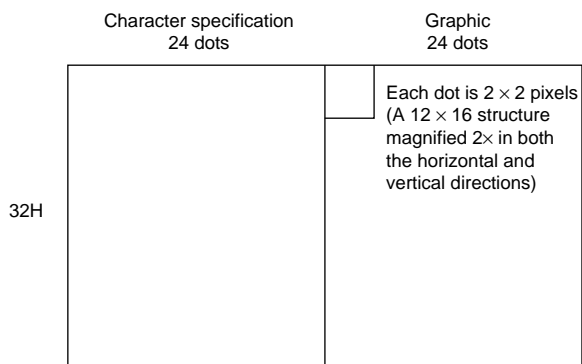
- For each screen: Display on/off (transparent) can be specified independently.
  - For each screen: The display start position can be specified independently.
- The wallpaper display screen and the main screen require xxxx clocks before the horizontal start position is reached.

## Display Format

- QVGA



- WVGA



## ROM structure

Internal ROM (512 characters)

- Character font

QVGA: 12 x 18-dot structure

WVGA: 24 x 32-dot structure, i.e. 12 x 16 times 4

- Graphics

CQVGA: 12 x 18-dot structure

WVGA: 12 x 16-dot structure, i.e. displayed magnified 2x in both the horizontal and vertical directions.

Note that the contents of ROM differ for QVGA and WVGA.

(That is, different ROMs for QVGA and WVGA must be created.)

External ROM (2048 characters)

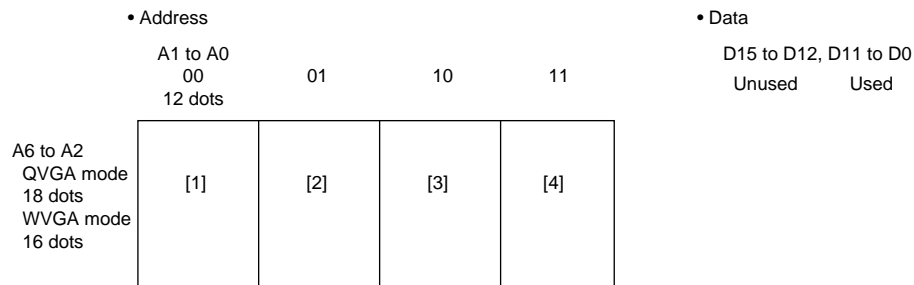
• Conditions

Use a 16-bit 4M ROM with an access time less than 3 times the dot clock period

Example: DCLK = 50 MHz = 20 ns period  $\times$  3 = under 60 ns

DCLK = 10 MHz = 100 ns period  $\times$  3 = under 300 ns

• ROM map



A17 to A7 (10 bits) = 2048 characters = character codes

• Display appearance

QVGA: 1 character =  $12 \times 18$  dots

Character font: [1]

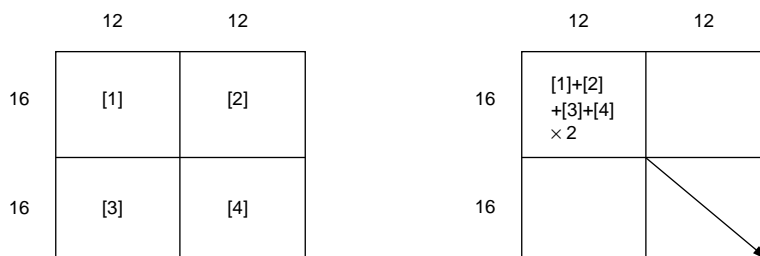
Graphics: [1] + [2] + [3] + [4]

WVGA: 1 character =  $12 \times 16$  dots

Character font: [1] [2]

[3] [4]

Graphics: ([1] + [2] + [3] + [4]) displayed magnified  $2\times$  in both the horizontal and vertical directions.



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