

SANYO**LA4587M****Preamplifier + Power Amplifier
for 1.5 V Headphone Stereos****Overview**

The LA4587M is a system IC that includes all of the necessary functions for a playback set on a single chip, reducing the number of external components needed.

Functions

- Stereo preamplifier (supports auto reverse function, switchable between metal and normal tape)
- Stereo power amplifier (OCL, mute function)
- Ripple filter
- Low boost function (BTL operation in low-frequency range)
- AMSS (Automatic Music Select System)
- Power switch

Features

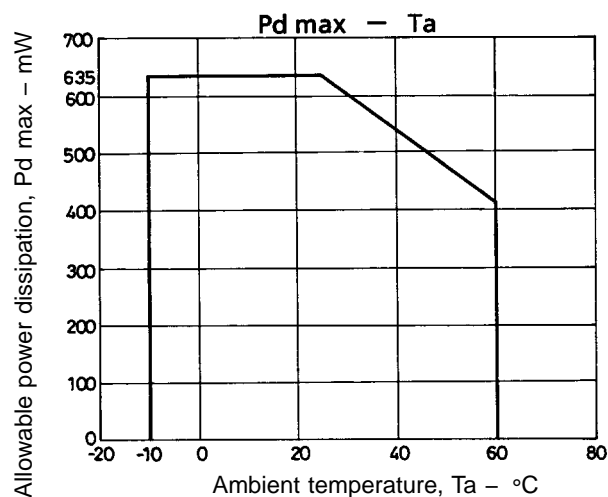
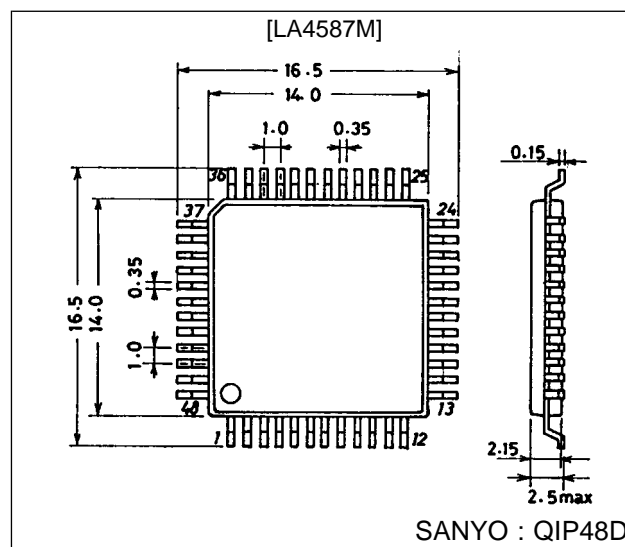
- Preamplifier has a high open-loop gain ($V_{GO} = 73$ dB).
- Preamplifier requires no NF capacitor.
- Virtual ground capacitor can be 1 μ F or less. (Lower impedance is achieved by having a V_{REF} amplifier built in.)
- Ripple filter requires no capacitor for preventing oscillation.
- Powerful output is obtained in low boost output ($P_o = 21$ mW/ $V_{CC} = 1.2$ V, $f = 100$ Hz).
- A high-frequency cutoff capacitor is built into the preamplifier and power amplifier inputs; anti-buzz provision.

Specifications**Maximum Ratings at $T_a = 25^\circ\text{C}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		3.0	V
Allowable power dissipation	P_d max		635	mW
Operating temperature	T_{opr}		-10 to +60	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Package Dimensions

unit : mm

3102-QFP48D

LA4587M

Operating Conditions at $T_a = 25^\circ\text{C}$

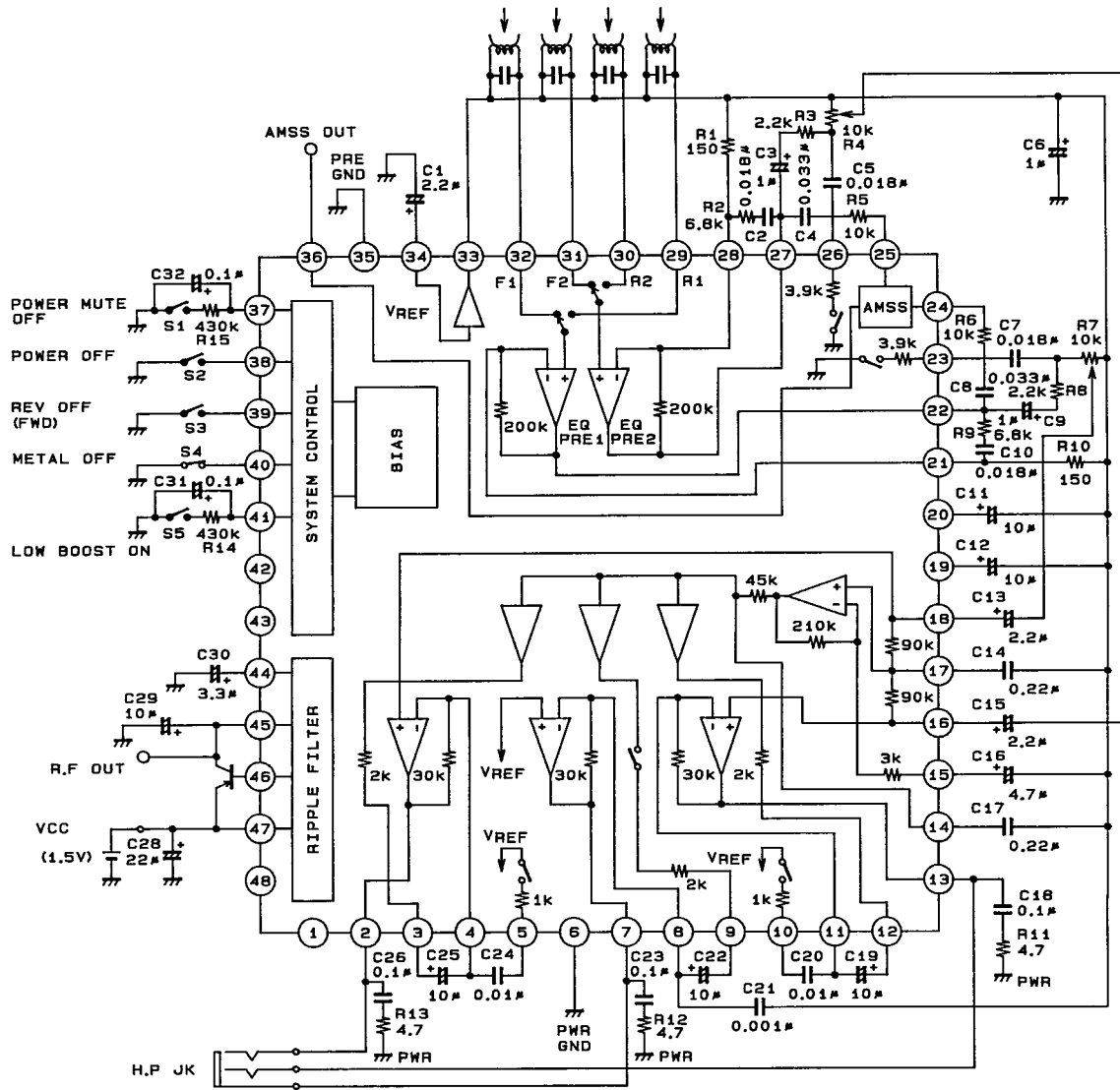
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		1.5	V
Operating supply voltage range	$V_{CC\text{ op}}$		0.95 to 2.2	V

Operation Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 1.2\text{ V}$, $f = 1\text{ kHz}$, $0.775\text{ V} = 0\text{ dBm}$, $R_L = 10\text{ k}\Omega$ (preamplifier), $R_L = 16\text{ }\Omega$ (power amplifier)

Parameter	Symbol	Conditions	min	typ	max	Unit
[Preamplifier + Power Amplifier]						
Quiescent current	I_{CCO1}	$R_g = 2.2\text{ k}\Omega$, $R_v = 0\text{ }\Omega$	8	15	24	mA
	I_{CCO2}	When power switch is off		0.1	5	μA
Voltage gain (closed)	V_{GT}	$V_O = -20\text{ dBm}$, $R_V = 10\text{ k}\Omega$	54	57	60	dB
[Preamplifier]						
Voltage gain (open)	V_{G0}	$V_O = -20\text{ dBm}$	60	73		dB
Voltage gain (closed)	V_{G1}	$V_O = -20\text{ dBm}$	34	35.5	37	dB
	V_{G2}	$V_O = -20\text{ dBm}$, $f = 10\text{ kHz}$, metal on	25.5	28	30.5	dB
Maximum output voltage	$V_{O\text{ max}}$	THD = 1 %	100	210		mV
Total harmonic distortion	THD ₁	$V_G = 35.5\text{ dB/NAB}$, $V_O = 100\text{ mV}$		0.1	0.5	%
Equivalent input noise voltage	V_{NI}	$R_g = 2.2\text{ k}\Omega$, BPF: 20 Hz to 20 kHz		1.3	3.0	μV
Interchannel crosstalk	CT ₁	$R_g = 2.2\text{ k}\Omega$, 1 kHz TUNE, $V_O = -20\text{ dBm}$	45	56		dB
Interchannel crosstalk between F and R	CT ₂	$R_g = 2.2\text{ k}\Omega$, 1 kHz TUNE, $V_O = -20\text{ dBm}$	65	78		dB
Ripple rejection ratio	Rr ₁	$R_g = 2.2\text{ k}\Omega$, $V_r = -30\text{ dBm}$, fr = 100 Hz, 100 Hz TUNE	45	52		dB
[Low Boost + Power Amplifier]						
Voltage gain (closed)	V_{G3}	$V_O = -20\text{ dBm}$	20.5	23	25.5	dB
	V_{G4}	$V_O = -20\text{ dBm}$, L.B. = on	20.5	23	25.5	dB
	V_{G5}	$V_O = -20\text{ dBm}$, L.B. = on, $f = 10\text{ kHz}$	24.5	27.5	30.5	dB
	V_{G6}	$V_O = -20\text{ dBm}$, L.B. = on, $f = 100\text{ Hz}$	30	34	38	dB
Output power	P _{O1}	THD = 10 %	5	9		mW
	P _{O2}	THD = 10 %, $f = 100\text{ Hz}$, L.B. = on	13	21		mW
Total harmonic distortion	THD ₂	$P_O = 1\text{ mW}$		0.5	1.5	%
Interchannel crosstalk	CT ₃	$V_O = -20\text{ dBm}$, $R_V = 0\text{ }\Omega$	38	43		dB
Output noise voltage	V_{NO}	$R_V = 0\text{ }\Omega$, BPF: 20 Hz to 20 kHz		35	48	μV
Ripple rejection ratio	Rr ₂	$R_V = 0\text{ }\Omega$, $V_r = -30\text{ dBm}$, fr = 100 Hz, 100 Hz TUNE	50	74		dB
Output mute voltage	V_M	$V_{IN} = -30\text{ dBm}$, 1 KHz TUNE, mute on			-85	dBm
Input resistance	R _i		8	10	12	k Ω
Voltage gain difference	ΔV_{G3}			0	+1.5	dB
[Ripple Filter]						
Ripple rejection ratio	Rr ₃	fr = 100 Hz, $V_r = -30\text{ dBm}$, $V_{CC} = 1.0\text{ V}$, $I_{RF} = 25\text{ mA}$, 2SB1295, h _{FE} 6 rank used	33	39		dB
Output voltage	V_{RF}	$V_{CC} = 1.0\text{ V}$, $I_{RF} = 25\text{ mA}$	0.89	0.93		V
[AMSS]						
Operating output voltage	V_{OAMSS}	Preout voltage when AMSS $V_O = 0.6\text{ Vp-p}$ Pin 34 is short-circuited through 270 k Ω .	1.80	2.55	3.60	mV

Note: L.B. = Low boost

Sample Application Circuit

Unit (resistance: Ω , capacitance: F)

A04505

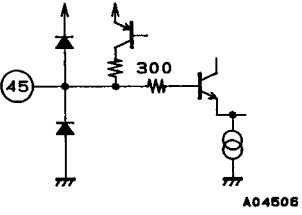
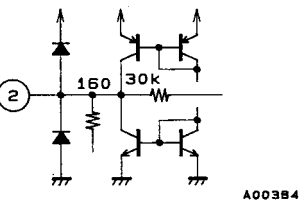
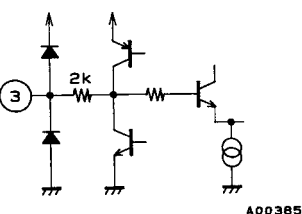
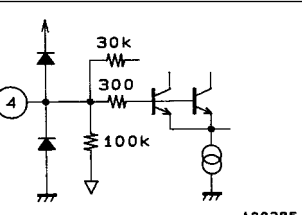
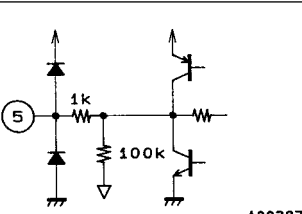
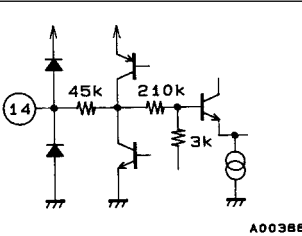
Note 1: Transistors equivalent to the 2SB1295 with $h_{FE}6$ rank and upward are recommended.

Note 2: C18, C23, and C26 are oscillation prevention capacitors; a polyester film or ceramic capacitor (which can guarantee the specified capacitance at operating temperatures) is recommended.

Pin Functions

Unit (resistance:Ω, capacitance: F)

* Pin voltage is when $V_{CC} = 1.2\text{ V}$

Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
45	R.F OUT	1.13		
2 7 13	POWER OUT1 POWER OUTC POWER OUT2	0.6		<ul style="list-style-type: none"> A 160 Ω resistor is connected between individual outputs (between pins 2 and 7, and between pins 13 and 7).
3 9 12	POWER NF REF1 POWER NF REFC POWER NF REF2	0.75		<ul style="list-style-type: none"> Each power NF connection
4 8 11	POWER NF1 POWER NFC POWER NF2	0.75		<ul style="list-style-type: none"> Each power NF connection.
5 10	POWER H.P1 POWER H.P2	0.75		<ul style="list-style-type: none"> Grounded to V_{REF} through a 1 kΩ resistor when low boost is on (pin 41: floating).
14	L.P2	0.75		<ul style="list-style-type: none"> Low boost secondary LP connection.

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Unit (resistance: Ω , capacitance: F)

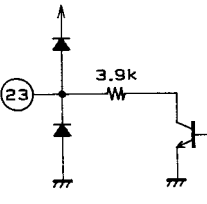
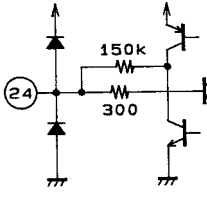
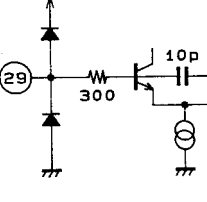
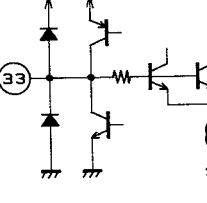
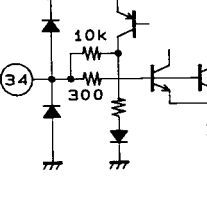
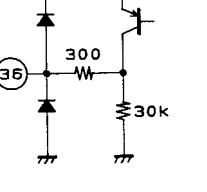
Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
15	Low Boost NF	0.75		<ul style="list-style-type: none"> Low boost amplifier NF connection.
16 18	POWER IN2 POWER IN1	0.75		<ul style="list-style-type: none"> Each power input connection. The input resistance is 10 kΩ. An anti-buzz capacitor is built in.
17	L.P1	0.75		<ul style="list-style-type: none"> Low boost primary LP connection.
19 20	NFC2 NFC1	0.75		
21 28	PRE NF1 PRE NF2	0.75		<ul style="list-style-type: none"> Each preamplifier NF connection. NF requires no capacitor.
22 27	PRE OUT1 PRE OUT2	0.45		<ul style="list-style-type: none"> 200 kΩ is connected between each output pin and NF pin.

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Unit (resistance: Ω , capacitance: F)

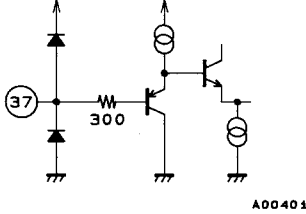
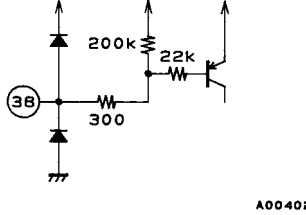
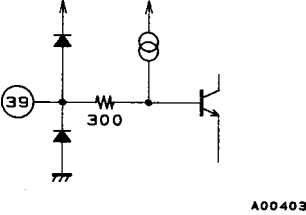
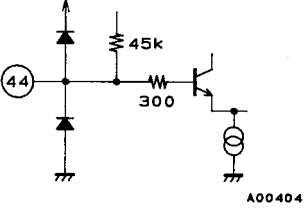
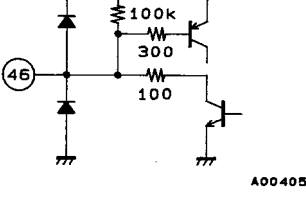
Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
23 26	METAL1 METAL2	0	 <p>A00395</p>	<ul style="list-style-type: none"> Connected to GND through 3.9 kΩ in metal on mode (pin 40: floating)
24 25	AMSS IN1 AMSS IN2	0.75	 <p>A00396</p>	<ul style="list-style-type: none"> AMSS inverting input connection. An external input resistor is required.
29 30 31 32	PRE REV IN1 PRE REV IN2 PRE FWD IN2 PRE FWD IN1	0.75	 <p>A00397</p>	<ul style="list-style-type: none"> Pins 29 and 30 turn on in REV mode (pin 39: GND). Pins 31 and 32 turn on in FWD mode (pin 39: floating) When not using the head, a bias resistor (2.2 kΩ) is required between these pins and V_{REF} (pin 33). An anti-buzz capacitor is built in.
33	V_{REF}	0.75	 <p>A00398</p>	<ul style="list-style-type: none"> V_{REF} amplifier output. Low impedance is achieved due to the output resistor ($r_o = 10 \Omega$). Inflow/outflow current: 200 μA max.
34	REF	0.75	 <p>A00399</p>	<ul style="list-style-type: none"> The V_{REF} amplifier is referenced hereto.
36	AMSS OUT		 <p>A00400</p>	<ul style="list-style-type: none"> Outputs a pulse waveform in accordance with the AMSS IN (pins 24 and 25) input level.

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Unit (resistance: Ω , capacitance: F)

Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
37 41	POWER MUTE SW Low Boost SW		 <p>A00401</p>	<ul style="list-style-type: none"> When pin 37 is grounded, mute is on. When pin 41 is floating, low boost is on.
38	POWER SW		 <p>A00402</p>	<ul style="list-style-type: none"> Power on when grounded.
39 40	FWD/REV SW METAL SW		 <p>A00403</p>	<ul style="list-style-type: none"> When pin 39 is floating: FWD mode; when grounded: REV mode. When pin 40 is in FL mode: metal on.
44	R.F REF	1.13	 <p>A00404</p>	<ul style="list-style-type: none"> RF is referenced hereto. An external capacitor can be used to vary RF SVRR.
46	R.F BASE	0.5	 <p>A00405</p>	<ul style="list-style-type: none"> Used for external PNP transistor base drive.

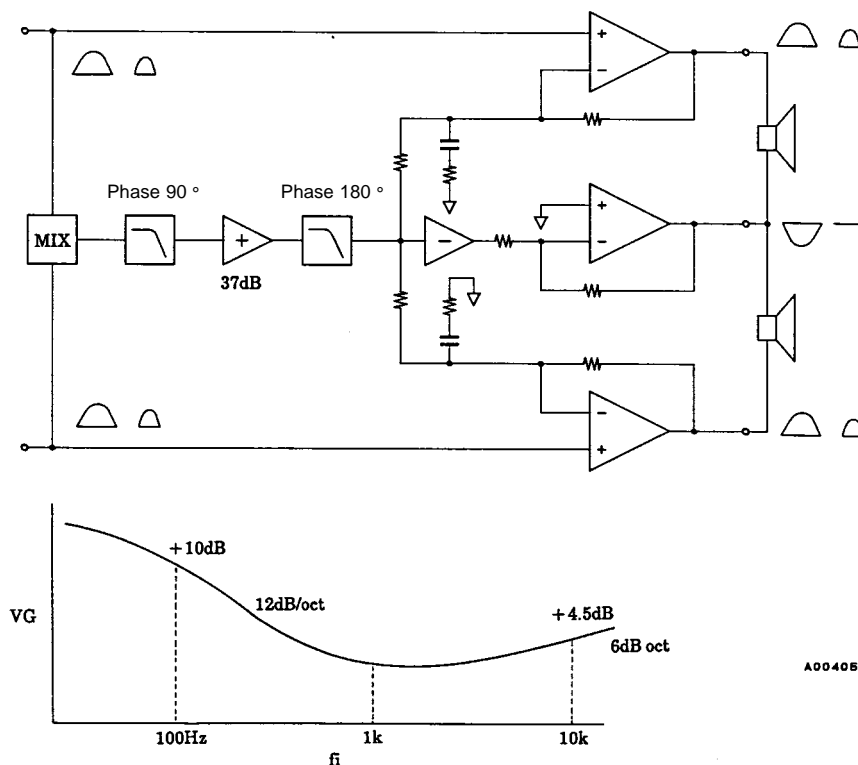
Description of External Components

- C_1 (1.0 to 10 μF): V_{REF} amplifier is referenced to this decoupling capacitor.
The V_{REF} SVRR depends on the value of this capacitor.
Note that if the capacitance is reduced, the SVRR worsens.
- C_2, C_{10} : Playback preamplifier EQ constant.
- C_3, C_9 (0.47 to 3.3 μF): Preamplifier output capacitor.
- C_4, C_8 : AMSS input HPF capacitor.
- C_5, C_7 : EQ constant for metal (built-in resistance 3.9 $\text{k}\Omega \pm 15\%$).
- C_6 (0.1 to 22 μF): V_{REF} decoupling capacitor.
For high-frequency noise rejection.
- C_{11}, C_{12} (3.3 to 10 μF): NFC decoupling capacitor.
Note that if the capacitance is reduced, the preamplifier low-frequency gain decreases.
- C_{13}, C_{15} (1.0 to 3.3 μF): Power amplifier input capacitor (Input resistance: 10 $\text{k}\Omega$).
- C_{14}, C_{17} : Capacitor for low boost LPF.
The low boost gain depends on the capacitance.
- C_{16} (1.0 to 4.7 μF): Boost amplifier NF capacitor.
Note that if the capacitance is reduced, the low boost low-frequency gain decreases.
- C_{18}, C_{23}, C_{26} (0.1 to 1.0 μF): Oscillation blocking capacitor.
- C_{19}, C_{22}, C_{25} (3.3 to 10 μF): Power amplifier NF capacitor.
Note that if the capacitance is reduced, the power amplifier low-frequency gain decreases.
- C_{20}, C_{24} : Bass high boost capacitor.
The high gain depends on the capacitance.
- C_{21} (100 to 2200 pF): Oscillation blocking capacitor.
- C_{29} (4.7 to 10 μF): RF output decoupling capacitor. (Also serves as the power supply capacitor and the oscillation blocking capacitor.)
- C_{28} (22 to 220 μF): Power supply capacitor.
- C_{30} (2.2 to 10 μF): RF is referenced to this LPF capacitor.
The RF SVRR depends on the capacitance.
- C_{31}, C_{32} (0.047 to 0.22 μF): Switching circuit smoothing capacitor. Must be adjusted according to the set timing.
- R_1, R_{10} : For preamplifier gain adjustment.
- R_2, R_9 : Playback preamplifier EQ constant.
- R_3, R_8 : EQ constant for metal.
- R_4, R_7 : 10 $\text{k}\Omega$ volume control.
- R_5, R_6 : For AMSS gain adjustment and HPF.
- R_{11}, R_{12}, R_{13} : For oscillation blocking.
- R_{14}, R_{15} (100 to 430 $\text{k}\Omega$): For switching circuit smoothing (discharge resistors).

Operation Description

- Low boost system

Low-frequency region amplification: 12 dB/oct, high-frequency region amplification: 6 dB/oct.



- Note on low boost

The signals that are applied to each power input are mixed and then passed through a two-stage LPF. Because the signal levels are attenuated by the LPF, level compensation is accomplished by amplifying the signals through a low boost amplifier located in between. The phase of signals that pass through the secondary LPF is inverted relative to the input signal; these signals are then input to each power amplifier.

- Note on channels 1 and 2

The positive phase signals that were input from the positive (“+”) input pins and the reverse phase signals that were input from the negative (“-”) input pins and then were passed through the secondary LPF are all input, amplified, and then output.

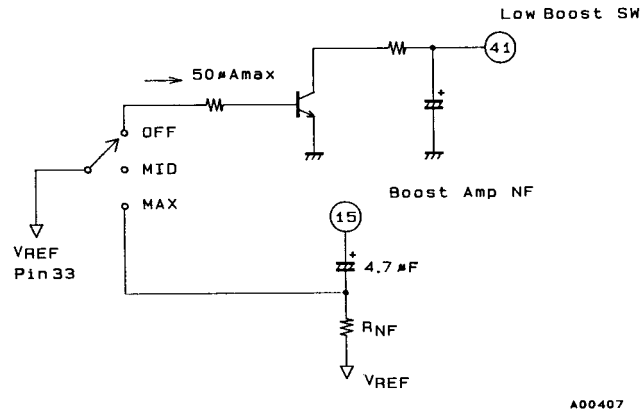
- Note on the common amplifier

The phase of the signals that passed through the secondary LPF is inverted by the inverting amplifier; the signals (with reversed phases relative to channels 1 and 2) are then input to the negative (“-”) inputs. The positive (“+”) input signals are grounded to V_{REF} , amplified by the inverting amplifier and then output.

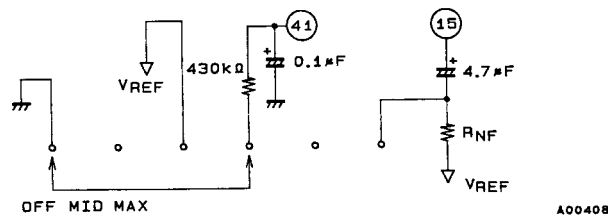
The phase of the channel 1 and 2 amplifier outputs and the common amplifier outputs are made to oscillate with inverted phases, making it possible to obtain the dynamic range efficiently.

Sample Application Circuits for Low Boost Switching

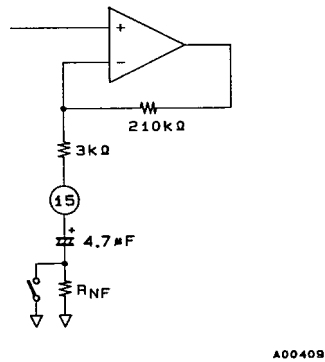
Sample 1



Sample 2

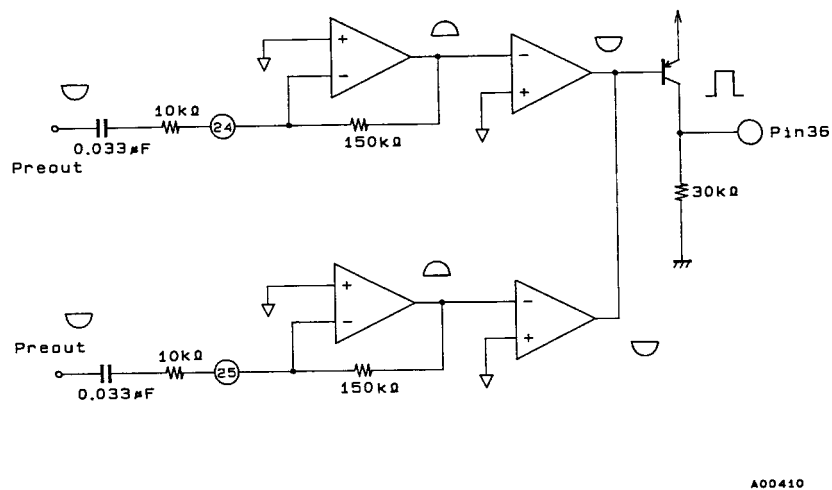


In the above circuits, MID and MAX are switched by changing the gain of the boost amplifier.



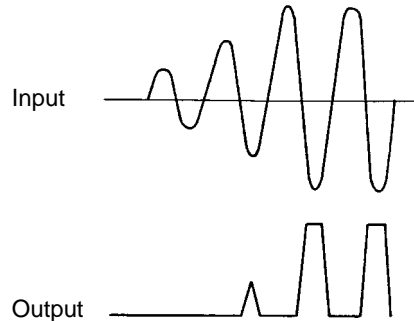
The AMSS comparator

Block Diagram



Operation Description

- The input amplifiers are inverting amplifiers. The gain and HPF characteristics can be adjusted through an external C-R (input impedance).
- The AMSS comparator outputs pulses for an input waveform that satisfies certain set conditions (frequency and voltage level).



- When AMSS is not used, the input pins (pins 24 and 25) are connected to V_{REF} (pin 33).

Notes on the ripple filter

- The RF SVRR can be adjusted by an external capacitor connected to pin 44.

3.3 μF \rightarrow 39 dB

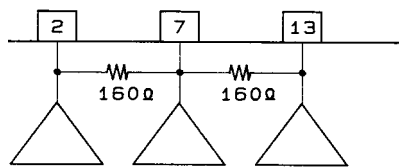
4.7 μF \rightarrow 42 dB

10 μF \rightarrow 47 dB

- It is recommended that external transistors be equivalent to the 2SB1295 with h_{FE} 6 rank and upward.

Note on power output

- The power amplifier output and the common amplifier output are connected by a resistor of approximately 160 Ω .



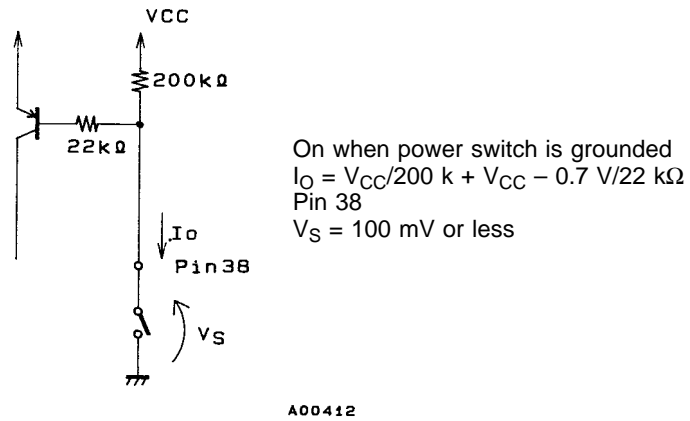
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Notes on power mute

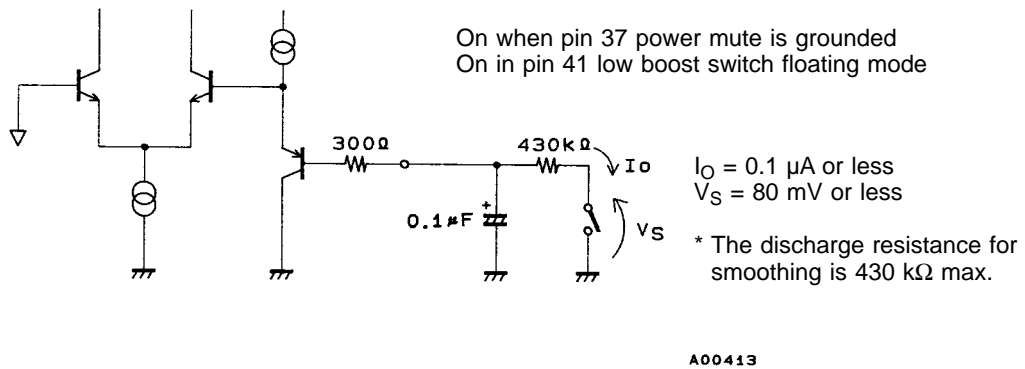
- Power mute turns off the fixed current that is supplied to the power section.
- The output DC when power mute is on is the V_{REF} electric potential (0.75 V).
- The output impedance when power mute is on is approximately 10 k Ω .

SW Pin Equivalent Circuit Diagram

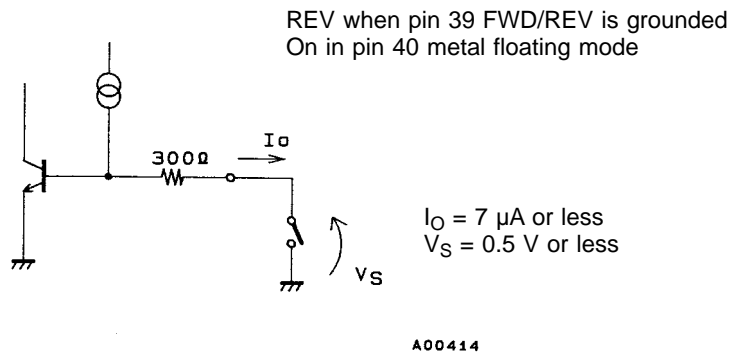
1. Power switch

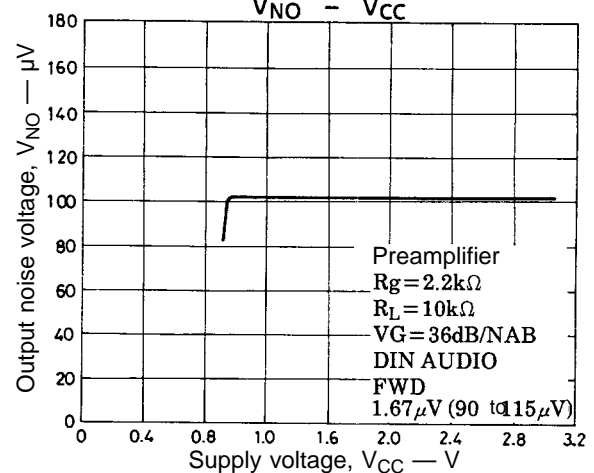
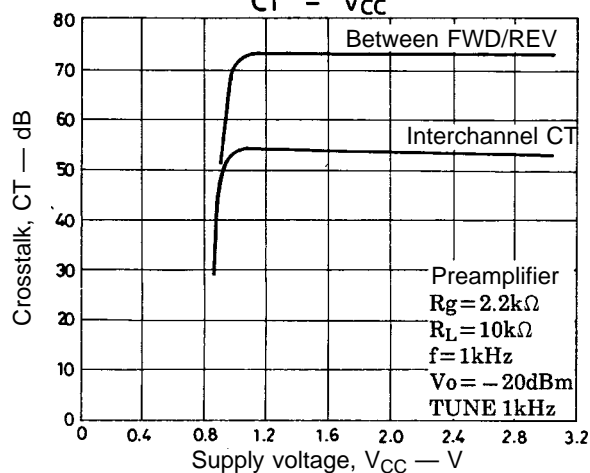
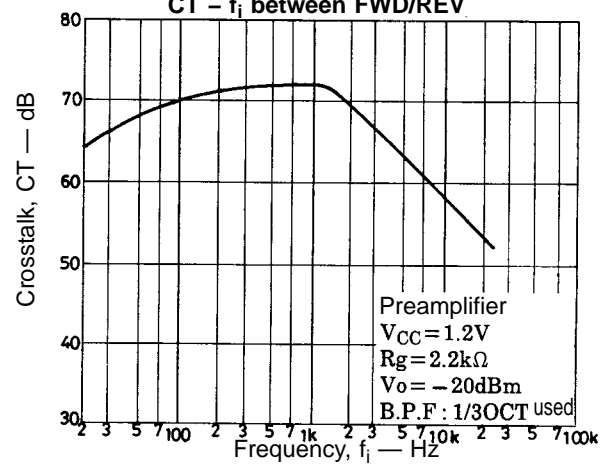
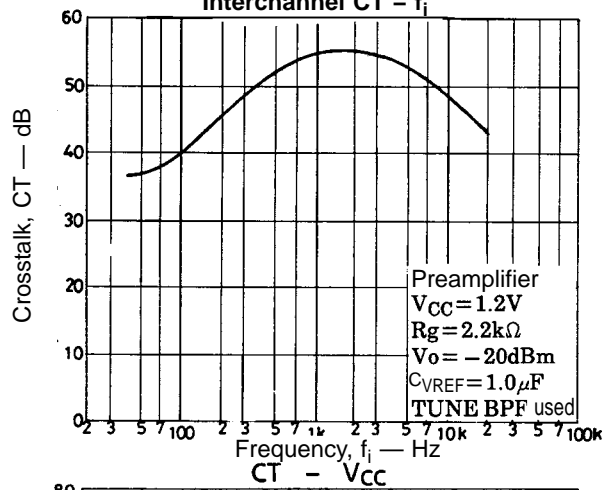
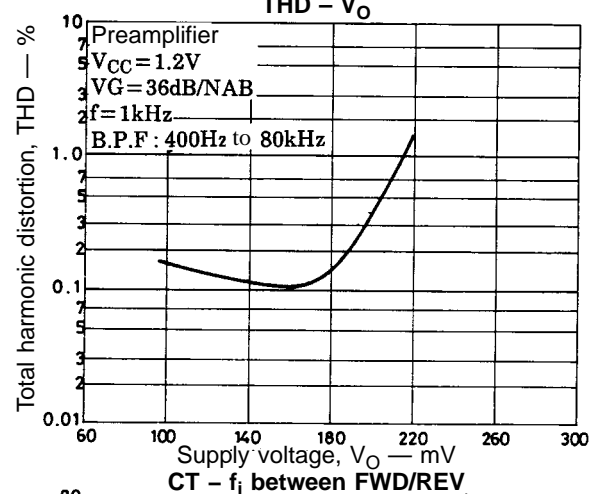
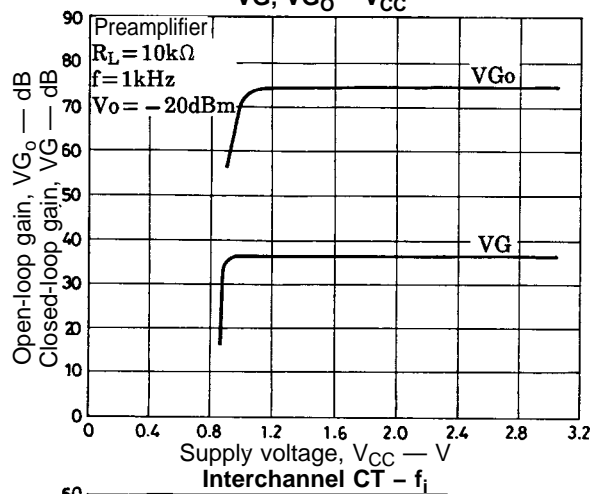
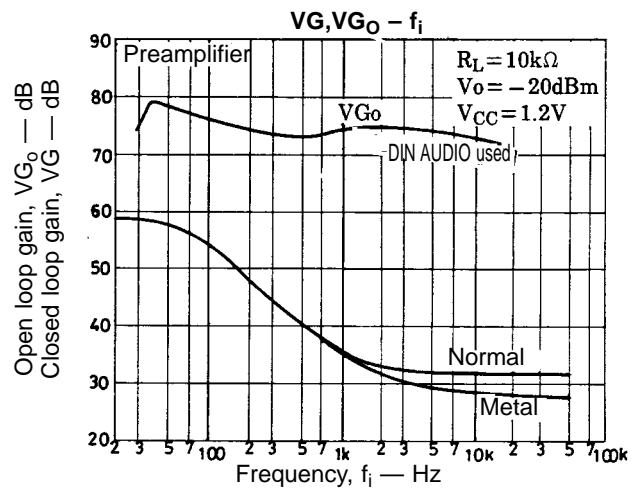
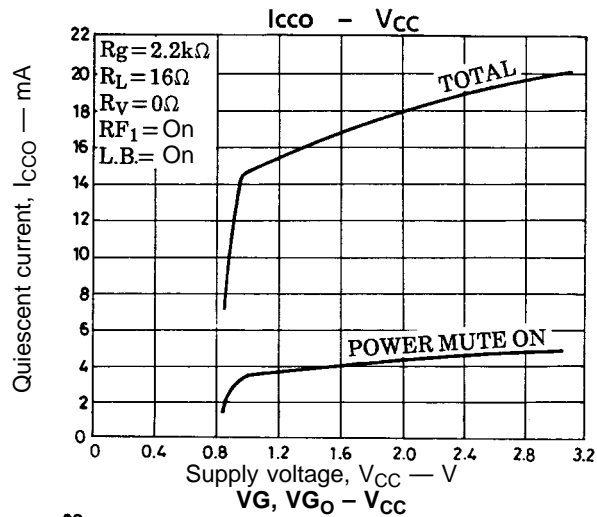


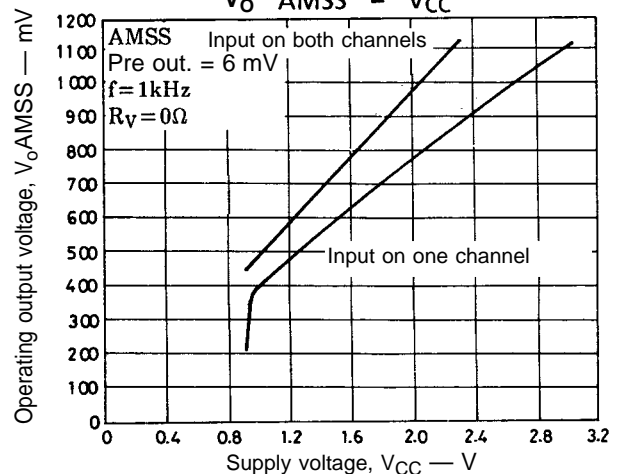
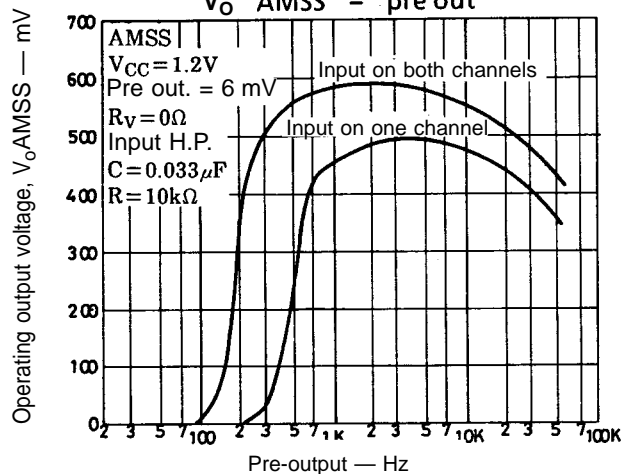
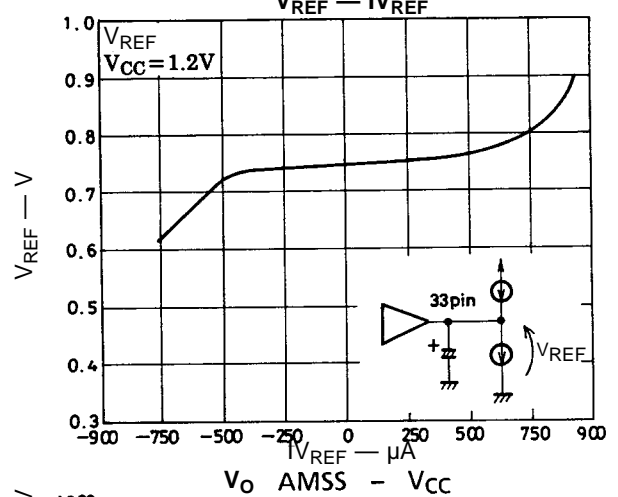
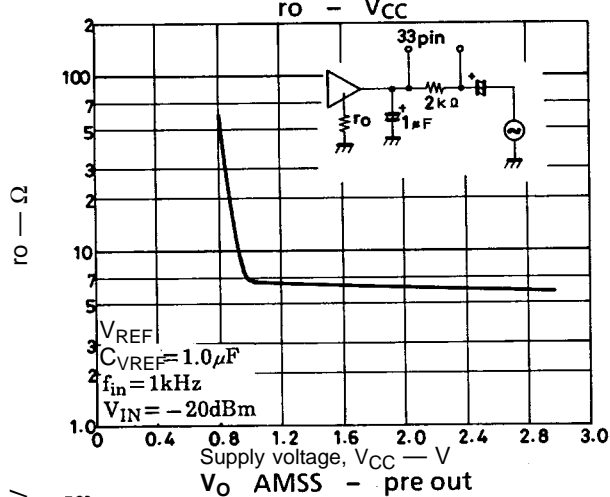
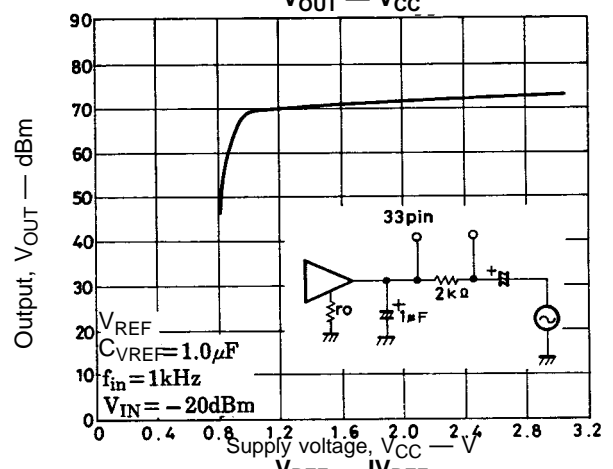
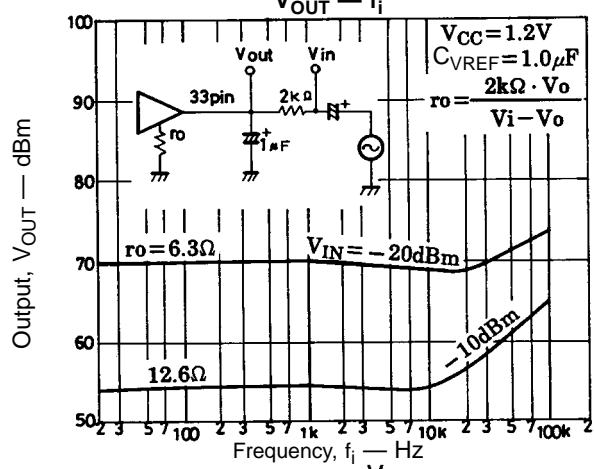
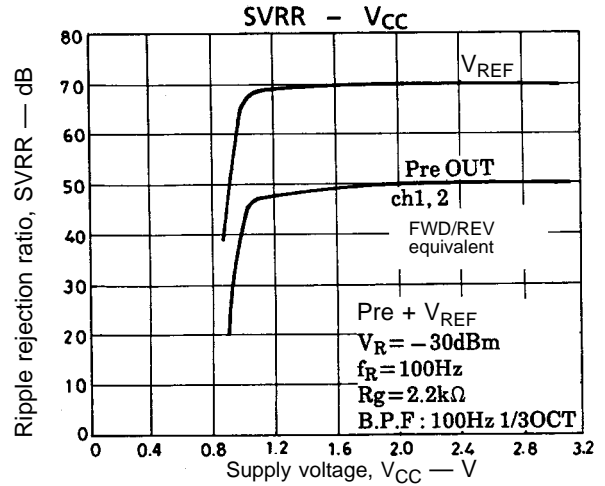
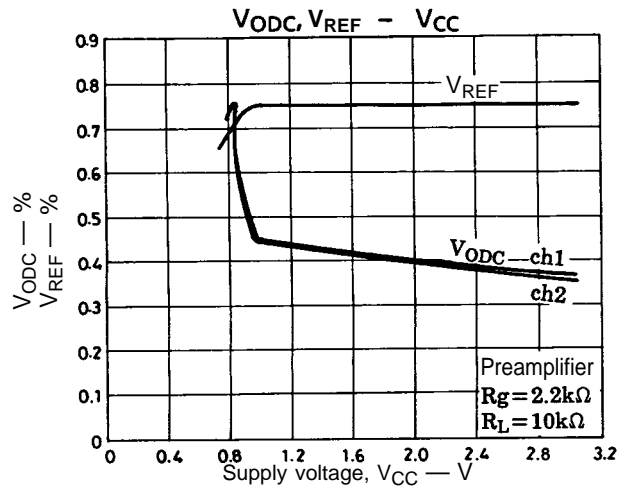
2. Power mute and low boost switch

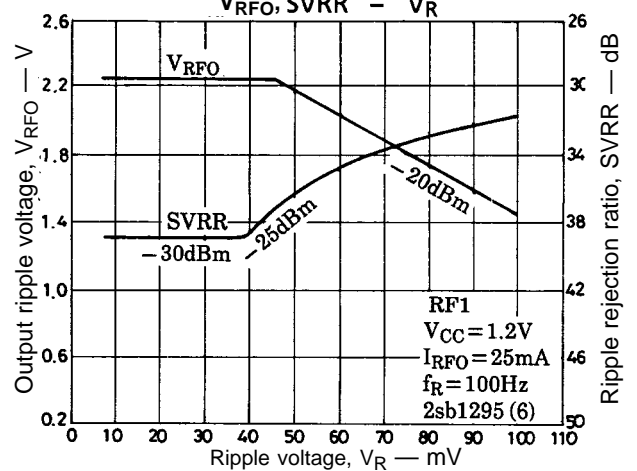
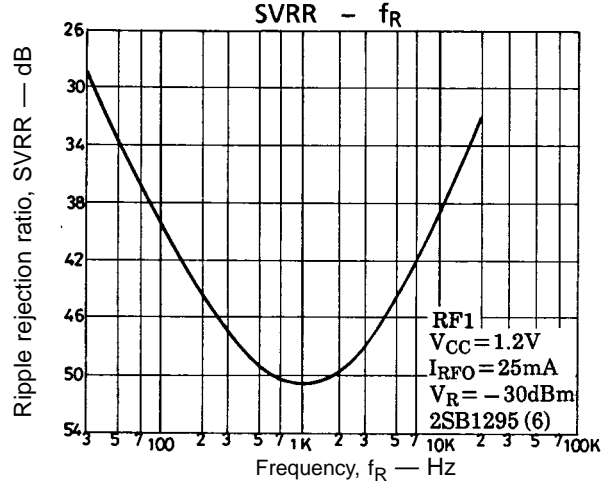
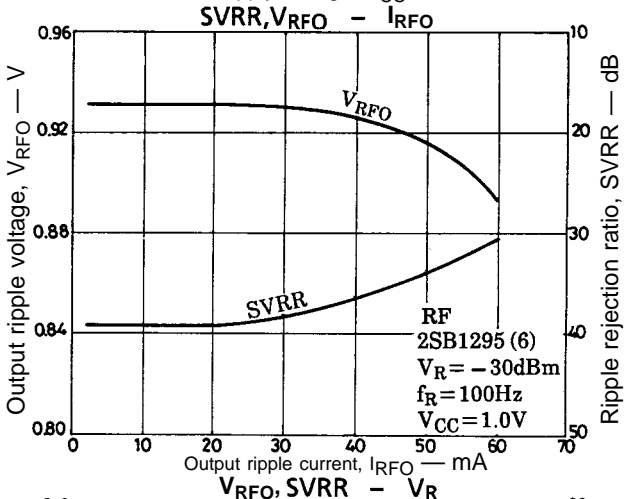
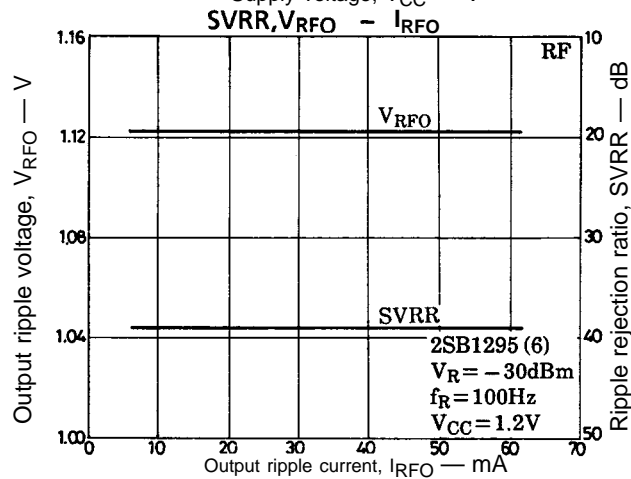
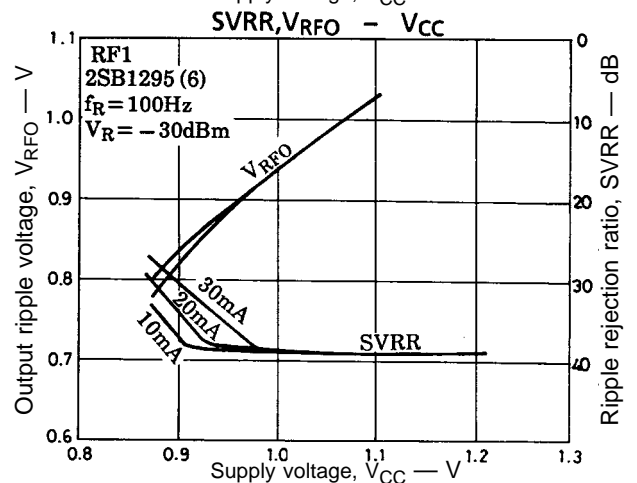
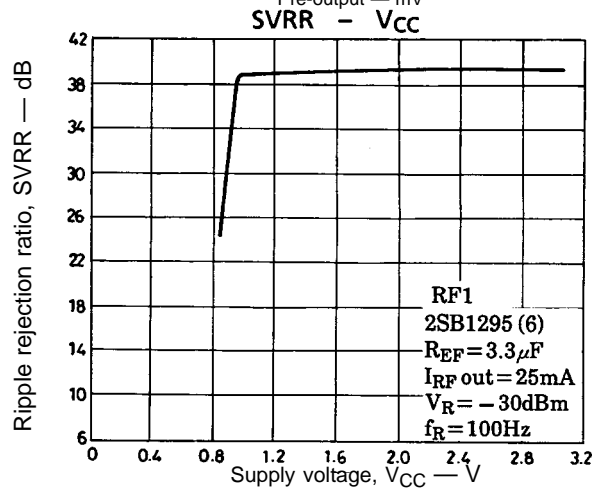
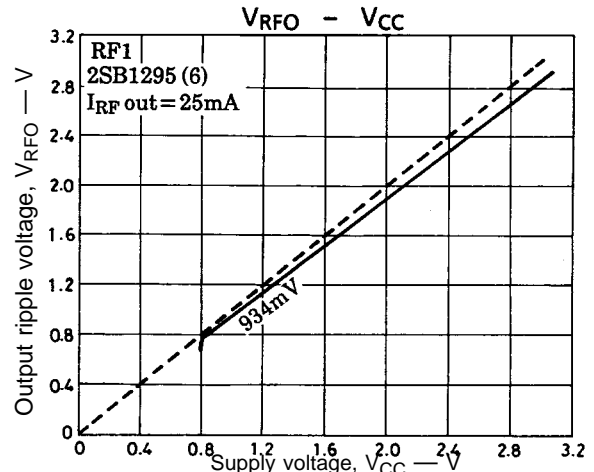
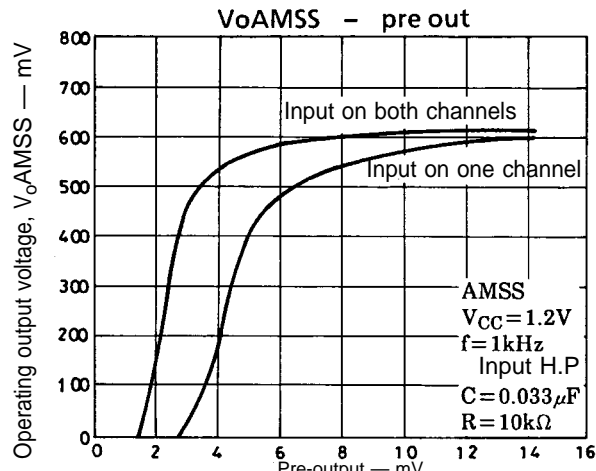


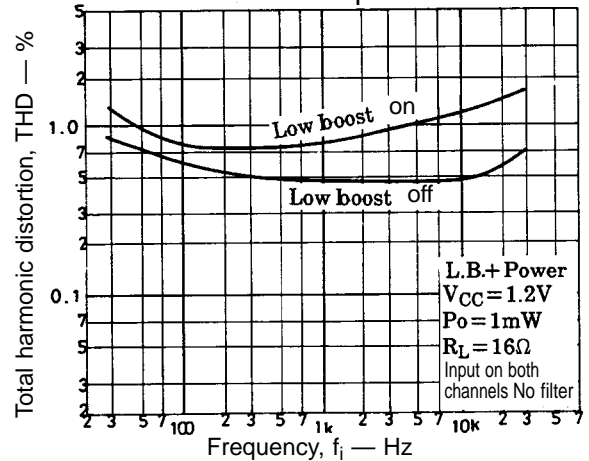
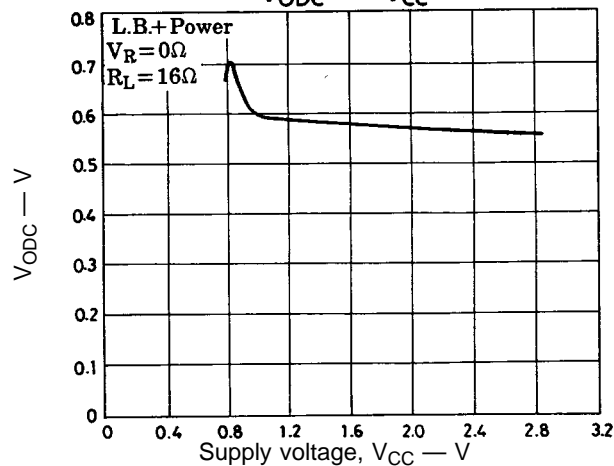
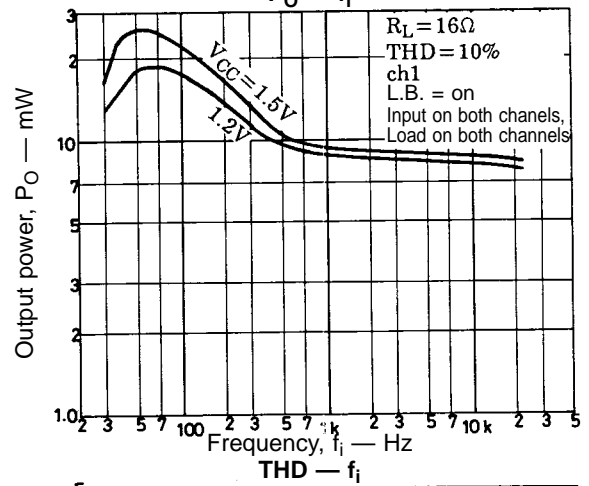
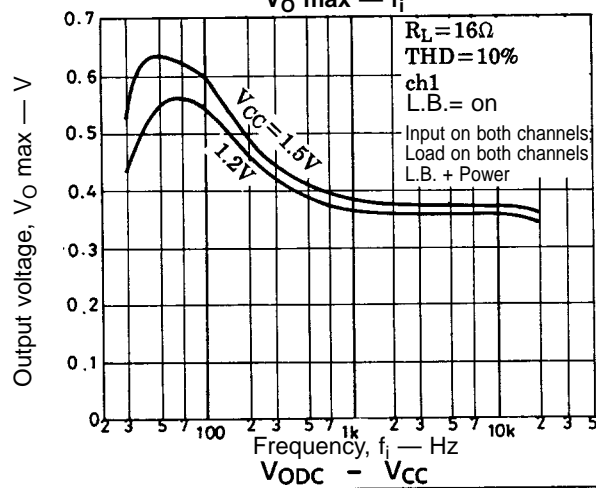
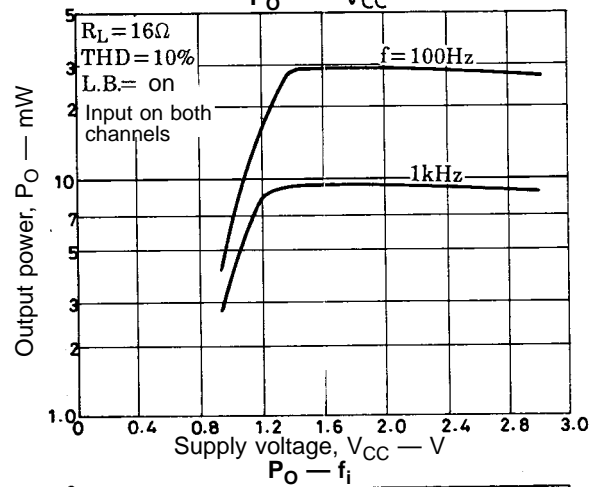
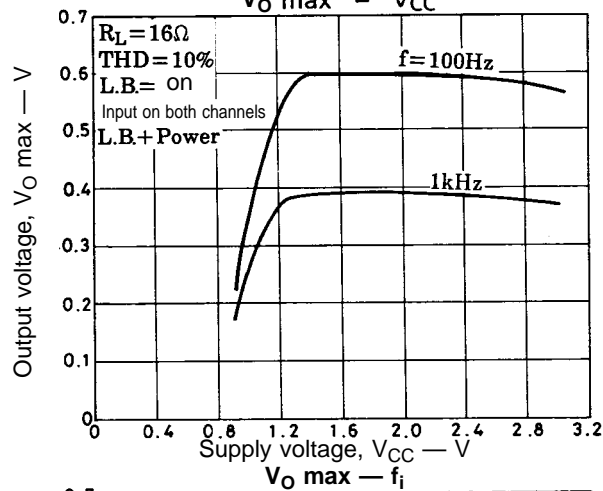
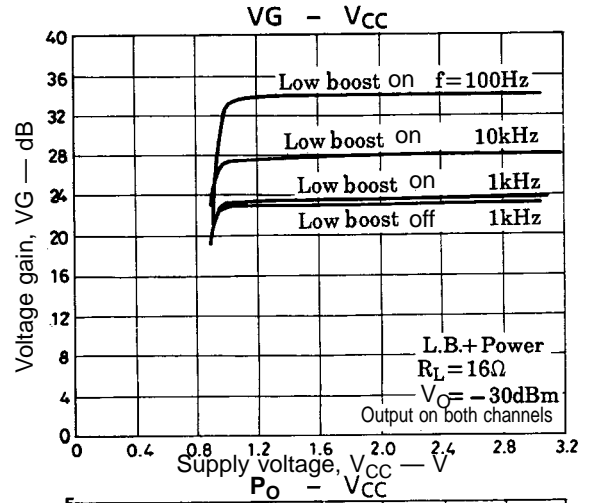
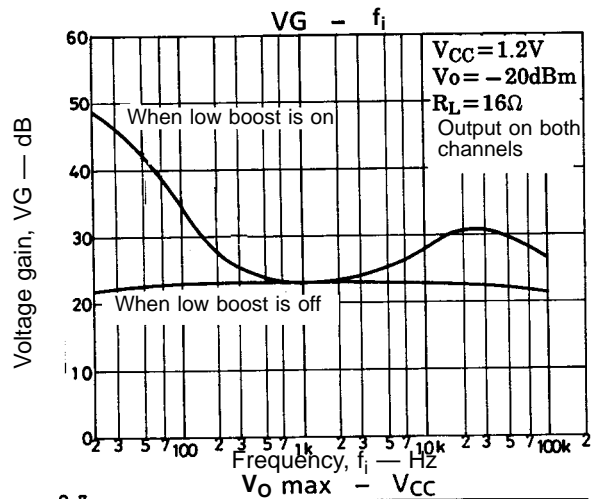
3. FWD/REV, METAL switch

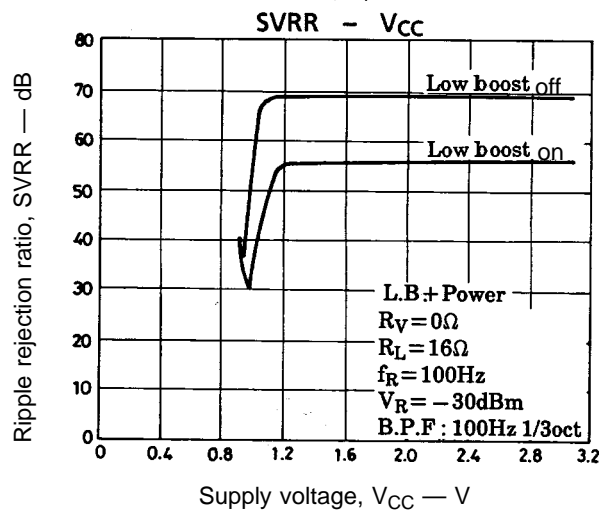
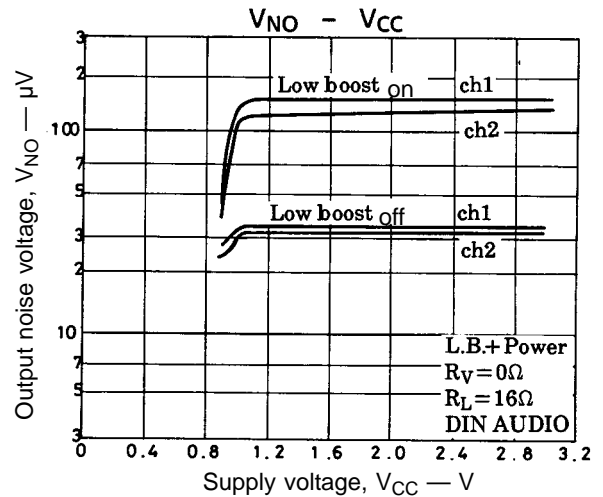
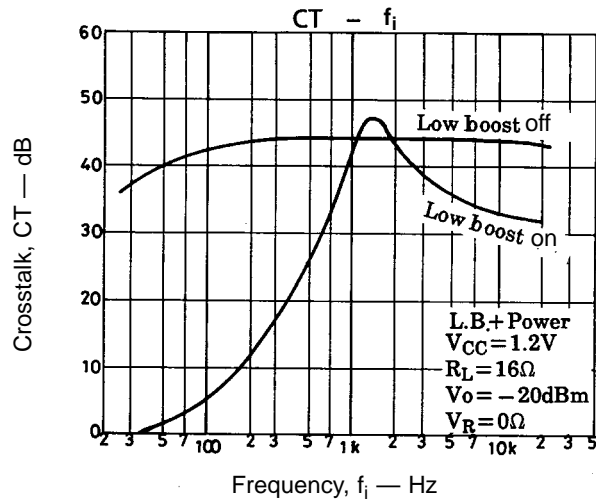












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