

**SANYO**

No. 4469A

**LA4805V****3 V Stereo Headphone Power Amplifier****Overview**

The LA4805V is a power IC developed for use in stereo headphones. It includes low frequency enhancement, beep function and output control circuits on-chip. Furthermore, the LA4805V realizes a high S/N ratio, a high ripple exclusion ratio, and low current drain.

**Functions**

- Stereo headphone power amplifier
- Low frequency enhancement (L.BOOST)
- Beep amplifier
- Output suppression circuit (PVSS)
- Power switch
- Muting switch

**Features**

- Low current drain (8.3 mA typical)
- High S/N ratio (90 dB typical, 13  $\mu$ V)
- High ripple exclusion ratio (75 dB typical)
- No output electrolytic capacitors required
- Ultra-miniature package (SSOP-30)

**Specifications****Maximum Ratings at Ta = 25°C**

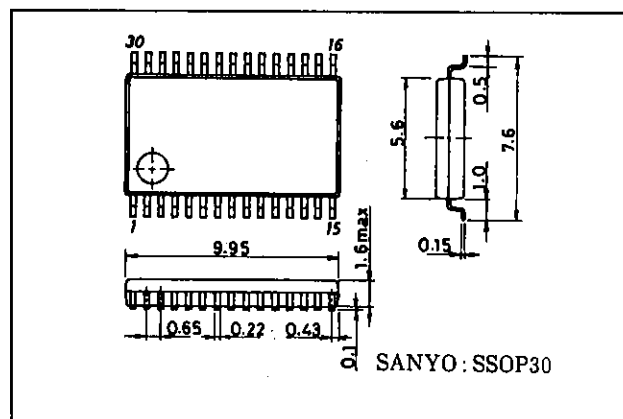
Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	$V_{CC\ max}$		4.5	V
Allowable power dissipation	$P_{d\ max}$		500	mW
Operating temperature	$T_{opr}$		-15 to +50	°C
Storage temperature	$T_{stg}$		-40 to +150	°C

**Operating Conditions at Ta = 25°C**

Parameter	Symbol	Condition	Rating	Unit
Recommended supply voltage	$V_{CC}$		3.0	V
Recommended load resistance	$R_L$		16 to 32	$\Omega$
Operating supply voltage range	$V_{CC\ op}$		1.8 to 3.6	V

**Package Dimensions**

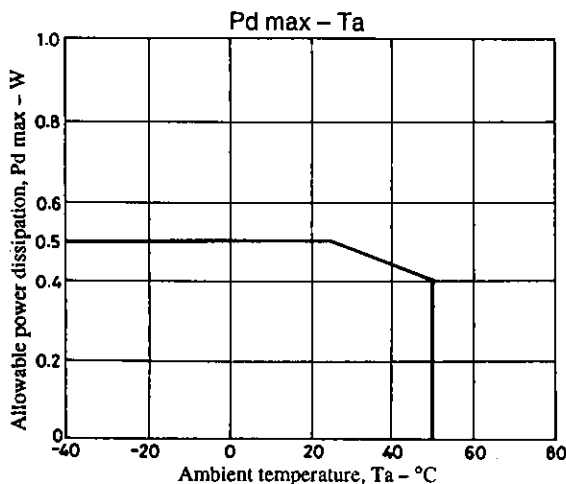
unit: mm

**3191-SSOP30**

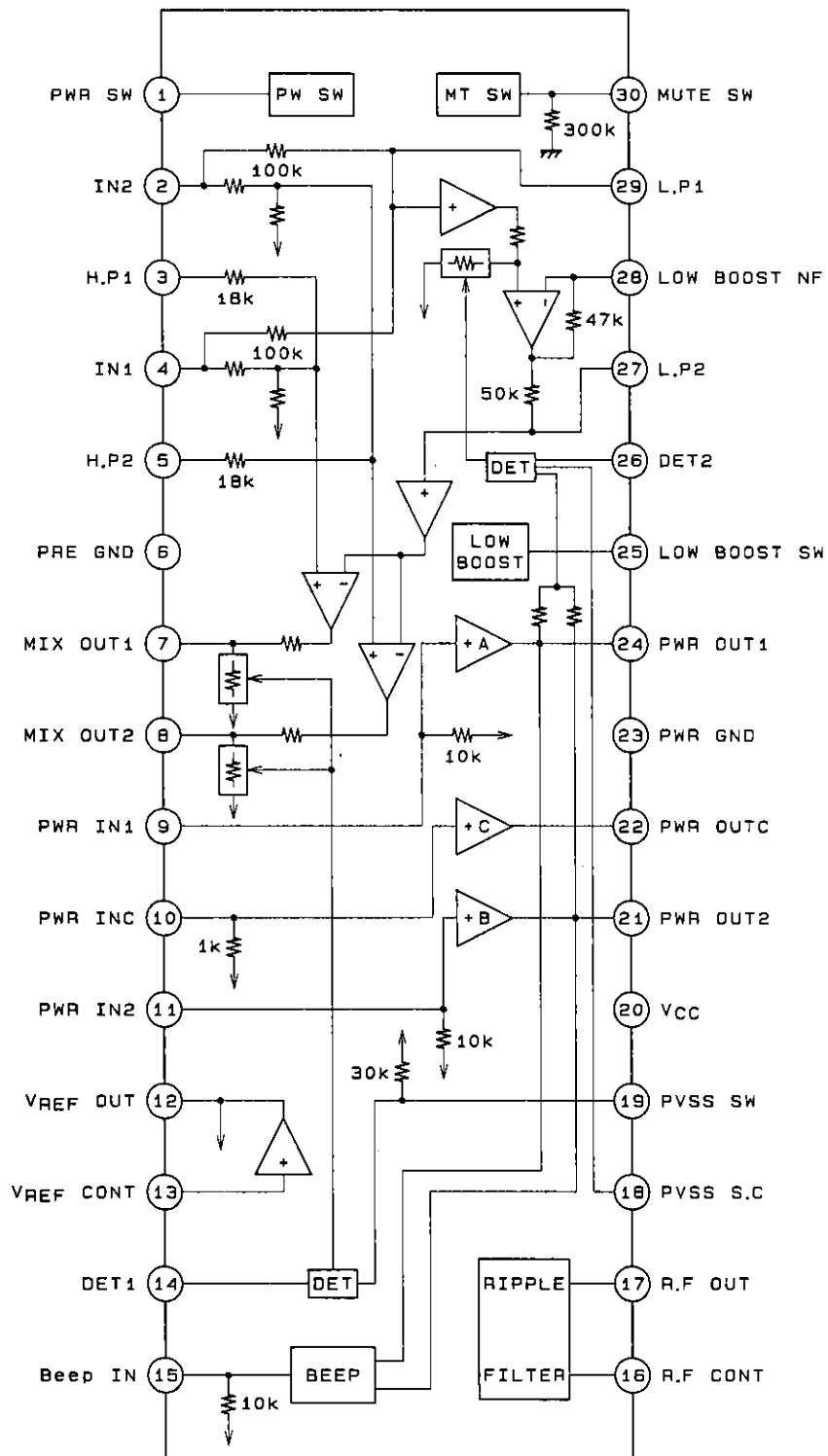
**Operating Characteristics**at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.0\text{ V}$ ,  $f = 1\text{ kHz}$ ,  $0.775\text{ V} = 0\text{ dBm}$ ,  $R_L = 10\text{ k}\Omega$  (L.B),  $R_L = 16\text{ }\Omega$  (PWR)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
[L.BOOST +PVSS + PWR]						
Quiescent current	I <sub>CCO1</sub>	IC off		0.05	1.0	μA
	I <sub>CCO2</sub>	Muting on	1.0	2.7	5.0	mA
	I <sub>CCO3</sub>	R <sub>g</sub> = 0, L.BST/PVSS off	4.0	8.3	12.0	mA
	I <sub>CCO4</sub>	R <sub>g</sub> = 0, L.BST/PVSS on	4.5	8.6	12.5	mA
[PWR AMP]						
Output power	P <sub>O</sub>	THD = 10%	15	25		mW
Voltage gain	VG1	V <sub>O</sub> = -10 dBm	15.7	17.7	19.7	dB
Channel balance	V <sub>BL</sub>	V <sub>O</sub> = -10 dBm	-1	0	1	dB
Total harmonic distortion	THD1	V <sub>O</sub> = 0.35 V		0.1	0.3	%
Output noise voltage	V <sub>NO1</sub>	R <sub>g</sub> = 0, DiN AUDIO		13	25	μV
Crosstalk	CT1	V <sub>O</sub> = -10 dBm, TUN = 1 kHz, R <sub>g</sub> = 0	35	45		dB
Ripple exclusion ratio	SVRR1	V <sub>CC</sub> = 1.8 V, f = 100 Hz, V <sub>R</sub> = -20 dBm, TUN = 100 Hz	60	75		dB
Muting attenuation	ATT <sub>M</sub>	THD = 1%, R <sub>g</sub> = 0 kΩ	80	90		dB
Beep output	V <sub>O</sub> BEEP	V <sub>IN</sub> = -16 dBm (sine wave)	1.0	3.0		mV
Output current offset	V <sub>DC OFF</sub>	V <sub>IN</sub> = 0 V, R <sub>g</sub> = 0	-20	0	20	mV
Input resistance	R <sub>i</sub>		7	10	13	kΩ
[L.BOOST]						
Voltage gain	VG2	V <sub>IN</sub> = -30 dBm, boost on/off	-3.2	-5.2	-7.2	dB
Boost*	L.BTS1	V <sub>IN</sub> = -30 dBm, f = 100 Hz, boost on	13	15	17	dB
	L.BTS2	V <sub>IN</sub> = -30 dBm, f = 10 kHz, boost on	3	5	7	dB
Maximum output voltage	V <sub>O</sub> max	THD = 1%, boost on	0.2	0.4	0.6	V
Total harmonic distortion	THD2	V <sub>O</sub> = 0.1 V, boost on		0.085	0.25	%
Crosstalk	CT2	V <sub>O</sub> = -20 dBm, R <sub>g</sub> = 0, boost on	25	30		dB
Output noise voltage	V <sub>NO2</sub>	R <sub>g</sub> = 0, boost off		3	10	μV
Ripple exclusion ratio	SVRR2	R <sub>g</sub> = 0, f = 100 Hz, V <sub>g</sub> = -20 dBm, boost on	50	60		dB
[L.BOOST + PWR]						
Voltage gain	VG3	V <sub>IN</sub> = -30 dBm, f = 1 kHz, boost on/off	8	10	12	dB
Output voltage	V <sub>O1</sub>	V <sub>IN</sub> = -30 dBm, f = 100 Hz, boost on	0.13	0.23	0.33	V
Total harmonic distortion	THD3	V <sub>IN</sub> = -30 dBm, f = 100 Hz, boost on		0.14	0.5	%
Crosstalk	CT3	V <sub>O</sub> = -20 dBm, R <sub>V</sub> = 0 Ω, boost on	25	32.5		dB
[L.BOOST + PVSS + PWR]: When V <sub>O1</sub> is maximum						
PVSS voltage	V <sub>O</sub> PVSS2	V <sub>IN</sub> = -30 dBm, PVSS2	-32.5	-37.5	-42.5	dBm
PVSS width	V <sub>O</sub> PVSS W	The input amplitude when the output is +3 dB over the starting point	25	30	35	dB
PVSS distortion	THD PVSS	V <sub>IN</sub> = -40 dBm, PVSS2		0.55	2.0	%
PVSS starting input	V <sub>IN</sub> PVSS	PVSS2	-41	-46	-51	dBm

Note: \* Boost levels relative to 1 kHz



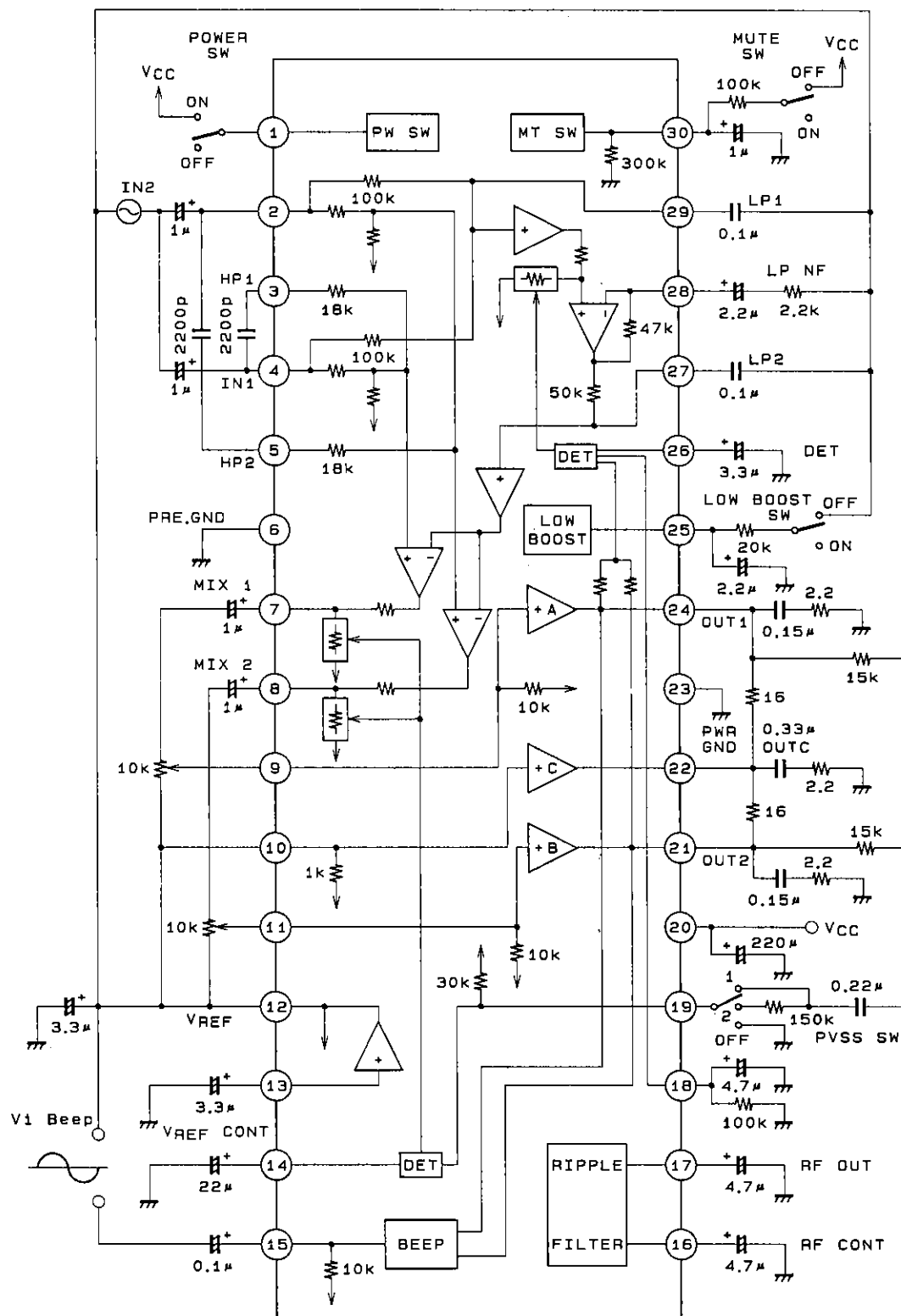
## Pin Assignment and Block Diagram



A01329

Unit (resistance:  $\Omega$ )

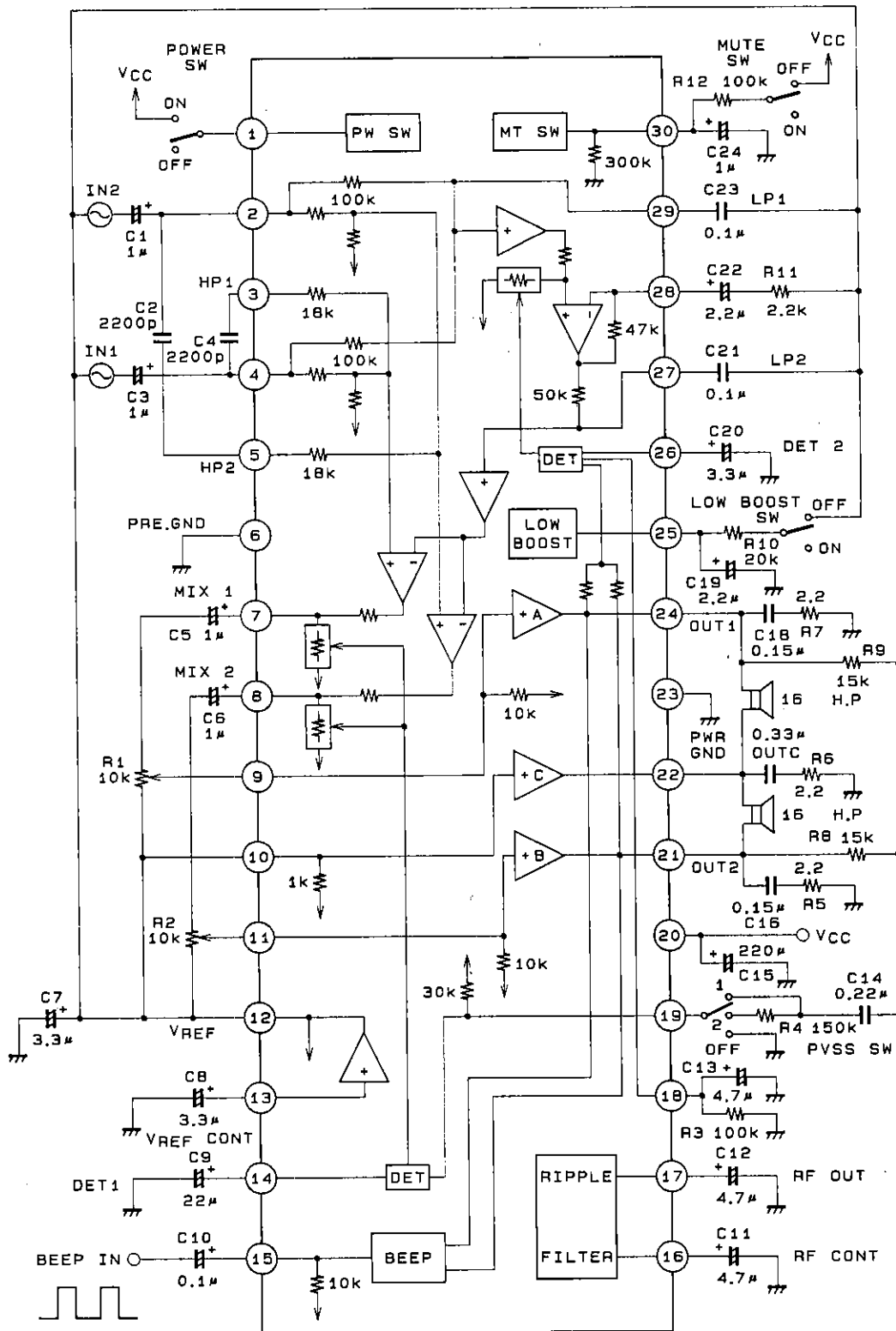
## Test Circuit



A01330

Unit (resistance: Ω, capacitance: F)

## Application Circuit



A01331

Unit (resistance:  $\Omega$ , capacitance: F)

Pin Functions and Equivalent Circuits ( $V_{CC} = 3.0\text{ V}$ )Unit (resistance:  $\Omega$ )

Pin No.	Symbol	$V_{DC}$ (V)	Equivalent circuit	Pin function
1	PWR SW	0 to 0.7		<ul style="list-style-type: none"> <li>Applying <math>V_{CC}</math> to pin 1 turns the IC power on.</li> </ul>
2 4	IN 2 IN 1	1.1 1.1		<ul style="list-style-type: none"> <li>Low boost input pin</li> </ul>
3 5	H.P 1 H.P 2	1.1 1.1		<ul style="list-style-type: none"> <li>High-pass input pin</li> </ul>
6	PRE GND			
7 8	MIX OUT 1 MIX OUT 2	1.1 1.1		<ul style="list-style-type: none"> <li>Low boost and buffer output pin</li> </ul>
9 11	PWR IN 1 PWR IN 2	1.1 1.1		<ul style="list-style-type: none"> <li>Power input pin</li> <li>The input resistance is 10 k<math>\Omega</math>.</li> </ul>
10	PWR IN C	1.1		<ul style="list-style-type: none"> <li>Power amp common input pin</li> <li>Connect to <math>V_{ref}</math> in normal operation</li> </ul>

Continued on next page.

Continued from preceding page.

Unit (resistance:  $\Omega$ , capacitance: F)

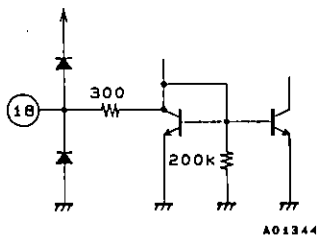
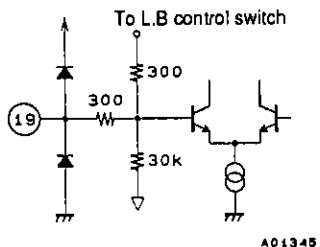
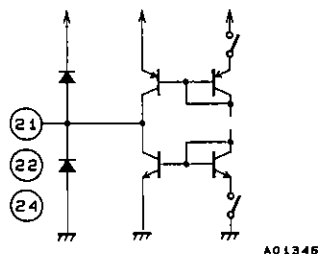
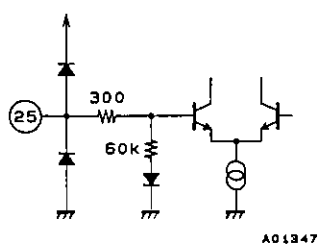
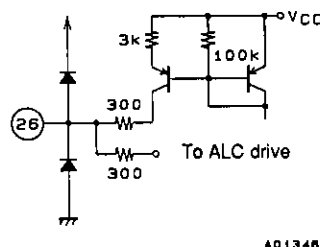
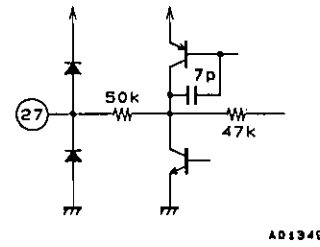
Pin No.	Symbol	V <sub>DC</sub> (V)	Equivalent circuit	Pin function
12	V <sub>REF</sub> OUT	1.1		<ul style="list-style-type: none"> <li>Fixed bias of 1.1 V</li> </ul>
13	V <sub>REF</sub> CONT	1.1		<ul style="list-style-type: none"> <li>The V<sub>REF</sub> CONT pin, 1.1 V</li> </ul>
14	DET 1	0 to 1.3		<ul style="list-style-type: none"> <li>AVLS operates at 0.65 V or higher.</li> </ul>
15	Beep IN	1.1		<ul style="list-style-type: none"> <li>Beep input pin</li> <li>Only operates when the muting function is on.</li> </ul>
16	R.F. CONT	2.2		<ul style="list-style-type: none"> <li>The R.F. CONT pin</li> </ul>
17	R.F. OUT	2.65		<ul style="list-style-type: none"> <li>Set to a bias of about 0.88 times V<sub>CC</sub>.</li> </ul>

Continued on next page.

# LA4805V

Continued from preceding page.

Unit (resistance:  $\Omega$ , capacitance: F)

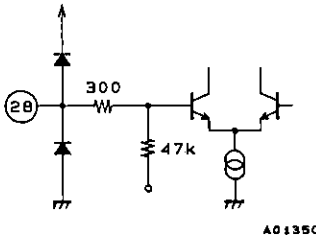
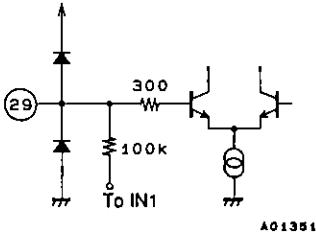
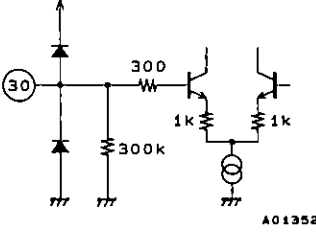
Pin No.	Symbol	V <sub>DC</sub> (V)	Equivalent circuit	Pin function
18	PVSS S.C	0 to 0.7		<ul style="list-style-type: none"> <li>Smoothing pin used when PVSS is turned on and off.</li> </ul>
19	PVSS SW	0 to 1.1		<ul style="list-style-type: none"> <li>PVSS is turned on by the power output signal, and turned off when grounded.</li> </ul>
20	V <sub>CC</sub>			
21 22 24	PWR OUT 2 PWR OUT C PWR OUT 1	1.1 1.1 1.1		<ul style="list-style-type: none"> <li>The power output pins</li> <li>The LA4805V drives headphones with pin 22 used as a common center. (No electrolytic capacitors are used in the output.)</li> </ul>
23	PWR GND			
25	LOW BOOST SW	0 to 1.0		<ul style="list-style-type: none"> <li>The low boost function is turned on when this pin is floating and turned off when it is connected to V<sub>ref</sub>.</li> </ul>
26	DET 2	0.5 to 1.3		<ul style="list-style-type: none"> <li>ALC operates at 0.65 V or higher.</li> </ul>
27	L.P 2	1.1		<ul style="list-style-type: none"> <li>Low boost secondary low pass pin</li> </ul>

Continued on next page.



Continued from preceding page.

Unit (resistance:  $\Omega$ )

Pin No.	Symbol	V <sub>DC</sub> (V)	Equivalent circuit	Pin function
28	LOW BOOST NF	1.1		• Low boost NF pin
29	L.P 1	1.1		• Low boost primary low pass pin
30	MUTE SW	0 to 2.2		• The muting function is on when this pin is floating and off when connected to V <sub>CC</sub> through a 100 k $\Omega$ resistor.

**External Component Functions:** Recommended values are indicated in parentheses.

- C1, C3 (1 to 4.7  $\mu$ F)

Input coupling capacitors

- C2, C4 (2200 pF)

Input high pass capacitors. The high region gain when low boost is on is determined by the IC internal 18 k $\Omega$  resistance and these external 2200 pF capacitors.

- C5, C6 (0.1 to 1  $\mu$ F)

Mixer amplifier to power amplifier coupling capacitors

- C7, C8 (3.3 to 10  $\mu$ F)

Reference bias (V<sub>ref</sub>) decoupling capacitors

- C9 (10 to 22  $\mu$ F)

Determines the PVSS recovery time.

- C10 (0.1 to 1  $\mu$ F)

Beep input coupling capacitor. Be sure that this capacitor does not attenuate the beep signal.

- C11, C12 (4.7 to 10  $\mu$ F)

Ripple filter capacitors. Care is required selecting their value, since although increasing the capacitance increases the ripple exclusion ratio, it also increases the rise time when the power is turned on.

- C13 (3.3 to 4.7  $\mu$ F)

Smoothing capacitor for PVSS on/off switching noise

- C14 (0.22 to 0.47  $\mu\text{F}$ )

Coupling capacitor that accepts the power output signal and inputs that signal to the PVSS function.

- C15 (220  $\mu\text{F}$ )

Power supply line decoupling capacitor

- C16, C17, C18 (0.22 to 0.47  $\mu\text{F}$ )

Oscillation suppression capacitors. We recommend using film capacitors.

- C19 (2.2 to 4.7  $\mu\text{F}$ )

Smoothing capacitor for low boost on/off switching noise

- C20 (3.3 to 4.7  $\mu\text{F}$ )

Determines the low boost attack time. Increasing the capacitance increases the attack time.

- C21, C23 (0.1  $\mu\text{F}$ )

Low pass capacitors used with the low boost function

- C22 (2.2 to 4.7  $\mu\text{F}$ )

Low boost amplifier NF capacitor. Values in excess of the recommended range will slow the low boost amplifier's rise time and may cause noise spikes.

- C24 (0.1 to 1.0  $\mu\text{F}$ )

Determines the muting time. See the "IC Usage Notes" section for a discussion of the muting time when the capacitor C24 value is varied.

- R1, R2 (10  $\text{k}\Omega$ )

Mixer amplifier load resistance and power input adjustment potentiometer.

- R3 (100 k to 1  $\text{M}\Omega$ )

Smoothing resistor for PVSS on/off switching noise

- R4 (50 k to 200  $\text{k}\Omega$ )

PVSS level adjustment resistor

- R5, R6, R7 (1 to 4.3  $\Omega$ )

Power amplifier oscillation suppression capacitors. We recommend using film capacitors.

- R8, R9 (15  $\text{k}\Omega$ )

Power output signal bias resistor for PVSS operation

- R10 (20  $\text{k}\Omega$ )

Determines the pin 25 bias when low boost is off.

- R11 (1.5 k to 2.2  $\text{k}\Omega$ )

Determines the low boost amplifier's voltage gain.

- R12 (100  $\text{k}\Omega$ )

Determines the pin 30 bias when muting is off (and PWR is on).

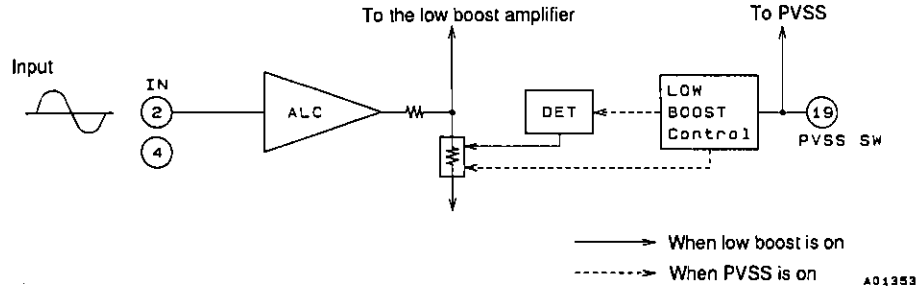
We recommend using a 100  $\text{k}\Omega$  resistor for R12, since the muting switch pin (pin 30) threshold area is determined by this (100  $\text{k}\Omega$ ) resistance and the IC's internal 300  $\text{k}\Omega$  resistance.



- The table below lists the  $t_{s\text{ ON}}$  and  $t_{s\text{ OFF}}$  times for different values of  $C_r$ .

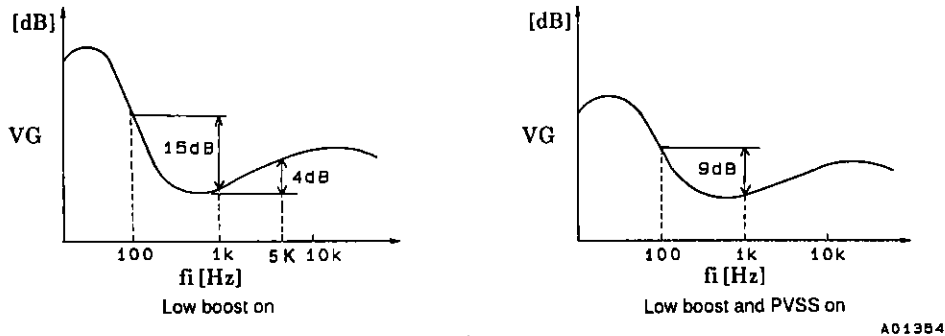
$C_r$	$t_{s\text{ OFF}}$	$t_{s\text{ ON}}$
0.1 $\mu\text{F}$	15 ms	3.2 ms
1.0 $\mu\text{F}$	150 ms	30 ms
2.2 $\mu\text{F}$	300 ms	56 ms

### 3. Boost level when the low boost function and PVSS are on

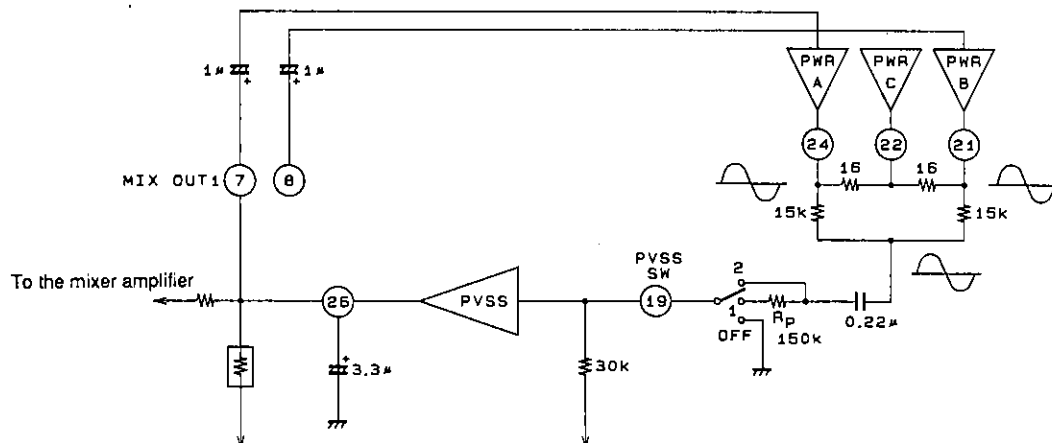


- Normally, the 100 Hz boost level with respect to 1 kHz is 15 dB when low boost is on. However, the LA4805V is designed so that the 100 Hz boost level with respect to 1 kHz is 9 dB when both PVSS and low boost are on. PVSS is turned on when the power output is input to pin 19, and the low boost level is determined by adjusting the DET as shown by the dotted lines in the figure. (See the separately provided detailed data describing the state where both low boost and PVSS are on.)

- The graphs below give a simplified view of the  $f_i$ -VG characteristics.

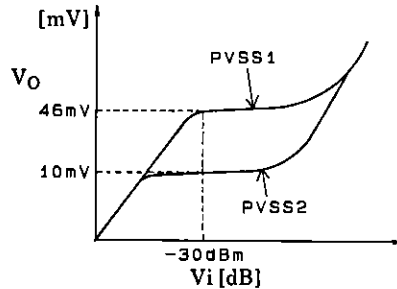


### 4. PVSS

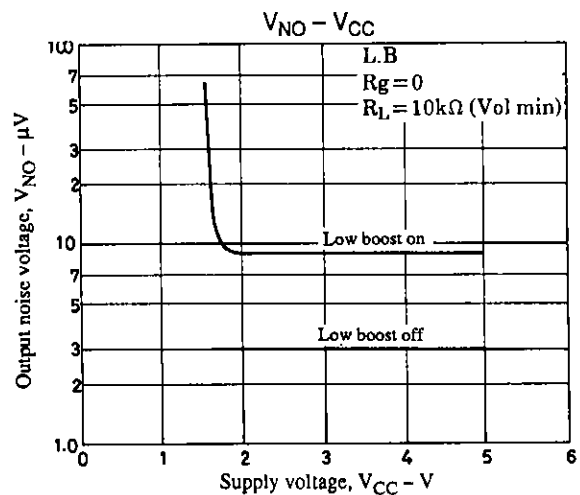
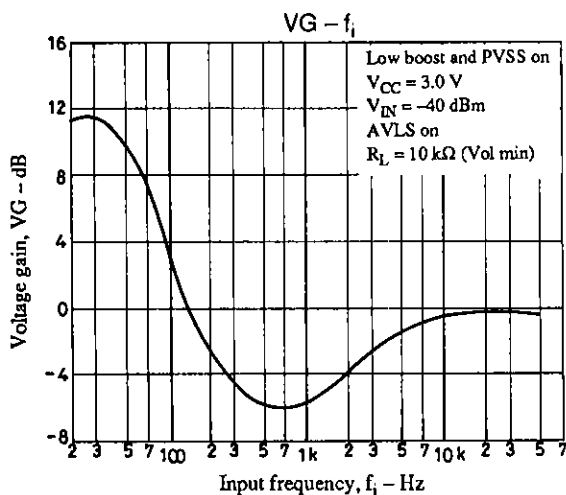
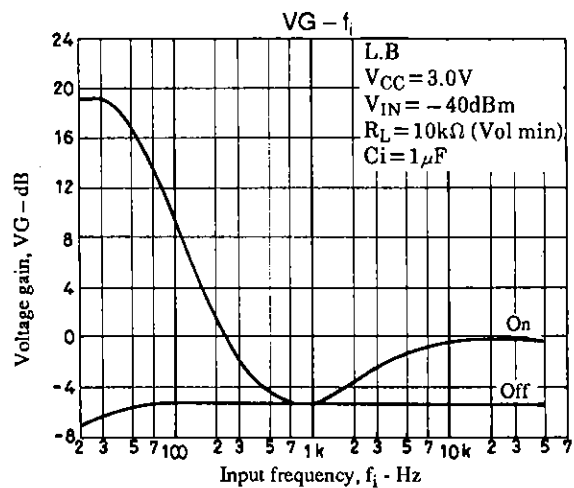
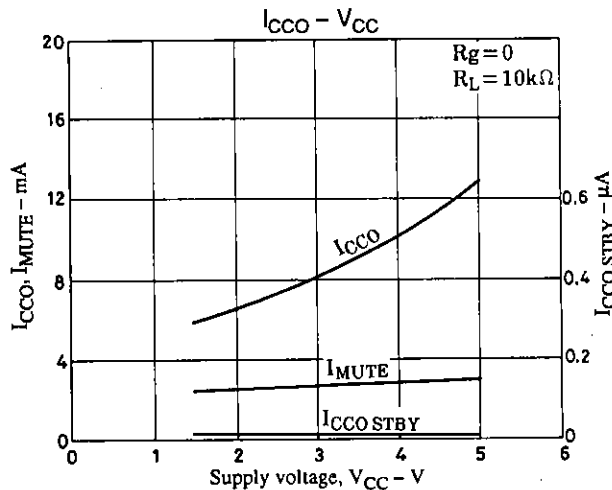


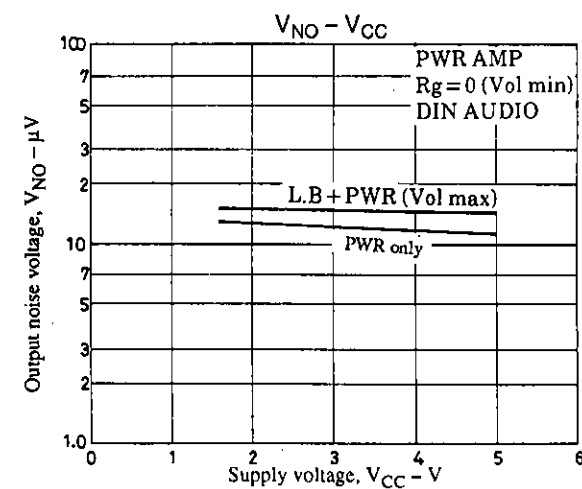
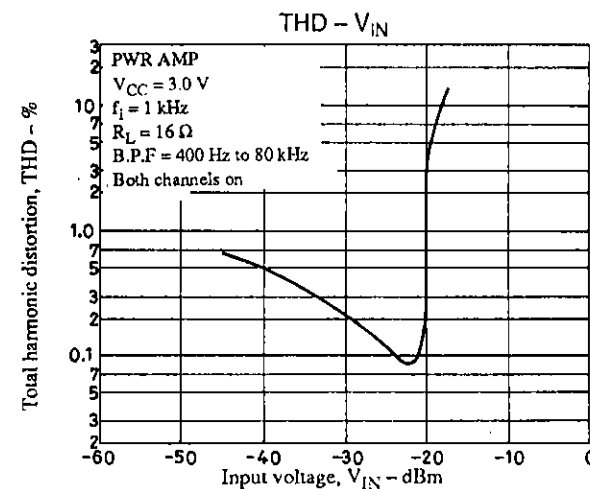
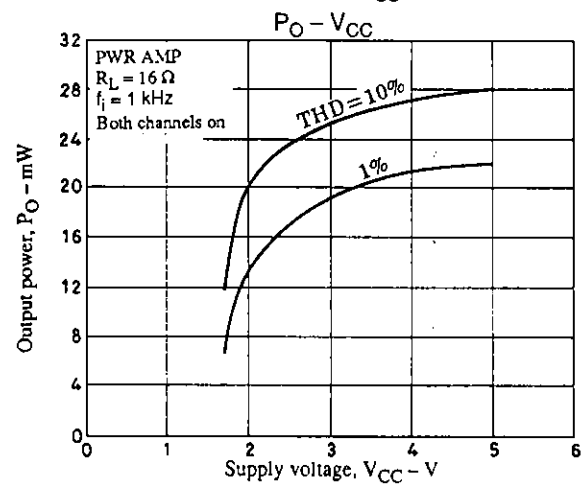
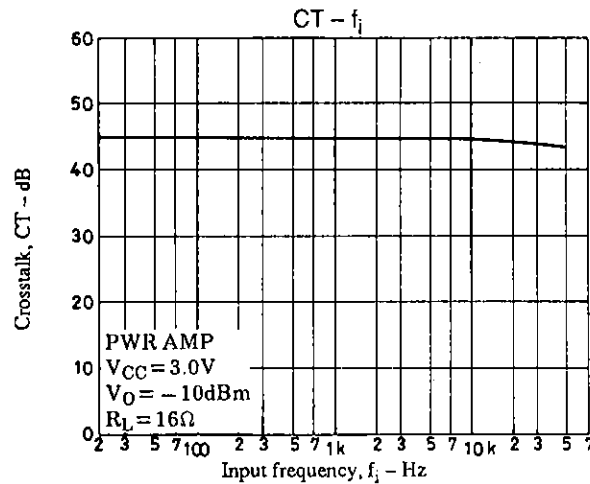
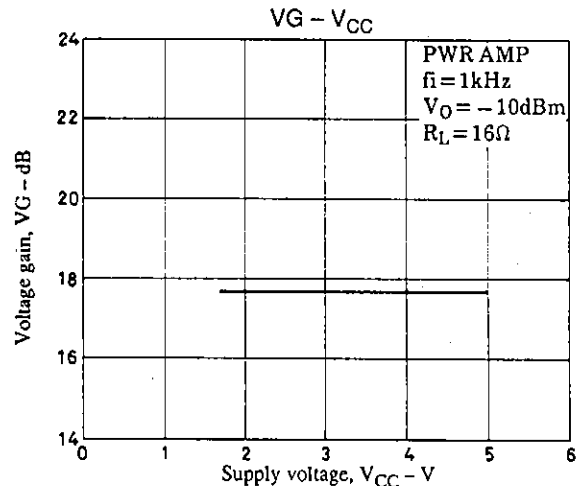
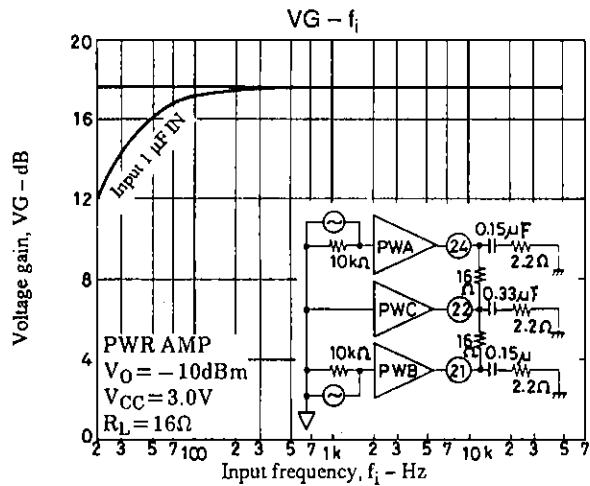
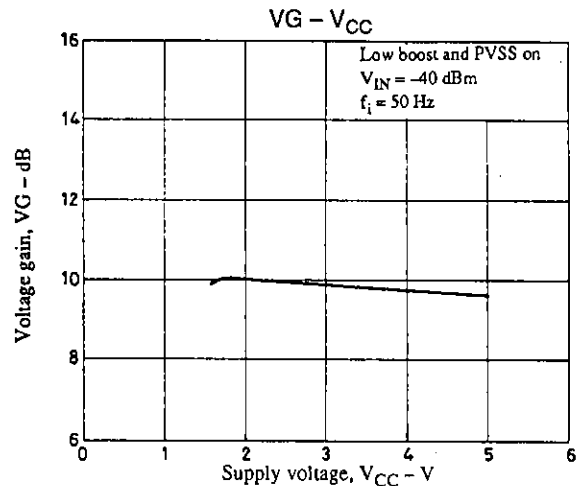
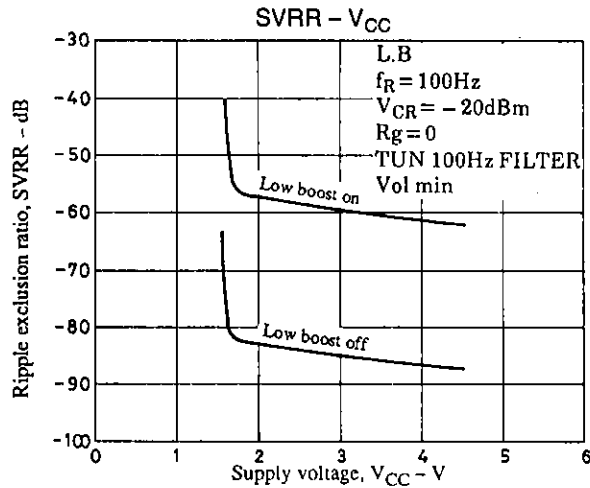
Unit (resistance:  $\Omega$ , capacitance: F)

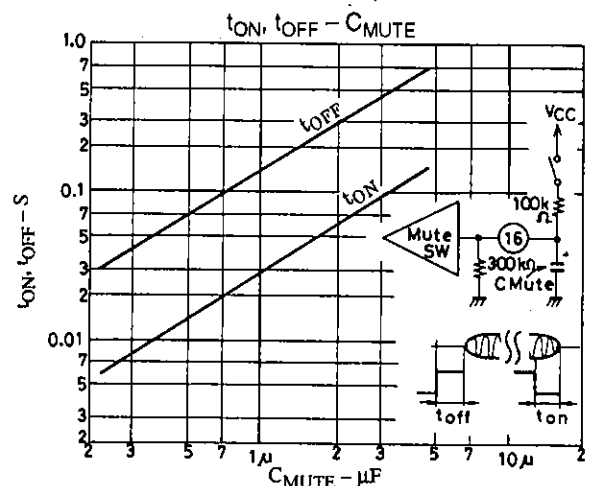
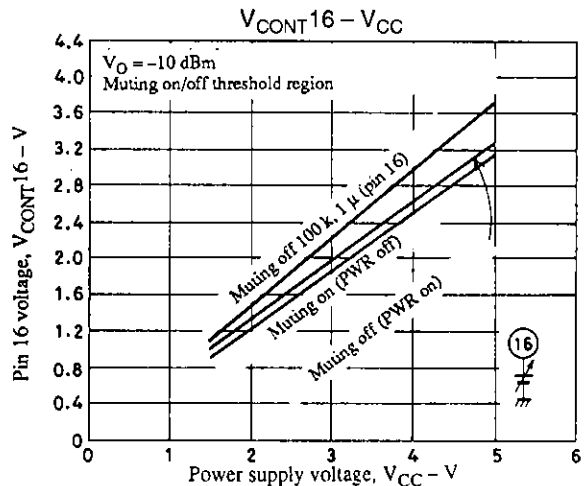
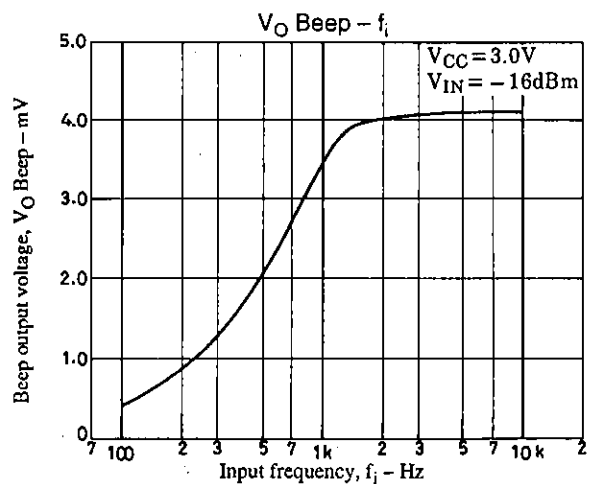
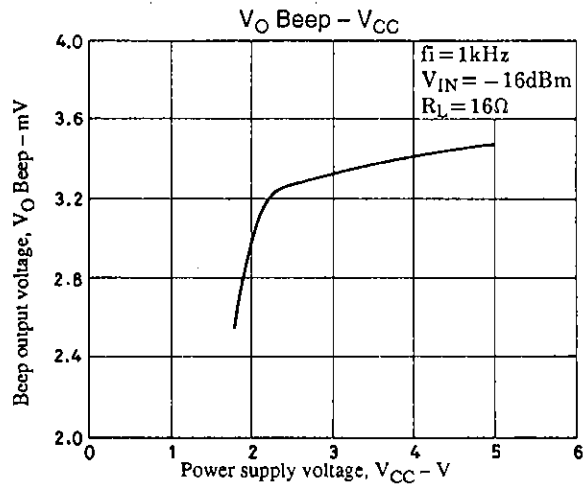
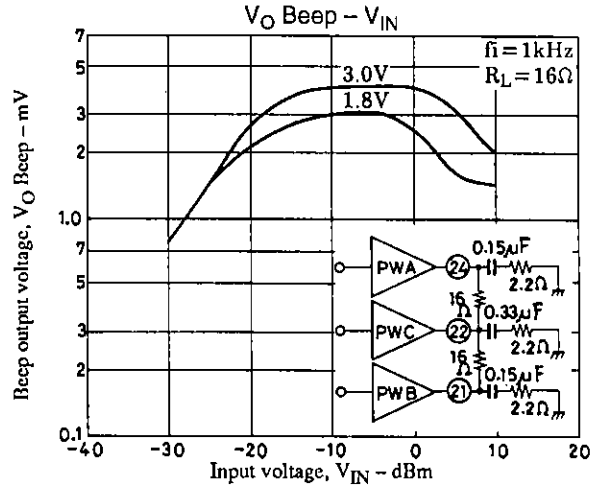
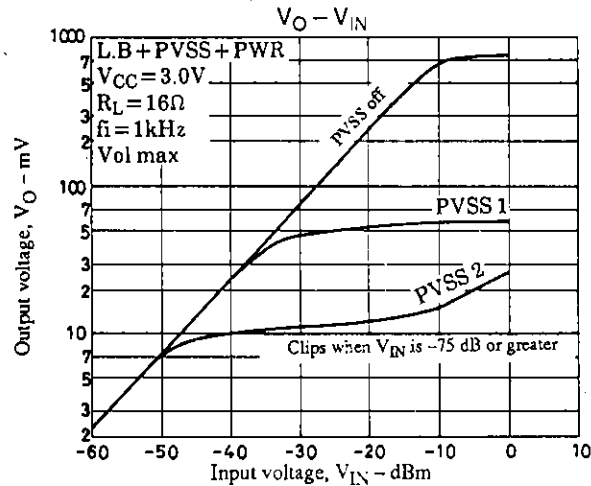
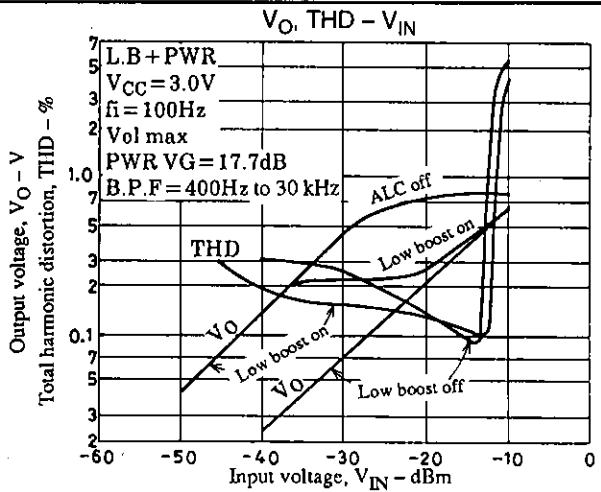
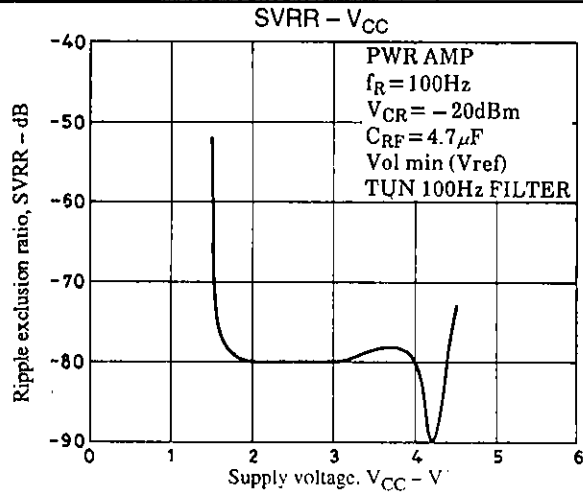
- As shown in the figure above, PVSS is designed so that PVSS is operated and turned on by inputting to pin 19 the mixed power outputs through 15 k $\Omega$  resistors. When this input is grounded, PVSS is turned off.
- PVSS switching can be changed by an IC internal 30 k $\Omega$  resistor and an external (150 k $\Omega$ ) resistor. When this function is used,  $V_O$  is set to 45 mV by passing the mixed signal through a 150 k $\Omega$  resistor at PVSS1, and is set to 10 mV by passing the mixed signal through only the 0.22  $\mu$ F capacitor at PVSS2. (Detailed data is provided separately.)
- The graph below gives a simplified view of the  $V_i$ - $V_O$  characteristics and the output  $V_O$  when  $R_P$  is varied.

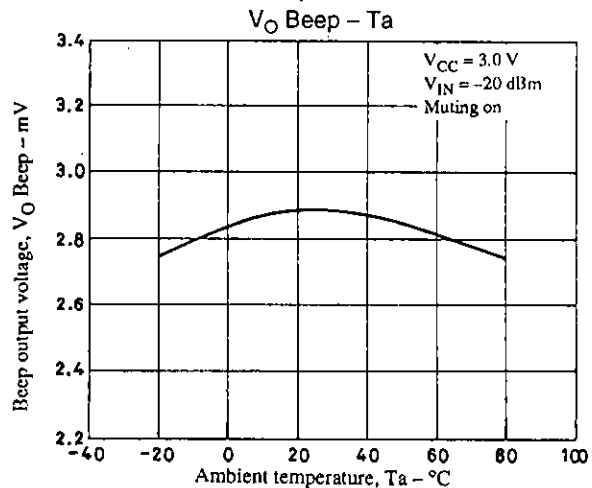
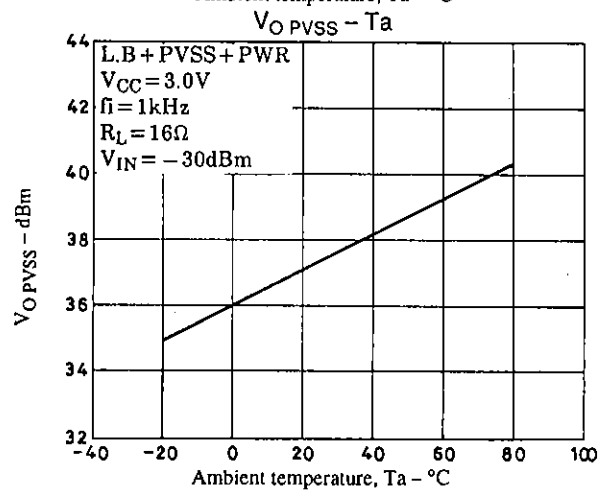
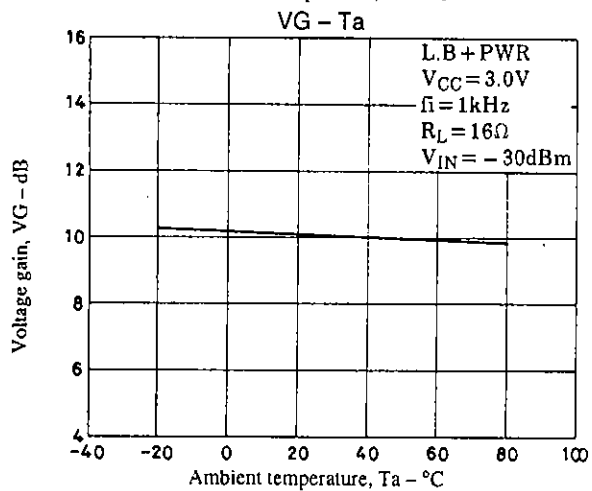
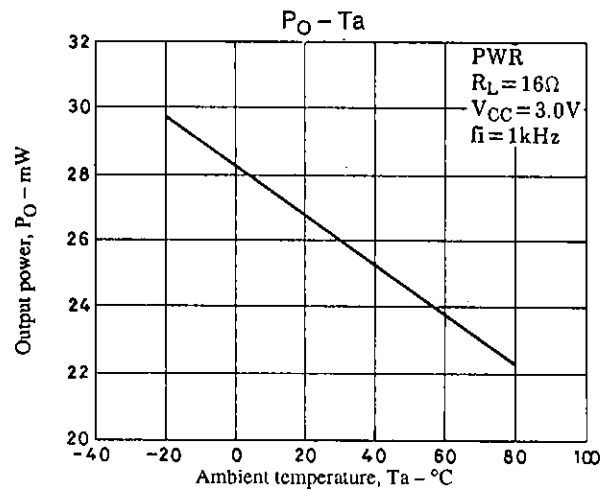
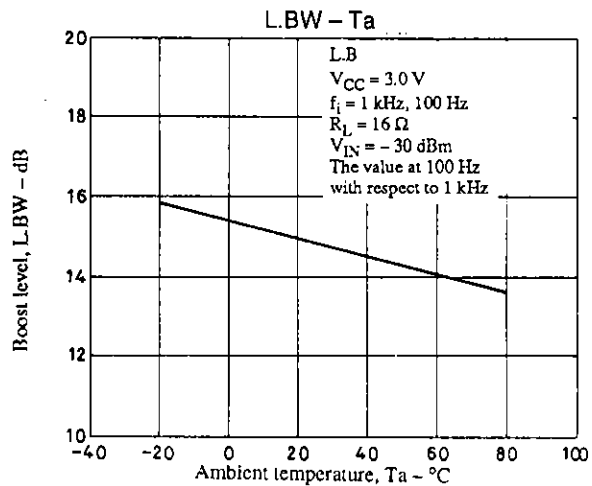
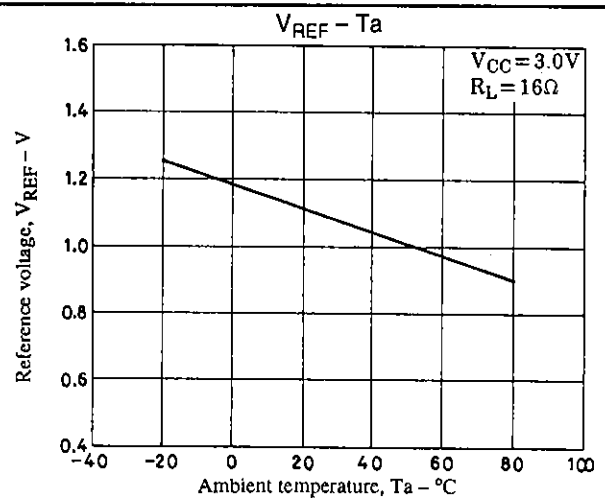
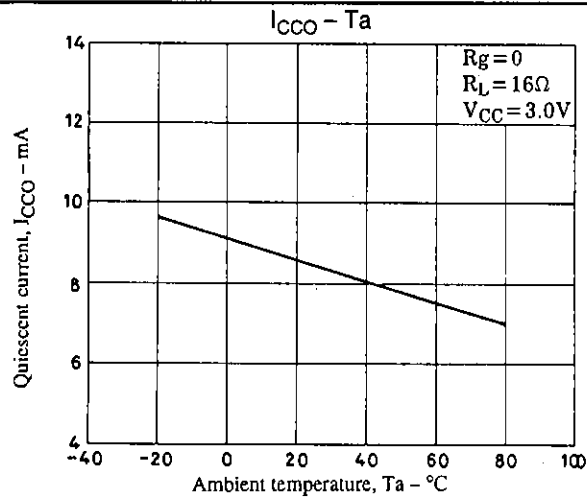


$R_P$	$V_O$
50 k $\Omega$	25 mV
100 k $\Omega$	35 mV
150 k $\Omega$	46 mV
200 k $\Omega$	56 mV











- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
  - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.