



LA5623M

Combination System Reset IC

Overview

The LA5623M is a combination reset IC that provides two reset functions. The first, reset 1, detects the input voltage and applies a reset to the CPU system and other logic systems. The second, reset 2, detects the power supply voltage when the power is turned on or off, and applies a reset to the CPU system and other logic systems. This latter function allows the reset time to be adjusted from two external pins.

Features

- Reset circuit (output 1) that detects the input voltage and provides a delay time of 200 μ s.
- System reset circuit (output 2) that provides a switchable delay time of 25, 50, 100, or 200 ms.
- Low operating limit voltage
- Both reset 1 and reset 2 have hysteresis characteristics.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		−0.3 to +12	V
Output 1 sink current	I _{SINK1}		8	mA
Output 2 sink current	I _{SINK2}		8	mA
Output voltage	V _O		−0.3 to +10	V
Manual input voltage	V _{RES}		−0.3 to +10	V
Input voltage range	V _{IN1}		−0.3 to +10	V
Ct0, Ct1 voltage	V _{ct}		0 to +10	V
Allowable power dissipation	P _{d max}		250	mW
Operating temperature	T _{opr}		−20 to +75	°C
Storage temperature	T _{stg}		−40 to +125	°C

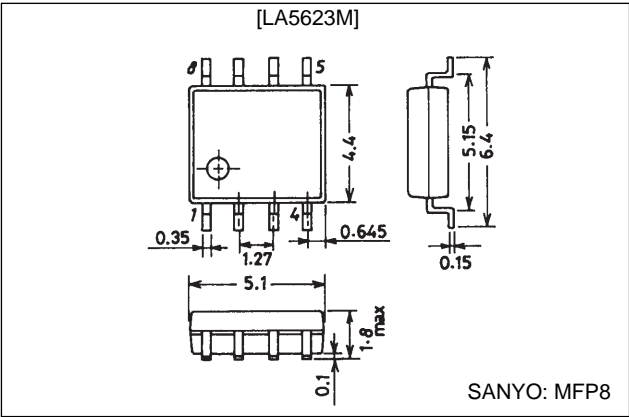
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		2 to 10	V
Input voltage range	V _{IN}	For pulse widths of up to 20 ns	−2 to V _{CC} + 1	V
Input high-level voltage	V _{RESH}	For pulse widths of up to 20 ns	V _{CC} + 1	V
Input low-level voltage	V _{RESL}	For pulse widths of up to 20 ns	−2	V

Package Dimensions

unit: mm

3032B-MFP8



LA5623M

Operating Characteristics at Ta = 25°C, VCC = 5 V

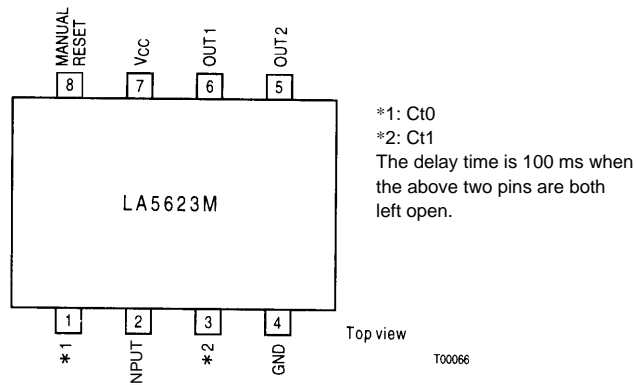
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Reset Circuit 1, 2 Common]						
Current drain when off	I _{CC1}		–	1.4	2.0	mA
Current drain when on	I _{CC2}	When reset 1 and 2 are both on	–	2	3	mA
Detection voltage temperature coefficient	VS/ΔT		–	0.01		%/°C
Output high-level voltage	V _{OH}	I _{OH} = –40 μA	0.9 V _{CC}	–	–	V
Low-level signal propagation delay	t _{PHL}	C _L = 100 pF	–	10	–	μs
Operating limit voltage *1	V _{OPL}	R _L = 2.2 kΩ, V(sat) ≤ 0.4 V	–	0.67	0.80	V
		R _L = 100 kΩ, V(sat) ≤ 0.4 V	–	0.55	0.70	V
Internal pull-up resistance	R		5	10	15	kΩ
[Reset Circuit 1]						
Sense voltage 1	VS1		1.20	1.25	1.30	V
Hysteresis voltage 1	ΔVS1		9	15	23	mV
High-level signal propagation delay 1	t _{PLH1}	C _L = 100 pF	80	200	500	μs
Output low voltage 1	V _{OL1}	V _{IN} < 1.2 V, I _{OL} = 5 mA	–	0.2	0.4	V
Input voltage range	V _{IN1}		–0.3	–	+10	V
Input current	I _{IN1}	V _{IN} = 1.25 V	–	100	500	nA
[Reset Circuit 2]						
Sense voltage 2	VS2		4.0	4.2	4.4	V
Hysteresis voltage 2	ΔVS2		30	50	100	mV
High-level signal propagation delay 2	t _{PLH2}	Ct0 = “L”, Ct1 = “H” : CL = 100pF	15	25	35	ms
		Ct0 = “H”, Ct1 = “L” : CL = 100pF	30	50	70	ms
		Ct0 = “H”, Ct1 = “H” : CL = 100pF	60	100	140	ms
		Ct0 = “L”, Ct1 = “L” : CL = 100pF	120	200	280	ms
Output low-level voltage 2	V _{OL2}	V _{CC} < 4.0 V, I _{OL} = 5 mA	–	0.2	0.4	V
Input high-level voltage *2	V _{RESH2}		2	–	10	V
Input high-level current *2	I _{RESH2}	V _{RES} = 2 V	–	–	80	μA
Input low-level voltage *2	V _{RESL2}		–0.3	–	+0.8	V

Notes: 1. The minimum supply voltage such that a low-level output can be maintained.

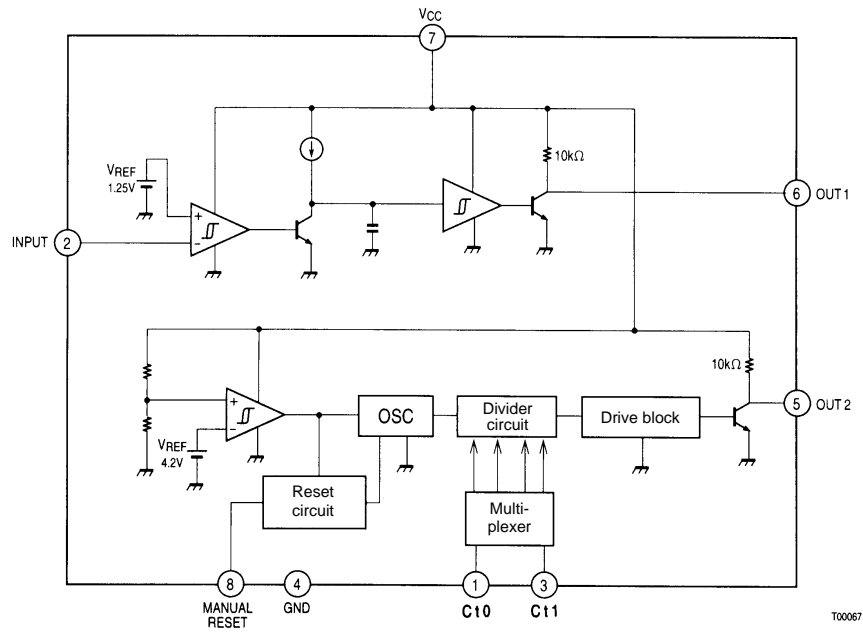
2. Manual reset.

A high level applied to the manual reset pin sets the output 2 pin low, and a low level sets the output 2 pin high.

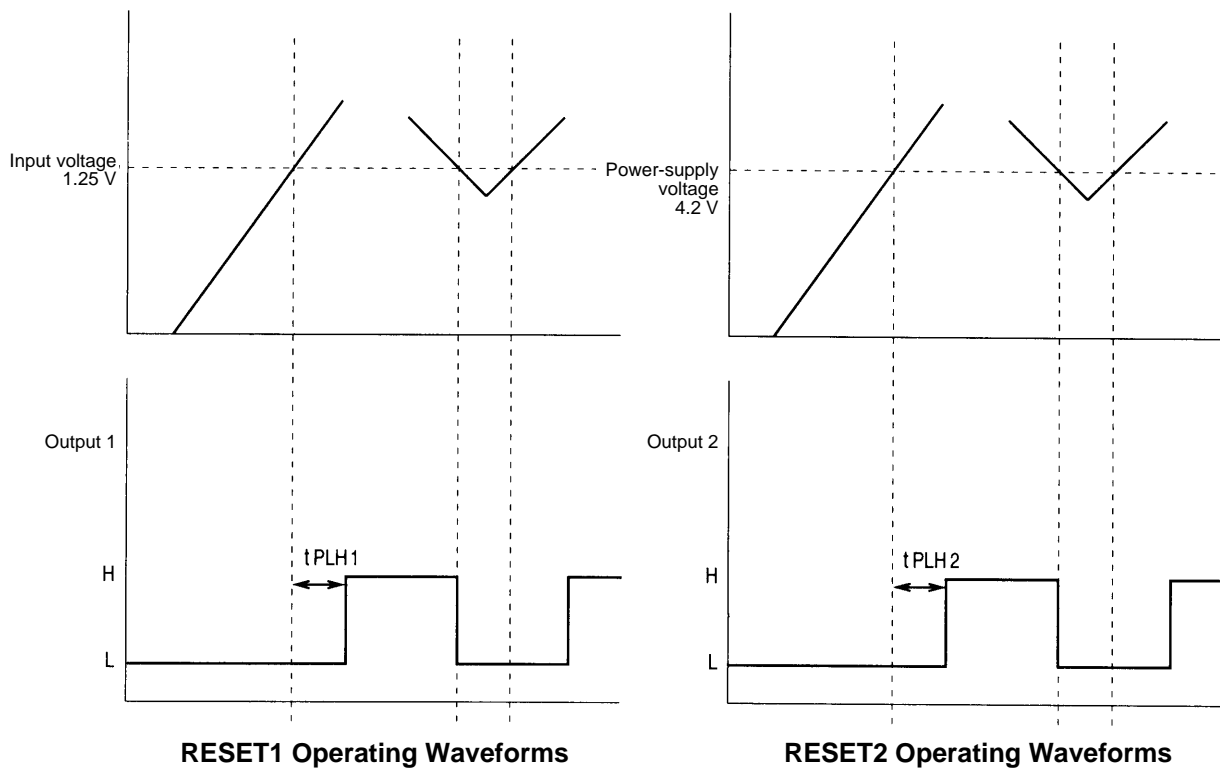
Pin Assignment



Block Diagram



Operating Waveforms

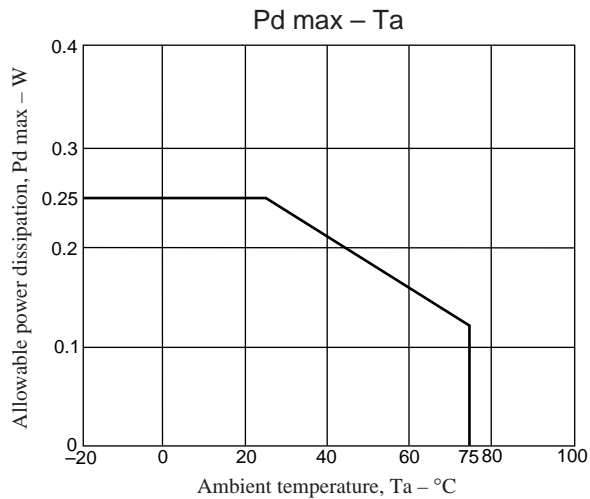


RESET2 Truth Table

Ct0	Ct1	RESET2 delay time
L	H	25 ms
H	L	50 ms
H or OPEN	H or OPEN	100 ms
L	L	200 ms

MANUAL RESET Truth Table

MANUAL RESET	OUT2
H	L
L	H



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