

**LA6311M****Precision Voltage Comparator****Preliminary****Overview**

The LA6311M is a voltage comparator that has low input currents. It is also designed to operate over a wide range of supply voltages ; from  $\pm 15$  V op amp supplies down to the single 5 V supply used for IC logic. Its output is compatible with TTL as well as MOS circuits. Offset balancing is provided, and the outputs can be OR wired.

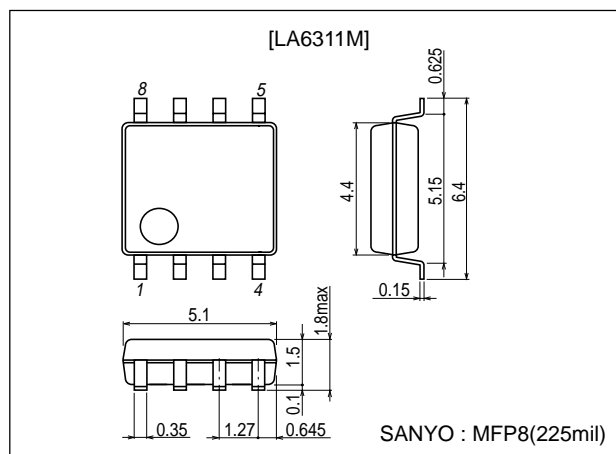
**Features**

- Response time (100 ns typ).
- Operating voltage (+6 V to +36 V).
- Single supply operation.
- Single circuit.
- With input offset trim terminal.
- Bipolar technology.
- Package outline (MFP8).

**Package Dimensions**

unit : mm

3032B-MFP8

**Specifications**Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ 

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V^+ / V^-$		$\pm 18$ (36)	V
Output-to-negative supply voltage	$V_{7-4}$		40	V
Ground-to-negative supply voltage	$V_{1-4}$		30	V
Differential input voltage	$V_{ID}$		$\pm 30$	V
Input voltage	$V_{IN}$		$\pm 15$ (note*)	V
Allowable power dissipation	PD		300	mW
Operating temperature	$T_{opr}$		$-40$ to $+85$	$^\circ\text{C}$
Storage temperature	$T_{stg}$		$-40$ to $+150$	$^\circ\text{C}$

Note : \*For supply voltage less than  $\pm 15$  V, the absolute input voltage is equal to the supply voltage.

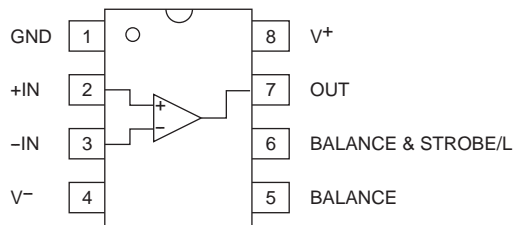
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# LA6311M

**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V^+ / V^- = \pm 15\text{ V}$

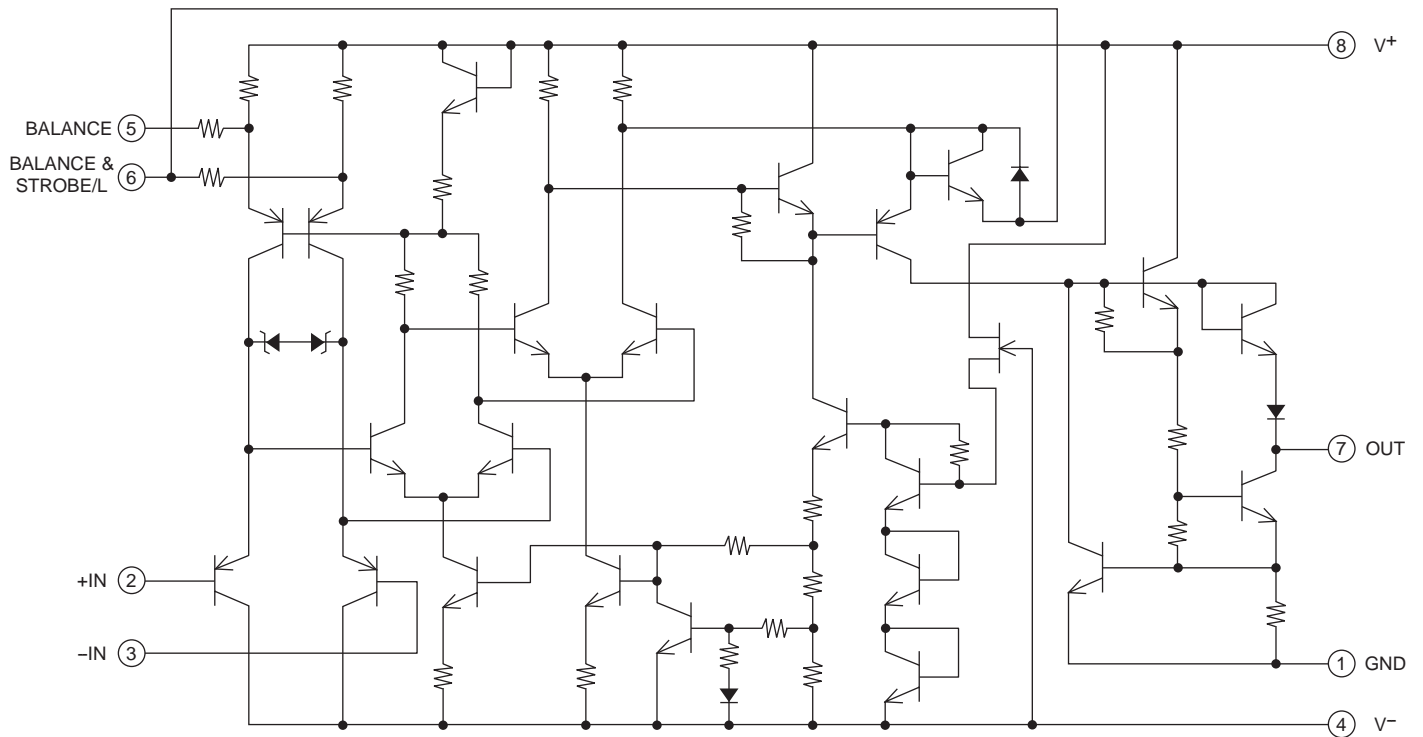
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input offset voltage	$V_{IO}$	$R_s \leq 50\text{ k}\Omega$		1.0	7.5	mV
Input offset current	$I_{IO}$			2.0	50	nA
Input bias current	$I_B$			70	220	nA
Voltage gain	$A_V$			110		dB
Response time	$t_R$			100		ns
Saturation voltage	$V_{SAT}$	$V_{IN} \geq 10\text{ mV}$ , $I_O = 50\text{ mA}$		0.65	1.0	V
Strobe ON current	$I_{STR}$			2.4		mA
Output leakage current	$I_{LEAK}$	$V_{IN} \leq -10\text{ mV}$ , $[V_O - V^-] = 35\text{ V}$		1	50	nA
Input common mode voltage	$V_{ICM}$			$\pm 14$		V
Positive quiescent current	$I^+$	$I_O = 0$		3.0	5.0	mA
Negative quiescent current	$I^-$	$I_O = 0$		1.5	2.5	mA

## Pin Assignment



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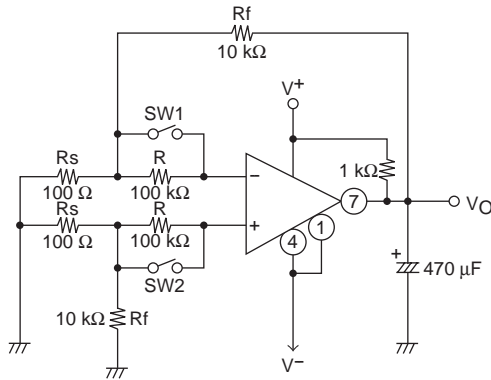
## Equivalent Circuit



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**Test Circuit** at  $V^{\pm} = \pm 15\text{ V}$ ,  $T_a = 25^{\circ}\text{C}$ , TYP

1. Input Offset Voltage ( $V_{IO}$ ), Input Offset Current ( $I_{IO}$ ), Input Base Current ( $I_B$ )



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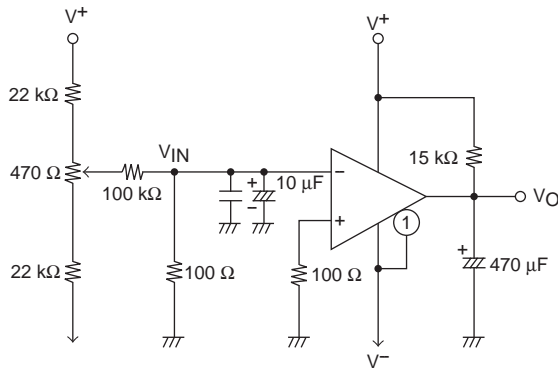
SW1	SW2	V <sub>O</sub>
ON	ON	V <sub>O1</sub>
OFF	OFF	V <sub>O2</sub>
ON	OFF	V <sub>O3</sub>
OFF	ON	V <sub>O4</sub>

$$V_{IO} = \frac{|V_{O1}|}{1 + \frac{R_f}{R_s}} \quad [\text{V}]$$

$$I_{IO} = \frac{|V_{O2} - V_{O1}|}{R \left[ 1 + \frac{R_f}{R_s} \right]} \quad [\text{A}]$$

$$I_B = \frac{|V_{O4} - V_{O3}|}{2R \left[ 1 + \frac{R_f}{R_s} \right]} \quad [\text{A}]$$

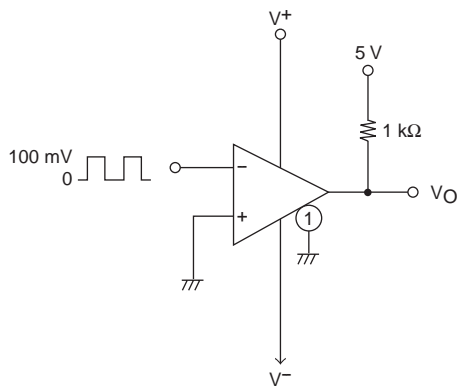
2. Voltage Gain ( $A_V$ )



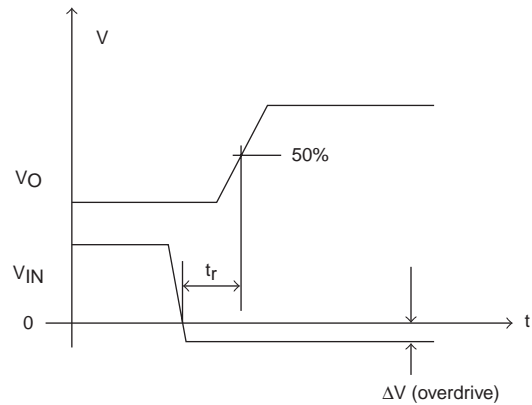
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$$A_V = 20 \log \left[ \frac{V_{O1} - V_{O2}}{V_{IN1} - V_{IN2}} \right] \quad (\text{dB})$$

3. Response Time ( $t_R$ )

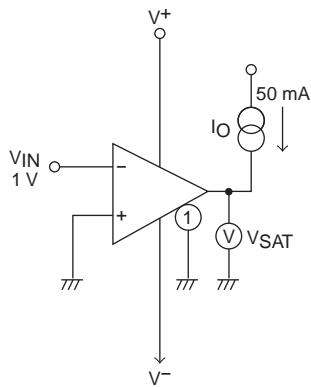


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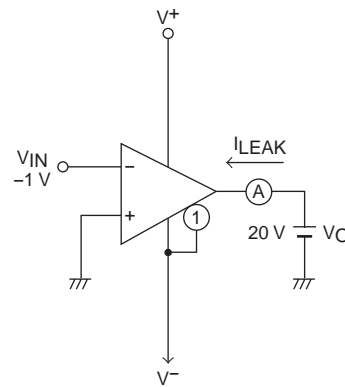
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4.Saturation Voltage ( $V_{SAT}$ )



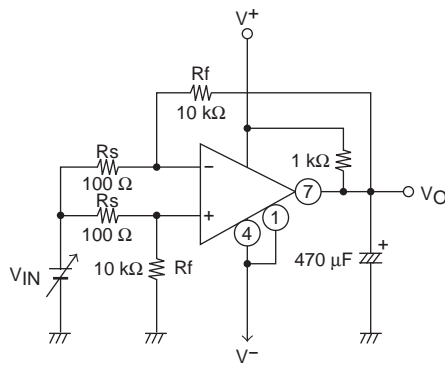
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5.Output Leakage Current ( $I_{LEAK}$ )



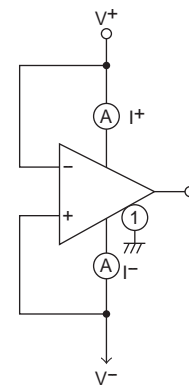
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6.Input Common Mode Voltage ( $V_{ICM}$ )



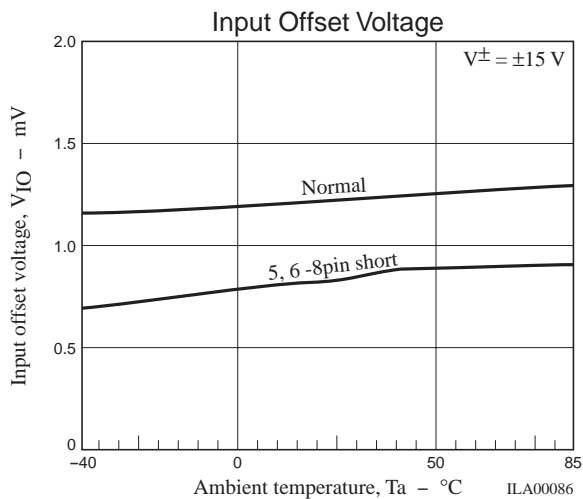
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7.Supply Current ( $I_{CC}$ )

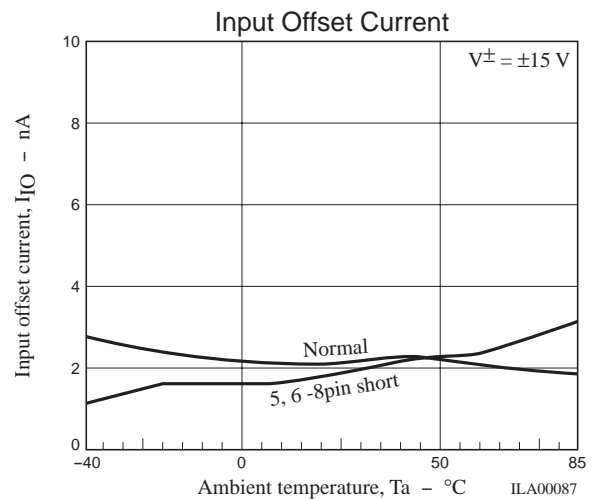


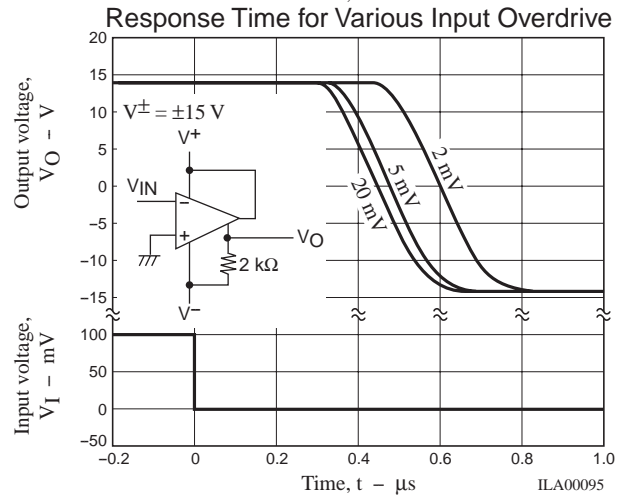
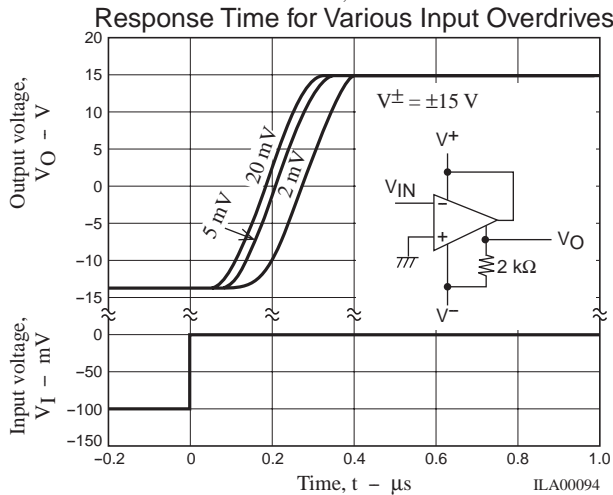
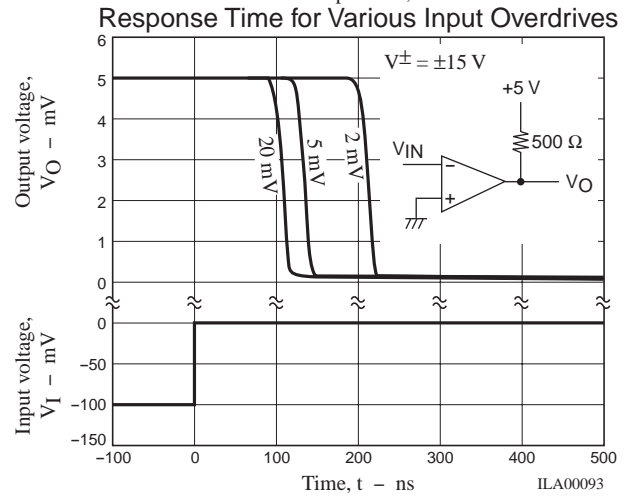
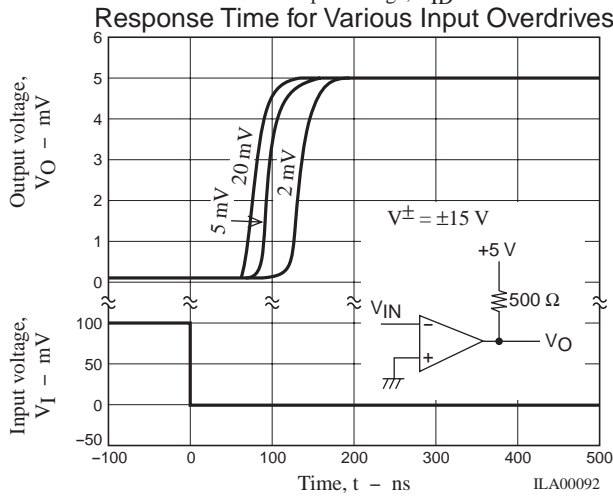
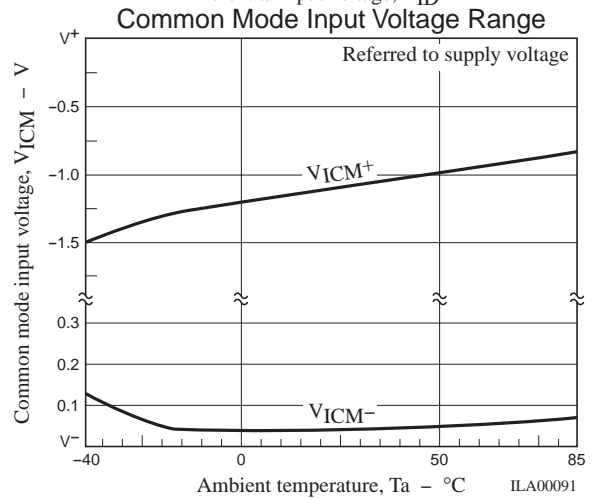
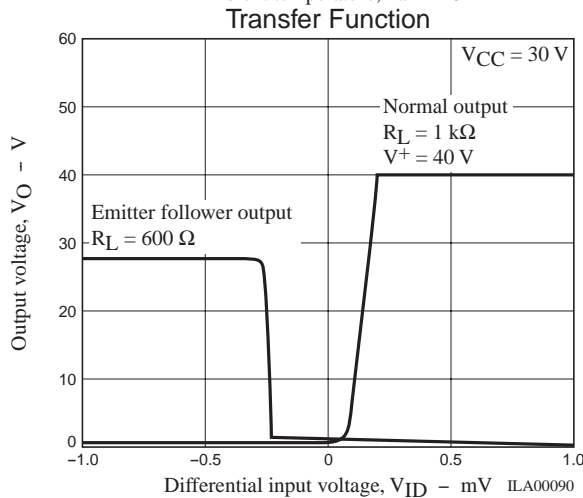
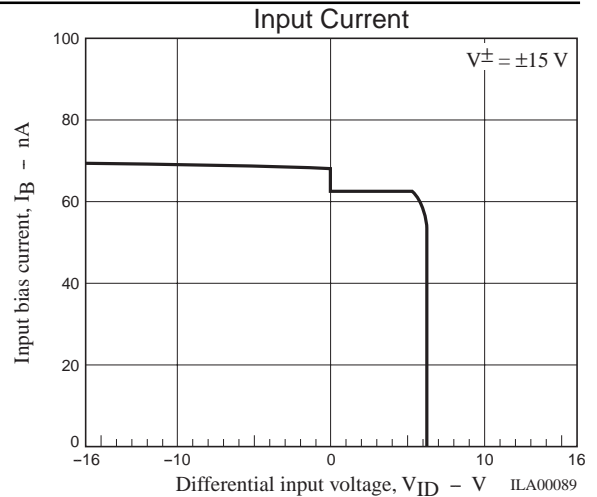
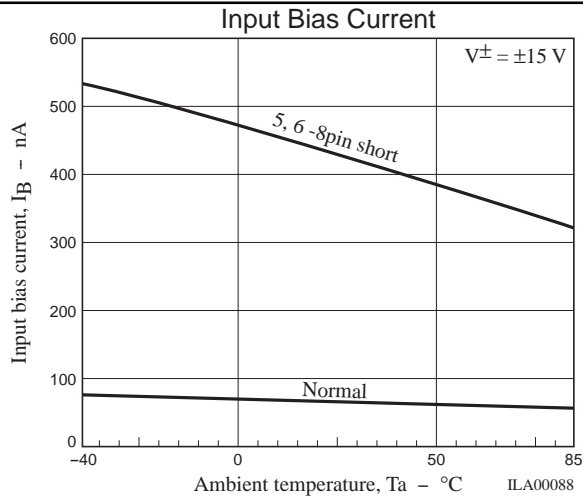
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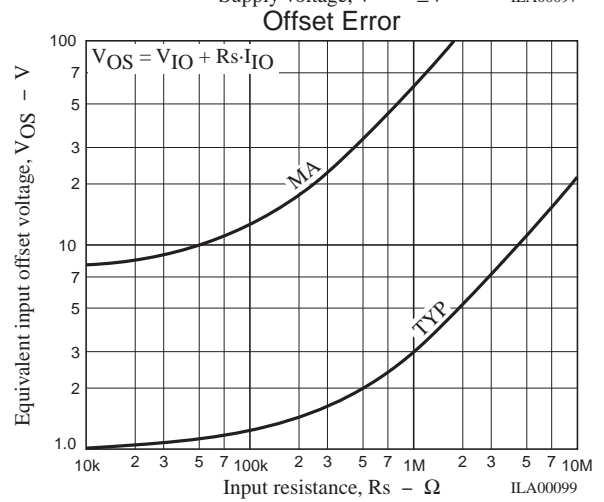
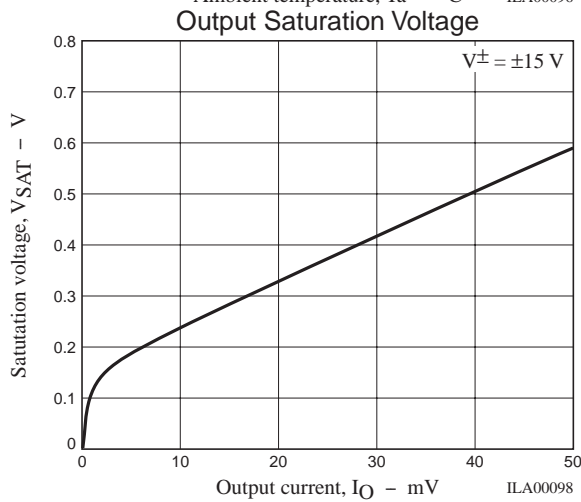
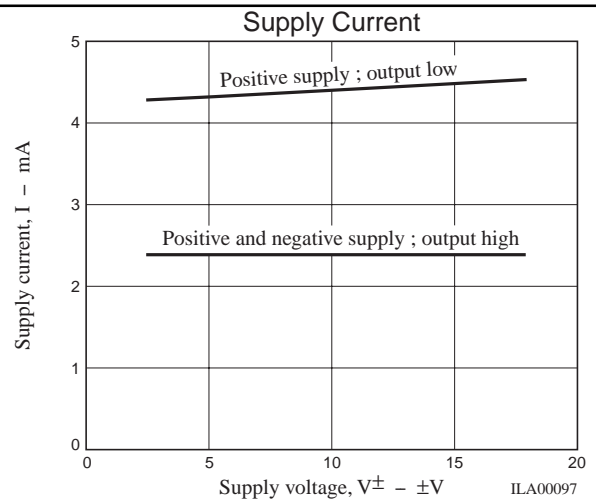
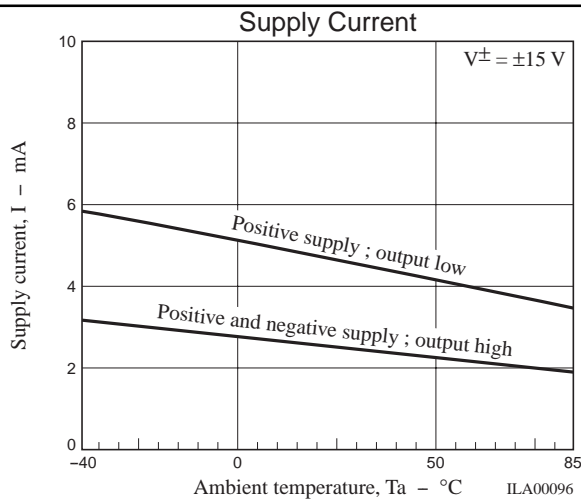
Typical Characteristics at  $T_a = 25^\circ\text{C}$ , TYP



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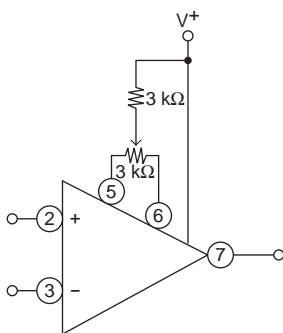






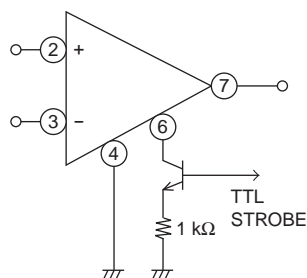
## Typical Connection and Applications

OFFSET VOLTAGE NULL CIRCUIT



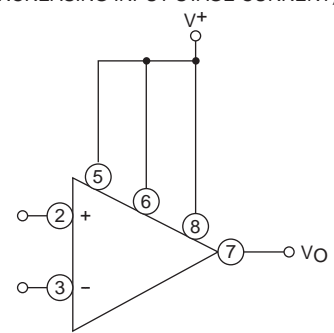
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STROBING CIRCUIT



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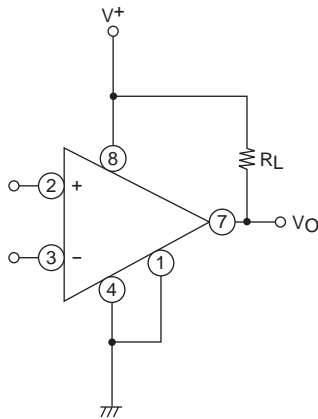
FAST RESPONSE CIRCUIT  
(INCREASING INPUT STAGE CURRENT)



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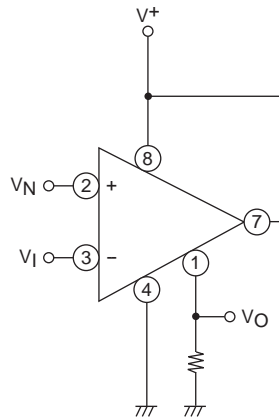
# LA6311M

OPEN COLLECTOR OUTPUT



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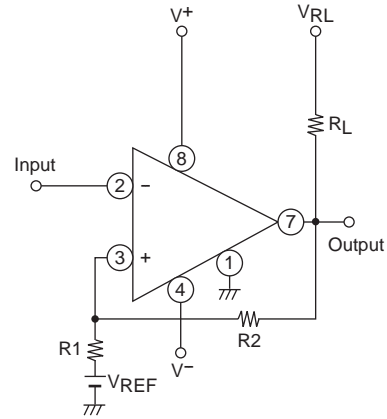
EMITTER FOLLOWER OUTPUT



Input polarity is reversed when 1pin (GND) is used as an output.  
 $V_N > V_I \rightarrow V_O : \text{Low}$

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COMPARATOR with HYSTERESIS CIRCUIT



Threshold voltage ( $V_{TH}$ )

$$V_{TH} (\text{high}) = V_{REF} + (V_{RL} - V_{REF}) \frac{R1}{RL + R2 + R1}$$

$$V_{TH} (\text{low}) = V_{REF} + (V_{RL} - V_{OL}) \frac{R1}{R1 + R2}$$

( $V_{RL} > V_{REF} ; V_{RL} > V_{OL}$ )

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