



LA7357

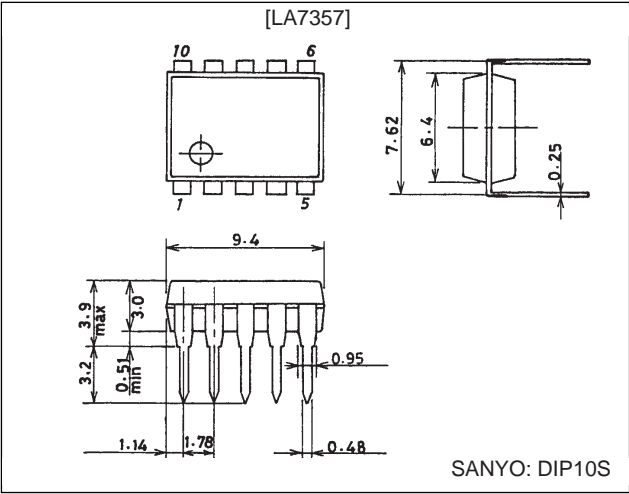
PAL/SECAM Discrimination Circuit for VHS VCRs

Overview

The LA7357 can be used as a PAL/SECAM discrimination IC. Since no ceramic resonator or tank circuit is required, only a small number of external components are used, and the LA7357 can contribute to reduced mounting areas and lower system costs.

Package Dimension

unit: mm  
3098B-DIP10S



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		7.0	V
Allowable power dissipation	P <sub>d</sub> max	Ta ≤ 65 °C	120	mW
Operating temperature	T <sub>opr</sub>		-10 to +65	°C
Storage temperature	T <sub>stg</sub>		-40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub>		5.0	V
Operating voltage range	V <sub>CC</sub> op		4.8 to 5.5	V

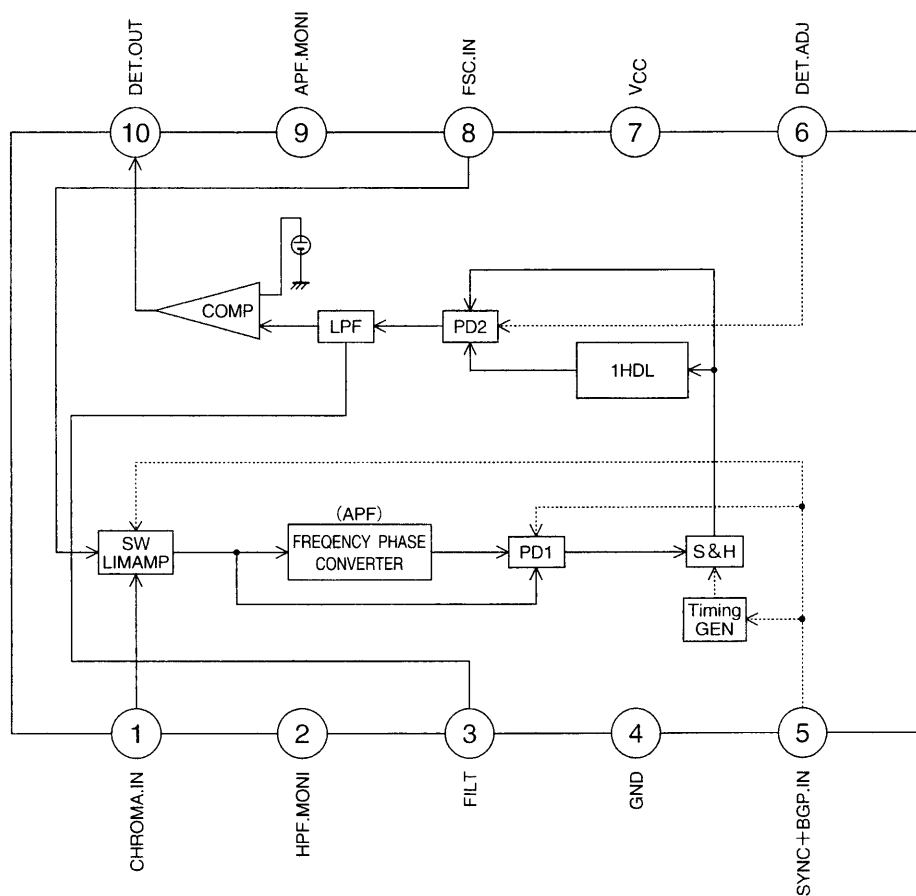
**Operating Characteristics at  $T_a = 25^{\circ}\text{C}$ ,  $V_{CC} = 5\text{ V}$** 

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	$I_{CC1}$	Pin 5 = ground, pin 7 influx current: T4 output	7.0	10.0	13.0	mA
	$I_{CC2}$	Pin 5 = $V_{CC}$ , pin 7 influx current: T4 output	7.5	10.5	13.5	mA
BGP threshold level	BTH	The pin 5 voltage when the pin 2 output appears when slowly raising the voltage applied to pin 5 from 0 V. The input signal should be 300 mVp-p: T2 output	2.2	2.5	2.8	V
SYNC threshold level	STH	The pin 5 voltage when the pin 2 output appears when slowly lowering the voltage applied to pin 5 from 5 V. The input signal should be 300 mVp-p: T2 output	0.6	0.8	1.0	V
Input limiter amplifier gain	LIMG	Stipulated as the output ratio when a 10 mVp-p amplitude sine wave is input to pin 1: T2 output	9	12	15	dB
Input limiter amplifier level	LIMD	Measure the output amplitude when a 300 mVp-p amplitude sine wave is input to pin 1: T2 output	150	190	230	mVp-p
Comparator hysteresis high-level voltage	Comp H	The V1 level when T1 switches from low to high when slowly raising V1 from 0 V: T1 output	2.7	3.0	3.3	V
Comparator hysteresis low-level voltage	Comp L	The V1 level when T1 switches from high to low when slowly lowering V1 from 5 V: T1 output	2.0	2.3	2.6	V
DET-OUT output high-level voltage	DETH	With a 2-k $\Omega$ load: T1 output	3.6	4.0	4.4	V
DET-OUT output low-level voltage	DETL	With a 2-k $\Omega$ load: T1 output	0	0.2	0.4	V

**Switching Conditions**

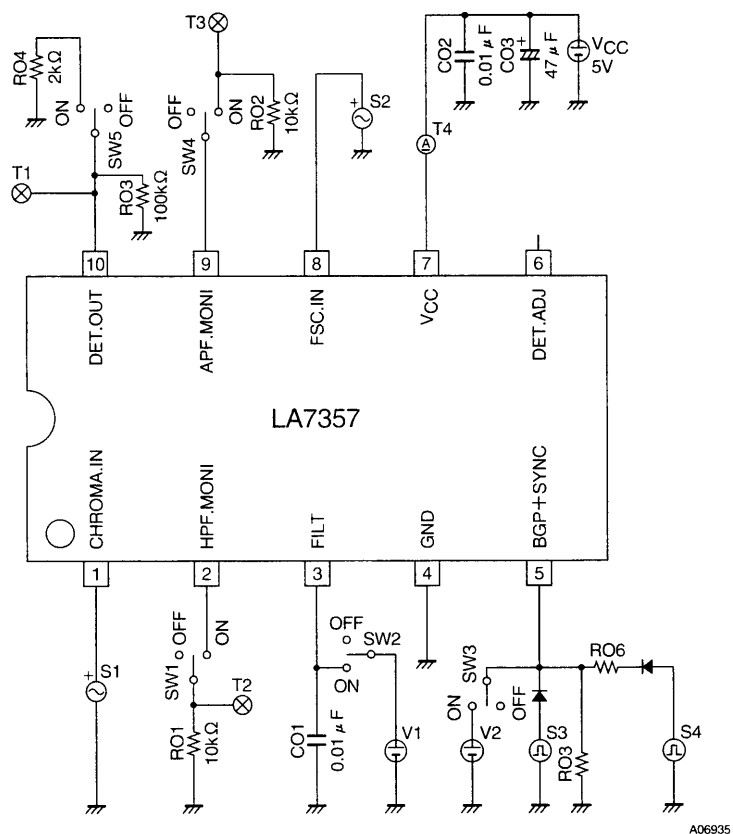
Symbol	Input signal		Input pulse		Applied voltage		Switch states				
	S1	S2	S3	S4	V1	V2	SW1	SW2	SW3	SW4	SW5
$I_{CC1}$	No signal	No signal	0 V	0 V			Off	Off	Off	Off	Off
$I_{CC2}$	No signal	No signal	5 V	5 V			Off	Off	Off	Off	Off
BTH	Sig.1	No signal	0 V	0 V		Variable DC level	On	Off	On	Off	Off
STH	No signal	Sig.1	0 V	0 V		Variable DC level	On	Off	On	Off	Off
LIMG	Sig.1	No signal	5 V	0 V			On	Off	Off	Off	Off
LIMD	Sig.1	No signal	5 V	0 V			On	Off	Off	Off	On
Comp H	No signal	No signal	No signal	No signal	Variable DC level		Off	On	Off	Off	On
Comp L	No signal	No signal	No signal	No signal	Variable DC level		Off	On	Off	Off	On
DETH	Sig.2	Sig.1	P2	P1			Off	Off	Off	Off	On
DETL	Sig.3	Sig.1	P2	P1			Off	Off	Off	Off	On

# Block Diagram



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# Test Circuit



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## Pin Functions

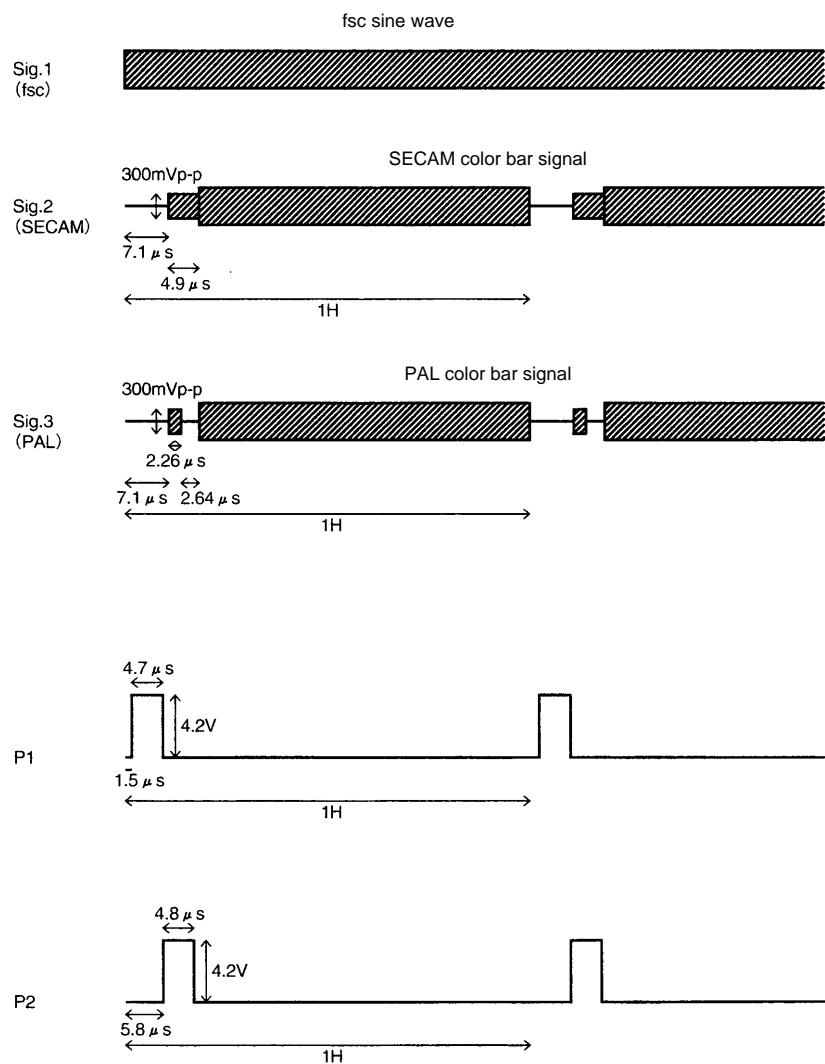
Pin No.	Pin	Pin Functions	Equivalent circuit
1	CHROMA-IN	<ul style="list-style-type: none"> <li>Chrominance signal input. This pin can handle burst (or unmodulated carrier for SECAM input) signal amplitudes of between 50 and 800 mVp-p.</li> </ul>	<p style="text-align: right;">A06936</p>
2	HPF.MONI	<ul style="list-style-type: none"> <li>High-pass filter output monitor</li> </ul> <p>To avoid interference between pin 1 and pin 3, this pin should be connected to <math>V_{CC}</math> during normal operation.</p>	<p style="text-align: right;">A06937</p>
3	FILTER	<ul style="list-style-type: none"> <li>Phase comparator output</li> </ul> <p>This signal is smoothed with an external capacitor. The smoothed level will be: 2.0 V or lower for PAL 3.5 V or higher for SECAM or MESECAM.</p>	<p style="text-align: right;">A06938</p>
4	GND		
5	SYNC+BGP	<ul style="list-style-type: none"> <li>BGP + SYNC input</li> </ul> <p>The input level is a 1.0- to 2.0-V rising pulse (┐) during the SYNC period, and a 3.0- to 4.5-V rising pulse (┐) during the BGP period. Note that since a combined BGP and C.SYNC pulse (┐) is output from the Y/C IC when the LA7357 is used in combination with a Sanyo single-chip Y/C IC (any one of the LA7430, LA7435, or LA71520) no external component will be required on pin 5.</p>	<p style="text-align: right;">A06939</p>
6	DET-ADJ	<ul style="list-style-type: none"> <li>Discrimination sensitivity adjustment pin</li> </ul> <p>The discrimination is shifted towards PAL as the pin voltage is increased, and towards SECAM as the pin voltage is lowered. This pin is normally left open.</p>	<p style="text-align: right;">A06940</p>
7	$V_{CC}$		

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Pin No.	Pin	Pin Functions	Equivalent circuit
8	FSC-IN	<ul style="list-style-type: none"> <li>PAL fsc (4.43 MHz) input</li> </ul> <p>This pin can handle inputs with amplitude between about 300 and 800 mVp-p.</p>	<p>(100 <math>\mu</math> A)</p> <p>A06941</p>
9	AFP.MONI	<ul style="list-style-type: none"> <li>APF output monitor</li> </ul> <p>This pin must be connected to <math>V_{CC}</math> to prevent interference between pins 8 and 10.</p>	<p>(50 <math>\mu</math> A)</p> <p>A06942</p>
10	DET-OUT	<ul style="list-style-type: none"> <li>Discrimination output</li> </ul> <p>This pin outputs a high level (4.2 V) for SECAM or MESECAM inputs, and a low level (close to 0 V) for PAL inputs.</p>	<p>A06943</p>

## Test Input Signals and Pulses



A06944

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