

Electrical Characteristics at Ta = 25°C

Parameter		Symbol			Conditions				Ratings			Unit
									min	typ	max	
[Playback Mode]					T15: 5.0 V, T13: OPEN, T7: OPEN	TRCK	HA	SW30 MUTE				
Current drain		I _{CCP}			Pin 15 influx current	OPEN	0	0	24	30	36	mA
Voltage gain	SP L CH1	VG _{P1}	T20A	T10A	V _{IN} = 38 mVp-p, f = 1 MHz	OPEN	0	0	54.0	57.0	60.0	dB
	SP H CH2	VG _{P2}	T23A	T10A		OPEN	0	2.5	54.0	57.0	60.0	dB
	EP L CH3	VG _{P3}	T27A	T10A		OPEN	5.0	0	56.0	59.0	62.0	dB
	EP H CH4	VG _{P4}	T30A	T10A		OPEN	5.0	2.5	56.0	59.0	62.0	dB
Voltage gain differential 1		VG _{P1}	–	–	VG _{P1} – VG _{P2}	–	–	–	–1	0	+1	dB
Voltage gain differential 2		VG _{P2}	–	–	VG _{P3} – VG _{P4}	–	–	–	–1	0	+1	dB
Inter-mode gain difference		VG _{P EP-SP}	–	–	VG _{P3} – VG _{P1}	–	–	–	1	2	3	dB
Equivalent input noise voltage	CH1	V _{NIN1}	T20A	T10A	After the 1.1-MHz LPF $\frac{V_{OUT}}{VG_{P1, 2, 3, 4}}$	OPEN	0	0	–	1.1	1.5	μVrms
	CH2	V _{NIN2}	T23A	T10A		OPEN	0	2.5	–	1.1	1.5	μVrms
	CH3	V _{NIN3}	T27A	T10A		OPEN	5.0	0	–	1.1	1.5	μVrms
	CH4	V _{NIN4}	T30A	T10A		OPEN	5.0	2.5	–	1.1	1.5	μVrms
Frequency characteristics	CH1	V _{fp1}	T20A	T10A	V _{IN} = 38 mVp-p f = 7 MHz $\frac{V_{OUT}}{VG_{P1, 2, 3, 4}}$ output ratio	OPEN	0	0	–2.5	0	–	dB
	CH2	V _{fp2}	T23A	T10A		OPEN	0	2.5	–2.5	0	–	dB
	CH3	V _{fp3}	T27A	T10A		OPEN	5.0	0	–2.5	0	–	dB
	CH4	V _{fp4}	T30A	T10A		OPEN	5.0	2.5	–2.5	0	–	dB
Second harmonic distortion	CH1	V _{HDP1}	T20A	T10A	V _{IN} = 38 mVp-p f = 4 MHz (8-MHz component)/(4-MHz component) output ratio	OPEN	0	0	–	–40	–35	dB
	CH2	V _{HDP2}	T23A	T10A		OPEN	0	2.5	–	–40	–35	dB
	CH3	V _{HDP3}	T27A	T10A		OPEN	5.0	0	–	–40	–35	dB
	CH4	V _{HDP4}	T30A	T10A		OPEN	5.0	2.5	–	–40	–35	dB
Maximum output level	CH1	V _{OMP1}	T20A	T10A	f = 1 MHz The output level when the third harmonic in the output is –30 dB	OPEN	0	0	1.0	1.2	–	Vp-p
	CH2	V _{OMP2}	T23A	T10A		OPEN	0	2.5	1.0	1.2	–	Vp-p
	CH3	V _{OMP3}	T27A	T10A		OPEN	5.0	0	1.0	1.2	–	Vp-p
	CH4	V _{OMP4}	T30A	T10A		OPEN	5.0	2.5	1.0	1.2	–	Vp-p
Crosstalk SP (Note 1)	CH1	V _{CR1}	T23A	T10A	V _{IN} = 38 mVp-p, f = 4 MHz $\frac{V_{OUT}}{VG_{P1, 2}}$	OPEN	0	0	–	–40	–35	dB
			T27A	T10A		OPEN	0	0	–	–40	–35	dB
			T30A	T10A		OPEN	0	0	–	–40	–35	dB
	CH2	V _{CR2}	T20A	T10A		OPEN	0	2.5	–	–40	–35	dB
			T27A	T10A		OPEN	0	2.5	–	–40	–35	dB
			T30A	T10A		OPEN	0	2.5	–	–40	–35	dB
Crosstalk EP (Note 1)	CH3	V _{CR3}	T23A	T10A	V _I = 38 mVp-p, f = 4 MHz $\frac{V_{OUT}}{VG_{P3, 4}}$	OPEN	5.0	0	–	–40	–35	dB
			T27A	T10A		OPEN	5.0	0	–	–40	–35	dB
			T30A	T10A		OPEN	5.0	0	–	–40	–35	dB
	CH4	V _{CR4}	T20A	T10A		OPEN	5.0	2.5	–	–40	–35	dB
			T27A	T10A		OPEN	5.0	2.5	–	–40	–35	dB
			T30A	T10A		OPEN	5.0	2.5	–	–40	–35	dB
Output DC offset	V _{ODC1}	–	T10	CH1-CH2	OPEN	–	0	–100	0	+100	mV	
					OPEN	0	2.5	–100	0	+100	mV	
	V _{ODC2}	–	T10	CH3-CH4	OPEN	–	0	–100	0	+100	mV	
					OPEN	5.0	2.5	–100	0	+100	mV	
	V _{ODC3}	–	T10	CH1-CH3	OPEN	0	–	–100	0	+100	mV	
					OPEN	5.0	0	–100	0	+100	mV	
	V _{ODC4}	–	T10	CH2-CH4	OPEN	0	–	–100	0	+100	mV	
					OPEN	5.0	2.5	–100	0	+100	mV	
V _{ODC5}	–	T10	CH1-CH4	OPEN	0	0	–100	0	+100	mV		
				OPEN	5.0	2.5	–100	0	+100	mV		
V _{ODC6}	–	T10	CH2-CH3	OPEN	0	2.5	–100	0	+100	mV		
				OPEN	5.0	0	–100	0	+100	mV		

Continued on the next page.

Note 1. With the input inductor L (8.2 μH) shorted.

2. Since the T4 (HA) control switch timing is synchronized with T6 (H-Sync), a T6 trigger (0 - 5 V - 0) must be input before measuring each of these items.

Continued from the preceding page.

Parameter	Symbol			Conditions				Ratings			Unit
		Input	Output		T2	T4	T5	min	typ	max	
				T15: 5.0 V, T13: OPEN, T7: OPEN	TRCK	HA	SW30 MUTE				
Enveloped detector output pin voltage	V _{ENV}		T8	The T8 DC voltage with no input	OPEN	0	0	0	0.4	0.8	V
Enveloped detector voltage SP1	V _{ENVSP1}	T20A	T8	f = 4 MHz T10A: Adjusted to 300 mV p-p	OPEN	0	0	2.1	2.6	3.1	V
Enveloped detector voltage SP2	V _{ENVSP2}	T20A	T8	f = 4 MHz T10A: Adjusted to 600 mV p-p	OPEN	0	0	4.5	4.8	5.0	V
Enveloped detector voltage EP1	V _{ENVEP1}	T27A	T8	f = 4 MHz T10A: Adjusted to 200 mV p-p	OPEN	5.0	0	2.0	2.6	3.0	V
Enveloped detector voltage EP2	V _{ENVEP2}	T27A	T8	f = 4 MHz T10A: Adjusted to 450 mV p-p	OPEN	5.0	0	4.5	4.8	5.0	V
Comparator output voltage 1	V _{COMP1}	T20A	T3	f = 4 MHz, V _{IN} = 38 mVp-p The T3 DC voltage	5.0	0	0	–	0.4	0.7	V
Comparator output voltage 2	V _{COMP2}	T20A	T3	f = 4 MHz, V _{IN} = 38 mVp-p The T3 DC voltage	5.0	5.0	0	4.5	4.8	–	V
Playback mode on switching transistor on resistance	R _{PON17}		P-17	The difference in the DC measurement for 1-mA and 2-mA influx currents	–	–	–	–	4.0	6.0	
	R _{PON18}		P-18		–	–	–	–	4.0	6.0	
Playback mode mode switching transistor on resistance	R _{PON21}		P-21	The difference in the DC measurement for 1-mA and 2-mA influx currents	OPEN	5.0	–	–	4.0	6.0	
	R _{PON24}		P-24		OPEN	5.0	–	–	4.0	6.0	
	R _{PON26}		P-26		OPEN	0	–	–	4.0	6.0	
	R _{PON29}		P-29		OPEN	0	–	–	4.0	6.0	
Trick 1 threshold level	TR1-1		T2	Normal → Trick1	*	–	–	3.2	–	5.0	V
	TR1-2		T2	Trick1 → Normal	*	–	–	1.2	–	2.8	V
Trick 2 threshold level	TR2-1		T2	Normal → Trick2	*	–	–	0.0	–	0.8	V
	TR2-2		T2	Trick2 → Normal	*	–	–	1.2	–	2.8	V
HAPB threshold level	HAP-1		T4	SP → EP	–	*	–	1.8	–	5.0	V
	HAP-2		T4	EP → SP	–	*	–	0.0	–	1.4	V
SW30 threshold level	SW30-1		T5	Lch → Hch	–	–	*	1.2	–	5.0	V
	SW30-2		T4	Hch → Lch	–	–	*	0.0	–	0.8	V
					T2	T4	T5				
[Record Mode]				T15: 5.0 V, T2: OPEN, T6: 5.0 V, T7: 5.0 V	REC Adj2	HA	SW30 MUTE				
Current drain	I _{CCR}			The pin 15 influx current	OPEN	0	0	44	55	66	mA
AGC amplifier output level	V _{RSP}	T11A	T21A	f = 4 MHz V _{IN} = 200 mVp-p	OPEN	0	0	147	156	165	mVp-p
	V _{REP}	T11A	T26A		OPEN	5.0	0	116	123	130	mVp-p
Inter-mode gain difference	V _{G R}	–	–	V _{RSP} /V _{REP}	–	–	–	1.30	2.05	2.80	dB
AGC amplifier control characteristics 1	V _{AGC1-SP}	T11A	T21A	f = 4 MHz, V _{IN} = 400 mVp-p The output level/V _{RSP} , EP ratio	OPEN	0	0	–	0.5	1.0	dB
	V _{AGC1-EP}	T11A	T26A		OPEN	5.0	0	–	0.5	1.0	dB
AGC amplifier control characteristics 2	V _{AGC2-SP}	T11A	T21A	f = 4 MHz, V _{IN} = 100 mVp-p The output level/V _{RSP} , EP ratio	OPEN	0	0	–1.0	–0.5	–	dB
	V _{AGC2-EP}	T11A	T26A		OPEN	5.0	0	–1.0	–0.5	–	dB
AGC amplifier frequency characteristics	V _{FRS}	T11A	T21A	f = 1 MHz, 7 MHz, V _{IN} = 100 mVp-p The 7 MHz/1 MHz output ratio	OPEN	0	0	–1.0	–0.0	+1.0	dB
	V _{FRE}	T11A	T26A		OPEN	5.0	0	–1.0	–0.0	+1.0	dB
AGC amplifier second harmonic distortion	V _{HDRS}	T11A	T21A	f = 4 MHz, V _{IN} = 200 mVp-p The (8 MHz component)/(4 MHz component) output ratio	OPEN	0	0	–	–45	–40	dB
	V _{HDRE}	T11A	T21A		OPEN	5.0	0	–	–45	–40	dB
AGC amplifier maximum output level	V _{OMRS}	T11A	T21A	f = 4 MHz, The output level for which the second harmonic is –35 dB	Adj.	0	0	20	22	–	mAp-p
	V _{OMRE}	T11A	T26A		Adj.	5.0	0	20	22	–	mAp-p
AGC amplifier muting attenuation	V _{MRS}	T11A	T21A	f = 4 MHz, V _I = 200 mVp-p The output level/V _{RSP} , EP ratio	OPEN	0	5.0	–	–45	–40	dB
	V _{MRE}	T11A	T26A		OPEN	5.0	5.0	–	–45	–40	dB

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Parameter	Symbol			Conditions				Ratings			Unit
		Input	Output		T2	T4	T5	min	typ	max	
[Record Mode]				T15: 5.0 V, T2: OPEN, T6: 5.0 V, T7: 5.0 V	REC Adj2	HA	SW30 MUTE				
AGC amplifier relative cross modulation level	V _{CYS}	T10A	T21A	T10A: f = 629 kHz, V _{IN} = 360 mVp-p T11A: f = 4 MHz, V _{IN} = 200 mVp-p (4 MHz ±629 kHz)/(4 MHz) output ratio	OPEN	0	0	–	–45	–40	dB
	V _{CYE}	T11A	T26A		OPEN	5.0	0	–	–45	–40	dB
Record mode mode switching transistor on resistance	R _{RON17}		P-17	The difference in the DC measurement for 1-mA and 2-mA influx currents	OPEN	5.0	–	–	4.0	6.0	
	R _{RON18}		P-18		OPEN	0	–	–	4.0	6.0	
	R _{RON21}		P-21		OPEN	5.0	–	–	4.0	6.0	
	R _{RON24}		P-24		OPEN	5.0	–	–	4.0	6.0	
	R _{RON26}		P-26		OPEN	0	–	–	4.0	6.0	
	R _{RON29}		P-29		OPEN	0	–	–	4.0	6.0	
HA record threshold level	HAR-1		T4	SP → EP	–	*	–	1.8	–	5.0	V
	HAR-2		T4	EP → SP	–	*	–	0.0	–	1.4	V
Record MUTE threshold level	MUTE-1		T5	MUTE OFF → ON	–	–	*	3.4	–	5.0	V
	MUTE-2		T5	MUTE ON → OFF	–	–	*	0.0	–	3.0	V
Record/playback threshold level	SW REC/PB			T7: control voltage	–	–	–	2.2	–	5.0	V

Notes 3. Measure with a DC voltage of about 1.8 V applied to the AGC detector filter pin (pin 12) and with the AGC amplifier gain fixed.

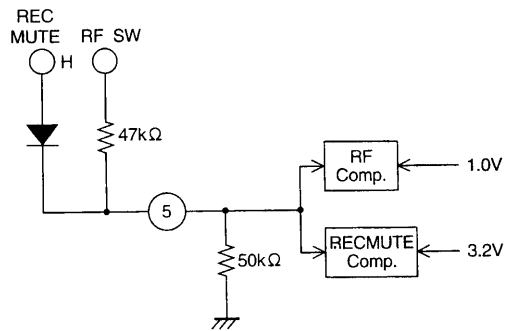
4. Adjust the output level by applying a DC voltage to T13 (REC CUR.Adj2)

5. Use a resistor with a ±1.0% tolerance between pins 14 and 15.

Usage Notes

1. Control Pin Logic

RF SW, REC MUTE: pin 5



Playback mode

If the pin 5 DC voltage is < 1.0 V: Lch

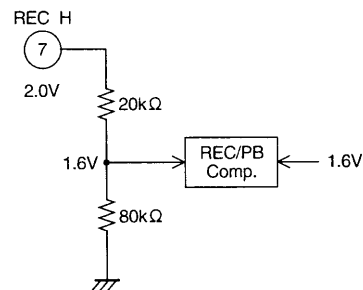
If the pin 5 DC voltage is > 1.0 V: Hch

Record mode

If the pin 5 DC voltage is < 3.2 V: Muting will be off

If the pin 5 DC voltage is > 3.2 V: Muting will be on

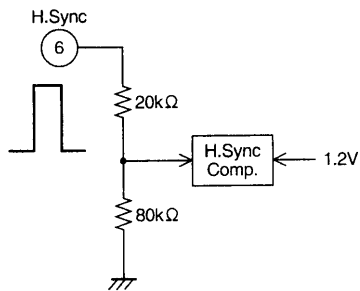
Record/playback mode switching: pin 7



If the pin 7 DC voltage is < 2.0 V: Playback mode

If the pin 7 DC voltage is > 2.0 V: Record mode

H.Sync input: pin 6

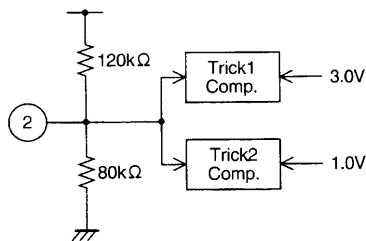


If the pin 6 DC voltage is > 1.5 V: Currently the signal is in an H.Sync period

*: Playback mode: Used for switching timing in SP search.

Record mode: Used as the record amplifier AGC synchronization block gate pulse.

(4) Playback trick mode switching: pin 2



If the pin 2 DC voltage is > 3.0 V: Trick 1

If the pin 2 DC voltage is < 1.0 V: Trick 2

If the pin 2 DC voltage is > 1.0 V and < 3.0 V: Normal

*: Normal mode: Two channels controlled (EP/SP) by pin 4: ON
Envelope comparator: OFF

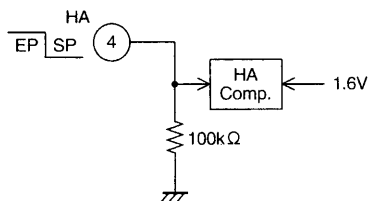
In trick 1 and 2 modes: All 4 channels: ON
Envelope comparator: ON

*: The difference between trick 1 and trick 2 is that:

Trick1 Envelope comparator (pin 3) output \rightarrow Servo (microcontroller) ^{or}
 \rightarrow Pin 4 HA \rightarrow SP search is performed in the HA switch path.

Trick2 Envelope comparator output \rightarrow SP search is performed in the HA switch path. (See the block diagram.)

HA SW (EP/SP mode switching): pin 4

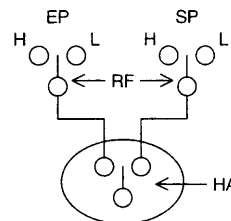


If the pin 4 DC voltage is < 1.6 V: SP mode

If the pin 4 DC voltage is > 1.6 V: EP mode

*: H.Sync synchronization for HA switching:

The switching of the HA SW circuit show in the figure at the right is synchronized with the H.Sync signal input to pin 6.
(Other EP/SP switching is performed in real time.)



Comp.OUT (pin 3)

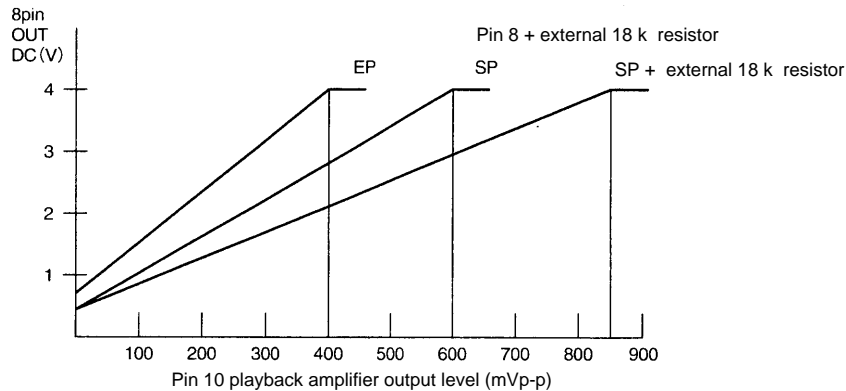
If the EP envelope is $> SP$: High (4.0 V or higher)

If the EP envelope is $< SP$: Low (0.7 V or lower)

2. Envelope Detector Characteristics: pin 8

The LA6529M includes an on-chip playback signal envelope detector circuit used to achieve automatic tracking adjustment with essentially linear characteristics.

Envelope Detector Characteristics (design target values) $f = 4 \text{ MHz}$

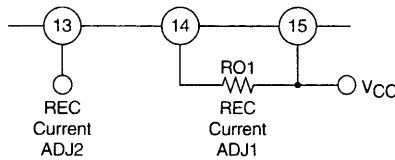


3. Record Amplifier Gain Control

The LA6529M achieves an adjustment-free record current by adding an AGC circuit in the record amplifier block. The record current can be modified using the circuit shown below.

(1) REC Current.Adj2: When open

The pin 13 DC level is set to $1/2 V_{CC}$ (about 2.5 V) by an internal bias and the record current is determined by RO1.



Design values: RO1: 1.5 k = 15.6 mAp-p (SP) (per channel)
= 12.3 mAp-p (EP)

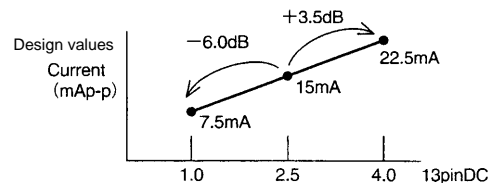
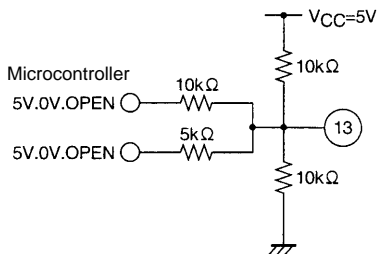
(2) REC Current.Adj2: When used

The value determined by RO1 can be adjusted from -6.0 dB to +3.5 dB by applying a control DC level (1 to 4 V) to pin 13.

(Reference)

The circuit below can be used to apply the DC control level to pin 13.

This allows 9 modes (1 to 4 V) to be applied.

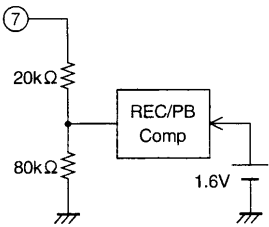
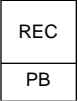
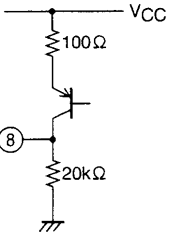
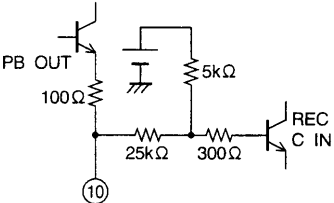
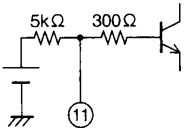
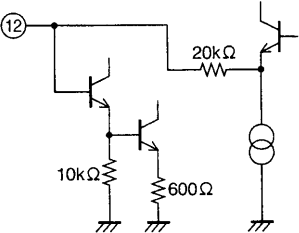
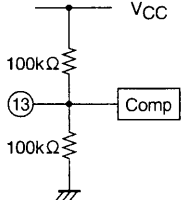


Pin Functions

Pin No.	Pin	Standard DC voltage (V)		Pin circuit	Notes						
1 19 22 28	PB Amp Second filter	PB	2.0								
		REC	3.6								
2	TRICK-H				<div>3.0 V 1.0 V</div> <table><tr><td>Trick1</td></tr><tr><td>NORMAL</td></tr><tr><td>Trick2</td></tr></table>	Trick1	NORMAL	Trick2			
Trick1											
NORMAL											
Trick2											
3	COMP-OUT	PB	High: 4.5 V or higher Low: 0.7 V or lower		EP > SP ENV: High						
		REC	OPEN								
4	HA (EP/SP)				<div>1.6 V</div> <table><tr><td>EP</td></tr><tr><td>SP</td></tr></table>	EP	SP				
EP											
SP											
5	RF-SW (REC-MUTE)				<div>SW30 REC MUTE</div> <table><tr><td>Hch</td><td>ON</td><td>3.2 (V)</td></tr><tr><td>Lch</td><td>OFF</td><td></td></tr></table> <div>1.0 (V)</div>	Hch	ON	3.2 (V)	Lch	OFF	
Hch	ON	3.2 (V)									
Lch	OFF										
6	H-SYNC				<div>1.5 V</div> <table><tr><td>Sync</td></tr><tr><td>H</td></tr><tr><td>L</td></tr></table>	Sync	H	L			
Sync											
H											
L											

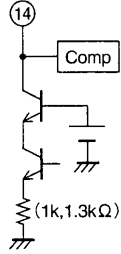
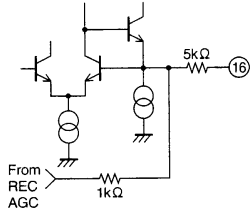
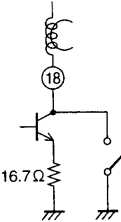
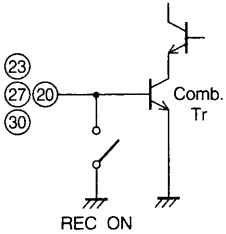
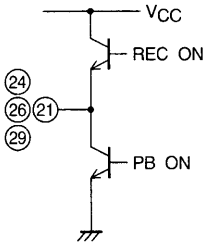
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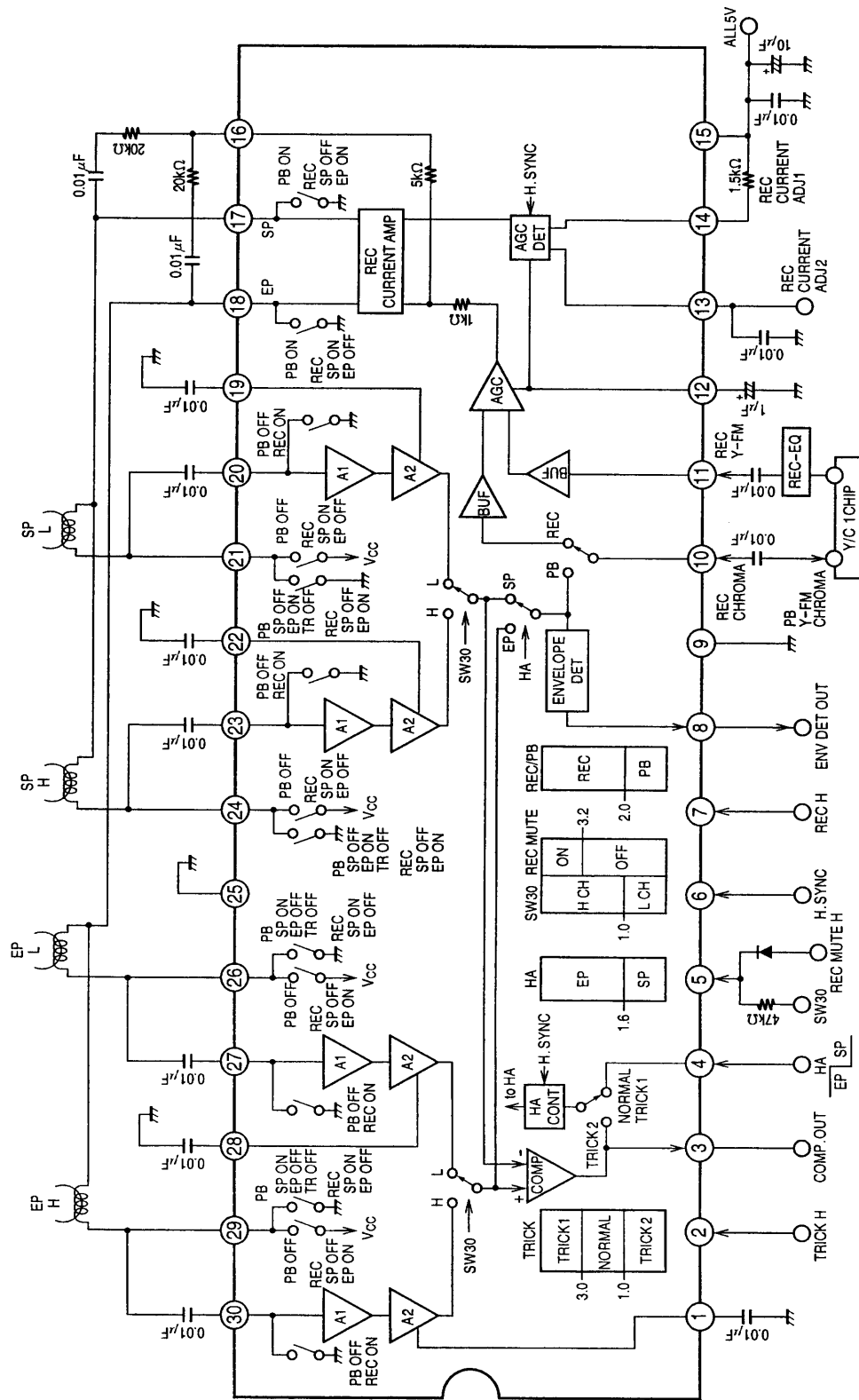
Pin No.	Pin	Standard DC voltage (V)		Pin circuit	Notes
7	REC-H	PB	0		
		REC	5		
8	ENV DET OUT	PB	Described in a separate document.		
		REC	0		
9	GND				
10	PB-OUT	PB	2.3		
	REC-C-IN	REC	3.6		
11	REC-Y-IN	REC	3.6		
12	AGC-FLT	PB	1.6		
		REC	1.6		
13	REC-CURRENT ADJ2	PB	2.5		4 V: +3.5 dB 2.5 V: ±0 dB (OPEN) 1 V: -6 dB
		REC	2.5		

Continued on the next page.

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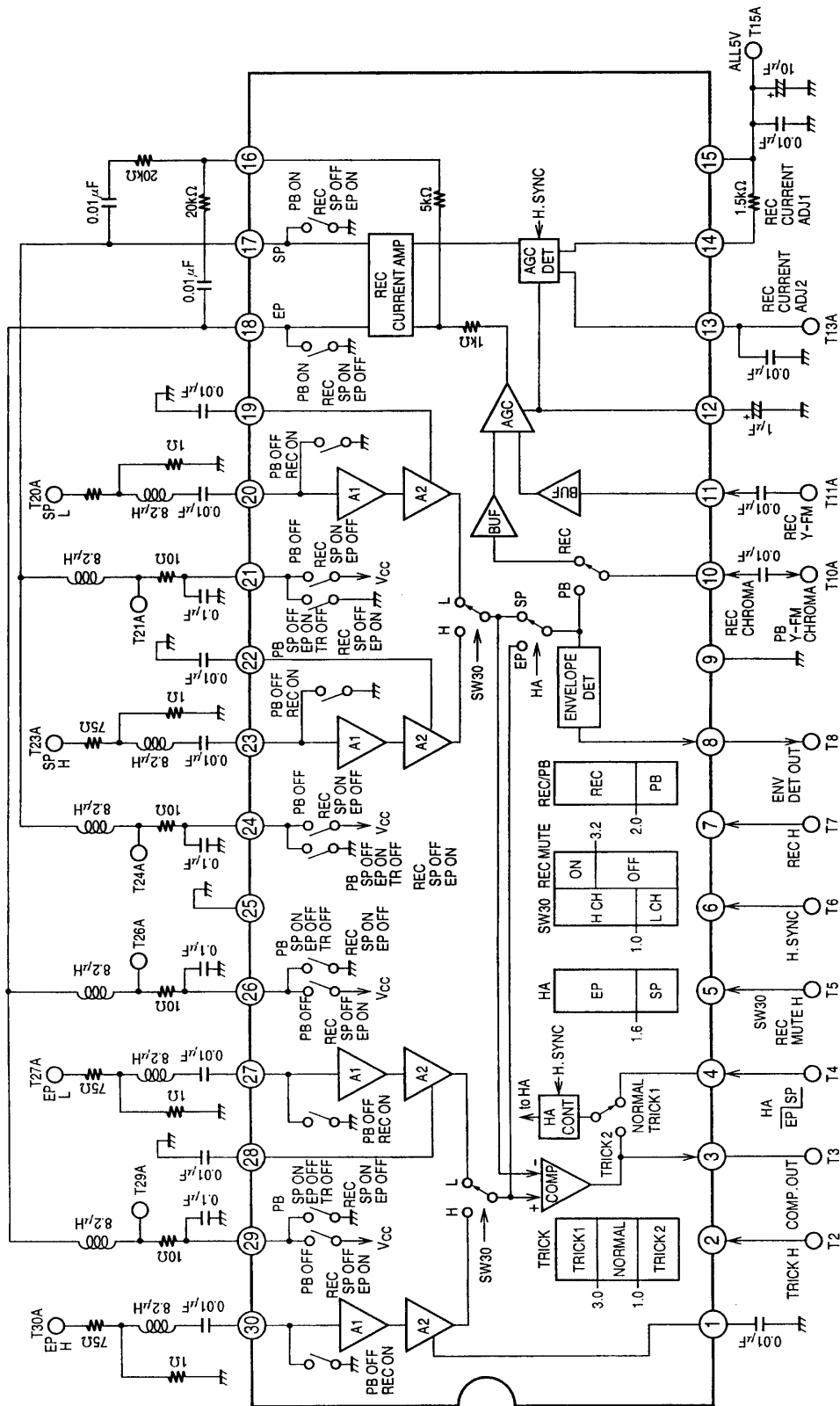
Pin No.	Pin	Standard DC voltage (V)		Pin circuit	Notes
14	REC-CURRENT ADJ1	PB	4.5		
		REC	5.0		
15	V _{CC}				
16	REC-BIAS	PB	2.5		
		REC	1.7		
17 18	REC-SP OUT REC-EP OUT	PB	0		
		REC	4.2		
20 23 27 30	SP-L-IN SP-H-IN EP-L-IN EP-H-IN	PB	0.7		
		REC	0		
21 24 26 29	SP-L-SW SP-H-SW EP-L-SW EP-H-SW	PB	0		
		REC	4.2		
25	PRE-GND				

Block Diagram



T00060

Test Circuit



T00061

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