



LA8522M

Audio Signal-Processing IC with I/O Switching

Overview

The LA8522M is an I/O switching audio signal-processing IC for use in facsimile units and telephones. It integrates a crosspoint switch, a BTL power amplifier, an electronic volume control, a microphone amplifier, and other functions on a single chip.

Applications

Personal facsimile units and telephones

Functions

- Crosspoint switch (equivalent to an 4×4 switch)
- BTL power amplifier
- Electronic volume control
- Output level switching (ATT1: 0, -4, -8, -12 dB, ATT2: 0, -6 dB)
- Serial interface

Features

- Built-in BTL power amplifier (8 to 32 Ω load): $V_{CC} = 5\text{ V}$, $R_L = 16\ \Omega$, $P_{omax} = 250\text{ mW}$

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		7	V
Allowable power dissipation	$P_{d\text{ max}}$	$T_a \leq 70^\circ\text{C}$ (Mounted on a glass-epoxy board: $114.3 \times 76.1 \times 1.6\text{ mm}^3$)	550	mW
Operating temperature	T_{opr}		-20 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +150	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Allowable operating supply voltage range	V_{CCop}		4.5 to 6.0	V

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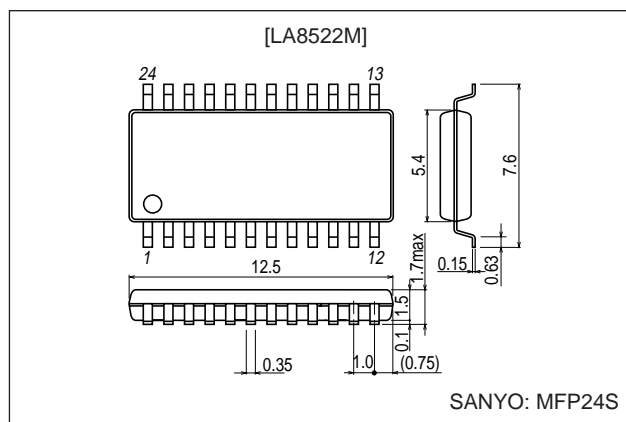
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- Built-in electronic volume (seven 4.0 dB steps)
- Two output level switching circuits (4 positions and 2 positions)
- Crosspoint switch that supports mixing

Package Dimensions

unit: mm

3112A-MFP24S



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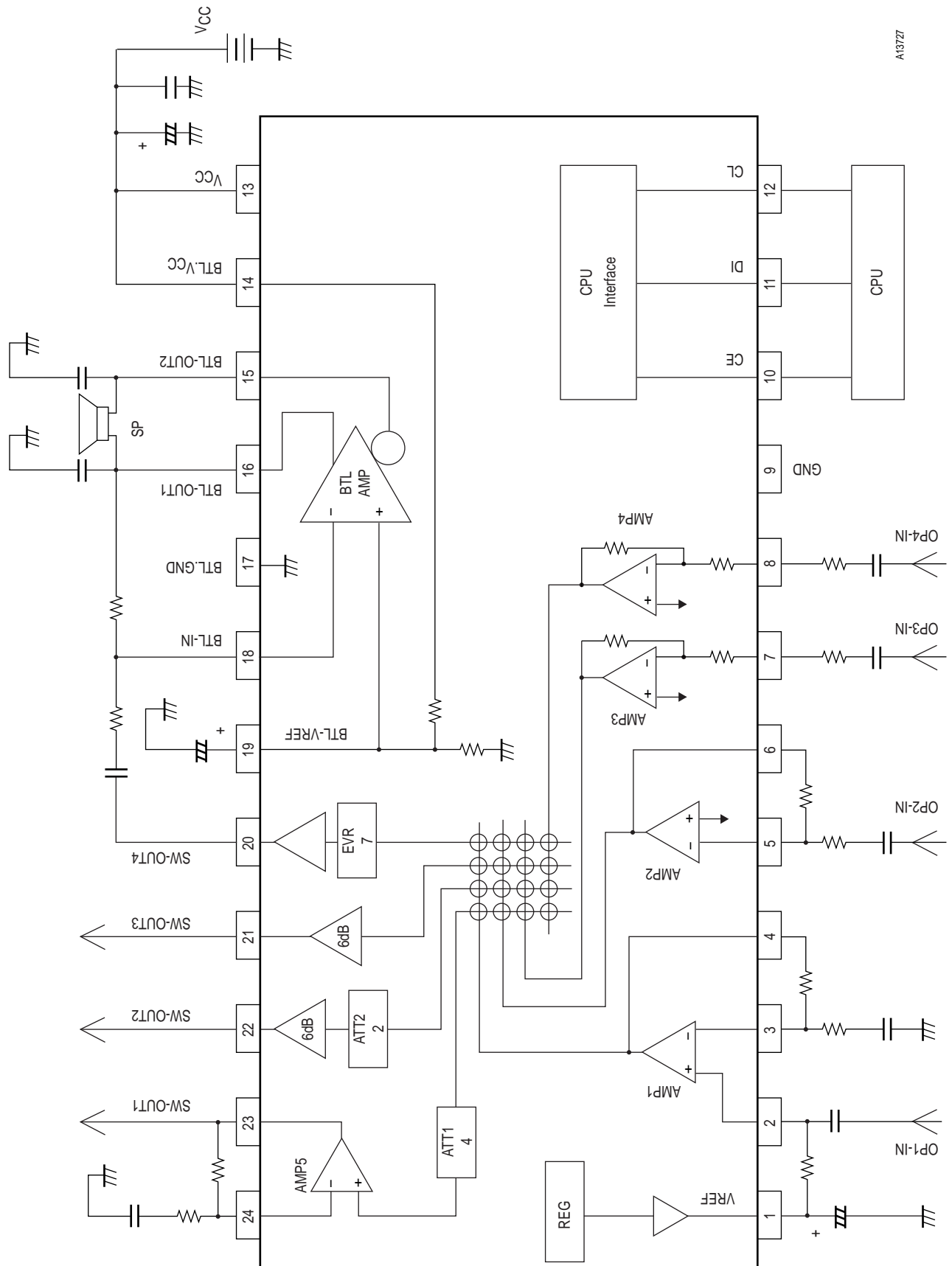
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LA8522M

Electrical Characteristics at Ta = 25°C, VCC = 5 V, fin = 1 kHz, RL = 10 kΩ

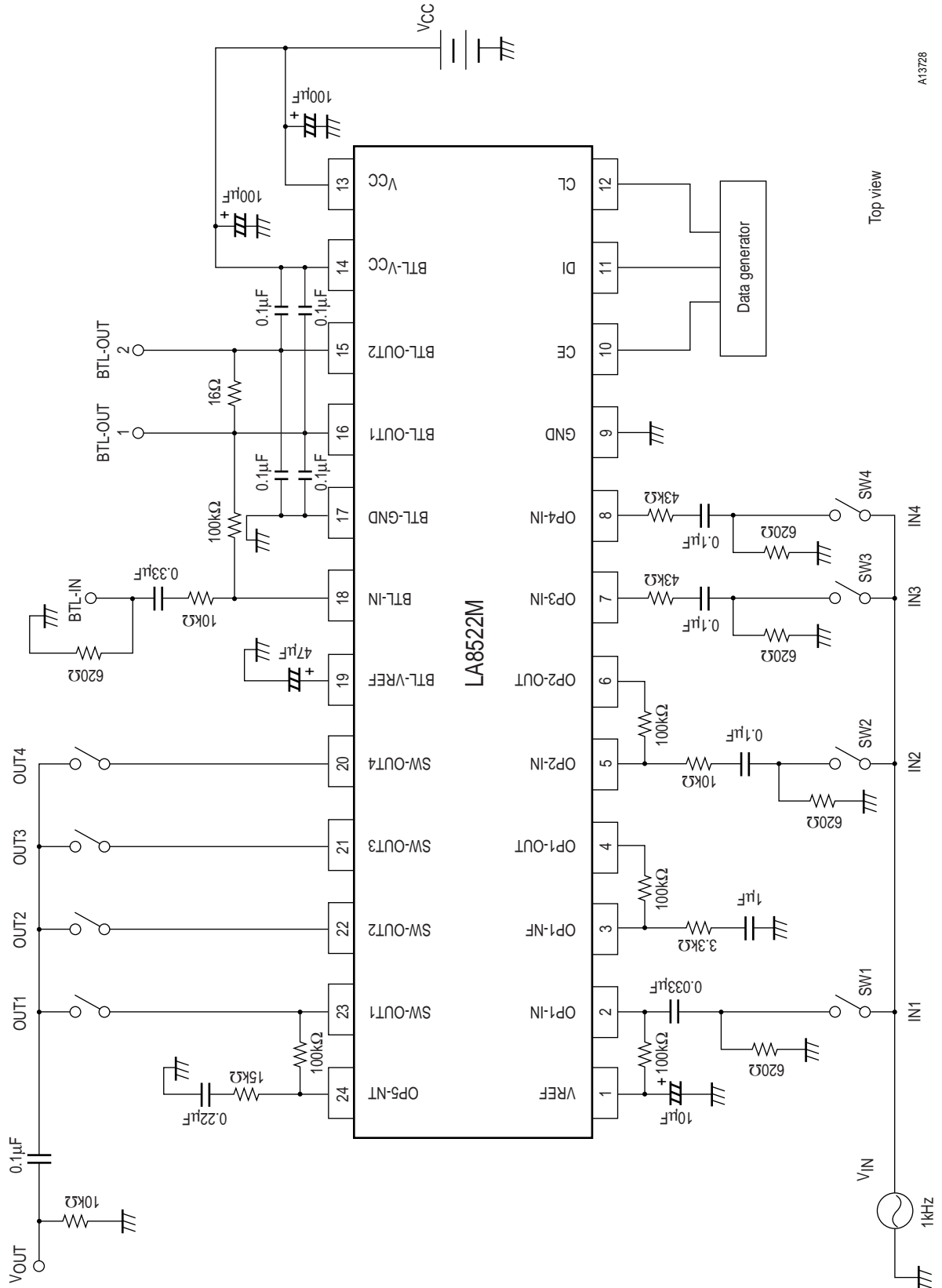
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Crosspoint switch]						
Voltage gain	Gsw	Vin = −14 dBV	−2.5	−0.5	1.5	dB
Maximum input level	Vimax	THD = 1.5 %	−14	−10		dBV
Output noise voltage	Nosw	20 to 20 kHz		15	60	μVrms
[AMP1]						
Voltage gain	G1	Vin = −43 dBV	28.2	29.2	30.2	dB
Output total harmonic distortion	THD1	Vin = −43 dBV		0.15	1.5	%
Equivalent input noise voltage	Niamp1	Rg = 620 Ω, 20 to 20 kHz		2.0	7.0	μVrms
[AMP2]						
Voltage gain	G2	Vin = −34 dBV	18.2	19.2	20.2	dB
Output total harmonic distortion	THD2	Vin = −34 dBV		0.16	1.5	%
[AMP3]						
Output level	VO3	Vin = −14 dBV, IN (7), OUT (22), sw (101101) on	−10.8	−8.3	−5.8	dBV
Output total harmonic distortion	THD3	Vin = −14 dBV, IN (7), OUT (22), sw (101101) on		0.31	1.5	%
[AMP4]						
Output level	VO4	Vin = −14 dBV, IN (8), OUT (21), sw (110111) on	−10.7	−8.2	−5.7	dBV
Output total harmonic distortion	THD4	Vin = −14 dBV, IN (8), OUT (21), sw (110111) on		0.30	1.5	%
[AMP5]						
Output level	VO5	Vin = −26 dBV, IN (7), OUT (23), sw (010001) on	−11.5	−9.0	−6.5	dBV
Output total harmonic distortion	THD5	Vin = −26 dBV, IN (7), OUT (23), sw (010001) on		0.17	1.5	%
Maximum voltage gain						
AMP1	G1max		30			dB
AMP2	G2max		25			dB
AMP3	G3max		20			dB
AMP4	G4max		18	20		dB
AMP5	G5max		18	20		dB
Attenuator attenuation 1-1	Att1-1	Address (010101)	3.5	4.2	4.9	dB
Attenuator attenuation 1-2	Att1-2	Address (011001)	7.5	8.2	8.9	dB
Attenuator attenuation 1-3	Att1-3	Address (011101)	11.7	12.4	13.1	dB
Attenuator attenuation 2-1	Att2-1	Address (000101)	5.5	6.2	6.9	dB
Electronic volume control output level	VOevr	Vin = −42 dBV, IN (2), OUT (20), sw (010001) on	−14.3	−12.2	−10.3	dBV
Electronic volume control step size	Wevr	Vin = −42 dBV, IN (2), OUT (20), sw (010010) on	3.1	4.0	4.9	dB
Electronic volume control output noise voltage	NOevr	20 to 20 kHz, OUT (20)		25	60	μVrms
[BTL Power Amplifier]						
Voltage gain	VGSPW	Vin = −20 dBV, RL = 16 Ω	18.1	19.6	21.1	dB
Maximum voltage gain	VGp max		30			dB
Total harmonic distortion	THDpw	Vin = −30 dBV, RL = 16 Ω		0.8	1.5	%
Maximum BTL output power	Po max	THD = 10 %, RL = 16 Ω	250	400		mW
Ripple rejection ratio	SVRR	Rg = 620 Ω, frin = 100 Hz, Vrin = −20 dBV, RL = 16 Ω	40	50		dB
Output noise voltage	VNOpw	Rg = 620 Ω, 20 to 20 kHz, RL = 16 Ω		23	60	μVrms
[CPU Interface]						
Clock frequency	Fck				500	kHz
Input signal high level	VH		2.1			V
Input signal low level	VL				1.0	V
[VREF and Current Drain]						
Internal reference voltage (the pin 10 voltage)	Vref		2.09	2.26	2.41	V
Quiescent current 1	Icco1	With the BTL power amplifier on and the crosspoint switch off		12.5	20	mA
Quiescent current 2	Icco2	With the BTL power amplifier off and the crosspoint switch off		7	11	mA

Block Diagram



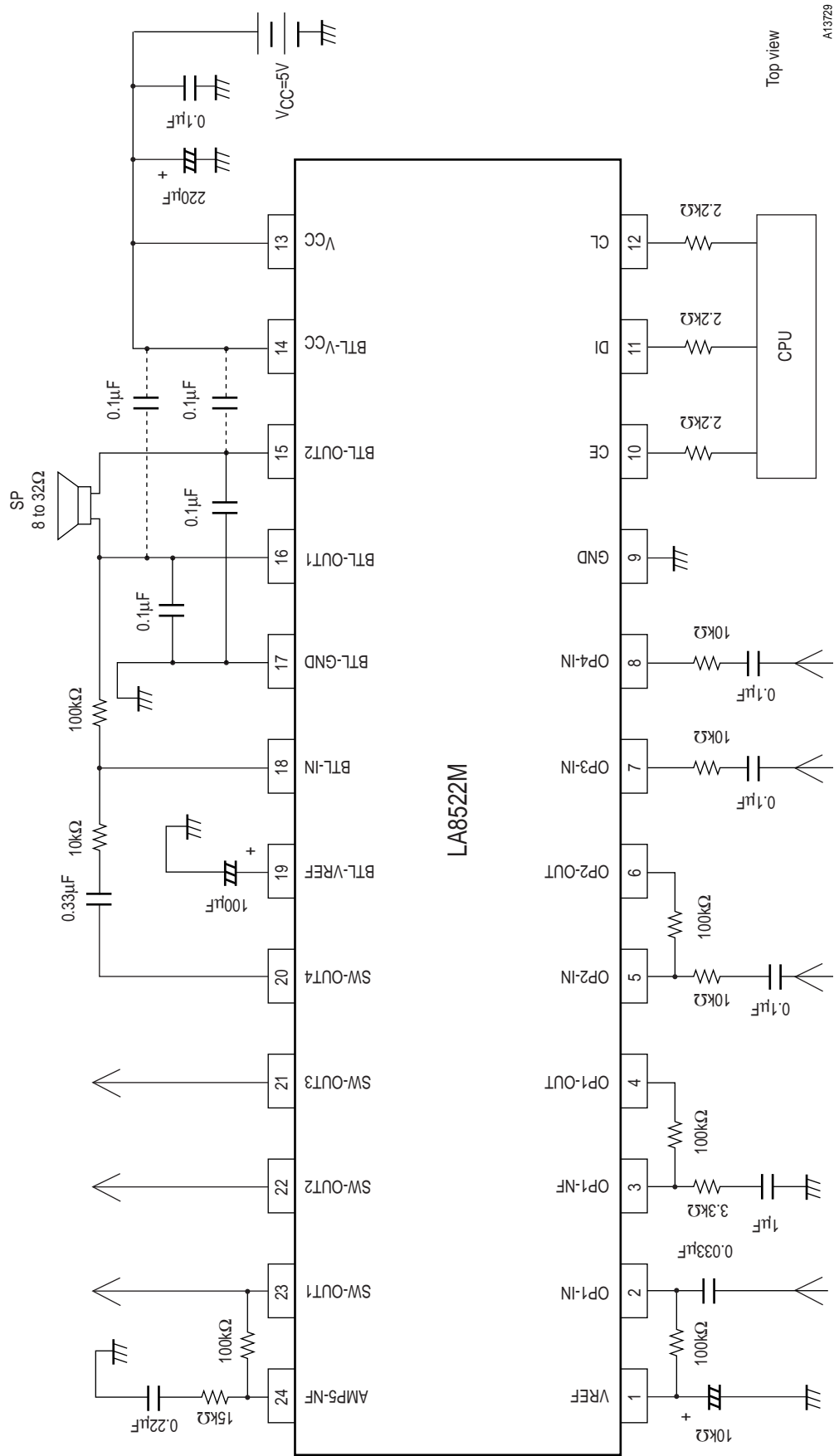
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Test Circuit Diagram



A13728

Application Circuit Diagram



Top view

A13729

Pin Functions

Pin No.	Pin	Pin voltage (V)	Notes	Equivalent circuit
1	VREF	2.25	Internal circuit reference voltage (about 2.25 V) • Circuits other than the BTL amplifier operate using this potential as a reference.	
2	OP1-IN	2.25	Amplifier 1 noninverting input	
3	OP1-NF	2.25	Amplifier 1 inverting input	
4	OP1-OUT	2.25	Amplifier 1 output	
5	OP2-IN	2.25	Amplifier 2 inverting input	
6	OP2-OUT	2.25	Amplifier 2 output	
7	OP3-IN	2.25	Amplifier 3 input	
8	OP4-IN	2.25	Amplifier 4 input	

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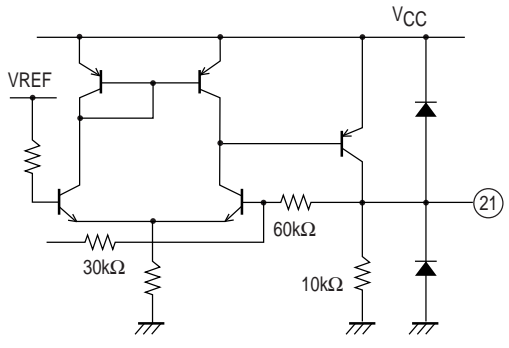
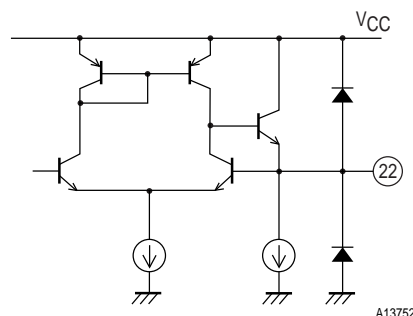
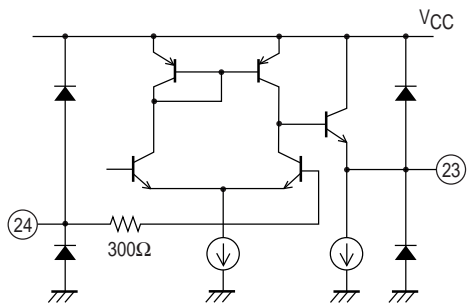
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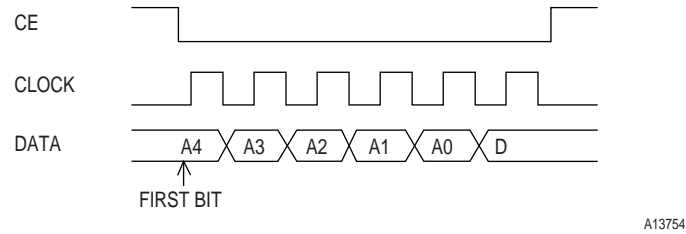
Pin No.	Pin	Pin voltage (V)	Notes	Equivalent circuit
10	CE	V_{CC}	Chip enable input	<p>A13747</p>
11	DI	V_{CC}	Data input	
12	CL	V_{CC}	Clock input	
16	BTL-OUT1	$0.44V_{CC}$	BTL power amplifier output 1	<p>To 19 pin</p> <p>A13748</p>
18	BTL-IN	$0.44V_{CC}$	BTL power amplifier inverting input	
15	BTL-OUT2	$0.44V_{CC}$	BTL power amplifier output 2	<p>To 16 pin</p> <p>A13749</p>
19	BTL-VREF	$0.44V_{CC}$	BTL power amplifier reference voltage	
20	SW-OUT4	2.25	Electronic volume control output (Fourth SW output)	<p>A13750</p>

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Pin No.	Pin	Pin voltage (V)	Notes	Equivalent circuit
21	SW-OUT3	2.25	Amplifier 7 output (Third SW output)	 <p>A13751</p>
22	SW-OUT2	2.25	Amplifier 6 output (Second SW output)	 <p>A13752</p>
23	SW-OUT1	2.25	Amplifier 5 output (First SW output)	 <p>A13753</p>
24	OP5-NF	2.25	Amplifier 5 noise filter connection	
9	GND	—	Ground	
13	V _{CC}	5 V applied	Power supply	
14	BTL-V _{CC}	5 V applied	Power amplifier power supply	
17	BTL-GND	—	Power amplifier ground	

Serial Data Format (6-bit structure)*1

A6:0 → Crosspoint switch (and other device) address setting (binary)
 D → Controls the crosspoint switch and power amplifier on/off state.
 Electronic volume control and attenuator selection

D = 1: Crosspoint switch: on

D = 0: Crosspoint switch: off

*1. When 8-bit serial data input mode is used.

Since the serial data has a 6-bit structure, the first and second bits are unused when 8-bit input mode is used.

Address table (Crosspoint switch)

[Data A4:0]

Input - Output	OUT1	OUT2	OUT3	OUT4
AMP1	10000	10100	11000	11100
AMP2	10001	10101	11001	11101
AMP3	10010	10110	11010	11110
AMP4	10011	10111	11011	11111

Other addresses [Data A4:0, D]

Address No.	A4:0	D	Mode	
	00000	*	Reset, control switch default	*2
	00011	0	BTL power amplifier: off	← Default setting
	00011	1	BTL power amplifier: on	
	01000	0	Electronic volume control	0 dB ← Default setting
	01001	0	Electronic volume control	-4 dB
	01010	0	Electronic volume control	-8 dB
	01011	0	Electronic volume control	-12 dB
	01100	0	Electronic volume control	-16 dB
	01101	0	Electronic volume control	-20 dB
	01110	0	Electronic volume control	-24 dB
	01111	0	Electronic volume control	-28 dB
	01000	1	Attenuator 1-0	0 dB ← Default setting
	01010	1	Attenuator 1-1	-4 dB
	01100	1	Attenuator 1-2	-8 dB
	01110	1	Attenuator 1-3	-12 dB
	00010	0	Attenuator 2-0	0 dB ← Default setting
	00010	1	Attenuator 2-1	-6 dB

*2. When the reset value is issued, the D data value can be either 0 or 1.

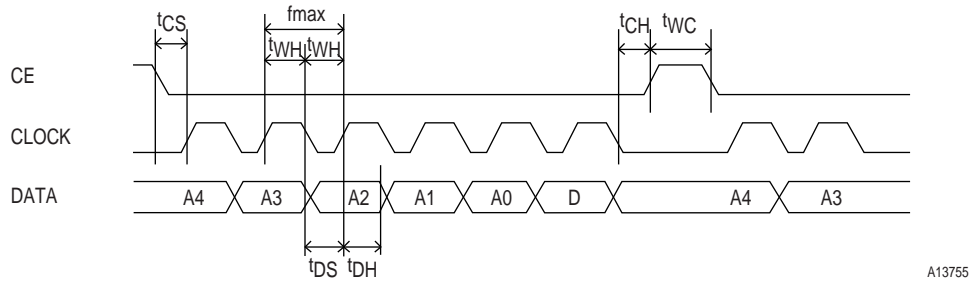
Notes 1. A reset command must be issued 200 ms after power is applied.

2. The electronic volume control is set to 0 dB by a reset (address: 00000*).

3. Attenuator 1 is set to 0 dB by a reset (address: 00000*).

4. Attenuator 2 is set to 0 dB by a reset (address: 00000*).

Serial Data Timing



- f_{max} (Maximum clock frequency) 500 kHz
- t_{WL} (Low-level clock pulse width) At least 1 μ s
- t_{WH} (High-level clock pulse width) At least 1 μ s
- t_{CS} (Chip enable setup time) At least 1 μ s
- t_{CH} (Chip enable hold time) At least 1 μ s
- t_{DS} (Data setup time) At least 1 μ s
- t_{DH} (Data hold time) At least 1 μ s
- t_{WC} (Chip enable pulse time) At least 1 μ s

Usage Notes

• Attenuator 1

Normally, attenuator 1 is set to 0 dB. It can be set to attenuate by -4, -8, or -12 dB by issuing serial data with a value of 010101, 011001, or 011101, respectively.

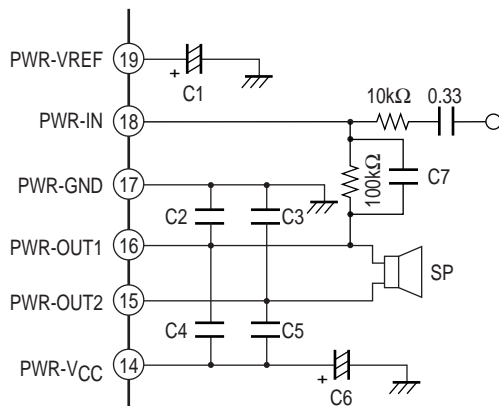


• Attenuator 2

Normally, attenuator 2 is set to 0 dB. It can be set to attenuate by -6 dB by issuing serial data with a value of 000101.



• Power amplifier phase compensation capacitors (Values shown are examples for reference purposes.)



- C1: 100 μ F
- C2: 0.1 μ F
- C3: 0.1 μ F
- C4: 0.1 μ F
- C5: 0.1 μ F
- C6: 100 μ F
- C7: 100 pF (The time constant will be under 10 μ s.)
- SP8: 8 to 32 Ω
- Voltage gain: 20 to 30 dB

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Of the external components, the capacitors C2 and C3 are the power amplifier phase compensation capacitors. If these capacitors are located away from the IC pin due to layout considerations, the impedance relationship will result in a reduction in the phase compensation effect, and high band oscillator may occur.

Therefore, we recommend that the two capacitors C2 and C3 discussed above be located as close as possible to the IC pins in the layout. However, if you find that, due to layout relationships, the circuit tends to oscillate, we recommend that, rather than compensation using only capacitors, you use a phase compensation design with resistors (about 1 to 2.2 Ω) inserted in series with the capacitors.

If the capacitor C7 is added to the feedback resistor path, the phase of the feedback path will be delayed and capacitors C4 and C5 will be required. Here, the time constant of the feedback resistor and C7 must be 10 μ s or less (100 k Ω , 100 pF).

- LA8522M ground line layout (See the figure on the following page.)

The LA8522M circuit blocks can be roughly classified as follows.

(1) Power amplifier system, (2) Crosspoint switch small-signal system

Since this block structure involves two significantly different circuit types, each block has independent VCC and ground pins. It is best if external devices are connected to the ground line for the corresponding block, and that finally the two block ground lines are connected to the power supply (regulator) ground, which is the final reference. In particular, the PCB pattern should be formed with two ground lines.

There are cases, however, where a single line is used for the power supply ground due to limitations on protruding PCB areas. In such cases, the ground line layout must be designed so that the sections of the ground line that carry large currents (the power amplifier block) are closer to the power supply ground (and thus have a lower impedance) than the sections of the ground line for circuits that draw smaller currents.

If the large currents drawn by the power amplifier pass through ground line that handles the lower currents from the small-signal processing blocks, the signal path may be influenced by the ground, loops may be created, and low-band oscillation may occur.

Therefore we recommend that the ground lines be designed as described above so that lines that carry larger amounts of current are connected the closest to the power supply ground that serves as the reference.

- Inter-pin shorting

This IC may be damaged or destroyed if power is applied with any pins shorted together. Therefore, when mounting this IC to a printed circuit board always check for pin shorting caused by stray solder or any other foreign material before applying power.

- Load shorting

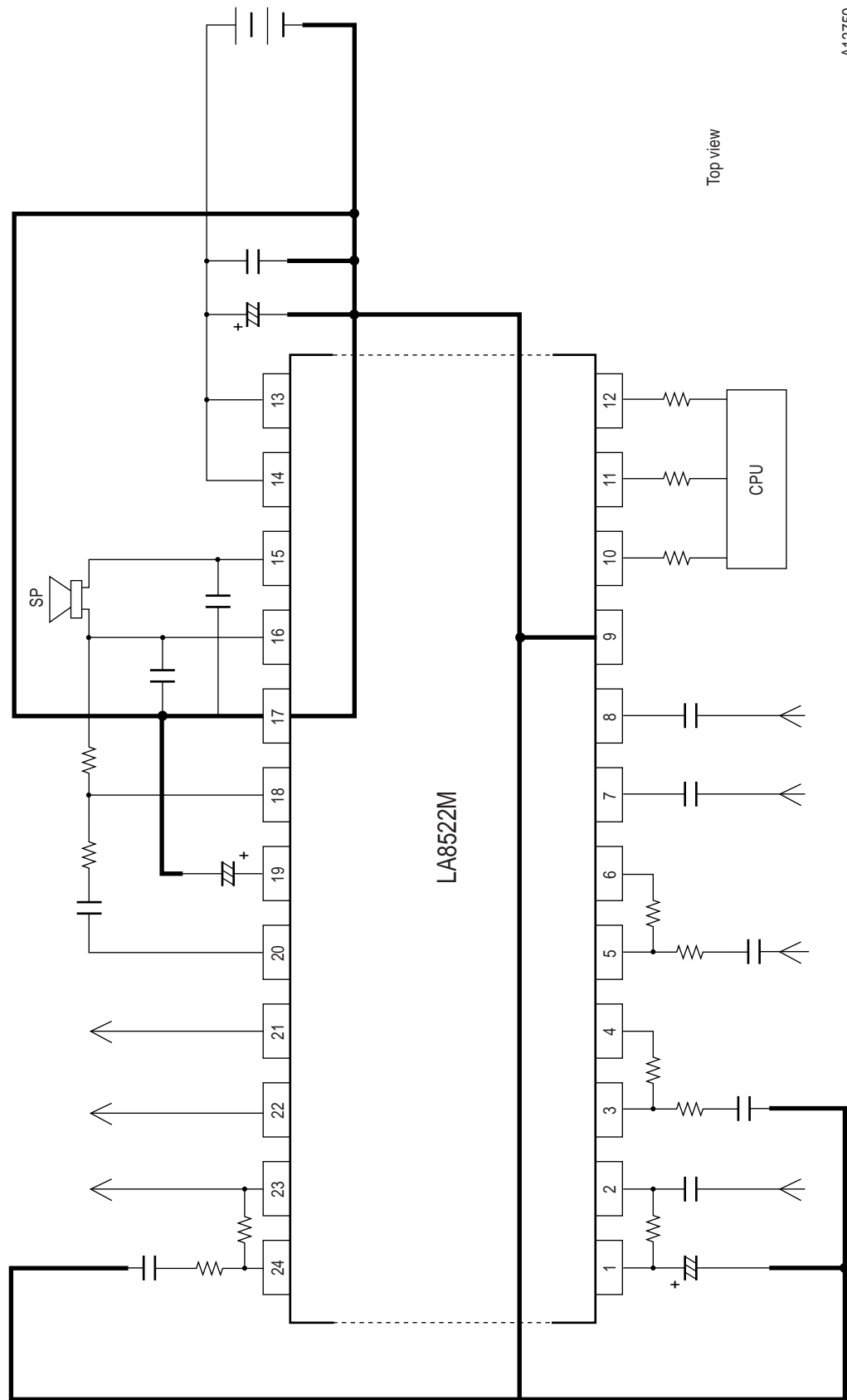
This IC may be damaged or destroyed if it is operated for extended periods with the load shorted. Do not allow the load to be shorted.

- Maximum ratings

The slightest fluctuations in operating conditions may cause the ratings to be exceeded if this IC is operated in the vicinity of the maximum ratings. Since this can lead to destruction of the device, applications must be designed with adequate margins with respect to the power-supply voltage and other parameters so that the maximum ratings are never exceeded.

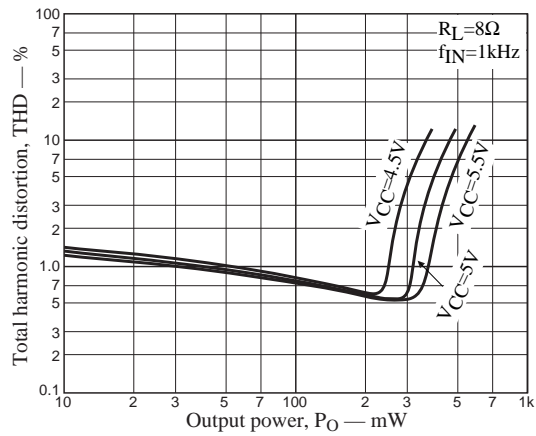
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Ground Line Layout

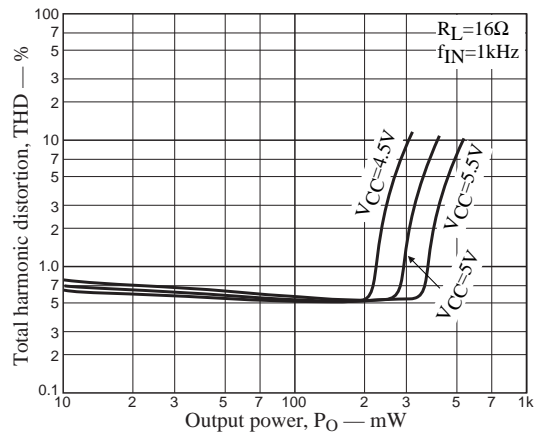


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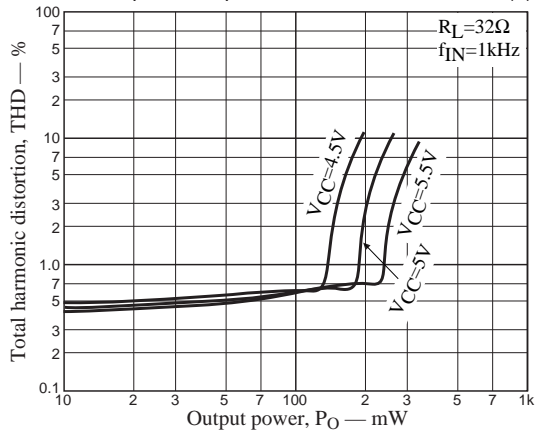
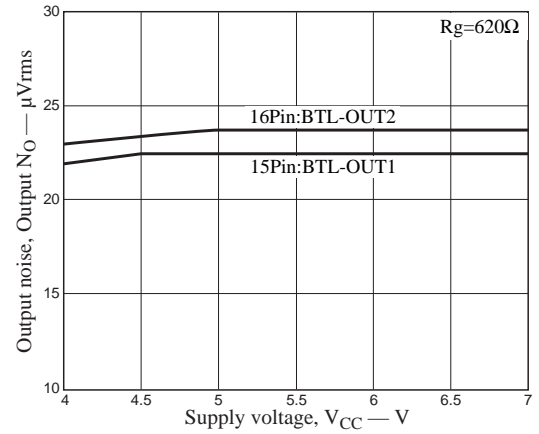
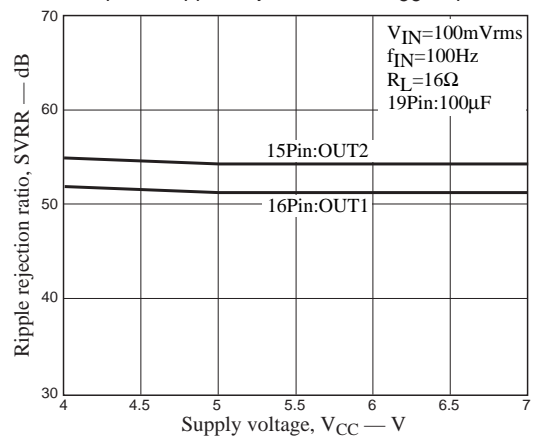
BTL Amplifier Output Distortion Characteristics (1)



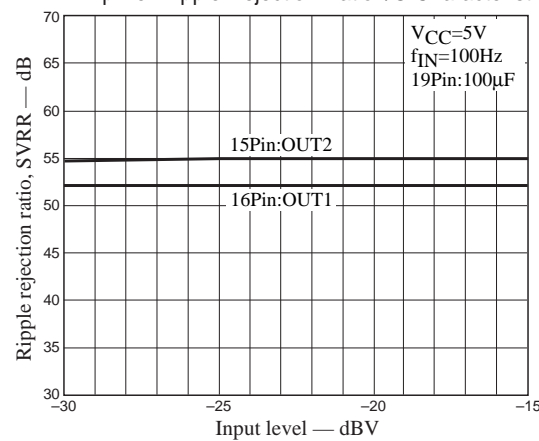
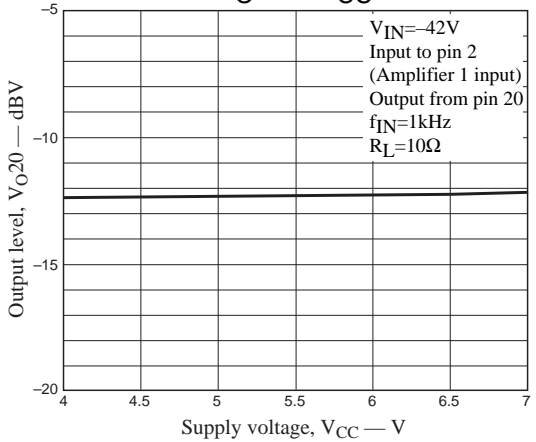
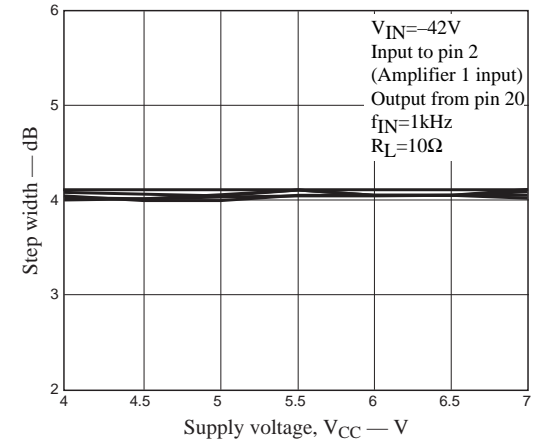
BTL Amplifier Output Distortion Characteristics (2)

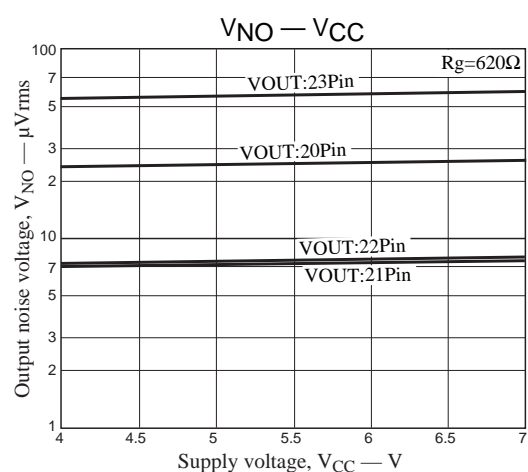
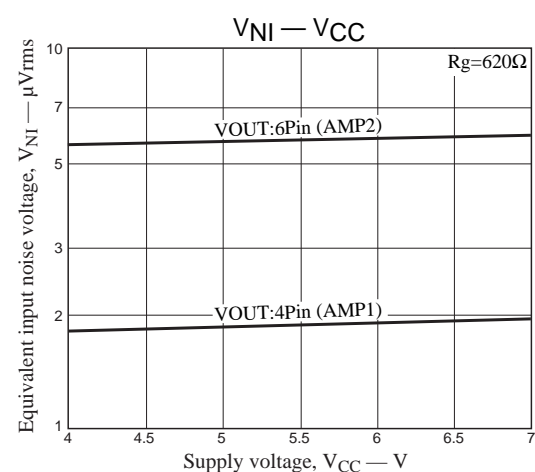
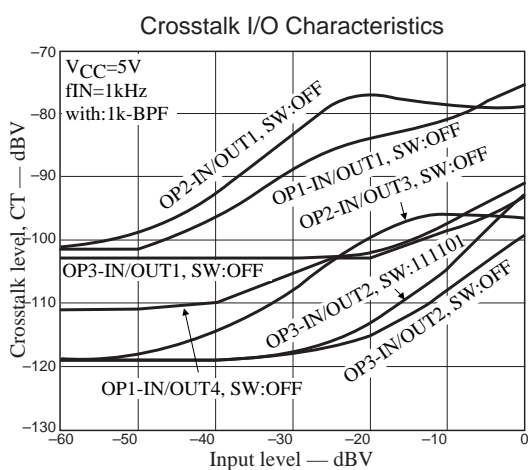
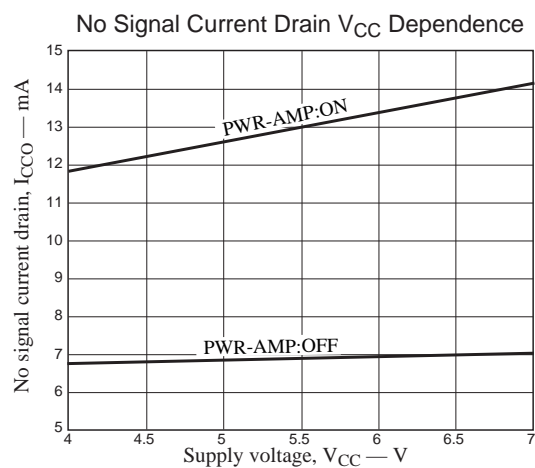
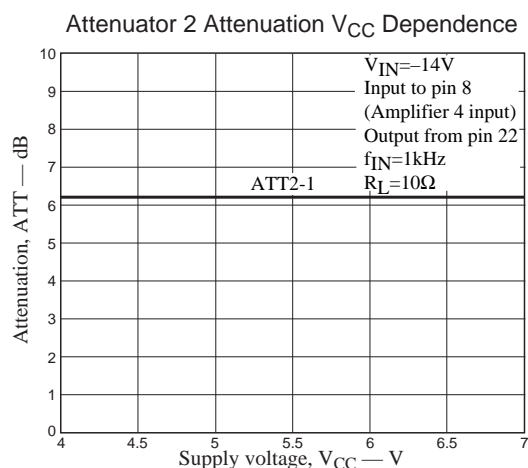
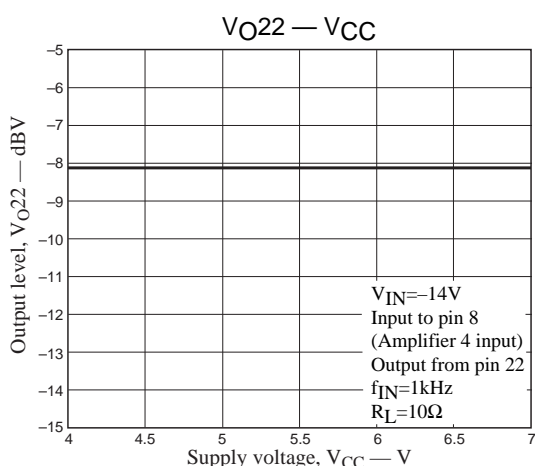
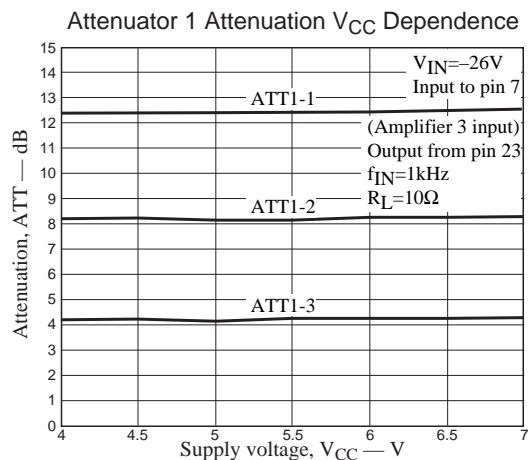
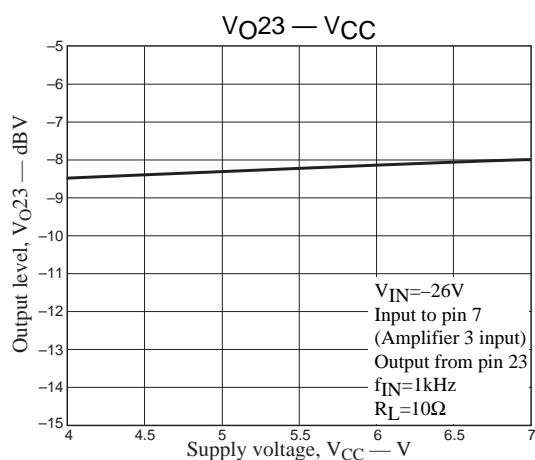


BTL Amplifier Output Distortion Characteristics (3)

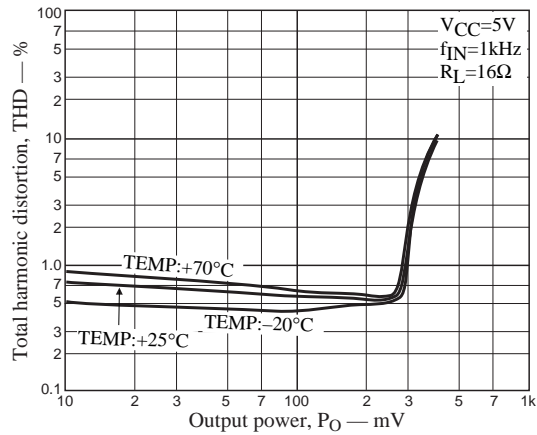
BTL Amplifier Output Noise V_{CC} DependenceBTL Amplifier Ripple Rejection Ratio V_{CC} Dependence

BTL Amplifier Ripple Rejection Ratio I/O Characteristics

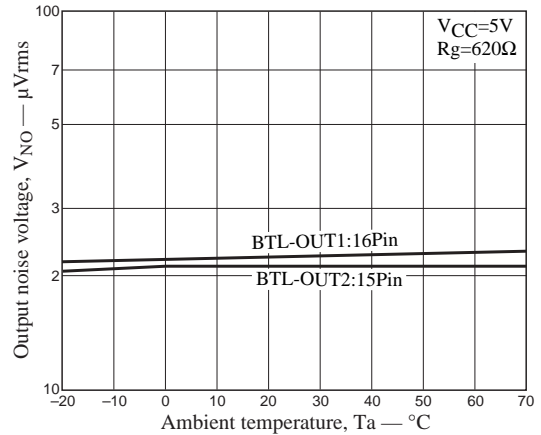
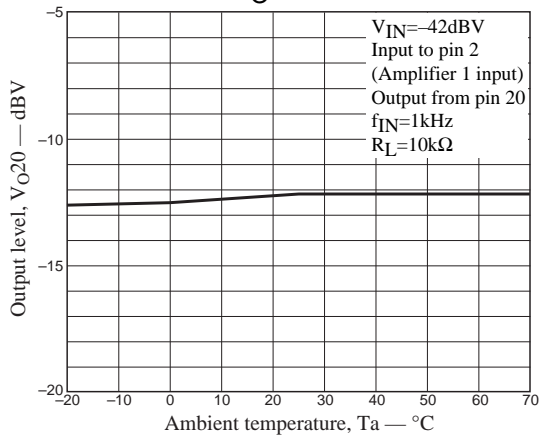
 $V_{O20} - V_{CC}$ Electronic Volume Control Step Width V_{CC} Dependence



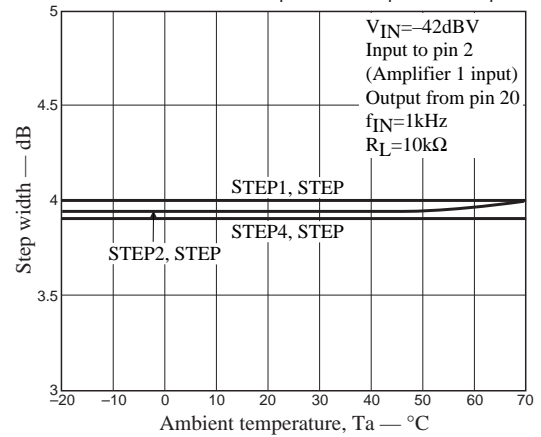
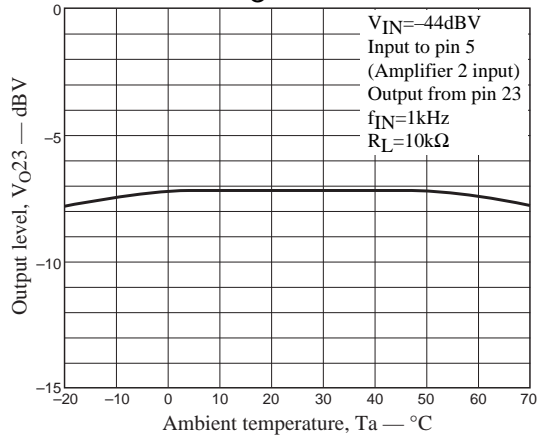
BTL Amplifier Output Distortion Characteristics (4)



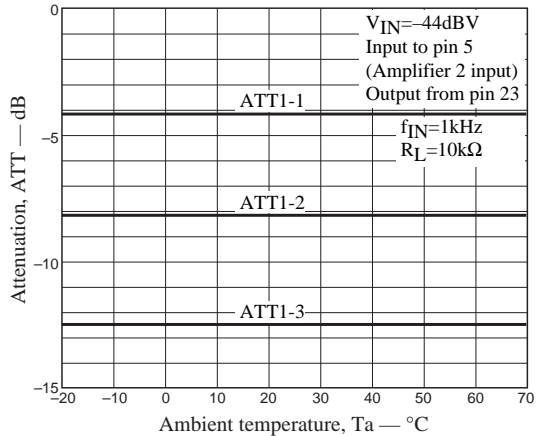
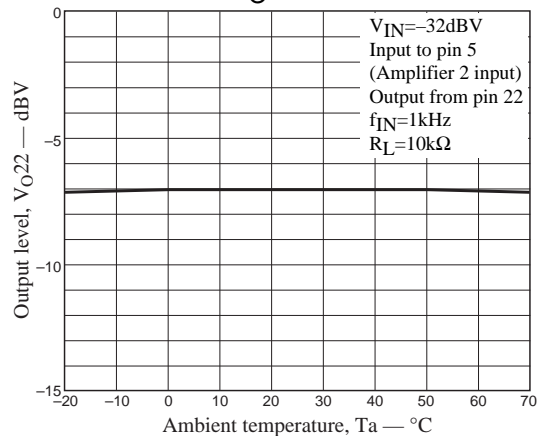
Output Amplifier Output Noise Temperature Dependence

 $V_{O20} - T_a$ 

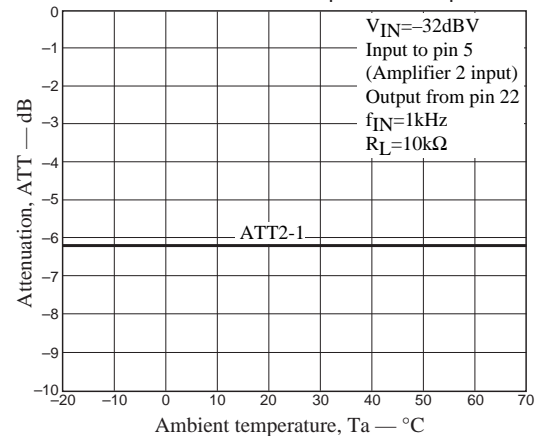
Electronic Volume Control Step Width Temperature Dependence

 $V_{O23} - T_a$ 

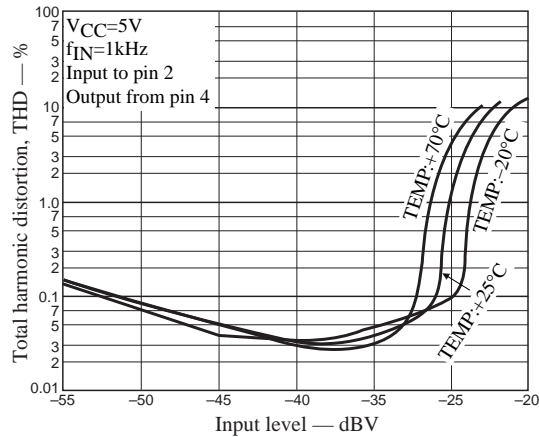
Attenuator Attenuation Temperature Dependence

 $V_{O22} - T_a$ 

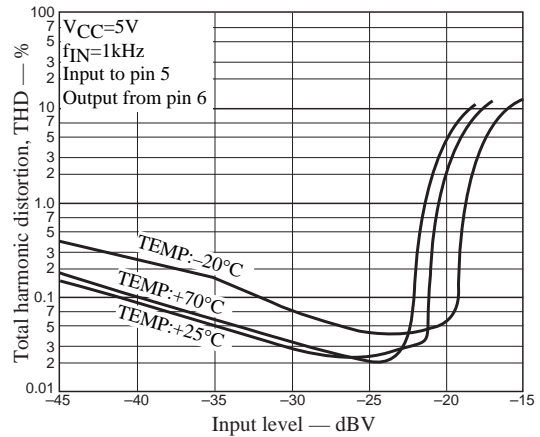
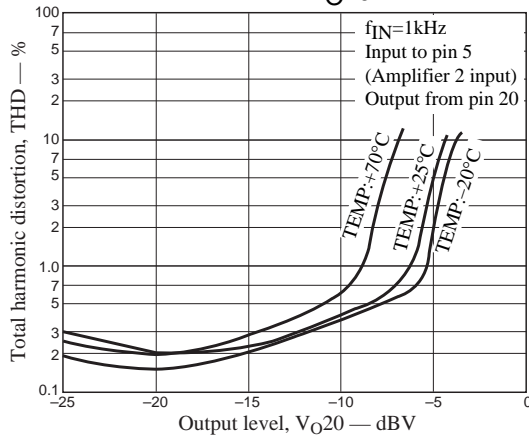
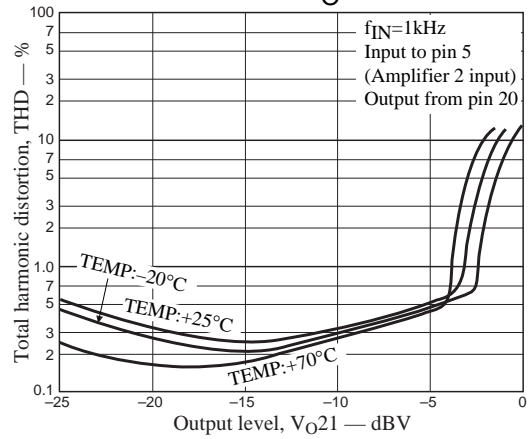
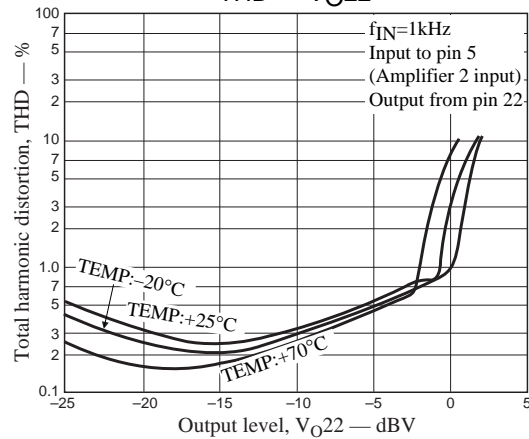
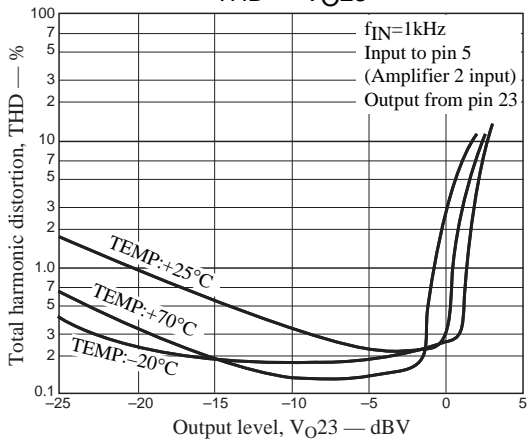
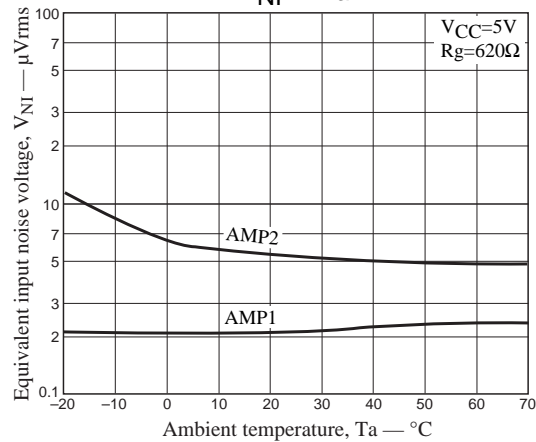
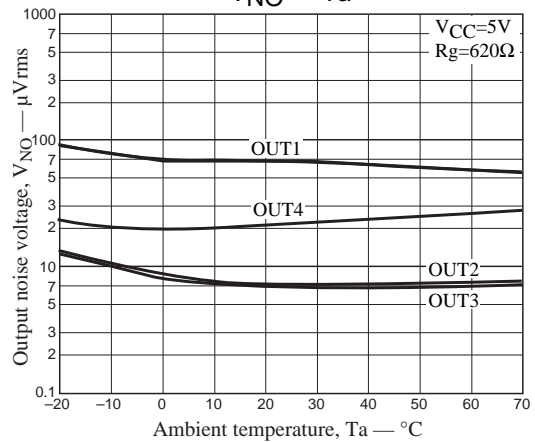
Attenuator Attenuation Temperature Dependence



Amplifier 1 I/O Characteristics



Amplifier 2 I/O Characteristics

THD — V_{O20} THD — V_{O21} THD — V_{O22} THD — V_{O23}  V_{NI} — T_a  V_{NO} — T_a 

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