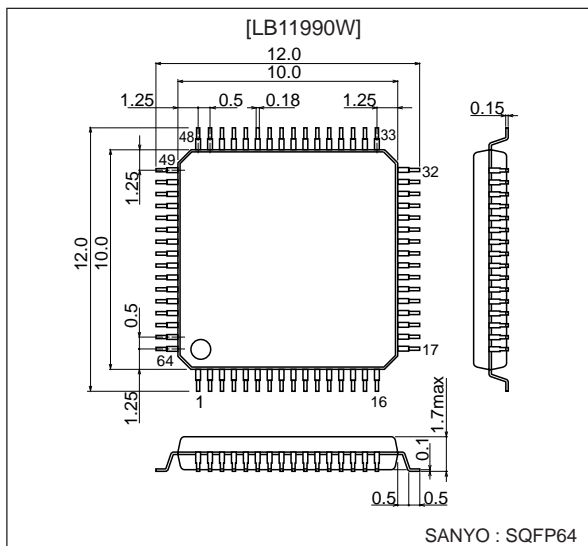


**SANYO****LB11990W****Three-Phase Brushless Motor Driver****Package Dimensions**

unit: mm

**3190-SQFP64****Specifications****Absolute Maximum Ratings at Ta = 25°C**

| Parameter                    | Symbol               | Conditions           | Ratings                        | Unit |
|------------------------------|----------------------|----------------------|--------------------------------|------|
| Maximum supply voltage 1     | V <sub>CC1</sub> max |                      | 7                              | V    |
| Maximum supply voltage 2     | V <sub>CC2</sub> max |                      | 8.5                            | V    |
| Maximum supply voltage 3     | V <sub>S_C</sub> max | Capstan motor driver | 7.0                            | V    |
| Maximum supply voltage 4     | V <sub>S_D</sub> max | Drum motor driver    | 7.0                            | V    |
| Maximum supply voltage 5     | V <sub>S_L</sub> max | Loading motor driver | 7.0                            | V    |
| Applied output voltage       | V <sub>o</sub> max   |                      | 8.0                            | V    |
| Applied input voltage        | V <sub>I1</sub> max  | Control circuits     | -0.3 to V <sub>CC1</sub> + 0.3 | V    |
|                              | V <sub>I2</sub> max  | U, V, W, COM         | 8.0                            | V    |
| Capstan motor output current | I <sub>OC</sub> max  |                      | 1.0                            | A    |
| Drum motor output current    | I <sub>OD</sub> max  |                      | 1.0                            | A    |
| Loading motor output current | I <sub>OL</sub> max  |                      | 0.6                            | A    |
| Allowable power dissipation  | P <sub>d</sub> max   | IC only              | 0.6                            | W    |
| Operating temperature        | T <sub>opr</sub>     |                      | -20 to +75                     | °C   |
| Storage temperature          | T <sub>stg</sub>     |                      | -55 to +150                    | °C   |

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

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**Allowable Operating Ranges at Ta = 25°C**

| Parameter              | Symbol            | Conditions                          | Ratings    | Unit  |
|------------------------|-------------------|-------------------------------------|------------|-------|
| Power supply voltage 1 | V <sub>CC1</sub>  | V <sub>CC1</sub> ≤ V <sub>CC2</sub> | 2.7 to 6.0 | V     |
| Power supply voltage 2 | V <sub>CC2</sub>  |                                     | 3.5 to 8.5 | V     |
| Power supply voltage 3 | V <sub>S_C</sub>  | V <sub>S_C</sub> ≤ V <sub>CC2</sub> | to 7.0     | V     |
| Power supply voltage 4 | V <sub>S_D</sub>  | V <sub>S_D</sub> ≤ V <sub>CC2</sub> | to 7.0     | V     |
| Power supply voltage 5 | V <sub>S_L</sub>  | V <sub>S_L</sub> ≤ V <sub>CC2</sub> | 2.2 to 7.0 | V     |
| Hall input amplitude   | V <sub>HALL</sub> | Capstan motor                       | ±20 to ±80 | mVp-p |

**Electrical Characteristics/Capstan Motor Driver Block at Ta = 25°C, V<sub>CC1</sub> = 3V, V<sub>CC2</sub> = 4.75V, V<sub>S</sub> = 1.5V**

|                      | Parameter                   | Symbol                          | Conditions   | Ratings |      |                  | Unit |
|----------------------|-----------------------------|---------------------------------|--|---------|------|------------------|------|
|                      |                             |                                 |  | min     | typ  | max              |      |
| Power supply current | Vcc1 power supply current   | I <sub>cc1</sub>                | I <sub>out</sub> = 100 mA V <sub>STBY_C</sub> = 3V                       |         | 4    | 8                | mA   |
|                      | Vcc2 power supply current   | I <sub>cc2</sub>                | I <sub>out</sub> = 100 mA V <sub>STBY_C</sub> = 3V                       |         | 6    | 12               | mA   |
|                      | Vcc1 idle current           | I <sub>cc1Q</sub>               | V <sub>STBY_C</sub> = 0V   |         | 2.1  | 4                | mA   |
|                      | Vcc2 idle current           | I <sub>cc2Q</sub>               | V <sub>STBY_C</sub> = 0V   |         |      | 100              | μA   |
|                      | Vs idle current             | I <sub>sQ</sub>                 | V <sub>STBY_C</sub> = 0V   |         | 75   | 100              | μA   |
| VX1                  | Upper side residual voltage | VXH1                            | I <sub>out</sub> = 0.2A  | 0.15    | 0.22 | 0.29             | V    |
|                      | Lower side residual voltage | VXL1                            | I <sub>out</sub> = 0.2A  | 0.15    | 0.20 | 0.25             | V    |
| VX2                  | Upper side residual voltage | VXH2                            | I <sub>out</sub> = 0.5A  |         | 0.25 | 0.40             | V    |
|                      | Lower side residual voltage | VXL2                            | I <sub>out</sub> = 0.5A  |         | 0.25 | 0.40             | V    |
|                      | Output saturation voltage   | V <sub>osat</sub>               | I <sub>out</sub> = 0.8A, Sink + Source                                   |         |      | 1.40             | V    |
|                      | Overlap amount              | O.L                             | RL = 39Ω × 3, Rangle = 20 kΩ Note 2                                      | 73      | 80   | 87               | %    |
| Hall amplifier       | Input offset voltage        | V <sub>H</sub> OFF              | Note 1 Design target value   | -5      |      | +5               | mV   |
|                      | Common mode input range     | V <sub>H</sub> CM               | Rangle = 20 kΩ   | 0.95    |      | 2.1              | V    |
|                      | Input/output voltage gain   | V <sub>G</sub> VH               | Rangle = 20 kΩ   | 24.5    | 27.5 | 30.5             | dB   |
| Standby pin          | High level voltage          | V <sub>STH</sub>                |  | 2.5     |      | V <sub>CC1</sub> | V    |
|                      | Low level voltage           | V <sub>STL</sub>                |  | -0.2    |      | +0.7             | V    |
|                      | Input current               | I <sub>STIN</sub>               | V <sub>STBY_C</sub> = 3V   |         |      | 50               | μA   |
|                      | Leakage current             | I <sub>STLK</sub>               | V <sub>STBY_C</sub> = 0V   |         |      | -30              | μA   |
| FRC pin              | High level voltage          | V <sub>F</sub> RCH              |  | 2.5     |      | V <sub>CC1</sub> | V    |
|                      | Low level voltage           | V <sub>F</sub> RCL              |  | -0.2    |      | +0.4             | V    |
|                      | Input current               | I <sub>F</sub> RCIN             | V <sub>F</sub> R <sub>C</sub> = 3V                                       |         | 20   | 30               | μA   |
|                      | Leakage current             | I <sub>F</sub> RCLK             | V <sub>F</sub> R <sub>C</sub> = 0V                                       |         |      | -30              | μA   |
| VH                   | Hall power supply voltage   | V <sub>HALL</sub>               | I <sub>H</sub> = 5 mA, V <sub>H</sub> (+) - V <sub>H</sub> (-)           | 0.75    | 0.85 | 0.95             | V    |
|                      | (-) pin voltage             | V <sub>H</sub> (-)              | I <sub>H</sub> = 5 mA  | 0.81    | 0.88 | 0.95             | V    |
| FG comparator        | Input offset voltage        | V <sub>F</sub> G <sub>OFF</sub> |  | -3      |      | +3               | mV   |
|                      | Input bias current          | I <sub>b</sub> FG               | V <sub>F</sub> G <sub>IN+</sub> = V <sub>F</sub> G <sub>IN-</sub> = 1.5V |         |      | 500              | nA   |
|                      | Input bias current offset   | ΔI <sub>b</sub> FG              | V <sub>F</sub> G <sub>IN+</sub> = V <sub>F</sub> G <sub>IN-</sub> = 1.5V | -100    |      | +100             | nA   |
|                      | Common mode input range     | V <sub>F</sub> G <sub>CM</sub>  |  | 1.2     |      | 2.5              | V    |
|                      | High level output voltage   | V <sub>F</sub> G <sub>OH</sub>  | With internal pull-up  | 2.8     |      |                  | V    |
|                      | Low level output voltage    | V <sub>F</sub> G <sub>OL</sub>  | With internal pull-up  |         |      | 0.2              | V    |
|                      | Voltage gain                | V <sub>G</sub> FG               | Note 1 Design target value   |         | 100  |                  | dB   |
|                      | Output current (Sink)       | I <sub>F</sub> G <sub>Os</sub>  | At output pin "L"  |         |      | 5                | mA   |

Note 1: Design target value, not measured

Note 2: The overlap amount specification is taken as the measurement specification.

**Cylinder Motor Driver Block at Ta = 25°C, V<sub>CC1</sub> = 3V, V<sub>CC2</sub> = 4.75V, V<sub>S</sub> = 3V**

| Parameter                               | Symbol  | Conditions                            | Ratings |      |                       | Unit |
|---|---------|---------------------------------------|---------|------|-----------------------|------|
|   |         |                                       | min     | typ  | max                   |      |
| Power supply current 4                  | ICC2    | IO = 76 mA VSTBY_D = 3V VSTBY_C = 0V  |         | 0.75 | 2.5                   | mA   |
| Output idle current 4                   | ICC2Q   | VSTBY_D = VSTBY_C = 0V                |         |      | 100                   | μA   |
| Output idle current 5                   | IS(D)Q  | VSTBY_D = VSTBY_C = 0V                |         | 100  | 300                   | μA   |
| Output saturation voltage, upper side 1 | VOU1    | IO = 0.1A RF = 0.25Ω                  |         | 0.3  | 0.5                   | V    |
| Output saturation voltage, lower side 1 | VOD1    | IO = 0.1A RF = 0.25Ω                  |         | 0.3  | 0.5                   | V    |
| Output saturation voltage, upper side 2 | VOU2    | IO = 0.4A, VS = 3V RF = 0.25Ω         |         | 0.5  | 0.8                   | V    |
| Output saturation voltage, lower side 2 | VOD2    | IO = 0.4A, VS = 3V RF = 0.25Ω         |         | 0.5  | 0.8                   | V    |
| COM pin common mode input voltage range | VIC     |                                       | 0.3     |      | V <sub>CC2</sub> -0.9 | V    |
| Standby pin High level voltage          | VSTBYH  |                                       | 2       |      | V <sub>CC1</sub>      | V    |
| Standby pin Low level voltage           | VSTBYL  |                                       | -0.2    |      | +0.7                  | V    |
| Standby pin input current               | ISTBYH  | VSTBY_D = 3V                          |         |      | 50                    | μA   |
| Standby pin leakage current             | ISTBYL  | VSTBY_D = 0V                          | -10     |      |                       | μA   |
| FRC pin High level voltage              | VFRCH   |                                       | 2       |      | V <sub>CC1</sub>      | V    |
| FRC pin Low level voltage               | VFRCL   |                                       | -0.2    |      | +0.7                  | V    |
| FRC pin input current                   | IFRCI   | VFRC_D = 3V                           |         |      | 50                    | μA   |
| FRC pin leakage current                 | IFRCL   | VFRC_D = 0V                           | -10     |      |                       | μA   |
| Slope pin source current ratio          | RSOURCE | ICSLP1SOURCE/ICSLP2SOURCE             | -15     |      | +15                   | %    |
| Slope pin sink current ratio            | RSINK   | ICSLP1SINK/ICSLP2SINK                 | -15     |      | +15                   | %    |
| CSLP1 source/sink current ratio         | RCSLP1  | ICSLP1SOURCE/ICSLP1SINK               | -35     |      | +15                   | %    |
| CSLP2 source/sink current ratio         | RCSLP2  | ICSLP2SOURCE/ICSLP2SINK               | -35     |      | +15                   | %    |
| Startup frequency                       | Freq    | Cosc = 0.1 μF, OSC frequency (Target) |         | 11.5 |                       | Hz   |
| Phase delay-width                       | Dwidth  | (Target)                              |         | 30   |                       | deg  |
| SELCSLP pin High level voltage          | VSELH   |                                       | 2       |      | V <sub>CC1</sub>      | V    |
| SELCSLP pin Low level voltage           | VSELL   |                                       | -0.2    |      | +0.7                  | V    |
| SELCSLP pin input current               | ISELH   | VSELCSLP = 3V                         |         |      | 50                    | μA   |
| SELCSLP pin leakage current             | ISELL   | VSELCSLP = 0V                         | -10     |      |                       | μA   |

Note) Items shown to be "Target" are not measured.

**FG/PG Amplifier Block at Ta = 25°C, V<sub>CC1</sub> = 3V, V<sub>CC2</sub> = 4.75V, V<sub>S</sub> = 3V**

| Parameter                          | Symbol | Conditions         | Ratings               |      |      | Unit |
|------------------------------------|--------|--------------------|-----------------------|------|------|------|
|                                    |        |                    | min                   | typ  | max  |      |
| [FG amplifier]                     |        |                    |                       |      |      |      |
| Input offset voltage               | VIO    | (Target)           |                       | ±1   | ±5   | mA   |
| Input bias current                 | IBIN–  | (Target)           |                       |      | 250  | nA   |
| Common mode input voltage range    | VICOM  | (Target)           | 1                     |      | 2    | V    |
| Open loop gain                     | GVFG   | f = 1 kHz (Target) |                       | 55   |      | dB   |
| Output ON voltage                  | VOL    | At IO = 10 μA      |                       |      | 0.4  | V    |
| Output OFF voltage                 | VOH    | At IO = 10 μA      | V <sub>CC</sub> 1–0.5 |      |      | V    |
| Schmitt amplifier hysteresis width | VSHIS  | (Target)           |                       | 50   |      | mV   |
| Reference voltage                  | VREF   |                    | 1.15                  | 1.30 | 1.45 | V    |
| [PG amplifier]                     |        |                    |                       |      |      |      |
| Input offset voltage               | VIO    | (Target)           |                       | ±1   | ±5   | mV   |
| Input bias current                 | IBIN–  | (Target)           |                       |      | 250  | nA   |
| Common mode input voltage range    | VICOM  | (Target)           | 1                     |      | 2    | V    |
| Open loop gain                     | GVPG   | f = 1 kHz (Target) |                       | 55   |      | dB   |
| Output ON voltage                  | VOL    | At IO = 10 μA      |                       |      | 0.4  | V    |
| Output OFF voltage                 | VOH    | At IO = 10 μA      | V <sub>CC</sub> 1–0.5 |      |      | V    |
| Schmitt amplifier hysteresis width | VSHIS  | (Target)           |                       | 50   |      | mV   |

Note) Items shown to be "Target" are not measured.

**Loading Motor Driver Block at Ta = 25°C, V<sub>CC1</sub> = 3V, V<sub>CC2</sub> = 4.75V, V<sub>S</sub> = 3V**

| Parameter                          | Symbol | Conditions  | Ratings |      |                  | Unit |
|------------------------------------|--------|---|---------|------|------------------|------|
|                                    |        |   | min     | typ  | max              |      |
| VCC1 power supply current 1        | ICC11  | VSTBY_C = VSTBY_D = 0V (standby)                    |         | 2.1  | 4                | mA   |
| VCC1 power supply current 2        | ICC12  | VSTBY_C = VSTBY_D = 0V (forward/reverse)            |         | 14   | 19               | mA   |
| VCC1 power supply current 3        | ICC13  | VSTBY_C = VSTBY_D = 0V (at braking)                 |         | 10   | 14               | mA   |
| VCC2 power supply current 1        | ICC21  | VSTBY_C, D = 0V (standby (V <sub>CC1</sub> = OPEN)) |         |      | 100              | μA   |
| VCC2 power supply current 2        | ICC22  | VSTBY_C, D = 0V (standby (V <sub>CC1</sub> = 3.0V)) |         |      | 100              | μA   |
| VCC2 power supply current 3        | ICC23  | VSTBY_C, D = 0V (forward/reverse)                   |         | 15.0 | 25               | mA   |
| VS L power supply current          | I VS L | VSTBY_C, D = 0V (standby)                           |         |      | 20               | μA   |
| [Logic input (DEC1 pin, DEC2 pin)] |        |   |         |      |                  |      |
| High level input voltage           | VINH   | V <sub>CC1</sub> = 2.7 to 4.0V                      | 2.0     |      | V <sub>CC1</sub> | V    |
| High level flowing current         | IINH   | VIN = 3.0V  |         | 41   | 65               | μA   |
| Low level input voltage            | VINL   | V <sub>CC1</sub> = 2.7 to 4.0V                      | -0.2    |      | 0.6              | V    |
| Low level flowing current          | IINL   | VIN = 0.6V  |         | 5    | 10               | μA   |
| [Loading motor driver]             |        |   |         |      |                  |      |
| Output saturation voltage 1        | VOH    | IO = 200 mA (upper/lower composition)               |         | 0.2  | 0.3              | V    |
| Output saturation voltage 2        | VSHIS  | IO = 400 mA (upper/lower composition)               |         | 0.4  | 0.6              | V    |
| [Reel FG amplifier]                |        |   |         |      |                  |      |
| Input offset voltage               | VIO    |   |         | ±1   | ±5               | mV   |
| Input bias current                 | IB     |   |         |      | 1                | μA   |
| Common mode input voltage range    | VICM   |   | 1       |      | 2                | V    |
| Open loop gain                     | GV1    |   |         | 55   |                  | dB   |
| [Thermal shutdown circuit]         |        |   |         |      |                  |      |
| TSD operating temperature          | T-TSD  | (Target)  |         | 180  |                  | °C   |
| TSD temperature hysteresis width   | ΔTSD   | (Target)  |         | 15   |                  | °C   |

Note) Items shown to be "Target" are not measured.

**Truth Table**

**Capstan Motor Truth Table**

|   | Source → Sink | Hall input |   |   | FRC |
|---|---------------|------------|---|---|-----|
|   |               | U          | V | W |     |
| 1 | V → W         | H          | H | L | H   |
|   | W → V         |            |   |   | L   |
| 2 | U → W         | H          | L | L | H   |
|   | W → U         |            |   |   | L   |
| 3 | U → V         | H          | L | H | H   |
|   | V → U         |            |   |   | L   |
| 4 | W → V         | L          | L | H | H   |
|   | V → W         |            |   |   | L   |
| 5 | W → U         | L          | H | H | H   |
|   | U → W         |            |   |   | L   |
| 6 | V → U         | L          | H | L | H   |
|   | U → V         |            |   |   | L   |

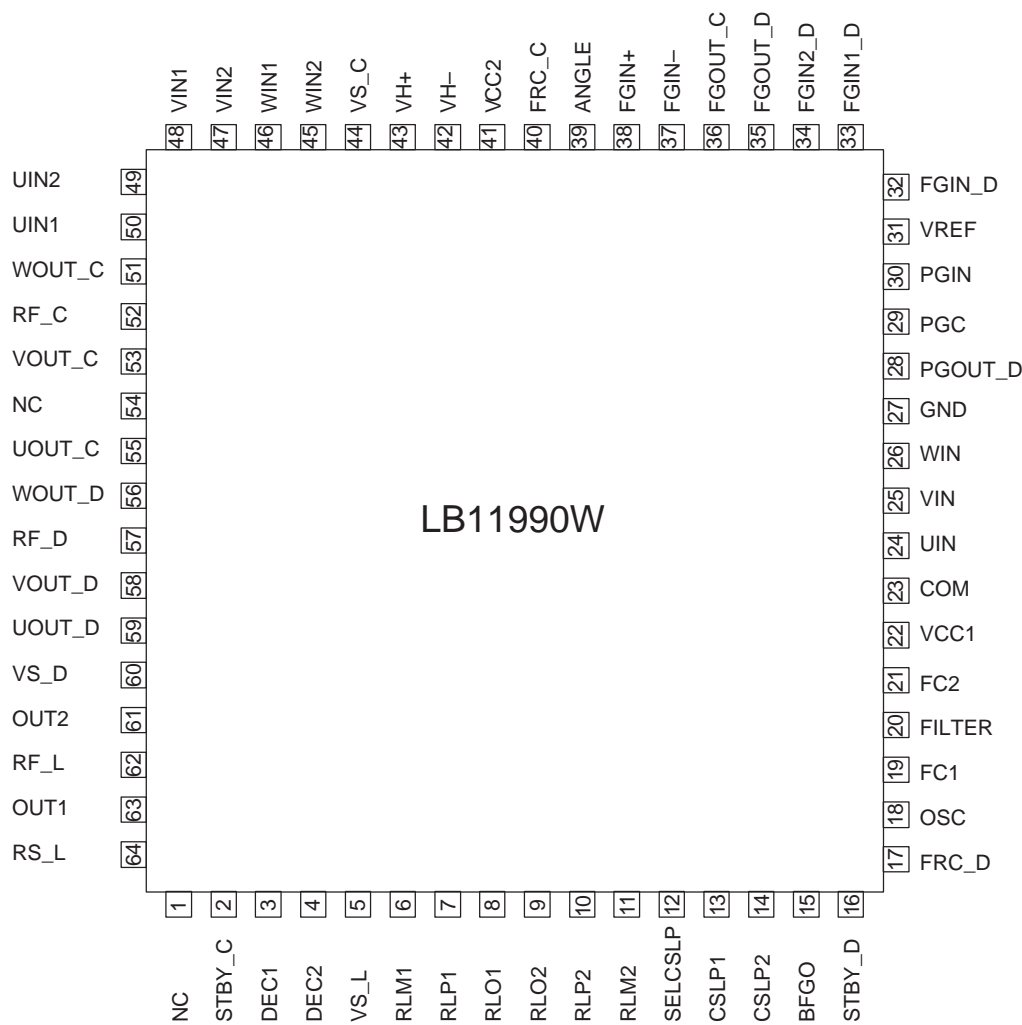
Note: "H" for FR means a voltage of 2.50V or above. "L" for FR means a voltage of 0.4V or below.  
(V<sub>cc1</sub> = 3V)

Note: At the Hall input, "H" means that the potential of the (+) terminal for each phase input is at least 0.02V higher than the (–) terminal.  
"L" means that the potential of the (+) terminal for each phase input is at least 0.02V lower than the (–) terminal.

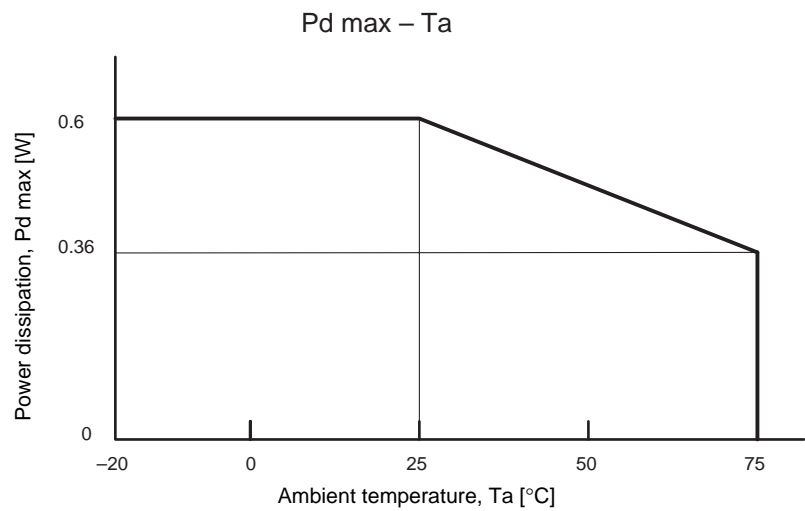
**Loading Motor Truth Table**

| Input |      | Output |      | Mode    |
|-------|------|--------|------|---------|
| DEC1  | DEC2 | OUT1   | OUT2 |         |
| L     | L    | Off    | Off  | Standby |
| H     | L    | H      | L    | Forward |
| L     | H    | L      | H    | Reverse |
| H     | H    | L      | L    | Brake   |

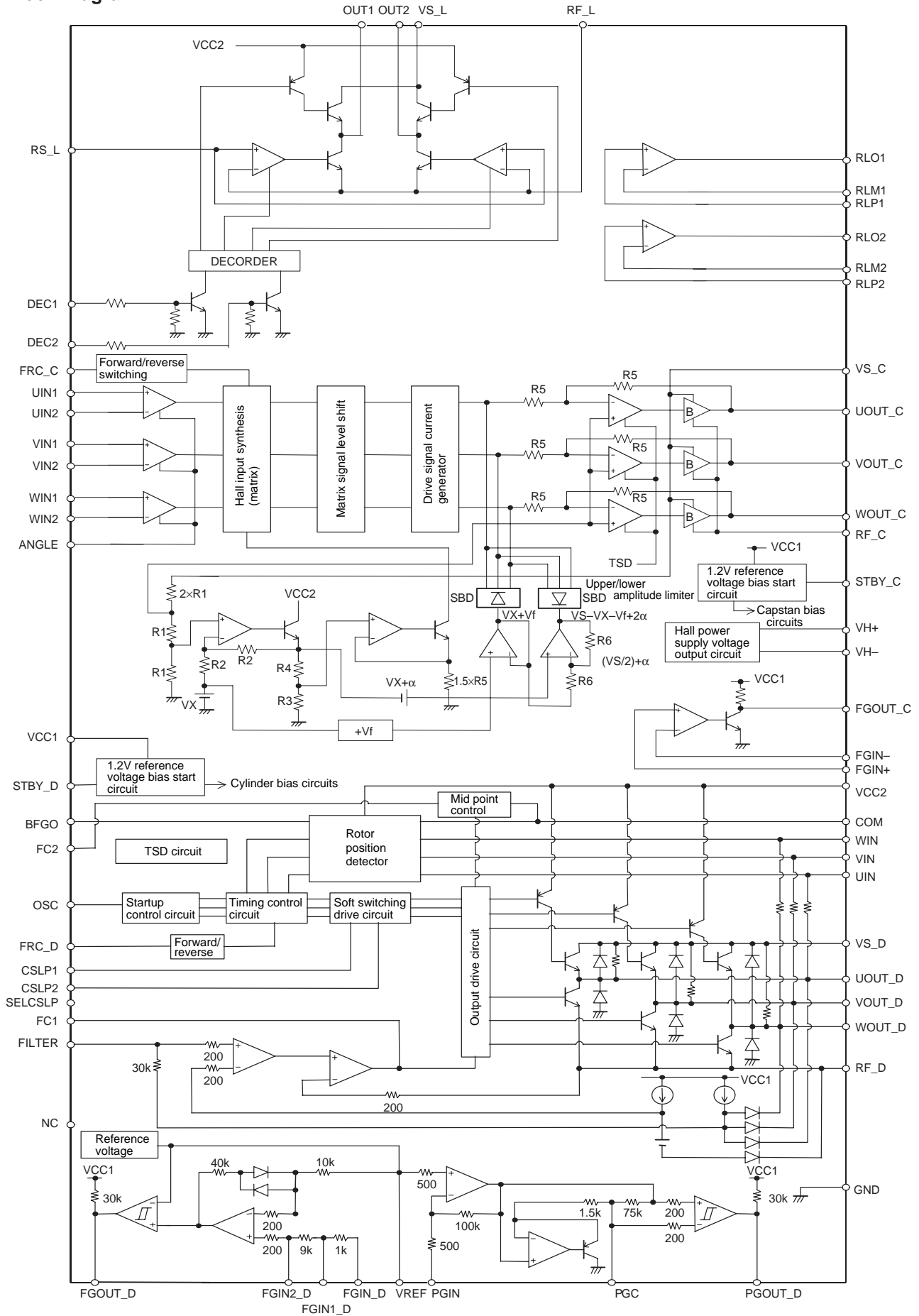
Pin Assignment



Top view



# Block Diagram



# Pin Description

| Pin number                       | Pin name                                     | Pin voltage           | Equivalent circuit | Pin function  |
|----------------------------------|--|-----------------------|--------------------|---|
| 50<br>49<br>48<br>47<br>46<br>45 | Uin1<br>Uin2<br>Vin1<br>Vin2<br>Win1<br>Win2 | 0 to V <sub>CC1</sub> |                    | Capstan motor driver U, V, W phase Hall element input/output pins. Logic High means IN1 > IN2.                                |
| 39                               | ANGLE  |                       |                    |   |
| 44                               | VS_C   | 0 to V <sub>CC2</sub> |                    | Capstan motor output amplitude control power supply pins. Voltage must be lower than V <sub>CC2</sub> .                       |
| 55<br>53<br>51<br>52             | U-OUT_C<br>V-OUT_C<br>W-OUT_C<br>RF_C        |                       |                    | Capstan motor driver U, V, W phase output pins.   |
| 43                               | VH+  |                       |                    | Hall element bias voltage supply pins. A voltage of 0.85V (typ.) is generated between VH+ and VH- (at I <sub>H</sub> = 5 mA). |
| 42                               | VH-  |                       |                    |   |

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| Pin number | Pin name | Pin voltage    | Equivalent circuit | Pin function   |
|------------|----------|----------------|--------------------|--|
| 37         | FGIN-    | 0 to $V_{CC1}$ |                    | FG comparator inverted input pin. No internal bias is applied.   |
| 38         | FGIN+    |                |                    | FG comparator non-inverted input pin. No internal bias is applied.   |
| 36         | FGOUT_C  |                |                    | FG comparator output pin. Internal load impedance is 20 kΩ.  |
| 40         | FRC_C    | 0 to $V_{CC1}$ |                    | Capstan motor forward/reverse select pin. The voltage at this pin (with hysteresis) selects forward or reverse rotation.                               |
| 2          | STBY_C   |                |                    | This pin selects bias supply to capstan circuits other than FG comparator. Setting the pin to Low cuts off the bias supply. Capstan motor standby pin. |
| 35         | FGOUT_D  |                |                    | FG amplifier output pin.   |
| 18         | OSC      |                |                    | Pin for connecting triangular wave oscillator capacitor. Serves for forced startup waveform generation.  |

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| Pin number | Pin name | Pin voltage | Equivalent circuit | Pin function  |
|------------|----------|-------------|--------------------|---|
| 19         | FC1      |             |                    | Frequency characteristics pin.<br>Connecting a capacitor between this pin and ground serves to prevent closed-loop oscillation in the current control circuitry.  |
| 20         | FILTER   |             |                    | Connecting a capacitor between this pin and ground activates the coil output saturation prevention function. In this condition, the VS pin is controlled for motor voltage control.<br>By adjusting the external capacitor, torque ripple compensation can be varied. |
| 28         | PGOUT D  |             |                    | PG amplifier output pin.  |
| 29         | PGC      |             |                    | PG amplifier peak hold capacitor connection pin.  |

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| Pin number | Pin name | Pin voltage                                    | Equivalent circuit | Pin function  |
|------------|----------|--|--------------------|---|
| 30         | PGIN     | max2.0V<br><br>min1.0V<br>(At $V_{CC} = 3V$ )  |                    | PG amplifier input pin.<br>Connect PG coil between this pin and VREF.   |
| 31         | VREF     |  |                    | Internal 1.3V reference voltage.<br>Used as reference voltage for FG and PG amplifiers.   |
| 32         | FGIN_D   | max2.0V<br><br>min1.0V<br>(At $V_{CC1} = 3V$ ) |                    | FG amplifier input pin.<br>Connect FG coil between this pin and VREF.   |
| 33         | FGIN1_D  |  |                    | FG amplifier input signal noise filter capacitor connection.  |
| 34         | FGIN2_D  |  |                    | FG amplifier input signal noise filter capacitor connection.  |
| 16         | STBY_D   | 0 to $V_{CC1}$                                 |                    | When this pin is at 0.7V or lower or when it is open, only the FG/PG amplifier operates.<br>In the motor drive state, the pin should be at 2V or higher.<br>Drum motor standby pin. |

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| Pin number | Pin name       | Pin voltage     | Equivalent circuit | Pin function   |
|------------|----------------|-----------------|--------------------|--|
| 17         | FRC_D          | 0 to $V_{CC1}$  |                    | Drum motor forward/reverse rotation select pin.<br>Low: forward (−0.2V to 0.7V or open)<br>High: reverse (2V to $V_{CC1}$ )  |
| 60         | VS_D           | 0V to $V_{CC2}$ |                    | Power supply pin for determining output amplitude by supplying drum motor voltage.<br>Must be lower than $V_{CC2}$ voltage.  |
| 41         | $V_{CC2}$      | 3.5V to 8.5V    |                    | Power supply pin for supplying source side predriver voltage and coil waveform detect comparator voltage. Common for loading, capstan, and drum motors.                          |
| 22         | $V_{CC1}$      | 2.7V to 6V      |                    | Power supply pin for circuits except motor voltage, source side predriver voltage, and coil waveform detect comparator voltage.<br>Common for loading, capstan, and drum motors. |
| 13<br>14   | CSLP1<br>CSLP2 |                 |                    | Pins for connecting triangular wave oscillator capacitor. This triangular wave coil output performs waveform soft switching.   |
| 27         | GND            |                 |                    | Ground pin for all circuits except output.   |

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| Pin number     | Pin name                   | Pin voltage           | Equivalent circuit | Pin function   |
|----------------|----------------------------|-----------------------|--------------------|--|
| 26<br>24<br>25 | WIN<br>UIN<br>VIN          |                       |                    | Coil waveform detect comparator input pins.  |
| 23             | COM                        |                       |                    | Motor coil midpoint input pin. Using this voltage as a reference, the coil voltage waveform is detected.                                     |
| 56<br>59<br>58 | WOUT_D<br>UOUT_D<br>VOUT_D |                       |                    | U, V, W phase coil output pins.  |
| 57             | RF_D                       |                       |                    | Drum motor driver output transistor ground. Constant current drive is performed by detecting the voltage at this pin.                        |
| 21             | FC2                        |                       |                    | Output midpoint control. Oscillation prevention capacitor connection pin.  |
| 12             | SELCSLP                    | 0 to V <sub>CC1</sub> |                    | When High, this pin sets CSLP slant to 15 times the slant at Low. When V <sub>CC1</sub> = 3.0V<br>2.0V or higher: High<br>0.7V or lower: Low |

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| Pin number         | Pin name                     | Pin voltage             | Equivalent circuit | Pin function   |
|--------------------|------------------------------|-------------------------|--------------------|--|
| 15                 | BFGO                         |                         |                    | Motor counter EMF voltage FG pulse pin.<br>Outputs a pulse using W phase counter EMF voltage as FG.<br>Connect to ground if not used.  |
| 5                  | VS_L                         | 2.2 to V <sub>CC2</sub> |                    | Loading motor power supply pin.<br>Stabilize against noise in the same way as for V <sub>CC2</sub> .                                   |
| 62                 | RF_L                         |                         |                    | Output transistor P-GND<br>Output current can be detected for motor current control by inserting a resistor between Rf pin and ground. |
| 63<br>61           | OUT1<br>OUT2                 |                         |                    | Loading motor driver output pins.<br>Connect to loading motor.   |
| 6<br>7<br>11<br>10 | RLM1<br>RLP1<br>RLM2<br>RLP2 | 0 to V <sub>CC1</sub>   |                    | L-FG amplifier input pins.<br>RLM1 and RLM2 are negative input.<br>RLP1 and RLP2 are positive input.                                   |

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| Pin number | Pin name     | Pin voltage             | Equivalent circuit | Pin function   |
|------------|--------------|-------------------------|--------------------|--|
| 8<br>9     | RLO1<br>RLO2 |                         |                    | R-FG amplifier output pins.  |
| 3<br>4     | DEC1<br>DEC2 | 0 to $V_{CC1}$          |                    | Loading motor input pins.<br>When $V_{CC1} = 3.0V$<br>2.0V or higher: High<br>0.6V or lower: Low |
| 64         | RS_L         | 0 to $V_{CC1}$<br>-1.5V |                    | Current limiter setting pin.<br>Set voltage between RF pin and ground, for limiting current.     |

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