

**SANYO**

No. 1542

**LC3101****128K-BIT CMOS MASK ROM**

The LC3101 is a 128k-bit CMOS mask ROM that contains an interface connectable direct to the speech synthesizer LSI LC8100. With one piece of this mask ROM, approximately 100 seconds of speech synthesis can be attained. Since it also contains an interface connectable direct to an EPROM, speech synthesis can be attained by using this mask ROM and an EPROM jointly.

A selection of 8-bit, 4-bit, or single-bit output data is allowed by means of external control. This mask ROM is also suited for use in applications other than speech synthesis.

**Features**

- ROM capacity
- Access time
- Cycle time
- Function

128K bits

25.6 $\mu$ sec typ (for operation at 200kHz typ.)30.6 $\mu$ sec typ (for operation at 200kHz typ.)

(1) Contains an interface to an EPROM.

(2) Contains an interface to the LC8100 (speech synthesizer LSI).

(3) Possible to select the bit length of output data.

• 8-bit data

• 4-bit data

• Single-bit data

- Low power dissipation
- Current dissipation

CMOS

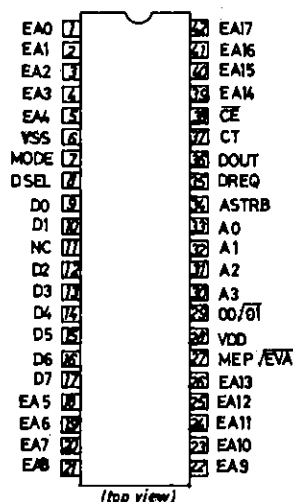
2mA max. (at operating mode)

1 $\mu$ A max. (at nonoperating mode)

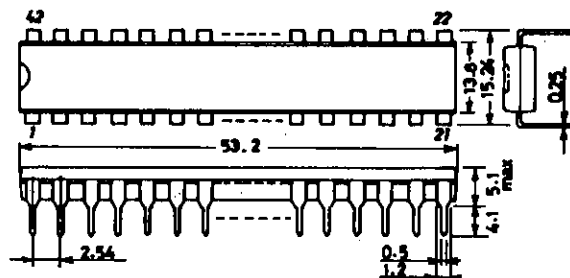
- Single +5V power supply
- Package

+2.7 to 6.0 V (supply voltage range)

DIP24

**Pin Assignment****Package Dimensions 3014A-D42IC**

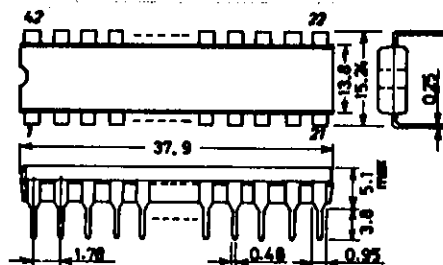
(unit: mm)



SANYO: DIP42

**Package Dimensions 3025B-D42SIC**

(unit: mm)

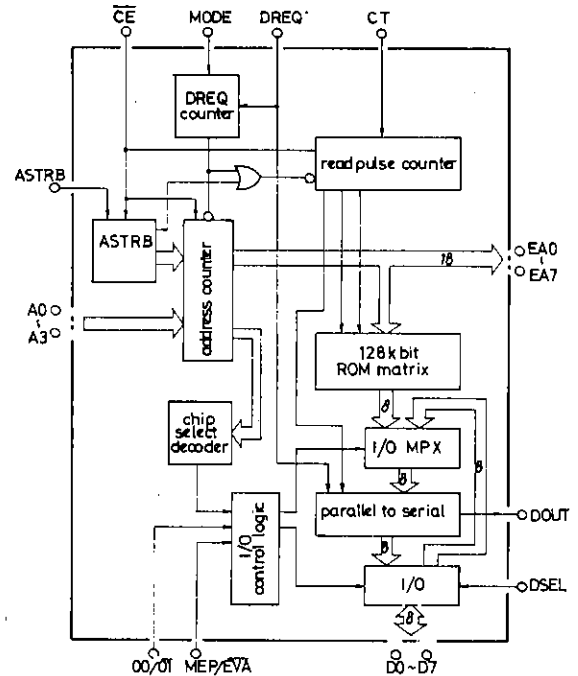


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**Equivalent Circuit Block Diagram**

- A0 to A3: 18-bit address setting pins  
 ASTRB: A0 to A3 strobe pin  
 DREQ: ROM data request pin  
 DOUT: ROM data serial output pin  
 CT: Basic operation clock input pin  
 D0 to D7: 8-bit input/output pins  
 MODE: DREQ pin input pulse count control pin  
 DSEL: Output bit length select pin  
 CE: Power-down control pin  
 EA0 to EA17: 18-bit address output pins

**Description of Operation of Internal Block**

- **ASTRB COUNTER:** Block which internally sets address information applied in 5 steps from A0 to A3 pins.
- **18bit ADDRESS COUNTER:** Address counter organized with 18 bits.
- **READ PULSE COUNTER:** Block which generates signal to operate address decoder, data selector.
- **CHIP SELECT DECODER:** Makes chip select signal with  $2^{14}$  to  $2^{17}$  bits of 18-bit address.
- **128kbit ROM MATRIX:** ROM matrix cell organized with 128K bits.
- **PARALLEL TO SERIAL:** Shift register which serially outputs 8-bit parallel data to DOUT pin.
- **I/O PORT:** Selects input/output at D0 to D7 pins.

**Pin Description**

Pin No.	Pin Name	Input/output	Function
34	ASTRB	Input	Pin for inputting strobe signal which causes data A0 to A3 to be latched at address setting mode.
35	DREQ	Input	ROM data request signal input pin.
36	DOUT	Output	Pin for outputting ROM data serially. When used in conjunction with the LC8100, this pin is connected to DIN pin of the LC8100.
37	CT	Input	Pin for inputting basic operation clock of ROM inside. When used in conjunction with the LC8100, this pin is connected to CT pin of the LC8100.

Pin No.	Pin Name	Input/output	Function
38	$\overline{CE}$	Input	Pin for controlling initialization of LSI inside immediately after application of power and internal operation stop (power-down). For performing synthesization or ROM data read-out, set $\overline{CE}$ to 'L'.
6	VSS	—	Connected to 0V of power supply.
28	VDD	—	Connected to + side of power supply.
29	00/ $\overline{01}$	Input	Always set to VSS
7	MODE	Input	Pin for controlling number of input pulses at DREQ pin. When ROM data read-out is performed serially in a single bit, set MODE to 'L'. When ROM data read-out is performed in 8 bits or 4 bits, set MODE to 'H'.
8	DSEL	Input	Used when ROM data read-out is performed in 4 bits. When DSEL is set to 'H', 24 to 27 bits are outputted to D0 to D3 pins.
9	D0	Input/output	Pins for outputting ROM data in 8 bits and inputting data in 8 bits.
10	D1		
12	D2		
13	D3		
14	D4		
15	D5		
16	D6		
17	D7		
27	MEP/ $\overline{EVA}$	Input	Open or connected to VDD.
30	A3	Input	Pins for setting 18-bit address. At address setting mode, address information is inputted by 4 bits from high-order bit downward in 5 steps.
31	A2		
32	A1		
33	A0		
1	EA0	Output	18-bit address output pins.
2	EA1		
3	EA2		
4	EA3		
5	EA4		
18	EA5		
19	EA6		
20	EA7		
21	EA8		
22	EA9		
23	EA10		
24	EA11		
25	EA12		
26	EA13		
39	EA14		
40	EA15		
41	EA16		
42	EA17		

### How to use the mask ROM and an EPROM jointly

The mask ROM and an external EPROM can be used jointly. Two selections of operation mode shown below are available by high-order 4 bits (EA14 to EA17) of 18-bit address.

Operation Mode Pins	D0 to D7	
(1)	Output	The mask ROM contents are delivered at pins D0 to D7 and DOUT.
(2)	Input	The EPROM output contents are read in from pins D0 to D7 and are delivered at pin DOUT.

### How to select the operation mode

The LC3101 contains a 4-bit chip select decoder (user option: Refer to "User mask"). Coincidence or uncoincidence with high-order 4 bits (EA14 to EA17) of 18-bit address is detected to select the operation mode.

Operation Mode	4bits of Chip Select Decoder	Operation of LC3101
(1)	Coincidence with EA14 to EA17	Pins D0 to D7: Output mode Mask ROM read enable mode
(2)	Uncoincidence with EA14 to EA17	Pins D0 to D7: Input mode Mask ROM read inhibit mode

Fig. 1 shows the schematic diagram of the control section related to these operation modes. Fig. 2 shows the assignment of 256k-byte (128k bits x 16) that can be specified by 18-bit address.

Fig. 1 Schematic Diagram of Control Section

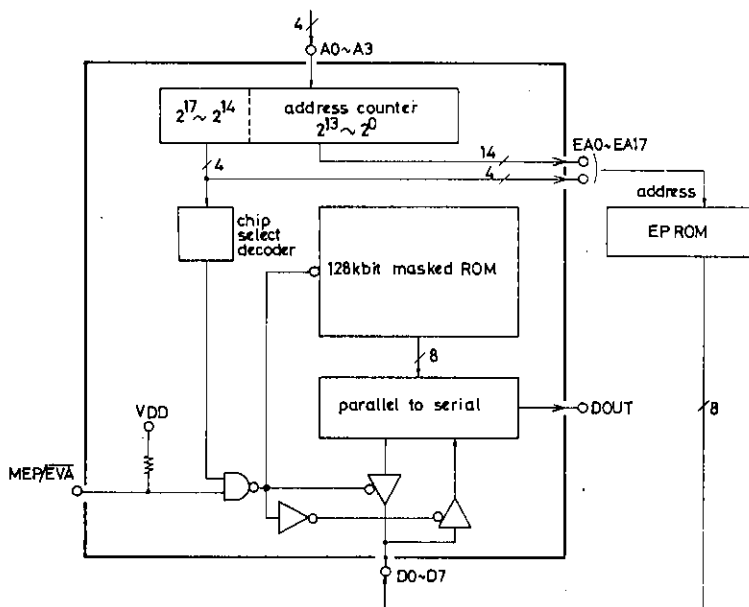
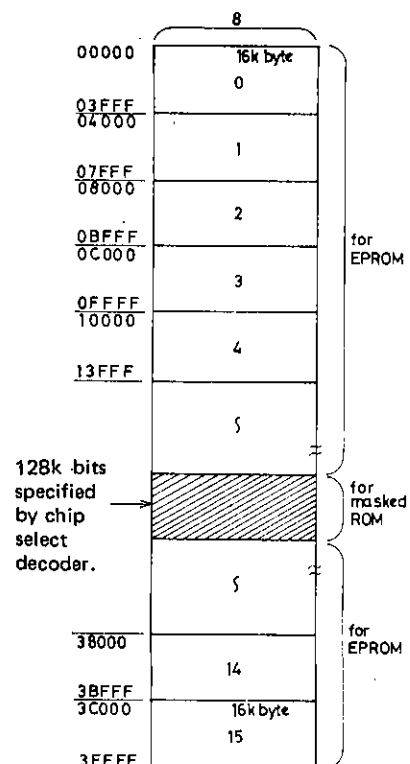
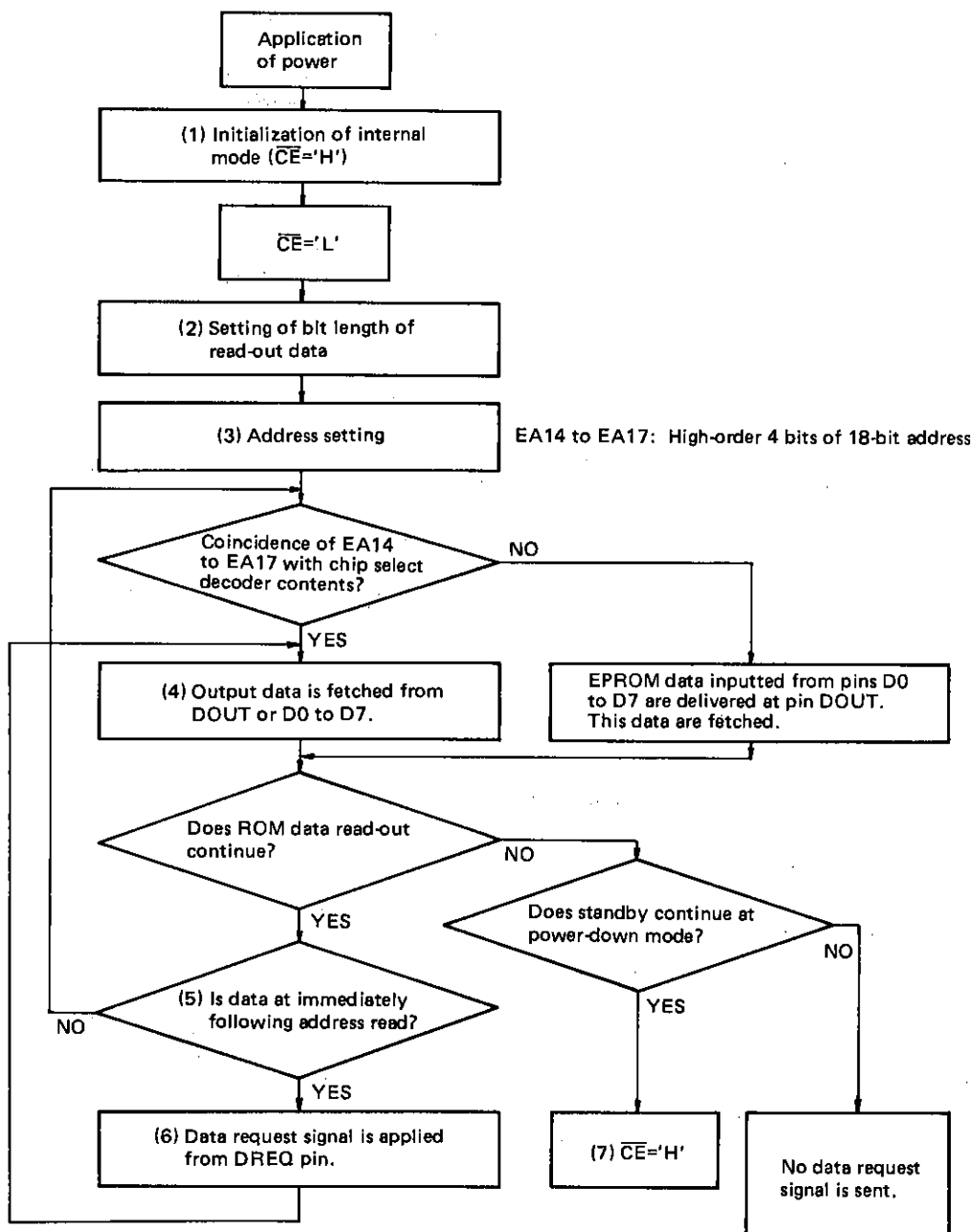


Fig. 2 Address Space Assignment



## ROM Data Read-out Procedure

The following flowchart shows the outline of read-out procedure. (1) to (7) give a more detailed description.



### (1) Initialization of internal mode

There are 4 counter blocks (ASTRB counter, 18-bit ADDRESS counter, READ PULSE counter, DREQ counter) inside the LC3101. Since initialization is required immediately after application of power, apply one 'H' level pulse to  $\overline{CE}$  pin. When  $\overline{CE}$  is set to 'L' level, the power-down mode is released (refer to (7)) and it is possible to start read-out any time.

### (2) Setting of bit length of read-out data

For the bit length of ROM data output, a selection of 3 lengths is allowed: 8 bits, 4 bits, and a single bit. For controlling this selection, MODE, DSEL pins are used. The following Table shows 3 types of pin setting.

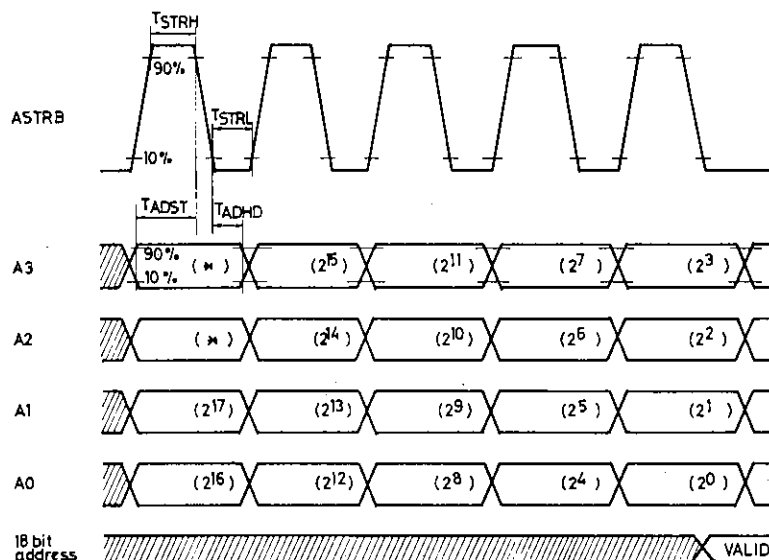
DSEL \ MODE	'L'	'H'
'L'	Single-bit length (speech synthesis)	8-bit or 4-bit length or 4-bit length (Note)
'H'	—	4-bit length (Note)

(Note) When DSEL is set to 'L',  $2^0$  to  $2^3$  bits are outputted at D0 to D3 pins.

When DSEL is set to 'H',  $2^4$  to  $2^7$  bits are outputted at D0 to D3 pins.

### (3) Address setting

Apply 5 successive pulses to ASTRB pin. Synchronously with these pulses apply 18-bit address information to A0 to A3 pins from high-order bit downward by 4 bits in 5 steps. At this address setting mode DREQ pin must be set to 'L' level. Shown below is the timing.



(Note) • "\*" = don't care.

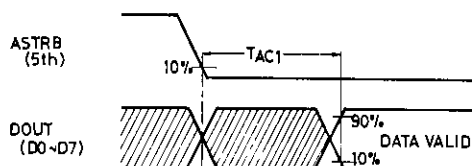
• " $2^n$ " = Binary number at the nth bit to be set in address counter.

• For the numeric values of  $T_{STRH}$ ,  $T_{STRL}$ ,  $T_{ADST}$ ,  $T_{ADHS}$ , refer to Electrical Characteristics.

### Start of read-out of set address data

Read-out of ROM data starts at the falling of the 5th ASTRB pulse or the first (MODE='H') or the 8th (MODE='L') DREQ pulse, and when access time  $T_{AC1}$  has elapsed  $2^0$  bit is outputted at DOUT pin and  $2^0$  to  $2^7$  data are outputted at D0 to D7 pins. (Refer to the following Timing Chart.)

Note) For the numeric value of  $T_{AC1}$ , refer to Electrical Characteristics.



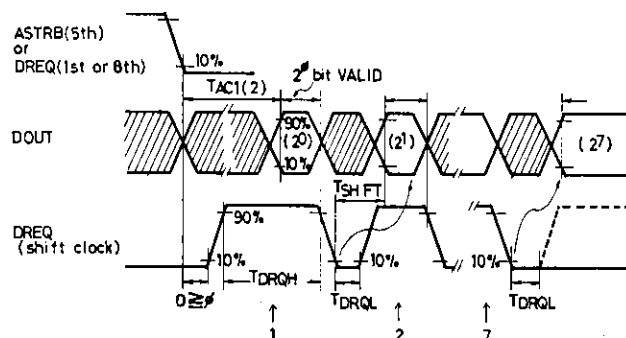
#### (4) Fetching of output data

As shown above, whenever access time  $T_{AC1}$  has elapsed, data can be fetched from output ports DOUT or D0 to D7 pins. (Pin setting as shown in Table in (2) is required.)

##### Counting one byte in a single bit from DOUT pin

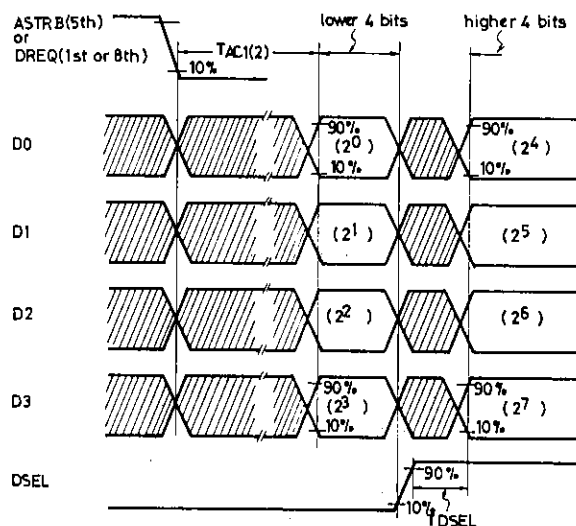
Count a single bit ( $2^n$  bit) from DOUT pin. To count the following single bit ( $2^{n+1}$  bit), apply a shift clock to DREQ pin. Shown below is Timing Chart.

For the numeric values of  $T_{AC1}$ ,  $T_{DRQH}$ ,  $T_{SHFT}$ , refer to Electrical Characteristics.



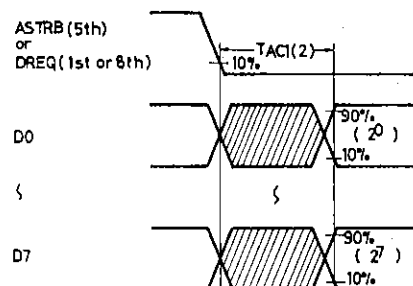
##### Counting one byte in 4-bits from D0 to D3 pins

In accordance with Table and (Note) in (2), fetch one byte from D0 to D3 pins by 4 bits in 2 steps. Shown below is Timing Chart.



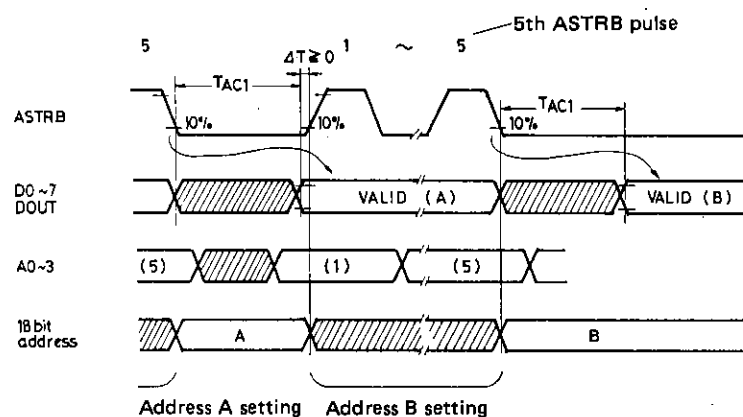
### Counting one byte in 8 bits from D0 to D7 pins

Fetch 8 bits from D0 to D7 pins. Shown below is Timing Chart.

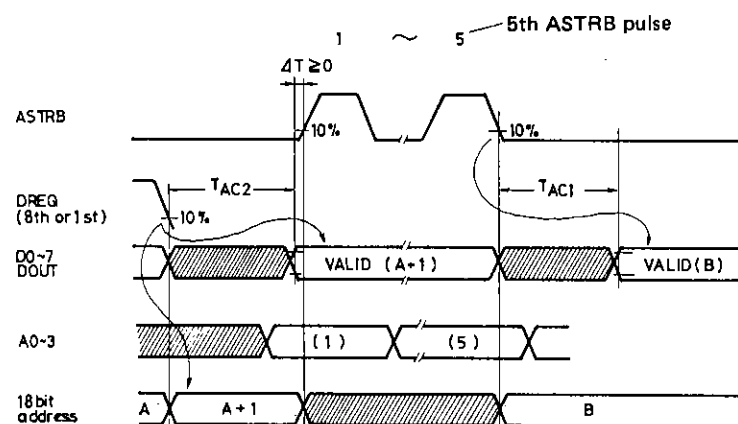


### (5) Setting address again and counting data

- (1) Timing for application of ASTRB pulse when address A is set and read out and then address B is set and read out.



- (2) Timing for application of ASTRB pulse when data is read out by application of DREQ signal (refer to (6) below) and then address B is set and read out.





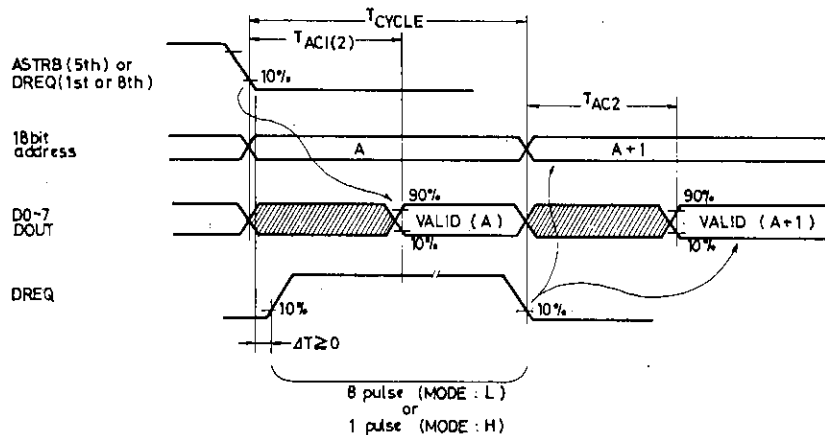
**(6) Request of ROM data at the following address**

When the signal shown below is applied to the LSI, the LSI begins to read out data at the address immediately following the address at which preceding data is read out.

Falling of 8th DREQ pulse (MODE='L')

Falling of 1st DREQ pulse (MODE='H')

Shown below is Timing Chart.



Note) Apply ROM data request signal after  $T_{CYCLE}$  or more has elapsed.  
For the numeric value of  $T_{CYCLE}$ , refer to Electrical Characteristics.

**(7) Power-down mode**

When the input at  $\overline{CE}$  pin is set to 'H' level, the LC3101 enters power-down mode (each block inside the LSI stops its operation, with no unnecessary current dissipated.). At this mode, the LSI inside becomes as follows and current dissipation is reduced.

- (1) Input at input ports (ASTRB, DREQ, A0 to A3) is inhibited.  
(It should be noted that if input is floating, current dissipation increases.)
- (2) Both address decoder and data selector in 128K-bit ROM matrix stop their internal operation.
- (3) Output at 3-state output pins DOUT, D0 to D7 is floating or fixed. (The user can select either of the two. Refer to "User mask") When  $\overline{CE}$  is set to 'H', in addition to reduction in current dissipation as mentioned above, 4 internal counters (ASTRB COUNTER, 18-BIT ADDRESS COUNTER, READ PULSE COUNTER, DREQ COUNTER) are initialized in readiness for read-out after power-down mode release ( $\overline{CE}$ ='L').

**User mask****(1) CHIP SELECT DECODER**

User mask option which makes LSI chip select signal (select, nonselect) with  $2^{14}$  to  $2^{17}$  bits of 18-bit addresses. Shown below is the output modes including  $\overline{CE}$  pin conditions.

	$\overline{CE}$ ='L'	$\overline{CE}$ ='H' (Power-down)
Chip select	DATA is outputted from DOUT, D0 to D7 pins.	Data immediately before $\overline{CE}$ ='H' occurs is held and outputted. (Note)
Chip nonselect	Output at DOUT, D0 to D7 pins has a high impedance.	Output at DOUT, D0 to D7 pins has a high impedance.

Note) In this case, the LSI only, having CHIP SELECT DECODER whose  $2^{14}$  to  $2^{17}$  bits are all 0, outputs data and all others have a high impedance.

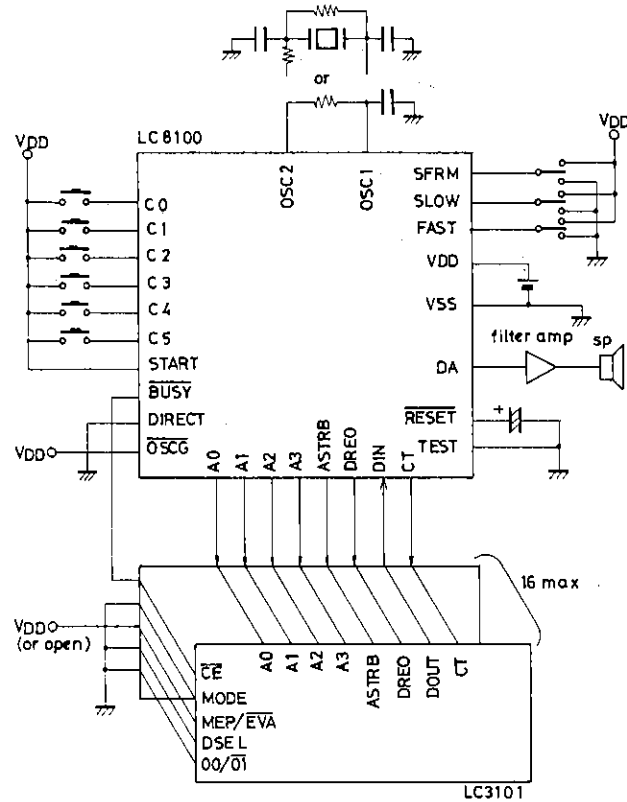
(2) SW mask

SW mask controls output at DOUT, D0 to D7 output pins in the following two ways at power-down mode. The user can select either of the two beforehand.

- (i) Output at DOUT, D0 to D7 pins is set to a high impedance.
- (ii) Data immediately before power-down mode is held and outputted.

Sample Application Circuit (1)

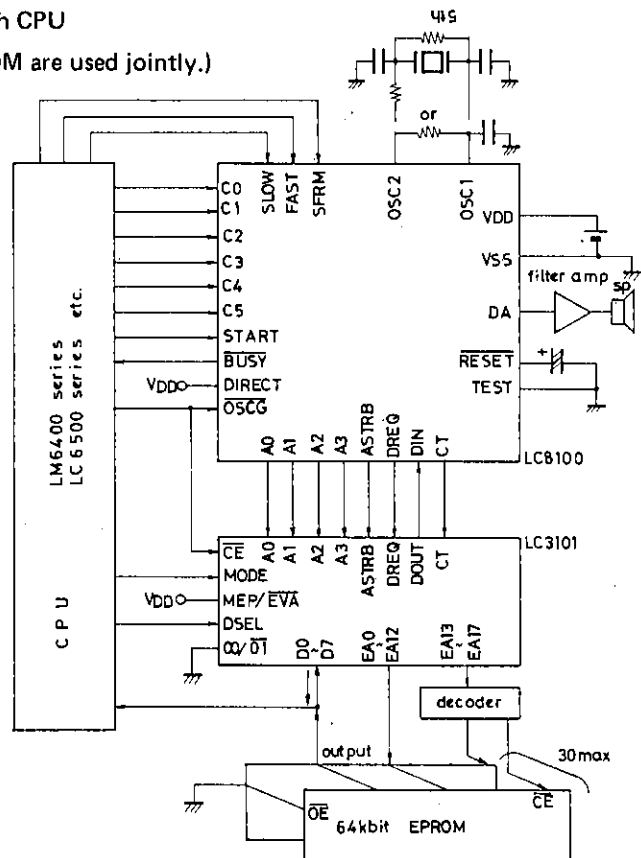
One word to one key correspondence



Sample Application Circuit (2)

CPU control: Edit and synthesis with CPU

(The mask ROM and a 64k-bit EPROM are used jointly.)



# LC3101

## Absolute Maximum Ratings at $T_a=25^\circ\text{C}$ , $V_{SS}=0\text{V}$

				unit
Maximum Supply Voltage	$V_{DD}$ max	$V_{DD}$ pin	-3.0 to +7.0	V
Input Voltage	$V_{IN}$	All input pins	-0.3 to $V_{DD}+0.3$	V
Output Voltage	$V_O$	All output pins	-0.3 to $V_{DD}+0.3$	V
Output Current	$I_O$	All output pins, per pin	-2.0 to +2.0	mA
Allowable Power Dissipation	$P_d$ max	$T_a=-30$ to $+70^\circ\text{C}$	200	mW
Operating Temperature	$T_{opr}$		-30 to +70	$^\circ\text{C}$
Storage Temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$

## Allowable Operating Ranges at $T_a=-30$ to $+70^\circ\text{C}$ , $V_{SS}=0\text{V}$ , $V_{DD}=4.5$ to $6.5\text{V}$

			min	typ	max	unit
Supply Voltage	$V_{DD}$	$V_{DD}$ pin	4.5	5.0	6.5	V
Input 'H'-Level Voltage	$V_{IH}(1)$	All input pins other than D0 to D7	$0.7V_{DD}$			V
	$V_{IH}(2)$	D0 to D7 pins	2.2			V
Input 'L'-Level Voltage	$V_{IL}(1)$	All input pins other than D0 to D7		$0.3V_{DD}$		V
	$V_{IL}(2)$	D0 to D7 pins			0.6	V
Operating Clock Frequency	$f_{CT}$	Fig. 1, $T_a=-30$ to $+60^\circ\text{C}$	150	800	960	kHz
Operating Clock 'H'-Level Pulse Width	$t_{wOH}$	Fig. 1	0.3			$\mu\text{s}$
Operating Clock 'L'-Level Pulse Width	$t_{wOL}$	Fig. 1	0.47			$\mu\text{s}$

## Electrical Characteristics at $T_a=-30$ to $+70^\circ\text{C}$ , $V_{DD}=4.5$ to $6.5\text{V}$ , $V_{SS}=0\text{V}$

			min	typ	max	unit
Input 'H'-Level Current	$I_{IH}$	$V_{IN}=V_{DD}$			1.0	$\mu\text{A}$
Input 'L'-Level Current	$I_{IL}$	$V_{IN}=V_{SS}$	-1.0			$\mu\text{A}$
Output 'H'-Level Voltage	$V_{OH}$	$I_{OH}=-0.3\text{mA}$	$V_{DD}-0.6$			V
Output 'L'-Level Voltage	$V_{OL}$	$I_{OH}=0.3\text{mA}$			0.6	V
Output OFF Leak Current	$I_{OFF1}$	$V_O=V_{DD}$ , D0 to D7, DOUT pin			1.0	$\mu\text{A}$
	$I_{OFF2}$	$V_O=V_{SS}$ , D0 to D7, DOUT pin	-1.0			$\mu\text{A}$
Input Pin Capacitance	$C_I$			5	10	pF
Pull-up Resistance	$R_{up}$	Each pin of MEP/EV $\bar{A}$ , 00/01	20		1000	k $\Omega$
Current Dissipation	$I_{DD}(1)$	At operating mode, $f_{CT}=960\text{kHz}$ , Fig. 2			2.0	mA
	$I_{DD}(2)$	At nonoperating mode, $T_a=-30$ to $+50^\circ\text{C}$ , Fig. 2			1.0	$\mu\text{A}$

## AC Characteristics at $T_a=-30$ to $+70^\circ\text{C}$ , $V_{DD}=4.5$ to $6.5\text{V}$ , $V_{SS}=0\text{V}$ , $R_L=200\text{kohm}$ , $C_P=50\text{pF}$

			min	typ	max	unit
Address Setup Time	$T_{ADST}$	Fig. 3	0.3			$\mu\text{s}$
Address Hold Time	$T_{ADHD}$	Fig. 3	0.3			$\mu\text{s}$
ASTRB 'H'-Level Pulse Width	$T_{STRH}$		0.3			$\mu\text{s}$
ASTRB 'L'-Level Pulse Width	$T_{STRL}$		0.3			$\mu\text{s}$
DREQ 'H'-Level Pulse Width	$T_{DRQH}$		0.3			$\mu\text{s}$
DREQ 'L'-Level Pulse Width	$T_{DRQL}$		0.3			$\mu\text{s}$
ASTRB Pulse Duration	$T_{ASTRB}$	Fig. 3	1.5			$\mu\text{s}$
DREQ Pulse Duration	$T_{DREQ}$	Fig. 4	1.5			$\mu\text{s}$
ROM Data Access Time (1)	$T_{AC1}$	$f_{CT}=200\text{kHz}$ typ., Fig. 5, Note 1	26.0			$\mu\text{s}$
ROM Data Access Time (2)	$T_{AC2}$	$f_{CT}=200\text{kHz}$ typ., Fig. 5, Note 1	26.0			$\mu\text{s}$
DREQ TO DOUT Delay Time	$T_{SHFT}$	Fig. 6	0.6			$\mu\text{s}$
DSEL TO D0-3 Delay Time	$T_{DSEL}$	Fig. 7	0.3			$\mu\text{s}$
Cycle Time	$T_{CYCLE}$	$f_{CT}=200\text{kHz}$ typ., Fig. 8, Note 1	30.6			$\mu\text{s}$

Fig. 1 Input waveform at CT pin

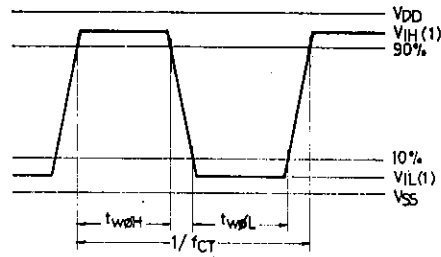


Fig. 2

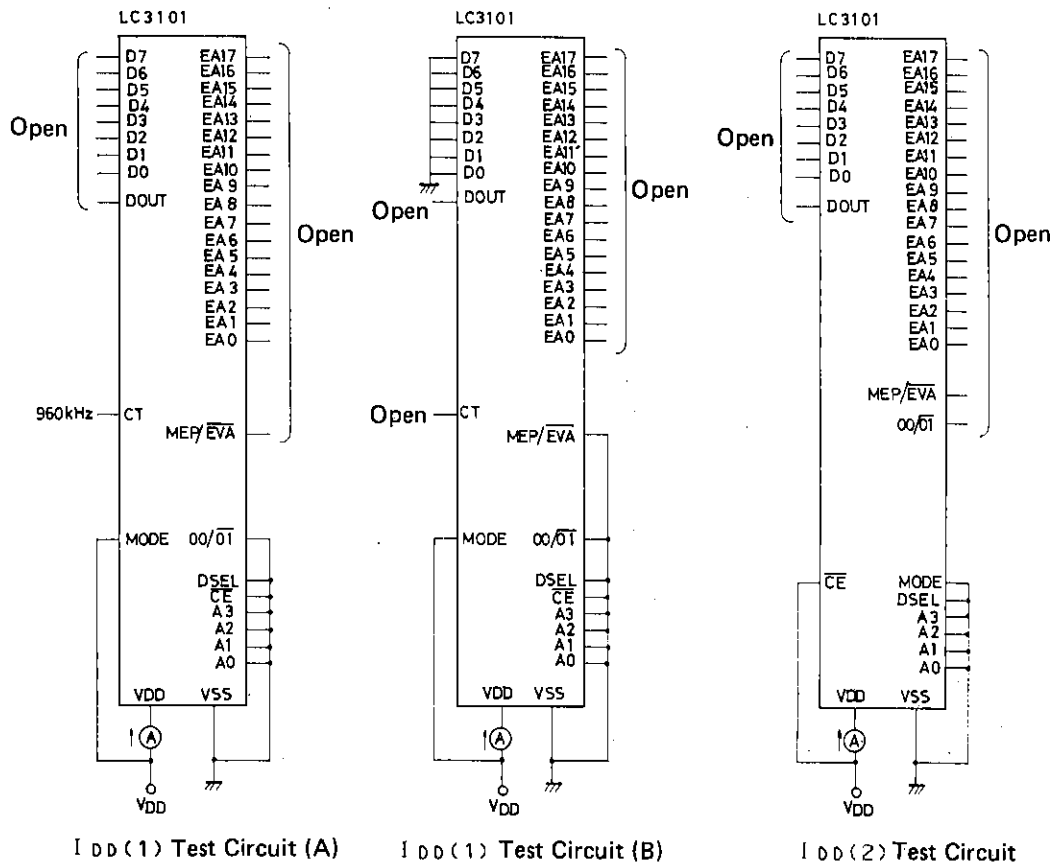


Fig. 3

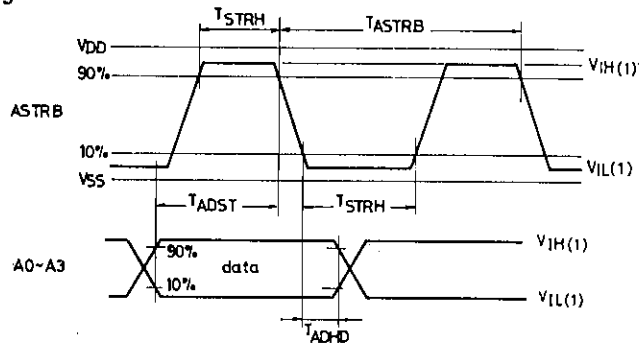


Fig. 4

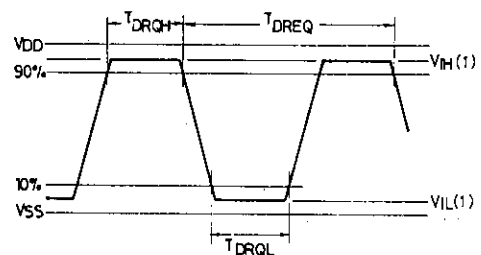


Fig. 5 (1)

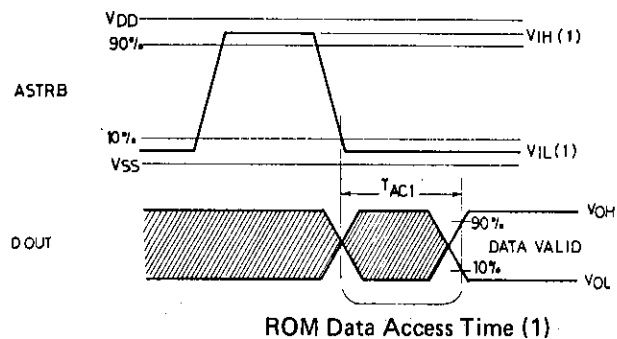


Fig. 5 (2)

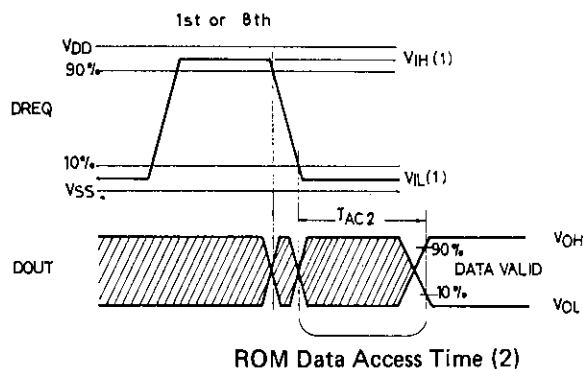


Fig. 6

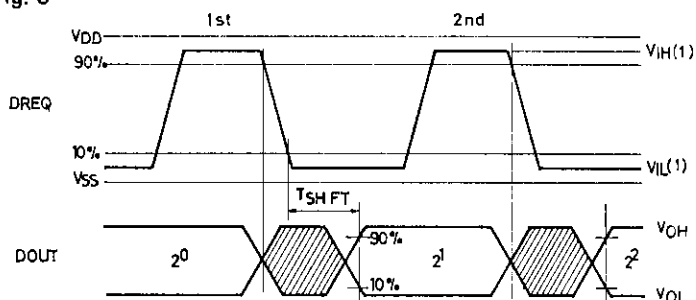


Fig. 7

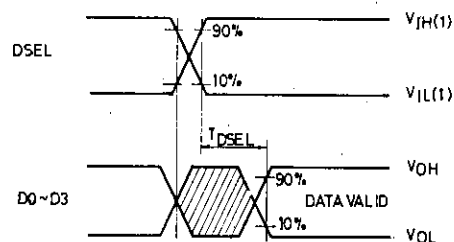
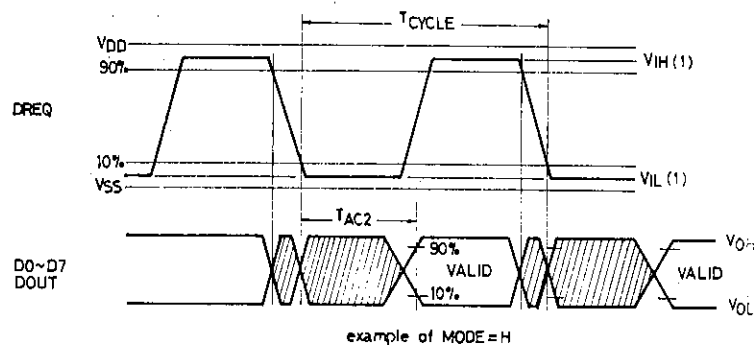


Fig. 8



Note 1 Use the following formulas to calculate  $T_{AC} \max$ ,  $T_{cycle} \max$ .

$$T_{AC} \max = \frac{5000}{f_{CT}(\text{kHz})} + 0.6 \mu\text{s} \quad T_{cycle} \max = \frac{6000}{f_{CT}(\text{kHz})} + 0.6 \mu\text{s}$$

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