

**SANYO**

No. 5082A

**LC321664BJ, BM, BT-70/80****1 MEG (65536 words × 16 bits) DRAM**  
**Fast Page Mode, Byte Write**

## Overview

The LC321664BJ, BM, BT is a CMOS dynamic RAM operating on a single 5 V power source and having a 65536 words × 16 bits configuration. Equipped with large capacity capabilities, high speed transfer rates and low power dissipation, this series is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment.

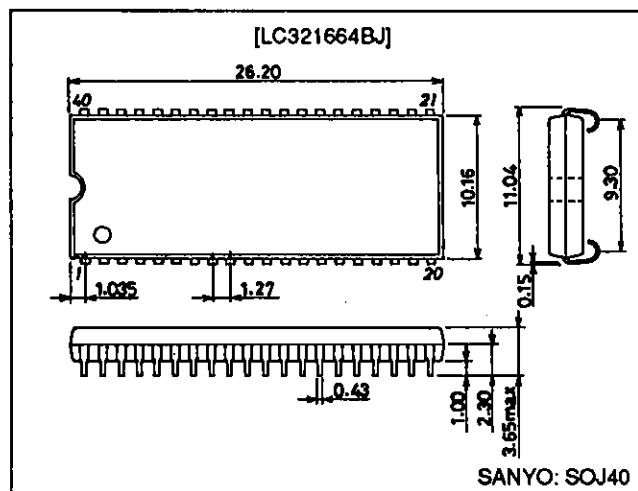
Address input utilizes a multiplexed address bus which permits it to be enclosed in a compact plastic package of 40-pin SOJ. Refresh rates are within 4 ms with 256 row address (A0 to A7) selection and support Row Address Strobe ( $\overline{\text{RAS}}$ )-only refresh, Column Address Strobe ( $\overline{\text{CAS}}$ )-before- $\overline{\text{RAS}}$  refresh and hidden refresh settings. There are functions such as fast page mode, read-modify-write and byte write.

## Features

- 65536 words × 16 bits configuration.
- Single 5 V ± 10% power supply.
- All input and output (I/O) TTL compatible.
- Supports fast page mode, read-modify-write and byte write.
- Supports output buffer control using early write and Output Enable ( $\overline{\text{OE}}$ ) control.
- 4 ms refresh using 256 refresh cycles.
- Supports  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh and hidden refresh.
- Packages
  - SOJ 40-pin (400 mil) plastic package : LC321664BJ
  - SOP 40-pin (525 mil) plastic package : LC321664BM
  - TSOP 44-pin (400 mil) plastic package : LC321664BT
- $\overline{\text{RAS}}$  access time/column address access time/ $\overline{\text{CAS}}$  access time/cycle time/power dissipation

## Package Dimensions

unit: mm

**3200-SOJ40**

Parameter		LC321664BJ, BM, BT	
		-70	-80
$\overline{\text{RAS}}$ access time		70 ns	80 ns
Column address access time		40 ns	45 ns
$\overline{\text{CAS}}$ access time		25 ns	25 ns
Cycle time		125 ns	135 ns
Power dissipation (max)	During operation	688 mW	633 mW
	During standby	5.5 mW (CMOS level)/11 mW (TTL level)	

**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**

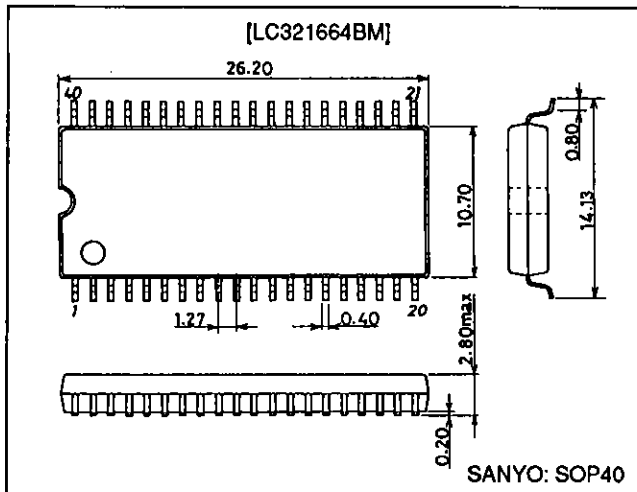
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

# LC321664BJ, BM, BT-70/80

## Package Dimensions

unit: mm

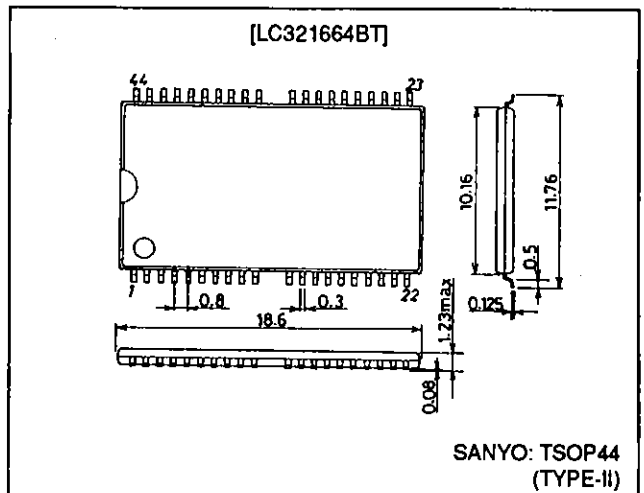
### 3195-SOP40



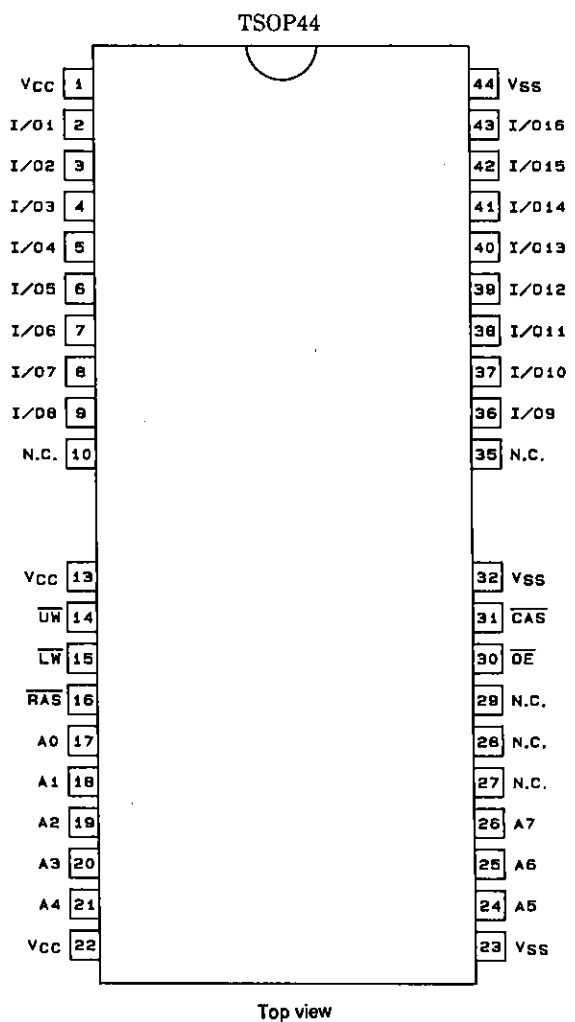
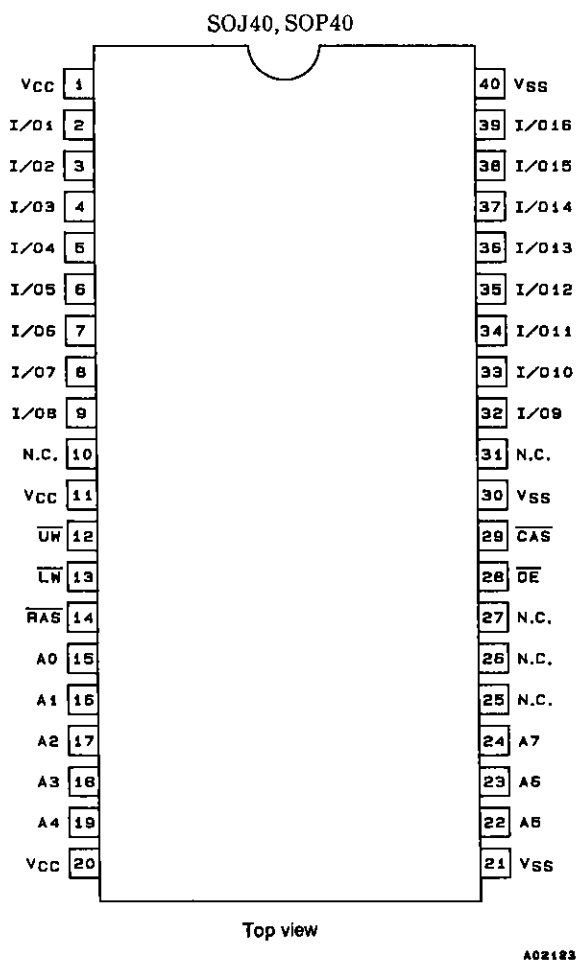
## Package Dimensions

unit: mm

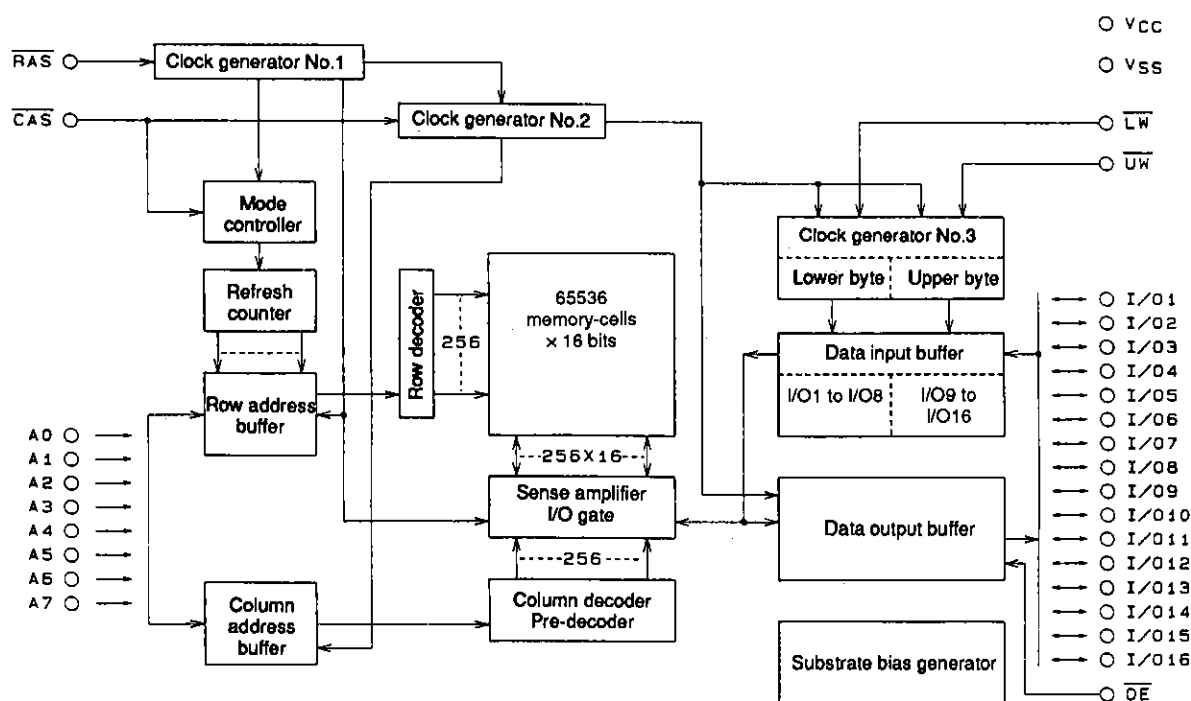
### 3207-TSOP44



## Pin Assignments



## Block Diagram



A02125

## Specifications

## Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Maximum supply voltage	$V_{CC \text{ max}}$	-1.0 to +7.0	V	1
Input voltage	$V_{IN}$	-1.0 to +7.0	V	1
Output voltage	$V_{OUT}$	-1.0 to +7.0	V	1
Allowable power dissipation	$P_d \text{ max}$	800	mW	1
		700		
Output short-circuit current	$I_{OUT}$	50	mA	1
Operating temperature range	$T_{opr}$	0 to +70	°C	1
Storage temperature range	$T_{stg}$	-55 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at  $T_a = 0$  to  $+70^\circ\text{C}$ 

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	$V_{CC}$	4.5	5.0	5.5	V	2
Input high level voltage	$V_{IH}$	2.4		6.5	V	2
Input low level voltage (A0 to A7, RAS, CAS, UW, LW, OE)	$V_{IL}$	-1.0*		+0.8	V	2
Input low level voltage (I/O1 to I/O16)	$V_{IL}$	-0.5*		+0.8	V	2

Note: 2. All voltages are referenced to  $V_{SS}$ .

A bypass capacitor of about 0.1  $\mu\text{F}$  should be connected between  $V_{CC}$  and  $V_{SS}$  of the device.

\*: -2.0 V when pulse width is less than 20 ns.

**DC Electrical Characteristics at  $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$** 

Parameter	Symbol	Conditions	LC321664BJ, BM, BT				Unit	Note
			-70		-80			
			min	max	min	max		
Operating current (Average current during operation)	I <sub>CC1</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}}$ , address cycling: $t_{\text{RC}} = t_{\text{RC min}}$		125		115	mA	3, 4, 5
Standby current	I <sub>CC2</sub>	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{IH}}$		2		2	mA	
$\overline{\text{RAS}}$ -only refresh current	I <sub>CC3</sub>	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{\text{IH}}$ : $t_{\text{RC}} = t_{\text{RC min}}$		125		115	mA	3, 5
Fast page mode current	I <sub>CC4</sub>	$\overline{\text{RAS}} = V_{\text{IL}}$ , $\overline{\text{CAS}}$ , address cycling: $t_{\text{PC}} = t_{\text{PC min}}$		80		70	mA	3, 4, 5
Standby current	I <sub>CC5</sub>	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{CC}} - 0.2 \text{ V}$		1		1	mA	
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I <sub>CC6</sub>	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling: $t_{\text{RC}} = t_{\text{RC min}}$		125		115	mA	3
Input leakage current	I <sub>IL</sub>	$0 \text{ V} \leq V_{\text{IN}} \leq 6.5 \text{ V}$ , pins other than test pin = 0 V	-10	+10	-10	+10	μA	
Output leakage current	I <sub>OL</sub>	D <sub>OUT</sub> disable, $0 \text{ V} \leq V_{\text{OUT}} \leq 5.5 \text{ V}$	-10	+10	-10	+10	μA	
Output high level voltage	V <sub>OH</sub>	I <sub>OUT</sub> = -2.5 mA	2.4		2.4		V	
Output low level voltage	V <sub>OL</sub>	I <sub>OUT</sub> = 2.1 mA		0.4		0.4	V	

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.

4.  $I_{CC1}$  and  $I_{CC4}$  are dependent on output loads. Maximum values for  $I_{CC1}$  and  $I_{CC4}$  represent values with output open.

5. Address change is less than or equal to one time during  $\overline{\text{RAS}} = V_{IL}$ . Concerning  $I_{CC4}$ , it is less than or equal to one time during 1 cycle ( $t_{PC}$ ).

**AC Electrical Characteristics at  $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$  (Notes 6, 7 and 8)**

Parameter	Symbol	LC321664BJ, BM, BT				Unit	Note
		-70		-80			
		min	max	min	max		
Random read, write cycle time	t <sub>RC</sub>	125		135		ns	
Read-write/read-modify-write cycle time	t <sub>RWC</sub>	170		180		ns	
Fast page mode cycle time	t <sub>PC</sub>	50		55		ns	
Fast page mode read-write/read-modify-write cycle time	t <sub>PRWC</sub>	95		100		ns	
RAS access time	t <sub>RAC</sub>		70		80	ns	9, 14, 15
CAS access time	t <sub>CAC</sub>		25		25	ns	9, 14
Column address access time	t <sub>AA</sub>		40		45	ns	9, 15
CAS precharge access time	t <sub>CPA</sub>		45		50	ns	9
Output low-impedance time from CAS low	t <sub>CLZ</sub>	0		0		ns	9
Output buffer turn-off delay time	t <sub>OFF</sub>	0	20	0	20	ns	10
Rise, fall time	t <sub>T</sub>	3	50	3	50	ns	
RAS precharge time	t <sub>RP</sub>	45		45		ns	
RAS pulse width	t <sub>RAS</sub>	70	10000	80	10000	ns	
RAS pulse width for fast page mode only	t <sub>RASP</sub>	70	100000	80	100000	ns	
RAS hold time	t <sub>RSH</sub>	25		25		ns	
CAS hold time	t <sub>CSH</sub>	70		80		ns	
CAS pulse width	t <sub>CAS</sub>	25	10000	25	10000	ns	
RAS to CAS delay time	t <sub>RCD</sub>	20	45	20	55	ns	14
RAS to column address delay time	t <sub>RAD</sub>	15	30	15	35	ns	15
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		ns	
CAS precharge time	t <sub>CP</sub>	10		10		ns	
Row address setup time	t <sub>ASR</sub>	0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		10		ns	
Column address setup time	t <sub>ASC</sub>	0		0		ns	
Column address hold time	t <sub>CAH</sub>	15		15		ns	
Column address hold time referenced to RAS	t <sub>AR</sub>	50		55		ns	
Column address to RAS lead time	t <sub>RAL</sub>	35		40		ns	
Read command setup time	t <sub>RCS</sub>	0		0		ns	
Read command hold time referenced to CAS	t <sub>RCH</sub>	0		0		ns	11
Read command hold time referenced to RAS	t <sub>RRH</sub>	0		0		ns	11
Write command hold time	t <sub>WCH</sub>	15		15		ns	
Write command hold time referenced to RAS	t <sub>WCR</sub>	50		55		ns	

Continued on next page.

# LC321664BJ, BM, BT-70/80

Continued from preceding page.

Parameter	Symbol	LC321664BJ, BM, BT				Unit	Note
		-70		-80			
		min	max	min	max		
Write command pulse width	tWP	15		15		ns	
Write command to RAS lead time	tRWL	20		20		ns	
Write command to CAS lead time	tCWL	20		20		ns	
Data input setup time	tDS	0		0		ns	12
Data input hold time	tDH	15		15		ns	12
Data input hold time referenced to RAS	tDHR	50		55		ns	
Refresh time	tREF		4		4	ms	
Write command setup time	tWCS	0		0		ns	13
CAS to UW, LW delay time	tCWD	45		45		ns	13
RAS to UW, LW delay time	tRWD	90		100		ns	13
Column address to UW, LW delay time	tAWD	60		65		ns	13
CAS precharge UW, LW delay time for fast page mode cycle only	tCPWD	65		70		ns	13
CAS setup time for CAS-before-RAS	tCSR	10		10		ns	
CAS hold time for CAS-before-RAS	tCHR	10		10		ns	
RAS precharge CAS active time	tRPC	10		10		ns	
CAS precharge time for CAS-before-RAS counter test	tCPT	40		40		ns	
RAS hold time referenced to OE	tROH	15		15		ns	
OE access time	tOEA		25		25	ns	9
OE delay time	tOED	15		15		ns	
OE output buffer turn-off delay time	tOEZ	0	15	0	15	ns	10
OE command hold time	tOEH	20		20		ns	
Data input to CAS delay time	tDZC	0		0		ns	16
Data input to OE delay time	tDZO	0		0		ns	16
Masked write setup time	tMCS	0		0		ns	
Masked write hold time referenced to RAS	tMRH	0		0		ns	
Masked write hold time referenced to CAS	tMCH	0		0		ns	

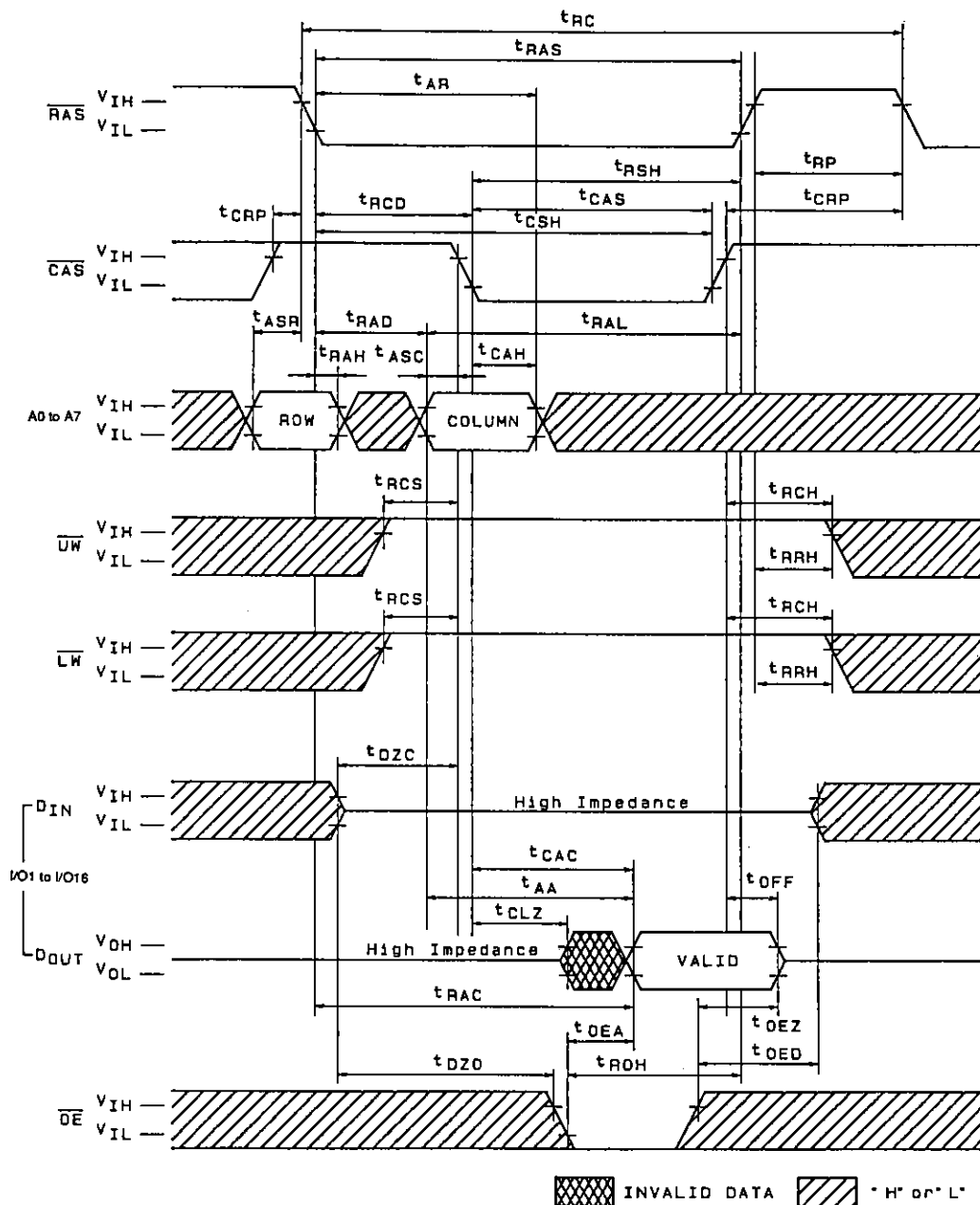
## Input/Output Capacitance at $T_a = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	min	max	Unit	Note
Input capacitance ( $A_0$ to $A_7$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{UW}$ , $\overline{LW}$ , $\overline{OE}$ )	$C_{IN}$		7	pF	
Input/Output capacitance ( $I/O_1$ to $I/O_{16}$ )	$C_{IO}$		7	pF	

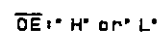
- Note:
- An initial pause of 200  $\mu\text{s}$  is required after power-up followed by eight  $\overline{RAS}$ -only refresh cycles before proper device operation is achieved. In case of using refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles instead of eight  $\overline{RAS}$ -only refresh cycles are required.
  - Measured at  $t_T = 5\text{ ns}$ .
  - When measuring input signal timing,  $V_{IH}$  (min) and  $V_{IL}$  (max) are used for reference points. In addition, rise and fall time are defined between  $V_{IH}$  and  $V_{IL}$ .
  - Measured using an equivalent of 50 pF and one standard TTL loads.
  - $t_{OFF}$  (max) and  $t_{OEZ}$  (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.
  - Operation is guaranteed if either  $t_{RRH}$  or  $t_{RCH}$  is satisfied.
  - These parameters are measured from the falling edge of  $\overline{CAS}$  for an early-write cycle, and from the falling edge of  $\overline{UW}$  and  $\overline{LW}$  for a read-write/read-modify-write cycle.
  - $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters for memory in that they specify the operating mode. If  $t_{WCS} \geq t_{WCS}$  (min), the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle.  
If  $t_{CWD} \geq t_{CWD}$  (min),  $t_{RWD} \geq t_{RWD}$  (min),  $t_{AWD} \geq t_{AWD}$  (min) and  $t_{CPWD} \geq t_{CPWD}$  (min) for fast page mode cycle only, the cycle switches to a read-write/read-modify-write cycle and data output equal information in the selected cells. If neither of the above timings are satisfied, output pins are in an undefined state.
  - $t_{RCD}$  (max) is not a restrictive operating parameter but instead represents the point at which the access time  $t_{RAC}$  (max) is guaranteed. If  $t_{RCD} \geq t_{RCD}$  (max), access time is determined according to  $t_{RAC}$ .
  - $t_{RAD}$  (max) is not a restrictive operating parameter but instead represents the point at which the access time  $t_{RAC}$  (max) is guaranteed. If  $t_{RAD} \geq t_{RAD}$  (max), access time is determined according to  $t_{AA}$ .
  - Operation is guaranteed if either  $t_{DZC}$  or  $t_{DZO}$  is satisfied.

# Timing Chart

## Read Cycle



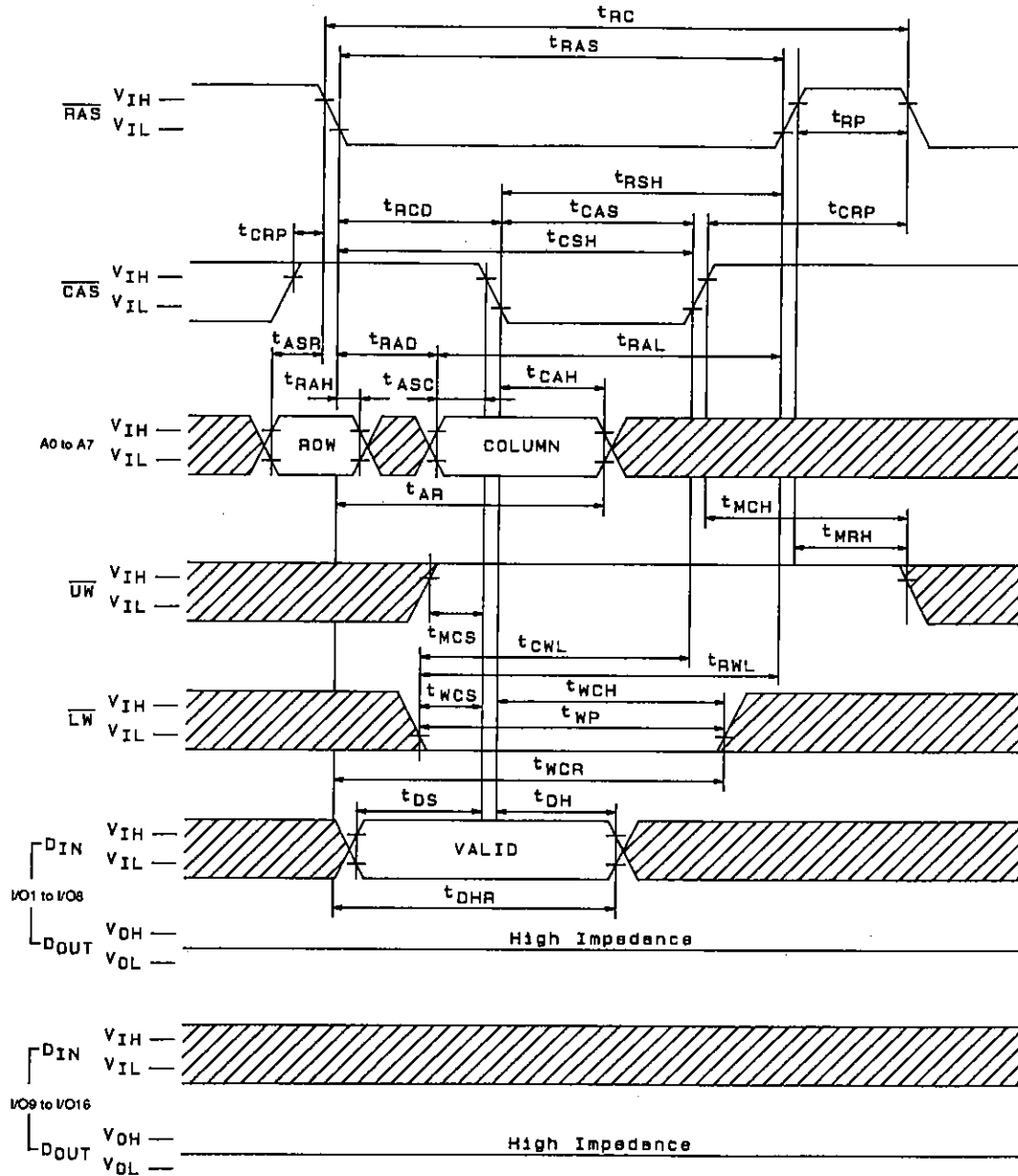
A02139



A02140



Lower Byte Early Write Cycle



• H\* or\* L\*

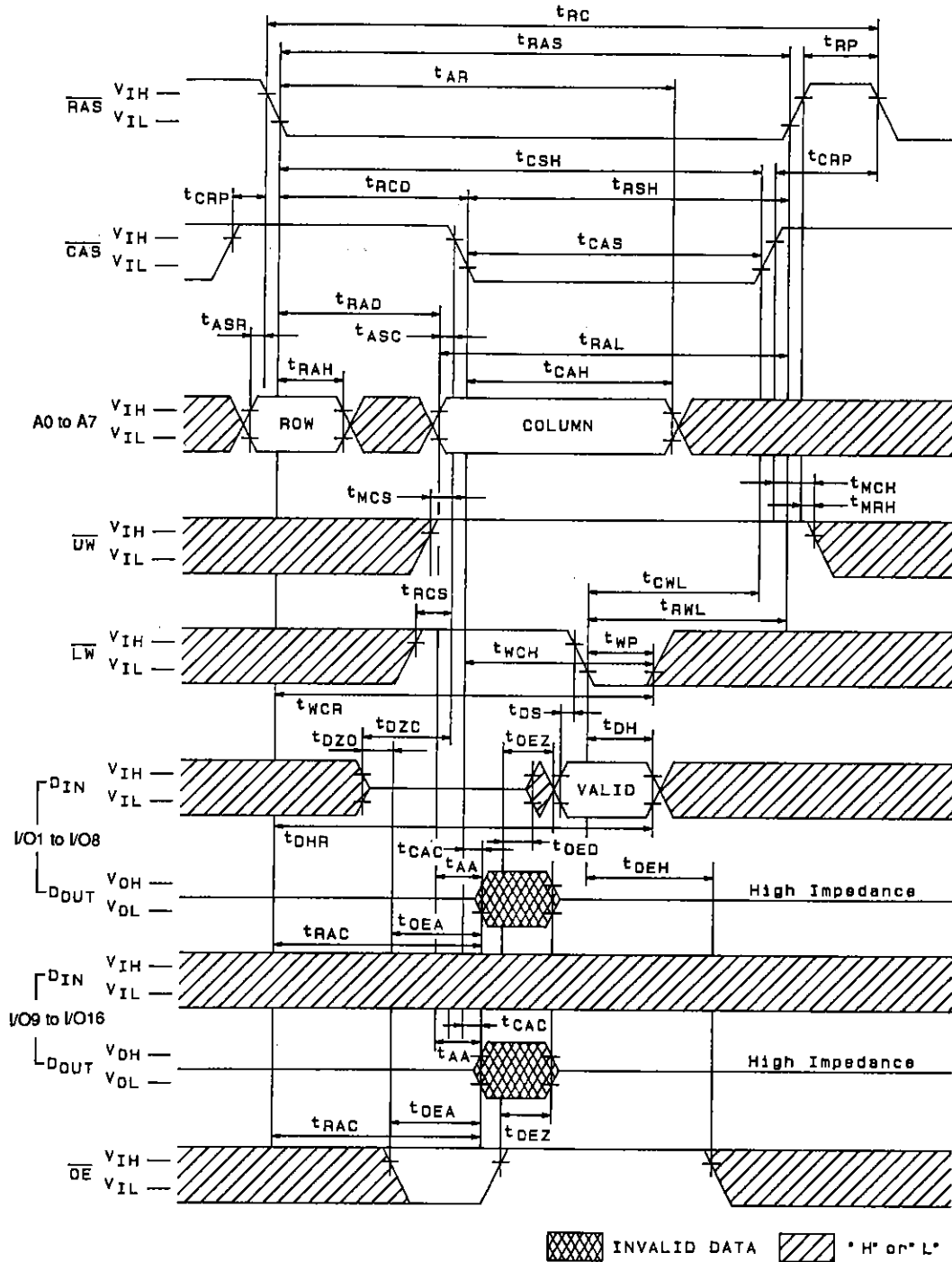
OE: H\* or\* L\*

A02142



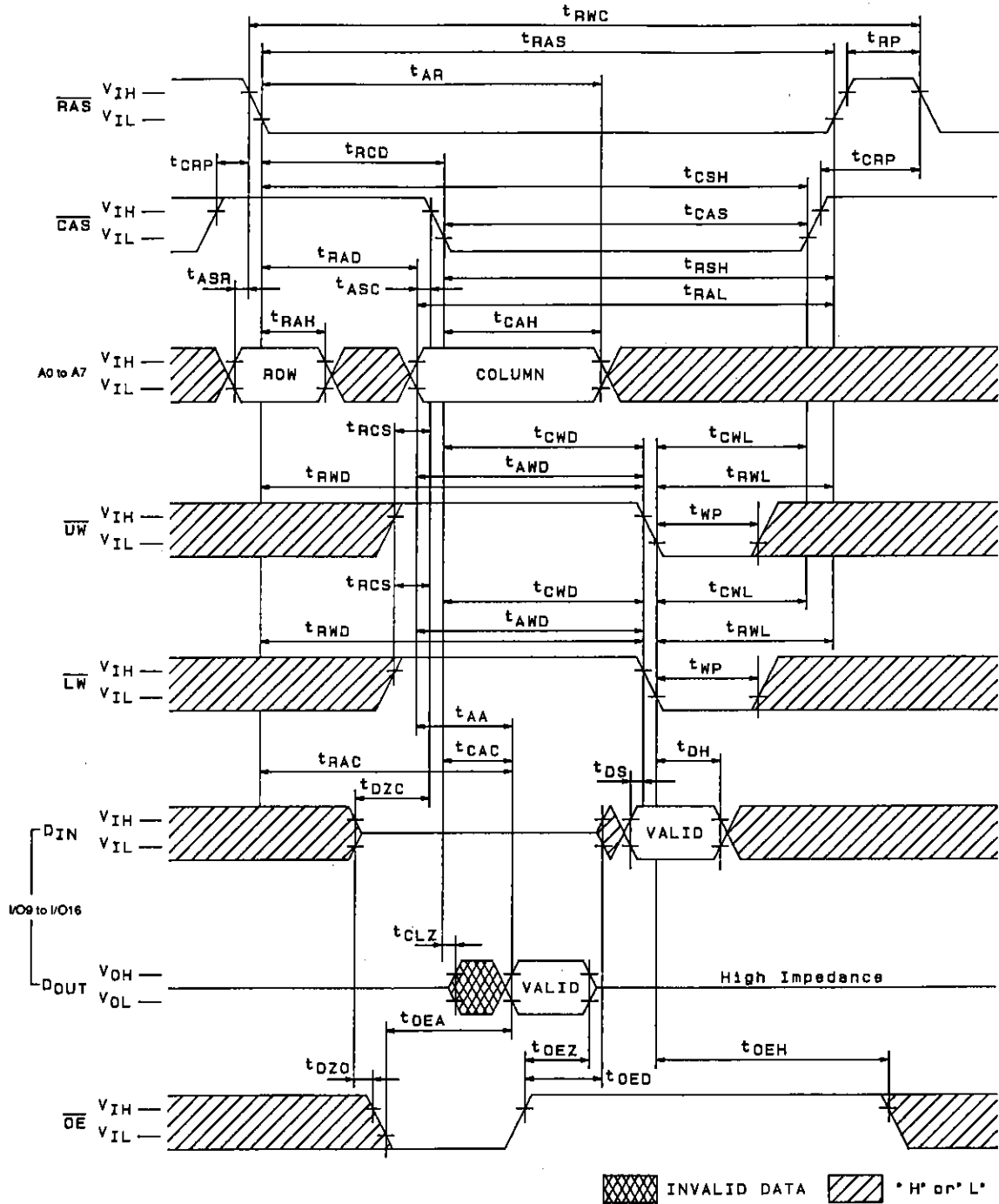


Lower Byte Write Cycle ( $\overline{OE}$  Control)



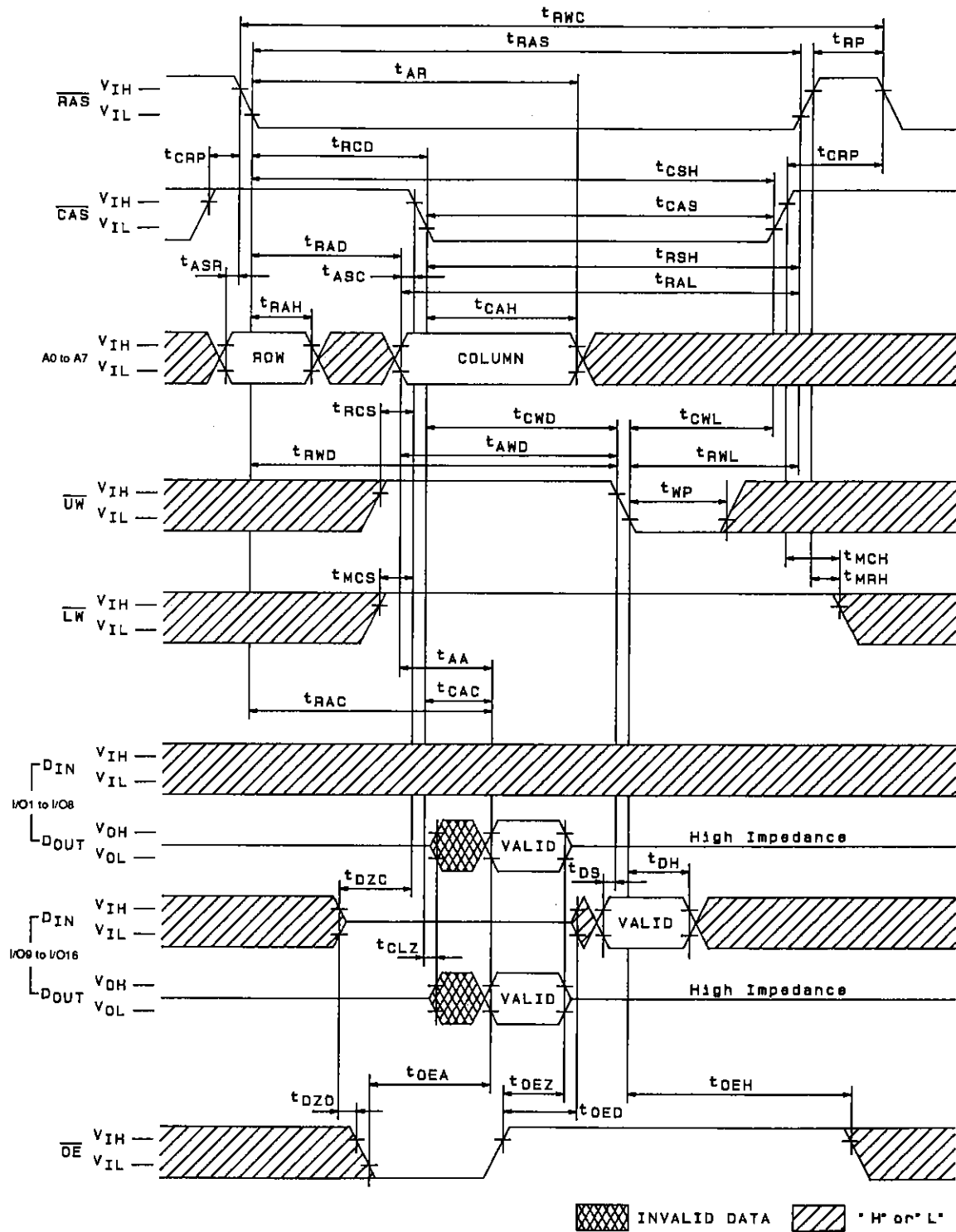
A02145

Read-Modify Write Cycle



A02146

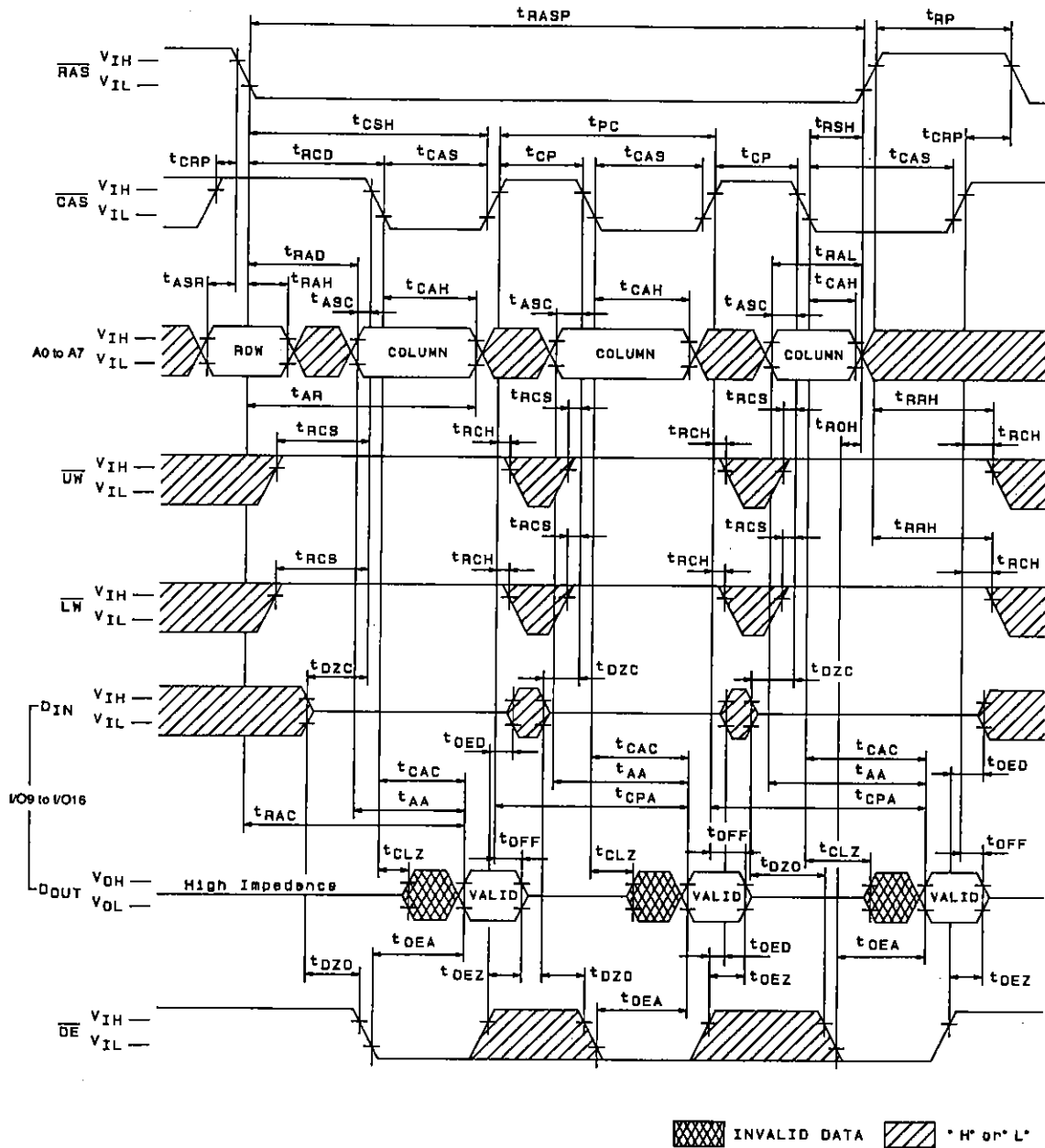
Read-Modify Upper Byte Write Cycle



A02147

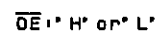


Fast Page Mode Read Cycle



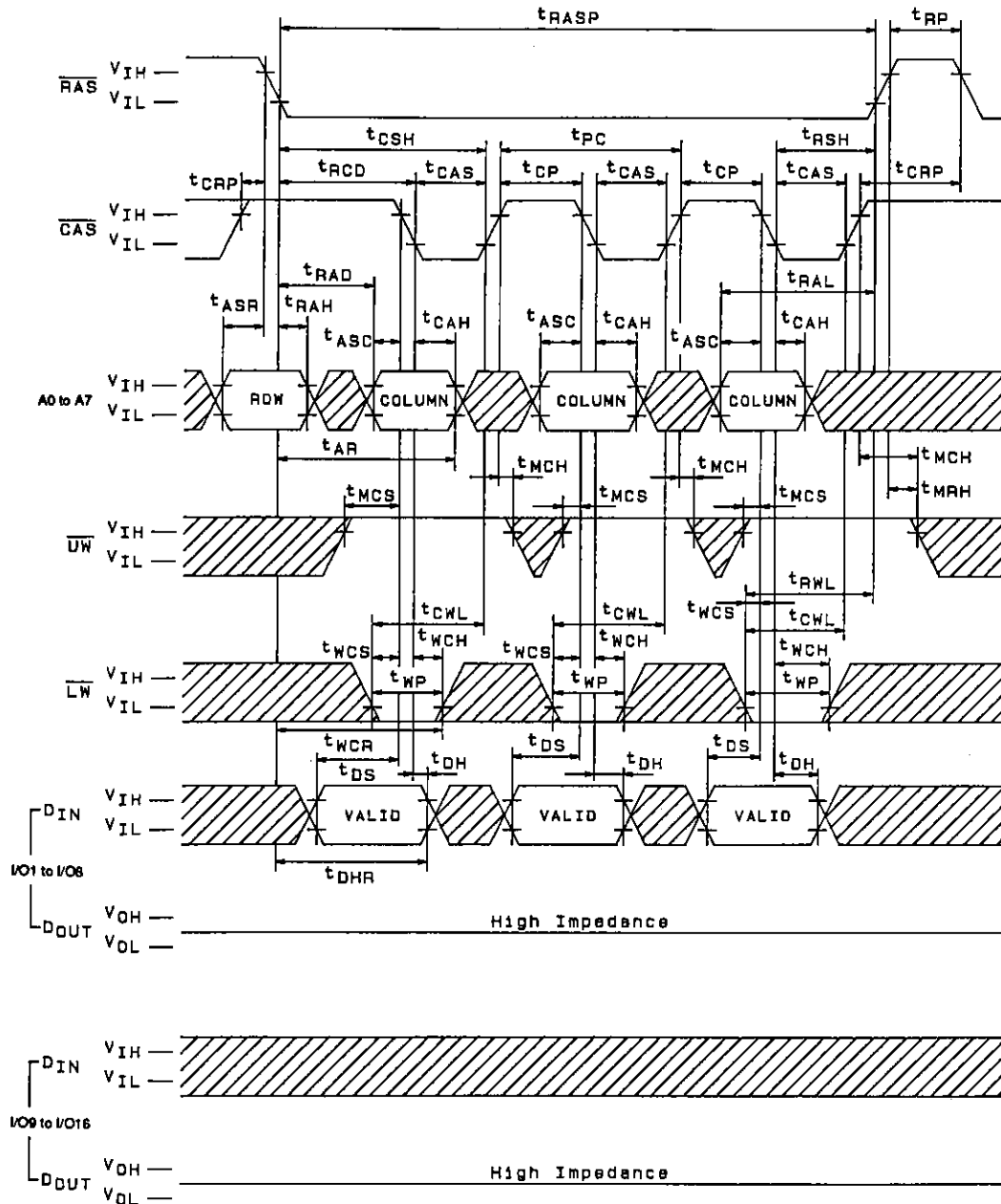
A02149





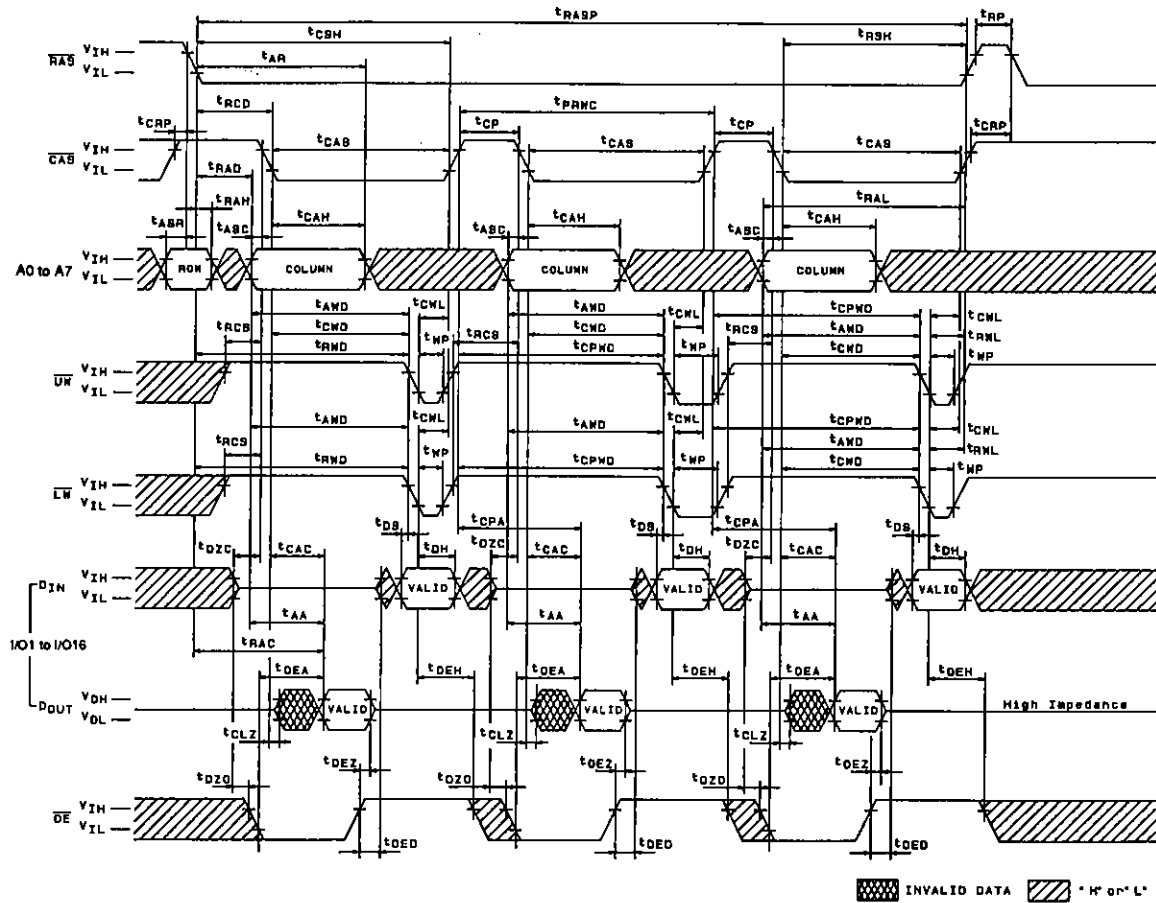
A02101

Fast Page Mode Lower Byte Early Write Cycle



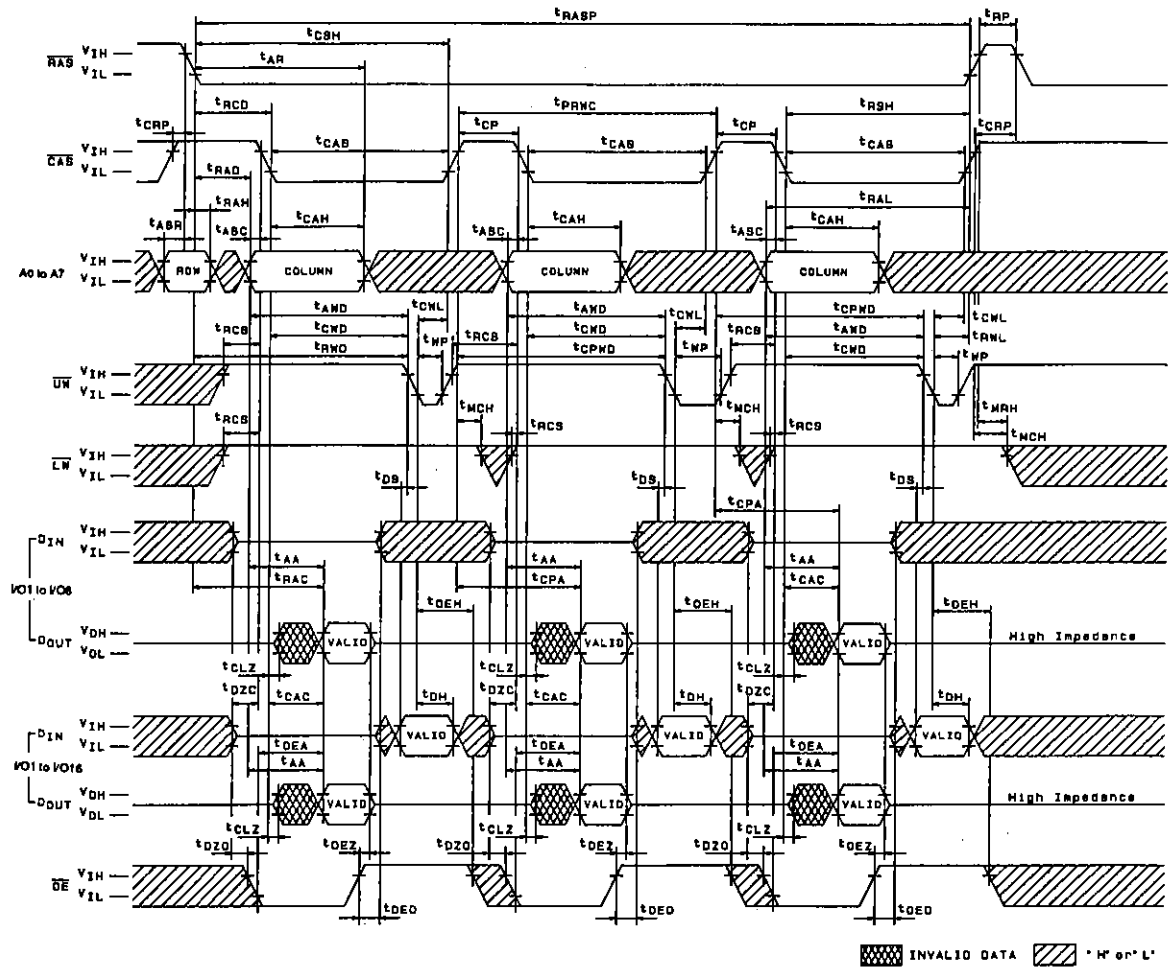
A02152

Fast Page Mode Read-Modify-Write Cycle



A03277

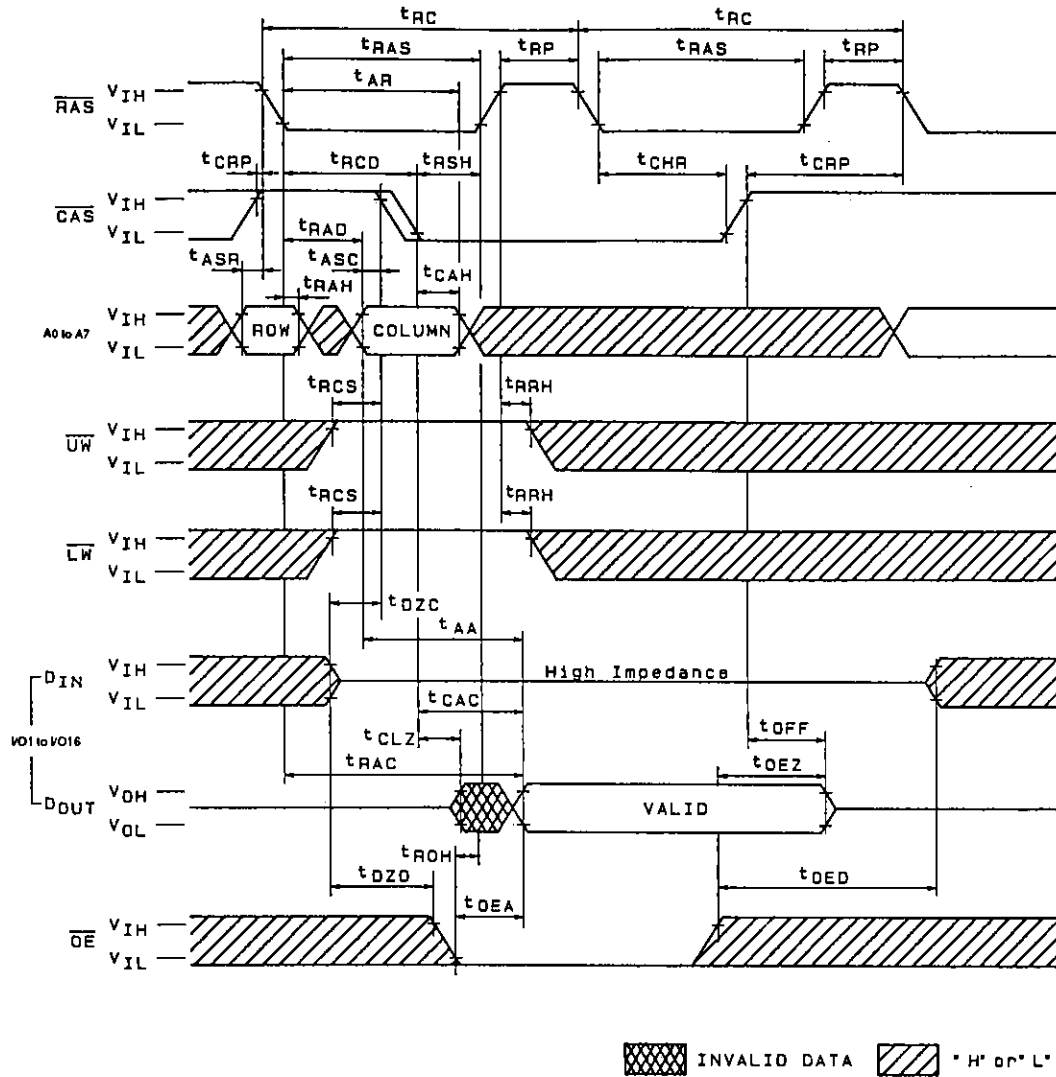
## Fast Page Mode Read-Modify Upper Byte Write Cycle



A03278

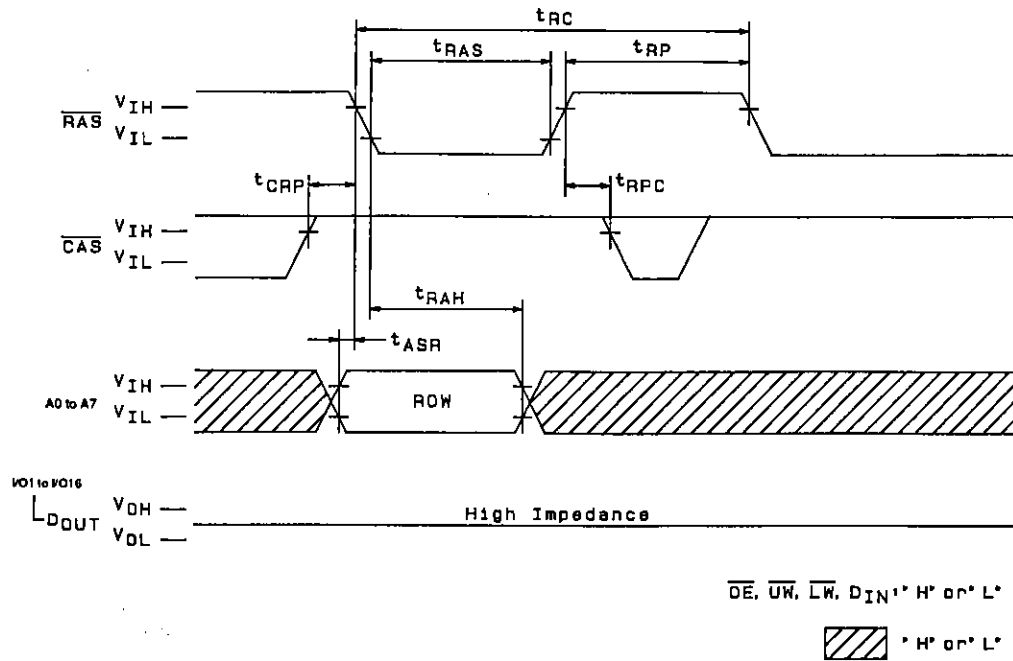


## Hidden Refresh Cycle



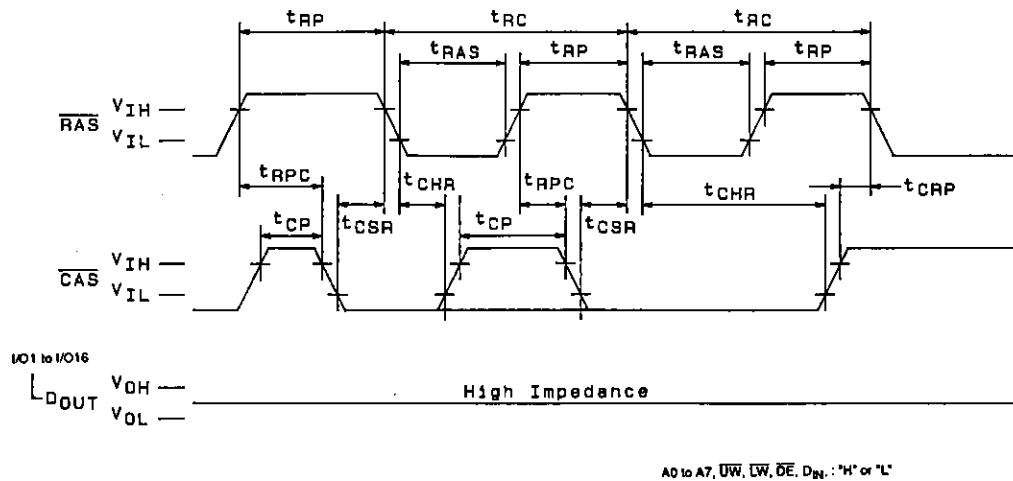
A03280

### RAS-Only Refresh Cycle



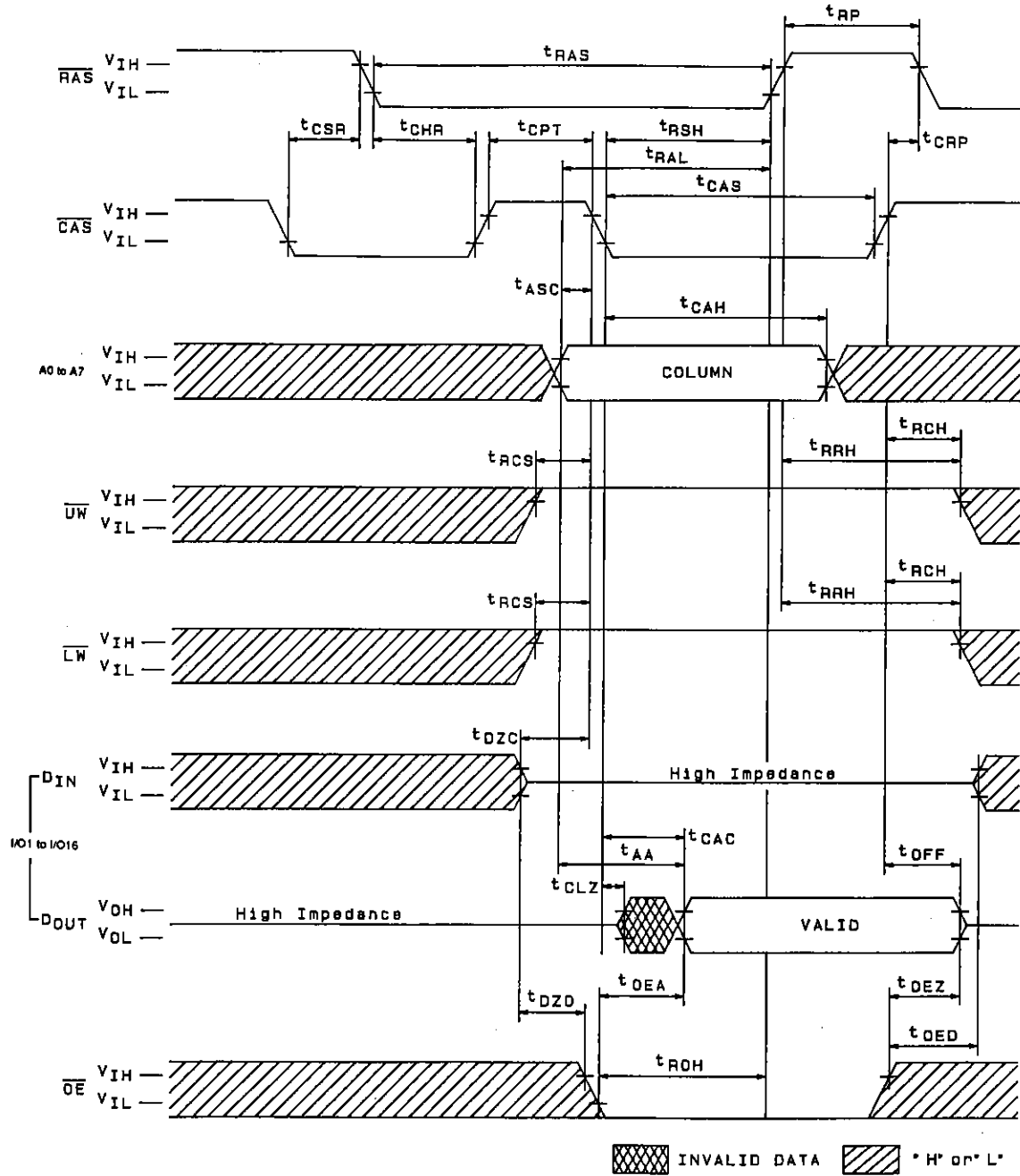
A02157

### CAS-Before-RAS Refresh Cycle



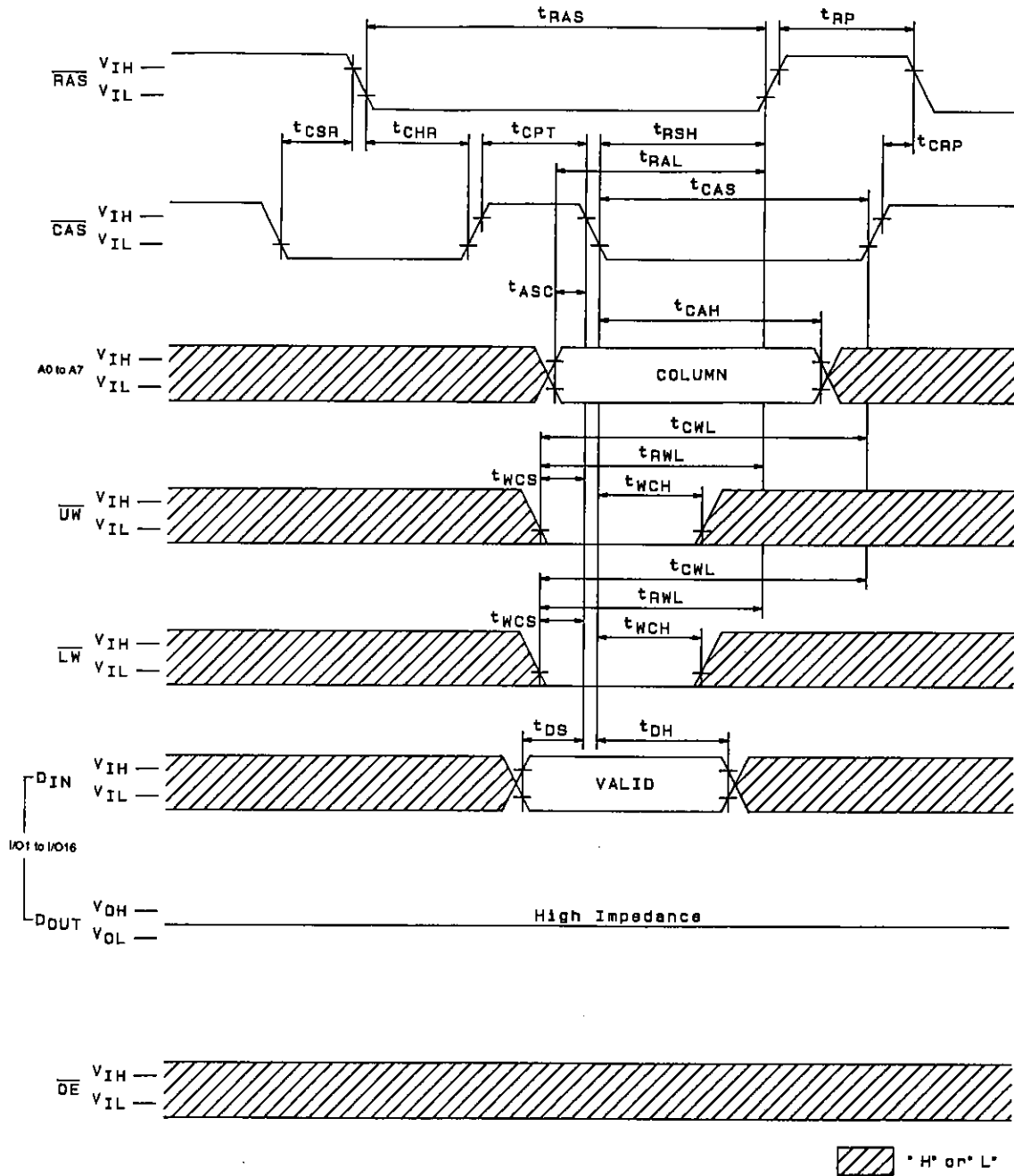
A02158

**CAS-Before-RAS Refresh Counter Test Cycle (Read)**



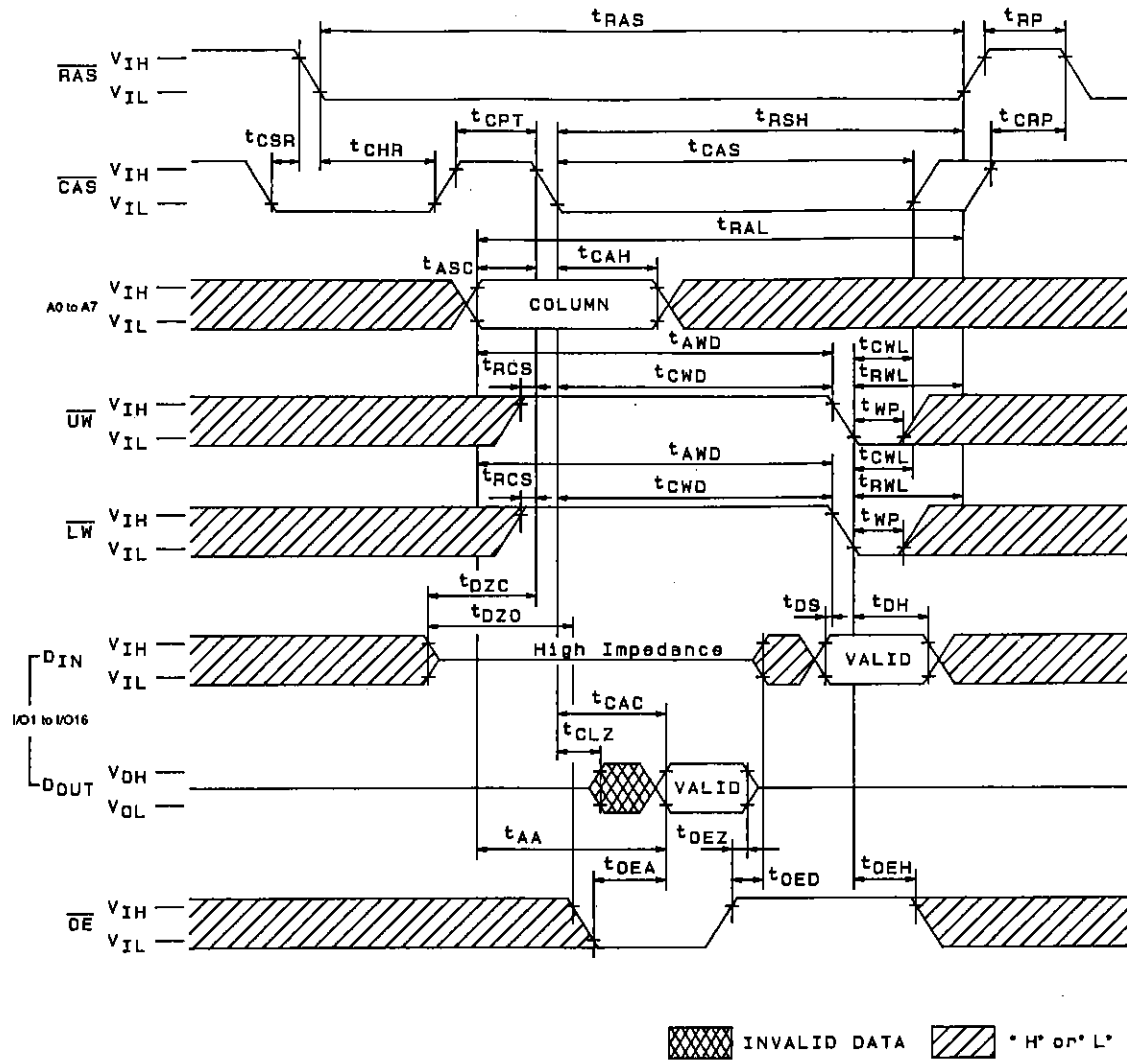
A02159

**CAS-Before-RAS Refresh Counter Test Cycle (Write)**



A02160

**CAS-Before-RAS Refresh Counter Test Cycle (Read-Modify-Write)**



A021B1

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
  - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of March, 1996. Specifications and information herein are subject to change without notice.