



LC35256D-10, LC35256DM, DT-70/10

Dual Control Pins: \overline{OE} and \overline{CE}
256K (32768-word \times 8-bit) SRAM

Overview

The LC35256D, LC35256DM, and LC35256DT are 32768-word \times 8-bit asynchronous silicon gate CMOS static RAMs. These devices use a 6-transistor full CMOS memory cell, and feature low-voltage operation, low current drain, and an ultralow standby current. They provide two control signal inputs: an \overline{OE} input for high-speed access and a chip select (\overline{CE}) input for device selection and low power operating mode. This makes these devices optimal for systems that require low power or battery backup, and they allow memory to be expanded easily. Their ultralow standby current allows capacitor-based backup to be used as well. Since they support 3-V operation, they are appropriate for use in portable systems that operate from batteries.

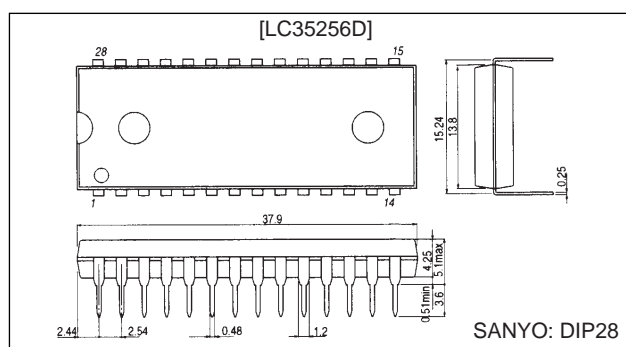
Features

- Supply voltage range: 2.7 to 5.5 V
 - 5-V operation: 5.0 V \pm 10%
 - 3-V operation: 2.7 to 3.6 V
- Access times
 - 5-V operation
 - LC35256DM, DT-70: 70 ns (max)
 - LC35256D, DM, DT-10: 100 ns (max)
 - 3-V operation
 - LC35256DM, DT-70: 200 ns (max)
 - LC35256D, DM, DT-10: 500 ns (max)
- Standby current
 - 5-V operation: 1.0 μ A ($T_a \leq 60^\circ\text{C}$),
5.0 μ A ($T_a \leq 85^\circ\text{C}$)
 - 3-V operation: 0.8 μ A ($T_a \leq 60^\circ\text{C}$),
4.0 μ A ($T_a \leq 85^\circ\text{C}$)
- Operating temperature range: -40 to $+85^\circ\text{C}$
- Data retention supply voltage: 2.0 to 5.5 V
- All I/O levels
 - 5-V operation: TTL compatible
 - 3-V operation: $V_{CC} - 0.2$ V/0.2 V
- Shared I/O pins and 3-state outputs
- No clock signal required.
- Packages
 - 28-pin DIP (600 mil) plastic package: LC35256D
 - 28-pin SOP (450 mil) plastic package: LC35256DM
 - 28-pin TSOP (8 \times 13.4 mm) plastic package: LC35256DT

Package Dimensions

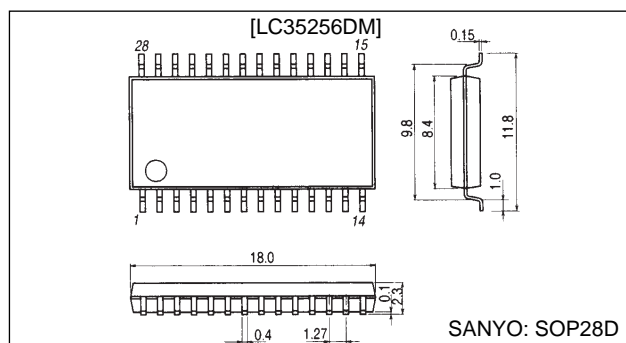
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3012A-DIP28



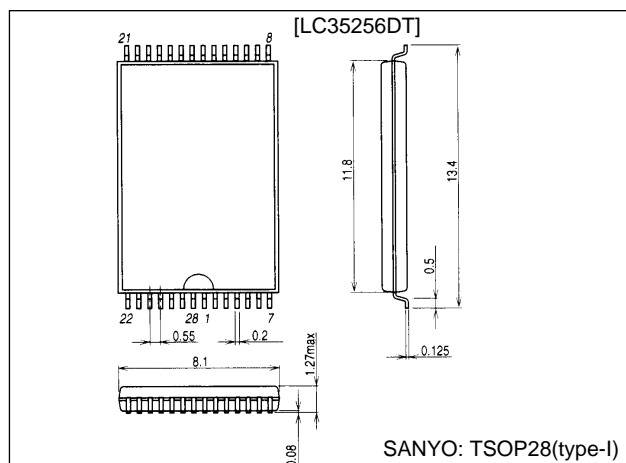
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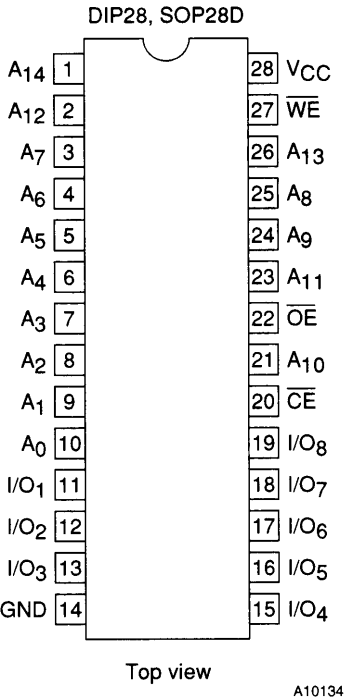
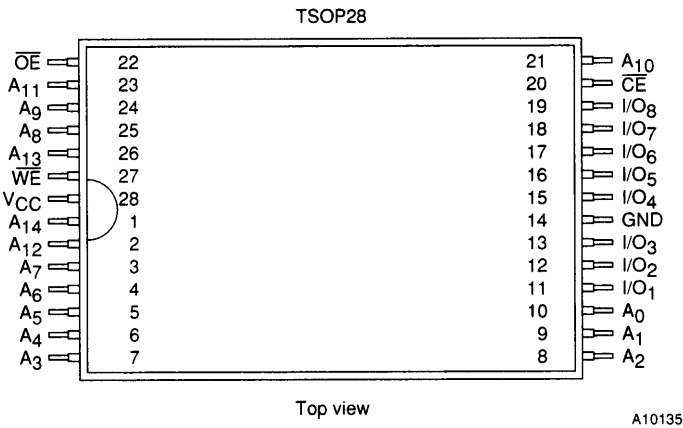
3221-TSOP28(type-I)



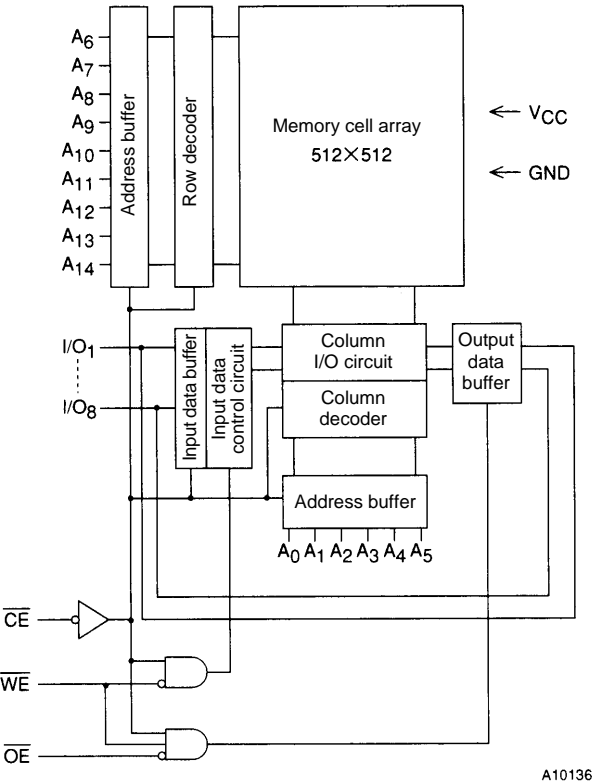
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Pin Assignment



Block Diagram



Pin Functions

A0 to A14	Address inputs
$\overline{\text{WE}}$	Read/write control input
$\overline{\text{OE}}$	Output enable input
$\overline{\text{CE}}$	Chip enable input
I/O1 to I/O8	Data I/O
VCC, GND	Power supply, ground

Function Table

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O	Supply current
Read cycle	L	L	H	Data output	I_{CCA}
Write cycle	L	X	L	Data input	I_{CCA}
Output disable	L	H	H	High-impedance	I_{CCA}
Unselected	H	X	X	High-impedance	I_{CCS}

X : H or L

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Input pin voltage	V_{IN}		-0.3* to $V_{CC} + 0.3$	V
I/O pin voltage	$V_{I/O}$		-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}		-40 to +85	°C
Storage temperature	T_{stg}		-55 to +125	°C

Note *: -3.0 V for pulse widths of up to 30 ns.

I/O Capacitances at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
I/O pin capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$		6	10	pF
Input pin capacitance	C_{IN}	$V_{IN} = 0\text{ V}$		6	10	pF

Note: These parameters are not measured in all units, but rather are only measured in sampled units.

[5-V Operation]

DC Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		4.5	5.0	5.5	V
Input voltages	V_{IH}		2.2		$V_{CC} + 0.3$	V
	V_{IL}		-0.3*		+0.8	V

Note *: -3.0 V for pulse widths of up to 30 ns.

DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V

Parameter		Symbol	Conditions			Ratings			Unit
						min	typ*	max	
Input leakage current		I _{LI}	V _{IN} = 0 to V _{CC}			-1.0		+1.0	μA
Output leakage current		I _{LO}	V _{CE} = V _{IH} or V _{OE} = V _{IH} or V _{WE} = V _{IL} , V _{I/O} = 0 to V _{CC}			-1.0		+1.0	μA
High-level output voltage		V _{OH}	I _{OH} = -1.0 mA			2.4			V
Low-level output voltage		V _{OL}	I _{OL} = 2.0 mA					0.4	V
Operating current drain	TTL inputs	I _{CCA2}	V _{CE} = V _{IL} , I _{I/O} = 0 mA, V _{IN} = V _{IH} or V _{IL}					5.0	mA
		I _{CCA3}	V _{CE} = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0 mA, Duty 100%	min cycle	LC35256DM, DT-70	35	40	mA	
					LC35256D, DM, DT-10	25	30	mA	
			1 μs cycle			3.5	6.0	mA	
Standby mode current drain	V _{CC} - 0.2 V/ 0.2 V inputs	I _{CCS1}	V _{CE} ≥ V _{CC} - 0.2 V, V _{IN} = 0 to V _{CC}		Ta ≤ 25°C			μA	
					Ta ≤ 60°C		1.0	μA	
					Ta ≤ 85°C		5.0	μA	
		TTL inputs	I _{CCS2}	V _{CE} = V _{IH} , V _{IN} = 0 to V _{CC}				1.0	mA

Note *: Reference value at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$.

LC35256D-10, LC35256DM, DT-70/10

AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V

AC test conditions		
Input pulse voltage level	$V_{IH} = 2.4$ V, $V_{IL} = 0.6$ V	
Input rise and fall times	5 ns	
Input and output timing level	1.5 V	
Output load	LC35256DM, DT-70	One TTL gate + 30 pF (Including jig capacitances.)
	LC35256D, DM, DT-10	One TTL gate + 100 pF (Including jig capacitances.)

Read Cycle

Parameter	Symbol	LC35256D, DM, DT				Unit
		-70*		-10		
		min	max	min	max	
Read cycle time	t _{RC}	70		100		ns
Address access time	t _{AA}		70		100	ns
\overline{CE} access time	t _{CA}		70		100	ns
\overline{OE} access time	t _{OA}		35		50	ns
Output hold time	t _{OH}	10		10		ns
\overline{CE} output enable time	t _{COE}	10		10		ns
\overline{OE} output enable time	t _{OOE}	5		5		ns
\overline{CE} output disable time	t _{COD}		30		30	ns
\overline{OE} output disable time	t _{OOD}		25		25	ns

Note *: Specification values for the LC35256DM and LC35256DT.

Write Cycle

Parameter	Symbol	LC35256D, DM, DT				Unit
		-70*		-10		
		min	max	min	max	
Write cycle time	t _{WC}	70		100		ns
Address setup time	t _{AS}	0		0		ns
Write pulse width	t _{WP}	55		60		ns
\overline{CE} setup time	t _{CW}	60		70		ns
Write recovery time	t _{WR}	0		0		ns
\overline{CE} write recovery time	t _{WR1}	0		0		ns
Data setup time	t _{DS}	35		40		ns
Data hold time	t _{DH}	0		0		ns
\overline{CE} data hold time	t _{DH1}	0		0		ns
\overline{WE} output enable time	t _{WOE}	5		5		ns
\overline{WE} output disable time	t _{WOD}		30		30	ns

Note *: Specification values for the LC35256DM and LC35256DT.

[3-V Operation]

DC Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		2.7	3.0	3.6	V
Input voltages	V_{IH}		$V_{CC} - 0.2$		$V_{CC} + 0.3$	V
	V_{IL}		-0.3*		+0.2	V

Note *: -2.0 V for pulse widths of up to 30 ns.

LC35256D-10, LC35256DM, DT-70/10

DC Electrical Characteristics at Ta = -40 to +85°C, VCC = 2.7 to 3.6 V

Parameter		Symbol	Conditions		Ratings			Unit
					min	typ*	max	
Input leakage current		ILI	VIN = 0 to VCC		-1.0		+1.0	μA
Output leakage current		ILO	VCE = VIH or VOE = VIH or VWE = VIL, VI/O = 0 to VCC		-1.0		+1.0	μA
High-level output voltage		VOH	IOH = -0.5 mA		VCC - 0.2			V
Low-level output voltage		VOL	IOL = 1.0 mA				0.2	V
Operating current drain	VCC - 0.2 V/ 0.2 V inputs	ICCA4	VCE = VIL, VIN = VIH or VIL, II/O = 0 mA, Duty 100%	min	LC35256DM, DT-70	7	10	mA
				cycle	LC35256D, DM, DT-10	3	5	mA
				1 μs cycle		1.5	2.5	mA
Standby mode current drain	VCC - 0.2 V/ 0.2 V inputs	ICCS1	VCE ≥ VCC - 0.2 V, VIN = 0 to VCC	Ta ≤ 25°C		0.01		μA
				Ta ≤ 60°C			0.8	μA
				Ta ≤ 85°C			4.0	μA

Note *: Reference value at Ta = 25°C, VCC = 3 V.

AC Electrical Characteristics at Ta = -40 to +85°C, VCC = 2.7 to 3.6 V

AC test conditions		
Input pulse voltage level		VIH = VCC - 0.2 V, VIL = 0.2 V
Input rise and fall times		10 ns
Input and output timing level		1.5 V
Output load	LC35256DM, DT-70	30 pF (Including jig capacitances.)
	LC35256D, DM, DT-10	100 pF (Including jig capacitances.)

Read Cycle

Parameter	Symbol	LC35256D, DM, DT				Unit
		-70*		-10		
		min	max	min	max	
Read cycle time	t _{RC}	200		500		ns
Address access time	t _{AA}		200		500	ns
$\overline{\text{CE}}$ access time	t _{CA}		200		500	ns
$\overline{\text{OE}}$ access time	t _{OA}		100		250	ns
Output hold time	t _{OH}	20		20		ns
$\overline{\text{CE}}$ output enable time	t _{COE}	20		20		ns
$\overline{\text{OE}}$ output enable time	t _{OOE}	10		10		ns
$\overline{\text{CE}}$ output disable time	t _{COD}		60		120	ns
$\overline{\text{OE}}$ output disable time	t _{OOD}		50		100	ns

Note *: Specification values for the LC35256DM and LC35256DT.

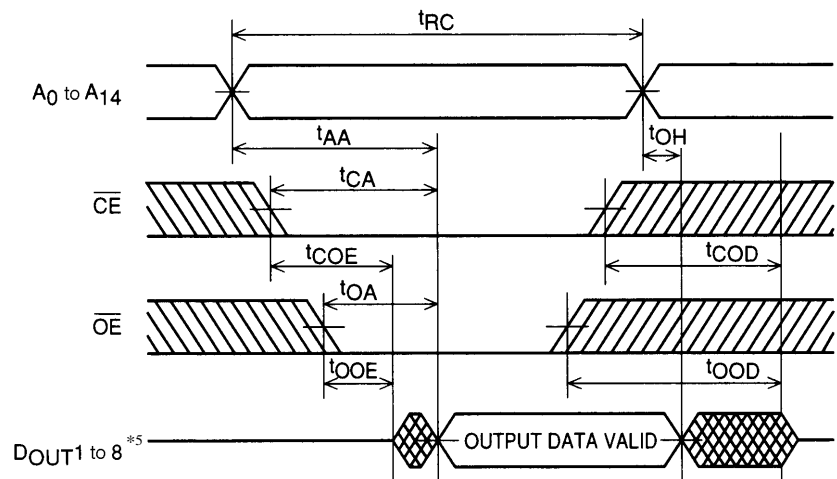
Write Cycle

Parameter	Symbol	LC35256D, DM, DT				Unit
		-70*		-10		
		min	max	min	max	
Write cycle time	t _{WC}	200		500		ns
Address setup time	t _{AS}	0		0		ns
Write pulse width	t _{WP}	140		200		ns
\overline{CE} setup time	t _{CW}	150		250		ns
Write recovery time	t _{WR}	0		0		ns
\overline{CE} write recovery time	t _{WR1}	0		0		ns
Data setup time	t _{DS}	130		180		ns
Data hold time	t _{DH}	0		0		ns
\overline{CE} data hold time	t _{DH1}	0		0		ns
WE output enable time	t _{WOE}	10		10		ns
WE output disable time	t _{WOD}		60		120	ns

Note *: Specification values for the LC35256DM and LC35256DT.

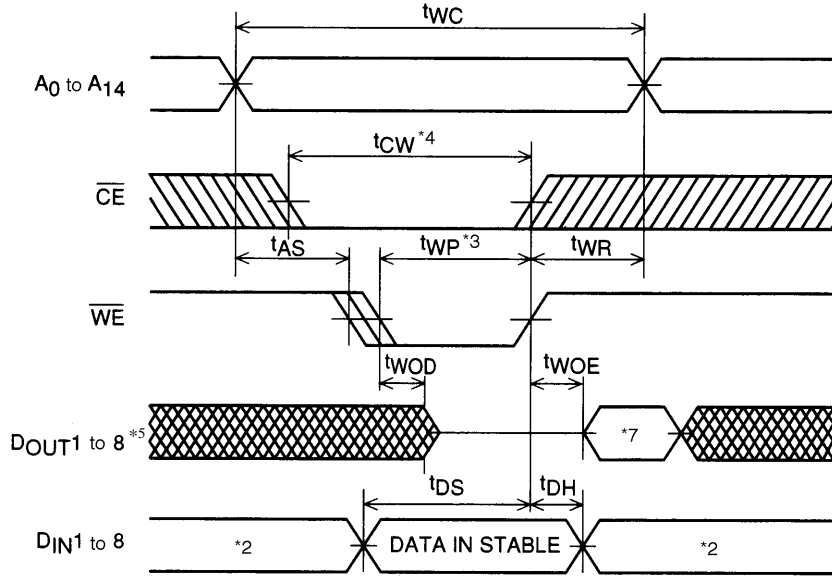
Timing Charts

Read Cycle *1



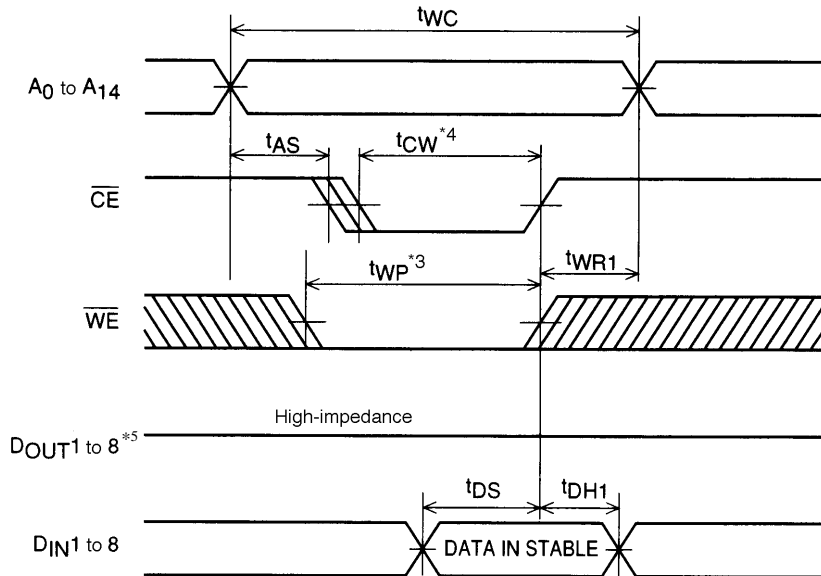
A10137

Write Cycle 1 (WE write) *6



A10138

Write Cycle 2 (CE write) *6



A10139

Notes: 1. Applications must set \overline{WE} high during the read cycle.

2. External circuits in the application must not apply reverse phase signals to the D_{OUT} pins when those pins are in the output state.

3. The time t_{WP} is the period when \overline{CE} and \overline{WE} are both low. It is defined as the time from the fall of \overline{WE} to the rise of \overline{CE} or the rise of \overline{WE} , whichever occurs first.

4. The time t_{CW} is the period when \overline{CE} and \overline{WE} are both low. It is defined as the time from the fall of \overline{CE} to the rise of \overline{CE} or the rise of \overline{WE} , whichever occurs first.

5. The data outputs (D_{OUT}) go to the high-impedance state if any one of the following conditions hold: \overline{OE} is high, \overline{CE} is high, or \overline{WE} is low.

6. \overline{OE} must be held either high or low during the write cycle.

7. The D_{OUT} pins have the same phase as the write cycle write data.

Notes on Circuit Design

Take the following operations into account when designing circuits that use these products to assure that none of the items in the maximum ratings are exceeded.

- Supply voltage variations and fluctuations
- Manufacturing variations in the electrical characteristics of the electrical components, including semiconductor devices, resistors, and capacitors.
- Ambient temperature
- Variations and fluctuations in the input and clock signals
- Possible application of abnormal pulses

Parameters listed in the allowable operating ranges must never exceed their stipulated ranges.

If input pins to a CMOS IC are left open, through currents may occur in internal circuits to which intermediate potentials are input and result in incorrect circuit operation. Always verify that any unused pins are set up in appropriate states.

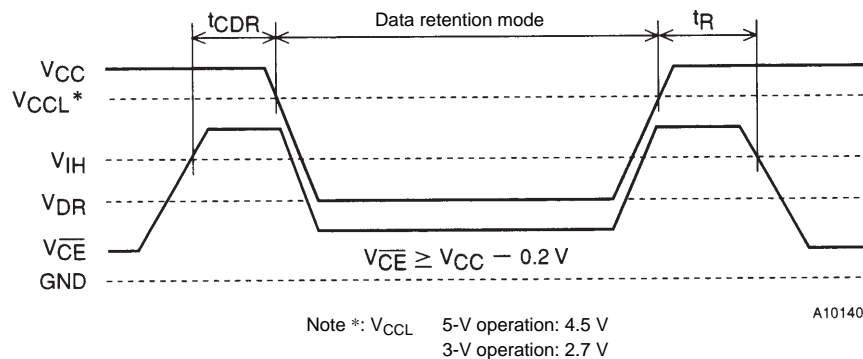
Data Retention Characteristics at $T_a = -40$ to $+85^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ*1	max	
Data retention supply voltage	V_{DR}	$V_{CE} \geq V_{CC} - 0.2\text{ V}$	2.0		5.5	V
Data retention current drain	I_{CCDR}	$V_{CC} = 3.0\text{ V}$, $V_{CE} \geq V_{CC} - 0.2\text{ V}$		0.01		μA
					0.7	μA
					3.5	μA
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		t_{RC}^{*2}			ns

Notes: 1. Reference value at $T_a = 25^\circ\text{C}$, $V_{CC} = 3\text{ V}$.

2. t_{RC} : Read cycle time

Data Retention Waveforms



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